Compact modeling of gate-all-around silicon nanowire MOSFETs

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Compact Modeling of Gate-All-Around Silicon Nanowire MOSFETs

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Summary

This thesis documents the compact model development for the silicon nanowire MOSFET. A surface-potential based scalable model is developed for silicon nanowire MOSFET. An accurate surface potential initial guess is derived for the iterative surface potential solution within a few iteration steps. An analytical single-piece expression of the surface potential solution is derived in all regions of operation. An intrinsic long channel transistor drain current model is developed as the core model without charge-sheet approximation. To extend the core model into short channel devices, many physical phenomena including mobility degradation, channel length modulation, velocity saturation, and drain induced barrier lowering are incorporated into the core model. Some threshold voltage definitions are discussed and a new threshold voltage expression is proposed for silicon nanowire MOSFETs. The threshold voltage roll-off, subthreshold slope degradation, and drain induced barrier lowering effects are modeled with an approximate solution of the 2D Poisson's equation. A simple, accurate, and continuous charge and capacitance model is developed based on the single-piece drain current model. The terminal charges are calculated using Ward-Button partition and the capacitances are obtained by the derivative of the terminal charges with respect to terminal voltages. The channel thermal noise model is developed, in which the thermal noise is obtained by integrating the output conductance along the channel. A novel flicker noise model that includes both mobility fluctuation and carrier fluctuation is developed. An analytical single-piece drain current mismatch model is developed to model the random fluctuation in the device parameters.

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List of symbols

Symbol	REMARK
V_{gs}	Gate to source voltage
V_{ds}	Drain to source voltage
V_{dseff}	Effective drain to source voltage
V_{gseff}	Effective gate to source voltage
V_{gb}, V_{GF}	Flat-band shifted gate voltage
V_{dsat}	Saturation drain to source voltage
V_T	Threshold voltage
V_C	Channel to source voltage
n_i	Intrinsic carrier concentration
v_{th}	Thermal voltage
t_{ox}	Gate oxide thickness
ϵ_{ox}	Permittivity of oxide
ϵ_{si}	Permittivity of silicon
ϕ_{ms}	work function difference
ϕ_m	Work function for poly gate
V_{FB}	Flat-band voltage
N_a	Acceptor
N_d	Donor
N	Number of carriers
R	Silicon nanowire radius
L_{eff}	Effective channel length
L_g	Drawn gate length
X_j	Lightly-doped drain junction depth
ϕ	Electric potential
$\phi(r,y)$	Position dependent electric potential
$\phi_s, \phi(y)$	Position dependent surface potential
ϕ_{sL}	Channel surface potential at drain end
ϕ_{s0}	Channel surface potential at source end
ϕ_F	Silicon intrinsic Fermi potential
ϕ_{Fn}	Silicon electron quasi Fermi potential
ϕ_{Fp}	Silicon hole quasi Fermi potential
ϕ_s	Surface potential
$\bar{\phi}$	Surface potential average
$\Delta\phi$	Surface potential difference
Q_g	Unified gate charge per unit area

Q_d	Unified drain charge per unit area
Q_s	Unified source charge per unit area
Q_i	Inversion charge per unit area
Q_{sc}	Channel induce charge per unit area
Q_{it}	Charge density of interface states
C_{ox}	Gate oxide capacitance
C_{gg}	Gate capacitance
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
C_{sg}	Source-gate capacitance
C_{sd}	Source-drain capacitance
C_{ds}	Drain-source capacitance
C_{dg}	Drain-gate capacitance
C_{ij}	i-j Capacitance, both i and j can be any of the drain, gate, source
C_{inv}	Inversion layer capacitance
I_{ds}	Drain current
μ_0	Mobility degradation with transverse-field effect
μ_{eff0}	Mobility degradation with lateral/transverse-field effect
μ_{eff}	Effective mobility degradation
E_{eff}	Effective transverse-field
E_{sat}	Saturation field
E_{satn}	Effective saturation field
v_0	Velocity field relation
v_{sat}	Saturation velocity
v_h	Velocity overshoot
$E_{ }$	Lateral-field
δ_0	Length-dependent lateral-field factor
g_m	Transconductance
g_{ds}	Output drain conductance
μ_{co}	Mobility parameter for Coulombic scattering
μ_{sr}	Mobility parameter for surface roughness scattering
μ_{ph}	Mobility parameter for phonon scattering
R_s	Series source resistance
R_d	Series drain resistance
R_{ch}	Intrinsic channel resistance
S_V	Voltage spectra density
S_I	Current spectra density
c_n	Electron capture coefficient
c_p	Hole capture coefficient
e_n	Electron emission coefficient
e_p	Hole emission coefficient
N_{it}	Interface trap density
τ	Time constant in generation-recombination process
σ	Standard deviation

CHAPTER 1: INTRODUCTION

As conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are scaled to the nanoscale regime, gate oxide tunneling and other short channel effects impose a physical limit on their ultimate performance. In recent years, a number of non-classical MOSFET structures are proposed to extend the scalability of MOSFET technology beyond the 45-nm technology node. Multiple-gate MOSFETs such as double-gate (DG), triple-gate and surrounding-gate (SG) or Gate-All-Around (GAA) MOSFETs are becoming intense research topics because of their better gate control ability and potential in scalability. Among these advanced MOSFET structures, theoretically, GAA MOSFETs provides the best gate electrostatic control capability. Therefore, GAA silicon-nanowire (SiNW) MOSFET is one of the most promising structures beyond bulk CMOS [1-3].

1.1. Motivation

Compact model is the link between the fab and the design community as well as the brain of circuit simulators [4]. The key for circuit simulators to predict real circuit performance depends mostly on the accurate modeling of the real electrical characteristics through mathematical equations coded in the simulators. A tractable and complete compact model of SiNW MOSFETs taking into consideration short channel effects is not available for circuit simulator at present. Based on various modeling methodologies, compact models are grouped into threshold-voltage based, surface-potential based, and charge-based approach[5]. A few charge-based compact models for undoped GAA MOSFETs have been reported, some with approximations to obtain explicit expression of the inversion charge [6-12]. However, charge-based models rely more on mathematical smoothing functions and less on physics-based approximations in the volume inversion region. And it has been recognized that surface-potential-based models are inherently single-piece and describe device operations in all regions accurately.

The motivation of this research is to understand the physics underlying GAA SiNW MOSFETs and develop a surface-potential-based compact model which can simulate and predict the SiNW MOSFET behaviors.

1.2. Objectives

The objectives of this research are to:

- i. Develop and improve on the surface-potential based direct current undoped SiNW MOSFET compact model that it is simple, scalable and accurate.
- ii. Develop and improve on the undoped SiNW MOSFET charge and capacitance model.
- iii. Develop the channel thermal noise and flicker noise undoped SiNW MOSFET model.
- iv. Develop the mismatch model so that it can predict the influence in drain current due to process variations.

1.3. Major Contributions of the Thesis

The major contributions of the thesis are listed below:

- i. Proposed a new iterative surface potential solution with an accurate initial guess, the iterative surface potential solution can be obtained in a few iterations and it is appropriate to be employed in compact modeling. A new analytical approximate surface potential solution for all regions of operation is also proposed.
- ii. Proposed a new analytical single-piece drain current model, which is valid in all regions without charge sheet approximation. The model can capture and predict the drain current behaviors in SiNW MOSFETs.

- iii. Proposed new formulations of short channel effects with approximate solution of 2D Poisson's equation. The 2D Poisson's solution is obtained with the superposition method. With the new formulation, the model can capture the threshold voltage shift in short channel devices as well as other major short channel effects.
- iv. Developed a new capacitance voltage (C-V) model to calculate the stored terminal charge and capacitances. It is a simple, accurate, non-negative, continuous, symmetric, and satisfying charge conversation.
- v. Developed a channel thermal noise model that is based on the core I-V drain current model.
- vi. Proposed a new flicker noise model that includes both mobility and number fluctuations. A novel equation of the generation-recombination noise considering the dependence of interface trap density on surface potential is derived.
- vii. Proposed a new drain current mismatch model based on the single piece drain current model. The analytical model can capture the drain current mismatch performance in all regions of operation. It is now possible to simulate the drain current mismatch in all regions without Monte Carlo simulation.

1.4. Organization of the Thesis

The following chapters provide extensive and detailed information about the proposal physical compact model of SiNW MOSFETs.

Chapter 2 presents the core I-V model developed for intrinsic long channel devices with constant mobility. It begins with the solution of Poisson's equation, and then, presents the iterative surface potential solution, which can be obtained within a few iterations using an accurate initial guess. An analytical surface potential is also presented, which is accurate enough in compact modeling. Lastly, the single-piece drain current model valid in all operation regions is presented. It is noted worthy that the drain current equation is derived without using charge sheet approximation.

Chapter 3 discusses the impact of mobility degradation and short channel effects in drain current. Low field mobility and high field mobility are first discussed, and followed by the velocity saturation and channel length modulation. This chapter also presents a novel threshold voltage equation of undoped GAA SiNW MOSFETs. And then, the drain induced barrier lowering and threshold voltage roll-off effects are discussed. Finally, the model has been verified with TCAD numerical simulations.

Chapter 4 presents a simple and accurate C-V model. The long channel C-V model is first described. For the purpose of being feasible in compact modeling, it is

developed using an approximate drain current equation to avoid the complexity. And then, it is extended to short channel device by including short channel effects.

Chapter 5 discusses the noise model in SiNW MOSFETs. This includes the thermal noise model and flicker noise model. The flicker noise model includes both mobility fluctuation and number fluctuation.

Chapter 6 explores to the mismatch in drain current. The mismatch sources in undoped SiNW MOSFETs are first discussed. And then, the impact of mismatches in SiNW radius, flat-band shifted gate voltage, and mobility on the drain current are discussed.

Finally, Chapter 7 concludes with a summary and suggestions for future work.

CHAPTER 2: INTRINSIC LONG CHANNEL DRAIN CURRENT MODEL OF UNDOPED SILICON NANOWIRE MOSFETs

The gate-all-around, or surrounding-gate, MOSFET is one of the most promising structures beyond bulk CMOS. Since early investigations on GAA/SOI devices, most recent experiments have demonstrated GAA silicon-nanowire structures with controlled diameters on the order of 3~6 nm using conventional CMOS technology [13-17]. Theoretically, GAA MOSFETs provide better gate electrostatic control capabilities than planar and double-gate counterparts. To develop a compact model for circuit simulation of these future-generation devices, these devices are best described theoretically under the cylindrical coordinate [18]. It has been recognized that surface-potential-based models are inherently single-piece and describe device operations in all regions accurately. This chapter will discuss the surface potential solution and the development of a core I-V model for undoped GAA SiNW MOSFETs without the charge-sheet approximation [19].

2.1. Introduction

To design and simulate the silicon integrated circuits, in a circuit simulator, the compact models are used to compute the MOSFETs' characteristics. To derive simple, fast and accurate analytical representations of the terminal electrical characteristics of a MOSFET is the purpose of compact modeling. The MOSFET is inherently a two-dimensional (2D) electronic device. In a MOSFET, the gate electrode creates an electric field in the x-direction perpendicular to the silicon layer to modulate the sheet conductance with input voltage applied. And the applied voltage between source and drain electrodes will cause the current passing through the silicon layer along the y-direction. The current is modulated by gate voltage. In almost all compact modeling, this 2D problem is decomposed into two coupled one-dimension (1D) problems [20].

Along x-direction, the 1D solution is known as the input voltage equation, which relates the gate voltage (V_g) with the surface potential (ϕ_s). This input voltage equation is usually obtained by solving 1D Poisson's equation and combining with the Gauss' law. In compact modeling, we need to develop an algorithm to invert the implicit dependence $V_g(\phi_s)$ to an explicit dependence $\phi_s(V_g)$. The 1D y-direction solution is known as the output current equation, which relates the output current to the surface potential, with input terminal voltages as parameters: $I_{ds}(V_d, V_s, \phi_s)$. The surface potential couples the current and voltage equations.

Based on Poisson's equation and charge balance equation, the solution of

MOSFET model was derived by Pao and Sah [9]. This double integral solution relates the input voltage and the channel surface potential. Based on the Sah's solution, three different approaches to compact the double integral solution have been developed over the years, namely, the threshold-voltage (V_t) based, charge (Q) based, and surface-potential (ϕ) based models.

Moreover, the compact model is the most important component in circuit simulations. It is developed based on device physics to provide a concise mathematical model of the device electrical behavior to aid the circuit design. In a circuit simulator, there are four kind of analyses: direct-current (DC), alternating-current (AC), transient and noise analyses, to support all these analyses, a compact model needs to model the currents through all terminals, the charges stored at each terminal, and the noise associated with each terminal. In other words, a complete compact model involves current-voltage (I-V) model, capacitance-voltage (C-V) model and noise model. Usually, the I-V model is always being developed first and then, the C-V model and noise model based on the I-V model. The I-V model describes the transistor terminal current behavior under different terminal bias conditions. For a compact I-V model, the two most important requirements are accuracy and efficiency. It has to describe and predict the device electrical behaviors precisely without compromising the computational speed.

Depending on the intermediate variable used to derive the current and charge model, compact models are classified into three categories, namely, threshold voltage based, surface potential based, and inversion charge based.

The first generation compact models were threshold voltage based models and had been widely accepted due to simplicity of equations. In traditional threshold voltage modeling, for gate voltages below the threshold voltage a linear approximation between the surface potential and the gate voltage was made, which relates the gate voltage to the drain current. The surface potential is assumed constant with gate voltages above the threshold voltage (surface potential pinned to twice of the Fermi potential, $2\phi_F$) [21]. Conventional threshold voltage based models use some smoothing functions to join subthreshold region and strong inversion region together, and apply regional approximations in each region [22, 23]. Nevertheless, this kind of models suffers from the symmetry problems, discontinuity and accuracy errors at moderate inversion, the region between subthreshold and strong inversion region).

In charge based models, the node charges are the intermediate variables [24]. The voltage equation is transformed into an equation of node charge versus node voltage. Similarly, the current equation is also transformed into a current versus node charge equation. This is the approach used in inversion charge models in both strong inversion and weak inversion regions. It is claimed that charge based model is more accurate and faster than threshold voltage based model and surface potential based model [12, 25, 26]. The charge based model, in principle, does not have the symmetry problem. Nevertheless, charge based models still use empirical descriptions in the moderate inversion region. Since charges cannot be measured with available instruments, it still needs to be calibrated by measurements of current-voltage characteristics.

The third approach in compact modeling is surface potential based modeling. The surface potential based model is inherently single-piece and gives a physics-based and accurate description in all operation regions[27, 28]. It solves the surface potential at the two ends of the channel through 1D Poisson solution, and then, the terminal charges and currents are formulated based on the solution of the surface potential. Surface potential solutions in a MOSFET have been established almost 40 years ago from Pao-Sah equation [20, 29]. The solution of the surface potential can either be obtained iteratively or non-iteratively. The surface potential based model is becoming more popular due to its strong physical contents.

Our model is a surface potential based model in which all electrical variables, such as terminal currents and terminal charges, are presented as functions of the surface potentials at drain and source ends. An accurate surface potential is the core of the model and the calculation of the surface potential is the foremost step in the model development. The surface potential solution is obtained by solving the Poisson's equation together with Gauss's law. Section 2.2 describes the solution of the Poisson's equation. In Section 2.3, we present a novel iterative surface potential solution for undoped GAA SiNW MOSFETs. With good initial guesses for the iteration, the accurate surface potential solution can be obtained within a few steps (less than 5). Therefore, the iterative surface potential solution is suitable in compact modeling. For the case in which CPU time is considered more important than accuracy, we also derive and present an analytical expression of the surface potential solution in Section 2.4.

Usually, the I-V model is developed using a bottom-up approach. Firstly, the intrinsic long channel transistor I-V model is developed and referred to as the core model. And then, other physical phenomena involving mobility degradation, channel length modulation, velocity saturation, and drain induced barrier lowering are incorporated into the core model to enable the modeling of short channel devices. In this chapter, the derivation of core model equations is described. For conventional MOSFETs, the drain current is usually modeled with the charge sheet approximation (CSA), which assumes the inversion charge is equal to the total charge minus the depletion charge. It is valid in conventional MOSFETs due to most current flowing through the surface of the channel [30]. But in undoped SiNW MOSFETs, the current is under a “body conducting” mode, in which the current flowing through the silicon body is not neglectable; therefore, the drain current has to be modeled without employing CSA[31, 32].

To validate a model, experimental measurement data or simulations from TCAD simulators [33, 34], which solve the 2D Poisson’s equation and transport equation with numerical techniques, are required to be taken as a “golden” reference. In this chapter, numerical simulations using TCAD (Medici) are used to validate the drain current model and surface potential solution.

2.2. Solution of Poisson Equation

Figure 2.1: Cross Section of a Surrounding-Gate Silicon Nanowire MOSFET

The cross-section of a surrounding-gate SiNW MOSFET is shown in Figure 2.1. The cylindrical undoped silicon body is surrounded by the silicon dioxide and the gate. This device structure provides better gate control capability than the planar conventional MOSFET structure. The electrostatic potential ϕ in surrounding-gate SiNW obeys Poisson equation:

$$\nabla^2 \phi = -\frac{q}{\epsilon_{Si}} \left(-N_a + N_a e^{-q(\phi-V)/kT} - \frac{n_i^2}{N_a} e^{q(\phi-V)/kT} \right) \quad (2.1)$$

where q is the electron charge, N_a is the net acceptor doping concentration, n_i is the intrinsic carrier concentration, ϵ_{Si} is permittivity of silicon, $V = \phi_{Fn} - \phi_{Fp}$ is defined as the imref split, with the assumption $\phi_{Fp} = \phi_F = 0$, where $V = 0$ and $V = V_{ds}$ at the source and drain ends, respectively.

Instead of solving the Poisson's equation directly, which is possible only with numerical techniques, we introduce the gradual channel approximation (GCA) [35], which assumes the longitudinal field is much smaller than the transverse field. The GCA

is valid in a long channel device due to the longitudinal electric field being negligible. In undoped SiNW MOSFETs, with the GCA and considering only the mobile electrons, the Poisson equation becomes [27]:

$$\frac{d^2\phi}{dr^2} + \frac{1}{r} \frac{d\phi}{dr} = \frac{qn_i}{\epsilon_{Si}} e^{(\phi-V)/v_{th}} \quad (2.2)$$

where v_{th} is the thermal voltage.

Because of the symmetry of SG SiNW MOSFET structure, the electric field has to be zero at the centre. And surface potential is defined as the potential at the interface between silicon and silicon dioxide. Therefore, the symmetric boundary conditions are as follows:

$$\left. \frac{d\phi}{dr} \right|_{r=0} = 0 \quad (2.3a)$$

$$\phi|_{r=R} = \phi_s \quad (2.3b)$$

where R is the radius of the silicon body.

We apply variable transformation technique to solve the Equation (2.2). A new variable z is defined as $z = \phi/v_{th}$ with which Equation (2.2) is rewritten as (assuming V is equal to 0 for simplicity):

$$\frac{d^2z}{dr^2} + \frac{1}{r} \frac{dz}{dr} = \delta e^z \quad (2.4)$$

$$\text{where } \delta = \frac{q^2 n_i^2}{\epsilon_{Si} kT}$$

Further, two transformation variables are defined as:

$$\eta = r^2 e^z, \quad (2.5a)$$

$$\beta = r \frac{dz}{dr}. \quad (2.5b)$$

Thus, Equation (2.4) is rewritten as:

$$\frac{d\beta}{d\eta} = \frac{\delta}{\beta + 2}, \quad (2.6)$$

Integrating Equation (2.6),

$$\beta^2 + 4\beta + h = 2\delta\eta. \quad (2.7)$$

According to the symmetric boundary conditions (2.3a) and (2.3b), the constant h is equal to zero. Substituting Equations (2.5a) and (2.5b) into Equation (2.7), yields:

$$\frac{1}{2} \left(\frac{dz}{dr} \right)^2 + \frac{2}{r} \frac{dz}{dr} = \delta e^z. \quad (2.8)$$

Combining with Equation (2.4):

$$\frac{d^2 z}{dr^2} - \frac{1}{r} \frac{dz}{dr} - \frac{1}{2} \left(\frac{dz}{dr} \right)^2 = 0. \quad (2.9)$$

The solution of the above differential equation is well known as [18]:

$$z = A - 2 \ln(Br^2 + 1). \quad (2.10)$$

Equation (2.10) is rewritten as:

$$\phi = v_{th} \cdot (A - 2 \ln(Br^2 + 1)) \quad (2.11)$$

where A and B are related by:

$$A = \ln(-8B/\delta) \quad (2.12)$$

and the boundary condition (2.3b) yields:

$$\phi_s = v_{th} \cdot \ln \left(-\frac{8B}{\delta(BR^2 + 1)^2} \right). \quad (2.13)$$

Extend to the case when channel voltage V is not equal to zero:

$$\phi = V + v_{th} \cdot \ln \left(-\frac{8B}{\delta(Br^2 + 1)^2} \right) \quad (2.14)$$

and

$$\phi_s = V + v_{th} \cdot \ln \left(-\frac{8B}{\delta(BR^2 + 1)^2} \right). \quad (2.15)$$

This is the relationship between the surface potential and B . Closed-form solution is obtained by solving Equation (2.15) analytically:

$$B = -\frac{\delta R^2 e^{(\phi_s - V)/v_{th}} + 4 - 2\sqrt{4 + 2\delta R^2 e^{(\phi_s - V)/v_{th}}}}{\delta R^4 e^{(\phi_s - V)/v_{th}}}. \quad (2.16)$$

2.3. Iterative Surface Potential Solution of Surrounding Gate Silicon Nanowire MOSFET

Equation (2.15) shows the relationship between the surface potential and variable B . With Equations (2.14) and (2.15), we recognize that if the surface potential is obtained, then we can calculate B from Equation (2.16) and evaluate the potential from Equation (2.14) at any position r . To obtain the surface potential solution, at a given terminal bias we solve Poisson's equation together with Gauss's law.

The electric field along the radius direction is obtained by taking the derivative of the potential,

$$\frac{d\phi}{dr} = -\frac{4v_{th}Br}{1+Br^2} \quad (2.17)$$

Applying the Gauss' law to the surface of SiNW, we obtain:

$$C_{ox}(V_{gf} - \phi_s) = -Q_{sc} = \epsilon_{Si} \left. \frac{d\phi}{dr} \right|_{r=R} \quad (2.18)$$

where C_{ox} is the cylindrical capacitor of the gate oxide, $V_{gf} = V_{gs} - V_{FB}$ is the flat-band shifted gate voltage where V_{FB} is the flat-band voltage. The total induced charge Q_{sc} is given by [27]

$$Q_{sc} = \frac{4\epsilon_{Si}v_{th}}{R} \left(\frac{\delta R^2 e^{(\phi_s - V)/v_{th}}}{4 - 2\sqrt{4 + 2\delta R^2 e^{(\phi_s - V)/v_{th}}}} + 1 \right). \quad (2.19)$$

Substituting Equations (2.18) into (2.19), the implicit equation for the surface potential of SiNW is obtained:

$$V_{gf} = \phi_s - C_R \left(\frac{\delta R^2 e^{(\phi_s - V)/v_{th}}}{4 - 2\sqrt{4 + 2\delta R^2 e^{(\phi_s - V)/v_{th}}}} + 1 \right) \quad (2.20)$$

where $C_R = \frac{4\epsilon_{si}v_{th}}{RC_{ox}}$.

Equation (2.20) relates the surface potential to the gate terminal voltage. With any gate voltage, surface potential can be obtained by solving Equation (2.20), and it is valid for all regions including volume inversion and strong inversion. Accurate ϕ_s solutions can be obtained from the above implicit equation with Newton-Raphson (NR) iteration method. An accurate initial guess is important for NR method to aid the convergence and improve computational efficiency. In this model, the initial guess is derived with the regional approach. In volume inversion, the slope of the surface potential is approximately equal to one, the regional surface potential (initial guess) is therefore given by $\phi_s = V_{gf}$. In the mean time, from Equation (2.20), we have

$$\frac{\delta R^2 e^{(\phi_s - V)/v_{th}}}{4 - 2\sqrt{4 + 2\delta R^2 e^{(\phi_s - V)/v_{th}}}} \approx -1 \quad (2.21)$$

In strong inversion region, the second term of Equation (2.20) can be approximated as

$$\frac{\delta R^2 e^{(\phi_s - V)/v_{th}}}{4 - 2\sqrt{4 + 2\delta R^2 e^{(\phi_s - V)/v_{th}}}} \approx -\sqrt{\frac{1}{2}\delta R^2 e^{(\phi_s - V)/v_{th}}} \quad (2.22)$$

therefore,

$$V_{gf} = \phi_s - C_R \left(-\sqrt{\frac{1}{2}\delta R^2 e^{(\phi_s - V)/v_{th}}} + 1 \right) \quad (2.23)$$

The solution of Equation (2.23) gives the initial guess in strong inversion:

$$\phi_s = V_{gf} + C_R + v_{th} - 2v_{th}\mathcal{L}\left\{C_R R\sqrt{2\delta}e^{(V_{gf} + C_R - V)/2v_{th}}/4v_{th}\right\} \quad (2.24)$$

where $\mathcal{L}$ is the *Lambert W* function (in which an extra v_{th} is added for convergence) [36].

The Equation (2.24) is analogous to Equation (9) in [37] which is derived for undoped bulk MOSFETs.

With these two initial guesses, accurate ϕ_s can be obtained by solving Equation (2.20) with NR iteration method in a few iteration steps.

Figure 2.2: Equation residue at each iteration count for NR solution of (2.20)

Figure 2.2 shows the NR equation residue for the first four iterations. The maximum equation residue of the initial guess is around 10^{-7} V, which indicates a very good one, and it improves with each iteration until reaching the tolerance of 10^{-15} V within four iterations. It can also be seen that in the volume inversion region, the equation residue can reach the desired tolerance within 1 or 2 iterations.

Figure 2.3: Surface potential solution at different channel voltage

Figure 2.3 shows the surface potential solution at different channel voltages. It shows that the surface potential characteristic in SG SiNW MOSFETs is similar to that in bulk MOSFETs. In volume inversion region, ϕ_s is roughly equal to V_{gf} which means inversion charge is very small. In strong inversion region, ϕ_s remains relatively constant with increase in the gate bias.

Figure 2.4. Modeled/numerical surface potentials and their difference (inset), showing increased “error” in numerical solutions at larger radius due to grid density.

We use TCAD (Medici) numerical simulations of an undoped cylindrical GAA MOSFET, with gate length $L = 10$ nm, gate oxide thickness $T_{ox} = 2$ nm, nanowire radius $R = 1, 10, 20$ nm, and a (fixed) constant mobility $\mu = 300$ cm²/V-s, for model validation. The comparison of surface potentials with numerical data generated with three values of SiNW radius is shown in Figure 2.4. The modeled surface potential shows excellent match with the numerical data for all different R . The “error” of the numerical solution is included in the inset. It can be seen that the error becomes larger as the radius increases. Such an increase in the difference is most likely due to the grid dependence of the numerical solution when the radius increases, since iterative solution represents the exact solution.

2.4. Analytical Approximation in Surface Potential Solution of Surrounding Gate Silicon Nanowire MOSFET

Table look-up and analytical approximations are two other approaches besides the iterative approach [38, 39]. In table lookup approach, the table will be very large due to many physical variables and the derivative problem is difficult to be solved. Thus, table lookup approach is not considered appropriate for surface potential solution in compact modeling. Another approach is to obtain the surface potential solution by solving Poisson's equation together with Gauss' law using an analytical approximation. The analytical approach can reduce the simulation time by eliminating the iterations, thus, it is desirable for compact modeling. A good initial approximate solution is also very important for the final accurate analytical solution. Firstly, we need to obtain the regional solutions in volume inversion and strong inversion regions, respectively. In volume inversion region the inversion charge is very small and $\phi_s \approx V_{GF}$, ϕ_s is solved from Equation (2.20):

$$\phi_{s1} \approx V_{gf} - \frac{4\epsilon_{si}v_{th}}{RC_{ox}} \left(\frac{\delta R^2 \left(1 + \frac{V_{gf}}{v_{th}} \right)}{-4 + 2\sqrt{4 + 2\delta R^2 \left(1 + \frac{V_{gf}}{v_{th}} \right)}} - 1 \right). \quad (2.25)$$

In strong inversion, neglecting the first term in the right hand side of Equation (2.20), we obtain the approximate surface potential solution

$$\phi_{s2} \approx v_{th} \ln \left(\frac{8 \cdot \frac{4\epsilon_{si}v_{th}}{RC_{ox}} \cdot V_{GF} \left(\frac{4\epsilon_{si}v_{th}}{RC_{ox}} \cdot V_{GF} + 1 \right)}{\delta R^2} \right). \quad (2.26)$$

The above two piecewise regional solutions are only physically correct in the respective regions. A unified solution valid in all regions is desirable. Therefore, we introduce the a smoothing function to link the two regions smoothly. With the smoothing function [40], a unified surface potential is obtained

$$\phi_{s3} = \frac{1}{2} \left(\phi_{s2} + \phi_{s1} - \sqrt{(\phi_{s2} - \phi_{s1})^2 - d} \right) \quad (2.27)$$

where d is a smoothing parameter.

To improve the accuracy of ϕ_{s2} , we substitute the V_{GF} with $V_{GF} - \phi_{s3}$ in Equation (2.26), which gives

$$\phi_{s4} \approx v_{th} \ln \left(\frac{8 \cdot \frac{4\epsilon_{si} v_{th}}{RC_{ox}} \cdot (V_{GF} - \phi_{s3}) \left(\frac{4\epsilon_{si} v_{th}}{RC_{ox}} \cdot (V_{GF} - \phi_{s3}) + 1 \right)}{\delta R^2} \right). \quad (2.28)$$

Again, with the smoothing function,

$$\phi_{s5} = \frac{1}{2} \left(\phi_{s4} + \phi_{s1} - \sqrt{(\phi_{s4} - \phi_{s1})^2 - d} \right). \quad (2.29)$$

In our model, (2.27)-(2.29) will be repeated twice, and then an accurate surface potential can be obtained, which will be used as the initial approximate solution. The rigorous surface potential is obtained by applying Schroder series [41]

$$\phi_s = \phi_{s5} + K - \frac{f_2}{2f_1} K^2 + \frac{(3f_2)^2 - f_1 f_3}{6(f_1)^2} K^3 + \frac{10f_1 f_2 f_3 - (f_1)^2 f_4 - 15(f_2)^3}{24(f_1)^3} K^4. \quad (2.30)$$

where $K = -f_0/f_1$ and $f_n(\phi_{s5}) = d^n f / d^n \phi_s$. In our model, the surface potential solution calculated with Equation (2.30) is accurate enough for most cases. If accuracy of the solution still does not meet the requirement, Equation (2.30) can be repeated a few more steps until the desired accuracy is reached. The accuracy of analytical approximation in surface

potential solution has been verified against TCAD numerical solutions. Figure 2.5 shows the comparison between analytical surface potential solution and TCAD numerical solution. The good agreement is shown from volume inversion region to strong inversion region. The error is very small indicating good accuracy of the analytical approximation solution. The small error is negligible for accurate current and charge calculations in the model.

Figure 2.5. Surface potential comparison between numerical solution and analytical solution.

2.5. Long Channel Drain Current Modeling

After different voltages are applied at the drain and source ends, respectively, the inversion charge (electrons in nMOSFET) will move from source to drain by a combination of drift and diffusion, resulting in the drain-source current. The drain current can be calculated by integrating the inversion charge with respect to the channel voltage from source to drain along the channel [42, 43]. Therefore, the first step is to obtain the channel voltage expression as a function of the applied gate voltage and surface potential.

In order to obtain the channel voltage expression, Equation (2.20) is rearranged as:

$$V_{gf} - \phi_s + C_R = -C_R \frac{C_1}{4 - 4\sqrt{1 + \frac{1}{2}C_1}} \quad (2.31)$$

where $C_1 = \delta R^2 \exp[(\phi_s - V)/v_{th}]$. C_1 can be solved from Equation (2.31) and, after rearranging,

$$e^{(\phi_s - V)/v_{th}} = \frac{8(V_{gf} - \phi_s + C_R)(V_{gf} - \phi_s)}{\delta R^2 C_R^2} \quad (2.32)$$

from which the channel voltage V as a function of ϕ_s can be obtained,

$$V = \phi_s - v_{th} \ln \left(\frac{8(V_{gf} - \phi_s + C_R)(V_{gf} - \phi_s)}{\delta R^2 C_R^2} \right). \quad (2.33)$$

Therefore, the derivatives of the channel voltage with respect to surface potential is given by

$$\frac{dV}{d\phi_s} = 1 + v_{th} \frac{2V_{gf} - 2\phi_s + C_R}{(V_{gf} - \phi_s + C_R)(V_{gf} - \phi_s)} \quad (2.34)$$

From current continuity, the drain current $I_{ds} = -\mu(2\pi R)Q_{sc}(y)dV/dy$ is constant at any position along the channel from drain to source. Drain current can be obtained by integrating inversion charge from source to drain:

$$I_{ds} = \mu \frac{2\pi R}{L} \int_0^{V_{ds}} (-Q_{sc}) dV. \quad (2.35)$$

Performing a change of variable and integrating Equation (2.18) together with Equation (2.35), we obtain

$$\begin{aligned} I_{ds} &= \mu \frac{2\pi R}{L} \int_{\phi_s(0)}^{\phi_s(L)} (-Q_{sc}) \frac{dV}{d\phi_s} d\phi_s \\ &= \mu C_{ox} \frac{2\pi R}{L} \left\{ V_{gf} \Delta\phi - \bar{\phi}_s \Delta\phi + v_{th} \left[2\Delta\phi + C_R \ln \left(\frac{V_{gf} - \phi_s(L) + C_R}{V_{gf} - \phi_s(0) + C_R} \right) \right] \right\} \end{aligned} \quad (2.36)$$

where

$$\Delta\phi = \phi_s(L) - \phi_s(0), \quad (2.37a)$$

and

$$\bar{\phi}_s = \frac{\phi_s(0) + \phi_s(L)}{2} \quad (2.37b)$$

are the difference and average surface potentials between source and drain, respectively. Equation (2.36) is a single-piece surface-potential-based current equation, which is valid for all regions without any approximations. The first two terms are the drift current and the third term ($2v_{th}\Delta\phi$) is the diffusion current. There is an extra logarithmic term that contributes to the diffusion current of the GAA SiNW MOSFET, compared to the bulk-MOS counterpart.

In doped MOSFET modeling, all current equations without integrations are

derived based on the Charge Sheet Approximation. For undoped devices, the Charge Sheet Approximation is not required because the depletion charge is zero. To compare the current equations derived with and without the CSA, we derive another current equation with CSA. Equation (2.34) is rewritten as:

$$\begin{aligned} \frac{dV_c}{d\phi_s} &= 1 + v_{th} \cdot \left(\frac{1}{V_{gf} - \phi_s} + \frac{1}{(V_{gf} - \phi_s + C_R)} \right) \\ &\approx 1 + v_{th} \cdot \left(\frac{1}{V_{gf} - \phi_s} \right) \end{aligned} \quad (2.38)$$

Substituting Equation (2.38) into Equation (2.36), it yields:

$$I_{ds} = \mu \frac{2\pi RC_{ox}}{L} \left[(V_{gf} + v_{th}) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) \right] \quad (2.39)$$

Equation (2.39) is the drain current following Brews Charge Sheet Approximation and it is similar to the Brews drain current equation in bulk MOSFET [19].

Figure 2.6 shows the comparison of drain current with and without CSA. In volume inversion region, the difference is very small because of the small inversion charge. In strong inversion region, the current without CSA becomes larger. Because in strong inversion region, the thickness of the inversion charge, which contributes to the drain current, is not zero.

Figure 2.6: Comparison of non-charge-sheet with charge-sheet drain current.

To verify the I-V model, we compare the model results with ideal numerical devices in all regions including volume inversion, strong inversion, linear and saturation regions. There are several mobility models implemented in TCAD including low field, parallel field and transverse field mobility models. In this chapter, the low field mobility model is employed with a constant mobility ($300\text{cm}^2/\text{V}\cdot\text{s}$) because mobility modeling is not involved in proposal long channel IV model and high field effects are neglected. In the MEDICI simulations in chapter 3, mobility model is employed with the mobility selection flags: LSMMOB and FLDMOB, the Lombardi surface mobility model activated with LSMMOB parameter and parallel field-dependent mobility is activated with FLDMOB parameter. In TCAD, several numerical methods are implemented to solve the partially difference equations and the most stable two methods are Newton's method and Gummel's method, Newton's method is used in our TCAD simulations. Without any

fitting parameter, the drain current model has been validated against TCAD numerical simulations.

Figure 2.7 compares I_{ds} – V_{gs} characteristics in linear/saturation and volume/strong-inversion regions with the numerical data. The model matches the data for all different radius for both subthreshold and strong-inversion current, in both linear and saturation regions. It also shows decreasing current at reduced radius since $2\pi R$ is equivalent to the MOSFET width.

(a)

(b)

Figure 2.7: Transfer characteristics in (a) linear and (b) saturation for three values of radius.

Figure 2.8: Transconductance characteristics in linear/saturation regions.

Transconductance is important for small-signal analyses [44]. A physical compact model needs to have correct transconductance behaviors. We show the comparison of the transconductance between the model and numerical data in Figure 2.8. It can be seen that both linear and saturation operations match the data in both volume inversion and strong-inversion regions for all different values of radius.

Figure 2.9: Output characteristics and drain conductance in strong inversion.

Figure 2.10: Output characteristics and drain-conductance derivative in subthreshold.

Figures 2.9 and 2.10 illustrate comparison of $I_{ds} - V_{ds}$ characteristics and output conductance between the model and numerical device. Both linear and saturation regions match well, including subthreshold-saturation region at low V_{gs} , as well as the derivative of the drain conductance (g_{ds}) plotted on logarithmic scale in Figure 2.10.

2.6. Summary

The core I-V model for ideal long-channel undoped SiNW MOSFETs is developed in this chapter. The Poisson's equation is solved with variable transformation technique and gradual channel approximation. The exact iterative surface potential solution is obtained within a few iteration steps based on a good initial guess; thus, it is appropriate to be employed in a compact model. The analytical approximate surface potential solution is derived by applying Schroder series and the accuracy is validated. An analytical single-piece drain current model valid for all regions is developed without making charge sheet approximation. Without any fitting parameters, we compare the I-V model with TCAD numerical simulation, and excellent agreement is shown in all operation regions. In the next chapter, the core I-V model will be further extended into short channel devices by modeling short channel effects.

CHAPTER 3: SHORT CHANNEL DRAIN CURRENT MODEL OF UNDOPED SILICON NANOWIRE MOSFETs

In the previous chapter, we consider the GAA SiNW MOSFET to be long channel ones and assume the mobility to be independent of the electric field. In this chapter, we extend the core I-V model, which is developed for long channel devices, into short channel devices by including the short channel effects. The mobility degradation due to both transverse and longitudinal fields will be included into the drain current model. The velocity saturation will also be considered. We also include the saturation voltage into the drain current model. The effect of the series source and drain junction resistance on drain current is modeled following the similar methodology adopted in our bulk MOSFET model. The short channel effects such as channel length modulation, drain induced barrier lowering, subthreshold slope degradation and threshold voltage roll-off are included into the drain current for a complete core I-V model. The Gummel symmetry test is also discussed.

3.1. Introduction

The core I-V model described in chapter 2 is developed for ideal intrinsic long channel devices with constant mobility. In this chapter, we extend the core I-V model into short channel devices by modeling the short channel effects, mobility degradation and extrinsic effects.

The carrier mobility is determined by scatterings carriers experience during their movement. The scattering rate is dependent on the carrier energy, obtained from the electric field in the channel. The electric field is separated into two components: transverse electric field and longitudinal (lateral) electric field. The mobility model is also separated into two parts, namely, low field mobility and high field mobility. With low V_{ds} , the effect of lateral electric field on mobility is ignored, the mobility is called low field mobility. Under high V_{ds} , the mobility is conventionally called high field mobility. For low field mobility, the universal relationship between the carrier mobility in the inversion layer and the effective electric field perpendicular to the channel has been well established. In our model, we model the low field mobility with the Matthiessen rule and the effective electric field is calculated using Gauss's law. To include the velocity saturation, the high field mobility is modeled.

The gate control ability of cylindrical SiNW MOSFETs is much better than that of conventional bulk MOSFETs and double gate MOSFETs. Therefore, the short channel effects are not as severe as in those devices. However, as the channel length reduces, the effectiveness of the gate voltage control will still be degraded due to lateral electric field

effects. Nevertheless, the short channel effects in cylindrical SiNW MOSFETs are still significant to be included into the model. For short channel devices, the gradual channel approximation is no longer valid due to the lateral electric field effect. The short channel effects are essentially 2D effects, thus, to model those effects the 2D Poisson's equation needs to be solved.

Some important short channel effects include velocity saturation, channel length modulation, drain induced barrier lowering, subthreshold slope degradation and threshold voltage roll-off. Velocity saturation has been included into drain current by lateral field mobility degradation model and saturation voltage model. The saturation voltage is determined by two piecewise drain current models, namely, linear and saturation region drain current models. Then, the unified drain current is obtained using a smoothing function. Channel length modulation has been modeled based on energy-balance formulations. The other three short channel effects are all related to the potential barrier lowering at the source end. The inclusion of these three short channel effects can be modeled through the threshold voltage shift.

3.2. Mobility Model

Carrier mobility is an important parameter in I-V model of modern MOSFETs and it is determined by scattering mechanisms. The scattering of the mobile electrons is caused by imperfections of the semiconductor crystal. Accurate mobility models require incorporation of all the basic scattering mechanisms in the inversion layer. At least three important scattering mechanisms have been identified: Coulombic scattering, phonon scattering, and surface roughness scattering. In compact modeling, most mobility models are semi-empirical [45-51].

The mobility variation is dependent on electric field (including both transverse and lateral fields). The transverse field-dependent mobility can be expressed with the well-known Matthiessen's rule for the three mechanisms as:

$$\frac{1}{\mu_s} = \frac{1}{\mu_{co}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}. \quad (3.1)$$

The phonon scattering, surface roughness scattering and Coulombic scattering are given by:

$$\mu_{ph} = \frac{\mu_2}{E_{eff}^{0.3}}, \quad (3.2)$$

$$\mu_{sr} = \frac{\mu_3}{E_{eff}^m}, \quad (3.3)$$

and

$$\mu_{co} = \mu_1, \quad (3.4)$$

where μ_1 , μ_2 , μ_3 , m are treated as fitting parameters. E_{eff} is the effective transverse

electric field. Coulombic scattering is caused by charged centers, thus it is independent of transverse electric field and it is the dominant scattering mechanism contributing to mobility degradation at low transverse field. Phonon scattering originates from the interaction of carriers with lattice vibrations. The interaction is dependent on transverse field and temperature. Surface roughness scattering is strongly dependent on the transverse electric field and is the most important scattering mechanism at high electric fields.

With Equations (3.2) to (3.4), transverse field-dependent mobility is given as

$$\mu_s = \frac{\mu_1}{1 + \frac{\mu_1}{\mu_2} E_{eff}^{0.3} + \frac{\mu_1}{\mu_3} E_{eff}^m} . \quad (3.5)$$

Effective transverse electric field is the average field and can be calculated with Gauss's law. The average transverse field from the surface to the center of silicon body is calculated from Equation (2.14):

$$\begin{aligned} E_{eff} &= \frac{\int_0^R E(r) dr}{R} \\ &= \frac{-2v_{th} \log(1 + BR^2)}{R} . \\ &= \frac{2v_{th} \log\left(\frac{Q_{sc} + C_R}{C_R}\right)}{R} \end{aligned} \quad (3.6)$$

And then taking average along the channel, we obtain:

$$E_{eff} = \frac{\int_0^{V_{ds}} E_{eff \perp} dV}{V_{ds}} \quad (3.7)$$

$$= \frac{\zeta_n v_{th}}{R \cdot C_{ox}} \ln \left(\frac{(C_{ox} \cdot (V_{gs} - \phi) + C_R)}{C_R} \right) \cdot \left(C_{ox} \cdot (V_{gs} - \phi) + C_R \right) + \left(C_{ox} \cdot (V_{gs} - \phi) + C_R \right) \Big|_{\phi_0}^{\phi_L} \Big/ V_{ds}$$

where ζ_n is a fitting parameter with a typical value 0.5.

Figure 3.1: Effective field vs. gate voltage.

Figure 3.1 is the effective field calculated with Equation (3.7) at different V_{gs} . It shows that effective field behavior in SiNW MOSFETs is similar to that in bulk MOSFETs. In volume inversion region, the effective field approaches zero and it increases rapidly in strong inversion region.

Lateral field plays a more significant role in mobility degradation than transverse field when V_{ds} increases beyond the gradual channel approximation due to the velocity saturation [52, 53]. For high lateral electric field, the velocity is no longer proportional to the field but tends to saturate. This phenomenon is known as velocity saturation. The mobility degradation due to coupled lateral and transverse field effects is commonly given by:

$$\mu_{eff0} = \frac{\mu_s}{\left(1 + \left(\frac{\delta_0 V_{ds}}{E_{sat} L}\right)^2\right)^{1/2}}, \quad (3.8)$$

where δ_0 is a fitting parameter used to match measurement data, its typical value is 1.

$E_{sat} = 2v_{sat}/\mu_s$ is the saturation field, v_{sat} is the saturation velocity.

3.3. Saturation Voltage Modeling

In saturation region, the drain current does not increase with increasing V_{ds} but saturates at some maximum current [54]. For conventional long channel devices, the saturation voltage is defined as the drain voltage at which the drain end inversion charge $Q_{sc}(L)$ approaching zero. However, this definition is not valid for short channel devices due to the fact that velocity saturation occurs before the drain end inversion charge satisfy saturation condition [55]. For short channel devices, the maximum current is limited by the velocity saturation, and the saturation voltage is defined as the voltage at which the current reaches the maximum current. The saturation voltage is the intercept between liner region and saturation region, which can be determined by the saturation current, at which the velocity reaches saturation velocity.

Firstly, an approximate linear drain current expression is derived. In linear region, the following approach is applied:

$$\phi_{sL} = \phi_{s0} + V_{ds} \quad (3.9)$$

therefore, drain current equation can be expressed as

$$I_{ds} = \mu_{eff} \frac{2\pi RC_{ox}}{L} \left[(V_{gf} + 2v_{th}) \cdot V_{ds} - \frac{1}{2} V_{ds} \cdot (V_{ds} + 2\phi_{s0}) + v_{th} C_R \ln \left(1 - \frac{V_{ds}}{V_{gf} - \phi_{s0} + C_R} \right) \right] \quad (3.10)$$

The above current equation is only valid in linear region. In saturation region, it is no longer valid.

In saturation region, with the velocity saturation concept, the drain current can be expressed as [56]:

$$I_{dsat} = \nu_{sat} 2\pi RC_{ox} (V_{gf} - V_{dsat} - \phi_{s0}) \quad (3.11)$$

where V_{dsat} is the saturation voltage at which the drain current begins to saturate.

Replacing V_{ds} and I_{ds} with V_{dsat} and I_{dsat} in (3.10), and neglecting the third term in (3.11), combined with (3.10) and (3.11), V_{dsat} can be solved as:

$$V_{dsat} = \frac{LE_{sat} (V_{gf} - \phi_{s0})}{V_{gf} + 2v_{th} - \phi_{s0} + LE_{sat}}. \quad (3.12)$$

The difference between linear and saturation drain current expressions in Equations (3.10) and (3.11) is only the drain-source voltage, where V_{ds} and V_{dsat} are both referred to the one used in the drain current expression in linear and saturation regions, respectively. Thus, a smoothing function is introduced to join the linear and saturation regions. An effective drain-source voltage is introduced:

$$\begin{aligned} V_{dseff} &= \mathcal{G}(V_{ds}, V_{dsat}, \delta_s) \\ &= V_{dsat} - \frac{1}{2} \left[V_{dsat} - V_{ds} - \delta_s + \sqrt{(V_{dsat} - V_{ds} - \delta_s)^2 + 4\delta_s V_{dsat}} \right] \end{aligned} \quad (3.13)$$

where δ_s is a smoothing parameter. Therefore, a unified drain current equation can be obtained:

$$I_{ds} = \mu_{eff} \frac{2\pi RC_{ox}}{L} \left[(V_{gf} + 2v_{th}) \cdot V_{dseff} - \frac{1}{2} V_{dseff} \cdot (V_{dseff} + 2\phi_{s0}) + v_{th} C_R \ln \left(1 - \frac{V_{dseff}}{V_{gf} - \phi_{s0} + C_R} \right) \right] \quad (3.14)$$

3.4. Series Resistance Effect in Drain Current Model

The parasitic series resistance is becoming an important issue in scaled MOSFETs and it is determined by unmeasurable S/D junction lateral diffusion and complicated by its dependence on the gate overdrive [57-61]. If we designate I_{ds0} to be the drain current without the effect of series resistance $R_{sd} = R_s + R_d$, the drain current including R_{sd} will be:

$$I_{ds} = \frac{I_{ds0}}{1 + \frac{R_{sd}}{R_{ch}}} \quad (3.15)$$

where R_{ch} is the intrinsic channel resistance.

It is difficult to distinguish two bias-independent components from the terminal current. Assume that R_{sd} is composed of two parts: a bias-dependent (intrinsic) R_{int} in series with a bias-independent (extrinsic) R_{ext} . We assume that the extrinsic resistance is mainly the sheet resistance:

$$R_{ext} = r_1 = \frac{2\rho S}{\pi R^2} \quad (3.16)$$

where ρ is a fitting parameter and S is the external source/drain length.

According to Ohm's law, the bias-dependent R_{int} is expressed as:

$$R_{int} = \frac{E \Delta y / 2}{J \pi R^2} = \frac{E \Delta y / 2}{I_{ds}} \quad (3.17)$$

where Δy is the source/drain to gate overlap.

Substituting Equation (3.14) into Equation (3.16) and neglecting the logarithmic term, it yields:

$$R_{\text{int}} \approx \frac{E\Delta y/2}{\mu_{\text{eff}} \frac{2\pi RC_{\text{ox}}}{L} \cdot \left[(V_{\text{gf}} + 2V_{\text{th}}) - \frac{1}{2}(V_{\text{dseff}} + 2\phi_s) \right]} \quad (3.18)$$

Equation (3.17) can be rewritten as:

$$R_{\text{int}} = 2 \frac{r_2}{2\pi RC_{\text{ox}} \cdot \left[(V_{\text{gf}} + 2V_T) - \frac{1}{2}(V_{\text{dseff}} + 2\phi_s) \right]} \quad (3.19)$$

where

$$r_2 = \frac{E\Delta y}{\frac{\mu_{\text{eff}}}{L} V_{\text{deff}}} \quad (3.20)$$

The final S/D series resistance is give by:

$$R_s = R_d = \frac{1}{2} R_{\text{sd}} = \frac{R_{\text{ext}} + R_{\text{int}}}{2} = r_1 + \frac{r_2}{2\pi RC_{\text{ox}} \cdot \left[(V_{\text{gf}} + 2V_{\text{th}}) - \frac{1}{2}(V_{\text{dseff}} + 2\phi_{s0}) \right]} \quad (3.21)$$

3.5. Channel Length Modulation Effect in Drain Current Model

The drain current equation (3.14) is derived based on two-region piecewise velocity-field relation model. It assumes that when the lateral-field reaches saturation condition, drift velocity will be saturated at v_{sat} . It is valid in long channel devices but no longer true in short channel devices. In short channel devices, channel-length modulation (CLM) and velocity overshoot become important.

Following the method presented in [62, 63], channel-length modulation model is developed based on momentum and energy conservation of Boltzmann transport equation as well as quasi-2D formulation through [63]. The high-field electron effective velocity is introduced to account for velocity overshoot effects.

High-field electron *effective velocity* is defined as [64]:

$$v_h = v_0 \left(1 + \frac{k}{qE_y} \frac{\partial T_e}{\partial y} \right) = \frac{\mu E_y}{1 + \frac{E_y}{E_{sat}}} \quad (3.22)$$

where

$$E_{sat} = E_{sat} \left[1 + h(V_{ds} - V_{dseff}) \right], \quad (3.23)$$

$$h = \frac{\frac{\xi c}{l^2} \left[1 + \sqrt{1 + \left(\frac{V_{ds} - V_{dseff}}{l E_{sat}} \right)^2} \right]}{\sqrt{1 + \left(\frac{V_{ds} - V_{dseff}}{l E_{sat}} \right)^2} - \frac{\xi c}{l^2} (V_{ds} - V_{dseff})}. \quad (3.24)$$

To model the CLM and velocity overshoot effects, we can apply these formulations in our current model by replacing E_{sat} with E_{satn} in our current model. The effective mobility becomes

$$\mu_{eff0} = \frac{\mu_s}{\left(1 + \left(\frac{\delta_0 V_{dseff}}{E_{satn} L_{eff}}\right)^2\right)^{1/2}}. \quad (3.25)$$

With R_{sd} , the effective mobility can be expressed as:

$$\mu_{eff} = \frac{\mu_{eff0}}{1 + R_{sd} \frac{2\pi R}{L} \mu_{eff0} C_{ox} \cdot \left[(V_{gf} + 2v_{th}) - \frac{1}{2}(V_{dseff} + 2\phi_{s0}) \right]}. \quad (3.26)$$

3.6. Threshold Voltage Definition and Threshold Voltage Shift Effect

Threshold voltage is one of the most important device parameters for the design, modeling, and simulation of MOSFETs[65]. Unfortunately, its value is dependant upon its definition. Most existing threshold voltage definitions based on bulk Fermi potential are only valid for doped MOSFETs and impossible to be extended to undoped MOSFETs. Here, we discuss the definitions of long channel threshold voltage and the shift of threshold voltage in short channel devices.

In undoped SiNW MOSFETs, it is well known that center potential ϕ_0 is roughly equal to the surface potential in volume inversion and saturate to some value in strong inversion. The voltage equation (2.20) can be rewritten in term of center potential,

$$V_{GF} = v_{th} \log\left(\frac{8}{\delta R^2}\right) + v_{th} \log\left(\frac{(1-\beta)}{\beta}\right) + v_{th} \log(\beta) + \frac{\varepsilon_{si} \cdot v_{th}}{C_{ox}} \cdot \frac{4}{R} \frac{(1-\beta)}{\beta}, \quad (3.27)$$

where

$$\beta = 1 - \frac{\delta}{8} \exp\left(\frac{\phi_0}{v_{th}}\right) R^2. \quad (3.28)$$

and ϕ_0 is the potential at the center of SiNW ($r=0$). Thus, the threshold voltage can be defined at the condition of maximum center potential, which is the value when $\beta \rightarrow 1$. Thus, the threshold voltage with the above definition is found from Equation (3.27) to be

$$V_T = V_{FB} + v_{th} \ln\left(\frac{8}{\delta R^2}\right). \quad (3.29)$$

Another method is to define the threshold voltage as the transition point from

volume inversion to strong inversion which is equivalent to the gate voltage at which volume inversion regional surface potential is equal to strong inversion regional potential.

In volume inversion region:

$$V_{GF} \approx \phi_s, \quad (3.30)$$

and in strong inversion region, Equation (2.20) can be approximated as

$$V_{GF} \approx \phi_s + \frac{4\epsilon_{si}v_{th}}{RC_{ox}} \cdot \left(\sqrt{\frac{1}{8}\delta R^2 e^{\frac{\phi_s - V_c}{v_{th}}}} - 1 \right). \quad (3.31)$$

The threshold voltage is obtained by equaling (3.30) and (3.31):

$$V_T = V_{FB} + v_{th} \ln \left(\frac{8}{\delta R^2} \right) \quad (3.32)$$

which is exactly as same as Equation (3.29).

Constant charge definition of threshold voltage for undoped double gate MOSFET is introduced in [66, 67]. The constant charge definition of threshold voltage is to define the threshold voltage as the gate voltage at which the charge is equal to some value Q_T (typical value is $1.2e^{12}cm^{-2}$). In volume inversion, the charge can be approximated as:

$$Q_{sc} \approx -q \cdot n_i \cdot R \cdot \exp \left(\frac{\phi_s}{v_{th}} \right). \quad (3.33)$$

Thus, the threshold voltage is defined as:

$$V_T = V_{FB} + v_{th} \ln \left(\frac{Q_T}{q \cdot R \cdot n_i} \right). \quad (3.34)$$

It is obvious that the threshold voltages defined with the above three definitions are insensitive to oxide capacitance, which is incorrect in physics. Therefore, we define

the threshold voltage as the gate voltage which satisfies $V_{GF}-\phi_s=v_{th}$. The input voltage equation is rewritten in term of center potential and surface potential as

$$C_{ox}(V_{GF}-\phi_s) = \varepsilon_{si} \cdot v_{th} \cdot \frac{R \cdot \delta}{2} \cdot \exp\left(\frac{\phi_0}{2v_{th}}\right) \exp\left(\frac{\phi_s}{2v_{th}}\right). \quad (3.35)$$

In volume inversion, ϕ_0 is approximated as ϕ_s and the threshold voltage is obtained by solving the Equation (3.35) with $V_{GF}-\phi_s=v_{th}$ and approximated as

$$V_T = V_{FB} + v_{th} \ln\left(\frac{8}{\delta R^2}\right) + v_{th} \ln\left(1 + \frac{T_{ox}}{R}\right) + \frac{2 \cdot \hbar^2 \cdot \pi^2}{qm^* R^2}. \quad (3.36)$$

In our model, Equation (3.36) without the last term will be used to calculate the threshold voltage since quantum confinement effect [68] has not been considered. Figures 3.2 and 3.3 show the comparison of threshold voltage with different radius and oxide thickness, the dots and lines are threshold voltage extracted from MEDICI and model with constant current method, respectively, and the triangles are threshold voltage predicted with Equation (3.36), with good agreement.

Figure 3.2: Comparison of threshold voltage with different R

Figure 3.3: Comparison of threshold voltage with different T_{ox}

In previous sections, velocity saturation effect and channel length modulation effect are discussed. Drain induced barrier lowering (DIBL), subthreshold (volume inversion) slope degradation and threshold voltage roll-off are some other important short channel effects, which are all related to the lowering of the source barrier. Reverse bias applied at the drain end creates an electric field, which can lower the potential separating the source and drain, resulting in increased injection of carriers at the source junction [69, 70]. This phenomenon is well-known as drain induced barrier lowering. In our model, subthreshold slope degradation and threshold voltage roll-off are modeled by DIBL model, which is included through a threshold voltage shift. In TCAD simulation, all these short channel effects are included because it solves the 2D Poisson's equation together with 2D current continuity equation.

DIBL is essentially a 2D effect and caused by the lateral electrical field contribution in the channel. DIBL can be modeled using charge sharing concept [71], numerical integration of Poisson's equation [69, 72, 73], or approximate solution of 2D Poisson's equation [74, 75]. The arbitrary division of the charge among gate, drain and source in the charge sharing concept will cause accuracy problems. Numerical integration of Poisson's equation gives accurate result but it is not suitable for compact modeling. Therefore, approximate solution of 2D Poisson's equation method is better than the other two methods in compact model development. In our model, DIBL is modeled by solving the 2D Poisson's equation in volume inversion region with the superposition method, in which we firstly solve the 1D Poisson's equation in the transverse direction, and then, solve the 2D Poisson's equation.

In cylindrical SiNW MOSFETs, neglecting the holes, the 2D Poisson equation is:

$$\frac{1}{r} \cdot \left(\frac{\partial \phi}{\partial r} + r \frac{\partial^2 \phi}{\partial r^2} \right) + \frac{\partial^2 \phi}{\partial y^2} = \frac{qn_i e^{\frac{\phi - \phi_F}{V_{th}}}}{\epsilon_{si}}, \quad (3.37)$$

with the boundary conditions:

$$\phi(O, r) = V_{bi} + V_s, \quad (3.38)$$

$$\phi(L, r) = V_{bi} + V_d. \quad (3.39)$$

where V_{bi} is the source and drain junction build-in potentials. In volume inversion region, it is appropriate to assume quasi Fermi level being constant along whole channel. This approximation is valid in most channel region. To solve the 2D Poisson equation (3.37) with the superposition method, the electric potential is divided into 2 parts:

$$\phi(r, y) = \phi_1(r) + \phi_2(r, y) \quad (3.40)$$

where $\phi_1(r)$ is the solution of 1D Poisson' equation:

$$\frac{1}{r} \cdot \left(\frac{\partial \phi_1}{\partial r} + r \frac{\partial^2 \phi_1}{\partial r^2} \right) = \frac{qn_i e^{\frac{\phi_1 - \phi_F}{V_{th}}}}{\epsilon_{si}}, \quad (3.41)$$

and $\phi_2(r)$ is considered as the potential caused by the lateral electrical field.

And then, we apply Gauss' law to a narrow polygon:

$$\frac{C_{ox}(V_{GF} - \phi_s(y))}{\epsilon_{si}} + \int_0^R \frac{\partial^2 \phi(r, y)}{\partial y^2} dr = \frac{Q_{SC}}{\epsilon_{si}}. \quad (3.42)$$

Neglecting charge induced by ϕ_2 , and in volume inversion $\phi_2(r, y) \approx \phi_2(y)$, we obtain:

$$C_{ox}(V_{GF} - \phi_1(y)) = Q_{SC}, \quad (3.43)$$

$$(-\phi_2(y)) + l_a^2 \frac{\partial^2 \phi_2(y)}{\partial y^2} = 0, \quad (3.44)$$

where l_a is the characteristic field penetration length for cylindrical GAA SiNW MOSFETs which can be determined with evanescent-mode analysis [76, 77]; the one used in the proposal model is given in [78]. The Equation (3.43) is equivalent to the input voltage equation (2.20) under $V_{GF} < V_T$ condition. With a smoothing function, Equation (3.43) becomes

$$C_{ox}(V_{GFS} - \phi_1(y)) = Q_{SC}, \quad (3.45)$$

where $V_{GFS} = \min(V_{GF}, V_T)$.

With the boundary conditions (3.38) and (3.39), the solution of equation (3.44) is found as:

$$\phi_2(y) = (V_d + V_{bi} - \phi_1) \frac{\sinh\left(\frac{y}{l_a}\right)}{\sinh\left(\frac{L}{l_a}\right)} + (V_s + V_{bi} - \phi_1) \frac{\sinh\left(\frac{L-y}{l_a}\right)}{\sinh\left(\frac{L}{l_a}\right)}. \quad (3.46)$$

The DIBL is determined by the minimum potential along the channel. The position of the minimum value of $\phi_2(y)$ at which $\phi_2 = \phi_{2min}$ can be easily found from Equation (28):

$$y_0 = \frac{L}{2} - \frac{l_a}{2} \ln \left(\frac{V_s + V_{bi} - \phi_1 - e^{\frac{L}{l_a}} (V_d + V_{bi} - \phi_1)}{V_d + V_{bi} - \phi_1 - e^{\frac{L}{l_a}} (V_s + V_{bi} - \phi_1)} \right). \quad (3.47)$$

The threshold voltage is defined at the minimum potential along the channel from source to drain; therefore, the threshold voltage shift due to DIBL can be approximated as:

$$\Delta V_T = \phi_{2min} = \phi_2(y_0). \quad (3.48)$$

In the proposal model, to include the DIBL effect, V_{GF} is replaced with an effective gate voltage $V_{GFEFF} = V_{GF} + \Delta V_T$. It is worth noting that with the effective gate voltage, the model captures not only the DIBL effect but also the subthreshold slope degradation and threshold voltage roll-off simultaneously. The surface potentials for short channel devices are calculated with the effective gate voltage and used to calculate the drain current in the I-V model. The DIBL model is validated with TCAD numerical simulations. Figure 3.4 shows the threshold voltage roll-off with different radius, in which the threshold voltage is extracted with the constant current method in MEDICI. The model and threshold voltage roll-off is defined as the difference between the long channel device's threshold voltage and those of the short channel devices. It is shown our model can predict the

threshold voltage roll-off in a large range of channel length. Figure 3.5 shows the comparison of subthreshold slope with different channel lengths and different oxide thicknesses, with good agreements without any fitting parameter. It also shows that the I_{on}/I_{off} ratio is highly dependent on the radius and oxide thickness.

Figure 3.4: Threshold voltage roll-off with different radius

(a)

Figure 3.5: Comparison of subthreshold slope with different L and Tox

3.7. Gummel Symmetry Test

Ideal MOS transistors are symmetric devices, the device behavior should remain the same if the source and drain are interchanged. The compact model is required to satisfy the source-drain symmetry. Gummel symmetry test (GST) was introduced as a benchmark test to qualify a compact model [79, 80]. In GST, the MOSFET is operated with an applied voltage V_g (referenced to ground) to the gate terminal and

$$V_s = V_{go} - V_x, \quad (3.49)$$

and

$$V_d = V_{go} + V_x, \quad (3.50)$$

to the source and drain terminals, respectively, where V_{go} is a constant value. To pass the GST, the drain current needs to meet the requirements:

$$I_d(V_x) = -I_d(-V_x), \quad (3.51)$$

and

$$\left. \frac{d^{2n} I_{ds}}{dV_x^{2n}} \right|_{V_x=0} = 0. \quad (3.52)$$

The core I-V model, which is developed for long channel devices, in principle can meet the GST requirements automatically without any fitting parameters. However, when the core I-V model is extended into short channel devices, the symmetry may be destroyed by the short channel effects modeling. Following the method in our bulk MOSFET model [40], the drain current model has been developed to fulfill the GST requirements without introducing extra parameters.

3.8. Model Verification

The model has been verified against TCAD numerical simulations. All the model parameters are required to be extracted using some methodology before verification based on “golden” data. The model parameters are extracted following the similar procedure in our bulk MOSFET model since both have similar model parameters [81, 82]. The model data successfully match the TCAD numerical results for the drain current and its 1st and 2nd derivatives, transconductance and output conductance for both long and short channel devices.

We use Medici numerical simulations of an undoped cylindrical GAA MOSFET, with gate length $L = 30$ nm, gate oxide thickness $T_{ox} = 2$ nm, nanowire radius $R = 10$ nm for model validation. Fig. 3.6 compares $I_{ds} - V_{gs}$ characteristics in linear/saturation and volume/strong-inversion regions with the numerical data. The model matches the data for all different lengths in both subthreshold and strong-inversion and in both linear and saturation regions. It also shows V_{gs} offset due to the DIBL effect in short channel device captured by our model. Transconductance is important for small-signal analyses. A physical compact model needs to have correct transconductance behavior. We show the comparison of the transconductance of the model and numerical data in Fig. 3.7. It can be seen that the model matches the data in linear and saturation operations in both subthreshold and strong-inversion regions. Fig. 3.8 shows the transconductance derivatives comparison. A continuous transconductance derivatives is important for converge.

Figures 3.9, 3.10 and 3.11 show comparisons of $I_{ds} - V_{ds}$ characteristics and output conductance between the model and numerical device. Both linear and saturation regions match well, including subthreshold-saturation region at low V_{gs} as plotted on a logarithmic scale in Figures 3.10 and 3.11. Figure 3.12 compares the “transconductance efficiency” (g_m/I_{ds}), which is one important feature in circuit design.

Figure 3.6: Transfer characteristics in linear and saturation for $L=30\text{nm}$

Figure 3.7: Transconductance characteristics in linear/saturation regions.

Figure 3.8: Transconductance derivatives in linear/saturation regions.

Figure 3.9: Output characteristics and drain conductance.

Figure 3.10: Output characteristics and drain-conductance derivative

Figure 3.11: Comparison of drain-conductance

 Fig. 3.12. g_m/I_{ds} at various $V_{ds}=0.05$ V, 0.1 V, and 1.2 V

To qualify the model, Gummel symmetry test is performed as shown in Fig. 3.13. The model passed GST with high-order derivatives, which are often required for distortion analyses [83]. It is shown that I_{ds} is an exact odd function of V_{ds} and all the even order derivatives cross $V_x=0$ smoothly.

(a)

(b)

(c)

(d)

(e)

Figure 3.13: GST of I_{ds} (a) and its first (b), second (c), third (d) and fourth (e) order derivatives at various $V_g=0.3 \text{ V}$, 0.6 V , 0.9 V and 1.2 V , $V_s=1/2V_g-V_x$ and

$$V_d=1/2V_g+V_x$$

3.9. Summary

In this chapter, a scalable and physical drain current model for cylindrical GAA SiNW MOSFETs is developed based on our core I-V model. The low field mobility is modeled following Matthiessen's rule, and high field mobility is included in the model with velocity saturation. The saturation voltage is calculated based on two piecewise drain current models similar to the V_T -based approach [60]. The core I-V model is further extended to short channel devices by modeling all major short channel effects, such as channel length modulation, drain induced barrier lowering, subthreshold slope degradation, and threshold voltage roll-off. Since the conventional threshold voltage definition based on bulk Fermi potential can not be adopted in undoped SiNW MOSFETs, a novel threshold voltage definition is introduced and the result is validated with TCAD numerical simulations. The model is verified against TCAD numerical simulations, with good agreement in all regions of operation. The Gummel symmetry test result shows the model's fulfilling GST requirements at high order derivatives.

CHAPTER 4: CAPACITANCE VOLTAGE MODEL OF UNDOPE SILICON NANOWIRE MOSFETs

Dynamic behavior of SiNW MOSFETs is determined by stored terminal charges and capacitances. The C-V model is developed to calculate the stored terminal charge and capacitances. It is as important as I-V model in compact modeling. The terminal charges are calculated based on the drain current model and using the Ward-Dutton partition, which dictates the partitioning of the inversion charge to the source and drain terminals [84]. The capacitances (transcapacitances) are simply obtained by the derivative of the terminal charge with respect to terminal voltage. The important requirements of the C-V model include: simple, accurate, non-negative, continuous, symmetric, and satisfying charge conservation.

4.1. Introduction

In previous chapters, the I-V model is developed assuming steady-state operations. In steady-state operation the terminal voltages of the device remain constant at all times. But in practice the device voltages will vary over time. In other words, the circuit works in dynamic operation. In dynamic operation, the charges stored in the device vary with time.

In a circuit simulator, DC analysis and Operation Point (OP) analysis are steady-state analyses where the voltages in the circuit are time independent. AC analysis and transient analysis are used to determine the circuit functionality in dynamic operation. AC analysis needs the capacitances between the device terminals. Transient analysis needs the charges stored in the device terminals. The C-V model describes the stored terminal charges and transcapacitances. In this chapter, the C-V model for undoped SiNW MOSFETs is developed.

Several models have been proposed for intrinsic capacitances [85-90]. Due to its simplicity, Meyer's model is universally used in all simulators. In the Meyer's model, the gate channel capacitances are modeled by some lumped capacitances. They are defined as the derivative of total gate charge with respect to the other terminal voltage. These capacitances are reciprocal; both terminals of the capacitor are equivalent. The main drawback of the Meyer's model is the charge conservation problem. Charge conservation is very important in some circuits such as switched capacitor filters. However, the charge conservation problem is not caused by Meyer's model itself. It is a result of fault

modeling of capacitive nonlinearities in a circuit simulator [91, 92]. To overcome the charge conversation drawback, charge is introduced as a state variable. The C-V model using charge as the state variable is known as charge based capacitance model. In charge based capacitance model, each terminal has a capacitance with respect to the remaining terminals. Thus, for SiNW MOSFETs, there are 9 capacitances including 3 self capacitances corresponding to its three terminals and 6 nonreciprocal intrinsic capacitances.

A simple, accurate charge based capacitance model for short-channel undoped SiNW MOSFETs is developed based on our surface-potential-based current model. The terminal charge expressions and transcapacitances for long channel device are derived first; and then, short channel effects are included. All information required to calculate the terminal charges can be obtained in the drain current model.

4.2. Intrinsic Long Channel Charge Model

The intrinsic capacitances are derived from the charges stored in each terminal. Thus, to formulate the C-V model we need to find the stored terminal charges Q_g , Q_s and Q_d first. The gate charge is equal to the total inversion charge in the silicon body and the total inversion charge is separated into source and drain terminal charges using the Ward-Dutton partition. The total inversion charge can be obtained by integrating the charge along the channel:

$$Q_i = 2\pi R \int_0^L C_{ox} (V_{gf} - \phi_s(y)) dy, \quad (4.1)$$

where Q_i is the total inversion charge.

As a result, we need to obtain the surface potential along the channel $\phi_s(y)$ and it is obtained using current continuity:

$$I_{ds}(y) = I_{ds}. \quad (4.2)$$

The drain current is given by Equation (2.36) which is valid in all operation regions without the charge sheet approximation. From Equation (2.36), the surface potential along the channel can be obtained and the terminal charge expressions can be formulated. However, the resulting expressions for terminal charges will be very complicated and not suitable to be implemented in a compact model. For simplicity, a charge-sheet approximation in the current expression of a long channel undoped GAA SiNW MOSFET is used to determine the surface potential along the channel, which is written as:

$$\begin{aligned}
 I_{ds} &= 2\pi R\mu Q_{sc}(y) \frac{dV_C}{dy} \\
 &\approx -\mu \frac{2\pi R}{L} \int Q_{sc}(y) d\phi_s + \mu v_{th} \frac{2\pi R}{L} \int dQ_{sc}(y). \\
 &= \mu \frac{2\pi RC_{ox}}{L} \left[(V_{gf} + v_{th}) \cdot \Delta\phi - \Delta\phi \cdot \bar{\phi} \right]
 \end{aligned} \tag{4.3}$$

This drain current expression has been compared with Equation (2.36) in chapter 2, which is used only for determining the surface potential along the channel but not for calculating the drain current. Using this drain current expression, a mathematically simple analytical expression for terminal charges can be obtained.

The expression of y is obtained from Equation (4.3):

$$\begin{aligned}
 y &= \frac{2\pi R\mu}{I_{ds}} \int_{V_s}^V Q_{sc}(y) dV_C \\
 &= \frac{L}{\left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right] \Delta\phi} \left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right] \Delta\phi,
 \end{aligned} \tag{4.4}$$

where

$$dV_C = \left(1 + v_{th} \frac{2V_{gf} - 2\phi_s + C_R}{(V_{gf} - \phi_s + C_R)(V_{gf} - \phi_s)} \right) d\phi_s. \tag{4.5}$$

The relationship between y and surface potential along the channel is given by the above Equation (4.4).

To simplify it, we take the second-order Taylor expansion of y at $\bar{\phi}_s$:

$$\begin{aligned}
 y &\approx \frac{L}{2} \left(1 + \frac{\Delta\phi}{4H} \right) + \frac{L}{\Delta\phi} (\phi_s - \bar{\phi}_s) + \frac{L}{\Delta\phi H} \frac{(\phi_s - \bar{\phi}_s)^2}{2}, \\
 &= \frac{L}{2} \left(1 + \frac{\Delta\phi}{4H} \right) + \frac{L}{\Delta\phi} \left(u - \frac{u^2}{2H} \right)
 \end{aligned} \tag{4.6}$$

where

$$H = \left[(V_{gf} + 2v_{th}) - \overline{\phi_s} \right], \quad (4.7)$$

and

$$u = \phi_s - \overline{\phi_s}. \quad (4.8)$$

Total stored charge of each terminal node is easily obtained by taking integral of the distributed charge densities over the active gate region:

$$Q_G = 2\pi R \int_0^L Q_G(y) dy \quad (4.9)$$

$$Q_i = 2\pi R \int_0^L Q_{SC}(y) dy \quad (4.10)$$

and $Q_G = -Q_i$ from the charge neutrality.

Combining Equations (4.6) and (4.9), we obtain the expression for the total gate charge in equilibrium:

$$\begin{aligned} Q_G &= 2\pi R \int_0^L Q_G(y) dy \\ &= 2\pi R C_{ox} L \left[(V_{gf} - \overline{\phi_s}) + \frac{\Delta\phi^2}{12H} \right]. \end{aligned} \quad (4.11)$$

Figure 4.1 shows the comparison of total gate terminal charge between TCAD numerical simulations and the model in linear and saturation regimes for the long-channel device. The relative error is below 0.1% in strong-inversion regime. Similar behavior to bulk MOSFETs is observed [93], the terminal gate charge follows a logarithm increase in the subthreshold regime and linear increase in the strong-inversion regime.

Figure 4.1: Terminal Gate charge versus gate-source voltage for different V_{ds} with $L=10\mu\text{m}$, $R=10\text{nm}$ and $T_{ox}=2\text{nm}$.

To obtain the source and drain terminal charges, the total inversion charge needs to be partitioned into source and drain portions. The Ward-Dutton method is used in the proposal model:

$$Q_D = 2\pi R \int_0^L \frac{y}{L} Q_i(y) dy$$

$$= \pi R C_{ox} \cdot \left[\frac{-\frac{L}{H^2} \frac{\Delta\phi^3}{80} - \frac{-y_m \Delta\phi^2 + \Delta\phi \cdot L(V_{gf} - \bar{\phi}_s)}{6H}}{-\frac{\Delta\phi L}{6} \left(1 + \frac{(V_{gf} - \bar{\phi}_s)}{2H} \right) + 2y_m (V_{gf} - \bar{\phi}_s)} \right], \quad (4.12)$$

$$Q_S = 2\pi R \int_0^L \left(1 - \frac{y}{L} \right) Q_i(y) dy, \quad (4.13)$$

$$= Q_G - Q_D$$

where

$$y_m = \frac{L}{2} \left(1 + \frac{\Delta\phi}{4H} \right). \quad (4.14)$$

With Equations (4.11)–(4.13), all terminal charges can be analytically calculated based on the surface-potential solution at the source and drain ends. In chapter 2, the surface-potential solution valid for all operation regions is shown. Therefore, the charge expressions (4.11), (4.12), and (4.13) are valid in all operation regions including linear, saturation, subthreshold, and strong inversion regions.

The intrinsic capacitance between two nodes is defined as the change of the charge due to the change of applied potential. The nonreciprocal capacitances are defined simply as [84]:

$$C_{ij} = \delta_{ij} \frac{\partial Q_i}{\partial V_j} \quad \delta_{ij} = \begin{cases} 1, i = j \\ -1, i \neq j \end{cases}. \quad (4.15)$$

C_{jj} capacitances are known as short-circuit input capacitances. It is worthy to note that the capacitances C_{ij} satisfy

$$\sum_i C_{ij} = \sum_j C_{ij} = 0, \quad (4.16)$$

due to charge conservation.

The C-V model is verified against the TCAD numerical simulations. Figures 4.2, 4.3, and 4.4 show the gate-related transcapacitances C_{gg} , C_{gs} and C_{gd} versus V_{gs} from the model in linear and saturation regimes compared with TCAD simulation results. Excellent agreement can be observed. Similar to bulk MOSFETs, C_{gs} and C_{gd} approach different values when $V_{ds} \neq 0$. C_{gs} , C_{gd} , and C_{gg} versus V_{gs} for $V_{ds} = 0$ are shown in Fig. 4.4. When $V_{ds} = 0$, in all operation regimes, C_{gs} is exactly equal to C_{gd} . In undoped body devices, due to lack of depletion charges, the C_{gg} is symmetric about the axis $V_{gs} = V_{FB}$.

Figure 4.5 shows the comparison of nonreciprocal drain-related transcapacitances between Medici and model. Again, excellent agreement is shown with smooth transition across all regimes. It is observed at high V_{ds} , the three transcapacitances approach zero, due to the surface potential being saturated at high V_{ds} .

It is well known that exactly at $V_{gs} = V_{FB}$, there is a singularity in the one-carrier surface potential solution due to ignoring holes [94]. This singularity will result in C_{gg} discontinuity at $V_{gs} = V_{FB}$ which may be detrimental in transient analyses. In the proposed model, ϕ_s is approximated by $\phi_s - \phi_{s_fb}$ where ϕ_{s_fb} is the surface potential at flat band. Fig. 4.6 shows the surface potential versus V_{gs} with and without the correction. It shows that with the correction, the singularity problem is solved.

Figure 4.2. Normalized gate transcapacitance coefficients in linear regimes.

Figure 4.3: Normalized gate transcapacitance coefficients in saturation regimes.

Figure 4.4: Normalized gate transcapacitance coefficients at $V_{ds}=0$.

 Figure 4.5: Normalized drain related transcapacitance coefficient with $V_{gs} = 1.2V$.

Figure 4.6: Surface Potential with/without flat band correction.

4.3. Short Channel Charge Model

In short-channel devices, non-ideal effects, such as mobility degradation, velocity saturation, velocity overshoot, series resistance, channel-length modulation, and drain-induced barrier lowering, threshold roll-off and subthreshold slope degradation are important and must be considered. The inclusion of the short channel effects in the charge model is the key to charge model scalability. The current expression for short-channel GAA SiNWs is obtained by including all the above non-ideal effects and approximated as:

$$I_{ds} \approx \frac{\mu_s 2\pi RC_{ox} \left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right] \Delta\phi}{L + \frac{\delta_L \Delta\phi}{E_{sat}} + R_{sd} \mu_s 2\pi RC_{ox} \left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right]}. \quad (4.17)$$

As described in previous chapter, the surface potential is calculated with inclusion of short channel effects.

Combining Equations (4.4) and (4.17), the y expression becomes

$$y \approx \frac{L}{2} \left(1 + \frac{\Delta\phi}{4H^*} \right) + \frac{L}{\Delta\phi} \left(u - \frac{u^2}{2H^*} \right), \quad (4.18)$$

where

$$H^* = \frac{\left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right]}{1 + \frac{\delta_L \Delta\phi}{LE_{sat}} + \frac{R_{sd} \mu_s 2\pi RC_{ox} \left[(V_{gf} + 2v_{th}) - \bar{\phi}_s \right]}{L}}. \quad (4.19)$$

The total terminal charges are:

$$Q_G = 2\pi RC_{ox} L \left[(V_{gf} - \bar{\phi}_s) + \frac{\Delta\phi^2}{12H^*} \right]. \quad (4.20)$$

$$Q_D = \pi R C_{ox} \left[\begin{aligned} & -\frac{L}{H^{*2}} \frac{\Delta\phi^3}{80} - \frac{-y_m \Delta\phi^2 + \Delta\phi \cdot L(V_{gf} - \bar{\phi}_s)}{6H^*} \\ & -\frac{\Delta\phi L}{6} \left(1 + \frac{(V_{gf} - \bar{\phi}_s)}{2H^*} \right) + 2y_m (V_{gf} - \bar{\phi}_s) \end{aligned} \right], \quad (4.21)$$

$$Q_S = Q_G - Q_D. \quad (4.22)$$

The expressions for terminal charges in short channel devices are similar to those for long channel devices. For short channel devices, the extrinsic capacitances, such as overlap capacitance and fringing capacitance, are important to be included in the model. In the proposal model, the bulk MOSFET extrinsic capacitance model will be adopted.

4.4. Summary

In this chapter, a simple, accurate charge and capacitance model for undoped cylindrical gate-all-around silicon-nanowire MOSFETs is described. The C-V model valid over all operation regions for long channel devices is first developed based on charge sheet approximation in the drain current expression. And then, the C-V model is extended to short channel devices by including the short channel effects. With a simple modification on the surface potential, the model overcomes the singularity problem at $V_{gs} = V_{FB}$. The model has been verified against TCAD numerical simulations, with good agreements in all terminal charges and transcapacitances.

CHAPTER 5: NOISE MODEL OF UNDOPED SILICON NANOWIRE MOSFETs

Noise is the fluctuation in the current or voltage. While the device dimensions keep scaling down, noise becomes a more and more important issue in circuit design since the voltage scaling brings the signal level closer to the noise level, noise has set a limit in semiconductor device scaling down. Noise in the undoped cylindrical SiNW MOSFETs is studied in this chapter. The noise model involving thermal noise and flicker noise of undoped SiNW MOSFETs will be presented. The thermal noise is obtained by integrating the transconductance along the channel. The flicker noise model includes two piece-wise models. In volume inversion region mobility fluctuation is dominating; therefore, Hooge's model is adopted. In strong inversion region, the noise model formulation is derived based on the McWorther model.

5.1. Introduction

The spontaneous fluctuations in current and voltage inside the device generate noise. Noise signal is a random signal which can be characterized by the power spectral density (PSD). In most circuits, noise is some unwanted signal which is to be eliminated or reduced.

In semiconductor devices and circuits, the most important noise sources are thermal noise, shot noise, generation-recombination noise, and flicker noise. The thermal noise is caused by the random motion of the electrons in the conducting current. Shot noise occurs when carriers cross the barriers at random [95]. Generation-recombination noise is caused by the trapping and detrapping of the carriers. And flicker noise, also known as $1/f$ noise, is an elusive noise source. The fluctuation source of the flicker noise is either fluctuation in mobility or fluctuation in number of carriers, which has been argued for decades.

The thermal noise and flicker noise are the two dominating noise in modern MOSFETs. In this chapter, the thermal noise model is derived for undoped cylindrical SiNW MOSFETs based on our I-V model. And a piece-wise flicker noise model is developed considering both fluctuation in mobility and fluctuation in the number of carriers. In number fluctuation model, the flicker noise model equation is derived based on the Shockley-Read-Hall theory [96].

5.2. Thermal Noise Model

As a result of finite temperatures, electrons in the conductor undergo Brownian motion via collisions with the lattice. The Brownian motion of the electron produces fluctuation in the terminal current and voltage. This stochastic fluctuation is known as thermal noise. It is first discovered by Jonhson in 1928; therefore, thermal noise is also called Johnson noise. For a resistance R at temperature T , the noise properties are described by Nyquist theorem [97]:

$$S_v(f) = 4kTR, \quad (5.1)$$

$$S_i(f) = 4kT/R. \quad (5.2)$$

The PSD of thermal noise is independent of the applied voltage; it is determined by the resistance and temperature.

The channel in a field effect transistor is indeed a modulated resistor; thus, there is thermal noise in the channel. The channel resistance is dependent of the applied voltages; therefore, the PSD of the thermal noise is a function of applied voltages. The local fluctuations in the channel will produce two noise currents: channel current noise and induced gate current noise. Induced gate current noise originates from channel noise due to the channel being coupled to gate through gate oxide capacitance. However, the induced gate current noise is only important in very high frequency and is not studied in our work.

The drain current can be represented as:

$$I_{ds} = g(V_C) \frac{dV_C}{dy}, \quad (5.3)$$

where $g(V)$ is the conductance at position y , V_C is the channel potential. According to current continuity, the current is constant everywhere in the channel, independent of y .

Integrating Equation (5.3) from source to drain end, it yields:

$$I_{ds} = \frac{1}{L} \int_{V_s}^{V_d} g(V) dV. \quad (5.4)$$

The PSD of the channel thermal noise can be obtained by integrating the conductance along the channel, it given by[98]:

$$S_{I_{ds}} = \frac{4kT}{L^2 I_{ds}} \int_{V_s}^{V_d} g^2(V) dV. \quad (5.5)$$

This equation is a general equation that can be applied to conventional MOSFETs, double gate MOSFETs, and SiNW MOSFETs. In undoped cylindrical SiNW MOSFETs, the drain current can be expressed as:

$$\begin{aligned} I_{ds} dy &= \mu_{eff} \cdot Q_{SC}(V_C) dV_C \\ &= \mu_{eff} \cdot Q_{SC}(V_C) \cdot \left(1 + v_{th} \frac{2V_{gf} - 2\phi_s + C_R}{(V_{gf} - \phi_s + C_R)(V_{gf} - \phi_s)} \right) d\phi_s, \end{aligned} \quad (5.6)$$

where Q_{SC} is the inversion channel charge, which is a function of the channel potential V_C .

From Equations (5.3) and (5.6), it follows:

$$g(V_C) = 2\pi R \cdot \mu_{eff} \cdot Q_{SC}(V_C) = 2\pi R \cdot \mu_{eff} \cdot C_{ox} \cdot (V_{gf} - \phi_s). \quad (5.7)$$

The expression of V_C is given by Equation (2.33), thus

$$g^2(V_C) dV_C = (2\pi R C_{ox})^2 \mu_{eff}^2 \left((V_{gf} - \phi_s)^2 + v_{th} \frac{(V_{gf} - \phi_s)(2V_{gf} - 2\phi_s + C_R)}{(V_{gf} - \phi_s + C_R)} \right) d\phi_s, \quad (5.8)$$

Substituting Equation (5.8) into Equation (5.5), the PSD of channel thermal noise current can be obtained as:

$$\begin{aligned}
 S_{I_{ds}} &= \frac{4k_B T}{I_{ds} \cdot L^2} \int_{V_s}^{V_d} g^2(V_c) dV_c \\
 &= \frac{(2\pi R C_{ox})^2 \mu_{eff}^2 4k_B T}{I_{ds} \cdot L^2} \left[\frac{1}{3} (V_{gf} - \phi_s)^3 + v_{th} (V_{gf} - \phi_s)^2 - \right. \\
 &\quad \left. C_R v_{th} (V_{gf} - \phi_s) + v_{th} C_R^2 \ln((V_{gf} - \phi_s) + C_R) \right] \Big|_{\phi_d}^{\phi_s}
 \end{aligned} \tag{5.9}$$

This equation is valid from volume inversion region to strong inversion region and from linear region to saturation region.

5.3. Generation-Recombination Noise

Generation-Recombination (g-r) noise is the noise produced in the Generation-Recombination process; it is caused by the fluctuation in the number of carriers due to emission and capture of the carriers by traps. Different from thermal noise, g-r noise is observed only if external bias is applied. G-r noise is considered as the origin of Random Telegraph Noise and flicker noise (1/f noise).

A summary of g-r noise model is presented as follows. Considering g-r process, the number of carriers change rate can be expressed as:

$$\frac{dN}{dt} = g(N) - r(N) + H(t), \quad (5.10)$$

where N is the number of carriers, $g(N)$ is generation rate and $r(N)$ is recombination rate, and $H(t) = \Delta g(t) - \Delta r(t)$ is the fluctuation in g-r rate. Under equilibrium condition, substituting $N_t = N_0 + \Delta N_t$ and $g(N_0) = r(N_0)$ in Equation (5.10) and taking first order Taylor expansion, it yields:

$$\begin{aligned} \frac{d(\Delta N)}{dt} &= \left[\left. \frac{d[g(N)]}{dN} \right|_{N_0} - \left. \frac{d[r(N)]}{dN} \right|_{N_0} \right] \cdot \Delta N + H(t), \\ &= -\frac{\Delta N}{\tau} + H(t) \end{aligned} \quad (5.11)$$

where τ is the lifetime of carrier (time constant) in the g-r process. Reverse Fourier transforms of ΔN and $H(t)$ are obtained as:

$$\Delta N(t) = \int_{-\infty}^{\infty} A e^{j\omega t} dt \quad (5.12)$$

$$H(t) = \int_{-\infty}^{\infty} B e^{j\omega t} dt. \quad (5.13)$$

Combining Equations (5.11), (5.12), and (5.13), we have

$$A = \frac{B\tau}{1 + j\omega\tau}. \quad (5.14)$$

Therefore, the relationship between PSD of ΔN and PSD of $H(t)$ can be obtained as:

$$S_N = S_H \frac{\tau^2}{1 + \omega^2 \tau^2}, \quad (5.15)$$

which is a Lorentzian spectrum. To obtain the PSD of g-r noise we only need to determine the time const τ and S_H . $H(t)$ is a white noise, thus

$$S_H(f) = S_H(0) = E(\Delta N^2) \frac{4}{\tau}, \quad (5.16)$$

where $E()$ is the mathematical expectation, the expression of $E(\Delta N^2)$ is given as $E(\Delta N^2) = g(N_0)\tau$. And for noise signals in a transistor, it is commonly known $E(\Delta N^2) = \sigma_{\Delta N}^2$ due to $E(\Delta N) = 0$. Equation (5.15) can be rewritten as:

$$\begin{aligned} S_N &= E(\Delta N^2) \frac{4\tau}{1 + \omega^2 \tau^2}, \\ &= g_0 \tau \frac{4\tau}{1 + \omega^2 \tau^2}, \end{aligned} \quad (5.17)$$

where $g_0 = g(N_0)$. This is the general equation to calculate the PSD of g-r noise, in which g_0 and τ are required to be determined. The expression of g_0 and τ are dependent on the approach used in modeling the g-r process. In almost all MOSFET compact models, the $E(\Delta N^2)$ is approximated to be a linear function of trap density N_{it} . In our model a different

approach is taken. According to Shockley-Read-Hall theory, the generation rate and recombination rate are expressed as:

$$g(N) = c_n n P_T - e_n N_T \quad (5.18)$$

and

$$r(N) = c_p p N_T - e_p P_T, \quad (5.19)$$

where c_n and c_p are the electron/hole capture coefficients, e_n and e_p are electron/hole emission coefficients, n and p are electron and hole densities, respectively, P_T and N_T are g-r centers filled with electrons and empty g-r centers, respectively. The time rate of change in carrier density is obtained as:

$$\begin{aligned} \frac{\partial(n-p)}{\partial t} &= c_n n P_T - e_n N_T - (c_p p N_T - e_p P_T) \\ &= -(c_n n + e_n + c_p p + e_p) N_T + (e_p + c_n n) N_{IT} \end{aligned} \quad (5.20)$$

where $N_{IT} = N_T + P_T$. Under steady-state conditions, N_T and P_T do not change with time, one can write

$$N_T = \frac{(c_n n + c_p p_1)}{c_n (n + n_1) + c_p (p + p_1)} N_{IT}, \quad (5.21)$$

and p_1, n_1 are given as:

$$n_1 = n_i e^{\frac{(E_T - E_i)}{kT}} \quad \text{and} \quad p_1 = n_i e^{\frac{(E_i - E_T)}{kT}}, \quad (5.22)$$

where E_T is the energy level of the g-r center. The total interface-trap charge is the sum of the charges at the neutral electron and hole interface traps over the silicon energy gap, given as $Q_{IT} = \int_{E_v}^{E_c} (Q_{NT} + Q_{PT}) dE_T$, Q_{NT} and Q_{PT} are the charges of electron traps and hole traps, respectively. Thus, the total interface-trap charge not only depends on the interface-

trap density but also the applied gate voltage because charge trapping rate is directly related to the surface carrier concentration which is modulated by the gate voltage.

Fig. 5.1 Gate-Source voltage dependence of interface-trap charges at various neutral electron interface-trap densities $N_T = P_T = 1.0 \times 10^{10}$, 1.0×10^{11} , 1.0×10^{12} , 2.0×10^{12} , and $5.0 \times 10^{12} cm^{-2}$.

Figure 5.1 shows the gate-voltage dependence of interface-trap charges at various interface-trap densities. As anticipated by Equation (5.21), the charge trapping rate is closely related to the surface carrier concentration, which is a function of the surface potential, and hence, the applied gate voltage. Thus, interface-trap charge is determined not only by interface-trap density but also by the charge trapping rate. For a device with large interface-trap densities, the interface-trap charge is small near the intrinsic region because of the low charge trapping rate while it is large in strong accumulation and

inversion ranges because nearly all the interface traps are trapped with a hole or electron as shown in Figure 5.1. It also shows that the trap charge will decrease rapidly in volume inversion region and, due to the number fluctuation noise being dependent on the trap charge, therefore, the number fluctuation noise also will decrease rapidly in volume inversion region.

In $1/f$ noise, only surface G-R process is contributed to noise in which the interface traps are functionally equivalent to R-G centers. Considering electrons only, Equation (5.20) is simplified as

$$\begin{aligned}\frac{\partial(n-p)}{\partial t} &= P_T(c_n n + e_p) - N_T(e_n + c_p p) \\ &= P_T(c_n n + c_p p_1) - N_T(c_n n_1) \approx P_T \cdot c_n n - N_T \cdot c_n n_1, \\ &= g(N_T) - r(N_T)\end{aligned}\tag{5.23}$$

$$g(N_T) = P_T c_n n \quad \text{and} \quad r(N_T) = N_T c_n n_1.\tag{5.24}$$

Under Stead-State conditions, $g(N_T) = r(N_T)$, thus,

$$N_T = \frac{n}{n + n_1} N_{it} \quad \text{and} \quad P_T = \frac{n_1}{n + n_1} N_{it}.\tag{5.25}$$

The time constant is obtained:

$$\frac{1}{\tau} = - \left(\frac{dg}{dN_T} - \frac{dr}{dN_T} \right) = c_n \cdot n + c_n \cdot n_1.\tag{5.26}$$

The mathematical expectation of the fluctuation in number of carriers is obtained as:

$$\begin{aligned}E(\Delta N^2) &= g_0 \tau = P_T(c_n n) \cdot \tau \\ &= \frac{c_n n \frac{n_1}{n + n_1} N_{it}}{c_n \cdot n + c_n \cdot n_1} = \frac{n \cdot n_1}{(n + n_1)^2} N_{it}^2.\end{aligned}\tag{5.27}$$

Thus, the PSD of the G-R noise caused by interface traps can be obtained by substituting Equation (5.27) into Equation (5.17):

$$S_N = 4 \cdot N_{it} \cdot \frac{n \cdot n_1}{(n + n_1)^2} \cdot \frac{\tau}{1 + \omega^2 \tau^2} . \quad (5.28)$$

5.4. Flicker Noise Model

Flicker noise was first observed in vacuum tubes by Johnson in 1925 [99]. Since its spectral density is inversely proportional to the frequency (it has a $1/f^\alpha$ spectrum with α being close to unity), flicker noise is also known as $1/f$ noise. The flicker noise is a fluctuation in the conductance of semiconductors and metals [100]. It could be a fluctuation in the number of free electrons or in their mobility. In MOSFETs, flicker noise is the dominating noise at low frequency.

For MOSFET flicker noise modeling, there are two conflicting models: number fluctuation model (McWhorter's model) and mobility fluctuation model (Hooge's model [101]). The mobility fluctuation is dominated if the current transport occurs in the body and number fluctuation is dominated only if the current transports near the surface. Unlike conventional MOSFETs in which the channel is highly doped to increase the current density, SiNW MOSFETs is usually undoped or lightly undoped. Thus, in volume inversion region the mobility fluctuation is dominated due to the current transport occurring not only near the surface but also in the body, and number fluctuation is dominated in strong inversion region since most current flows near the surface. Therefore, to model the noise in undoped SiNW MOSFETs we have to involve both mobility fluctuation model and number fluctuation model. In this subsection, we propose two piece-wise noise models for volume inversion and strong inversion regions, respectively. However, a unify flicker noise model valid for both volume inversion region and strong

inversion region can be easily obtained by linking the two piece-wise models with a fitting parameter.

In volume inversion region, the flicker noise in undoped cylindrical SiNW MOSFETs can be modeled empirically with mobility fluctuation model. In mobility fluctuation model, the $1/f$ noise is caused by fluctuations in the mobility of carriers in the conducting channel. The Hooge's model is given by [102]:

$$\frac{S_{I_{ds}}}{I_{ds}^2} = \frac{\alpha_H}{f \cdot N}, \quad (5.29)$$

where $S_{I_{ds}}$ is the power spectral density, α_H is the Hooge parameter, f is the frequency and N is the total number of carriers in the channel. The Hooge parameter, α_H , which is a universal dimensionless constant, is determined only by electron properties and independent of the device structure. Thus, the mobility fluctuation noise also refers to as fundamental $1/f$ noise. It is widely accepted that noise described by the Hooge model is a body effect noise. Although Hooge model equation is an empirical equation, Handel's model explains the mobility fluctuation theoretically with quantum theory [103]. With N given by Equation (4.11), it follows that

$$\frac{S_{I_{ds}}}{I_{ds}^2} = \frac{\alpha_H}{f} \cdot \frac{q}{2\pi R C_{ox} L \left[(V_{gf} - \overline{\phi_s}) + \frac{\Delta\phi^2}{12H} \right]}. \quad (5.30)$$

The volume inversion noise model is verified with real silicon data. The details of the SiNW MOSFETs fabrication process were presented in [3]. The radius of the silicon nanowire is 40nm, the thickness of the gate oxide is 4nm, and the gate length is 90nm.

(a)

(b)

Figure 5.2: (a) Drain current versus gate source voltage (b) Transconductance versus gate source voltage

 Figure 5.3: Drain current spectral density at $V_{ds}=50\text{mV}$ and $f=10\text{Hz}$

 Figure 5.4: $S_{I_{ds}}/I_{ds}$ versus V_{ds} at $f=10\text{Hz}$

Fig. 5.5: S_{IdS} versus V_{ds} at $f=10\text{Hz}$

Prior to calculating the spectral density of the drain current noise, drain current is required to be evaluated first. Figure 5.2 shows the drain current I_{ds} and transconductance versus gate-source voltage V_{gs} at $V_{ds}=50\text{mV}$, in which good agreement is observed. Figure 5.3 shows the normalized drain current noise spectral density S_{IdS}/I_{ds} as a function of I_{ds} at $V_{ds}=50\text{mV}$. The symbols are measured from real silicon wafer and the line is our model result with the Hooge's parameter extracted as 1.575×10^{-4} . Good agreement is seen in both linear and logarithmic scales. The slope of the S_{IdS}/I_{ds}^2 is close to -1, which shows the noise is caused by mobility fluctuation. Figure 5.4 shows the S_{IdS}/I_{ds} versus V_{ds} at $V_{gs}=0.1\text{V}$. It shows our model can match the measurement data very well. It also shows that S_{IdS}/I_{ds} increases linearly in low V_{ds} bias and remains almost constant at high V_{ds} . Figure 5.5 shows the S_{IdS} versus V_{ds} at $f=10\text{Hz}$. The line is the proposal model and the symbols are the result from Equation (10) in [104].

In strong inversion region, the current flowing along the channel can be seen as surface conduction current. The interaction between the interface trap and the electrons in the inversion channel becomes significant. The interaction produces the fluctuations in number of carriers in the inversion channel. Compared to the fluctuations in number of carriers, the mobility fluctuation can be ignored in strong inversion region. Therefore, the main contribution of flicker noise in strong inversion is believed to be the fluctuations in number of carriers.

It is widely accepted that 1/f noise caused by number fluctuation is the summation of many G-R noises. The derivation of the 1/f noise number fluctuation model equation is presented as follows. In the derivation of noise model equation, we assume the device is in linear region (V_{ds} is small) to simplify the derivation. However, it can be easily extended to high V_{ds} condition using Langevin method. If the traps have only one time constant, the spectrum is a Lorentzian spectrum and the PSD of the noise equation, which can be written as

$$S_{N_t} = \sigma_{\Delta N_t}^2 \frac{4\tau}{1 + \omega^2 \tau^2}. \quad (5.31)$$

In real devices the time constant usually vary in a large range, the noise PSD can be obtained by integrating the time constant, which yields

$$S_{N_t} = \sigma_{\Delta N_t}^2 \int_0^{\infty} \frac{4\tau \cdot p(\tau)}{1 + \omega^2 \tau^2} d\tau, \quad (5.32)$$

where $p(\tau)$ is the probability distribution function of time constant τ , and we have

$$\int_0^{\infty} p(\tau) d\tau = 1 \quad \text{and} \quad p(\tau) = \frac{1}{\tau} \cdot \frac{1}{\ln\left(\frac{\tau_2}{\tau_1}\right)}, \quad \tau_1 < \tau < \tau_2. \quad (5.33)$$

Substituting Equation (5.33) into Equation (5.32), it gives

$$S_{N_t}(f) = \frac{\sigma_{\Delta N_t}^2}{\ln\left(\frac{\tau_2}{\tau_1}\right)} \cdot \frac{1}{f}, \quad \left(\frac{1}{2\pi\tau_2} < f < \frac{1}{2\pi\tau_1} \right) \quad (5.34)$$

Combining Equations (5.27) and (5.34) results in

$$S_{N_t}(f) = \frac{1}{\ln\left(\frac{\tau_2}{\tau_1}\right)} \cdot \frac{1}{f} \cdot \int_{E_v}^{E_c} \frac{n \cdot n_1}{(n + n_1)^2} N_{it} dE_T. \quad (5.35)$$

Instead of calculating the integration, we assume only those traps with energy levels near the Fermi level are contributed to the fluctuations in the carriers, and approximate N_{it} as $N_{it} = A \cdot D_{it}$, Equation (5.35) becomes

$$S_{N_t}(f) = \frac{1}{\ln\left(\frac{\tau_2}{\tau_1}\right)} \cdot \frac{1}{f} \cdot D_{it} \cdot \frac{A \cdot n \cdot n_1}{(n + n_1)^2}. \quad (5.36)$$

In SiNW MOSFET, the drain current can be expressed as,

$$I_{ds} = \mu_{eff} \cdot q \cdot n \cdot \frac{dV_C}{dy}, \quad (5.37)$$

where n is the inversion charge. The interaction of the interface traps and the electrons in the channel cause the fluctuations in the flat-band voltage. Furthermore, the fluctuations in flat-band voltage will produce fluctuations in both number of carriers and mobility of the mobile carriers. The fluctuation in drain current is expressed as:

$$\Delta I_{ds} = \frac{dI_{ds}}{dn} \Delta n + \frac{dI_{ds}}{d\mu_{eff}} \Delta \mu_{eff} = \frac{I_{ds}}{n} \frac{dn}{dV_{FB}} \frac{dV_{FB}}{dN_T} \Delta N_T + \frac{I_{ds}}{\mu_{eff}} \frac{d\mu_{eff}}{dV_{FB}} \frac{dV_{FB}}{dN_T} \Delta N_T, \quad (5.38)$$

and,

$$\frac{\Delta I_{ds}}{I_{ds}} = \left(-\frac{R}{n} + \frac{1}{\mu_{eff}} \frac{d\mu_{eff}}{dV_{FB}} \frac{dV_{FB}}{dN_T} \right) \Delta N_T = - \left(\frac{R}{n} + \alpha \cdot \mu_{eff} \right) \Delta N_T, \quad (5.39)$$

where

$$\alpha = \frac{1}{\mu_{eff}^2} \frac{d\mu_{eff}}{dV_{FB}} \frac{dV_{FB}}{dN_T} \quad (5.40)$$

$$R^* = \frac{dn}{dN_T}. \quad (5.41)$$

Therefore, the spectrum density of drain current can be written as:

$$S_{I_{ds}} = I_{ds}^2 \cdot \left(\frac{R^*}{n} + \alpha \cdot \mu_{eff} \right)^2 \cdot S_{N_t}(f). \quad (5.42)$$

To evaluate α , we need to find the relationship between mobility and the interface trap density. It is widely accepted that Coulomb scattering is dominated in trap induced mobility fluctuations. The universe mobility expression is given by

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} E_{eff}^{0.3} + \frac{1}{\mu_3} E_{eff}^m \quad (5.43)$$

where μ_1, μ_2, μ_3 are mobilities limited by Coulomb scattering, phonon scattering and surface roughness, respectively, m is a fitting parameter, and $E_{eff} = 0.5 \varepsilon_{si} N$ is the effective electric field. Therefore, α can be obtain from Equation (5.43)

$$\alpha = \left(\frac{1}{3} \frac{1}{\mu_2} E_{eff}^{-2/3} + m \cdot \frac{1}{\mu_3} E_{eff}^{m-1} \right) \frac{dE_{eff}}{dN_T}. \quad (5.44)$$

To further simplify the expression, we neglect the surface roughness and phonon scattering terms and introduce two fitting parameters, resulting in

$$\alpha = \frac{1}{\mu^*} N^C \cdot R^*, \quad (5.45)$$

where μ^* and C are fitting parameters (C is temperature dependent, at room temperature C equals -1/2 [105]).

The expression of R^* can be obtained based on the surface potential solution together with Gauss's law. Applying Gauss's law we obtain:

$$V_{gf} - V_{FB}^* = \frac{-q \cdot n}{C_{ox}} + \phi_s, \quad (5.46)$$

where $V_{FB}^* = -qN_T/C_{ox}$ is the flat-band shift caused by the interface traps.

With Taylor's expansion on both sides, we have

$$-\Delta V_{FB}^* = \left(\frac{-q}{C_{ox}} \cdot \frac{dn}{d\phi_s} + 1 \right) \Delta \phi_s, \quad (5.47)$$

and the fluctuation in number of carriers is approximated as

$$\Delta n = \frac{dn}{d\phi_s} \Delta \phi_s. \quad (5.48)$$

Equations (5.47) and (5.48) lead to

$$\Delta n = - \frac{\frac{dn}{d\phi_s}}{\left(\frac{-q}{C_{ox}} \cdot \frac{dn}{d\phi_s} + 1 \right)} \Delta V_{FB}^*. \quad (5.49)$$

From (5.49), one can write

$$\frac{dn}{dV_{FB}^*} = - \frac{\frac{dn}{d\phi_s}}{\left(\frac{-q}{C_{ox}} \cdot \frac{dn}{d\phi_s} + 1 \right)}. \quad (5.50)$$

Thus,

$$R^* = \frac{dn}{dN_T} = \frac{\frac{dn}{d\phi_s}}{\frac{C_{ox}}{q} \frac{dn}{d\phi_s}}. \quad (5.51)$$

In undoped cylindrical SiNW MOSFETs, the expression of $dn/d\phi_s$ is given as:

$$\frac{dn}{d\phi_s} = \left(\frac{n}{v_{th}} + 4 \frac{\epsilon_{si}}{q \cdot R} \right) - \frac{1}{2} \cdot \left(\frac{n}{v_{th}} + 4 \frac{\epsilon_{si}}{q \cdot R} \right)^2 \frac{v_{th}}{\sqrt{4 \cdot \left(\frac{\epsilon_{si} v_{th}}{q \cdot R} \right)^2 + n \cdot \left(4 \cdot \frac{\epsilon_{si} v_{th}}{q \cdot R} + n \right)}}. \quad (5.52)$$

Figure 5.6 shows the R^* at the source end versus applied gate-source voltage V_{gs} with different oxide thickness in (a) and with different SiNW body radius in (b). It is shown that the behavior of R^* is similar to a step function. In volume inversion region, the inversion charge can be assumed independent of the oxide trap density due to the R^* approaching zero. From the volume inversion region to strong inversion region, R^* increases rapidly and approaches unity in strong inversion region.

(a)

(b)

Figure 5.6: R^* versus gate source voltage. (a) with $T_{ox}=2,3,4\text{nm}$ and $R=5\text{nm}$, $L=350\text{nm}$ (b) with $R=5,10,20\text{nm}$ and $T_{ox}=2\text{nm}$, $L=350\text{nm}$

R^* can also be derived from charge conservation. With the charge conservation concept, we have

$$\Delta Q_G + \Delta Q_T + \Delta Q_{inv} = 0, \quad (5.53)$$

where ΔQ_G , ΔQ_T , ΔQ_{inv} are the change of the gate charge, trap charge and inversion charge respectively.

Thus,

$$R^* = -\frac{dn}{dN_T} = -\frac{\Delta Q_{inv}}{\Delta Q_G + \Delta Q_{inv}}, \quad (5.54)$$

and $\Delta Q_{inv} = C_{inv} \cdot \Delta \phi_s$ and $\Delta Q_G = C_{ox} \cdot \Delta \phi_s$,

where

$$C_{inv} = \frac{dQ_{inv}}{d\phi_s}. \quad (5.55)$$

After some algebra, we obtain

$$R^* = -\frac{dn}{dN_T} = -\frac{\frac{dQ_{inv}}{d\phi_s}}{C_{ox} + \frac{dQ_{inv}}{d\phi_s}} = -\frac{\frac{dn}{d\phi_s}}{\frac{C_{ox}}{q} - \frac{dn}{d\phi_s}}. \quad (5.56)$$

Equation (5.56) is exactly the same as Equation (5.51).

To further simplify it, we may apply an approximation:

$$C_{inv} = \frac{dQ_{inv}}{d\phi_s} \approx \frac{dQ_{inv}}{dV_C} = v_{th} \cdot Q_{inv}. \quad (5.57)$$

Substituting Equation (5.57) into Equation (5.56), a simple expression of R^* is obtained as

$$R^* \approx -\frac{v_{th} \cdot Q_{inv}}{C_{ox} + v_{th} \cdot Q_{inv}}. \quad (5.58)$$

Introducing a fitting parameter Q^* into Equation (5.59), we have

$$R^* = -\frac{Q_{inv}}{Q^* + Q_{inv}}. \quad (5.59)$$

Figure 5.7: R versus gate source voltage with different radius=5,10,20nm, $L=350\text{nm}$ and $T_{ox}=2\text{nm}$.

Figure 5.7 shows the R^* calculated using Equation (5.59) with the fitting parameter $Q^*=7.2998 \times 10^{-8}$. Similar to the one calculated with Equations (5.51) and (5.52), the behavior of R^* is like a step function. The R^* also approaches unity in strong inversion region and zero in volume inversion region. And the slope between volume

inversion region and strong inversion region depends on the fitting parameter. Equation (5.59) is integrable although a fitting parameter is required.

The model has been verified with experimental data. The NMOS undoped SiNW MOSFET is fabricated with a conventional poly-silicon gate. The thickness of the silicon oxide is 4nm, the radius of the silicon nanowire is 5nm, and the gate length of the device is 350nm. The $1/f$ noise measurements were performed at $f=10\text{Hz}$. The comparison of drain current and transconductance are shown in Fig. 5.8 and Fig. 5.9, with good agreement.

Figure 5.8: Drain current versus gate source voltage at $V_{ds}=50\text{mV}$.

Figure 5.9: Transconductance versus gate source voltage at $V_{ds}=50\text{mV}$.

Figure 5.10: Comparison of the gate-voltage referred noise spectral density.

Figure 5.11: Spectral density of drain current noise versus V_{gs} .

Figure 5.10 shows the comparison of gate-voltage referred noise spectral density versus V_{gs} at $V_{ds}=50mV$. Symbols are measured at $f=10Hz$ and line is the model result. The curve shows that the correlated mobility fluctuation is significant and can not be ignored. Figure 5.11 shows the normalized drain current noise spectral density versus V_{gs} at $f=10Hz$ and $V_{ds}=50mV$. Good agreement is shown in both linear and logarithmic scale. In linear scale, it decreases exponentially at low V_{gs} and reaches a plateau at high V_{gs} . The curve shows similar behavior of $(G_m/I_{ds})^2$, which indicates that the number fluctuation is the dominated mechanism in strong inversion region.

5.5. Summary

In this chapter, a thermal noise model valid for all operation regions is first described. And then the g-r noise is discussed, a novel equation of the g-r noise spectral density is derived in which the g-r process is described by the SRH model. Rather than assuming a constant as in most existing compact models, the interface-trap charge is expressed as a function of the gate voltage and surface potential. The flicker noise model contain two piece-wise models, one for volume inversion and the other for strong inversion. In the proposal model, the mobility fluctuation is accepted to be the dominant mechanism contributing to flicker noise in volume inversion. In strong inversion region, a number fluctuation model is developed based on the g-r noise model. Lastly, the flicker model is verified against with the measurement data with good agreement.

CHAPTER 6: CURRENT MISMATCH MODEL OF UNDOPE SILICON NANOWIRE MOSFETs

No two transistors are identical, and the difference can be observed if closely examined. Transistor mismatch is caused by the stochastic parameter fluctuations due to microscopic fluctuations. Mismatch is becoming more important for both analog and digital IC design with scaling down of transistor dimensions. Depending on the correlation distances, mismatch sources can be classified in two categories: local and global. In this work, only the local mismatch sources with short correlation distances are studied. Current factor and threshold voltage are taken as two mismatch parameters in most existing drain current mismatch models. However, the threshold voltage is not a variable in the drain current equation of surface potential based models. Therefore, new mismatch models are required to be developed for surface potential based models. In this chapter, we present a simple and physical model that accurately describes the mismatch in drain current in all operation regions. And the model has been verified with Monte Carlo simulation results.

6.1. Introduction

It is widely recognized that random device mismatch plays an important role in the design of accurate analog circuits [106]. Also, for digital circuits, the mismatch is becoming more important with transistor dimensions scaling down. The variation will set ultimate limits on the scaling of MOSFETs.

Variation can be represented by mismatch parameters at different levels [107]. Modeling at the level of process parameters and modeling at level of spice parameters are both feasible for circuit simulation. Modeling at the level of process parameters maybe a good way to model mismatch due to most process parameters being uncorrelated. The large number of process parameters will lead to a significantly complex mismatch model. Modeling at the level of spice parameters is the most common way in mismatch modeling and is adopted in the proposal model.

Parameter mismatch has been extensively studied since the first matching study on capacitors [108]. At that time, random edge variations and random variation of oxide thickness were considered as mismatch sources. A general parameter mismatch variance model was developed by Pelgrom et al. [109], the variance of mismatch is found to be inversely proportional to device area. It is widely used in analog circuit design due to its simplicity.

In this chapter, the impact of the mismatch in parameters on the drain current is studied. It can be achieved by either sensitivity analysis or derivative of the drain current

model. For analytical expressions of the mismatch model, the derivative of drain current is derived to model the drain current mismatch in our work.

6.2. Random Mismatch in Undoped SiNW MOSFETs

In undoped SiNW MOSFETs, due to very low unintentional channel doping, body doping fluctuation is not a dominant factor. Oxide thickness is a well controlled variable in modern process technologies, and not an important factor in MOSFETs [110]. Oxide granularity, oxide fixed charge, surface roughness scattering, edge roughness, and gate doping are supposed to be the main origins of random fluctuations in undoped cylindrical GAA SiNW MOSFETs. The mismatch of drain current is caused mostly by these random mismatch sources, these mismatch sources will contribute to V_{gf} mismatch and mobility mismatch.

In general, the cross-section of the cylindrical nanowire silicon body will not be a perfect circle due to the limit of process technology. It always exhibits a certain roughness at silicon body edge and the silicon body cross-section is approximated as a circle. Thus, the radius of the silicon body can only be an effective radius due to the edge roughness of the silicon body. In cylindrical SiNW MOSFETs, the mismatch of radius will cause the mismatch of the gate oxide capacitance due to the gate oxide capacitance being a function of radius. And the mismatch of the radius also causes the mismatch in the surface potential. The mismatch of the radius is one important source to the drain current mismatch.

There are three scattering mechanisms considered in our low field mobility model: Coulomb scattering, surface roughness scattering and phonon scattering. The mobility

degradation due to Coulomb scattering is not related to the electric field or fixed oxide charge. Both surface roughness scattering and phonon scattering are dependent on the effective electric field, more fluctuations can arise from the electric field. Experiment results show that the low field mobility decreases hyperbolically while increases the fixed oxide charge density, and in previous chapter we also show the relationship between fixed oxide charge and low field mobility. The fluctuation of the electric field also depends on the fixed oxide charge and radius. Therefore, the mobility fluctuation is dependent on fixed oxide charge and radius.

The variation of V_{gf} may be due to variation in process parameters: radius, variation in fixed oxide charge, variation in gate oxide capacitance, and variation in gate-silicon work-function difference. In our drain current model, the DIBL and threshold voltage roll-off are included in the model through a threshold voltage shift. In calculating the impact of V_{gf} mismatch on the drain current, it is assumed that the V_{gf} is the effective V_{gf} ($V_g - V_{FB} - \Delta V_T$). Therefore, the mismatch of the threshold voltage is included through the mismatch of threshold voltage shift.

In this model, nano-wire radius mismatch ΔR , mobility mismatch $\Delta\mu$, and flatband shifted gate voltage mismatch ΔV_{gf} are assumed implicitly as three main factors affecting the device mismatch. Several models have been developed to model device geometry dependence of the variance of mismatch in a certain parameter ($\sigma^2_{\Delta P}$) and the correlation factors between parameters ($\rho(\Delta P_1, \Delta P_2)$). In conventional MOSFETs, Pelgrom gives [109]

$$\sigma^2(\Delta P) = \frac{A_p^2}{WL}, \quad (6.1)$$

where A_p is a constant to be determined from experimental data, W is the width of the conventional MOSFET. This simple equation shows the variance of mismatch parameter is inversely proportional to device area. For SiNW MOSFETs, it is appropriate to replace W with radius R in Equation (6.1). Equation (6.1) is valid for long channel devices. For short channel devices, it needs some corrections. The empirical equation is suggested in [111]:

$$\sigma^2(\Delta P) = \frac{A_p^2}{RL} + \frac{A_{L,P}^2}{RL^2} + \frac{A_{R,P}^2}{R^2L} + \frac{A_{RL,P}^2}{R^2L^2}, \quad (6.2)$$

where $A_{L,P}$, $A_{R,P}$ and $A_{RL,P}$ are constants to be determined.

6.3. Drain Current Mismatch Model

To study the mismatch of drain current, a simple yet scalable drain current model is required due to the requirement in deriving parameter sensitivities. Usually, the piece-wise drain current model is used for mismatch studies, in which different drain current models are used in different operation regions. It is apparent that it can not provide a unified drain current mismatch model for all operation regions. In our drain current model, only a few parameters are required and most of those parameters are uncorrelated. Therefore, the single piece drain current model, as described in chapters 2 and 3, valid in all operation regions is used in drain current mismatch model, which is rewritten below

$$I_{ds} = \mu_{eff} \frac{2\pi RC_{ox}}{L} \left[(V_{gfeff} + 2v_{th}) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) + v_{th} C_R \ln \left(\frac{V_{gfeff} - \phi_{sL} + C_R}{V_{gfeff} - \phi_{s0} + C_R} \right) \right], \quad (6.3)$$

where μ_{eff} is given by equation (3.26) and

$$V_{gfeff} = V_{gf} + \Delta V_T, \quad (6.4)$$

ΔV_T is the threshold voltage shift due to barrier lowering.

In drain current mismatch modeling, it is safe to assume that the mismatch in a parameter ΔP is much smaller than the parameter value P . For a pair of transistors M1 and M2, I_1 and I_2 are the drain currents of M1 and M2, respectively, the impact of mismatch in parameters on the drain current $\Delta I = I_1 - I_2$ can be calculated by first order Taylor approximation:

$$\frac{\Delta I}{I} \approx \frac{1}{I} \frac{\partial I}{\partial P_1} \Delta P_1 + \frac{1}{I} \frac{\partial I}{\partial P_2} \Delta P_2 + \dots + \frac{1}{I} \frac{\partial I}{\partial P_n} \Delta P_n. \quad (6.5)$$

The distribution of the drain current difference can be safely assumed as a normal (Gauss) distribution. Thus, the distribution can be described by standard deviation ($\sigma_{\Delta I/I}$).

It is obtained from Equation (6.5):

$$\sigma_{\Delta I/I}^2 \approx \left(\frac{1}{I} \frac{\partial I}{\partial P_1} \right)^2 \sigma_{P_1}^2 + \left(\frac{1}{I} \frac{\partial I}{\partial P_2} \right)^2 \sigma_{P_2}^2 + \dots + \left(\frac{1}{I} \frac{\partial I}{\partial P_n} \right)^2 \sigma_{P_n}^2 + \text{Correlation Terms} , \quad (6.6)$$

where σ_P is the standard deviation of ΔP , the square of standard deviation σ_P^2 is the variance.

In most mismatch models [112-114], the drain current model is a threshold voltage based model, and mismatch in threshold voltage and mismatch in current factor are assumed as the sources of mismatch in drain current. In our mismatch model, the drain current model is surface potential based model in which threshold voltage is not taken as a variable. And the surface potential should not be considered as a mismatch parameter in view of the fact that surface potential is highly correlated to other parameters. Therefore, for SiNW MOSFETs the mismatch in drain current is assumed to result from mismatch in process variable ΔR , mismatch in mobility $\Delta \mu$ and mismatch in flat-band shifted gate voltage ΔV_{gf} . Mismatch in drain current is achieved simply by first order sensitivity analysis on a simple drain current model. Follows Equation (6.5) the general model for mismatch in the drain current is given as:

$$\frac{\Delta I_{ds}}{I_{ds}} = \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial R} \Delta R + \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial V_{gf}} \Delta V_{gf} + \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial \mu} \Delta \mu . \quad (6.7)$$

In this work, we assume the mismatch parameters are the same in all operation regions. The single piece drain current model is also valid for all operation regions. Therefore, the drain current mismatch model is valid for all operation regions.

To calculate the impact of radius mismatch on the drain current, we ignore the impact of radius mismatch on surface potential to avoid the unnecessary complexity. And two intermediate variables are introduced into the drain current equation (6.3):

$$I_{ds} = \mu_{eff} \alpha \left[(V_{gfeff} + 2v_{th}) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) + \chi \right], \quad (6.8)$$

where α and χ are given by:

$$\alpha = \frac{2\pi RC_{ox}}{L}, \quad (6.9)$$

$$\chi = v_{th} C_R \ln \left(\frac{V_{gfeff} - \phi_{sL} + C_R}{V_{gfeff} - \phi_{s0} + C_R} \right), \quad (6.10)$$

respectively. In the gate lithography process, during exposure of the resist as limited by Poisson statistics on the number of photons, it will exhibit roughness, which causes variations in the gate length L [115]. The variation of L will also affect the mismatch of drain current. In cylindrical SiNW MOSFETs, L is usually much larger than R and the process variations in L is better controlled than R variations. Thus, the contribution of mismatch in L is ignored in this work. However, it can be included in model following the similar approach if necessary.

Using Equation (6.5), it follows that:

$$\begin{aligned} \frac{\Delta I_{ds}}{I_{ds}} \Big|_{\Delta \alpha} &= \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial \alpha} \cdot \Delta \alpha \\ &= \frac{\mu_{eff} \left[(V_{gfeff} + 2v_{th}) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) \right] + \frac{\partial(\alpha\chi)}{\alpha}}{I_{ds}} \cdot \Delta \alpha, \\ &\approx \frac{\mu_{eff} \left[(V_{gfeff} + 2v_{th}) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) \right]}{I_{ds}} \cdot \Delta \alpha \end{aligned} \quad (6.11)$$

As discussed in previous chapters, the contribution of the χ term to the drain current is very small compared to other terms. To obtain a simple close-form equation suitable to be implemented into a circuit simulator, we simply drop the logarithm term χ in the current equation since its contribution to drain current's derivatives is negligible.

The derivative of α with respect to R is derived as

$$\begin{aligned}
 \frac{\partial \alpha}{\partial R} &= \frac{2\pi C_{ox}}{L} + \frac{2\pi R}{L} \left(\frac{\epsilon_{ox} T_{ox}}{R^3 \ln \left(1 + \frac{T_{ox}}{R} \right)^2 \left(1 + \frac{T_{ox}}{R} \right)} - \frac{\epsilon_{ox}}{R^2 \ln \left(1 + \frac{T_{ox}}{R} \right)} \right) \\
 &= \frac{2\pi C_{ox}}{L} + \frac{2\pi}{L} \left(\frac{C_{ox}^2 T_{ox}}{\epsilon_{ox} \left(1 + \frac{T_{ox}}{R} \right)} - C_{ox} \right) \\
 &= \frac{2\pi C_{ox}^2}{L} \frac{T_{ox}}{\epsilon_{ox} \left(1 + \frac{T_{ox}}{R} \right)}
 \end{aligned} \tag{6.12}$$

Combining Equations (6.11) and (6.12), it gives

$$\begin{aligned}
 \frac{\Delta I_{ds}}{I_{ds}} \Big|_{\Delta R} &= \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial \alpha} \cdot \frac{\partial \alpha}{\partial R} \Delta R \\
 &= \frac{2\pi C_{ox}^2}{L} \cdot \frac{T_{ox}}{\epsilon_{ox} \left(1 + \frac{T_{ox}}{R} \right)} \cdot \frac{\mu_{eff} \left[\left(V_{gfeff} + 2v_{th} \right) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) \right]}{I_{ds}} \cdot \Delta R
 \end{aligned} \tag{6.13}$$

Figure 6.1 Mismatch for transistor pair in drain current with R mismatch

Figure 6.1 plots the drain current mismatch for a transistor pair $M1$ ($R=10\text{nm}$), $M2$ ($R=9.85\text{nm}$). The symbols are the numerical device result of the two drain current mismatch and the lines are the mismatch model result with Equation (6.13). The numerical results are obtained from MEDICI simulations with a pair of transistors in which their radius is slightly different. Good agreement is observed in all regions including linear, saturation and volume inversion regions. Note that the mismatch of drain current decreases as V_{gs} increases.

A detailed description of the mobility is required to evaluate the impact of mismatch in mobility on the drain current. In our drain current model, the low field mobility μ_s is calculated with Matthiessen's rule. Due to the lateral electric field as well as considering the velocity saturation effect, the mobility degradation is given as:

$$\mu_{eff0} = \frac{\mu_s}{\left(1 + \left(\frac{\delta_0 V_{ds}}{E_{sat} L}\right)^2\right)^{1/2}}. \quad (6.14)$$

In short channel devices, the channel length modulation effect and series resistance are included in the drain current model with an effective mobility:

$$\mu_{eff} = \frac{\mu_{eff0}}{1 + R_{sd} \frac{2\pi R}{L} \mu_{eff0} C_{ox} \cdot \left[\left(V_{gfeff} + 2v_{th} \right) - \overline{\phi_s} \right]}. \quad (6.15)$$

Using the Equation (6.5), we obtain

$$\begin{aligned} \frac{\Delta I_{ds}}{I_{ds}} \Big|_{\Delta \mu_{eff}} &= \frac{1}{I_{ds}} \frac{\partial I_{ds}}{\partial \mu_{eff}} \Delta \mu_{eff} \\ &= \frac{1}{I_{ds}} \alpha \left[\left(V_{gfeff} + 2v_{th} \right) \cdot (\phi_{sL} - \phi_{s0}) - \frac{1}{2} (\phi_{sL}^2 - \phi_{s0}^2) + \chi \right] \Delta \mu_{eff}. \end{aligned} \quad (6.16)$$

The derivative of the high field mobility with respect to the low field mobility is given as

$$\frac{\partial \mu_{eff}}{\partial \mu_{eff0}} = - \frac{1}{\left(1 + R_{sd} \frac{2\pi R}{L} \mu_{eff0} C_{ox} \cdot \left[\left(V_{gfeff} + 2v_{th} \right) - \overline{\phi_s} \right] \right)^2} = \frac{\mu_{eff}^2}{\mu_{eff0}^2}. \quad (6.17)$$

And then, the derivative of μ_{eff} with respect to μ_s is obtained:

$$\begin{aligned} \frac{\partial \mu_{eff}}{\partial \mu_s} &= \frac{\partial \mu_{eff}}{\partial \mu_{eff0}} \cdot \frac{\partial \mu_{eff0}}{\partial \mu_s}^{-1/2} = \frac{\mu_{eff}^2}{\mu_{eff0}^2} \frac{1}{\left(1 + \left(\frac{\delta_0 V_{ds}}{E_{sat} L_{eff}} \right)^2 \right)^{1/2}} \\ &= \frac{\mu_{eff}^2}{\mu_s^2} \left(1 + \left(\frac{\delta_0 V_{ds}}{E_{sat} L_{eff}} \right)^2 \right)^{1/2}. \end{aligned} \quad (6.18)$$

With Equations (6.16)-(6.18), it follows that

$$\left. \frac{\Delta I_{ds}}{I_{ds}} \right|_{\Delta \mu_s} = \frac{\mu_{eff}}{\mu_s^2} \left(1 + \left(\frac{\delta_0 V_{ds}}{E_{satn} L_{eff}} \right)^2 \right)^{1/2} \Delta \mu_s. \quad (6.19)$$

In calculating the impact of flat-band shifted gate voltage on the drain current, it is implicitly assumed that the mismatch parameter is the effective flat-band shifted gate voltage, in which the threshold voltage shift is involved:

$$V_{gfeff} = V_{gf} - \Delta V_T, \quad (6.20)$$

where ΔV_T is the threshold voltage shift caused by barrier lowering. Thus, the mismatch in threshold voltage shift is included in drain current mismatch model. As described in chapter 3, the drain induced barrier lowering, threshold voltage roll-off and subthreshold slope degradation effects are included in the model through the threshold voltage shift.

Applying Equation (6.5), it yields:

$$\left. \frac{\Delta I_{ds}}{I_{ds}} \right|_{\Delta V_{gf}} = \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial V_{gfeff}} \cdot \Delta V_{gf}, \quad (6.21)$$

where

$$\begin{aligned} \frac{\partial I_{ds}}{\partial V_{gfeff}} &= g_m \approx \left[\mu_{eff} \alpha \left[(\phi_{sL} - \phi_{s0}) + \frac{\partial \chi}{\partial V_{gf}} \right] \right] \\ &\approx \mu_{eff} \alpha [(\phi_{sL} - \phi_{s0})] \end{aligned} \quad (6.22)$$

The complete mismatch drain current model is obtained by combining the contributions due to mismatch in radius, mismatch in mobility, and mismatch in flat-band shifted gate voltage:

$$\frac{\Delta I_{ds}}{I_{ds}} = \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial R} \Delta R + \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial V_{gf}} \Delta V_{gf} + \frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial \mu_s} \Delta \mu_s. \quad (6.23)$$

Rather than using the piece-wise drain current equation, in our model the single piece drain current is used. Thus, the mismatch model is valid in all regions.

6.4. Mismatch Model Verification

To validate the mismatch drain current model, our model is verified against numerical results. The device with parameters $T_{ox} = 2nm$, $L=1\mu m$, $R=10nm$, $V_{FB}=-0.2V$, and $\mu_s=300cm^2V^{-1}s^{-1}$ is taken as nominal parameters in this study. To validate the current mismatch model, another device with different parameters ($R=9.5nm$, $V_{FB}=-0.195V$, $\mu_s=290cm^2V^{-1}s^{-1}$) is evaluated as well as the nominal device. The current mismatch in all regions are evaluated by comparing the two devices' drain current calculated with our drain current model and the mismatch parameters ΔR , ΔV_{FB} , and $\Delta\mu$ are extracted with least-squares optimization method to fit Equation (6.22) [116].

Figure 6.2: Relative drain current mismatch for transistor pair.

Figure 6.3: Relative transconductance mismatch for transistor pair.

Figure 6.4: Relative Mismatch for transistor pair in drain current versus drain-source voltage.

Figure 6.2 shows the comparison on mismatch in the drain current for matched pair of transistors versus gate-source voltage (0-1.2V), and for two different drain-source voltages 0.05V and 1.2V. Symbols are numerical results and lines are model results. Figure 6.3 shows the mismatch in transconductance for the transistor pair. Mismatch in transconductance is given as:

$$\Delta G_m = \frac{d(\Delta I_{ds})}{dV_{gs}}. \quad (6.24)$$

Figure 6.4 shows the mismatch in drain current versus drain-source voltage (0-1.2V) with different gate-source voltages (0.1V, 0.3V, 0.6V, 0.9V and 1.2V). Figures 6.2, 6.3 and 6.4 show that our model, which is a single piece equation, can capture the drain current mismatch and transconductance mismatch in all operation regions. Decrease in the applied gate voltage in volume inversion or increase in strong inversion region, the current mismatch will reach a plateau roughly about 27% and 5%, respectively. It is seen that the mismatch in drain current will decrease if the applied gate voltage increases from volume inversion to strong inversion. In the design of precision circuits, to improve transistors matching, we can increase the device geometry dimension (L or R) or the applied voltage. However, the transistor power also will increase with increasing applied voltage. In the volume inversion region, the mismatching is almost constant due to short channel effects being less severe. And it is also observed in Figures 6.2 and 6.3, the mismatch in volume inversion is independent of the drain-source voltage. Figure 6.4 shows drain current mismatch is slightly affected by V_{ds} in volume inversion and strong inversion. In the region between volume inversion and strong inversion, mismatch will increase from linear region to saturation region.

Figure 6.5: Relative mismatch for the transistor pair in drain current versus gate-source voltage.

In Figure 6.5, the gate length of the transistor pair is 100nm and 50nm respectively, the mismatch behavior is verified in volume inversion region and strong inversion region. In strong inversion region the behavior of mismatch in short channel devices is similar to that in long channel devices, the mismatch will decrease with increasing applied gate voltage. When the short channel effects become significant, the mismatch behavior in volume inversion region will be different from that in long channel devices. It will not reach a plateau; rather, it keeps increasing with decreasing applied gate voltage. And it is interesting to note that the mismatch behavior is similar to the low frequency noise behavior in both volume inversion and strong inversion region, as mismatch is also known as “spatial noise”.

In order to study the standard derivation and variance of parameters' mismatch in the drain current, a Monte Carlo simulation is performed. Monte Carlo simulation relies on repeated random sampling to compute their results. Individual parameters (R , V_{FB} , μ_s) are assumed to follow a Gaussian distribution with the mean (at nominal value) and 3σ variations (within 12%), and random sampling is performed by the Monte Carlo method for a total of $N=1,000$ samples. And each sample's mismatch parameters are extracted individually in saturation region. The statistics of the mismatch parameters are evaluated based on the mismatch parameters extracted with statistical techniques

$$\frac{\sigma_{I_{ds}}^2}{I_{ds}^2} = \left(\frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial R} \right)^2 \sigma^2(R) + \left(\frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial V_{gf}} \right)^2 \sigma^2(V_{gf}) + \left(\frac{1}{I_{ds}} \cdot \frac{\partial I_{ds}}{\partial \mu} \right)^2 \sigma^2(\mu) + \text{Correlation Terms.} \quad (6.25)$$

Figure 6.6: Comparison of Monte Carlo simulation and predicted mismatch in the drain current versus gate-source voltage, $L=1\mu m$.

Figure 6.6 shows the comparison of Monte Carlo simulation and model, symbols

are Monte Carlo simulation results and lines are model results. Excellent agreement between Monte Carlo and model results verify the model's validity. Similar to the mismatch of a transistor pair, the variance is almost constant in volume inversion region and strong inversion region.

Figure 6.7: Histogram plots of the drain current with different bias condition.

(a)

(b)

Figure 6.8: Comparison of Monte Carlo simulation and predicted mismatch in the drain current versus gate-source voltage, $L=100nm$.

The normality of the drain current is checked for the transistors with $L=100nm$. Figure 6.7 shows the histogram plots of drain current with different bias conditions and the fitted normal probability distribution curves. It is seen that the drain current exactly follows the normal distribution from volume inversion to strong inversion. Figure 6.8 shows the good agreement between Monte Carlo and model results on the variance of drain current in linear and saturation regions.

Figure 6.9: Comparison of Monte Carlo simulation and predicted mismatch in the drain current versus gate-source voltage, $L=1um$.

In most cases, it is appropriate to assume that the mismatch parameters follow a Gaussian distribution. However, the proposed model is not limited to those mismatch parameters only following a Gaussian distribution. Figure 6.9 shows the comparison of

the Monte Carlo simulation and the model results with mismatch parameters following the uniform distribution (vary from 99% to 101%). The good agreement is also observed.

The model has also been verified against TCAD simulation. The TCAD simulations were performed with 20 SiNW MOSFETs in which the device parameters such as the radius, mobility, and gate work-function are varied according to a Gaussian distribution as well as $L=1\mu m$, $T_{ox}=2nm$, with $V_{ds}=0.1V$ and $V_{ds}=1.2V$, respectively. The 20 devices' drain currents versus gate-source voltage with $V_{ds}=1.2V$ are shown in Figure 6.10. The mismatch of the drain current caused by the parameter mismatch is observed in the plot, the drain current mismatch increases from volume inversion region to strong inversion region. The comparison of the standard derivation of the drain current mismatch between Monte Carlo simulation and the proposed mismatch model is shown in Figure 6.11. The symbols are Monte Carlo results based on TCAD simulations and the line is the model results. The good agreement is observed with RMS error between the Monte Carlo and proposed model results being less than 1%. The error between model result and Monte Carlo result is almost zero in strong inversion region. The curves presented in Figure 6.12 show similar behavior to that seen in the drain current mismatch of the transistor pair, it reaches a plateau in the volume inversion region and the relative drain current mismatch reaches the maximum value. It also shows that the drain current mismatch can be suppressed by increasing the applied gate voltage. However, the power consumption also will increase with increasing applied gate voltage. In the region between volume inversion and strong inversion, different from the gate voltage, the increase in the drain voltage will result in a larger mismatch in drain current. In strong

inversion region, once the applied bias is determined the mismatch of the drain current can be estimated using the proposed model. With this approach we can avoid the Monte Carlo analysis to save the simulation time since Monte Carlo analysis requires numerous simulations. This study represents a first step towards “compact statistical modeling”.

Figure 6.10: TCAD drain current simulation results of 20 devices

Figure 6.11: Comparison of standard deviation of drain current between TCAD Monte Carlo simulation and model

Monte Carlo simulation is stochastic, different set of statistics would result if we repeat the simulation. To reduce the difference between the repeated simulations it needs to increase the sample size in Monte Carlo simulations. On the other hand, increasing the sample size will also increase the computational time. Therefore, there is a common question being asked for Monte Carlo simulation: how large the sample size is adequate. It is supposed to depend on the required accuracy. Figure 6.12 shows the comparison between the model result and Monte Carlo simulations, symbols are Monte Carlo simulation results and lines are model results. Good agreement is observed with sample size from 10 to 10,000. In Figure 6.13, the symbols are the Monte Carlo simulation with 10,000 samples and the lines are model results with mismatch parameter extracted from 10 to 10,000 samples. The Monte Carlo simulation with 10,000 samples is taken as a reference. It shows the difference between Monte Carlo simulation and the model results

with 1,000, 2,000 and 10,000 sample sizes are small enough to be ignored. The Root Mean Square (RMS) error is shown in Figure 6.14. The RMS errors are less than 4% in all model results with sample size varying from 10 to 10,000. And it also shows that RMS error will decrease if the sample size increases. The main trend of the RMS error is that it will decrease if the sample size is increased.

(1)

(2)

(3)

(4)

(5)

(6)

(7)

(8)

(9)

Figure 6.12. Comparison of standard deviation of drain current with different sample sizes

Figure 6.13: Comparison of standard derivation of drain current between Monte Carlo simulation and model

Figure 6.14: Root Mean Square error versus samples size

6.5. Summary

In this chapter we presented a drain current mismatch model for undoped SiNW MOSFET devices. The random mismatch sources that lead to mismatch in drain current are first discussed. And mismatch in radius, mismatch in flat-band shifted gate voltage, and mismatch in mobility are considered as three most important mismatch sources. The analytical mismatch model is developed based on our single piece drain current model which is valid in all operation regions. To validate the mismatch model, Monte Carlo simulations are performed and good agreement is seen in the comparison of variance between Monte Carlo simulations and mismatch model results.

CHAPTER 7: CONCLUSION AND RECOMMENDATION

This chapter summaries the conclusion and suggestions for future research work in related areas.

7.1. Summary and Conclusion

In this work, we present a complete compact model for undoped surrounding-gate silicon nanowire MOSFETs. In five chapters, we have presented the modeling of the I-V model for long channel SiNW MOSFETs, I-V model for short channel SiNW MOSFETs, C-V for SiNW MOSFETs, noise for SiNW MOSFETs, and mismatch in drain current. This includes all major areas of compact modeling. The overall conclusions are presented chapter by chapter.

Chapter 2: *Intrinsic Long Channel Drain Current Model of Undoped Silicon Nanowire MOSFETs*. A physics-based single-piece surface potential based drain current model has been developed for long channel SiNW MOSFETs without employing charge sheet approach. Both iterative and analytical approximation surface potentials with accuracy in the nV level have been derived for the first time in undoped cylindrical SiNW

MOSFETs. This results in a model that matches TCAD simulations excellently without any fitting parameters in all operation regions.

Chapter 3: *Short Channel Drain Current Model of Undoped Silicon Nanowire MOSFETs*. Modeling of mobility degradation and short channel effects such as velocity saturation, channel length modulation, drain induced barriers lowering, etc., are included into the core I-V model. A concise threshold voltage equation has been derived and verified with TCAD simulations. By solving the 2D Poisson's equation using superposition method, the threshold voltage shift due to barrier lowering is obtained.

Chapter 4: *Capacitance Voltage Model of Undoped Silicon Nanowire MOSFETs*. By using an approximation in the drain current equation, a simple, accurate and continuous capacitance model has been developed. The model is valid from volume inversion region to strong inversion region as well as from linear region to saturation region. With a simple modification on the surface potential at flat-band we solved the singularity problem caused by ignoring the holes.

Chapter 5: *Noise Model of Undoped Silicon Nanowire MOSFETs*. We derived the model to calculate the spectral density of channel thermal noise. A new generation-recombination noise model is developed in which the generation-recombination process is described by the SRH model and the interface trap charge is a function of inversion charge. The flicker noise in volume inversion region is modeled by the mobility fluctuation model and verified with measurements. A strong inversion flicker noise model is developed according to the number fluctuation theory.

Chapter 6: *Current Mismatch Model of Undoped Silicon Nanowire MOSFETs.*

We discussed the mismatch sources in undoped SiNW MOSFETs. The impact of mismatch in radius, mobility and flat-band shifted gate voltage on the drain current is modeled. The validation of drain current mismatch shows that it is valid in all regions.

7.2. Recommendations for Future Work

The following topics are recommended for future research.

1. Investigate the mobility in undoped silicon channel of nano scale SiNW MOSFETs.
The universal mobility model, which is an empirical model, is employed in our model. When the gate length is shorter than 10nm the quantum effects become significant, the drift mobility might be inappropriate. Therefore, developing the mobility model in undoped silicon channel considering quantum effects will be a very interesting topic. However, in our model the drain current equation is a drift-diffusion equation and a quantum correction is required to model the quantum transport.
2. Develop high frequency model for RF circuit design. The proposed model is limited to quasi-static conditions. RF IC applications receive more and more interest in industries, in which a high frequency model is required. This work can be continued to include the non-quasi-static model and the RF parasitic effects. Moreover,

parameter extraction from RF measurement is also a very interesting area for future research.

3. Investigate mismatch properties on small signal. In the mismatch model we only consider the drain current mismatch. Small signal parameters such as capacitances, transconductances are important in analog circuit design. The mismatch properties of small signal parameters are very interesting to be modeled.
4. Develop a unified flicker noise model from volume inversion to strong inversion and the interface trap relationship with applied bias. The mobility fluctuation model and number fluctuation model should be seen in a “and-and” not a “either-or” scenario. It needs experimental data to determine the fitting parameter to link the two piece wise model to acquire a unified model in all regions. Therefore, experimental study of flicker noise in undoped SiNW MOSFETs from volume inversion region to strong inversion region is an interesting research area. In the model the interface trap charge is modeled as a function of gate voltage and surface potential. However, it has not been validated with experiments. Therefore, experimental study on the relationship between interface trap charges and gate voltage is also an interesting topic.
5. Investigate the interface trap in undoped SiNW MOSFETs. Interface traps along the surface channel region are directly related to transistor reliability, endurance and standby power dissipation, critical to device performance. In existing compact models the interface trap charge is considered as a constant in all bias conditions and only be

included in the flat-band voltage. It will be very interesting to study the impact of interface trap in drain current, flicker noise, standby power dissipation and reliability.

6. Implementation of the proposal model into a SPICE simulator for investigation of SiNW MOSFETs in IC circuit design. Before implementation into SPICE simulator, the model can't be used in circuit design. As we have developed IV, CV and noise models which are required in SPICE simulation, the model can be implemented in SPICE simulator with C programming language. Or in a more efficient way, the model can be implemented using Verilog-A hardware description language which is supported in most SPICE simulators on the market. Different with the implementation in C programming language, Verilog-A implementation does not require calculating the partial derivatives of currents and charges. Therefore, model implementation in Verilog-A is very efficient. After the model be implemented in SPICE simulator, it will be very interesting to study the SiNW MOSFETs application in circuit design, especially in the low power circuit design because of its low leakage current.

Author's Publications

Major Author:

1. S. H. Lin, X. Zhou, G. H. See1, Z. M. Zhu, G. H. Lim, C. Q. Wei, G. J. Zhu, Z. H., Yao, X. F. Wang, M. Yee, L. N. Zhao, Z. F. Hou, L. K. Ang, T. S. Lee, W. Chandra, "A Rigorous Surface-Potential-Based I-V Model for Undoped Cylindrical Nanowire MOSFETs," *Proc. of the 7th International Conference on Nanotechnology (IEEE-Nano2007)*, Hong Kong, Aug. 2-5, 2007, Vol. 3, pp. 889-892.
2. S. H. Lin, X. Zhou, G. H. See, G. J. Zhu, C. Q. Wei, J. B. Zhang, and Z. H. Chen, "A Simple, Accurate Capacitance-Voltage Model of Undoped Silicon Nanowire MOSFETs," *Proc. of the 12th International Conference on Modeling and Simulation of Microsystems (WCM-Nanotech2009)*, Houston, TX, May 2009, Vol. 3, pp. 643-646.
3. X. Zhou, S. H. Lin, and M. K. Srikanth, "Statistical Compact Modeling for Emerging Nanowire / FinFET Mismatch and Variance Studies," (Invited Paper), *Proc. of the 6th International Conference on Materials for Advanced Technologies (ICMAT2011)*, Symposium W: Reliability and Variability of Emerging Devices for Future Technologies and ULSI Circuits and Systems, Singapore, June 2011, Paper W6-2.
4. S. H. Lin, X. Zhou, Z. H. Chen, M. K. Srikanth, and J. B. Zhang, "Hot-Carrier-Induced Current Degradation in Deep Sub-Micron MOSFETs from Subthreshold to Strong Inversion Region," *Proc. Nanotech (WCM-Nanotech2011)*, Boston, MA, Jun. 2011, vol. 2, pp. 806-809.

Co-author:

1. G. J. Zhu, G. H. See, S. H. Lin, and X. Zhou, "'Ground-Referenced" Model for Three-Terminal Symmetric Double-Gate MOSFETs with Source/Drain Symmetry," *IEEE Trans. Electron Devices*, Vol. 55, No. 9, pp. 2526-2530, Sep. 2008.
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3. X. Zhou, G. H. See, G. J. Zhu, S. H. Lin, C. Q. Wei, and J. B. Zhang, "Unified Regional Modeling Approach to Emerging Multiple-Gate/Nanowire MOSFETs," (Invited Paper), *Proc. of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT2008)*, Beijing, China, Oct. 20-23, 2008, Paper B1.2.
4. G. J. Zhu, X. Zhou, G. H. See, S. H. Lin, C. Q. Wei, and J. B. Zhang, "A Unified Compact Model for FinFET and Silicon Nanowire MOSFETs," *Proc. of the 12th International Conference on Modeling and Simulation of Microsystems (WCM-Nanotech2009)*, Houston, TX, May 2009, Vol. 3, pp. 588-591.
5. X. Zhou, G. J. Zhu, M. K. Srikanth, R. Selvakumar, Y. F. Yan, W. Chandra, J. B. Zhang, S. H. Lin, C. Q. Wei, and Z. H. Chen, "Compact Model Application to Statistical/Probabilistic Technology Variations," *Proc. of the 12th International Conference on Modeling and Simulation of Microsystems (WCM-Nanotech2009)*, Houston, TX, May 2009, Vol. 3, pp. 612-615.

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