Dual band low-noise amplifier designs for bluetooth and hiperLAN applications

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Dual Band Low-Noise Amplifier Designs for Bluetooth and HiperLAN Applications

Mou Shouxian

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2007

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research
and has not been submitted for a higher degree to any other university or institution.

Date

Mou Shouxian

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SUMMARY

The last decade saw an explosion of wireless communication technology, together with a rapid development of consumer demand for information. Intensive research efforts have focused on a lot of application areas, such as mobile cellular phones, cordless telephones, global positioning system (GPS), wireless short-distance communication and wireless local area network communication (WLAN/HiperLAN). With so many coexistent communication standards, it is necessary to develop a single-chip transceiver, which can adapt to several bands at the same time. One of the crucial bottlenecks for the multi-standard communications is how to design a low noise amplifier (LNA) that can operate in different frequency bands, as the LNA serves as the first amplification block in the receiving chains.

It is also known that, with the scalability of CMOS technology, the obtained cutoff frequency (f_T) could be up to one hundred gigahertz. However, the passive on-chip inductors implemented with the current CMOS process are usually lossy and bulky. This is a very significant problem in LNA design, especially in the input stage design using source inductive degeneration architecture. To make the circuit compact and fully integrated, research efforts should be done to reduce the required inductor number and inductor value.

Based on the above-mentioned concerns, the investigation on the designs of dual-band LNAs, as well as a modified architecture used for input matching in CMOS LNAs to make the circuit more compact, is presented in this thesis. According to the proposed investigation, a narrow-band LNA (LNA1), a wideband LNA (LNA3) and

two dual-band LNAs (LNA4 and LNA5) are designed with CSM 0.18 μ m CMOS technology. The corresponding design considerations are also presented in detail in the thesis.

The narrow-band LNA operates at 2.4GHz–2.5GHz. It has a measured power gain of 24dB, a noise figure of 2.6dB–2.8dB and a power consumption of 15mW. The wideband LNA operates at 5.1GHz–5.9GHz. It produces 22.6dB–24.6dB of power gain and 2.85dB–3.5dB noise figure while drawing 6mA current from a 1.5V voltage supply. Compared with their traditional counterparts, the proposed LNAs consume less chip area and achieve better gain performance.

The dual-band LNA4 has two operating bands: 2.4GHz–2.5GHz and 5.47GHz – 5.825GHz, with gains of 18dB and 16dB respectively. LNA4 obtains a noise figure of 2.26dB–2.4dB and 3.27dB for the first band and the second band respectively. Its power consumption is around 15mW. The dual-band LNA5 also has two operating bands of 2.4GHz–2.5GHz and 5.45GHz–5.85GHz. The measured power gain is 25dB for the first band and 10dB–12dB for the second band. The operating bands of LNA4 and LNA5 can cover the frequency range of Bluetooth and part of HiperLAN and wireless LAN.

In brief, the thesis investigates the CMOS RFIC designs, especially for single-band/dual-band LNA designs. It provides an approach which can help to achieve a compact and fully-integrated LNA.

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Chapter 1 Introduction

1.1 Motivation

Over the past few years, the wireless services industry has experienced a tremendous growth owing to rising consumer demand for information and the continuously growing need for connectivity [1-7]. Intensive research efforts have focused on mobile cellular phones, cordless telephones, global positioning systems (GPS), wireless short-distance communication and wireless local area network communication (WLAN/HiperLAN). Most of the operating frequency bands of these communications have the range between 800MHz and 6GHz. Table 1.1 summarizes the main features of cellular phone systems, including the Global System for Mobile communication (GSM), the Personal Digital Cellular (PDC) and the International Mobile Telecommunication (IMT2000). Besides these, there are also RF network systems, such as Bluetooth, Wireless 1394, HiperLAN [8] and IEEE 802.11a/b.

Table 1.1 Features of the cellular phone systems and RF network systems [5]

Standards	GSM	PDC	IMT 2000	Bluetooth	Wireless 1394	IEEE 802.11b	IEEE 802.11a
Freq (GHz)	0.9/1.8/1.9	0.8/1.4	1.9-2.1	2.4	5.2	2.4	5.2
Data rate (Mbps)	0.27	0.042	1.92	1	70	11	54
Access method	TDMA	TDMA	CDMA	TDMA	TDMA	CSMA/CA	CSMA/CA
Modulation	GMSK	QPSK	QPSK	GFSK	BPSK, QPSK	CCK, BPSK	BPSK, QPSK, 16/64 QAM
TX power (mW)	2000	800	250	1/100	NA	100	40
RX sense (dBm)	-108	-100	-116	-70	NA	-80	-82

In order to satisfy so many coexistent communication standards and at such high frequencies, these communication systems often consist of several ICs and lots of discrete components which are bulky and power consuming. These factors limit the size, weight and the battery life of wireless communication systems [9-11]. Therefore, the highly competitive market demands low-cost, low-power and small form-factor devices. Such demands call for the development of single-chip RF receivers, which are capable of adapting to the various communication bands and different modes in low-cost CMOS technology [1, 7].

Figure 1.1 An RF receiver diagram

One of the crucial bottlenecks for multi-standard communication applications is how to design an LNA that can operate in several frequency bands. It is known that the LNA is the first active amplification block in the receiving path as shown in Figure 1.1. In fact, the performance of the RF receiver is significantly influenced by the LNA. In the thesis, concurrent dual-band CMOS LNAs will be investigated and designed to meet the requirement.

Radio frequency integrated circuits (RFICs) were once the primary domain of GaAs or bipolar technologies, as they provide relatively high cutoff frequency (f_T). Presently, the continuous scaling of the CMOS process makes it possible for f_T to achieve tens of or a hundred gigahertz in typical deep-submicron CMOS technology.

Compared with GaAs and BJT technologies, CMOS technology has a higher level of integration and lower cost. Thus CMOS has become an attractive alternative for transceiver implementation [3-7]. However, the passive on-chip inductor implemented with the current CMOS process is usually lossy and consumes a large chip area. This is a very significant problem in LNA design, especially for the input stage design adopting source inductive degeneration architecture. To obtain a compact and fully-integrated low noise amplifier, research efforts should be devoted to the reduction of the required inductance, so as to reduce the chip area and manufacturing cost.

1.2 Objectives

The successful implementation of many RF front-end circuits with CMOS technology demonstrates the feasibility to realize a low-cost high-performance single-chip receiver [1, 12-14]. But CMOS RF circuit designs are still at an early stage of exploration, especially for dual-band/multi-band RFIC designs. The thesis tries to investigate the design issues of CMOS RFIC designs, with emphasis on single-band/dual-band LNA designs. It also attempts to find an approach which can help to implement a compact, reliable and fully-integrated RF system.

1.3 Major Contributions of the Thesis

Firstly, a modified architecture used for input matching in CMOS LNAs is investigated in the thesis. In traditional source inductive degeneration CMOS LNAs, the gate inductor L_g and source inductor L_s are basic components. In the proposed

architecture, L_g is reduced and L_s is removed. It decreases the requirement for the on-chip inductors with high inductance. The architecture is finally verified by a narrow-band LNA (LNA1) and a wideband LNA (LNA3) operating at 2.4GHz–2.5GHz and 5.1GHz–5.9GHz respectively. The narrow-band LNA has a measured power gain of 24dB, a noise figure of 2.6dB–2.8dB and a power consumption of 15mW. The wideband LNA produces 22.6dB–24.6dB of power gain and 2.85dB–3.5dB noise figure while drawing 6mA current from a 1.5V power supply. Compared to their traditional counterparts, the two LNA designs consume less chip area and achieve better gain performance.

Secondly, two concurrent dual-band LNAs (LNA4 and LNA5) have been successfully designed using 0.18 μ m CMOS. The design concerns are presented in details as well. Some techniques are adopted and analyzed in the designs, such as the load tuning technique and the Q -enhancement technique. Both of the two dual-band LNAs have two operating bands: 2.4GHz–2.5GHz and 5.47GH–5.83GHz. The operating bands can cover the frequency range of Bluetooth and part of HiperLAN and wireless LAN.

Finally, some issues on stability and input matching that are considered in LNA designs are discussed and highlighted.

The four fully-integrated LNAs presented in the thesis are all based on the Chartered Semiconductor Manufacturing (CSM) 0.18 μ m 1P6M CMOS technology. The proposed designs and investigations provide a practical insight for multi-standard

operation, decreasing manufacturing cost and enhancing system integration in RFIC designs.

1.4 Organization of the Thesis

The thesis is organized into seven chapters. Chapter 1 provides an introduction to the problem addressed and an outline of the thesis. In Chapter 2, the RFIC design background and noise fundamentals are described. Chapter 3 describes and reviews single-band/dual-band LNA designs, including corresponding design theories, design techniques and other concerns. In Chapter 4, noise modeling and considerations of passive devices are presented first. In the following section, a modified architecture used for input matching, is proposed and investigated extensively. With the proposed architecture, LNA designs can be more compact and fully-integrated. In Chapter 5, a narrow-band LNA (LNA1) and a wideband LNA (LNA3) are designed to verify the proposed input architecture. A narrow-band LNA2 with traditional source inductive degeneration input architecture, is also implemented for comparison with LNA1. Chapter 6 describes the designs of two concurrent dual-band LNAs for Bluetooth and HiperLAN applications. Stability considerations and some issues concerning input matching are also proposed and discussed in Chapter 6. The thesis is finally concluded in Chapter 7.

Chapter 2 Background and Noise Fundamentals

The past decades would be remembered for the tremendous growth of wireless services industry. Advances in integrated circuit technologies coupled with novel system level solutions have given rise to small, low-cost, low-power and portable units. The ultimate goal is to integrate a radio transceiver on a single semiconductor chip. To realize this goal, a fully-integrated CMOS LNA would be required.

In this chapter, a discussion on the technology involved in the design towards a single-chip transceiver will be presented. Subsequently, various performance measures for RF communication circuit design will be defined. Finally, fundamentals of noise will be introduced, as the design of a low noise amplifier highly relates to noise analysis and optimization.

2.1 Technology Trends in RFICs

There are three primary semiconductor materials used for integrated circuits: silicon (Si), gallium arsenide (GaAs) and silicon germanium (SiGe). Additionally, silicon-on-insulator technology, once mainly used in radiation-hard applications, has emerged as a promising candidate for applications in radio frequency [15].

In general, the traditional approach towards wireless transceiver design is to use GaAs based circuits for the realization of the RF components, such as power amplifiers, low noise amplifiers and so on. Silicon-based analog circuits are then used for the IF to baseband sections and possibly the RF mixers. In these approaches, band

selections at RF and IF are typically performed by discrete off-chip components. This eliminates the difficulties associated with the realization of on chip high- Q filters.

Compared to other technologies, CMOS offers substantial advantages in terms of the manufacturing cost and the level of integration. By integrating many of the RF functional blocks together with baseband analog circuits and potentially, backend DSP, the component count and the complexity of circuit board assembly can be greatly reduced, which will in turn lead to a low cost solution. A low cost CMOS solution is highly demanded due to the surge of interest in radio frequency integrated circuits in the last decade. And it is driven by the fast expansion of the mobile communication market in a variety of forms: from pagers and cordless telephones to analog and digital cellular telephones.

However, the technical requirements for the function of a typical wireless device are considerably more multi-dimensional than that of a digital integrated circuit – where power dissipation, speed, and yield are the major performance merits. In addition to these factors, RFICs have to contend with issues of noise, linearity, gain, and matching. Advances in CMOS technology have continuously reduced the minimum channel length of the MOSFETs and increased the f_T of the transistor [5, 16-22]. Figure 2.1 shows the f_T improvements of various processes over the years and the projected trends for this decade [22]. The figure indicates that, owing to technology scaling, the cutoff frequency of NMOS devices has increased to approximately 100GHz. It not only promises gigahertz integration and gigahertz clock rate, but also arouses great expectations for CMOS RF circuits at 1GHz–6GHz or

even higher frequencies [23-26], where the dominant technology is currently silicon bipolar and GaAs.

Figure 2.1 Progress of the cutoff frequency in several processes [22]

In the last few years, various CMOS RF chips have been implemented. It demonstrates the feasibility of using CMOS technology for RF circuit designs [1, 12-14, 27-30]. However, there are still some challenges in the approach towards the ultimate goal of integrating a radio transceiver on a single CMOS chip: low silicon substrate resistivity, which increases substrate loss and substrate thermal noise; inaccurate high-frequency transistor models; and lack of high- Q and precise on-chip passive components such as the inductor, capacitor and resistor. All of these issues greatly affect the performance and the integration of a CMOS based system.

2.2 Basic Concepts/Parameters in RF Designs

In this section, concepts and terminology used in RF electronics, for example, noise figure, 1-dB compression point, intermodulation distortion and so on will be described and defined. It is important to understand the meaning of these parameters as they are the common languages for engineers to specify the entire system. Analysis on these parameters helps to optimize the performance of circuits for different applications.

2.2.1 Noise Figure

Noise factor (F) is a measurement of the noise performance of a circuit. It is frequently expressed in decibels and commonly referred to as noise figure (NF).

$$NF = 10 \log_{10} F \quad (2.1a)$$

Noise figure is defined in many ways. The most common definition is:

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}}, \text{ where } NF = 10 \log_{10} F \quad (2.1b)$$

SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output, respectively. In other words, NF is a measure of SNR degradation due to noise generated by the circuit itself.

For a cascade of N stages, the overall noise factor can be obtained in terms of the F and gain at each stage. The total noise factor can be expressed by the Friis Equation [31]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1}A_{p2}} \dots + \frac{F_N - 1}{A_{p1}A_{p2} \dots A_{p(N-1)}} \quad (2.2)$$

where F_m is the noise factor of stage m and A_{pm} is the available power gain of the m^{th} stage. This equation indicates that the noise contributed by each stage decreases as the gain of the preceding stage increases. Thus, the first few stages in a cascade are the most critical stages. In practice, the LNA is the first active block in the receiving chain, therefore, its noise figure directly adds to that of the system. An LNA should provide enough gain to overcome the noise contribution of the subsequent stages and add as little noise as possible.

2.2.2 1-dB Compression Point

The linearity of a system determines the maximum allowable signal level to its input. All real-life systems exhibit some degree of nonlinearity. Signal distortion is a direct consequence of the nonlinear behavior of solid-state devices in circuits. The most common measures of non-linearity are the 1-dB compression point ($P_{1\text{-dB}}$) and the third-order intercept point (IP_3).

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. When the input signal is $x(t) = A \cos \omega \cdot t$, then the output through the system will be:

$$y(t) = \alpha_1 A \cos \omega \cdot t + \alpha_2 A^2 \cos^2 \omega \cdot t + \alpha_3 A^3 \cos^3 \omega \cdot t + \dots$$

$$\approx \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{\alpha_3 A^3}{4}) \cos \omega \cdot t + \frac{\alpha_2 A^2}{2} \cos 2\omega \cdot t + \frac{\alpha_3 A^3}{4} \cos 3\omega \cdot t \quad (2.3)$$

where α_1 , α_2 , α_3 and so on are the corresponding equation coefficients; A is the amplitude of the input signal $x(t)$. In Equation (2.3), the term with the input frequency is called the “fundamental” and the higher-order terms are the “harmonics”. For most

circuits of interest, there is $\alpha_3 < 0$ [32]. Therefore, the gain $(\alpha_1 A + \frac{\alpha_3 A^3}{4})$ is a decreasing function of A (amplitude). As the input power increases, the circuit components become saturated and the fundamental output fails to respond linearly to the input. Figure 2.2 shows that the gain compression due to the nonlinearities in the system causes the power gain to deviate from its idealized curve. The point at which the power gain is down 1dB from the ideal curve is referred to as the 1-dB compression point. The input power where $P_{1\text{-dB}}$ occurs is known as $IP_{1\text{-dB}}$. A system must operate several decibels below this level to avoid the nonlinear region. The 1-dB compression point can be calculated as [32]:

$$IP_{1\text{-dB}} = 20 \log_{10} \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \quad (2.4)$$

2.2.3 The 3rd Order Intercept Point

Besides the 1-dB compression point, the 3rd order intercept point (IP_3) is another common measure of a circuit's nonlinearity. It is caused by the intermodulation (IMD) products of a signal and interferers. When their frequencies are close enough, they can fall within the passband of the system and appear at the output as signal distortion.

If the two-tone inputs have the same amplitude, the 3rd order IMD power will grow to a value that is equivalent to the cube of the input power as shown in Figure 2.2. In other words, the power of the third-order IMD increases three times faster than that of the fundamental. The input signal level, where the power of the third-order IMD equals to that of the fundamental is defined as “two-tone input-referred

third-order intercept point” (IIP_3). And the corresponding output level is called the “output third-order intercept point” (OIP_3). The fundamental amplitude is a linear extrapolation of the small-signal fundamental output curve without the effect of gain compression. IIP_3 can be calculated as [32]:

$$IIP_3 = 20 \log_{10} \sqrt{\frac{4}{3} \frac{\alpha_1}{\alpha_3}} \quad (2.5)$$

Figure 2.2 Illustrations of $P_{1\text{-dB}}$ and IP_3

For a cascade of N -stage network, the IIP_3 of the system ($IIP_{3_{tot}}$) can be expressed as [33]:

$$\frac{1}{IIP_{3_{tot}}} = \frac{1}{IIP_{3_1}} + \frac{G_1}{IIP_{3_2}} + \frac{G_1 G_2}{IIP_{3_3}} + \dots + \frac{G_1 G_2 \dots G_{N-1}}{IIP_{3_N}} \quad (2.6)$$

where IIP_{3_i} and G_i ($i=1,2,\dots,N$) are the IIP_3 and the available power gain of the i^{th} stage network respectively. It is observed from (2.6) that, for the IIP_3 calculation, the

last stage contributes the most to the distortion of the system. It is unlike the noise figure calculation, where the first stage is the most critical. Thus it is important to end the system with a high linearity block [34].

2.2.4 Sensitivity

Sensitivity is a measure of a system's ability to amplify and demodulate weak signals. Sensitivity is often expressed in terms of the minimum detectable signal (MDS) level at the input, which produces some acceptable level of signal-to-noise ratio (SNR) at the demodulator output. MDS is given by [32]:

$$P_{in,min} (dBm) = -174dBm / Hz + NF + 10 \log B + SNR_{min} \quad (2.7)$$

where SNR_{min} is the minimum signal-to-noise ratio; $P_{in,min}$ is the minimum input level that achieves SNR_{min} , and B is the effective noise bandwidth. Note that the sum of the first three terms is the total integrated noise of the system and is sometimes called the “noise floor”.

2.2.5 Dynamic Range

In a wireless environment, the radio signal strength can vary greatly depending on the distance between the transmitter and receiver and on the path of the radio signal. A receiver's ability to accommodate both large and small signals is indicated by its dynamic range (DR). DR is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit can provide a reasonable signal quality. “Spurious-free dynamic range” ($SFDR$) and

blocking dynamic range (*BDR*) are two commonly used definitions of the dynamic range [35].

SFDR is a measure of the receiver's immunity to distortion generated by spurious signals. The upper bound of *SFDR* is defined as the maximum input level $P_{in,max}$ in a two-tone test, at which the third-order IMD products do not exceed the noise floor. The lower bound is set by MDS, given by (2.7). *SFDR* can be expressed as [33]:

$$SFDR = P_{in,max} - P_{in,min} = \frac{2P_{IP3} + N_{floor}}{3} - (N_{floor} + SNR_{min}) = \frac{2(P_{IP3} - N_{floor})}{3} - SNR_{min} \quad (2.8)$$

where the P_{IP3} is the power of the input IP_3 and the N_{floor} is the noise floor.

BDR is a measure of the resilience of the receiver to a large out-of-band blocking signal which, by driving the receiver into compression, desensitizes it to a small desired signal [35]. The upper bound of *BDR* is the 1-dB compression point, and the lower bound is also MDS. When expressed in dBm, *BDR* is given by:

$$BDR = IP_{1dB} - P_{in,min} \quad (2.9)$$

The graphic representations of *SFDR* and *BDR* are shown in Figure 2.3.

2.2.6 S-Parameters

It is known that a two-port network is commonly used in circuit design. To characterize its behavior, measured data of both transfer function and impedance function of the two-port network must be obtained. At low frequencies, Z, Y, H and ABCD parameters are used in the description of the two-port network. But at high frequency, these parameters cannot be measured accurately because the required

short-circuit and open-circuit tests are difficult to achieve. Scattering parameters (S-Parameters), based on incident and reflected waves, are very useful in radio frequency range.

Figure 2.3 Dynamic ranges for a receiver

Figure 2.4 A two-port network

Figure 2.4 illustrates a two-port network, where a_1 , a_2 are incident waves, b_1 , b_2 are reflected waves. Their relation is expressed as:

$$\begin{bmatrix} b_1(l_1) \\ b_2(l_1) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1(l_1) \\ a_2(l_1) \end{bmatrix} = [S] \begin{bmatrix} a_1(l_1) \\ a_2(l_1) \end{bmatrix} \quad (2.10)$$

Figure 2.5 Meaning of S-parameters

The matrix $[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$ is called scattering matrix, where S_{11} is the input reflection coefficient, S_{12} is the reverse transmission coefficient, S_{21} is the forward transmission coefficient, and S_{22} is the output reflection coefficient. They can be calculated according to Figure 2.5 and Equations (2.11a) – (2.11d):

$$S_{11} = \frac{b_1(l_1)}{a_1(l_1)} \Big|_{a_2(l_2)=0} = \text{input reflection coefficient with matched output port;} \quad (2.11a)$$

$$S_{12} = \frac{b_1(l_1)}{a_2(l_2)} \Big|_{a_1(l_1)=0} = \text{reverse transmission coefficient with matched input port;} \quad (2.11b)$$

$$S_{21} = \frac{b_2(l_2)}{a_1(l_1)} \Big|_{a_2(l_2)=0} = \text{forward transmission coefficient with matched output port;} \quad (2.11c)$$

$$S_{22} = \frac{b_2(l_2)}{a_2(l_2)} \Big|_{a_1(l_1)=0} = \text{output reflection coefficient with matched input port.} \quad (2.11d)$$

From the view point of amplifier design, S_{11} and S_{22} denote how well the input and output impedances are matched to the reference impedance respectively. S_{21} measures the insertion effect (amplification gain) of the amplifier. S_{12} represents the isolation between output and input ports. S-parameters can be converted to y-parameters or other network representations. Detailed formula can be found in most microwave textbooks, such as [36- 37].

2.3 Fundamentals of Noise

Noise is any unwanted signal that interferes with a desired signal. Most electronic noise can be categorized as being either random or deterministic [38]. An example of deterministic noise is the hum in a loudspeaker caused by an ac ripple on a supply voltage in an amplifier. Deterministic noise is caused by an identifiable external source and can usually be eliminated by proper methods of grounding and shielding. In contrast, other noise sources classified as random noise sources are irreducible by shielding since they are inherent in the device itself. These noise sources set the lower bound of the dynamic range in a system.

The microscopic noise theory at the material level is straightforward and well established. Physically, two types of noise can be identified: thermal and quantum.

However, phenomenologically, several types of noise sources could be observed, for instance, thermal, shot, flicker and generation-recombination noise.

2.3.1 Thermal Noise

A thermally-excited electron in a conductor undergoes a random walk [39] (Brownian Motion) via collisions with the lattice of the conductor. As a result it produces fluctuations in the terminal characteristics. The phenomenon was discovered (or anticipated) by Schottky [40] in 1918 which he called the “warneffect.” In 1927, Johnson discovered that the noise power spectrum of a conductor is independent of its material and measurement frequency [39]. Noise properties are determined only by the temperature and electrical resistance under thermal equilibrium [39]:

$$\overline{v_n^2} = S_{v_n} \Delta f = 4kTR\Delta f \quad (2.12)$$

$$\overline{i_n^2} = S_{i_n} \Delta f = 4kT\Delta f / R \quad (2.13)$$

This noise is referred as thermal noise, which is the most fundamental and important noise in electronic devices. Johnson’s colleague Nyquist explained the original observations based on the equipartition theorem thermodynamics and a transmission line cavity without going into the details of the microscopic electron transport process [40].

Thermal Noise in Electronic Devices

Thermal noise assumes that the system is in thermal equilibrium, which only applies strictly if no bias is applied to the device. When there is a bias, the carrier collisions produce noise called either diffusion noise or velocity-fluctuation noise.

Since the behavior of these kinds of noise agrees well with Johnson's thermal noise model, they are often called thermal noise as well, especially for resistors.

Thermal Noise in MOSFETs

Thermal noise of MOSFETs imposes a fundamental limitation on CMOS devices [41]. Based on the fact that the MOSFET is a modulated resistor, which is capacitively coupled to the gate, Van Der Ziel proposed a thermal noise model for MOSFETs. It consists of drain current noise, induced gate current noise and their cross-correlation part as follows [40]:

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \quad (2.14)$$

$$\overline{i_{n,g}^2} = 4kT\delta g_g\Delta f \quad \text{with} \quad g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (2.15)$$

$$c = \frac{\overline{i_g i_d^*}}{(\overline{i_g i_g^*} \cdot \overline{i_d i_d^*})^{1/2}} \quad (2.16)$$

where γ and δ are bias-dependent factors; g_{d0} is the drain output conductance at zero drain source voltage ($V_{ds}=0$); g_g is the real part of the gate-to-source admittance; and c is the cross correlation coefficient. For long-channel devices, γ is 2/3 when the MOSFET operates in the saturation region, whereas when the drain bias is zero γ is 1 [40]. δ is normally considered to be two times of γ . The correlation coefficient c is $\pm 0.395j$, the sign of which depends on the adoption of the reference polarity for the drain current noise [42]. For short-channel devices, the above parameters increase. However, the amount of the increase is still controversial [43-44]. The physical mechanism responsible for this increase remains an open question. This issue will be discussed in later chapters.

Note that the induced gate current noise is induced by local fluctuations in the channel via capacitive coupling through the gate oxide. The induced gate noise is proportional to f^2 , owing to the ωC_{gs} dependence. Drain current noise is frequency independent, and is called white noise. $\overline{i_{n,g}^2}$ plays a very significant role in the noise performance of the MOSFET at radio frequency.

2.3.2 Shot Noise

Shot noise is generated by the random emission of electrons or by the random passage of electrons and holes across a potential barrier. It is first described by Schottky [40] in 1918. The mean-square shot noise current in the frequency band Δf is given by:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \quad (2.17)$$

where q is the electronic charge and I_{DC} is the DC current flowing across the device. Two conditions must be satisfied for shot noise to occur: a flow of direct current and a potential barrier over which the carriers hop [41]. Linear devices do not generate shot noise. In the case of MOSFETs, shot noise dominates the noise characteristics when the device is in the subthreshold region due to the carriers' transport. Recently, with MOS scaling, the VDD and bias voltage also decrease. Thus, the operation region is constantly away from the region of strong inversion. It is suspected that shot noise may contribute much to the device's noise performance.

2.3.3 Flicker Noise

Flicker noise is noise that has a spectral density proportional to $1/f^n$, where n is around 1. It is also called $1/f$ noise. Flicker noise is ubiquitous, but no universal mechanism has been proved definitively as its origin. Generally, they can be categorized into three major types: carrier number fluctuation theory, mobility fluctuation theory and their combination [45]. Therefore, its model contains various empirical parameters. The typical model is given by [46]:

$$\overline{i_n^2} = \frac{K}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \quad (2.18)$$

where K is a device-specific constant; g_m is the transconductance; W is the device width; L is the device length; and C_{ox} is the gate oxide capacitance per unit area.

At low frequencies, flicker noise is the dominant noise source in MOS devices. At high frequencies, its effect becomes negligible but there is an exception in the case of a CMOS VCO, where it causes a significant increase of phase noise due to up-conversion [47].

2.3.4 Generation-Recombination Noise

Generation-recombination noise is caused by the carrier density fluctuation due to emission and capture of carriers by traps. It manifests itself as resistance fluctuations. Generation noise is observed only when external bias voltage is applied. This noise is closely related to the localized energy states. Its behavior depends much on the temperature, frequency and bias conditions. In modern MOSFET technologies,

this component is usually much smaller than flicker noise and generally can be neglected [46].

2.3.5 Four Noise Parameters

A noisy (but linear) two-port driven by a source, which has admittance Y_s and an equivalent shunt noise current $\bar{i}_s$, is shown in Figure 2.6 (a). It has an equivalent form as shown in Figure 2.6 (b). The noise factor can be expressed as:

$$F = \frac{\bar{i}_s^2 + \overline{|i_n + Y_s e_n|^2}}{\bar{i}_s^2} \quad (2.19)$$

Figure 2.6 (a) Noisy two-port; (b) equivalent noise model

After complex derivation, Equation (2.19) can be finally written as [41]:

$$F = F_{\min} + \frac{R_n}{G_s} [(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \quad (2.20)$$

where $Y_s = G_s + jB_s$ is the source admittance seen by the two-port network; $Y_{opt} = G_{opt} + jB_{opt}$ is the optimal source admittance; $F_{\min}$ is the minimum noise factor that the network can achieve under the optimum source admittance condition ($Y_s = Y_{opt}$); R_n is the noise resistance, which determines the sensitivity of noise figure when Y_s differs from Y_{opt} .

This representation is widely used in RF circuit design since it offers a more intuitive way to deal with noise properties [36]. These four noise parameters, $F_{\min}$, R_n ,

G_{opt} and B_{opt} , are determined by intrinsic noise sources of the given system. Given these four parameters, RF designs can be optimized. Generally, to get a low noise figure, the criteria is to have a low NF_{min} , a small R_n and minimal difference between Y_s and Y_{opt} .

2.4 Summary

In this chapter, the technology background for RFIC design, especially the advantages and disadvantages of CMOS technology, is described. Subsequently, the basic concepts and definitions of parameters in RF design are explained. In the last section of this chapter, noise fundamentals are introduced. The contents of this chapter provide a better understanding of CMOS LNA designs in the following chapters.

Chapter 3 Literature Review on LNA Designs

In this chapter, an introduction to LNAs as well as several different receiver structures will be firstly presented and highlighted, so as to understand current trends in LNA research. Next, the input matching architectures in LNA designs will be classified and examined. Thirdly, the LNA load tuning techniques will be discussed. Finally, in the last three sections, the designs of recent narrow-band LNAs, wideband LNAs and dual-band/multi-band LNAs will be reviewed.

Figure 3.1 A conventional superheterodyne receiver architecture

3.1 Introduction to LNAs

The front-end of a typical transceiver consists of a receiving path and a transmitting path. For the transmitting path, the only existent signal is the wanted signal. This simplifies the design of the transmitting path, as issues such as noise, interference rejection and selectivity can be relaxed [33]. In contrast, for the receiving path, the wanted RF signal is weak and surrounded by noise and interferers. Thus, the design of the receiver involves many issues and tradeoffs. LNA is the first active element in the receiving chain. Its noise figure (NF) and gain play a significant role in the overall performance of the receiver [33]. Before exploring the design details of

single-band/dual-band LNAs, it is helpful to have a knowledge of the LNA and the receiver first.

3.1.1 LNA in Conventional Architecture Receivers

Figure 3.1 illustrates a simplified block diagram of the superheterodyne receiver architecture. Because of its reliable performance, this architecture has been widely used in various radio applications.

In the figure illustrated, the incoming signal is first filtered by an RF filter to lower unwanted out-of-band signals. After amplification by an LNA, the signal is then filtered by the image-reject filter to further reduce the power level of undesired signals. Next, the RF signal is down-converted to the intermediate frequency (IF). After passing through a narrow-band IF filter, it is converted to baseband signal for further processing in subsequent stages.

In practice, the incoming RF signals are considerably small (generally around -100dBm), which leads to a small signal to noise ratio (SNR). Any additional noise will further degrade the overall SNR and therefore the receiver performance. Because LNA is the first gain stage along the receiver chain, its noise figure (NF) has to be low enough to keep the overall system's NF low. On the other hand, the gain of the LNA needs to be high enough to reduce the noise contribution from the subsequent mixer and other stages, but not too high to degrade the overall system's linearity. In many systems, where the dynamic range of the incoming signal is large, LNAs are often designed as variable-gain amplifiers (VGA) to reduce the dynamic range requirement for later stages. The linearity requirement of the LNA by itself is, in general, not very

critical, except for systems such as CDMA, in which both receiver and transmitter are on at the same time. In addition, because the RF filter and the image-reject filter, which are typically required to be matched to 50Ω , are placed in front of and after the LNA, input/output impedance matching is part of LNA's specifications. Finally, power consumption is a concern, especially for portable devices.

In summary, the ideal features of an LNA are [23-24]: low noise figure, sufficient gain, good impedance matching, low power consumption and good linearity.

3.1.2 LNA in High-Integration Architecture Receivers

The superheterodyne architecture requires at least 3 discrete filters, as discussed in the previous section. Although this architecture provides very high performance, it is very costly due to the discrete components, the packages and the additional assembly process. Hence, new radio architectures which can replace expensive discrete components with low-cost integrated circuits should be proposed. The ultimate goal is to implement a single-chip radio system. Single-chip architectures usually include homodyne/direct IF, image-reject (including Weaver architecture [32-33] and Hartley architecture [32-33]), wide IF with double conversion (WIF) [27] and so on.

Figure 3.2 A direct conversion (homodyne) receiver architecture

Figure 3.3 A wideband IF with double conversion receiver architecture

Figure 3.2 and Figure 3.3 show the simplified diagrams of a homodyne architecture and a WIF architecture, respectively. Figure 3.3 can be taken as an example. This architecture replaces the discrete image-reject filter with an active image-reject mixer and does not need the IF filter (only simple RC low pass filter is required to attenuate the higher order terms due to mixing). It gives the possibility of implementing a single-chip system. In addition, this architecture uses a fixed RF local oscillator (LO) to down-convert the entire band of interest and perform channel selection by the IF local oscillator. By using a fixed RF LO, it allows the entire frequency synthesizer to be implemented using on-chip low- Q components with the wideband PLL approach. It further eliminates the requirement of discrete high- Q LC tanks as in conventional radio architectures [51].

The qualities of the above architecture allow high integration LNA design. Firstly, due to the removal of the image-reject filter, the output of the LNA no longer needs to be matched exactly to 50Ω . Therefore, the output impedance can be optimized for a better performance and the power consumption can be reduced due to the elimination of the additional 50Ω output driver stage that is normally required. Secondly, aiming for full-system integration, the LNA is required to provide input

matching with minimum discrete components. A fully-integrated LNA is the best option.

Figure 3.4 (a) & (b): Two simplified dual-band receiver architectures [10-11]; (c) & (d): detailed dual-band receiver architectures [1, 70]

3.1.3 LNA in Dual-Band/Multi-Band Receivers

Currently, most of the receivers in literature are for single-band applications [6, 12-14, 25, 49-65]. Their operation modes limit the system's available bandwidth and robustness due to channel variations, thus limiting the system's functionality as well [11, 66]. However, the diverse range of modern wireless applications offers communication systems more bandwidth and flexibility [66-69]. There are some examples for dual dual-band/multi-band/wideband applications [10-11, 67-69]. Figure 3.4 (a) & (b) illustrate two simplified receiver diagrams for dual-band applications

[10-11, 67-69]. Figure 3.4 (c) & (d) depict the detailed diagrams from literatures [1, 70].

Although the dual-band receiver shown in Figure 3.4 increases the functionality of the system, it consumes either more chip area or more power, owing to additional building blocks or different independent signal processing paths¹. Akira Matsuzawa [5] proposed a structure for the next-generation multi-function cellular phone handset [5] in 2002. In fact, his proposal is similar to the architecture shown in Figure 3.4 (b): simultaneous operation at different frequency bands is achieved by building multiple independent signal paths, which causes an increase of cost, footprint and power consumption.

Figure 3.5 System configuration for the next-generation cellular phone handset [5]

In fact, the feasibility of a multi-standard receiver is to a great extent influenced by the feasibility of the development of a concurrent and efficient

¹ The architecture shown in Figure 3.4 (a) can only work at one frequency band at one time (non-current) through the use of a switch. The architecture shown in Figure 3.4 (b) can operate at two different frequency bands simultaneously (or concurrently) at the expense of two independent signal processing paths. Generally, with the rapid development of various wireless communication products and services, a concurrent receiver is highly demanded.

dual-band/multi-band LNA owing to LNA's importance in the receiving chain. In Chapter 6, efforts are devoted to the research and design of the dual-band LNA. With a low-cost and low-power concurrent dual-band LNA, the simplified diagram of a dual-mode operation receiver is illustrated in Figure 3.6.

Figure 3.6 A simple diagram of the concurrent dual-band receiver architecture

3.2 Input Architecture of LNAs

Recall from the previous section, it is known that input impedance matching to 50Ω is one of the common goals in LNA design. Input matching architectures in LNAs can be classified into four types as shown in Figure 3.7- Figure 3.10. Each of these architectures can be implemented in single-ended or differential form.

3.2.1 Common Source Stage with Resistive Termination

This technique uses resistive termination in the input port to provide 50Ω impedance. This approach is adopted in its differential form by Chang [71]. As shown in Figure 3.7, a 50Ω resistor R_1 is placed in parallel with the input, to realize input matching for the LNA. However, this termination resistor generates noise. The noise factor of the circuit can be calculated:

Figure 3.7 Common source with resistive termination

$$F = \frac{\overline{V_{n,out}^2}}{\overline{V_{n,o,Rs}^2}} = \frac{\overline{V_{n,o,Rs}^2} + \overline{V_{n,o,R1}^2} + \overline{V_{n,o,M1}^2}}{\overline{V_{n,o,Rs}^2}} \approx \frac{4kT(R_s // R_1)g_m^2 R_L^2 \Delta f + \overline{i_{n,d}^2} R_L^2}{\frac{1}{4} g_m^2 R_L^2} \frac{1}{4kTR_s \Delta f} \quad (3.1)$$

where $\overline{V_{n,out}^2}$ represents the total output noise; $\overline{V_{n,o,Rs}^2}$, $\overline{V_{n,o,R1}^2}$ and $\overline{V_{n,o,M1}^2}$ are the output noise due to R_s , R_1 and M1, respectively. k is the Boltzmann's constant and T is the absolute temperature. MOSFET M1 has various noise sources. Here, for simplicity in calculation, only the channel noise $\overline{i_{n,d}^2} = 4kT\gamma g_{d0} \Delta f$ is taken into account, since in most conditions, channel noise is the dominant noise source.

Equation (3.1) can be further simplified to:

$$F = \frac{4(R_s // R_1)}{R_s} + \frac{4\gamma}{g_m R_s} = 2 + \frac{4\gamma}{\alpha g_m R_s} > 3dB \quad (\text{in decibels}) \quad (3.2)$$

where $\alpha = \frac{g_m}{g_{d0}}$. α is typically less than one. It is mentioned in Chapter 2 that for

long-channel devices, γ is unity when the MOSFET operates in the triode region and 2/3 in the saturation region. For short-channel devices, γ can be significantly larger than 2/3. Taking $R_1=R_s=50$, $\gamma=1$, $\alpha=0.8$, $g_m=0.06$ as an example, F is calculated to be 3.67, which is 5.6dB. Thus, the noise figure of this architecture can far exceed 3dB.

The noise figure degradation is due to two effects. Firstly, the added resistor R_1 contributes as much noise as the source resistor R_s does. It results in a factor of 2 in the first term of Equation (3.2). Secondly, the input is attenuated, leading to a factor of 4 differences in the second term of Equation (3.2) [23]. The poor noise figure makes this architecture unattractive for applications where a low NF as well as a good input matching is desired.

3.2.2 Common Gate Stage

Figure 3.8 shows a simplified $1/g_m$ termination architecture. This configuration requires that $1/(g_m + g_{mb}) \approx 1/g_m$ equal to R_s , where R_s is the 50Ω source resistance. This topology is suitable for wideband input matching designs, since $1/g_m$ is nearly constant over a quite wide frequency range. The main drawback of this method is that the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise figure. Here, for the simplicity of calculation, only the channel thermal noise $\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f$ of the MOSFET is taken into account. Through derivation, F can be expressed as:

$$F = \frac{4kTR_s g_m^2 R_L^2 \Delta f + \overline{i_{n,d}^2} R_L^2}{g_m^2 R_L^2} \cdot \frac{1}{4kTR_s \Delta f} \approx 1 + \frac{\gamma}{\alpha} \geq 1 + \frac{2/3}{1} = \frac{5}{3} = 2.2dB \text{ (in decibels)} \quad (3.3)$$

The above calculations suggest a reasonable noise figure. But, in fact, other noise sources such as gate induced noise and substrate noise can degrade the performance substantially. In short-channel MOSFETs, γ can be higher than $2/3$, and α can be much less than 1. Using $\gamma=1$, $\alpha=0.8$ as an example again, Equation (3.3) gives a noise factor of 2.25, which is about 3.5dB. Furthermore, the load as well as the biasing

circuits can generate additional noise. This architecture is used when a 3dB noise figure is acceptable.

Figure 3.8 Common gate input architecture

Figure 3.9 Common source input stage with shunt feedback

3.2.3 Common Source Stage with Shunt Feedback

Figure 3.9 illustrates another topology, which uses the resistive shunt and series feedback to set the 50Ω input impedance of the LNA. The input impedance can be expressed as [41]:

$$Z_{in} \approx R_{fb} / (1 + |A_v|) \quad (3.4)$$

where R_{fb} is the feedback resistor and A_v is the corresponding voltage gain. The topology has several disadvantages. Firstly, Equation (3.4) shows that the input

impedance Z_{in} depends on R_{fb} and A_v . Therefore it is sensitive to process variation. Secondly, the feedback signal may contain substantial noise, thus raising the noise figure to an unacceptable level. Thirdly, this architecture often has high power dissipation. The high dissipation is partially due to the fact that shunt-series amplifiers of this type are naturally wideband; hence techniques which reduce the power consumption through LC tuning are not applicable [23]. At last, the total phase shift around the loop may create instability for certain source and load impedances. The noise factor for this configuration can be expressed as follows [72]:

$$F = 1 + R_s \delta g_g + \left(\frac{G_s + G_{fb}}{g_m - G_{fb}} \right)^2 R_s (R_l + \gamma g_{d0}) + \left(\frac{G_s + g_m}{g_m - G_{fb}} \right)^2 R_s G_{fb} \quad (3.5)$$

where G_s , G_{fb} and G_1 is the conductance of the resistors R_s , R_{fb} and R_1 , respectively. The analysis in [59] indicates that the drain noise is the largest contributor. Nevertheless, as power consumption increases, the gate noise and the noise due to R_{fb} also become significant. Federico used noise canceling technique to reduce the noise figure of a wideband LNA of this structure [73]. It looks effective. However, the design of the circuit becomes complicated.

3.2.4 Common Source Stage with Source Inductive Degeneration

As shown in Figure 3.10, the fourth architecture employs source inductive degeneration to generate a real term in the input impedance. The input impedance is:

$$Z_{in} \approx j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} + (g_{m1} / C_{gs}) L_s \quad (3.6a)$$

Figure 3.10 Common source input stage with source inductive degeneration

The impedance shown in Equation (3.6a) has a resistive term $(g_{m1} / C_{gs})L_s$, which is directly proportional to the inductance value. Whatever value this resistive term is, it does not generate thermal noise like an ordinary resistor does, because a pure reactance is noiseless. Therefore, this structure can be exploited to provide a specified input impedance without degrading the noise performance of the amplifier. For example, to get a 50Ω input impedance, let the real part $(g_{m1} / C_{gs})L_s$ of Equation (3.6a) equal to 50Ω and the imaginary part $\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}$ be zero at the frequency of interest, which can be obtained through the following expression:

$$\omega_0 = 1 / \sqrt{(L_g + L_s)C_{gs}} \quad (3.6b)$$

Detailed noise analysis and optimization of the LNA with this architecture are presented in [23, 42]. The noise factor can be expressed as:

$$F = 1 + \left(\frac{\omega_0}{\omega_T}\right)R_s\gamma g_{d0} + \left[\left(\frac{\omega_T}{\omega_0 g_m R_s}\right)^2 + 1\right]R_s\delta g_g + 0.79R_s\left(\frac{\omega_0}{\omega_T}\right)\sqrt{\gamma g_{d0}\delta g_g} \quad (3.7)$$

where $\omega_T = g_m / C_{gs}$ is the unity current gain frequency and ω_0 is the center operating frequency. In practice, the gate inductor and source inductor can not be

implemented as ideal ones. Both of them have parasitic resistance which will contribute thermal noise. Thus, their effect must be taken into account while doing noise optimization and the calculation of input impedance, especially in the case where on-chip integrated inductors are adopted.

Based on the analysis in [23], the common source input topology with source inductive degeneration provides a low noise figure, comparable gain and low power consumption. This topology is most prevalently used in GaAs MESFET amplifiers [36]. Currently, it is also widely used in the design of CMOS narrow-band LNAs [1, 10-11, 23-24, 46, 66-67, 74-79].

3.3 Tuning Techniques of LNAs

Besides the input matching network, the tuning techniques applied to the load at the device output will affect the performance of the LNA. A good design of the tuning load helps to reject out-of-band signals and noise as well as to achieve a high gain. Three types of tuning loads are commonly used.

3.3.1 Ordinary Resistor as Load

Resistive load is commonly used before as shown in Figure 3.11. The voltage gain is around $A_v = g_{m1}R_d$, where g_{m1} is the transconductance of transistor M1. Sometimes, resistor R_d is replaced by a MOS transistor. This method produces wideband output impedance and can be easily implemented. However, it is not suitable for low noise applications, because the resistor generates thermal noise.

Figure 3.11 Resistive load

Figure 3.12 (a) LNA with passive LC tuning stage; (b) RLC parallel network

3.3.2 Passive LC as Tuning Load

Figure 3.12 shows another type of load. It is the most prevalent type used in LNA design [1, 10-11, 23-24, 46, 66-67, 74-79]. It is used extensively in communication circuits to provide selective amplification of wanted signals and to filter out unwanted signals to some extent. The RLC network has an admittance of:

$$Y = j\left(\omega C - \frac{1}{\omega L}\right) + G \quad (3.8)$$

When the inductor L and capacitor C are designed to resonate at a selected frequency (that is $f = \frac{1}{2\pi\sqrt{LC}}$), the impedance is purely real and at its maximum.

The higher the quality factor of L is, the larger $1/G$ is, and the higher the voltage gain is². This type of tuning load is very suitable for narrow-band applications. It allows LNAs to achieve substantial gain at relatively high frequencies with low power consumption.

In practice, the silicon-based on-chip spiral inductor does not have a large quality factor Q . Hence, $1/G$ is not very high. $1/G$ is around several hundreds ohms for most of the cases. There are several ways to increase $1/G$. One way is to use high- Q off-chip inductors by sacrificing the market demands for highly-integrated products. Another way is through process modification to obtain a higher inductor Q . For example, a higher Q can be achieved by removing the inductor's underlying silicon substrate or by using a thick top metal. These might introduce additional processing steps and increase the cost. The third way is to use the Q -enhanced technique [80-82], as illustrated in Figure 3.13.

Figure 3.13 The Q -enhancement technique

The basic principle of the Q -enhancement technique is to add a negative conductance to the LC resonator so that the resistive loss of the inductor can be

² At the resonant frequency, the voltage gain A_v is about $g_m \times (1/G)$.

compensated. In Figure 3.13, G_p is the parasitic resistance of the inductor L^3 , C_l includes the load capacitor and the parasitic capacitor of the inductor L . Ignoring $-G_n$, Q can be expressed as $Q = \frac{1}{G_p} \sqrt{\frac{C_l}{L}}$ [41]. The above equation indicates that Q is drastically reduced because of the ohmic loss in the inductor. To reduce the effect of G_p on the Q , a negative conductance $-G_n$ is employed to compensate the loss in the inductor. Thus the Q of the tuned circuit increases to $Q = \frac{1}{(G_p - G_n)} \sqrt{\frac{C_l}{L}}$. With this method, the achieved Q can be 20 or even higher. G_n can not be larger than G_p ; otherwise, the circuit will oscillate.

3.3.3 Active Inductor and Passive Capacitor as Tuning Load

Due to the limitation of spiral inductors, for example, large chip area or parasitic capacitance and resistance loss, active inductors that can be implemented with a reasonable physical size offer a good alternative for its passive equivalent [83-87]. Traditional active inductors are typically implemented by using high gain operational amplifiers with negative feedback, and are unsuitable for operating frequencies up to gigahertz. Another type of active inductor is implemented by exploiting the parasitic capacitance of the transistors to generate the required poles and zeros [83-87]. Figure 3.14 illustrates a simplified schematic diagram of an active inductor [88]. Its input impedance can be expressed as [88]:

$$Z_{in}(s) = \frac{g_{ds1}g_{ds2}g_{ds3}/(g_{m2}g_{m3}) + sC_{gs4}}{(g_{m4} + sC_{gs4})(g_{m1} + 2sC_{gd2})} \quad (3.9)$$

³ In reality, the load capacitor also contributes parasitic resistance to G_p . However, its contribution is much less significant than that of the inductor. Here, for simplicity, the capacitor is taken as ideal.

Figure 3.14 Simplified schematic diagram of an active inductor [88]

By varying I_1 and I_2 , the required value of the inductor can be obtained. There are two limitations for this circuit. Firstly, it has poor linearity [88]. Secondly, the active inductor has poor noise performance. In general, active inductors are always noisier than passive inductors due to the active devices.

3.4 Review of Narrow-Band LNAs

Generally, according to the operation bands, LNAs can be divided into narrow-band LNAs, wideband LNAs and dual-band/multi-band LNAs. Narrow-band LNAs are widely used in wireless communications. It is suitable for single-function applications, such as GSM (900MHz, 1800 MHz or 1900MHz), GPS (1575MHz) and other single-band operation systems.

Recalling from Section 3.2 and Section 3.3, it is known that the source inductive degeneration input topology and LC parallel tuning load are commonly used in narrow-band LNA designs, so as to get a lower noise figure and enough gain with

lower power consumption. Through the LNA design, either a single-ended form or a differential form can be adopted. The differential architecture has better rejection of on-chip interference than its single-ended counterpart. However, it consumes twice the power and chip area for the same noise figure as the single-ended version. Typical single-band LNA designs and differential LNA designs are presented in [23, 62, 74-76, 78-80] and [1, 25-26, 84, 89], respectively.

3.5 Review of Wideband LNAs

Wideband LNAs are useful for Gigabit-per-second (Gpbs) high data-rate optical communications, instrumentation, commercial industrial-scientific-medical (ISM) wireless applications, cellular telephone, as well as satellite receiver applications. Frequently, the wideband amplification circuit appears in three configurations: the feedback amplifying circuit, the balance circuit and the distributed circuit.

3.5.1 Feedback Circuit

Since Harold Black's invention in 1921, the negative feedback amplifier has been a powerful technique that enjoys wide application in analog circuits [90]. Feedback circuits have four merits: gain desensitization, terminal impedance modification, bandwidth modification and nonlinearity reduction. Due to these advantages, the feedback amplifying circuits are often used in wideband amplifiers.

Simple Feedback Circuit

Generally, there are two types of feedback techniques in LNA designs: one is resistive feedback; another is active feedback. Figure 3.15 shows a wideband

amplifier with resistive feedback [88]. The first stage is designed as a cascode stage (M1, M2). The output stage is a transimpedance structure. The feedback resistor R_2 as well as M3 and R_3 assures the flatness of the overall gain and provides a 50Ω output.

Figure 3.15 A wideband LNA using resistive feedback [88]

Figure 3.16 A wideband LNA with active feedback [91]

Figure 3.16 illustrates a wideband LNA [91] with active feedback. The core of the circuit consists of three cascaded common source stages (M0, M1 and M2) to provide a higher gain. The active feedback network is composed of M3, R_4 , R_{f1} and R_{f2} . Compared to Figure 3.15, this multi-stage design guarantees a high reverse isolation, preventing LO-leakage from feeding through to the LNA's input. The -3dB bandwidth of this amplifier ranges from 420 MHz to 1.2 GHz [91].

Figure 3.17 A Darlington amplifier [92]

Darlington Amplifier

Figure 3.17 presents a Darlington low noise amplifier [92]. The first stage acts as a low noise common-emitter amplifier stage. Its size and bias determine the noise figure of the overall 2-stage amplifier. The second stage of the Darlington feedback amplifier provides wideband gain and output drive capability. A feedback resistor R_{f2} , coupled from the emitter of Q2 to the base of Q1 is used to realize a tradeoff between wideband minimum noise matching and input impedance matching.

3.5.2 Common Gate Input Topology Wideband LNA

The common gate input stage configuration can be used to achieve wideband input matching, owing to the fact that $1/g_m$ is constant over a large frequency range. If Q1 in Figure 3.17 is changed to a common base configuration, wideband impedance matching from DC to microwave frequencies is achievable. It is attractive for applications such as test instrumentation, light-wave fiber optical communication, digital ICs and modulator ICs, where noise figure is not very critical.

Figure 3.18 A wideband LNA with balanced structure [93]

3.5.3 Balanced Circuit

The balanced topology uses two identical circuits to realize the wideband output. Figure 3.18 shows an example of a balanced wideband amplifier [93]. The topology allows optimum impedance control for gain flatness and provides design flexibility in achieving optimum noise match. Balanced amplifier units are also easy to cascade

with other units, since each unit is isolated by the coupler. Furthermore, even if one of the amplifiers fails to work, the balanced amplifier unit will still operate with reduced gain. The balanced amplifier is suitable for high power applications.

Figure 3.19 A simplified distributed amplifier [94]

3.5.4 Distributed Circuit

The distributed amplifier is a well-known monolithic-microwave integrated-circuit (MMIC) design technique. It has been intensively investigated and realized successfully for the past three decades for various applications using hybrid and monolithic technologies [94-95]. Results show that the distributed amplifier has good input/output matching, a comparatively wider frequency band and a better noise figure. The distributed circuit is therefore the ideal selection for wideband or ultra-wideband amplifiers.

A basic four-stage design would take the form shown in Figure 3.19 [94]. If the gate and drain-line inductors are matched, and the drain capacitance is made equal to

the gate capacitance, then the phases of the input and output currents will be synchronized. When the transmission line load is matched with the characteristic-impedance, it is equivalent to the infinite bandwidth transmission line with dissipation. The microwave signals transmit in the form of traveling wave in the transmission line. When the phase of the input line is the same as that of the output line, it amplifies the microwave signals successively through the active device. This is the wide band principle of the distributed circuit [95].

Most distributed amplifiers, since the early 1980s have been realized as MMICs on compound semiconductor technology (GaAs or InP). Recently, interests in MOSFET distributed amplifiers [96-100] have been fueled by the fast scaling of current CMOS technology. However, there are still obstacles in the realization of useful CMOS distributed amplifiers due to difficulties in realizing high- Q factor inductors and transmission lines in standard CMOS processes.

3.6 Review of Dual-Band/Multi-Band LNAs

As described in Section 3.1.3, the great development of wireless communication in the past decades results in many coexistent communication standards spanning the frequency range 800MHz–6GHz as shown in Figure 3.20. Therefore, the development of a cost-effective, multi-standard transceiver is necessary. The design of a dual-band/multi-band low noise amplifier is the first obstacle towards the design of a multi-standard receiver [101].

Figure 3.20 Receiving band distribution of current wireless communication standards in the range of 800MHz-6GHz

3.6.1 Switched Mode Dual-Band/Multi-Band LNA

There are a number of approaches for the design of a multi-mode LNA. The first approach is switched mode LNA, as shown in Figure 3.21 [10]. The LNA can operate at WCDMA mode or GSM mode depending on the operational states of the transistors Q1, Q2, Q3 and Q4. In fact, the left half and the right half of the dual-band LNA are two single-band LNAs respectively. When Vb1 & Vb3 are high, and Vb2 & Vb4 are low, transistors Q1 & Q3 are turned on, while Q2 & Q4 are switched off. The dual-band LNA thus operates at WCDMA mode. Vice versa, the dual-band LNA will operate at GSM mode.

Figure 3.21 A switched mode dual-band LNA [10]

Figure 3.22 Another type of switched mode dual-band LNA [102]

The switched mode dual-band LNA shown in Figure 3.21 has some drawbacks. Firstly, when the LNA operates at one mode, although the other half of the circuit turns off, its existent capacitance and resistance can still have negative effect on the

working block. Thus, the performance might be degraded. For example, the frequency response can be shifted to the higher or lower frequency. Secondly, this type of LNA has two separate input matching networks and tuning load networks, which will consume much chip area.

Figure 3.23 A switched mode dual-band LNA3 [103]

Figure 3.22 illustrates another type of switched mode dual-band LNA [102]. In this topology, the separate input matching networks in the previous topology (Figure 3.21) are combined together, thus the transistor numbers are reduced. A similar method is also adopted for the output tuning loads. Hence, the circuit in Figure 3.22 is simple and compact to some extent. Figure 3.23 and Figure 3.24 illustrate more compact schematics [103-104]. The dual-band input matching network is simplified to a single-band input matching form, which is only viable when the high band and low band are close enough. For the output stage, there are still switches used to tune

the value of the capacitance (Figure 3.23)⁴ or the value of the inductance (Figure 3.24)⁵ so as to generate dual-band resonant loads.

Figure 3.24 A switched mode dual-band LNA4 [104]

Due to the easiness of implementation, the switched-mode approaches are widely used [10, 67, 79, 101-112]. However, there is one disadvantage. It is non-current, which means that this type of LNA can only work at one frequency band at a time. It can not amplify signals of two different frequency bands at the same time. It is not convenient when a simultaneous operation is required, e.g., a person is talking on a mobile phone on the frequency band of 1900MHz, while at the same time, he/she wants to exchange data stored on the mobile phone with the WLAN server on the frequency band of 5.15GHz–5.35GHz. Hence, the multi-function performance of switched mode dual-band LNAs is limited.

⁴ The tuning of the capacitance in Figure 3.23 is performed by a PMOS capacitor connected to the drain of M2. By biasing the PMOS in the strong inversion region and weak inversion region, the unit-area capacitance varies between C_{ox} and the series combination of C_{ox} and C_{dep} [90].

⁵ The tuning of the inductance in Figure 3.24 is realized through an NMOS switch.

3.6.2 Single-Band LNAs in Parallel

To enhance the multi-function performance, a concurrent dual-band LNA, which composes two single-band LNAs in parallel, is introduced [11, 68, 113-116]. This type of dual-band LNA is shown in Figure 3.25.

Figure 3.25 A dual-band LNA in a dual-band receiver [11]

Based on this approach, a multi-functionality system can be achieved by building multiple independent signal paths, at the cost of chip area and power consumption, as proposed by Akira Matsuzawa [5].

3.6.3 Wideband Multi-Mode Operation LNAs

The existing way to obtain multi-mode functionality is to use a wideband LNA, as described in Section 3.5. But the wideband LNA can introduce strong unwanted bands and significantly degrade the receiver's sensitivity [66, 117].

3.6.4 Concurrent Dual-Band/Multi-Band LNAs

From the above sections, it is known that the switched-mode LNA is either non-concurrent or working with two parallel input matching circuits and two output

resonant loads, which will cause great increase in cost, chip area and power consumption. Even the wideband LNA has its own drawbacks. This is why another type of dual-band/multi-band LNA, which is concurrent and highly-efficient, has to be developed.

Figure 3.26 Frequency response of a concurrent dual-band LNA [66]

Figure 3.27 A pseudo-concurrent multi-band LNA [117]

A concurrent dual-band LNA (2.4GHz and 5.2GHz), used for Bluetooth and wireless LAN applications was developed in the year 2002 [66]. This dual-band LNA achieves voltage gains of 14dB and 15.5dB at the lower band and the higher band respectively (Figure 3.26). It is designed based on 0.35 μ m CMOS technology with high- Q off-chip input matching components for better performance. Another type of dual-band LNA (Figure 3.27) is presented in [117] in the year 2003, also with off-chip input matching networks. However, its simulation results indicate that it does not have a good S-parameter performance. The performance will definitely be degraded further after fabrication, due to various parasitic resistance, capacitance and inductance. Therefore, it is not suitable for practical utilization. Another two concurrent dual-band LNAs are presented in Year 2004 [118]⁶ and Year 2005 [119]⁷ respectively, with almost the same architecture as [66]. Only simulation results are presented in [118] and [119].

From Year 2001, our research group has been conducting investigations of fully-integrated, dual-band LNA designs. Detailed analyses and designs will be presented in Chapter 6.

3.7 Summary

In this chapter, low noise amplifiers as well as the corresponding receiver architectures are introduced in order to have a better understanding of LNA designs.

⁶ The design of [118] adopts off-chip input matching and offers poor simulation gain (10dB), which practically will be worse after fabrication.

⁷ The design in [119] uses PHEMT transistor and a special substrate. The design provides poor S_{11} simulation results for the first band.

Four commonly-used input architectures in LNA designs are classified and examined.

Also, LNA load tuning techniques are explained. Based on the knowledge of input matching and output tuning load, operational characteristics of the designs of narrow-band LNAs, wideband LNAs and dual-band/multi-band LNAs are discussed.

In the later chapters, noise modeling and detailed LNA designs will be investigated.

Chapter 4 A Modified Input Architecture Used in CMOS Low Noise Amplifiers

In this chapter, in order to provide an accurate noise figure prediction during LNA design, the noise modeling of MOSFETs is firstly presented. Subsequently, some considerations in passive devices will be discussed, since the integrated inductors and capacitors are fundamental components in RF applications. Finally, an architecture used for input matching in CMOS LNAs will be investigated. In the proposed architecture, gate and source inductors, which are used in the traditional source inductive degeneration CMOS LNA, are either reduced or removed.

Figure 4.1 Input and output noise of a typical LNA

4.1 Noise Modeling of MOSFETs

As mentioned in Chapter 3, noise figure is one of the specifications to indicate the LNA's performance. In terms of the illustration in Figure 4.1, NF can be defined as:

$$NF = 10 \log_{10} F = 10 \log_{10} \left(\frac{A^2 \bar{v}_n^{-2} + \bar{v}_m^{-2}}{A^2 \bar{v}_n^{-2}} \right) \quad (4.1)$$

where $\bar{v}_m^{-2}$ is the output noise due to the amplifier itself. Thus, in order to get an accurate simulation result of RF CMOS circuits, the accuracy of the noise model for MOSFET is very important. But the accuracy of existing compact models for RF design is not satisfactory. The induced gate noise of the MOSFET, which plays an important role in determining the fundamental limits of noise performance for LNAs, is not included in standard MOSFET models, with the exception of the Philips MOS9, MOS11 and BSIM4 models [120]. To incorporate the induced gate noise of the MOSFET into our simulation, equations developed by Lee [41] will be used to generate the noise parameters for the MOSFET.

Figure 4.2 Description of noise sources in a MOS transistor [121]

In a MOS device, the prominent noise sources are drain channel noise $\bar{i}_{n,d}^2$, gate induced noise $\bar{i}_{n,g}^2$, distributed gate resistance thermal noise, substrate thermal noise and $\bar{i}_{n,cor}^2$, which is the correlation between $\bar{i}_{n,g}^2$ and $\bar{i}_{n,d}^2$ (Figure 4.2 and Figure 4.3).

Figure 4.3 An equivalent circuit to illustrate noise sources in a MOSFET

Figure 4.4 Cross section of a MOSFET channel divided into a gradual channel region

(I) and the velocity saturation region (II)

4.1.1 Channel Thermal Noise

As described in Chapter 2, the channel thermal noise comes from the random motion of the carriers in the device channel. It can be calculated by the well-known Klaassen-Prins Equation [122]:

$$S_{I_D}(f) = \frac{1}{I_D L_{elec}^2} \int_{V_{SB}}^{V_{DB}} 4kTg_0^2(V)dV \quad (4.2)$$

where $L_{elec} = L_{eff} - \Delta L$, as shown in Figure 4.4, which includes the channel length modulation effect. When the velocity saturation effect is taken into account, Equation (4.2) can be rewritten as [44]:

$$S_{I_D}(f) = \frac{1}{I_D L_{elec}^2 \left(1 + \frac{V_{DS}}{L_{elec} E_C}\right)} \int_0^{V_{DS}} 4kTg_0^2(V) \left(1 + \frac{E}{E_C}\right) dV \quad (4.3)$$

where E_C is the critical field at which the carrier velocity becomes saturated. It was argued recently that the possible noise contribution of the pinch-off region is negligible [44, 120, 123]. Equation (4.3) can be simplified to:

$$\overline{i_{n,d}^2} \cong \frac{4kT_0}{L_{elec}^2} \mu_{eff} Q_{inv} \Delta f \quad (4.4)$$

Note that the channel length used in this equation is L_{elec} , not the one L_{draw} used in [124-125], which can generate significantly different results. ΔL can be calculated based on [124]:

$$\Delta L = \frac{1}{\alpha_1} \ln \left[\frac{\alpha_1 (V_{ds} - V_{dssat}) + E_D}{E_{crit}} \right] \quad (4.5a)$$

$$E_D = E_{crit} \sqrt{1 + \left[\frac{\alpha_1 (V_{ds} - V_{dssat}) + E_D}{E_{crit}} \right]^2} \quad (4.5b)$$

$$\alpha_1 = \lambda \sqrt{\frac{3}{2} \frac{C_{ox}}{x_j \epsilon_{si} \epsilon_0}} \quad (4.5c)$$

where x_j is the junction depth of the source and drain region; C_{ox} is the gate oxide capacitance and λ is a fitting parameter to adjust the channel length modulation. Channel thermal noise is often expressed using the so-called “white noise gamma factor” γ [40]:

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \quad (4.6)$$

Figure 4.5 γ characteristics in [44, 120 and 123]

As shown in Figure 4.3, an equivalent drain current thermal noise $\overline{i_{n,d}^2}$, in parallel with the channel, is used to represent the total channel thermal noise. It is known that for long-channel MOSFETs, γ satisfies the inequality $2/3 \leq \gamma \leq 1$. The value of $2/3$ holds when the MOSFET operates in the saturation region, whereas the value of 1 holds when the drain bias is zero [40]. For short-channel MOSFETs, γ will increase. As presented in Chapter 2, the amount of the increase is still controversial [43-44]. Adibi presents a γ of 7.98 (a factor of 12 enhancement with respect to the long-channel value) at a bias of $V_{GS} = 1$ V and $V_{DS} = 4$ V [126]. Recent research shows

that γ is around 1-2 for a short-channel device [44, 120, 123]. Figure 4.5 illustrates several examples of γ versus V_{DS} , channel length and V_{GS} .

Figures 4.5 (a) and (b) present γ versus V_{DS} at the constant gate voltage of 1.8V and 0.6V, respectively. In the linear region, γ is nearly independent of channel lengths. At high gate bias, V_{DSSAT} becomes small due to velocity saturation effect, which causes the increase of the drain thermal noise. In the saturation region, γ increases moderately at low gate voltage with drain bias, which is attributed to channel length modulation effect. Figures 4.5 (c) and (d) indicate that, with the scaling of channel length, γ has a significant increase in the saturation region.

Generally, Figure 4.5 shows, at intermediate channel lengths, γ is close to the classical value of 2/3. Short channels show some enhancement of γ . Recent researches indicate that usually the contribution of hot carriers can be neglected, and the increase of γ is mainly due to short channel effects such as velocity saturation and channel length modulation [43-44, 123]. Thermal noise of parasitic resistance might be another source leading to the increase of γ [120]. The increase of γ (Figure 4.5 (c)) for longer channel length is due to the nonquasi-static effect [120].

In most MOSFET SPICE models, the following equation is widely used in noise simulation [124]:

$$\overline{i_{n,d}^2} = \frac{8}{3} kT (g_m + g_{ds} + g_{mb}) \Delta f \quad (4.7)$$

4.1.2 Gate Current Noise

Another source of noise contribution that may be overlooked is the noise coming from the gate, which includes gate resistance thermal noise and gate induced noise.

Gate Resistance

At high frequencies, MOSFET must be considered as an RC distributed network, with the capacitive coupling to the gate representing the distributed capacitance, and the channel itself representing the distributed resistance [40], as illustrated in Figure 4.6. In many RF applications, devices with very large gate widths are used. In such cases, gate resistance effects can be very significant. The gate resistance can be decomposed into two components: the distributed gate electrode resistance ($R_{g\text{eltd}}$), and the channel-induced gate resistance ($R_{g\text{ch}}$), which is the distributed channel resistance seen from the gate. The overall resistance is:

$$R_G = R_{g\text{eltd}} + R_{g\text{ch}} \quad (4.8)$$

Figure 4.6 Illustration of distributed nature of the gate electrode resistance $R_{g\text{eltd}}$, channel resistance R_{ch} and gate capacitance C_{ox}

(1) Distributed Gate Electrode Resistance

Considering the distributed network in Figure 4.6, in the case where the gate electrode is contacted only on one side, the network has been solved analytically

using transmission line theory [127]. Defining $Y_{g\text{eltd}}$ as the admittance towards the gate from the contact point, then [127-128]:

$$Y_{g\text{eltd}} = j\omega(C_{gs} + C_{gd}) \tanh[j\omega R_{\text{eltd}}(C_{gs} + C_{gd})] / [j\omega R_{\text{eltd}}(C_{gs} + C_{gd})] \quad (4.9)$$

where R_{eltd} is the dc resistance for the portion of the gate electrode on top of the gate oxide, which is given by:

$$R_{\text{eltd}} = R_{\text{sqr}} W / L \quad (4.10)$$

R_{sqr} is the sheet resistance of the polysilicon. W is the total gate width of the device. L is the gate length. Equation (4.9) can be expanded as:

$$Y_{g\text{eltd}} = j\omega C_g [1 - \frac{1}{3} j\omega R_{\text{eltd}} C_g + \frac{2}{15} (j\omega R_{\text{eltd}} C_g)^2 - \dots] \text{ with } C_g = C_{gs} + C_{gd} \quad (4.11)$$

Generally, there is $\omega R_{\text{eltd}} C_g \ll 1$. The first order approximation of (4.11) is,

$$Y_{g\text{eltd}} = j\omega C_g \frac{1}{1 + \frac{1}{3} j\omega R_{\text{eltd}} C_g} \Rightarrow Z_{g\text{eltd}} = \frac{1}{3} R_{\text{eltd}} + \frac{1}{j\omega C_g} \quad (4.12)$$

In general, the first order approximation is accurate enough for most of the applications in gigahertz. If the gate electrode is connected on both sides, the equivalent resistance then changes to $R_{\text{eltd}}/12$. When the layout of the MOSFET adopts interdigitation structure, let N be the finger number, then the gate electrode resistance can be represented as:

$$R_{g\text{eltd}} = \frac{1}{12N} R_{\text{eltd}} = \frac{1}{12N} \frac{R_{\text{sqr}} W}{L} + \frac{1}{2N} \frac{R_{\text{via}}}{N_{\text{via}}} \quad (4.13)$$

where R_{via} is the resistance of a metal1-to-polysilicon contacts and N_{via} is the number of such contacts.

(2) Gate Resistance R_{gch} due to Non-Quasi Static Effect

At very high frequencies, the MOSFET will manifest the non-quasi-static effect. For example, placing an ac excitation voltage source v_g at the gate in a quasi-static (QS) model, the channel charge is assumed to be a unique function of the instantaneous biases, i.e., the charge has to respond to a change of v_g with infinite speed. Thus, the finite charging time of the carriers in the inversion layer is ignored. The resulting effect is modeled by connecting a capacitance C_{gs} from source to gate. In reality, at high frequencies, the carriers in the channel do not respond to the signal immediately, and hence, the variation of channel charge will have some delay. It is called non-quasi static (NQS) effect [128]. A resistance R_{gch} is used to determine the time constant of the non-quasi static effect. R_{gch} is modeled as [128]:

$$R_{gch} \approx \frac{1}{5g_m} \quad (4.14)$$

Figure 4.7 Terminal resistance of NMOS with $L = 0.18 \mu\text{m}$, $W_f = 8 \mu\text{m}$ and $N_f = 25$

Gate Resistance Thermal Noise

The presence of gate resistance is undesired, because it reduces the overall transconductance, degrades the quality factor of the input stage and contributes

additional thermal noise to the devices. The thermal noise of the distributed gate electrode resistance $R_{g\text{eltd}}$ is:

$$\overline{i_{g\text{eltd}}^2} = 4kT\Delta f / R_{g\text{eltd}} \quad (4.15)$$

$R_{g\text{eltd}}$ can be reduced by proper layout, such as interdigitation and connecting the gate from both sides. Using salicided poly-gate or new metal-gate techniques will lower $R_{g\text{eltd}}$ as well [128]. $R_{g\text{eltd}}$ is about several ohms for typical applications, as shown in Figure 4.7.

Figure 4.8 Channel thermal noise capacitive coupling to the gate causes induced gate noise

Gate Induced Noise

At high frequencies, local channel voltage fluctuates due to the coupling of thermal noise to the gate through the oxide capacitance. As a result, induced gate noise current is produced (Figure 4.8). Van der Ziel's derived [40]:

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}, \text{ and } \overline{i_{n,g}^2} = 4kT \delta g_g \Delta f = 4kT \delta \frac{\omega^2 C_{gs}^2 \Delta f}{5g_{d0}} \quad (4.16)$$

where δ is a bias-dependent factor that is equal to 4/3 for a long-channel device in saturation. Similar to γ , δ also increases with the scaling of channel length. Generally, δ is considered as twice of γ [23]. Note that the ratio of δ/γ (around 2) remains approximately independent of the channel length [129]. This noise current can be modeled by a single noisy current source $\overline{i_{n,g}^2}$ in parallel with C_{gs} , as shown in Figure 4.3. Since both the induced gate noise and the drain thermal noise have the same physical origin, they are correlated. A correlation coefficient can be defined [40]:

$$c = \frac{\overline{i_{n,g} i_{n,d}^*}}{(\overline{i_{n,g} i_{n,g}^*} \cdot \overline{i_{n,d} i_{n,d}^*})^{1/2}} \quad (4.17)$$

It has a theoretical value of $\pm 0.395j$ for long-channel devices. Its sign depends on the adoption of the reference polarity for the drain current noise [42]. With this coefficient, the induced gate noise can be divided into two parts:

$$\begin{cases} \overline{i_{n,g,u}^2} = 4kT \delta g_g \Delta f (1 - |c|^2) & \text{uncorrelated} \\ \overline{i_{n,g,c}^2} = 4kT \delta g_g \Delta f |c|^2 & \text{correlated} \end{cases} \quad (4.18)$$

Frequency dependence and scaling of the correlation coefficient has recently been investigated using device noise simulations. Contradictory results have been reported. In [130], it is shown that both the imaginary and real parts are frequency-dependent. The real part is negative and tends to be zero at low frequency. At a given positive frequency, its value tends to decrease when reducing the channel length. On the other hand, the imaginary part of c is positive and tends to increase when reducing the channel length. While the results published in [131] show that the correlation factor remains mainly imaginary (the real part is about ten times smaller than the imaginary

part) and that its value is slightly smaller than the long-channel value of 0.4 for short-channel devices [131]. Another study has compared the results obtained from drift-diffusion (DD) and hydro-dynamic (HD) simulations [129]. [129] indicates both

Figure 4.9 Correlation coefficient [120]

DD and HD models produces an increase in the correlation factor up to a value between 0.7 and 0.8 for the same device. Today, it is hard to draw any conclusions from these simulation results. The only observation that can be made from these different results is that for frequencies far below the cutoff frequency (typically ten times lower), the correlation coefficient remains mainly imaginary [43]. Figure 4.9 presents the correlation coefficient for

transistor lengths of 1 μm, 0.5 μm and 0.18 μm respectively.

Yannis [128] points out that the gate-induced noise can be estimated by assuming that R_{gch} produces the same amount of thermal noise as an actual resistor of value R_{gch} (Figure 4.10 (a)):

$$\overline{v_{n,g}^2} = 4kT\Delta f R_{gch} \approx 4kT\Delta f / 5g_m \quad (4.19a)$$

Figure 4.10 Equivalent circuit of gate-induced noise source

In its equivalent circuit in Figure 4.10 (b), $\overline{i_{n,g}^2}$ can be derived and expressed as:

$$\overline{i_{n,g}^2} = \overline{v_{n,g}^2} / \left| R_{gch} + 1/(j\omega C_{gs}) \right|^2 \approx \delta \frac{4kT\Delta f}{5g_{d0}} / \left[(R_{gch})^2 + \frac{1}{\omega^2 C_{gs}^2} \right] \approx 4kT\delta \frac{\omega^2 C_{gs}^2 \Delta f}{5g_{d0}} \quad (4.19b)$$

where δ is a fitting factor. Equation (4.19b) agrees well with Van der Ziel's expression in Equation (4.16).

4.1.3 Source and Drain Terminal Resistance Thermal Noise

Apart from the above intrinsic noise sources, various parasitic elements contribute to the overall noise measured at the terminals of the MOSFETs. These types of noise sources include drain/gate/source terminal resistance thermal noise. They are expressed as follows:

$$\overline{i_D^2} = 4kT\Delta f / R_D \quad (4.20a)$$

$$\overline{i_s^2} = 4kT\Delta f / R_s \quad (4.20b)$$

In practice, terminal resistance can be reduced through multi-finger layout. As illustrated in Figure 4.7, for an NMOS transistor with $L = 0.18\mu\text{m}$, $W_f = 8\mu\text{m}$ and $N_f = 25$, based on the CSM (Chartered Semiconductor Manufacturing) $0.18\mu\text{m}$ CMOS technology, the terminal resistance of source and drain can be reduced to

around 1 ohm. Hence, their noise contributions can be reduced as well. The gate electrode resistance is larger than R_D and R_S . Its typical value is 3-5 ohms.

4.1.4 Substrate Resistance Thermal Noise

The influence of the substrate resistance is usually ignored in compact models for low frequency application. However at high frequency, the signal at the drain couples to the source and bulk terminals through the source/drain junction capacitances and substrate resistance. The substrate resistance influences output characteristics and can contribute as much as 20% of the total output admittance [132]. It contributes noise as well.

Figure 4.11 Cross section of an NMOSFET

Substrate components become distributed at high frequency. It is too complex to model the substrate using a distributed RC network in a compact model. A good compromise is to use a lumped RC network, to simulate the contribution of the substrate components in the required operating frequency range. It is shown in Figure 4.3 and Figure 4.11. It is found that the three-resistor substrate network can ensure good modeling accuracy in a frequency range up to 10GHz [132]. Generally,

assuming the device is symmetric between source and drain and there is no difference between the outer and inner source/drain regions in a multi-finger device:

$$R_{DSB} = \frac{r_{dsb} L_f}{N_f W_f} \quad (4.21a)$$

where r_{dsb} is the sheet resistance in the substrate between the source and drain. R_{SB} and R_{DB} are functions of the channel width of the device. They are described approximately as:

$$R_{DB} \approx \frac{r_{dbw}}{W_f} \quad (4.21b)$$

$$R_{SB} \approx \frac{r_{sbw}}{W_f} \quad (4.21c)$$

where r_{dbw} and r_{sbw} are the substrate resistance per unit-channel-width under the drain region and source region respectively.

An accurate calculation of the substrate noise source is complex. A qualitative representation is simply expressed as [133]:

$$\overline{i_{n,dB}^2} = 4kT\xi \frac{d}{W} g_{mb}^2 \Delta f \quad (4.22)$$

where ξ is a constant; d is the space size between gate and bulk contact; W is the gate width and g_{mb} is the bulk transconductance which depends on the bulk to source voltage V_{BS} .

4.1.5 Additional Drain Current Noise

Figure 4.12 illustrates the noise contributions to drain current noise in bulk MOSFETs [46]. In the figure, the solid line is total noise power; the circle-symbol line is the $1/f$ noise component; the triangle-symbol line is the noise induced by

substrate, and the diamond-symbol line is the channel thermal noise. The figure indicates that in low frequencies, drain current noise only exhibits $1/f$ noise, which corresponds to Region I. As frequency becomes much higher than ω_T , the capacitive coupling between the channel and gate makes propagation of local fluctuations in the channel stronger. Consequently, the output current noise increases as shown in Region IV. The substrate network also influences the quantity of the drain current noise. The fluctuations in the substrate potential (due to the substrate resistance) modulate the channel charge of the depletion capacitor (C_{dep}) and subsequently produce additional current noise ($S_{id,sub}$) amplified by g_{mb} . Since the $R_{sub}C_{depl}$ network in Figure 4.12 acts as a low-pass filter, the amount of additional channel noise is given by [46]:

Figure 4.12 Noise contribution of bulk MOSFETs [46]

$$S_{id,sub} = \frac{4kTR_{sub}g_{mb}^2}{1 + (\omega R_{sub}C_{dept})^2} \quad (4.23)$$

This equation suggests that $S_{id,sub}$ has a low frequency noise plateau ($4kTR_{sub}g_{mb}^2$) dominating Region II and has a pole at $f = (2\pi R_{sub}C_{dept})^{-1}$. Thus, $S_{id,sub}$ effectively increases the drain current noise factor γ in low frequency band.

Figure 4.13 Effect of inductor Q factor on circuit performance: (a) an LNA; (b) noise performance; (c) power gain performance.

4.2 Considerations in Passive Devices

RFIC designs are characterized by the use of active transistors as well as many passive components, such as inductors, capacitors, varactors and resistors. However,

since most mainstream CMOS processes have evolved to satisfy the demands of digital electronics, RFIC designers need to have an in-depth understanding of the characteristics of passive components implemented in CMOS process in order to apply them effectively. In this section, designs of inductors and capacitors will be presented.

4.2.1 Inductor Design

Integrated inductors can be implemented using package bondwire or on-chip metal spirals. The quality factor (Q) of the inductor is one of the key factors to determine an RF circuit's performance. For example, high- Q inductors can lead to improved power or figure of merit in low noise amplifiers (as shown in Figure 4.13), lower insertion loss in bandpass filters, and better phase noise and power in the voltage controlled oscillator (VCO). Practically, bondwire inductors have higher Q (in the range of 20-50) than on-chip spiral inductors. However, bondwire inductors are only available at the edge of the die, and the value of inductance varies, depending on the choice of package and size of the die [134]. On the other hand, planar spiral inductors have limited Q , but have inductances that are well-defined over a broad range of process variations.

A practical inductor is specified by its inductance, quality factor, and self-resonant frequency. The impedance of a real inductor increases with frequency until it reaches self-resonance caused by the parasitic capacitance of the inductor. Beyond the self-resonant frequency, the inductor behaves like a capacitor and the

impedance decreases with frequency. The value of an inductor is measured by Q which is defined as [135]:

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} = \frac{\text{Im}(Z_L)}{\text{Re}(Z_L)} \quad (4.24)$$

For an inductor, only the energy stored in the inductor's magnetic field is of interest. Any energy stored in the inductor's electric field because of the parasitic capacitance, is counterproductive [136]. Hence, Q reduces to zero at the self-resonant frequency when the peak magnetic energy and electric energy are equal.

Figure 4.14 On-chip spiral inductor realization: (a) square; (b) octagonal; (c) hexagonal; (d) circular.

A. Spiral Inductors

Figure 4.14 shows the top views of the most popular on-chip spiral inductors (square, octagonal, hexagonal and circular). The majority of the spiral is formed by the top metal layer, and a second metal layer is used to bridge out the other end from the centre to make the connection. For a given shape, an inductor is specified by the number of turns n , the turn width, the turn spacing S , the oxide thickness, the conductivity of the substrate, the outer diameter and the inner diameter [134].

B. Non-Ideality of the Spiral Inductors

The inductance of a spiral inductor comes from the self inductance of each segment in the spiral as well as the mutual inductance between any two segments. However, many non-idealities, such as metal ohmic loss, skin effects, eddy current effects and parasitic capacitance, degrade the inductor's performance.

(1) Metal Ohmic Loss

The dc resistance of a spiral, which is equal to the metal layer's resistance, is calculated by:

$$R_{dc} = R_{sh} \frac{\text{total length of the spiral}}{W} \quad (4.25)$$

where R_{sh} is the sheet resistance of the metal layer and W is the width of the spiral.

(2) Skin Effect

At high frequencies, the current tends to flow toward the surface; therefore, the overall resistance of the metal spiral increases. The sheet resistance can be calculated as [137]:

$$R_{ac} = \rho / \delta_s \text{ (}\Omega/\text{square)} \text{ and } \delta_s = \sqrt{\frac{\rho}{\pi f \mu_r \mu_o}} \quad (4.26)$$

where ρ is the resistivity of the metal; f is the frequency; μ_r and μ_o are the relative permeability and permeability of the surrounding material, respectively. δ_s is called the skin depth, which is the figure of merit to characterize the skin effect of the metal. If δ_s is much larger than the thickness of the metal, then the skin effect has little influence on the overall resistance. Equation (4.26) indicates that R_{ac} is proportional to $f^{1/2}$. Therefore, skin effect can contribute significant loss at high frequencies in the spiral inductors.

Figure 4.15 Parasitic capacitance and resistance network for an on-chip spiral inductor.

(3) Parasitic Capacitance

In spiral inductors, there is parasitic capacitance between the metal layer and substrate. In addition, parasitic capacitance is also formed in the substrate, as shown in Figure 4.15. The latter complicates the estimation of the total capacitance between

the spiral and the reference ground. Another source is the inter-winding capacitance, which is not very significant in most cases if the size of the spiral is small compared with the wavelength, because the phase delay between two adjacent segments is negligible. The distributed RC network in the lossy silicon substrate is one of the major causes for Q degradation [138].

(4) Eddy Current Effect

In the spiral inductor, the spiral is on top of a ground plane, and the magnetic field will cause current to circulate on the ground plane. This effect can be modeled by considering an equally-sized image inductor on the other side of the plane with a current flowing in the opposite direction. The net effect is that the inductance will be reduced due to the negative mutual inductance between the original and the image inductors. On lossy silicon substrate, the eddy current not only degrades the overall inductance but also introduces additional loss on the path of the circulating current.

C. Techniques to Improve the Performance of the Spiral Inductors

Energy losses in the silicon substrate result from I^2R losses (due to the currents flowing through the metal to the substrate capacitance) and those generated due to the magnetic field induced by the inductor. These losses can be eliminated by either shorting the substrate or making it open. One approach suggested by Yue and Wong [136] is the use of patterned ground shield that can reduce the induced loop current by insertion of slots in the shield. The main drawback of this technique is that the parasitic capacitance to the substrate is significantly increased. Patterned ground

shields are effective for lower frequency applications where the parasitic capacitance can be absorbed in the LC tank. Increasing the substrate resistance is another approach that is useful for reducing substrate losses. The use of high resistivity silicon [139] and sapphire substrates have been used by researchers to demonstrate high- Q planar inductors, thus achieving quality factors of 40 at 5.8 GHz for a 1.4-nH inductor [140]. However, the use of high resistivity material is not common in a digital logic CMOS process, and many submicron CMOS technologies use epitaxial silicon wafers. Substrate removal is a method of choice for large area inductors. It can improve self-resonant frequency and extend usable frequency range. But substrate removal needs extra processes step, which will definitely increase the manufacturing cost. Researchers also aim to integrate MEMS (Figure 4.16) or 3D inductors using customized fabrication techniques [141-143].

Figure 4.16 Conceptual schematic of integrated RF circuits with on-chip MEMS inductors [143]

There are also some other techniques that are used to enhance the performance of the inductor. The proposed techniques include the use of higher conductivity metal layers, for instance: copper is used to reduce the lossy resistance of the inductor [144] and multi-metal layers are used to increase the effective thickness of the spiral inductor and thereby reduce loss [145-146]. As no special process is required, the technique of multi-layers is widely used.

D. Design of the Spiral Inductors

Besides the process technology, the performance of the inductor is also influenced by the shape of its layout (Figure 4.14). Here, the designs of circular integrated inductors are our main concerns. It has been reported that circular inductors exhibit better quality factors than square integrated ones at the expense of a slight increase in area [145]. Circular spiral inductors perform 20-30% better than rectangular spiral inductors [147], because rectangular inductors suffer loss caused by scattered currents at the corners. Another technique for improving the inductor Q involves removing the inner turns [134]. These inner turns do not contribute much to the total inductance value, but they can significantly attenuate the magnetic field⁸ and enhance the skin effect. In addition, their resistance is higher than the resistance of other turns, although their length is smaller [147]. Therefore, circular spiral inductors, with hollowed inside holes for the purpose of obtaining an improved Q , will be chosen for our LNA designs.

⁸ The magnetic field is the strongest at the centre of the spiral, and would be attenuated by the inner turns.

With a 6-metal 0.18 μm standard CMOS process, two topmost metal layers are stacked together to improve the Q values. A maximum number of contacts is required between these two layers to reduce contact resistance. Figure 4.17 illustrates the inductor structure. The two metal layers used are top metal and metal 5. The diameter of the hollowed center core is 100 μm . The width of the metal stripe w and its spacing s are 12 μm and 1.4 μm , respectively.

Figure 4.17 Structure of the circular spiral inductor

Figure 4.18 Physical model of the inductor

The typical physical model of the spiral inductors with parasitic capacitance is shown in Figure 4.18 [41]⁹. L_s is the inductance, R_s denotes the series resistance of the inductor, i.e. the resistance of the metal line. L_s and R_s are modeled by Equations (4.27a) and (4.27b) [148]:

$$L_s = K_L \frac{A_r^{3/2}}{w^2} \eta_{Ar}^{5/3} \eta_w^\alpha \quad (4.27a)$$

$$R_s = \frac{\rho_{metal}}{t_{metal}} \frac{A_r}{w} \left(\frac{1}{w} + \frac{1}{\delta} \right) \eta_{Ar} \quad (4.27b)$$

The parameters are $K_L = 1.3e-7 H/m$; $\eta_w = \frac{w}{w+s}$; $\delta = \left(\frac{\rho_{metal}}{t_{metal}} \frac{K_R}{\omega_o} \right)^2$ and $K_R = 3.6 \cdot 10^9 \sqrt{m} \cdot Hz/\Omega$. η_{Ar} is the ratio of the metal area to the total area A ;

$\frac{\rho_{metal}}{t_{metal}}$ is the sheet resistance of the metal, and ω_o is the operational frequency. C_p represents the shunt capacitance that arises from the overlaps of the cross-under and the main spirals, and its value is determined by the overlapped area and the thickness of the oxide between the cross-under and the main spirals. The oxide capacitance C_{ox} between the spiral and the substrate is modeled as $C_{ox} = \frac{\epsilon_{ox} A}{t_{ox}}$, where ϵ_{ox} is the permittivity of SiO₂. $\epsilon_{ox} = K_{ox} \epsilon_0$ where ϵ_0 (8.854E-12F/m) is the permittivity of free space and K_{ox} (around 3.9) is the relative permittivity of SiO₂. A is simply approximated as the total area of the inductor. t_{ox} is the thickness of the oxide between the spirals and the substrate. R_1 and C_1 represent the substrate loss due to the substrate resistance and capacitance as well as the effect of the induced image current in the

⁹ Actually, there are more complicated models for the on-chip spiral inductors [133, 149].

substrate. R_1 and C_1 can be approximated as $R_1 \approx \frac{2}{w l G_{sub}}$ and $C_1 \approx \frac{w l C_{sub}}{2}$ [41].

G_{sub} and C_{sub} are fitting parameters that are constant for a given substrate. The typical value of G_{sub} and C_{sub} are $10^{-7} S/\mu m^2$ and $10^{-3}-10^{-2} fF/\mu m^2$, respectively [41].

Figure 4.19 and Figure 4.20 illustrate the measured results of inductance and Q for such implemented inductors with a turn number of 5 and 1, respectively. The figure indicates that the inductance and Q of the inductor are not constant for inductors with a large number of turns. They vary with frequency, for example, at 2.45GHz, the proposed inductor ($n=5$) in Figure 4.19 has an inductance of 5.77nH and a quality factor of 6.27. At 5GHz, the values change to 6.82nH and 5.5 respectively. This increases the difficulty of the design, especially for wideband and dual-band applications. On the other hand, it indicates that the use of large inductors should be avoided.

Figure 4.19 Measurement result of a circular spiral inductor

Figure 4.20 Measurement result of a one-turn circular spiral inductor [149]

4.2.2 Capacitor Design

Four types of capacitors have been commonly used in IC design: gate capacitors, junction capacitors, conventional metal-to-metal/poly capacitors, and thin-insulator capacitors. Gate capacitors have high density (high capacitance per unit area), but they are nonlinear and require a dc bias voltage to operate. Due to the thin gate oxide, gate capacitors have a low breakdown voltage. They also have a medium quality factor (about 7 at 1 GHz for a 2pF capacitor) [150]. Junction capacitors suffer from some of the above problems as well. They are highly nonlinear and they also need a dc bias voltage. Besides that, their sensitivity to process variations, poor quality factor and large temperature coefficient limit their application. Metal-to-Metal and metal-to-poly capacitors, on the other hand, are more linear, and have higher quality factors as well as smaller temperature variations. The capacitance is given by:

$$C_p = \epsilon \frac{WL}{d} \quad (4.28)$$

where ϵ is the permittivity of the dielectric; W and L are the width and length of the capacitor's plate respectively; d is the separation distance between the top and bottom plates. The metal-oxide-metal (MOM) capacitor has a lower capacitance density compared to the MOS capacitor and poly-poly capacitor due to the rather thick inter-level dielectric. Usually, a sandwich structure made of available metal layers is used to reduce the area and increase capacitance (Figure 4.21). In most cases, a metal-insulator-metal (MIM) capacitor is used instead.

Besides the MIM-CAP (Metal/Si₃N₄/Metal), there are two other types of linear capacitors described in the CSM 0.18 μ m CMOS process: PIP-CAP (Poly/SiO₂/Poly) and Hi-PIP-CAP (Poly/SiO₂/Poly). All the three types have high-densities (1.55fF/ μ m² for PIP-CAP, 2.5fF/ μ m² for HI-PIP-CAP, and 1.15fF/ μ m² for MIM-CAP). The Hi-PIP-CAP has a lower accuracy with a tolerance of 15%. Although PIP-CAP has a tolerance of 10%, it has a higher parasitic capacitance to substrate (15%). Comparatively, MIM-CAP has a high capacitance density, a high accuracy and a low parasitic capacitance to substrate (2.6%).

Figure 4.21 Capacitor using sandwich structures

Figure 4.22 Structure of an MIM capacitor

In our design, the MIM capacitors are adopted. The MIM capacitor is a plug-in module inserted between the last two metal layers. The fused top layer, which defines the top plate of MIM capacitor, is an additional metal layer inserted between the last two metal layers; whereas the bottom plate is the second last metal layer (M5 in our design). MIM capacitors use a thin oxide to achieve high density. The capacitance density is much higher than the density of a standard metal-oxide-metal capacitor. Because the two layers are far from the substrate, the ratio of parasitic capacitance to inter-plate capacitance will be much lower than other structures. The structure and layout of the MIM CAP are illustrated in Figure 4.22.

Figure 4.23 Model for MIM capacitor [149]

Figure 4.23 shows the corresponding model for the MIM capacitor. In the model, C_p is the main capacitor associated with Equation (4.28). L_s and R_s represent the parasitic inductance and resistance, which come from the interconnections and the metal plates. R_a and C_a (R_b and C_b) are parasitics between the plates and the substrate.

Figure 4.24 shows the plot of the measured capacitance versus the frequency for an MIM capacitor with an area of $31.62\mu\text{m} \times 31.62\mu\text{m}$. The value is around 1.03pF below 3GHz and has an increase around 10% at 5GHz. Generally, the quality factor of the on-chip MIM capacitor is more than 100.

Figure 4.24 Measured capacitance of the MIM capacitor

4.2.3 Resistor Design

There are relatively few good resistor options in standard CMOS processes. For the CSM 0.18 μm CMOS process, the layers that can be used to implement resistors are N-well, N+, P+, and poly. N+ and P+ layers have low sheet resistance

(60 Ω /square for N+, 120 Ω /square for P+) but low accuracy (10% and 25% for N+ and P+, respectively). The N-well layer has high sheet resistance of 680 Ω /square and a tolerance of 19%. This type is chosen as the bias resistor whose values are not critical in the circuit. The poly resistor with a low sheet resistance of 65 Ω /square and a low tolerance of less than 10% is chosen to implement the resistors in the output buffer of the LNAs. The maximum current density of the poly resistor is 0.5mA/ μ m. The selection of the square width of the poly resistor should be based on the current flowing through and should give enough space to avoid resistor disruption. During implementation, for low sheet-resistance resistors, an N⁺CAP mask is required to define the high dose implant region on poly2; whereas for high sheet-resistance resistors, a resistor block layer is needed to define the high sheet resistors. Figure 4.25 illustrates the structures of these two types of resistors.

Figure 4.25 (a) The high sheet-resistance poly2 resistor; (b) the low sheet-resistance poly2 resistor.

4.3 A Modified Architecture Used for Input Matching in CMOS Low Noise Amplifiers

Described in previous chapters, CMOS technology has become a competitive technology for radio transceiver implementation due to its fast scaling, high level of integration and low cost. The LNA serves as the first amplification block in wireless receivers and plays an important role in the receiver's overall performance. An LNA is implemented using either off-chip components (especially inductors and capacitors) [23, 25 and 76] or large on-chip spiral inductors [151], which are bulky and costly. The rapid developing market demands communication devices with small size as well as low cost. To alleviate the above-mentioned problems, an architecture that can be used for input matching in CMOS low noise amplifiers is investigated in this section. In the proposed architecture, gate and source inductors, which are the basic components in traditional source inductive degeneration CMOS LNAs, are either reduced or removed.

Figure 4.26 Source inductive degeneration input stage

4.3.1 Traditional Source Inductive Degeneration Architecture

As presented in Chapter 3, the source inductive degeneration input architecture is widely used in LNA designs. According to Figure 4.26, its input impedance is expressed as:

$$Z_{in} \approx j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} + (g_{m1} / C_{gs}) L_s \quad (4.29)$$

To reach input matching, the real part of Equation (4.29) should be 50Ω , whereas the imaginary part should be zero at the frequency of interest:

$$(g_{m1} / C_{gs}) L_s = \omega_T L_s = 50 \quad (4.29a)$$

$$j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} = 0 \quad (4.29b)$$

The LNA's operating frequency ($\omega_0 = 1/\sqrt{(L_g + L_s)C_{gs}}$) can be derived from Equation (4.29b). Vice versa, when the operating frequency ω_0 and the transistor size are known, inductors L_s and L_g can be calculated as well. This is the input matching design rule for single-band LNAs. However, there is a drawback for this topology. In order to realize the series resonance with transistor M1's small gate to source capacitance C_{gs} (about 0.23pF for a 240 μ m/0.18 μ m NMOS transistor), the gate inductor L_g is usually too huge to be integrated on chip - 56nH in Zencir's work [152], 20nH in Gatta's work[25] and tens of nH in Shaeffer's work[23]¹⁰. This shows that a

¹⁰ Here, L_g in an LNA used for Bluetooth application can be calculated as an example. From Equation (4.29b):

$$L_g + L_s = \frac{1}{(2\pi f_0)^2 C_{gs}} \quad (4.29c)$$

large and high quality factor inductor is difficult to be implemented on chip with the current standard CMOS technology. Even if it is implemented, a considerably large chip area will be consumed.

A diameter of more than 250 μm using CSM 0.18 μm CMOS is required for a 10nH inductor. Moreover, to ensure the quality of the on-chip inductor, the distance between the inductor and any other components should generally be at least 50 μm . Otherwise, the coupling effect and other electro-magnetic effects can degrade the inductor's performance, especially at gigahertz frequency. In other words, it means that a 10nH inductor will occupy an area with a diameter of at least 350 μm . It is thus very costly. Furthermore, in LNA design, the quality factor (Q) of L_g must be high, because its parasitic resistance contributes to thermal noise [76]. For instance, for a 10nH on-chip inductor with $Q=7$ at 2.45GHz, the relative resistance is 22 Ω , which is 44 percent of the 50 Ω source resistance. It can lead to quite a large noise figure (NF) increment. Therefore, L_g is often used as off-chip solutions [23, 25 and 151], although this goes against the trend of system integration demanded by the competitive market. In short, the use of large-value inductors should be avoided, from either the perspective of system integration or NF improvement or chip area reduction.

Let the size of the transistor M1 (Figure 4.26) be 240 $\mu\text{m}/0.18\mu\text{m}$; then the gate to source capacitance $C_{gs} \approx \frac{2}{3}WLC_{ox}$ [128] is about 0.23pF [149]. Substituting $f_0=2.5\text{GHz}$ and $C_{gs}=0.23\text{pF}$ into Equation (4.29c), the sum of $L_g + L_s$ can be obtained, which is 17.6nH. Generally, the cut-off frequency f_T is higher than 10GHz, and according to Equation (4.29a), $L_s \leq 1\text{nH}$. Therefore, L_g has to be more than 16.6nH in this example. Miller effect adds a capacitive component in parallel with C_{gs} , and the final L_g is around 10nH, which is still very large.

4.3.2 The Proposed Input Architecture

There are several ways to reduce L_g . According to Equation (4.29), one way is to increase the input transistor's width W so as to increase C_{gs} ($C_{gs} \approx 2WLC_{ox}/3$ [128]). However, it will result in a large drain current I_d (corresponding to large power consumption). Although a low I_d can be obtained by decreasing the over-drive voltage V_{od} , practically, V_{od} is only fractional volt higher than the threshold voltage V_T . If V_{od} is reduced further, the circuit might not operate normally due to variations in the fabrication process.

Another method is to connect an additional capacitor C_d in parallel with C_{gs} [24]. But the quality factor of the input stage ($Q_L = 1/\{2R_S\omega_0(C_{gs} + C_d)\}$ [24]) will be degraded. As a result, the LNA's performance will be degraded as well. In our work, we want a modified architecture that will neither increase power consumption nor degrade Q_L .

Figure 4.27 An LC parallel network and its equivalent circuit

Considering the L_1C_1 parallel network illustrated in Figure 4.27 (a), its impedance can be derived and simplified as:

$$Z = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} = j\omega \left(\frac{L_1}{1 - \omega^2 L_1 C_1} \right) = j\omega \frac{L_1}{1 - (\omega/\omega_{01})^2} \quad (4.30)$$

where $\omega_{01} = 1/\sqrt{L_1 C_1}$ is the resonant frequency of the $L_1 C_1$ parallel network. To guarantee normal operation of the circuit, ω_{01} should be located outside the operating frequency band. It is easy to find that the $L_1 C_1$ parallel network is equivalent to an inductor L_2 where $L_2 = \frac{L_1}{1 - \omega^2 L_1 C_1} = \frac{L_1}{1 - (\omega/\omega_{01})^2}$. Under the condition of $0 < 1 - \omega^2 L_1 C_1 < 1$ (to ensure L_2 to be positive), $L_2 > L_1$, and as ω approaches ω_{01} , L_2 will be significantly larger than L_1 . Hence, a small $L_1 C_1$ parallel network can be expected to generate a large inductance and replace the large L_g .

Figure 4.28 Relation of the generated L_2 with frequency ($L_1=3.2\text{nH}$, $C_1=0.8/0.9/1.0\text{p}$)

Figure 4.28 shows a graph of L_2 versus frequency when $L_1=3.2\text{nH}$ and $C_1=0.8/0.9/1.0\text{pF}$, respectively. The figure indicates that at 2.45GHz , the $L_1 C_1$ parallel network can generate an inductance of 10nH when $L_1=3.2\text{nH}$ and $C_1=0.9\text{pF}$. Compared to the 10nH inductor, a 3.2nH inductor is easier to be implemented on-chip based on the current CMOS technology, and it consumes a chip area with a diameter

of only around $150\mu\text{m}$. The 0.9pF capacitor has an area of $30\mu\text{m} \times 30\mu\text{m}$, which is relatively small compared to that of the on-chip inductor. Table 4.1 summarizes the area consumption before and after C_1 is introduced. From the table, it can be seen that, compared to the large L_{g1} , the chip area of $L_{g2}C_1$ decreases significantly. The simulation results also indicate an improved input-reflection coefficient, as demonstrated in Figure 4.29.

Table 4.1 Comparison of the L_g parameter with/without C_1

	L_{g1} (without C_1)	L_{g2} (after C_1 is connected)
Effective inductance (nH)	10	10 ($L_1=3.2$)
Radius including the $50\mu\text{m}$ outside the inductor	$175\mu\text{m}$	$125\mu\text{m}$
Area (mm^2)	0.0962	0.0491
Area of C_1 (mm^2)	0	0.0009
Sum (mm^2)	0.0962	0.0500
Saved area (%)	0	48

Figure 4.29 Simulated S_{11} @ $L_{g1}=10\text{nH}$ (without C_1); $L_{g2}=3.2\text{nH}$, $C_1=0.9\text{pF}$.

4.3.3 The Proposed Input Architecture with Realistic On-Chip Inductors

In the analyses of the previous section, the parasitic resistance of the inductor L_1 is ignored. In practice, the on-chip spiral inductor suffers from metal ohmic loss, parasitic capacitive loss and eddy current loss, as presented in Section 4.2.1. In our case, for analytical simplicity, the inductor is simply modelled as an ideal inductor in series with its parasitic resistance. This is feasible when the spiral inductor is implemented with the top metal and has a relative small size¹¹. Hence, Figure 4.27 can be modified into Figure 4.30.

Figure 4.30 Modified LC parallel network and its equivalent circuit

Consequently, Equation (4.30) should be rewritten as:

$$Z = R_{p2} + j\omega L_2 \quad (4.31)$$

$$\text{where } R_{p2} = \frac{R_{p1}}{(1 - \omega^2 L_1 C_1)^2 + (\omega C_1 R_{p1})^2} \approx \frac{R_{p1}}{(1 - \omega^2 L_1 C_1)^2} = \frac{R_{p1}}{(1 - (\omega / \omega_{01})^2)^2} \quad (4.31a)$$

$$L_2 = \frac{L_1 - \omega^2 L_1^2 C_1 - C_1 R_{p1}^2}{(1 - \omega^2 L_1 C_1)^2 + (\omega C_1 R_{p1})^2} \approx \frac{L_1 - \omega^2 L_1^2 C_1 - C_1 R_{p1}^2}{(1 - \omega^2 L_1 C_1)^2} \approx \frac{L_1}{1 - (\omega / \omega_{01})^2} \quad (4.31b)$$

$$\omega_{01} = 1 / \sqrt{L_1 C_1} \quad (4.31c)$$

¹¹ Here, also for simplicity purpose, the on-chip capacitor is considered as ideal. Practically, the quality factor of the on-chip capacitor is more than 100. Therefore, the influence of its parasitic is relative un-significant compared with the parasitic of the on-chip inductor.

Due to the influence of the parasitic resistance R_{p1} , the value of L_2 is decreased a little. The simplification of Equation (4.31a) and Equation (4.31b) are reasonable for estimation. Figure 4.31 gives a detailed illustration of $L_1=3.2\text{nH}$ ($Q=10$) and $C_1=0.9\text{pF}$. The figure shows that, at 2.45GHz , $L_{2_simplify}$ is around 10nH , while L_2 is around 9.4nH , which indicates a 6% difference. The figure also shows that a high inductance can still be achieved with a small on-chip L_1C_1 parallel network, even if L_1 is not an ideal inductor. Using the L_1C_1 parallel network (Figure 4.30) to replace the large gate inductor L_g (Figure 4.26), the input impedance can be re-written as:

$$Z_{in} = \{j\omega L_2 + j\omega(1 + g_m R_i)L_s - j\frac{1}{\omega C_{gs}}\} + (\frac{g_{m1}}{C_{gs}}L_s + R_{p2} + R_g + R_i) \quad (4.32)$$

Figure 4.31 Relation of the generated L_2 , $L_{2_simplify}$ and R_{p2} , $R_{p2_simplify}$ with frequency

where R_i is the channel charging resistance [153], which is about $1/(5g_{d0})$ [128]; R_g is the sum of the intrinsic and extrinsic gate resistance. Through multi-finger layout, the typical value of R_g is $3\Omega-5\Omega$ (for a transistor width around $200\mu\text{m}$). The value of R_i

depends on g_m . It is about 2Ω – 4Ω for general operations and around 10Ω for a small-sized transistor. R_{p2} is expressed in Equation (4.31a) and is larger than R_{p1} . Figure 4.31 shows R_{p2} is around 48Ω at 2.45GHz in the proposed example. Consequently, it can be seen that $(R_{p2}+R_i+R_g)$ leads to an R_{in} of 53Ω – 57Ω , which is very close to the required 50Ω input impedance. It means that through the introduction of L_1C_1 , the unavoidable harmful parasitic resistance R_{p1} of L_1 can be utilized to generate a real term to satisfy the 50Ω input matching. As such, L_s can be reduced or removed. Usually, the original purpose of adding L_s (lossless) is to optimize input matching by introducing a 50Ω real term [23]. Now it helps to improve noise matching [154]. However, the realistic on-chip L_s is lossy. It generates thermal noise and affects noise or gain matching conditions, and it can significantly degrade LNA's gain owing to its series feedback. The removal of L_s is helpful in improving gain and more chip area can be saved. After the removal of L_s , Equation (4.32) is modified:

$$Z_{in} = \{j\omega L_2 - j\frac{1}{\omega C_{gs}}\} + (R_{p2} + R_g + R_i) \quad (4.33)$$

Figure 4.32 The final modified input architecture

The resonant frequency is changed to $\omega_{03} = 1/\sqrt{L_2 C_{gs}}$. Thus, at frequency $\omega_{03}=2.45\text{GHz}$, S_{11} is calculated to be between -31dB and -23.7dB without L_s . In practice, the required S_{11} is typically just below -10dB [74]. Hence, S_{11} , being in the range -31dB – -23.7dB, is more than enough for practical applications. It may be argued that the input resistance of $53\Omega - 57\Omega$ will contribute a lot of thermal noise to the LNA. In fact, the $48\Omega R_{p2}$ is not a physical resistance. It might not generate as much thermal noise as a 48Ω real resistor does¹². Since R_i is relative to the channel noise $\overline{i_{n,d}^2}$ and gate-induced noise $\overline{i_{n,g}^2}$ [128], only R_{p1} and R_g contribute thermal noise. Besides, R_{p1} is much smaller than the parasitic resistance of the large L_g required in a normal topology LNA. A relative low NF can still be achieved through noise optimization. The final modified input architecture is illustrated in Figure 4.32.

4.4 Summary

In this chapter, various MOSFETs noise sources are classified and modeled, including drain channel thermal noise, gate induced noise, distributed gate resistance noise and so on. A good understanding of noise sources and modeling is helpful in the accurate prediction of noise figure while doing design. Subsequently, the design of passive devices, such as on-chip spiral inductors, capacitors and resistors, are introduced and presented. Finally, a modified architecture used for input matching in CMOS LNAs is investigated. In the proposed architecture, gate and source inductors,

¹² According to the noise figure measurement results of LNA1 presented in Chapter 5, it can be estimated that the noise contributed by the $48\Omega R_{p2}$ is slightly less than that of a 48Ω real resistor, which should be $\geq 80\%$.

which are essential in the traditional source inductive degeneration CMOS LNAs, are either reduced or removed. With this input architecture, the LNA circuit can be fully-integrated and more compact. As a result, manufacture cost can be decreased. In the next chapter, the proposed input architecture will be verified by a narrow-band LNA and a wideband LNA.

Chapter 5 A Narrow-Band LNA and a Wideband LNA Using the Proposed Input Architecture

In the previous chapter, a modified architecture used for input matching in CMOS LNAs is presented. In this chapter, a narrow-band LNA and a wideband LNA are designed to include and verify the proposed idea.

5.1 Design of a Narrow-Band LNA

A basic LNA consists of a transconductance stage and an RF load. The transconductance stage translates an input voltage into an output current, while the RF load translates the current into an output voltage. The noise performance of the load translates the current into an output voltage. The noise performance of the transconductance stage affects the LNA's noise performance.

Figure 5.1 Simplified small-signal model for LNA NF calculation

5.1.1 Noise Optimization

In this section, a 2.4GHz LNA is designed based on the analysis given in Chapter 4. The previous chapters stated that in a CMOS LNA there are several main noise

sources: channel noise $\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f$, gate induced noise

$\overline{i_{n,g}^2} = 4kT\delta g_g\Delta f$ [23], thermal noise of various parasitic resistance and so on.

Figure 5.1 illustrates a simplified small-signal model for LNA NF calculation. Based on Figure 5.1, the output noise can be derived and expressed in Equations (5.1a) to (5.1f). The detailed derivation can be found in Appendix 1.

$$\overline{i_{n,o,R_S}^2} = \left| \frac{g_m R_S}{j\omega C_{gs}(R_1 + R_S) + j\omega C_{gs} D_0} \right|^2 \overline{i_{n,R_S}^2} \quad (5.1a)$$

$$\overline{i_{n,o,d}^2} = \overline{i_{n,d}^2} \quad (5.1b)$$

$$\overline{i_{n,o,R_\Delta}^2} = \left| \frac{g_m R_\Delta}{j\omega C_{gs}(R_1 + R_S) + j\omega C_{gs} D_0} \right|^2 \overline{i_{n,R_\Delta}^2} \quad (5.1c)$$

$$\overline{i_{n,o,g}^2} = \left| \frac{g_m}{j\omega C_{gs}} \left(1 - \frac{1}{j\omega C_{gs}(R_S + R_1) + j\omega C_{gs} D_0} \right) \right|^2 \overline{i_{n,g}^2} \quad (5.1d)$$

$$\overline{i_{n,o,R_{out}}^2} = \overline{i_{n,R_{out}}^2} \quad (5.1e)$$

$$\overline{i_{n,o,corr}^2} = \frac{2g_m c}{\omega C_{gs}} \left(1 - \frac{jD_0}{\omega C_{gs}((R_S + R_1)^2 + |D_0|^2)} \right) \sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} \quad (5.1f)$$

where $D_0 = j\omega L_2 + \frac{1}{j\omega C_{gs}}$ is the imaginary part of the input impedance of Figure

4.32 and equals to zero at the corresponding resonant frequency (2.45GHz in this work); R_Δ is the sum of the parasitic resistance which generates thermal noise; R_1 is the input resistance¹³; other parameters such as α , δ , γ and c can be found in [23, 40].

From the above equations, the noise factor is obtained and simplified as:

¹³ R_{p2} increases rapidly as ω approaches to $\omega_{01} = 1/\sqrt{L_1 C_1}$, leading to a large R_1 . Equation (5.2)

indicates that a large R_1 causes a large NF . Hence, we suggest that the operating frequency ought to be several hundreds MHz away from ω_{01} to maintain a roughly constant 50ohm R_1 and to avoid NF degradation in the frequency band of interest.

$$F = \frac{\overline{i_{n,o,R_S}^2} + \overline{i_{n,o,g}^2} + \overline{i_{n,o,d}^2} + \overline{i_{n,o,corr}^2} + \overline{i_{n,o,R_\Delta}^2} + \overline{i_{n,o,R_{out}}^2}}{\overline{i_{n,o,R_S}^2}} = 1 + \frac{R_\Delta}{R_S} + \frac{\delta\alpha}{5g_m R_S} \{(j\omega C_{gs} D_0 - 1)^2 + \omega^2 C_{gs}^2 (R_S + R_1)^2\} \\ + \frac{\gamma}{\alpha g_m R_S} \{(j\omega C_{gs} D_0)^2 + \omega^2 C_{gs}^2 (R_S + R_1)^2\} + \frac{2c}{g_m R_S} \sqrt{\frac{\gamma\delta}{5}} \{(j\omega C_{gs} D_0)^2 - j\omega C_{gs} D_0 + \omega^2 C_{gs}^2 (R_S + R_1)^2\} \quad (5.2)$$

Through the derivation, $g_{d0} = g_m / \alpha$ [23] is used. The noise factor at resonance frequency ω_0 ($D_0=0$ under this condition) can be achieved as well:

$$F_0 = 1 + \frac{R_\Delta}{R_S} + \left(\frac{\omega_0}{\omega_T}\right)^2 \frac{g_{d0}}{R_S} \left\{ [(R_S + R_1)^2 + \frac{1}{\omega_0^2 C_{gs}^2}] \frac{\delta\alpha^2}{5\gamma} + (R_S + R_1)^2 + 2(R_S + R_1)^2 c \sqrt{\frac{\delta\alpha^2}{5\gamma}} \right\} \quad (5.3)$$

In CMOS LNAs, the MOS transistor usually operates in the saturation region [40, 128]. When the transistor operates in the saturation region [128], the equation for the drain current is:

$$I_{ds} = \frac{W}{2\xi L_{eff}} \mu_{eff} C_{ox} (V_{GS} - V_T)^2 \quad (5.4)$$

where μ_{eff} is the carrier's effective mobility in the transistor channel and ξ is a factor which takes the short channel effect and other effect into account [24]. ξ is often set to one in the simplified MOS transistor model, but can be significantly larger in short-channel MOS transistors. Taking the derivative of Equation (5.4) with respect to V_{GS} yields:

$$g_m = \frac{W}{\xi L_{eff}} \mu_{eff} C_{ox} (V_{GS} - V_T) = \sqrt{\frac{2W}{\xi L_{eff}} \mu_{eff} C_{ox} I_{ds}} \quad (5.5)$$

Combining Equation (5.3) and Equation (5.5), F can be rewritten as a function of the transistor width. The detailed derivation can be found in Appendix 1.7.

$$F = 1 + R_\Delta / R_S + k_1 W^{-1/2} + k_2 \omega_0^2 L_{eff}^2 W^{3/2} \quad (5.6)$$

where k_1 and k_2 are equation coefficients. Both are functions of power consumption $P_d = V_{dd} I_{ds}$. Figure 5.2 illustrates the relation between NF , I_d and W in

Equation (5.6). The plot shows that the LNA has an optimum W of around $240\mu\text{m}$, which corresponds to $NF_{\min}$ when I_d is chosen.

Figure 5.2 NF versus I_d and W for $\gamma=2$, $\delta=4$, $\zeta=1.25$, $\alpha=0.8$, $\mu_{eff}=0.03\text{m}^2/\text{V}$,

$$C_{ox}=0.847\text{mF}/\text{m}^2, L_1=1.9\text{nH} (Q=7.5) \text{ and } C_1=1.4\text{pF}$$

W_{opt} can also be obtained through direct mathematic derivation. By differentiating Equation (5.6) with respect to W and equalizing it to zero, the resulting equation is:

$$W_{opt} = \sqrt{k_1 / (3k_2\omega_0^2 L_{eff}^2)} \quad (5.7)$$

5.1.2 Design of the 2.4GHz LNA (LNA1)

Generally, noise optimization is a process to find the optimum device size, so that a relative low NF can be obtained while giving consideration to the input reflection coefficient, power consumption and so on. In this design, $L_1=1.9\text{nH}$ ($Q=7.5$ at 2.45GHz), $C_1=1.4\text{pF}$, $I_d=8\text{mA}$ and $W=240\mu\text{m}$ are the configurations that are finally

chosen, giving an NF of about 2dB and an S_{11} of -22dB – -18dB¹⁴. The parasitic resistance and the terminal resistance together contribute around 1dB to the total 2dB NF . Although the NF is high compared to its counterpart using high- Q off-chip inductors, it is compact and fully-integrated.

Figure 5.3 Relation of the generated L_2 and R_{p2} with frequency ($L_1=1.9\text{nH}$, $C_1=1.4\text{pF}$, $Q=7.5$ and $\omega_{01}=3\text{GHz}$)

Once the input stage is determined, the resonant load $L_d C_d$ can be decided according to the gain and output matching requirements. Figure 5.4 presents the final schematic diagram. In this circuit, cascode transistor M_2 is used to reduce the Miller effect. It is known that the Miller effect can degrade power gain, reduce input

¹⁴ Figure 5.3 indicates that a 5.4nH inductance is obtained at 2.4GHz with a very small $L_1 C_1$. Compared to the chip area of the large L_g , the chip area of $L_1 C_1$ decreases significantly. The figure also shows that R_{p2} is around 34Ω at 2.45GHz in the proposed example. Consequently, it can be seen that $(R_{p2}+R_i+R_g)$ leads to an R_{in} of 39Ω–43Ω, which corresponds to an S_{11} of -22dB – -18dB (at resonance). It is relatively sufficient for most of current applications.

impedance and increase input referred noise [23]. Although M_2 produces noise and noise is proportional to its size, in reality the noise generated is not so significant. ΔF can be obtained by:

Figure 5.4 A 2.4GHz LNA1 based on the proposed parallel LC input architecture.

$$\Delta F = \frac{F_{M2} - 1}{A_{M1}^2} \quad (5.8a)$$

$$A_{M1} \approx - \left| \frac{g_{m1}}{j\omega C_X} \right| \quad (5.8b)$$

$$C_X = C_{gs2} + C_{dB1} + (1 + |1/A_{vM1}|)C_{gd1} \approx C_{gs2} + C_{dB1} + C_{gd1} \quad (5.8c)$$

where F_{M2} is the noise factor of M_2 , and C_x is the capacitance at node X as shown in Figure 5.4. Through calculation, it can be seen that A_{M1}^2 is normally greater than 20; hence, ΔF is very small. Generally, M_2 contributes around 0.1dB of noise, so the dimension selected for M_2 is the same as that of M_1 . This suppresses the Miller effect and enhances reverse isolation more efficiently. The derivation of Equation (5.8b) is presented in Appendix 1.8.

Figure 5.5 A 2.4GHz LNA2 with traditional source inductive degeneration input stage

5.1.3 Measurement Results

The LNA designed by applying the modified input architecture is implemented using the CSM 0.18 μ m CMOS process and tested with on-wafer RF probes. S-parameter measurements are carried out using a HP8510C network analyzer; noise figure is measured using an ATN (ATN Microwave Inc) setup. For comparison purposes, another LNA (LNA2) based on the conventional source inductive degeneration input architecture is also designed and fabricated. Its schematic is illustrated in Figure 5.5. Both LNAs have the same device sizes except L_g , L_s and C_1 of the input network. Parameters are measured under the same condition. The detailed measurement setup is illustrated in Appendix 2.

Figure 5.6 and Figure 5.7 illustrate and compare measurement results, including power gain, input reflection coefficient, output reflection coefficient, reverse isolation coefficient and noise figure. It can be seen that with the removal of L_s , LNA1 still

achieves an S_{11} of -18.5dB – -14.4dB at 2.4GHz–2.5GHz. It substantiates the feasibility of the proposed input architecture discussed in Chapter 4.

(a)

(b)

(c)

Figure 5.6 S-parameter comparisons of LNA1 and LNA2: (a) power gain; (b) S_{11} ; (c) S_{12} and S_{22} .

Figure 5.7 NF comparisons of LNA1 and LNA2.

The results also indicate that, compared to LNA2, LNA1's power gain and noise figure performance have improved. We suspect that is the result of the removal of the lossy degeneration inductor L_s and the decrease of the lossy gate inductor L_g . L_s can significantly degrade LNA's gain in a normal topology [155]. From Figure 5.6 (c), it can be seen that LNA1 has a better reverse isolation (S_{12}), compared to that of LNA2. There is a compatible output reflection coefficient because both LNAs adopt the same output structure and devices¹⁵. The better performance for S_{12} of LNA1 is achieved by the removal of the series feedback inductor L_s .

Figure 5.8 Die photos of (a) LNA1 and (b) LNA2

¹⁵ The obtained S_{22} is only around -12dB. One of the reasons is that in the resonant frequency, the load LC parallel network exhibits a high impedance, which is for a high gain purpose. Hence the output impedance is much higher than 50Ω , which leads to a poor S_{22} . In practical applications, LNA is often combined with a mixer. In this case, the LNA's load inductor and capacitor must be optimized to incorporate the input impedance (usually gate capacitance) of the mixer. When the LNA is packaged and used as a discrete component, a 50Ω output impedance source follower [73] or other type of output matching network can be adopted.

Figure 5.8 shows the corresponding die photos of LNA1 and LNA2 respectively, where port vb is the bias for the on-chip testing buffer. The detailed chip area consumption is illustrated in Table 5.1.

Table 5.1 Chip area consumption comparison of LNA1 and LNA2

	LNA1		LNA2	
	L_1	C_1	L_g	L_s
Value	1.9nH	1.4pF	6nH	1nH
Size ¹⁶	125 μ m	35 μ m	170 μ m	110 μ m
Area (mm ²)	0.0415	0.0012	0.0908	0.038
Sum (mm ²)	0.0427		0.1288	
Final Chip area (mm ²) ¹⁷	0.35 $\times$ 0.6=0.21		0.53 $\times$ 0.63=0.3339	
Saved area (%)	37		0	

Table 5.2 Measured results of recent CMOS LNAs at 2.4GHz

	[151]	[156]	[157]	LNA1	LNA2
Vdd (V)	1.8	1.8	N.A.	1.5	1.5
Current (mA)	8	4.23	11.4	10	10
Operating Band (GHz)	2.4	2.4	2.4	2.4	2.4
Gain (dB)	7.5	7	14.7	24 – 25	19 – 20.5
S_{11} (dB)	-12 – -8	N.A.	<-7	-18.5 – -14.4	-17.2 – -14.5
S_{22} (dB)	-19	N.A.	<-25	-12 – -11	-11
S_{12} (dB)	N.A.	N.A.	<-10	-31 – -27.5	-25 – -22
NF (dB)	4.5	3	2.88	2.62 – 2.8	2.8 – 2.95
Chip Area (mm ²)	N.A.	0.79	N.A.	0.21	0.334
CMOS	0.18	0.18	0.25	0.18	0.18
Process (μ m)					

Other performance specs of LNA1 and LNA2 are shown in Table 5.2. The table also summarizes the comparisons of several recent LNAs used for Bluetooth

¹⁶ The size of the inductors is the radius including the 50 μ m space outside, which is to reduce the mutual coupling between inductors and other devices nearby, so as to guarantee its quality [149].

¹⁷ It is the effective chip area without the pad region. With Padding, the chip area is 0.4mm² and 0.56mm² respectively.

applications. The two tables indicate that, with the proposed input topology, LNA1 consumes less chip area while keeping an equivalent or better performance compared to other fully-integrated 2.4GHz LNA designs. The test results verify the strength of the proposed input architecture.

Figure 5.9 A wideband LNA (LNA3)

5.2 Design of a Wideband LNA (LNA3)

5.2.1 Topology of the Wideband LNA

In addition to the narrow-band LNA presented in Section 5.1, a wideband LNA (5.1GHz–5.9GHz) used for IEEE802.11a and HiperLAN applications will be presented in this section for verification purposes. The wideband LNA also adopts the proposed input architecture. Its schematic diagram is shown in Figure 5.9. It is a two-stage amplifier with an additional buffer for output matching and testing purposes, whereby the first and second stages are designed to resonate at 5.3GHz and 5.8GHz

respectively. This stagger tuning technique is used to yield a flat and broad bandwidth.

The input stage is designed for impedance matching at 5.5GHz, which is the mid-frequency of the passband. The L_1C_1 parallel network is set to 1nH and 0.5pF relative to the $\omega_{01} = 1/\sqrt{L_1C_1}$ around 7GHz. The corresponding R_{p1} is around 4 Ω at 5.5GHz [149]. According to Equations (4.31a) and (4.31b), L_1C_1 generates an inductance of around 3nH and a series resistance R_{p2} of around 27 Ω . Incorporating the 3 Ω –5 Ω gate resistance R_g and 2 Ω –4 Ω R_i , the input resistance is about 32 Ω –36 Ω at the middle resonant frequency 5.5GHz, which corresponds to an input reflection coefficient of -16dB – -13dB. Through noise optimization, the optimum transistor width is 120 μ m. The 120 μ m NMOSFET has a gate resistance of 5.7 Ω , which is larger than R_g of the 240 μ m NMOSFET used in LNA1. Thus, the estimated S_{11} at 5.5GHz is changed to -16.3dB – -15dB.

Figure 5.10 The layout of the wideband LNA

To prevent degrading the overall linearity of the LNA, a transistor width of $150\mu\text{m}$ and a gate bias voltage of 0.6V are chosen for the second stage. To achieve a higher power gain, parallel LC tanks are used as loads for the first and second stages, where the impedance is the maximum at the frequency of 5.3GHz and 5.8GHz respectively. Besides that, using LC tanks instead of resistors, the LNA can have improved noise performance and more voltage headroom under the 1.5V voltage supply. This configuration helps to reject the out-of-band signals and noise at the output as well.

Figure 5.11 Simulation and post-simulation S_{21}

5.2.2 Post-Layout Simulation Results

The proposed circuit is designed and prepared for fabrication based on the CSM $0.18\mu\text{m}$ CMOS technology. Its layout is shown in Figure 5.10. A post-layout simulation with extracted parasitics is carried out using the Cadence SpectreRF simulator.

Figure 5.11 illustrates the simulation and post-simulation S_{21} . Practically, due to the parasitics of the layout, especially the parasitic capacitance, the operating band (S_{21_post1}) will shift to the lower frequency. In this case, the operating band shifts by 300MHz to the lower frequency and the gain degrades by 2.5dB. The layout was then modified. The two capacitors C_{d1} and C_{d2} of the two resonant loads are reduced from 600f to 500f and 360f to 340f respectively. The final post simulation result is shown as S_{21_post2} . Frequency shift to the lower frequency still exists. However, S_{21} degrades only around 1dB. Table 5.3 presents the detailed outcome data under the above-mentioned three conditions.

Table 5.3 Comparisons of the simulated and post-simulated S_{21} and noise figure

	S_{21} (dB)		BW _{-3dB} (GHz)	NF (dB)	
	5.1GHz	5.9GHz		5.1GHz	5.9GHz
Simulation	24.95	24.27	4.8-6.2	2.87	3.62
Post_simulation1	22.4	20.81	4.4-6.0	3.1	3.7
Post_simulation2	24.61	22.58	4.6-6.0	2.85	3.53

Other post-simulation results are illustrated in Figure 5.12. The results indicate that the LNA has an in-band S_{11} of approximately -17.5dB – -10dB and a flat gain of approximately 24dB. The reverse isolation between the input and the output is below -87dB (Figure 5.12(b)). It will help to reduce the LO leakage substantially, which arises from the capacitive paths and substrate coupling. The LNA has a noise figure of 2.85dB–3.5dB within the 800MHz bandwidth. Most of the noise comes from parasitic resistance as well as the parasitic capacitance and inductance. They affect the noise transfer function and matching condition. Two-tone signals with equal power levels at 5.5GHz and 5.52GHz are applied to the LNA. Both tones are swept from -30dBm to

10dBm to observe the first-order and third-order gain compression behavior. Figure 5.12(d) shows a -5.4dBm IIP3 (+19dBm OIP3), which has a relatively good linearity. LNA3 obtains an in-band S_{22} of -15dB – -11dB. In the condition that a lower S_{22} is required, a 50 Ω output impedance source follower can be incorporated [73].

(a)

(b)

(c)

(d)

Figure 5.12 Post-simulation results of the proposed wideband LNA: (a) S_{11} and S_{21} ; (b) S_{12} and S_{22} ; (c) noise figure; (d) the third-order intercept point

Comparison of results with other 5GHz LNAs in recent researches [50, 104, 158-160] is illustrated in Table 5.4. The table indicates the non- L_s wideband LNA has comparable performance - flat and high gain and small chip area. This proves the

feasibility of the proposed input architecture. With proper design, the bandwidth of the proposed design can be realized up to 1GHz.

Table 5.4 Comparisons of recent 5GHz CMOS LNAs

	LNA3	[104]	[158]	[159]	[160]	[50]
Frequency (GHz)	5.1–5.9	5	5.8	5.25	5–6	5.1
CMOS Process (μm)	0.18	0.18	0.18	0.25	0.24	0.25
Vdd (V)	1.5	1	1	3	2	2
Gain (dB)	22.6–24.6	10.8	13.2	14	8	18(A_v)
S_{11} (dB)	-17.5 – -9.5	-26	-5.3	-12.3	-23.5	-12
S_{22} (dB)	-15 – -11	N/A	-10.3	-11.9	N/A	N/A
S_{12} (dB)	-90 – -87	N/A	N/A	-26.4	-30	N/A
NF (dB)	2.85–3.5	2.9	2.5	2.5	4.8	4.8
IIP3 (dBm)	-5.4	N/A	N/A	-1.5	10	N/A
Power (mW)	10	14.2	22.2	48	10	7.2
Chip area (mm^2)	0.56	0.9	>1	N.A	N.A	N.A

5.3 Summary

The rapidly developing market calls for low-cost and fully-integrated chips. For current RFIC designs, inductors are widely used. However, on-chip inductors are usually lossy and occupy a large chip area. This will definitely affect system performance and product cost. In this chapter, the inevitable parasitic resistance on the on-chip inductor is utilized to enhance input matching through a parallel LC network in CMOS LNAs. The parallel LC network is also used to replace the large gate inductor, which is normally required for normal input architecture LNA. A narrow-band CMOS LNA and a wideband CMOS LNA are designed based on the proposed idea. The results show that, using the modified input architecture, both

LNAs still achieve acceptable input reflection coefficients and present very good gain performance at relatively low power consumption.

For comparison purposes, a narrow-band LNA2 using the traditional source inductive degeneration architecture is also designed and fabricated. The comparison of LNA1 with LNA2 indicates that with the modified input-architecture, L_g is greatly reduced and L_s is removed. Up to 37 percent of the chip area is saved. Therefore, the manufacturing cost is reduced.

In brief, the work presented in this chapter shows that, with the proposed input architecture, the current CMOS LNA can be integrated more easily and compactly. It provides an insight for decreasing manufacturing cost and increasing system integration.

Chapter 6 Two Dual-Band Low Noise Amplifiers

As described in the previous chapters, the telecommunication industry has experienced an immense growth in the past two decades. Home RF network and wireless local area network (WLAN) communications are becoming more and more popular. Figure 6.1 illustrates a communication application example based on the WLAN and Bluetooth standards. LNA is one of the most important building blocks in the multi-standard/multi-band operation communication system. In this chapter, the designs of two dual-band low noise amplifiers (LNA4 and LNA5) for Bluetooth and HiperLAN/WLAN applications are investigated. In the last section, stability and input matching considerations in LNA designs are highlighted.

Figure 6.1 One communication application example based on WLAN and Bluetooth standards

6.1 Design of a Dual-Band LNA (LNA4)

6.1.1 Input Matching Analysis

The 50Ω input matching is one of the considerations in LNA design. As introduced in Chapter 3, there are currently four input architectures in LNA designs:

common source with resistive termination, common gate ($1/g_m$) termination, common gate with shunt-series feedback topology and source inductive degeneration topology. Of the above four architectures, the fourth (as shown in Figure 6.2(a)) is the most widely adopted due to its easiness to achieve the required input matching. Its input impedance is:

$$Z_{in} \approx j\left\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\right\} + (g_{m1} / C_{gs})L_s \quad (6.1)$$

Figure 6.2 (a) A typical single-band LNA using source inductive degeneration input topology; (b) source inductive degeneration topology with variable L_g

As mentioned in the previous chapters, to arrive at optimum input matching, the real part of Equation (6.1) should be 50Ω , whereas the imaginary part should be zero at the required operating frequency $\omega_0 = 1/\sqrt{(L_g + L_s)C_{gs}}$. This is the rule for input matching design for single-band LNAs.

For the dual-band LNA, a similar topology can be adopted. To meet the requirement of the imaginary part to be zero at two different frequencies ω_{01} and ω_{02}

simultaneously, the gate inductor L_g is expected to present different values L_{g1} and L_{g2} at the two corresponding operating frequency points. L_{g1} and L_{g2} should also satisfy:

$$\omega_{01}(L_{g1} + L_s) - 1/(\omega_{01}C_{gs}) = 0 \quad (6.2a)$$

$$\omega_{02}(L_{g2} + L_s) - 1/(\omega_{02}C_{gs}) = 0 \quad (6.2b)$$

It can be seen from Equations (6.2a) and (6.2b), that for a fixed transistor width W (corresponding to a fixed $C_{gs} \approx 2WLC_{ox}/3$ operating in the saturation region [40, 128]), the required L_{g2} is smaller than L_{g1} under the condition $\omega_{02} > \omega_{01}$. It is described in the following example. A CSM 240 μ m NMOS transistor has a transconductance g_m of around 0.071S and C_{gs} of around 0.23pF at 0.62V bias [149]. In practice, the Miller effect will generate additional capacitance C_M in parallel with C_{gs} :

$$C_M = (1 + |A_v|)C_{gd} \quad (6.3)$$

where A_v is the voltage gain seen from the drain to the gate. In the current 0.18 μ m CMOS technology, $C_M \approx C_{gs}$ [153]. Taking the Miller effect into account, C_{gs} in Equations (6.1), (6.2a) and (6.3b) is adjusted to approximately $2C_{gs}$. After calculation, $L_s=0.32$ nH, $L_{g1}=8.85$ nH ($\omega_{01}=2.45$ GHz) and $L_{g2}=1.43$ nH ($\omega_{02}=5.6$ GHz).

It is difficult to implement an inductor that has two proper values such as 8.85nH and 1.43nH corresponding to ω_{01} and ω_{02} respectively. The required inductor can be implemented using a specific circuit block: a relatively constant inductor L_A in series with a network. The network should present a positive inductance $+L_{\Delta1}$ at ω_{01} and a negative inductance $-L_{\Delta2}$ at ω_{02} . $(L_A + L_{\Delta1})$ and $(L_A - L_{\Delta2})$ are expected to be equal to L_{g1} and L_{g2} respectively, as $L_{g1} > L_{g2}$.

Recall the parallel LC network discussed in Section 4.3.2. Its impedance is:

$$Z = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} = j\omega \left(\frac{L_1}{1 - \omega^2 L_1 C_1} \right) = j\omega \frac{L_1}{1 - (\omega / \omega_p)^2} \quad (6.4)$$

where $\omega_p = 1/\sqrt{L_1 C_1}$ is the resonant frequency of the $L_1 C_1$ parallel network.

Equation (6.4) indicates that the $L_1 C_1$ network has an inductive attribute with the inductance of:

$$L_2 = \frac{L_1}{1 - \omega^2 L_1 C_1} = \frac{L_1}{1 - (\omega / \omega_p)^2} \quad (6.5)$$

L_2 is a function of the frequency. From Equation (6.5), the inductance value is positive (inductive) when $\omega < \omega_p$ and negative (capacitive) when $\omega > \omega_p$. Consequently, the parallel $L_1 C_1$ network can be considered as a variable inductor (Figure 6.3). The behavior of the parallel network is illustrated in Figure 6.4 where $L_1 = 2.81\text{nH}$ and $C_1 = 0.563\text{pF}$ ($\omega_p = 4\text{GHz}$). The figure shows that L_2 is about 4.5nH ($L_{\Delta 1}$) at 2.45GHz and -2.93nH ($-L_{\Delta 2}$) at 5.6GHz . Thus, $L_1 C_1$, in series with a real inductor L_A having relatively constant value of around 4.36nH (Figure 6.5), can be used to realize the dual-band input matching variable inductor¹⁸.

Figure 6.3 An LC parallel network and its equivalent circuit

¹⁸ A similar input network has been adopted for a concurrent dual-band LNA by Hossein [66] in 2002, but with very different analysis. According to his analysis, the LC parallel network is used to generate a zero-dB S_{11} point, so as to split the single-band S_{11} curve into two parts. In his design, the gate network components are all off-chip. It is not suitable for full-integration.

Figure 6.4 The behavior of the proposed L_1C_1 parallel network with frequency

Figure 6.5 The variable inductor required in a dual-band LNA

Figure 6.6 (a) LC parallel network and its equivalent circuit with parasitic resistance;

(b) equivalent circuit of the variable-inductance network

As introduced in Chapter 4, current on-chip inductors used in LNA designs are not ideal, and their quality factors (Q_s) are too limited. The parasitic resistance of the lossy on-chip inductors should be taken into account, as illustrated in Figure 6.6 (a).

The impedance is expressed as:

$$Z = R_{p2} + j\omega L_2 \quad (6.6)$$

$$R_{p2} = \frac{R_{p1}}{(1 - \omega^2 L_1 C_1)^2 + (\omega C_1 R_{p1})^2} \approx \frac{R_{p1}}{(1 - \omega^2 L_1 C_1)^2} = \frac{R_{p1}}{(1 - (\omega / \omega_p)^2)^2} \quad (6.6a)$$

$$L_2 = \frac{L_1 - \omega^2 L_1^2 C_1 - C_1 R_{p1}^2}{(1 - \omega^2 L_1 C_1)^2 + (\omega C_1 R_{p1})^2} \approx \frac{L_1 - \omega^2 L_1^2 C_1 - C_1 R_{p1}^2}{(1 - \omega^2 L_1 C_1)^2} \approx \frac{L_1}{1 - (\omega / \omega_p)^2} \quad (6.6b)$$

$$\omega_p = 1 / \sqrt{L_1 C_1} \quad (6.6c)$$

The network shown in Figure 6.5(a) should be modified as well (Figure 6.6 (b)).

Consequently, the input impedance of the dual-band LNA can be rewritten as:

$$Z_{in} = \{j\omega L_g(f) + j\omega(1 + g_m R_i)L_s - j\frac{1 + R_{Ls}}{\omega C_{gs}}\} + (\frac{g_{m1}}{C_{gs}}L_s + R_g + R_i + R_{Ls} + R_{pg}) \quad (6.7)$$

$$L_g(f) = L_A + L_2(f) \quad (6.7a)$$

$$R_{pg} = R_{pA} + R_{p2} \quad (6.7b)$$

where R_i is the channel charging resistance [128], which is about $1/(5g_{d0})$ [128]; R_g includes the intrinsic and extrinsic gate resistance, while R_{Ls} is the parasitic resistance of L_s . As presented in the previous chapters, through multi-finger layout, the typical value of R_g is 3Ω – 5Ω (for a transistor width of around $200\mu\text{m}$). The value of R_i depends on g_m . It is about 2Ω – 4Ω for general operations and about 10Ω for a small-sized transistor. R_{pA} is around 9.6Ω at 2.45GHz and 22Ω at 5.6GHz ($Q=7$). R_{p2} can be calculated according to Equation (6.6a). Figure 6.4(b) indicates that it is around 15Ω and 13Ω for the 2.81nH ($Q=7.5$), 0.563pF L_1C_1 network at 2.45GHz and 5.6GHz respectively. Subsequently, it can be seen $R_{pA} + R_{p2} + R_g + R_i$ leads to an R_{in} of 29.6Ω – 33.6Ω at 2.45GHz (S_{11} of -11.7dB – -14.1dB), and 40Ω – 44Ω at 5.6GHz (-19dB – -23.9dB). The impedance is close to the required 50Ω input impedance. Therefore, through the introduction of L_1C_1 , the source degeneration inductor L_s can be removed too. As a result, more chip area can be saved, and an improved gain can be also obtained. After the removal of L_s , Equation (6.7) is modified:

$$Z_{in} = j\omega\{L_A + L_2(f) - \frac{1}{\omega C_{gs}}\} + (R_g + R_i + R_{pA} + R_{p2}) \quad (6.8)$$

Without L_s , it can be calculated that S_{11} is -11.7dB – -14.1dB and -19dB – -23.9dB at 2.45GHz and 5.6GHz respectively. In practice, the proposed input

reflection coefficient is sufficient for most of applications [74]. There is another dual-band LNA input matching architecture in [161], shown in Figure 6.7 (b).

Figure 6.7 (a) The proposed input architecture in our work; (b) a dual-band input matching architecture [161]

The impedance of the network shown in Figures 6.7 (a) and (b) can thus be derived and compared:

$$Z_1 = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} + j\omega L_A = j\omega \left(\frac{L_1}{1 - \omega^2 L_1 C_1} + L_A \right) \quad (6.9a)$$

$$Z_2 = j\omega \frac{L_2(1 - \omega^2 L_1 C_1)}{1 - \omega^2 (L_1 + L_2) C_1} = j\omega \left(\frac{\omega^2 L_2^2 C_1}{1 - \omega^2 (L_1 + L_2) C_1} + L_2 \right) \quad (6.9b)$$

The two equations indicate that Equation (6.9b) is more complicated than Equation (6.9a). Some items of Equation (6.9b) are in the form of product or sum of two or more parameters. It might cause an even larger deviation from the optimized matching condition if there is a small deviation in the inductor value L_2 through the fabrication process. Therefore, S_{11} matching condition is more sensitive to the accuracy of the fabricated L_1 , L_2 and C_1 . The result is that the measured matching

outcome is most likely to be different from the simulation results¹⁹. Besides that, the NF matching condition is more likely to be affected as well.

Figure 6.8 Simplified small-signal model for LNA NF calculation

6.1.2 Design of the Dual-Band LNA (LNA4)

A. Noise Figure Optimization

In this section, an LNA operating at 2.4GHz and 5.6GHz is designed based on the analyses in the previous section. Firstly, noise optimization is conducted. A simplified small-signal model for the LNA's NF calculation is then illustrated in Figure 6.8. Similar to the method in Section 5.1.1, the noise factor F can be finally derived as:

$$F = \frac{\overline{i_{n,o,R_s}^2} + \overline{i_{n,o,g}^2} + \overline{i_{n,o,d}^2} + \overline{i_{n,o,corr}^2} + \overline{i_{n,o,R_\Delta}^2} + \overline{i_{n,o,R_{out}}^2}}{\overline{i_{n,o,R_s}^2}} = 1 + \frac{R_\Delta}{R_s} + \frac{\delta\alpha}{5g_m R_s} \{ (j\omega C_{gs} D_0 - 1)^2 + \omega^2 C_{gs}^2 (R_s + R_1)^2 \} \\ + \frac{\gamma}{\alpha g_m R_s} \{ (j\omega C_{gs} D_0)^2 + \omega^2 C_{gs}^2 (R_s + R_1)^2 \} + \frac{2c}{g_m R_s} \sqrt{\frac{\gamma\delta}{5}} \{ (j\omega C_{gs} D_0)^2 - j\omega C_{gs} D_0 + \omega^2 C_{gs}^2 (R_s + R_1)^2 \} \quad (6.10)$$

¹⁹ In fact, there is a matching deviation around 800MHz for the second frequency band between the simulation results and the measurement results [161].

where $D_0 = j\omega\{L_A + L_2(f) - \frac{1}{\omega C_{gs}}\}$ is the imaginary part of the input impedance (see Equation (6.7)), and D_0 equals zero at the two corresponding resonant frequencies ($\omega_{01}=2.45\text{GHz}$ and $\omega_{02}=5.6\text{ GHz}$, which are the centre points of the two operating frequency bands respectively in this design). When $D_0=0$, the noise factor can be expressed as:

$$F_0 = 1 + \frac{R_\Delta}{R_S} + \left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\mathcal{G}_{d0}}{R_S} \left\{ [(R_S + R_1)^2 + \frac{1}{\omega_0^2 C_{gs}^2}] \frac{\delta \alpha^2}{5\gamma} + (R_S + R_1)^2 + 2(R_S + R_1)^2 c \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right\} \quad (6.11)$$

where R_Δ is the sum of the parasitic resistance which generates thermal noise; R_1 is the input resistance. Similar to the derivation in Section 5.1.1, F can also be rewritten as a function of the transistor width:

$$F = 1 + R_\Delta / R_S + k_1 W^{-1/2} + k_2 \omega_0^2 L_{eff}^2 W^{3/2} \quad (6.12)$$

Figure 6.9 NF versus I_d and W for $\gamma=2$, $\delta=4$, $\zeta=1.25$, $\alpha=0.8$, $\mu_{eff}=0.03\text{m}^2/\text{V}$,

$C_{ox}=0.847\text{mF}/\text{m}^2$ (a) first band; (b) second band

Figure 6.9 illustrates the relation between NF , I_d and W in Equation (6.12) for 2.45GHz and 5.6GHz respectively. For a fixed P_d , there is an optimum W_{opt} corresponding to a minimum noise figure. For example, for a current consumption of

10 mA, there is an $NF_{\min1}$ of around 2.3dB corresponding to W_{opt1} of around 230 μ m at 2.45GHz. However, as the LNA has to operate at two different frequency bands, there exists another W_{opt2} of around 180 μ m relative to the minimum noise figure at 5.6GHz. Therefore, a tradeoff between W_{opt1} and W_{opt2} has to be made. A transistor width of 200 μ m is finally chosen after considering various factors, such as the gain and NF as well as the circuit stability.

B. Design of the Dual-Band LNA (LNA4)

Once the input stage is determined, the resonant load $L_d C_d$ can be obtained according to the gain and output matching requirements. Figure 6.10 (a) presents the final schematic diagram. In this circuit, cascode transistor M_2 is also used to reduce Miller effect. For the single-band LNA, the drain load network is generally composed of one LC parallel network, which exhibits high impedance (at resonance) at the required operating frequency so as to achieve a high gain. For the dual-band LNA, a series LC network is inserted into the drain load network. For the load network shown in Figure 6.10 (a), its impedance can be expressed as:

$$\begin{aligned} Z_d &= j\omega L_d \frac{1 - \omega^2 L_{d2} C_{d2}}{(1 - \omega^2 L_d C_d)(1 - \omega^2 L_{d2} C_{d2}) - \omega^2 L_d C_{d2}} \\ &= j\omega L_d \frac{1 - \omega^2 L_{d2} C_{d2}}{\omega^4 L_d L_{d2} C_d C_{d2} - \omega^2 (L_{d2} C_{d2} + L_d C_d + L_d C_{d2}) + 1} \end{aligned} \quad (6.13)$$

Equation (6.13) has a zero point at $\omega_0 = 1/\sqrt{L_{d2} C_{d2}}$, which is the resonance frequency of the series $L_{d2} C_{d2}$ network. At this point, the load impedance is zero. Therefore, the LNA has the lowest gain at this point. Equation (6.13) also indicates that there are two poles ω_{p1} and ω_{p2} , where the drain load network exhibits high

impedance. At these two poles, the LNA also exhibits high gain. For the dual-band LNA in our design, the poles ω_{p1} and ω_{p2} can be set to 2.45GHz and 5.6GHz respectively through calculation of the drain load network. Thereafter, high gain at the two operating frequency bands can be achieved. By placing the zero point $\omega_0 = 1/\sqrt{L_{d2}C_{d2}}$ in the middle of ω_{p1} and ω_{p2} , a notch in the gain transfer function curve can be created so as to filter out the out-of-band signals. This dual-band loading network is only suitable to be used when the second band is more than 1GHz away from the first operating band. Otherwise, the introduction of the series $L_{d2}C_{d2}$ network can greatly degrade the gain of both operating bands.

Figure 6.10 Dual-band LNA: (a) simplified schematic diagram; (b) layout (0.78mm × 0.77mm=0.6 mm² with pads; 0.5mm × 0.6mm=0.3mm² without pads)

6.1.3 Post-Layout Simulation Results of LNA4

The proposed circuit is designed and prepared for fabrication based on the CSM 0.18μm CMOS technology. Its layout is shown in Figure 6.10(b). A post-layout

simulation with extracted parasitics is carried out using the Cadence SpectreRF simulator.

Figure 6.11 Simulation and post-simulation voltage gain and S_{11}

Table 6.1 The final post-simulation S_{21} and noise figure

Voltage Gain (dB)		BW1 _{-3dB} (GHz)	BW2 _{-3dB} (GHz)	NF (dB)	
1 st Band 2.4-2.5GHz	2 nd Band 5.47-5.825GHz			1 st Band 2.4-2.5GHz	2 nd Band 5.47-5.825GHz
17.59-18.79	16.62-15.59	2.32-2.8	5.26-6	2.26-2.41	3.27-3.25

Figure 6.11 illustrates the simulated and post-simulated voltage gain and S_{11} . In practice, the realistic operating band will shift to the lower frequency due to the parasitics of the layout, especially parasitic capacitance. Thus the two operation bands are initially designed at 2.7GHz and 5.8GHz instead of 2.45GHz and 5.6GHz in order to compensate the layout parasitics. Referring to Figure 6.11, the first band shifts from 2.7GHz to 2.6GHz (100MHz), and the second band shifts from 5.84GHz to 5.6GHz (240MHz). The same case also happens for the input reflection coefficient

S_{11} . Detailed data are presented in Table 6.1, Figure 6.12 and Figure 6.13.

Figure 6.12 Post-simulation of S_{12} and S_{22}

(a)

(b)

(c)

(d)

Figure 6.13 The post-simulation results of the proposed dual-band LNA: (a) NF of 1st band; (b) NF of 2nd band; (c) IP_3 of 1st band; (d) IP_3 of 2nd band

The results indicate that the LNA has an in-band S_{11} of approximately -12dB – -15dB for the first frequency band and -13dB – -16dB for the second frequency band. The reverse isolation S_{12} between the input and the output is below -43dB as shown in Figure 6.12. A low S_{12} helps to reduce the LO leakage substantially. The noise figure of the dual-band LNA4 is 2.26dB – 2.41dB and 3.3dB for the first band and second band respectively. Two-tone signals, with equal power levels (2.4GHz and 2.42GHz for the 2.4GHz band; 5.6GHz and 5.62GHz for the 5GHz band) are applied to the LNA. Both tones are swept from -30dBm to 10dBm to observe the first-order and third-order gain compression behavior. Figures 6.13 (c) and (d) show a -2.5dBm IIP_3 and a -0.15dBm IIP_3 for the two corresponding frequency bands, respectively.

Figure 6.14 Comparisons of voltage gain and NF for the dual-band LNA with and without L_s : (a) voltage gain comparison; (b) noise figure comparison

In our design, the traditional source inductive degeneration inductor L_s is removed in order to save chip area and enhance gain performance. In this case, if an inductor L_s with 0.45nH inductance is added, the S_{11} performance can improve a little. However, the voltage gain degrades more. Figure 6.14 compares the voltage gain and

NF performance for the dual-band LNA with L_s and without L_s . The results show that with the introduction of L_s , the gain is significantly degraded, mainly due to its series feedback. As the on-chip L_s is not an ideal inductor, its parasitic resistance contributes noise to the LNA (Figure 6.14 (b)). Accordingly, the removal of L_s is helpful in improving the gain. Besides that, more chip area can be saved.

The chip area of the proposed dual-band LNA (LNA4) is $0.78\text{mm} \times 0.77\text{mm} = 0.6\text{ mm}^2$ with pads and $0.5\text{mm} \times 0.6\text{mm} = 0.3\text{mm}^2$ without pads. The chip area is relatively small. The LNA draws 10.25mA current from a 1.5V voltage supply. In general, with the proposed variable inductor network and the removal of the traditional source inductive degeneration inductor L_s , the fully-integrated dual-band LNA4 optimizes input matching and achieves good gain and linearity performance, while at the same time, consumes only a small chip area.

6.2 Design of another Dual-Band LNA (LNA5)

In the previous section, the dual-band LNA input matching topology as well as a single stage dual-band LNA (LNA4) is presented. In this section, another dual-band LNA (LNA5) is investigated. The measurement results will also be presented.

6.2.1 Input Matching

In the case of inductor L_A (Figure 6.10 (a)) which is also large in value (when transistor M1 is small), a capacitor C_p can also be introduced in parallel with L_A in order to reduce L_A . The relevant analysis can be found in Chapter 4. The final modified dual-band input matching architecture is illustrated in Figure 6.15 (a).

Figure 6.15 (b) illustrates the effect of the input matching performance under the condition with and without C_p . The result indicates that the LC parallel network acts like a high- Q inductor.

Figure 6.15 (a) Modified dual-band input matching ; (b) comparison of $S_{11}@$ with and without C_p

6.2.2 Noise Optimization

Similar to the noise analysis method presented in Section 5.11 and Section 6.12, the noise factor F can be presented as:

$$F = \frac{\overline{i_{n,o,R_S}^2} + \overline{i_{n,o,g}^2} + \overline{i_{n,o,d}^2} + \overline{i_{n,o,corr}^2} + \overline{i_{n,o,R_A}^2} + \overline{i_{n,o,R_{out}}^2}}{\overline{i_{n,o,R_S}^2}} \approx 1 + \frac{R_A}{R_S} + \frac{\delta\alpha}{5g_m R_S} \{ (j\omega C_{gs} D_0 - 1)^2 + \omega^2 C_{gs}^2 (R_S + R_1)^2 \} \\ + \frac{\gamma}{\alpha g_m R_S} \{ (j\omega C_{gs} D_0)^2 + \omega^2 C_{gs}^2 (R_S + R_1)^2 \} + \frac{2c}{g_m R_S} \sqrt{\frac{\gamma\delta}{5}} \{ (j\omega C_{gs} D_0)^2 - j\omega C_{gs} D_0 + \omega^2 C_{gs}^2 (R_S + R_1)^2 \} \quad (6.14)$$

where D_0 changes to $D_0 = j\omega L_S + \frac{j\omega L_A}{1 - \omega^2 L_A C_p} + \frac{1}{j\omega C_{gs}} + \frac{j\omega L_1}{1 - \omega^2 L_1 C_1}$, which is the imaginary part of the input impedance and is equivalent to zero at the two corresponding resonant frequencies ($\omega_{01}=2.45\text{GHz}$ and $\omega_{02}=5.5\text{GHz}$, which are the centre points of the two operating frequency bands respectively in LNA5). A rough

determination procedure of the L and C parameters in Equation (6.14) is presented in Appendix 1.9.

By combining Equations (5.5), (6.14) with $C_{gs} \approx \frac{2}{3}WLC_{ox}$ and other parameters, the relationship of NF versus frequency can be plotted, as shown in Figure 6.16. The figure indicates that there are two frequency points which correspond to two minimum noise figures. Through noise optimization, the two minimum noise figure points should shift to the two operation frequency bands of interest.

Figure 6.16 NF versus frequency for $W/L=240\mu\text{m}/0.18\mu\text{m}$, $\gamma=2$, $\delta=2.5$, $\zeta=1.6$, $\alpha=0.8$, $\mu_{\text{eff}}=0.035\text{m}^2/\text{V}$, $C_{ox}=0.008\text{F}/\text{m}^2$ and $I_{ds}=8\text{mA}$

In practice, we are more interested in the NF at the resonant frequencies like 2.45GHz and 5.5GHz, where $D_0=0$. According to the expressions of g_m and C_{gs} , Equation (6.14) can be rewritten as:

$$F = 1 + R_{\Delta} / R_S + k_1 W^{-1/2} + k_2 \omega_0^2 L_{\text{eff}}^2 W^{3/2} \quad (6.15)$$

where k_1 and k_2 are equation coefficients. Based on Equation (6.15), a plot of NF versus transistor width W at 2.45GHz and 5.5GHz respectively is shown in Figure

6.17. Equation (6.15) contains terms which are constant, proportional to $W^{3/2}$ and inversely proportional to $W^{1/2}$. It indicates that there must exist an optimum transistor width W_{opt} corresponding to the minimum noise factor. Differentiating Equation (6.15) with respect to W and equalizing it to zero yields:

$$W_{opt} = \sqrt{\frac{k_1}{3k_2\omega_0^2 L_{eff}^2}} \quad (6.16)$$

Figure 6.17 NF versus W for $\gamma=2$, $\delta=2.5$, $\zeta=1.6$, $\alpha=0.8$, $\mu_{eff}=0.035\text{m}^2/\text{V}$,

$$C_{ox}=0.008\text{F}/\text{m}^2 \text{ and } I_{ds}=8\text{mA}$$

Figure 6.18 W_{opt} versus I_{ds} and f_0

Figure 6.19 NF for different W

Equation (6.16) has the same form as Equation (5.7). According to Equation (6.16), W_{opt} can be calculated. Figure 6.18 shows the variation of W_{opt} with respect to I_{ds} and f_0 . For a fixed current $I_{ds}=8\text{mA}$, Equation (6.16) generates two W_{opt} values of $W_{opt1}=240\mu\text{m}$ and $W_{opt2}=100\mu\text{m}$, corresponding to $f_{01}=2.45\text{GHz}$ and $f_{02}=5.5\text{GHz}$ respectively. A compromise between W_{opt1} and W_{opt2} has to be reached too. A transistor width of $200\mu\text{m}$ is finally decided in our design.

Figure 6.19 compares the NF for different W : $240\mu\text{m}$, $100\mu\text{m}$ and $200\mu\text{m}$. Following the above procedure and plots, the LNA can be optimized further according to different design requirements.

Figure 6.20 Simplified schematic of the proposed dual-band LNA5

6.2.3 LNA (LNA5) Implementation and Measurement Results

Based on the above analyses, a concurrent dual-band LNA is designed and fabricated. Figure 6.20 shows the simplified schematic diagram. It is a two-stage amplifier with an additional buffer stage for output matching and testing purposes. In

the circuit, a cascode structure is used to reduce the influence of the gate-to-drain overlap capacitance C_{gd} on the LNA's input impedance and to improve the LNA's reverse isolation in order to prevent the LO leakage from the subsequent mixer back to the LNA's RF input. Proper adjustment of the parameters of the passive and active components of the schematic enables the LNA work at two different frequency bands at the same time, which is meaningful for the development of multi-standard operation devices.

In this design, great efforts have been made to shape the passbands of the LNA. The inductors L_{d1} and L_{d2} are designed to resonate at two different frequencies (2.45GHz and 5.5GHz in this work). The proper selection of inductors and biasing voltage can determine the main frame of the gain transfer function curve. The objective of introducing the feedback capacitor C_f , connected between the first stage and the second stage, is for the extension and flattening of bandwidth. C_f can not be too large²⁰. Otherwise, the circuits might resonate. It is around 100f in our design.

From Section 3.3.2, it is known that for an LC parallel network, when the inductor L and capacitor C are designed to resonate at a selected frequency

²⁰ Through simulation, it is found that the introduction of C_f can degrade the peak of the second band gain, which flats the second band as a result. It might come from two mechanisms. Firstly, feedback is often used to extend the bandwidth [88, 91-92]. Secondly, C_f is connected in parallel with C_{gd2} through the path of M2 (with channel resistance R_{ch2}) and the large C_B . Figure 6.21 (a) illustrates the simplified schematic. This R - C shunt feedback technique is often adopted in broadband power amplifier designs for band extension and flatness purpose [163-165].

C_f can not be too large. Otherwise, node D1 and node D3 in Figure 6.20 is AC short, which might disturb the normal operation. In addition, C_f in series with C_{gd3} and C_B is connected in the form of Q -enhancement to M2 (connected between the drain and source of M2). Refer to the analysis in Section 3.3.2 and [80], when C_f increases, the combination of C_f , C_{gd3} , C_B and M2 might generate negative resistance and lead to oscillation.

($f = \frac{1}{2\pi\sqrt{LC}}$), the impedance is purely real and at its maximum. The higher the quality factor of L is, the larger the impedance ($1/G$) is, and the higher the voltage gain is. In practice, the silicon-based on-chip spiral inductor does not have a large quality factor Q . Hence, $1/G$ is not very high, which is generally around several hundreds ohms. In the proposed circuits, a Q -enhancement technique [80-82] is adopted. The MIM capacitor C_e connected between the drain and source of transistor M4, can be used to enhance the quality factor of the resonant network $L_{d2}C_{dM4}$. C_{dM4} is the total capacitance at the drain of M4. Detailed analysis can be found in Section 3.3.2 and [80]. Figure 6.21 (b) illustrates the effect of the proposed Q -enhancement technique. The figure indicates that the introduction of C_e makes the gain improve without increasing the power consumption.

Figure 6.21 (a) Simplified RC shunt feedback; (b) the effect of C_e on the gain and the resonant frequency

The proposed dual-band LNA was fabricated at CSM and was measured using a HP8510C network analyzer with on-wafer RF probes. Figures 6.22 (a) – (c) present

the measured S-parameters and noise figure. It is shown that the LNA reaches dual-band input matching at the 2.45GHz frequency band and the 5.5GHz frequency band respectively. A dual-band power gain of 25dB in the first band and 10dB–12dB in the second band are achieved²¹. The detailed performance characteristics can be found in Table 6.2. The measured data indicate that the LNA's noise figure is not as good as that of GaAs devices. However, it is compact and fully-integrated. The higher NF is mainly due to lossy on-chip integrated inductors. The parasitic resistance of the low- Q inductors has a severe impact on LNA's noise performance. Generally, it contributes 30 percent or even more to the LNA's total noise. Thus, in the future, efforts on high- Q on-chip inductors should be concentrated. Figure 6.22 (d) shows the die photo of the proposed dual-band LNA5.

Table 6.3 compares the performance of several recent dual-band (2.4GHz/5GHz) LNAs with LNA4 and LNA5. The table indicates that LNA4 and LNA5 realize input matching, present good gain performance and achieve comparable noise figure. The comparison proves that the proposed input matching architecture is viable in LNA designs.

Table 6.3 shows that the S_{22} of LNA4 and LNA5 is around -10dB. As explained in Section 5.1.3, one of the reasons is that the load LC parallel network is tuned to

²¹ It is found that the measured power gain of the first band is around 25dB. It is reasonable. LNA5 is a two-stage amplifier. The load network of the first stage is tuned to resonate at 2.45GHz so as to generate a very high impedance, therefore to obtain a high gain G_1 . The second stage is tuned to resonate at around 5.5GHz. However, the second stage still has positive gain G_2 for the first band. The simulated $G_1 + G_2$ for the first band is around 30dB, while the measured one is around 25dB.

resonate at the interest frequency to generate a high impedance, and realize high gain performance. Hence the output impedance is much higher than 50Ω , which leads to a poor S_{22} . In practical applications, LNA is often combined with a mixer. A good interface of the two blocks can be achieved by optimizing the load network parameters (L and C) of the LNA. In this case, a 50Ω output matching is not so necessary. When the output matching is critical, a 50Ω output impedance source follower [73] or other type of output matching network can be adopted.

Figure 6.22 (a) Measured S_{11} and S_{21} ; (b) measured S_{12} and S_{22} ; (c) NF ; (d) die photo of the dual-band LNA ($0.8\text{mm} \times 0.85\text{mm}$)

Table 6.2 Detailed performance characteristics of LNA5

	1 st band	2 nd band
V_{dd} (V)	1.5	
P_d (mW)	19	
Operating Band (GHz)	2.4 – 2.5	5.45 – 5.85
Power Gain (dB)	25	10 – 12
S_{11} (dB)	-16 – -10	-26 – -14
S_{22} (dB)	-18 – -17	-7
S_{12} (dB)	-60 – -18	
NF (dB)	3.6	4

Table 6.3 Comparisons of recent dual-band CMOS LNAs

	[66]**		[104]		[161]		LNA4		LNA5	
	Band1	Band2	Band1	Band2	Band1	Band2	Band1	Band2	Band1	Band2
V_{dd} (V)	2.5		1		0.5		1.5		1.5	
P_d (mW)	10		14.2		2.5		15.3		19	
Power Gain (dB)	14*	15.5*	11.6	10.8	13.9	8.7	18*	16*	25	10 – 12
S_{11} (dB)	-25	-15	-5.1	-26.3	-14.4	-12.4	-15 – -12	-16 – -13	-16 – -10	-26 – -14
S_{22} (dB)	N.A	N.A	N.A	N.A	N.A	N.A	-7	-14 – -10	-18 – -17	-7
S_{12} (dB)	N.A	N.A	N.A	N.A	N.A	N.A	-43		-60 – -18	
NF (dB)	2.3	4.5	2.3	2.9	4.98	6.58	2.35	3.26	3.6	4
Process	0.35 μ m CMOS		0.18 μ m CMOS		0.18 μ m SiGe BiCMOS		0.18 μ m CMOS		0.18 μ m CMOS	

*: voltage gain.

**: off-chip matching

In brief, the proposed CMOS dual-band low noise amplifier covers the operating frequency bands of both Bluetooth and part of wireless LAN. The LNA is implemented entirely on a single-chip and is possible to be integrated with other CMOS devices. The design of the proposed LNA shows that with the constant downscaling of CMOS technology, a fully-integrated, multi-standard wireless communication system can be implemented using low-cost CMOS process.

6.3 Several Considerations in LNA Designs

6.3.1 Stability Considerations

The stability of an amplifier, or its resistance to oscillate, is an important consideration in a design. It can be determined from the S-parameters, the matching networks and the terminations. In a two-port network illustrated in Figure 6.23, oscillations are possible when either the input or output port presents a negative resistance. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$; whereas for a unilateral device, it occurs when $|S_{11}| > 1$ or $|S_{22}| > 1$ [36].

Figure 6.23 A two-port network

The two-port network illustrated in Figure 6.23 is said to be unconditionally stable at a given frequency if the real parts of Z_{IN} and Z_{OUT} are positive for all passive load and source impedance. Otherwise, it is said to be potentially unstable. That is, some passive load and source terminations can produce input and output impedance having a negative real part. Generally, a convenient way of expressing the conditions for unconditional stability is [36]:

$$K > 1 \quad (6.17a)$$

$$\text{and} \quad |\Delta| < 1 \quad (6.17b)$$

$$\text{where } K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (6.17c)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (6.17d)$$

Another way to express the conditions for unconditional stability is [36]:

$$K > 1 \quad (6.18a)$$

$$\text{and } B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (6.18b)$$

From a theoretical point of view, a two-port network can have any value of K and $|\Delta|$. From a practical point of view, most microwave transistors (such as GaAs discrete transistors in microwave engineering area) are either unconditionally stable or potentially unstable with $K < 1$ and $|\Delta| < 1$. In fact, in potentially unstable transistors, most practical values of K are in the range of $0 < K < 1$. These potentially unstable transistors have source and load stability circles that intersect at the boundary of the Smith Chart [36]. The input matching and output matching networks must be optimized, so that the operating frequency region is located at the stable region.

For CMOS low noise amplifier designs, with the rapid development of EDA tools, the optimization of the stable region can be assisted with simulation tools which can pinpoint the source stability circle, load stability circle, the parameters K and B_1 . In all our designs presented in this thesis, Equations (6.18a) and (6.18b) satisfy the required operating frequency regions.

Practically, in CMOS integrated circuits designs, even if the simulation results satisfy Equations (6.18a) and (6.18b), the fabricated circuits might oscillate in some cases when the layout of the circuits is not properly done. In radio frequency, the influence of parasitic capacitance and inductance of interconnection lines becomes

significant. In certain conditions, the parasitic capacitance and inductance can create a positive feedback path and cause oscillation. It can be demonstrated by another LNA (LNA6).

(a)

(b)

Figure 6.24 (a) Simplified schematic of LNA6; (b) measured S_{11} and S_{21} results

The schematic of LNA6 is shown in Figure 6.24 (a). It is a two-stage amplifier with an additional buffer stage for output matching purpose. R_o is around 50Ω . The buffer stage in LNA6 provides around 3 to 4 dB gain. M1 and M2 have equivalent transistor width of $300\mu\text{m}$. M3 and M4 have equivalent transistor width of $180\mu\text{m}$. LNA6 is also designed to work at 2.4GHz band and 5GHz band. The design procedure is similar to Section 6.1, except that a 0.45nH L_s is incorporated in LNA6.

(a)

(b)

Figure 6.25 (a) Partial layout; (b) schematic with parasitic inductance

Figure 6.24 (b) illustrates the measured results of the input reflection coefficient and power gain of LNA6. It is shown that the oscillation occurs at 2.4GHz and

4.6GHz. At 2.4GHz, S_{11} is greater than 0. The results indicate that the LNA is not stable at these two points. However, the simulation results of the K factor and B_1 satisfy the stable condition. Through analyses, it is found that oscillation is caused by parasitics of the layout.

Figure 6.25 (a) depicts partial layout of LNA6. In this case, three ground lines coming from Circuit Block1, Circuit Block2 and Circuit Block3 respectively are connected together at G1, G2 and G3. The interconnection line, which connects G1, G2 and G3 together, is short (around tens of microns). Thus G1, G2 and G3 are merged at the point G only. However, the ground line that reaches the ground pad (GND) is long. It is several hundred microns and has significant effects on the circuit.

In radio frequency, the long interconnection metal line generates parasitic inductance, resistance and capacitance. Here, the long metal line is simply modeled as L_{gnd} . For the voltage supply pad Vdd in this work, some of the Vdd paths are also merged at some points. Thereafter, they reach to the Vdd pad through a long metal path too. This long path is modeled as L_{vdd} . The final schematic is illustrated in Figure 6.25 (b). L_{gnd} and L_{vdd} are added according to the interconnections of the realistic layouts²².

Figure 6.25 (b) indicates that due to the introduction of the parasitic L_{gnd} , point G (G1, G2 and G3) is not really AC or DC grounded anymore. There exists AC and DC potential between G (G1/G2/G3) and the ground pad GND. The AC signals at point G (G1, G2, and G3) can feedback to each other, which finally cause oscillation. In the

²² According to the study done by our group, a metal line, implemented with a top metal using CSM 0.18 μ m CMOS technology, with $L=400\mu$ m and $W=10\mu$ m, can present an inductance around 0.15nH.

proposed LNA6, the load of the first stage is tuned to resonate at 2.4GHz, and the load of the second stage is tuned to resonate at 5.6GHz. Generally, the gain of the lower frequency (2.4GHz in this work) is higher than that of the higher frequency (5.6GHz). The highly amplified 2.4GHz signal feedbacks to the first stage. It definitely affects the matching condition of the 2.4GHz band. Due to the introduction of L_{vdd} , there also exists feedbacks in other paths. The impact of both L_{gnd} and L_{vdd} significantly changes the matching condition of the dual-band LNA and causes oscillation, especially in the lower frequency 2.4GHz. A basic analysis of the instability mechanism is illustrated in Appendix 1.10.1.

A simulation for L_{gnd} and L_{vdd} is carried out. Figure 6.26 (a) shows the simulation results of S_{11} with and without L_{gnd} and L_{vdd} . Figure 6.26 (b) shows the measured results of S_{11} under power on and power off²³. Under “power off” condition, there is almost no potential between G and GND, and the gain of the amplifier is negative. Therefore, there is no strong feedback signal. Consequently, in this case, the measured S_{11} is very similar to the simulation result under the condition of no parasitic L_{gnd} or L_{vdd} . Figure 6.26 (a) and (b) indicate that the trend and shape of the simulated S_{11} with parasitic L_{gnd} and L_{vdd} , are very similar to the measured S_{11} during power on. The results of Figure 6.26 (a) and (b) are roughly compatible. It indicates that the parasitic L_{gnd} and L_{vdd} are possibly the main source of the instability. It is demonstrated by the later designed LNA5, which is presented in Section 6.2. When doing layout of LNA5, the three ground lines as well as the power lines are separated to avoid the common

²³ The difference of S_{11} under power on and power off is also explained in Appendix 1.10.2.

parasitic L_{gnd} and L_{vdd} . The measurement results show that LNA5 is stable. Therefore, it proves that the parasitic L_{gnd} and L_{vdd} are really the instability origins of LNA6.

Figure 6.26 (a) Simulation result of S_{11} with and without L_{gnd} and L_{vdd} ; (b) measured S_{11} under the conditions of power on and power off

To guarantee the stability of the LNA, there are some measures to minimize the impact of L_{gnd} and L_{vdd} from the viewpoint of layout. Firstly, in order to reduce the parasitics, the layout should be compact and the interconnection line should be short. Secondly, it is better to separate the ground line of every circuit block. If possible, different ground pads can be adopted for different circuit blocks. The same method is also required for the layout of the power supply line. Thirdly, decoupling capacitors should be added between the power supply and ground, so that most of the ripples can be filtered out. If permitted, the spare area of the chip can be filled with MOS CAP or MIM CAP. Adopting these methods, another simulation is carried out. The simulation result is given in Figure 6.27 (a), in which the oscillation in Figure 6.26 is eliminated. A layout example using large area decoupling MOS CAPs is illustrated in Figure 6.27 (b). It is a dual-modulus prescaler. There are many common ground lines in the circuit,

but with proper layout and the use of decoupling MOS CAPs, the final measured result is stable.

Figure 6.27 (a) Simulation result of S_{11} after adoption of the mentioned methods; (b) a layout example with large area decoupling CAPs

6.3.2 Input Matching Considerations

In LNA designs, Equation (6.1) $Z_{in} \approx j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} + (g_{m1} / C_{gs})L_s$ is always used to estimate the input impedance. This equation is obtained assuming that C_{gd} is neglected. Figure 6.28 (a) shows a simplified small-signal model for the common source LNA. The input impedance can be derived as:

$$Z_{in} = \frac{(Z_L + Z_{gd})\{Z_{gs}(1 + g_b Z_s) + Z_s(1 + g_m Z_{gs})\}}{(Z_{gs} + Z_{gd})(1 + g_b Z_s) + (Z_s + Z_L)(1 + g_m Z_{gs})} + Z_g \quad (6.19a)$$

Practically, g_b is very small compared to g_m and can be neglected. Equation (6.19a) can be modified as:

Figure 6.28 (a) A simplified small-signal model for common source LNA; (b) a common source LNA

$$Z_{in} = \frac{(Z_L + Z_{gd})\{Z_{gs} + Z_s(1 + g_m Z_{gs})\}}{(Z_{gs} + Z_{gd}) + (Z_s + Z_L)(1 + g_m Z_{gs})} + Z_g \quad (6.19b)$$

When C_{gd} is very small compared to C_{gs} , Z_{gd} can be infinitely large. Equation (6.19a) can be further simplified as:

$$Z_{in} = Z_g + Z_s + Z_{gs} + g_m Z_{gs} Z_s \quad (6.19c)$$

By substituting $Z_g = j\omega L_g$, $Z_s = j\omega L_s$ and $Z_{gs} = 1/(j\omega C_{gs})$ into Equation (6.19c), the frequently used Equation (6.19d) can be obtained:

$$Z_{in} \approx j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} + (g_{m1} / C_{gs}) L_s \quad (6.19d)$$

C_{gd} affects the input matching performance due to the Miller effect. It is illustrated by the example shown in Figure 6.28 (b). By substituting $Z_g = j\omega L_g$, $Z_s = j\omega L_s$ and $Z_{gs} = 1/(j\omega C_{gs})$ into Equation (6.19a), the detailed input impedance equation can be expressed as:

$$Z_{in} = \frac{(Z_L + \frac{1}{j\omega C_{gd}}) \{ \frac{1}{j\omega C_{gs}} (1 + g_b j\omega L_s) + j\omega L_s (1 + g_m \frac{1}{j\omega C_{gs}}) \}}{(\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}})(1 + g_b j\omega L_s) + (j\omega L_s + Z_L)(1 + g_m \frac{1}{j\omega C_{gs}})} + j\omega L_g \quad (6.19e)$$

For the CSM 0.18 μ m technology, an NMOS transistor with a width of 300 μ m and 0.7V gate-bias has following parameters: C_{gs} =0.318pF, C_{gd} =0.09pF, g_m =0.099 and g_b =0.015. According to Equation (6.19e) and the above parameters, the input impedance of the LNA in Figure 6.28 (b) can be calculated. And the input reflection coefficient S_{11} can be calculated using the following equation:

$$S_{11} = 20 \log_{10} \left| \frac{Z_{in} - 50}{Z_{in} + 50} \right| \quad (\text{amplitude in dB}) \quad (6.20)$$

Figure 6.29 C_{gd} effect and cascode effect on S_{11}

Based on Equations (6.19e) and (6.20), the effect of C_{gd} on S_{11} is demonstrated by Curve (a) and Curve (d) as shown in Figure 6.29²⁴. The S_{11} (Curve (a)), neglecting the effect of C_{gd} , matches very well at 2.46GHz. However, after taking into account

²⁴ The two curves are plotted according to Equations (6.19e) and (6.20) using Matlab. Curve (a) is plotted with C_{gd} set to zero in Equation (6.19e). Curve (d) is plotted with C_{gd} set to 0.09pF in Equation (6.19e).

the effect of C_{gd} , the matching frequency shifts about 800MHz to the lower frequency and the matching performance degraded as well (see Curve (d)).

Figure 6.30 The Miller Effect of C_{gd}

Figure 6.30 illustrates the Miller effect of C_{gd} . Based on the Miller theory [90], this capacitor is equivalent to two separate capacitors at the input port and the output port: $C_A = (1 + |A_{vl}|)C_{gd}$ and $C_B = (1 + 1/|A_{vl}|)C_{gd} \approx C_{gd}$, respectively, where A_{vl} is the voltage gain (negative) of M1. Normally, in LNA designs, $|A_{vl}| > 4$, and C_{gd} is around $1/5 C_{gs}$. Therefore, the equivalent gate to source capacitance of M1 is around $2C_{gs}$. The real part generated by $g_m L_s / C_{gs}$ in the traditional source inductive degeneration LNA is greatly reduced (changes to $g_m L_s / 2C_{gs}$). The input impedance with and without C_{gd} can be simplified to:

$$Z_{in1} \approx j\{\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\} + (g_{m1} / C_{gs})L_s \quad \text{without } C_{gd} \quad (6.21a)$$

$$Z_{in2} \approx j\{\omega L_g + \omega L_s - \frac{1}{2\omega C_{gs}}\} + (g_{m1} / (2C_{gs}))L_s \quad \text{with } C_{gd} \quad (6.21b)$$

If L_g and L_s are chose to satisfy Equations (6.21a) at 2.45GHz, namely:

$$\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}} = 0 \quad \text{with } \omega = 2\pi \bullet 2.45 \text{GHz} \quad (6.22a)$$

$$(g_{m1} / C_{gs})L_s = 50 \quad (6.22b)$$

then there are:

$$\omega L_g + \omega L_s - \frac{1}{2\omega C_{gs}} \gg 0 \quad \text{with} \quad \omega = 2\pi \bullet 2.45 \text{GHz} \quad (6.23a)$$

$$(g_{m1} / (2C_{gs}))L_s = 25 \quad (6.23b)$$

The above six equations indicates that at 2.45GHz, when C_{gd} is taken into account, the real part is only 25Ω and the imaginary part doesn't equal to zero any more. The imaginary part exhibits inductive impedance and the resonant point shifts to the lower frequency.

The Miller effect not only degrades the input reflection coefficient, but also degrades the reverse transmission coefficient S_{12} . When the LNA is connected to a mixer directly, the LO leakage from the mixer might feedback to LNA's input port more easily. Besides that, Equation (6.19a) also indicates that the input impedance does not remain constant when the load impedance varies. In other words, the input matching condition varies with the load. The variation of the load impedance has great impact on S_{11} when C_{gd} is large. A high consistency load impedance in the required frequency band is thus necessary.

The Miller effect, poor reverse isolation and load impedance consistency problem can be suppressed by a cascode stage in the low noise amplifier. Figure 6.29 illustrates S_{11} 's results with and without the introduction of the cascode transistor M2. We found that with a larger cascode transistor, the suppression is more efficient. In practical design, M2's size is often the same as M1 or a little smaller than M1. The influence of M2's size on noise figure is discussed in Section 5.1.3. With the isolation

of M2, the reverse transmission coefficient S_{12} improves, and the demand for a highly constant load impedance becomes flexible.

6.4 Summary

In this chapter, a variable inductance network is investigated for the application of dual-band input matching. Two dual-band low noise amplifiers (LNA4 and LNA5) are designed and presented. Both LNAs have two operating frequency bands: 2.4GHz–2.5GHz and 5.47GHz – 5.83GHz. The operating range covers the frequency bands of Bluetooth, IEEE 802.11a/b/g and part of HiperLAN. The designs of the two dual-band LNAs indicate the possibility of implementing a fully-integrated, multi-standard wireless communication system using low-cost CMOS processes.

In the last section of this chapter, two considerations in LNA designs are also highlighted and discussed. They include stability issues and input matching issues. Stability issues are mainly investigated from the viewpoint of layout parasitics. Input matching issues are mainly discussed based on the three concerns: the Miller effect, reverse isolation and load impedance consistency.

Chapter 7 Conclusion and Recommendations

7.1 Conclusion

In this thesis, the design issues of CMOS RFIC designs, especially in single-band LNA and dual-band LNA designs, are investigated extensively in order to find an approach that can help to achieve a compact, reliable and fully-integrated RF system.

Firstly, design issues including input matching architectures, tuning techniques, noise fundamentals, noise models, and considerations for passive components in LNA designs are presented in detail.

Secondly, a modified architecture used for input matching in CMOS low noise amplifier designs, is studied exhaustively. In the proposed architecture, the essential L_g and L_s in the conventional source inductive degeneration CMOS LNAs, are either reduced or removed. As a result, the LNA can be fully-integrated and the consumed chip area is reduced significantly.

The modified architecture is verified by a narrow-band LNA (LNA1) and a wideband LNA (LNA3) operating at 2.4GHz–2.5GHz and 5.1GHz–5.9GHz respectively. The narrow-band LNA has a measured power gain of 24dB, a noise figure of 2.6dB–2.8dB and a power consumption of 15mW. The wideband LNA provides 22.6dB–24.6dB of power gain, 2.85dB–3.5dB noise figure, and draws 9mW power. For comparison, a conventional single-band LNA (LNA2) with source inductor L_s and large on-chip inductor L_g is designed and fabricated as well. The

results indicate that LNA1 with the proposed modified input architecture has higher gain and 37% less chip area.

Thirdly, a variable inductance network is investigated and introduced for dual-band input matching designs. Based on the analysis, two concurrent dual-band low noise amplifiers (LNA4 and LNA5) are successfully designed. Each LNA has two operating frequency bands: 2.4GHz–2.5GHz and 5.47GHz–5.83GHz. The obtained operating range can cover the frequency bands of Bluetooth, IEEE 802.11a/b/g and part of HiperLAN. In the LNA designs, dual-band LNA's load tuning technique and Q -enhancement technique are adopted and presented as well.

Finally, considerations for stability and input matching optimization in LNA design are discussed and emphasized. Stability is mainly investigated from the view point of layout parasitics. The input matching consideration is mainly discussed from the viewpoint of the Miller effect, reverse isolation and the load impedance consistency. An understanding of above-mentioned concerns helps to achieve successful LNA fabrications, so that time is shortened between research development and mass production.

Generally, good investigation and design of a CMOS device provide a deeper insight into the multi-standard operations of RFICs and their characteristics and behavior. This helps to decrease manufacturing cost and enhance system integration during RFIC fabrication.

7.2 Recommendations

Although the designs of single-band LNA, wideband LNA and dual-band LNA have been demonstrated, some issues need to be addressed before the proposed designs can be successfully used for commercial applications. Firstly, in radio frequency, test results of the fabricated circuits usually deviate from simulation results. Therefore, accurate RF models for passive and active devices are required in order to improve the design accuracy. Secondly, it is known that in RFIC design, the performance, especially noise performance (for LNA and VCO), is much related to the inductors. Therefore, efforts for developing high- Q on-chip inductors should be devoted, so as to improve the circuit's performance and enhance system integration. Finally, for an LNA to be used for practical applications, gain control functions should be incorporated. Usually the high/medium/low gain modes can be realized by bias tuning or introducing a gain attenuation branch in parallel with the high-gain load network. The control digital bits and switches are required as well.

In short, the implementation of a fully-integrated, low-cost communication system is becoming more feasible with the development of CMOS technology.

Appendix 1 Equation Derivations

A1.1 Source Resistor Output Noise

The noise expression equations used in Chapter 5 are mainly derived based on the methods presented in [23-24]. When only the noise of source resistor R_S is considered, Figure 5.1 can be simplified to Figure A1.1.

Figure A1.1 Simplified small-signal model for output noise of source resistor R_S

Based on Figure A1.1, neglecting C_{gd} , the following expressions can be obtained:

$$V_{gs} = i \bullet 1/(j\omega C_{gs}) \quad (\text{A1.1a})$$

$$i = \overline{V_{n,R_S}} / (Z_{in} + R_S) \approx \overline{V_{n,R_S}} / (R_S + R_1 + D_0) \quad (\text{A1.1b})$$

$$\overline{i_{n,o,R_S}^2} = |g_m V_{gs}|^2 \quad (\text{A1.1c})$$

$$\overline{V_{n,R_S}^2} = \overline{i_{n,R_S}^2} R_S^2 \quad (\text{A1.1d})$$

where R_1 is the input resistance and D_0 is the imaginary part including “ j ” of the input impedance. D_0 equals to zero at the interested resonant frequency ω_0 . Incorporating Equations (A1.1a) to (A1.1d), the output noise of R_S can be achieved:

$$\overline{i_{n,o,R_s}^2} = \left| \frac{g_m R_s}{j\omega C_{gs} (R_1 + R_s) + j\omega C_{gs} D_0} \right|^2 \overline{i_{n,R_s}^2} \quad (\text{A1.2})$$

A1.2 Channel Noise Output Noise

When only the channel noise $\overline{i_{n,d}}$ is considered, Figure 5.1 can be simplified to

Figure A1.2. Neglecting C_{gd} , the following expressions can be obtained:

Figure A1.2 Simplified small-signal model for output channel noise

$$V_{gs} = -i_2 \bullet 1/(j\omega C_{gs}) \quad (\text{A1.3a})$$

$$\overline{i_{n,o,d}} = \overline{i_{n,d}} + g_m V_{gs} \quad (\text{A1.3b})$$

$$\overline{i_{n,d}} + g_m V_{gs} = i_2 + i_3 \quad (\text{A1.3c})$$

$$i_3 \bullet Z_s = i_2 \bullet (R_s + Z_g + Z_{gs}) = i_2 \bullet (R_s + Z_{in} - Z_s - g_m Z_s Z_{gs}) \quad (\text{A1.3d})$$

$$Z_{in} = Z_g + Z_{gs} + Z_s + g_m Z_s Z_{gs} \quad [23] \quad (\text{A1.3e})$$

$$Z_{gs} = 1/(j\omega C_{gs}) \quad (\text{A1.3f})$$

Equations (A1.3a) to (A1.3c) can be simplified to:

$$\overline{i_{n,o,d}} = \overline{i_{n,d}} + g_m V_{gs} = \overline{i_{n,d}} - g_m i_2 \bullet 1/(j\omega C_{gs}) \quad (\text{A1.3g})$$

$$\overline{i_{n,d}} - g_m i_2 \bullet 1/(j\omega C_{gs}) = i_2 + i_3 \Rightarrow i_3 = \overline{i_{n,d}} - (1 + g_m/(j\omega C_{gs})) \quad (\text{A1.3h})$$

Substituting Equation (A1.3h) into Equation (A1.3d) and incorporating it with Equation (A1.3g), $\overline{i_{n,o,d}}$ can be obtained:

$$\overline{i_{n,o,d}} = \left(1 - \frac{g_m Z_s}{j\omega C_{gs} R_s + j\omega C_{gs} Z_{in}}\right) \overline{i_{n,d}} \quad (\text{A1.4a})$$

$$\overline{i_{n,o,d}^2} = \left|1 - \frac{g_m Z_s}{j\omega C_{gs} R_s + j\omega C_{gs} Z_{in}}\right|^2 \overline{i_{n,d}^2} \quad (\text{A1.4b})$$

In the case of normal source inductive degeneration input stage, in the interested resonant frequency, when the input impedance is perfectly matched, there are the following expressions:

$$Z_s = j\omega L_s \quad (\text{A1.5a})$$

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + j\omega(L_s + L_g) + 1/(j\omega C_{gs}) = \frac{g_m L_s}{C_{gs}} = R_s \quad [23] \quad (\text{A1.5b})$$

Therefore, Equation (A1.4b) should be rewritten to:

$$\overline{i_{n,o,d}^2} = \left|1 - \frac{g_m j\omega L_s}{2j\omega C_{gs} R_s}\right|^2 \overline{i_{n,d}^2} = \left|1 - \frac{1}{2R_s} \frac{g_m L_s}{C_{gs}}\right|^2 \overline{i_{n,d}^2} = \left|1 - \frac{1}{2R_s} R_s\right|^2 \overline{i_{n,d}^2} = \frac{1}{4} \overline{i_{n,d}^2} \quad (\text{A1.6a})$$

In the case of LNA1, there is no degeneration L_s and $Z_s \approx 0$. Hence Equation (A1.4b) should be expressed as:

$$\overline{i_{n,o,d}^2} = \overline{i_{n,d}^2} \quad (\text{A1.6b})$$

A1.3 Thermal Resistor R_Δ Output Noise

The derivation method of the output noise of the gate parasitic resistance R_Δ is the same as the method presented in Section A1.1. And its output noise is expressed as:

$$\overline{i_{n,o,R_\Delta}^2} = \left| \frac{g_m R_\Delta}{j\omega C_{gs} (R_1 + R_s) + j\omega C_{gs} D_0} \right|^2 \overline{i_{n,R_\Delta}^2} \quad (\text{A1.7})$$

A1.4 Gate Induced Noise Output Noise

Neglecting the channel charging resistance R_i [153], Figure 5.1 can be simplified to Figure A1.3. Neglecting C_{gd} and channel charging resistance R_i [153], the following expressions can be obtained:

Figure A1.3 Simplified small-signal model for output gate induced noise

$$\overline{V_{n,g}} \approx \overline{i_{n,g}} / (j\omega C_{gs}) \quad (\text{A1.8a})$$

$$V_{gs} = \overline{V_{n,g}} - i / (j\omega C_{gs}) \quad [24] \quad (\text{A1.8b})$$

$$\overline{i_{n,o,g}} = g_m V_{gs} \quad (\text{A1.8c})$$

$$i = \overline{V_{n,g}} / (Z_{in} + R_s) \approx \overline{V_{n,g}} / (R_s + R_1 + D_0) \quad (\text{A1.8d})$$

Based on the above equations, the output gate induced noise can be expressed as:

$$\begin{aligned} \overline{i_{n,o,g}^2} &= |g_m V_{gs}|^2 \approx \left| g_m \frac{\overline{i_{n,g}}}{j\omega C_{gs}} \cdot \left(1 - \frac{1}{j\omega C_{gs} (R_s + R_1 + D_0)} \right) \right|^2 \\ &= \left| \frac{g_m}{j\omega C_{gs}} \left(1 - \frac{1}{j\omega C_{gs} (R_s + R_1) + j\omega C_{gs} D_0} \right) \right|^2 \overline{i_{n,g}^2} \end{aligned} \quad (\text{A1.9})$$

A1.5 Thermal Noise of The Output Resistance

Figure 5.1 indicates that the thermal noise of the output resistance R_{out} directly adds to the total output noise. Hence, there is:

$$\overline{i_{n,o,R_{out}}^2} = \overline{i_{n,R_{out}}^2} \quad (A1.10)$$

A1.6 Output Noise of Drain/Gate Correlation Noise

The drain channel noise $\overline{i_{n,d}}$ and gate induced noise $\overline{i_{n,g}}$ has correlation [23-24].

The correlation part can be achieved through [24]:

$$\overline{i_{n,o,corr}^2} = (jcHK^* - jcH^*K)\sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} \quad (A1.11a)$$

$$H = \frac{g_m}{j\omega C_{gs}} \left(1 - \frac{1}{j\omega C_{gs}(R_s + R_l) + j\omega C_{gs}D_0}\right) \quad (A1.11b)$$

$$K = 1 \quad (A1.11c)$$

H and K are the transfer functions in Equations (A1.9) and (A1.6b) respectively. Thereafter, Equation (A1.11a) can be rewritten to:

$$\overline{i_{n,o,corr}^2} = \frac{2g_m c}{\omega C_{gs}} \left(1 - \frac{jD_0}{\omega C_{gs}((R_s + R_l)^2 + |D_0|^2)}\right) \sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} \quad (A1.12)$$

When the imaginary part $D_0=0$ in the interested resonant frequency, it can be simplified to:

$$\overline{i_{n,o,corr}^2} = \frac{2g_m c}{\omega_0 C_{gs}} \sqrt{\overline{i_{n,g}^2} \cdot \overline{i_{n,d}^2}} \quad (A1.13)$$

A1.7 Derivation of Equation (5.6)

From [23] and [128], there are Equations:

$$g_{d0} = g_m / \alpha \quad (A1.14a)$$

$$\omega_T = g_m / C_{gs} \quad (\text{A1.14b})$$

By substituting Equations (A1.14a) and (A1.14b) into Equation (5.3), the following expression can be obtained:

$$F_0 = 1 + \frac{R_\Lambda}{R_S} + \frac{\delta\alpha}{5g_m R_S} [1 + \alpha_0^2 C_{gs}^2 (R_S + R_1)^2] + \frac{\gamma}{\alpha g_m R_S} \alpha_0^2 C_{gs}^2 (R_S + R_1)^2 + \frac{2c}{g_m R_S} \sqrt{\frac{\gamma\delta}{5}} \alpha_0^2 C_{gs}^2 (R_S + R_1)^2 \quad (\text{A1.15})$$

In CMOS LNAs, the MOS transistor usually operates in the saturation region [40, 128]. When the transistor operates in the saturation region, there are [24, 128]:

$$I_{ds} = \frac{W}{2\xi L_{eff}} \mu_{eff} C_{ox} (V_{GS} - V_T)^2 \quad (\text{A1.16})$$

$$C_{gs} \approx \frac{2}{3} W L_{eff} C_{ox} \quad (\text{A1.17})$$

where μ_{eff} is the carrier's effective mobility in the transistor channel; ξ is a factor which takes the short channel effect and other effect into account [24]; W is the transistor width and L_{eff} is the channel length. Taking the derivative of Equation (A1.16) with respect to V_{GS} yields:

$$g_m = \frac{W}{\xi L_{eff}} \mu_{eff} C_{ox} (V_{GS} - V_T) = \sqrt{\frac{2W}{\xi L_{eff}}} \mu_{eff} C_{ox} I_{ds} = D_1 \bullet W^{1/2} \quad (\text{A1.18})$$

where D_1 is a function of power consumption $P_d = V_{dd} I_{ds}$.

By substituting Equations (A1.17) and (A1.18) into Equation (A1.15), the noise factor can be rewritten to:

$$F_0 = 1 + \frac{R_\Lambda}{R_S} + \frac{\delta\alpha}{5R_S} \left[\frac{1}{D_1} W^{-1/2} + \frac{4}{9D_1} \alpha_0^2 C_{ox}^2 L_{eff}^2 (R_S + R_1)^2 W^{3/2} \right] + \frac{4\gamma}{9\alpha R_S D_1} \alpha_0^2 C_{ox}^2 L_{eff}^2 (R_S + R_1)^2 W^{3/2} \quad (\text{A1.19})$$

$$+ \frac{8c}{9D_1 R_S} \sqrt{\frac{\gamma\delta}{5}} \alpha_0^2 C_{ox}^2 L_{eff}^2 (R_S + R_1)^2 W^{3/2} = 1 + \frac{R_\Lambda}{R_S} + k_1 W^{-1/2} + k_2 \alpha_0^2 L_{eff}^2 W^{3/2}$$

$$k_1 = \frac{\delta\alpha}{5D_1 R_S} \quad (\text{A1.19a})$$

$$k_2 = \frac{4\delta\alpha}{45D_1 R_S} C_{ox}^2 (R_S + R_1)^2 + \frac{4\gamma}{9\alpha R_S D_1} C_{ox}^2 (R_S + R_1)^2 + \frac{8c}{9D_1 R_S} \sqrt{\frac{\gamma\delta}{5}} C_{ox}^2 (R_S + R_1)^2 \quad (\text{A1.19b})$$

A1.8 Derivation of Equation (5.8b)

A part of the simplified small-signal model of Figure 5.4 is illustrated in Figure A1.4. According to [32], the voltage gain of node X is:

Figure A1.4 Simplified small-signal model for LNA1

$$A_{M1} \approx -g_{m1}|Z_X| \quad (\text{A1.20a})$$

At the resonant frequency, the parallel $L_d C_{d2}$ network exhibits very high impedance. For analysis simplicity, the impedance at node X roughly comes from the capacitance at node X [162], where

$$C_X = C_{gs2} + C_{dB1} + (1 + |1/A_{vM1}|)C_{gd1} \approx C_{gs2} + C_{dB1} + C_{gd1} \quad (\text{A1.20b})$$

Hence, Equation (A.12a) can be rewritten to:

$$A_{M1} \approx -\left| \frac{g_{m1}}{j\omega C_X} \right| \quad (\text{A1.21})$$

A1.9 Determination of L and C Parameters in Equation (6.14)

In practical LNA designs, the transistor width of M1 is usually hundreds of microns [23-24, 80]. For CSM 0.18 μm CMOS process, at a moderate bias voltage

(around 0.7V), an NMOS transistor width of 240 μ m has a drain current around 10mA. Hence, $W=240\mu$ m is chosen as the initial width of M1. Based on the analysis of Page 119, $L_s=0.32$ nH, $L_{g1}=8.85$ nH ($\omega_{01}=2.45$ GHz) and $L_{g2}=1.43$ nH ($\omega_{02}=5.6$ GHz) are obtained.

Figure A1.5 The variable inductor network in a dual-band LNA

For the network illustrated in Figure A1.5, there are:

$$\frac{L_1}{1 - \omega_1^2 L_1 C_1} + L_A = 8.85 \text{ nH} \quad (\text{A1.22a})$$

$$\frac{L_1}{1 - \omega_2^2 L_1 C_1} + L_A = 1.43 \text{ nH} \quad (\text{A1.22b})$$

$$\text{Let } \frac{1}{2\pi\sqrt{L_1 C_1}} \approx 4 \text{ GHz} \quad (\text{A1.22c})$$

where ω_1 and ω_2 are the centre frequencies of the two operating frequency bands respectively. Through calculation, $L_1 \approx 2.81$ nH, $C_1 \approx 0.563$ pF and $L_A = 4.36$ nH are achieved. However, for CSM 0.18 μ m CMOS process, there is no inductor model for a 4.36nH inductor. In LNA5, the 4.36nH inductor is approximated by the $L_A C_p$ network as shown in Figure 6.15a (with $L_A=3.2$ nH, $C_p=0.1$ pF and $\omega_p=8.9$ GHz. The choosing of L_A quite depends on the inductor model amount provided by foundry.). The $L_A C_p$ network is corresponding to an inductance of 3.46nH (2.45GHz) and an inductance of 5.1nH (5.6GHz). Practically, it is not recommended to use such a network to replace the 4.36nH inductor, since the $L_A C_p$ network can not generate a constant 4.36nH

inductance over a wide frequency range. The circuit can not get perfect match at the two corresponding frequencies. Owing to lack of inductor models, this method is adopted in LNA5.

After choosing the initial values, the initial schematic can be built up. The parameters, including transistor width, inductor and capacitor values, can be adjusted and optimized through subsequent noise figure/input matching/power gain simulations. It is really a complicated process.

Figure A1.6 Feedback paths to stage 1

A1.10 Instability Issue Analysis of Section 6.3.1

A1.10.1 Instability Issue of Section 6.3.1

As Figure 6.25 (b) illustrated, due to the introduction of the parasitic L_{gnd} , node G (G1, G2 and G3) is not really AC or DC grounded anymore. The signal of stage 1, stage 2 and stage 3 may feedback to each other. There are mainly three feedback paths: signal of stage 2 feeds to stage1 and signal of stage 3 feeds to stage1; signal of stage 1

feeds to stage 2 and signal of stage 3 feeds to stage2; signal of stage 1 feeds to stage 3 and signal of stage 2 feeds to stage 3. Figure A1.6 shows the feedback paths to stage 1. It forms two loops.

The signal with amplitude A at the gate of M1 is firstly amplified by stage 1 (original gain of A_1). Secondly, it passes by stage 2 (gain of A_2). Thirdly, it comes out of stage 3 (gain of A_3). The total gain should be around $A_1 A_2 A_3$ (A_1 , A_2 and A_3 are expressed in magnitude, not in decibels). If the signal comes out of stage 3 at the source node of M5 (illustrated in Figure 6.24 (a)), stage 3 can be treated as a source follower, owing to the introduction of the parasitic inductor L_{gnd} . The gain from gate to source is A_{3a} . Then the initial signal amplitude at source of M5 should be around $(A_1 A_2 A_{3a})A$.

Here, for simplicity, only the feedback path 2 in Figure A1.6 is analyzed. The signal with amplitude of $(A_1 A_2 A_{3a})A$ at the source node of M5, then feeds to node G. If $\kappa(A_1 A_2 A_{3a})A$ passes by L_s into transistor M1, the signal at node D2 should be around $\kappa(A_1 A_2 A_{3a})A \bullet A_{1a}$, where κ is the section portion that the signal at G passes by L_s , and A_{1a} is the gain from node G to node D2. When the source of a transistor is used as the input port, it is connected as common gate form. The common gate gain is [90]:

$$A_v = g_m (1 + \eta) R_{load} \quad (A1.23a)$$

$$\eta = \partial V_{TH} / \partial V_{SB} \quad (A1.23b)$$

In LNA6, R_{load} is approximated to the impedance of $L_d C_d$ tank. Thus, in the resonant frequency, the gain A_{1a} (from G to D2) should be high. The signal with

amplitude of $\kappa(A_1 A_2 A_{3a}) A \bullet A_{1a}$ passes by stage 2 and stage 3 and reaches to the source of M5 again with the amplitude around $\kappa(A_1 A_2 A_{3a}) A \bullet A_{1a} A_2 A_{3a}$. If this signal repeats the above-mentioned transmission again, the signal at the source of M5 is changed to $\kappa^2(A_1 A_2 A_{3a}) A \bullet (A_{1a} A_2 A_{3a})^2$. After n rounds, it reaches to:

$$\kappa^n(A_1 A_2 A_{3a}) A \bullet (A_{1a} A_2 A_{3a})^n, \quad n = 1, 2, 3, 4, \dots \quad (\text{A1.24})$$

In LNA6, $L_{d1}C_d$ tank is designed to resonate at 2.4GHz band, therefore A_{1a} is high. A_2 also has positive gain. In the case of the parasitic L_{gnd} is large (comparable to L_s), the amplification coefficient $\kappa(A_{1a} A_2 A_{3a})$ can satisfy:

$$\kappa(A_{1a} A_2 A_{3a}) > 1 \quad (\text{A1.25})$$

Hence, the circuit oscillates in this frequency. The feedback of other paths can speed the oscillation. When Equation (A1.25) is satisfied in other frequency, the circuit can oscillate in the corresponding frequency too. It is known from the oscillation design theory [32] that the amplitude can not increase infinitely. It will reach a steady oscillation after a certain time.

A1.10.2 Input Reflection Coefficient Issue of Section 6.3.1

It can be found from Figure 6.26 (b) that LNA6 obtains input matching in the case of “power off”. But in the case of “power on”, S_{11} is greater than zero in 2.4GHz, which indicates LNA6 is not stable in this frequency. LNA6 shown in Figure 6.24 (a) can be illustrated in Figure A1.7 with the simplified small-signal transistors models. Based on Equation (6.19(b)), there is:

$$Z_{in} = \frac{(Z_L + Z_{gd1})\{Z_{gs1} + Z_{s1}(1 + g_{m1}Z_{gs1})\}}{(Z_{gs1} + Z_{gd1}) + (Z_{s1} + Z_L)(1 + g_{m1}Z_{gs1})} + Z_{g1} \quad (\text{A1.26a})$$

where Z_L denotes the load impedance at the drain of M1. For simplification, neglecting C_{gd} , Equation (A1.26a) can be simplified as:

$$Z_{in} = Z_{g1} + Z_{s1} + Z_{gs1} + g_m Z_{gs1} Z_{s1} \quad (\text{A1.26b})$$

Figure A1.7 Small-signal model of LNA6

By substituting $Z_{g1} = j\omega L_g + R_g$ and $Z_{gs} = 1/(j\omega C_{gs1})$ into Equation (A1.26b), another equation can be obtained:

$$Z_{in} = R_g + Z_{s1} + j(\omega L_g - \frac{1}{\omega C_{gs1}}) + \frac{g_{m1} Z_{s1}}{j\omega C_{gs1}} \quad (\text{A1.26c})$$

where L_g is the equivalent gate inductance and R_g is the equivalent gate resistance, which can be found from Section 6.1.1. The source network is L_s in series with $L_{gnd} Z_1$ network as shown in Figure A1.8.

Figure A1.8 The source network

Under “power off” condition (namely the bias voltage is set to zero), all the NMOS transistors turn off and g_{mx} ($x=1, 2, 3, 4, 5$) is zero. Their responding channel charging resistance r_{ox} is very large. The load network exhibits very high impedance. And the source network can be approximately simplified to an inductor L_{s2} (L_s in series with L_{gnd} and possibly some resistance). Then Equation (A1.26c) can be rewritten to:

$$Z_{in} = R_g + j(\omega L_g + \omega L_{s2} - \frac{1}{\omega C_{gs1}}) + \frac{g_{m1}(=0)\omega L_{s2}}{\omega C_{gs1}} = R_g + j(\omega L_g + \omega L_{s2} - \frac{1}{\omega C_{gs1}}) \quad (A1.26d)$$

Based on the analysis in Section 6.1.1, it is known that R_g is close to 50Ω . And at most of the time, the source inductor L_s (to generate $g_{m1}L_s / C_{gs}$) can be set to a very small value or it can be even removed. Therefore, according to Equation (A1.26d), under “power down” condition, the input impedance is matched in the two operating frequency bands of interest. Hence, the curve in “power down” case plotted in Figure 6.26 (b) is much like the simulation curve with no parasitic L_{gnd} .

Under “power on” condition, all the NMOS transistors turn on and g_{mx} ($x=1, 2, 3, 4, 5$) is not zero anymore. It is known from Equation (A1.26a) that the load impedance definitely has influence on the input impedance. According to the analysis in Section A1.10.1, the circuit oscillates when “power on”. Under an oscillation

condition, there is possibly negative resistance $-R_{neg}$ created in the loop, which will affect the input impedance at the oscillation frequency points:

$$Z_{in} = R_1 - R_{neg} + j*(imaginary\ part) \quad (A1.27)$$

In the case of $R_1 - R_{neg} < 0$, S_{11} is greater than 0. The input resistance is negative at 2.4GHz in LNA6. Therefore, the “power on” S_{11} curve in Figure 6.26 (b) has a positive point at 2.4GHz, which is different from the “power off” curve.

Appendix 2 LNA Measurement Setup

The fabricated LNAs are tested with on-wafer RF probes. Figure A2.1 illustrates the equipments for LNA testing:

- Vector network analyzer : HP8510C
- DC power supplier: HP4142
- Bias network (bias tee) 11612B K11 and 11612V K21
- Workstation with IC-CAP software for S-parameter measurement control
- ATN NP5B noise parameter and S-parameter device characterization system from ATN Microwave Inc

Figure A2.1 LNA test equipments setup

A2.1 S-parameter Measurement

S-parameter measurements are carried out according to the following steps:

- Connecting the network analyzer, workstation with IC-CAP software, bias tee and other necessary equipments.
- Equipment calibration.
- LNA S-parameter testing.

Throughout the testing, DC biasing and frequency sweep range and step are controlled through IC-CAP software.

A2.2 Noise Figure Measurement

Noise figure measurement is controlled by ATN NP5B noise parameter and S-parameter device characterization system. The measurement is carried out according to the following steps:

- Connecting the network analyzer, IC-CAP software, bias tee, ATN NP5B system and other necessary equipments.
- ATN NP5B system calibration (load, open and thru).
- ATN NP5B S-parameter calibration.
- Noise figure testing.

Through noise figure testing, IC-CAP is used only to control the DC biasing. The frequency sweep step and range are controlled by ATN NP5B system. ATN NP5B system firstly conducts S-parameter testing. Then the system will automatically calculate the corresponding noise figure. Detailed information is expected to be found from ATN Microwave Inc.

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