Characterization and modeling of on-chip interconnects for silicon RFIC design

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CHARACTERIZATION AND MODELING OF ON-CHIP INTERCONNECTS FOR SILICON RFIC DESIGN

ONG BENG HWEE

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING
NANYANG TECHNOLOGICAL UNIVERSITY

2005

**Characterization and Modeling of On-chip
Interconnects
For Silicon RFIC Design**

Ong Beng Hwee

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Master of Engineering

2005

STATEMENT OF ORIGINALITY

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Ong Beng Hwee

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SUMMARY

The characterization and modelling of on-chip interconnects had been carried out in this project. First, an overview of the on-chip interconnect on lossy silicon-based process is presented. Second, on-wafer high frequency measurements of the on-chip interconnects are carried out and investigated in depth. A new figure of merit, Quality factor, is proposed for the on-chip interconnects on lossy silicon to measure its behaviour in a high frequency environment. Third, a new lumped/distributed hybrid physical model for the on-chip interconnect on lossy silicon, which is capable of providing simpler and more accurate predictions, as compared to the conventional inductor model is developed in this thesis.

Forth, the evaluation of the new hybrid on-chip interconnect model is performed using two different high frequency circuits. More specifically, three giga-hertz amplifiers are designed with different interconnect widths and they are fabricated and measured for their S-parameters. Comparisons are made on the measurement results for the effects of different interconnect widths. Next, a high frequency voltage-controlled oscillator is fabricated and measured. With the new on-chip interconnect model, the simulated results are then used to compare with the measured results. Finally, the effects of the 45 degree bend on the performance of the on-chip interconnect are also measured and studied against the straight on-chip interconnect.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Increasing demands for personal mobile communication equipments have motivated recent research activities to focus on the development of inexpensive, small size, low power consumption and low noise systems [1-18]. Because of its mature technology, low fabrication cost as well as high packing density, silicon has been recognized as the most suitable material to meet the demands of this rapidly growing wireless communication market [1]. The use of silicon for Radio Frequency Integrated Circuits (RF ICs) is now finding wider applications in the giga hertz frequency range. This is largely due to the fact that modern Bipolar, CMOS and BiCMOS processes are able to provide high performance transistors, allowing silicon RF ICs to compete with GaAs ICs in the important low GHz frequency range (DC to 5GHz).

For many years, device studies for RF ICs on silicon have been very much focus on active device such as MOSFETs and passive devices such as the capacitor and inductor. To build high-performance transceivers, these devices are the essential ingredients for designing RF front-end circuits such as low noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), RF switches and RF power amplifiers. However, in-depth studies for interconnect on silicon, especially in high frequency, has always been neglected or overlooked. Similar to the fabrication of the silicon on-chip spiral inductor, on-chip interconnects on silicon are fabricated on lossy substrate, hence suffer from capacitive and magnetic losses. In addition, thin metal lines giving high dynamic resistance at GHz frequencies further aggravate the signal integrity hence the overall RF circuit performances in the CMOS technology. As such, there are great incentives in studying and characterizing interconnects on silicon and this is fast becoming the current key research area [18-19].

Efforts put in by researchers for the studies of silicon-based interconnect can be categorised into two areas [20-23]. The first area is on the studies of materials used to

better the performance of the silicon-based interconnects. Aluminium (Al) is the traditionally used material on silicon-based ICs. This is because it is inert with silicon and silicon dioxide but the conductivity of Al is apparently inferior than copper (Cu). Copper is an excellent electrical conductor but it readily forms intermetallic compounds with several semiconductors including silicon and it has electromigration problems. The mixture of Aluminium-Copper (AlCu) to be used in silicon-based interconnects provide the best compromise to exploit the advantages of each metal while avoiding the problems associated with either metal on its own. As ICs feature size is scaled below $0.18\mu\text{m}$, the use of copper, copper alloy or copper with buffer layers is essential. This is to reduce the resistance of the conductors. In the area of material studies for silicon-based interconnects, researchers have also recommended the used of low-K dielectrics for multi-layers metal interconnects. Conventionally, silicon-based ICs used silicon-dioxide (SiO_2) insulators between multi-layers conductors. For high frequency operation, it is necessary to use insulator materials with permittivities below that of SiO_2 (~ 4) to reduce the self-capacitance and mutual coupling of neighbouring interconnects.

The second area, which researchers are studying on the silicon-based interconnects, is to fully characterize the behaviours of interconnect lines in high-frequency environment just like characterising a passive device such as the on chip spiral inductor. The motive is apparently to allow circuit designers to accord for the effects of the silicon-based interconnects into their design so as to achieve the target performances [1-4]. In this area, many techniques have already been proposed and some are adopted by the industries to predict the performance of silicon-based interconnects. This project aims to investigate some of these existing techniques, develop new and effective ones and also put the newly developed techniques into practical experiments.

1.2 OBJECTIVES

The objectives of this project are summarised as follows:

- (i) To study and understand the various behaviours of silicon-based interconnects in a high frequency environment;
- (ii) To study the behaviours of the silicon-based interconnects with various physical orientations;
- (iii) To fully characterize the silicon-based interconnects;
- (iv) To develop an accurate, simple, physical and scalable model for silicon-based interconnects; and
- (v) To study the effect of the developed model.

1.3 MAJOR CONTRIBUTIONS OF THE THESIS

The major contributions of this thesis are broadly presented in the following sub-sections:

- (i) In this project, a simple, physical, accurate and scalable silicon-based interconnect model has been developed. The introduction of a new resistive element to model the skin effects as well as the non-uniform current flow within the interconnect metal conductor not only simplifies the entire modelling process but also provides better accuracy and scalability. The use of the double Π network in the model helps to describe the distributed effects seen in long interconnects. A comparative evaluation shows that the new model can predict more accurately both the inductance and S-parameters of silicon-based interconnects with different sizes as compared to the conventional model. This model is an essential tool for both RF IC designers and process engineers. This

work has been presented and published in the 2004 International Workshop on System Level Interconnect Prediction (Author's Publications [1]) and 2004 IEEE Radio and Wireless Conference (Author's Publications [2]).

- (ii) The behaviours on various orientations for the silicon-based interconnects are also studied in this project. A general guide rules for the use of interconnect on silicon-based material are written to allow circuit designers to optimise their layout in term of circuit performance and silicon space.
- (iii) Two RF circuits, namely a RF amplifier and a voltage-controlled oscillator, are designed and fabricated to investigate the consequences of the newly developed scalable silicon-based interconnect physical model.

1.4 ORGANIZATION OF THE THESIS

This thesis is organised into 6 chapters. Chapter 1 presents the motivation of this research work. It also defines the objectives of the project and highlights the major contributions of the thesis.

Chapter 2 provides a comprehensive literature review of silicon-based interconnects. The various basic definitions of interconnects are covered in details. Various loss mechanisms pertaining to interconnect on silicon are also discussed.

Chapter 3 focuses on the high frequency measurement on the on-chip interconnect test structures. The high frequency on-wafer measurement calibration methodology is discussed together with the de-embedding techniques used on the measurement of the on-chip interconnects. The measurement results for all the test structures are then presented and discussed in details. Finally, a new quality (Q) factor definition for interconnect on silicon is proposed.

Chapter 4 concentrates on the physical modelling of the on-chip interconnect. Various commonly used on-chip interconnect model is put forward and discussed. A new physical

model for on-chip interconnect is proposed to complement the weakness of the commonly used on-chip interconnect physical model. The performance of the new physical model for on-chip interconnects are presented and discussed eventually.

Chapter 5 verifies the accuracy of the new on-chip interconnect physical model. Two radio frequency circuits, a RF amplifier and a voltage-controlled oscillator, are designed to help in accessing the accuracy of the new model. Simulations of the circuits performances are made for three cases, 1) with no interconnect model, 2) with conventional parasitics extraction for interconnect and 3) with the new interconnect model. All the simulated results are then compared with the actual measured results to validate the accuracy of the new interconnect model.

Finally, Chapter 6 summarizes the results of this work and recommends a few promising areas for future research.

CHAPTER 2

LITERATURE REVIEW

2.1 DEFINITIONS FOR VARIOUS INTERCONNECTS

Interconnects serve the basic function of providing electrical connections for active devices, such as the MOS and BJT, at the lowest level to the system level connections, such as a GSM (Global System for Mobile Communications) mobile phone, at the highest of a electrical connections hierarchy. The interconnect hierarchy can be defined as follows:

Level 1 Interconnect: Chips

Level 2 Interconnect: Multi-Chip Modules (MCM Package)

Level 3 Interconnect: Printed Circuit Board (PCB)

Level 4 Interconnect: BackPlane (Package)

Level 5 Interconnect: Rack, Connect Systems (Package)

The size of interconnects varies with interconnect level with both the smallest interconnects, both in cross-section and in length, being at the chip level. At the various level in the interconnect hierarchy, interconnects are designed and modelled differently. Method such as electromagnetic (EM) simulation using HFSS (High-Frequency Structure Simulation) or ADS (Advanced Design System), circuit model using partial element equivalent circuits (PEEC) and passive device physical modelling are used on different level on the hierarchy.

2.2 OVERVIEW OF ON-CHIP INTERCONNECTS IN HIGH FREQUENCY DESIGN

With fast growth in the radio-frequency (RF) wireless communications market, the demand for high performance but low cost RF solution is rising. The common perception is that silicon CMOS is suitable for digital applications while other technologies such as silicon bipolar and III-V material based processes are suitable for high-frequency applications. However, advances in CMOS fabrications have resulted in deep submicron

transistors with high transit frequencies and low noise figures. RF designers have already started to explore the use of CMOS technology in RF circuits. In Table 2.1, the RF performance of several generations of CMOS technologies is listed. The F_t (the frequency at which the current gain of the device equals to 1) for a 0.25 μm CMOS process is around 30GHz, while the F_t for a 0.18 μm CMOS process is in the 50GHz range. The improvement in F_t is primarily due to the result of aggressive device scaling.

Table 2.1 RF performances in MOSFETs in different technology generations.

Year	1995	1997	1999	2001	2003
L (μm)	0.25	0.18	0.14	0.12	0.1
F_t (GHz)	33	49	70	84	112
F_{max} (GHz)	41	47	51	52	60
NF_{min} (dB)	0.5	0.35	0.23	0.2	0.15

(F_{max} is the frequency at which the maximum available power gain of the device equals to 1)

(NF_{min} is the minimum noise figure)

The advanced performance of MOSFETs is attractive for RF circuit design in view of a system-on-chip realization, where digital, mixed-signal base-band and RF transceiver blocks would be integrated on a single chip.

On-chip interconnect is fast becoming the bottom-neck to the advancement of silicon technology. It exhibits negative effects while MOSFET's performance continues to improve due to device scaling. CMOS on-chip interconnects are fabricated on a lossy silicon substrate, typically with resistivity of about 10-20m Ω -cm. This causes potential signal loss as operating frequency increased into giga hertz range. The presence of loss mechanism due to series resistive, substrate capacitive and series self-inductance that is frequency dependence in on-chip interconnects, will get worse with higher operating frequency.

2.3 THE CONCEPT OF RADIO FREQUENCY TRANSMISSION LINE

When transmission line structures have dimensions, which are substantially smaller than the wavelengths of the signals being transmitted, then the structures may be satisfactorily analysed on the basis of line voltages and currents. Considering if the level of a signal is reasonably constant along the entire length of an interconnect, then it can be safely be treated as a lump element and need not be treated as a transmission line. If the signal is a sinusoid then it is generally agreed in [24] that the signal does not change much in time over an interval equal to one twentieth of the period, T , of the signal. Consider a sinusoidally varying signal, $x(t) = A \sin(\omega t)$, where $\omega = 2\pi f$, is the radian frequency of the signal and $f = 1/T$ is its frequency so that $x(t) = A \sin(2\pi t/T)$. The maximum changes occurs when the signal goes from a time, $t = -\alpha T/2$ to $t = +\alpha T/2$ where α is the fraction of the period. So in one twentieth of the period ($\alpha = 0.05$) the signal can change by 16% of its maximum possible change in value. Hence when the interconnect line is less than $1/20^{\text{th}}$ of the wavelength, λ , of the signal, it is regarded as safe to use a lumped circuit model for the interconnect. Table 2.2 below illustrates the model criteria for interconnect.

Table 2.2 Model criteria for interconnect.

Signal Type	Model Required	
	<i>Transmission Line model</i>	<i>Lumped model</i>
<i>Sinusoid</i>	Length $> \lambda/10$	Length $< \lambda/20$

Using the criteria in Table 2.2, the physical length of the interconnect can be computed over frequency,

$$\text{Critical length} < \lambda / 20$$

Where $\lambda = c / \text{frequency}$ $c = \text{speed of light (in free space} \cong 3\text{e}+08 \text{ m/sec)}$

$$\text{Critical length} < c / (\text{frequency} * 20)$$

Table 2.3 Interconnect Lumped Model Frequency Range Vs Physical Length Range.

Frequency (GHz)	10	20	30	40	50
Critical Length=$\lambda/20$ (μm)					
i) in free space (μm)	1500	750	500	375	300
ii) in silicon $\epsilon_r=11.9$ (μm)	434	217	145	109	87

As the frequency goes higher, and correspondingly the wavelength becomes smaller, it is necessary to set up a complete electromagnetic field solution to analyse the line structures. If we assume small line dimensions prevail, then a number of useful results are obtained on a voltage and current basis. The theory thus developed is called the distributed circuit theory. With operating frequency for silicon chip in radio frequency applications moves into giga-hertz range, the dimensions of the chip and the interconnects use in the design are approaching an order of magnitude in relation to the wavelength of the transmitted signals. At these frequencies, transmission line effects may begin to interfere with the proper operation of the signal propagating across the chip.

The response of the interconnect line depends on the source resistance and the termination resistance looking into and out of the interconnect line [25]. If the source resistance is much larger than the interconnect line impedance, only a small portion of the applied voltage will be placed on the line initially. The voltage will slowly increase, in exponential fashion until reaching steady state over time. In such cases, the interconnect line effect is negligible and the line could be approximated by a lumped RLC physical model. If the source resistance is reduced and the line's response begins to include more and more ringing over time, this demonstrates the delay through the transmission line. In such cases, a transmission line is a better approximation. Alternatively, this kind of line can be approximated by cascading several interconnect lump models, for a reasonable accuracy.

2.3.1 Transmission Line Constants

In a uniform transmission line, the line parameters are defined as follows:

Resistance per unit length	= R
Inductance per unit length	= L
Conductance per unit length	= G
Capacitance per unit length	= C

R, L, G and C are referred to as resistance, inductance, conductance and capacitance per unit length. In most radio-frequency transmission lines, the effects due to L and C tend to dominate because of the relatively high inductive reactance and capacitive susceptance. In such cases, we refer to “loss-free” or “lossless” line although in practice some information about R or G maybe necessary to determine the actual power losses. The lossless concept is just a useful and good approximation. The propagation of a wave along the line is characterized by the propagation coefficient, γ ,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.1)$$

or

$$\gamma = \alpha + j\beta \quad (2.2)$$

Where, α = attenuation coefficient, in Nepers per metre.

β = phase change coefficient, in degrees, or radians, per metre.

ω = angular frequencies in radians per second

At sufficiently high radio frequencies, equations (2.1) and (2.2) yield

$$\beta = \omega\sqrt{LC} \quad (2.3)$$

β is called the “wave number”. From the relationship for the propagation velocity, we can write the signal velocity propagation as

$$v_p = w / \beta \text{ (m/sec)} \quad (2.4)$$

Using equation (2.3), we can obtain

$$v_p = 1 / \sqrt{LC} \text{ (m/sec)} \quad (2.5)$$

The velocity of propagation is also given in terms of the absolute permeability μ and permittivity ϵ of the medium through which the wave passes,

$$v_p = 1 / \sqrt{\mu\epsilon} = c / \sqrt{\mu_r\epsilon_r} \text{ (m/sec)} \quad (2.6)$$

Where, $c = 2.99793 \times 10^8$ m/sec, the velocity of light in free space.

μ_r = relative permeability of the medium through which the wave passes

ϵ_r = relative permittivity of the medium through which the wave passes

From equation (2.6), we note that the wave propagation speed is dependent on the dielectric medium.

2.3.2 Transmission Line Impedances

The characteristic impedance Z_0 is generally given by

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.7)$$

At high radio frequencies this simplifies to

$$Z_0 = \sqrt{\frac{L}{C}} \quad (2.8)$$

Changing Z_0 requires a change in the dimensions of the transmission line. The impedance looking into a transmission line varies with the distance progressed along the line. By setting down the distance limits into expressions for the voltage and current at any point along the line we obtain, for a specific impedance Z_L the following expression for the input impedance of the line is given by.

$$Z_{in} = Z_0 \frac{Z_L \cosh \gamma l + Z_0 \sinh \gamma l}{Z_0 \cosh \gamma l + Z_L \sinh \gamma l} \quad (2.9)$$

Equation (2.9) is a general expression for Z_{in} . For lossless lines equation (2.9) simplifies to

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \quad (2.10)$$

Using equation (2.10), the shorted-circuit (at the far end of the transmission line) case where $Z_L = 0$, gives

$$Z_{sc} = jZ_0 \tan \beta l \quad (2.11)$$

And for open-circuit (at the far end of the transmission line) case, where $Z_L = \infty$, gives

$$Z_{oc} = -jZ_0 \cot \beta l \quad (2.12)$$

When the line is terminated with a load impedance exactly equal to the characteristic impedance (Z_0) of the line itself, it is a perfectly broadband matched. The denominator is equal to the numerator in the right-hand parentheses of equation (2.9) and hence

$$Z_{in} = Z_0 \quad (2.13)$$

This completely matched condition is often used in test and measurement procedures.

2.3.3 Reflection and Voltage Standing Wave Ratio

In all cases, unless the line is in completely matched condition, the load termination reflects some of the energy originally injected into the transmission line. When a signal is reflected back to the launching point, interference between the incident and reflected waves, travelling at the same velocity but in opposite directions, causes a standing-wave field pattern to be formed. The voltage reflection coefficient, Γ , the ratio of reflected to incident voltage at the load is give by

$$\Gamma = \frac{Z_L - Z_0}{Z_0 + Z_L} \quad (2.14)$$

The ratio of maximum to minimum amplitude of the standing wave is called the Voltage Standing-Wave Ratio (or VSWR) given by

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (2.15)$$

For matched condition, $\Gamma = 0$ and $VSWR = 1$. The reflection coefficients and standing wave ratios for short-circuit and open-circuit terminated conditions are -1 and $+1$ respectively, and in both cases mentioned above, the VSWR is infinite.

2.3.4 Frequency-Dependent Charge Distribution

On-Chip interconnects are essentially planar structure as shown in Figure 2.1 below

Figure 2.1: Planar structures as on-chip interconnects

Such lines have an unusual frequency dependent behaviour. Figure 2.2 shows the charge distribution of the interconnect structure when there is a positive DC voltage applied on the top conductor. In this case, the positive charges on the top conductor generally arranged in a fairly uniform distribution. The bottom conductor, which is the ground

plane, have balanced negative charges, so that the electric field lines begin on the positive charges and terminate on the negative charges. The negative charges on the ground plane are uniformly distributed over the whole of the ground plane. In Figure 2.2(a), the charge distribution at DC indicates that both positive charges on the conductor and negative charges at the ground plane are uniformly distributed.

Figure 2.2: Cross-sectional view of the charge distribution on an interconnect at various frequency. (The dots and crosses indicate charge concentration of different polarity).

As the signal's frequency injected into the interconnect increases, the charges do not have sufficient time to rearrange and the charges do not spread out uniformly. Also, the electromagnetic fields, now being time varying, are not able to penetrate the conductor as much as the frequency increases and this phenomenon is known as the skin effect, which will be discussed later in this chapter. This is shown in Figure 2.2(b) at 100MHz. The effect is more prominent when the frequency of the signal is at 1GHz in Figure 2.2(c). The top conductor the charges are not uniformly distributed with respect to the depth of penetration into the conductor. Consequently, the current flow is mostly concentrated near the surface of the conductor and the effective cross-sectional area of the conductor, for current to flow, is reduced. Hence, the resistance of the conductor increases. At the ground plane, the charge distribution is not uniformly distributed over the whole of the ground plane. Instead, charges become more concentrated under the strip. This effect increases the resistance of the ground plane as again the effective cross-sectional area of the ground plane has reduced.

The redistribution of the current as discussed above results in a change of the inductance of the conductor line with frequency. This is principally because, for the same current, magnetic energy is stored inside as well as outside of the conductors at low frequencies. As frequency increases, the magnetic field becomes confined to the region outside the

conductors and the inductance remains approximately constant. The most significant frequency dependent effect is the resistance of the interconnect, which increases indefinitely approximately as the square root of frequency (refers to equation 2.18).

2.3.5 The Effects of Dielectric On Interconnect

As shown in Figures 2.1 and 2.2, on-chip interconnects are immersed in insulating materials such as SiO₂. The presence of a material between the conductors alters the electrical characteristics of the interconnect. With a dielectric, the application of an electric field moves the centres of positive and negative charge at the atomic and molecular level. Moving the charge centres changes the amount of energy stored in the electric field. The extra energy storage property is described by the relative permittivity, ϵ_r , which is the ratio of the permittivity of the material to that of free space, ϵ_0

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \quad (2.16)$$

The relative permittivity of the materials, used in on-chip interconnects, range from 3.8-4.2 for silicon dioxide (SiO₂) and 11.9 for silicon (Si). If the interconnect is immersed more than one medium, hence a non-homogeneous transmission line, the effective permittivity, ϵ_{eff} , is used. The ϵ_{eff} changes with frequency as the proportion of energy stored in the different regions changes. This effect is called dispersion and can cause a input pulse to spread out as the different frequency components of the pulse travel at different speeds.

A similar effect on energy storage in the magnetic field occurs for a few materials. The magnetic properties of materials are due to the magnetic dipole moments resulting from alignment of electron spins. In most materials the electron spins occur in pairs with opposite polarity with the each result cancelling one another, eventually, the net outcome is zero magnetic moment. However, when the net outcome is not equal to zero magnetic

moment, this remaining net magnetic moment will aligns with an magnetic field and provides a mechanism for additional storage of magnetic energy. The relative permeability, μ_r , describes this effect. Nearly all material used with interconnects have, $\mu_r=1$.

2.4 LOSS MECHANISMS IN ON-CHIP INTERCONNECT IN HIGH FREQUENCY ENVIRONMENT

As mentioned in section 2.2, the low resistive silicon substrate and the aluminium interconnect technology do not provide good high frequency properties for on-chip interconnects. In general, there are four main loss mechanisms, namely, metallization resistive loss, substrate capacitive, resistive and magnetic losses. These loss mechanisms will inevitably increase the difficulty in the prediction of the silicon-based on-chip interconnect in a high-frequency environment. [26].

2.4.1 Metallization Resistive Loss

At low frequencies, the current flow within a metal conductor trace is uniform and its series resistance (R_s) can be easily determined by,

$$R_s = \rho \frac{L}{W \times t} \quad (2.17)$$

where ρ is the resistivity ($\Omega\text{-cm}$) of the metal used, L refers to the length, W refers to the width of the metal conductor and t refers to the thickness of the conductor. However, at high frequencies, the induced electromotive force (EMF) causes a non-uniform current distribution in the metal conductor. This non-uniform current flows along the conductor surface, effectively reduces the cross-sectional area of the conductor. As a result, there is an increase in the series resistance, which causes a further reduction in the signal power

moving through the on-chip interconnect. This phenomenon is known as the skin effect and it is directly proportional to the square-root of the operating frequency. The skin effect can be visualised from a straight conductor with a circular cross section. Figure 2.3 shows that at high frequencies, the current can only flows in the thin conducting cylinder of a thickness equal to the skin depth δ .

Figure 2.3: Skin effect in a on-chip interconnect.

Skin depth δ is defined [27] as,

$$\begin{aligned}\delta &= \sqrt{\frac{2}{\omega\mu\sigma}} \\ &= \frac{1}{\sqrt{\pi f\mu\sigma}}\end{aligned}\tag{2.18}$$

where f refers to the frequency, σ is the conductivity and μ is the permeability of the metal conductor. Since skin depth, δ , is inversely proportional to the frequency, f , at higher frequencies, δ decreases and this suggests that there is lesser low resistive path within the conductor for current to flow easily. Hence, the resistance of the conductor increases with the operating frequency.

Equation (2.17) can be further deduced to define the skin resistance, R_{skin} (Ω/m^2),

$$\begin{aligned}R_{\text{skin}} &= \frac{1}{\sigma\delta} \\ &= \sqrt{\frac{\pi f\mu}{\sigma}}\end{aligned}\tag{2.19}$$

Therefore, increasing the metal thickness of on-chip interconnect can minimize the conduction losses. This is especially so for CMOS technology because the metal thickness is typically between 0.25 μm to 0.7 μm . Many experimental results have shown that the skin resistance improves significantly when the metal thickness increases from 0.25 μm to 1.0 μm . This is due to a massive reduction in the series resistance of the on-chip interconnect at low frequencies.

2.4.2 Substrate Capacitive and Resistive Losses

The conventional silicon-based on-chip interconnects are fabricated using metal layers and it sits on top of the inter-metal dielectric layers (which are made up of silicon oxide) and the silicon substrate. The layers of silicon oxide and the substrate itself contribute to unwanted capacitive coupling, which define the unwanted self-resonant frequency of the on-chip interconnect. The self-resonant frequency, f_{SR} , as defined for a passive device [28-30] is the parallel resonance achieved between the device's inductance and its parasitic capacitances and resistances. Here, the parasitic capacitances refer to the oxide capacitance between the on-chip interconnect and silicon substrate and capacitance of the silicon substrate itself. The parasitic resistance, on the other hand, refers to the resistance of the silicon substrate. Ideally, the substrate and the oxide layer should not be capacitive and should have infinite resistivity so as to minimise unwanted substrate coupling.

The presence of these parasitic components promotes undesirable energy dissipation and losses into the silicon substrate, which will also degrade the on-chip interconnect's behaviour in a high-frequency environment. For long on-chip interconnect structures, the distributed structure, together with the complexity of all these parasitic components make it difficult to estimate the overall behaviour of the interconnect. It usually requires tedious and time-consuming electromagnetic field simulations to make accurate predictions. Therefore, to understand the effects of these parasitics and their impact on the overall device performance, an accurate and scalable on-chip interconnect model has to be developed. Accurate physical on-chip interconnect model that takes into considerations the substrate effects will definitely enable circuit designers to predict and tuned their designs inconsideration of the on-chip interconnect effects.

2.4.3 Magnetic Loss

Magnetic loss occurs in two phases. When a current-natured signal move through the on-chip interconnect, a self-induced emf (electromagnetic fields) is generated due to the change in the current flowing through the on-chip interconnect. This is the self-inductance of the on-chip interconnect.

And according to Faraday's law, an image current will be induced in the substrate underneath the conductor by this magnetic field generated in the first phase. Since the silicon substrate has low resistivity, this image current can flow easily. In compliance with Lenz's law, the direction of flow for this induced current is opposite to that of the conductor. This generates an opposing magnetic field in the substrate, which interacts with the magnetic field of the conductor, hence, changing the self-induced inductance of the on-chip interconnect. Figure 2.4 shows the top and cross-sectional views of an conductor fabricated on a silicon substrate. It also illustrates the formation of image current in the substrate and its magnetic flux interaction with that of the conductor.

Figure 2.4: Formation of image current and its magnetic flux interaction with that of the conductor.

CHAPTER 3

ON-CHIP INTERCONNECT MEASUREMENT AND PARAMETERS EXTRACTION

3.1 RF MEASUREMENT AND CALIBRATION TECHNIQUES FOR ON-CHIP INTERCONNECT

In order for an interconnect model to describe the device characteristics accurately, all important model parameters should be extracted from the measured data. To extract the RF model parameters, on-chip high frequency measurements are performed using specifically designed test structures. Also, a de-embedding methodology has to be developed to remove the influence of the parasitic in the test structure from the measured raw data in order to obtain the data for the characteristics of the DUT (device-under-test). Figure 3.1 below illustrates the set-up for the high frequency measurement system for on-chip interconnect measurements.

Figure 3.1: RF equipment setup for interconnect measurement

When engaged in a RF measurement, the RF test system and DUT together form a complete circuit. As the frequency increases, discriminating between the two becomes a delicate issue. The simplest method of separation is to sketch a line and divide the test system and the DUT. Subsequent measurements of the DUT are then referred to this dividing line. The DUT being measured is inside the line, while the test system is outside. This is the concept of reference plane. Normally, the reference plane for a RF

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measurement is “drawn” at the probe tip. Reference plane can be achieved by using the calibration.

Calibration de-embeds imperfections in the test system equipment by measuring known quantities called standards. The RF characteristics of the standards are found beforehand. By measuring the standards mounted in place of the DUT, the test system equipment’s imperfections can be isolated, quantified and mathematically removed. The goal of any calibration is to provide the DUT with an electrically pure connection to the test system’s terminal. Thus the signal at the test ports should have zero magnitude, no phase shift and the characteristic impedance Z_0 . Figures 3.2 below shows the standards that are used for calibration. The standards are SHORT, OPEN, LOAD and THROUGH.

Figure 3.2: SHORT, OPEN, LOAD and THRU standards

3.2 DE-EMBEDDING INTERCONNECT TEST STRUCTURES FOR INTRINSIC DEVICE MEASUREMENT

De-embedding is the process of removing unwanted contributions, which can be quantified as extrinsic elements, from the S-parameter data. These contributions may be due to interface discontinuities, launches, and any other features that is not part of the intrinsic element but is added to the layout for aids in providing accurate measurement. Most importantly, in order to de-embed all unwanted contributions, the contributions must already be characterized either by, measurement, using mathematical formulas or rigorous full-wave analysis. In other words, the contributions must be known or assumed before it can be removed.

The two-port parameter analysis facilitates the removal of these contributions since the contributions can be represented as an equivalent circuit, which consists of resistors, inductors, and/or capacitors. An equivalent circuit can be ascertained by inspecting the device's physical construction, interface, and test set up.

Using the fundamental of the so-called two-step de-embedding procedure [31-33] that is commonly used for RF transistor modeling, a one-step de-embedding procedure is used for de-embedding the interconnect test structures. Figures 3.3(a) and 3.3(b) show the interconnect test structures and its de-embedding structure, which is also known as open structure. The open structure is basically the test structure minus the DUT (Device Under Test), hence all the pads are open without any connections between them.

Each interconnect requires three pads for measurement, noticed that the pads are shared between adjacent interconnect test structures. This technique of pad sharing helps in reducing the size of the total die size. Typically, an interconnect test structure can be represented by an equivalent network block as shown in Figure 3.4.

(a) With GSG Probe

(b) With OPEN Structure

Figure 3.3: The straight interconnect test structure layout

Figure 3.4: Equivalent network block used for one-step de-embedding the interconnect test structure.

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Y_{p1} , Y_{p2} and Y_{p3} represent the influence of the parallel parasitic contributed by the open structure. These parallel parasitics can be obtained by performing S-parameter measurement and then S-to-Y parameters transform, to derive at,

$$Y_{p1} = Y_{11(\text{open})} + Y_{12(\text{open})} \quad (3.1)$$

$$Y_{p2} = Y_{22(\text{open})} + Y_{21(\text{open})} \quad (3.2)$$

$$Y_{p3} = -Y_{12(\text{open})} = -Y_{21(\text{open})} \quad (3.3)$$

Y_{p1} and Y_{p2} represent the parasitic capacitance contributes by the measurement pads. Y_{p3} represents the parasitic coupling between the two measurement ports. Since in the open-structure, Z_{p3} is inherently large, Y_{p3} being its reciprocal, contributes insignificantly in the open-structure. The majority of the parasitic contributions in the open-structure come from the measurement pads, which are represented by Y_{p1} and Y_{p2} . Eventually, the measured data corresponding to the interconnect can be obtained according to the following equation,

$$\mathbf{Y}_{\text{interconnect}} = \mathbf{Y}_{\text{test-structure}} - \mathbf{Y}_{\text{open}} \quad (3.4)$$

Hence, according to the discussion above, the procedures for de-embedding the interconnect test structure can be given as follows:

1. Measure the S-parameters (S_{DUT} and S_{open}) for DUT and open test structure and convert them to Y-parameters ($\mathbf{Y}_{\text{DUT}}$ and $\mathbf{Y}_{\text{open}}$).
2. Perform the de-embedding by removing the parallel parasitics from $\mathbf{Y}_{\text{DUT}}$,

$$\mathbf{Y}_{\text{interconnect}} = \mathbf{Y}_{\text{DUT}} - \mathbf{Y}_{\text{open}} \quad (3.5)$$

Figures 3.5 to 3.8 show the data of the measured S11 and S12 of a interconnect test structure before and after performing the de-embedding procedure. Significant difference between the data can be observed.

Figure 3.5: S11 Magnitude Plot

Figure 3.6: S11 Phase Plot

Figure 3.7: S12 Magnitude Plot

Figure 3.8: S12 Phase Plot

3.3 HIGH FREQUENCY MEASUREMENT OF INTERCONNECT TEST STRUCTURES

A total of 50 test structures, set of 25 for top metal (top metal) and another set of 25 for metal 5, are sent for fabrication. These test structures are fabricated using an industry compatible 0.18 μm CMOS process technology with additional plug-in analogue modules such as deep-Nwell, MIM capacitor and thicker top metal back-end-of-line process flow. Each group has all the combination of physical dimension (length and width) as listed in Table 3.1

Table 3.1: Straight interconnect test structures dimension.

Length	800 μm	400 μm	200 μm	100 μm	50 μm
Width	1.5 μm	3 μm	5 μm	10 μm	20 μm

The criteria for selecting the minimum width for the test structure is derived from the foundry design rule. The design rule states that the minimum top-metal width is 1.5 μm and selecting 20 μm as the largest width is because for a typical RF circuit design, the inductor, which is largest passive device in a circuit, has a width less than 20 μm .

The criteria for selecting the minimum length for the test structure is due to the minimum distance that the RF measurement probe can be placed together during measurement and the criteria for selecting the maximum length for the interconnect test structure is because for a typical RF circuit sub-block, eg. LNA, VCO or mixer, the total sub-block die size is about 800 μm by 800 μm .

RF circuit designer has been taking the advantage of using thick top-metal for routing critical high frequency path because of the lower sheet resistive which will result in lower resistive loss. Furthermore, by routing high frequency line as far away from the die substrate, high frequency signal loss, due to the substrate distributed-effects will be reduced. Hence, top-metal and metal 5 are used as the test structure for this study.

3.3.1 Measurement Analysis

On-wafer RF device measurements are carried out using a 50GHz Vector Network Analyser and GSG RF probes. The wafer and RF probes are shielded within the chamber of a semi-automated probe station throughout the measurements. Substrate taps near the top metal lines are included in all ground pads of the 6-pad GSG configuration, refers to Figure 3.3, to ensure that the substrate is indeed effectively grounded. Figures 3.9 and 3.10 show the measurements and analysis of the various fabricated interconnect test structures.

Figure 3.9: S11 plot (Length = 800 μ m, Width = 1.5 μ m, 3 μ m, 5 μ m, 10 μ m, 20 μ m)

Interconnect test structures have identical input and output port. More specifically, the measurement data for the S11 and S22 for identical port is symmetrical as shown in Figure 3.11. S11/S22 measured the input/output matching or reflection looking into the input/output of the interconnect test structures. From the measurements, the input/output reflection loss is inversely proportion to the width of the test structure.

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The RF test system uses a 50 ohm matched for its input and output port, since the resistance of the interconnect at DC or low frequency is derived as:

$$\text{Resistance} = \rho \times (\text{Length}/\text{Area}) \quad (3.6)$$

Where ρ : sheet resistivity of the metal ($\Omega\text{-cm}$)

As the width of the interconnect decreases, the total resistance looking from the input port to the output will increase. This increase causes the 50ohm input and output port to deviated from the ideal matched condition and signal reflection increases.

From Figure 3.9, as the frequency increases, the reflection loss increases almost linearly before it is saturated at above 30GHz. The increase is caused by the resistive elements looking into interconnect. This resistive element is frequency dependent, as discussed in chapter 2, will be extracted from the measurement data in the next section.

Figure 3.10: S12 plot (Length = 800 μm , Width = 1.5 μm , 3 μm , 5 μm , 10 μm , 20 μm)

S_{12}/S_{21} measured the forward loss of the interconnect test structure. Since interconnect is a passive element and have identical ports, hence reciprocal. Measurement data for the S_{12} and S_{21} will be identical as shown in Figure 3.12.

From the measurement results in Figure 3.10, forward loss is inversely proportional to the width of the test structure. This is due to the resistive elements of interconnect as explained for Figure 3.9. Similar measurement trend can be observed for Figures 3.9 and 3.10. The measurement results reacted almost linearly to increase in measurement frequency before saturation at above 30GHz. To understand the behaviours in Figures 3.9 and 3.10, frequency dependence elements of interconnect are extracted in subsequence for in-depth study.

Figure 3.11: S_{11} and S_{22} plot (Length = 800 μm , 400 μm , 200 μm , 100 μm and 50 μm , Width = 20 μm)

3.3.2 Frequency Dependence Parameters Extraction

One of the primary concerns for this study is to extract the frequency dependence elements of on-chip interconnects. This section will discuss the strategy that is deployed to extract frequency dependence elements such as the series resistance, the series inductance, the oxide capacitance and the substrate capacitance.

After the raw S-parameters have been de-embedded as discussed earlier in the earlier section, the interconnect can be represented using a Π network as shown in Figure 3.13.

Figure 3.13: Π network

The Π network shown in Figure 3.13 is derived using the S-to-Y parameter transform. Y_3 represents the series elements and Y_1/Y_2 represents the parallel elements. By taking the reciprocal of Y_3 such that,

$$Z_3 = 1/Y_3 \quad (3.7)$$

we can derived the series resistance, R_s which is the real part of $\text{real}(Z_3)$.

$$R_s = -\frac{1}{\text{Real}[Y_{12}]} \quad (3.8)$$

Recalling the measurement results in Figures 3.9 and 3.10, the series resistance is the major contributor to the S_{11} , reflection loss, and the S_{12} , forward loss. Collectively, both losses are known as the conductor loss [13][34].

Figure 3.14: Series resistance plot (Length = 800 μ m, Width = 1.5 μ m, 3 μ m, 5 μ m, 10 μ m, 20 μ m)

Figure 3.15: Series resistance plot (Length = 100 μ m, Width = 1.5 μ m, 3 μ m, 5 μ m, 10 μ m, 20 μ m)

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Figures 3.14 and 3.15 above show the series resistance plots for interconnect test structures of length $800\mu\text{m}$ and $100\mu\text{m}$ respectively. Two observations can be made from the plots. In Figure 3.14, with measurement frequency going beyond 20GHz , the series resistance decline with the frequency. The decline eventually causes the series resistance to obtain a negative value. The declining trend suggests that the measurement results are suffering from distributed effect. Distributed effect occurs when a sinusoidal signal passing through an interconnect line, that is long enough to cause the amplitude of the signal to have significant changes between intermediate points on an interconnect line. The distributed effect is not seen in Figure 3.15, as the series resistance plots do not have a declining trend with increasing measurement frequency. This is because the test structures are shorter in length as compared to the one in Figure 3.14.

In addition to the distributed effect, skin effect can also be observed in Figures 3.14 and 3.15. The series resistance increases as measurement frequency increases as discussed in chapter 2.

Figure 3.16: Series self-inductance plot (Length = $800\mu\text{m}$, Width = $1.5\mu\text{m}$, $3\mu\text{m}$, $5\mu\text{m}$, $10\mu\text{m}$, $20\mu\text{m}$)

Figure 3.16 shows the extracted series self-inductance of the interconnect test structure of length 800 μm .

Refer to Figure 3.13, the series self-inductance is extracted by taking the inverse of Y_{11} ,

$$Y_{11} = Y_1 + Y_3 \quad (3.9)$$

$$\text{Series self-inductance, } L_s = \frac{\text{Imag}\left[\frac{1}{Y_{11}}\right]}{2 \times \pi \times \text{Frequency}} \quad (3.10)$$

Since the Π network is reciprocal, the overall inductance of the interconnect line looking into either port, can be fully described by taking the imaginary part of the inverse of Y_{11} . As shown in Equation (3.9), by extracting the overall inductance using Y_{11} which include Y_1 , that represents the capacitive elements looking from the interconnect line down to the underlining substrate, will provide a more accurate model.

From Figure 3.16, interconnect line with narrower width are subjected to more series self-inductance. With narrower width, the cross-sectional surface area of interconnect will be reduced. Current flowing through interconnect will induce magnetic field that will be more concentrated, hence the increase in inductance for narrower interconnect.

As the measurement frequency increases, the series self-inductance increases gradually. This is because with skin effect, the effective cross-sectional area for current flows through interconnect is reduced and magnetic field created is more confined hence series self-inductance will increase. Eventually, the series inductance will resonate due to the stray capacitance from the metal oxide and substrate.

3.3.3 Defining The Figure of Merit, Quality Factor for Interconnect

In the context of deep sub-micron passive devices modelling, such as spiral inductor and metal-insulator-metal (MIM) capacitor, quality factor or Q-factor, a dimensionless figure, is defined as a figure of merit to compare the performance of the passive devices. For instance, in the study of on-chip spiral inductor, the Q-factor of the inductor is defined by

the ratio of the inductive reactance to the total resistive power dissipation for an equivalent circuit consisting of inductance, L_S , in series with a resistor, R_T (representing the power dissipation) [35]. For a two-port S-parameter measurement, Q-factor of the spiral inductor, Q_{IND} , is often estimated by taking the ratio of the imaginary and real components of the Y_{11} parameter.

$$Q_{IND} = -\frac{\text{Imag}[Y_{11}]}{\text{Real}[Y_{11}]} \quad (3.11)$$

Equation (3.11) suggests that at a fixed resistive loss, the Q_{IND} is proportional to the inductance. This suggestion cannot be sustained in the study for the on-chip interconnect because self-inductance occurrence in the on-chip interconnect is considered as parasitic. Hence, the inductance should not be proportional to the Q-factor. A more suitable figure of merit, Q_{INT} , for interconnect is then introduced below,

$$Q_{INT} = \frac{1}{\text{Imag}\left[\frac{1}{Y_{11}}\right] \times \text{Real}\left[\frac{1}{Y_{11}}\right]} \quad (3.12)$$

From equation (3.12), the Q_{INT} for the interconnect is inversely proportional to the real and imaginary part of the impedance looking into the interconnect. This suggests that to obtain a high figure of merit for the interconnect, the device should possess a low parasitic resistance as well as inductance.

Figures 3.17 and 3.18 show the Q_{INT} plots for the on-chip interconnect test structures with length of 800 μm and 400 μm at various widths. The Q_{INT} plots are extracted using the equation (3.12). Similar trend can be observed in both plots. As the width of the on-chip interconnects test structure decreases, its corresponding Q_{INT} decreases as well. This can be verified using Figure 3.14, Figure 3.16 and equation (3.12). In both Figures 3.14 and 3.16, as the width of the test structure decreases, its parasitic inductance and series resistance increases. Hence, when apply to equation (3.12), the Q_{INT} factor decreases as well. Comparing Figure 3.17 and Figure 3.18, the Q_{INT} factor for on-chip interconnects with length at 400 μm is higher. This is because the test structures with shorter length have a lower series resistance and induced lesser parasitic inductance.

Figure 3.17: Q_{INT} plot (Length = 800μm, Width = 1.5μm, 3μm, 5μm, 10μm, 20μm)

Figure 3.18: Q_{INT} plot (Length = 400μm, Width = 1.5μm, 3μm, 5μm, 10μm, 20μm)

CHAPTER 4

ON-CHIP INTERCONNECT PHYSICAL MODELING

4.1 On-Chip Interconnect Model

There have been many different approaches [2][15] to the dynamic problem of interconnect characteristics at high frequency. Many physical models [16-17] have been put forward to describe its frequency dependence behaviour.

Figure 4.1: Conventional distributed model for transmission line interconnect

Figure 4.1 shows the conventional transmission line model, which can be implemented using the ABCD transmission parameters. The element R , L , G and C are the distributed resistance, inductance, conductance and capacitance respectively. The model is mainly used for very long transmission line when distributed effect of the transmission line is inherently large [17]. The model, however, cannot cater to the requirements for CMOS on-chip interconnects. This is because on-chip interconnect are comparably shorter than transmission line and the measurement data collect for the CMOS on-chip interconnect test structure, which are using two symmetrical ports, are not suitable to implement into the model above.

Figure 4.2 shows the lumped model also known as the single π model use for on-chip interconnect on lossy silicon based design. This lumped model is popularly used in CMOS design because the single π model includes the substrate loss effect with the R_{SUB} and C_{SUB} . The R_{SUB} and C_{SUB} element together with the C_{OX} element, which model the oxide capacitance, form the substrate branch looking down from the interconnect.

Figure 4.2: Lumped model (single π model)

As discussed in chapter 2, using the rule of thumb, if the interconnect line is less than $1/20^{\text{th}}$ of the wavelength, λ , of the signal, it is regarded as safe to use a lumped circuit model for the interconnect. Using the physical length for interconnect compute in Table 2.3 as a reference, the physical length of the interconnect in silicon will definitely be reduced because the wavelength, λ , calculation not in free air has to consider the relative permittivity, ϵ_r , and permeability, μ_r , of the material the signal propagate in. However, most material do not possess any ferromagnetic properties, thus $\mu_r=1$. Hence, the critical physical length calculation for the on-chip interconnect in silicon base process is,

Critical length $< \lambda_g / 20$, (λ_g is the wavelength in material g)

Where, $\lambda_g = \frac{c}{\left[\sqrt{\epsilon_r} \times \sqrt{\mu_r} \times \text{frequency} \right]}$, c = speed of light (in free air $\cong 3\text{e}+08$ m/sec)

$$\text{Critical length} < \frac{c}{\left[\sqrt{\epsilon_r} \times \sqrt{\mu_r} \times \text{frequency} \times 20 \right]} \quad (4.1)$$

Using equation (4.1) to calculate the critical length and compare the interconnect test structures that are measured, it is inherently that the interconnect test structures will exhibit distributed effects. As CMOS RFIC designs are moving above 10GHz range [36], and with the current wireless LAN 802.11a operating at the 5GHz to 6GHz UNII (Unlicensed National Information Infrastructure) band, the lumped model for

interconnect shown in Figure 4.2 is insufficient to cater for RFIC designers to run crucial harmonic simulations such as the IP3 and harmonic interference for RFIC designs due to the distributed effect. Hence, between lumped model and distributed model, there is an ambiguous “region” in which a lumped model is sufficient for simulation of RFIC in fundamental frequency but not sufficient to perform harmonics simulations.

Furthermore, it is obvious that the lumped model shown in Figures 4.1 and 4.2 are not able to describe the skin effects in interconnect at high frequency as the series resistance is a standalone component.

As discussed above, the physical models in Figure 4.1 and Figure 4.2 are not sufficient to model effectively the characteristic of on-chip interconnect in high frequency environment. A double π model is hence introduced to overcome the shortcomings of the single π model. Figure 4.3 shows the proposed scalable double π distributed RF sub-circuit model for RF interconnects.

Figure 4.3: Scalable double π distributed RF model for interconnect on lossy silicon

L_S and R_S describe the parasitic self-inductance and resistive loss on the metallization respectively. L_{SK} and R_{SK} model the skin effects of the metallization at radio frequencies. Substrate loss for interconnect is modeled by the RC network that consists of C_{OX} , C_{SUB} and R_{SUB} . These 3 elements describe the oxide capacitance between the silicon substrate and metallization, the capacitive and resistive losses in the silicon substrate respectively. Although the proposed double π model is rather complicated with numerous RLC elements, this model is symmetrical and values for the model parameters are identical for

the two π networks. This simplifies the extraction procedure and yet provides the necessary accuracy to model the higher radio frequencies effects of interconnects. By strategically cascading two lump models together, the distributed effect of interconnect can be introduced into a lump model. This makes the double π model a lump-distributed hybrid model.

4.2 ACCURACY AND CONTINUITY OF THE INTERCONNECT MODEL

The sub-circuit elements in the scalable RF Interconnect model are extracted using a popular device characterization and modeling software. This scalable RF model is developed using 25 interconnect test structures with 5 different sets of widths and lengths on the top-metal (metal 6) using an industrial compatible 0.18 μm RF CMOS process. To demonstrates how well this model can predict the high frequency effects the on-chip interconnects will behave, the measured S-parameters for an interconnect with length and width of 800 μm and 20 μm respectively are shown in Figure 4.4. In Figure 4.5, the measured verse extracted parasitic inductance and series resistance of the same dimension of interconnect are also presented. The plots also include the errors between the measured and extracted value for the parasitic inductance and resistance. In both cases, the error falls below the 10% mark.

In Figure 4.6 the quality factors, Q_{IND} (for quality factor defined for on-chip spiral inductor) and Q_{INT} , (for quality factor defined for interconnect) over the measured frequency range for an interconnect with length and width of 800 μm and 20 μm respectively are shown. The plots conclude the need to define the Q_{INT} for interconnect study. In Figure 4.6(a), the Q_{IND} increases with frequency, this does not truly implies that the figure of merit of an interconnect is getting better over frequency. If fact, due to the increase of parasitic series self-inductance and series resistance, the figure of merit should deteriorate as frequency increases. Figure 4.6(b) shows this deterioration of the figure of merit of the interconnect over frequency.

Figure 4.4: Measured vs Simulated S-parameters (a-d) vs frequency for Interconnect with length and width of 800 μm and 20 μm respectively using the proposed Double π Distributed RF sub-circuit model.

Figure 4.5: Measured vs Simulated Parasitic Inductance (a), Series Resistance extracted from Y_{12} (b), vs frequency for Interconnect with length and width of 800μm and 20μm respectively using the proposed Double π Distributed RF sub-circuit model.

Figure 4.6: Measured vs Simulated Quality Factor, Q_{IND} (a) and Quality Factor, Q_{INT} (b) vs frequency for Interconnect with length and width of 800μm and 20μm respectively using the proposed Double π Distributed RF sub-circuit model.

A single π lumped element RF sub-circuit model shown in Figure 4.7 can also be used to model interconnects operating at radio frequencies. However, there is a limitation to this approach at the higher RF regime (> 6 GHz) and this model-inadequacy is even more evident for long interconnect lines whereby the single π model is not able to predict the reduction of the extracted series resistance, R_S , revealed in Figure 4.5(b). When single π lumped element model is adopted for the same interconnect in Figure 4.6, the error between the measured and simulated values for R_S , Q_{IND} and Q_{INT} worsen from about $\pm 8\%$ to more than $\pm 25\%$ as shown in Figure 4.8.

Hence, double π distributed model is not only more superior in predicting high frequency effects as compared to the single π lumped element model, it is also scalable and continuous across various physical dimensions of the metallization interconnects. Many circuit simulators in the market are descendant of the legendary SPICE. In SPICE implementation, passive elements such as resistor, inductor and capacitor will not have frequency dependency capability built into them. Hence, to provide the frequency dependency effect on the resistor such as the skin effect, the R_{SK} and L_{SK} are placed in parallel with R_S . At DC or low frequency, the interconnect will have series resistance making up from R_{SK} in parallel with R_S . As frequency increases, the series resistance will be further increase by the introduction of L_{SK} .

Figure 4.7: Single π Lumped Element RF Sub-circuit Model for Interconnects.

Figure 4.8: Measured vs Simulated Parasitic Inductance (a), Series Resistance extracted from Y_{12} (b), Quality Factor, Q_{IND} (c) and Quality Factor, Q_{INT} (d) vs frequency for Interconnect with length and width of 800μm and 20μm respectively using a Single π Lumped Element RF sub-circuit model.

To examining the model accuracy as well as continuity in predicting all the test structures at popular application frequencies such as Bluetooth (at 2.45GHz) and wireless LAN (at 2.45GHz and 5GHz to 6GHz) applications, box plot in Figure 4.9 consolidates the deviation between the measured and simulated parasitic inductances for majority of the 25 interconnect test structures to be within $\pm 1\%$ at 2.45 and 5.05 GHz. It also shows that the proposed double π model has a quality factor, Q_{INT} accuracy of within $\pm 5\%$ at 2.45 and 5.05 GHz.

Figures 4.10 and 4.11 demonstrate that for both frequencies of 2.45 and 5.05 GHz, the scalable interconnect model can accurately predict the measured inductances and is continuous for all the RF interconnects with different metallization widths and lengths. Figures 4.12 and 4.13 examine the simulated versus measured interconnect quality factor, Q_{INT} , for all the interconnects at both 2.45 and 5.05 GHz, and they further assures that the scalable double π model is incessant and precise.

Figure 4.9: Percentage Deviation between Simulated and Measured Parasitic Inductance and Quality Factor, Q_{INT} at 2.45 and 5.05 GHz for all 25 Metal 6 Interconnect Test Structures.

Figure 4.10: Double π Distributed Interconnect Model Continuity – Simulated vs Measured Interconnect Inductance at 2.45 GHz.

Figure 4.11: Double π Distributed Interconnect Model Continuity – Simulated vs Measured Interconnect Inductance at 5.05 GHz.

Figure 4.12: Double π Distributed Interconnect Model Continuity – Simulated vs Measured Quality Factor, Q_{INT} at 2.45 GHz.

Figure 4.13: Double π Distributed Interconnect Model Continuity – Simulated vs Measured Quality Factor, Q_{INT} at 5.05 GHz.

CHAPTER 5**MODEL VERIFICATION USING GIGA-HERTZ
AMPLIFIER AND VOLTAGE-CONTROLLED
OSCILLATORS****5.1 Giga-Hertz Amplifier**

Conventional giga-hertz amplifiers and voltage-controlled oscillator circuits are designed and fabricated in the same 0.18 μ m RFCMOS technology to verify the accuracy of the double π distributed RF interconnect model. The amplifier design consisting of a RF NMOS thin gate transistor with input and output matching networks are expected to operate at 2.45 GHz with a gain of about 10 dB. With reference to the giga-hertz amplifier circuit schematic summarized in Figure 5.1, C_1 , C_2 , R_1 and L_1 are used to provide narrowband (2.45GHz) 50 ohm input matching at the gate of the transistor, M_1 . R_1 is employed to marginally reduce the quality factor of L_1 such that a large input matching bandwidth can be achieved. Output matching network to the external test system is made up of L_2 and C_3 . R_2 is used to isolate the DC biasing from high frequency signal path at the gate of the transistor. Last but not least, for the giga-hertz amplifier to operate, 0.9V and 1.8V DC are applied to V_G and V_{DD} terminals respectively.

To verify the validity and accuracy of the proposed RF interconnect model, 3 device-identical giga-hertz amplifier circuitry are fabricated using the same interconnect lengths but with different interconnect widths of 1.5, 10 and 20 μ m. Experimental control of maintaining the same interconnect length helps preserve minimal unfavourable effects on circuit performance, which are associated with signal coupling and device placement. Figure 5.2 shows the die photos of 3 device-identical amplifier circuits with different interconnect widths.

Figure 5.1: Schematic of a simple giga-hertz amplifier circuit to verify the accuracy of the RF interconnect model.

Figure 5.2: Die photos showing on-wafer circuit characterization of giga-hertz amplifiers with different interconnect widths of (a) $1.5 \mu\text{m}$, (b) $10 \mu\text{m}$ and (c) $20 \mu\text{m}$.

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On-wafer RF circuit performance characterization for the amplifiers are carried out using similar experimental setup described in chapter 3 section 3 taking into consideration the selection of source power on the network analyzer. The three different width giga-hertz amplifiers' measured two-port S-parameters consolidated in Figure 5.3 reveals that amplifier with the largest interconnect width of $20\mu\text{m}$ has the highest gain and width of $1.5\mu\text{m}$ results in the smallest gain. This is primarily due to the high resistive loss in the interconnect when the operating frequency increases. More importantly, this plot discloses the existence of discrepancies on the amplifier's operation between simulated and measured circuit performances when interconnects are not considered carefully during post-layout simulations. Such frequency dependant discrepancies can be observed at the S11 and S22 of the amplifier. The simulated results show the gig-hertz amplifier is operating at a higher frequency when compare to the measured results.

Figure 5.3. Magnitude of measured S-parameters versus frequency for the 3 amplifier circuits with interconnect widths of 1.5, 10 and $20\mu\text{m}$ respectively.

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Figure 5.4 illustrates a post-layout back-annotated schematic highlighting lengths of the interconnect metallization within the amplifier circuitry. With this information, the double π distributed RF interconnect model proposed in chapter 4 can be deployed to predict the overall circuit degradation contributed by the interconnects at high frequencies.

Figure 5.4: Schematic of the giga-hertz amplifier circuit showing the lengths of metallization interconnects in various parts of the circuit.

Figure 5.5 on the other hand, shows the amplifier schematic with a typical RC approach to investigate the effects of the interconnects. These 2 schematics have allowed additional simulations of the amplifiers to make meaningful comparisons between the 2 interconnect modeling approaches. Measured and simulated S-parameters of the amplifier with the interconnect widths of $1.5\ \mu\text{m}$ are evaluated in Figure 5.6.

Figure 5.5: Schematic of the giga-hertz amplifier circuit showing representation of metallization interconnects with simple RC elements.

Figure 5.6: Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 1.5μm using RF interconnect model.

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Simulated gain (11.3 dB) and peak gain frequency (2.95 GHz) of this amplifier without any interconnects are very much higher compared to the actual measured gain (8.92 dB) and peak gain frequency (2.88 GHz). With the RC interconnects, the simulated results only managed slight improvement in predicting the measured gain and the simulated peak gain frequency but it is still higher by 150 MHz. Nevertheless, when the double π RF interconnect model is used, the simulated results correlate well with the measured amplifier performance in terms of absolute gain and peak gain frequency with the input and output matching characteristics within acceptable limits. This superior agreement is possible because the parasitic inductance as well as high-frequency resistive loss associated with the interconnects are well emulated by the double π RF interconnect models.

Similar improvements between the measured and simulated S-parameters are noted for the amplifiers with 10 and 20 μ m widths in Figures 5.7 and 5.8 respectively. In these two plots, it is again noted that the RC interconnect approach is inadequate in predicting the measured gain and peak gain frequency of the amplifiers. Utilizing the RF interconnect models generate excellent agreement between the measured and simulated two-port characteristics for the 2 amplifiers. Figure 5.9 summarizes and compares the measured and simulated gain at the corresponding measured peak gain frequency for the 3 amplifiers using the RC and RF interconnect models. Employing interconnect widths of 1.5 μ m, the error between the measured and simulated gain without any interconnect model is +26.5%. This error is reduced to +10% when RC interconnect is used and further improvement to an error of just -2.9% is observed when RF interconnect model is utilized. Similar enhancements are also observed for the case of 10 and 20 μ m interconnect-width amplifiers with RF interconnect model.

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Figure 5.7: Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 10µm using RF interconnect model.

Figure 5.8: Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 20µm using RF interconnect model.

Figure 5.9: Measured and simulated gain at measured peak gain frequency versus interconnect widths for the 3 device-identical amplifier using RF interconnect models.

Test structures in the test element group for the double π RF interconnect model consist only of straight line interconnects. Giga-hertz amplifier circuit layouts, on the other hand, contain metal lines with 45° bends. One would expect some degree of inaccuracy in using the RF interconnect model to predict such bend interconnects. Nonetheless, on-wafer RF measurements of straight and bend top metal interconnects that are $300\mu\text{m}$ in length, with widths of 1.5 and $20\mu\text{m}$, as shown in Figure 5.10, unveils that only small deviations exist between these two types of structures. Plots in Figure 5.11 reveal good correlations between these 2 types interconnect structures with discrepancies in inductance and quality factor, Q_{INT} , to be within 2% and $\pm 5\%$ respectively for both interconnect widths of 1.5 and $20\mu\text{m}$. Therefore, employing RF interconnect model developed using straight metal line test structures is sufficient in predicting the characteristics of bend interconnects.

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Figure 5.10: Die photos showing on-wafer circuit characterization of straight [(a) & (b)] and 45° bend [(c) & (d)] interconnect structures with widths of 1.5μm [(a) & (c)] and 20μm [(b) & (d)], length fixed at 300μm.

Figure 5.11: Measured parasitic inductance and quality factor, Q_{INT} , for straight and 45° bend interconnect structures with widths of 1.5μm [(a) & (b)] and 20μm [(c) & (d)], length fixed at 300μm.

5.2 Voltage-Controlled Oscillator

Accuracy and reliability of the double π RF interconnect model is further scrutinized in a conventional giga-hertz voltage-controlled oscillator (VCO) design with its schematic illustrated in Figure 5.12. The VCO tank circuitry comprises of L_1 , L_2 , C_1 , C_2 , C_3 and C_4 to define the oscillation frequency of the differential signal pair at terminals $-V_{OSC}$ and $+V_{OSC}$. These two terminals are then each connected to an output buffer amplifier with low output impedance for higher load driving capability. The crossed-coupled nMOSFETs, M_1 and M_2 generate negative resistance to counteract the resistance from the LC tank thereby launching the VCO into oscillation. MOS Varactors, C_3 and C_4 , operating in the accumulation mode, are used to vary the oscillating frequency of the VCO. Reference and control voltages, applied on terminals V_{REF} and V_{CTRL} respectively, are utilized to change the capacitances of the MOS varactors. Lastly, isolation of the DC biasing from the RF oscillating signal is achieved using R_1 , R_2 and R_3 .

The die photo capturing the VCO with the RF and DC probes for on-wafer circuit measurement is shown in Figure 5.13. The post-layout back-annotated schematic illustrating the addition of interconnect metallization in the VCO and buffer amplifier designs are summarized in Figure 5.14. The double π interconnect model is used to perform a second VCO circuit simulation. With the RF interconnect model, the simulated oscillation frequency with respect to the control voltage associates very well with the on-wafer measured results. From Figure 5.15, it is observed that the percentage error between the simulated and measured oscillating frequency for the VCO has improved from more than 10% when interconnects are not considered to within 3% when RF interconnect models are utilized.

Figure 5.12: Schematic of a simple giga-hertz voltage-controlled oscillator to verify the accuracy of the RF interconnect model.

Figure 5.13: Die photo showing on-wafer circuit characterization of giga-hertz voltage-controlled oscillator with interconnect width of 10μm.

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS

Great advances in silicon processing technologies over the past ten years have generated a remarkable surge in research as well as immense commercial interests to use these established and cost-effective technologies for RF and microwave applications. Silicon technology is fast gaining popularity for RFIC's designs due to a larger possibility and ease of achieving system-on-chip integration with the RF front-end and digital/analogue baseband coexisting on a common platform. Enhanced device characteristics such as higher cutoff frequencies for transistors allow the traditional digital technologies to cope with stringent RF specifications set forth in popular communication standards such as Bluetooth and IEEE 802.11a/b/g etc. Nevertheless, low resistive bulk silicon which helps improve latch-up immunity at tighter design rules and high resistive loss associated with the back-end-of-line metallization are still major road blocks to achieving high circuit performance at giga-hertz frequencies.

Therefore, to exploit the advantages of silicon technologies for wireless applications targeted at the domestic markets, it is extremely important for circuit designers to understand the technology limitations and design trade-offs before employing this manufacturing technology for their RFIC's. Silicon-based RF designs are now conceptualized on EDA tools that utilize feature-rich process design kits (PDKs) with accurate and scalable device models developed based on extensive and reliable on-wafer RF device characterization. Despite having accurate device models that are capable of predicting radio frequencies device degradation effects, a typical RFIC's still require several design iterations before it can comply with the design specifications. These design iterations can be avoided if substrate and metallization losses at giga-hertz frequencies have been carefully considered when circuits are in the design-optimization and layout phase. Metallization interconnects which becomes part of the circuit when they are used to provide electrical connections between devices are often ignored during post-layout circuit simulations. These interconnects have detrimental effects on circuits,

and as frequency increases, undesirable parasitic responses, both inductive and resistive in nature as well as capacitive coupling to the substrate are even more pronounced, leading to significant deterioration in circuit performance and shifts in operating frequencies.

Most foundries do provide extensive information on the interconnect characteristics of their technology, but they are generally characterized at low frequencies. Such simple Resistance-Capacitance, RC, post layout extraction approach cannot satisfy the need to accurately emulate and predict first order effects such as substrate losses, inductive parasitics and skin effects of metallization at radio frequencies. Therefore, accurate and scalable RF interconnect models are necessary to help cope with the escalating demands of designing RFIC's with higher operating frequencies on cost-effective silicon technologies. Armed with these interconnect models, circuit designers will be able to take preventive measures prior to circuit fabrication if the RF interconnects are found to have adverse effects on their circuits during post-layout simulations, thereby reducing the number of design iterations, saving development cost as well as shortening the product time-to-market cycle.

In this thesis, a comprehensive literature review of the past and current works of the modelling of on-chip interconnect on silicon-based process was introduced. The various concerns of on-chip interconnects on silicon, especially in radio frequency environment were also covered. The basic definitions that relate to transmission line have been carefully presented. High frequency measurement for on-chip interconnect test structures was proposed. The de-embedding techniques used to extract the intrinsic elements of the on-chip interconnect was performed. After the S-parameter of each on-chip interconnect test structures was performed, the frequency dependence elements of the interconnect were extracted and studied.

Characterisation of on-chip interconnect on lossy silicon-based process was then carried out. The importance of developing an accurate, simple, physical and scalable interconnect model was clearly addressed. All the inductive, resistive and capacitive parasitics in an interconnect, required for predicting the interconnect frequency

dependence behaviour at radio frequencies were considered. With the measurement data, a new quality factor, a figure of merit, was defined for the on-chip interconnect. A new on-chip interconnect on lossy silicon model capable of providing precise predictions to the interconnect behaviour has been proposed. The new double π was demonstrated in this research work to be simpler and more accurate than the existing interconnect models.

The performances of the on-chip interconnect on lossy silicon, the double π model, was then evaluated using a giga-hertz amplifier and a voltage-controlled oscillator circuits. Three similar giga-hertz amplifiers with various interconnect widths are designed and measured. The measured results were then compared with the simulated results using the new double π model and the convention RC interconnect model. The new double π model was found to outshine conventional RC interconnect model since it was able to predict the frequency dependence behaviour of on-chip interconnect at high frequency operations. In addition, 45 degree bended interconnect structures were also measured and studied against the straight on-chip interconnects. It was concluded that the differences between the 45 degree bended and straight interconnect structures was too small and could be ignored. Similar model verification on the double π model was performed again using a voltage-controlled oscillator circuit. Once again, the double π model was able to obtain data that was close to those measured when compared to the convention RC interconnect model.

6.2 RECOMMENDATIONS FOR FUTURE RESEARCH

With the experiments and verifications performed on the on-chip interconnect in this project, there were a few critical observations on the layout of on-chip interconnect pertaining to high frequency design that we could summarise,

- i) Routing of critical high frequency path signal should be done on the highest metal available for the process technology, this is to isolate the signal as much as from the lossy silicon substrate.

- ii) The width of the on-chip interconnect that is used to route critical high frequency signal should be as wide as possible, for our studies 10 μ m to 20 μ m wide. This is because thin interconnect line are very resistive and inductive. They are also subjected to more frequency depending effects than wide interconnect line.
- iii) Bending of the interconnect should be avoided, if it is not possible, use 45 degree bend rather than 90 degree bend.

This project has presented and demonstrated several important studies on the frequency dependence elements of on-chip interconnects. Furthermore, a new lumped/distributed hybrid model, which is able to predict high frequency behaviours of on-chip interconnects, was demonstrated as well. There are still interesting and value-added research areas that we had encountered and are not able to look into for the studies of on-chip interconnect. They are:

- (i) To develop comprehensive design guidelines for allowing on-chip interconnects to operate with the highest quality factor at the desired frequency range.
- (ii) To characterise and model the coupling issues, for example the interconnect sides wall coupling and different level of metals coupling.
- (iii) To investigate the resistive noise introduced by the on-chip interconnects in circuits level.

AUTHOR'S PUBLICATIONS

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