Design of CMOS front-end receiver for wideband optical communication systems

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Design of CMOS Front-end Receiver for Wideband Optical Communication Systems

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A Thesis Submitted to the Nanyang Technological University in fulfillment of the
requirement for the degree of Doctor Philosophy of Engineering

January, 2011

Statement of Originality

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Chen Dandan

Acknowledgement

First and foremost, I gratefully extend my most sincere appreciation and deepest gratitude to my supervisor, Professor Yeo Kiat Seng, for giving me the opportunity to undertake this challenging and rewarding research project. His time, effort, support, constructive advice and valuable guidance as well as encouragement in the course of my Ph.D. candidature are deeply appreciated and will always be remembered.

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Abstract

In the current wireless indoor communication market, Bluetooth is the dominating technology used. The main purpose of Bluetooth is to eliminate the need of cables interconnecting electronic devices. Operates at a range of 10 meters with the top data rate of 24 Mbps [1,4], the use of Bluetooth in terms of high speed data communication is however, limited.

To achieve high data rate transmission, optical communication is the preferred method. In today's high speed optical fiber communication systems, such as 10Gb/s Ethernet and SONET OC-192 / STM64, transimpedance amplifiers are widely utilized due to its performance of wide bandwidth as well as low noise level. Transimpedance amplifier, which translates and amplifies incoming current generated by photodiode into a voltage signal, is an important part of receiver frontend.

In short distance applications like Local Area Network, unlike the stringent requirement of low transmission loss in long distance applications, cost effectiveness are of great importance due to the high deployment scale. As a result, integrated deep submicron CMOS solutions have been accepted as a suitable solution for short distance applications, due to its high manufacturability, low cost and acceptable performance. Thus, it is the interest of current research society to design transimpedance amplifier with better performance with low cost material and manufacturing technology.

Wireless optical communication is more feasible for short range communication system due to high path attenuation, as such the requirement for a

transimpedance amplifier with better performance as well as affordable material and manufacturing technology is desired.

In this thesis, an indoor wireless optical communication system using white LED light as the communication channel has been proposed. In the proposed system, signal is carried with light wave transmitted by white LED. The receiver terminal consists of a photodiode and a general CMOS optical receiver front-end. The specific design requirements and techniques for CMOS transimpedance amplifiers in a fully integrated CMOS optical receiver for the proposed system are then discussed. A novel cross-coupled current conveyor based transimpedance circuit topology has been proposed based on the requirement and techniques presented. This proposed cross-coupled current conveyor based input stages is capable to present a “zero” input impedance so that a high bandwidth can be achieved. Some well known bandwidth enhancement techniques have also been implemented in the proposed design. The proposed transimpedance amplifier has been implemented using GlobalFoundries’ 0.18 μm CMOS technology. The simulation as well as the measurement results have been presented, compared and analyzed in this thesis. The novel circuit also facilitates differential structure, while greatly reduce the cost and power consumption. The result indicates that the proposed TIA is indeed suitable to be employed in a low noise optical wireless communication system, however, further improvement of bandwidth, layout optimizations are necessary for a high speed system.

Design challenges for limiting amplifier have also been reviewed in this thesis, and a DC generating circuit is proposed to be incorporated in the limiting amplifier design as DC offset compensation network, making the limiting amplifier to be fully

integrated by eliminating the traditional off-chip component in the offset compensation network. The simulation result has been presented.

In summary, the thesis focuses on CMOS design of transimpedance and limiting amplifiers which are major components of an optical receiver front-end. Following review of design challenges, a new transimpedance amplifier and a fully integrated limiting amplifier have been proposed and studied.

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Chapter 1. Wireless Indoor Communication

System

Wireless communication is a very broad concept, and ever since Marconi successfully demonstrated the original form of wireless communication – telegram back in the year 1901, it has become an inseparable part of our daily life, and also a hot topic in the front line of the engineering research and development.

Wireless communication can be categorized by many criteria, such as the spectrum used, the communication throughput, etc. One way to categorization is using the distance among the participants, which are: Wireless Wide Area Network (WWAN), Wireless Metropolitan Area Network (WMAN), Wireless Local Area Network (WLAN) and Wireless Personal Area Network (WPAN).

In view of the different categories in wireless communication, each category has its own established standards. In WWAN, the dominated standards are mobile telecommunication network standard, such as the UMTS (WCDMA), CDMA2000 and TD-SDMA. In WMAN, the governing standard today is IEEE 802.16, and the most successful implementation of this standard is the WiMax protocol developed by Intel and Alvarion back in 2002. WiMax can achieve a data rate of 70Mbps in a range of 50Km [2]. In WLAN, the market dominating standard is the IEEE 802.11 variations, such as 802.11b, 802.11g and the latest 802.11n. 802.11n standard allows the devices to communicate with each other at a maximum rate of 150Mbps within the range of 70m [3]. And in WPAN, one of the widely used standards is IEEE802.15, which is based on the Bluetooth technology. The latest Bluetooth technology can achieve a data

rate of 24Mbps within a range of 10 meters [1,4]. In all these wireless communication categories, WPAN is also known as indoor wireless communication.

In the world of wired communication, optical signal has replaced electrical signal to be the preferred choice of data carrier in the long distance, high data rate applications. However, light is not suitable in terms of long distance wireless communication. The visible light has the wave length between 400 to 700 nm, and infrared has the wave length less than 0.1mm [5]. The small wave length determines that the poor diffraction capability of light, which makes it extremely susceptible to the physical blockings.

There are applications of wireless communication using laser beam as carrier for a line of sight (LOS) distance of up to a few kilometers, such as [6] and [7]. Real life example can also be found in Singapore. In order to provide a high speed network to Nanyang Technological University (NTU)'s One North campus, and to avoid laying underground fiber cables, NTU has utilized laser beam to connect its One North campus directly to the nearest research center – Fusionopolis. However, all these applications involve high power, high complexity hardware setups, which render them inappropriate to be used in a WPAN scenario. Also, the utilization of laser means the light beam and thus the data communication can only be transmitted in a straight line with no obstacles in between.

As a result, in the world of indoor wireless communication, the dominant technology is still based on data transmission using radio frequency, Bluetooth, to be specific. While Bluetooth getting its popularity, the maximum data rate of 24 Mbps (as found in Bluetooth v3.0 + HS [4]) still seems to fail lots of WPAN applications,

such as the wildly anticipated wireless USB protocol. The current specification of USB, the USB v2.0, can achieve a theoretical data rate of 480Mbps, and the upcoming USB v3.0, can achieve a theoretical data rate of 3.2Gb/s [8]. With the abandoning of Ultra Wide Band (UWB) as an implementation of Bluetooth protocol, it is rather difficult for Bluetooth to achieve such a high data transmission rate. In fact, Bluetooth itself is not even able to achieve the claimed 24Mbps rate, the implementation of Bluetooth v3.0 + HS is in such a way that the Bluetooth protocol is used only as negotiation mechanism and leave the data transmission part to be handled by IEEE802.11 protocol [9].

Table 1-1: Data Transmission Rate of Various Bluetooth Versions [10]

Bluetooth Version	Data Transmission Rate
1.1	312Kbps
1.2	1Mbps
2.0 + EDR	3Mbps
3.0 + HS	24Mbps

1.1 Indoor Optical Wireless Communication

As mentioned previously, optical communication has been the preferred choice for high data rate, long distance data transmission in the wired network. So naturally, optical communication has been considered for as an alternative method for indoor optical wireless communication.

As of today, the most commonly utilized form of optical communication for indoor wireless communication is Infrared communication. It is commonly found in

mobile phones and notebook computers, and before the booming of RF and Bluetooth technology, it was also widely used as the communication channel for computer wireless peripherals, such as keyboard and mouse. However, from the communication perspective, Infrared communication bares all the disadvantages of optical communication, while lacks of the most important advantage of it.

Infrared, with its wavelength measured around 0.7 to 300 μm , requires a direct line-of-sight between the two communication entities so that the communication can take place, any obstacles in between will block the channel [11]. The data can be transmitted in a range of around 5 meters, and yet, the highest data transmission rate achievable is only 14Mbps (with IrDA-VFIR, various data rate specifications of Infrared communication is given in Table 1-2) [12]. Such a low data transmission rate has made Infrared less popular for data transmission applications today, in fact, the most common application of Infrared indoor optical wireless communication today, and in the past 30 years, is the remote controller which is used by small home appliances, such as television and Hi-Fi system.

Table 1-2: Data Transmission Rate of Infrared Communication [13], [14]

Infrared Communication Mode	Data Transmission Rate
IrDA-SIR (Slow Speed)	Up to 115 Kbps
IrDA-MIR (Medium Speed)	Up to 1.15Mbps
IrDA-FIR (fast Speed)	Up to 4 Mbps
IrDA-VFIR (Very Fast Speed)	Up to 16 Mbps

As a result, it is highly demanding to have a new way of indoor optical wireless communication. It should be able to achieve a data rate which is high enough

to support the WPAN applications such as multimedia transmission; meanwhile it should be also flexible enough to be used in the household environment where the single direction communication which is found in laser and Infrared communication is not desirable.

This leads to the proposed indoor communication system which makes use of white Light Emitting Diode (LED) as the light source for indoor optical wireless communication.

1.2 White LED as light source for indoor optical wireless communication system

1.2.1 Motivation of using white LED

Due to significant energy savings possible with LED technology as well as the increased lifetimes over standard incandescent lighting, white LED is believed to be a promising illumination device for the next generation [21]. As such, it is anticipated that white LED will be widely deployed for indoor places such as home space and offices. Using white LED as the light source for indoor optical wireless communication present a few obvious advantages:

- 1) Very low cost. Since the electro-magnetic spectrum is not licensed in the optical band, spectrum licensing fee is avoided. And with white LED become so popular, the system hardware cost can be expected to be at the very minimum.

- 2) Higher data rate. The reported highest data transmission rate of white LED light is 500 Mbps [15], which is more than 30 times of the Infrared communication. There are also publications claims to achieve the simulated data rate of up to 1 Gb/s such as in [16].
- 3) Omni-directional. Unlike Infrared or laser beams, which are uni-directional, white LED is used to provide illuminations to the whole indoor area, say, a room. In that case, anywhere that is illuminated by the white LED within the room will be able to use the wireless communication through white LED light.

1.2.2 Proposed indoor wireless communication system

Figure 1-1 shows the proposed indoor wireless optical communication system, which is capable of providing illumination, and realizing data communication. This system comprises fixed stations such as personal computer, modulators, a multiple of white LEDs on the roof and mobile terminals within a confined region. In this system, optical wireless communication between the fixed stations and the mobile terminals is carried out through the white LEDs' illumination.

Figure 1-1: Proposed wireless indoor communication system with White LED

The modulator following the fixed station modulates the baseband digital data into the transmitted signal. The detailed configuration of the modulator is determined by the chosen modulation scheme. White LEDs provide illumination for the confined region and radiates visible light consisting transmitted signal to entire confined region. Finally, the transmitted signals are received by mobile terminals, and communication between fixed station and mobile terminals are completed.

There are two key steps to complete the communication: modulating the signal to be transmitted and receiving the signal. Most present-day optical wireless channels are termed as intensity modulated, direct detection channels [17]. There are two popular ways to control the optical intensity of white LED. First is to adjust forward current value since LED is basically a current driving device. Second is to employ Pulse Width Modulation (PWM). For white LED, the optical intensity is directly

related to the current but it is not a linear function of the current [18]. In addition, although the optical intensity can be controlled by changing forward current, the change in forward current will also change the color of the output light which is termed as shift of chromaticity coordinate [19]. A benefit of the PWM method is that it enables intensity control with minimum color shift of the output. A simple implementation method is described with reference to Figure 1-2(a) showing a circuit with an NMOS switch M_1 which opens and closes the circuit. That essentially turns LED on and off. The input modulated signal that controls on and off switching of the NMOS M_1 is demonstrated in Figure 1-2(b). By modulating the amount of time 'on', which is the shaded region, and 'off' within one cycle time T , the optical intensity of output visible light can be controlled. To increase the intensity, one must increase the time 'on'; to decrease the intensity, one must decrease the time 'off'. The percentage of 'on' time within one cycle time, which essentially determines the optical intensity of output visible light, is termed as duty cycle. During the cycle where largest duty cycle appears, the optical intensity of output visible light is the largest. Since human eye has a limit of 60 frames per second, by increasing the frequency of switching, the change then becomes human imperceptible.

Figure 1-2: (a) Controlling white LED option intensity using PWM method; (b) On / Off switching of NMOS controlled by input signal

The baseband and band-pass modulation schemes have also been investigated for low-power optical communication system. It is concluded that the power efficiency of baseband schemes such as On-Off Keying (OOK) and Pulse Position Modulation (PPM), are better than the power efficiency of band-pass schemes such as Phase Reversal Keying (PRK), Quadrature Phase Shift Keying (QPSK), Frequency-

Shift Keying (FSK) [20]. The further comparison between OOK and PPM shows that PPM has better power efficiency. By adjusting the number of slots per frame, the bandwidth of the modulated signal can be adjusted so as to match the available channel width, thereby to optimize the power efficiency independently from the data rate.

1.3 Contribution of My Research

As the possibilities and feasibilities of using white LED to serve both illumination and data transmitting purposes have been explored, a patent has been filed based on the concept of indoor wireless communication system utilizing white LED. While every aspect of the White LED indoor optical wireless communication needs further research, after carefully study the complete process, the focus of my project has been identified to be the following in order to tackle the practical implementation part.

- 1) CMOS design of transimpedance amplifier
- 2) Research in low cost limiting amplifier design

1.4 Objectives

The main objective of this report is to research and explore the design challenges and techniques in CMOS transimpedance and limiting amplifiers, and then to come out with innovative solution to overcome these challenges. The implementation of the innovative solution will be a transimpedance amplifier designed

in 0.18 μ m CMOS technology for high speed short-haul network. A fully integrated CMOS limiting amplifier is also targeted.

1.5 Report Organization

The thesis is organized into seven chapters.

Chapter 1 provides an introduction to background information such as wireless indoor communication standards, communication using white LED light as a medium. Apart from a general introduction, it also highlights the author's proposed system, which utilizes white LED light as illumination source as well as the medium for data communication. This chapter also outlines the major contribution of the author, and introduces the structure of the whole thesis.

Chapter 2 provides the fundamentals in receiver circuit design. After a brief literature review, this chapter introduces the general receiver model. In general, a receiver consists of photodiode, front-end circuit, and decision making circuit. Photodiode is briefly touched in this chapter, and then followed by the introduction of a few important parameters in receiver design, which are: Noise, Bit-error rate, Sensitivity, Dynamic Range, Phase Noise and Jitter. Each parameter is elaborated in detail with the help of diagram and equations.

Chapter 3 is dictated to the transimpedance amplifier specifications. As TIA is the first part of the receiver front-end circuit, it is the principal factor in determining the overall noise performance and sensitivity of the optical receiver. The following TIA design specifications are discussed in detail: transimpedance gain, input overload

current, input-referred noise current and sensitivity as well as bandwidth and group-delay variation. The mathematical equation for each specification is given.

Chapter 4 is dictated to the transimpedance amplifier basic topologies. Five different types of basic topologies are introduced, which are: open-loop TIA, shunt feedback TIA, voltage mode TIA, current mode TIA and differential TIA. For each basic topology, the typical circuit is depicted, and noise performance is discussed with the aid of formula. After the basic topologies, some bandwidth enhancement techniques are introduced. The last part of chapter 4 focuses on the noise analysis of TIA, which includes the noise analysis of shunt-feedback common source TIA, common gate TIA as well as the noise analysis of the RGC TIA input stage.

Chapter 5 discusses the proposed cross-coupled TIA structure. After a brief introduction of cross-coupled current conveyor, the proposed cross-coupled current conveyor based TIA input stage structure is elaborated through the circuit diagram and the detailed derivation of the transfer functions. After that, the proposed differential TIA incorporating the proposed input stage is introduced in detail. Various performance boosting techniques are employed for the proposed circuit, such as capacitive degeneration and shunt inductive peaking. This chapter also presents the noise analysis of the proposed differential TIA. The detailed derivation is given with the aid of the noise equivalent circuit. With all the discussion on the design, Chapter 5 then moves on to discuss the circuit layout and post-layout results, as well as the actual measurement results of the designed circuit. From the results presented, three merits of the proposed design are highlighted, which are: input capacitance insensitive, ease of obtaining differential output signals and low noise level.

Chapter 6 introduces the limiting amplifier basics and proposes an on-chip DC offset compensation network. Various design considerations are discussed, including gain cell, bandwidth and input offset voltage. Followed by an introduction of the typical limiting amplifier implementation with offset compensation network, each component of the proposed offset compensation scheme is elaborated in detail, basically the DC generating circuit and the gain cell. The simulation results of the proposed structure is then presented, the result is also been compared with three other recent works published by others.

Chapter 7 concludes the whole thesis and also provides some suggestions for further research and study related to the proposed circuit designs.

Chapter 2. Receiver Fundamentals

2.1 Literature Review

Ever since mid 90s of last century, the internet has grown tremendously. From the mere four hosts in the initial Advanced Research Project Agency Network (ARPANET) back to 1969, today, there are more than 350 million hosts in the internet [30]. The applications of internet have been expanded to provide live multimedia streaming, online real-time research collaboration, and etc. The increasing number of users and high data rate applications has stimulated the evolution in carrier technologies. Today, the dominating networking backbone technology, be it Internet or Intranet, is optical carrier transmitted in optical fiber media.

Figure 2-1 Growing trend of number of internet hosts [30]

Optical signal running in fiber media, comparing to conventional electrical signal running in copper media, has in general four major advantages.

1. Higher transmission data rate. Optical signal can carry data rate up to 100Gb/s as found in 100 gigabit Ethernet.
2. Longer distance. When operating in single mode with laser light source, optical fiber cable can support over 10 km or even longer before signal booster is required.
3. Resistance to noise. Due to the nature that in fiber channel, data is carried in optical signal, the effect from other EM wave resources and nearby cables is minimized.
4. Enhanced data security. In order to intercept an optical fiber communication channel, the only way is to physically tap the light out from the fiber, since there is no radiated EM field outside the fiber channel [33].

One of the most widely used optical communication protocol in Metropolitan Area Network (MAN) and Wide Area Network (WAN) is Synchronous Optical Networks (SONET) protocol. SONET OC-192 based communication system theoretically can provide a data rate of up to 10Gb/s. As of 2005, OC-192 connections are most common for use on backbones of large Internet Service Providers (ISPs) [34]. Due to the success of the standard, the International Standard Organization (ISO) has developed a variation to its 10Gigabit Ethernet standard 802.3AE (LAN-PHY), called WAN-PHY (10GBase-W), which has been designed to interoperate with SONET OC-192 standard [34, 35].

Figure 2-2 shows a simplified model of SONET OC-192 optical transceiver front-end. At the transmitter, a 4:1 or 16:1 multiplexer (MUX) combines four parallel 2.488Gb/s electrical signals or 16 parallel 622-Mbps electrical signals to generate a 10Gb/s serial data, re-timed by a clock synthesizer. The system data rate is 9953.28Mb/s (containing 9621.504 Mbps payload and 331.775Mbps overhead). This non-return-to-zero (NRZ) 10Gb/s electrical signal drives a laser diode to produce the optical output. A typical receiver starts with a photo-detector, i.e. PIN photodiode or avalanche photodiode (APD). The photo-detector will convert the optical power into current, which will subsequently be converted to voltage by the transimpedance amplifier (TIA). In order to function over a wide dynamic range, an automatic gain control amplifier maybe added. The signal will be further amplified by limiting amplifier and then extracted from the signal stream by clock-data-recovery circuit and de-multiplexed to parallel digital signals [23, 24].

Figure 2-2: Basic SONET transceiver architecture [23, 24]

In long-haul optical transport systems, the transmission losses over long distances and optical sensitivity are of greater importance than cost, thus the light wave traveling through the fiber is usually amplified by expensive Erbium-doped Fiber-optical Amplifier (EDFA) before reaching the receiver. The optical communication wavelength is about 1300nm or 1550nm and the low attenuation and high efficiency is achieved by using EDFA [25, 26]. This is especially true for high-speed optical front-end designs found in MAN and WAN applications. Apart from high cost, EDFA also cannot be integrated easily with other semiconductor devices [27]. However, the stringent performance requirements make the EDFA the best choice for such applications.

Unlike the long-haul applications which mainly concerns huge telecoms and ISPs who are rich in capital and more concerned with performance, short-haul applications are used by almost every organization nowadays to provide intranet services or campus wide LAN. The wide deployment of the short-haul optical communication equipment makes it impossible to use the costly EDFA, and instead, the cost effective CMOS technology is dominating the short-haul transceiver design. Apart from the cost effectiveness, using CMOS in short-haul optical system design also has other important advantages due to the nature of the short-haul network. Firstly, CMOS technology is much easier to be integrated with other digital circuit blocks as compared to EDFA. Secondly, the power consumption of CMOS circuits is much lower. Last but not least, it has a high technology compatibility compared to EDFA [28].

Despite the obvious advantages of using CMOS technology in the short-haul optical network design, today, only very few fully integrated monolithic CMOS optical receiver front-end circuits have been reported for short-haul networks in the speed of 10 Gb/s range (OC-192). This is due to the challenges in the design of high speed TIAs, which is mainly concerned with the tradeoff among input noise current, bandwidth, transimpedance gain as well as the power consumption [29].

Similarly, referring to the wireless indoor system introduced in Chapter 1, to setup a home communication system which can ease the control and communication of mobile devices, a high speed low cost receiver front-end is essential.

2.2 Receiver Model

At the receiver front-end, the photodiode first transforms the incoming light intensity to a proportional electrical current, which is then to be amplified and converted to voltage signal by the transimpedance amplifier (TIA). Subsequently the limiting amplifier (LA) is to produce a large enough signal level for the clock and recovery circuit (CDR) to operate properly [23, 36, and 40]. In this project, we are focusing on the receiver front-end TIA design.

The basic receiver model used here is shown in Figure 2-3, where the photodiode is modeled with a signal current source i_{PD} and a noise current source $i_{n,PD}$. The characteristics of these two current sources will be discussed in the photodiode session. The overall transfer function $H(f)$ relating the output voltage v_o at the LA to the input current i_{PD} can be decomposed into a product of two transfer functions: one for TIA and one for the limiting amplifier.

The noise characteristics of the overall amplifying stages consisting TIA and LA are modeled by a single noise current source $i_{n,Amp}$ at the input of TIA. The noise spectrum of this source is termed as the input-referred noise source of the combination of TIA and LA. In practice, according to Friss Equation [47], this $i_{n,Amp}$ is determined almost completely by the input-referred noise of the TIA, which is the first element of the amplifying stage, if the gain of TIA is large enough.

In addition, the amplifying stages may become strongly nonlinear for large input signals. Fortunately, the receiver's own noise as well as the signal levels at the sensitivity limit usually is so small that we don't need to worry about the nonlinearity.

Hence, for the subsequent noise and sensitivity calculations, a linear model for the amplifying stages is adopted [40].

Figure 2-3: Basic receiver model

2.3 Photodiodes

As the first element in an optical receiver, the photodiode has a significant impact on the sensitivity and speed of the receiver front end and also sets limitations for the design of following amplifying circuitry [32].

Photodiodes produce current in response to light, in a sense the reverse action of light-emitting diodes. Taking a simple PIN photodiode for example, a PIN photodiode consists of a p-n junction with a layer of intrinsic semiconductor interposed in between as shown in Figure 2-4 [23, 48-51]. With a reverse-bias voltage, the intrinsic region is almost completely depleted, providing a depletion region as wide as W , typically about $20\mu\text{m}$. Photons incident on the i-layer create electron-hole

pairs, which become separated by the electric field applied. As a result, a photocurrent is produced.

Figure 2-4: PIN photodiode

In an ideal photodiode, every photon entering the device generates an electron-hole pair. However, in reality some photons are absorbed by materials or reflected from the surface. The fraction of photons that create electron-hole pairs is defined as the quantum efficiency and designated by η . PIN diodes exhibit a quantum efficiency of approximately 0.8 [23]. Only this fraction of photons contributes to the photocurrent produced, thus electrical current I_{PD} produced for a given amount of optical power P_{opt} illuminating the photodiode is [23, 40]:

$$I_{PD} = \eta \cdot \frac{\lambda q}{hc} \cdot P_{opt} \quad (2-1)$$

The constant describing the light-current relationship is known as the responsivity of the photodiode and is denoted by the symbol $\mathfrak{R}$:

$$I_{PD} = \mathfrak{R} \cdot P_{opt} \quad (2-2)$$

with

$$\mathfrak{R} = \eta \frac{\lambda q}{hc} = \frac{\eta \lambda}{1.24} \quad (2-3)$$

where h is the Planck constant, q is the elementary charge each electron carries, c is speed of light and λ is the wave-length of incident light in μm . The responsivity of a typical InGaAs PIN photodiode is in the range of 0.6 to 0.9A/W [40]. However the responsivity for silicon photodiode which is compatible with the CMOS process is much lower. Recent research shows that the best responsivity of silicon photodiode for 10Gb/s application is around 0.3A/W [52-54].

Another important characteristic of photodiode is the junction capacitance, C_j . Figure 2-5 shows the equivalent small signal circuit for a bare photodiode [40]. For AC model, the current and light density relationship still holds. Hence the current source representing the electrical current produced by incident light has the value:

$$i_{PD}(t) = \mathfrak{R} \cdot P_{opt}(t) \quad (2-4)$$

Figure 2-5: Equivalent AC circuit for bare PIN photodiode

The main parasitic are the junction capacitance C_j and the combination of contact and spreading resistance R_{PD} . Since at the frequency of interest the impedance of PIN photodiode is mostly capacitive, the impedance can be modeled by a single capacitance by neglecting the resistance R_{PD} .

The bandwidth of photodiode is determined by the R-C time constant given by the parasitic R_{PD} and C_j , and also by the transient time, that is the time it takes the carriers to travel through the intrinsic region [40]. C_j also greatly impacts the design of the transimpedance amplifiers as it appears at the input node of TIA directly, adding a significant input loading to TIA. For photodiodes operating in gigahertz range, C_j falls in the range of 0.1 to 0.5pF [23].

As PIN diodes display a low noise, in this report, the noise component contributed by the photodiode is neglected and the subsequent amplifier becomes the major noise contributor in the receiver frontend.

2.4 Noise and Bit-error rate

Noise refers to any unwanted disturbance that masks, corrupts, reduces the information content of, or interferes with the desired signal. Here, distortion effects that arise within the receiver circuitry are not included in our definition of noise [36].

The source of noise present in a receiver circuit can be broadly classified into two parts. The first are intrinsic noise sources arising from fundamental physical effects in the optoelectronic and electronic devices used to construct the receiver, such as thermal noise found in resistors, electronic shot noise and thermal noise in transistors, and the quantum shot noise inherent in photo detection. These intrinsic noise sources are found in all optical receivers. The second are coupled noise sources arising from interactions between the receiver circuitry and surrounding environment. Coupled noise can be caused by power supplies, nearby transmission lines, fast switching logic circuitry, etc. Coupled noise that degrades receiver performance is

usually termed as interference or circuit cross-talk. In a well designed receiver with adequate shielding, coupled noise can be made to be negligible when compared to intrinsic noise [36].

As shown in Figure 2-3, two current sources, $i_{n,PD}$ and $i_{n,Amp}$, are used to model the overall noise of the receiver front-end. The output signal of the amplifying stages, v_o , is a superposition of the desired signal voltage v_s and the undesired noise voltage v_n which originates from the input-referred noise of amplifying stages $i_{n,Amp}$ and the photodiode noise current $i_{n,PD}$ [40]. That is:

$$v_o = v_s + v_n \quad (2-5)$$

The power spectrum of noise due to input-referred noise $i_{n,Amp}$ of amplifiers can be calculated with the transfer function of the amplifying stages, $H(f)$:

$$v_{n,Amp}^2(f) = |H(f)|^2 \cdot i_{n,Amp}^2(f) \quad (2-6)$$

Integrating the noise spectrum in (2-6) over the system bandwidth BW_D , the total noise power introduced by the amplifiers is obtained:

$$\overline{v_{n,Amp}^2} = \int_0^{BW_D} |H(f)|^2 \cdot i_{n,Amp}^2(f) df \quad (2-7)$$

Although the photodiode noise $i_{n,PD}$ is non-stationary, that is $i_{n,PD}$ not only varies with frequency, but also changes along time, we can still approximate its output noise power using the similar equations as above:

$$\overline{v_{n,PD}^2} = \int_0^{BW_D} |H(f)|^2 \cdot i_{n,PD}^2(f, t) df \quad (2-8)$$

The above two noise sources are assumed to be uncorrelated, and then the total root-mean-square (RMS) noise at the output of the limiting amplifier can be obtained by adding the noise powers and under the square root [40]:

$$v_n^{rms}(t) = \sqrt{v_{n,PD}^2(t) + v_{n,Amp}^2} = \sqrt{\int_0^{BW} |H(f)|^2 \cdot [i_{n,PD}^2(f,t) + i_{n,Amp}^2(f)] df} \quad (2-9)$$

After going through the amplifying stages, the data bits must ideally be sampled by the clock at their midpoints so as to provide maximum distance from the decision threshold. However, at the time when instantaneous noise voltage $v_n(t)$ becomes so large that it corrupts the desired signal $v_s(t)$, a decision error or bit error occurs at the decision circuit. Thus the noise $v_n(t)$ adds to the signal and degrades both the amplitude and the time resolution, closing the eye and increasing BER. As the non-return-to-zero (NRZ) binary sequence is employed in most high-speed applications, in this project, we assume $v_s(t)$ to be a NRZ signal with a peak-to-peak value v_s^{pp} and free of distortions.

As mentioned, the preset threshold voltage in the decision circuit usually locates at the midpoint between the zero and one levels, namely $v_s^{pp}/2$. Assuming equal probability for zeros and ones, bit error rate (BER) is defined to be the probability that a zero is misinterpreted as a one or that a one is misinterpreted as a zero. With the assumption the noise amplitude exhibits a Gaussian distribution with zero mean and the standard deviation v_n^{rms} as we calculated in (2-9), the probability of errors can be obtained using following equation [23, 40]:

$$\begin{aligned}
BER &= \int_0^\infty \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) dx = \frac{1}{2} \operatorname{erfc}\left(\frac{Q}{\sqrt{2}}\right) \\
&\approx \frac{1}{\sqrt{2\pi}} \cdot \frac{\exp\left(-\frac{Q^2}{2}\right)}{Q}
\end{aligned} \tag{2-10}$$

With

$$Q = \frac{v_s^{pp}/2}{v_n^{rms}} \tag{2-11}$$

The approximation at the last is correct within 10% for $Q > 3$. For some commonly used BER values, the precise numerical values of the integral are listed in Table 2-1 [40].

Table 2-1: Numerical relationship between Q and BER

Q	BER	Q	BER
0.0	0.5	5.998	10^{-9}
3.090	10^{-3}	6.361	10^{-10}
3.719	10^{-4}	6.706	10^{-11}
4.265	10^{-5}	7.035	10^{-12}
4.753	10^{-6}	7.349	10^{-13}
5.199	10^{-7}	7.651	10^{-14}
5.612	10^{-8}	7.942	10^{-15}

For different systems and applications, BER requirement varies. The following are BER values that are commonly used: the SONET OC-48 standard requires a system BER of less than 10^{-10} , which corresponds to $Q > 6.4$. The faster SONET OC-192 standard is tougher and requires a system BER at least 10^{-12} corresponding to $Q > 7.0$. To obtain the required BER at the output of decision circuit, we need to relate BER to quantities that can be measured in other parts of the system. From (2-10) we can see that the first and most direct predictor of BER is the Q parameter, termed as the Personick Q and determined from the sampled values at the input of the decision circuit.

2.5 Sensitivity and Dynamic Range

Another key characteristics of an optical receiver is the sensitivity. The light traveling through the fiber experiences loss, requiring a highly-sensitive receiver to detect the signal with acceptable bit error rate. Here we define the electrical receiver sensitivity, i_{sens}^{pp} , as the minimum peak-to-peak signal current at the input of the receiver necessary to achieve the required BER [40]. Denoting the signal current swing at the input of TIA as i_s^{pp} , then at required BER, we have:

$$i_{sens}^{pp} = i_s^{pp} \quad (2-12)$$

The output signal swing from amplifying stages can also be obtained as following:

$$v_s^{pp} = H_0 \cdot i_s^{pp} \quad (2-13)$$

Where H_0 is the mid-band value of the overall transfer function $H(f)$ for the amplifying stages. In conjunction with (2-11), we can derive the electrical sensitivity to be:

$$i_{sens}^{pp} = \frac{v_s^{pp}}{H_0} = \frac{2Q \cdot v_n^{rms}}{H_0} = 2Q \cdot i_n^{rms} \quad (2-14)$$

where i_n^{rms} is defined as the input-referred noise as the RMS noise at the output of the amplifying stages. With (2-14), for any given input-referred RMS noise and required BER, the electrical sensitivity i_{sens}^{pp} can be worked out.

The sensitivity can also be defined in optical domain as the minimum optical power, P_{sens} , averaged over time, necessary to achieve the required BER [40]. For a DC-balanced signal with high extinction, we have:

$$\overline{i_s} = \frac{i_s^{pp}}{2} \quad (2-15)$$

Combining with (2-2), the average optical power received at the photodiode can be obtained as:

$$\overline{P_s} = \frac{i_s^{pp}}{2\mathfrak{R}} \quad (2-16)$$

Thus the optical sensitivity is:

$$\overline{P_{sens}} = \frac{i_{sens}^{pp}}{2\mathfrak{R}} = \frac{2Q \cdot i_n^{rms}}{2\mathfrak{R}} = \frac{Q \cdot i_n^{rms}}{\mathcal{R}} \quad (2-17)$$

Again, with (2-17), for a given input-referred noise and a specified BER, and with the knowledge of responsivity of photodiode, the optical sensitivity can be obtained. One point that we need to pay attention to is that the optical sensitivity defined is based on the average signal value, whereas the electrical sensitivity is based on the peak-to-peak signal value [40]. As a result, optical sensitivity depends on the pulse width of the optical signal.

From (2-14) and (2-17), it can be observed that the sensitivity of the receiver is determined by three factors: first, the responsivity of the photodiode; second, the overall input-referred noise of the receiver, and third the required BER. Additionally, sensitivity also depends on the detection method employed in the receiver.

As introduced that sensitivity sets the lower limit of the input signal power to achieve the required BER, for weaker signals, noise at the input of receivers will lead to more bit errors that is unacceptable. Besides the lower limit, there is also an upper level known as overload limit, beyond which the required BER cannot be met. In analogy to the sensitivity, we define the input overload current, i_{ovl}^{pp} , as the maximum peak-to-peak signal current for which a specified BER can be achieved [40].

Similarly, we define the optical overload power, $\overline{P_{ovl}}$, as the maximum time-averaged optical power for which a specified BER can be achieved. The interval between lower end set by sensitivity and upper end set by overload current limit is termed as dynamic range of a receiver [40]. The specifications of receiver sensitivity and overload limit for SONET OC-192 and 10Gb/s Ethernet short distance standards are listed in Table 2-2 [55, 56].

Table 2-2 Sensitivity and overload specifications in 10GB/s Ethernet and OC-192

Standard	Sensitivity (dBm)	Overload (dBm)	Reach	Application
10Gb/s Ethernet	-9.9	-1	2~300m	VSR
	-14.4	1.5	2~10km	LAN
	-15.8	-1	2~40km	LAN and MAN
Very short reach (VSR) SONET OC-192	-16	-3	0~300m	VSR in Centre office

2.6 Phase Noise and Jitter

The design of communication systems often deals with phase noise and jitter. The two are closely related effects and usually studied in the contexts of oscillators and phase-locked loops. However, phase noise also brings jitter problem in TIA design. In optical communication, the time-domain behavior of phase noise is of great interest as it represents the extent to which the zero crossings of a waveform are

corrupted. The deviation of the zero crossings from their ideal position in time is called jitter [23, 40].

Chapter 3. TIA Specifications

Being the receiver front-end, TIA will generally be the principal factor in determining the overall noise performance and sensitivity of the optical receiver. As optical communication system is moving toward higher bit rate and larger volume of data transmission, TIA tends to satisfy more stringent requirements. Therefore the design of TIA entails a lot of trade-offs among bandwidth, gain, power dissipation and noise performance. In the following session, we will focus on the main design parameters that characterize the TIA: gain, bandwidth, input-referred noise and input overload current.

3.1 Transimpedance Gain

As introduced, a transimpedance amplifier converts and amplifies the electrical current, i_{PD} , generated from photodiode into voltage signals v_{out} . The transimpedance gain, Z_T , is thus defined as the output voltage change, Δv_{out} per input current change, Δi_{PD} , to characterize the circuit [40]:

$$Z_T = \frac{\Delta v_{out}}{\Delta i_{PD}} \quad (3-1)$$

As operating in the small signal domain, the transfer function defined in (3-1) need be extended into complex domain with a frequency dependent transimpedance $|Z_T(f)|$ and a frequency dependent phase shift $\phi(f)$ between the input and output signals. A generalization of the transimpedance in complex quantity is then to be:

$$Z_T = |Z_T| \cdot \exp(j\phi) \quad (3-2)$$

The higher the transimpedance gain, the larger the output signal can be produced for a given input current. In addition, based on the Friis equation [37], a larger transimpedance gain has a better effect to suppress the noise of the subsequent stages, typically a limiting amplifier. Therefore, it is desirable to make the transimpedance gain of a TIA as high as possible. With this high transimpedance, the input-referred noise $i_{n,Amp}$ can be estimated using the noise of TIA only. However, there is always tradeoff between gain and bandwidth. Also there is an upper limit to the transimpedance that can be achieved. The limit depends on many factors, including the process technology, circuit topology and bit rate. Tradeoffs need to be carefully adjusted between gain and bandwidth to fulfill system requirements. For higher bit rates, it is difficult to obtain a high transimpedance gain while keeping bandwidth as large as low bit rates. Therefore, typical value of transimpedance gain for 10Gb/s system is around 50dB Ω , which is lower than that for 2.5Gb/s [40].

3.2 Input Overload Current

The transimpedance gain, $Z_T(f)$, usually is specified for an input signal that is small enough such that the transfer function can be regarded as linear. However, for short reach distance, TIA may receive large input signals. As the input signal grows larger, the transfer function becomes compressive, that is the transimpedance gain drops. Finally, pulse-width distortion and jitter may set in [40]. These undesirable distortions cause the bit-error rate (BER) of the receiver to increase rapidly with received power.

The critical input signal that causes the BER to go above the specified value for the system, measured peak-to-peak, is called the input overload current of TIA and denoted by i_{ovl}^{pp} . For $i_{PD}^{pp} > i_{ovl}^{pp}$, TIA is said to be overloaded. As introduced before, the overload current also determines the upper limit of the dynamic range of TIA and can be derived from the largest expected optical signal, $\overline{P_{ovl}}$, at the receiver input:

$$i_{ovl}^{pp} = 2\Re\overline{P_{ovl}} \quad (3-3)$$

Where the photodiode responsivity $\Re$ for 10Gb/s application system is assumed to be 0.3A/W. With the overload power specified in Table 2-2, the overload current i_{ovl}^{pp} can be obtained numerically. Taking the OC-192 VSR as an example, we have:

$$\overline{P_{ovl}} = -3dBm = 10^{-3/10}mW = 0.501mW \quad (3-4)$$

$$\therefore i_{ovl}^{pp} = 2\Re\overline{P_{ovl}} = 2 \times 0.3A/W \times \overline{P_{ovl}} = 0.6A/W \times 0.501mW = 0.3mA \quad (3-5)$$

3.3 Input-referred noise current and sensitivity

As discussed in previous section, the noise of TIA often dominates all other noise sources from photodiode and the limiting amplifier, and therefore determines the sensitivity of the receiver. Apparently, input-referred noise current is one of the most critical parameters for TIA.

Again, with (2-17) and the specifications listed in Table 2-2, the input-referred noise current can be calculated as following:

$$i_n^{rms} = \frac{\overline{P_{sens}} \cdot \Re}{Q} \quad (3-6)$$

We still take OC-192 VSR as an example, where 10^{-12} is required for BER, corresponding to a Q factor to be 7.035. With above equation and specifications known, the input-referred noise is:

$$\overline{P_{sens}} = -16dBm = 10^{-16/10} = 0.0251mW \quad (3-7)$$

$$\therefore i_{n,TIA}^{rms} = \frac{\overline{P_{sens}} \cdot \Re}{Q} = \frac{0.0251 \times 0.3}{7.035} = 1.07\mu A \quad (3-8)$$

Once the RMS input-referred noise is obtained, the sensitivity that determines the minimum peak-to-peak signal current at the receiver input necessary to achieve a required BER can be derived using (2-14). Continuously, TIA for OC-192 VSR is taken as an example:

$$i_{sens}^{pp} = 2Q \cdot i_{n,TIA}^{rms} = 2 \times 7.035 \times 1.07 = 15.0549\mu A \quad (3-9)$$

3.4 Bandwidth and Group-delay variation

Similar as for conventional voltage amplifiers, bandwidth of TIA is defined as the upper frequency at which the transimpedance gain $|Z_T(f)|$ drops by 3dB below its mid-band value [40]. Apparently, the bandwidth needs to be large enough to prevent inter-symbol interference (ISI) in random data stream, closing the eye both vertically and horizontally. With this consideration, a large bandwidth is preferred. However, tradeoff comes in again. On the other hand, a larger bandwidth means more noise will be picked up into the system and may lead to an unacceptable signal-to-noise ratio (SNR) level, degrading circuit performance [23]. As a result, bandwidth needs to be well controlled since it is a very important parameter affecting ISI and SNR in the

optical transmission systems. A rule of thumb for NRZ receivers says that the optimum 3-dB bandwidth is approximated to be [40]:

$$BW_{3dB} \approx \frac{2}{3} R_B \quad (3-10)$$

where R_B is the system bit rate. Since in our design the focus is the optical receiver front-end, it is natural for us to assume that the overall bandwidth is set by TIA. In this case, the TIA bandwidth is chosen to be 0.6 to 0.7 times of the system bit rate R_B , that is 6 to 7GHz [40].

Group-delay variation is the other important parameters in determining the amount of ISI and jitter introduced in TIA. Even with large enough bandwidth, distortions in the form of data-dependent jitter may occur if the phase linearity of $Z_T(f)$ is insufficient. As a common parameter to measure the phase linearity, group-delay with respect to frequency, τ , is calculated as [40]:

$$\tau = -\frac{d\phi}{d\omega} \quad (3-11)$$

where ϕ is the phase of transimpedance $Z_T(f)$. Typically, a group-delay variation, $\Delta\tau$, of less than $\pm 10\%$ of the bit period over the specified bandwidth is required to limit the generation of data-dependent jitter. That is for 2.5Gb/s data rate system, group-delay variation should be kept below 40ps, while for 10Gb/s, the upper limit is 10ps.

Based on previous discussions in this chapter and the corresponding standards listed in Table 2-2, we can now summarize the major performance parameters of TIA as shown in Table 3-1.

For the proposed indoor optical wireless communication system, the target design specifications for the transimpedance amplifier are as follows: a bandwidth of

6~7GHz, a transimpedance gain of 50dBΩ, and a low input-referred noise current of less than $20pA/\sqrt{Hz}$.

Table 3-1: Performance parameters for 10Gb/s TIA

Standard	Electrical Sensitivity (μA)	Input Overload Current (mA)	RMS input-referred noise current (μA)	Bandwidth Power Transimpedance	Reach	Application
10Gb/s Ethernet	61.4	0.48	4.36	BW≈6~7 GHz Power < 20mW Zτ ≈50db	2~300m	VSR
	21.8	0.85	1.55		2~10km	LAN
	15.8	0.48	1.12		2~40km	LAN and MAN
Very Short Reach (VSR) SONET OC-192	15.1	0.3	1.07		0~300m	VSR in Centre office

Chapter 4. Basic TIA Topologies

The stringent noise-bandwidth tradeoff constrains TIA circuits to primarily two topologies: open-loop stages and current-feedback amplifiers.

4.1 Open-loop TIAs

Based on the input impedance, open-loop TIA circuits can be classified into two types: low-impedance front-end and high-impedance front-end, as shown in Figure 4-1(a) and (b). Both front-ends essentially consist of a resistor from the photodiode to ground. In the low-impedance front-end case, we assume R_1 to be 50Ω , whereas for the high-impedance front-end, we assume R_2 to be 500Ω [40, 57].

Obviously, the two circuits provide transimpedance gain equal to its resistance correspondingly. However, the time constant RC_j leads to severe trade-off between gain, noise and bandwidth. First, denoting the front-end resistor as R_L , we then derive the general equation for the total output noise. Modeling the thermal noise of R_L as shown in Figure 4-1 (c), we have [23]:

$$\overline{i_n^2} = \frac{4kT}{R_L} \quad (4-1)$$

$$\begin{aligned} \overline{V_{n,out}^2} &= \int_0^\infty \frac{4kT}{R_L} \left| R_L // \frac{1}{j2\pi f C_j} \right|^2 df \\ &= \int_0^\infty \frac{4kT}{R_L} \cdot \frac{R_L^2 df}{R_L^2 C_j^2 4\pi^2 f^2 + 1} \\ &= \frac{kT}{C_j} \end{aligned} \quad (4-2)$$

Figure 4-1: Open-loop TIAs (a) Low impedance (b) High impedance front-end (c) Equivalent circuit for noise calculation

This equation tells us that the total integrated noise is constant and independent of R_L . Hence for both circuits, despite the different front-end resistances, they have the same total output noise. However, for a fair comparison, we need to refer the noise to the input so that it does not depend on the gain. The total input-referred noise current is obtained as:

$$\overline{i_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{R_L^2} = \frac{kT}{R_L^2 C_D} \quad (4-3)$$

Based on above equation, it can be observed that to have the minimum noise, R_L must be maximized. However, we must also take the bandwidth into consideration.

As R_L increases, the time constant $R_L C_j$ also increases, limiting the bandwidth thus the incoming bit rate:

$$BW = \frac{1}{2\pi R_L C_j} \quad (4-4)$$

Equations (4-3) and (4-4) indicate a direct trade-off between speed and noise. Specifically, assuming a photodiode capacitance C_j of 0.25 pF , for the 50Ω low-impedance front-end, we will have a respectable bandwidth 12.7GHz but also a significant input-referred noise current, which is about $2.57\mu\text{A}_{\text{RMS}}$. The other major drawback is the low transimpedance that it provided. For the high-impedance front-end, transimpedance gain increases to 500Ω , which is a reasonable value for 10Gb/s TIA circuit. The noise performance is improved as well. The total input-referred noise current is now down to $0.257\mu\text{A}_{\text{RMS}}$. However, the bandwidth reduces to a mere 1.27GHz , too narrow for 10Gb/s system [40].

The fundamental trade-offs that have been shown suggest that the open-loop topology with no matter low or high impedance front-end is not suitable for high-performance application. Next, we will look into a popular circuit topology which relaxes those constraints.

4.2 Shunt Feedback TIA

4.2.1 First order TIA

The basic shunt feedback TIA is shown in Figure 4-2 (a), in which a negative feedback network is employed to form a shunt-shunt feedback topology. By far, the

shunt feedback transimpedance front-end [58-66] is still the most popular circuit for converting the photodiode current into a voltage signal due to its ability to optimally solve the noise, gain, and bandwidth tradeoff problems at receiver front-end.

Figure 4-2: (a) Shunt feedback TIA (b) Equivalent circuit for noise estimation

Assuming the voltage amplifier is ideal with an inverting voltage gain $-A$, the bandwidth is then determined by the time constant at input node. First, apply KCL at input node:

$$\frac{V_{out} - V_X}{R_F} + I_{in} = \frac{V_X}{sC_j} \quad (4-5)$$

where,

$$V_X = -\frac{V_{out}}{A} \quad (4-6)$$

Reordering (4-5), we have:

$$\frac{V_{out}}{I_{in}} = -\frac{A}{A+1} \cdot \frac{R_F}{1 + \frac{R_F C_D}{A+1} s} \quad (4-7)$$

With above transfer function, the -3dB bandwidth obtained is $(A + 1)/2\pi R_F C_j$, which is consistent with approach by estimating the time constant at input node. With a feedback resistor R_F , the input resistance can be lowered to:

$$R_{in} = \frac{R_F}{A+1} \quad (4-8)$$

$$\therefore BW = \frac{1}{2\pi R_{in} C_j} = \frac{1}{2\pi \frac{R_F}{A+1} C_j} = \frac{A+1}{2\pi R_F C_j} \quad (4-9)$$

The estimated bandwidth for this shunt feedback topology is A+1 times greater than that of the simple resistive open-loop circuit as in Figure 4-1 (b). We also need to examine the noise performance since the low input impedance now presents. The small signal equivalent circuit for noise modeling adopted is shown in Figure 4-2 (b). The noise characteristic of the ideal inverting amplifier is modeled by an input-referred voltage noise source $\overline{v_{n,A}^2}$. Still applying KCL at input node X, we have:

$$\frac{v_{n,out} - v_X - v_{n,R}}{R_F} = \frac{v_X}{sC_j} \quad (4-10)$$

substituting

$$v_X = -\frac{v_{n,out}}{A} + v_{n,A} \quad (4-11)$$

We then have:

$$v_{n,out} = \frac{v_{n,R} + (R_F s C_j + 1) v_{n,A}}{1 + \frac{s R_F C_j}{A}} \quad (4-12)$$

Where A is assumed to be much larger than 1. Here we consider two extreme cases: one is when sC_j is zero, the other is when sC_j approaches infinity. For the first case, with $C_j = 0$, (4-12) is simplified to:

$$v_{n,out} = v_{n,RF} + v_{n,A} \quad (4-13)$$

The corresponding input noise current (per unit bandwidth) is then:

$$\overline{i_{n,in}^2} = \frac{\overline{v_{n,R}^2} + \overline{v_{n,A}^2}}{R_F^2} = \frac{4kT}{R_F} + \frac{\overline{v_{n,A}^2}}{R_F^2} \quad (4-14)$$

Apparently, R_F is directly referred to the input. As R_F value increases, the input-referred noise decreases while the input impedance can still be kept relative small as it is $(A+1)$ times smaller than R_F .

In the other extreme case, when sC_j approaches infinity, (4-12) shows that $v_{n,out}$ approaches $Av_{n,A}$. Therefore if $Av_{n,A}$ does not fall with frequency, the total output noise, the integral of squared magnitude of $v_{n,out}$ from $f = 0$ to $f = \infty$, diverges, leading infinite noise at output. Hence, to do noise analysis, we need to take a look into the core amplifier and employ a more realistic model.

4.2.2 Second-order TIA

We now assume the frequency response of the core amplifier exhibits a single pole, and thus its transfer function can be written as following form:

$$A(s) = \frac{A_0}{1+s/\omega_0} \quad (4-15)$$

where $A_0 \gg 1$. Substituting the new transfer function of the voltage amplifier into (4-7), the new close-loop transfer function for the TIA can be obtained as:

$$\frac{V_{out}}{I_{in}} = -\frac{R_0 \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \quad (4-16)$$

where,

$$R_0 = \frac{A_0}{A_0 + 1} R_F, \quad (4-17)$$

$$\omega_n = \sqrt{\frac{(A_0 + 1) \omega_0}{R_F C_j}} \quad (4-18)$$

$$\zeta = \frac{1}{2} \cdot \frac{R_F C_D \omega_0}{\sqrt{(A_0 + 1) \omega_0 R_F C_j}} \quad (4-19)$$

From basic control theory, ζ is known as damping factor which controls the peaking and ringing of frequency response. The value of ζ has been well studied and chosen to be $\sqrt{2}/2$ to achieve the so-called Butterworth response [42], which gives the maximum flat frequency response. The corresponding ω_0 to keep the critical damping factor can be calculated by setting $\zeta = \sqrt{2}/2$ in (4-19), we then have:

$$\omega_0 = \frac{A_0 \pm \sqrt{A_0^2 - 1}}{R_F C_j} \approx \frac{2A_0}{R_F C_j} \quad (4-20)$$

The interpretation of this equation is that the pole of core amplifier need to be set $2A_0$ times far away from the pole at the input node. The -3dB bandwidth of the second-order TIA is calculated by setting the magnitude of transimpedance gain to the $\sqrt{2}/2$ times its low-frequency value. The obtained result is:

$$BW = \frac{\sqrt{2} A_0}{2\pi R_F C_j} \quad (4-21)$$

Comparing with the bandwidth obtained in (4-9) for the first-order TIA, we notice that the bandwidth increased by a factor of $\sqrt{2}$ as a result of making the bandwidth of the core amplifier finite. The reason is that the pole introduced by the core amplifier creates an inductive behavior, cancelling the roll-off due to the input node pole.

As we have seen so far, the shunt feedback topology offers not only an acceptable transimpedance gain but also satisfied bandwidth, making an obvious advantage over the open-loop topology. In next chapter, we are going to introduce some typical implementations of the shunt feedback TIA in CMOS technology. However, it is worth to note that in order to keep the damping factor under the critical damping point, the transimpedance limit [40] is implied in our derivation, that is:

$$R_0 \leq \frac{A_0 f_0}{2\pi C_j BW^2} \quad (4-22)$$

The $A_0 f_0$ represents the gain-bandwidth product of the core amplifier, and is proportional to the technology parameter f_T . Therefore for given a particular technology, transimpedance gain and the bandwidth directly trades off each other, inspiring researchers to explore more techniques to achieve better performance.

4.3 Voltage Mode TIAs

Voltage mode TIA is the most straightforward implementation of the shunt-feedback topology discussed above. The core voltage amplifier employs either common-source or common-drain configuration. Figure 4-3 shows a typical CMOS voltage mode TIA [23], consisting of a common-source amplifier and a source

follower. With the feedback resistor R_F , the large open loop input impedance at the gate of transistor M_1 does not cause the bandwidth limitation at input node anymore. It is easy to see that the open-loop common source amplifier provides a mid band voltage gain equal to $-g_{m1}R_L$, which is also the scaling factor of the input resistance.

Figure 4-3: CMOS implementation of voltage mode TIA

In addition, the source follower isolates R_L from the loading effect from the feedback resistor R_F and the subsequent stage, providing a more stable frequency response. Intuitively, to achieve a higher gain, we shall increase the value of R_L . However, for a given bias current, as R_L increases, the voltage headroom issue comes in. The voltage drop across R_L is limited to V_{DD} and the gate-source voltage of two transistors. Thus for the common 1.8V V_{DD} design, it is difficult to drive the following source follower. Through the noise analysis studied in [23], we realize that for a given transimpedance gain, the noise contributed by the core amplifier can be minimized by

maximizing R_L and transconductances of transistors M_1 and M_2 . Again, the voltage headroom problem makes it not feasible to implement.

4.4 Current Mode TIAs

Different from the voltage mode TIA, in which the current directly converts to voltage signal in the first step, current mode TIA typically inserts a current buffer between photodiode and basic shunt-feedback TIA, as shown in Figure 4-4. The current buffer inserted here is normally common-gate configured, which provides a low input resistance as the incoming photocurrent sees the source of the transistor. Besides the low input resistance, the current buffer also isolates the photodiode capacitance from input node X of the core amplifier. Thus the parasitic of node X does not add on to the photodiode capacitance any more, pushing the pole at input node further away, relaxing the bandwidth limitation at the input node. This is the key advantage of the current mode TIA compared to the voltage mode.

Figure 4-4: Current mode TIA with common-gate current buffer

Instead of inserting the current buffer, the other form of current mode TIA is to replace the feedback voltage amplifier by a feedback current amplifier as shown in Figure 4-5 (a). The photocurrent is sensed with a small resistor first and then amplified accordingly. A simple implementation of the current amplifier using current mirror is shown in Figure 4-5 (b). The output transistor has a transconductance A times that of the input transistor, performing the current amplification. Similarly, this implementation provides low input impedance, relaxing the bandwidth limitation due to input node pole.

Figure 4-6 shows a balanced TIA, where the unused input terminal is loaded with the same capacitance as the true input terminal. To obtain the symmetrical input impedance, we can connect either a dummy photodiode kept in dark or a capacitor providing the same parasitic as the photodiode. The balanced TIA exhibits excellent noise immunity since any noise from the power supply or the substrate couples equally to the inverting and non-inverting input of the core amplifier and is suppressed as a common mode disturbance [23, 40].

Figure 4-6: Differential TIA with single-ended photodiode

Pseudo-differential amplifier is to replace the matched capacitor in Figure 4-6 by a very large capacitor, shorting the unused terminal to AC ground. This large coupling capacitor is normally implemented off chip. In pseudo-differential TIA, noise immunity is not as good as balanced one since the two input terminal is asymmetric. But pseudo-differential TIA has a better sensitivity and its single-ended input resistance has a lower value.

There are two issues that both types of differential TIA suffer from. First, no matter whether the two input terminal is balanced with same capacitance or not, the incoming signal is always single-ended. Therefore the output signals are not exactly differential as difference in amplitude and phase will always exist. Second, the input-referred noise current of differential TIA is $\sqrt{2}$ times that of its single-ended counterpart, degrading the sensitivity [23].

4.6 Bandwidth enhancement techniques

4.6.1 RGC input stage

It is well known even in early 90s that Regulated Cascode (RGC) configuration provides the characteristics of high output impedance and also wide output voltage [41]. Figure 4-7 shows a RGC input circuit implemented using NMOS transistor and its small signal equivalent circuit.

Figure 4-7: (a) schematic of RGC TIA input stage; (b) Small-signal equivalent circuit

It can be calculated from the small signal analysis that the input resistance of the RGC circuit is given by:

$$Z_{in}(s) \cong \frac{\left(\frac{1}{R_B} + sC_j\right)}{\left(g_{mB} + \frac{1}{R_B}\right)(g_{m1} + sC_j) + \left(\frac{1}{R_B} + sC_j\right)\left(\frac{1}{R_B} + sC_i\right)} \quad (4-23)$$

Also, we have the following approximation:

$$C_i \cong C_{sb1} + C_{gsB} \quad (4-24)$$

$$C_j \cong C_{gs1} + C_{gdB} \quad (4-25)$$

From (4-23), (4-24) and (4-25), we can derive that the input impedance of the RGC input stage is as follows:

$$Z_{in}(0) \cong \frac{1}{g_{m1}(1 + g_{mB}R_B)} \quad (4-26)$$

As the input impedance of a common gate input stage is approximately $\frac{1}{g_{m1}}$, it is obvious that the input impedance of the RGC input stage is $(1 + g_{mB}R_B)$ times smaller than the input impedance of a common gate input stage.

The main reason for the small input impedance is due to the incorporation of a strong local negative feedback. The factor of $(1 + g_{mB}R_B)$ is in fact the voltage gain of the local feedback group [45]. This can effectively reduce negative effect on the TIA bandwidth which is generated by the large input capacitance, including the large photodetector parasitic capacitance [45]. In addition to the low input impedance, it is also noted in [46] that RGC input stage will introduce another zero. This additional zero can be placed at the roll-off region of the gain curve, which can further enhance the circuit bandwidth. With these features and advantages, RGC input stage can be a much better choice for a high speed current-mode TIAs.

4.6.2 Other Bandwidth Enhancement Techniques

Besides the RGC structure, there are other techniques which are commonly used to enhance the circuit bandwidth, such as capacitive degeneration and inductive peaking. These methods will be discussed in Section 5.4.2, 5.5 and 6.2 where the implementation of transimpedance amplifier and limiting amplifier are discussed in detail.

4.7 Noise Analysis

As the first circuit block of front-end receiver, noise performance of transimpedance amplifier is the key factor that determines the overall noise performance and the input sensitivity of the receiver. Therefore the input-referred noise current is a significant figure of merit of TIA design. For optical preamplifiers noise performance is measured in terms of this input-referred noise current. The equivalent input-referred noise is defined to be the current at the input port of a noiseless TIA reproduces the same output noise as the actually noisy TIA. Figure 4-8 shows a typical TIA front-end noise model, where TIA is modeled as a noiseless TIA core circuit with $i_{n,eq}$ as the equivalent input noise current source.

Figure 4-8: TIA noise model based on equivalent input noise current

Denoting the transimpedance gain to be Z_T , for a measured output noise $v_{n,out}$ at output port of TIA, we have:

$$i_{n,eq} \cdot \frac{Z_s}{Z_s + Z_{in}} \cdot Z_T = v_{n,out} \quad (4-27)$$

Manipulating (4-23), we can obtain:

$$i_{n,eq}^2 = \left| \frac{Z_s + Z_{in}}{Z_s Z_T} \right|^2 v_{n,out}^2 \quad (4-28)$$

where Z_s is the source impedance and Z_{in} denotes the input impedance seeing into the TIA circuit. In case of a photodiode as input source for TIA, the source impedance is mainly dominated by C_j , while input impedance of TIA depends on the front-end structure.

4.7.1 Noise model of MOSFET

Figure 4-9: (a) The van der Ziel thermal noise model of a MOSFET (b) The small-signal circuit thermal noise model of a MOSFET

Since MOSFETs are essentially voltage-controlled resistors, they exhibit thermal noise, shot noise and flicker noise. Referring to Figure 4-9 there are three major noise sources as identified in the following equations: drain-source channel thermal noise $\overline{i_{n,d}^2}$, shot noise $\overline{i_{n,g}^2}$ that is due to the gate leakage current, and flicker noise $\overline{i_f^2}$ that decreases as frequency increases [67, 68].

$$\overline{i_{n,d}^2} = 4KT\gamma g_{d0}\Delta f \quad (4-29)$$

$$\overline{i_{n,g}^2} = 4KT\delta g_g\Delta f \quad (4-30)$$

$$\overline{i_f^2} = \frac{K_F g_m^2}{C_{ox}^2 WL f} \quad (4-31)$$

where g_{d0} is the drain-source conductance at zero V_{DS} . The parameter γ equals to 1 at zero V_{DS} , and in long devices, decrease toward a value of 2/3 in saturation. K is the Boltzmann constant, T is the absolute temperature, and K_F is dependent on devices and can vary widely for different devices in the same process. W , L and C_{ox} represent the transistor's width, length and gate capacitance per unit area respectively. Van der Ziel gives a value of 4/3 for the gate noise coefficient, δ , in long devices. The parameter g_g is:

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (4-32)$$

At high frequencies, the channel thermal noise current will be coupled to the gate terminal through the gate-oxide capacitance and thus the gate noise source is also called the induced gate noise. Clearly, it increases with frequency. In addition, since the gate and drain noise sources do share a common origin, they are correlated to each other. The correlation coefficient c is expressed by:

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \overline{i_d^2}}} \quad (4-33)$$

As shown in Figure 4-9(a), the drain noise current flows from the drain to the source and the gate noise flows from the source to the gate, making the correlation coefficient take a negative value. According to recent research works, although the induced gate noise of the input transistors of CMOS TIAs adds directly to the total input-referred noise current, the correlated noise cancels the equivalent input noise due to the channel thermal noise. This means the channel thermal noise is shorted out by the gate capacitance and hence the total noise at the input is reduced. According to

numerical data, the input-referred noise current reduction for optimum transistor size is about 10% to 20% [70]. Therefore, in subsequent noise estimation, the noise term due to the correlation will be neglected since it doesn't have any add-on effect to the overall noise.

To avoid analysis based on this frequency dependent gate noise source, we can recast the model in a form with a noise voltage source that has a constant spectral density [69], as shown in Figure 4-10. The equivalent series noise voltage source is:

$$\overline{v_{n,g}^2} = 4KT\delta\gamma_g\Delta f = 4KT\delta\frac{1}{5g_{d0}}\Delta f \quad (4-34)$$

Figure 4-10: MOS noise model

4.7.2 Noise analysis of shunt-feedback common source TIA input stage

Figure 4-11 shows the shunt-feedback TIA with the input stage implemented with an NMOS transistor. For noise analysis, it is sufficient to consider just the input transistor. There are two major components of the input-referred noise current for TIA: the noise from resistors and the noise from the amplifier front-end [40]. Since they are usually uncorrelated, we can have:

$$i_{n,TIA}^2(f) = i_{n,res}^2(f) + i_{n,front}^2(f) \quad (4-35)$$

In high speed receiver, the front-end noise contribution is generally larger than the noise component contributed by resistors. Now considering the very simple shunt-feedback common-source TIA input stage as shown in Figure 4-11(a). The equivalent small-signal circuit used to derive input-referred noise current is illustrated in Figure 4-11(b). The output noise voltage depends on four noise sources, namely $i_{n,d}^2$, $i_{n,g}^2$, $i_{n,R1}^2$, and $i_{n,R2}^2$. Thus the input noise current is a summed effect of these four noise sources. While $i_{n,g}$ is directly added on to the input noise current, the other noise current components are computed individually as below:

$$C_i = C_{PD} + C_{sb} \quad (4-36)$$

$$C_{out} = C_L + C_{db} \quad (4-37)$$

(c)

Figure 4-11: (a) Schematic of the shunt feedback common source TIA input stage, (b) block diagram for noise analysis (c) its small signal equivalent noise circuit

$$\overline{i_{n,R1}^2} \approx \frac{4KT}{R_1} \left(1 + \frac{1}{g_m^2 |Z_{in}|^2} \right) \quad (4-38)$$

$$\overline{i_{n,R2}^2} \approx \frac{4KT}{R_2} \frac{1}{g_m^2 |Z_{in}|^2} \quad (4-39)$$

$$\overline{i_{n,d}^2} \approx 4KT \gamma g_{d0} \frac{1}{g_m^2 |Z_{in}|^2} \quad (4-40)$$

where Z_{in} is the input impedance mainly determined by C_{PD} and C_{gs} of input transistor, neglecting the effect of feedback resistor R_1 . The total equivalent input noise current spectral density based on (4-38) to (4-40) is estimated to be:

$$\overline{i_{n,eq}^2} \approx 4KT \left[\frac{1}{R_1} \left(1 + \frac{\omega^2 C_{in}^2}{g_m^2} \right) + \frac{\omega^2 C_{in}^2}{g_m^2} \left(\frac{1}{R_2} + \gamma g_{d0} \right) + \delta \frac{\omega^2 C_{gs}^2}{5g_{d0}} \right] \quad (4-41)$$

where C_{in} is the sum of C_i , C_{gs} and the Miller capacitance of C_{gd} . Accounting the correlation between gate noise and drain noise sources to cancel the total equivalent

noise, the overall equivalent input noise current is to be smaller than derived in (4-41).

According to [67, 71], the equivalent input noise current is to be:

$$\overline{i_{n,eq}^2} = 4KT \left\{ \frac{1}{R_1} \left(1 + \frac{\omega^2 c_{in}^2}{g_m^2} \right) + \frac{\omega^2 c_{in}^2}{g_m^2} \left[\frac{1}{R_2} + \gamma g_{d0} \left(1 - \frac{c_{gs}}{c_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] + \delta \frac{\omega^2 c_{gs}^2}{5g_{d0}} (1 - |c|^2) \right\} \quad (4-42)$$

In deep submicron devices, the magnitude of the correlation coefficient can take a value of more than 0.75, which can help to reduce the total input noise significantly for optimum transistor size according to (4-42) and [70].

4.7.3 Noise analysis of common gate TIA input stage

Figure 4-12 shows the common gate TIA input stage implemented with an NMOS transistor. There are a few noise sources introduced at this input node stage. Considering a very simple common gate TIA input stage depicted in Figure 4-12 (a) and (b), and the equivalent small-signal circuit used to derive the input-referred noise current is illustrated in Figure 4-12 (c). The output noise voltage depends on the four noise sources, namely $i_{n,R1}^2$, $i_{n,d}^2$, $i_{n,R2}^2$, and $i_{n,g}^2$. Thus the input noise current is assumed effect of these four noise sources. While $i_{n,g}$ and $i_{n,R1}$ are directly added on to the input noise current, the other noise components are computed individually as below:

Figure 4-12 : (a),(b) Schematic of the common gate TIA input stage; (c) Small signal equivalent circuit

$$\overline{i_{n,R2}^2} \approx \frac{4KT}{R_2} \frac{1}{g_m^2 |Z_{in}|^2} \approx \frac{4KT}{R_2} \left(1 + \frac{\omega^2 C_{in}^2}{g_m^2} \right) \quad (4-43)$$

$$\overline{i_{n,d}^2} \approx 4KT \Gamma_{g_{do}} \left(\frac{1}{g_m^2 |Z_{in}|^2} - 1 \right) \approx 4KT \Gamma_{g_{do}} \frac{\omega^2 C_{in}^2}{g_m^2} \quad (4-44)$$

where Z_{in} is the input impedance mainly determined by C_{PD} and C_{gs} of input transistor. The total equivalent input noise current spectral density based on (4-43) and (4-44) is estimated to be:

$$\overline{i_{n,eq}^2} = 4KT \left[\frac{1}{R_1} + \frac{1}{R_2} + \delta \frac{\omega^2 C_{gs}^2}{5g_{d0}^2} + \frac{\omega^2 C_{in}^2}{g_m^2} \left(\frac{1}{R_2} + \Gamma_{g_{d0}} \right) \right] \quad (4-45)$$

where C_{in} is the sum of C_i from (4-36), C_{gs} . Accounting the correlation between gate noise and drain noise sources to cancel the total equivalent noise, the overall equivalent input noise current is to be smaller than derived in (4-45). According to [44], the equivalent input noise current is to be:

$$\overline{i_{n,eq}^2} \approx 4KT \left\{ \frac{1}{R_1} + \frac{1}{R_2} + \frac{\omega^2 C_{in}^2}{g_m^2} \left[\frac{1}{R_2} + \Gamma_{g_{d0}} \left(1 - \frac{C_{gs}}{C_{in}} |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right)^2 \right] + \delta \frac{\omega^2 C_{in}^2}{g_m^2} (1 - |c|^2) \right\} \quad (4-46)$$

In deep submicron devices, the magnitude of the correlation coefficient $|c|$ can take a value of more than 0.75, which can help to reduce the total input noise significantly for optimum transistor size according to [43].

4.7.4 Noise analysis of RGC TIA input stage

Figure 4-7 in Chapter 4.6.1 has shown a RGC TIA input stage implemented using an NMOS transistor and its small signal equivalent circuit. A few high speed TIA circuit designs reported in the recent years have utilized the RGC input stage, such as the one found in [45] and [44].

The proposed circuit in [45] is given in Figure 4-13:

Figure 4-13: An implementation of TIA with RGC input stage

The noise analysis shows that the equivalent noise current spectral density of the entire circuit is approximately given by the following equation (4-47):

$$\begin{aligned} \overline{i_{eq}^2} \cong & \frac{4kT}{R_s} + \frac{4kT}{R_f} + \frac{4kT \left(\Gamma_{gd0,B} + \frac{1}{R_B} \right)}{\left(g_{mB} + \frac{1}{R_B} \right)^2} \times \left[\frac{1}{R_s^2} + \omega^2 (C_{in} + C_{gsB} + C_{sb1})^2 \right] \\ & + \frac{4KT\omega^2 (C_{gs1} + C_{gbB})^2}{g_{m1}^2} \left(\Gamma_{gd0,1} + \frac{1}{R_f} \right) + \frac{4KT\omega^2 (C_{gd2} + C_{gb1} + C_{db1} + C_f)^2}{g_{m3}^2} \left(\Gamma_{gd0,3} + \frac{1}{R_3} \right) \end{aligned} \quad (4-47)$$

The proposed implementation in [44] is given in Figure 4-14:

Figure 4-14: Another implementation of TIA with RGC input stage

The noise analysis shows that the equivalent noise current spectral density of the entire circuit is approximately given by the following equation (4-48):

$$\begin{aligned} \overline{i_{eq}^2} \cong & \frac{4KT}{R_s} + \frac{4KT}{R_1} + \frac{4KT \left(\Gamma_{gd0,1} + \frac{1}{R_1} \right)}{g_{m1}^2} \omega^2 \left(C_j + \frac{C_{pd}}{1 + g_{mB} R_2} \right)^2 \\ & + \frac{4KT \omega^2 \left(\Gamma_{gd0,2} + \frac{1}{R_2} \right)}{\left(g_{mB} + \frac{1}{R_2} \right)} \left[\frac{1}{R_s^2} + \omega^2 (C_{pd} + C_i)^2 \right] + \frac{4KT \omega^2 C_y^2}{1 + \omega^2 R_b^2 C_b^2} \left[\left(\Gamma_{gd0,3} + \frac{1}{R_3} \right) \left(\frac{1 + g_{m3} R_b}{g_{m3}} \right)^2 + \right. \\ & \left. R_b \right] \end{aligned} \quad (4-48)$$

In (4-48), the third term shows that the estimated input-referred-noise current will be directly related to the photodiode capacitance C_{PD} at high frequency with power of two. With a large photodiode capacitance, the large noise at high frequency is inevitable.

4.8 Summary

In this chapter, basic TIA topologies, including open-loop TIAs and shunt feedback TIAs are introduced with pros and cons. It is shown that the open-loop topology is not suitable for high performance application, therefore subsequent sections focus on shunt feedback topology by reviewing voltage mode and current mode TIAs.

Some commonly used bandwidth enhancement techniques for transimpedance amplifiers, which are single-ended, are also discussed. In the noise analysis section, typical TIA front-end noise model is presented and followed by introducing noise model used for MOSFET transistors: van der Ziel thermal noise model. Various noise analysis examples are provided for different TIA input stage designs, such as shunt feedback common source input stage, current mode common gate input stage, and RGC input stage. All the derived input-referred noise current equations reveal a direct relation of noise to photodiode capacitance C_{PD} at high frequencies with a power order of two, which implies the challenge in designing a high frequency low noise TIA.

Chapter 5. Proposed Cross-Coupled TIA

The small signal equivalent circuit for a photodiode that we used in Figure 2-5 indicates that a photodiode has a different impedance characteristic than a 50Ω resistor. A photodiode generally appears to be a capacitive current source to the first stage amplifier of the receiver, TIA. Being dominated by capacitance, the magnitude of the input source impedance is not constant but keeps increasing with frequency. Therefore a small input resistance is desirable, making the current mode TIA with a common-gate current buffer popular. In this project, we present a cross-coupled current conveyor based TIA which provides us a zero input resistance and also a differential structure.

5.1 Cross-Coupled Current Conveyor

The proposed circuit topology results from the conventional CMOS current conveyor shown in Figure 5-1 [72]. When the four PMOS PM_1 , PM_2 , PM_3 and PM_4 are in saturation region, ideally,

$$V_{sg1} = V_{sg3} = V_1 \text{ \& } V_{sg2} = V_{sg4} = V_2 \quad (5-1)$$

Suppose the bias voltage V_B is 0 V first, the voltage at node a , V_a and voltage at node b , V_b are:

$$V_a = V_{sg1} + V_{sg4} = V_1 + V_2 \quad (5-2)$$

$$V_b = V_{sg2} + V_{sg3} = V_2 + V_1 \quad (5-3)$$

Thus,

$$V_a = V_b$$

(5-4)

Figure 5-1: Conventional CMOS current conveyor

When the current flowing through node a is $I + \Delta i$ and current flowing through node b is I , the differential impedance across node a and b looking into the circuit is:

$$\Delta Z = \frac{\Delta V}{\Delta i} = \frac{V_a - V_b}{\Delta i} = \frac{0}{\Delta i} = 0 \quad (5-5)$$

Thus, no matter how large the current difference between node a and b is, ΔZ will be zero, which is independent of Δi and the parasitic capacitance of the four transistors. If the same capacitors with capacitance C_{PD} are added on nodes a , b respectively, ΔZ will still be zero since $\Delta V_a = \Delta V_b$. This unique property of cross-coupled PMOS current conveyor is referred as “zero differential impedance”.

5.2 Cross-Coupled Current Conveyor Based TIA Input Stage

The proposed cross-coupled current conveyor input stage for broadband TIA is illustrated in Figure 5-2(a), where NMOS transistors are employed for speed advancement over PMOS transistors. The shielded dummy photodiode provides the same junction capacitance as the true input terminal, forming a balanced differential TIA structure.

(a)

(b)

Figure 5-2: Proposed cross-coupled current conveyor input stage:

(a) Circuit schematic, (b) Equivalent input impedance schematic, (c) Small signal analysis model

Now, we will derive the input impedance seen into the source of transistor M_1 as the input signal sees. Applying a test voltage source v_{test} as shown in Figure 5-2(b-c), we then assume that r_0 is very large so that channel-length modulation can be neglected. The following equations can be obtained by applying KCL at nodes S_1 , D_1 , D_2 and S_2 :

$$i_{test} = -g_{m1}v_{gs1} = -g_{m1}(v_{g1} - v_{test}) \quad (5-6)$$

$$i_{test} = -g_{m3}v_{gs3} = g_{m3}v_{d1} \quad (5-7)$$

$$g_{m4}(0 - v_{g1}) = g_{m2}v_{gs2} \quad (5-8)$$

$$g_{m2}v_{gs2} = \frac{v_{s2}}{R_1 // \frac{1}{sC_{PD}}} \quad (5-9)$$

It is reasonable to assume that transistors M_1 and M_2 of cross-coupled pair have the same transconductance that is $g_{m1} = g_{m2}$. Similarly, transistor M_3 and M_4 are also under same bias condition, therefore we have $g_{m3} = g_{m4}$. Manipulating above equations (5-6)-(5-9), we can obtain the input impedance at the source of M_1 :

$$r_i = \frac{v_{test}}{i_{test}} = \frac{1}{g_{m1}} - \frac{1}{g_{m3}^2 R_C} \quad (5-10)$$

$$\text{where } R_C = R_1 // \frac{1}{sC_{PD}} + \frac{1}{g_{m1}} \quad (5-11)$$

In this design R_1 is chosen to be in the range of several hundred ohms and C_{PD} has a nominal value of 0.25pF, therefore within the bandwidth of interest which is in the range of gigahertz range, R_C is in the range of several tens of ohms. At low frequency, $R_C \approx R_1$. From (5-10), it can be seen that input resistance r_i can be adjusted to be zero when transistors M_1 and M_3 are properly biased to fulfill the following equation:

$$g_{m1} = g_{m3}^2 R_1 \quad (5-12)$$

The input impedance seen by i_{in} is the parallel impedance of C_{PD} , R_1 and r_i . As R_1 is in the order of hundred ohms, which is much larger than r_i , the time constant at the input node is $C_{PD}r_i$. With above conditions fulfilled, ideally the input node would have infinite bandwidth frequency response. However, exact zero input impedance is impractical to realize since there is always a small discrepancy between two inputs of the cross-coupled structure due to single-ended supply current. In addition, in real implementation the zero input impedance is hard to obtain since the above equation derived neglects all parasitic impedance which may be significant when high frequency signal is applied. Another consideration is that the zero input impedance

may turn to negative impedance due to various undesirable effects such as variations of component values, or variations caused by physical layout and so on. The amplifier may therefore become an oscillator. As a result, it is reasonable to design $g_{m3}^2 R_1$ to be slightly larger than g_{m1} to compensate possible variations in practical design. For example, $g_{m3}^2 R_1$ can be tuned to be 1.1 times of g_{m1} , and the input impedance is then given by:

$$r_i = \frac{1}{g_{m1}} - \frac{1}{g_{m3}^2 R_1} \approx \frac{1}{g_{m1}} - \frac{1}{g_{m3}^2 R_1} = \frac{1.1-1}{1.1g_{m1}} = \frac{1}{11g_{m1}} \quad (5-13)$$

The resulting input impedance r_i is in the order of several ohms, that is much smaller than the common gate counterpart which is usually the reciprocal of g_{m1} . In this way, the proposed input stage indeed presents very low input impedance. The time constant at the input node, $C_{PD}r_i$ is low enough to cope with the high speed TIA requirement. With such low input impedance, the dominant pole of this cross-coupled current conveyor based TIA is located within the amplifier rather than at the input node.

5.3 Input stage transfer functions

While providing very low input impedance, the cross-coupled structure of the current conveyor raises the circuit complexity by introducing additional poles and zeros. A small signal analysis yields (5-14) – (5-19) of the summed currents at respective circuit nodes S_1 , $D_1(S_3)$, D_3 , $D_2(S_4)$, S_2 , and D_4 :

$$i_{in} = (Y_p + g_{m1} + g_{ds1} + j\omega C_{gs1})V_{S1} - (g_{m1} + j\omega C_{gs1})V_Y - g_{ds1}V_X \quad (5-14)$$

$$0 = (g_{m1} - j\omega C_{gd1} - j\omega C_{gd2})V_Y - (g_{m1} + g_{ds1})V_{S1} + (g_{ds1} + g_{m3} + g_{ds3} + j\omega C_{gs3} + j\omega C_{gd2} + j\omega C_{gd1})V_X - g_{ds3}V_{D3} - j\omega C_{gs2}V_{S2} \quad (5-15)$$

$$(g_{m3} + g_{ds2})V_X = (Y_2 + j\omega C_{gd3} + g_{ds2})V_{D3} \quad (5-16)$$

$$0 = (j\omega C_{gs4} + j\omega C_{gs1} + j\omega C_{gd1} + j\omega C_{gd2} + g_{ds4} + g_{m4} + g_{ds2})V_Y - j\omega C_{gs1}V_{S1} - (j\omega C_{gd1} - g_{m2} + j\omega C_{gd2})V_X - g_{ds4}V_{D4} - (g_{ds2} + g_{m2})V_{S2} \quad (5-17)$$

$$0 = g_{ds2}V_Y - (g_{ds2} + g_{m2} + Y_p + j\omega C_{gs2})V_{S2} + (g_{m2} + j\omega C_{gs2})V_X \quad (5-18)$$

$$(g_{ds4} + g_{m4})V_Y = (g_{ds4} + Y_2 + j\omega C_{gd4})V_{D4} \quad (5-19)$$

where g_{mx} is the gate-source transconductance, g_{dsx} the output conductance, C_{gsx} the gate-source capacitance, C_{gdx} the gate-drain capacitance of transistor M_x . The parameter Y_2 denotes the admittance of resistor R_2 , and Y_p denotes the admittance of C_{PD} in parallel with R_1 .

For simplicity, g_{dsx} can be neglected since $g_{mx} > g_{dsx}$, and $Y_2 > g_{dsx}$. The existence of more than one path between the input and the output node usually creates a zero in the transfer response [73].

By mathematical manipulations, the above six equations yield the following transfer function for this cross-coupled current conveyor,

$$H_1(0) = \frac{V_X}{i_{in}} = \frac{g_{m1}g_{m3}R_1(g_{m1}R_1 + 1)}{g_{m1}g_{m3}^2R_1(g_{m1}R_1 + 2) + (g_{m3}^2 - g_{m1}^2)} \quad (5-20)$$

$$H_2(0) = \frac{V_Y}{i_{in}} = -\frac{g_{m1}^2R_1}{g_{m1}g_{m3}^2R_1(g_{m1}R_1 + 2) + (g_{m3}^2 - g_{m1}^2)} \quad (5-21)$$

$$H_{pov}(0) = \frac{V_{D3}}{i_{in}} = \frac{g_{m1}g_{m3}^2R_1R_2(g_{m1}R_1 + 1)}{g_{m1}g_{m3}^2R_1(g_{m1}R_1 + 2) + (g_{m3}^2 - g_{m1}^2)} \quad (5-22)$$

$$H_{neg}(0) = \frac{V_{D4}}{i_{in}} = - \frac{g_{m1}^2 R_1 R_2}{g_{m1} g_{m3} R_1 (g_{m1} R_1 + 2) + (g_{m3}^2 - g_{m1}^2)} \quad (5-23)$$

In (5-22) and (5-23) if $(g_{m3}^2 - g_{m1}^2)$ is much smaller than the first term in the denominator, we can further simplify them into:

$$H_{pov}(0) = \frac{V_{D3}}{i_{in}} \approx R_2 \quad (5-24)$$

$$H_{neg}(0) = \frac{V_{D4}}{i_{in}} \approx - \frac{R_2}{g_{m3} R_1} \quad (5-25)$$

From above two equations, we can observe that the transimpedance at positive and negative outputs are different, which causes two output signals to have different swing magnitude. We will look into this issue in greater details in later section.

5.4 Proposed Differential TIA

The differential TIA based on the proposed cross-coupled current conveyor input stage is shown in Figure 5-3. The presented TIA circuit, implemented using GlobalFoundries' 0.18μm-1.8V CMOS technology, is composed of four stages, namely a current conveyor input stage, a inter-stage source follower, a gain stage with capacitive source degeneration and an output stage.

With the DC transimpedance of the input stage shown in (5-24) and (5-25), it is easy to derive the overall DC transimpedance z_{o+} and z_{o-} at the positive and negative output port of the proposed TIA circuit as follows:

$$z_{o+}(0) \approx R_2 \frac{g_{m5} R_3}{1 + g_{m5} R_3} \frac{g_{m6} R_4}{1 + g_{m6} R_s} \frac{g_{m7} R_5}{1 + g_{m7} R_5} \quad (5-26)$$

$$z_{o-}(0) \approx -\frac{R_2}{g_{m3}R_1} \frac{g_{m5}R_3}{1+g_{m5}R_3} \frac{g_{m6}R_4}{1+g_{m6}R_s} \frac{g_{m7}R_5}{1+g_{m7}R_5} \quad (5-27)$$

Figure 5-3: Proposed TIA schematic

5.4.1 Pole Estimation

As mentioned above, since the cross-coupled current conveyor presents very low impedance, the lowest pole is located within the TIA circuit. In order to study the bandwidth limiting factors it is necessary to analyze the circuit to estimate pole locations. As the circuit complexity rises with cross-coupled structure, there are more forward paths from input to output port, indicating an increasing number of poles and zeros. It is observed that two pairs of high impedance nodes present in the cross-coupled current conveyor: the drain of M_1 and M_2 (Node A) and the drain of M_3 and

M₄ (Node B), creating two poles:

$$f_A \approx \frac{1}{2\pi r_A (C_{gs3} + C_{sb3} + C_{g2} + C_{gd1} + C_{db1})} \quad (5-28)$$

$$f_B \approx \frac{1}{2\pi r_B (C_{gd3} + C_{db3} + C_{g5})} = \frac{1}{2\pi R_2 (C_{gd3} + C_{db3} + C_{g5})} \quad (5-29)$$

where C_{g2} represents the total gate parasitic capacitance, namely,

$$C_{gs2} + C_{gd2} + C_{gb2} \quad (5-30)$$

In addition, r_A , the resistance at node A, is the parallel resistance seeing down to the drain of M₁ and up to source of common gate transistor M₃. Similarly, the resistance at node B, r_B is the parallel resistance of R_2 , gate resistance of M₅ and drain resistance of M₃. Since the loading resistor R_2 is much smaller than drain resistance r_0 , we can approximate r_A to be $1/g_{m3}$, and r_B to be R_2 . When R_2 is chosen to be 400Ω , larger than r_A , the pole at node B is lower as compared to that at node A. Plugging in the simulated value for the parasitic capacitance of transistors and other parasitic effects, the lower pole f_B is around 4.5GHz.

5.4.2 Capacitive Degeneration

Besides pushing the dominate pole to higher frequencies as that is done at input node, it is also possible to compensate the lower pole f_B with a zero, which could be accomplished by capacitive degeneration [23, 40]. The capacitive degeneration stage, consisting of M₆, R_S and C_S , contributes a zero that is used to compensate the dominant pole. A source follower is added between the input stage

and the capacitive degeneration stage to facilitate DC coupling. With this source follower stage, an additional pole is introduced at the source of M_5 that is node C. By carefully choosing the size of M_6 and proper biasing, this additional pole can be pushed to frequency which is more than two times higher than f_B , keeping the dominant pole unchanged. The zero introduced by the capacitive degeneration stage is then to satisfy the following equation:

$$z = \frac{1}{2\pi R_S C_S} = f_B \quad (5-31)$$

Besides the zero, this capacitive degeneration stage also brings an additional pole at:

$$f_s = \frac{1 + g_{m6} R_S}{2\pi R_S C_S} \quad (5-32)$$

In our design, as the bandwidth is targeted at 6 to 7GHz, we then set the new lowest pole f_s at 6.5GHz, which means to set $g_{m6} R_S \approx 0.44$. The value of R_S and C_S can be easily determined using (5-31) and (5-32) once the size of M_6 is chosen.

The last stage of the TIA circuit is a source follower to provide a 50Ω output impedance matching for measuring purpose. Again, the sizes of transistor at output stage need to be carefully chosen so that the pole at node D won't degrade the overall performance. For simplicity, poles at nodes C and D are neglected since they are placed at higher frequency. However, they will shift the actual pole in (5-32) to a lower value.

5.5 Shunt inductive peaking

To cancel out the deteriorating effect of bandwidth caused by the pole at node

D, an inductor is inserted in series with the load resistor at the capacitive degeneration stage as shown in Figure 5-4. This shunt inductive peaking is a well known technique for bandwidth enhancement [23]. However, since node D is not the dominant pole, the bandwidth enhancement effect is not as obvious as in general cases where the dominant pole is targeted to be cancelled out. The shunt inductive peaking technique here helps to ensure that the targeted bandwidth calculated using (5-32) is achieved. It also helps to reduce the combined effect of poles at higher frequency. Besides boosting the bandwidth shunt peaking also improves the roll-off characteristics [40]. For example, the schematic simulated bandwidth is 5.8GHz for the capacitive degeneration stage. However, its bandwidth is extended to 7.3GHz with shunt peaking inductor inserted.

Figure 5-4: (a) Shunt peaking inductor added

(b) Corresponding pre-layout simulation result for bandwidth and gain

5.6 Noise analysis

The proposed cross-coupled current conveyor stage proves to be a good input stage as it presents a small input load. However, it suffers from a drawback which originates from its structure.

The proposed stage is more complex than conventional common gate input stage. Therefore, more noise sources are introduced along the signal path, deteriorating the noise performance.

As derived in the previous section, V_X and V_Y are not at the same level due to the single input supplied at the positive input port only. However, for noise estimation, it is reasonable to neglect the voltage difference. So we can treat the cross-coupled current conveyor input stage as two identical and separate circuits with M_1 in a diode connected configuration: the gate of M_1 is tied to its drain as shown in Figure 5-5(a). Figure 5-5 (b) shows its noise equivalent circuit including the channel thermal noise sources of the active devices and thermal noise sources of the resistors.

Figure 5-5: (a) Equivalent single-ended input stage for noise analysis of proposed TIA, (b) Its noise equivalent circuit with four noise sources.

Noise sources are assumed to be uncorrelated, output noise voltage can be computed with individual noise current source, and the total output noise is summed as following:

$$\overline{v_{opn}^2} = \overline{v_{opR1}^2} + \overline{v_{opR2}^2} + \overline{v_{opid1}^2} + \overline{v_{opid2}^2} \quad (5-33)$$

The equivalent input noise current spectral density can be estimated as,

$$\overline{i_{eq,1}^2} = \frac{\overline{v_{opn}^2}}{|H(f)|^2} = \frac{\overline{v_{opR1}^2}}{|H(f)|^2} + \frac{\overline{v_{opR2}^2}}{|H(f)|^2} + \frac{\overline{v_{opid1}^2}}{|H(f)|^2} + \frac{\overline{v_{opid2}^2}}{|H(f)|^2} \quad (5-34)$$

Where, $H(f)$ is the transfer function and defined as:

$$H(f) = \frac{v_{op}}{i_{in}} = \frac{gm_3[R_2/(C_{db3}+C_{gd3}+C_{gs5})](R_1/C_{PD})(gm_1+sC_{gs1})}{gm_1+sC_{gs1}+gm_3+sC_{gs3}+(R_1/C_{PD})(gm_1+sC_{gs1})(gm_3+sC_{gs3})} \quad (5-35)$$

Taking noise current source i_{d1} as example, by applying KCL at nodes S_1 ,

$G_1/D_1/S_3$ and D_3 , we have:

$$g_{m1}v_{gs1} + i_{d1} + \frac{v_{gs1}}{Z_{C_{gs1}}} = \frac{v_{s1}}{R_1 // Z_{C_{PD} + C_{sb1}}} \quad (5-36)$$

$$g_{m1}v_{gs1} + i_{d1} + \frac{v_{gs1}}{Z_{C_{gs1}}} + \frac{v_{g1}}{Z_{C_{gs3} + C_{sb3}}} = g_{m3}v_{gs3} \quad (5-37)$$

$$\frac{v_{opn}}{R_2 // Z_{C_{db3} + C_{gd3} + C_{gs5}}} = g_{m3}v_{gs3} \quad (5-38)$$

Through manipulations, we can have:

$$v_{opn} = \frac{g_{m3}[R_2 // (C_{db3} + C_{gd3} + C_{gs5})] i_{d1}}{g_{m1} + sC_{gs1} + g_{m3} + sC_{gs3} + (R_1 // C_{PD})(g_{m1} + sC_{gs1})(g_{m3} + sC_{gs3})} \quad (5-39)$$

The equivalent input noise current spectral density can be estimated as,

$$\begin{aligned} \overline{i_{eq,1}^2} &\approx \overline{i_{R1}^2} + \overline{i_{R2}^2} + \overline{i_{d1}^2} \frac{1}{\left| \left(R_1 // C_{PD} \right) \left(g_{m1} + sC_{gs1} \right) \right|^2} + \overline{i_{d3}^2} \left(\frac{\left| \left(g_{m3} + sC_{gs3} \right) \right|^2}{g_{m3}^2} + 1 \right) \\ &\approx \frac{4KT}{R_1} + \frac{4KT}{R_2} + \frac{4KT\gamma g_{d0,1} \left[1 + R_1^2 \omega^2 (C_{PD} + C_{sb1})^2 \right]}{R_1^2 (g_{m1}^2 + \omega^2 C_{gs1}^2)} \\ &\quad + \frac{4KT\gamma g_{d0,3} \left[g_{m3}^2 + \omega^2 (C_{gs3} + C_{sb3})^2 \right]}{g_{m3}^2} + 4KT\gamma g_{d0,3} \end{aligned} \quad (5-40)$$

The input noise current spectral density for capacitive degeneration stage is as follows [74],

$$\overline{i_{eq,2}^2} = \frac{4KT\omega^2 C_{tot}^2}{1 + \omega^2 R_s^2 C_s^2} \left[\left(\gamma g_{d0,6} + \frac{1}{R_4} \right) \left(\frac{1 + g_{m6} R_s}{g_{m6}} \right)^2 + R_s \right] \quad (5-41)$$

where C_{tot} is the total parasitic capacitance at node D, including C_{gd6} , C_{db6} , C_{gs7} , and C_{gb7} . The noise contributed by the buffer stages are ignored here, because the major focus is given to the cross-coupled input stage and the capacitive degeneration stage.

It can be seen from (5-40) that the thermal noise contributions from R_1 and R_2

become dominant at low frequencies, while the dominant high-frequency noise comes from the fourth term, and is dependent on the parasitic capacitances C_{gs3} and C_{sb3} . As can be seen from the analysis in Chapter 4, the high-frequency noise of the input-referred noise current for conventional common-gate (CG), and Regulated Cascode (RGC) input stages, is related to the photodiode capacitance C_{PD} directly. Therefore, the proposed cross-coupled input structure can achieve more effective isolation of the photodiode capacitance from the bandwidth determination.

The third term in (5-40) is due to the noise current of additional transistor M_1 . As observed in (5-40), ω^2 appears in both denominator and numerator of the third noise term, making the overall value finite. The reason lies in the additional zero the cross-coupled structure introduced. This noise term which is related to the photodiode capacitance C_{PD} doesn't increase with the frequency monolithically as in the conventional CG, RGC cases in [74], [75]. The noise term, which increases with frequency, is contributed by the parasitic capacitance $(C_{gs3} + C_{sb3})$. $(C_{gs3} + C_{sb3})$ is much smaller as compared to C_{PD} . Therefore, the input-referred noise current spectral density is expected to be smaller at high frequency than those of conventional CG, RGC structure.

Similarly, the negative half part of the input stage also has the same equivalent noise current at negative input port, that is $i_{eq,1}$. As now we treat negative input port as input, the noise voltage at negative output port is the same as v_{opn} that is derived in (5-33). As mentioned in Section 4.5, the overall input-referred noise current is $\sqrt{2}$ times [40] of the single-ended output counterpart for the differential circuit. This argument treats both positive and negative ports as input terminal. In the proposed

TIA, considering the differential input ports, the overall input noise current will also be $\sqrt{2} i_{eq,1}$.

5.7 Layout and Post-layout Simulation Results

The proposed TIA is designed and fabricated in GlobalFoundries' 0.18- μm 1.8-V Industry Compatible (IC) CMOS technology. L_1 and L_2 are implemented using on-chip spiral inductors for the purpose of monolithic implementation and area efficiency. An on-chip MIM capacitor C_{PD} of 0.25pF is used to mimic a typical junction capacitance of the photodiode. Pre-layout, post-layout and measurement results are superimposed in Figure 5-8 to ease comparison. The pre-layout simulation fits the analysis well. With capacitive generation and inductive peaking techniques, the proposed TIA achieves a transimpedance gain of 50.2dB Ω with a -3dB bandwidth of 7.3GHz through schematic simulation, as shown in Figure 5-8 with blue line. Excluding the output stage, core part of the proposed TIA consumes power of 10.9mW.

The layout of the proposed TIA circuit shown in Figure 5-6 has a total size of 0.48mm². The post-layout simulation results degrade due to parasitic effects. To facilitate measurement setup, two input coupling capacitors are added, causing the transimpedance gain reduced by 3dB Ω compared to pre-layout simulation. As shown in Figure 5-8 with red line, we notice that the bandwidth has also reduced to around 5.5GHz, failing to meet the specification. Therefore more work need to carry on in both layout optimization and circuit modification. More discussions are presented in Chapter 7.

Figure 5-6: Layout of proposed TIA circuit

5.8 Measurement results and analysis

Figure 5-7: Microphotograph of fabricated chip of the proposed TIA design

Figure 5-8: Pre-layout, post-layout and measured transimpedance gain of the proposed TIA design

The measurement results degrade due to underestimation of parasitic effects and process imperfection as compared to the post-layout simulation. Figure 5-7 shows the chip microphotograph, where the core has an area of $0.7 \times 0.5 \text{ mm}^2$. With the buffer included, the total power consumption is 31.5mW. The frequency response of the chip is measured with HP8510C network analyzer. Figure 5-8 shows the measured transimpedance frequency response with green line. It is observed that the low-frequency transimpedance gain for the positive single-ended port is around 46dBΩ and the -3dB bandwidth is about 4GHz. As compared to the blue and red lines for pre-/post-layout simulation results, the peaking effect in the measured result is less severe. The pole within the band of interest is not tuned out well. This could be due to the non-ideality of inductors as well as larger parasitic effects for real implementation. In addition, the unaccounted EM radiation loss, the silicon substrate loss and process variations all contributed to the bandwidth degradation. Again in Chapter 7.2, there

are more discussions on the variations in fabrication and potential methods to achieve a better bandwidth.

5.9 Input Capacitance Insensitive

One of merits of this cross-coupled current conveyor based TIA is its ability to tolerate large variations of total capacitive load at the input node. The major contributor of this load is the junction capacitance of the photodiode. Therefore, this merit makes the proposed TIA circuit efficient to work for a wide range of systems with various types of photodiodes. As shown in (5-7), as the junction capacitance of photodiode C_{PD} increases, R_C will decrease, and r_i in (5-6) will decrease accordingly. Therefore, the time constant at the input load with increasing C_{PD} can still keep at a low value since r_i is moving in the opposite direction. This property makes the usage of large area photodiodes possible since the TIA performance will not be that sensitive to the variations of C_{PD} . With a larger area photodiode, a better signal power can be captured with acceptable degradation of the bandwidth and noise performance [40].

For conventional design, the value of the photodiode junction capacitance directly affects the TIA bandwidth. As C_{PD} increases, the bandwidth reduces proportionally. Table 5-1 shows the post-layout simulated bandwidth and transimpedance for different photodiode junction capacitances. It can be seen that the variations in bandwidth and transimpedance are kept within 6% of the nominal value as C_{PD} varies from 0.05pF to 0.5pF. Thus, the “zero differential impedance” property of the current conveyor stage indeed makes the TIA bandwidth less sensitive to the variations of C_{PD} .

Table 5-1: Proposed TIA performance at different C_{PD}

C_{PD} (pF)	Transimpedance(dB Ω)	BW (GHz)
0.05	48.58	5.26
0.10	48.23	5.37
0.15	47.89	5.42
0.20	47.56	5.46
0.25	47.32	5.46
0.30	46.94	5.44
0.35	46.65	5.41
0.40	46.36	5.39
0.45	46.09	5.36
0.50	45.82	5.06

5.10 Differential TIA Output

The other merit of the proposed TIA circuit is the ease of obtaining differential output signals. The proposed TIA is based on a cross-coupled structure, therefore it is convenient to make the TIA circuit differential. Unlike the conventional single-ended TIA circuit, where an extra single to differential conversion step is needed, this cross-coupled structure provides a good base for a differential TIA circuit as shown in Figure 5-3. Due to the measurement setup, the negative output port has been internally terminated with 50 Ω resistor. As a result, only the schematic simulation results are provided here for demonstration and comparison.

The drawback of this differential TIA circuit is that the two output signals do not have the same swing magnitude as shown in Figure 5-9, since the negative input terminal has no input signal supply. The solid line which represents the output signal

at the positive terminal has a peak-to-peak swing of 72mV with a 200 μ A input current source, while the bar representing the output signal at the negative terminal only has a peak-to-peak swing of 30mV. This difference in swing magnitude will be greatly reduced and eventually eliminated in subsequent amplification stages. However, due to the cross-coupled structure, there will always be a small phase difference between the two output signals. Again, the phase difference can be controlled to a negligible level: as shown in Figure 5-9, the phase difference is within 5ps for 5GHz sinusoid input waveform.

Figure 5-9: Transient simulation of output signals.

5.11 Low Noise

As the negative output port is internally terminated for measurement purpose, only the positive output port noise is measured. Different from the typical differential circuits, due to the cross-coupled structure in proposed TIA, the negative half part of the TIA also contributes to the measured output noise at positive output terminal. Based on analysis in Section 5.3, the input noise current $i_{eq,1}$ at negative input terminal will result in a noise voltage at the positive output terminal following transfer function in (5-27). (5-26) and (5-27) reveal that the transimpedance gain for an input signal at the positive input port is $g_{m3}R_1$ times smaller for the negative output terminal than that of the positive one. As seen from simulation parameters, $g_{m3}R_1$ is estimated to be 4. Therefore, for the same input-referred noise current at differential input ports, $i_{eq,1}$, the resulted noise voltage at the positive output terminal will be:

$$\overline{v_{on}^2} = \overline{v_{opn}^2} + \left(\frac{1}{4}v_{opn}\right)^2 = \left(\frac{17}{16}v_{opn}\right)^2 \approx \overline{v_{opn}^2} \quad (5-42)$$

Therefore, the measured input-referred noise is close to $\overline{i_{eq,1}^2}$ for the positive single-ended circuit part. Figure 5-10 shows the input-referred noise current spectral density for positive half portion of the TIA circuitry in frequency range from 600MHz to 6GHz. The input-referred noise current spectral density is up to $18pA/\sqrt{Hz}$. The average input-referred noise current spectral density over 6GHz is estimated to be $10pA/\sqrt{Hz}$. As compared to other CMOS TIA design, the cross-coupled current conveyor based TIA has a very apparent advantage in the noise performance with single-ended configuration.

In typical case when the proposed TIA is employed with differential outputs, the overall input-referred noise current spectral density will be $\sqrt{2}i_{eq,1}$, around $14pA/\sqrt{Hz}$. However, if treating the positive input port as the only input terminal, with differential output terminals, the overall input-referred noise current spectral density will be much larger. The output noise voltage at negative output terminal v_{opn} is now discounted to the positive input terminal with a $g_{m3}R_1$ times smaller gain, resulting a $g_{m3}R_1$ times larger input-referred noise current. The overall equivalent noise current at positive input port is estimated to be:

$$\overline{i_{eq,p}^2} = \overline{i_{eq,1}^2} + \frac{\overline{v_{opn}^2}}{z_{o-}^2} = \overline{i_{eq,p}^2} + (g_{m3}R_1)^2 \overline{i_{eq,p}^2} \approx \sqrt{17} \overline{i_{eq,p}^2} \quad (5-43)$$

Therefore, the input-referred noise current is estimated to be 4.1 times larger, which is $41pA/\sqrt{Hz}$ for single positive input and differential output configuration of the proposed TIA.

Figure 5-10: Input-referred noise current for single-ended configuration

The group-delay variation is the other important parameter in determining the amount of ISI and jitter introduced in TIA. Even with large enough bandwidth,

distortions in the form of data-dependent jitter may occur if the phase linearity of the transimpedance response $Z_T(f)$ is insufficient [74], [40]. As the common parameter to measure the phase linearity, group-delay with respect to frequency is calculated and shown in Figure 5-12. It can be observed that within the bandwidth of 4GHz, the group delay is about 125 ± 25 ps.

Figure 5-11: Measured group delay response of the proposed TIA.

5.12 Summary

In this chapter, a cross-coupled current conveyor based input stage for TIA is presented to provide very low input impedance. Therefore, the influence on the TIA bandwidth of the large input capacitance dominated by the photodiode capacitance can be greatly reduced as shown in Table 5-1. Based on this cross-coupled topology, a prototype of differential TIA design is proposed, which also employs series inductive peaking and source degeneration for bandwidth enhancement. The detail analysis of the proposed TIA is then followed and mainly focused on pole allocations and noise

performance by mathematical calculation. It is worth to note that during gain derivation, pole allocation calculations and even the noise analysis, there are several assumptions made to simplify the model adopted, such as transconductance of transistors in differential pair are perfectly matched, output resistance seeing into the drain of transistors are assumed infinite and so on. In fact, in heavily scaled processes today, especially in sub-100nm process technology, perfectly matched transconductances become unrealistic. Taking consideration of these factors, the cross-coupled stage need carefully and even over design to avoid oscillation occurs. In addition, the actual gain would be reduced with a smaller finite output resistance. The under-estimate of these parasitic effects may also result in an unexpected reduction in bandwidth, such as the pole turns out to be not well tuned out by the inductors compared to simulations, or more severely, poles estimated further away from dominated pole shifts closer or even become the dominate pole. The complexity of noise performance would also increase tremendously.

The proposed TIA design has been realized using GlobalFoundries' 0.18 μ m IC CMOS technology. The measurement results show a transimpedance gain of about 46dB Ω and a -3dB bandwidth of about 4GHz. The noise measurement shows an average input-referred noise current spectral density of about 10 $pA/\sqrt{Hz}$ up to 6GHz for single-ended configuration, which suggests an average input-referred noise current spectral of 41 $pA/\sqrt{Hz}$ for the differential outputs referring to the positive single input port. The measured group delay response is within ± 25 ps over the bandwidth of interest. The circuit consumes 10.9mW DC power from a single 1.8V supply.

The Table 5-2 below summarizes the performance of the proposed TIA design in comparison with other CMOS TIA designs. For measurement purpose, the negative output is terminated internally rather than presents a differential output in general applications. Therefore, the transimpedance gain measured here is only for positive output portion. The negative part gain is estimated to be $\frac{1}{g_{m3}R_1}$ of positive output terminal gain as derived in section 5.3. The actual differential output TIA gain is then expected to be higher. With a differential gain counted in, the proposed design exhibits great potential for 10Gb/s optical data links compared to existing designs.

However, according to the TIA specifications discussed in Table 3-1, the measured bandwidth failed to meet targeted 6-7GHz. Further improvement in bandwidth enhancement as well as layout optimizations is necessary. More discussion on future work is presented in Chapter 7.

Table 5-2: Measured results of the proposed TIA design in comparison with other CMOS TIA designs

Design	[84] Simulation results	[85]	[86]	[87] Simulation results	[88]	This work
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.5 μ m CMOS	80nm CMOS	0.18 μ m CMOS
Topology	Regulated cascode	Two stage	Common gate	Common gate	Common gate	Cross-coupled current conveyor input stage
BW (GHz)	7.7	8.6	4.7	3.5	13.4	4
Gain (dBΩ)	61	59	50	64	52	46
Power (mW)	N. A.	19	90	20	2.2	11
Supply Voltage (V)	1.8	1.8	3	3.3	1	1.8
PD Cap. (pF)	0.3	0.15	0.25	0.25	0.3	0.25
Input-ref Noise (pA/sqrtHz)	20	25	80	15	50	10 (single-ended)
No. of Inductors	0	4	2	1	4	2
Techniques Employed	Source follower RGC Double three- order active feed-back	Inductive shunt peaking Series peaking	Inductive shunt peaking Voltage- current feedback	Inductive shunt peaking Voltage- current feedback	Inductive shunt peaking Common gate feed-forward	Inductive shunt peaking Capacitive source degeneration

Chapter 6. Limiting Amplifiers

As introduced in previous chapters, following transimpedance amplifier, limiting amplifier is used to further amplify the small voltage signal to facilitate subsequent decision circuitry. Therefore, limiting amplifiers exhibits a high voltage gain as well as large output swings.

6.1 Design Considerations for Limiting Amplifier

There are many design considerations for a limiting amplifier, such as bandwidth, gain, and DC offset voltage. With TIA to be the first signal amplification stage, noise performance is less critical in limiting amplifier [89].

6.1.1 Gain Cell

The definition of gain for limiting amplifier is the same as other voltage amplifiers, which is the ratio of output and input voltage change:

$$A = \frac{\Delta v_o}{\Delta v_{in}} \quad (6-1)$$

As a result, with a higher gain, larger voltage swing at output is expected. As mentioned above, the gain of limiting amplifier needs to be large enough to drive the subsequent digital circuit. Therefore, limiting amplifier generally amplifies signal through few stages. A typical limiting amplifier can be implemented with several differential pairs cascaded together as shown in Figure 6-1. As a rule of thumb, the number of stages should be limited to 4. The reason is that even only the first

amplifying stage is the main noise contributor, too many stages will still negatively impact the overall circuitry in other factors, such as the total power dissipation, bandwidth, and also the total noise voltage generated at output port.

Figure 6-1: Cascaded gain stages for limiting amplifier

6.1.2 Bandwidth

The bandwidth requirement is more stringent for limiting amplifier compared to transimpedance amplifier. For TIA, as discussed in Chapter 3, the bandwidth is set to be 70% of the data rate to minimize the noise. However, in case of limiting amplifier, it is desired to have bandwidth equal to the data rate. This is to take the bandwidth reduction when cascading TIA and limiting amplifier into consideration. If both TIA and limiting amplifier have same bandwidth, the overall bandwidth will be much smaller [23].

6.1.3 Input offset voltage

The input offset voltage is defined as the input voltage for which the output voltage is zero. Due to process variation or mismatch in the signal path routing and many other factors, the offset voltage for the differential pairs is usually finite but not zero. In case of signal differential pair, the offset voltage can be tolerable. However, in limiting amplifier where signals propagate through several differential stages, the

small offset voltage at input can be amplified significantly, even saturate the subsequent. This non-zero offset voltage may also result in more bit errors, pulse width distortions and so on. In view of the possible significant negative effect of the offset voltage, an offset voltage cancellation circuit to compensate the offset voltage is necessary for the limiting amplifier [23, 40].

6.2 Design Techniques for Limiting Amplifiers with High Bandwidth

As mentioned in Section 6.1, a limiting amplifier often involves a few amplifying stages so that a larger gain can be achieved. The number of stages is no more than 4 to minimize the negative effect of noise and power dissipation. However, in situations whereby the operating bandwidth is high and input signal amplitude is small, mere cascading of simple differential pair stages with resistive loads as shown in Figure 6-2 are inadequate.

Figure 6-2: A cascade of simple differential pair stages with resistive loads

With the current technology, there are a number of commonly known circuit design techniques which allow higher bandwidth of operation. Some of them are described respectively in the following sections.

6.2.1 Capacitive Degeneration with Series Feedback

It is desirable to suppress the transistors' capacitance in a differential pair so that the effective transconductance can be increased when system operates at higher frequency ranges. In this manner, the gain roll-off which resulted from the pole at the output node can be compensated. Figure 6-3 shows a circuit with both capacitive and resistive degeneration, and its half equivalent circuit [77].

Figure 6-3: (a) Differential Pair with capacitive and resistive degeneration (b) the half equivalent circuit

An obvious advantage of using the above described degeneration technique comes from the change in the input impedance of the amplifier and subsequently changes the load as perceived by the preceding stage. In a cascade of differential

pairs, it is possible to allow the zero resulting from capacitive degeneration to cancel the pole due to the gate-source capacitance of the transistors themselves.

It can be shown that by applying capacitive degeneration, the amplifier's bandwidth is increased by a factor of $\frac{(1+g_m R_S)}{2}$, while the DC gain is lower by the same amount; and also the capacitance seen by the preceding stage is also reduced by the same factor [77].

6.2.2 Inductive Peaking

The idea of inductive peaking is to allow the capacitance which limits the bandwidth to resonate together with the inductor, in this way, the speed of the circuit can be improved. This resonance should take place with minimal overshoot as well as peaking so that for a random data, a well-behaved response can be provided. A common source stage with load capacitance and inductor peaking is shown in Figure 6-4, the small-signal equivalent circuit is shown together.

Figure 6-4: (a) A CS stage with load Capacitance and inductor peaking (b) small-signal equivalent circuit

Although inductive peaking can substantially increase the bandwidth, when the chip area is critical, the traditional components, such as inductor may not be suitable to be used. In such a case, inductive peaking can also be realized by using active devices. An active inductor can be achieved using a simple source follower such as the one shown in Figure 6-5. The small signal equivalent circuit of the source follower neglecting the source-bulk capacitance, the gate-drain overlap capacitance, the body effect and the channel-length modulation is shown as well.

Figure 6-5: (a) Source Follower; (b) Small-signal equivalent circuit

Where v_x and i_x are small testing sources to derive the impedance seeing into source of M1, z_{out} . Applying KCL at source and gate of M1, we have:

$$g_m v_{gs} + i_x + v_{gs} s C_{gs} = 0 \quad (6-2)$$

$$v_{gs} s C_{gs} + \frac{v_{gs} + v_x}{R_s} = 0 \quad (6-3)$$

By manipulating (6-2) and (6-3), we obtain:

$$v_x = -v_{gs} (s R_s C_{gs} + 1) \quad (6-4)$$

$$i_x = -v_{gs} (s C_{gs} + g_m) \quad (6-5)$$

$$\therefore Z_{out} = \frac{s R_s C_{gs} + 1}{s C_{gs} + g_m} \quad (6-6)$$

In (6-6), the impedance seeing into source of M1 contains a zero at $1/R_s C_{gs}$ and a pole at g_m/C_{gs} as shown in Figure 6-6. With $R_s \gg 1/g_m$, within certain frequency band, z_{out} will increase with frequency, exhibiting an inductive behavior as shown in Figure 6-6.

Figure 6-6: The impedance seeing into source of M1

A major drawback of using a simple source follower as the active inductor is the large voltage headroom consumption. To maximize the transconductance while not introducing significant source-body and gate-drain overlap capacitance, it is crucial that the bias current of the active device is maximized. The maximization of the bias current will lead to a large gate-source voltage. As a result, such a circuit is not suitable to be used when the supply voltage is below 1.5 V.

6.3 DC Offset Compensation Network Literatures

Extensive research work has been carried out to make limiting amplifier a full integration and low cost using CMOS technology [76-80]. These designs focus on improving its bandwidth and gain, while its offset compensation network is left off-chip. Recently, a limiting amplifier with a fast settling time for its offset compensation circuit is reported [81]. Apart from novel TIA circuit design, the implementation of the new fully integrated DC offset compensation network for limiting amplifier is also an important contribution of this research.

6.3.1 Typical LA Implementation with Offset Compensation Network

A typical architecture of the limiting amplifier is shown in Figure 6-1. It consists of several gain cells which are basically NMOS differential pairs to provide sufficient high voltage gain and large output swings. Therefore, even very tiny input offset voltage can be amplified through propagation in these cascaded stages, eventually shut off subsequent differential pairs and result in imbalanced outputs. It also brings more bits errors, and pulse-width distortions as introduced in Section 6.1.3.

There are various sources to bring the undesired input offset voltage, such as process imperfections causing the mismatched differential pair, or mismatched resistors, or imbalance in layout routing of differential signal paths and so on. As a result, DC offset compensation network is an essential element of limiting amplifier designs to minimize the offset voltage.

6.3.2 Other Offset Compensation Network Designs

As mentioned a limiting amplifier with a fast settling time for its offset compensation circuit is reported [81]. Different from traditional offset compensation network in which the offset input voltage is compensated with difference between LPF filtered output differential signals, the proposed offset compensation technique in [81] estimates the output referred offset of the main amplifiers as the difference between the peak values of the differential outputs. As peak value is used to estimate the offset between differential outputs, if the feedback is from a saturated output, the offset voltage between differential signals cannot be accurately estimated. To avoid this corruption of the offset information, peak detectors need to be placed at the output of each amplifier stage, and a digital selection logic is then implemented to select the last unsaturated peak detector output to feed back to input through a continuous-time integrator as shown in Figure 6-8. As number of amplifier stages in the compensation loop can change with different input level, the overall gain in feedback loop also changes. To keep consistent overall loop gain, the integrator gain need to be adjusted with number of amplifier stages involved in feedback loop. The layout area for this proposed offset compensation network occupies more than 60% of total chip area.

Figure 6-8: Limiting amplifier with proposed offset compensation network in [81]

6.4 Proposed Offset Compensation Scheme

To get rid of large off-chip RC LPF elements in traditional offset compensation schemes, and also to reduce circuitry complexity in the offset compensation network in [81], the offset compensation scheme proposed is illustrated in Figure 6-9. The output-referred offset of the gain cells is defined as the difference between two differential common-mode voltages at output port. Assuming the system is processing a bi-phase NRZ signal, the DC level of the processed signal is then its mid value. As a result, the output-referred offset of the gain cells can be estimated as the difference between mid values of the two differential outputs. Thus, we propose an offset compensation scheme using DC generating circuits to sense the difference between mid values of two differential outputs, on which a feedback loop is built.

Compared to peak value is used to estimate the offset voltage in [81], the benefit of using mid value instead of peak value of differential outputs is that even the

peak value saturated in both signals, the offset information can be still picked in the valley of differential signals. The assumption here is that differential signals are not saturated in both peak and valley simultaneously. As in case of any offset input voltage existing, only one of output will be saturated.

Figure 6-9: Proposed LA offset compensation network using DC generating circuit

6.4.1 DC generating circuit

In order to sense the difference between mid values of two differential outputs, we basically need a circuit to detect the maximum and minimum of an input waveform and output the average of the two. Therefore, this DC generating circuit here consists of a peak and a valley detector. Peak and valley value of the signal are detected and stored to obtain its mid value. The peak detector is implemented with a rail-to-rail buffer with a switching MOSFET and a storing capacitor as shown in Figure 6-10 [82].

Figure 6-10: Peak detector circuit

The buffer has a pair of differential inputs and a single two-level output controlling the switching of the following PMOS. If the input at positive terminal is larger than the negative one, that means voltage stored on the storing capacitor is larger than the input signal. Hence the buffer outputs a “high” to turn off the following PMOS. Then the capacitor stores the larger value. Conversely, if the voltage on the capacitor is smaller than the input signal, the buffer then outputs a “low” to turn on the PMOS. And then V_{dd} starts to charge the capacitor till the voltage exceeds the input signal. As a result, the peak value of the input signal is stored [82].

The valley detector works in a similar way as shown in Figure 6-11. The PMOS in peak detector circuit is now replaced with a NMOS transistor. With the input at positive terminal larger than the negative one, the buffer outputs a “high”, turning on NMOS. Then charges stored on the capacitor start to discharge as it sees a path to ground. Until the voltage on capacitor decreases to V_{in} , the output of the buffer starts to toggle and a “low” to turn off the NMOS, shunting of the discharging path to ground of the capacitor. As long as the buffer sees a smaller input signal at negative input terminal, a discharge path will be formed to decrease the voltage across the capacitor accordingly. In this way, the output always tracks to the lowest input signal [82].

Figure 6-11: Valley detector circuit

The buffer used in peak and valley detectors can be implemented using a differential amplifier as shown in Figure 6-12. The idea is to make use of amplifier to amplify the difference between two inputs, and thus to pull the output towards ground or V_{cc} . When v_{in+} is greater than v_{in-} , I_{D2} will be larger than I_{D1} . As $I_{D3} = I_{D1}$ and the current in M_3 will be mirrored to M_4 , we have:

$$I_{D2} > I_{D1} = I_{D3} = I_{D4} \quad (6-7)$$

This will pull the voltage at drain of M_2 towards ground until $I_{D2} = I_{D4}$. At the same time, as V_{D2} decreases, M_5 of the inverter will be turned on and outputs a “1”.

Figure 6-12: Differential amplifier input buffer

This buffer has no external bias voltage input. When incorporating it into the feedback loop of limiting amplifier, the output signal from limiting amplifier directly couples to the input of the buffer. If the inputs to the buffer fall below the threshold voltage, the transistors in differential pair will move into the sub-threshold region, reducing the response speed of the buffer. This will cause the propagation delays to increase. Besides carefully design the DC level of output limiting amplifier. To get better performance for lower input level signals, a PMOS version of the buffer can be used together with the NMOS buffer to obtain a rail-to-rail input buffer as shown in Figure 6-13.

Figure 6-13: A rail to rail input buffer based on the NMOS and MPOS differential amplifier input
buffer [82]

6.4.2 Mid value

As shown in Figure 6-9, the peak and valley values of the input signal are then going through two resistors and stored at a capacitor. The two resistors are used to average the maximum and minimum voltages and then feedback the result to another buffer. The two resistors are also used to leak charge off from the capacitors so that the DC generating circuit can follow the changes in the input data.

6.5 Gain Cells

Differential pair with active inductive load is chosen for gain cell structure as shown in Figure 6-14. As shown in Section 6.2.2, the active inductor with a source follower configuration indeed behaves as an inductor in certain frequency range. The drawback is the voltage headroom dropped across the gate-source of the transistors, making it not suitable for low power supply design. As the proposed design is carried out with 1.8V supply voltage, this active inductor can be implemented and has apparent advantage in terms of chip area.

Figure 6-14: Gain cell with active inductor

6.6 Simulation Results and Performance Comparison

The proposed limiting amplifier has been optimized and simulated using Cadence based on a 1.8V/0.18 μ m CMOS process from GlobalFoundries. The total power consumption (excluding output buffer) is only 18.39mW at a 1.8V voltage supply. The circuit obtains a differential gain of 46dB with a -3dB bandwidth of 1.9GHz as shown in Figure 6-15. The eye diagram in Figure 6-16 shows that the limiting amplifier operates well with a 1.25GHz (2.5Gb/s data rate) signal input. As compared to other designs with traditional offset compensation scheme, the proposed design is a fully integrated circuit block without any off-chip components, which leads to very small layout area. With compared to the offset compensation network design in [81], the proposed design has a significant reduction in circuitry complexity and power consumption. A figure-of-merit (FOM) [83] is used to compare the performance of the new design with the state-of-the-art limiting amplifiers reported in [79-81].

Figure 6-15: Schematic simulated AC response of proposed LA

Figure 6-16: Eye diagram showing the operation of the limiting amplifier

$$FOM = 20lg \left(\frac{Gain \cdot BW(GHz)}{Power(mW)} \right) = Gain(dB) + 20lg \left(\frac{BW(GHz)}{Power(mW)} \right) \quad (6-8)$$

The FOM indicates the gain-bandwidth product per unit power consumption, and the higher FOM means the higher circuit performance under unit power consumption [83]. Table 6-1 compares its circuit performance parameters with those reported in papers [79-81]. The FOM of the proposed limiting amplifier is 26.3 based on simulation results, while other compared designs are with measurement results. Although it may not be a fair comparison, the proposed limiting amplifier does show apparent advantages in power consumption and chip area. To accommodate in high speed systems, further research work can be carried on in extending bandwidth, which may bringing a power or area trade off. In general, the proposed offset compensation

network helps to achieve a fully integrated limiting amplifier with low cost in circuitry complexity.

Table 6-1: Comparison of various performance parameters and the FOM among 4 LA designs

	This work (simulation result)	[80]	[81]	[79]
Process	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Supply voltage	1.8V	1.8V	1.8V	2.4V
Power consumption (excluding buffers)	18.39mW	95mW	113mW	120mW
Operating data rate	2.5Gb/s	3.125Gb/s	3.125Gb/s	10Gb/s
Differential gain	46	45dB	42dB	30dB
-3dB bandwidth	1.9GHz	3.125GHz	5GHz	6.5GHz
Chip area (mm^2)	0.26	1.1696	1	0.39
FOM	26.3	15.34	16.42	4.67

Chapter 7. Conclusions and Future Work

In this thesis, the design challenges, tradeoffs, considerations and techniques for high-speed CMOS transimpedance amplifiers have been thoroughly reviewed and explored. A novel input structure based on cross-coupled current conveyor has been proposed. The new design has been analyzed in detail and it is backed by extensive simulation and measurement results. A limiting amplifier with fully integrated offset compensation network is proposed as well. These two circuit blocks form the analog front-end of a typical optical receiver. In this chapter, the current work in this thesis is concluded, and suggestions are given for the future research and design in the related field.

7.1 Conclusions

Reviewing various TIA topologies reveals that the major design challenge of a broadband TIA is brought by large capacitance of the photodiode at input terminal. A cross-coupled current conveyor based input stage has been proposed, providing very low input impedance. The proposed input stage relaxes the bandwidth limitation at input node effectively with simulated results showing less dependency of bandwidth on the input capacitance compared to other TIA topologies. As the dominant pole resides within the circuit, the transistor sizes need then to be carefully chosen for both transimpedance gain and bandwidth. Therefore, detail analysis of pole location has also been presented for this proposed structure. The noise characteristics of proposed TIA have then been studied in detail based on the Van der Ziel MOSFET noise model

mathematically. Capacitive degeneration technique is also employed to compensate the lower pole, extending the bandwidth. Additional bandwidth extension method shunt peaking is also used to achieve broad-bandwidth performance while maintain good gain flatness.

The proposed TIA has been implemented and fabricated using GlobalFoundries' 0.18 μ m 1.8V Industrial Compatible (IC) CMOS process technology. On-wafer measurements of the proposed TIA with single-ended termination demonstrates a 46dB Ω transimpedance gain with 4GHz bandwidth for a 0.25pF photodiode capacitance with an average input-referred noise current spectral density over 6GHz estimated to be $10\text{ pA}/\sqrt{\text{Hz}}$. The measurement results show great potential of proposed design for broadband optical communication system applications. Comparing with existing TIA designs in Chapter 5 Table 5-2, the proposed CMOS TIA shows apparent advantages in power consumption, noise performance and ease of implementing differential structures. However, the large deviations from schematic, post layout simulations to measured results suggest that improvement of layout is essential.

According to Table 5-2, CMOS technology gains significantly in terms of Gain-Bandwidth Product (GBP) due to its low power characteristic. This advantage increases tremendously with the down scaling of process technology. Taking the common-gate feedforward TIA design in [88] implemented in 80nm CMOS technology as example, it shows the largest GBP brought by the very low power consumption and excellent cut-off frequency characteristics of sub-100nm CMOS technology. With the down scaling trend, the improvement of performance in terms of

transistor cut-off frequency makes it an good candidate for low noise ultra low power broadband TIAs in high speed system. The proposed TIA design in this thesis can be easily employed in sub-100nm CMOS technology to enjoy the advantages of very high speed, ultra low power and improved high frequency noise performance.

Later portion of this thesis focused on design of limiting amplifier which is the second amplification stage following transimpedance amplifier in the receiver frontend. The limiting amplifier is nothing more than a series cascaded amplifying stages, therefore major design challenge is laid in the balancing and integrating part. A DC offset cancellation network is essential for limiting amplifier to avoid saturation of later stages caused by misbalancing of signals in early stage. The typical implementation of this offset compensation network employs a feedback path consisting of an RC low-pass filter (LPF) and an error amplifier. To achieve a low cut-off frequency, the LPF is usually implemented with off-chip large capacitors and resistors. A fully integrated DC offset compensation network has then been proposed by making use of DC generation circuit to sense mid values of positive and negative output signals separately and feed them back to input. The apparent advantage of limiting amplifier with the proposed DC offset compensation network is to get rid of off-chip components successfully. The gain cells in amplifying stages are implemented with active inductive load to achieve an inductor-less broadband amplifier. The simulated results were summarized in Chapter 6 Table 6-1 with comparison with existing limiting amplifier designs. The simulation results demonstrate highest figure-of-merits in terms of gain, bandwidth and power. Looking into performance parameters separately, the advantage mainly lies in lower power

consumption. The bandwidth of proposed limiting amplifier restricts it for application in high speed communication system beyond 5Gb/s.

In the next section, some recommendations on future work are given to further improve the proposed designs with the aim of building a high speed receiver front-end for optical communication system.

7.2 Future work

As the targeted indoor wireless communication system using white LED transmitting device is still in the intact stage of research, the specifications for the transimpedance amplifier are defined based on high speed optical communication system standards, so that the designed TIA has the potential for much wider applications. Ever since exchanging information using light starts in old times, the effort toward faster, more accurate optical communications is continuous and incessant especially after modern optical communications came into reality. With a mature and widely spread optical communication systems operating at 10Gb/s, higher speed and low cost system has drawn wide attention.

7.2.1 Future work for TIA

The transimpedance amplifier, the first amplifying stage in the optical receiver frontend, set limitations and render difficulties to the whole system design. Being one of the bottlenecks of the optical communication system, the future challenges and directions of TIA design will be higher speed, lower noise, higher integration and lower cost. For higher integration and lower cost purpose, CMOS technology is the

best candidate so far. However, SiGe or III-V technologies are definitely superior over CMOS when speed and noise are concerned.

The proposed cross-coupled input stage TIA design in this thesis shows great potential in applications in low power low noise systems. It proves to be a good candidate for 10Gb/s applications with a simulated bandwidth of 7.3GHz. Its post-layout simulation shows a 5.5GHz bandwidth, implying a layout optimization is needed. The large reduction in bandwidth after chip fabrication could be due to several factors, such as underestimation of parasitic effects, inaccurate simulation model and process variations, especially in on-chip spiral inductors. In addition, at very high frequency, the performance of the TIA can be severely affected by the parasitic elements, the probes used as well as the calibration and de-embedding techniques employed during on-wafer measurements. For example, from Figure 5-8, it can be seen that the peaking effect in the measured results is much less as compared to the simulation results. A substantial improvement in bandwidth is expected by implementing high Q inductors.

However, even with the above mentioned layout optimization and implementation of high Q inductors, the performance degradation from pre-layout simulation to measurement is inevitable. To achieve the targeted TIA bandwidth for 10Gb/s communication system in the same 0.18 μ m CMOS technology, guardband or over design may be necessary. That is a larger bandwidth should be targeted in simulation, for example 9GHz. As discussed in Chapter 5.4, as R_2 determines the overall gain, to have a larger dominate pole f_B in (5-29) by reducing R_2 is to scarify gain. Therefore the dominate pole f_B is relatively fixed, and in order to achieve a large

bandwidth, the pole introduced by capacitive degeneration is the one that can be played with. In (5-32), f_s is now targeted to be 9GHz instead of 6GHz, and then $g_{m6}R_s$ need to be set to 1 instead of 0.44. A larger transconductance g_{m6} requires larger current and thus larger power consumption.

Besides layout optimization, over design and so on, the proposed TIA could be employed in sub-100nm process technology which allows circuit to enjoy various advantages as mentioned in Section 7.1. However, additional design challenges come into picture. For example in sub-100nm process technology, the voltage headroom and the input overload current will be reduced. Next, the maximum cut-off frequency, which is usually measured when a device is biased under maximum supply voltage, becomes not practical. Last but not least, MOSFET in sub-100nm suffers from larger leakage current, leading to reduced gain [92]. All these problems need to be taken care of when transistors are cascaded in current-mode TIA designs.

7.2.2 Future work for limiting amplifier

As part of the receiver front-end, LA needs to provide not only a large gain for the proper operation of the CDR circuit, but also a wide bandwidth. The focus on LA design presented in this thesis is to study the possibility for inductor-less and integrated structure. The LA design proposed is a fully integrated structure by eliminating traditional off-chip RC components for DC offset compensation network. However, with a simple source follower as the active inductor in gain cells, the bandwidth of the proposed LA is only able to cater for lower data transmission rate instead of the targeted 10Gb/s for TIA. Another drawback of this active inductor is the

large voltage headroom consumption, especially when scaling down to sub-100nm MOSFET technology. Along with technology scaling down, the typical power supply also scales to 1.0V. However, by looking at the gain cells with active inductor implemented, the voltage drop across the active inductor is V_{gs} for transistor working in saturation region, making sub-1.0V voltage supply insufficient.

As active inductors are impractical with technology and supply voltage scaling down, for limiting amplifier, higher bandwidth is generally attained by implementing two on-chip spiral inductors for every stage. This is achieved at the expense of a larger chip area, which will result in higher fabrication cost. In addition, high Q factor on-chip spiral inductors at high frequencies are difficult to realize. Therefore, new techniques for bandwidth extension should be looked into and can be the focus area for further research to make the limiting amplifier suitable for high speed operation. High speed limiting amplifiers have been reported recently such as the one in [91].

With a larger bandwidth achieved, research work can also focus on exploring the possibility to implement the proposed DC offset compensation network on the high speed LA designs, as a fully integrated high speed limiting amplifier is a necessary block for a high speed optical receiver.

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