Study of degradation mechanism of metal nanocrystal-based gate stacks

Chen, Yining

2011

Chen, Y. (2011). Study of degradation mechanism of metal nanocrystal-based gate stacks.
Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/49981>

<https://doi.org/10.32657/10356/49981>

NANYANG
TECHNOLOGICAL
UNIVERSITY

**STUDY OF DEGRADATION MECHANISM
OF METAL NANOCRYSTAL-BASED GATE
STACKS**

CHEN YINING

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2011

STUDY OF DEGRADATION MECHANISM OF METAL NANOCRYSTAL-BASED GATE STACKS

CHEN YINING

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

A thesis submitted to Nanyang Technological University in partial fulfillment of
the requirement of the degree of Doctor of Philosophy.

2011

ACKNOWLEDGEMENTS

First and foremost, I would like to express my great gratitude to my research supervisor Professor Pey Kin Leong, for giving me this precious opportunity to pursue a higher degree in Nanyang Technological University, Singapore. I am deeply indebted to him for his constant guidance and support from the first day I arrived at this country. Prof. Pey has always been a role model to me scientifically, technologically and ethically. I consider myself privileged to work with such an outstanding and motivated professor.

I would like to express my sincere appreciations to my co-supervisor Dr. Johnson Goh Kuan Eng, Institute of Material Research and Engineering (IMRE), Singapore, and Dr. Michael Bosman, IMRE, Singapore for their guidance during the course of this thesis work.

I would like to thank Nanyang Technological University, Singapore for providing the research opportunity and research facilities. I would also like to thank Professor Souvik Mahapatra and Dr. Pawan Singh in Indian Institute of Technology Bombay, India for providing the metal nanocrystal-based memory devices.

Many thanks goes to the members of our research group, Dr. Lo Vui Lip, Dr. Li Xiang, Dr. Ong Yi Ching, Mr. Qin Hailang, Mr. Shubhakar Kayla, Mr. Liu Wenhui, Mr. Nagarajan Raghavan, Ms. Zin Zar Lwin and Ms. Wu Xing for their supporting and sharing of knowledge of me.

TABLE OF CONTENTS

Acknowledgements.....	i
Table of Contents.....	ii
Summary	viii
List of Figures.....	xi
List of Tables.....	xviii
List of Abbreviations	xix
List of Symbols	xxi
 Chapter One Introduction.....	 1
1.1 Background.....	1
1.2 Motivation	2
1.3 Objectives	3
1.4 Organization of Thesis	3
1.5 Contributions	4

Chapter Two	Literature Review	9
2.1	Introduction	9
2.2	Reliability of gate dielectric	10
2.2.1	Gate Dielectric Breakdown	10
2.2.2	Dielectric Relaxation Current	13
2.3	Reliability of NC-based Gate Stack	17
2.3.1	Charge Retention Property of Si NC-based Memory cell	17
2.3.2	Charge Retention Property of MNC-based Memory Cell	20
2.3.3	Leakage Current in the MNC-based Memory Cell.....	21
2.3	Resistive Switching Random Access Memory (RRAM).....	224
2.4	Summary.....	25
Chapter Three	Experimental Procedure and Details.....	29
3.1	Introduction	29
3.2	Sample Information and Equipments.....	29
3.3	Electrical Characterization methodology	37
3.3.1	Dual Voltage Sweep <i>I-V</i> Characterization.....	37
3.3.2	Relaxation Current Measurement	38
3.3.3	Capacitance-Voltage Technique	40

3.4 Stressing methodology	42
3.4.1 Calculation of Stressing Voltages (V_{stress}) for Constant Voltage Stress (CVS)	42
3.4.2 Successive CVS	44
3.4.3 Improved K-cycle multiple-stage CVS.....	46
3.5 Summary.....	49

Chapter Four Study of Relaxation Current in Single and Dual

Layer Metal Nanocrystal-based High- κ /SiO ₂ gate stack	52
4.1 Introduction	52
4.2 Experimental Details	53
4.3 Temperature-dependent Relaxation Current on Single and Dual layer Pt Metal Nanocrystal-based Al ₂ O ₃ /SiO ₂ Gate Stack	56
4.3.1 Temperature-dependent J_{relax} slope of SL and DL MNC-based gate stack samples	56
4.3.2. Role of MNC in relaxation current	60
4.3.3 Relaxation current as a reliability characterization tool	68
4.4 Summary.....	69

Chapter Five	Lateral Charging and Degradation of Single Layer Metal Nanocrystal-based High- κ /SiO ₂ Gate Stack	73
5.1	Introduction	73
5.2	Experimental Details	74
5.3	Lateral Charging in the Soft Breakdown Metal Nanocrystal-based High- κ /SiO ₂ Gate Stack	76
5.3.1	<i>I</i> - <i>V</i> Hysteresis Boost of Post-Soft Breakdown Ru Nanocrystal-based High- κ /SiO ₂ Gate Stack	76
5.3.2	Nanometer-scale Lateral Propagation of HBD Area	84
5.4	Summary	90
Chapter Six	Recovery of Post-breakdown In Single Layer Metal Nanocrystal-based High- κ /SiO ₂ Gate Stack	93
6.1	Introduction	93
6.2	Experimental Details	93

6.3	Polarity-dependent Electrical Recovery on Control and Tunnel Oxide Layers.	97
6.3.1	Application of Positive V_{RC} : Partial RC of SBD.....	97
6.3.2	Application of Negative V_{RC} : Full RC of SBD	100
6.3.3	Application Bipolar V_{RC} : Full RC of HBD	103
6.3.4	Proposed Physical Model of Electrical Recovery.....	106
6.3.4	Non-recoverability	109
6.4	Automatic RC.....	109
6.4.1	Automatic RC on I_{leak} of low I_{max} SBD	109
6.4.2	Thermal RC	111
6.4.3.	Physical Explanation of Automatic Recovery	113
6.6	Summary.....	116
Chapter Seven The Metal Nanocrystal-based High- κ /SiO ₂		
Charge-Trapping Gate Stack As A Resistive Switching Memory		
	Cell	119
7.1	Introduction	119
7.2	Experimental Details	121

7.3 Tri-level Resistive Switching of Metal Nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ Gate

Stack 122

7.4 Mechanism of Tri-level Resistive Switching129

7.5 Summary.....133

Chapter Eight Summary and Conclusions136

8.1 Conclusions136

8.2 Suggestions.....138

SUMMARY

This thesis focuses on the degradation and reliability mechanism of the metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stacks which is believed to be a promising candidate for next generation non-volatile memory. A series of novel approaches were used to obtain in-depth knowledge of the gate stack in terms of charge retention, gate dielectric breakdown and post-breakdown recovery. We also discuss the phenomenon of the post-breakdown recovery on the metal nanocrystal-based gate stack and the possibility of such charge-trapping gate stack as a candidate for a resistive switching memory cell.

For the study of the charge leakage of the metal nanocrystal, a simple but effective method of relaxation current measurement was adopted. The unique temperature dependent relaxation current behaviors of single and dual-layer platinum nanocrystal-based gate stacks that are much different from pure high- κ dielectric were investigated. The dual-slope in the relaxation current of the single-layer metal nanocrystal device was found to be due to two competing mechanisms of the metal nanocrystal-induced relaxation current. This quick characterization method of relaxation current measurement provides direct information of the short-term charge retention property of the metal nanocrystal-based devices.

For the study of the scalability of metal nanocrystal-based memory cell, the phenomenon of lateral charging of discrete metal nanocrystals was studied. In the single-layer ruthenium nanocrystal-based gate stack, an enhanced I - V hysteresis was realized when the stack suffered a soft breakdown. We propose that an increased lateral charge-trapping current through the breakdown path and lateral charge propagation are the origin. Through a series of nano-scale electrodes prepared by electric beam lithography for localized electrical characterization, it was

observed that the lateral charging of the metal nanocrystals eventually led to the lateral propagation of breakdown path under hard breakdown

To further enhance the reliability margin of the metal nanocrystal-based memory cell, partial or full recoveries of the leakage current and relaxation current of broken-down single-layer ruthenium nanocrystal-based gate stacks were studied for different breakdown hardness. The recovery of the dielectric properties of either the high- κ control oxide layer or the SiO_2 tunnel oxide layer was found to be dependent on the polarity of the recovery voltage. A physical model was established to explain the phenomena. Polarity-dependent annihilation of oxygen vacancies in the breakdown percolation path by oxygen ions released from the top metal electrode/oxide and metal nanocrystal/oxide interfaces is proposed as the recovery mechanism. Furthermore, an automatic recovery of leakage current was observed in the constant voltage stressing if we controlled the breakdown hardness at a relatively soft level. Control experiments at elevated temperature confirmed the temperature-related recovery behavior. Our findings suggest that high local temperature increase in the percolation path induced by Joule heating is responsible for the automatic recovery.

Furthermore, we explored the possibility of the metal nanocrystal-based charge-trapping memory cell to be used as a resistive switching memory cell. The soft breakdown (i. e., SET) and selective recovery (i. e., RESET) of the top and bottom dielectric layers in a metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack were successfully realized by an electrical method, giving rise to 3 distinct resistivity states. Bias-dependent oxygen vacancy annihilation in dielectric layers is proposed as the switching mechanism which makes a tri-bit resistive switching possible. This finding brings us new perspectives for the possible application of the metal nanocrystal-based high- κ/SiO_2 gate stack as a future non-volatile memory cell.

In summary, leveraging on novel approaches, the reliability and degradation mechanism of the metal nanocrystal-based memory cell were thoroughly studied. The finding of the recovery after breakdown extends the “reliability” margin of the metal-nanocrystal-based devices. An alternative application of the metal nanocrystal-based high- κ /SiO₂ memory cell is proposed.

LIST OF FIGURES

Figure	Caption	Page
2.1.	Cross-section of (a) Conventional floating gate memory device and (b) NC-based memory device.	8
2.2.	Schematic of a percolation path formed within the gate dielectric due to the accumulation of defects or electronic traps.	11
2.3.	Conduction band minimum up-shift of Si and Ge NC and Fermi-level up-shift of metal Ni NC as a function of the NC size.	13
2.4	(a) A particle in a double-well potential $V(x)$. The zero of $V(x)$ is the bottom of the upstream well, the top of the barrier is V_2 and the bottom of the downstream well is V_3 . (b) The effect of a potential of $-e\zeta_x$ on $V(x)$, with the dashed line being $V(x)$ and the solid line $V(x)-e\zeta_x$, the particle “fall” downstream in a manner describable by classical mechanics. (c) If the potential is not strong enough to eliminate the barrier, the particle can still switch wells by quantum-mechanical tunneling, and (d) particle can also switch wells by thermally hopping over the barrier.	14
2.5.	Band-diagram of a Si NC under (a) programming (b) erasing and (c) retention.	17
2.6.	Conduction band minimum up-shift of the Si and Ge NC and Fermi-level up-shift of metal Ni NC as a function of the NC size.	19
2.7.	Band diagram illustrating the work function engineering for MNC in (a) programming and (b) erasing.	20
2.8.	The impact of (a) control oxide material and (b) tunneling oxide thickness on retention time for SNCs and MNCs.	21
3.1.	Cross-sectional illustration of MNC-based MOS capacitor used in	27

	this study: (a) single layer MNC-based high- κ /SiO ₂ gate stack and (b) dual MNC-based high- κ /SiO ₂ gate stack.	
3.2.	Planar view of nano-dot electrode formed by EBL. (a) Schematic illustration and (b) SEM picture.	29
3.3.	Flow chart of nano Au/Cr electrode formed with EBL.	30
3.4.	(a) Suss PM8 200mm manual probe station and (b) Keithley 4200 Semiconductor Characterization System.	31
3.5.	Example of LEO 1550 Gemini Field Emission SEM.	32
3.6.	Components of Zyvex KZ100 Nanomanipulator/Prober: (a) Zyvex Nanomanipulator and (b) Controller.	33
3.7.	Typical dual voltage sweep curve on a single layer Ru-MNC-based gate stack, a hysteresis is observed.	35
3.8.	Typical relaxation current of after sudden removal of V_{ini} . The inset shows that the relaxation current vs. time curve is almost a straight line in double log scale.	36
3.9.	Typical C - V curve of a dual layer Pt-MNC-based gate stack under its fresh, programmed and erased condition.	38
3.10.	Voltage ramp to determine the BD voltage V_{BD} .	40
3.11	Successive CVS showing different progressive BD stage captured by I_{max} .	42
3.12.	Flow chart of an improved K-cycle multiple-stage constant-voltage stress.	44
4.1.	Schematic cross-sections showing dimensions of three samples (not to scale): (a) Control HK, (b) SL Pt MNC-based gate stack and (c) DL Pt MNC-based gate stack.	50
4.2.	TEM micrographs showing the cross section of (a) SL MNC-based gate stack and (b) DL MNC-based gate stack samples.	51

4.3.	Relaxation current density of the control HK sample at four different temperatures, the inset shows the slope n extracted from the respective curves.	53
4.4.	Relaxation current density of SL MNC-based gate stack sample at four different temperatures, the two insets shows the slope n extracted from curve fittings of the initial part and the tail part.	54
4.5.	Relaxation current density of the DL MNC-based gate stack sample at four different temperatures, the inset shows the slope n extracted from the respective curves.	55
4.6.	(a) J_{10s} and (b) J_{60s} of control HK, SL MNC and DL MNC samples at four different temperatures.	57
4.7.	Band diagram of SL MNC-based gate stack sample when (a) under V_{ini} , programming current consisting of both thermionic emission J_1 and quantum tunnelling J_2 charges the MNCs, (b) under zero bias ($t = 0$, beginning of J_{relax} measurement), charges leak out of MNCs to Si substrate, J_1 and J_2 comprise J_{relax} .	58
4.8.	Band diagram of DL MNC-based sample when (a) under V_{ini} , programming current consisting of both thermionic emission J_1 and quantum tunnelling J_2 charges the MNCs, (b) under zero bias ($t = 0$, beginning of J_{relax} measurement), not only the electrons of MNC1, but also MNC2 electrons can quantum mechanically tunnel to the Si substrate to form J_2 ; nevertheless, J_1 can only come from the excess electrons in MNC1 because of the non-directional property of thermionic emission. Thus a more dominant role of J_2 is expected in J_{relax} of the DL MNC-based gate stack sample.	59
4.9.	Discharge time constant τ of the SL and DL MNC-based gate stacks at four temperatures. SL and DL sample show different trend as T increases. DL samples have larger τ at all temperatures.	64
5.1	Cross-sectional schematic of devices with a similar leakage path in the bottom tunnel oxide in case of (a) a traditional floating gate	68

	memory cell and (b) a NC-based memory cell.	
5.2	(a) Cross-sectional TEM and (b) planar view TEM [4] of SL Ru MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack.	69
5.3.	Dual sweep showing (a) I - V hysteresis on a fresh sample. The arrows show the sweep directions. Current difference I_{dif} is defined as value difference between the positive and the negative direction sweep. (b) I_{dif} between the positive and negative sweep.	72
5.4.	Dual sweep showing (a) I - V hysteresis on fresh and SBD samples. The smaller arrows show the sweep directions. The hysteresis of the SBD sample shows larger window than the fresh one. (b) I_{dif} between the positive and negative sweep. Steady-state I_{dif} of the SBD samples is more than two orders larger than the fresh one.	73
5.5.	Relaxation current of the fresh and SBD samples. The similarity of these two curves suggests that the SBD sample experienced an one-layer (SiO_2) BD.	74
5.6.	(a) Cross-sectional illustration shows that in the post-SBD sample, leakage current flows through the percolation path in the tunnel oxide, local electric field is created between the charged and uncharged MNC. (b) Band diagram shows that the local electric field causes electron charging in the MNC laterally.	75
5.7.	Dual sweep showing (a) I - V hysteresis of the fresh and HBD samples. The smaller arrows show the sweep directions. The HBD sample shows no hysteresis. (b) I_{dif} between the positive and negative sweep. I_{dif} of the HBD is much smaller than the fresh one.	77
5.8.	Nanometer-scale probing on Au/Cr nanometer-scale electrode with a W probe under SEM.	79
5.9.	SEM micrograph showing nanometer-scale Au/Cr electrodes with same area but different spacings.	80
5.10.	After the CVS ($V_{stress} = 6.5\text{V}$, and $I_{max} = 5\mu\text{A}$) on nanometer-scale electrode D2, the dual voltage sweep curve shows HBD behavior. The dual sweep of an un-stressed D1 which is 30nm away to the left	81

	of the BD dot (D2) shows a HBD characteristic. For another un-stressed nanometer-scale dot D3 which is 60nm away to the right of the BD dot, a SBD curve is observed. All dots are of 200nm in diameter.	
5.11.	After CVS ($V_{stress} = 6.5V$, and $I_{max} = 5\mu A$) on D5, the dual voltage sweep curve shows HBD behavior. The dual sweep of an un-stressed nanometer-scale electrode D4 which is 120nm away to the left of the BD dot shows a SBD-like behavior. For another un-stressed nanometer-scale electrode D6 which is 150nm away to the right of the BD dot (D5), a fresh-like curve is observed. All dots are of 200nm in diameter.	82
6.1.	(a) TEM micrograph showing the cross-section of gate stack gate stacks with Ru MNCs embedded above the Al_2O_3/SiO_2 interface. (b) Planar TEM showing the individually embedded MNCs.	88
6.2.	The plot of leakage current I_{leak} under constant voltage stressing of V_{stress} . A compliance current limit I_{max} was used to arrest the stack under different BD hardness.	92
6.3.	Partial RC of SBD with positive RC voltage (a) $ I_{leak} @ V_{bias} = 2V$ (the insets show the existence of hysteresis in the fresh sample, but not in the BD sample) (b) I_{relax} of the fresh gate stack, after BD and after RC. The BD event used $V_{stress} = -6.5V$ and $I_{max} = 200nA$. The RC event used $V_{RC} = +4V$.	93
6.4.	Full RC of SBD with negative RC voltages: (a) $ I_{leak} @ V_{bias} = 2V$ (the inset shows that the fully recovered $I-V$ resembles fresh device), (b) I_{relax} of fresh device, after BD and after RC; $V_{stress} = +6.5V$, $I_{max} = 200nA$ and $100nA$, respectively in BD1 and BD2. $V_{RC} = -4V$ in both RC1 and RC2.	96
6.5.	Full RC of HBD with RC voltages of both polarity: (a) $ I_{leak} @ V_{bias} = 2V$ (the inset shows that the fully recovered $I-V$ resembles the fresh sample). (b) I_{relax} of fresh device, after BD and after RC; the BD1 and BD2 used $V_{stress} = +6.5V$, $I_{max} = 10\mu A$ and	99

	5 μ A, respectively. RC1 ($V_{RC} = -4V$) and RC2 ($V_{RC} = +4V$) were performed after BD1 and RC3 ($V_{RC} = -4V$) was performed after BD2.	
6.6.	Schematic models showing the Au electrode/ Al_2O_3 (with embedded MNCs)/ SiO_2 /Si substrate gate stack at (a) fresh condition, (b) BD condition (c) negative V_{rec} , leading to minor and major V_o annihilation in Al_2O_3 and SiO_2 layers respectively, and (d) positive V_{rec} providing V_o annihilation only in Al_2O_3 layer.	102
6.7.	Room temperature constant voltage stressing ($V_{stress} = 6.5V$) with different I_{max} . (a) $I_{max} = 10nA$, auto-recovery of I_{leak} back to the pre-stress current level after the BD1 and BD2. (b) $I_{max} = 10nA$, auto-recovery of I_{leak} back to the pre-stress level is observed only after the BD1, and automatic partial recovery found after the BD2. (c) $I_{max} = 100nA$, automatic partial recovery is observed after the BD1, no recovery after the BD2. The inset shows the detailed I_{leak} behavior.	104
6.8.	Device characterization at room and elevated temperatures (Sample used was the capacitor stack broken down beyond auto-recovery in 6.7(c)). (a) Capacitor leakage current $I_{leak}@V_{bias}=2V$ shows significant reduction after going through higher temperature (125°C and 225°C) anneal, and the final I_{leak} at room temperature is almost one order higher than the pre-stress level; (b) a full RC of I_{relax} is observed after the high temperature anneal, suggesting significant passivation of the BD percolation path in the Al_2O_3 high- κ layer.	106
6.9.	Schematic illustration of the conduction band diagram in Au electrode/ Al_2O_3 , MNC/ Al_2O_3 and MNC/ SiO_2 interfaces at elevated temperatures, showing thermally agitated O^{2-} de-trapping from the metal/oxide interfaces to passivate the neighbor V_o in the BD percolation path. Note that there are two sources providing kinetically mobile O^{2-} to the Al_2O_3 layer, but only one source for the BD path in SiO_2 , indicating a higher recoverability of the Al_2O_3 layer for the same BD hardness. The dashed and solid lines indicate the	110

	original (before BD) and lowered barrier height (after BD) for O^{2-} ions.	
7.1.	Classification of the switching characteristics in a voltage sweeping experiment. (a) Unipolar switching. The SET voltage is higher than the voltage that RESET takes place, and both voltages are of same polarity. CC is the compliance current limit. (b) Bipolar switching. The SET operation takes place on one polarity and the RESET operation requires the opposite polarity. CC is the compliance current limit [6].	114
7.2.	Typical resistive switching in 3 successive voltage sweep tests: SBD (forming process) at +6.5 V in sweep1; negative RESET at -4.3 V in sweep2; positive RESET and SET at +4.45 V and +6.35 V respectively in sweep3.	117
7.3.	Resistive switching between 3 states: (a) leakage current showing the resistance of the gate stack (b) relaxation current (after a 3V initializing voltage stressing for 5s) indicating the insulating property of the Al_2O_3 high- κ layer.	119
7.4.	Resistance vs. switch steps of the MNC-based Al_2O_3/SiO_2 gate stack.	121
7.5.	Cross-section schematics illustrating the resistive switching mechanism under (a) fresh condition (HRS1); (b) forming/SET voltage (LRS1), (c) positive RESET voltage (MRS1) and (d) subsequently negative RESET voltage (HRS2).	125
7.6.	A 0 to -2V voltage sweep on a MNC-based gate stack with unstable resistance state resulting from applying a only a V_{RESET} .	127

LIST OF TABLES

Figure	Caption	Page
3.1	List of I_{max} for each cycle CVS stress to control the BD hardness.	45
7.1	Switching conditions for the 3 resistance states.	123

LIST OF ABBREVIATIONS

DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
P/E	Programming/Erasing
SILC	Stress-Induced Leakage Current
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NC	Nanocrystal
NVM	Non-Volatile Memory
BTI	Bias-Temperature Instability
TDDDB	Time-Dependent Dielectric Breakdown
EBIC	Electron-Beam Induced Current
MNC	Metal Nanocrystal
FN	Fowler-Nordheim
MONOS	Metal-Oxide-Nitride-Oxide-Silicon
BD	Breakdown
ITO	Indium-Tin Oxide
EOT	Equivalent Oxide Thickness
RRAM	Resistive Switching Random Access Memory
MIM	Metal Insulator Metal
VCM	Valence Change Mechanism
ECM	Electrochemical Metallization Mechanism
LRS	Low Resistance State
HRS	High Resistance State
MRS	Medium Resistance State
RC	Recovery
RTP	Rapid Thermal Process
PVD	Physical Vapor Deposition
SL	Single Layer

DL	Dual Layer
ILD	Inter-Layer Dielectric
EBL	Electron-Beam Lithography
TEM/EELS	Transmission Electron Microscopy/Electron Energy Loss Microscopy
SMU	Source-Monitor Unit
CVS	Constant Voltage Stressing
MRAM	Magneto-resistive Random Access Memory
PCRAM	Phase-change Random Access Memory
HK	High- κ
I_{leak}	Leakage Current
I_{relax}	Relaxation Current
J_{relax}	Relaxation Current Density
I_{max}	Compliance Current Limit
V_{SET}	Set Voltage
V_{RESET}	Reset Voltage
V_{RC}	Recovery Voltage
V_{stress}	Stressing Voltage
$V_{\text{stress_nano}}$	Stressing Voltage on Nanometer-scale Electrode
V_{ini}	Initial Voltage
t_{stress}	Stressing Time
t_{BD}	Time-to-breakdown
T	Temperature

LIST OF SYMBOLS

A	ampere
F	farad
μ	micro
κ	dielectric constant
K	Kevin
eV	electron volt
Ω	ohm

CHAPTER ONE

INTRODUCTION

1.1 Background

The semiconductor industry has followed Gordon Moore's prediction that the transistor's performance and density doubles every 3 years [1], which is well known as Moore's Law. Aggressive scaling of the semiconductor memory cells and the dramatic increase in the memory array sizes demand a high density, low cost, and low power consumption cell structure. It is difficult to scale a DRAM (Dynamic Random Access Memory) cell with a large capacitor. Due to their short retention time (less than a few seconds [2]), DRAM requires frequent refreshing which results in large power consumption. Flash EEPROM (Electrically Erasable Programmable Read-Only Memory) does not require refreshing and thus consumes less power and may achieve much larger array density with stacked floating gate structure. However, Flash EEPROM suffers from slow Programming/Erasing (P/E) speed and poor endurance. In order to improve the P/E speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. To achieve a 100ns P/E, the tunnel oxide must be less than 2nm thick in order to achieve a reasonable programming voltage ($<10\text{V}$) [3]. Unfortunately, the retention time will be too short then. Stress-induced-leakage-current (SILC) [4] will further degrade the retention time. Currently, commercial floating gate memory devices use tunnel oxides thicker than 8nm to guarantee ten years retention time, which results in high programming/erasing (P/E) voltage and slow P/E speed.

In 1996, Metal-oxide-semiconductor field effect transistor (MOSFET) structure memories employing silicon nanocrystals (NC) was proposed to meet the challenge of the scaling limits of traditional floating gate non-volatile memory (NVM) by Tiwari *et al.* [5]. It is believed that by utilizing a discrete nanocrystal memory structure, the serious leakage problem in conventional floating gate memory devices during retention could be eliminated. Hence the tunnel oxide in the nanocrystal memory device can be reduced to allow faster P/E and also lower operation voltage (lower power dissipation). Various techniques have been developed to fabricate nanocrystal memory device adopting semiconductor (e.g. Si [6] and Ge [7]) nanocrystals. A few issues with semiconductor NC that have been widely noted are small work function (thus weak charge-holding capability), quantum confinement leading to Fermi Level pinning [8] and poor control over the NC size which results in poor overall performance. However, metal-based nanocrystals (MNC) excels over their semi-conductor counter parts in having higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of available work functions, and smaller energy perturbation due to carrier confinement.

1.2 Motivation

The reliability of gate dielectric has been an intensively research topic for more than three decades, especially when the device dimensions are continuously scaled down. Presently, high- κ gate dielectrics are aggressively developed to replace SiO_2 in order to reduce gate leakage currents in future CMOS generations. Intensive reliability studies, such as threshold voltage instability [9] bias-temperature instability (BTI) [10], time-dependent dielectric breakdown (TDDB) [11], Electron-Beam Induced Current (EBIC) [12], etc., are carried out to understand the degradation and breakdown mechanism of the new kind of gate stacks. However, there is

limited research on the reliability issues of MNC-based high- κ /SiO₂ gate stack as non-volatile memory candidate. At this juncture, more detailed and systematic understanding on the degradation and breakdown issues of the MNC-based high- κ /SiO₂ gate stack are required for the future design and development of the next generation NVM devices.

1.3 Objectives

The objective of this project is to study the degradation and failure mechanism of MNC-based high- κ /SiO₂ dual layer dielectric gate stack for the candidate of next generation NVM device.

1.4 Organization of Thesis

This thesis is divided into seven major chapters. The organization is as follows:

- *Chapter One* provides the background, motivation, objectives and contributions of this project.
- *Chapter Two* is a literature review on the research work that has been reported for degradation mechanism of conventional high- κ /SiO₂ gate stacks as well as for the charge retention and charge leakage mechanism of MNC-based high- κ /SiO₂ gate stacks. We also briefly review the development of a new NVM concept, the resistive switching memory.
- *Chapter Three* provides the procedure and the details of experiments that are carried out in our studies.
- *Chapter Four* is the detailed study of the origin of the relaxation current and its application as a reliability tool for single and dual layer Pt MNC-based high- κ /SiO₂ gate stack.

- *Chapter Five* presents several novel degradation mechanisms in the single and dual layer Pt MNC-based high- κ /SiO₂ gate stack.
- *Chapter Six* provides a comprehensive study of the electrical and automatic post-breakdown recovery on the single layer Ru MNC-based high- κ /SiO₂ gate stack.
- *Chapter Seven* presents a study of the single layer Ru MNC-based high- κ /SiO₂ gate stack as a possible candidate for resistive switching memory.
- *Chapter Eight* provides the conclusions and the future extensions of this project.

1.5 Contributions

Our studies provide unique insights into the novel characteristics of MNC-based high- κ /SiO₂ gate stack through a series of reliability studies. A simple method of relaxation current measurement was adopted to study the charge leakage of nanocrystals. The unique temperature dependent relaxation current behaviors of single and dual-layer Pt nanocrystal-based gate stack were investigated. The dual-slope in the relaxation current of the single-layer MNC device is explained by the two competing mechanisms of the MNC-induced relaxation current. It is proposed that at the early stage of the relaxation current, thermionic emission current is the dominant source and at the late stage quantum mechanical tunneling current takes the dominance. Whereas in the dual-layer MNC-based stack, the quantum mechanical tunneling current is always dominant, giving rise to an exponent-linear relationship of the temperature-dependent relaxation current behavior. The simple method of relaxation current provides direct information on the short-term charge retention property of the MNCs.

In order to study the main advantage of the MNC-based based high- κ /SiO₂ gate stack which is the discreteness of the charge trapping media, the phenomena of lateral charging of the

MNCs were studied. In the single-layer Pt nanocrystal-based gate stack, an enhanced I - V hysteresis was realised when the stack reached a soft breakdown. We propose that an increased lateral charge-trapping current through the breakdown path and the lateral charge propagation are the origin. We also prepared nano-level electrodes by electric beam lithography for nano-scale localized electrical characterization. It was observed that the lateral charging of the MNCs eventually leads to the lateral propagation of breakdown path under hard breakdown. The lateral charging among MNCs is a major issue for the scaling of this kind of memory cell.

To further study the failure and degradation mechanism, we expanded our study to the post-breakdown stage. We studied the post-breakdown behavior using a small work function metal ruthenium as the nanocrystal material. Partial or full recoveries of leakage current and relaxation current were observed for different breakdown hardness if we stressed the broken down ruthenium nanocrystal-based high- κ /SiO₂ gate stack with a small voltage with certain polarity. The recovery on the dielectric properties of either the high- κ control oxide layer or the SiO₂ tunnel oxide layer was found to be dependent on the polarity of the recovery voltage. A physical model is proposed to understand this. Polarity-dependent annihilation of oxygen vacancies in the BD percolation path by oxygen ions released from the gate/oxide and MNC/oxide interfaces is proposed as the recovery mechanism. Furthermore, an automatic recovery of leakage current was observed in the constant voltage stressing if we controlled the breakdown hardness at a relatively soft level. Control experiments at elevated temperature confirmed the temperature-related recovery behavior. Our findings suggest that high local temperature increase in the percolation path induced by Joule heating is responsible for the automatic recovery. During the recovery process, the oxygen-vacancy annihilation in the percolation path was facilitated by the thermally agitated oxygen ions that were stored in the metal electrode/Al₂O₃ and ruthenium MNC/oxide

interfaces upon the removal of the stressing electric field. The recovery behavior offers extra reliability margin for the MNC-based gate stack.

In the last part of the study, we explored the possibility of using the MNC-based gate stack and a candidate for the resistive switching memory cell. The soft breakdown (i. e., SET) and selective recovery (i. e., RESET) of the top and bottom dielectric layers in a metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack was successfully realized by an electrical method, giving rise to 3 distinct resistivity states. Oxygen ions de-trapping from the metal-oxide interfaces (including metal nanocrystal/oxide interfaces) which serve as oxygen ion reservoir, and passivating back with the oxygen vacancies in the dielectric breakdown percolation paths is proposed to be the reason of the tri-level transition of the resistance state of the metal nanocrystal-based gate stack. Gate bias dependent oxygen vacancy annihilation in dielectric layers is proposed as the mechanism which makes the electrical tri-bit resistive switching possible. This finding brings us new perspectives for the possible application of the metal nanocrystal-based high- κ/SiO_2 gate stack as future non-volatile memory cell.

The above work has been published in world-recognized conferences, which are *IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)* and *International Conference on Solid State Devices and Materials (SSDM)*, as well as prestigious journals, such as *Applied Physics Letters (APL)* and *Transactions on Electron Devices (TED)*.

References

- [1] Moore, G., "Progress in digital integrated electronics," *IEDM Tech. Dig.*, 1975(21): p. 11.
- [2] R. Divakaruni, B. El-Kareh and W.R. Tonti., "Device design methodology and reliability strategy for deep sub-micron technology," in *IEEE International Integrated Reliability Workshop*. 1997. Lake Tahoe, Ca.
- [3] Y.C. King, , "Thin dielectric technology and memory devices." *Dissertation Abstracts International*, Volume: 60-05, Section: B, page: 2265.; 136 p., 1999, University of California, Berkeley: United States -- California.
- [4] B. Ricco, G. Gozzi and M. Lanzoni "Modeling and simulation of stress-induced leakage current in ultrathin SiO₂ films," *Electron Devices, IEEE Transactions on* , vol.45, no.7, pp.1554-1560, Jul 1998.]
- [5] S. Tiwari, "Silicon nano-crystal memories: Devices in the limit of conventional miniaturization," in *3rd International Symposium on the Physics and Chemistry of SiO₂ and the Si-SiO₂ Interface. at the Spring Meeting of the Electrochemical-Society*. 1996. Los Angeles, Ca.
- [6] A. Dutta, M. Kimura, Y. Honda, M. Otobe, A. Itoh and S. Oda,, et al. "Fabrication and electrical characteristics of single electron tunneling devices based on Si quantum dots prepared by plasma processing," in *4th International Colloquium on Scanning Tunneling Microscopy*, Kanazawa, Japan,1996.
- [7] J.H. Chen, Y.Q. Wang, W.J. Yoo, Y.C. Yeo, G. Samudra, D. Chan, A.Y.Du and D.L. Kwong, , "Nonvolatile flash memory device using Ge nanocrystals embedded in HfA10 high-kappa tunneling and control oxides: Device-fabrication and electrical performance," *IEEE Transactions on Electron Devices*, 2004. 51(11): p. 1840-1848.
- [7] Schroder, D.K. and J.A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *Journal of Applied Physics*, 2003. 94(1): p. 1-18.
- [8] K. Shiraishi, Y. Akasaka, G. Nakamura, M. Kadoshima, H. Watanabe, A. Ohta, S. Miyazaki, K. Ohmori, T. Chikyow, K. Yamabe, Y. Nara, Y. Ohji, and K. Yamada, "Theoretical studies on fermi level pinning of Hf-based high-k gate stacks based on thermodynamics", *ECS Transactions - 5th International Symposium on High Dielectric Constant Materials and Gate Stacks*, v 11, n 4, p 125-133, 2007,]

- [9] C.M. Compagnoni, C. Miccoli, R. Mottadelli, S. Beltrami, M. Ghidotti, A.L. Lacaita, A.S. Spinelli, and A.Visconti, "Investigation of the Threshold Voltage Instability after Distributed Cycling in Nanoscale NAND Flash Memory Arrays," *2010 IEEE International Reliability Physics Symposium (IRPS 2010)*, p 604-10, 2010.],
- [10] D.K. Schroder, and J.A. Babcock, "*Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing*," *Journal of Applied Physics*, 2003. 94(1): p. 1-18.
- [11] J.W. McPherson, and H.C. Mogul, "Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in SiO₂ thin films," *Journal of Applied Physics*, 1998. 84(3): p. 1513-1523.
- [12] J. Chen, T. Sekiguchi, N. Fukata, M. Takase, R. Hasunuma, K. Yamabe, M. Sato, Y. Nara, K. Yamada and T. Chikyo, "Trap-Related Carrier Transports in p-Channel Field-Effect Transistor with Polycrystalline Si/HSiON Gate Stack," in *International Conference on Solid State Devices and Materials*. 2008. Tsukuba, JAPAN.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

There are two main categories in memory: volatile and nonvolatile. Volatile memory loses any data as soon as the power supply is turned off. Hence it requires constant power to remain viable. Most types of random access memory (RAM) fall into this category. Nonvolatile memory (NVM) does not lose its data when the system or device is turned off. A nonvolatile memory device is a MOS transistor that has a source, a drain, an access or a control gate, and a floating gate. It is structurally different from a standard MOSFET in its floating gate, which is electrically isolated, or "floating".

Figure 2.1. Cross-section of (a) Conventional floating gate memory device and (b) NC-based memory device.

The NC-based MOS structure memories, first introduced in 1996 [1], was are based on a charge trapping non-volatile memory device. There are two categories of the NC material: semiconductor NC and MNC. The NC-based NVM is one of the most promising candidates for future flash memory device, as the conventional floating gate NAND Flash has hit its scaling bottleneck [2]. A typical NC based NVM device is shown in Fig. 2.1 (b). Compared to the conventional floating gate memory cell [(Fig. 2.1(a)], the tunneling oxide could be much thinner, allowing more significant Fowler-Nordheim (FN) tunneling when the control gate is under positive bias (programming) or negative bias (erasing) and thus faster program/erase rates. NC memory devices can be seen as an evolution of the MONOS (metal-oxide-nitride-oxide-silicon) device where the whole nitride layer which acts as the charge storage layer is replaced by discrete semiconductor or metal nanocrystals, so that better immunity to gate oxide defects, and better retention characteristics may be achieved. In the conventional floating-gate flash memory, if there is just one defect chain across the tunnel oxide, all of the charges stored on the floating-gate will leak back to either the channel or the source/drain through the defect chain. This serious leakage problem which threatens data retention is supposed to be eliminated by utilizing a discrete nanocrystal memory structure. Only the electrons stored in the nanocrystal directly above the defect chain will be affected since the nanocrystals are separated from each other by the gate oxide dielectric.

2.2 Reliability of Gate Dielectric

2.2.1 Gate Dielectric Breakdown

One of the most severe problems in the reliability of the MOS structure gate stack-based memory device is the dielectric breakdown (BD) of the gate oxide (either tunnel oxide or control oxide), which leads to a considerably huge gate leakage current and loss of information.

Dielectric BD is generally defined as the loss of the insulating properties of the oxide. In other words, the occurrence of a dielectric BD event corresponds to a substantial decrease in the resistances of some of the local areas in gate dielectric. J. Sunê *et al.* [3] first reported the simulations of a percolation approach to model gate dielectric BD in the thin film of silicon dioxide. In this work, spheres with the radius of a_0 , which are defects generated during the electrical stressing, are randomly placed in a three-dimensional matrix that represents the covalent network of silicon dioxide. The statistical distribution of sphere or defect densities that permits the formation of a conductive channel within the gate oxide can be determined. At a given sphere or defect density, a dielectric BD event will occur with higher probability with decreasing thickness. In addition, the spread of dielectric breakdown distribution is larger in thinner gate oxides. Both of these behaviors are in good agreement with experimental observations.

Fig. 2.2 [4] shows the general schematic of a percolation path formed within the gate oxide due to the accumulation of defects or electronic traps. The gate and the silicon substrate are electrically connected with each other, allowing the flow of a huge amount of electrons from the cathode to the anode.

J. H. Stathis [5] further developed the percolation model to very thin gate oxide for which the critical defect density becomes independent of thickness. According to Stathis, the percolation model with a non-uniform distribution of defective sites may be a more appropriate

model for dielectric breakdown events where defects are preferentially generated near the substrate and the gate electrode.

The application of percolation concepts and theories to dielectric BD may be traced to the observations of fractal-like electrical discharge patterns [6, 7]. These patterns could be reproduced through the numerical simulations of bond percolation on a two-dimensional lattice, in which it was assumed that the growth probability of these patterns depends on the local electric field. A similar approach was recently used to model the time-to-breakdown of thin gate dielectric situated in between two conductors [8]. In this approach, dielectric BD takes place when the cluster of connected bonds grows from one interface to another.

Figure 2.2. Schematic of a percolation path formed within the gate dielectric due to the accumulation of defects or electronic traps [4].

In 2008, our group unveiled the chemical nature of the percolation path in gate dielectric of SiO₂ [9, 10], showing that the physical defects in the percolation path are related to oxygen deficiencies. The oxygen deficiency spreads out radically from the center of the percolation path to its surrounding area. The Si/O composition changes from SiO_{1.76} to SiO_{0.7} while moving from the centre of the percolation path towards outside of the percolation path, which corresponds to a lowering of the SiO₂ conduction band minimum from 0.14eV to 0.78eV.

The percolation theory and the elucidation of the chemical nature of the percolation path provided a major impetus toward a comprehensive understanding of the breakdown in gate dielectric.

2.2.2 Dielectric Relaxation Current

One approach to study the reliability of the gate dielectric is via the dielectric relaxation current (I_{relax}) measurement. Dielectric relaxation is a bulk-related general phenomenon. A typical dielectric relaxation happens when a sudden voltage change is applied to a dielectric, and the resulting current follows the direction of dV/dt . It has been detected in polycrystalline, disordered, or amorphous films but not in single-crystal dielectric [11]. As the dielectric film normally has very low conductivity, the relaxation is a slow process in which the relaxation current decays with time, following the Curie-von Schweidler law [12]:

$$I_{relax} = at^{-n} \quad (2.1)$$

where I_{relax} is the relaxation current, a is a constant, and n is a real number close to 1.

Figure 2.3. Conduction band minimum up-shift of Si and Ge NC and Fermi-level up-shift of metal Ni NC as a function of the NC size [12].

Figure 2.3 compares the relaxation currents of different high- κ dielectric film with respect to SiO_2 [12]. The relaxation current was normalized to the surface charge density. It is obvious that all high- κ films had relaxation currents one to two orders of magnitude larger than that of SiO_2 . This is expected because high- κ dielectrics generally have lower crystallinity and more defects compared to SiO_2 . The metal-oxygen bonds lack symmetry, so dipoles are easily created in high- κ dielectrics, resulting in larger relaxation current. In fact, the highly polarizable bonds are a reason for larger dielectric constants as well, since they can screen the external electric field [13]. The slope of the relaxation current vs. time varies from materials to material, but all are near value of one.

The main mechanism of relaxation current could be explained by the material polarization model [14] and charge model [15]. The polarization model claims that external electric field applied on a dielectric film separates the bound charges, resulting polarization and a compensating internal field. At the moment the external electric field is released, the bound charges are neutralized by the hopping of free charges while a remnant polarization and internal field still remain in the film, resulting in a time-decaying remnant current. The charge model is similar except that it attributes the relaxation current to the electron trapping and de-trapping in the high- κ dielectric. In fact, it is almost impossible to distinguish the polarization induced current with charge trapping/de-trapping induced current. It is natural to ask which explanation is correct, but in fact the two mechanisms might not be physically distinct, because the lack of spin resonance in dielectric glasses suggests that if charge is being trapped, it is being trapped in pairs, presumably in the negative-U centers described by Anderson [16]. Then, the motion of an electron pair, with its accompanying atomic motion, could be called an atomic rearrangement with an appropriately chosen local dipole. In the case of either charge trapping or polarization, the important point is that an atomic mass enters the problem, and we proceed by describing the atomic rearrangements as a particle in a double well, with the two wells representing the configurations of the atoms before and after the rearrangement.

This double well picture of dielectric relaxation current was first suggested by Anderson *et al.* [18] and Phillips [19] in 1972, following the discovery [20] that a universal property of glasses is a specific heat linear in T , in contrast to the T^3 dependence of the perfectly insulating crystals. They pointed out that a collection of two-level systems will have a linear specific heat if it contains a finite density of systems with zero energy splitting. They imagined that the atomic

disorder in dielectric allows some atoms or groups of atoms to have more than one local equilibrium position, which they represented as a particle in a double well like that in Fig. 2.4(a). At sufficiently low temperatures, the particle is in either the ground state or the first excited state of the double well, and in this sense it is a two-level system. Then, atomic disorder could produce a distribution of energy splitting extending all the way to zero energy. J. R. Jameson *et al.* [21] further optimized the double well model for dielectric to describe the relaxation current in a systematic way. An electric field ξ adds a term $-e\xi_x$ to the potential, which distorts the double well as in Fig. 2.4(a), shifting the “upstream” well by an energy of $\mu\xi/2$ and the “downstream” well by $-\mu\xi/2$. If it is sufficiently large, as shown in Fig. 2.4(b), the barrier disappears, causing the particle to “fall” downstream in a manner describable by classical mechanics. If the field is not strong enough to eliminate the barrier, the particle can still switch wells by quantum-mechanical tunneling, as in Fig. 2.4(c). For this to happen, the field must “invert” the double well, making its upstream well higher than its downstream well. It is also possible for the particle to switch wells by thermally hopping over the barrier, as shown in Fig. 2.4(d).

Figure 2.4. (a) A particle in a double-well potential $V(x)$. The zero of $V(x)$ is the bottom of the upstream well, the top of the barrier is V_2 and the bottom of the downstream well is V_3 . (b) The effect of a potential of $-e\xi_x$ on $V(x)$, with the dashed line being $V(x)$ and the solid line $V(x) - e\xi_x$, the particle “fall” downstream in a manner describable by classical mechanics. (c) If the potential is not strong enough to eliminate the barrier, the particle can still switch wells by quantum-mechanical tunneling, and (d) particle can also switch wells by thermally hopping over the barrier [17].

2.3 Reliability of NC-based Gate Stack

2.3.1 Charge Retention Property of Si NC-based Memory Cell

At the introduction of Si nanocrystal in 1996, Tiwari et al. [1] have introduced the formula for the threshold voltage shift of Si NC memory device due to the stored electrons:

$$\Delta V_t = \frac{npq}{\epsilon_{ox}} \left(t_{control} + \frac{\epsilon_{ox} t_{nc}}{2\epsilon_{si}} \right) \quad (2.2)$$

where n is the number density of nanocrystal, p is the average number of electrons which are stored per nanocrystal, q is the elementary electronic charge, ϵ_{si} and ϵ_{ox} are the medium permittivity of Si NC and tunnel dielectric, t_{nc} is the average diameter of nanocrystal and $t_{control}$ is the thickness of control dielectric. Given a fixed number density of electrons, np , susceptibility of the Si NC device to the isolated defects in the tunnel dielectric is mitigated by using a larger n ,

density of the NCs and a smaller p , the number of electrons stored in one Si NC. From the above equation, it is also clear that a greater n and p will be desirable for the NC memory to achieve larger storage per unit area. Unfortunately, n and p each has its upper limit. It is reported that for the Si nanocrystals to be electrically isolated with respect to adjacent tunneling transport, the optimal separation distance must be greater than 4nm from one another [2]. When multiple electrons are stored in one NC (p increases), charge confinement or Coulomb blockade effects will increase the energy levels, resulting in an upward shift of the Si NC conduction band minimum, thus reducing the effective potential well depth for the electron storage. And this becomes pronounced especially for Si NC (and other semiconductor NCs) below a diameter of about 3nm. These effects jeopardize the device charge retention characteristics and limit the size of Si NC to be approximately greater than 4nm (and thus the number of density, n). To approximately calculate the actual energy level rising of the Si NC caused by multiple stored electrons, one may compute from the reversible work needed to charge the NC with the additional electron. The capacitance of the NC is given by [23]

$$C = 2\pi\epsilon_{ox}d \quad (2.3)$$

The addition of n^{th} electron gives the NC an energy increase of

$$\Delta E_{n,n-1} = \frac{e^2}{2C} [n(n-1) - (n-1)(n-2)] = \frac{(n-1)e^2}{C} \quad (2.4)$$

Hence, the electrochemical potential change due to one added electron stored in NC is given by

$$\Delta\mu = \Delta E_{n,n-1} - \Delta E_{n-1,n-2} = \frac{q^2}{C} \quad (2.5)$$

Note that the capacitance of each NC in the size range of a few nms falls in the range of atto farads (10^{-18} F) or less. This change of energy level is not to be neglected. For example, for a

5nm diameter Si NC, the self capacitance is approximately 7×10^{-19} F. The energy level increase calculated by Equation (2.5) is about a few tenth of 1eV. In reality, the self-capacitance of a NC is higher than the theoretical value, given the fact that each NC has coupling effect with neighboring NCs as well as the substrate. Even so, the energy level for a 5 electron Si NC is about 0.5eV above the ground stage [24]. As shown in Fig. 2.5, after electron storage, the band gap of the Si NC is wider than the Si substrate. In addition, the fact that the stored electrons generate an electric field directly impacts the tunneling mediated charge loss through the bottom tunneling dielectric after programming, as well as limits the number of electrons can be stored, thus the overall device retention capability. The only merit of the raising energy level is the faster erasing speed of the charges stored in the NC by quantum mechanical tunneling.

Figure 2.5. Band-diagram of a Si NC under (a) programming (b) erasing and (c) retention [18].

2.3.2 Charge Retention Property of MNC-based Memory Cell

The higher density of states of metal over semiconductor makes the metal nanocrystal (MNC) suffer less from the quantum confinement. As the electrons been trapped in the MNC, unlike Si NC where limited density of states are present, MNC has enough density of states for the trapped electrons, thus less probability of conduction band minimum up-lifting is expected. Figure 2.6 shows the conduction band minimum up-shift of the Si and Ge NC and Fermi-level up-shift of metal Ni as a function of the NC size. The band splitting in nano-level leading to Fermi-level up-shift is only obvious for a NC size less than 2nm in diameter. For a state of the art MNC memory, the diameter is always larger than 2nm [25]. Some experimental researchers working on the treatment of indium-tin oxide (ITO) by Pt films have reported that the work function of metal thin films does not deviate from their bulk material dramatically even down to about 0.4nm in thickness [26]. The higher density of states also makes MNC more immune to Fermi-level fluctuation caused by contamination. Another advantage of MNC over its semiconductor counterpart is the wider range of work function available, which adds another degree of freedom in design. The work function of MNC affects both the depth of the potential well (key for charge retention time) and the density of states available for tunneling in the Si substrate. Engineer must consider the trade-off between the P/E and charge retention characteristics among the available work function of the metal. By aligning the MNC Fermi-level to be within the Si band-gap under charge retention, and above the conduction band under erasing, a large ratio of erase current to retention leakage current can be achieved. In a word, large P/E current (fast P/E speed) and long retention time can be simultaneously achieved when we use metal as NC material.

In Si NC based-NVM, a thin oxide with thickness less than 3 nm is used to separate the NCs from the channel. During P/E, the electrons/holes can pass through the oxide by direct

tunneling. This gives the advantage of fast P/E and low operation voltage. Besides the quantum confinement effect, the traps inside the Si NC and at the NC/SiO₂ interface can cause the device to suffer from poor retention time [27, 8]. Adopting metal as NC material can overcome this shortcoming; the traps at the NC/SiO₂ interface can hardly play any role simply due to the high density of states of the metal, which gives more uniform device characteristics and better process control.

Figure 2.6. Conduction band minimum up-shift of the Si and Ge NC and Fermi-level up-shift of metal Ni NC as a function of the NC size [21].

2.3.3 Leakage Current in the MNC-based Memory Cell

The leakage current problem arising from the thin tunneling oxide can be overcome by changing to a thicker oxide, thus changing the P/E mechanism from direct tunneling to FN tunneling. For

SNC, FN tunneling cannot serve as an effective P/E process because the strong electric field cannot be confined in only one oxide layer. However, for MNC, by manipulating the work function of both the NC and the control gate thus changing the barrier height, the turn-on electric field for FN tunneling from the NC and the control gate can be engineered.

It can be seen from Fig. 2.7 that FN tunneling probability has a very strong dependence on the MNC and control gate work function, because both the height and width of the barrier are modulated by the 2 work functions. For example, the work function of control gate ϕ_{CG} can be tuned to effectively suppress or enhance the tunneling from it. If the $\phi_{CG} < \chi_{Si}$, a smaller control gate bias is needed for the programming tunneling to be limited only in the control gate and extra electrons can be injected into the MNC; if $\phi_{CG} > \chi_{Si}$, tunneling can be confined only in tunneling oxide and the programming is by extracting electrons from the MNC. After setting the ϕ_{CG} , the threshold voltage can be determined by choosing the MNC work function.

Figure 2.7. Band diagram illustrating the influence of the work function of control gate and MNC in (a) programming and (b) erasing [27].

After electrons are stored in the MNC, there are mainly 3 discharge paths: electrons from discharging MNC to the control oxide; discharging from one MNC to the adjacent MNCs and discharging from the MNC to the substrate. The first path is often neglected, since the control oxide is always thicker than the tunneling oxide and the fact that it is often a high- κ material. Figure 2.8(a) shows the impact of control oxide on retention time. As expected, with the same equivalent oxide thickness (EOT), high- κ tunneling oxide improves the retention performance remarkably. However, there is no clear relation between the high- κ material permittivity and the retention time, due to the different energy barrier height at the interface of NC/high- κ .

The second path can be ignored if the spacing between the MNCs are relatively large, giving a wide enough barrier to prevent electrons from tunneling through. The last one is the dominant discharging path. Figure 2.8 (b) shows a relationship of retention time with tunneling oxide thickness (SiO_2 as the tunneling oxide). Again MNCs show better retention property than SNCs, and a tunneling oxide of 3.6 nm is thick enough for the Au MNC to ensure 10 years of life.

Figure 2.8. The impact of (a) control oxide material and (b) tunneling oxide thickness on retention time for SNCs and MNCs [23].

2.3 Resistive Switching Random Access Memory (RRAM)

Even though the NC-based flash memory has been proposed to further extend the limit of charge-trapping memory, this kind of memory will finally reach its scaling limit in the near future due to decreasing feature sizes, which results in constraints on the material and the geometries [29]. In addition, the cost-intensive production and the volatility of the market are the major challenges in the field of memory devices. A variety of alternative approaches are under research, in particular, novel materials and the use of alternative physical effects (e.g. spintronics) together with novel architectures are one of the focuses of primary investigations [30-32]. The resistive switching effect is a new and attractive storage concept combining fast operation and high storage densities with non-volatile data storage [33, 34]. It was also reported recently that the resistive switching is closely related to memristors as the fourth fundamental passive circuit element [35]. A resistive switching memory element is a simple two-terminal device formed from two metal electrodes separated by an insulator layer (MIM structure). Unipolar the bipolar switching has been observed. In unipolar switching, both the SET and RESET processes occur with the same voltage polarity, whereby the RESET currents exceed the SET currents. In bipolar material systems, different voltage polarities are needed for the SET and RESET processes.

There are two major proposed switching mechanisms: one that triggered by anion transport and redox reactions in the cation sublattice of transition metal oxides are subsumed under the generic term of “valence change mechanism” (VCM). Another mechanism is called “electrochemical metallization mechanism” (ECM) which is related to an electrochemical redox reaction of mobile cations. Common examples of VCM Resistive switching Random Access Memory (RRAM) stacks are SrTiO_3 and TiO_2 [37, 37] sandwiched between metal electrodes. Typical examples of ECM MIM stacks are formed by an electrochemically active electrode (e.g.

Cu or Ag) and an inert counter electrode (e.g. Pt or W) [34, 38, 39] with a cation-conducting electrolyte separating the electrodes in the MIM stack. In ECM material systems, the switching process is determined by (i) the anodic dissolution of the metal of the active electrode, (ii) the migration of the metal cations through the solid electrolyte, and (iii) the reduction of the metal cations at the inert electrode, forming a metal filament.

The RRAM stack can exhibit typically two different resistance levels referred to simply as high resistance state (HRS), i. e., the OFF state, and low resistance state (LRS, ON state). The states are non-volatile and the information is retrieved by measuring the electrical current when a small read voltage is applied. Intermediate states between the ON and OFF state might be used to store more than one bit per cell [40].

2.4 Summary

In summary, metal NC embedded in high- κ film is a promising candidate for future generation NVM. Its advantages over flash and DRAM are reviewed. The practice of choosing metal as the NC material provides performance characteristics that cannot be realized by its semiconductor counter-part. The reliability study of the normal gate dielectric is also reviewed. The charge retention property and the charge leakage mechanism of the metal nanocrystal-based high- κ /SiO₂ memory have been presented in detail. We point that there is however a lack of studies on the failure mechanism of MNC based high- κ /SiO₂ gate stack.

References

- [1] S. Tiwari, "Silicon nano-crystal memories: Devices in the limit of conventional miniaturization," in *Physics and Chemistry of SiO₂ and the Si-SiO₂ Interface-3*, 1996, vol. 96, H. Z. Massoud, *et al.*, Eds., ed, 1996, pp. 250-259.
- [2] C. Y. Lu, K.Y. Hsieh and R. Liu., "Future challenges of flash memory technologies," *Microelectronic Engineering*, vol. 86, pp. 283-286, Mar 2009.
- [3] J. Sune, I. Placencia, N. Barnoil, E. Farres, F. Martin and X. Aymerich, "On the Breakdown Statistics of Very Thin SiO₂-Films," *Thin Solid Films*, vol. 185, pp. 347-362, Mar 1990.
- [4] V. L. Lo, K.L. Pey, C.H. Tung and X. Li, "Multiple digital breakdowns and its consequence on ultrathin gate dielectrics reliability prediction," in *2007 IEEE International Electron Devices Meeting, Vols 1 and 2*, ed, 2007, pp. 497-500.
- [5] J. H. Stathis, "Percolation models for gate oxide breakdown," *Journal of Applied Physics*, vol. 86, pp. 5757-5766, Nov 1999.
- [6] L. Niemeyer, A.C. Razzitte, and E.E. Mola, "Fractal Dimension of Dielectric-Breakdown - Response," *Physical Review Letters*, vol. 57, pp. 650-650, Aug 1986.
- [7] D. A. Willming and C. H. Wu, "A Stochastic-Model for Dielectric-Breakdown in Thin Capacitors," *Journal of Applied Physics*, vol. 63, pp. 456-459, Jan 1988.
- [8] T. Tanamoto and A. Toriumi, "A percolation approach to dielectric breakdown statistics," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers*, vol. 36, pp. 1439-1442, Mar 1997.
- [9] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The Chemistry of Gate Dielectric Breakdown," in *IEEE International Electron Devices Meeting 2008, Technical Digest*, ed, 2008, pp. 779-782.
- [10] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The physical origin of random telegraph noise after dielectric breakdown," *Applied Physics Letters*, vol. 94, Mar 2009.
- [11] A. K. Jonscher, "Dielectric relaxation in solids," *Journal of Physics D-Applied Physics*, vol. 32, pp. R57-R70, Jul 1999.
- [12] M. Schumacher and R. Waser, "Curie-von Schweidler behaviour observed in ferroelectric thin films and comparison to superparaelectric thin film materials," *Integrated Ferroelectrics*, vol. 22, pp. 629-641, 1998.
- [13] M. V. Fischetti, M.V. Fischetti, D.A. Neumayer and E.A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-kappa insulator: The role of remote phonon scattering (vol 90, pg 4587, 2001)," *Journal of Applied Physics*, vol. 91, pp. 546-546, Jan 2002.
- [14] G. Steinlesberger, H. Reisinger, H. Bachhofer, H. Schroeder and W.S.M. Wolfgang, "Dielectric relaxation and charge transport mechanisms in (Ba,Sr)TiO₃ thin films," *Integrated Ferroelectrics*, vol. 38, pp. 893-902, 2001.
- [15] Z. Xu, L. Pantisano, A. Kerber, R. Degraeve, E. Cartier, S. De Gendt, M. Heyns and G. Groeseneken, "A study of relaxation current in high-kappa dielectric stacks," *IEEE Transactions on Electron Devices*, vol. 51, pp. 402-408, Mar 2004.
- [16] P. W. Anderson, "Model for Electronic-Structure of Amorphous-Semiconductors," *Physical Review Letters*, vol. 34, pp. 953-955, 1975.
- [17] J. R. Jameson, W. Harrison, P.B. Griffin and J.D. Plummer, "Double-well model of dielectric relaxation current," *Applied Physics Letters*, vol. 84, pp. 3489-91, 2004.

- [18] P. W. Anderson, B.I. Halperin and C.M. Varma, "Anomalous Low-Temperature Thermal Properties of Glasses and Spin Glasses," *Philosophical Magazine*, vol. 25, pp. 1-&, 1972.
- [19] W. A. Phillips, "Tunnelling States in Amorphous Solids," *Bulletin of the American Physical Society*, vol. 17, pp. 115-&, 1972.
- [20] R. C. Zeller and R. O. Pohl, "Thermal Conductivity and Specific Heat of Noncrystalline Solids," *Phys. Rev. B* **4**, 2029, 1971.
- [21] J. R. Jameson, K. Usami, M.A. Rafiq, Y. Tsuchiya, H. Mizuta and S. Oda, "Double-well model of dielectric relaxation current," *Applied Physics Letters*, vol. 84, pp. 3489-3491, May 2004.
- [22] L. Ding, K. Usami, M.A. Rafiq, Y. Tsuchiya, H. Mizuta and S. Oda, "Influence of nanocrystal size on optical properties of Si nanocrystals embedded in SiO₂ synthesized by Si ion implantation," *Journal of Applied Physics*, vol. 101, May 2007.
- [23] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories - Part II: Electrical characteristics," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1614-1622, Sep 2002.
- [24] J. J. Welser, S. Tiwari, S. Rishton, K.Y. Lee and Y. Lee, "Room temperature operation of a quantum-dot flash memory," *IEEE Electron Device Letters*, vol. 18, pp. 278-280, Jun 1997.
- [25] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories - Part I: Device design and fabrication," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1606-1613, Sep 2002.
- [26] S. M. Tadayyon, K. Griffiths, P.R. Norton, C. Tripp and Z. Popovic, "Work function modification of indium-tin-oxide used in organic light emitting devices," *Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films*, vol. 17, pp. 1773-1778, Jul-Aug 1999.
- [27] Y. Shi, S.L. Gu, X.L. Yuan, Y.D. Zheng, K. Saito, H. Ishikuro and T.Hiramoto, "Silicon nano-crystals based MOS memory and effects of traps on charge storage characteristics," in *1998 5th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, M. Zhang and K. N. Tu, Eds., ed, 1998, pp. 838-841.
- [28] M. She, T.J. King, C.M. Hu, W.J. Zhu, Z.J. Luo, J.P. Han and T.P. Ma "Low-voltage, fast-programming P-channel flash memory with JVD tunneling nitride," in *2001 International Semiconductor Device Research Symposium, Proceedings*, ed, 2001, pp. 641-644.
- [29] V. V. Zhirnov, R.K. Cavin, S. Menzel, E. Linn, S. Schmelzer, D. Brauhhaus, C. Schindler and R. Waser, "Memory Devices: Energy-Space-Time Tradeoffs," *Proceedings of the IEEE*, vol. 98, pp. 2185-2200, Dec.
- [30] S. Tehrani, J.M. Slaughter, M. Deherrera, B.N. Engel, N.D. Rizzo, J. Salter, M. Durlam, R.W. Dave, J. Janesky, B. Butcher and K. Smith, "Magnetoresistive random access memory using magnetic tunnel junctions," *Proceedings of the IEEE*, vol. 91, pp. 703-714, May 2003.
- [31] A. DeHon, "Deterministic addressing of nanoscale devices assembled at sublithographic pitches," *IEEE Transactions on Nanotechnology*, vol. 4, pp. 681-687, Nov 2005.
- [32] C. Chappert, A. Fert and F. Nguyen Van Dau, "The emergence of spin electronics in data storage," *Nature Materials*, vol. 6, pp. 813-823, Nov 2007.

- [33] K. Terabe, T. Hasegawa, T. Nakayama and M. Aono, "Quantized conductance atomic switch," *Nature*, vol. 433, pp. 47-50, Jan 2005.
- [34] M. N. Kozicki, C. Gopalan, M. Balakrishnan and M. Mitkova, "A low-power nonvolatile switching element based on copper-tungsten oxide solid electrolyte," *IEEE Transactions on Nanotechnology*, vol. 5, pp. 535-544, Sep 2006.
- [35] D. B. Strukov, G.S. Snider, D.R. Stewart and R.S. Williams, "The missing memristor found (vol 453, pg 80, 2008)," *Nature*, vol. 459, Jun 2009.
- [36] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline SrTiO_3 ," *Nature Materials*, vol. 5, pp. 312-320, Apr 2006.
- [37] D. S. Jeong, H. Schroeder and R. Waser, "Abnormal bipolar-like resistance change behavior induced by symmetric electroforming in Pt/TiO₂/Pt resistive switching cells," *Nanotechnology*, vol. 20, Sep 2009.
- [38] M. Meier, C. Schindler, S. Gilles, R. Rosezin, A. Rudiger, C. Kugeler and R. Waser, "A Nonvolatile Memory With Resistively Switching Methyl-Silsesquioxane," *IEEE Electron Device Letters*, vol. 30, pp. 8-10, Jan 2009.
- [39] C. Schindler, G. Staikov and R. Waser, "Electrode kinetics of Cu-SiO₂-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories," *Applied Physics Letters*, vol. 94, Feb 2009.
- [40] A. Beck, J.G. Bednorz, C. Gerber, C. Rossel and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," *Applied Physics Letters*, vol. 77, pp. 139-141, Jul 2000.

CHAPTER THREE

EXPERIMENTAL PROCEDURE AND DETAILS

3.1 Introduction

In this chapter, the main steps for the characterization of the MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ flash memory gate stack are presented. Fabrication of micrometer- and nanometer-scale electrodes, as well as various equipment used for the characterization of the stack under micrometer-scale and nanometer-scale are described here. Three electrical characterization methods to study the properties of the MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stacks are presented. Also, the procedure and the details of various types of stressing methodologies used in our studies are thoroughly discussed. These methodologies allow us to further understand the physical mechanisms responsible for governing the BD and recovery (RC).

3.2 Sample Information and Equipments

The devices used in this study were MOS capacitor with ruthenium (Ru) metal nanocrystal. The devices were fabricated on an n-type Si wafer with doping level of $\sim 3 \times 10^{19}/\text{cm}^3$ of As. After cleaning, a 4nm SiO_2 as tunnel oxide was grown as the tunnel oxide. This tunnel oxide for this MNC-based flash memory gate stack was prepared by thermally grown SiO_2 using in-situ-steam-generation process in an Applied Materials 200mm RTP (Rapid Thermal Process) Chamber. MNC was formed by PVD (Physical Vapor Deposition) sputter deposition followed by an annealing at 970 K to 1170 K (depending on the metal material). The metal thin film would ball

up into the shape of MNCs because of surface energy minimization [1]. For the single layer (SL) sample, a layer of 6nm Al_2O_3 was then deposited as the by PVD control oxide. For the dual layer (DL) MNC-based gate stack, after forming the bottom layer of MNC, a thin film of Al_2O_3 was deposited on top as the inter layer dielectric (ILD). This is followed by formation of the top layer MNC. A thick layer of Al_2O_3 was then deposited as the control oxide on top. The details of the MNC-based gate stack formation is discussed in [2]. The cross-sections of typical SL and DL MNC-based gate stacks are shown in Fig. 3.1.

Figure 3.1. Cross-sectional illustration of MNC-based MOS capacitor used in this study: **(a)** single layer MNC-based high- κ /SiO₂ gate stack and **(b)** dual MNC-based high- κ /SiO₂ gate stack.

The electrode was prepared in 2 different ways for micro- and nanometer-scale electrical characteristics. For the micrometer-scale characterization, top electrodes with 160 μm

diameter/spacing of Au or Pt dots and a thickness of 100nm were formed using electron-beam evaporator. The electrode array of 160 μ m diameter/spacing was realized by a shadow mask covered on top of the cleaned sample surface during the metal evaporation.

For the nanometer-scale characterization, as illustrated in Fig. 3.2, aligned nano-sized Au/Cr dots (thickness of 100nm/20nm) with different spacing and same width (200nm) were deposited using electron-beam lithography (EBL). The process flow of forming the nano electrode deposition is illustrated in Fig. 3.3. The purpose of the 200nm width and dots alignment on a straight line is to facilitate the TEM/EELS (Transmission Electron Microscopy/Electron Energy Loss Microscopy) physical study of the stressed area under the nano dot electrodes.

The equipment used for micrometer-scale reliability characterization includes an Suss PM8 200mm manual probe station and a Keithley 4200 Semiconductor Characterization system, which are shown in Fig. 3.4(a) and Fig. 3.4(b), respectively.

(a)

(b)

Figure 3.2. Planar view of nano-dot electrode formed by EBL. (a) Schematic illustration and (b) SEM picture.

Figure 3.3. Flow chart of nano Au/Cr electrode formed with EBL.

The Suss PM8 200mm manual probe station serves as a platform for the wafer stressing and all the related electrical measurements. Its main components are a probe chamber, a microscope, a gas distribution panel, a vibration isolation table and a chuck and platen controls. The Keithley 4200 Semiconductor Characterization System is mainly used to perform the gate oxide stressing and all the related electrical measurements. It consists of four highly accurate source-monitor units (SMUs) with a current resolution of 0.1fA as shown in Fig. 3.4(b). These

SMUs are separately connected to four probe heads placed on the Suss 200mm manual wafer probe station via Kelvin tri-axial cables with low leakage currents. These probe heads are primarily used to steadily hold the tungsten needles, which can separately connect device terminals or the ground.

(a)

(b)

Figure 3.4. (a) Suss PM8 200mm manual probe station and (b) Keithley 4200 Semiconductor Characterization System.

The equipment for nanometer-scale reliability characterization is the Zyvex KZ100 Nanomanipulator/Prober incorporated in a LEO 1550 Gemini Field Emission SEM (scanning electron microscopy) (Fig. 3.5) for precise imaging and probe placement. The SEM has a

magnification range of 20x to 900,000x, and a resolution of 3nm at 2mm work distance and 1kV acceleration voltage; 1nm at 2mm work distance and 20kV acceleration voltage.

Figure 3.5. Example of LEO 1550 Gemini Field Emission SEM.

The Zyvex KZ100 Nanomanipulator/Prober consists of a Zyvex Nanomanipulator (Fig. 3.6(a)), a controller (Fig. 3.6(b)), and a Keithley 4200 Semiconductor Characterization System. The Zyvex Nanomanipulator capable of landing four sharp probes easily within a 200x200 nm area with less than 5 nm precision. The size of the minimum landing area is dependent on the sharpness of the probes. The minimum landing area could be much smaller than that stated above

with proper sharpened probes. The KZ100 can be outfitted with as many as four probes which are independently and linearly operated in X, Y, and Z with less than 5 nm precision. Tungsten probes with a 45-degree bend were prepared using a proprietary Zyvex process and installed in the four positioners. A Keithley 4200 Semiconductor Characterization System was used for biasing the probes and collecting electrical data of the device of interest. The system was equipped with four 4200-SMUs (source measurement unit) and triaxial cabling. Before and during data acquisition, the microscope's scanning beam was blanked to minimize any charge-induced influence.

(a)

(b)

Figure 3.6. Components of Zyvex KZ100 Nanomanipulator/Prober: (a) Zyvex Nanomanipulator and (b) Controller.

3.3 Electrical Characterization Methodology

3.3.1 Dual Voltage Sweep I - V Characterization

There are various electrical characterization methods to study the reliability of a charge-trapping gate stack, the simplest and maybe the quickest one is a dual voltage/bias sweep I - V characterization.

A dual voltage sweep is simply a continuous forward and backward voltage ramp test. With the top electrode of the MOS capacitor connecting to one of the SMU and the substrate connecting to the ground, the dual voltage I - V characterization shows the apparent top electrode-to-substrate leakage current of the capacitor under a varying stressing voltage. The purpose of this test is to examine the functionality of the charge trapping gate stack. Figure 3.7 shows a typical -2V ~ +2V dual voltage sweep on a single layer Ru-MNC-based gate stack (the blue arrows show the sweeping direction). It could be seen that the current increases or decreases dramatically when the positive direction voltage sweep or negative direction voltage sweep begins, indicating charge de-trapping or charge trapping behavior in the gate stack. It was noticed that the shape of the I - V curve does not change much if we chose the dual voltage sweep range as -4V ~ 0V or 0V to +4V. Because of the charging and de-charging of the gate stack in the forward and backward voltage sweep, a current hysteresis is observed. This hysteresis can be used as sign of the functionality of the charge-trapping flash memory gate stack [3]. Furthermore, the magnitude of the leakage current I_{leak} can reflect whether the gate stack has been broken-down and roughly the BD hardness.

Figure 3.7. Typical dual voltage sweep curve on a single layer Ru-MNC-based gate stack, a hysteresis is observed.

3.3.2 Relaxation Current Measurement

As mentioned in Section 2.2.2, as the dielectric relaxation current in high- κ film overwhelms the one in SiO_2 , the existence of relaxation current acts as a signal indicating the integrity of the high- κ film after the stress. A relaxation current (I_{relax}) is recorded immediately after a sudden removal of an initializing voltage (marked as V_{ini}). The magnitude of V_{ini} is chosen to be from +3V to +5V (for substrate injection) or -3V to -5V (for top electrode injection) depending on the thickness of the gate stack. The value the V_{ini} chosen was a compromise between achieving a sufficiently large voltage change to have I_{relax} and avoiding the BD voltage at which physical

damages are created. Fig. 3.8 shows a typical I_{relax} measurement with a $V_{ini} = +4V$ on a single layer Pt nanocrystal-based high- κ /SiO₂ gate stack. The I_{relax} reaches the peak value immediately at the removal of the V_{ini} , and then decays with time, finally approaches zero value. The inset shows that the I_{relax} vs. time curve is almost a straight line. Due to a machine limitation, in this study, the I_{relax} current is only recorded after about 4s of the V_{ini} removal.

Figure 3.8. Typical relaxation current of after sudden removal of V_{ini} . The inset shows that the relaxation current vs. time curve is almost a straight line in double log scale.

The behavior of I_{relax} of the MNC-based high- κ /SiO₂ is very similar to the I_{relax} of pure dielectric film, which follows a linear-log relationship with respect to time. This is referred to as Curie-von Schweidler law [4]:

$$I_{relax} = at^{-n} \quad (3.1)$$

where I_{relax} stands for the relaxation current, t stands for time, a and n are both constants. It is worth noticing that n is the slope of the I_{relax} vs. time curve in the double log scale. For most dielectric films (without embedded MNCs), n is a number close to 1. In our MNC-based high- κ /SiO₂ gate stack, the slope of n of the I_{relax} is essentially different from pure dielectric films. The details are discussed in *Chapter Four*.

3.3.3 Capacitance-Voltage Technique

The most commonly used tool for studying the MOS capacitor gate stack quality is the Capacitance-Voltage ($C-V$) technique. To measure a MOS capacitor $C-V$ curve, the capacitor is typically connected to a two-terminal $C-V$ analyzer. The $C-V$ analyzer applies a high-frequency (1MHz or 100kHz) drive signal to the backside of the substrate, via the chuck of the prober. Meanwhile, the prober chuck must be electrically floating to avoid diverting the drive signal to ground. The high frequency alternating current is superimposed to a relatively slow direct current bias sweep. The signal is picked up through the gate via the probe needle.

Figure 3.9 shows a typical $C-V$ curve of a dual layer Pt-MNC-based gate stack in three states which under fresh condition, programmed and erased using single voltage sweep. The voltage applied on the top electrode swept from -4 to 4V. The programming voltage adopted was +6V and the erasing voltage was -6V.

Figure 3.9. Typical C-V curve of a dual layer Pt-MNC-based gate stack under its fresh, programmed and erased condition

It should be noticed that the C-V measurement acquires data only under equilibrium conditions. A MOS capacitor takes time to become fully charged after a voltage step is applied. The fully charged condition is generally referred to as the equilibrium condition. Therefore, to allow the MOS capacitor to reach equilibrium, following steps are taken:

- 1) After initially applying voltage to a MOS capacitor, allow an adequate hold time before recording the capacitance. In our measurement, the hold time is chosen as 1s.
- 2) After each step of the MOS capacitor voltage, allow an adequate delay time before recording the capacitance. The delay time is chosen to be 1s as well.

- 3) C-V test results offer a wealth of device and process information that we need for reliability study. For example, the oxide capacitance, which can be read from the capacitance value of the accumulation region, can be used to calculate the equivalent SiO_2 oxide thickness (EOT). The flat-band voltage (V_{FB}) could also be extracted from the C-V curve, which is a key parameter in to determine the flash memory window.

3.4 Stressing Methodology

3.4.1 Calculation of Stressing Voltages (V_{stress}) for Constant Voltage Stress (CVS)

Before the stressing on the MNC embedded in $\text{Al}_2\text{O}_3/\text{SiO}_2$ is carried out, the BD voltage (V_{BD}) of the device must be determined. First, a voltage ramp I - V measurement was carried out by sweeping the bias voltage (V_{bias}) from 0 V to a higher value with a constant voltage increment of 0.05 or 0.1 V, while substrate was grounded. Here V_{bias} represent the voltage applied to the top electrode and I_{leak} represents the leakage current through the top electrode. I_{leak} increased with increasing V_{bias} due to the quantum mechanical tunneling of the charge carriers through the Al_2O_3 and SiO_2 oxide layers. When I_{leak} experienced a sudden, abrupt increase, the device was said to encounter a dielectric BD event, and the corresponding V_{bias} was regarded as BD voltage V_{BD} . Fig. 3.10 shows a typical voltage ramp I_{leak} - V_{bias} curve with increment step of 0.1 V in 0.1 s by setting a gate leakage compliance current limit of 10nA, in which V_{BD} is recorded. This procedure was repeated for about 20 electrodes which possess the same dimensions and was well distributed over a whole desired wafer area. Eventually, the average BD voltage (V_{BDA}) of a Ru NC memory device was obtained. The time to BD at V_{BDA} is 0.1s.

Figure 3.10. Voltage ramp to determine the BD voltage V_{BD} .

Second, by knowing V_{BDA} , V_{stress} which defines the top electrode voltage in a CVS test could be determined. V_{stress} must be lower than V_{BDA} such that a BD event will not occur immediately upon CVS stressing. The equation for calculating V_{stress} is given by [5]

$$\ln(t_{BD}) = \ln(t_{BD}') + \beta(V_{BDA} - V_{stress}) \quad (3.2)$$

where t_{BD} and t_{BD}' (in our case 0.1s) are the time-to-dielectric-breakdown of CVS stress at V_{stress} and V_{BDA} , respectively. Note that in our experiments, the value of t_{BD} was in the range of 100-2000 s, and β is a voltage acceleration factor which is dependent on temperature, applied voltage,

area and thickness of the dielectric under stress [5]. The calculated V_{stress} our sample used in this study is between 5.8V ~ 6.8V for substrate injection, and -6.6V ~ -7.5V for top electrode injection. While in the nano-electrode, V_{stress_nano} is about 6.5V for substrate injection and -7.5V for top electrode injection, the increased BD voltage (so stressing voltage) in nano-electrode is believed to be due to parasitic resistance of the probing tip, sample holder, etc. which is negligible at micrometer-scale characterization.

3.4.2 Successive CVS

Constant-voltage stress is a widely used stressing methodology in the study of gate dielectric reliability [6], [7]. When the dielectric is under constant voltage, the energy of carriers injected from the anode to the dielectric, which is primarily dependent on the V_{stress} , is believed to be kept at constant, until the point when the local property of the dielectric changes (band gap, conductivity, local temperature, etc.). This implies that the generation of defects happens at a relatively constant speed. Therefore, in order to more precisely study the dielectric BD, a CVS is adopted in our studies. A single CVS stressing was normally terminated when a sudden, abrupt increase in I_{leak} with the magnitude of more than two times larger than the fresh or non-BD I_{leak} was detected, which is generally identified as the occurrence of a dielectric BD event. According to the percolation model proposed by R. Degraeve *et al.* [8, 9], a dielectric BD event occurs when a conductive percolation path, which is constituted by various types of defects or electronic traps, is formed within the dielectric for which the top electrode and the substrate are electrically connected with each other. When the dielectric is stressed using a CVS, I_{leak} will gradually increase with time due to the generation of electronic traps within the oxide caused by the charge carrier tunneling, resulting in the generation of stress-induced-leakage-current (SILC) [10, 11]. The whole process involving the generation of electronic traps within the gate oxide and the

occurrence of a dielectric BD event is universally referred to as time-dependent-dielectric-breakdown [12].

A successive CVS, or current-limited CVS, was developed to study the I - V characteristics at different stages of the progressive BD [7], in which a current compliance limit (I_{max}) is used to control one particular stage of the progressive BD, or BD hardness. In the beginning of a successive CVS, the device of interest was stressed with a high V_{stress} . The amount of I_{leak} flowing through the percolation path formed within dielectric upon the occurrence of a dielectric BD event was limited by I_{max} , when the stressing is automatically halted when I_{leak} reached I_{max} . After each I_{max} , the post-BD dual I - V sweep at low voltage level is conducted to check the hysteresis as well as the leakage current level. Then the device stressing is resumed and continued by setting a higher I_{max} without changing V_{stress} . A successive CVS allows us to monitor the I - V characteristics at different levels of I_{leak} during the progressive BD for a device by successively increasing I_{max} (see Fig. 3.11).

Figure 3.11 Successive CVS showing different progressive BD stage captured by I_{max} [13].

3.4.3 Improved K-cycle Multiple-stage CVS

Both successive CVS and K-cycle CVS stressing methodology have been developed by our research group members. In general, a K-cycle multiple-stage CVS [14] is a repetitive process of stressing the dielectric with one particular range of V_{stress} . It is used to study the behaviors of I_{leak} at different stages of the progressive BD under various conditions. A K-cycle multiple-stage CVS starts by stressing the dielectric with V_{stress} calculated by Equation (3.1), ensuring that the TDDB could be completed within a reasonable time span. A relatively low I_{max} is used during the occurrence of a dielectric BD event such that the early stage of the progressive

BD could be successfully captured. Thereafter, the 1st-cycle multiple-stage CVS is carried out. V_{init} and V_{final} define an initial and a final V_{stress} used in the 1st-cycle multiple-stage CVS, respectively. The device is stressed with $V_{stress} = V_{init}$ for a specific constant duration t_{stress} . Following stressing is repeated by increasing V_{stress} with a constant step denoted as ΔV , until V_{final} is reached, which could be determined I_{leak} hits the compliance I_{max} . This is followed by the 2nd-, the 3rd-, and the Kth-cycle multiple-stage CVS, which is similar to the 1st-cycle multiple-stage CVS.

Figure 3.12. Flow chart of an improved K-cycle multiple-stage constant-voltage stress.

Incorporated with the I_{relax} test and reverse bias CVS stressing, the improved K-cycle multi-stage CVS methodology not only studies the dielectric damage in each layer via I - V characteristics and I_{relax} at different BD hardness, but also examines the RC effects on each dielectric layers. The basic procedure was as follows: first, I - V data and I_{relax} of the fresh sample was tested as a reference; second, a stressing CVS was conducted with a relatively low compliance current limit (I_{max}) to induce a BD event. The CVS stressing was not stopped until the compliance current limit I_{max} was reached. After a BD event (i. e., leakage current I_{leak} reached I_{max}), the post-BD I_{relax} and I - V characteristics data was collected; Then at a RC bias CVS of V_{RC} for time a $t_{RC} = 20s$ was applied after which a post-RC I_{relax} and dual I - V voltage sweep tests were conducted. Using a post-RC dual voltage sweep, the I_{relax} was collected to check the degree of the RC. If the I_{relax} cannot be observed anymore, the device was considered to have a hard BD (HBD) and the stressing was completed. All above were considered as one cycle, the next cycle was the same except that the I_{max} was increased, inducing a harder BD event. The $I_{max,K}$ for K^{th} cycle stress is listed in table 3.1. There are several things worth mentioning, the stress voltage V_{stress} of the stressing CVS was the same as in the successive CVS, i. e., calculated for formula 3.1. The absolute value of the top electrode voltage in the reverse bias CVS (V_{RC}) was ± 3 to $\pm 4V$, as a compromise between the effective RC and the BD voltage. The time span t_{RC} of the reverse bias CVS was 10s to 20s to ensure an effective and complete RC event was realized. Fig. 3.12 shows a flowchart of a complete improved K-cycle multiple-stage constant-voltage stress, for both top electrode injection and substrate injection experiments. The improved K-cycle multiple-stage CVS is an optimization of the K-cycle multiple-stage CVS which is developed by our group in 2004 [15].

Table 3.1 List of I_{max} for each cycle CVS stress to control the BD hardness.

K	1	2	3	4	5	6	...
$I_{max,K}$	100nA	200nA	500nA	800nA	0.1 μ A	0.2 μ A	...

3.5 Summary

In summary, the preparation of fabrication for the micrometer- and nanometer-scale metal electrodes on the MNC-based devices is described in this chapter. The equipment for micro- and nanometer-scale characterization are introduced. Electrical characterization techniques that are adopted in this study: dual voltage sweep, I_{relax} measurement and C-V test are described briefly. Various stressing methodologies employed (CVS, successive CVS and improved K-cycle multiple-stage CVS) are discussed in details.

References

- [1] B. Mondal and S. K. Saha, "Hydrothermal synthesis of silver nanoshells: Formation and plasmon hybridization," *Journal of Materials Science*, vol. 46, pp. 5153-5159.
- [2] S. K. Samanta, P.K. Singh, J. Y. Won, G. Samudra, Y.C. Yeo, L.K. Bera and N. Balasubramanian, "Enhancement of memory window in short channel non-volatile memory devices using double layer tungsten nanocrystals," in *IEEE International Electron Devices Meeting 2005, Technical Digest*, ed, 2005, pp. 177-180.
- [3] J.S. Lyu, B.W. Kim, K.H. Kim, J.Y. Cha and H.J. Yoo, "Metal-ferroelectric-semiconductor field-effect transistor (MPSFET) for single transistor memory by using Poly-Si source/drain and BaMgF/sub 4/ dielectric," in *Electron Devices Meeting, 1996. IEDM '96., International*, 1996, pp. 503-506.
- [4] M. Schumacher and R. Waser, "Curie-von Schweidler behaviour observed in ferroelectric thin films and comparison to superparaelectric thin film materials," *Integrated Ferroelectrics*, vol. 22, pp. 629-641, 1998.
- [5] A. Berman, "Time-zero dielectric reliability test by a ramp method [for field effect ICs]," New York, NY, USA, 1981, pp. 204-9.
- [6] B. P. Linder, J.H. Stathis, R.A. Wachnik, E. Wu, S.A. Cohen, A. Ray and A. Vayshenker, "Gate oxide breakdown under current limited constant voltage stress," in *20th Symposium on VLSI Technology*, Honolulu, Hi, 2000, pp. 214-215.
- [7] K. L. Pey, C.H. Tung, M.K. Radhakrishnan, L.J. Tang, Y. Sun, X.D. Wang and W.H. Lin, "Correlation of failure mechanism of constant-current-stress and constant-voltage-stress breakdowns in ultrathin gate oxides of nMOSFETs by TEM," in *14th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, Bordeaux, France, 2003, pp. 1471-1476.
- [8] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas and H.E. Maes, "A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides," in *1995 International Electron Devices Meeting*, Washington, Dc, 1995, pp. 863-866.
- [9] R. Degraeve, G. Groeseneken, R. Bellens, J.L. Ogier, M. Depas, P.J. Roussel and H.E. Maes, "New insights in the relation between electron trap generation and the statistical properties of oxide breakdown," *IEEE Transactions on Electron Devices*, vol. 45, pp. 904-911, Apr 1998.
- [10] D. J. Dimaria and E. Cartier, "MECHANISM FOR STRESS-INDUCED LEAKAGE CURRENTS IN THIN SILICON DIOXIDE FILMS," *Journal of Applied Physics*, vol. 78, pp. 3883-3894, Sep 1995.
- [11] K. Okada, "Analysis of the relationship between defect site generation and dielectric breakdown utilizing A-mode stress induced leakage current," *IEEE Transactions on Electron Devices*, vol. 47, pp. 1225-1230, Jun 2000.
- [12] D. L. Crook, "Method of determining reliability screens for time dependent dielectric breakdown," New York, NY, USA, 1979, pp. 1-7.
- [13] V. L. Lo, K.L. Pey, C.H. Tung, D.S. Ang, T.S. Foo and L.J. Tang, "Percolation resistance evolution during progressive breakdown in narrow MOSFETs," *IEEE Electron Device Letters*, vol. 27, pp. 396-398, 2006.
- [14] V. L. Lo K.L. Pey, C.H. Tung, D.S. Ang, T.S. Foo and L.J. Tang, "Multiple digital breakdowns and its consequence on ultrathin gate dielectrics reliability prediction," in *2007 IEEE International Electron Devices Meeting, Vols 1 and 2*, ed, 2007, pp. 497-500.

- [15] K. L. Pey, N. Raghavan, X. Li, W.H. Liu, K. Shubhakar, X. Wu and M. Bosman, "New insight into the TDDB and breakdown reliability of novel high-k gate dielectric stacks," in *2010 IEEE International Reliability Physics Symposium (IRPS 2010)*, 2-6 May 2010, Piscataway, NJ, USA, 2010, pp. 354-63.

CHAPTER FOUR

STUDY OF RELAXATION CURRENT IN SINGLE AND DUAL LAYER METAL NANOCRYSTAL-BASED HIGH- κ /SiO₂ GATE STACK

4.1 Introduction

Continual scaling of traditional floating gate flash memory cell size below 22nm is challenging because of the bottleneck issues for scaling tunnel oxide, lateral dimension and control oxide [1]. A novel structure adopting a SL or DL MNC as localized charge storage medium has been proposed as a candidate for sub-22nm flash memory cell [2]. Besides the possibility of scaling below 22nm, the discrete individual charge storage nodes (i. e., MNCs) also provide better immunity to defects than conventional floating gate flash memory [3]. In particular, it has been reported that stacks containing DL MNC provide an enhanced memory window over SL MNC, and have the potential capability of storing multi-bits per cell for the future NAND flash applications [2]. Extensive reliability studies have been carried out for this type of novel memory cells [2, 4-6]. In this study, dielectric relaxation current measurement is used to characterize the electrical properties of flash memory gate stack containing SL and DL MNC with Al₂O₃ and SiO₂ layer as the respective control and tunnel oxide layers. A physical model is proposed to elucidate the origin of different behaviors of the relaxation current in the SL and DL Pt MNC gate stacks.

4.2 Experimental Details

The fabrication of the SL and DL MNC-based samples was introduced in Section 3.2. The tunnel oxide for this Pt MNC-based flash memory gate stack was prepared by thermally grown SiO_2 . MNCs were formed by first depositing a thin film of Pt and then annealing it at 1170 K for 30s. The metal thin film would ball up into numerous MNCs (roughly uniform in size) because of surface energy minimization [7]. The control oxide for the SL MNC gate stack of Al_2O_3 (high- κ) is deposited by PVD. For the DL MNC-based gate stack, after forming the bottom layer of MNC, a thin film of Al_2O_3 was deposited on top as the inter layer dielectric (ILD). This is followed by formation of the top layer MNC. A thick layer of Al_2O_3 was finally deposited as the control oxide on top. A pure high- κ (HK) layer of 10nm Al_2O_3 deposited directly to Si substrate (with approximately 1nm interfacial layer (IL) SiO_2) was used in this study as a control sample. The top metal electrodes for all samples are Pt dots of 160 μm diameter and 100nm thickness realized by shadow masking. Fig. 4.1(a), (b) and (c) show the schematic of the control HK, SL and DL MNC-based gate stack, respectively. The cross-sectional TEM micrographs of the SL and DL samples are shown in Fig. 4.2(a), the mean diameter of the MNCs is approximately 3nm [8] in both samples. The top layer of MNC (labeled as MNC2) shows a slightly higher diameter and a slightly lower number density than the bottom layer of MNC (MNC1). The planar view TEM of the SL MNC-based sample (the same as the bottom layer of MNC in DL sample) is shown in Fig. 4.2(b). We can see that the MNCs are individually isolated by the Al_2O_3 dielectric.

For electrical measurements, the relaxation current density (J_{relax}) at different temperatures was measured by a Keithley 4200 semiconductor characterization system. The dielectric relaxation current was measured at zero stressing voltage, instantly after the removal of an initial stressing voltage (V_{ini}). This approach was used to eliminate any possible leakage

current that might affect the magnitude the relaxation current. The stressing time was chosen as a compromise between avoiding stressed induced effects (such as stress-induced leakage current) and ensuring an effective initial electric field to produce a measureable relaxation current.

Figure 4.1. Schematic cross-sections showing dimensions of three samples (not to scale): (a) Control HK, (b) SL Pt MNC-based gate stack and (c) DL Pt MNC-based gate stack.

(a)

(b)

Figure 4.2. TEM micrographs showing the cross section of (a) SL MNC-based gate stack and (b) DL MNC-based gate stack samples.

4.3 Temperature-dependent Relaxation Current on Single and Dual layer Pt Metal Nanocrystal-based Al₂O₃/SiO₂ Gate Stack

4.3.1 Temperature-dependent J_{relax} slope of SL and DL MNC-based gate stack samples

When a sudden electric field change is applied to (or removed from, in our case) capacitors with high- κ dielectric gate stacks, the leakage current amplitude reaches a peak value immediately and then decays with time [9]. This current is referred to as dielectric relaxation current, which is often observed in dielectric materials. As mentioned in *Chapter Two*, the relaxation current in dielectric materials was attributed to polarization of the dielectric material in a double potential well induced by carrier hopping, with the two wells representing the physical configurations before and after the rearrangement [10]. A normal dielectric relaxation current follows the sign of dV_{ini}/dt , and follows the Curie-von Schweidler law: $J_{relax} = at^n$ [11], which is a straight line on a log-log scale with a slope n . Reisinger *et al.* [12] have shown that the contribution of the total relaxation current from the SiO₂ layer is negligible because of its small magnitude compared to that from the high- κ layer. Thus in this study we assume that the J_{relax} comes primarily from the high- κ layer (with or without MNC). It is also shown that the J_{relax} of the high- κ dielectric (such as HfO₂, ZrO₂ and Al₂O₃) is independent of temperature and proportional to the initial electric field (E_{ini}) [12]. In this study, E_{ini} for the relaxation current measurement on the high- κ Al₂O₃ layer (embedded with SL or DL MNCs) of the SL and DL sample was calculated by

$$E_{ini} = \frac{(V_{ini} - V_{FB} - \Psi_s)EOT_{HK}}{t_{HK} * EOT_{stack}} \quad (4.1)$$

where V_{ini} is the magnitude of the initial step voltage applied to the top stack for the production of J_{relax} , V_{FB} is the initial flat band voltage of the MOS capacitor, Ψ_s is the initial Si surface potential, EOT_{HK} and EOT_{stack} are the equivalent SiO_2 thickness of the total Al_2O_3 layer and the whole gate stack respectively, and t_{HK} is the thickness of the total Al_2O_3 layer. In this study, all the E_{ini} are chosen to be the same value of 3MV/cm for the ease of parallel comparison.

Figure 4.3. Relaxation current density of the control HK sample at four different temperatures, the inset shows the slope n extracted from the respective curves.

Figure 4.3 shows the J_{relax} of the control Al_2O_3 sample (control HK) at 300, 350, 400 and 450K, and the inset lists the slope n extracted from the respective curves at the log-log scale. Consistent with previous reporting of the relaxation current [12], n of a pure HK is a constant number close to one and is independent of temperature. The amplitude of J_{relax} increases slightly with temperature (T). This is probably because of the increased charge trapping/de-trapping in the oxide layers with increasing T [13]. The J_{relax} of the SL Pt MNC sample at the same four temperatures is shown in Fig. 4.4. It is evident that J_{relax} curve no longer shows a single slope but manifests primarily two parts with different slopes. These two parts of the J_{relax} exhibit different temperature dependencies. We consider as the “initial part” the data from the first data point up to 20s and the “tail part” as the points from 40s to the end of the measured time range. The slope n extracted from the curve-fitting of the two parts are shown in the two insets. It can be seen that n increases with increasing T in the initial part, whereas in the tail part n appears to decrease with T .

Figure 4.4. Relaxation current density of SL MNC-based gate stack sample at four different temperatures, the two insets shows the slope n extracted from curve fittings of the initial part and the tail part.

Figure 4.5. Relaxation current density of the DL MNC-based gate stack sample at four different temperatures, the inset shows the slope n extracted from the respective curves.

In contrast, a different dependence of J_{relax} on temperature is observed for the DL MNC sample. As shown in Fig. 4.5, J_{relax} shows significant fluctuation especially at elevated temperatures, which is also observed in the tail part of J_{relax} in Fig. 4.4. The inset lists the slope n of the DL MNC sample from general curve-fitting. It is clear that n decreases as T rises, as if the DL sample exhibits only the behavior of the tail part of the SL sample.

4.3.2. Role of MNC in Relaxation Current

To compare the magnitude J_{relax} of the control HK, SL MNC, and DL MNC samples, we shall focus on the trend of J_{10s} and J_{60s} as a function of T , as shown in Fig. 4.6. It can be observed from

Fig. 4.6(a) that the magnitude of J_{I0s} for the control sample is relatively insignificant compared to that of J_{I0s} for the SL and DL Pt MNC-based gate stack samples, indicating that the dominant J_{relax} behavior in the SL and DL samples came from the MNC, especially at the initial stage of relaxation. Hence, we neglect the effects in J_{relax} induced by the Al_2O_3 layer in our analysis. The J_{I0s} value for the SL sample is observed to decrease slightly with increasing T , in accordance with the increasing slope n . However, the J_{I0s} value of the DL sample exhibits the opposite behavior, i. e. i. e. increases with rising T . Furthermore, the J_{I0s} value of the DL shows much higher magnitude than the SL, especially at high temperatures.

Here we propose a model to explain the J_{relax} behavior of the SL and DL MNC-based high- κ / SiO_2 gate stack at different temperatures. When the SL and DL MNC-based gate stack is under positively-biased V_{ini} , as shown in the band diagram of Fig. 4.7(a) and Fig. 4.8(a), the electrons are being injected from the substrate. The electron flux direction is from substrate toward the top electrode, which is basically a programming process of the MNC-based flash memory gate stack. The electrons could be trapped by the potential wells resulting from the embedded MNCs (charging of the MNCs). The energy level needed to trap an additional electron in the MNC is described by [14]

$$E_c = \frac{e^2}{2C} \quad (4.2)$$

where e is the electronic charge and C is the self-capacitance of the charged MNC. The energy states of the charged electrons are quantized.

(a)

(b)

Figure 4.6. (a) J_{10s} and (b) J_{60s} of control HK, SL MNC and DL MNC samples at four different temperatures.

Figure 4.7. Band diagram of SL MNC-based gate stack sample when (a) under V_{ini} , programming current consisting of both thermionic emission J_1 and quantum tunnelling J_2 charges the MNCs, (b) under zero bias ($t = 0$, beginning of J_{relax} measurement), charges leak out of MNCs to Si substrate, J_1 and J_2 comprise J_{relax} .

Figure 4.8. Band diagram of DL MNC-based sample when (a) under V_{ini} , programming current consisting of both thermionic emission J_1 and quantum tunnelling J_2 charges the MNCs, (b) under zero bias ($t = 0$, beginning of $J_{relax.}$ measurement), not only the electrons of MNC1, but also MNC2 electrons can quantum mechanically tunnel to the Si substrate to form J_2 ; nevertheless, J_1 can only come from the excess electrons in MNC1 because of the non-directional property of thermionic emission. Thus a more dominant role of J_2 is expected in $J_{relax.}$ of the DL MNC-based gate stack sample.

Upon the removal of the V_{ini} , a negative relaxation current is observed, indicating that the direction of the electron flux now comes from the top electrode towards the Si substrate. Since the magnitude of HK-induced relaxation current is relatively small compared to the MNC-induced relaxation current at the early stage of the J_{relax} measurement (see Fig. 4.6(a)), we shall focus primarily on the J_{relax} contributed by the MNC. We consider two main components of the MNC-induced J_{relax} . One part arises from the charges that are no longer confined in the MNC because of the sudden removal of V_{ini} . These charges are probably the trapped electrons that were at the top energy states of the potential wells of the MNCs. As shown by the dash line in Fig. 4.7(b), it is proposed that these charges leak from the MNCs and travel to the Si substrate through thermionic emission process [15]:

$$J_1 = J_1(t) \propto T^2 \exp\left[\frac{e}{kT} (a\sqrt{E_i(t)d} - \phi_B)\right] \quad (4.3)$$

where J_1 is the time-dependent thermionic emission current density, e is the elementary electron charge, T is the absolute temperature, a is a constant, $E_i(t)$ is the time-dependent internal electric field across the SiO₂ tunnel oxide with a maximum value at $t = 0$, d is the thickness of the tunnel oxide and ϕ_B is the barrier height of the MNC material. The internal electric field across the SiO₂ tunnel oxide is a result of trapped electrons in the potential well of MNC. At the moment V_{ini} is removed ($t = 0$), there is certain number of trapped electrons, and as these electrons leak out of the MNC ($t > 0$), internal electric field would drop. So $E_i(t)$ and J_1 both decay with time.

The other component of the MNC-induced J_{relax} is the charge leakage current that comes from the MNC-trapped electrons tunneling through the SiO₂ tunnel oxide and reaching the Si substrate (solid line in Fig. 4.7(b)). This charge leaking process is proposed to be quantum tunneling [16] since there is no external electric field on the stack and the SiO₂ oxide layer is relatively thin :

$$J_2 = J_2(t) \propto [E_i(t)d]^2 \exp[-b/E_i(t)d] \quad (4.4)$$

where J_2 is the time-dependent quantum tunneling current density, b is a constant, and $E_i(t)$ and d have the same meanings as in Eqn. (4.3). $E_i(t)$ and $J_2(t)$ also decay with time because of the fixed number of initial trapped electrons in the MNC. Both thermionic emission and quantum tunneling mechanisms could also result in electrons going toward the top electrode, but since only negative relaxation current is measured, these electrons may be annihilated or masked by the main electron flux. Similar to the SL MNC sample, both thermionic emission current J_1 and quantum tunneling current J_2 comprise the J_{relax} in DL MNC sample (see as shown in Fig. 4.8 (b)). The difference is that, there is considerable probability that the electrons released by thermionic emission from one layer of MNC could be re-trapped by another layer of MNC in the DL-MNC based gate stack. On the other hand, the quantum tunneling could happen not only from the electrons of the bottom layer of MNC1, but also via the two-time tunneling of the electrons of the top layer of MNC2. The possibility of the two-time tunneling is discussed as follows. At an equilibrium state, there is no net electric field in the ILD Al_2O_3 , as shown in the Fig. 4.8(b). However, as the electrons of MNC1 tunnel out, the charge equilibrium of the two layers are broken and a subtle internal electric field across the very thin ILD with a direction from MNC1 to MNC2 will arise. This internal electric field results in a finite probability for the electrons from MNC2 to tunnel through the ILD to MNC1, until a new equilibrium is established. Although occurrence of the thermionic emission current between MNC1 and MNC2 is also possible, the random nature of this process is assumed to produce no net current contribution. Thus, we expect that the contribution of J_2 to play a more dominant role in the total J_{relax} for the DL sample than the SL sample.

When the MNC-based gate stack was under V_{ini} before the relaxation current measurement, it is proposed that both thermionic emission current and quantum tunneling current contribute to the programming current. Eqn. (4.3) suggests T -dependence of the thermionic emission current. As the carrier density of the Si substrate also increases with T [8], the corresponding increase in the substrate conductivity implies for a given V_{ini} and stressing time, the programming current would be higher and more electrons get stored at the MNC (assuming they are not saturated). This implies that, $E_t(t=0)$ increases with T . This explains the slight increase of the first data point in the J_{relax} curve as increasing T in Fig. 4.4. In Fig. 4.5, the increase of J_{relax} at the first data point is significant because of the increased number for electron-trapping centres associated with the MNC. We propose that, in the SL sample, at the early stage of the relaxation current measurement, J_1 resulting from the trapped electrons released from the MNC dominates the behavior of J_{relax} . This is evidenced by the increasing slope n of the initial part of J_{relax} in Fig. 4.4 and a slightly decrease of the J_{10s} value in Fig. 4.6(a) with increasing T in the SL sample. As the J_1 electrons leaks out, the value of J_{relax} drops dramatically until a transition happens where J_2 becomes dominant in the tail part the J_{relax} . . Eqn. (4.4) suggests no T dependence of J_2 , so J_2 should decay with time at a fixed rate at all four temperatures. However, because of the increased programming current which results in extra amount of trapped electrons in the MNC, the total number of the trapped electrons increases with T . Thus, at certain time of the tail part of the relaxation, the residual charge in the gate stack increases with temperature, leading to a decreasing slope n in Fig. 4.4 and a slightly increasing J_{60s} in Fig. 4.6(b). In the case of DL MNC-based gate stack sample, as the J_1 component of J_{relax} is not as significant in the DL sample, we propose that the behavior of J_{relax} mainly arises from J_2 (no T dependence). In addition, there is an increased amount of trapped electrons with increasing T because of an extra

layer of MNCs. Thus, we can deduce that the residual charge in the DL MNC sample increases with T . As a result, a more significant decreasing of slope n in Fig. 4.5, as well as the increase of J_{10s} and J_{60s} in Figs. 4.6(a) and 4.6(b) with T , are observed in DL MNC sample. The increased fluctuation of the J_{relax} value at elevated temperatures in the DL sample could be attributed to the enhanced thermionic trapping and de-trapping of electrons between the two layers of MNCs.

4.3.3 Relaxation Current as a Reliability Characterization Tool

As indicated in Fig. 4.6, the main part of the relaxation current of the MNC-based gate stack comes from the MNC. As the MNC-induced relaxation current is basically the short-term leakage current of the trapped-charge in the MNC, the relaxation current can be used as a reliability tool to evaluate the short-term retention properties of the MNC. Here we define a discharge time constant τ as the time taken for the relaxation current to decay to 37% (or $1/e$) of its initial value [17]. The value of τ could be extracted from Fig. 4.4 and 4.5. This parameter provides an indication of the short-term charge retention property of MNC-based flash memory cells. The extracted values of τ are listed in Fig. 4.9 for the SL and DL MNC-based gate stack samples at four temperatures. Because of the different dominance in the relaxation current in the SL and DL samples discussed above, the τ values show different temperature dependence. It is noticed that at the temperature of 300K the value of τ of the DL sample is slightly larger than SL and control HK. A much larger τ value is observed for the DL sample at high temperatures than the SL, indicating a better short-term charge retention performance of the DL MNC-based high- κ /SiO₂ gate stack. This supports the enhancement of charge retention behavior by introducing an extra layer of MNC [2].

Figure 4.9. Discharge time constant τ of the SL and DL MNC-based gate stacks at four temperatures. SL and DL sample show different trend as T increases. DL samples have larger τ at all temperatures.

4.4 Summary

We have investigated the relaxation current behavior of high- κ /SiO₂ flash memory gate stacks embedded with SL and DL MNC at different temperatures. We observed a unique dual slope behavior in the log-log plot of the relaxation current transient as a function of discharge time for the SL MNC sample but correspondingly only a single slope behavior for the DL MNC-based gate stack. We propose a model to explain these behaviors based on a competition between the thermionic emission current and quantum tunneling current. Using this model, the dual-slope behavior for the SL sample arises from the respective dominance of the thermionic emission in the initial part, and quantum tunneling in the tail part of the relaxation current. Whereas the

single slope behavior of the DL sample is mainly attributed to the dominance of the quantum tunneling throughout the relaxation process. In addition, we also extracted a discharge time constant from the relaxation current which provides support for DL MNC-based gate stacks exhibiting better short-term charge retention property, especially at high temperatures.

REFERENCES

- [1] C. Y. Lu, K.Y. Hsieh and R. Liu, "Future challenges of flash memory technologies," *Microelectronic Engineering*, vol. 86, pp. 283-286, Mar 2009.
- [2] P. K. Singh, G. Bisht, K. Auluck, M. Sivatheja, R. Hofmann, K.K. Singh and S. Mahapatra, "Performance and Reliability Study of Single-Layer and Dual-Layer Platinum Nanocrystal Flash Memory Devices Under NAND Operation," *IEEE Transactions on Electron Devices*, vol. 57, pp. 1829-1837, Aug.
- [3] T. H. Hou, C.H. Lee, V. Narayanan, U. Ganguly and E.C. Kan, "Design optimization of metal nanocrystal memory - Part II: Gate-stack engineering," *IEEE Transactions on Electron Devices*, vol. 53, pp. 3103-3109, Dec 2006.
- [4] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna and Mahapatra, "Reliability of single and dual layer Pt nanocrystal devices for NAND flash applications: A 2-region model for endurance defect generation," Montreal, QC, Canada, 2009, pp. 301-306.
- [5] P. K. Singh, *et al.*, "Dual layer Pt metal nanocrystal flash for multi- level-cell NAND application," Piscataway, NJ, USA, 2009, p. 4 pp.
- [6] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna and Mahapatra, "Metal nanocrystal memory with pt single- and dual-layer NC with low-leakage Al₂O₃ blocking dielectric," *IEEE Electron Device Letters*, vol. 29, pp. 1389-91, 2008.
- [7] B. Mondal and S. K. Saha, "Hydrothermal synthesis of silver nanoshells: Formation and plasmon hybridization," *Journal of Materials Science*, vol. 46, pp. 5153-5159.
- [8] S. K. Samanta, P.K. Singh, J. Y. Won, G. Samudra, Y.C. Yeo, L.K. Bera and N. Balasubramanian, "Enhancement of memory window in short channel non-volatile memory devices using double layer tungsten nanocrystals," in *IEEE International Electron Devices Meeting 2005, Technical Digest*, ed, 2005, pp. 177-180.
- [9] A. K. Jonscher, "Dielectric relaxation in solids," *Journal of Physics D-Applied Physics*, vol. 32, pp. R57-R70, Jul 1999.
- [10] J. R. Jameson, W. Harrison, P.B. Griffin and J.D. Plummer, "Double-well model of dielectric relaxation current," *Applied Physics Letters*, vol. 84, pp. 3489-3491, May 2004.
- [11] M. Schumacher and R. Waser, "Curie-von Schweidler behaviour observed in ferroelectric thin films and comparison to superparaelectric thin film materials," Netherlands, 1998, pp. 109-21.
- [12] H. Reisinger, G. Steinlesberger, S. Jakschik, M. Gutsche, T. Hecht, M. Leonhard, U. Schroder, H. Seidl and D. Schumann, "A comparative study of dielectric relaxation losses in alternative dielectrics," Piscataway, NJ, USA, 2001, pp. 12-2.
- [13] L.-P. Chiang, N.K. Zous, T. Wang, T.E. Chang, K.Y. Shen and C. Huang, "Field and temperature effects on oxide charge detrapping in a metal-oxide-semiconductor field effect transistor by measuring a subthreshold current transient," *Applied Physics Letters*, vol. 71, pp. 1068-1070, 1997.
- [14] P. Beecher, A.J. Quinn, E.V. Shevchenko, H. Weller and G. Redmond, "Insulator-to-metal transition in nanocrystal assemblies driven by in situ mild thermal annealing," *Nano Letters*, vol. 4, pp. 1289-93, 2004.
- [15] C. Wagner and H. H. Soonpaa, "A simple picoammeter for thermionic emission measurements," *American Journal of Physics*, vol. 62, pp. 473-4, 1994.

- [16] S. Ju-Yong and L. Hai-Woong, "Quantum tunneling, dynamical symmetry, and quantum revival," *Physical Review E (Statistical Physics, Plasmas, Fluids, and Related Interdisciplinary Topics)*, vol. 53, pp. 3096-100, 1996.
- [17] Z. Z. Lwin, K.L. Pey, Y.N. Chen, P.K. Singh and S. Mahapatra, "Charging and Discharging Characteristics of Metal Nanocrystals in Degraded Dielectric Stacks," in *2010 International Reliability Physics Symposium*, ed, pp. 89-93.

CHAPTER FIVE

LATERAL CHARGING AND DEGRADATION OF SINGLE LAYER METAL NANOCRYSTAL-BASED HIGH- κ /SiO₂ GATE STACK

5.1 Introduction

One major advantage claimed for the MNC-based flash memory cell is the immunity to defects because of the discretely isolated charge-trapping media (i. e., MNCs), which are isolated by the inter-MNC control dielectric [1]. It is assumed that if there is a leakage path in the tunnel oxide, for the tradition floating gate flash memory cell, all the information stored in the floating gate will leak through the leakage path, as shown in Fig. 5.1(a). Whereas for the MNC-based flash memory cell, a similar leakage path in the tunnel oxide is supposed to only cause the information stored in local MNCs to leak, while the charges stored in other MNCs that are far from the leakage path remain intact.

A variety of studies have been reported on the dielectric BD, flash memory retention property and other reliability aspects of the MNC-based gate stack [2-4]. However, few studies have been reported for the interaction of the MNC in the lateral direction. In this chapter, we focus on the pre- and post-BD lateral charge distribution among the MNCs and the dielectric BD of inter-MNC Al₂O₃ in lateral direction.

Figure 5.1 Cross-sectional schematic of devices with a similar leakage path in the bottom tunnel oxide in case of (a) a traditional flash memory cell and (b) a NC-based memory cell.

5.2 Experimental Details

The sample used in this study was SL Ru MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack. The cross-sectional and planar view TEM [5] micrographs of the gate stack are shown in Figs. 5.2(a) and (b), respectively. The mean diameter of the MNC is approximately 3nm [6]. Notice that the thickness

of the TEM sample is 200nm, so the MNCs appear overlapped in Fig 5.2(a). The spacing of two adjacent MNCs is in the range of 2nm to 5nm, as shown in Fig. 5.2(b).

(a)

(b)

Figure 5.2 (a) Cross-sectional TEM and (b) planar view TEM [5] of SL Ru MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack.

We adopted the dual voltage sweep as the main characterization tool for the fresh and post-BD MNC-based gate stack. For a normal memory gate stack, an I - V hysteresis is expected in the dual voltage sweep. As mentioned in *Chapter Three*, this hysteresis can be used as sign of the functionality of the charge trapping and de-trapping of the floating gate (or MNC, in this case) in the flash memory gate stack [7]. We also monitor the magnitude of the leakage current I_{leak} in the dual voltage sweep, which was reflective of the the BD hardness. The BD was realized by CVS. The methodology of determining the magnitude of the V_{stress} is discussed in *Chapter Three*. The relaxation current I_{relax} was measured immediately after the removal of an initializing voltage of +3V on the fresh and post-BD samples to examine the dielectric property of the gate stacks.

5.3 Lateral Charging in the Soft Breakdown Metal Nanocrystal-based High- κ /SiO₂ Gate Stack

5.3.1 I - V Hysteresis Boost of Post-Soft Breakdown Ru Nanocrystal-based High- κ /SiO₂ Gate Stack

In order to study the charge/discharging effect of the MNC, a low level continuous dual voltage sweep (from -2V to +2V or from -3V to +3V) was performed on fresh and post-BD samples. A hysteresis was observed in I_{leak} between the positive and the negative voltage sweeps, as shown in Fig. 5.3 (a). The hysteresis is evident of electron trapping/de-trapping in the MNC, i. e., the memory effect. From Fig. 5.3(a), it is obvious that at the beginning of the positive direction sweep when V_{bias} swept from -2V towards positive direction, I_{leak} experienced an abrupt increase. This was when the discharging of the MNC occurred as the electrons tunneled from the MNC to

the Si substrate through the tunnel SiO_2 . Similar abrupt decrease was observed when V_{bias} swept from +2V towards negative direction, when electrons tunneled from Si substrate to the MNC through tunnel oxide. Fig. 5.3(b) shows the current difference (I_{dif}) between the positive and negative sweep. Except the initial and end parts of the dual voltage sweep where steep increase or decrease of the I_{leak} happened, a steady-state I_{dif} was found to be from 1pA to 1.5pA. The magnitude of the I_{dif} shows the current difference between the charging and discharging processes of the positive and negative direction voltage sweepings.

(a)

(b)

Figure 5.3. Dual sweep showing (a) I - V hysteresis on a fresh sample. The arrows show the sweep directions. Current difference I_{dif} is defined as value difference between the positive and the negative direction sweep. (b) I_{dif} between the positive and negative sweep.

(a)

(b)

Figure 5.4. Dual sweep showing (a) I - V hysteresis on fresh and SBD samples. The smaller arrows show the sweep directions. The hysteresis of the SBD sample shows larger window than the fresh one. (b) I_{dif} between the positive and negative sweep. Steady-state I_{dif} of the SBD samples is more than two orders larger than the fresh one.

Next we compare the dual voltage sweep data of a post-soft breakdown (SBD) device with that of the fresh device. The SBD was realized by a CVS of $V_{gstress}$ of +6.5V and I_{max} of 200nA. As shown in Fig. 5.4(a), the post-BD dual voltage sweep still shows a similar hysteresis as the fresh sample. We can see from Fig 5.4(b) that the I_{dif} of the SBD sample is in the range of 30pA to 40pA, much larger than the fresh gate stack.

Fig. 5.5 shows that the I_{relax} curve of the post-SBD sample is similar to that of the fresh sample. As discussed in *Chapter Four*, the contribution of the SiO₂ layer to the total I_{relax} is negligible. Thus the fresh-like I_{relax} curve of the SBD device indicates the integrity of the high- κ Al₂O₃ layer and MNCs. It has also been reported by our group that for a SBD case where the magnitude of I_{leak} is in the range of 1pA to 10pA, the gate stack encounters a one-layer BD [8]. So we assume that in our SBD case, only the SiO₂ tunnel oxide is broken down, while the other dielectric layer (Al₂O₃) remains intact.

Figure 5.5. Relaxation current of the fresh and SBD samples. The similarity of these two curves suggests that the SBD sample experienced an one-layer (SiO₂) BD.

The mechanism responsible for enlarged post-SBD I - V hysteresis is proposed as follows. When the top electrode is under a programming voltage, the majority of the I_{leak} arises from the electrons that are injected from the Si substrate and then flows through the BD percolation path in the tunnel oxide [9], charging the local MNCs. Local electric field is created in the inter-MNC Al_2O_3 dielectric between the charged and the un-charged MNC, as shown in the cross-sectional illustration in Fig. 5.6(a). As the top dielectric layer of the Al_2O_3 remains intact, there is finite probability that some of the electrons would flow laterally with the aid of the local electric field to the neighboring un-charged MNCs, until the empty energy states in these un-charged MNC are occupied, and a new local electric field is created among the newly charged and un-charged MNCs. Fig. 5.6(b) shows the band-diagram of the lateral charging process from the charged MNC to the un-charged MNC through the inter-MNC Al_2O_3 dielectric. As a result, there is slight band bending the inter-MNC Al_2O_3 dielectric.

It was estimated by our group in 2010 that the diameter of the lateral charging area in the MNC-based gate stack could be up to 380nm [8]. This value is almost one order larger than the BD area of the SiO_2 gate dielectric [10]. The phenomenon of the lateral charging induces further programming (and erasing) of the MNCs than the fresh case. The over-programming and over-erasing could contribute to the enhancement of I_{dif} window (and thus device memory capability). Another reason for the increase in the I_{dif} hysteresis window is that there are more traps in the defective dielectric [11], which can act as charge-trapping sites, thus enhancing the memory effect.

Figure 5.6. (a) Cross-sectional illustration shows that in the post-SBD sample, leakage current flows through the percolation path in the tunnel oxide, local electric field is created between the charged and uncharged MNC. (b) Band diagram shows that the local electric field causes electron charging in the MNC laterally.

(a)

(b)

Figure 5.7. Dual sweep showing (a) I - V hysteresis of the fresh and HBD samples. The smaller arrows show the sweep directions. The HBD sample shows no hysteresis. (b) I_{dif} between the positive and negative sweep. I_{dif} of the HBD is much smaller than the fresh one.

In the case of a hard breakdown (HBD) which was realized by a CVS of $V_{gstress}$ of +6.5V and I_{max} of 5 μ A, As shown in Fig. 5.7(a), the post-BD dual voltage sweep shows no hysteresis and the I_{leak} value is 4 to 5 orders larger than that of the fresh device. The current window I_{dif} in Fig. 5.7(b) is also zero, much smaller than the fresh case. This indicates that the sample has lost its charge-trapping capability. It is suggested that both the control oxide and tunnel oxide have been broken down, and a more conductive and larger percolation path than for the SBD case has been formed in the HBD sample [10]. This leakage path causes the device to lose its capability of memory effect.

5.3.2 Nanometer-scale Lateral Propagation of HBD Area

Next, we study the post-BD Ru MNC-based Al_2O_3/SiO_2 gate stack at nanometer-scale. This set of experiments was conducted in Zyvex KZ100 Nanomanipulator/Prober on nanometer-scale Au/Cr electrodes illustrated in Fig. 3.2. Fig. 5.8 shows a SEM micrograph of a tungsten (W) tip probing a Au/Cr nanometer-scale electrode.

Figure 5.8. Nanometer-scale probing on Au/Cr nanometer-scale electrode with a W probe under SEM.

In this experiment, we chose the nanometer-scale electrodes that have the same area (same diameter of 200nm) and different spacings, as shown in Fig. 5.9. We induced a BD in one of nanometer-scale electrodes by CVS, and examined the I - V characteristics using a dual voltage sweep of the adjacent nanometer-scale electrodes that have different distances away from the BD dot. A dual voltage sweep of -2V to 2V was carried out on all the pre-stressed nanometer-scale dots to ensure the functionality and integrity of the dielectric layers under the nanometer-scale electrodes.

Figure 5.9. SEM micrograph showing nanometer-scale Au/Cr electrodes with same area but different spacings.

As illustrated in Fig. 5.10, a CVS test was carried out with $V_{stress} = +6.5V$ and $I_{max} = 5\mu A$ on one nanometer-scale electrode D2 to bring a HBD on the local gate stack. An un-stressed nanometer-scale electrode (D1) which is 30nm to the left of the BD dot also exhibits a HBD-like curve, though the breakdown hardness (in terms of $I_{leak}@V_{bias}=2V$) is smaller than the stressed dot. This indicates that a conductive path is already formed between this nanometer-scale electrode and the substrate, even though D1 was never stressed by a bias voltage. Another un-stressed nanometer-scale electrode (D3) that is 60nm to the right of the BD dot shows a SBD-like curve. The dual voltage sweep on D3 shows that the $I-V$ hysteresis remains from -1V to 2V, but I_{leak} shows a steep and non-stable increase for voltages below -1V. This indicates that the un-stressed local dielectrics under the D3 electrode have degraded.

Figure 5.10. After the CVS ($V_{\text{stress}} = 6.5\text{V}$, and $I_{\text{max}} = 5\mu\text{A}$) on nanometer-scale electrode D2, the dual voltage sweep curve shows HBD behavior. The dual sweep of an un-stressed D1 which is 30nm away to the left of the BD dot (D2) shows a HBD characteristic. For another un-stressed nanometer-scale dot D3 which is 60nm away to the right of the BD dot, a SBD curve is observed. All dots are of 200nm in diameter.

Figure 5.11. After CVS ($V_{\text{stress}} = 6.5\text{V}$, and $I_{\text{max}} = 5\mu\text{A}$) on D5, the dual voltage sweep curve shows HBD behavior. The dual sweep of an un-stressed nanometer-scale electrode D4 which is 120nm away to the left of the BD dot shows a SBD-like behavior. For another un-stressed nanometer-scale electrode D6 which is 150nm away to the right of the BD dot (D5), a fresh-like curve is observed. All dots are of 200nm in diameter.

A similar experiment was conducted on another equivalent sample. A HBD on a nanometer electrode D5 was realized by a CVS under a similar condition ($V_{stress} = + 6.5V$ and $I_{max} = 5\mu A$). Fig 5.11 confirms that the dual voltage sweep curve of the stressed D5 shows a HBD behavior. It is observed that an un-stressed nanometer-scale electrode D4 that is 120nm to the left of the BD dot exhibits a SBD-like curve. Another nanometer-scale electrode D6, which is 150nm to the right of D5, the dual voltage sweep curve shows no degradation, i. e. a fresh-like behavior was observed.

From Fig. 5.10 and Fig. 5.11, we can see that when we induced a HBD on a nanometer-scale electrode on the MNC-based Al_2O_3/SiO_2 gate stack, the BD area propagated laterally, to a distance of at least 120nm. This value is much larger than the diameter of the percolation path for a HBD case in the SiO_2 gate dielectric [10]. The mechanism of the lateral propagation of the BD area in the MNC-based gate stack is proposed as follows. Upon a BD in the dielectric layers, majority of the leakage current arise from the electrons that are injected from the Si substrate and flow through the percolation path. A local electric field between the sandwiched Al_2O_3 dielectric between the charged and the uncharged MNC as discussed in Section 5.3.1. The band bending of sandwiched Al_2O_3 dielectric between the MNCs would increase the probability of the electrons to tunnel through the potential barriers in the lateral direction. The electrons in the percolation path only need to overcome a thin sandwiched Al_2O_3 dielectric to reach an adjacent MNC, which would serve as a sink for the extra electrons from the percolation path. This lateral transport of electron flows would facilitate the dielectric BD of the inter-MNC Al_2O_3 . As the I_{leak} increased from a SBD level to HBD level, these laterally-injected electrons would act as hot electrons and bring defects in the thin inter-MNC Al_2O_3 dielectric and eventually led to a dielectric BD, thus accelerating the lateral propagation of the defected area. It should be mentioned that in some

similar experiments, after the HBD of a nanometer-scale electrode, a nearer dot may exhibit more severe BD than a farther electrode, indicating that the lateral propagation of the BD area is not ideally a circle-shape. We can see from the planar view TEM of the MNC layer (Fig. 5.2 (b)) that the size of and spacing among MNCs vary, which could cause the non-circular propagation of the BD area. Besides of the fact that of the randomness of the MNC distribution, irregular grain boundary orientation in the Al_2O_3 layer, which is believed to be a vulnerable part in a high- κ film in a dielectric BD event [12], is assumed to be another reason.

The lateral propagation of the BD area puts a serious problem in the adopting of the MNC-based gate stack as the future memory cell candidate, as our results show that the discreteness of the information storage centres and thus the immunity to local defect are likely overestimated. Further optimization in the engineering of the control oxide (so the inter-MNC dielectric), size and spacing of the MNC (thus density of the MNC) are required for this kind of memory cell to be realized at 22nm node or further.

5.4 Summary

In summary, lateral charging and BD area lateral propagation of SBD and HBD single layer Ru MNC-based $\text{SiO}_2/\text{Al}_2\text{O}_3$ gate stacks have been studied. The enhanced I - V hysteresis of the post-SBD gate stack is believed to be due to the lateral charging of the MNCs by the current that flows through the BD percolation path in the tunnel oxide of SiO_2 layer. The nanometer-level characterization results show that the local defective area of a HBD would propagate laterally to the neighboring area. It is proposed that unbalanced potential between the charged MNC and the un-charged MNC would facilitate the thin inter-MNC dielectric to breakdown. These findings

bring new insights into the performance of the MNC-based gate stack and challenges of using this kind of structure as a future memory cell candidate.

References

- [1] S. Tiwari, "Silicon nano-crystal memories: Devices in the limit of conventional miniaturization," in *3rd International Symposium on the Physics and Chemistry of SiO(2) and the Si-SiO(2) Interface. at the Spring Meeting of the Electrochemical-Society*, Los Angeles, Ca, 1996, pp. 250-259.
- [2] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna and Mahapatra, "Metal nanocrystal memory with Pt single- and dual-layer NC with low-leakage Al₂O₃ blocking dielectric," *IEEE Electron Device Letters*, vol. 29, pp. 1389-1391, 2008.
- [3] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories - Part I: Device design and fabrication," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1606-1613, Sep 2002.
- [4] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories-part II: electrical characteristics," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1614-22, 2002.
- [5] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna and Mahapatra, "Reliability of single and dual layer Pt nanocrystal devices for NAND flash applications: A 2-region model for endurance defect generation," Montreal, QC, Canada, 2009, pp. 301-306.
- [6] S. K. Samanta, P.K. Singh, J. Y. Won, G. Samudra, Y.C. Yeo, L.K. Bera and N. Balasubramanian,, "Enhancement of memory window in short channel non-volatile memory devices using double layer tungsten nanocrystals," in *IEEE International Electron Devices Meeting 2005, Technical Digest*, ed, 2005, pp. 177-180.
- [7] J.S. Lyu, B.W. Kim, K.H. Kim, J.Y. Cha and H.J. Yoo, "Metal-ferroelectric-semiconductor field-effect transistor (MPSFET) for single transistor memory by using Poly-Si source/drain and BaMgF/sub 4/ dielectric," in *Electron Devices Meeting, 1996. IEDM '96., International*, 1996, pp. 503-506.
- [8] Z. Z. Lwin, K.L. Pey, Y.N. Chen, P.K. Singh and S. Mahapatra, "Charging and Discharging Characteristics of Metal Nanocrystals in Degraded Dielectric Stacks," in *2010 International Reliability Physics Symposium*, ed, pp. 89-93.
- [9] J. Sune, I. Placencia, N. Barnoil, E. Farres, F. Martin and X. Aymerich, "On the breakdown statistics of very thin SiO₂ films," *Thin Solid Films*, vol. 185, pp. 347-62, 1990.
- [10] X. Li, C.H. Tung and K.L. Pey, "The radial distribution of defects in a percolation path," *Applied Physics Letters*, vol. 93, 2008.
- [11] R. Ranjan, *et al.*, "Failure defects observed in post-breakdown high-k/metal gate stack MOSFET," Piscataway, NJ, USA, 2006, p. 5 pp.
- [12] K. Shubhakar, *et al.*, "Grain boundary assisted degradation and breakdown study in cerium oxide gate dielectric using scanning tunneling microscopy," *Applied Physics Letters*, vol. 98.

CHAPTER SIX

RECOVERY OF POST-BREAKDOWN IN SINGLE LAYER METAL NANOCRYSTAL-BASED HIGH- κ /SiO₂ GATE STACK

6.1 Introduction

Majority of reliability research on the MNC-based memory cell gate stack focuses on the pre-BD stage [1-3]. After the BD, the gate stack is considered broken or malfunctioned. Few studies have been reported on the post-BD stage. The recovery (RC) of a logic MOSFET after the BD has been reported by our group in 2009 [4]. However, the idea of re-use the broken-down device by “recovering” it has not been reported on the MNC-based high- κ /SiO₂ flash memory gate stacks.

In this chapter, we will present the RC on post-BD metal MNC-based high- κ /SiO₂ gate stack. The phenomena of RC on the leakage current as well as relaxation current by electrical and thermal methods after the gate stack has experienced a SBD or HBD are demonstrated. The mechanisms of different recoveries are discussed. These findings bring significant understandings on prolonging the reliability margin of MNC-based flash memory gate stacks.

6.2 Experimental Details

Gate stacks of capacitor structure adopting single layer of Ru MNCs as charge trapping media with a high- κ Al₂O₃ as a control oxide and a SiO₂ layer as a tunnel oxide were used in our

studies. Fig. 6.1(a) is the TEM micrograph showing the cross-section of the gate stack. For the single layer (SL) sample, a layer of 6nm Al_2O_3 was then deposited as the by PVD control oxide. The randomly distributed Ru MNCs locate above the SiO_2 and are embedded in the Al_2O_3 layer. As the mean diameter of the MNCs is about approximately 3nm [5] and the TEM sample thickness is 200nm, the MNCs seem to be overlapped. The thickness of the high- κ control oxide layer (including the MNCs) is 6nm and the SiO_2 tunnel oxide layer is 4nm. The planar view TEM micrograph [6] of Fig. 6.1(b) shows the individually isolated MNCs. The density of the MNCs is calculated to be about $3 \times 10^{12} \text{ cm}^{-2}$ [5]. In addition, Au dots of 300nm thickness are deposited on top of the layer as top electrodes. The diameter of the Au electrodes was chosen to be $160\mu\text{m}$ so that the area of each capacitor is large enough to detect reasonable relaxation current I_{relax} .

Figure 6.1. (a) TEM micrograph showing the cross-section of gate stack gate stacks with Ru MNCs embedded above the $\text{Al}_2\text{O}_3/\text{SiO}_2$ interface. (b) Planar TEM showing the individually embedded MNCs [6].

The capacitor was stressed using an improved K-cycle multiple stage CVS. In the beginning of each cycle, the electrical data of dual I - V voltage sweep and I_{relax} measurement was collected to examine the functionality of the MNC-based gate stack. The dual voltage sweep ranged from 0 to +2V or -2V in the substrate injection or gate injection mode, respectively (depending on the polarity of the V_{stress}). The initial voltage of the I_{relax} was 3V and its polarity was the same as V_{stress} , which was to avoid any possible RC effect induced by the initial voltage in the I_{relax} measurement. After measuring the dual voltage sweep and I_{relax} of the fresh sample, the dielectric BD of the gate stack was realized with a high constant stressing voltage V_{stress} in either substrate or gate injection mode at the room temperature. The V_{stress} for the first BD was chosen to be +6.5V or -6.5V in the substrate injection or gate injection mode, respectively. The value of the V_{stress} is determined by the methodology described in *Chapter Three*. From the 2nd cycle on, a relatively lower V_{stress} (+5V or -5V) was used to stress the gate stack for the consequent BD. This was because that even though the gate stack was recovered, the quality of the control and tunnel dielectric layers were not as good as that of the fresh state. Furthermore, a lower V_{stress} enabled us to prolong the time-to-breakdown (t_{BD}), allowing us to study the characteristics of at the different stages of progressive breakdown. As shown in Fig. 6.2, a low current compliance limit I_{max} in the range of 100nA~10 μ A was used to limit the flow of I_{leak} through a percolation path formed within the gate stack such that BDs with different degree of harness can be captured. When each BD was achieved, after collecting the dual I - V and I_{relax} data again, a RC voltage stressing with either a positive or a negative recovery voltage (V_{RC}) was applied for t_{RC} , trying to bring a total or partial RC of the broken-down gate stack. The value of V_{RC} was +4V or -4V. The t_{RC} for all RC stressing was chosen to be 10s. The value of the t_{RC} was

selected as a tradeoff between the effective RC and short experimental time, after performing similar experiments on 20 equivalent samples.

Figure 6.2. The plot of leakage current I_{leak} under constant voltage stressing of V_{stress} . A compliance current limit I_{max} was used to arrest the stack under different BD hardness.

We depicted the dual voltage sweep I - V curve and I_{relax} curve after each BD or RC stage, and we picked the absolute value of the I_{leak} in the dual I - V curve at bias voltage V_{bias} of 2V ($|I_{leak}|@V_{bias} = 2V$) to show the electrical characteristics of the gate stack that reflect the dielectric

properties of both the control and tunnel oxide layers. The implementation of an improved K-cycle multiple stage CVS has been discussed in details in *Chapter Three*.

6.3 Polarity-dependent Electrical Recovery on Control and Tunnel Oxide Layers

It was mentioned in *Chapter four* that the I_{relax} magnitude of the SiO₂ layer is at least one or two orders smaller than the high- κ film [7]. Thus, in our gate stack system consisting of high- κ /SiO₂ embedded with MNC, the contribution of the SiO₂ layer to the total I_{relax} is negligible compared to that of the high- κ layer. In this study, we assume that the I_{relax} is mainly contributed by the high- κ Al₂O₃ dielectric and the embedded MNCs. As discussed in *Chapter Four*, we propose that the component of I_{relax} that comes from the high- κ dielectric arises from the local dipole re-arrangement and the part from the MNCs comes from charge de-trapping from the potential well of MNCs and the surrounding high- κ Al₂O₃ dielectric. Thus, the I_{relax} signal reflects primarily the dielectric integrity of the Al₂O₃ layer (embedded with MNCs). In other words, the curve of I_{relax} could be used as a sign that indicates whether the high- κ film was at its broken-down or recovered state.

6.3.1 Application of Positive V_{RC} : Partial RC of SBD

In the dual voltage sweep measurement, the absolute value of the leakage current at the bias voltage on the top electrode V_{bias} of 2V ($|I_{leak}|@|V_{bias}|=2V$) for the fresh MNC-based high- κ /SiO₂ gate stack was around 10pA, as shown in Fig. 6.3(a). We use this absolute value of the leakage

current under the bias voltage of +2V (or -2V in the gate injection mode) as a reference to show the hardness of the BD.

It can be seen from Fig. 6.3(b) that I_{relax} of the fresh single layer Ru MNC-based gate stack generally decays exponentially with time:

$$I_{relax} = at^{-n} \quad (6.1)$$

where I_{relax} is the relaxation current, t is the time, a and n are both constants. As discussed in *Chapter Four*, this behavior is similar to the pure dielectric relaxation behavior of Curie-von Schweidler law [8].

To study the RC behavior, the MNC-based capacitor was firstly brought to a SBD using CVS with $V_{stress} = -6.5V$ and a compliance current limit I_{max} of 200nA. After the BD, the Curie-von Schweidler-like behavior of the I_{relax} disappeared, as shown in the right inset of Fig. 6.3(a). Instead, as we can see from Fig. 6.3(b), the post-BD I_{relax} did not decay with time as the Curie-von-Schweidler law, and the magnitude of the post-BD I_{relax} was almost one order larger than the fresh one, which shows a typical dielectric BD behavior [9].

(a)

(b)

Figure 6.3. Partial RC of SBD with positive RC voltage (a) $|I_{leak}|@|V_{bias}| = 2V$ (the insets show the existence of hysteresis in the fresh sample, but not in the BD sample) (b) I_{relax} of the fresh gate stack, after BD and after RC. The BD event used $V_{stress} = -6.5V$ and $I_{max} = 200nA$. The RC event used $V_{RC} = +4V$.

The RC phenomenon was first observed when the broken-down gate stack was stressed with a small magnitude constant voltage V_{RC} . The RC could be reflected both in terms of the leakage current I_{leak} and relaxation current I_{relax} . In the first RC attempt, we only used the positive V_{RC} of +4V for a $t_{RC} = 10$ s. After adopting the V_{RC} stressing, the I_{relax} curve returned to the fresh-like behavior. We can see from Fig. 6.3(b) that the post-RC I_{relax} curve behavior becomes similar to that of the fresh gate stack. Fig. 6.3(a) shows that the $|I_{leak}|@|V_{bias}| = 2$ V after the BD was about 3 orders larger than the fresh one, indicating the loss of dielectric property of the gate stack. After the RC, however, the $|I_{leak}|@|V_{bias}| = 2$ V was still 10 times larger than that of the fresh sample. It is suggested that the dielectric properties of the tunneling or control oxide have not been restored totally, i. e., a “partial recovery” was achieved. The fact that the I_{relax} after the RC voltage stressing almost overlapped with that of the fresh device suggests that the control oxide of the high- κ Al_2O_3 layer had been fully recovered to a fresh-like condition. Whereas the fact that the total leakage current was approximately one order larger than the fresh device suggests that the bottom tunnel oxide layer (SiO_2) is still broken-down.

6.3.2 Application of Negative V_{RC} : Full RC of SBD

In a second RC attempt, we applied a negative V_{RC} to the gate stack which had two BDs with low I_{max} . The first BD (BD1) was realized with a CVS of $V_{stress} = +6.5$ V and a low $I_{max} = 200$ nA. The second BD (BD2) had a V_{stress} of +5V and a low I_{max} of 100nA. The first RC event (RC1) used a negative V_{RC} of -4V and was conducted immediately after BD1. The second RC stressing (RC2) was applied after BD2 also with a negative V_{RC} of -4V. The RC2 was conducted after the BD2. Dual voltage sweep in a range of 0 to +2V was used after each BD and RC. The initial voltage of the I_{relax} measurement was +3V.

Fig. 6.4 compares the I_{leak} and I_{relax} of the gate stack recovered by the two RC events after the two SBDs both with low I_{max} . Fig. 6.4 (a) shows that after BD1, the value of $|I_{leak}|@|V_{bias}|=2V$ was more than 2 orders larger than that of the fresh gate stack. And the hysteresis in the dual voltage sweep had disappeared, similar to the case in Fig. 6.3(a). In Fig. 6.4(b), we can see that I_{relax} of the BD1 was a non-decaying high leakage current, similar to Fig. 6.3(b). After RC1, Fig. 6.4(a) shows that the value of $|I_{leak}|@|V_{bias}|=2V$ had decreased for about one order, but it was still more than one order larger than the fresh gate stack. Furthermore, as shown in Fig. 6.4(b), the I_{relax} still did not follow the linear-log Curie-von Schweidler-like behavior. Thus a partial recovery of the gate stack was realized in this case. A BD2 which is softer than BD1 was achieved after RC1. Figures 6.4(a) and (b) show that the leakage current increases again to a value smaller than BD1. And the I_{relax} curve exhibited a fluctuating behavior with an average magnitude smaller than that of BD1 but still higher than the fresh condition. The fluctuation is assumed to arise from the charge trapping/de-trapping in the potential wells of the MNC embedded in the oxide. Both $|I_{leak}|@|V_{bias}|=2V$ and I_{relax} behaviors are typical in soft BD MNC-based gate stack.

Figure 6.4. Full RC of SBD with negative RC voltages: (a) $|I_{leak}|@|V_{bias}|=2V$ (the inset shows that the fully recovered I - V resembles fresh device), (b) I_{relax} of fresh device, after BD and after RC; $V_{stress} = +6.5V$, $I_{max} = 200nA$ and $100nA$, respectively in BD1 and BD2. $V_{RC} = -4V$ in both RC1 and RC2.

A RC2 with the same negative V_{RC} was applied the gate stack after RC1. We can see from Fig. 6.4(a) that after RC2, the magnitude of $|I_{leak}|@|V_{bias}|=2V$ decreased to a value which was almost the same as the fresh one. The inset showed that the I - V curve after RC2 almost overlapped with that of the fresh device in the dual voltage sweep and the hysteresis was restored. Fig 6.4 (b) shows that I_{relax} curve after RC2 was fully recovered to resemble the fresh-like performance.

6.3.3 Application Bipolar V_{RC} : Full RC of HBD

In the third RC experiment, we applied both negative and positive V_{RC} to the gate stack which had experienced three BDs of high I_{max} and r RC attempts with bipolar polarities of V_{RC} . The BD1 was realized with CVS of $V_{stress} = +6.5V$ and a high $I_{max} = 10\mu A$. The BD2 had a V_{stress} of $+5V$ and a slightly lower I_{max} of $5\mu A$. The first RC event (RC1) used a negative V_{RC} of $-4V$ and was conducted after BD1, followed by a second RC event (RC2) with a positive V_{RC} of $+4V$. The RC3, however, was applied after BD2 with a negative V_{RC} of $-4V$. The RC3 was conducted after the BD2. The dual voltage sweep used a range of 0 to $+2V$. The initial voltage of the I_{relax} measurement was $+3V$.

Fig. 6.5 compares the I_{leak} and I_{relax} of the gate stack recovered by the three RC events with after the two HBDs with high I_{max} . Fig. 6.5(a) shows that after BD1, the value of $|I_{leak}|@|V_{bias}|=2V$ became more than 3 orders larger than the value of the fresh gate stack. And the hysteresis in the dual I - V voltage sweep had disappeared, similar to the case in Fig. 6.3(a). After RC1 with negative V_{RC} , the value of $|I_{leak}|@|V_{bias}|=2V$ had decreased for about one order, but was still more than one order larger than the fresh gate stack. In Fig. 6.5(b), we can see that I_{relax} of the

BD1 was a non-decaying current with a high magnitude, similar to Fig. 6.3(b). After RC1, the I_{relax} curve was recovered to be similar to the Curie-von Schweidler-like behavior. A RC2 stressing with positive V_{RC} of +4V (i. e., bipolar recovery) was carried out after RC1. We can see that further decrease of the value $|I_{leak}|@|V_{bias}|=2V$ was observed, but it was still larger than the fresh. The I_{relax} curve had restored to resemble the fresh behavior. A second BD (BD2) was achieved with $V_{stress} = +5V$ and half the I_{max} (5 μA) compared to BD1. This is to ensure that the BD would not be too severe to recover. A RC3 with negative V_{RC} of -4V was performed after the BD2, and we can see from Fig. 6.5 that from that the I_{leak} magnitude, I - V hysteresis and I_{relax} behavior were all fully recovered to resemble the fresh-like behavior.

(a)

(b)

Figure 6.5. Full RC of HBD with RC voltages of both polarity: (a) $|I_{leak}|@|V_{bias}| = 2V$ (the inset shows that the fully recovered I - V resembles the fresh sample). (b) I_{relax} of fresh device, after BD and after RC; the BD1 and BD2 used $V_{stress} = +6.5V$, $I_{max} = 10\mu A$ and $5\mu A$, respectively. RC1 ($V_{RC} = -4V$) and RC2 ($V_{RC} = +4V$) were performed after BD1 and RC3 ($V_{RC} = -4V$) was performed after BD2.

6.3.4 Proposed Physical Model of Electrical Recovery

We now propose a physical model to explain the RC mechanism. Fig. 6.6(a) shows a cross-sectional illustration of the single layer Ru MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack at its fresh condition. We previously reported that upon electrical BD in a gate dielectric layer, a percolation path consisting of oxygen vacancies (V_o) is formed (Fig. 6.6(b)), resulting in large I_{leak} [10]. The amount of V_o in the percolation path increases with BD hardness [11, 12]. The expelled oxygen travels in the form of ions (O^{2-}), and can be trapped in the potential wells of the metal/oxide interfaces: Au electrode/oxide and Ru MNC/oxide. They act as two types of O^{2-} reservoirs [13]. Given the fact that the MNCs are nanometer-scale spheres with average diameter of about 3nm (Fig. 6.1(b)) and a density of $\sim 3 \times 10^{12} \text{ cm}^{-2}$, the MNC/oxide interface has larger effective surface area per unit volume than that of the Au electrode/oxide interface, and hence stores a larger amount of O^{2-} . V_o could either be neutral or positively charged (V_o^{2+} , with electrons depleted).

Under a negative V_{RC} (Fig. 6.6(c)), the neutral V_o are depleted, increasing the capture cross-section of O^{2-} , while the O^{2-} ions de-trap from the two O^{2-} reservoirs and travel towards the anode side (substrate). Because of the larger amount of trapped O^{2-} and smaller work function (hence shallower potential well for O^{2-} to de-trap) of the MNC material (Ru, 4.71eV) compared to the metal gate material (Au, 5eV), more O^{2-} ions are released from the MNC/oxide interfaces than that of the gate/oxide. V_o annihilation is realized when an electron depleted V_o^{2+} captures an O^{2-} ($\text{V}_\text{o}^{2+} + \text{O}^{2-} = \text{O}_\text{o}$), similar to what happened at the NiSi gate with SiON or HfO_2 gate dielectric reported by Liu W. H. *et al.* [4]. Thus minor and major V_o annihilation occur in the top Al_2O_3 and bottom SiO_2 layers respectively.

Whereas under a positive V_{RC} (Fig. 6.6(d)), only O^{2-} in the MNC/oxide interface can move towards the anode side (Au electrode). Whereas the O^{2-} ions at the Au electrode/ Al_2O_3 interface cannot penetrate into the Au electrode as interstitial defects or form oxide with Au, thus they remain at the interface. In this case, V_o annihilation happens only in the top Al_2O_3 layer. The percolation path in Al_2O_3 and SiO_2 layers can then be “switched off” when enough oxygen vacancies are passivated to prevent electron-hopping. The amount of V_o in the percolation path of soft BD is relatively small, so the application of a negative V_{RC} (minor and major repair in Al_2O_3 and SiO_2) enables realization of a full RC (the Fig. 6.4 case), while a positive V_{RC} causes RC only in the Al_2O_3 high- κ layer (as in the case of Fig. 6.3) . For a harder BD, V_{RC} of both polarities are required to fully passivate the percolation path in two oxide layers (see Fig. 6.5). It is suggested that the voltage stressing (i. e., external electric field) brings about two competing mechanisms in the dielectric layers. One mechanism causes the dielectric to undergo electrical BD, oxygen vacancies are being created in the dielectric. This mechanism is more significant if the external electric field is high. The other mechanism is to move the negative-charged O^{2-} ions and may bond them back to the oxygen vacancies V_o and this is a recovery mechanism.

Figure 6.6. Schematic models showing the Au electrode/ Al_2O_3 (with embedded MNCs)/ SiO_2 /Si substrate gate stack at (a) fresh condition, (b) BD condition (c) negative V_{RC} , leading to minor and major V_o annihilation in Al_2O_3 and SiO_2 layers respectively, and (d) positive V_{RC} providing V_o annihilation only in Al_2O_3 layer.

The fact that full RC often happened after the second or third BD is suggested to be related to the elevated local temperature in the BD percolation path which is a result of Joule heating of the BD events. It is believed that increased temperature in the percolation path causes an increase in the mobility of the trapped O^{2-} ions, which leads to increased probability of de-trapping of the O^{2-} ions from the MNC/oxide potential wells, and passivating of the BD path. The temperature effect of the post-BD recovery is discussed in detail in the following in *Section 6.4*.

6.3.4 Non-recoverability

The electrical recovery effect has so far not been observed in harder BD with ultra-high I_{max} more than 20 μ A. We believed that there are other structural defects apart from oxygen vacancy that are so far irreversible are being created in the gate stack. Such structural damages could include dielectric-breakdown-induced epitaxy (DBIE) in the Si substrate/SiO₂ interface [14], and/or metal-like filament formation of the percolation path [15].

6.4 Automatic RC

Besides the electrical RC by V_{RC} , we also discovered automatic RC in much softer BDs with a relatively long time-to-breakdown (t_{BD}). In this section, we discuss the phenomena of automatic recovery of leakage current. The mechanism of the automatic recovery was verified by the high temperature measurements. A physical model is proposed.

6.4.1 Automatic RC on I_{leak} of low I_{max} SBD

The auto-recovery was first observed after the BD1 under the CVS at room temperature with a low I_{max} of 10nA. Fig. 6.7(a) shows that the t_{BD} of the BD1 happened at 2033s. The same CVS

was resumed after BD1 and the I_{leak} level recovered from a very leaky stage to a level comparable to the pre-stress state, before it subsequently increased to I_{max} again (BD2). The t_{BD} of BD2 is 982s, much less than that of BD1. This process was repeated and again auto-recovery of I_{leak} was observed, before detecting a third BD (BD3) with a t_{BD} of 509s. Though the I_{leak} recovered to the same level each time, the fact that t_{BD} became shorter for CVS2 and CVS3 indicates the likely deteriorating quality of the dielectric layers [16] caused by the dielectric BD events. We found that the full auto-recovery of I_{leak} to its pre-stress level was no longer observed after the 6th BD for most of the samples studied.

Figure 6.7. Room temperature constant voltage stressing ($V_{stress} = 6.5V$) with different I_{max} . (a) $I_{max} = 10nA$, auto-recovery of I_{leak} back to the pre-stress current level after the BD1 and BD2. (b) $I_{max} = 10nA$, auto-recovery of I_{leak} back to the pre-stress level is observed only after the BD1, and automatic partial recovery found after the BD2. (c) $I_{max} = 100nA$, automatic partial recovery is observed after the BD1, no recovery after the BD2. The inset shows the detailed I_{leak} behavior.

Even for harder BD with an increased I_{max} of 50nA, as shown in Fig. 6.7(b), the auto-recovery was still observed after BD1. However, in this case, after BD2, the I_{leak} returned to the pre-stress level but then increased gradually to 10nA, then finally reached the I_{max} of 50nA upon the subsequent CVS. In the case of $I_{max} = 100\text{nA}$, (Fig. 6.7(c)), significant auto-recovery of I_{leak} was not achieved after BD1. The post-BD I_{leak} is about 200 times higher than that before BD. After CVS2, we found that the t_{BD} value (252s) of BD2 was significantly less than that of the first t_{BD} (2209s). When a CVS3 was carried out, the I_{leak} was likely well beyond the compliance of 100nA under CVS of 6.5V since I_{leak} immediately attained the compliance level (i. e., BD3) which was a typical post-BD dielectric behavior, and no auto-recovery was observed.

6.4.2 Thermal RC

To further investigate the mechanism of the automatic RC, we studied in detail the temperature dependence of I_{leak} and I_{relax} for the broken-down sample that was used in Fig. 6.7(c). We measured its fresh and post-BD I_{leak} at a low stress voltage of 2V and the I_{relax} at room temperature and elevated temperatures of 125°C and 225°C (each with a duration for one minute before carrying out measurements), respectively. Fig. 6.8(a) shows that I_{leak} decreased when the stack was heated to 125°C and a further reduction was observed at 225°C. When the stack was cooled down to the room temperature again, the post-BD I_{leak} had decreased from the original value of 208nA to 94pA, although this value was still about one order of magnitude higher than that of the pre-stress I_{leak} .

(a)

(b)

Figure 6.8. Device characterization at room and elevated temperatures (Sample used was the capacitor stack broken down beyond auto-recovery in Figure 6.7(c)). **(a)** Capacitor leakage current $I_{leak} @ V_{bias} = 2V$ shows significant reduction after going through higher temperature (125°C and 225°C) anneal, and the final I_{leak} at room temperature is almost one order higher than the pres-stress level; **(b)** a full RC of I_{relax} is observed after the high temperature anneal, suggesting significant passivation of the BD percolation path in the Al_2O_3 high- κ layer.

It can be seen from Fig. 6.8(b) that the double-log plot of the fresh I_{relax} at room temperature is linear with respect to the measurement time (black squares), indicating a typical dielectric relaxation behavior according to the Curie-von Schweidler law [8]. This behavior was not been observed immediately after BD (red dot). However, after going through a thermal cycle of 125°C and 225°C and then finally cooled down to 25°C, we found that the I_{relax} curve of the post-BD stack (magenta left triangles) essentially overlapped that of the pre-stress state in Fig. 6.8(b). As mentioned above that the contribution of the SiO₂ layer to the total I_{relax} is negligible because of its small magnitude and quick decay time constant as compared to that of high- κ layer [7]. Thus, the I_{relax} of the gate stack reflects primarily the dielectric integrity of the Al₂O₃ high- κ layer. The I_{relax} behavior in Fig. 6.8(b) suggests that the Al₂O₃ layer has significantly recovered to a state comparable to its pre-stress level. Since the capacitance leakage current $I_{leak}@V_{bias}=2V$ of the stack is still almost one order higher than that of the pre-stress case, as shown in Fig. 6.8(a), it is likely that the SiO₂ layer did not significantly recover from the BD. Note that we also found that there was no further recovery of I_{leak} even if the sample was subjected to a higher temperature cycle up to 325° C.

6.4.3. Physical Explanation of Automatic Recovery

Based on the studies of I_{leak} and I_{relax} at elevated temperatures, we propose an explanation for the automatic RC mechanism in the MNC-based high- κ /SiO₂ stack after multiple cycle CVSs. As discussed in *Section 3.3.4*, a BD event occurs by forming a percolation path consisting of oxygen vacancies V_o in the stack oxide, resulting in large I_{leak} [10]. The amount of V_o in the percolation path increases with increasing BD hardness [11, 12]. The expelled oxygen atoms, which are in ion form (O^{2-}), can be trapped in the potential wells of two metal-oxide interfaces (Au

electrode/ Al_2O_3 and Ru MNC/oxide), which act as two O^{2-} reservoirs [13]. Upon a BD event, the high local current density in the percolation path causes significant Joule heating, increasing the local temperature. When the CVS is stopped, the deteriorating electrical stressing disappears, but the local temperature in the BD percolation path remains high. Some of the trapped O^{2-} ions with sufficient thermal energy can overcome the already lowered (by BD) potential barriers of the Au electrode/ Al_2O_3 and Ru MNC/oxide interfaces, and hence return to passivate the V_o defects in the percolation path, as illustrated schematically by the conduction band diagram of the electrode/oxide and MNC/oxide interfaces shown in Fig. 6.9. The percolation path in the Al_2O_3 and SiO_2 layers can then be “switched off” when enough V_o defects are passivated, which is the case of the realization of the full RC of I_{leak} in the very soft BD with $I_{\text{max}} = 10\text{nA}$ (i. e., Fig. 6.7 (a) case). Unlike the electrical RC in which there is an electric field induced by the recovery voltage to drive the O^{2-} ions, in the case of auto-recovery, only limited number of the V_o defects that are near the metal Au electrode and Ru MNC can be passivated by the kinetically mobile O^{2-} ions that de-trapped from the two O^{2-} reservoirs and diffused into the percolation path at elevated temperatures (the diffusion length of the O^{2-} increases with increasing temperature). However, the V_o defects that are beyond the diffusion length of the O^{2-} ions in the oxide layers from the two O^{2-} reservoirs cannot be repaired. The absence of auto-recovery after multiple BDs in Fig. 6.7(a) was mainly because of the cumulatively generated V_o defects that are beyond the automatic RC regime. Other reasons may include multiple breakdown spots and lateral propagation of the breakdown area under successive CVS [11]. Even for the V_o defects that are automatic recoverable after each BD, only a portion of the BD-expelled O^{2-} ions could gain thermal kinetic energy to overcome the barrier of the metal/oxide interfaces and passivate the V_o defects, which is supported by the decreasing t_{BD} values from BD1 to BD3 in Fig. 6.7(a). As the

BD hardness increases with increasing I_{max} , the number of V_o defects and the diameter of the BD percolation path also increase [11, 12]. However, there are limited V_o annihilation events by the passivation of the thermally agitated O^{2-} ions from the two O^{2-} reservoirs at the post-BD automatic recovery stages and only the V_o defects near metal electrode and MNC could be repaired. Thus, we could reach the conditions of partial recovery of the I_{leak} in the case of Fig. 6.7(b) and non-recovery of Fig. 6.7(c) case as the I_{max} increased.

When the stack with certain BD hardness (shown in Fig. 6.8) was subjected to high temperatures to improve the thermal agitation of the O^{2-} ions and passivation of the V_o defects, a full recovery was realized in the Al_2O_3 layer but not the SiO_2 layer. This is because both of the O^{2-} reservoirs can provide thermally agitated O^{2-} to passivate the V_o defects in the Al_2O_3 layer; while only O^{2-} ions from the MNC/ SiO_2 can passivate the V_o defects in the SiO_2 layer (schematically shown in Fig. 6.9). Therefore the high- κ layer could be recovered significantly whereas the SiO_2 layer remains leaky. The fact that further increase in the temperature did not bring further recovery of the dielectric stack suggests that there is limited number of kinetically mobile O^{2-} ions de-trapped from the Au/oxide and MNC/oxide interfaces that could diffuse and passivate the V_o defects in the BD percolation path in the oxide layers.

Figure 6.9. Schematic illustration of the conduction band diagram in Au electrode/ Al_2O_3 , MNC/ Al_2O_3 and MNC/ SiO_2 interfaces at elevated temperatures, showing thermally agitated O^{2-} de-trapping from the metal/oxide interfaces to passivate the neighbor V_o in the BD percolation path. Note that there are two sources providing kinetically mobile O^{2-} to the Al_2O_3 layer, but only one source for the BD path in SiO_2 , indicating a higher recoverability of the Al_2O_3 layer for the same BD hardness. The dashed and solid lines indicate the original (before BD) and lowered barrier height (after BD) for O^{2-} ions.

6.6 Summary

The phenomena of recovery of Ru metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ NVM gate stack after soft and hard BDs were studied. Partial and full recovery on the leakage current and relaxation current are achieved by electrical methods. Polarity-dependent annihilation of oxygen vacancies in the breakdown percolation path by oxygen ions released from the Au electrode/oxide and metal nanocrystal/oxide interfaces is proposed as the recovery mechanism.

Furthermore, the phenomenon of automatic recovery of leakage current after soft breakdown was observed. We also found that modest anneals up to 225 °C could significantly recover a stack that was broken-down beyond the auto-recovery regime. It is suggested that the high local temperature increase in the percolation path induced by Joule heating is responsible for the recovery. During the recovery process, the oxygen-vacancy annihilation in the percolation path was facilitated by the thermally agitated O^{2-} ions that were stored in the Au electrode/ Al_2O_3 and MNC/oxide interfaces upon the removal of the stressing electric field.

References

- [1] H.H. Gu, X.L. Cheng, L. Shi and K. Lin, "Modeling and verifying for data retention capability of metal nanocrystal memory device," *Semiconductor Technology*, v 33, n 3, p 269-71, 274, March 2008.
- [2] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories - Part I: Device design and fabrication," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1606-1613, Sep 2002.
- [3] Z. T. Liu, C. Lee, V. Narayanan, G. Pei and E. Kan, "Metal nanocrystal memories-part II: electrical characteristics," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1614-22, 2002.
- [4] W. H. Liu, K.L. Pey, X. Li and M. Bosman, "Observation of Switching Behaviors in Post-Breakdown Conduction in NiSi-gated Stacks," Piscataway, NJ, USA, 2009, p. 4 pp.
- [5] S. K. Samanta, P.K. Singh, J. Y. Won, G. Samudra, Y.C. Yeo, L.K. Bera and N. Balasubramanian,, *et al.*, "Enhancement of memory window in short channel non-volatile memory devices using double layer tungsten nanocrystals," in *IEEE International Electron Devices Meeting 2005, Technical Digest*, ed, 2005, pp. 177-180.
- [6] P. K. Singh, G. Bisht, R. Hofmann, K. Singh, N. Krishna and Mahapatra, "Metal nanocrystal memory with pt single- and dual-layer NC with low-leakage Al₂O₃ blocking dielectric," *IEEE Electron Device Letters*, vol. 29, pp. 1389-91, 2008.
- [7] H. Reisinger, G. Steinlesberger, S. Jakschik, M. Gutsche, T. Hecht, M. Leonhard, U. Schroder, H. Seidl and D. Schumann, "A comparative study of dielectric relaxation losses in alternative dielectrics," Piscataway, NJ, USA, 2001, pp. 12-2.
- [8] M. Schumacher and R. Waser, "Curie-von Schweidler behaviour observed in ferroelectric thin films and comparison to superparaelectric thin film materials," Netherlands, 1998, pp. 109-21.
- [9] L. Wen, K. Yue and K. Way, "Dielectric relaxation and breakdown detection of doped tantalum oxide high-k thin films," *IEEE Transactions on Device and Materials Reliability*, vol. 4, pp. 488-94, 2004.
- [10] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The nature of dielectric breakdown," *Applied Physics Letters*, vol. 93, 2008.
- [11] X. Li, C.H. Tung and K.L. Pey, "The radial distribution of defects in a percolation path," *Applied Physics Letters*, vol. 93, 2008.
- [12] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The physical origin of random telegraph noise after dielectric breakdown," *Applied Physics Letters*, vol. 94, 2009.
- [13] B. Gao, S. Yu, N. Xu, L.F. Liu, B. Sun, X.Y. Liu, R.Q. Han, J.F. Kang, B. Yu and Y.Y. Wang, "Oxide-based RRAM switching mechanism: a new ion-transport-recombination model," Piscataway, NJ, USA, 2008, p. 4 pp.
- [14] K. L. Pey, C.H. Tung, M.K. Radhakrishnan, L.J. Tang and W.H. Lin, "Dielectric breakdown induced epitaxy in ultrathin gate oxide - a reliability concern," Piscataway, NJ, USA, 2002, pp. 163-6.
- [15] R. Ranjan, K.L. Pey, C.H. Tung, D.S. Ang, L.J. Tang, T. Kauerauf, R. Degraeve, G. Groeseneken, S. De Gendt and L.K. Bera, "Failure defects observed in post-breakdown high-k/metal gate stack MOSFET," Piscataway, NJ, USA, 2006, p. 5 pp.
- [16] B. Kaczer, R. Degraeve, N. Pagon, T. Nigam and G. Groeseneken, "Investigation of temperature acceleration of thin oxide time-to-breakdown," Netherlands, 1999, pp. 47-50.

CHAPTER SEVEN

THE METAL NANOCRYSTAL-BASED HIGH- κ /SiO₂ CHARGE-TRAPPING GATE STACK AS A RESISTIVE SWITCHING MEMORY CELL

7.1 Introduction

The increasing demand for miniaturization in microelectronics has led to an upsurge of the interest in developing nanometer-scale structures as part of the effort to establish small memory-bit cells. The aim is to overcome the spatial limitations imposed on conventional semiconducting devices based on charge storage. Many memory concepts that have been recently pursued range from spin-based memories (magneto-resistive random access memories, MRAM), in which a magnetic field is involved in the resistance switching [1], to phase-change random access memories (PCRAM), in which thermal processes control a phase transition in the switching material from an amorphous to a crystalline state [2]. Yet another class of resistive switching phenomena is based on the electrically stimulated change of the resistance of a metal-insulator-metal (MIM) memory cell, usually called resistive switching RAM, or RRAM for short.

Starting with the report on oxide insulators by Hickmott [3] in 1962, a huge variety of materials in a MIM configuration have been reported to show hysteretic resistance switching. In general, the “I” in MIM can be one of a wide range of binary and multi-nary oxides as well as organic compounds, and the “M” stands for a large variety of metal electrodes including electron-conducting non-metals.

Typically, an initial electroforming step such as a current-limited electric breakdown is induced in a virgin sample. This is called a “forming” step which preconditions the system that can be subsequently be switched between a conductive ON state and a less conductive OFF state. Switching is called unipolar when the switching procedure does not depend on the polarity of the voltage and current signal. A system in its high-resistance state (OFF) is switched (or “SET”) by a threshold voltage into a low resistance state (ON) as shown in Fig. 7.1(a). The current is limited by the compliance current of the control circuit. The “RESET” into the OFF state takes place at a higher current and a voltage below the SET voltage. In contrast, the characteristic is called bipolar when the SET operation occurs at one voltage polarity and the RESET operation is on reversed voltage polarity, as shown in Fig. 7.1(b).

Figure 7.1. Classification of the switching characteristics in a voltage sweeping experiment. **(a)** Unipolar switching. The SET voltage is higher than the voltage that RESET takes place, and both voltages are of same polarity. CC is the compliance current limit. **(b)** Bipolar switching. The SET operation takes place on one polarity and the RESET operation requires the opposite polarity. CC is the compliance current limit [4].

Alternatively, metal nanocrystal-based high- κ /SiO₂ gate stack has always been considered as a potential charge trapping memory cell for future NVM application. It adopts the traditional floating gate flash memory structure, but replaces the continuous layer of floating gate with discrete MNCs. In this chapter, we report the resistive switching behavior of a MNC-based Al₂O₃/SiO₂ gate stack with “metal-insulator-semiconductor (MIS) embedded with MNCs” structure. Furthermore, the metal nanocrystal-based Al₂O₃/SiO₂ gate stack is compatible to the contemporary high- κ /metal gate CMOS process, adding to the convenience of implementation for massive production. We believe that with further engineering of the constitutional layers, this kind of gate stack would be a potential candidate for RRAM or mixed-mechanism memory applications.

7.2 Experimental Details

The sample used was the single layer Ru metal nanocrystal-based high- κ /SiO₂ gate stack. The fabrication and sample dimension details are given in *Chapter Three*. The resistance switching from high-resistance state (HRS) to medium-resistance state (MRS) or low-resistance state (LRS), i. e. the SET operation, utilized a constant voltage stressing procedure with a stressing voltage (V_{SET}) of +6 V and a compliance current limit (I_{max}) of 100nA (so as to attain a MRS) or 500nA (to attain a LRS) selectively. The CVS was not stopped until the capacitor leakage current (I_{leak}) reaches I_{max} . The value of V_{SET} was determined by the mean breakdown voltage in the voltage ramp test of about 20 equivalent electrodes distributed over a wafer area of 10x10 cm². Switching from LRS to MRS or MRS to HRS (RESET operation) utilized a 10 second constant voltage of +4 V (V_{RESET+}) or -4 V (V_{RESET-}). The values SET and RESET voltages were chosen as a tradeoff of effective setting/resetting and stressing induced degradation. A 0 to -2 V voltage

sweep was applied to the top electrode to check the resistance/conductance of the gate stack. The dielectric relaxation current (I_{relax}) [5] was measured immediately after the removal of an initializing voltage of +3 V for a stressing time of 5 s. The combination of the I_{relax} and I_{leak} data could be used to examine the BD of the high- κ and SiO₂ dielectric layers, as discussed in *Chapter Six*.

7.3 Tri-level Resistive Switching of Metal Nanocrystal-based Al₂O₃/SiO₂ Gate Stack

In order to observe resistive switching behavior in the MNC-based Al₂O₃/SiO₂ gate stack, a soft BD of both Al₂O₃ and SiO₂ layers is required. This process resembles the “forming” stage in the MIM ReRAM [6]. Fig. 7.2 shows a typical switching behavior in the positive and negative voltage sweep tests. After the SBD (forming process) at +6.5V with I_{max} of 500nA in the first voltage sweep (sweep1, positive direction), a sudden current drop (RESET) appears in the second voltage sweep (sweep2, negative direction) at voltage bias (V_{bias}) of -4.3 V. A third sweep (sweep3, positive direction) starting from -4.6V sees a current drop (RESET) at V_{bias} of +4.45V before the gate stack SET at +6.35V. The SET, negative RESET and positive RESET voltage points were collected over 20 identical voltage sweep experiments. The SET voltage ranges from +6.1V to +7.5V, negative RESET voltage ranges from -2.3V to -5.5V and the positive RESET voltage ranges from +1.6V to +4.8V.

Figure 7.2. Typical resistive switching in 3 successive voltage sweep tests: SBD (forming process) at +6.5 V in sweep1; negative RESET at -4.3 V in sweep2; positive RESET and SET at +4.45 V and +6.35 V respectively in sweep3.

Successful tri-level resistive switching is realized when utilizing CVS as the stressing (or switching) method. This method adds on the controllability of the resistance states. The forming voltage value is chosen to be +6V, a bit smaller than the mean breakdown voltage (about +6.5V) in the voltage sweep tests to ensure reasonable time-to-breakdown. The value of SET voltage to set a HRS to a MRS or LRS is the same with the forming voltage (signified as V_{SET1}) of +6V. However, the SET voltage to set a MRS to LRS (signified as V_{SET2}) is +4.5V. This is because a

lower voltage is required to set a MRS gate stack, which is already partially broken down. The V_{RESET+} and V_{RESET-} values were chosen to be +4 V and -4 V with the same stressing time of 10 s to attain stable RESET resistance states. The values of V_{SET1} , V_{SET2} , V_{RESET+} , and V_{RESET-} are chosen after many repeated experiments on 20 equivalent samples.

Figure 7.3 presents the 0 to -2V voltage sweep test and the relaxation current measured on a fresh sample. It is obvious that the fresh sample is in a first HRS (denoted as HRS1), by virtue of the presence of the two insulating dielectric layers (Al_2O_3 and SiO_2).

As mentioned in *Chapter Four*, the I_{relax} of the fresh single layer Ru MNC-based gate stack follows a linear-log relationship with respect to time, which is similar to the dielectric relaxation behavior of Curie-von Schweidler law [7]:

$$I_{relax} = at^{-n} \quad (7.1)$$

where I_{relax} stands for the relaxation current, t stands for time, a and n are both constants. The “ I_{relax} vs. time” curve is generally a straight line in the log-log scale if Eqn.1 is obeyed. The contribution of the SiO_2 layer to the total gate stack dielectric I_{relax} is negligible because of its quick decay time and small magnitude compared to high- κ films [8]. Thus the I_{relax} provides direct information on primarily the insulator integrity on the high- κ Al_2O_3 layer (with embedded MNCs).

(a)

(b)

Figure 7.3. Resistive switching between 3 states: (a) leakage current showing the resistance of the gate stack (b) relaxation current (after a 3V initializing voltage stressing for 5s) indicating the insulating property of the Al_2O_3 high- κ layer.

After the forming process of +6V CVS with I_{max} of 500nA, a 0 to -2V voltage ramp shows that the device was in a first LRS (LRS1 in Fig. 7.4 (a)). The switching from LRS to first MRS (MRS1) was realized by a short CVS with a V_{RESET+} of +4 V for 10 s. Fig. 7.4 (a) shows that in the MRS, I_{leak} was still more than 2 orders of magnitude larger than that of the fresh sample. We can then use the same forming process ($V_{SET} = +6V$, $I_{max} = 500nA$) to switch the first MRS (MRS1) to a LRS, i. e., a second LRS called LRS2. To RESET the device back to a HRS, we first used a V_{RESET+} of +4 V for 10s to bring the sample from LRS2 back to a second MRS (MRS2). Subsequently, by utilizing a negative RESET voltage ($V_{RESET-} = -4V$ for 10 s), the device could be switched from MRS2 back to a fresh-like second HRS (HRS2). In Fig. 7.3 (a) and (b), it can be seen that both I_{leak} and I_{relax} of the second HRS (HRS2) overlap that of the fresh first HRS (HRS1), indicating a complete RESET operation. We can then repeat the entire sequence by using a SET condition which was the same as the forming process ($V_{SET1} = +6V$, $I_{max} = 500nA$) to bring the device from the fresh-like HRS2 to another LRS. Alternatively, with reduced SET voltage of $V_{SET2} = +4.5V$ and reduced compliance current ($I_{max} = 100nA$), the device can directly reach another MRS.

Figure 7.4. Resistance vs. switch steps of the MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack.

The repeatability and reversibility of the resistive switching are next studied. Fig. 7.4 shows the effective resistance of the gate stack at V_{bias} of -1V for 40 SET/RESET switching steps. The gate stack resistance exhibits a consistent and stable behavior when switched amongst the 3 resistance states by applying the corresponding SET/RESET voltages described before. We observe that HRS-to-MRS switching and MRS-to-LRS switching processes are bi-directional. However, HRS-to-LRS switching is unilateral (i. e., single direction). Switching from a LRS directly to a fresh-like HRS is only possible when the stack first goes through a transition state of

MRS (i. e., first switch to from LRS to MRS by application of V_{RESET+} , followed by V_{RESET-} to reset the MRS to a HRS). We found that applying a V_{RESET-} of -4V to LRS, to attempt direct reset to HRS, brings the gate stack into unstable resistance states that cannot be maintained during the subsequent 0 to -2V voltage ramp and relaxation current tests; hence we exclude the feasibility of a direct reset from LRS to HRS. Table 7.1 summarizes the switching conditions between the 3 resistance states.

We postulate that the 3 observed resistance states correspond to fresh or fresh-like gate stack (no dielectric breakdown, HRS), stack with a broken-down SiO_2 layer (MRS), and stack with both Al_2O_3 and SiO_2 layers broken down (LRS). Fig. 7.3(a) shows that when the device is at a MRS, I_{leak} is over 100 times larger than when the device is at a HRS. Since the I_{relax} of MRS in Fig. 7.3(b) still obeys the Curie-von Schweidler-like behavior (a straight line with negative slope of n), we postulate that at the MRS, only the SiO_2 layer is broken down whereas the top Al_2O_3 layer still retains its insulator property. It can be seen in Fig. 7.3(b) that when the device is at the LRS, the I_{relax} after the SBD forming process shows no Curie-von Schweidler-like behavior, indicating that the Al_2O_3 layer has also lost its insulator property (i. e., broken down) [9]. Besides, I_{leak} is now much larger than any reasonable tunneling currents from either a 4nm SiO_2 or even a 3nm (thickness of the whole high- κ layer minus the mean diameter of the MNC) Al_2O_3 . We therefore postulate that both dielectric layers of Al_2O_3 and SiO_2 have been broken down and a percolation path [10] has been formed, shorting the top electrode and substrate.

TABLE 7.1 Switching conditions for the 3 resistance states.

	To LRS	To MRS	To HRS
From LRS		$V_{RESET+} = +4 \text{ V}$ for 10 s	N/A
From MRS	$V_{SET2} = +4.5 \text{ V}$, $I_{max} = 500 \text{ nA}$		$V_{RESET-} = -4 \text{ V}$ for 10 s
From HRS	$V_{SET1} = +6 \text{ V}$, $I_{max} = 500 \text{ nA}$	$V_{SET1} = +6 \text{ V}$, $I_{max} = 100 \text{ nA}$	

7.4 Mechanism of Tri-level Resistive Switching

Here we propose a physical model to explain the tri-level resistive switching behavior induced by the application of electrical field of the MNC-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack. Fig. 7.5 (a) shows the schematic of the fresh device cross-section at its initial HRS (HRS1). Oxygen vacancies (V_o) began to accumulate in the Al_2O_3 and SiO_2 during a CVS or voltage sweep test. A SBD event of both dielectric layers (forming process), illustrated in Fig. 7.5 (b), happens when the density of electrical stress-induced V_o reaches a critical value so that a percolation path is formed by oxygen deficiency through both the Al_2O_3 and SiO_2 layers [11-13], resulting the device into its first LRS (LRS1) (Fig. 7.5 (b)).

The expelled oxygen travels in the form of ions (O^{2-}), and can be trapped in the $\text{Au}/\text{Al}_2\text{O}_3$ and $\text{Ru MNC}/\text{oxide}$ (Al_2O_3 and SiO_2) interfaces which act as O^{2-} reservoirs [14]. Due to the fact the MNCs are individual “spheres” with an average diameter of 3nm and a mean spacing of

~1nm, the MNC/oxide interface will have larger effective surface area than that of the Au/Al₂O₃ interface, thus storing a larger amount of O²⁻ ions (Fig. 7.5 (b)). V_o that are present in the SBD could either be neutral (with trapped electrons) or positively charged (V_o²⁺, trapped electrons are depleted) [15].

If we apply a V_{RESET+} of + 4V (Fig. 7.5 (c)), the neutral V_o are depleted, increasing the capture cross-section for O²⁻, while the O²⁻ ions in the MNC/Al₂O₃ interface move towards the anode side (top electrode). However, the O²⁻ in Au electrode/Al₂O₃ interface cannot penetrate into the Au electrode as interstitial defects or form oxide with this noble metal and thus they remain trapped at the interface. V_o annihilation is realized only in the top Al₂O₃ layer when an electron depleted V_o²⁺ captures an O²⁻ (V_o²⁺ + O²⁻ = O_o), similar to what happened at the NiSi gate with SiON or HfO₂ gate dielectric reported by Liu W. H. *et al.* [16]. When enough O²⁻s are released from the MNC/Al₂O₃ interface and passivate the V_o²⁺ in the Al₂O₃ layer, as shown in Fig. 7.5 (c), the percolation path in the Al₂O₃ layer is disrupted or “switched off”, putting the device to a first MRS (MRS1).

Figure 7.5. Cross-section schematics illustrating the resistive switching mechanism under (a) fresh condition (HRS1); (b) forming/SET voltage (LRS1), (c) positive RESET voltage (MRS1) and (d) subsequently negative RESET voltage (HRS2).

Another V_{SET} of +6 V may be used to break down the Al_2O_3 layer again (“switch on” the percolation path) to bring the device to back to a LRS. On the other hand, a $V_{\text{RESET-}}$ of -4 V may be used to RESET MRS1 further to a fresh-like second HRS (HRS2). Under this $V_{\text{RESET-}}$, more neutral V_0 are depleted (becoming V_0^{2+}), the O^{2-} ions trapped at the metal/oxide interfaces travel

towards the anode side (substrate). Because of the larger amount of trapped O^{2-} , as well as smaller work function of the MNC material (Ru, 4.71 eV) compared to the top electrode (Au, 5 eV), more O^{2-} ions are released from the Ru MNC/oxide interfaces than that of Au/ Al_2O_3 . Thus minor and major V_o annihilation occur in the top Al_2O_3 and bottom SiO_2 layers respectively (Fig. 7.5 (d)). When there are enough V_o annihilation events to “switch off” the remaining percolation path in the bottom SiO_2 layer, the device is put back to its fresh-like HRS. Attempts to switch directly from LRS to HRS did not work because a single application of a negative RESET voltage implies that the V_o annihilation in the Al_2O_3 section of the percolation path can only occur via the O^{2-} reservoir that stores less amount of O^{2-} ions (the Au/ Al_2O_3 interface), and this is likely insufficient to fully passivate that section of the percolation path. The resulting unstable resistance states in this case could be due to the partially passivated Al_2O_3 layer being in the regime of digital-like breakdown [17].

Figure 7.6 shows the 0 to -2V voltage sweep curve of such a gate stack with an unstable state, which is a result of applying only a V_{RESET} to a LRS. We can see that at the beginning of the voltage sweep, the device was at a LRS. A switch to a MRS happened when the bias voltage reached -0.45V. At $V_{bias} = -0.8V$, the stack was returned to a LRS. A disrupt decrease of I_{leak} occurred at $V_{bias} = -1.55V$, and the device was in a HRS. However, the HRS was not retained for long when it switched back to a MRS at $V_{bias} = -1.75V$.

Figure 7.6. A 0 to -2V voltage sweep of a MNC-based gate stack with unstable resistance state resulting from applying only a V_{RESET} .

7.5 Summary

The dielectric soft breakdown and selective recovery of the top and bottom dielectric layers in a metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack are successfully realized by a simple electrical method, giving rise to 3 distinct resistance states. Compared to existing RRAM ([4], [18]) where only 2 resistance states are available per memory, metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack

gives a promising future for multi-bit RRAM single cell. We propose a model to explain these observations based on oxygen ions de-trapping from the metal-oxide interfaces (including metal nanocrystal/oxide interfaces) which serve as oxygen ion reservoirs, and the passivation of depleted oxygen vacancies in the dielectric breakdown percolation path. Bias-dependent oxygen vacancy annihilation in percolation path in dielectric layers is proposed as the mechanism responsible for the electrical tri-level resistive switching.

References

- [1] R. R. Katti and T. Zhu, "Attractive magnetic memories," *IEEE Circuits and Devices Magazine*, vol. 17, pp. 26-34, 2001.
- [2] S. Zhitang, R. Feng, Y. Lin, L.C. Wu and B. Liu., "Phase change materials and random access memory," Piscataway, NJ, USA, p. 4 pp.
- [3] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films," *Journal of Applied Physics*, vol. 33, pp. 2669-2682, 1962.
- [4] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Materials*, vol. 6, pp. 833-840, 2007.
- [5] A. K. Jonscher, "Dielectric relaxation in solids," *Journal of Physics D-Applied Physics*, vol. 32, pp. R57-R70, Jul 1999.
- [6] D. C. Kim, *et al.*, "Electrical observations of filamentary conductions for the resistive memory switching in NiO films," *Applied Physics Letters*, vol. 88, 2006.
- [7] M. Schumacher and R. Waser, "Curie-von Schweidler behaviour observed in ferroelectric thin films and comparison to superparaelectric thin film materials," Netherlands, 1998, pp. 109-21.
- [8] H. Reisinger, G. Steinlesberger, S. Jakschik, M. Gutsche, T. Hecht, M. Leonhard, U. Schroder, H. Seidl and D. Schumann, "A comparative study of dielectric relaxation losses in alternative dielectrics," Piscataway, NJ, USA, 2001, pp. 12-2.
- [9] W. Luo, *et al.*, "Breakdown phenomena of zirconium-doped hafnium oxide high-k stack with an inserted interface layer," *Applied Physics Letters*, vol. 89, pp. 72901-1, 2006.
- [10] J. Sune, I. Placencia, N. Barnoil, E. Farres, F. Martin and X. Aymerich, "On the breakdown statistics of very thin SiO₂ films," *Thin Solid Films*, vol. 185, pp. 347-62, 1990.
- [11] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The nature of dielectric breakdown," *Applied Physics Letters*, vol. 93, 2008.
- [12] X. Li, C.H. Tung and K.L. Pey, "The radial distribution of defects in a percolation path," *Applied Physics Letters*, vol. 93, 2008.
- [13] X. Li, C.H. Tung, K.L. Pey and V.L. Lo, "The physical origin of random telegraph noise after dielectric breakdown," *Applied Physics Letters*, vol. 94, 2009.
- [14] B. Gao, S. Yu, N. Xu, L.F. Liu, B. Sun, X.Y. Liu, R.Q. Han, J.F. Kang, B. Yu and Y.Y. Wang, "Oxide-based RRAM switching mechanism: a new ion-transport-recombination model," Piscataway, NJ, USA, 2008, p. 4 pp.
- [15] N. Xu, B. Gao, L.F. Liu, B. Sun, X.Y. Liu, R.Q. Han, J.F. Kang and B. Yu, "A unified physical model of switching behavior in oxide-based RRAM," *VLSI Technology*, 2008, pp. 100-101.
- [16] W. H. Liu, K.L. Pey, X. Li and M. Bosman, "Observation of Switching Behaviors in Post-Breakdown Conduction in NiSi-gated Stacks," *International Electron Devices Meeting (IEDM)*, 2009, p. 4 pp.
- [17] N. Raghavan, X. Wu, X. Li, W.H. Liu, V.L. Lo and Pey, K.L. "Post breakdown reliability enhancement of ULSI circuits with novel gate dielectric stacks," Piscataway, NJ, USA, 2009, pp. 505-13.
- [18] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki and Y. Sugiyama, "Reduction in reset current of unipolar NiO-based resistive switching through nickel interfacial layer", *Appl. Phys. Lett.* 93, 033506 (2008)

CHAPTER EIGHT

SUMMARY AND CONCLUSIONS

8.1 Conclusions

Novel approaches have been used to thoroughly study the novel charge leakage and device degradation mechanisms in single and dual layer metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stacks which are promising candidates for future flash memory applications. In addition, we discuss the phenomenon of the post-breakdown recovery on the metal nanocrystal-based gate stack and the possibility of such charge-trapping gate stack as a candidate for resistive switching memory cell.

A relaxation current measurement was adopted to study the charge leakage of the nanocrystals. The unique temperature dependent relaxation current behaviors of single and dual-layer platinum nanocrystal-based gate stacks that are much different from pure high- κ dielectric were investigated. The dual-slope in the relaxation current of the single-layer metal nanocrystal sample was found to be due to the different dominance of two competing mechanisms of the metal nanocrystal-induced relaxation current. It is proposed that in the single layer metal nanocrystal-based sample, in the early stage of the relaxation current, thermionic emission current is the dominant source, whereas at the late stage, quantum tunneling current becomes dominant. Whereas in the dual-layer metal nanocrystal-based stack, the quantum tunneling current is always dominant, giving rise to an exponent-linear relationship of the temperature-dependent relaxation current behavior. This simple method of relaxation current provides direct

information and assess of short-term charge retention property of the metal nanocrystals-based memory devices.

The phenomena of lateral charging of the discrete metal nanocrystals were also studied here. In the single-layer ruthenium nanocrystal-based gate stack, an enhanced I - V hysteresis was realized when the stack suffered a soft breakdown. We propose that an increased lateral charge-trapping current through the breakdown path and the lateral charge propagation is the origin. Through a series of electrodes prepared nano-level electrodes by electric beam lithography for nano-scale electrical characterization, it was observed that the lateral charging of the MNCs eventually leads to the lateral propagation of breakdown area under hard breakdown. The lateral propagation can reach a distance as far as 120nm.

Partial or full recoveries of the leakage current and relaxation current of broken-down metal nanocrystal-based gate stacks were observed for different breakdown hardness if we stressed the broken-down ruthenium nanocrystal-based high- κ /SiO₂ gate stack with a small voltage with certain polarity. The recovery of the dielectric properties of either the high- κ control oxide layer or the SiO₂ tunnel oxide layer was found to be dependent on the polarity of recovery voltage. A physical model was established to explain the phenomena. Polarity-dependent annihilation of oxygen vacancies in the BD percolation path by oxygen ions released from the top metal electrode/oxide and metal nanocrystal/oxide interfaces is proposed as the recovery mechanism. Furthermore, an automatic recovery of leakage current was observed in the constant voltage stressing if we controlled the breakdown hardness at a relatively soft level. Control experiments at elevated temperature confirmed the temperature-related recovery behavior. Our findings suggest that high local temperature increase in the percolation path induced by Joule heating is responsible for the automatic recovery. During the recovery process, the oxygen-

vacancy annihilation in the percolation path was facilitated by the thermally agitated oxygen ions that were stored in the metal electrode/ Al_2O_3 and ruthenium metal nanocrystal/oxide interfaces upon the removal of the stressing electric field. This recovery behavior offers extra reliability margin for the metal nanocrystal-based gate stack.

In the last part of this work, the soft breakdown and selective recovery of the top and bottom dielectric layers in a metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack was successfully realized by an electrical method, giving rise to 3 distinct resistivity states. Oxygen ions de-trapping from the metal-oxide interfaces (including metal nanocrystal/oxide interfaces) which serve as oxygen ion reservoir, and passivating back with the oxygen vacancies in the dielectric breakdown percolation paths is proposed to be the reason of the tri-level transition of the resistance state of the metal nanocrystal-based gate stack. Bias-dependent oxygen vacancy annihilation in dielectric layers is proposed as the switching mechanism which makes the electrical tri-bit resistive switching possible. This finding brings us new perspectives for the possible application of the metal nanocrystal-based high- κ/SiO_2 gate stack as future non-volatile memory cell.

8.2 Suggestions

Despite all the insights we have uncovered, MNC-based memory devices could benefit from further extensions of the work we report here. Some of the possible directions for future investigations and studies are as follows:

- A thorough approach on the lateral interaction of the MNC can be investigated. Parameters such as diameter, spacing and density of the MNC could be taken into account to study their influence on the lateral interaction.

- Breakdown of the MNC-based gate stack could be further analyzed. A localized physical study (e.g., TEM, EELS, etc) on the breakdown spot could be carried out. Similarities and differences to the traditional gate stack without MNC should be compared in details such that the understandings on breakdown and the device reliability can be further enhanced.
- The recovery mechanism of different MNC materials and different electrode material could be further studied, e.g. through computational modelling. It is still challenging to design the MNC-based flash memory cell with excellent performance and also reasonable recoverability after breakdown. Optimization in the gate stack engineering requires more understandings on the recovery mechanisms.
- A hybrid memory cell which combines charge trapping memory function as well as resistive switching is a potential project. Design parameters such as dielectric thickness, MNC and electrode material, density and size of MNC need to be carefully engineered. Their influences on the device function of charging trapping and resistive switching requires further research.

PUBLICATIONS

- [1] **Y. N. Chen**, K. L. Pey, K. E. J. Goh, Z. Z. Lwin, P. K. Singh, and S. Mahapatra, "Tri-level Resistive Switching in Metal-nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ Gate Stack," *IEEE Transactions on Electron Devices*, vol. 57, pp. 3001-5, (2010).
- [2] **Y. N. Chen**, K. L. Pey, K. E. J. Goh, Z. Z. Lwin, P. K. Singh, S. Mahapatra, Q. X. Wang and J. Zhu, "Post-breakdown recoverable metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack for non-volatile memory", International Conference on Solid State Devices and Materials, pp 762-763, (2010)
- [3] **Y. N. Chen**, K. L. Pey, K. E. J. Goh, Z. Z. Lwin, P. Singh, and S. Mahapatra, "Study of automatic recovery on the metal nanocrystal-based $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack," *Applied Physics Letters*, vol. 98, pp. 083504, (2011).
- [4] **Y. N. Chen**, K. L. Pey, K. E. J. Goh, Z. Z. Lwin, P. Singh, and S. Mahapatra, " Study of the Charge Leakage of Dual Layer Pt Metal Nanocrystal-based high- κ/SiO_2 Flash Memory Cell - A Relaxation Current Point of View", 18th International Symposium on the Physical and Failure Analysis on integrated circuits (IPFA), Incheon, Korea, pp38-41 (2011).
- [5] Z. Z. Lwin, K. L. Pey, **Y. N. Chen**, P. K. Singh, and S. Mahapatra, "Charging and discharging characteristics of metal nanocrystals in degraded dielectric stacks," Garden Grove, CA, Canada.
- [6] Zin Zar Lwin, P. Kin Leong, N. Raghavan, **Y.N. Chen**, and S. Mahapatra, "New Leakage Mechanism and Dielectric Breakdown Layer Detection in Metal-Nanocrystal-Embedded Dual-Layer Memory Gate Stack," *IEEE Electron Device Letters*, vol. 32, pp. 800-2.

- [7] K. L. Pey, N. Raghavan, X. Wu, W. Liu, X. Li, M. Bosman, K. Shubhakar, Z. Z. Lwin, **Y.N. Chen**, H. Qin, and T. Kauerauf, "Physical analysis of breakdown in high-k/metal gate stacks using TEM/EELS and STM for reliability enhancement (**invited**)," 7th Conference on Insulating Films on Semiconductors, Grenoble – France pp 1365-1372, (2011).
- [8] **Y.N. Chen**, K. E. J. Goh, X. Wu, Z. Z. Lwin¹, P.K. Singh, S. Mahapatra and K.L. Pey, "Temperature-dependent Relaxation Current on Single and Dual ^{layer} Pt Metal Nanocrystal-based Al₂O₃/SiO₂ Gate Stack", *IEEE Transactions on Electron Devices*, under review, (2011).