Band selectable low-noise amplifier design for flexible wireless receiver front-ends

Chiu, Chun Chi

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BAND SELECTABLE LOW-NOISE AMPLIFIER DESIGN FOR FLEXIBLE WIRELESS RECEIVER FRONT-ENDS

SUBMITTED
BY
CHIU CHUN CHI

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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Abstract

One of the main reasons behind the tremendous growth of the wireless communication technology in the past few decades is the development of wireless standards for the different field of wireless applications. These standards, which can be set by industries or worldwide organizations, help in the fast adoption of the technology into the consumer markets because standardization brings about cheaper, faster, better interoperable and more compatible consumer products. However, as technology progress, the number of wireless standards also increases and complicates the situation. Newer standards that are supposed to be better and superseding older standards often fail to fully replace them. The wide penetration of the older standards demands backward compatibility from the newer standards. On top of this, the convergence of standards that are originally from different field of applications into a single mobile device for the consumer markets further increases the complexity of situation. All these demands points to the development of a multi-standard radio.

To avoid the problems of large silicon area required for multiple front-ends and the power draining single high performing front-end, this thesis aims to explore on the idea of flexible front-ends as a more advance alternative solution to the multi-standard radio development. A truly flexible front-end should be small and power efficient in supporting multi-standard operations.

In this thesis, the review of recently published Low-Noise Amplifiers (LNAs) that exhibits the flexible characteristics is first presented. Focusing only on achieving flexibility in the operating frequency of the LNAs, design techniques of these published

LNAs are organized and discussed before they are employed into the design of such a flexible LNA (FLNA).

Next, the idea of a flexible receiver front-end is presented and defined, followed by the new design strategy and characterization parameters that only targets flexible designs. The inherent benefits of using the flexible approach will be highlighted as compared to using the traditional approach. Issues regarding the use of flexible designs are also briefly summarized.

Finally, the proposed FLNA will be presented. The designed FLNA, unlike the other reported FLNAs, is based on a resistive feedback topology that is conventionally used in wideband designs. Design techniques are then employed to the FLNA to achieve flexible operating frequencies. These techniques however, forgo the usual wideband characteristic of the resistive feedback topology and realized a switchable narrowband design at an acceptable wide frequency range.

The proposed FLNA is simulated in the 0.18 μ m RFCMOS technology and achieved switchable operating frequencies from 2.4GHz to 5.8GHz with a noise figure of less than 2.4dB throughout the different switchable bands. The FLNA has a linearity better than -13dBm (IIP3) at 13mW of power consumption.

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Chapter 1 – Introduction

1.1 Background

Wireless communication technology has continued to see tremendous growth in the past few decades. The quest to have as much wireless connectivity as possible continues to drive the rapid development and application of the wireless communication technology into many different fields, ranging from the short distance infra-red remote control systems to the long distance satellite systems.

One very important factor for the advancement of the wireless communication technology is the development of wireless standards in each of the individual field of applications. These standards, which can be set by industries or worldwide organizations, help in the fast adoption of the technologies into the consumer markets because standardization brings about better interoperability and higher compatibility for the users, on top of the potential of cheaper and faster manufacturing process due to mass production.

However, as technology continues to progress, the number of wireless standards also increases, which complicates the situation. Newer standards that are supposed to be better and superseding older standards often fail to fully replace them. The wide penetration of the older standards makes it a necessity to retain them and to such an extent that even newer standards are required to provide some form of backward compatibility.

To make the matter worst, standards that are originally from different field of applications begin to converge and are also required to be made compatible or at the minimum, be supported simultaneously. This situation is clearly evident in mobile devices available in the market today, where standards like 3G, Wi-Fi, GPS and Bluetooth are seen as the basic connectivity requirements.

1.2 Motivation

The existence of many different wireless standards for different applications and the need for mobile devices to support them demand the development of a multi-standard radio [1]. Through the progress of CMOS technology and RFIC design, full integration of a wireless transceiver in CMOS technology that works in the low-GHz bands currently enables such a multi-standard radio but often at the expense of using multiple front-ends in parallel [2].

The continual improvement of the CMOS technology now allows RFIC designers to seek more capability in their designs with better device performances. Other than seeking designs with higher frequencies of operation beyond 10GHz for higher data rates [3], the design of a single high performing multi-standard front-end for multi-standard radios in the low-GHz range is also realizable [4].

However, more work can still be done to further exploit the advantages of the improved device performances. Instead of designing a single high performing front-end that meets all the different kinds of requirements, a highly flexible wireless transceiver front-end that allows its performance parameters to be changeable would possibly

provide an alternative multi-standard radio solution with benefits such as lower power consumption, which is one of the essential requirements for mobile devices.

1.3 Objective

The aim of this research is to enable a multi-standard radio using a flexible front-end, with emphasis on the receiver part of the radio, to provide a more efficient alternative to the current multi-standard radios.

Other than exploring a flexible solution, the actual design of such a receiver front-end, which targets most of the wireless standards in the low-GHz range, will be done using the Global Foundries (GF) 0.18 μ m RFCMOS process so as to support the possibility of full integration and low cost.

1.4 Contribution and Scope

This research explores the idea of a flexible receiver front-end that is targeted for use as a multi-standard radio. A new design strategy is being proposed to design the flexible receiver front-end. The strategy will focus on achieving flexibility in the design before trying to find out its applications, which is fundamentally different to most of the current design steps. This process of designing, assumes that the inherent benefits of a flexible receiver front-end will surface as long as sufficient flexibility is achieved. To facilitate the design process, new parameters are set to better describe the flexibility of a design.

To further expand on this design strategy in a receiver front-end, a review of the different recently published Flexible Low-Noise Amplifiers (FLNAs) are summarized and analyzed to identify the different flexible design techniques used. Following, a FLNA with flexible operating frequencies in the low-GHz range is being proposed and designed.

1.5 Organization

This thesis is organized into six chapters including this introduction chapter. Chapter 2 gives a better understanding into RFIC design by introducing the performance parameters used in RF designs and their relevance in a receiver system. The different receiver architectures and the technology trends in RFIC design are also briefly presented in the chapter. Chapter 3 presents the literature review on LNAs. Starting from the basic operation of the different LNA topologies, the chapter quickly discuss the different needs of the LNA in different types of multi-standard receiver front-ends and finally presents the State-of-the-Art FLNA designs. Chapter 4 discuss the proposed idea of flexible receiver front-ends and its unique features. New parameters that are proposed to characterize the flexibility and the new design strategy are also discussed in the chapter. Chapter 5 contains the design, the simulation results and the discussions on the proposed FLNA design. Lastly, Chapter 6 concludes the thesis with clear future plans.

Chapter 2 – Fundamentals of Radio Frequency Integrated Circuit Design

2.1 Performance Parameters

The first important aspect in RFIC design is to understand the concepts and terminologies used in RF designs and their significance. These concepts can be slightly different to the usual IC design field. Therefore it is important to first discuss these different performance parameters that are typically used to characterize RF systems and their relevance to IC design [5, 6].

Performance parameters like noise, sensitivity, linearity, dynamic range, s-parameters, gain, matching and power consumption will be briefly discussed in reference to a receiver system whenever possible. These are essential parameters to specify the system performance and they help to provide common understanding to the design engineers. Analysis on these parameters can also help to better optimize the performance of the designs for different applications.

This is not to say that other parameters not discussed are not important. Other parameters like chip area or stability can be even more important than the few discussed parameters which the designer should also consider. However, the discussed parameters are originated from RF designs and hence require more discussions.

Noise Factor, Noise Figure and Sensitivity

The noise factor (F) is used to measure the noise performance of a system and is defined by the IEEE as [5, 6]:

$$\text{Equation (1): } F = \frac{(\text{total output noise power})}{(\text{output noise power due to source noise})}$$

This is applicable when the source is at a temperature of 290K as the noise of the source changes with temperature. Another more common expression of F is:

$$\text{Equation (2): } F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}$$

SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output of the system respectively. The expression simply suggests that F is used to measure the SNR degradation of the input signal when it passes through the system, as this degradation is due to the noise generated by the system.

The noise figure (NF), which is F expressed in decibels, is more commonly used in the actual designs:

$$\text{Equation (3): } \text{NF (dB)} = 10 \log_{10} F$$

In situation where a number of stages are cascaded to form a larger system, the total noise factor (F_{total}) of the system can be calculated in terms of the noise factor (F_i) and the gain (G_i) of the individual stage, which is known as the Friis equation [5, 6]:

Equation (4): $F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots$

Although the Friis equation is only valid when the output of one stage is power matched to the input of the following stage [7], which is not usually implemented in fully integrated receivers, the concept remains the same. The equation shows the concept that the noise contributed by the different stages decrease if the gain of the preceding stages increase. Thus, the noise and gain of the first stage in a cascade system are therefore the most critical parameters in determining the total noise of the system. In a simple illustration shown in Figure 1 below, the noise of the first stage will set the lower limit of the total system noise, while the effect of a larger gain of the first stage helps to reduce the noise contribution of the following stages significantly. In Figure 1, the noise of the first stage is fixed at 2dB while the noise of the following stages are combined and taken as the noise of the second stage (NF_2) in a simplified two-stage cascade system.

Figure 1: Total Noise Figure of Two-Stage Cascade System with Different NF_2

This brings about the importance of a Low-Noise Amplifier (LNA), which is the first active stage of a receiver front-end. Figure 1 clearly displays its role of providing enough gain so as to minimize the noise contribution of the subsequent stages, while at the same time, adding as little noise as possible to the system.

The NF of a receiver system is closely related to its sensitivity, which is a measure of the receiver's ability to detect the desired but weak signal. The sensitivity of a receiver is therefore also referred as the minimum detectable signal (MDS) power at the input which provides the required SNR at the output [5, 6]. Hence the MDS, which is derived from the F of the receiver system, can be calculated using:

$$\text{Equation (5): } \text{MDS (dBm)} = P_{\text{noise_floor}} + 10 \log_{10} B + \text{NF} + \text{SNR}_{\text{min}}$$

Here, $P_{\text{noise_floor}}$ is the noise floor level at matched condition and is taken as -174dBm, B is the bandwidth of the input signal and SNR_{min} is the minimum required SNR at the output.

Linearity (P1dB and IP3) and Dynamic Range

The linearity of a system helps to characterize the level of distortion caused by the system itself to the signals passing through the system. Such distortions are only significant when the input signal is large and hence is often measured by the nonlinear impact of the system using the 1dB compression point (P1dB) and the third order intercept point (IP3) [5, 6].

Both the P1dB and the IP3 will be explained using the following general expression of the output of a nonlinear system [6]:

$$\text{Equation (6): } y(t) = a_0 + a_1x(t) + a_2x^2(t) + a_3x^3(t) + \dots$$

Here, $y(t)$ is the output signal and $x(t)$ is the input signal respectively. In the scenario when $x(t)$ is only a single sinusoid signal ($x(t) = A\cos(\omega t)$, where A , ω is the amplitude and angular frequency of the signal respectively), the output will be:

$$\text{Equation (7): } y(t) = \left(a_1 + a_3 \left(\frac{3A^2}{4} \right) \right) A\cos(\omega t) + \dots$$

The equation, though showing only the fundamental term, explains the source of the gain compression in the system since a_3 is generally negative and this shows that gain compression happens without any interference. Gain compression happens because the gain of the system is a decreasing function of A (due to a_3). Physically, it means that when the input power level increase, the system saturates and the output cannot continue to respond linearly to the input. Therefore, the gain compression is measured using the P1dB, which is defined as the point at the input power level such that the system's actual output power level is 1dB less than the linearly predicted output power level as shown in Figure 2 below. However, in receiver systems where its use is to detect weak signals, gain compression is not so common as compared to transmitter systems.

Figure 2: Graph to Illustrate P1dB and IP3

Figure 2 also shows the IP3 [7], which is caused by interferers. Interferers can cause different undesired effects, especially in a receiver. For example, they will desensitize the gain of the receiver, impose unwanted cross modulation information and also corrupt the input with intermodulation products. All of which reduce the ability of the receiver in detecting the weak input signals.

The IP3 is used to measure the effect of the third order intermodulation (IM_3) products, which is the most significant distortion caused by interferers to a receiver system. Fundamentally, many intermodulation products exist due to the nonlinearity of the

system but only the IM_3 products are of major concern because of the fact that they are of the same frequency band as the desired input signal.

The undesired IM_3 products are quite easily produced when two interferers, which are at some nearby frequencies around the input signal frequency band, exist together at the input of the receiver. To further explain its impact, consider two interferers at the input of the system [6]:

Equation (8): $x_{\text{interferers}}(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$

The IM_3 products at the output of the system with the two interferers will be:

Equation (9): $IM_3 = \frac{3a_3 A_1^2 A_2}{4} \cos((2\omega_1 - \omega_2)t) \text{ or } \frac{3a_3 A_2^2 A_1}{4} \cos((2\omega_2 - \omega_1)t)$

From equation (9), the main impact of the IM_3 products is the unwanted cubic “gain” of the IM_3 product output power level with respect to the interferers’ input power level (if they have the same input amplitude, $A_1 = A_2 = A$), which can easily corrupt the desired signal. The IP3 is therefore defined to characterize this corruption and is measured using a two-tone test that resembles the two interferers. By plotting both the linear gain and the cubic “gain” on the logarithmic scale, the interception point between the two gains will be the IP3. Following, the input power level at IP3 is called input-IP3 (IIP3) while the output power level at IP3 is called output-IP3 (OIP3). Thus, the IIP3 (or OIP3) is used to measure the performance of small signal circuits under larger signal interferers and is more meaningful in measuring the linearity of receiver systems

like LNA and Mixers. One important issue of the two-tone test is the negligence of the multiple tones in real systems. In cases where there are more than two nearby interfering signals, the linearity of the system will be further degraded.

Again, in the situation where a number of stages are cascaded to form a larger system, the total input-IP3 ($IIP3_{total}$) of the system can be calculated in terms of the input-IP3 ($IIP3_i$) and the gain (G_i) of the individual stage:

Equation (10):
$$\frac{1}{IIP3_{total}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \dots$$

Equation (10) shows an obvious observation that the IIP3 of the last stage contributes most to the IIP3 of the system. The input signal level increase as it moves to the later stages of the system through the gain of the preceding stages, so do the nearby interfering signals. Hence, this makes the linearity of the later stages more and more important. Equation (10), similar to equation (4), is only valid when the output of one stage is power matched to the input of the input of the following stage [7].

The linearity of the system thus greatly determines the maximum power level at its input. Together with the NF, they define the dynamic range (DR) of the system. In real life wireless environment, the received signal level varies greatly. The DR of the receiver is a measure of its ability to react to the various signal levels. DR is generally defined as the ratio of the maximum tolerable input level to the minimum detectable input level. In reference to the IIP3 of the receiver system, the spurious-free dynamic range (SFDR) is used to measure the receiver's ability to tolerate the distortion created

by the spurious signals. The maximum tolerable input power level is the maximum power level of the IM_3 products, under a two-tone test scenario, that will not exceed the noise floor.

S-Parameters, Matching and Gain

The scattering parameters (S-parameters) are often used to characterize RF systems. At RF, not only the open and short circuit conditions are not always available, the voltages and currents are also difficult to be measured. Thus, S-parameters that measure the incident and reflected waves at matched conditions are more useful in characterizing RF systems.

Although S-parameters can be used to characterize multi-port systems, the two-port network show in Figure 3 below will be used to discuss the definition of S-parameters and their role in characterizing a receiver system.

Figure 3: A Two-Port Network

In Figure 3, a_1 and a_2 are the incident waves and b_1 and b_2 are the reflected waves. The S-parameters relate the waves according to:

$$\text{Equation (11): } \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = [\mathbf{S}] \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

In the equation, $\mathbf{S}$ is called the scattering matrix and the elements are the S-parameters.

Based on the matrix equation, the S-parameters have the following definitions:

S_{11} is the input reflection coefficient with matched output port:

$$\text{Equation (12): } S_{11} = \frac{b_1}{a_1} \text{ when } a_2 = 0$$

S_{12} is the reverse transmission coefficient with matched input port:

$$\text{Equation (13): } S_{12} = \frac{b_1}{a_2} \text{ when } a_1 = 0$$

S_{21} is the forward transmission coefficient with matched output port:

$$\text{Equation (14): } S_{21} = \frac{b_2}{a_1} \text{ when } a_2 = 0$$

S_{22} is the output reflection coefficient with matched input port:

Equation (15): $S_{22} = \frac{b_2}{a_2}$ when $a_1 = 0$

These definitions of S-parameters are meaningful in receiver system designs. By representing the voltages at the input and output port with normalized waves, the S-parameters can be used to characterize the receiver system's input matching, output matching, gain and reverse isolation. To begin, the input and output voltages at the respective ports are represented by waves of incident and reflection according to:

Equation (16): $V_{in} = V_1^+ + V_1^-$

Equation (17): $V_{out} = V_2^+ + V_2^-$

Here, V_{in} and V_{out} are the input and output voltages at the respective ports. V_1^+ and V_2^+ are the input and output incident wave voltages at the respective ports and V_1^- and V_2^- are the input and output reflected wave voltages at the respective ports. Next, the wave voltages are normalized to the waves as represented in S-parameters:

Equation (18): $a_1 = \frac{V_1^+}{\sqrt{Z_0}}$

Equation (19): $b_1 = \frac{V_1^-}{\sqrt{Z_0}}$

Equation (20): $a_2 = \frac{V_2^+}{\sqrt{Z_0}}$

Equation (21): $b_2 = \frac{V_2^-}{\sqrt{Z_0}}$

Z_0 is usually the characteristic impedance of the transmission lines that are used to connect the receiver system. Thus the S-parameters become:

Equation (22): $S_{11} = \frac{V_1^-}{V_1^+}$

Equation (23): $S_{12} = \frac{V_1^-}{V_2^+}$

Equation (24): $S_{21} = \frac{V_2^-}{V_1^+}$

Equation (25): $S_{22} = \frac{V_2^-}{V_2^+}$

Therefore, based on the above representation, S_{11} and S_{22} actually represents the input and output matching of the system respectively, while S_{12} and S_{21} represents the gain and reverse isolation of the system respectively.

Power Consumption

Power is always the major concern for any designs. It is usual and normal to see that almost all the performing parameters for different applications trades-off with power consumption. On top of this aspect, the power consumption of a receiver system is more important because the receiver front-end is always on.

In a receiver front-end, the only source of power consumption is the DC power dissipation, which is the supply voltage multiplied by the current consumption. As the supply voltage is usually fixed in a system, the power consumption is mainly determined by the current needed for the system to work.

2.2 Receiver Architectures

There are three traditional receiver architectures, classified by comparing the difference of the RF input signal and LO signal frequencies, which is known as the intermediate frequency (IF) of the receiver, with the bandwidth (BW) of the input signals. If the IF is larger than the BW, it is a high-IF architecture, a low-IF architecture if the IF is less than BW and lastly, a zero-IF if the IF is at DC.

The section below briefly discusses the different architectures. However, to simplify the discussion, the low-IF and zero-IF are grouped together as both are more suitable for full integration.

High-IF Receiver

High-IF receiver architecture, also known as the super heterodyne architecture, has its IF sufficiently greater than the BW of input signal for the benefit of better selectivity, sensitivity and noise performance [7].

Figure 4: High-IF Receiver Architecture

Shown in Figure 4 above, the heterodyne receiver has been the most popular receiver architecture due to its high performance. The input signal from the antenna is first being filter by the RF filter to lower the unwanted out of the band signals. After being amplified by the LNA, an image-reject filter is needed before the signal passes through the mixer. This image reject filter is a band pass and high-Q filter as its BW is usually small as compared to its operating frequency and therefore high-Q components are needed. It is also possible to combine the image-reject filter with the RF filter so that this high-Q filter can be removed. However, this combined filter, being in front of the LNA, contributes more noise and often increases the minimum noise figure of the system.

After the first mixer, the RF signal is down convert to the IF signal and therefore needs a channel select filter to reject the in-band interference before it is further down-convert by the second mixer. Finally, the signal passes through another filter, a low pass this time, before it is presented to the ADC for subsequent digital signal processing.

The high-Q filter required at the image-reject stage makes the full integration of heterodyne receiver difficult as the CMOS process can only provide relatively low Q passive elements. The use of two IF also increases the complexity of the architecture where detailed frequency planning is often needed. Therefore, this architecture is not as popular in fully integrated receiver systems.

Low-IF and Zero-IF Receiver

Low-IF and zero-IF receiver architectures are quite similar by looking at their block diagram in Figure 5 below. The zero-IF receiver architecture, which is also known as homodyne receiver or direct conversion receiver, has its IF at DC. This selection of the IF removes the problem associated with image rejection as now the LO signal and the input signal are at the same frequency. Hence full integration of the receiver is now possible as the high-Q filters are no longer needed. However, this is done at the expense of DC off-set issue which may cause saturation of the receiver system and the higher flicker noise at low frequencies. Also, in zero-IF receivers, quadrature down-conversion is needed to prevent signal loss. Overall, the zero-IF architecture is still the simplest form of receiver architecture and most suitable for full integration.

Figure 5: Low-IF or Zero-IF Receiver Architecture

The low-IF receiver architecture on the other hand, tries to minimize the DC-offset issue of zero-IF receiver by setting its IF less than the signal BW but not zero. However, for such architectures, the image issues re-surface as the image signals are now so close to the input signal that the use of an image reject filter is almost impossible. Similar to the zero-IF architecture, the IF of the low-IF architecture is now sufficiently low that a second down-conversion is unnecessary and the IF signals can be directly filtered and presented to the ADC. This however, will put more demand in the filter and ADC designs. Although the low-IF receiver needs higher performance filter and ADC, the high-Q image filter is not needed and therefore still makes the architecture suitable for full integration. The image issue of the low-IF receiver can still be tackled using the image-reject architecture that uses quadrature mixing, making its architecture now almost identical to that of a zero-IF receiver.

2.3 Technology Trends

Radio Frequency Integrated Circuits (RFICs) are traditionally designed using the GaAs or Si-bipolar technology due to their superior high frequency performance as compared to the CMOS technology of comparable technology nodes, even though CMOS is the cheaper and more dominant technology for almost all other systems.

The insufficient RF performance of CMOS devices delayed the entrance of RFICs into CMOS technology, depriving it from the cheaper fabrication cost and the prospect of full Systems-on-Chip (SoC) integration, which would also bring about lower cost due to the reduction of the component count.

Figure 6: Progress of the Cut-Off Frequency of Different Devices [9]

Figure 6 above shows the progress of the cut-off frequency (f_T) of NMOS with other devices. The f_T of NMOS has increased to approximately 100GHz at the production level in year 2000, which is a sufficient performance for most consumer market based wireless standards that normally uses the low-GHz frequency bands. Once the issue of low f_T is overcome, coupled with the modification to conventional CMOS process that produces reasonably better inductors [10], full integration of RFICs in CMOS technology are reported, both in academia papers and commercial products [11].

The full integration of RFICs also brought about solutions to the issue of multi-standard radios, especially in the receiver systems. Multiple receiver front-ends can be

implemented in parallel on the same chip, at the cost of larger chip area, to support multi-standard operation. The analog baseband and digital signal processing systems, on the other hand, becomes more complex but need not be entirely duplicated to support more standards.

Very soon, a single, high performing receiver front-end becomes realizable and can easily replace the use of multiple front-ends to save on the chip size. This design, however, is still based on the classic RF techniques. CMOS implementation of the RFICs provides ample chance of innovation. The availability of MOSFET switches and the support of powerful digital circuits, paves way for the design of what is loosely acknowledge as digitally-assisted RF systems. One such example is the development of digital receivers that utilized quantized sub-sampling [12], whereas this thesis tries to explore the idea of digitally controlled flexible receiver front-end. Both of which, are highly suitable for multi-standard operation.

Chapter 3 – Literature Review on Low-Noise Amplifiers

3.1 Conventional LNA Topologies

As previously discussed, the role and importance of an LNA is to provide adequate gain at minimum noise such that the noise contribution of the subsequent stages can be reduced accordingly, depending on the gain of the LNA. This is the direct result of being at the first active block of the receiver system. Furthermore, being the first active block also means that the input of the LNA needs to be properly designed to link with the off-chip passive filters. Therefore the LNA's design and performance plays a very significant role in the overall performance of the receiver system. Thus, in the design of LNAs, one will need an understanding of the different LNA design requirements before the actual designing process takes place.

Other than providing low noise and high gain, another important requirement of the LNA is to provide an input matching to the RF filter in front of it. In RF designs, matching is important as it allows for maximum power transfer in the receiving path, especially in the very high frequency range where almost all kinds of connectors will behave like transmission lines. Thus matching is required to reduce the reflected signals where the signal paths are connected through these transmission lines. On top of minimizing the reflected signals, the RF filters preceding the LNA, which are commonly designed using passive components, needs proper output matching load from the LNA for its operation.

This is the reason why even though in fully integrated receiver designs, where voltage levels are usually used instead of power levels, input matching of the LNA is still a necessary requirement [7]. The output matching of the LNA is not necessary required now. This is because in the full integration of the receiver design that uses either the low-IF or zero-IF architectures, the output of the LNA no longer needs to drive an off-chip passive high-Q filter. This difference thus allows more room for better optimization of the LNA. Power consumption of the LNA can also be reduced as the previously required buffer that drives the matching output load can now be removed completely.

Finally, the operating frequencies of the LNA complete the few notable requirements of a LNA. The need to provide the required gain at the desired high frequencies is still the primary function in LNA designs. Such frequency selectivity in LNA also helps to provide some form of linearity enhancement to the out of the band signals as they are not amplified.

Considering the different requirements of a LNA design as discussed above, the different LNA topologies that are commonly used are presented in the following subsections, which helps to give a better understanding of their respective advantages and disadvantages and relates to why and where these LNA topologies are used.

3.1.1 Noise Theory of Two-Port Network for LNA Designs

Before the different LNA topologies are introduced, there is a need to introduce the noise theory of two-port networks, which has been the fundamental to the design of

LNAs. The noise theory is based on the use equivalent input noise voltage ($\overline{e_n}$) and noise current ($\overline{i_n}$) to represent the total noise of a noisy two-port network as shown in Figure 7 below.

Figure 7: (a) Noisy Two-Port Network (b) Noiseless Two-Port Network with Equivalent Input Noise

Figure 7 above also includes the noise of the signal source ($\overline{i_s}$), which is associated with its internal admittance (Y_s). From the noise factor equation shown earlier in (1), the noise factor of the above two-port network is [5, 6]:

$$\text{Equation (26): } F = \frac{\overline{i_s^2} + |\overline{i_n} + Y_s \overline{e_n}|^2}{\overline{i_s^2}}$$

After some complex derivation, equation (26) can be expressed as [6]:

$$\text{Equation (27): } F = 1 + 2R_n(G_{\text{opt}} + G_c) + \frac{R_n}{G_s} \left[(G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 \right]$$

In equation (27), G_s and B_s represent the conductance and susceptance component of the source admittance ($Y_s = G_s + jB_s$), while G_{opt} and B_{opt} represent the optimum source conductance and susceptance ($Y_{opt} = G_{opt} + jB_{opt}$) for the minimum noise factor. At $Y_s = Y_{opt}$, the noise factor of the two-port network will be at its minimum, which is:

Equation (28): $F = F_{min} = 1 + 2R_n(G_{opt} + G_c)$ for $Y_s = Y_{opt}$

Y_{opt} is derived as:

Equation (29): $Y_{opt} = \sqrt{\left(\frac{G_u}{R_n} + G_c\right)^2} - jB_c$

To complete the explanation of the terms in the equations (27) to (29), R_n is the noise resistance associated with $(\overline{e_n})$, G_u is the noise conductance associated with $(\overline{i_u})$, the un-correlated part of $(\overline{i_n})$, while Y_c (where $Y_c = G_c + jB_c$) is the coefficient of the correlation part of $(\overline{i_n})$, and:

Equation (30): $R_n = \frac{\overline{e_n}}{4KT}$

Equation (31): $G_u = \frac{\overline{i_u}}{4KT}$

Equation (32): $\overline{i_n} = \overline{i_u} + Y_c \overline{e_n}$

The above equations and especially equation (28) suggest that the minimum noise factor ($F_{\min}$) can only be achieved at some specific source impedance. However, in almost all applications, the source impedance is usually fixed by the passive components used prior to the two-port network as briefly discussed earlier.

Therefore to achieve $F_{\min}$, matching network is usually added such that Y_s is transformed to be equal to Y_{opt} , which is commonly known as noise matching. It is obvious that the noise matching requirement is entirely different from the power matching requirement, which means that noise match and power match will usually not occur at the same time. As a result, a compromise between the gain and noise matching is usually done using the constant noise circles and the constant gain circles in the Smith Chart.

Other than noise matching, equation (27) also suggests another way to achieve very low noise figure, which is to reduce the absolute value of R_n . The reduction of R_n not only reduces the absolute value of $F_{\min}$, it also reduces the noise that arises due to the mis-match of Y_s and Y_{opt} .

There are two major ways to reduce the absolute value of R_n , one is to use higher current for the LNA and the other is to operate the LNA at frequencies much lower than its unity gain frequency (f_T). In fact, it is shown [6] that by operating at frequency 20 times smaller than f_T , it is able to achieve a $NF_{\min}$ of less than 1dB, which far exceed the usual sub-3dB requirements.

3.1.2 Common Source LNA with Resistive Termination

The common source LNA with resistive termination (R-CSLNA) is developed mainly to provide the required input matching to the preceding RF filter. Shown in Figure 8 below, a 50Ω resistor R_1 is added in parallel to the input of the LNA for achieving the input matching of the LNA to the 50Ω source resistance R_s . Ignoring the capacitive input of the input transistor M1, this design has a very wide-band input matching.

Figure 8: Common Source LNA with Resistive Termination

However, the major drawback of the R-CSLNA topology is also the added resistor which generates noise that is of equal magnitude to the source resistance. By considering only the output noise due to R_s , R_1 and the drain noise of M1, the noise factor is [7]:

Equation (33):
$$F = 2 + \frac{4\gamma}{\alpha g_{m1} R_s}$$

In the equation, γ and α are device dependent constants and g_{m1} the transconductance of M1. The NF of the R-CSLNA is therefore substantially higher than 3dB and not suitable for very low noise applications. This is because other than generating noise, the presence of R_1 also causes the attenuation of the input signal at the input matching network, which leads to the increase of the noise contribution of the drain noise of M1 by a factor of four. Therefore, as the derivation shows, the R-CSLNA topology is not a popular choice for many.

3.1.3 Common Source LNA with Inductive Degeneration

The inductive degeneration common source LNA (L-CSLNA) shown in Figure 9 below is the most popular topology in narrowband LNA designs. It is generally accepted as the best performing narrowband LNA topology, simply because it can provide perfect input matching, high gain and low noise at the same time [13].

Figure 9: Common Source LNA with Inductive Degeneration

In L-CSLNA, the source inductor L_s is added to provide the required input matching while the gate inductor L_g is added to provide the desired input resonance frequency. Including the input capacitance C_{gs} of M1, the input impedance of the L-CSLNA can be derived as:

$$\text{Equation (34): } Z_{in} = j \left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}} \right) + \frac{g_m L_s}{C_{gs}}$$

The second term of the equation is a resistive term and can be designed to be equal to 50Ω to provide input matching. Most interestingly, this resistive term does not produce noise as oppose to a physical resistor. However, for the input matching to occur, the reactive terms must be equal to zero and this can only happen at one particular frequency, which is the series resonance frequency. Ignoring the noise of the inductors, the noise factor of this topology by considering only the drain noise of M1 is [13]:

$$\text{Equation (35): } F = 1 + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T} \right)^2$$

In the equation, g_{d0} is the drain output transconductance at zero drain source voltage ($V_{ds} = 0$ V), ω_0 is the operating frequency and ω_T is the cut-off frequency of M1. Depending on the ratio of ω_0 and ω_T , the F of the L-CSLNA can be made impractically small and is not possible in actual designs. More detailed analysis of the noise of the L-CSLNA that includes the induced gate noise of M1 has been done [13] but their results still suggest that the noise performance of L-CSLNA is far better than other topologies. This is partly due to the use of the series resonance input matching network that allows

a voltage transformation of the input signal such that a passive voltage gain is observed over the input matching network, which is also the reason behind the high gain of the L-CSLNA topology.

This LNA topology, though popular, can only be useful in narrowband designs due to the use of inductors to realise the input matching at one particular series resonance frequency. In situations where wider bandwidth is required, designers will have to shift to other topologies even though they exhibit more noise.

3.1.4 Common Source LNA with Shunt Feedback

The common source LNA with shunt feedback or simply a resistive feedback LNA (RFLNA) shown in Figure 10 below has not been popular due its large power consumption used to achieve low noise. The RFLNA uses a shunt feedback resistor R_{fb} to realize the feedback of the output to the input.

Figure 10: Common Source LNA with Shunt Feedback

The main purpose of R_{fb} is to provide the input matching resistance of the RFLNA. The input matching of this topology is similar to the R-CSLNA where a physical resistor is used and hence is able to provide a wideband matching. However in this case, R_{fb} can be substantially larger than the 50Ω due to the feedback network. Again, by ignoring the C_{gs} of M1, the input impedance of FBLNA is now [5, 6]:

Equation (36):
$$Z_{in} = \frac{R_{fb} + R_d}{1 + g_{m1}R_d}$$

The equation shows that if g_{m1} can be sufficiently large, the value of R_{fb} can be made larger, which means that its noise contribution can be minimized. Larger value of g_{m1} also reduces the drain noise contribution M1 and provides larger gain. However, this is usually achieved by using large power consumptions and hence is not a popular topology even better wideband performance can be achieved.

3.1.5 Common Gate LNA

The common gate LNA (CGLNA) shown in Figure 11 below is therefore the most popular topology for wideband designs. Being able to provide wideband input matching at acceptable noise figure and power consumption, CGLNA topology is able to meet most of the wideband requirements.

Figure 11: Common Gate LNA

The input impedance CGLNA is approximately equals to the inverse of g_{m1} ($Z_{in} = 1/g_{m1}$). Since g_{m1} is relatively constant over a wide frequency range, the input matching of the CGLNA will be wideband just by the proper design of g_{m1} ($g_{m1} = 1/50 \Omega$). However, this requirement of the g_{m1} limits the noise performance of CGLNA topology. By considering only the drain noise of $M1$, the noise factor of a matched CGLNA is:

Equation (37): $F = 1 + \frac{\gamma}{\alpha}$

In equation (37), γ and α have typical values of about 2/3 and 1 in submicron MOSFET which means that the NF of CGLNA will be around 2.2dB, which is good enough for most applications. In actual case where other noise contributors are considered, the NF of CGLNA can still be maintain at below 4dB, which is still acceptable for many applications, especially the wideband applications that normally expect more noise. Hence this topology leads the popularity for wideband applications.

3.2 LNAs in Multi-Standard Receivers

The discussions on the different LNA topologies earlier show the usefulness of the different topologies when there are different needs. In narrowband applications, L-CSLNA gives the best performance at low power. CGLNA on the other hand, provides wideband operation with an acceptable noise performance and at low power. RFLNA can provide better noise performance with wideband operation but at high power consumption. It is therefore, necessary to understand the needs of the LNA in multi-standard receiver so as to find the most suitable topologies. This section will first try to explain the different kinds of multi-standard receivers and then subsequently, briefly discuss the different LNAs used in these multi-standard receiver front-ends.

Multi-standard receivers are required to support the operation of more than one wireless standard. The different wireless standards often have different requirements on the front-end performance. Therefore, a multi-standard receiver generally needs to meet the demand of multiple requirements.

There are basically three main approaches to meet the many demands [14, 15]. To help in the discussion on the different approaches, the meaning of a receiver front-end will be narrow down so as to provide a common ground for better understanding. Firstly, as previously indicated, the zero-IF architecture will be the only receiver architecture considered due to its simplicity, wideband compatibility and potential for full integration. A simplified diagram of the zero-IF receiver without the compulsory quadrature mixing is shown in Figure 12 below.

Figure 12: Simplified Zero-IF Receiver

The zero-IF receiver has generally become the norm for multi-standard receiver. Other than the possibility for full integration, the straight forward frequency planning of the architecture also makes it suitable for operating in many different carrier frequencies, even though this is often at the expense of requiring a wideband PLL system. However, in this thesis, where the focus is on the LNA design, these other important concerns of the receiver is put aside by assume an integrated LO is always available.

Therefore, the kind of LNA used in the receiver front-end will be solely used to classify the three approaches in multi-standard receiver designs. The simplified architectures of the three approaches are shown in Figures 13 to 15 below.

Figure 13: Multiple Narrowband LNAs

Figure 14: Single Multiband or Wideband LNA

Figure 15: Single Flexible LNA

These approaches in realizing multi-standard receivers also partly reflect the trends in the implementation of multi-standard receivers. Initially, when full integration of the receiver front-end becomes possible, multiple LNAs are used in order to achieve multi-standard operation. This method is more feasible then due to the fewer number of available standards. Thus, very soon, the design of single wideband LNA that is able to meet the worst-case requirements of the different standards becomes available. The high performance of such LNAs allows it to work across more standards without significant increase in the die area needed. However, large power consumption is often required as these LNAs cannot be optimized specifically for each of the desired operating standard. Therefore, recently, flexible LNAs are seen to improve the efficiency of the multi-standard receivers.

For the multiple LNA approach in Figure 13, as multiple narrowband LNAs are used, they can be individually optimized and hence power efficient but they consume large area as these LNAs usually used the L-CSLNA topology that requires three large inductors. Since this research focuses on the design of flexible LNA, this approach will not be discussed further. For the single wideband LNA approach in Figure 14, many wideband design techniques are available and proposed to improve the gain and noise performance of these designs at low power. However, they are again not discussed further. As for the case of the flexible LNA approach in Figure 15, the State-of-the-Art designs will be presented and discuss in the following sub-section.

To provide a more insightful comparison of these three approaches, a qualitative comparison table below briefly summarizes the advantages and disadvantages of these different approaches.

Table 1: Comparison of Different Multi-Standard LNA Approaches

	Multiple LNA	Wideband LNA	Flexible LNA
Area (Cost)	Very large. There is a need to use up to three inductors for the individual LNA used.	Large, A few inductors are need to create broadband matching and broadband resonance.	Large, A few inductors may be needed to achieve flexible frequency bands.
Power Consumption	Very high efficiency. Since each LNA is being individual optimized, the power consumption is usually the minimum possible for normal operation.	Low efficiency. High power is often needed to maintain the good performance across the different frequency bands.	High efficiency. Extra power may be needed to cater for the flexibility but power saving can occur when less stringent performance are required.
Performance	Very good. All LNAs should perform to the minimum requirement	Good. The LNA usually meet all the requirements.	Good. The LNA can change its performance to meet the requirement.
Ease of Design	Simple. Many report example of LNA optimization design techniques.	Complicated. Multiple considerations are needed to maintain the performance across different frequencies.	Complicated. Enormous efforts are needed to implement the flexibility.
Concurrent Operation	Possible if multiple back-end circuits available	Possible if multiple back-end circuits available.	Not possible.

Also, to complete the different solutions to a multi-standard receiver, Figures 16 and 17, which involves direct sampling and sub-sampling respectively are shown below. Although both designs are different to the traditional receiver architecture, they still demand a wideband LNA, which will still be beneficial if it is replaced by a flexible LNA.

Figure 16: Direct Sampling Receiver

Figure 17: Sub-Sampling Receiver

3.3 Flexible LNAs

The State-of-the-Art flexible LNA designs are mostly focused on achieving flexibility in the operating frequencies of the FLNA. One important assumption of all FLNA is that concurrent operation of more than one standard is not required and therefore, the FLNA can change its performance parameters in real time while still maintaining the wireless connection, though the standards involve can be different from time to time. This disadvantage of the FLNA will be discussed in more details in the next chapter as the section will focus on the design techniques in achieving flexible operating frequencies of the FLNAs.

3.3.1 Brief Organization of FLNA Design Techniques

Many FLNAs have been identified and review during the research. Their analysis and design will be presented in this section. The study of FLNA is not a simple task due to the confusion of the term flexible. Nonetheless, many designs though not necessary are truly flexible, still contain flexible design techniques that may are useful in designing a FLNA. These design techniques are briefly organized according to Figure 18 shown below.

Figure 18: Brief Organization of Published Flexible Design Techniques

Referring to the diagram in Figure 18 above, the design techniques are organized into five main categories. It is more useful and specific to organize them according to the design techniques instead of the changeable parameters to keep to the research focus on identifying the useful flexible design techniques.

These categories are normally the physical area where controls are added into their designs for achieving flexibility. The controls are implemented either by switching for discrete changes or tuning for continuous changes. As can be seen later, some designs actually use more than one technique at the expense of more a complex design to achieve more flexibility and therefore appeared in more than one category.

3.3.2 Flexible Design Techniques

Out of the many publication that shows flexible design techniques, only selected of them will be discussed in this section to show the more interesting design techniques. The relevant circuit diagrams available in the publications will be shown, together with an explanation on the working principle and a short discussion on the pros and cons of the presented designs.

For clarification purposes in the following review, when explaining the working principles, switchable and tunable are used to separate the idea of flexibility into discrete change and continuous change respectively.

Passive Components – Output

Both Figure 19 and 20 below show the design technique that involves the switching of the output passive components for flexible output resonance frequencies. Switches are used to select the inductors [16] or capacitors [17] that are pre-designed for the different output resonance frequencies. However, both designs still use a wideband input matching network which is not considered as flexible.

Figure 19: A Multi-Band CMOS RF Front-End for 4G WiMAX and WLAN Applications [16]

Figure 20: A Tunable Multi-Band CMOS LNA for Mobile WiMAX [17]

The design technique in Figure 18 also allows switchable transistor sizes that can provide better optimized performance. The switches used are actually the cascode transistor in the LNA. However, this design also uses more inductors that occupy large chip area. This design also has multiple outputs that will need a more complex multiple-input mixer at the subsequent stage. Figure 19 on the other hand has no such issues.

Passive Components – Input and Output

Both Figure 21 and 22 below show the design technique that involves switching both the input and output passive components to achieve both flexible input matching and output resonance frequencies.

Figure 21: A New Technique for Design CMOS LNA for Multi-Standard Receiver [18]

Figure 22: A Sub-2 dB NF Dual-Band CMOS LNA for CDMA/WCDMA Applications

[19]

Figure 21 achieves flexibility by adding a parallel switch and capacitor across the input, inter-stage and output inductors to allow switching of input and output resonance frequencies [18]. However, this is done at the expense of additional noise from the switches, especially for the switch used across the input inductor. Figure 22 on the other hand, adds a parallel switch and capacitor across the input transistor and the output load for switching of the input and output resonance frequencies [19]. This design technique has better noise performance than Figure 21 but at the expense of limited frequency range due to the limitation on the size of the parallel capacitor. Large capacitor will narrow down the bandwidth of the FLNA and allows more noise of the switch into the input.

Passive Components – Tunable

Figure 23 below tries to change the input matching frequencies by tuning the input effective inductance [20]. An amplifier and a variable resistor are used to form a complex feedback circuitry that has the ability to change the input effective inductance through the variable resistor. This design technique in theory can allow a continuous tuning of the input matching frequency. However, this approach needs additional power to drive the additional circuitry that can consume up to 40% of the total power needed. Also, noise from the additional circuitry also affects the overall noise of the FLNA.

Another tunable design technique is shown in Figure 24 below [21]. This technique simply uses a varactor at the output load to achieve continuous tuning of the output resonance frequencies. The frequency tuning range of this technique is however, limited by the tuning range of the varactor.

Figure 23: A CMOS Low-Noise Amplifier with Reconfigurable Input Matching Network [20]

Figure 24: A 3-5 GHz Frequency-Tunable Receiver Frontend for Multiband Applications [21]

Transistor Size & Biasing Condition

Both Figure 25 and 26 shown below use the technique of switching on more parallel input transistors to increase the total size of the input transistors [22, 23]. This result in the increase of the input capacitance of the input matching network and cause input matching frequency to vary. Due to the increase in size of the input transistor, the input transconductance and current consumption of the input transistor also varies. Hence to provide adequate matching, the bias condition of the input transistor also has to be changed accordingly and as a result, more power is often consumed with larger transistor width. Also, this technique needs deal with the noise of the switches that is directly connected to the input.

Figure 25: A Compact 2.4/5.2-GHz CMOS Dual Band Low-Noise Amplifier [22]

Figure 26: A 2.1 to 6 GHz Tunable-band LNA with Adaptive Frequency Responses by Transistor Size Scaling [23]

Feedback Amount

Figure 27 below shows the design technique involving feedback. Based on the resistive feedback topology [24], input matching can be achieved through the effective input resistance due to the feedback resistor and open loop gain of the LNA. Therefore, by switching the resonance frequency of the output load, gain of the LNA and hence input matching of the LNA will both be achieved at the switched resonance frequency of the output load.

Figure 27: A Multi-Band 900MHz/1.8GHz/5.2GHz LNA for Reconfigurable Radio

[24]

Figure 28 below shows another design technique involving feedback. This technique on the other hand, is based on a common gate topology with positive feedback [25]. Again, through the use of feedback, the input matching frequencies are dependent on

the resonance frequencies of the load. The used of positive feedback in this technique has the benefit of improved effective transconductance. However, this is done at the expense of the stability of the LNA. To ensure enough stability, the increase in the effective transconductance becomes limited and the tuning range of the LNA becomes limited as well.

Figure 28: A 0.13 μ m CMOS Front-End, for DCS1800/UMTS/802.11b-g With Multiband Positive Feedback Low-Noise Amplifier [25]

3.3.3 Summary of Flexible Design Techniques

Most of the reviewed flexible design techniques are based on the inductive degenerative common source (L-CS) topology. This is mainly because of the superior narrowband performance of the L-CS topology and its ease of designing. As

mentioned, these designs focus on achieving flexible operating frequencies, which are generally narrowband in nature. Therefore, it is not surprising that the high performing, narrowband characteristic of the L-CS topology are being utilized for its excess performance margin so as to realize the additional “degree of freedom” required for flexibility.

However, it can be seen from the almost all the techniques above [16-23], the L-CS topology is not really suitable for flexibility [25]. Additional circuits are both needed at the input and output individually to achieve proper input matching and output resonance concurrently. The bias condition of the L-CS topology is also rather restricted as any change of transconductance of the input transistor will affect the matching of the LNA. Techniques that try to change the input transistor sizes again require the bias conditional to be changed accordingly.

On the other hand, feedback techniques seem to be more suitable for flexibility [24, 25]. Circuits are only added at the output of the designs and yet it can achieve both input matching and output resonance at the same time. This technique is therefore explored in our design and will be presented in details in the next chapter.

Finally, to provide better comparison of the different design techniques, a summary of the performance of all the above selected design techniques are provided in Table 2 below.

Table 2: Summary of Selected Design Techniques

Paper	Frequency (GHz)	NF (dB)	S21 (dB)	S11 (dB)	IIP3 (dBm)	Power (mW)	Vdd (V)	Method	Process
[16]*	2.6	2.5	32	-25	-16.9	45	1.8	A, C, E	180nm
	3.6	3.5	32	-40	-7	45			
	5.5	5.9	32	-13	-7.8	48			
[17]	2.7	1.97	9.13	-11	2.2	7.5	1.2	A	130nm
	3.5	1.55	10	-11	3.2	7.5			
	5.55	1.86	10	-13	1.43	7.5			
[18]	0.95	2.6	24.9	NA	-21.55	9.04	1	A	180nm
	2.14	3.96	23.3		-6.27	9.04			
[19]**	1.8	1.75	14.54	-11.52	-5.8	7.5	1.5	A, B, E	130nm
	2.14	1.97	16.6	-15.18	-5.3	7.5			
[20]	2.4 – 5.2	2 – 4.2	19 – 23	-13	-3	17	1.2	A, E	130nm
[21]***	3.0	17.4	19.8	-10.5	-2.4	8	2.0	A	180nm
	4.0	15.4	24.6	-11.8	-6.0	8			
	5.0	16.2	20.6	-15.2	-2.7	8			
[22]**	2.4	2.9	10.1	-10.1	4	11.7	1.8	A, B, C	180nm
	5.2	3.7	10.9	-11	-5	5.7			
[23]**	2.5 – 5.4	2.16 – 2.81	15.2 – 17.0	-20.5	-3.9 – 0.5	3.6 – 24.3	1.2	B, C	90nm
[24]**	0.9	2.3	14	-12	-14	7.5	1.8	A, D, E	180nm
	1.8	2.9	13	-14	-14	7.5			
	5.2	2.6	16	-15	-14	7.5			
[25]***	1.8	5.2	13.5 – 28.5	-33	-7.5	24	1.2	A, B, C, D	130nm
	2.1	5.6	14.5 – 29.5	-20	0	24			
	2.4	5.8	8.4 – 23.4	-20	-4.8	24			

*Front-end simulation result

**LNA + buffer measurement result

***Front-end measurement result

Method A – Passive component

Method B – Bias condition

Method C – Transistor Size

Method D – Feedback

Method E – Others

Chapter 4 – Proposed Idea of Flexible Receiver Front-End

4.1 Definition of Flexible Receiver Front-End

The definition of a flexible receiver front-end in this research, which can be extended to all relevant front-ends, is actually trying use the word “flexible” as a universal term to describe any front-ends that have the ability to change the performance parameters of its individual building blocks.

To the author’s awareness, the idea of such a flexible front-end was first proposed in 2003 [14]. The paper, without presenting a complete solution, described that “*systems with multifunctional components*” where “*functional blocks have to change not only their specifications but also their functionalities*” is the “*most advanced method*” to “*fulfill all different standard requirements.*”

Later in 2005, Gielen [26] introduce the term of “flexible” to describe a “*transceiver with reconfigurable building blocks*” where “*performance and hence power consumption can be scaled.*” And finally, Rosa in 2009 [27], describe in the system level that “flexibility” refers to “*the ability of circuits and systems to reconfigure their topology and to adapt their performance to different specifications.*”

To put them together, a flexible receiver front-end or in general, a flexible front-end or a flexible system should have the ability, through digital controls or software programmability, to change the performing parameters of its own individual building

blocks, through scalable power trade-offs, so as to suit the different requirements of the different standards or signal conditions at maximum power efficiency.

It should also be noted that receiver front-ends that use the idea similar to Figure 13, where different building blocks can be reconfigured to achieve changeable performing parameters when looking at the system level, are not considered flexible.

4.2 Other Terms Similar to Flexible

As previously mentioned, the word “flexible” are used as a universal term. The need of such a universal term is due to the tremendous interests in multi-standard radio designs that many terms are used in the publications to best describe the techniques implemented in their designs. This can cause some confusion in identifying the different flexible design techniques. For design approach similar to Figure 13, terms like “reconfigurable”, “programmable” and “switchable” are often used. For design approach similar to Figure 15, terms like “adjustable”, “tunable”, “changeable” and “variable” are used. Also, more generic terms like “multi-standard”, “multi-functional”, “multi-band”, “adaptable”, “digitally controlled” and “software defined” are also used. To make the situation worse, some of the terms are used in both approaches which make it difficult to identify the true flexible designs. On top of this, many actual designs actually use a combination of the different approaches and cannot be considered as either flexible or inflexible.

Therefore, the understanding of these terms becomes important not only to effectively identify the different design techniques but also shows the need of having such a

universal term for clearer differentiation. And most important of all, provides a clear path to the research work.

4.3 Proposed Design Strategy and Performance Parameters

Most published flexible designs place less significance in the flexibility and emphasize on multi-standard operation. In which different selected standards are first analyzed to provide a range of performances that the flexible design must achieved. And as a result, “reconfigurable” becomes the most common term to describe the design being able to be re-configured to the different standards.

However, in this research, the idea of flexibility is being place at the top priority. The idea to achieve as much flexibility as possible is first explored in the design. And it is assumed that all relevant benefits of a flexible design will be achieved as an inherent result.

For better illustration, a flow chart shown in Figure 29 below shows the proposed design strategy process. To avoid the flexibility of the design being irrelevant, pre-defined worst case requirements of the different standards are first being identified. A single standard circuit topology which has high performance and also potentially suitable for flexibility is then adopted and designed to meet the pre-defined requirements. The flexible circuit design techniques are then “added” into the design to serve as a kind of “degree of freedom” to the adopted circuit topology to achieve flexibility.

Figure 29: Flow Chart of Design Strategy

The designed flexible receiver front-end will then be characterized for its flexibility. However, it is not so straightforward to characterize a design's flexibility. By enhancing previous publications [28, 29], new set of parameters are proposed to specifically targets the flexibility of the designs. These parameters are namely, tuning range, tuning step, settling time and power trade-off ability.

Tuning range refers to the range of achievable performance parameters of the flexible designs [28]. Tuning step refers to how the performance parameter varies where it can be varied through either continuous or discrete step changes. Settling time refers to the

time the flexible designs needs before it reaches a steady state ready for operation after a change is occurred [29]. Finally, rather than the usual way of comparing through standard Figure of Merits (FOMs), a power trade-off analysis of a flexible design that takes into account the extra (or less) power used when the design changed into better (or worst) performance can be used to provide a much better comparison of the different designs.

After the characterization on the flexibility of the designed receiver front-end, it is then used to filter with the different standards. The requirements of different standards are placed together with the tuning range of the flexible receiver front-end. As long as the requirement of a specific standard falls into the tuning range of the flexible receiver front-end, the designed flexible receiver front-end can work in that particular standard. After all the suitable standards are being identified, settling time analysis will be needed to make sure that the designed flexible receiver front-end can change its performance needed for the different standards in the allocated time frame of the standards. Finally, the power trade-off ability of the designed flexible receiver front-end will be useful to provide a fair comparison with the other multi-standard or single-standard receiver front-ends.

4.4 Inherent Benefits and Issues of Flexible Receiver Front-End

There are many features and benefits to design a flexible receiver front-end but we would like to treat them as inherent once we achieved a truly flexible design. These benefits include the ability for multi-standard operation, shorter development time, better real time efficiency and less sensitive to process variation. All of them will be

possible if a truly flexible design exists. Therefore, by focusing on designing a flexible receiver front-end, we always assume these benefits will surface if sufficient flexibility is attained.

However, such a flexible receiver front-end has several drawbacks and will also be discussed.

One concern of a flexible approach is the issue of concurrent operation. It is usual that a mobile device will need to be able to maintain two or more separate radio links simultaneously under normal usage. This calls for the requirement of concurrent operation of the multi-standard radio. For the solution that uses multiple parallel building blocks, the issue can be easily solved. However, when a flexible solution is used, this is not possible and more than one such flexible radio will be required. It has been proposed though [30], that the flexible radio can switch between standards through methods similar to time division multiplexing, however, this will put constrain into the settling time requirement of the flexible radio.

Another issue may arise if too much flexibility is being achieved. This issue generally requires system level analysis for better understanding. The ultimate requirement of a receiver is its sensitivity at the input and its bit error rate that appear at the output. Therefore, it is possible that not all changes in the performance parameters of the individual building blocks can have significant effect on the overall receiver performance. Hence, system level analysis on the most impactful parameters of the building blocks and the trade-offs between them will be needed for better designs.

Lastly, the need for control signals is also an important issue to consider. More pin counts will be necessary to implement the control signals that change the parameters of the flexible receiver. This will make the design of the flexible receiver more complicated and increase the effort needed to test the design.

Chapter 5 – Proposed Flexible Low-Noise Amplifier

5.1 Design Considerations of Proposed Flexible Low-Noise Amplifier

The discussions in the previous chapter on the idea of flexibility present many challenges to the implementation of a FLNA. It is suggested that a truly FLNA should be able to change as many of its performance parameters as possible with suitable power trade-offs. However, such flexibility in these parameters, which includes noise figure, gain, linearity and operating frequency, is very difficult to be designed and achieved simultaneously. Currently, no truly FLNA are reported.

There are several reasons to why a truly FLNA does not exist yet. Other than technology limitations, such FLNA might not be seen as important in the past because multi-standard radios are not popular then. Also as suggested earlier, one major issue of a flexible design is the need to avoid too much flexibility. This means that a truly FLNA can only be beneficial if the achieved flexibility is of significant impact and at the same time does not require large power and area consumption. Therefore, although the focus of this research is to achieve a truly flexible designs, only selected more significant parameters are considered and made flexible in the proposed FLNA.

The first considered parameter is the operating frequencies of the proposed FLNA. The operating frequency of LNAs usually refers to the frequency where there is sufficient input matching. Consequently, due to the narrowband feature of most wireless standards, both the peak gain and the minimum noise figure are also designed at this frequency. As a result, the operating frequency of an LNA entirely determines its

relevance. Thus, in order to design a FLNA usable for multi-standard radios, achieving flexible operating frequencies is seen as the one of the most important considerations. This is also justified by the reviews of the recently published State-of-the-Art FLNAs presented earlier.

On top of achieving flexible operating frequencies, the proposed FLNA further considers the potential of achieving flexible noise figure and gain, which are lacking in many of the reported FLNAs. These again are very important parameters for LNA designs and should also be made flexible for better optimization of the receiver front-ends.

By considering these parameters, the design and simulation results of the proposed FLNA will be presented in the following sub-sections. Other performing parameters, like the linearity and stability of the FLNA, on the other hand, are seen as less impactful and thus not made flexible. Nonetheless, they will still be designed to perform comparably to other reported designs in the proposed FLNA.

5.2 Circuit Description of Proposed Flexible Low-Noise Amplifier

With the above design considerations, the designed FLNA achieved flexible operating frequencies with the potential of having both flexible noise figure and gain. Following the design strategy and the relevant design techniques presented in the earlier chapters, a resistive feedback low-noise amplifier (RFLNA) topology is being adopted in the proposed FLNA, instead of using the inductive degeneration common source low-noise amplifier (L-CSLNA) topology that has been proven to give the best narrowband

performance. This is because the L-CSLNA topology uses LC resonance at its input network to achieve its good narrowband performance, which may seem to allow it with some “headroom” to design for flexibility, actually has less potential for flexibility as discussed in the earlier reviews and also mentioned in [25].

Figure 30: Proposed Flexible Low-Noise Amplifier

The simplified schematic of the proposed FLNA is shown in Figure 30 above. Based on the RFLNA topology, a cascode transistor M_2 is added to reduce the miller effect of

the gate-drain capacitance of transistor M1 to improve stability. The resistive load is also being replaced by a switchable LC load in the proposed FLNA. This switchable LC load provides the desired range of LC resonance frequencies.

In this design, the idea of tuning the output resonance frequencies together with the input matching frequencies through the use of resistive feedback [24] is being explored to achieve a FLNA. By using the LC load which is consist of switchable inductors in parallel with switchable capacitor bank, sufficient range of output resonance frequencies can be achieved. At the different resonance frequencies of the load, the peak gain of the FLNA occurs and as a result of the resistive feedback, the input matching of the FLNA also occurs. The proposed FLNA also includes a small gate inductor L_g to help provide a passive gain to the FLNA.

5.3 Analysis of the Proposed Flexible Low-Noise Amplifier

The analysis of the proposed FLNA is separated into three sections. Firstly, conventional RFLNA topology is being discussed in more detail to show its potential for flexibility, especially in its operating frequencies. Next, the flexible design techniques implemented to the RFLNA topology is being discussed to show how flexibility is being achieved. Finally, methods that can be used to further improve the FLNA performance will be discussed.

5.3.1 Conventional Resistive Feedback Low-Noise Amplifier

The conventional RFLNA topology shown in Figure 10 earlier and again shown in Figure 31 (a) below is usually used in wideband LNAs that demands good noise figures

with less consideration on power consumption. Briefly discussed earlier, both wideband gain and wideband input matching are easy to achieve in RFLNAs because the topology mainly uses resistors at both its input network for matching and its output load for gain instead of the narrowband LC resonators.

Figure 31: (a) Conventional RFLNA (b) RFLNA with R_{eff} (c) Small Signal of RFLNA
(d) Small Signal of RFLNA with C_d

The use of output load resistor (R_d) results in the wideband gain of the RFLNA, which subsequently accounts for the wideband input matching due to the effective input resistance (R_{eff}) that is seen at its input as shown in Figure 31 (b). The R_{eff} exists due to both the gain and the feedback resistor (R_f) and can be easily derived using the small signal analysis shown in Figure 31 (c). R_{eff} is equivalent to the Z_{in} in equation (36) and is derived as:

$$\text{Equation (38): } R_{eff} = \frac{R_f + R_d}{1 + g_m R_d} \approx \frac{R_f + R_d}{g_m R_d} \text{ for } g_m R_d \gg 1$$

In equation (38), g_m is the transconductance of the input transistor M1 and $g_m R_d$ is the open-loop gain of the RFLNA. This result shows the ease of achieving input matching in the RFLNA across wide range of frequencies as long as the gain (mainly g_m) remains relatively constant. This makes the topology very suitable for wideband designs and at the same time, shows its potential for flexibility. This unique ability to achieve input matching just by the proper design of the output load becomes the main reason why this topology is being adopted in the proposed FLNA.

However, before presenting the proposed FLNA, more insight into the RFLNA topology is needed to better understand its characteristics. Further analysis on the topology will not only serve as a guide in the design process of the FLNA but more importantly, help to identify its main drawbacks. These drawbacks will first be presented before the proposed FLNA, which will actually help to minimize many of these problems.

Firstly, the gain bandwidth of the RFLNA topology is being limited by the presence of the output parasitic capacitance (C_d). Due to C_d , the value of R_d is also being limited in order to maintain the large gain bandwidth (determined by $R_d C_d$). On top of that, the input matching bandwidth is also being limited by the gate-source capacitance (C_{gs}) of M1.

Other than the bandwidth issues, the RFLNA topology has also limited performance. The noise of conventional RFLNA is mainly contributed by both R_f and M1. Large value of R_f is needed to reduce its noise contribution. However, as shown in equation (38), large R_f requires a large g_m in order to maintain the input matching of the RFLNA. Larger g_m can be achieved by using larger transistor width or using larger current. The use of larger transistor width will cause an increase in its parasitic capacitance, which further affects the gain bandwidth of the RFLNA. The use of larger current, which means large power consumption, also has its limitations. Although large current can also improve the noise performance of the RFLNA, its effect is limited by the operating voltage of the RFLNA. Due to the use of R_d , large current will cause a large voltage drop across R_d . Hence in low voltage operation, the size of R_d will need to be reduced for the proper operation of the RFLNA, which will then reduce the gain of the RFLNA and partly reduce the effort to increase the g_m of M1. Thus, the size of R_f used is still being limited and its noise contribution will still be significant.

This commonly known drawback of the RFLNA topology heavily limits its popularity as briefly mentioned earlier. However, other than the above well-known drawbacks, the impact of C_d is worse than usually seems. Further feedback analysis of C_d reveals that

the presence of C_d can affect the bandwidth of the input matching as well. Small signal analysis of the RFLNA that includes the effect of C_d , as shown in Figure 31 (d), shows that R_{eff} is actually more complicated. By including C_d , the R_{eff} is now derived as:

$$\text{Equation (39): } R_{eff} = \frac{R_f + Z_d}{1 + g_m Z_d}$$

Where

$$\text{Equation (40): } Z_d = R_d // C_d$$

These expressions suggest that R_{eff} is actually a complex number and hence will now be replaced by the term Z_{eff} . Further derivation of Z_{eff} shows that Z_{eff} is actually a series combination of a resistive term and an inductive term (when $g_m * R_f > 1$). The expression of Z_{eff} is derived as:

$$\text{Equation (41): } Z_{eff} = \frac{(R_f + R_d + g_m R_f R_d + g_m R_d^2 + \omega^2 C_d^2 R_d^2 R_f) + j\omega C_d R_d^2 (g_m R_f - 1)}{(1 + g_m R_d)^2 + (\omega C_d R_d)^2}$$

This Z_{eff} expression suggests that the input matching frequencies will be affected by the inductance caused by C_d at the cut off frequencies where this inductance becomes less significant. The cut off frequency (f_0) is:

$$\text{Equation (42): } f_0 = \frac{1}{2\pi C_d R_d}$$

For practical C_d value of 400fF and R_d value of 50 Ω , this frequency is as high as 0.8GHz, which limits the lower end of the input matching bandwidth on top of the effect of C_{gs} as the input impedance is now:

Equation (43): $Z_{in(RFLNA)} = Z_{eff} // C_{gs}$

Therefore, to solve these issues, extra efforts are often employed to improve the bandwidth of the RFLNA [31, 32] which will not be discussed in this report. This is because in this research that focuses on flexibility, the wideband characteristic of the RFLNA is being given up in order to implement a flexible narrowband design. Such FLNA will still achieve comparable operating frequency range by using design techniques that will be discussed in the next section.

5.3.2 Implemented Design Techniques

In order to minimize the effect of C_d that exists in the conventional RFLNA, a resonating load consisting of the switchable inductors in parallel with a switchable capacitor bank is being implemented, replacing the R_d in the RFLNA. This technique converts the normally wideband RFLNA into a flexible narrowband LNA, which at the same time removes the concern of the C_d effect on the input matching and gain bandwidth of the RFLNA.

Although the wideband characteristic of the RFLNA is lost with this design technique, the implementation of such a flexible narrowband LNA will not lose out much if a sufficiently wide tuning range can be achieved. In fact, due to the narrowband nature of

most of the wireless standards (except for UWB), a flexible narrowband approach is actually more beneficial to the overall receiver design due to its inherent filtering feature [33]. To illustrate the possibility of using the RFLNA topology for narrowband designs, two simple simulations are done to justify its potential.

In the first simulation, the RFLNA is being modified as shown in Figure 32 below, which is a cascode RFLNA with its output load being replaced by an ideal inductor L_d in series with a modeled parasitic resistance R_{Ld} of quality (Q) factor being fixed at 8 across all frequencies. This inductor will resonates with the output node parasitic capacitance at a fixed frequency just like the usual use of LC load and as expected, the peak gain of this LNA occurs at the resonance frequency. Together with the proper design of the feedback resistor R_f , the input matching of this LNA can also be achieved at this frequency.

Figure 32: RFLNA with Ideal Variable Inductor

This is seen in the simulation results shown in Figure 33 and 34 below. In this simulation, as an ideal inductor is being used, its value can be easily varied to achieve different resonance frequencies. Figure 33 shows the various S_{21} of the LNA with five different practical inductor values being simulated and a wide range of resonance frequencies is achieved. Figure 34 shows the corresponding S_{11} of the LNA, which also peaks at the resonance frequency of the output load.

Figure 33: S21 of Different Inductor Load

Figure 34: S11 of Different Inductor Load

In the next simulation, the RFLNA is again being modified as shown in Figure 35 below. In this simulation, an ideal capacitor C_d is being implemented in parallel with a real inductor L_d , which is obtained from the experimentally verified process design kit (PDK) provided by Global Foundries (GF) for the 0.18 μ m RFCMOS process.

Figure 35: RFLNA with Ideal Variable Capacitor

Again, the ideal capacitor is being varied and the simulation results are shown in Figure 36 and 37 below. Figure 36 shows the various S_{21} of the LNA where the capacitor values are being increased from 0fF to 2pF in 200fF steps. The resonance frequency ranges is also sufficiently wide with these practical capacitor values, just like the first simulation results. Similarly, in Figure 37, the corresponding S_{11} of the LNA peaks at the respective resonance frequencies of the output load.

Figure 36: S21 of Different Capacitor Load

Figure 37: S11 of Different Capacitor Load

In both simulations, all the components, except for the ideal inductor and capacitor, are obtained from the PDK library for the GF 0.18 μ m RFCMOS process. Also, to simplified the illustration and for fast comparing the effects of the different implementation of the LC tuning load, all the other components and simulating conditions are kept constant.

Although ideal load components are used in the simulations, the results can still reflect the improved performances of using LC load in the RFLNA topology for narrowband designs. This is because the use of ideal inductor includes a modeled series parasitic resistor that helps to better represent a real inductor. And in the case of using ideal capacitor, real capacitors usually have much better Q factors and hence their parasitic

resistance effect is normally not significant. Thus similar results are can be expected when all real components are simulated. Acknowledging the obvious trade-offs of the much smaller operating bandwidth, the LC load helps in improving the gain of the RFLNA, which has the benefit of further minimizing the noise contributed by the feedback resistor.

Other than proving the effectiveness of using LC load in the RFLNA topology, the simulation also shows the difference in using either tuning inductance or tuning capacitance. The use of larger inductance not only increases the gain of the LNA, it also increases its gain bandwidth. Whereas the use of larger capacitance not only causes a decrease in the gain of the LNA, it also decreases its gain bandwidth.

Although this is actually the result of the change in the Q value of the output network, it is still a point of concern to the proposed FLNA design. The use of tunable inductance and tunable capacitance will lead to the proposed FLNA having different performance at different bands. Such limitations will greatly affect the attractiveness of the proposed designs. Fortunately, there are suitable methods to overcome these performance variations. For example, adaptive bias [22, 23] can be employed through adaptive change to the bias gate voltage of the input transistor. Other techniques like switching cascode transistors [16, 25] and output resistance [19, 24] as discussed in the earlier sections are also possible ways to overcome the performance variations across the different bands. However, most of the methods are not implemented in the proposed FLNA which focuses on achieving flexible operating frequency bands.

Moreover, it is interesting to note that the ability to provide variable performance at the different frequency bands is one of the desired feature of a truly FLNA and therefore the concern on the variation on the performance will cease once a truly FLNA is being achieved.

Based on these simple simulations, narrowband LNAs based on resistive feedback with tuned LC load are shown to be able to achieve relatively good performances in the low-GHz range. This shows the promise of designing a flexible narrowband LNA. However, the illustrations also show the main challenge to design such a FLNA, which is largely due to the difficulties in implementing the required tunable, wide range resonating LC load in CMOS technology. Firstly, passive high-Q inductors are already a limitation in full integrated designs, let alone to realize a tunable one. Next, although varactors are readily available, they have limited tuning range. Even with the availability of wide range varactor, the reduction in the gain and bandwidth of the FLNA when using a larger capacitance still restricts the performance of the FLNA.

Figure 38: Implemented Switchable LC Load Design

As a result, a resonating LC load is being implemented through the use of switchable inductors in parallel with switchable capacitors to achieve the required wide range of resonance frequencies. The actual design of the LC load is shown in Figure 38 above.

This design technique is similar to the earlier discussed design technique that involves the switching of the passive components [19, 24]. However, due to the use of resistive feedback, both the input matching frequencies and the output peak gain frequencies are being tuned at the same time through the switchable LC load of the FLNA. This has the benefit of better noise performance as the use of switches is now solely at the output node where there is already sufficient gain to the input signal, making the load component's noise contribution less significant [34].

Notice in Figure 38, binary weighted capacitors are implemented to reduce the number of switches needed. In general, more switches will provide finer tuning steps but the switches' 'ON' resistance and parasitic capacitance can limit the FLNA's performance. Also, the number of switchable capacitors needs to be kept low so that reduction in the gain and bandwidth of the FLNA caused by the use of large capacitance can be minimized. Therefore, to overcome the limited range of the capacitance available, a switchable inductor will be needed to further increase the tuning range of the FLNA. Moreover, the use of switchable inductors can improve the gain and bandwidth of the FLNA, which helps to overcome the effect of using large capacitance.

The design of the individual switches is also another important component in the LC load. Larger switch will provide smaller ‘ON’ resistance that improves the Q factor of the load. However, large switches also come with large parasitic capacitance that affects the tuning range of the FLNA. In the design of the switches used for the capacitors, the size of the switch is reduced when possible to improve the tuning range of the FLNA.

The implementation of the LC load also has other benefits as compared to the conventional RFLNA, where higher peak gain is possible with the use of the relatively high-Q inductors. Better linearity is also possible due to the removal of the voltage headroom required for R_d , which may also allow for low voltage operation.

However, the design technique has its drawbacks. The need of the relatively high-Q inductors demands a large chip area, which is costly. On top of that, the use of inductors and capacitors together to provide the required resonance frequencies makes the tuning range of the FLNA very sensitive to process variation, especially at higher frequencies, where a slight change in the component value can cause a big shift in the resonance frequencies.

5.3.3 Improvement to the Proposed FLNA

To complete the discussion of the proposed FLNA shown in Figure 30, the purpose of the gate inductor (L_g) used in the proposed FLNA is presented here. Due to the narrowband characteristic of the proposed FLNA, the addition of a small L_g would not

alter the input matching frequencies much. However, though small, L_g can still help to improve the performance of the FLNA [35].

The use of L_g provides a passive voltage gain at the input matching network of the FLNA, similar to that of the L-CSLNA. This helps to lower the noise and increase the gain of the LNA. However, unlike in [35], where a large L_g is used to achieve resonance with the input capacitance C_{gs} for matching, L_g is kept small in the proposed design. This is done so that together with the small C_{gs} , their resonance frequencies are pushed further to the higher frequencies range to minimize their effect on the input matching of the proposed FLNA.

Figure 39: Noise Figure of Different L_g

Figure 39 above shows the noise figure (NF) of the FLNA with and without L_g . A slight improvement (0.1dB) in the NF is seen when L_g is used. This minimum increase in the NF of the FLNA is due to the noise of the L_g that is added to the input of the FLNA. As the NF of the FLNA is already quite low in this design, even a small noise from L_g becomes significant. Therefore, to better demonstrate the benefit of L_g , the FLNA is being re-biased to operate at lower power consumption where its NF is now substantially higher at more than 4dB and better improvement in the NF of the FLNA can be seen (0.5dB). In this illustration, the L_g used is only about 1nH at the operating frequency.

Figure 40: S21 of Different L_g

Figure 40 shows the peak gain of the LNA of the various conditions of L_g use. However, in this case the improvement of using L_g is not as significant. This can be partly due to the large drop in the current consumption used in this illustration that uses the same R_f . As g_m is smaller, the R_{eff} is larger and hence the gain across C_{gs} is smaller.

Also, there is another side effect to the use of L_g , which is the potential change in the noise circles of the proposed FLNA, as L_g can be seen as a matching network in between the source impedance and the RFLNA. Although the use of small L_g should have minimum effect on the input matching of the FLNA, its noise circles are simulated and shown in Figure 41 below to prove it also causes minimum changes to its noise circles.

Figure 41: Noise Circles of Different Lg

The effect of adding Lg on the noise circles is shown to be insignificant as can be seen from the above simulated noise circles. The noise figure of both scenarios is not at Fmin but well below 2.5dB which is good enough for many applications. This is largely due to the small Lg used and the small Rn of the proposed FLNA that help in reducing the increase in the noise figure when there is noise mis-matches.

Although it seems that the minimum improvement in the NF due to L_g will not justify its large area used, it is still implemented in this design to show the benefit of a flexible narrowband design as oppose to a wideband design. Without having to be restricted by the need to achieve flat performance across wide frequencies, possible design techniques that can only provide narrowband improvements can be readily implemented.

Furthermore, it is preferred that L_g is added into the FLNA as bondwire, which is easily possible because the inductor is added in series to the input of the FLNA. The use of bondwire reduces its noise contribution and helps to save on chip area.

5.4 Implementation and Simulation Results of Proposed Flexible Low-Noise Amplifier

Before the implementation of the proposed FLNA, it is important to identify the desired performance of such a FLNA. Other than achieving the aim of flexibility, the proposed FLNA should be feasible in real life application and thus be able to meet the performance requirement of the different wireless standards available. Based on the earlier literature survey, it is summarized that a multi-standard LNA should be able to operate from 2.4GHz to 5.8GHz while achieving a noise figure of less than 3dB. The gain is usually more than 15dB while having an acceptable IIP3 of at least -10dBm at a current consumption of 10mA for reasonable battery life. These requirements, if achieved, should qualify the FLNA suitable for real life multi-standard applications. These requirements are summaries in Table 3 below.

Table 3: Summary of Proposed FLNA Design Requirements

Frequency	2.4GHz to 5.8GHz
S11	less than -10dB
S21	more than 15dB
Noise Figure	less than 3dB
IIP3	better than -10dBm
Current Consumption	less than 10mA

However, there is a need to note that such requirements should be seen as the “worst case” performance as discussed in Chapter 4. If possible, both the noise figure and gain of the FLNA should be able to be trade-off with power. The IIP3 of the FLNA, usually not the critical requirement in LNA design, should not worsen when the FLNA changes its operating frequency band.

5.4.1 Implementation of Proposed Flexible Low-Noise Amplifier

The implementation of the proposed FLNA including the bias circuit and the output buffer used for testing purpose is shown in Figure 42 below. The proposed FLNA is designed using the GF 0.18 μ m RFCMOS technology. Transistor M1 and M2 forms the cascode amplifying stage of the FLNA. Two inductors (L_{d1} and L_{d2}) and three capacitors (C_d , $2C_d$ and $4C_d$) forms the switchable LC load. They are switched by the transistors MS1 to MS4. The FLNA is being biased by the current mirror involving M3 and R_{ref} . Blocking capacitors C_{b1} to C_{b3} and C_f are used to block DC current flow but allows the RF signal flow, thus their values are chosen to be 4pF in the FLNA design. The output buffer is added for testing purpose, which can be totally removed in fully integrated designs.

Figure 42: Captured Schematic of Proposed Flexible Low-Noise Amplifier Design

The designed component values are listed together in Table 4 below. They are obtained after some fine tuning on the hand calculated values. Following the basic steps in design a RFLNA in [32], the size of the input transistor M1 is first determined in the calculation. As the proposed design fails to minimize the effect of C_{gs} of M1, the size of M1 will need to be first calculated based on the largest possible C_{gs} that will not affect the input matching of the FLNA at a pre-determined frequency. After which, the width of M2 is set at half of M1 so that its parasitic capacitance can be minimized. Next, by using a suitable current of 5mA, the transconductance of M1 can be

calculated. Finally, careful design and optimization of the switchable LC loads and R_f are done to achieve a suitable operating frequency range and tuning step.

Table 4: Designed Component Values of the Proposed FLNA

Component	Values
M1	320 μ m
M2	160 μ m
L_{d1} & L_{d2}	2nH @ 2.45GHz
L_g	0.98nH @ 2.45GHz
R_f	800 Ω
C_d	100fF
MS1	30 μ m
MS2	60 μ m
MS3	120 μ m
MS4	300 μ m
C_{b1} , C_{b2} , C_{b3} , C_f	4pF
Mbuffer	80 μ m
Rbuffer	300 Ω
R_{ref}	2000 Ω
M3	36 μ m
R_b & R_{bias}	10K Ω

5.4.2 Simulation Results

Based on the designed component values, the proposed FLNA is able to achieve a wide operating frequency range though the different configurations of the switches. As four such switches are used, the FLNA will therefore have 16 different operating frequencies, which range from about 2.4GHz to 5.8GHz. For simplicity of future explanation, the configuration of the switch MS4 to MS1 will be represented by a 4-bit number such that the first digit will represent the value of inductance and the last 3 digits will represent the value of capacitance. For example, 1111 will means the use of

4nH and 700fF load while 0000 will mean the use of 2nH and 0fF load. The simulated performances of the proposed FLNA are shown in Figure 43 to 45. For clearer representation, only the results of four configurations are shown, namely, the 1111, 1000, 0111 and 0000 switching configurations.

Figure 43 shows the various voltage gain (S_{21}) of the FLNA at the four switching configurations. The S_{21} of the designed FLNA varies from about 13dB to 19dB. Trends on the effect of using variable inductance and capacitance are observed in the simulation results. The S_{21} of the FLNA reduced from 16.6dB to 13.7dB when the operating frequency of the FLNA reduced from 5.8GHz to 3.7GHz. This is due to the use of increasing capacitance in the LC load to reduce its resonance frequency. Therefore, a jump in the S_{21} of the FLNA to 19dB is observed when the FLNA is switched to operate in 3.3GHz such that at this frequency, the capacitors are being opened and the second inductor is being switched on. Due to this jump, the 3.7GHz to 5.8GHz operating range of the FLNA is recognized as the High Band (but lower gain) while the 2.4GHz to the 3.3GHz operating range of the FLNA is term the Low Band (but higher gain). This issue of the performance change in the tuning step of the FLNA may suggests that the FLNA cannot be used for application in the 3.3GHz to the 3.7GHz bands. However, as these values are taken at the peak frequencies, the 3dB bandwidths of the designed FLNA would mean that this unusable range is actually much smaller than it seems.

Figure 43: S21 of Proposed FLNA

Figure 44 shows the various input matching (S_{11}) of the FLNA at the corresponding peak S21 of the FLNA shown earlier. The S_{11} is better than -10dB at the respective peak S21 of the FLNA, which is the standard minimum requirement. In fact, the S_{11} is better than -10dB for almost the entire frequency range from 2.4GHz to 5.8GHz except for a very small band (marked by 'O' in Figure 44) that is in between the Low Band and High Band of the FLNA. Even at this small band, the S_{11} is still better than -9dB.

In fact, the S_{11} of the proposed FLNA will be better than -10dB as long as the gain of the FLNA is larger than a certain value determined by the value of the feedback resistor used. This is a direct result from equation (38) and the main benefit of using the RFLNA topology. This will also means that the design can have the potential of noise

figure tuning by changing the bias of the FLNA. The current consumption of the FLNA can be lowered to save power in the event when higher noise figure is acceptable as briefly seen in Figure 40. This is of course, only applicable when the gain of the FLNA is still maintained at above the minimum required value for matching. The same case can be also possible by the use of switchable parallel resistors at the load for tuning gain. However, both are not implemented in this design and not pursue further.

Figure 44: S11 of Proposed FLNA

Next, the noise figure of the proposed FLNA is shown in Figure 45 below. One interesting result is that the minimum noise figure of the FLNA also occurs at the peak S21 of the FLNA at the corresponding operating frequency, unlike in wideband designs where the NF normally increases at higher frequencies. This happens due to the use of

most switching elements at the output node of the FLNA. At the output node, the input signal is now much larger and hence the noise contributed by the switching elements becomes relatively small and less significant. The noise contributors at the input node are therefore same at all the operating frequencies which then sets the minimum noise figures of the FLNA. This result further justifies the effort of implementing flexible narrowband designs than wideband designs.

Figure 45: NF of Proposed FLNA

Finally, the linearity and stability of the FLNA is simulated to complete the characterization of the FLNA. The linearity of the FLNA is represented by the simulated IIP3 of the FLNA. It is simulated using a test tone of 10MHz off the fundamental tone, which is set at the middle of both the High Band and Low Band.

Therefore only two sets of IIP3 values are obtained and shown in in Figures 46 and 47 below. The IIP3 of the FLNA is simulated together with the buffer stage. This is because in the event where the FLNA is fabricated and measured, the buffer will be needed and there is actually no perfect way to fully de-embed its effect on the linearity of the FLNA. In fact, all the previous results are simulated together with the buffer stage, which is usually not needed in fully integrated front-ends. Though in these other parameters where the de-embed values of the FLNA are more reliable, they are not done so that the simulated result of the FLNA in this design can better compare with the State-of-the-Art FLNAs that has experimental results.

Figure 46: IIP3 of Low Band

Figure 47: IIP3 of High Band

The stability of the FLNA is simulated using the k_f and $B1_f$ factors, which are provided by the simulator to represent stability. For unconditional stability, k_f needs to be more than 1 and $B1_f$ more than zero simultaneously. The stability of the FLNA is well satisfied in the simulation. All the stability factors of the different configuration are listed in table 5 below.

Table 5: Stability Factors of FLNA

Configuration	Frequency (GHz)	K_f	$B1_f$
1111	2.4	9.14	0.912
1000	3.3	5.27	0.936
0111	3.7	14.96	1.022
0000	5.8	5.37	0.948

In summary, the designed FLNA achieves operating frequencies from 2.4GHz to 3.3GHz (Low Band) and 3.7GHz to 5.8GHz (High Band) with adequate gain and noise figure while using 7.2mA of current. The achieved range of the FLNA is specifically designed to cover the range from 2.4GHz to 5.8GHz that consist of the different ISM bands. Including the 3dB bandwidth of the designed FLNA, this range can be from 2GHz to 6GHz, a range widely acceptable as the range required for multi-standard radios. The operating frequency range is also achieved in a total of 8 steps in the individual bands. Simulated results at both bands are summarized in Table 6 together with the State-of-the-Art FLNAs.

Table 6: Performance Summary of Proposed FLNA

Paper	Frequency (GHz)	NF (dB)	S21 (dB)	S11 (dB)	IIP3 (dBm)	Power (mW)	Vdd (V)	Process
Proposed	2.4 – 3.3	2.1 – 2.2	18.0 – 19.1	-18	-13.3	13	1.8	180nm
	3.7 – 5.8	2.2 – 2.4	13.7 – 16.6	-10	-10.3	13		
[17]	2.7	1.97	9.13	-11	2.2	7.5	1.2	130nm
	3.5	1.55	10	-11	3.2	7.5		
	5.55	1.86	10	-13	1.43	7.5		
[18]	0.95	2.6	24.9	NA	-21.55	9.04	1	180nm
	2.14	3.96	23.3		-6.27	9.04		
[19]	1.8	1.75	14.54	-11.52	-5.8	7.5	1.5	130nm
	2.14	1.97	16.6	-15.18	-5.3	7.5		
[20]	2.4 – 5.2	2 – 4.2	19 – 23	-13	-3	17	1.2	130nm
[22]	2.4	2.9	10.1	-10.1	4	11.7	1.8	180nm
	5.2	3.7	10.9	-11	-5	5.7		
[23]	2.5 – 5.4	2.16 – 2.81	15.2 – 17.0	-20.5	-3.9 – 0.5	3.6 – 24.3	1.2	90nm
[24]	0.9	2.3	14	-12	-14	7.5	1.8	180nm
	1.8	2.9	13	-14	-14	7.5		
	5.2	2.6	16	-15	-14	7.5		

From the table, only [20] and [23] achieved flexible operating frequencies covering wide range from 2GHz to 6GHz. In the case of [20], tuning is achieved by the tuning of input gate inductor through active components. As such, at higher frequencies where the size of the gate inductor is small, its noise degrades to be more than 4dB. In [23], the use of changing input transistor will means larger current use for larger transistor

size. Both designs unlike the case of the proposed FLNA can adjust its current consumption while still maintaining suitable gain and matching.

5.4.3 Post Layout Simulation

To further verify the feasibility of the proposed FLNA, a layout of the designed FLNA has been done so as to extract the effect of the parasitic. For simple implementation, the bias circuit to the FLNA has been taken off-chip and replaced with an input bias pin as shown in Figure 48 below. This is to allow for easy change in bias point of the FLNA through external supply and to save the effort to design a complicated adaptive bias circuit on-chip. The output buffer, on the other hand, will still be included as it will still be necessary to act as the FLNA's output stage load and also for measurement purpose.

Figure 48: Modified Schematic of Proposed Flexible Low-Noise Amplifier for Layout

The layout is shown in Figure 49 below. To save the area of the layout, the three large inductors are placed in an L-shape so that they take up roughly three quarter of the area and the last quarter can be used for the other components. Due to the use of many pins, the inductors are slightly spaced apart to allow for additional pins. The total layout area of the proposed FLNA is $0.7 \times 0.7 \text{ mm}^2$.

Figure 49: Layout of Proposed Flexible Low-Noise Amplifier

During the layout drawing, post-layout simulations are done with the parasitic. To optimize the performance of the FLNA with the parasitic, certain component values are slightly changed from the original designed. The final component values are listed in Table 7 below.

Table 7: Designed and Layout Values of Proposed FLNA

Component	Design Values	Layout Values
M1	320 μ m	360 μ m
M2	160 μ m	120 μ m
L _{d1} & L _{d2}	2nH @ 2.45GHz	1.6nH @ 2.45GHz
L _g	0.98nH @ 2.45GHz	0.98nH @ 2.45GHz
R _f	800 Ω	700 Ω
C _d	100fF	100fF
MS1	30 μ m	20 μ m
MS2	60 μ m	40 μ m
MS3	120 μ m	80 μ m
MS4	300 μ m	540 μ m
C _{b1} , C _{b3}	4pF	2.4pF
C _{b2} , C _f	4pF	0.8pF
Mbuffer	80 μ m	80 μ m
Rbuffer	300 Ω	300 Ω
R _{ref}	2000 Ω	NA (external)
M3	36 μ m	NA (external)
R _b & R _{bias}	10K Ω	10K Ω

Based on the layout, post-layout simulations results are shown in Figures 50 to 52. Again, for clearer representation, only results for the 1111, 1000, 0111 and 0000 configurations are shown.

Figure 50: Post-Layout S21 Results of Proposed FLNA

The S21 of the proposed FLNA has dropped from 13dB to 19dB to 11dB to 15dB in the post layout simulation result. This is due to the decrease in the size of the inductors used to compensate for the parasitic capacitance so as to ensure that the resonance frequencies of the FLNA remain at the same band of 2.4GHz to 5.8GHz. Although the gain of the FLNA is smaller, it is still comparable to other flexible FLNAs that usually achieve a S21 of about 10 to 15dB.

Figure 51: Post-Layout of S11 Result of Proposed FLNA

Figure 51 shows that the input matching of the FLNA is maintained at above -8.1dB as compared to the -9dB in the pre-layout results. This is again due to the decrease in the gain of the FLNA so that the input effective resistance becomes too large to achieve a better input matching.

Figure 52: Post-Layout NF Result of Proposed FLNA

Next, Figure 52 shows the noise figure of the proposed FLNA. Again, due to the decrease in the gain of the FLNA, the noise figure degrades from 2.1-2.4dB to 2.4-2.7dB. This is again still acceptable as compared to the results of other FLNAs and considering the possible application of FLNA.

The simulation result shown from Figures 50 to 52 is expected as the additional parasitic capacitance that exists after the layout is drawn is bound to affect the operating frequency range of the FLNA. This will then subsequently affect gain and the noise figure of the FLNA. This is clearly seen in the above post-layout simulation results. Nonetheless, the results still support the feasibility of the proposed FLNA. The

concept of the proposed FLNA will still work and can be fine tuned to meet the same frequency bands, though with a slightly inferior “worst case” performance.

Chapter 6 – Conclusion and Future Plans

6.1 Conclusion

The main focus of this research is to study the approach to implement flexibility in the wireless receiver front-ends for the multi-standard radios. The direction to achieve flexibility lies in the utilization of the progress in CMOS technology that allows full integration of the receiver front-end through the use of direct conversion architectures that removes the need to have power matching. The CMOS technology further provides cheap implementation of powerful digital signal processing and relative good switches that fully supports the idea of digitally-assisted receiver systems and is further utilized in this research.

To expand the idea of flexible wireless receivers, the inherent benefits and possible issues of using a flexible receiver front-end solution for multi-standard radios are briefly discussed in this report. The term “flexible” is being used with reference to several past publications so as to provide a universal term for ease of summarizing the different published flexible designs. To complete the discussion on the idea of flexibility, new design strategy and characterization parameters that are only suitable for flexible designs are proposed.

To further explore the feasibility of flexible designs, a review of the different FLNA is done. Subsequently, a FLNA with flexible operating frequencies is being designed with adequate performance. The designed FLNA achieve operating frequencies ranging from 2.4GHz to 5.8GHz with adequate performances while consuming acceptable

power. The FLNA is based on the resistive feedback topology that shows high potential for flexibility. A switchable output resonance load implemented by using switched inductors and capacitors in parallel are used to provide the wide range of operating frequencies of the FLNA.

6.2 Future Plans

Although a FLNA with flexible operating frequencies are achieved in the current design, more work is still needed to realize the idea of an ideal FLNA and subsequently flexible receiver.

The implementation of the resonance load using switched inductors and capacitors are prone to process variations. The need for larger inductance and capacitance and the presence of significant parasitic capacitance limits the range of operating frequencies. An alternative using active inductance and capacitance which may help to improve the performance of the proposed FLNA can be analyzed in the future. Ideas in [20] that use a real inductor with active circuit techniques to achieve variable inductance is also another possible alternative to achieve better performance of the FLNA.

Other than operating frequencies, flexibility in the other parameters of the LNA is also needed for a truly FLNA design. Briefly suggested through modifying the bias conditions and addition switchable resistor in the earlier sections can be pursued further to achieve a FLNA with flexible gain and noise figure in addition to the designed flexible operating frequencies. This will possible complete the solution in achieving the complete solution of a truly FLNA.

Finally, similar techniques can also be implemented to the other building blocks of the receiver front-end for a flexible receiver design and further system analysis might also be useful in selecting the parameters that needs to be made flexible.

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