3D electromigration modeling at the circuit layout level

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NANYANG TECHNOLOGICAL UNIVERSITY

**3D ELECTROMIGRATION MODELING
AT THE CIRCUIT LAYOUT LEVEL**

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ABSTRACT

Integrated circuit (IC) reliability is of increasing concern in present-day IC technology where the interconnect failures significantly increases the failure rate for ICs with decreasing interconnect dimension and increasing number of interconnect levels. Electromigration (EM) in the interconnects has now become the dominant failure mechanism that determines the circuit reliability.

To model the EM reliability of the interconnects in ICs, a 3-dimensional (3D) electro-thermo-structural model as opposed to the conventional current density based 2-dimensional (2D) models is now necessary because ICs are 3D in their actual physical implementation. In this work, we study the EM reliability of the interconnects in ICs using a 3D finite element circuit model. A simplified circuit structure with only the intra-block interconnects is used as an example to show the construction of a 3D finite element model from its 2D IC layout. This modeling method is then used in the analysis of a realistic circuit structure with the inclusion of both intra- and inter-block interconnects.

Transient electro-thermo-structural simulations are carried out using both Cadence (a circuit simulator) and ANSYS (a finite element tool). By limiting our study only to EM failure, the current density, temperature and thermo-mechanical stress

distributions of the interconnects are computed by considering the heat transfer and Joule heating, and these values are used to compute the atomic flux divergences (AFDs). As the failure time of the interconnects is inversely proportional to its AFD and void nucleates at the location with highest AFD, the EM lifetime and the EM weak spot of the interconnects can be determined from the value and the location of the maximum AFD respectively.

The transient temperature changes with the applied electrical loads and the transient thermo-mechanical stress changes with the circuit temperature demonstrated the transient modeling capability of the model at the circuit layout level, and this is an improvement to the conventional 3D EM models at the test structure level.

From our simulation results, it is found that at the circuit operation temperature of 90 °C, the location of the maximum AFD is determined by the product of the temperature gradient and the thermo-mechanical stress gradient; while at the EM test temperature of 300 °C, the location of the maximum AFD is determined by the current density.

From the simulations performed using different structures, it is observed that the line-via test structure showed the same maximum AFD location as the circuit structure at 300 °C (i.e. at the location with the highest current density). However,

due to the incompleteness in the test structure, the temperature gradient distribution and hence the maximum total AFD location of the line-via test structure are different from the circuit structure at 90 °C. The change in the maximum AFD location may cause a wrong interpretation of the EM weak spot location when the test structure is used for data extrapolation in predicting the EM reliability of the entire circuit.

From the simulation performed based on a realistic circuit layout (i.e. a low noise amplifier circuit), it is found that the regions with high thermo-mechanical stress gradient can have comparably high AFD values as the regions with high current density and/or high temperature gradient. Ignoring or overlooking this thermo-mechanical stress effects may cause the simulator to miss out some locations with high possibility of EM failures. This again proves the inadequacy of the conventional current density based EM simulators.

Modifications to the interconnect structures, surrounding materials, circuit layout and process are carried out based on the EM weak spots identified. The improvements in the EM lifetime for the modified models are as expected and agree with the reported experimental results in literature. This provides validation to the proposed model.

Due to the complexity of the model and the constraint in computation memory, the microstructure and back stress effects are not included in the current model. These effects will be considered in our future work.

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LIST OF SYMBOLS

ΔD_{it}	the interface damage
I_s	the substrate current
I_w	the well current
β_{pnp}	the common-emitter current gains for the <i>pnp</i> transistor
β_{npn}	the common-emitter current gains for the <i>npn</i> transistor
F_{wind}	the wind force
F_w	the electron wind force
F_d	the direct force
F_{net}	the net force
n_e	the electron density
n_d	the defect density
e	the electron charge
τ_i	the mean time between two successive collisions between the electrons and the defects
ρ	the resistivity of the conductor, which depends on temperature as $\rho = \rho_0(1 + \alpha(T - T_0))$
α	the temperature coefficient of resistivity
ρ_0	the electrical resistivity at temperature T_0
ρ_d	the resistivity contribution from the defects in the metallization
E	the electric field

λ	the mean free path, which is the average distance a molecule travels between collisions
σ_i	the cross-section for collision between the electrons and the conducting atoms
j	the current density
a	the factor accounting for the migration effects of the conducting atom ($a \ll 1$)
Z	the actual valence of the conducting atom
Z_w	the effective valence for the electron wind force
Z_d	the effective valence for the direct force
Z_{eff}^*	the effective valence for the net force
t_{50}	the median time to failure
A	a constant which contains a factor involving the cross-sectional area of the metal line
E_a	the activation energy
k_B	the Boltzman's constant
T	the temperature of the metal line
$(jL)_c$	the critical product for EM failure
Ω'	the atomic volume
W	the metal line width
L	the metal line length
σ_{th}	the maximum stress the metal line can withstand

σ_0	the stress at $x = 0$
C_v	the instantaneous vacancy concentration at position x and time t
C_{ve}	the equilibrium concentration of the vacancies within the grain
γ	the sink/source term which allows for the recombination or generation of vacancies at the grain boundaries, the dislocations, or the surfaces
τ_v	the average lifetime of a vacancy at the grain boundary
D_v	the diffusivity of the vacancy given by $D_v = D_0 \exp\left(-\frac{\Delta E_a}{k_B T}\right)$
D_0	the prefactor of the self-diffusion coefficient
D	the diffusivity of the metal atoms
eZ^*	the effective charge of the diffusing species
v_d	the EM drift velocity
$N(r, t)$	the normalized atomic concentration at location r and time t
N	the atomic concentration
N_0	the initial atomic concentration
J_v	the vacancy flux
J	the total atomic flux
J_N	the atomic flux due to the concentration gradient of the metal atoms
J_{EWF}	the atomic flux due to electron wind force
J_T	the atomic flux due to temperature gradient induced driving force
J_S	the atomic flux due to thermo-mechanical stress gradient induced driving force
$\nabla \cdot J$	the total atomic flux divergence

Q^*	the heat of transport of the metal line
σ_H	the local hydrostatic stress
∇N	the concentration gradient of the metal atoms
∇T	the temperature gradient along the metal line
$\nabla \sigma_H$	the stress gradient along the metal line
ΔN	the number of atoms accumulated in a small interconnect segment of length Δl for a time period of Δt due to the presence of the atomic flux divergence $\nabla \cdot J$
p_w	the effective diffusion path width
p_t	the effective diffusion path thickness
V_c	the critical volume of mass depletion or accumulation required for failure to occur
t_f	the time-to-failure
E'	the Young's Modulus of the metal line
α'	the thermal expansion coefficient, CTE, of the metal line
ν	the Poisson ratio of the metal line
$\nabla \cdot J_{EWF}$	the atomic flux divergence due to electron wind force, AFD_EWF
$\nabla \cdot J_T$	the atomic flux divergence due to temperature gradient induced driving force, AFD_T
$\nabla \cdot J_S$	the atomic flux divergence due to thermo-mechanical stress gradient induced driving force, AFD_S
h	the convection heat transfer coefficient

V_{dd}	the supply voltage
V_{in}	the input voltage
V_{out}	the output voltage
V_{bias}	the bias voltage
I_{ps}	the current flow from the V_{dd} line to the source of PMOS
I_{pd}	the current flow from the drain of PMOS to the output line
I_{nd}	the current flow from the output line to the drain of NMOS
I_{ns}	the current flow from the source of NMOS to the ground
δ	the skin depth
ω	the angular frequency of current ($2\pi \times$ frequency)
μ	the absolute magnetic permeability of the conductor
V_t	the threshold voltage of the transistor
W_t	the width of the transistor
I_{out}	the output current

CHAPTER 1 INTRODUCTION

1.1 Motivation

With the continuous increasing circuit complexity and the down scaling of the minimum feature size in ICs, the electromigration (EM) reliability of the circuit is becoming increasingly important. As re-design and re-manufacture are very time and resource consuming for present-day Ultra-Large Scale Integration (ULSI), “Design-for-Reliability” is essential.

Reliability of an IC depends on the reliability of the embedded circuit elements, including the transistors and the interconnects. The interconnect dimension scales about 30% with each advancing technology node, and this causes an approximate 1.5 times increase in the maximum current density and an increase in the ratio of the Cu/cap interface (i.e. the interface between the Cu interconnects and the cap layers, which is the fast Cu diffusion path) to the total Cu volume [1]. In present-day ICs of nanometer scale, the interconnect reliability has become the main factor that determines the circuit reliability [2], and the failures in the interconnects are mainly due to EM. The study by Srinivasan *et al.* [2] showed that the failure rate of a processor using the 65 nm process is more than 3 times higher than that using the 0.18 μm process, and the main cause of failure was EM. It is because the circuits with a narrower interconnects tend to have a higher current density and are more

sensitive to the increase in the interconnect line resistances, especially when the circuits are operating at higher frequencies. Therefore they are expected to have a shorter time to failure and a higher failure rate. Furthermore, although the use of the low- κ dielectric can help reducing the parasitic capacitance and thus enabling faster switching speeds, the poor thermal conductance of the low- κ materials aggravates the EM deterioration [3]. EM turns out to be the most dominant failure mechanism in a high density ICs with a highly scaled interconnect dimension [4]. Therefore, it is important to ensure that the circuit has a long EM lifetime if the reliability of an IC is to be improved.

Electromigration is the gradual displacement of metal atoms in a metal line when the current density is high enough (above 10^5 A/cm^2) to cause the drift of the metal atoms in the direction of the electron flow [5]. The number of atoms passing through a specific cross sectional area in a unit of time is called the atomic flux [6]. The difference between the atomic flux into and out of a volume element per unit time is the atomic flux divergence (AFD) and it is the main cause for EM failures in the metal line [7]. Voids or hillocks form when the number of atoms arrives in a volume element is different from the number of atoms be carried away (i.e. when there is a non-zero flux divergence). The formation of the voids and the hillocks may cause open circuit or short circuit and hence results in serious reliability problem.

The rate of the atomic flow depends on the magnitude of the force that tend to hold the atoms in place and the force that tend to displace them [5].

The factors that affect the “holding” force include the nature of the metal, the grain size and its orientation, the interface and the grain boundary. These factors are mainly the physical properties of the metal line [5]. The “holding” force is larger in a metal line with a higher activation energy, a lower resistivity, a smaller number of diffusion interfaces, and less amount of grain size variation [7]. A large “holding” force is favorable in the EM lifetime improvement as the metal atoms are more resistant to the atomic flow.

The factors that affect the “dislodging” force include current density, temperature, and thermo-mechanical stress [5]. High current density can greatly accelerate the EM degradation by displacing more metal atoms at a faster rate [7]. When the current flows through a metal line, heat is released due to the interactions between the moving electrons and the metal atoms. As a result, the metal line temperature increases and this phenomenon is known as Joule heating [8]. The rise in temperature not only increases the rate of the atomic flow but also causes a non-uniform temperature distribution, especially in long metal lines with complex structure and/or material inhomogeneity [4]. The non-uniformity in temperature can result in temperature gradients in the metal line. These temperature gradients render the metal atoms to flow from the high temperature region to the low

temperature region [7]. The temperature gradients also induce thermo-mechanical stress due to the thermal mismatch between the metallization and its surrounding materials. The magnitude of the thermo-mechanical stress is affected by the surrounding materials and the stress free temperature of the metallization (i.e. the temperature at which the stress in the metal line is zero, usually taken as the final annealing temperature of the metallization) [7]. The metal atoms move along the metal line in order to relax the thermo-mechanical stress and this movement is faster when the stress gradient is higher.

As all of the above mentioned factors affect the EM process in the interconnects, it is important to include all of them when performing the EM modeling of the interconnects.

Simple line or line-via test structure 3D modeling is a common practice in EM modeling in the semiconductor industry. The 3D physics based EM models [9-12] have the advantages of including all the above mentioned factors. These models can predict the EM lifetime and failure sites of the interconnects [9-11], simulate the void nucleation and growth process [12], and evaluate the back stress, microstructure and material effects [12]. However, as will be discussed in the latter sections, the EM weak spots are different under different temperature, and for different interconnect structures. Furthermore, the effect of the substrate area is overlooked if only the “localized” region (i.e. only part of the circuit structure) is

considered. The model based on the simple line or line-via test structure may therefore not always be able to predict the correct EM failure sites and is not a suitable choice if we want to study the EM reliability of the entire circuit under the circuit operation condition. When looking at the EM reliability of a circuit, the entire interconnect structures must be considered as a part of a system that includes the package and the Si substrate. This drives the need for 3D EM modeling at the circuit layout level.

Many circuit layout level EM simulators had been reported in literature, and all of them are 2D. The traditional 2D circuit simulators [13-16] assumed a constant temperature across the surface of the chip. This assumption is no longer valid at the 90 nm technology node. In high density circuits with multiple metal layers, the temperature difference at different portions of the chip may vary by 50 °C or more and that between the top-most and the lowest layer of the metallization can be larger than 45 °C [17]. The temperature effects can significantly affect both the performance (e.g. timing, power consumption, noise) and the reliability (e.g. lifetime, failure rate) of an IC [17].

As explained earlier, the rate of the atomic flow is faster at a higher temperature. Furthermore, the material degradation rates of both the metallization and its surrounding layers are faster when the temperature is higher [18]. Therefore, the temperature effects cannot be ignored and the later EM simulators [19-22] took

these effects into consideration. However, due to the limitation in dimensionality (only 2D), these simulators were unable to correctly represent the true temperature profile of the circuit as the heat dissipation of an IC depended on its actual 3D structures [17]. It is important to include the full 3D temperature profile of the circuit into the simulation tools so as to correctly assess the thermal impacts on the chip [17]. Hence a 3D circuit model for an IC is needed as its actual physical implementation in a wafer is indeed 3D in nature.

Also, all the 2D circuit simulators ignored the thermo-mechanical stress effects. The work by Li *et al.* [23] showed that the thermo-mechanical stress was the dominant factor in determining the EM reliability of the interconnects and should not be ignored. Moreover, after the formation of the voids and hillocks, the presence of the back stress in the interconnects can relieve the EM degradation, and thus affect the EM lifetime.

The temperature and the thermo-mechanical stress in various parts of the circuits are highly dependent on the surrounding materials and their materials properties (e.g. thermal conductivity, thermal expansion coefficient, Young's modulus, Poisson ratio, etc). The ITRS for interconnect [24] pointed out that, with the use of various interconnect, barrier and dielectric materials, it is imperative to include the material modeling capabilities into the circuit simulators so as to accurately predict the

structural, physical and electrical performances of the materials used in the interconnect structures.

The new developments in electronic system integration drives the need for 3D packaging, system-in-package (SiP), system-on-chip (SOC), stacked-integrated-circuit (SIC), and 3D integrated-circuit (3D-IC) for a variety of reasons, such as miniaturization, heterogeneous integration, improved circuit performance and lower power consumption [24]. The vertical stacking of the circuits and the overlapping of the metal layers make it increasingly difficult to use the 2D simulators to model the EM reliability of the circuit in these new technologies.

In summary, reported physics based 3D EM models have the merits of accurate modeling but they are unable to reflect the reliability of the entire circuit. Reported 2D circuit simulators, on the other hand, are able to model the EM reliability at the circuit layout level but are unable to consider many important factors for EM in the interconnects in present-day ICs and ICs of the future. It is hence imperative that a complete 3D circuit model would need to be developed, where electrical, thermal, structural and material effects are considered in order to correctly ascertain the EM reliability of the interconnects.

1.2 Objectives

This thesis aims to model the EM reliability of the interconnects at the circuit layout level using 3D model.

- (1). To construct a 3D finite element circuit model from a given 2D IC layout, and perform the transient electro-thermo-structural simulations using both Cadence (a circuit simulator) and ANSYS (a finite element software). A simple two-transistor circuit with two metal layers is used as the example.
- (2). To identify the EM weak spots of the interconnects and to analyze the effects of current density, temperature gradient, and thermo-mechanical stress gradient on the EM reliability of the circuit.
- (3). To compare the EM weak spots in a 3D circuit structure and a standard line-via test structure under both the EM test condition and the circuit operation condition.
- (4). To improve the model in (1) by extending the number of metal layers from two to six, and by including all the intra-block interconnects and the circuit components, so that the structure modeled is comparable to the real-life circuit.
- (5). To investigate the effects of the barrier layer thickness, the dielectric material, and the layout and process modifications (e.g. interconnect structures, transistor placement, SFT of the metallization) on the EM reliability of the circuit.

1.3 Contributions

The method of modeling the EM reliability in 3D at the circuit layout level has not been reported in literature, the contributions of this PhD work include:

- a. The development of the procedure for the construction of a 3D finite element circuit model from a given 2D GDSII IC layout, and the method of applying the transient current and voltage waveforms obtained from Cadence to the finite element circuit model. An investigation of the temperature response to the electrical loads and the thermo-mechanical stress response to the circuit temperature under the transient operation condition. A comprehensive analysis of the AFDs in the interconnects due to current density, temperature gradient, and thermo-mechanical stress gradient is performed and from which the EM weak spots can be identified.
- b. A study of the effects of the barrier layer thickness and the dielectric material on the EM reliability of the circuit.
- c. A demonstration of the invalidity of the use of the standard line-via test structure to evaluate the EM reliability of the circuit. Although the EM weak spots of the standard line-via test structure and the 3D circuit structure are found to be the same under the EM test condition, they are different under the circuit operation condition due to the change in the dominant driving force for EM at a lower temperature.

-
- d. An investigation on the effects of the interconnect structures on the EM reliability of the circuit. The simulation results are found to be in agreement with reported work in literature.
 - e. The construction of a 3D finite element circuit model of a realistic circuit with the inclusion of the intra-block interconnects up to the metal top. The electro-thermo-structural simulations and the identification of the EM weak spot based on the AFDs of the model are also performed.
 - f. Modifications to the circuit layout and process based on the EM weak spots identified. An improvement in the EM reliability of the circuit is observed after the modifications and it is in agreement with reported work in literature. This demonstrates the capability of the proposed model for the “design-in” reliability of an IC.

1.4 Organization of the Thesis

This thesis is organized as follows.

An introduction to the background, the objectives and the contributions of the thesis are given in Chapter 1.

In Chapter 2, literature review on the failure mechanisms in ICs and the electromigration fundamentals are presented. The importance of the 3D circuit modeling with a review of the previous work is discussed in this chapter.

Using a simple inverter circuit as an example, the construction of the 3D finite element circuit model from its 2D IC layout, the conduction of the transient electro-thermo-structural simulations using both Cadence and ANSYS, and the discussions on the results obtained are presented in Chapter 3. The effects of the barrier layer thickness and the dielectric material are analyzed as well.

A comparison on the EM performance in a 3D finite element circuit structure and a standard line-via test structure is performed in Chapter 4. The output stage of a class-AB amplifier is used as an example. The effects of the interconnect structures on the EM reliability of the circuit are also studied.

As an extension to the two metal layers circuit models in Chapter 3 and 4, a six metal layers real circuit model with the inclusion of the intra-block interconnects is constructed in Chapter 5. A RF low noise amplifier (LNA) is used as an example. Modifications to the circuit layout and process are performed based on the EM weak spots identified.

In Chapter 6, an experiment plan for the verification of the proposed model is presented. Potential difficulties during the experimentation are discussed with suggested solutions.

This thesis ends with a conclusion and a plan for the future work in Chapter 7.

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

This literature review is organized as follows. In Section 2.2, the three phases of the reliability bathtub curve and the major failure mechanisms in the wear-out phase of an IC are presented. In present-day ICs with highly scaled dimension and high current density, EM in the interconnects has become one of the dominant failure mechanisms of an IC. The fundamentals of EM and the developments in technology to reduce EM degradation are discussed in Section 2.3. In Section 2.4, a comprehensive review of the physics based EM models at the test structure level and the current density based EM simulators at the circuit layout level in literature are presented. The merits and shortcomings of these EM models and simulators are discussed. This chapter ends with a summary emphasizing the necessity of a complete 3D model at the circuit layout level in Section 2.5.

2.2 Failure Mechanisms in the Integrated Circuits

The causes of electronic equipment failure attribute 43% of the failures to design, 30% to operation and maintenance, 20% to manufacturing and 7% to miscellaneous factors [25]. As ICs become more and more complicated, the cost of re-design and re-manufacture increases dramatically, not to mention that

re-design and re-manufacture may not always be possible. As a result, it becomes increasingly necessary to incorporate “Design-for-Reliability” into the chip design flow and the CAD tools in order to reduce the failures due to design related factors.

Fig. 2.1. “Design-for-Reliability” activities and their relationship with the standard reliability bathtub curve [26].

IC reliability is usually described by the standard bathtub curve, which consists of three phases: early failure, useful life, and wear-out failure as shown in Fig. 2.1. In the early failure phase, the failure rate decreases with time and the causes of failures are mainly the design faults, poor quality components, manufacturing faults, installation errors, operator and maintenance error, etc. In the useful life stage, the failure rate is constant and the causes of failures are random. In the wear-out failure phase, the failures are due to material wear, fatigue and other intrinsic aging mechanisms. The failure rate in this phase increases with time. Reliability should be designed throughout all the three phases, so as to have a high

quality, long-lasting product.

Early failures can be screened out by burn-in tests, functional tests, or IDDQ tests, and the failures during the useful life stage can be avoided by proper management. Using a proper design to reduce the failures in the wear-out phase is one of the main tasks of the designer [26].

In a CMOS IC, the three major failure sites in the wear-out phase are the interconnects, the oxide interface, and the junction [26]. The main failure mechanisms at these failure sites are shown in Fig. 2.2.

Fig. 2.2. Main failure mechanisms at the major failure sites of a CMOS device [26].

(1). Interconnect Failures:

Electromigration and stress migration are the dominating failure mechanisms in the interconnects.

Electromigration is the movement of the conducting atoms through a conductor as a result of the momentum transfer between the current-carrying electrons under high current density (above 10^5 A/cm^2) [27], as illustrated in Fig. 2.3.

Fig. 2.3. The momentum transfer between the electrons and the metal atoms in the interconnects [27].

The momentum transfer causes a net flux of the conducting atoms. Depletion or accumulation of atoms occurs when there is a non-zero divergence of the atomic flux along the conductor. Voids are formed upon depletion and hillocks are formed upon accumulation. The formation of the voids can cause an unfavorable increase in the line resistance and the current density. Open circuit occurs if the void continues to grow and breaks the line. On the other hand, if the hillocks get large enough, the adjacent lines or the overlying lines can be shorted together, and this can cause serious reliability problem [27]. The formation of the void and the hillock in the metal interconnects is shown in Fig. 2.4(a) and (b) respectively.

Fig. 2.4. The formation of (a) the void and (b) the hillock in the interconnects [5].

Sites with structural inhomogeneity (e.g. triple point) and local grain size variation are the typical places for the divergence of the atomic fluxes. In Fig. 2.5(a),

accumulation of atoms occurs when the flux into the junction is larger than that out of the junction, and depletion occurs otherwise [27]. In Fig. 2.5(b), accumulation of atoms occurs when the atomic migration is from a fine grained region (i.e. more grain boundaries for atomic migration) to a coarser grained region, and voiding occurs when the migration is from a coarse region to a finer region [28].

Fig. 2.5. Typical places for flux divergence in the interconnects. (a) At the grain boundary triple point [27] and (b) with local grain size variation [28].

Interfaces between different materials are the common locations for mass divergence due to the difference in diffusivity [29]. In Fig. 2.6(a), when the current flows through the contacts, the metal atoms are either moved away from or towards the contact/substrate interfaces depending on the direction of current flow. Assuming the metal lines are surrounded by the barrier material and thus the diffusion across the interface is negligible, depletion of atoms occurs at the region where the removed metal atoms are unable to be replenished, and accumulation occurs when the brought metal atoms are unable to be removed. In Fig. 2.6(b), as the bulk lattice diffusivity of Al at room temperature (27 °C) is much larger than that of W ($3.2 \times 10^{-29} \text{ m}^2 \text{ s}^{-1}$ and $5 \times 10^{-88} \text{ m}^2 \text{ s}^{-1}$ respectively) [30], the Al atoms tend

to migrate whilst W exhibits negligible atomic transport. There is a high chance that large mass divergence forms at the via/interconnect interfaces.

Fig. 2.6. Material accumulation and depletion at the interfaces of (a) contact and (b) via [29].

Stress migration, also known as stress-induced voiding, is the metal voiding as a result of thermo-mechanical stress gradient in the absence of electric current. After the high temperature processing of the interconnect structures, a large tensile stress is built in the interconnects due to the mismatch of the thermal expansion coefficient of the metallization with its surrounding materials. This gives rise to the large intrinsic stress in the interconnects at room temperature (e.g. a few hundreds MPa) [31]. The intrinsic stress relaxes with time through the diffusion of the vacancies in the interconnects. This diffusion process leads to the formation the voids, as can be seen in Fig. 2.7. The continuous growth of the void

can totally break the metal line and causes circuit failure.

Fig. 2.7. SEM micrograph of a stress-induced void in an aluminum interconnect [32].

(2). Gate Oxide Failures:

The main failure mechanisms found at the oxide interface are hot carrier injection and gate oxide breakdown.

After the excitation by the electric field in the transistor channel region, the carriers (either electrons or holes) gain sufficient kinetic energy to overcome the energy barrier necessary to cross the oxide/substrate interface, and inject into the gate oxide. This phenomenon is called hot carrier injection [33]. The injection of the carriers can cause damage to the oxide/substrate interface and/or trapped charges in the gate oxide, as shown in Fig. 2.8. The oxide damage and the trapped charges can shift the electrical parameters of the transistor, as shown in Fig. 2.9.

Fig. 2.8. The trapped charges (+) and the interface damage (ΔD_{it}) during hot carrier injection in an NMOS transistor [33].

Fig. 2.9. Degradation of the I - V curve of (a) an n-channel and (b) a p-channel transistor after hot carrier injection [33].

Gate oxide breakdown is caused by the positive charge build up in the oxide near the injecting cathode interface. As shown in Fig. 2.10(a), the tunneling current across the oxide layer causes impact ionization and produces positive charge. Initially, the tunneling currents are extremely low. The positive charges drift back towards the cathode and are believed to be trapped at the localized “weak spots”. These trapped positive charges lower the energy band and lead to further electron injection as shown in Fig. 2.10(b). The injection of the electrons leads to

further impact ionization and positive charge trapping, and results in a runaway process. The current at the positive charge trapping sites increases dramatically. This high current produces a heating effect sufficient to melt the oxide and causes oxide rupture. Electrical shorts occur through the thermal oxide between the metallization and the silicon. Oxide usually becomes leaky before the catastrophic oxide rupture, and the leakage currents can cause the circuits to be nonfunctional [34].

Fig. 2.10. (a) A model for the oxide breakdown mechanism and (b) the energy band diagram showing a lowering of the injection barrier due to positive charge trapping in the oxide [34].

(3). Junction Failures:

At the junction of a transistor, the main failure mechanisms are latch-up and EOS/ESD.

Latch-up occurs when a parasitic *pnpn* device in a CMOS device is triggered by a

voltage or current transient and a low resistance path is formed between the power supply and the ground [35], as shown by the bold lines in Fig. 2.11.

Fig. 2.11. The formation of the parasitic bipolar transistors in a CMOS device [35].

A CMOS structure has the inherent pnp and npn parasitic bipolar transistors. For the n -well CMOS shown in Fig. 2.11, the $p+$, n -well and p -substrate form a parasitic vertical pnp bipolar transistor, whereas the $n+$, p -substrate and n -well form a parasitic lateral npn transistor. When the substrate current I_S and the well current I_W are sufficient to cause an ohmic drop of approximately 0.7 V, the base-emitter junctions for both transistors are sufficiently forward-biased to provide a significant amount of current to trigger the bipolar transistor action. Both bipolar devices are in the active mode. The base of the pnp are connected to the collector of the npn , and a feedback loop is formed by the two bipolar transistors with the loop gain equal to the beta product $\beta_{pnp}\beta_{npn}$ (β_{pnp} and β_{npn} are the common-emitter current gains for the pnp and npn transistors respectively). If the loop again is larger than one, positive feedback and latch-up occur [35]. The

circuit can be destroyed due to overcurrent during latch-up. Once latch-up has begun, the only way to stop it is to reduce the current below a critical level, usually by removing the power from the circuit.

Electrical overstress (EOS) is typically caused by an over voltage or over current event with a duration exceeding 100 ns to 1000 ns or a nominal duration of 1 ms during the device operation [36]. Events that can lead to EOS damage include voltage spikes, lightning strikes and any temporary and unexpected connections to power or ground. Electron static discharge (ESD) occurs when two objects at different potentials come into direct contact with each other, or when a high electrostatic field develops between two objects in close proximity. The duration of ESD is shorter (about 1 ns to 1 μ s) than that of EOS [37]. EOS and ESD can induce failures due to thermal runaway from Joule heating, junction leakage, short, burn-out, dielectric rupture, resistor-metal interface rupture, resistor/metal fusing, and die surface charging. Fig. 2.12 shows the damages caused by EOS and ESD in an IC.

Fig. 2.12. Damage due to (a) EOS and (b) ESD in an IC. Images Courtesy of Rohm Electronics and Bunny Studios LCC.

To manage the failures due to the above failure mechanisms, the “Reliability-Rule-Checker” had been integrated into the circuit design tools [26], as shown in Fig. 2.13.

Fig. 2.13. The development and implementation of the “Reliability-Rule-Checker” tools [26].

The design rules for electromigration are based on the current density (i.e. time-average current or root-mean-square current). There are different maximum current density specifications for different metal layers under different operation temperatures. To prevent gate oxide breakdown, the maximum voltage limits have been specified by the design rules depending on the gate oxide thickness of the transistors. The design rules for hot-carrier injection are typically defined in terms of the substrate and drain currents. The control of latch-up is through the management of IR drops in terms of the well-tap to gate distances. The in-process ESD is controlled by a set of layout-based design rules that limit the ratio of the conductor (antenna) area and the gate area.

Various design practices have been implemented based on the “Reliability-Rule-

Checker” to prevent or reduce the wear-out failures. For example, use wider metal lines and dummy contacts to reduce the current density and retard EM [38]; avoid placing the metal lines near the chip corner to reduce shear stress [39]; use thick oxide transistor for high voltage operation [40]; use long channel device and large transistor to eliminate hot carrier effects [41]; use bipolar spoiling or bipolar decoupling and guard rings to prevent latch-up [42]; use protection circuit to enhance ESD resistance [43]. Furthermore, as temperature is a key factor in determining the circuit reliability, innovative materials and designs for better heat dissipation and lower power consumption are being investigated continuously [44].

In present-day ULSI, interconnect reliability has become the main factor that affects the circuit reliability due to the continuous scaling of the width, length and current density, as well as the increase in the number of metal layers.

Fig. 2.14 shows the width, length and current density scaling in the interconnects at nanometer technology. The decreasing width x length product decreases the current density limit for EM, J_{EM} . On the other hand, the increasing circuit operating frequency and the reduced cross sectional area increase the maximum operating current density in the circuit, J_{max} . J_{max} will exceed the J_{EM} limits for the current Cu technology in year 2018, as shown in Fig. 2.15 according to ITRS [45]. The width scaling further aggravates the EM degradation by a rise in the interconnect resistivity due to electron scattering [46-48].

Fig. 2.14. Width, length and current density scaling in the interconnects [5].

Fig. 2.15. Evolution of J_{max} (from device requirement) and J_{EM} (from targeted lifetime) [45].

Fig. 2.16 illustrates the typical cross-sections of a MPU device and an ASIC device. In year 2009, the number of metal layers (includes ground planes and passive devices) in a MPU had already reached 12 layers, and it continued to increase by one every four years and will become 15 layers in year 2021 [24]. The growth in the number of metal layers greatly increases the total interconnect length and the possible EM failure sites in a device. The increase in the total interconnect length and the scaling of Metal 1 pitch (Fig. 2.17) increase the line resistance and result in a longer resistive-capacitive delay (RC delay) for both the local and the

intermediate interconnects, as shown in Fig. 2.18. As the interconnect-based delay accounts for more than 80% of the total path delays in the 90 nm node and below [17], the increase in the RC delay of the interconnects increases the delay of the circuit. Longer delay not only degrades the circuit performance but also increases the circuit power dissipation and the circuit temperature. The EM degradation rate increases at higher temperatures and the circuits will fail faster.

Fig. 2.16. Typical cross-sections of hierarchical scaling for (a) a MPU device and (b) an ASIC device [24].

Fig. 2.17. Metal 1 pitch scaling in the interconnects [45].

Fig. 2.18. The increase in the interconnect RC delay (for 1 mm wires) with year [45].

From the aforesaid, we can see that EM has become the dominant failure mechanism in ICs, and it remains to be a major issue in present-day ICs and ICs of the future. It is important to ensure the EM reliability throughout the IC design flow, so as to achieve a reliable, long-lasting product.

It is always better to model the EM process before conducting the experiments as the experiments are usually very costly especially for the advanced technology nodes. Therefore, many models and simulators have been developed to simulate the EM reliability of the interconnects at both the test structure level and the circuit layout level. To simulate the EM process, one has to understand the EM physics. A brief introduction to the EM fundamentals is presented in the next section.

2.3 Electromigration Fundamentals

The phenomenon of EM was first discovered by the French scientist Gerardin in 1861 [49] and the study of EM gained practical interest with the commercial appearance of the integrated circuits in 1960s. After the first systematic report by Fiks in 1959 [50], Huntinton *et al.* [51] made great contribution to the study of EM by proposing the first EM model known as the ballistic model. The model was based on electron scattering by the defect (or the impurity). The momentum transfer from the scattered electrons to the defect per unit time, which was also called the driving force, was given as [51],

$$\vec{F}_{wind} = -\frac{n_e e \tau}{n_d \tau_i} \vec{E} = -\frac{n_e \rho_d}{n_d \rho} e \vec{E} \quad (2.1)$$

where

F_{wind} is the wind force,

n_e and n_d are the electron and the defect density respectively,

e is the electron charge,

$-e \tau E$ is the momentum transferred from the electron to the defect,

τ_i is the transport life time corresponding to the scattering by the defects under consideration (or the mean time between two successive collisions between the electrons and the defects),

ρ is the resistivity of the conductor, which depends on temperature as $\rho = \rho_0(1 + \alpha(T - T_0))$, and α is the temperature coefficient of resistivity, ρ_0 is the electrical resistivity at temperature T_0 ,

ρ_d is the resistivity contribution from the defects in the metallization,

and

E is the electric field.

Later, Bosvieux *et al.* [52] and Verbruggen *et al.* [53] improved the ballistic model by considering the disturbance of current flow near the defect due to the scattering of the electrons by the defect.

The equation mentioned above, though is the fundamental to all the calculations of the wind force in metals, it is too complicated to be used in practical. Simplified equations are used instead where two opposing forces are assumed to act on a single atom in a conductor, namely the electron wind force and the direct force [53]. The electron wind force is the force experienced by the conducting atoms in the direction of the electron flow due to the momentum exchange between the moving electrons and the atoms, and it can be described as [53],

$$\vec{F}_w = -en_e\lambda\sigma_i \vec{E} = -en_e\lambda\sigma_i \vec{j} \rho \quad (2.2)$$

where

λ is the mean free path, which is the average distance a molecule travels between collisions,

σ_i is the cross-section for collision between the electrons and the conducting atoms, and

j is the current density.

The direct force, on the other hand, is the force experienced by the activated positive atoms in the opposite direction to the electron flow due to the application of the electric field, and it is given by [53],

$$\vec{F}_d = -aZe \vec{E} = -aZe \vec{j} \rho \quad (2.3)$$

where

a is the factor accounting for the migration effects of the conducting atom ($a \ll 1$), and

Z is the actual valence of the conducting atom.

The net force experienced by the conducting atom is the resultant effect of the above two forces [53],

$$\vec{F}_{net} = \vec{F}_w + \vec{F}_d = (Z_w + Z_d) e \vec{j} \rho = Z_{eff}^* e \vec{j} \rho \quad (2.4)$$

where

Z_w , Z_d and Z_{eff}^* are the effective valences for the electron wind force, direct force and the net force respectively.

In good conductors like metals, the electron wind force is the dominant force experienced by the meal atoms, and it results in the atomic migration towards the anode.

In 1969, Jim Black derived the Black's equation that related the median time to failure with the current density and temperature of the metal line [54]. The

equation was given as [54],

$$t_{50} = Aj^{-2} \exp\left(\frac{E_a}{k_B T}\right) \quad (2.5)$$

where

t_{50} is the median time to failure,

A is a constant which contains a factor involving the cross-sectional area of the metal line,

E_a is the activation energy,

k_B is the Boltzman's constant, and

T is the temperature of the metal line.

The formulation of this semi-empirical formula was one of the most important millstones in the EM study of the interconnects, and this formula was widely used by the researchers later on. However, this simple equation was unable to consider many physical factors that could seriously affect the EM process. Recent reports [55-58] showed that the Black's equation was no longer true for the application in present-day ULSI interconnect system.

In 1976, Blech *et al.* discovered the Blech effect [59]. They found that during the formation of the voids and hillocks, there was a “back flow” of atoms (i.e. a reverse migration) due to the presence of back stress in the interconnects and EM process stopped when the back stress compensated the EM driving force (i.e. the

net force). With this finding, Blech derived an expression as given below, and the term $(jL)_c$ is called the critical product for EM failure [59],

$$(jL)_c = \frac{\Omega'(\sigma_{th} - \sigma_0)}{|Z_{eff}^*|e\rho} \quad (2.6)$$

where

Ω' is the atomic volume,

L is the metal line length,

σ_{th} is the maximum stress the metal line can withstand, and

σ_0 is the stress at $x = 0$.

This critical product was known as the “Blech product”. For a given current density j , the maximum length that the metal line will not fail due to EM was the “Blech length”. The wire with a length below the “Blech length” was called the “immortal” wire.

In 1989, Vaidya *et al.* discovered the grain size effect [60]. They found that the bamboo structure had a longer EM lifetime than the polycrystalline structure due to the significant reduction in the grain boundary mass flow of the atoms and the number of triple points in the interconnects. The work by Blech and Vaidya provided the insight of the physical factors that affected the EM reliability of the interconnects.

With the development of the technology, the use of the barrier material had dramatically improved the EM reliability of the interconnects. The barrier material not only prevents the out diffusion of the metal atoms but also provides an alternative current path after the void formation due to EM [7], and thus enhance the EM resistance.

With the understanding of the basic theories of EM and the major technological developments to improve the EM reliability, accurate prediction of the EM reliability of the interconnects should therefore include the physical factors as well as the structural and material effects.

2.4 EM Models and Simulators

Many EM models and simulators have been developed in literature. In this section, they are categorized as two main types, the physics based EM models at the test structural level (i.e. the localized interconnect structure like the simple metal line or the line-via structure), or the current density based EM simulators at the circuit layout level.

2.4.1 Physics based EM models at the Test Structure Level

2.4.1.1 1-Dimensional (1D) EM models

The focus of the 1D EM modeling is on the simulation of EM kinetics. The 1D EM models are usually based on solving the EM equations. The basic EM equation is the continuity equation from the first principle, which is given by [61],

$$\frac{\partial C_v}{\partial t} + \frac{\partial J_v}{\partial x} + \gamma = 0 \quad (2.7)$$

where

C_v is the instantaneous vacancy concentration at position x and time t ,

J_v is the vacancy flux due to the EM driving forces, and

γ is a sink/source term which allows for the recombination or generation of vacancies at the grain boundaries, the dislocations, or the surfaces.

The sink/source term in Eqn. (2.8) can be described as [61],

$$\gamma = \frac{C_v - C_{ve}}{\tau_v} \quad (2.8)$$

where

C_{ve} is the equilibrium concentration of vacancies within the grain, and

τ_v is the average lifetime of a vacancy at the grain boundary.

Based on the net vacancy flux along the length of the interconnects due both to the electron wind force and the concentration gradient, the 1D continuum EM model can be written as [61],

$$J_v = -D_v \left(\frac{\partial C_v}{\partial x} - \frac{eZ^*E}{k_B T} C_v \right) \quad (2.9)$$

where

$$D_v \text{ is the diffusivity of the vacancy given by } D_v = D_0 \exp\left(-\frac{\Delta E_a}{k_B T}\right)$$

with D_0 as the prefactor of the self-diffusion coefficient, and

eZ^* is the effective charge of the diffusing species.

Combining with the continuity equation, and assuming that D_v does not vary with position, the evolution of the vacancy concentration with time along the interconnect line length can be written as [61],

$$\frac{\partial C_v}{\partial t} - D_v \frac{\partial}{\partial x} \left(\frac{\partial C_v}{\partial x} - \frac{eZ^*E}{k_B T} C_v \right) + \gamma = 0 \quad (2.10)$$

Based on Eqn. (2.10), Rosenberg *et al.* developed a 1D model that described the interaction of vacancies between the grain boundaries and the grains in an infinite metal line [62]. This model was one of the pioneer works in 1D EM modeling and provided a numerical solution to Eqn. (2.7).

However, the unbounded condition in Rosenberg's model made it unable to deal with the length effect (i.e. Blech effect) that might occur in a short metal line. As an improvement, Shatzkes *et al.* modeled the evolution of vacancies at the end of a semi-infinite line with a blocking boundary (Fig. 2.19) [63], and Clement *et al.* did a similar modeling in a finite line under different boundary conditions [64].

Fig. 2.19. The semi-infinite grain boundary in Shatzkes *et al.*'s model.

However, both Shatzkes and Clement's models ignored the sink/source term, and this could cause the calculated time-to-failure to become too short, e.g., a few second, which is unrealistic as the EM damage is a long time process and usually takes hundreds of hours as observed from the experimental results.

Furthermore, the above models assumed that the current density was evenly distributed throughout the metal lines and an isothermal condition was considered. This is not true especially in multi-level structures containing the contacts and vias [17]. Moreover, the thermo-mechanical stress factors were ignored in these models. The ignorance of the thermo-mechanical stress factor seriously affects the accuracy of the simulation as the thermo-mechanical stress gradient is one of the most important factors in EM modeling as will be shown in the latter sections.

Another disadvantage of the aforementioned vacancy flux models is that the back stress effect cannot be observed as the vacancy concentration gradient does not retard the EM damage. To solve this problem, Korhonen *et al.* developed a

model that used the atomic flux approach instead of vacancy flux [65]. With the consideration of the stress evolution, the retardation of EM due to back flow stress could be properly modeled.

In summary, the 1D EM models are simple to use and easy to solve, and they are able to identify the critical location along a certain length of a metal line once a proper boundary condition is set up. However, most of the 1D models are unable to consider the temperature and thermo-mechanical stress effects in the interconnects, render an inaccuracy in the simulation results. Furthermore, the inadequacy on dimensionality limits the application in modeling the microstructure effect on the EM performance. To improve the modeling, 2D models were developed.

2.4.1.2 2-Dimensional (2D) EM models

Different from the 1D EM models which track the vacancy concentration evolution in a 1D metal line, most of the 2D EM models are based on the formulation and calculation of the atomic flux using either the diffusion path approach, or the driving force approach.

In the diffusion path approach, the electron wind force is usually taken as the sole driving force for the EM mass transport. It is assumed that one or more diffusion paths for the vacancies and/or metal atoms are dominant in EM and the effects of

the other paths are negligible. For an accurate simulation, it is important to correctly determine the dominant diffusion path from the values of the activation energies obtained from the experiments. Typical EM diffusion paths include the lattice diffusion inside a grain (i.e. bulk diffusion), the grain boundary diffusion, the interface diffusion, the diffusion at the dislocations, and the surface diffusion, as shown in Fig. 2.20.

Fig. 2.20. Different diffusion paths in an interconnect. 1. bulk, 2. grain boundary, 3. grain/bulk interface, 4. dislocation, 5. surface [66].

Taking into account of all the possible diffusion paths, the EM drift velocity can be written as [66],

$$\vec{v}_d = \frac{D_{eff}(T)}{k_B T} \cdot (Z_{eff}^* \cdot e \cdot \rho \cdot j) \quad (2.11)$$

where

$$D_{eff} \cdot Z_{eff}^* = D_b \cdot Z_b^* \cdot f_b + D_d \cdot Z_d^* \cdot f_d + D_i \cdot Z_i^* \cdot f_i + D_s \cdot Z_s^* \cdot f_s + D_{gb} \cdot Z_{gb}^* \cdot f_{gb} \quad (2.12)$$

The subscripts in Eqn. (2.12) denote the diffusion paths as follows: b : bulk, d : dislocation, i : interface, s : surface, gb : grain boundary with f_r ($r = b, d, i, s, gb$) as the fraction of atoms diffusing through a given path way.

As the interconnect line width shrinks to submicron level, the diffusion path approach is no longer valid as the other driving forces become dominant [7]. This motivated the development of the driving force approach. In the driving force approach, more than one driving forces are considered. An example of the driving force model from the work by Sukharev *et al.* is shown below, and the model is based on the mass balance equation for atomic concentration [67],

$$\frac{\partial N}{\partial t} + \nabla \cdot J = 0 \quad (2.13)$$

where

$N(r, t) = N/N_0$ is the normalized atomic concentration at location r and time t ,

N is the atomic concentration,

N_0 is the initial atomic concentration,

J is the total atomic flux at this location, and

$\nabla \cdot J$ is the total atomic flux divergence.

The total atomic flux in the above equation is the sum of the fluxes caused by the driving forces due to the concentration gradient of the metal atoms, electron wind

force, temperature gradient, and thermo-mechanical stress gradient, which are given as J_N , J_{EWF} , J_T , and J_S respectively [67],

$$J_N = -D\nabla N \quad (2.14)$$

$$J_{EWF} = \frac{NeZ^*D\rho}{k_B T} j \quad (2.15)$$

$$J_T = -\frac{NDQ^*}{k_B T^2} \nabla T \quad (2.16)$$

$$J_S = -\frac{ND\Omega'}{k_B T} \nabla \sigma_H \quad (2.17)$$

where

D is the diffusivity of the metal atoms,

∇N is the concentration gradient of the metal atoms,

∇T is the temperature gradient along the metal line,

Q^* is the heat of transport of the metal line,

σ_H is the local hydrostatic stress, and is calculated using the average

hydrostatic stress values in the metal line in the x , y , z direction as

$$\sigma_H = (\sigma_{xx} + \sigma_{yy} + \sigma_{zz})/3, \text{ and}$$

$\nabla \sigma_H$ is the stress gradient along the metal line.

For a given current density, temperature and stress gradients, the atomic concentration at any point of the considered segment can be obtained using Sukharev's model. In addition, the model included different diffusivity values along different diffusion paths, so as to simulate the effect of microstructure on the atomic fluxes.

In summary, the 2D EM models use the atomic flux instead of vacancy flux. The diffusion path approach and the driving force approach are the main modeling methods for the 2D models. The 2D models have the advantage over the 1D models as they are able to consider more factors that are essential to EM.

With the shrinking interconnect dimension and the use of the barrier and low- κ materials, the impact of the surrounding materials on the EM reliability of the interconnects becomes more and more significant. Most of the 1D and 2D EM models consider only the EM process within the interconnect line itself and ignore the temperature and thermo-mechanical stress effects brought by the surrounding materials. For an accurate EM modeling, the factors due to the interconnect line as well as the surrounding materials should be taken into consideration. This drives the need for 3D EM modeling.

2.4.1.3 3-Dimensional (3D) EM models

Finite element analysis using the AFD approach is a common practice in 3D EM modeling. This approach is used as there is a direct relationship between the EM failure time and the AFD.

Let ΔN be the number of atoms accumulated in a small interconnect segment of length Δl for a time period of Δt due to the presence of the atomic flux divergence $\nabla \cdot J$. For an infinitesimal time period, ΔN can be written as [68],

$$\Delta N = \lim_{\Delta t \rightarrow 0} p_w p_t \Delta t \Delta l (\nabla \cdot J) \quad (2.18)$$

where

p_w and p_t are the effective diffusion path width and thickness respectively.

The growth rate of volume V_o of mass depletion or accumulation can be obtained by multiplying Eqn. (2.18) with the atomic volume Ω [68],

$$\frac{\partial V_o}{\partial t} = p_w p_t \Omega (\nabla \cdot J) \quad (2.19)$$

Integrating Eqn. (2.19), the critical volume of mass depletion or accumulation required for failure to occur, V_c , is calculated as [68],

$$\int_0^{V_c} \partial V_o = \Omega \Delta l \int_0^{t_f} p_w p_t (\nabla \cdot J) \partial t \quad (2.20)$$

Applying the concept of average, a qualitative relationship between the time-to-failure t_f and the AFD can be derived [68],

$$t_f = \frac{V_c}{\Omega \Delta l p_w p_t \nabla \cdot J} \quad (2.21)$$

From Eqn. (2.21), it is obvious that the EM failure time of the interconnects is inversely proportional to the AFD. Void is assumed to nucleate at the location with the highest positive AFD and grows irreversibly. Experimental observation in [69] showed that the void was found at the location of the maximum AFD with

excellent agreement, indicating the accuracy of this approach.

After the first study of the AFD by Sasagawa *et al.* in 1998 [9, 10], Rzepka *et al.* developed a 3D finite element EM model in the interconnects in 1999 [11]. This pioneer work in 3D modeling simulated the migration of matters due to various driving forces, namely the concentration gradient, the thermo-mechanical stress gradient, the electrical field, the temperature gradient, and the surface tension due to the changes in surface curvature [11].

In 2001, Dalleau *et al.* proposed a 3D finite element model that simulated the 3D void formation and propagation process in a pad and a meander structure [12]. In their model, they used three dominant driving forces for the AFD, namely the electron wind force, the temperature gradient induced driving force, and the thermo-mechanical stress gradient induced driving force.

The atomic flux due to the three driving forces were modeled using Eqn. (2.22) to (2.24) respectively [12],

$$\vec{J}_{EWF} = \frac{N}{k_B T} e Z^* \vec{j} \rho D_0 \exp\left(-\frac{E_a}{k_B T}\right) \quad (2.22)$$

$$\vec{J}_T = -\frac{NQ^* D_0}{k_B T^2} \exp\left(-\frac{E_a}{k_B T}\right) \nabla T \quad (2.23)$$

$$\vec{J}_S = \frac{N\Omega' D_0}{k_B T} \exp\left(-\frac{E_a}{k_B T}\right) \nabla \sigma_H \quad (2.24)$$

After obtaining the atomic fluxes, the divergences due to electron wind force, temperature gradient induced driving force, and thermo-mechanical stress gradient induced driving force were calculated using Eqn. (2.25) to (2.27) respectively [12]:

$$\nabla \cdot \vec{J}_{EWF} = \left(\frac{E_a}{k_B T^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho} \right) \cdot \vec{J}_{EWF} \nabla T \quad (2.25)$$

$$\nabla \cdot \vec{J}_T = \left(\frac{E_a}{k_B T^2} - \frac{3}{T} + \alpha \frac{\rho_0}{\rho} \right) \cdot \vec{J}_T \nabla T + \frac{NQ^* D_0}{3k_B^3 T^3} \vec{j}^2 \rho^2 e^2 \exp\left(-\frac{E_a}{k_B T}\right) \quad (2.26)$$

$$\begin{aligned} \nabla \cdot \vec{J}_S = & \left(\frac{E_a}{k_B T^2} - \frac{1}{T} \right) \cdot \vec{J}_S \nabla T + \frac{2E' N \Omega' D_0 \alpha'}{3(1-\nu) k_B T} \exp\left(-\frac{E_a}{k_B T}\right) \left(\frac{1}{T} - \alpha \frac{\rho_0}{\rho} \right) \nabla^2 T \\ & + \frac{2E' N \Omega' D_0 \alpha'}{3(1-\nu) k_B T} \exp\left(-\frac{E_a}{k_B T}\right) \frac{\vec{j}^2 \rho^2 e^2}{3k_B^2 T} \end{aligned} \quad (2.27)$$

where E' , α' and ν are the Young's Modulus, the thermal expansion coefficient, and the Poisson ratio of the metal line respectively.

In summary, the 3D EM models are mainly based on the AFD approach. As there is a direct relationship between the time-to-failure and the AFD, this approach can be used to predict the EM failure time and the void nucleation location of the interconnects.

The 3D models have the advantage of considering both the structural (e.g. metal line structure, metal stack pattern) and the material effects for both the interconnect line itself and the surrounding materials. Physical factors such as the back stress effect and the microstructure effect can be included. The dynamic simulation of the void

nucleation process along different diffusion paths can be carried out in the 3D model using the Monte Carlo method [23]. The 3D models are much more accurate and flexible as compared with the 1D or 2D models.

However, the 3D modeling is much more complicated and usually performed only at the localized region of an interconnect tree, e.g., on a simple metal line or at the line-via region. Fig. 2.21 shows the standard line-via test structures commonly used in 3D EM modeling and EM experiments. Depending on the current flow direction, the structures can be characterized as the downstream (Fig. 2.21(a)) or upstream structure (Fig. 2.21(b)).

Fig. 2.21. The side views of the two-level Cu Dual Damascene (DD) line-via test structures, showing (a) the downstream structure and (b) the upstream structure [7].

Simple straight line and two level line-via structures are only part of the real circuit structures. The results obtained from these partial-circuit structures can only represent the reliability of the respective localized region. The impact of excluding the rest of the circuit structures to the overall EM reliability of the circuit has not

been investigated. As will be shown in Chapter 4, the EM weak spots for a line-via test structure is different from the 3D circuit structure under the circuit operation condition. Therefore, using a localized structure may not be able to correctly predict the EM weak spots in a circuit. This drives the need to perform the EM reliability evaluation at the circuit layout level.

2.4.2 Current Density Based EM Simulators at the Circuit Layout Level

While the physics based EM models are usually adopted by the researchers studying the EM failures in the test structures, current density based EM simulators are more commonly used by the circuit designers in identifying the EM weak spots at the circuit layout level.

Besides the “Reliability-Rule-Checker” that had already been integrated into the circuit design tools as discussed in Section 2.2 [26], various 2D simulators and modeling tools had been developed to predict the possible failure locations in ICs due to EM.

In 1992, a well-known EM simulator BERT was developed by Hu *et al.* [16]. This simulator calculated the EM lifetime based on the current density distributions in the interconnects and expressed the EM failure rate of the circuit as a function of time, voltage, and temperature. However, the exclusion of the Joule

heating effect give rise to an overestimation of the median time to failure (MTTF) of the circuit by two orders of magnitude as the interconnect temperature can be 100 °C higher than the ambient temperature due to Joule heating [19].

Later on, Teng *et al.* developed a temperature-dependent EM simulator iTEM [19]. iTEM predicted the EM lifetime based on the current density at the power and ground bus network, and took into consideration the temperature effects. However, breaking the interconnect trees into individual straight line segments could result in an inaccurate result. This is because the current densities from different segments of an interconnect tree interact with each other and the stress evolution of different segments are coupled. These effects were ignored when treating the interconnects as independent failing units [70-72].

As an improvement, Alam *et al.* built an interconnect-tree based reliability tool SysRel [13-15]. A hierarchical analysis method was used in this modeling tool. The immortal interconnect trees were filtered off based on the critical product. The lifetime of the remaining mortal trees was calculated using the void nucleation, extrude and growth model [73] depending on whether the interconnect tree was “via-above” or “via below” (i.e. whether it is a downstream or an upstream structure). To cater for the temperature effects during circuit operation, the via temperature at different metal layers and the substrate temperature were included in this model. However, the constant temperature assumption for the vias and the

substrate is not true in the real case, as their temperatures continuously vary with the switching activities of the transistors and are affected by other factors like current crowding, etc.

Due to the complexity of ICs, almost all the circuit layout level EM simulators are 2D. 2D simulations may underestimate the peak current density when the track and via widths are different. This underestimation may result in an EM susceptible design as shown by Trattle *et al.* [74]. To overcome this problem, Jerke *et al.* built a quasi 3D model at the interconnect contact and via region [75]. In this quasi 3D model, the 2D metal lines were connected by the 3D contacts and vias at the region of interest as identified by the 2D simulation. The irregularities in current densities within the contact and via structures could be identified. However, the impact on the current density distribution due to the changes in the metal layer thickness, especially at the thick metal top is unable to be included in this model.

All the above mentioned methods estimated the EM reliability of the circuit based on the current density distribution or the critical product in the interconnects. The work by Hau-Riege *et al.* showed that the probability of immortality in a Cu-based interconnect is no longer described by the critical product as in an Al-based interconnect [76]. Also, as already mentioned in the previous section, electron wind force due to current density is no longer the sole driving force for EM in the

interconnects, especially when the metal line width scales to 0.20 μm and below [77]. In fact, the AFD due to thermo-mechanical stress gradient induced driving force (AFD_S) dominates over electron wind force (AFD_EWF) in the interconnects with a line width smaller than 0.20 μm . As can be seen in Fig. 2.22, the ratio of AFD_S over AFD_EWF is larger than 150% when the interconnect line width is smaller than 0.20 μm , and this ratio increases when the test temperature approaches the circuit operation temperature (around 100 $^{\circ}\text{C}$). Therefore, the simulators with current density as the main consideration for EM are no longer adequate.

Fig. 2.22. Ratio of the AFD due to thermo-mechanical stress gradient induced driving force (AFD_S) over electron wind force (AFD_EWF) with different line width [77].

Moreover, other phenomena such as high stress at the sharp corners, current crowding due to the changes in the current flow paths, and the changes in the void nucleation location due to the changes in the aspect ratio of the cross section of the

metal line are difficult to be observed in 2D [23, 78]. Fig. 2.23 shows the change in the void nucleation location when the aspect ratio of the metal line changes. The void nucleation location is at the Metal 1/via interface in a wide metal line in Fig. 2.23(a) while it is at the outer corner of Metal 1 in a narrow metal line in Fig. 2.23(b).

Fig. 2.23. The void nucleation location in (a) a wide metal line and (b) a narrow meal line [23]. The arrows indicate the maximum AFD location.

In addition, the 2D model is unable to represent the entire circuit geometry due to layer overlapping. Complex geometries include the junctions and the segments with varying shapes and widths cannot be built in a 2D model. As the metallization level and the number of contacts and vias increases due to scaling, it becomes increasingly difficult to simply use the 2D simulations for an efficient and effective EM awareness design.

In summary, although the 2D circuit simulators are able to model the EM

reliability of the interconnects at the circuit layout level, their accuracies are not as good as the physics based EM models due to the ignorance of some essential factors for EM such as the temperature gradient, the thermo-mechanical stress gradient, the properties of the surrounding materials, the interconnect structures and geometries. Furthermore, the 2D simulators are unable to handle complex structures in the vertical direction, and hence their applications are limited with increasing circuit density and number of metal layers. It is imperative that the 3D circuit model with the consideration of multiple driving forces should be developed at the circuit layout level, so as to accurately predict the EM failure sites in ICs.

2.5 Summary

This chapter summarized the common failure mechanisms in ICs. Electromigration (EM) is the major failure mechanism of the interconnects at advanced technology nodes. Some fundamentals on EM were introduced. A literature review on the physics based 1D, 2D and 3D EM models at the test structure level, and the current density based 2D EM simulators at the circuit layout level was presented.

With the inclusion of the factors due to electrical, thermal, and thermo-mechanical stress, the physics based 3D EM models were able to accurately predict the EM

process in the interconnects. However, the complexity of the models limited their application at the circuit layout level. The “localized” modeling might not always predict the correct EM failure sites of the circuit, especially under the circuit operation condition. On the other hand, the 2D circuit simulators were able to look at the entire circuit as a whole. However, treating current density as the sole driving force for EM was no longer valid at submicron level. The limitation in dimensionality increased the difficulty in including the structural and material effects. Therefore the 2D simulators were unable to provide an accurate result as the 3D models.

There is a need to combine the benefits of the two and extended the multiple driving forces based 3D EM model to the circuit layout level. The development of the complete 3D circuit modeling is necessary.

CHAPTER 3 3D CIRCUIT MODEL CONSTRUCTION AND SIMULATION

3.1 Introduction

As delineated in Chapter 1 and 2, there is a need to model the EM reliability of the interconnects using 3D model at the circuit layout level. In this chapter, a method for the complete 3D circuit model construction and the transient electro-thermo-structural simulations for the EM reliability assessment of an IC are introduced.

Power and ground rails used to be the major concerns for the EM failure of the circuit due to the large, unidirectional currents in these lines. As the technology node goes down to 65 nm and below, the EM effects become significant on signal wires and even in the logic cells themselves [17]. To evaluate the EM reliability of the circuit, we should look at both the power and the signal wires, and both the global and the local interconnects.

To show a step by step approach, the modeling is first carried out on a small circuit with two transistors, and only the transistor region (i.e. a simplified circuit structure that only includes the local interconnects with two metal levels) is focused. The extension to the real circuit structure with the inclusion of other circuit components

and the global interconnects up to the metal top will be discussed in detail in Chapter 5.

This chapter is organized in the following manner. In Section 3.2, the construction of the 3D finite element circuit model from its 2D IC layout is presented. The substrate, passivation and packaging layers are included in the model to represent the realistic chip structure. In Section 3.3, the setup for the transient electro-thermo-structural simulations using the current and voltage waveforms extracted from the circuit design tool is introduced. The total AFD in the interconnects are computed based on the current density, the temperature gradient and the thermo-mechanical stress gradient obtained from the electro-thermo-structural simulations on the 3D finite element circuit model, and the results obtained are discussed in Section 3.4. In Section 3.5, the effects of the barrier layer thickness and the dielectric material are investigated so as to demonstrate the structural and material modeling capability of the proposed model. Finally, conclusions are given in Section 3.6.

3.2 Layout Extraction and 3D Model Construction

CMOS inverter is a basic building block in digital circuits [79]. Clock drivers made of inverter trees are prone to EM failure due to the large current demand on every cycle. To reduce the complexity of the illustration of the EM reliability of the

interconnects study using the 3D circuit model, a simple two-transistor inverter circuit as shown in Fig. 3.1(a) is used as an example. The circuit layout is drawn in Cadence using the 0.18 μm technology based on the standard cell design of Global Foundry, as shown in Fig. 3.1(b). The sizes of the PMOS and NMOS are kept small so as to reduce the size of the 3D model that is going to be built. The 0.18 μm technology is chosen because the technology file is readily available and it will also be easier for the subsequent experimental verification as the process technology is mature. Unnecessary unknown reliability issues can be avoided during the experimentation. The circuit designs using other technologies can also be used for the 3D model construction with the same method introduced here.

Fig. 3.1. (a) The schematic and (b) the layout of a simple inverter circuit.

The Cadence GDSII file is first converted layer by layer into an ANSYS compatible SAT or ANS file using third party software (e.g. LinkCAD). The thicknesses of

each layer are specified during the conversion. The converted layers are combined and a 3D model is built as shown in Fig. 3.2.

Fig. 3.2. (a) The front (b) the isometric and (c) the tilted view of the 3D inverter circuit model.

As we are studying the EM reliability of the interconnects, the transistors are assumed to be reliable. When the circuit is under operation, the current flowing in the interconnects causes Joule heating and affects the temperature of the circuit, especially when the current spikes occur during switching. The focus of attention, the interconnect layers, together with the heat sources which are the transistor diffusion regions, are extracted and imported into ANSYS WORKBENCH. As the layout tool provides only the basic interconnection structures, the Ta barrier layer of 25 nm and the SiN cap layer of 50 nm [77] are added around the interconnects, as shown in Fig. 3.3.

Fig. 3.3. The side view of the interconnects under study showing the barrier and the cap layer.

After importing the essential structures, additional layers that are present in the chip, such as the Si substrate, the inter-level dielectric (ILD), the passivation and the packaging materials such as the plastic encapsulant, the adhesive die attach and the die pad as shown in Fig. 3.4 are added to the model, so as to represent the realistic chip condition.

Fig. 3.4. Illustration of the plastic encapsulation used in a microelectronic device [80].

To reduce the area effect on the circuit temperature as will be discussed in Section 3.4.3, the substrate and the encapsulation are drawn to be much larger than the size of the inverter circuit. The complete 3D model with a size of $1000\text{ }\mu\text{m} \times 1000\text{ }\mu\text{m} \times 400\text{ }\mu\text{m}$ (i.e. the size of a die) is shown in Fig. 3.5. The inverter circuit is

enclosed at the center just above the Si substrate. PS, PD, NS, and ND in Fig 3.5(a) denote the contacts at the PMOS source, PMOS drain, NMOS source, and NMOS drain respectively. The geometrical parameter, the properties of the materials used, and the variation of thermal conductivity with temperature for some of the materials are listed in Tables 1 to 3 respectively [80-84]. The thermal conductivity of the encapsulation is assumed to be temperature independent in this case as the test temperature is below its glass transition temperature which is usually taken as 260 °C [85].

Fig. 3.5. (a) The zoom-in view of the inverter circuit after removing the covered layers and (b) the global view of the 3D model showing different layers. The chip is modeled in a package with encapsulation and die attached to the leadframe represented by the metal plate shown in the figure.

Table 1. The geometry parameters of the model [81].

Feature	Size
Contact size	0.22 μm
Contact space	0.305 μm
Contact height	0.85 μm
Metal overlap contact	0.06 μm
Metal 1/Metal 2 width	0.34/0.42 μm
Metal 1/Metal 2 height	0.53 μm
Via 12 size	0.26 μm
Via 12 space	0.26 μm
Via 12 height	0.85 μm
PMOS diffusion region dimension (width $\times$ length)	$2.46 \times 1.46 \mu\text{m}^2$
NMOS diffusion region dimension (width $\times$ length)	$0.96 \times 1.46 \mu\text{m}^2$
Si substrate thickness	300 μm
Si substrate dimension (width $\times$ length)	$1000 \times 1000 \mu\text{m}^2$
Dielectric thickness	3.10 μm
Passivation thickness	3.25 μm
Die attach thickness	2 μm
Metal plate base thickness	100 μm
Encapsulation thickness	400 μm
Encapsulation dimension (width $\times$ length)	$1020 \times 1020 \mu\text{m}^2$
Barrier layer thickness	25 nm
Cap layer thickness	50 nm

Table 2. The material properties of the model [80, 82, 83].

Materials	Properties						
	Young's Modulus (MPa)	Poisson's Ratio	Density (kg/m ³)	Thermal Expansion (1/ $^{\circ}\text{C}$)	Thermal Conductivity (W/m $^{\circ}\text{C}$)	Specific Heat (J/kg $^{\circ}\text{C}$)	Resistivity (Ohm $\cdot\text{m}$)
Cu	1.10×10^5	0.34	8300	1.80×10^{-5}	403	385	1.72×10^{-8}
Si Substrate	1.30×10^5	0.28	2330	2.60×10^{-6}	149	700	1.00×10^{17}
As-doped Si							9.90×10^{-3}
B-doped Si							2.81×10^{-2}
Heavily doped Si							1.00×10^{-5}
SiO ₂	7.14×10^4	0.16	2200	6.80×10^{-7}	1.38	1000	1.00×10^{17}
SiN	2.20×10^5	0.27	3100	3.20×10^{-6}	30	700	1.00×10^{13}
Ta	1.86×10^5	0.34	16690	6.30×10^{-6}	57.50	140	1.31×10^{-7}
Polyimide	3100	0.33	1430	5.00×10^{-5}	0.18	1100	1.00×10^{15}
96% Alumina	276	0.25	3965	7.10×10^{-6}	20.90	779	1.00×10^{13}

Table 3. The temperature dependency of thermal conductivity for some materials [84].

Materials	Thermal Conductivity (W/m ² °C)					
	0 °C	27 °C	127 °C	227 °C	327 °C	427 °C
Cu	403	395	390	380	370	365
Si Substrate	149	148	99	76	62	51
SiO ₂	1.38	1.38	1.51	1.61	1.75	1.92

3.3 Transient Electro-thermo-structural Simulations and the AFD Computation

After the construction of the 3D finite element circuit model, the next step is to perform the EM analysis. The equations used in our model are based on the work by Dalleau *et al.* [12], and we extend their model from the line-via level to the circuit layout level. Different from the work in [12] and many in literature [86-88] which used DC analysis, the simulation of our 3D circuit model is performed under the transient condition so as to account for the possible temperature and stress effects due to the change in the magnitude and/or the direction of the current flow. Coupled thermal-electric and structural-thermal simulations are performed to calculate the AFDs in the interconnects due to different driving forces, and these values are used to evaluate the EM reliability of the interconnects.

3.3.1 Transient Thermal-Electric Analysis

The transient thermal-electric analysis is performed to study the effect of the electrical loads on the temperature and current density distributions. For an

accurate simulation, the boundary conditions and the electrical loads should be properly set.

3.3.1.1 Boundary Conditions

The running speed, the cooling method, and the operation modes of the transistors determine the temperature of an IC. The desktop processors usually run at a temperature between 70 °C to 90 °C [89]. In this work, a worst-case temperature of 90 °C is used to represent the interconnect heating in a chip under operation [90]. Other temperatures can be used depending on the application of the circuits. The metal base plate is treated as the heat sink since it has more than 100 times better thermal conductivity than the encapsulation material as can be seen in Table 2, and thus it is the major heat dissipation path for the model. A convection heat transfer coefficient h of 20 W/m²·°C [91] is used to simulate the 90 °C ambient condition. A constant h is used for simplicity as the convection has minor effect to the model temperature in this work as verified by our simulation where the model temperature is found to remain unchanged when the value of h varies from 10 W/m²·°C to 40 W/m²·°C. The boundary conditions of the thermal-electric simulation used in the model are shown in Fig. 3.6.

Fig. 3.6. The boundary conditions of the thermal-electric simulation, titled view from the back.

3.3.1.2 Electrical Loads

The instantaneous source and drain currents flowing in the interconnects, together with the voltages across the interconnects, are the causes of the heat up of the interconnects. These currents and voltages are treated as the electrical loads in the ANSYS thermal-electric simulation, and their values are determined from the circuit design tool, Cadence.

The power consumed in the inverter circuit includes the dynamic power due to the charging and discharging of the capacitors, and the short circuit power due to the direct current flow from the power source to the ground during switching when both transistors are on [92]. The diode leakage power is assumed to be negligible and is ignored in this simulation. To simulate the power consumption in the inverter, both

the charging and discharging currents and the short circuit current should be considered.

When PMOS is on, the path of the current flow is from the V_{dd} line to the source of PMOS, and then from the drain of PMOS to the output line. For the NMOS-on condition, the current flows from the output line through the NMOS to the ground. The current flow paths and the name of the four current sources are listed below:

- (1). the current flow from the V_{dd} line to the source of PMOS: I_{ps} ,
- (2). the current flow from the drain of PMOS to the output line: I_{pd} ,
- (3). the current flow from the output line to the drain of NMOS: I_{nd} ,
- (4). the current flow from the source of NMOS to the ground: I_{ns} .

The above charging and discharging currents are represented by the gradual increase or decrease of the current waveforms. The short circuit currents are represented by the current spikes during switching and they quickly drop to zero after switching. The currents in the gates of the two transistors are assumed to be negligible.

The root-mean-square (RMS) current density is usually used in the EM simulations performed under DC or low frequency pulsed DC condition. The study in [93] showed that, the steady-state simulation using the RMS current density of 1.5 MA/cm² gives a small temperature difference of around 4% as compared with the

transient simulation using an unipolar pulsed DC load at 1 MHz. With a pulsed DC load, EM occurs during the switch-on (i.e. DC) period and nothing or stress relaxation may occur during the switch-off (i.e. no current flow) period [4]. At low frequency of no more than 1 MHz, the metal line can respond thermally to the pulses and thus has a higher temperature during the switch-on period than during the switch-off period. Relaxation of the EM induced stress does not occur during the switch-off period as the temperature of the metal line is low. Therefore the RMS values can be used in the low frequency regime. However, at higher frequencies, the switching speed is faster than the thermal response time of a typical thin-film conductor (i.e. a few μs), stress relaxation occurs as the metallization cannot respond thermally to the pulses [94]. The stress relaxation during the switch-off period results in an enhanced EM lifetime and this effect is overlooked if the RMS value is used. Under an AC operation condition, besides the stress relaxation effect at high frequency, the bi-directional current (e.g. at the output line of the inverter) further affect the stress state in the metal line. It is found in [95] that the EM damage by the positive (forward) current stress can be partially healed by the following negative (reverse) current stress. Therefore it is not suitable to use the RMS values under the AC condition with a frequency higher than 1 MHz.

In our simulations, in order to account for the possible stress effects, the instantaneous electrical loads under the AC operation condition are used instead of the RMS values. The voltage and current pulses at selected circuit nodes (i.e. the

source and drain of the two transistors, the V_{dd} and ground lines, the input and output lines) are extracted from Cadence, including both the charging and discharging currents and the current spikes during switching. These current and voltage values are used as the inputs to the 3D circuit model in ANSYS.

In the delay analysis of the CMOS inverter driving a RC load in [96], the load resistance varies from 10 Ω to 1 k Ω , and the load capacitance is in the range of 0.01 pF to 1 pF. Here an extreme case of 1 k Ω and 1 pF under an operation frequency of 100 MHz is used as an example. Here a large load and a low frequency are used so that the power consumption of the circuit is larger and the temperature change within one operation cycle is more obvious. Furthermore, the difference between the temperature responses to the rapid current change (e.g. current spike) and the gradual current change (e.g. slow charging or discharging) can be clearer. This non-typical condition is for the validation of the 3D model construction and simulation. Other typical loading and operating frequencies can be used in case of the application in a real circuit under the realistic circuit operation condition.

When high frequency AC current flows in a conductor, it tends to redistribute itself within a conductor with the current density being largest near the surface of the conductor, and decreasing at greater depths. The electric current concentrates at the “skin” of the conductor and this phenomenon is called the “skin effect”. The

depth at which the current density has fallen to $\exp^{-1}$ (about 0.37) of its original value at the conductor surface is called the “skin depth” and is calculated as [97],

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (3.1)$$

where

δ is the skin depth,

ω is the angular frequency of current ($2\pi \times$ frequency), and

μ is the absolute magnetic permeability of the conductor.

When the skin effect occurs, the effective cross-section of the conductor decrease and its effective resistance increases, especially at higher frequencies where the skin depth is smaller. The increase in the effective resistance of the conductor increases the Joule heating ($Q=I^2R$) and hence enhance EM. The increased current density at the surface further increases the surface temperature and aggravates the EM process.

At the operating frequency of 100 MHz in this case, the skin depth calculated based on Eqn. (3.1) is 6.60 μm and is larger than the thicknesses of Metal 1 (0.53 μm), Metal 2 (0.53 μm), Via 12 (0.85 μm), and the contacts (0.75 μm), and the skin effect is ignored in this model.

The electrical loads of the inverter circuit within one load cycle (i.e. one period of 10 ns) under the condition specified above are shown in Fig. 3.7. We can see that

the PMOS source and drain current waveforms show the same pattern but in opposite direction. The same trend is observed for the NMOS current waveforms. The output voltage does not switch instantaneously with the input voltage due to the presence of the RC load. The threshold voltage V_t of the PMOS and NMOS are -0.495 V and 0.482 V respectively, which are obtained from cadence.

(a)

(b)

Fig. 3.7. The electrical loads of the inverter circuit within one load cycle (10 ns) showing (a) the PMOS source and drain currents (b) the NMOS source and drain currents and (c) the input and output voltages.

As it is not possible to include all the thousands of data points in Fig. 3.7 into the 3D circuit simulation, the data should be simplified. The electrical loads within one load cycle can be divided into four stages: the first switching stage, the first operation/off stage, the second switching stage, and the second operation/off stage. These four stages are called Stage 1, 2, 3, and 4 respectively. For I_{ps} and I_{pd} , there is an only-rise/fall current spike at Stage 1, a gradual current change waveform (i.e. transistor in operation, slow charging of the capacitor) at Stage 2, a rise-and-fall current spike at Stage 3, and a constant current waveform (i.e. transistor is off, almost zero current) at Stage 4. For I_{ns} and I_{nd} , there is a rise-and-fall current spike at Stage 1, a constant current waveform (i.e. transistor is off, almost zero current) at Stage 2, an only-rise/fall current spike at Stage 3, and a gradual current change waveform (i.e. transistor in operation, slow discharging of the capacitor) at

Stage 4. For V_{in} , there is an only-rise/fall voltage spike at Stage 1 and 3, and a constant voltage waveform at Stage 2 and 4. For V_{out} , there is a gradual voltage increase waveform at Stage 1 and 2, and a gradual voltage decrease waveform at Stage 3 and 4.

The selection of data points depends on the shape of the current and voltage waveforms used in the simulation. For example, we should select more data points at the region with more significant and/or irregular changes. More data points should be chosen if particular accuracy is required at a specific time interval.

In this case, the gradual current or voltage change waveforms need around 5 data points to represent their shapes. The number of data points selected can be changed depending on the accuracy requirement and the PC computation capability. Here 5 points are used so that there can be a gradual change in current or voltage at around 1 ns interval. The only-rise/fall current or voltage spikes need 5 data points: 1 at the beginning, 1 at the peak, 3 on the rise/fall slope. The rise-and-fall current spikes need 8 data points: 1 at the beginning, 1 at the peak, 3 on the rise-slope and 3 on the fall-slope. The constant current or voltage waveforms need only 2 data points: 1 at the beginning and 1 at the end. As the current and voltage waveforms occur simultaneously, there are 6 waveforms with different shapes in each stage. When the waveforms within the same stage have

different shapes, the number of data points selected is determined by the waveform that needs more points to represent its shape.

At Stage 1, the only-rise/fall current spikes for I_{ps} and I_{pd} need 5 data points; the rise-and-fall current spikes for I_{ns} and I_{nd} need 8 data points; the voltage spike for V_{in} need 5 data points; and the gradual voltage increase waveform for V_{out} need 5 data points. Therefore 8 data points are selected at Stage 1. At Stage 2, the gradual current change waveforms for I_{ps} and I_{pd} need 5 data points; the constant current waveforms for I_{ns} and I_{nd} and the constant voltage waveform for V_{in} need 2 data points; and the gradual voltage increase waveform for V_{out} need 5 data points. Therefore 5 data points are selected at Stage 2. At Stage 3, the rise-and-fall current spikes for I_{ps} and I_{pd} need 8 data points; the only-rise/fall current spikes for I_{ns} and I_{nd} need 5 data points; the voltage spike for V_{in} need 5 data points; and the gradual voltage decrease waveform for V_{out} need 5 data points. Therefore 8 data points are selected at Stage 3. At Stage 4, the constant current waveforms for I_{ps} and I_{pd} need 2 data points; the gradual current change waveforms for I_{ns} and I_{nd} need 5 data points; the constant voltage waveform for V_{in} need 2 data points; and the gradual voltage decrease waveform for V_{out} need 5 data points. Therefore 5 data points are selected at Stage 4.

The data point selection at Stages 1 and 4 for I_{nd} and Stage 2 and 3 for I_{ps} is shown in Fig. 3.8. The time scale at Stage 1 and 3 (i.e. the current spike stages) in Fig.

3.8 are exaggerated for better illustration purpose. The data point selection for all the current and voltage waveforms at the four stages is summarized in Table 4.

Fig. 3.8. Data point selection at different stages (I_{nd} and I_{ps}), not to scale.

Table 4. The current and voltage waveforms and the data point selection at different stages. The number in the bracket is the data points selected at this stage for this waveform.

	Current waveforms		Voltage waveforms		Data points
	I_{ps} and I_{pd}	I_{ns} and I_{nd}	V_{in}	V_{out}	
Stage 1	only-rise/fall spike (5)	rise-and-fall spike (8)	only-fall spike (5)	gradual increase (5)	8
Stage 2	gradual change (5)	constant (2)	constant (2)	gradual increase (5)	5
Stage 3	rise-and-fall spike (8)	only-rise/fall spike (5)	only-rise spike (5)	gradual decrease (5)	8
Stage 4	constant (2)	gradual change (5)	constant (2)	gradual decrease (5)	5

In total, 26 data points are selected to present the shapes of the current and voltage waveforms in Fig. 3.7. The simplified current and voltage waveforms within one load cycle are shown in Fig. 3.9. Each data point corresponds to one load step in the ANSYS simulation. The instantaneous voltage and current inputs used in ANSYS within one load cycle are shown in Appendix A. A do-loop is used to repeat the 26 load steps for multiple cycles to represent a continuous circuit operation.

(a)

(b)

(c)

Fig. 3.9. The simplified electrical loads of the inverter circuit within one load cycle (10 ns) showing (a) the PMOS source and drain currents (b) the NMOS source and drain currents and (c) the input and output voltage s.

3.3.1.3 Application of the Electrical Loads

The locations for applying the current and voltage loads in the 3D circuit model correspond to the data extraction nodes in Cadence, and they are shown in Fig. 3.10.

(a)

(b)

Fig. 3.10. Application of the current and voltage inputs to the 3D circuit model in ANSYS. (a) The isometric and (b) the tilted view showing the current flow direction during circuit operation.

After the application of the boundary conditions and the electrical loads, the transient thermal-electric simulation is performed and the results are discussed in Section 3.4.1 and 3.4.2.

3.3.2 Transient Structural-Thermal Analysis

Besides the intrinsic stress that is already present at the beginning of the simulation, when the current and voltage loads are applied to the model, there is a difference in the interconnect temperature at different locations, and the thermal mismatch between the materials in an interconnect structure causes thermally induced thermo-mechanical stress. The transient structural-thermal analysis is needed to study the thermo-mechanical stress distribution in the interconnects.

3.3.2.1 *Boundary Conditions*

All the nodes on the base surface of the model are assumed to be fixed as they are mounted on the circuit board. The stress free temperature (SFT) of the Cu DD structure is usually between 350 °C to 400 °C [98, 99], depending on the final annealing temperature of the sample. In this work, a SFT of 350 °C is used.

3.3.2.2 *Thermal Loads*

The temperatures of all the nodes of the model at each load step are retrieved from the results of the transient thermal-electric simulation. These temperature values,

together with the time of their occurrence, are used as the thermal loads in the transient structural-thermal simulation.

After the application of the boundary conditions and the thermal load, the transient structural-thermal simulation is performed and the results are discussed in Section 3.4.4.

3.3.3 Application of Submodeling

A fine mesh is critical in achieving an accurate simulation result. The original full model is too large and thus very time and resource consuming for the transient analysis if a fine mesh is applied to the entire model. As a result, submodeling is used in this simulation.

Submodeling, also known as cut-boundary displacement method or specified boundary displacement method, cuts through the global model. A fine mesh is done at the “cut out” region, while the global model can be meshed much coarser. Mesh refinement is achieved at the cut out sub-model region and thus we are able to obtain an accurate simulation result and at the same time eliminate the redundant effort on solving the region that is not the focus of attention. The main disadvantage of the submodeling method is that the simulation needs to be performed twice, first for the global model and then for the sub-model, and thus complicated the process.

When submodeling is applied, a cut boundary (i.e. the boundary that cuts through the coarse model) is specified, the displacement and/or the temperature results extracted from the cut boundary of the coarse model are applied as the boundary conditions of the sub-model. According to St. Venant's principle [100], if an actual distribution of forces is replaced by a statically equivalent system, the distribution of the stress and strain is changed only near the regions of load application. This implies that, acceptable results can be obtained in the sub-model if the cut boundaries of the sub-model are adequately far away from the stress concentration, in view of the fact that the stress concentration effects are localized around the concentration site [101].

A simple steady-state simulation is carried out on the full model to determine where the cut boundary should be, i.e. the size of the sub-model. With the same setup for the boundary conditions in Section 3.3.1.1, the first current spike is used as the input for the simulation. This current spike is used because it is one of the worst-case values which can result in a higher temperature than that using the normal operation current in the circuit. The resultant worst-case temperature is enough for determining the cut boundary location.

From Fig. 3.11, it can be seen that the temperature is almost constant at around 5 μm away from the model center in the x direction and 10 μm in the y direction, as indicated by the rectangular box. Hence it is acceptable to place the cut boundary

there. A $10\text{ }\mu\text{m}\times 20\text{ }\mu\text{m}\times 15\text{ }\mu\text{m}$ sub-model centered with the inverter circuit is cut out from the original $1000\text{ }\mu\text{m}\times 1000\text{ }\mu\text{m}\times 400\text{ }\mu\text{m}$ full model as shown in Fig. 3.12.

Fig. 3.11. The front view of the steady-state temperature distribution of the full model using the worst-case current. The box indicates the margin where the temperature becomes almost constant.

Fig. 3.12. The cut out of the sub-model (left) from the full model (right).

The complexity of the model limits the application of the hexahedral mesh. Wang *et al.* showed that the quadratic tetrahedral shaped element can produce as accurate result as the linear hexahedral element [102], and hence a quadratic tetrahedral mesh using 20-node coupled-field solid element SOLID98 is used in this work. The quadratic tetrahedral mesh is applied to both the full model and the sub-model. A fine mesh with a size of 0.50 μm is used for the interconnects in the full model, and an even finer mesh is used in the sub-model. A transient analysis using the electrical loads in Appendix A is conducted to determine the mesh size to be used in the sub-model and the simulation results at the end of one load cycle (i.e. 10 ns) are shown in Fig. 3.13.

Fig. 3.13. The temperature and thermo-mechanical stress variation with mesh size, convergence achieves at 0.20 μm .

From Fig. 3.13, it is clear that a local fine mesh of $0.20\ \mu\text{m}$ is adequate as the temperature and the stress curves both converge (i.e. the curve becomes flat) at $0.20\ \mu\text{m}$. Similarly, the barrier layer can be meshed at $0.10\ \mu\text{m}$ without the loss of accuracy. The coarse mesh for the full model and fine mesh for the sub-model is shown in Fig. 3.14.

Fig. 3.14. The tetrahedral mesh at the interconnect region showing (a) the coarse mesh for the full model and (b) the fine mesh for the sub-model.

The outer surfaces of the sub-model are treated as the cut boundary. According to the transient submodeling analysis technique introduced by Wang *et al.* [103], the simulation results of the full model at each load step are recorded, and the solution of the first load step is retrieved and applied to the cut boundary of the sub-model as the boundary conditions. The sub-model is then solved with the current and the voltage loads and the applied boundary conditions for the first load step. This is repeated for the remaining load steps.

After the setup for the size and the mesh of the sub-model, the transient thermal-electric and structural-thermal simulations are repeated for the sub-model. The distributions of the current density, temperature, and thermo-mechanical stress of the interconnects can be obtained from the simulation results, and these values are used to calculate the AFDs in the interconnects.

3.3.4 Computation of the Atomic Flux Divergences

To compute the AFDs in the interconnects, the thermal-electric simulation is first carried out using the boundary conditions and the electrical loads as shown in Section 3.3.1.1 and 3.3.1.2. The nodal temperatures extracted from the thermal-electric simulation are used as the thermal loads for the structural-thermal simulation. The structural-thermal simulation is performed based on these thermal loads and the boundary conditions in Section 3.3.2.1. Submodeling technique is used in both the thermal-electric and the structural-thermal simulation. The thermo-mechanical stress gradient of the model is calculated based on the thermo-mechanical stresses extracted from the structural-thermal simulation. The thermo-mechanical stress gradient, together with the current density, temperature, and temperature gradient extracted from the thermal-electric simulation, are used to compute the atomic fluxes and the flux divergences due to electron wind force, temperature gradient induced driving force, and thermo-mechanical stress gradient induced driving force, using Eqn. (2.22) to (2.27). The flowchart for the

computation of the AFDs in ANSYS is shown in Fig. 3.15. The total AFD in the interconnects is the sum of the three AFDs from their respective driving forces and the results obtained are discussed in Section 3.4.5.

Fig. 3.15. The flowchart for the computation of the atomic flux divergences.

The simulations are carried out using an Intel Quad core computer (Q9400@ 2.66 GHz) with 4G RAM. The computation time and result file size of each transient simulation for one load cycle (10 ns, 26 load steps) are listed in Table 5. It can be seen from the listed values that the overall simulation takes about 6 hours running time and the result file is nearly 26 GB.

Table 5. The computation time and result file size of each transient simulation for one load cycle.

Simulation	Computation time (min)	Result file size (GB)
Thermal-electric	70	9.81
Structural-thermal	156	9.52
Thermo-mechanical stress extraction & AFD Analysis	144	6.60
Total	370	25.93

Due to the complexity of the problem and the constraint of the time and resource, the current simulation is focusing on the void nucleation location instead of the dynamics of void growth. This is justifiable due to the following two reasons. Firstly, recent simulation and experimental results by Li *et al.* in [23] showed that the void nucleation time occupies the largest portion of the EM lifetime, and thus reducing the void nucleation time can effectively enhance the EM lifetime. Secondly, it is always important to identify the weakest site or the damage nucleation site so that one can strengthen these sites for the “design-in” reliability of a device or system. Also, the microstructure and back stress effects of the interconnects are not considered in this initial attempt due to the time and resource constraint. However, as they will affect the void nucleation sites, their effects will be considered in the future when the computational efficiency is improved.

In summary, this section presents the setup of the boundary conditions and the application of the electrical and thermal loads for the electro-thermo-structural simulations. The application of the submodeling technique for better accuracy is discussed as well. The distributions of the current density, temperature and temperature gradient, thermo-mechanical stress and stress gradient of the interconnects can be obtained from the electro-thermo-structural simulations and they are used to compute the AFDs in the interconnects. The results obtained are discussed in the next section.

3.4 Results and Discussions

3.4.1 Current Density and Temperature Distributions

The current density and temperature distributions of the 3D model at any load step can be viewed after the thermal-electric simulation.

Figures 3.16 and 3.17 show the temperature and the current density distributions of the interconnects of the inverter model under study after one and ten load cycles (i.e. 10 ns and 100 ns) respectively. The figures on the right of Fig. 3.16(a) are the zoom-in views at the PMOS and NMOS contact regions. Depending on the operation condition of the transistor, the current density values at the PMOS or NMOS contact regions may be quite different from that with all the interconnect structures (e.g. the values are lower during the switch-off period and higher during the switch-on period, and the range is generally smaller due to current crowding at those regions). It will be hard to differentiate the higher value regions from the lower value regions by color in the zoom-in views if the global contour of the inverter model is used. For a better illustration, the zoom-in views are done using their own contours and SMX and SMN shown on the top right hand side of the zoom-in views are their respective maximum and minimum values.

Fig. 3.16. The distributions of (a) current density (unit: $\text{pA}/\mu\text{m}^2$) and (b) temperature (unit: $^{\circ}\text{C}$) of the interconnects at the end of one load cycle (i.e. 10 ns).

AVG ELEMENT SOLUTION

STEP=260

SUB =1

TIME=.100E-06

E_J (AVG)

SMN =.218E-09

SMX =.132E+10

(a)

NODAL SOLUTION

STEP=260

SUB =1

TIME=.100E-06

TEMP (AVG)

RSYS=0

SMN =90.002

SMX =90.34

(b)

Fig. 3.17. The distributions of (a) current density (unit: $\text{pA}/\mu\text{m}^2$) and (b) temperature (unit: $^{\circ}\text{C}$) of the interconnects at the end of ten load cycles (i.e. 100 ns).

It is found that the current density distributions after 10 ns and 100 ns are similar because the same current pulses are applied to the model. Higher current density (i.e. the red and orange regions in the zoom-in views of Fig. 3.16(a)) is found at the Via 12/Metal 1 interfaces due to current crowding. The location of the maximum current density depends on the direction of the current flow. For example, the highest current density at the PMOS region is found at the upper corners of the upper most contact at the PMOS source region as the current is flowing from the V_{dd} line to the PMOS source, while it is found at the lower corners of the lowest contact at the PMOS drain region as the current is flowing from the PMOS drain to the output line, as indicated by the black arrows in Fig 3.16(a). For the NMOS contacts, the maximum current densities are at the lower corners of the source contact and the upper corners of the drain contact, as indicated by the red arrows.

For the temperature distribution, higher temperature is found at the interconnect contact regions as they are nearer to the heat sources, i.e. the diffusion regions. This result is as expected as the power consumption of the transistors is large due to the large load the transistors are driving. At the end of one load cycle, NMOS is on and PMOS is off, the temperature at the NMOS contacts at this instant is higher than that at the PMOS contacts (i.e. the light blue region for the PMOS contacts as compared with the green to red regions for the NMOS contacts as shown in Fig. 3.16(b)). The maximum temperature of the NMOS and PMOS contacts are 90.29 °C and 90.05 °C respectively. As time progresses, the

temperatures at the diffusion regions increase, and this renders an increase in the interconnect temperature, gradually from the contact regions to the upper Metal 1, Via 12 and Metal 2 layers, as showing by the increase in area of the light blue regions in Fig 3.17(b). The location of the maximum temperature remains unchanged.

In the case of the inverter trees with hundreds or thousands of inverters working together, the circuit temperature is expected to be higher due to the interaction of the inverters with each other. The problem is even worse when the loads and the activities of the inverter trees are heavier (e.g. with more fan outs and/or at higher operating frequencies). The increase in temperature increases the total AFD in the interconnects.

3.4.2 Transient Temperature Variation During Circuit Operation

The transient temperature curve at various locations of the model can be plotted from the extracted results of the thermal-electric simulation. Fig. 3.18 shows the temperature change with time within one load cycle at the interconnect contact regions.

From Fig. 3.18, it is observed that the temperatures of the PMOS contacts gradually increase from time 0 to 5 ns (i.e. when V_{in} is at 0 V and PMOS is on). A slight increase in the temperatures of the NMOS contacts at the beginning is due to the

current spike occurred during switching. The temperatures of the NMOS contacts drop slowly thereafter, but they do not drop to their initial values.

From 5 to 10 ns, NMOS turns on and PMOS turns off. The temperatures of the PMOS contacts gradually decrease due to heat loss to the surrounding, and they also do not fall back to their initial values. The temperatures of the NMOS contacts start to increase at 5 ns when NMOS begins to operate.

Fig. 3.18. The temperature change with time at the interconnect contact regions within one load cycle.

The increase in temperature for the NMOS contacts (around 0.29 °C) when NMOS is on is higher than that for the PMOS contacts (around 0.11 °C) when PMOS is on. This is as expected because the size of PMOS in this design is around 2.56 times larger than that of NMOS so as to achieve a symmetric characteristic (i.e. equal rise and fall time at the output). The number of contacts that can be placed at the PMOS

region (four pairs) is larger than that at the NMOS region (one pair). With the same current loads, the average current density of the NMOS contacts is higher than that of the PMOS contacts during their respective switch-on period, and thus a higher temperature rise for the NMOS contacts.

For a continuous circuit operation, the temperature variation at the interconnect contact regions shows a zig-zag shape corresponds to the turning on and off of the transistors. A general increasing trend in temperature is observed as shown in Fig. 3.19, which is also in agreement with the simulation result of Alam *et al.* [22].

Fig. 3.19. The temperature change with time at the interconnect contact regions for multiple load cycles. A general increasing trend in temperature is observed.

Based on Fig. 3.19, the final temperature of the interconnect contact can be obtained through extrapolation using the curve fitting method. The extrapolated curve for

the contact at NMOS drain is shown in Fig. 3.20. The final temperature is assumed as the temperature at time tends to be infinity, which is 106.90 °C in this case.

Fig. 3.20. The temperature extrapolation for the contact at NMOS drain.

3.4.3 Effect of the Substrate Dimension on the Circuit Temperature

It is expected that the substrate dimension (length $\times$ width) can affect the heat dissipation and the circuit temperature. Its effect is studied in this work. Keeping all other parameters the same, six models with different substrate areas varying from 20 $\mu\text{m} \times 20 \mu\text{m}$ to 1000 $\mu\text{m} \times 1000 \mu\text{m}$ with the substrate thickness fixed at 300 μm are simulated under the same operation condition, and the results are shown in Fig. 3.21. As the convection of the chip surface to the surrounding has minor impact on the circuit temperature as already explained in Section 3.3.1.1, a lower final steady-state temperature is observed for models with larger substrate areas due to their larger conduction areas at the heat sink, the metal base plate. The rise in the

final circuit temperature is small when the substrate dimension decrease from 1000 $\mu\text{m} \times 1000 \mu\text{m}$ to 200 $\mu\text{m} \times 200 \mu\text{m}$. A very rapid increase in temperature is observed when the dimension of the substrate area is smaller than 200 $\mu\text{m} \times 200 \mu\text{m}$, showing that the rate of heat lost to the surrounding through the small area is not enough to cater for the rate of increase in temperature of the circuit.

Fig. 3.21. The final circuit temperature of the 3D inverter model with different substrate dimension. The substrate thicknesses of the models are fixed at 300 μm .

The above results further emphasizes the necessity of the complete 3D circuit model with the consideration of the size of the surrounding materials as in the actual physical implementation of the circuit.

3.4.4 Transient Thermo-mechanical Stress Variation During Circuit Operation

The time evolution of the thermo-mechanical stress at any location of the model can be plotted from the results of the transient structural-thermal simulation of the 3D model, as shown in Fig. 3.22. The thermo-mechanical stress distribution of the interconnects at the end of one load cycle (10 ns) is shown in Fig. 3.23.

Intrinsic stress is present at the beginning of the simulation due to the thermal expansion mismatch between the metallization and its surrounding materials when the metallization is cooled down from the process temperature (i.e. SFT) to the circuit operation temperature. The total thermo-mechanical stress in the interconnects is the resultant stress of the intrinsic stress and the stress due to the temperature difference in the interconnects caused by the thermal loads. The magnitude of the total thermo-mechanical stress depends on the difference between the SFT of the metallization and the interconnect temperature.

When the interconnect temperature increases and approaches the SFT, the total thermo-mechanical stress in the interconnects decreases and shows an inverse relationship with the interconnect temperature as can be seen in Fig. 3.22. The change in the total thermo-mechanical stress at the end of one load cycle is only around 0.56 MPa and is much smaller than the intrinsic stress (559.49 MPa at 90 °C). The small change in the thermo-mechanical stress is because the increase in temperature at the end of one load cycle is small (about 0.29 °C).

Fig. 3.22. Comparison of the temperature and thermo-mechanical stress profile of the interconnect contact at NMOS drain.

Fig. 3.23. The thermo-mechanical stress distribution (unit: MPa) of the interconnects at the end of one load cycle.

The temperature difference at different locations of the interconnects at the end of one load cycle is less than 0.29°C and thus the stress caused by the thermal loads is small, even at the location with the highest temperature rise (only 0.10% of the intrinsic stress). Therefore the thermo-mechanical stress shown in Fig. 3.23 is mainly due to the intrinsic stress in the interconnects, which is more than 50% higher at the corners (i.e. in contact with other materials) than in the center.

3.4.5 Distributions of the Atomic Flux Divergences

With the current density, temperature, temperature gradient and thermo-mechanical stress gradient obtained from the electro-thermo-structural simulations, the AFDs due to the three driving forces and the total AFD in the interconnects at a specific load step can be obtained.

Fig. 3.24 shows the total AFD distribution of the interconnects at the end of one load cycle. The AFD distributions due to electron wind force, temperature gradient induced driving force and thermo-mechanical stress gradient induced driving force are shown in Fig. 3.25(a), (b), and (c) respectively.

Fig. 3.24. The total AFD distribution (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$) of the interconnects at the end of one load cycle. The figures on the right are the zoom-in views of the interconnect contacts at the PMOS and NMOS regions.

(a)

(b)

(c)

Fig. 3.25. The AFD distributions of the interconnects due to (a) electron wind force (b) temperature gradient induced driving force and (c) thermo-mechanical stress gradient induced driving force (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$) at the end of one load cycle. The figures on the right are the zoom-in views of the interconnect contacts at the PMOS and NMOS regions.

With recent process improvement on the use of metal cap on Cu interconnects, one can assume a strong Cu/cap layer interface [104], and the void nucleation location (i.e. the EM weak spot) is found at the contact or via bottom as determined by the location of the maximum total AFD [105]. At the end of one load cycle, the maximum AFD location is found at the bottom of the NMOS contacts as indicated by the arrows in Fig. 3.24, which is consistent with the work by Tan *et al.* [106] and Li *et al.* [23].

Comparing Fig. 3.16(a), 3.24 and 3.25(a), it is clear that the total AFD distribution is very different from the current density distribution and the AFD due to electron wind force (AFD_EWF) is not the main factor that determines the total AFD in the interconnects. The AFD_EWF is 1 and 3 orders of magnitude smaller than the AFD due to temperature gradient induced driving force (AFD_T) and thermo-mechanical stress gradient induced driving force (AFD_S) respectively. In fact, the AFD_S has over 98% contribution to the total AFD and the total AFD distribution of the model actually follows the distribution of the AFD_S. In other words, if only current density is considered, the EM weak spot will be different from that if all the driving forces are considered.

From Eqn. (2.25), we can see that the AFD_EWF depends on the product of the current density and the temperature gradient of the interconnects. For the PMOS contacts, the locations of the maximum current density are the same as the

maximum temperature gradient, as indicated by the black arrows in Fig. 3.16(a) and Fig. 3.26. The locations of the maximum AFD_EWF for the PMOS contacts are found at the upper corners of the upper most contact at the source region and the lower corners of the lowest contact at the drain region, as indicated by the black arrows in Fig. 3.25(a). For the NMOS contacts, the maximum current densities are at the top of the contacts as indicated by the red arrows in Fig. 3.16(a), while the maximum temperature gradients are at the bottom of the contacts as indicated by the red arrows in Fig. 3.26. The temperature gradient at the bottom of the contacts is more than 10 times higher than that at the top while the current density at the top is only less than 2 times higher than that at the bottom. Therefore the locations of the maximum AFD_EWF are found at the bottom of the NMOS contacts, as indicated by the red arrows in Fig. 3.25(a).

The maximum AFD due to AFD_T at the interconnect contact region is negative in value as shown in Fig. 3.25(b). This is because at the locations with high temperature gradient and comparably small current density (e.g. the blue regions in the zoom-in views of Fig. 3.16(a) and the red to yellow regions in the zoom-in views of Fig. 3.26), term 1 in Eqn. (2.26) is negative due to its negative coefficient. It dominates over term 2 and results in a negative AFD_T (i.e. the blue to orange regions in the zoom-in views of Fig. 3.25(b)). At the region with low temperature gradient (e.g. the blue regions in the zoom-in views and blue regions in the global view of Fig. 3.26), term 2 dominates and a positive AFD_T is obtained.

Fig. 3.26. The temperature gradient distribution of the interconnects (unit: $^{\circ}\text{C}/\mu\text{m}$) at the end of one load cycle. The figures on the right are the zoom-in views of the interconnect contacts at the PMOS and NMOS regions.

Fig. 3.27. The thermo-mechanical stress gradient distribution (unit: $\text{MPa}/\mu\text{m}$) of the interconnects at the end of one load cycle. The figures on the right are the zoom-in views of the interconnect contacts at the PMOS and NMOS regions.

From Eqn. (2.27), term 1 dominates over term 2 and term 3 at 90 °C and the AFD_S depends on the product of the temperature gradient and the thermo-mechanical stress gradient. The thermo-mechanical stress gradient distribution of the interconnects is shown in Fig. 3.27. This stress gradient is mainly caused by the intrinsic stress in the interconnects. Similar distributions are found for the PMOS and NMOS contacts as they have similar intrinsic stresses. The values of the stress gradient at the two regions are also similar. At the regions where the temperature gradient are less than 0.06 °C/μm (e.g. PMOS contacts, Metal 1, Via 12 and Metal 2), the distribution of the AFD_S follows the distribution of the thermo-mechanical stress gradient in the interconnect. At the regions with comparably large temperature gradient (e.g. the bottom of the NMOS contact), the AFD_S distribution follows the temperature gradient distribution. Therefore, to reduce the AFD_S and hence the total AFD of the model, one can reduce the thermo-mechanical stress gradient and the temperature gradient. This will be studied in Section 5.4.

At the beginning of the circuit operation, the temperature and the resultant thermo-mechanical stress gradient are changing with time due to the variation in the electrical and thermal loads. The total AFD of the interconnects also changes with time as a result of the changing temperature gradient and thermo-mechanical stress gradient. However, as time progresses, the circuit temperature and temperature gradient become constant and are found to be highest at the bottom of the NMOS

contacts (i.e. the same locations as in Fig.3.16(b) and 3.26 but with a higher value).

Therefore we can conclude that the maximum total AFD location at the end of one load cycle is the final maximum total AFD location.

In summary, the simulation results in this section show the transient temperature response to the changes in the electrical loads and the transient thermo-mechanical stress response to the changes in the circuit temperature. This demonstrates the ability of the proposed 3D model for performing the transient temperature and stress analysis at the circuit layout level. The distributions of the AFDs are discussed based on the current density, temperature gradient, and thermo-mechanical stress gradient distributions of the interconnects. The void nucleation location and hence the EM weak spot is found at the location with the highest total AFD, which is at the bottom of the NMOS contact for the inverter model under study. It is also found that the electron wind force is no longer the sole driving force for EM as the value and the distribution of the total AFD of the 3D circuit model are determined by the AFD_S. To reduce the AFD_S and hence the total AFD, the thermo-mechanical stress gradient and the temperature gradient of the circuit should be reduced.

3.5 Effects of the Barrier Thickness and the Low- κ Dielectric on the Circuit EM Reliability

This section aims to show the structural and material modeling capability of the 3D circuit model by studying the effect of the barrier layer thickness and the low- κ dielectric on the EM reliability of the circuit.

Copper has a lower resistivity and a higher melting temperature than Aluminum. It is replacing the traditional Al-alloy as an EM-resistance interconnect material. However, the high diffusivity of Cu in Si and SiO₂ demands a diffusion barrier layer around the Cu interconnects to prevent the out-diffusion of Cu [107]. A commonly used material for the barrier layer is Ta [108]. As the device feature size goes to 0.18 μm and below, thick barrier layer is found to be undesirable in the circuit application due to its high total interconnect resistance [109]. On the other hand, the effectiveness of a diffusion barrier may degrade if its thickness is too thin. Lu *et al.* showed that thin barrier rendered an early failure and resulted in a shorter EM lifetime due to Cu out-diffusion [110].

On the other hand, low- κ dielectric is replacing the conventional SiO₂ ILD so as to meet the demand on the circuit switching speed. However, with a poorer interfacial adhesion and a smaller material elastic modulus, the reliability of the Cu/low- κ structure remains as a concern [111, 112]. Furthermore, the thermal conductivity of the low- κ dielectric is smaller than that of SiO₂, this increases the

circuit temperature and causes a faster degradation. Using the inverter model in the previous section as an example, the final circuit temperature is 106.90 °C and 133.02 °C for the SiO₂ and low-κ (carbon doped oxide) dielectric respectively. The temperature is much higher for the model using the low-κ dielectric due to its poorer thermal conductivity (0.58 W/m·°C) as compared with SiO₂ (1.38 W/m·°C).

To study the effect of the barrier layer thickness on the EM reliability of the circuit, four models with the barrier layer thickness varying from 1 to 25 nm are simulated. The setup for the simulation are the same as in Section 3.2 and 3.3 and the simulation results at the end of one load cycle are shown in Fig. 3.28.

Fig. 3.28. The maximum total AFD v.s. the barrier layer thickness for the contact at NMOS drain.

From Fig. 3.28, an increasing trend in the value of the maximum total AFD is observed with the decreasing barrier layer thickness, and the rate increases by

32.28 times when the barrier layer thickness goes below 7.5 nm, indicating a significant degradation in the EM lifetime with a barrier of thinner than 7.5 nm.

The percentage contribution of the three driving forces AFD_EWF, AFD_T, and AFD_S to the total AFD with different barrier layer thickness at the end of one load cycle is shown in Table 6. We can see that the AFD_S dominates over the other two driving forces, especially for the models with thinner barriers.

Table 6. The percentage contribution of the three driving forces to the total AFD.

Barrier thickness (nm)	Percentage contribution		
	AFD_EWF	AFD_T	AFD_S
1	0.017	0.128	99.855
5	0.051	0.317	99.632
10	0.075	0.532	99.393
25	0.097	0.619	99.284

As explained in the previous section, the value of the AFD_S at 90 °C is determined by the product of the thermo-mechanical stress gradient and the temperature gradient. With the same electrical loads, the maximum temperature gradients of the four models with different barrier layer thickness are similar, and it is the difference in the maximum thermo-mechanical stress gradients causes the difference in the maximum AFD_S and total AFD.

As compared with that of Cu, Ta has a lower CTE ($6.30 \times 10^{-6} \text{ }^{\circ}\text{C}^{-1}$ and $1.80 \times 10^{-5} \text{ }^{\circ}\text{C}^{-1}$ respectively) and a higher elastic modulus ($1.86 \times 10^5 \text{ MPa}$ and $1.10 \times 10^5 \text{ MPa}$ respectively), the presence of the Ta barrier introduces a tensile stress in the Cu

interconnects in the direction normal to the surface [99, 113]. The structural confinement provided by the Ta barrier increases the thermo-mechanical stress in the metal line as compared with the condition with no barrier. When the barrier thickness decreases, the confinement effect from the barrier is reduced and thermo-mechanical stress gradient increases, as shown in Fig. 3.29. The increase in the thermo-mechanical stress gradient causes an increase in the maximum total AFD. A higher maximum AFD reflects a shorter EM lifetime [7], therefore a thinner barrier can cause the reliability degradation of the circuit, and the effect is increasingly significant when the barrier layer thickness goes below 7.5 nm.

Fig. 3.29. The maximum thermo-mechanical stress gradient v.s. the barrier layer thickness for the contact at NMOS drain.

Keeping all other conditions the same, various low- κ dielectric, e.g. SiLK, MSQ (methyl silsesquioxane), CDO (carbon doped oxide), and SiCOH are used to

replace the traditional SiO₂ ILD. The material properties of the low- κ dielectric are listed in Table 7, and the values of the maximum total AFD and thermo-mechanical stress gradient of the models with different low- κ dielectric are shown in Fig. 3.30. The barrier layer thicknesses of the models are kept at 25 nm.

Table 7. The material properties of the low- κ dielectric as compared with SiO₂ [114, 115].

Materials	Properties				
	Young's Modulus (MPa)	Poisson's Ratio	Density (kg/m ³)	Thermal Expansion (1/°C)	Thermal Conductivity (W/m·°C)
SiLK	2.50×10^3	0.40	900	6.60×10^{-5}	0.14
MSQ	3.60×10^3	0.25	890	7.30×10^{-6}	0.40
CDO	4.47×10^3	0.30	1510	1.29×10^{-5}	0.58
SiCOH	1.62×10^4	0.30	910	1.20×10^{-5}	0.40
SiO ₂	7.14×10^4	0.16	2200	6.80×10^{-7}	1.38

Fig. 3.30. The maximum total AFD and thermo-mechanical stress gradient variation with different dielectric materials for the contact at NMOS drain.

As shown in Fig. 3.30, the models using the low- κ dielectric have a higher maximum total AFD than that using the SiO_2 ILD due to a higher thermo-mechanical stress gradient. This is because the low- κ materials have lower elastic modulus than SiO_2 , as can be seen in Table 7. The confinement effect provided by the elastic property of the low- κ dielectric is lower as proven by the experimental work of Webb *et al.* [116]. Looking at the high stress gradients due to MSQ and CDO, and that they have much lower elastic modulus than SiO_2 , one can expect that Cu with MSQ or CDO dielectric suffers significant reduction in EM lifetime. In addition, as can be seen in Table 7, the low- κ materials have higher CTE than SiO_2 , and this further reduces the confinement effect. When the CTE of the low- κ material increases and becomes comparable to that of Cu, the tensile stress in the interconnects decreases, as shown in Fig. 3.31.

Fig. 3.31. The relationship between the CTE and the thermo-mechanical stress for different dielectric materials for the contact at NMOS drain.

If the CTE of the low- κ dielectric is much larger than that of Cu, the confinement effect provided by the Ta barrier is no longer enough to produce the tensile stress and a compressive stress is produced which is negative in value. This is the reason of the extremely high stress gradient in the Cu/SiLK structure. With varying line width on different parts of the interconnect structure, the relative barrier thickness and the structural confinement from the barrier are different [99]. This results in a combination of the tensile (positive) and compressive (negative) stresses on different parts of the interconnects in the Cu/SiLK structure. The stress state of this interconnect structure becomes dominated by shear stresses and the reliability concern changes to interfacial delamination [113].

Fig. 3.32. The thermo-mechanical stress distribution in the Cu/SiLK structure (unit: MPa).

In summary, this section presents the increase in the total AFD with decreasing barrier layer thickness and the use of low- κ materials, using the inverter model as an example. The increase in the total AFD with decreasing barrier layer thickness is due to the increase in the thermo-mechanical stress gradient with a thinner barrier. The low- κ dielectric with a lower elastic modulus and a higher CTE as compared with SiO₂ reduces the structural confinement and renders a higher thermo-mechanical stress gradient, and thus a higher total AFD.

3.6 Summary

This chapter demonstrated the step by step construction of a complete 3D circuit model from its 2D IC layouts. For ease of demonstration, a simple inverter circuit with only the intra-block interconnects was used as an example. The method of conducting the transient electro-thermo-structural simulations using both Cadence (a circuit simulator) and ANSYS (a finite element tool) was also introduced.

The current density, temperature and thermo-mechanical stress, as well as the atomic flux divergences (AFDs) at any load step and any node of the model could be determined and plotted from the simulation results, and hence the EM weak spots of the interconnects of the circuit, which is the location with the highest total AFD could be identified.

Different from other 3D EM models in literature, our 3D model was able to perform the transient analysis at the circuit layout level. The simulation results successfully showed the transient temperature and stress responses to the change in the electrical loads and the circuit temperature respectively. Therefore the model was capable to evaluate the EM reliability of the interconnects of the circuit with different loadings and under different operation conditions.

To demonstrate the structural and material modeling capability of the 3D circuit model, the effects of the barrier layer thickness and the low- κ dielectric on the EM reliability of the circuit were studied using the inverter model. It was found that, although the use of sub-5 nm barrier layers in combination with low- κ dielectric was beneficial for reducing the RC delay, in our model a higher maximum total AFD was observed in the structures with a thinner barrier or with the low- κ dielectric. A shorter EM lifetime was expected when the barrier thickness scaled below 7.5 nm and/or when the SiO₂ ILD was replaced by a low- κ dielectric.

The 3D simulation is time and resource consuming, especially when the structure is large and complex. Due to the scale of the problem and the constraint of the time and resource, the current simulation was focusing on the void nucleation location. The microstructure and back stress effects were assumed to be negligible in this work.

CHAPTER 4 COMPARISON OF THE EM PERFORMANCE IN CIRCUIT STRUCTURE AND TEST STRCTURE

4.1 Introduction

As discussed in Chapter 2, 3D EM simulation is necessary as the circuit structure is indeed 3D in their actual physical implementation. Most of the 3D EM models in literature use the line-via test structures which are only part of the real circuit structure. To further demonstrate the necessity for complete circuit modeling, the comparison of the EM performances in a circuit structure and a standard test structure is performed in this chapter. Both the EM test condition and the circuit operation condition are considered.

Also, modifications to the interconnect structures are carried out and the effects of different interconnect structures such as the change in the via/contact position and its number, the inter-transistor distance, the metal structure and layers, and the transistor finger number on the EM reliability of the circuit are examined.

This chapter is organized in the following manner. Section 4.2 introduces the structures used for the comparison and Section 4.3 analyzes the simulation results obtained for the two structures under different conditions. Section 4.4 studies the

effects of the interconnect structures on the EM reliability of the circuit and the effects of the transistor finger number is shown in Section 4.5. This chapter ends with a conclusion in Section 4.6.

4.2 Model Construction and Simulation Setup

The previous chapter focused on the methodology of the construction and simulation of the 3D finite element circuit model and a circuit with an obvious variation in the current and voltage waveforms is chosen, so as to demonstrate the transient effects. The main purpose of this chapter is to compare the difference in the EM performance in the circuit structure and the test structure. As the EM modeling and experiments of the test structures are usually performed under DC condition, a DC dominating circuit is more suitable than the inverter circuit in the previous chapter.

Class-AB amplifier is a common building block of an analog circuit. To reduce the complexity of the work, only the output stage of a class-AB amplifier is used as an example. The schematic of the output stage of the class-AB amplifier studied in this work is shown in Fig. 4.1.

Fig. 4.1. The schematic of the output stage of a class-AB amplifier.

This output stage contains one PMOS (MP0) and one NMOS (MN0) as the functional block, and two short circuit protection transistors MN1 and MN2. As we are focusing on the functional block of the circuit, the short circuit protections MN1 and MN2 are not included in the 3D model as they do not affect the temperature and thermo-mechanical stress distributions of the model. To minimize the size of the 3D model, the sizes of MP0 and MN0 are kept small with a transistor width $W_t = 3 \mu\text{m}$. The supply voltage from V_{dd} is 3.3 V and the input voltage V_{in} is 0.7 V. The circuit operates under small signal excitation and drives a resistive load of 1 k Ω [79]. The threshold voltage V_t of MP0 and MN0 are -0.461 V and 0.483 V respectively as obtained from Cadence with this setup. The same frequency as in the previous chapter is chosen as an example. Other loadings and operating frequencies can be used as long as the circuit remains DC dominating. The source

and drain currents and voltages of the transistors extracted from Cadence are used as the inputs of the 3D model in ANSYS.

Note here that only one PMOS and one NMOS are used for the model construction and simulation, in the remaining section of this chapter, “PMOS” refers to MP0 and “NMOS” refers to MN0.

Fig. 4.2 shows the 3D model of the output stage of the class-AB amplifier and the line-via test structure. As can be seen in Fig. 4.2(c), the line-via test structure is part of the connection between the two transistors of the circuit structure. The rectangular region “cut out” from the circuit structure is the line-via test structure and it is used to compare with the circuit structure. The structure is taken from the PMOS region as the PMOS is the main current flow path under this loading condition, and the amount of current flow in the PMOS is more than 10 times larger than that in the NMOS.

(a)

Fig. 4.2. The 3D circuit structure and the line-via test structure. (a) The side view of the circuit structure showing all the surrounding layers (b) the isometric view of the circuit structure with the surrounding layer removed (c) the side view of the line-via test structure which is part of the circuit mode (the rectangle region) and (d) the isometric view of the line-via test structure with the surrounding layer removed.

In this modeling work, the following assumptions are made:

- (1). The transistors are assumed to be reliable and the focus of this work is on the EM reliability of the interconnects.
- (2). Transistor diffusion region is treated as the heat source and the input currents are applied at the contact/diffusion region interface of the 3D circuit structure.
- (3). Local current density at Metal 1 is extracted from the simulation results of the circuit structure, and it is used as the input in the simulation of the line-via test structure, so as to make sure that the two structures are operating under the same condition.
- (4). Real circuit using the $0.18\ \mu\text{m}$ technology has six metal layers. To reduce the complexity of the model and for the purpose of easy comparison, only

Metal 1, Metal 2, Via 12, and the contacts of the interconnect structure are considered, and the input voltage is applied at Metal 2.

- (5). The skin depth at an operating frequency of 100 MHz is larger than the thicknesses of Metal 1, Metal 2, Via 12, and the contacts, and thus the skin effect is ignored in this simulation.

Quadratic tetrahedral element type SOLID 98 is used in the ANSYS simulation for both structures. The additional layers and the surrounding materials and their properties, the boundary conditions, and the setup for the transient electro-thermo-structural simulations are the same as the inverter model in Chapter 3.

In summary, the output stage of a class-AB amplifier that is DC dominating is chosen to compared with the line-via test structure. For a better comparison, the simulation conditions for both structures are made as similar as possible, and the simulation results are discussed in the next section.

4.3 Distributions of the Atomic Flux Divergences under Different Conditions

This section discusses the similarities and the differences in the distributions of the AFDs due to the three driving forces and the locations of the maximum AFDs for both the circuit structure and the test structure under different conditions.

High temperature of around 250 °C to 300 °C is usually used in the EM tests to shorten the test time. The high temperature does not destroy the functionality of the structure as the line-via test structure only contains the metallization and its surrounding materials with no circuit components involved. The simulation is first conducted at an EM test temperature of 300 °C.

At the end of one load cycle (10 ns), the two structures have similar total AFD distributions as can be seen in Fig. 4.3. The locations of the maximum total AFD are found at the Metal 1/Via 12 interface (Site A) for both structures, and Region 1 has high total AFD values (i.e. above 8.05×10^9 atoms/ $\mu\text{m}^3 \cdot \text{s}$ for the circuit structure and 1.27×10^{10} atoms/ $\mu\text{m}^3 \cdot \text{s}$ for the line-via test structure). This result is consistent with the experimental results in literature [117, 118].

However, a test temperature of 300 °C is too high for the circuit under actual operation because most of the circuit components are not able to function well at above 125 °C and the chip packaging will change its properties significantly above its glass transition temperature which is 260 °C for the commonly used packaging materials in IC packaging [85]. The simulation is performed again at a circuit operation temperature of 90 °C and the results are shown in Fig. 4.4.

Fig. 4.3. The total AFD distributions of (a) the circuit structure and (b) the line-via test structure at 300 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$). The maximum AFD locations are found at the Metal 1/Via 12 interface for both structures.

Fig. 4.4. The total AFD distributions of (a) the circuit structure and (b) the line-via test structure at 90 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$). The maximum AFD locations are different for the two structures.

From Fig. 4.4, we can see that the total AFD distributions at 90 °C are different from those at 300 °C for both structures. For the circuit structure, the region with high total AFD values (i.e. above 5.70×10^7 atoms/ $\mu\text{m}^3\cdot\text{s}$) is now at the contact region (Region 2) instead of Region 1. The location of the maximum total AFD changes to the contact/Metal 1 interface (Site B) which is the location of the 2nd highest total AFD at 300 °C in Fig. 4.3(a). For the line-via test structure, the location of the maximum total AFD changes to the corner of Metal 1 (Site C).

Incidentally, the locations of the maximum total AFD of the circuit structure and the line-via test structure are the same at 300 °C in this case study. The EM failure site in the circuit structure, if possible, will be the same as that obtained in the line-via test structure under the EM test condition. Therefore no suspicion arises and the extrapolation of the EM test data from 300 °C will then be conveniently performed. However, as can be seen in Fig. 4.4, the locations of the maximum total AFD of either structure are different between 300 °C and 90 °C, and as will be seen later in Table 8, the dominant driving forces for EM at 300 °C for both structures are different from that at 90 °C. Therefore the EM weak spot and the EM lifetime obtained through the conventional extrapolation method will be incorrect. In fact, with different dominant failure physics, the conventional extrapolation method is not valid [119]. Further experimental verification will be interesting.

The change in the distribution and the location of the maximum total AFD is due to the increase in the thermo-mechanical stress and stress gradient, and hence the change in the dominant driving force for the total AFD at the circuit operation temperature. The AFD distributions due to electron wind force, thermo-mechanical stress gradient induced driving force, and temperature gradient induced driving force at the two test temperatures for both structures are shown in Fig. 4.5 to 4.8 and their percentage contribution to the total AFD is shown in Table 8.

The thermo-mechanical stress in the interconnects is directly proportional to the temperature difference between the interconnect temperature and the SFT of the metallization [120]. At the EM test temperature of 300 °C, the interconnect temperature is close to the SFT (i.e. 350 °C). The thermo-mechanical stress and stress gradient in the interconnects is relatively small (i.e. less than 100 MPa and 850 MPa/μm respectively), and this results in a smaller percentage contribution of the AFD_S to the total AFD as compared with the AFD_T, as shown in Table 8. The total AFD distribution mainly follows the distribution of the AFD_T. From Eqn. (2.23) and (2.26), the AFD_T depends on the current density and temperature gradient of the interconnects. At 300 °C, term 2 in (2.26) is around 5 orders of magnitude larger than term 1, thus the current density in the interconnects is the determining factor for the AFD_T.

Fig. 4.5. The AFD distributions due to (a) electron wind force (b) thermo-mechanical stress gradient induced driving force and (c) temperature gradient induced driving force of the circuit structure at 300 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$).

Fig. 4.6. The AFD distributions due to (a) electron wind force (b) thermo-mechanical stress gradient induced driving force and (c) temperature gradient induced driving force of the line-via test structure at 300 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$).

Fig. 4.7. The AFD distributions due to (a) electron wind force (b) thermo-mechanical stress gradient induced driving force and (c) temperature gradient induced driving force of the circuit structure at 90 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$).

Fig. 4.8. The AFD distributions due to (a) electron wind force (b) thermo-mechanical stress gradient induced driving force and (c) temperature gradient induced driving force of the line-via test structure at 90 °C (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$).

Table 8. The percentage contribution of the three driving forces to the total AFD for the two structures under different conditions.

Test Temperature		Percentage contribution		
		AFD_EWF	AFD_S	AFD_T
Circuit structure	300 °C	1.95	33.32	64.73
	90 °C	0.62	93.57	5.81
Line-via test structure	300 °C	1.67	37.10	61.23
	90 °C	0.51	97.65	1.84

As shown in Fig. 4.9, current crowding occurs at Site A and Site B of the circuit structure and high current density of more than $2.06 \times 10^{10} \text{ pA}/\mu\text{m}^2$ is observed at these locations. The locations of the maximum AFD_T and the maximum total AFD are found at the place with the highest current density, i.e. the Metal 1/Via 12 interface (Site A).

Fig. 4.9. The current density distribution of the circuit structure at 300 °C (unit: $\text{pA}/\mu\text{m}^2$). The arrow and the box indicate the maximum current density location and the high current density region respectively.

From Table 8, we can also see that the AFD_S has significant contribution to the total AFD. The location of the 2nd highest total AFD is at the place with the highest AFD_S, i.e. the contact/Metal 1 interface (Site B). From Eqn. (2.24) and (2.27), the AFD_S depends on the current density, thermo-mechanical stress gradient and temperature gradient of the interconnects. At 300 °C, term 1 and term 3 in Eqn. (2.27) are both around 6 orders of magnitude larger than term 2, and thus the AFD_S is determined by the current density and the product of the thermo-mechanical stress gradient and the temperature gradient.

The distributions of the temperature, temperature gradient and thermo-mechanical stress gradient of the circuit structure are shown in Fig. 4.10. At the end of one load cycle, Region 1 has a high temperature (i.e. above 300.23 °C) due to high current density (i.e. above 1.18×10^{10} pA/ μm^2) at this region. The temperature gradient is higher at the bottom of the PMOS contacts (i.e. above 0.10 °C/ μm), which is closer to both the heat source (the diffusion region) and the heat sink (the base of the metal plate). The temperature and current density of the PMOS contacts gradually decrease as we move away from Region 1, and the temperature gradient follows this trend. Site A has a small temperature gradient of less than 0.015 °C/ μm due to the relatively uniform temperature distribution around Site A, as can be observed in Fig. 4.10(a) (i.e. the red color region with a temperature difference of less than 0.026 °C). The thermo-mechanical stress of the interconnect is dominated by the intrinsic stress of the metallization as explained in

Section 3.4.4, but its value is more than 5 times smaller than that in Fig. 3.23 when the difference between the interconnect temperature and the SFT drops from 260 °C to 50 °C. This causes the model to have a smaller thermo-mechanical stress gradient (i.e. less than 850 MPa/μm) at 300 °C as compared with the case at 90 °C, as shown in Fig. 4.10(c).

With similar stress gradients at Site A and B, though the current density at Site A is around 1.5 times higher than that at Site B, the temperature gradient at Site B is more than 3 times higher than that at Site A. The combined effect of term 1 and term 3 in Eqn. (2.27) causes the AFD_S at Site B to be slightly higher (i.e. around 1.11 times) than that at Site A.

The same analysis applies to the simple line-via test structure. Fig. 4.11 shows the distributions of the current density, temperature gradient and thermo-mechanical stress gradient of the line-via test structure at 300 °C. For this structure, the Metal 1/Via 12 interface (Site A) also has the highest current density, and thus the locations of the maximum AFD_T and the maximum total AFD are found at Site A. The absence of the contact region causes the maximum AFD_S to fall at the corner of Metal 1 (Site C) with the highest stress gradient and temperature gradient product. With high current density of more than 2.21×10^{10} pA/μm², Site A still has relatively high AFD_S of above 2.51×10^{10} atoms/μm³·s.

Fig. 4.10. The distributions of (a) temperature (unit: $^{\circ}\text{C}$) (b) temperature gradient (unit: $^{\circ}\text{C}/\mu\text{m}$) and (c) thermo-mechanical stress gradient (unit: $\text{MPa}/\mu\text{m}$) of the circuit structure at 300 $^{\circ}\text{C}$.

Fig. 4.11. The distributions of (a) current density (unit: $\text{pA}/\mu\text{m}^2$) (b) temperature gradient (unit: $^{\circ}\text{C}/\mu\text{m}$) and (c) thermo-mechanical stress gradient (unit: $\text{MPa}/\mu\text{m}$) of the line-via test structure at 300 $^{\circ}\text{C}$.

In addition, when the input current rises and reaches the current density level used in the EM test, the percentage contribution of the AFD_S to the total AFD increases and overrides that of the AFD_T. The percentage contribution of term 3 (i.e. the current density determining term) to the AFD_S in Eqn. (2.27) also increases. These cause a change of the location of the maximum AFD_S to Site A for both structures. Now the location of the maximum AFD_T and the maximum AFD_S are both at Site A, and it is the location of the maximum total AFD.

At the circuit operation temperature of 90 °C, the distributions of the current density and temperature gradient for both structures are similar to that at 300 °C as the current and voltage loads under the two conditions are the same. The distributions of the thermo-mechanical stress and stress gradient for both structures are similar to that at 300 °C due to their similar intrinsic stress distributions. However, the large difference between the interconnect temperature and the SFT causes around 5 times increase in the magnitudes of the thermo-mechanical stress and stress gradient in the interconnects at 90 °C as compared with that at 300 °C. With the same current loads, the AFD_S becomes the dominant factor for the total AFD, and the total AFD distribution and the location of the maximum total AFD depends on that of the AFD_S. Term 1 in Eqn. (2.27) is 8 and 1 order of magnitude larger than the other two terms respectively. The AFD_S now mainly depends on the product of the thermo-mechanical stress gradient and the

temperature gradient, but no longer on the current density. As a result, the location of the maximum AFD_S of the circuit structure changes to Site B, and the region with high values of AFD_S (i.e. above 5.32×10^7 atoms/ $\mu\text{m}^3\cdot\text{s}$) moves to the contact region (Region 2) with high temperature gradient (i.e above 0.10 °C/ μm). For the line-via test structure, as the total AFD is now mainly determined by the AFD_S, the location of the maximum total AFD is the same as that of the AFD_S, and it is at the corner of Metal 1 (Site C). Site A no longer has the highest AFD_S even though it still has the highest current density.

In summary, while the circuit structure and the line-via test structure have the same maximum total AFD locations at the EM test temperature, they do not show the same location at the circuit operation temperature as the total AFD is no longer mainly determined by the current density. This can cause a misinterpretation of the void nucleation location when using the line-via test structure to model the EM reliability of the circuit.

Although the above results may be specific to this circuit, they do show a difference in the void nucleation location for the two structures under the different conditions. In other word, the EM tests based on the line-via test structure is only to validate the reliability of the interconnect technology with respect to EM, but not necessary the EM reliability of the circuit.

4.4 Effects of the Interconnect Structures on the Circuit EM Reliability

After the comparison with the test structure, the circuit model is modified to study the effects of interconnect structures on the EM reliability of the circuit.

Based on the model in Fig. 4.2(a), eleven models with the following changes in the interconnect structures are built. All the layouts are checked to comply with the design rules.

- (I). *Change in the position of the vias*: The vias are moved from the extreme end of Metal 1 (Fig. 4.12(a)) to the region closer to the contacts (Fig. 4.12(b)), and directly above the contacts (Fig. 4.12(c)).
- (II). *Change in the inter-transistor distance*: The inter-transistor distance (i.e. the distance between the diffusion regions of PMOS and NMOS) is varied from 2 μm (i.e. minimum distance, Fig. 4.12(d)) to 5 μm (Fig. 4.12(e)) and then to 8 μm (Fig. 4.12(f)).
- (III). *Change in the number and the position of the contacts*: The number of contacts at the source and drain regions is reduced from 6 in Structure 4.12(d) to 3, with the contact position directly below the vias (Fig. 4.12(g)) and at the other end of Metal 1 (Fig. 4.12(h)).
- (IV). *Change in the metal structure at the output line*: Metal 1 is used as the output line instead of Metal 2 (Fig. 4.12(i)).

(V). *Change in the number and the position of the metal layers*: In the real circuit, the output line of the transistor may connect to the next stage directly via Metal 2 or Metal 1 (e.g. to another transistor, like in Structure 4.12(a) to 4.12(i)), or via Metal 1 to Metal 6 (e.g. to a capacitor or inductor, or to the output pad). The connection may be directly above the transistor (Fig. 4.12(j)), or at a distance away from the transistor (Fig. 4.12(k)). For easy comparison purpose, similar structures are used in 4.12(j) and 4.12(k).

The functionality of the circuit for the above structures remains unchanged as verified by Cadence. The simulation is carried out under the circuit operation of 90 °C with the same setup as in the previous section. The current loads are applied at the contact/diffusion region interface and the voltage loads are applied at the top metal layer (Metal 2 for Structure 4.12(a) to (i) and Metal 6 for Structure 4.12(j) and (k)). The total AFD distributions and the maximum total AFDs of the above structures at the end of one load cycle (10 ns) are shown in Fig. 4.13 and summarized in Table 9.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)

Fig. 4.12. The side views of the circuit models with different interconnect structures. (a) The vias positioned far away from the contact region (b) the vias positioned nearer to the contact region (c) the vias positioned directly above the contact region (d) an inter-transistor distance of $2\ \mu\text{m}$ (the isometric and the side view) (e) an inter-transistor distance of $5\ \mu\text{m}$ (f) an inter-transistor distance of $8\ \mu\text{m}$ (g) 3 contacts positioned directly below the vias (h) 3 contacts positioned at the other end of Metal 1 (i) Metal 1 used as the output line (the isometric and the side view) (j) 6 metal layers positioned directly above the transistor (the side and the plain view) and (k) 6 metal layers positioned at a distance of $5\ \mu\text{m}$ away from the transistor (the plain view).

The observations in Table 9 may be explained as follows:

Under the circuit operation condition, the AFD_S has more than 90% contribution to the total AFD among the three driving forces. The total AFD distribution and the location of the maximum total AFD of the 3D model are mainly determined by that of the AFD_S. The location of the maximum AFD_S is found at the place where the product of the thermo-mechanical stress gradient and the temperature gradient is the highest, and it is also the location of the maximum total AFD, as indicated by the arrows in Fig. 4.13.

Fig. 4.13. The total AFD distributions of Structures 4.12(a) to (k) (unit: atoms/ $\mu\text{m}^3 \cdot \text{s}$).

Table 9. Maximum total AFD for different interconnect structures.

Structural changes	Maximum total AFD (atoms/ $\mu\text{m}^3\cdot\text{s}$)			Remarks
Distance between the vias and the contacts	1.5 μm (Fig. 4.13a)	1 μm (Fig. 4.13b)	0 μm (Fig. 4.13c)	The closer the vias to the contacts, the smaller the max AFD.
	1.71×10^8	1.52×10^8	1.09×10^8	
Inter-transistor distance	2 μm (Fig. 4.13d)	5 μm (Fig. 4.13e)	8 μm (Fig. 4.13f)	Insignificant effect.
	1.09×10^8	1.04×10^8	1.04×10^8	
Number and position of the contacts	6 (Fig. 4.13d)	3		Fewer contacts increase the max AFD, especially when the distance between the contacts and the vias is larger.
		near to via (Fig. 4.13g)	far from via (Fig. 4.13h)	
	1.09×10^8	1.36×10^8	1.72×10^8	
Metal structure at the output line	Metal 1+2 (Fig. 4.13d)	Metal 1 only (Fig. 4.13i)		Metal 1 only structure shows a lower max AFD and an even total AFD distribution.
	1.09×10^8	1.59×10^7		
Number and position of the metal layers	2 (Fig. 4.13d)	6		Higher number of metal layers increases the max AFD. The increase in max AFD is smaller when the additional metal layers are added further away from the transistor.
		directly above Metal 2(Fig. 4.13j)	5 μm away (Fig. 4.13k)	
	1.09×10^8	1.54×10^8	1.36×10^8	

The rise in temperature of the models at the end of one load cycle is less than 0.45 °C and the thermo-mechanical stress of the interconnects is mainly determined by the intrinsic stress. The values of the maximum thermo-mechanical stress and stress gradient of Structures 4.12(a) to (k) are similar due to their similar intrinsic stresses. The values and the locations of the maximum AFD_S and total AFD are therefore mainly affected by the temperature gradients of the models. The temperature gradient profile at the location with the highest total AFD of the eleven structures is shown in Fig. 4.14.

Fig. 4.14. The temperature gradient profile of different interconnect structures.

(I). The location of the maximum total AFD for Structure 4.12(a) is at the contact/Metal 1 interface. The change in the position of the vias causes a change in the value and distribution of the current density as shown in Fig. 4.15. From Fig. 4.15(a), we can see that there are two current crowding places for Structure 4.12(a), the Metal 1/Via 12 interface (Site A) and the contact/Metal 1 interface (Site B). When the distance between the vias and the contacts decreases, the crowding effect reduces. This causes a decrease in the current density with decreasing via/contact distance, especially when the vias are directly above the contacts. The reduction in the current density reduces the heat up and the temperature gradient of the model, as shown in Fig. 4.14. Therefore Structures 4.12(b) and 4.12(c) have a smaller maximum AFD_S and hence a smaller maximum total AFD as compared with Structure 4.12(a) (11.11% and 36.26% reduction respectively). A smaller maximum total AFD means a longer void

nucleation time [7]. As the void nucleation time occupies a large portion of the EM lifetime [121], increasing the void nucleation time can effectively enhance the EM lifetime of the circuit, and Structures 4.12(b) and 4.12(c) are expected to have a longer EM lifetime than Structures 4.12(a).

Fig. 4.15. Vector plot of the current density distributions of Structures 4.12(a) to (c) (unit: $\text{pA}/\mu\text{m}^2$).

Structure 4.12(b) has the same maximum total AFD location (Site B) as Structure 4.12(a). For Structure 4.12(c), the contact/Metal 1 interface (Site B) is no longer

the current crowding region when the vias are directly above the contacts. The temperature gradient at this location decreases by more than 5 times as shown in Fig. 4.16(c). The locations of the maximum AFD_S and total AFD change to the bottom of the contact (Site C) where the product of the stress gradient and the temperature gradient is highest. Besides the effect due to current crowding, the temperature gradient at Site A increases by more than two times as the vias are now directly above the heat source (the diffusion region) and the heat sink (the meal plate base). The location of the 2nd highest AFD_S and total AFD is found at Site A.

Fig. 4.16. The temperature gradient distributions of Structure 4.12(a), (b) and (c) (unit: $^{\circ}\text{C}/\mu\text{m}$).

(II). The increase in the inter-transistor distance from 2 μm to 5 μm causes around 0.10% reduction in the circuit temperature and temperature gradient as the heat sources are further apart. The reduction in the temperature and the temperature gradient gives rise to a 4.59% reduction in the value of the maximum total AFD. The distributions of the temperature gradient and total AFD, the locations of the maximum total AFD for Structure 4.12(d) and 4.12(e) are similar to 4.12(c) due to their similar interconnect structures. This circuit has only one main heat generating transistor as the amount of current flow in NMOS is more than 10 times smaller than in PMOS. Hence the effect of the inter-transistor distance is insignificant and separating the two transistors further apart has very limited impact on the circuit temperature and temperature gradient. No further reduction in the value of the maximum total AFD is observed when the inter-transistor distance increases from 5 μm to 8 μm .

(III). When the number of contacts is reduced from 6 to 3, the increase in the current density at each contact for Structures 4.12(g) and 4.12(h) causes a rise in the temperature and temperature gradient of the model [93]. 24.77% and 57.80% rise in the values of the maximum total AFD are observed for Structures 4.12(g) and 4.12(h) (i.e. the 3 contacts structure) respectively as compared with Structure 4.12(d) (i.e. the 6 contacts structure), implying a shorter void nucleation time with fewer contacts. This result is expected and it agrees with the reported experimental observations in [117, 118]. The observation also agrees with the

design rule for preventing EM. Structure 4.12(h) has an even higher maximum total AFD than 4.12(g) due to the change in the position of the contacts (i.e. further away from the vias), and this corresponds to the observations in (I). The location of the maximum AFD for Structure 4.12(h) is different from 4.12(a) as the increase in the temperature gradient at the contact bottom has a larger impact on the AFD_S than the increase in the current density at the contact/Metal 1 interface. The locations of the maximum AFD_S and total AFD are found at the contact bottom.

Fig. 4.17. The temperature gradient distributions of Structure 4.12(d), (g) and (h) (unit: $^{\circ}\text{C}/\mu\text{m}$).

(IV). In the previous structures, the total AFD is always higher (i.e. above $1.00 \times 10^8 \text{ atoms}/\mu\text{m}^3$) at the contacts nearer to the current crowding site (i.e. the vias at the output line), and lower (i.e. below $1.00 \times 10^7 \text{ atoms}/\mu\text{m}^3$) at the contacts further

away. When Metal 1 is used as the output line, the removal of the Metal 2/Via 12 structure eliminates the current crowding at this location. From Fig. 4.18 and 4.19, we can see that the distributions of the current density and temperature gradient at each contact on both the source and drain interconnects are uniform. The total AFD distribution is also uniform at each contact regardless of the contact position, as can be observed Fig. 4.13(i). The avoidance of the current crowding results in an 85.41% drop in the value of the maximum total AFD for Structure 4.12(i) as compared with 4.12(d). The location of the maximum total AFD is found at the contact connecting to the source interconnects where the voltage is higher than at the drain interconnects (around 3.30 V and around 1.30 V respectively).

Fig. 4.18. The current density distribution of Structure 4.12(i) (unit: pA/μm²).

Fig. 4.19. The temperature gradient distribution of Structure 4.12(i) (unit: $^{\circ}\text{C}/\mu\text{m}$).

Fig. 4.20. The temperature gradient distributions of Structure 4.12(j) and (k) (unit: $^{\circ}\text{C}/\mu\text{m}$).

(V). Adding more metal/via layers causes an increase in the temperature gradient in the z-direction due to a larger distance from the metal top to the heat source (Fig. 4.20), and thus the maximum total AFD for this structure increases. The total AFD distribution and the location of the maximum total AFD for Structure 4.12(j) is almost the same as Structure 4.12(d), therefore the trends in (I) to (III) (where only two metal layers are considered) apply to the structures up to 6 metal layers.

When the metal/via stacks are added at a distance away from the transistor (i.e. away from the heat source), the impact of the additional metal/via layers on the temperature gradient of the circuit reduces. This results in a smaller increase in the maximum total AFD for Structure 4.12(k) as compared with 4.12(j) (24.77% and 41.28% respectively). The maximum total AFD further reduces to 1.30×10^8 atoms/ $\mu\text{m}^3 \cdot \text{s}$ when the width of the additional metal layers is doubled, and this is due to the decrease in current density with wider metal lines and more vias.

In summary, this section presents the impacts of the interconnect structures on the EM reliability of the circuit. From the simulation results, it is observed that we can improve the EM lifetime of the circuit by placing the vias directly above the contact region, using more contacts and more uniform interconnect structures, or adding the Metal 3 to Metal 6 connection away from the transistors. The observations are consistent with the design rules and the experimental results in literature.

4.5 Effects of the Transistor Finger Number on the Circuit EM Reliability

The effects of the transistor finger number on the EM reliability of the circuit are studied in this section based on the circuit model in Fig. 4.2(a). In order to have at least two contacts on each finger, the transistor with a larger W_t of $9\text{ }\mu\text{m}$ is used (i.e. more contacts than the model in Fig. 4.2(a)). Fig. 4.21 shows four circuit layouts with different number of fingers. Based on Layout 4.21(a), the models with the number of contacts on the source and drain interconnects vary from 1 to 18 are constructed. The simulations are performed on these models as well.

Fig. 4.21. The circuit layouts at the output stage of a class-AB amplifier with different finger number.
(a) finger number = 1 (b) finger number = 2 (c) finger number = 3 and (d) finger number = 5.

An increase in the maximum total AFD is observed with decreasing number of contacts on the source and drain interconnects for Layout 4.21(a), and this is illustrated in Fig. 4.22. The effect of the number of contacts becomes significant when the contact number goes below 4 as shown in Fig. 4.22.

Fig. 4.22. The change in the maximum total AFD with the number of contacts on the source and drain interconnects of Layout 4.21(a).

The locations of the maximum total AFD of the four layouts with different number of fingers are found to be similar. Due to the limitation in the metal line length (i.e. the width per finger), the transistor with more fingers (i.e. a smaller width per finger) tends to have fewer contacts on the source and drain interconnects. An increase in the value of the maximum total AFD is observed with increasing number of fingers due to a decrease in the number of contacts on the source and drain interconnects, as illustrated in Table 10 and Fig. 4.23. This increase in the value of the maximum total AFD is not very significant as the smaller number of contacts on the source and drain interconnects for the four models are all larger than 4 as can be seen in Table 10.

Table 10. The number of contacts on the source and drain interconnects for Layouts 4.21(a) to (d).

Layout	Finger number	Contact number	
		Source	Drain
4.21(a)	1	18	18
4.21(b)	2	18	9
4.21(c)	3	12	12
4.21(d)	5	9	9

Fig. 4.23. The relationship between the finger number, the maximum total AFD and the smaller number of contacts on the source and drain interconnects.

Fig. 4.24. The relationship between the finger number and the maximum total AFD for a given number of contacts on the source and drain interconnects. The impact of finger number becomes insignificant when the number of contacts on the source and drain interconnects are the same.

Layout 4.21(b) with two fingers has two metal lines for the source and one metal line for the drain of a transistor. There are 18 contacts on the source interconnects and only 9 contacts on the drain interconnect. As such, the current density at the drain region becomes almost double than that at the source region, and this greatly increases the maximum total AFD of Layout 4.21(b). The smaller number of contacts on the source and drain interconnects for Layout 4.21(b), 4.21(c) and 4.21(d) is 9, 12 and 9 respectively. From Fig. 4.23, we can see that the maximum total AFD depends on the smaller number of contacts on either the source or the drain interconnect instead of the number of fingers. For a given number of contacts on the source and drain interconnects, the impact on the maximum total AFD due to number of fingers is insignificant as can be seen in Fig. 4.24.

In summary, the increase in the number of fingers can cause a decrease in the total number of contacts due to the limitation in the metal line length of the source and drain interconnects for the case of small transistor, and this is not favorable as it increases the average current density and the total AFD.

On the other hand, the difference in the total number of contacts with different finger number is insignificant for large transistors due to their longer metal line lengths. The maximum total AFD is therefore similar with varying finger number. However, in order to obtain an even distribution in the current density and total AFD, it is better to use odd number of fingers so as to achieve the same number of

contacts and thus the even current density and temperature distributions on both the source and the drain interconnect.

Another option in the case of large transistor is the use of waffle layout. An example of the waffle layout is shown in Fig. 4.25. Comparing with the simple line structure in Fig. 4.12, the uneven distribution of the contacts on the source and drain interconnects in the waffle layout (varying from 1 to 4 for the example in Fig. 4.25) creates significant current crowding and high temperature gradient on the interconnects with only one contact, as indicated by the circle in Fig. 4.26. The contact at this location tends to fail much faster than the others because this contact has a much larger maximum total AFD as can be seen in Fig. 4.27. Hence the waffle layout is not favorable in the reliability point of view.

Fig. 4.25. The layout of a waffle transistor [122].

(a)

(b)

Fig. 4.26. The distributions of (a) current density (unit: pA/μm²) and (b) temperature gradient (unit: °C/μm) of the waffle layout in Fig. 4.25, titled view from the back. The circles indicate the problematic region.

Fig. 4.27. The total AFD distribution (unit: $\text{atoms}/\mu\text{m}^3\cdot\text{s}$) of the waffle layout in Fig. 4.25, titled view from the back. The circle indicates the problematic region.

4.6 Summary

In this chapter, the 3D circuit model of the output stage of a class-AB amplifier was compared with the line-via test structure, under both the EM test condition and the circuit operation condition. It was observed that though the location of the maximum AFD of the circuit model coincided with that of the line-via test structure at EM test temperature, the locations for the two structures are different at the circuit operation temperature as current density was no longer the dominant driving force for EM at this temperature. The EM modeling based on the line-via test structure might not be able to identify the correct EM failure sites for a circuit

at its operation temperature. This study again implied the need for the complete 3D circuit modeling in the EM study.

A few sets of models were constructed to compare the difference in the values and locations of the maximum total AFD when there was a change in the interconnect structure. Higher maximum total AFD was observed for the structures with a longer via and contact distance, a shorter inter-transistor distance, a smaller number of contacts, and more metal layers. Some changes in the interconnect structure could cause a change in maximum total AFD location. The observations were consistent with the experimental results and the design rules, and thus validated the capability of the 3D finite element circuit model for performing the EM lifetime comparison when there was a structural change in the interconnects.

In the case of small transistors, there were fewer contacts on the source and drain interconnects for the transistor with more fingers due to the limitation in the metal line length of the source and drain interconnects. An increase in the maximum total AFD was observed with increasing finger numbers, and the value of the maximum total AFD depended on the smaller number of contacts on the source and drain interconnects. The impact was insignificant in the case of large transistors as the number of contacts on the source and drain interconnects are similar for the transistors with different finger numbers. The use of the waffle

layout might degrade the EM reliability of the circuit due to the non-uniform current density and temperature gradient distributions as a result of the non-uniform distribution of the contacts on the source and drain interconnects.

CHAPTER 5 MODLING THE INTERCONNECT EM RELIABILITY AT THE CIRCUIT LAYOUT LEVEL

5.1 Introduction

The circuit models built in Chapter 3 and 4 only consider the intra-block interconnects and simple inter-block connections up to Metal 2. Real circuits consist of a large number of transistors and other circuit components connected by complex inter-block connections made of multiple metal layers. In this chapter, a complete 3D circuit model including both intra- and inter-block interconnects is constructed. Electro-thermo-structural simulations are performed and the modifications that can help enhancing the EM reliability of the circuit are carried out based on the observations in the simulation.

This chapter is organized as follows. In Section 5.2, the construction of the 3D circuit model with the inclusion of the inter-block interconnects up to the metal top and the simulation setup for the model is presented. In Section 5.3, the discussions on the simulation results obtained are presented and the EM weak spots for the circuit under study are identified. Some possible changes to the layout of the circuit based on the EM spots identified in Section 5.3 are presented

in Section 5.4, and the resultant improvements in the EM performance are discussed. This chapter ends with a conclusion in Section 5.5.

5.2 Model Construction and Simulation Setup

Low noise amplifier (LNA) is widely used in communication or microwave system. It boosts the desired signal power with little noise and distortion. The LNA circuit is chosen as an example in this chapter because it is a simple and common circuit and has wide application. Also, the LNA is susceptible to reliability degradation because it is very sensitive to circuit condition. The construction and modeling procedures introduced in this section are applicable to other circuits as well.

The schematic and layout of a two-stage LNA circuit is shown in Fig. 5.1 and 5.2 respectively. The first stage of the circuit consists of a main input transistor M1 and a cascode transistor M2, and the second stage consists of a main input transistor M3 and a cascode transistor M4. The supply voltage from V_{dd} and the input voltage V_{in} are both 1.8 V, and the bias voltage V_{bias1} and V_{bias2} are both 0.7 V, as indicated in Fig. 5.1. The operating frequency of the circuit is 5.8 GHz.

Fig. 5.1. The schematic of a simple LNA circuit.

(a)

(b)

Fig. 5.2. (a) The layout of the circuit in Fig. 5.1 and (b) the zoom-in view at the transistor region.

with the assumption that the same amount of current flows in the top and bottom of the metal layers on the same source or drain interconnect (i.e. the current flows in the source interconnect at location A and B and in the drain interconnect at location C and D are assumed to be the same). There are changes in the current density along the current flow paths due to the variation in the track and via widths and the metal thicknesses. Current crowding and high thermo-mechanical stress built up occur at the locations with significant dimensional or geometrical changes, such as the contact/metal and via/metal interfaces as indicated by the rectangular boxes in Fig. 5.3.

As our work is focusing on the EM reliability of the interconnects, the circuit components (i.e. transistors, capacitors, inductors, and resistors) are assumed to be reliable. The study in [123] showed that the EM lifetime is independent of the surrounding dummy structures for metal line width larger than $0.063\text{ }\mu\text{m}$. The LNA circuit under study is using the $0.18\text{ }\mu\text{m}$ technology and the minimum metal line width is $0.23\text{ }\mu\text{m}$. Therefore the dummy structures in this circuit do not affect the EM lifetime of the model and they are removed during the 3D model construction in order to reduce the simulation time and computation memory.

The simulation is first conducted on a coarsely meshed full model that includes all the inter-block interconnects, as shown in Fig. 5.4. The intra-block interconnects are lumped together as simple blocks. Skin effect, reflected by a 10% increase in

resistance below the skin depth region (i.e. $0.87\ \mu\text{m}$ at the operating frequency of 5.8 GHz in this case) is included in the model [124]. Here only the thick metal top, Metal 6 with a thickness of $2.34\ \mu\text{m}$ is affected.

Fig. 5.4. The top view of the full model of the LNA circuit after removing the dummy structures, showing only the interconnects.

The operating temperature of a LNA with a supply voltage of 1.8 V is between $-40\ ^\circ\text{C}$ to $85\ ^\circ\text{C}$ [125, 126]. Here the worst-case case temperature of $85\ ^\circ\text{C}$ is used. Quadratic element SOLID 98 is used in the ANSYS simulation and the model construction and the simulation setup are the same as in Chapter 3 and 4.

In summary, this section introduces the method of constructing the 3D circuit model of a REAL circuit structure that includes all the inter-block interconnects up to the metal top. For demonstration purpose, a simple LNA circuit is used as an example.

5.3 Distributions of the Atomic Flux Divergences

The distributions of the AFDs in the interconnects are discussed in this section for both the full model and the sub-model. The EM weak spots are identified and will be used for the layout and process modifications in Section 5.4.

5.3.1 Total AFD Distribution of the Full Model

The total AFD distribution of the full model at the end of one load cycle (0.172 ns) is shown in Fig. 5.5. The location of the maximum total AFD is found at the turning corner of the source interconnect of Transistor M1, as indicated by the arrow in Fig. 5.5.

Fig. 5.5. The total AFD distribution of the full model of the LNA circuit (unit: atoms/μm³·s). The arrow indicates the maximum total AFD location.

The current density and temperature gradient distributions of the full mode are shown in Fig. 5.6 and 5.7 respectively. In the circuit layout, the V_{dd} lines are connected to the gate of Transistor M2 and M4. With negligible gate current, the current density and the resulting temperature gradient of the V_{dd} lines are small (they are all inside the blue regions as can be seen in Fig. 5.6 and 5.7). These interconnects are therefore of little concern in this work.

Although the current flows in the V_{dd} and ground lines connected to the inductors are high, these lines are made of the thick top metal (Metal 6 in this case). The maximum current density in these interconnects is more than 10 times smaller than that in the source and drain interconnects at the transistor region which are made of the thinner Metal 3 layer. Table 11 shows the metal layer type and shape as well as the line width of the source and drain interconnects at the transistor regions. The highest current density is found at the source interconnect of Transistor M1 with a sharp turn, as indicated by the arrow in Fig. 5.6.

Table 11. Metal layer type, shape and line width of the source and drain interconnects of the four transistors.

Interconnect		Type	Shape	Line Width (μm)
Transistor M1	Source	Metal 3	Sharp turn	6.40
	Drain	Metal 3	Small turn	6.40
Transistor M2	Source	Metal 3	Small turn	6.40
	Drain	Metal 6	Simple strip	15
Transistor M3	Source	Metal 3	Simple strip	6.40
	Drain	Metal 3	Simple strip	6.40
Transistor M4	Source	Metal 3	Simple strip	6.40
	Drain	Metal 6	Sharp turn	12

The interconnect temperature is affected by the heat convection to the surrounding through the outer surface of the chip, the heat conduction through the heat sink, and Joule heating due to current flow in the interconnects, in which the latter two are more dominant. If the Joule heating effect is ignored, the upper metal layers are found to have a higher temperature than the lower metal layers due to a larger distance between the upper layers and the heat sink [127]. However, when the Joule heating effect is taken into consideration, the heat flux in the current carrying lines becomes the determining factor for the temperature and temperature gradient of the interconnects [128]. The temperature rise in a single line interconnect is proportional to the square of the current density [93], and it increases with increasing current density, so does the temperature gradient [129].

Local high current density causes a high temperature gradient at the source and drain interconnects of Metal 3, especially at the sharp turning corners, as shown by the orange and the red regions in Fig. 5.7. Based on our simulation results in Chapter 3 and 4, the total AFD under the circuit operation condition is mainly determined by the AFD_S, which in turn depends on the product of the local thermo-mechanical stress gradient and the temperature gradient. The source interconnect of Transistor M1 with a sharp turn therefore has the highest AFD_S and the highest total AFD due to the highest temperature gradient at this location.

Fig. 5.6. The current density distribution of the full model (unit: $\text{pA}/\mu\text{m}^2$). The arrow indicates the location with the highest current density.

Fig. 5.7. The temperature gradient distribution of the full model (unit: $^{\circ}\text{C}/\mu\text{m}$). The arrow indicates the location with the highest temperature gradient.

However, lumping the intra-block interconnects together causes a sharp drop in the thermo-mechanical stress gradient due to the uniformity in structure in the simplified blocks. This results in a drop in the values of the AFD_S and hence the total AFD as compared with the real circuit structure, especially for the transistor with more fingers (i.e. more complicated structure) as can be seen in Fig. 5.8.

Fig. 5.8. The percentage drop in the maximum total AFD due to structural simplification v.s. the transistor finger number.

Moreover, the over-simplification of the interconnect structure causes the disappearance of the structures with significant dimensional or geometrical changes. Comparing Fig. 5.3 (before simplification) and Fig. 5.9 (after simplification), we can see that the complex structures at Region II disappear. The disappearance of the complex structures may affect the current density and thermo-mechanical stress distributions of the model and thus results in an inaccurate prediction. The coarse mesh of the full model further reduces the accuracy of the simulation results.

Fig. 5.9. The partial side view of Transistor M2 after structural simplification.

Therefore, the simulation is performed again on a finely meshed sub-model at the “problematic” region with the inclusion of the detailed structures of the intra-block interconnects. Due to the limitation in the computation memory, the model file size cannot be bigger than 100 MB. The model size limit is exceeded if all the intra-block contacts and vias are included and hence a simplification is performed to reduce the model size. The simulation in [19] showed that the temperature difference of the lumped structure (i.e. the contacts and vias on the same metal line

are lumped together) and the original structure is less than 5%, mostly due to the inherent error. Hence the lumped contact and via structure can be used. The structural simplification at the contact and via regions is shown in the left figure of Fig. 5.10. The simulation results of the sub-model are discussed in the next section.

Fig. 5.10. Submodeling at the transistor region, with the inclusion of the detailed intra-block interconnect structures. The surrounding materials are removed for clarity.

5.3.2 Total AFD Distribution of the Sub-Model

The maximum total AFD of the sub-model at the end of one load cycle is also at the source interconnect of Transistor M1 as shown in Fig. 5.11, which corresponds to the simulation results of the full model in Fig. 5.5.

An increase in the value of the total AFD is observed for the sub-model as compared with that of the full model. This is due to the increase in the thermo-mechanical stress gradient after the inclusion of the detailed structures of the intra-block interconnects.

Fig. 5.11. The total AFD distribution of the sub-model of the LNA circuit (unit: atoms/μm³·s). The arrow indicates the maximum total AFD location.

The total AFD distribution and the distributions of the AFDs due to the three driving forces of the sub-model at Transistor M1 region (i.e. the region where EM is the most severe) are shown in Fig. 5.12, and the distributions of the current density, temperature gradient, and thermo-mechanical stress gradient are shown in Fig. 5.13.

As explained previously, the total AFD distribution follows the AFD_S distribution, and this agrees with the observations in Fig. 5.12(a) and (c). In addition, it is observed from Fig. 5.12(a) that, besides the sharp turn of the source interconnect of Transistor M1, the interface between Via 23 and Metal 3 (Region II in Fig. 5.3) is also a location with high total AFD values (i.e. above 6.36×10^6 atoms/μm³·s). Although the current density and the temperature gradient at the Via 23/Metal 3 interface is around half of that at the sharp turn of the source interconnect, the 90° turning of the interconnect structure at this interface builds up significant thermo-mechanical stress, as shown in Fig. 5.13(c). The thermo-

mechanical stress gradient at this region is almost 2 times larger than that at the sharp turn of the source interconnect. Therefore the Via 23/Metal 3 interface has comparably high AFD_S and total AFD values as that at the sharp turn of the source interconnect.

The Via 56/Metal 6 interface (Region III in Fig. 5.3) is another location with this kind of high stress and stress gradient built up. However, as explained in Section 5.3.1, the current density and temperature gradient at the thick metal top are more than 10 times smaller than those at the thin Metal 3 layer. The AFD_S and total AFD at this location are also more than 10 times smaller than those at the two aforementioned locations. Therefore this region is not a major concern.

From Fig. 5.13(a), besides the sharp turn of the source interconnect of Transistor M1, the contact/ Metal 1 and Via 12/Metal 2 interfaces (Region I in Fig. 5.3) of the drain interconnect of Transistor M1 is also a current crowding site and it has the highest current density, but the presence of the large amount of contacts and vias separated at a distance smaller than the thermal diffusion length (usually 1 μm to 20 μm) reduces the temperature and temperature gradient at Metal 1 [130, 131]. As a result, the maximum AFD_S and total AFD here are around 10% smaller than those at the sharp turn and the Via 23/Metal 3 interface, but the values are still higher than at other places.

Fig. 5.12. The AFD distributions due to (a) total AFD (b) electron wind force (c) thermo-mechanical stress gradient induced driving force and (d) temperature gradient induced driving force (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$) of the sub-model at Transistor M1 region, titled view from the back. The arrows indicate the locations with high total AFD.

(c)

Fig. 5.13. The distributions of (a) current density (unit: $\text{pA}/\mu\text{m}^2$) (b) temperature gradient (unit: $^\circ\text{C}/\mu\text{m}$) and (c) thermo-mechanical stress gradient (unit: $\text{MPa}/\mu\text{m}$) of the sub-model at the Transistor M1 region, titled view from the back. The arrows indicate the locations with high values.

For Transistor M3, the source and drain interconnects are in simple rectangular shape. The regularity in shape greatly reduces the current density and the temperature gradient in Metal 3. The elimination of the sharp turn in the interconnects eliminate the possible EM weak spot at this location.

Fig. 5.14. The total AFD distribution of the sub-model at Transistor M3 region (unit: $\text{atoms}/\mu\text{m}^3\cdot\text{s}$), titled view from the back. The arrow indicates the maximum total AFD location.

On the other hand, the number of contacts and vias at the Transistor M3 and M4 regions are only around 2/3 of that at the Transistor M1 and M2 regions due to their smaller transistor sizes. The current crowding at Region I and the reduced number of dummy contacts and vias causes a large rise in temperature. The location of the maximum temperature gradient coincides with that of the maximum current density for Transistor M3. The effect of the temperature gradient on the AFD_S takes over that of the thermo-mechanical stress gradient, and thus Region I becomes the place with the maximum AFD_S and total AFD, as shown in Fig. 5.14. Region II has high thermo-mechanical stress gradient of more than 3500 MPa/ μm , and the location of the 2nd highest AFD_S and total AFD is found at Region II.

In summary, this section discussed the possible EM failure sites of the LNA circuit model. It is found that, the full model is able to identify the most severe EM failure location. However, some possible failure locations are overlooked in the full model due to the over simplification in the interconnect structures. This problem is remediated by using the sub-model that includes the detailed interconnect structures at the transistor region. Additional EM failure locations due to high thermo-mechanical stress gradient are identified in the sub-model simulation.

The total AFD distribution of the circuit under the circuit operation condition is the combined effect of the three driving forces, and is not purely due to current density as one usually assumes. In fact, the location with the highest current density may (e.g. Transistor M3) or may not (e.g. Transistor M1) be the location of the maximum total AFD.

5.4 Effects of the Layout and Process Variation on the Circuit EM Reliability

As discussed in Chapter 2.4.1.3, the total AFD of the circuit is inversely proportional to the EM lifetime of the circuit. To improve the EM reliability of the circuit, the total AFD should be reduced. With the findings in the previous section, there are two possible ways for the reduction of the total AFD:

(1). Reduce the temperature gradient by:

- ♦ Reducing the current density (e.g. increase the interconnect line width).
- ♦ Relieving the degree of current crowding (e.g. use a smoother edge or a simple strip instead of the structure with a sharp turn).
- ♦ Reducing the temperature of the circuit (e.g. increase the inter-transistor distance)

(2). Reduce the thermo-mechanical stress gradient by:

- ♦ Avoiding significant geometry change.

-
- ♦ Reducing the intrinsic stress in the interconnects (e.g. decrease the SFT of the metallization).

This section shows some common practices that are usually adopted for improving the EM reliability of the circuit. The LNA model is used as an example.

5.4.1 Change in the Line Width and the Degree of Turning

The high total AFD at the sharp turn of Transistor M1 is due to the high temperature gradient at this location as a result of current crowding. It can be reduced by using a wider metal line or a smoother edge for the source interconnect of Transistor M1 as shown in Fig. 5.15. A 2.80% reduction in the maximum total AFD and a decrease in the area of the high total AFD region (i.e. the region with light blue color) at the turning corner are observed when the line width increases from 6.00 μm to 6.40 μm , as shown in in Fig. 5.16(a). This result is expected and it agrees with the observations in literature [132-134]. A further reduction of 2.80% is observed in Fig. 5.16(b) with the use of a smoother edge.

Fig. 5.15. Layout modification for the EM lifetime improvement at Transistor M1 region. (a) The original layout with a high current density at the circled region, line width $W = 6.00 \mu\text{m}$ (b) the modified layout that removes the sharp turn at the circled region, $W = 6.40 \mu\text{m}$ and (c) the modified layout with a smoother edge, $W = 6.40 \mu\text{m}$.

Fig. 5.16. The total AFD distributions of the modified layout at Transistor M1 region with (a) the sharp turn removal by using a wider metal line and (b) the use of a smoother edge (unit: atoms/ $\mu\text{m}^3 \cdot \text{s}$), titled view from the back.

Fig. 5.17 shows the decrease in the maximum total AFD with increasing line width.

Up to 16.78% reduction in the maximum total AFD and 20.17% improvement in

the EM lifetime can be achieved when the line width increases to 8.00 μm . There is no further change at above 8.00 μm .

Fig. 5.17. The maximum total AFD v.s. the line width of the source interconnect of Transistor M1.

5.4.2 Change in the Orientation of the Transistor

Fig. 5.18 shows a 16.09% reduction in the value of the maximum total AFD at the source interconnect of Transistor M1 after a 90° rotation of the transistor. The change in shape of the source interconnect eliminates the high current crowding at the turning corner, and thus effectively reduces the temperature gradient and the maximum total AFD of the circuit. However, this rotation produces another sharp turn at the inter-transistor interconnect between Transistor M1 and M2, and the improvement in lifetime may not always be possible and is case dependent.

Fig. 5.18. Total AFD distribution of the sub-model with a different orientation for Transistor M1 (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$).

Fig. 5.19 is another modified layout with the transistor finger number doubled. The presence of the two inductors around Transistor M1 forces a 90° rotation of M1, and this layout has the same transistor orientation as in Fig. 5.18. The total AFD distribution of this layout is shown in Fig. 5.20.

Fig. 5.19. The modified layout with the transistor finger number doubled. There is a limitation in space at Transistor M1 region.

Fig. 5.20. The total AFD distribution of the sub-model with the transistor finger number doubled (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$). The arrows indicate the locations with high total AFD.

As observed from Fig. 5.20, there is a significant increase in the value of the maximum total AFD for this layout version as compared with the original one and the location of the maximum total AFD moves from Transistor M1 to M2. Different from the simple two metal layer circuit models in Chapter 3 and 4, the source of the transistors of the LNA circuit is connected to the inter-block interconnects via the contacts, Metal 1, Via 12, Metal 2, Via 23 and Metal 3, as can be seen from the back view of the transistor in Fig. 5.20. The width of the source interconnect made of Metal 3 is determined by the width per finger of the transistor. When the number of fingers is doubled, the width per finger of the transistor and thus the line width of the source interconnect becomes half of that of Layout 5.2. As a result, very high current crowding is observed at the source interconnect of Transistor M1 and M2 because of the narrower Metal 3 line. The rotation of Transistor M1 eliminates the current crowding at the turning corner of the source

interconnect of Transistor M1, but the turning corner of the inter-transistor interconnect between Transistor M1 and M2 becomes another region with high total AFD (i.e. the region with light blue color) due to its small line width. The location of the maximum total AFD is found at the narrow and long source interconnect of Transistor M2 with the highest temperature gradient. The temperature gradient of the circuit almost doubles with the halved inter-block interconnect line width. 176.22% increase in the value of the maximum total AFD is observed, and the EM lifetime for this layout is expected to be less than half of that of Layout 5.2.

5.4.3 Change in the Inter-transistor Distance

Changing the placement of the electronic components is a common practice for the modification of the temperature and stress distributions in printed wiring board (PWB) and multichip module (MCM) [135-137]. This measure is tried in this circuit model.

In the LNA circuit, all the four transistors are the main heat generating sources, and their placements do have an impact on the circuit temperature. Fig. 5.21 shows two modified layouts of the LNA circuit with different inter-transistor distance. The inter-transistor distances of the original and the modified layout designs are shown in Table 12.

(a)

(b)

Fig. 5.21. The zoom-in view at the transistor region of the modified layouts with (a) the transistors placed further apart ($\sim 2x$) and (b) the transistors placed closer together (the minimum distance).

Table 12. The inter-transistor distance of the LNA circuit with different layout designs.

Horizontal Distance (μm)	Layout 5.2	Layout 5.20(a)	Layout 5.20(b)
M1 to M2	7.69	65.10	0.00
M1 to M4	132.425	218.425	34.925
M3 to M2	99.50	209.50	34.925
M3 to M4	29.175	74.125	0.00
Vertical Distance (μm)	Layout 5.2	Layout 5.20(a)	Layout 5.20(b)
M1 to M2	35.25	89.70	32.75
M1 to M4	25.40	97.35	29.175
M3 to M2	9.875	18.125	32.75
M3 to M4	2.175	25.675	29.175
Center-to-Center Distance (μm)	Layout 5.2	Layout 5.20(a)	Layout 5.20(b)
M1 to M2	36.08	110.83	32.75
M1 to M4	134.84	239.14	45.51
M3 to M2	99.99	210.28	47.88
M3 to M4	29.26	78.45	29.175

The total AFD distributions of the modified layouts are shown in Fig. 5.22. The increase in the inter-transistor distance reduces the value of the maximum total AFD with little change in the location of the maximum total AFD.

Fig. 5.22. The total AFD distributions of the modified layouts with (a) the transistors placed further apart and (b) the transistors placed closer together (unit: atoms/ $\mu\text{m}^3\cdot\text{s}$). The arrows indicate the locations with high total AFD.

The current density and thermo-mechanical stress gradient for Layout 5.2, 5.21(a) and 5.21(b) are similar due to the same current and voltage loads and similar transistor architecture. As a result, the total AFD distributions of these three

layouts are similar. The regions with high total AFD are found at the sharp turn of the source interconnect of Transistor M1, the Via 23/Metal 3 interface, and the contact/Metal 1/Via 12 interfaces of the drain interconnect, as explained in Section 5.3.2.

The impact of the inter-transistor distance on the total AFD of the models in Section 4.4 is insignificant as there is only one main heat generating transistor for that circuit. However, the inter-transistor distance does have an impact on the reliability of the LNA. In the LNA circuit, all the four transistors have significant amount heat generation due to high current flows inside the transistors. The increase in the inter-transistor distance in Layout 5.21(a) effectively reduces the temperature and temperature gradient of the circuit, resulting in a 49.23% reduction in the maximum total AFD as compared with the original layout.

As the “problematic” region consists of Transistor M1 and M2 as can be seen in Fig. 5.22, the simulation is re-done with different inter-transistor distance between Transistor M1 and M2, and the drop in the maximum total AFD with increasing inter-transistor distance is shown in Fig. 5.23. One can see from Fig. 5.23 that the impact becomes insignificant when the inter-transistor distance goes beyond 105 μm .

Fig. 5.23. The drop in the maximum total AFD with increasing inter-transistor distance (center-to-center) between Transistor M1 and M2.

For Layout 5.21(b), as the original layout is already compact enough, any further reduction in the inter-transistor distance does not cause significant rise in the circuit temperature. The maximum total AFD of Layout 5.21(b) is similar to that of Layout 5.2.

5.4.4 Change in the Stress Free Temperature of the Metallization

The high total AFD at the Via 23/Metal 3 and Via 56/Metal 6 interfaces is due to high thermo-mechanical stress gradient. Modification to the layout geometry is restricted by the design of the transistors. However, the EM lifetime is still able to be improved by decreasing the SFT of the metallization down to 250 °C [138]. With a smaller difference between the interconnect temperature and the SFT (165 °C as compared with 265 °C), the intrinsic stress in the interconnects reduces proportionally. The stress built up and hence the stress gradient at the Via 23/Metal 3 and Via 56/Metal 6 interfaces are reduced. Fig. 5.24 shows the

decrease in the maximum total AFD with decreasing SFT and it agrees with the simulation results of Roy *et al.* [139].

Fig. 5.24. Maximum total AFD v.s. stress free temperature.

In summary, when the temperature gradient and thermo-mechanical stress gradient of the model decrease, a decrease in the total maximum AFD is observed. This reflects an enhancement in the EM lifetime for the modified layout.

5.5 Summary

In this chapter, the application of the 3D finite element circuit model to a real circuit consists of both intra- and inter-block interconnects up to the metal top was demonstrated, using a RF low noise amplifier (LNA) as an example. The analysis was first carried out on a full circuit model that contained all the circuit components and interconnections. As the simplified circuit geometry structures of the full model did affect the simulation accuracy, a sub-model simulation with

the inclusion of the detailed circuit structures was performed at the problematic region as identified by the full model simulation.

The simulation results of the full model and sub-model showed great agreement and the location of the maximum total AFD was found at the sharp turn of the source interconnect of Transistor M1 with the highest temperature gradient. With the inclusion of the detailed interconnect structures, the sub-model simulation was able to identify additional EM weak spots such as the interface between Via 23 and Metal 3 (i.e. the locations with geometry irregularity and thus high thermo-mechanical stress gradient). The locations with high thermo-mechanical stress gradient had comparably high AFD values as the locations with high current density and/or high temperature gradient. These locations were prone to EM failures and may be missed out if only current density is considered. This again proved the importance of including the thermo-mechanical stress effects into EM modeling and the inadequacy of the conventional current density based EM simulators.

The current density and temperature gradient at the metal top were found to be more than 10 times smaller than those at Metal 3 due to the larger thickness of the metal top, and thus the interconnects made of the thick metal layers were not a concern in this circuit model.

Modifications were performed based on the observations in the simulation, and up to 20.17% and 59.59% improvement in the EM lifetime were achieved with the layout and the process modifications respectively. Change in the orientation of the transistor might help to reduce the value of the maximum total AFD and enhance the EM lifetime. The results agreed with the experimental results in literature and thus validated the capability of the model for correlating the layout and process modifications with the EM reliability of the circuit.

CHAPTER 6 EXPERIMENT PLAN

6.1 Introduction

The experimental verification of the 3D finite element circuit model is necessary.

A proper setup for the experiments is important to ensure accurate interpretation.

This section is organized in the following manner. In Section 6.2, the detailed experiment plan for the LNA circuit in Chapter 5 is presented. The possible difficulties faced by the experiment and the suggested solutions are discussed in Section 6.3 and the conclusions are given in Section 6.3.

6.2 Experiment Setup

The EM test for the test structure is usually conducted under high temperature (around 250 °C to 300 °C) and high current density (a few MA/cm²) condition in order to shorten the duration of the test. However, this accelerated test condition may render a change in the failure mechanism as shown by Roy *et al.* [140]. There is also a possible change in the void initiation location under the EM test condition as illustrated in Chapter 4. Moreover, different from the simple test structure with only the metallization and its surrounding materials, real circuit is much more complicated and its functionality is very sensitive to temperature. For

the proper operation of the circuit components, the test temperature of a circuit should not be too high. In order to maintain the circuit functionality, the test temperature for a circuit usually does not exceed 125 °C (it may go as high as 150 °C for some cases, depending on the packaging and the application).

As a REAL circuit structure, the LNA circuit will be used in the experiment. However, if the supply voltages and the operation temperature in Section 5.2 are used, the experiment will take extremely long test time and is not practical. Therefore a stressed condition of $1.1V_{dd}$ (i.e. 2 V) and 125 °C is used. Under this condition, there is 546.85% increase in the value of the maximum total AFD of the model without any change in the location of the maximum total AFD as verified by the ANSYS simulation, as shown in Fig. 6.1. This can effectively reduce the duration of the test and the experiment will be carried out under this stressed condition.

Fig. 6.1. The total AFD distribution of the LNA circuit at $1.1V_{dd}$ and 125 °C (unit: atoms/μm³·s).
There is 546.85% increase in the value of the maximum total AFD.

Black's equation (i.e. Eqn. (2.5)) is usually used to predict the median time to failure t_{50} of the interconnects under different conditions. Extrapolation of the EM test data is performed and the expected lifetime under the normal operation condition can be obtained. However, the high temperature (above 250 °C) and high current density (a few MA/cm²) under the EM test condition may result in different failure mechanisms from that under the normal operation condition. The acceleration factor due to high temperature and high current density may also cause an inaccurate lifetime extrapolation under the normal operation condition at wafer level [7]. The experiment will therefore be conducted at package level which is the most reliable method for the applicability of the Black's equation [7].

Beside the original layout in Fig. 5.2, the modified layouts in Section 5.4 will be tested as well, so as to compare the change in the EM lifetime with the original version. The fabricated wafer will be diced and attached to the package with the die attach that can withstand high temperature of at least 125 °C. The die will be packaged using wire bonding method with gold wires. A sample of the packaged die after wire bonding is shown in Fig. 6.2.

Fig. 6.2. A sample die after wire bonding.

High temperature operating life test will be carried out on the packaged die using high temperature oven. The temperature of the oven will be kept constant at 125 °C throughout the test. To account for the statistical nature of the fabrication process and also to reduce the experimental error, 20 to 24 samples will be used for each layout version. The samples will be mounted on a high temperature PCB board in parallel connection to ensure that the same voltage is applied to all samples. The Keithley Source Measurement Unit (SMU) model 2602A will be used to provide the sinusoidal input voltage to the circuits. The supply voltage and the bias voltages of the circuits will be provided by the DC voltage supplies.

The instantaneous voltage at the output line V_{out} will be recorded and compared with the expected V_{out} as extracted from Cadence using a comparator. The SMU will be programmed using National Instruments (NI) LabVIEW to monitor the output current I_{out} of the samples continuously. The ground line of each sample will be connected to a switch (e.g. a multiplexer) which is controlled by the comparator. The switch is able to cut off the ground voltage supply and stop the operation of the circuits under the user specified condition. The set up for the output monitoring circuit under both the circuit operation condition and the voltage cut-off condition are shown in Fig. 6.3.

Fig. 6.3. The output monitoring circuit. (a) When $V_{out} - \text{Expected } V_{out} < \Delta V$, the circuit is operating, and (b) when $V_{out} - \text{Expected } V_{out} \geq \Delta V$, the voltage supply at the ground line is cut off, the circuit operation stops and there is a step drop in the output current.

As EM progresses, the interconnect line resistance increases. This causes a decrease in the output current and voltage. Taking the LNA circuit as the example, assuming the circuit fails when there is 10% increase in the line resistance, the decrease in the output voltage is around 1.48% as determined from

Cadence. The circuit is treated as “failed” when the voltage difference ΔV between the measured and the expected V_{out} is larger than 4.88×10^{-2} V. A signal will be sent to the switch to stop the ground voltage supply of the samples so as to terminate further EM process. A step drop in I_{out} will be observed by the SMU and this represents the failure of a unit.

Individual switch and comparator will be used for each sample as shown in Fig. 6.4, so that the failure of one sample will not affect the operation of the others. The failed sample will be kept in the oven until the end of the experiment to ensure that the results of other DUT will not be affected.

Fig. 6.4. The output monitoring circuits for the samples in parallel connection.

After the experiment, the failed chips will be sent for failure analysis. The observed failure sites will be compared with the void nucleation locations identified in the simulation, and the lifetime of each layout version will be compared with the value of the maximum total AFD as calculated in the simulation.

In summary, this section presents the proposed procedures for conducting the experimental verification of the 3D finite element circuit model of the LNA circuit. To shorten the test time, the experiment will be performed at a stressed condition of $1.1V_{dd}$ and $125\text{ }^{\circ}\text{C}$. The output current and voltage of the circuit will be monitored and the chip will be treated as “failed” when there is 10% increase in the line resistance.

6.3 Possible Difficulties

There are still many potential difficulties faced by the experimental verification of the 3D finite element circuit model.

The test temperature of $125\text{ }^{\circ}\text{C}$, though is higher than the normal operation temperature of the circuit ($-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$), it is still much lower than the EM test temperature ($250\text{ }^{\circ}\text{C}$ to $300\text{ }^{\circ}\text{C}$). The duration of the experiment may still be very long and may take months to complete.

The magnitude of ΔV is only 1.48% of that of the output voltage, even with a small signal excitation of around 1 mV. To achieve a proper measurement result of the circuit, an AC input to the circuit is necessary. However, with the continuous variation of the input sinusoidal wave, the distinguish between the “real” ΔV from the normal variation of the output signal can be difficult, especially with the

presence of the noise and delay which may distort the ideal shape and magnitude and/or change the phase of the output signal. To solve this problem, the rectangular wave might be used instead of the sinusoidal wave. The comparison can be performed in the region when the output voltage becomes “flat”. Taking the RMS value of the V_{out} signal at a certain time interval (e.g. every 1 day) for the comparison may be another solution.

The magnitude and the phase differences in the measured V_{outs} of different samples also add obstacles to the comparison. Individual ΔV adjustment and monitoring for each sample is necessary.

Although the experiment at package level is able to provide a better result of the extrapolated lifetime under the normal operation condition than at wafer level, the packaging of the chip introduces additional parasitic effects to the circuit and degrades the circuit performance (e.g. delay, skew, reflections, impedance, reflections, crosstalk and power/ground fluctuations, etc., as shown in Fig. 6.5). These parasitic effects aggravate the noise and delay of the output signal and thus make it more difficult for the V_{out} comparison. To reduce the parasitic effects, flip chip packaging may be used instead of wire bonds, especially for a circuit operates at high frequency (> 1 GHz).

Fig. 6.5. Package parasitics [141].

Moreover, package failures like plastic deformation, interfacial delamination, solder fatigue and creep can be another concern. The failures in the package and the bond pad may disturb the experiment process and cause “good” unit to be treated as “failed”. Special care should be taken when choosing the package interconnection materials, underfill, substrate metallization, substrate solder mask, chip passivation, and during the processing and the assembly of the packages.

When a sudden high current spike in the input signal appears, there may be failures due to EOS/ESD and latch-up, especially for flip chip packaging. Therefore, a stable power supply is necessary.

In summary, this section introduces some possible difficulties that may present during the experiment and the measures to prevent or moderate them.

6.4 Summary

This chapter presented the experiment plan for the verification of the 3D finite element circuit model. LNA will be used for the experiments, and a stressed condition of $1.1V_{dd}$ and $125\text{ }^{\circ}\text{C}$ was used to shorten the EM test time. The failure condition was taken as 10% increase in the line resistance at the output.

Factors like the long test time, the small V_{out} difference, and the disturbance of the noise and the delay from the outside or the packages were the main difficulties faced by the experiment. Precautions and measures were suggested to prevent, or at least alleviate the problems. For example, use the rectangular wave instead of the sinusoidal wave, use individual monitoring circuit for each sample, use a suitable packaging material, etc.

CHAPTER 7 CONCLUSIONS

7.1 Conclusions

With shrinking device size and interconnect dimension, electromigration (EM) in the interconnects had become the main failure mechanism that determined IC reliability. The discussion in Chapters 1 and 2 demonstrated the increasing severity of EM on the circuit reliability with device scaling and hence the need for accurate EM modeling. The conventional physics based 3D EM models were at the “localized” regions and thus could not represent the EM reliability of the entire circuit. As current density was no longer the sole factor that determined the EM reliability, and the temperature and thermo-mechanical stress distributions of the circuit was greatly affected by the interconnect structures and the surrounding materials, the 2D EM circuit simulators based only on the current density were no longer adequate. Thus, there is a need for 3D EM modeling at the circuit layout level.

A new 3D EM modeling method at the circuit layout level using the atomic flux divergence (AFD) approach was proposed in this work. The 3D finite element circuit models were built from the 2D IC layouts, first for a simple two metal layer circuit with only the intra-block interconnects, and then for a complex circuit with the REAL circuit structures up to the metal top.

In Chapter 3, the method of constructing the 3D finite element circuit model was presented, using a simple inverter circuit as an example. Transient thermal-electric and structural-thermal analyses were performed on the circuit model using both ANSYS (a finite element software) and Cadence (a circuit simulator). The computed transient temperature response to the current and voltage changes and the transient thermo-mechanical stress response to the circuit temperature changes demonstrated the capability of the model for performing the transient temperature and stress analyses based on the activities executed by the circuit. This function was not available in the 3D models reported in literature.

The current density, temperature and temperature gradient, thermo-mechanical stress and stress gradient at any node of the 3D finite element circuit model were able to be extracted from the simulation results. The AFD due to the three driving forces as well as the total AFD of the model were computed based on these extracted values. The void nucleation location and nucleation time could be determined from the location and value of the maximum total AFD respectively, therefore the simulation results was useful in identifying the EM weak spots of the interconnects.

Models based on the inverter circuit using different barrier layer thicknesses and dielectric materials were simulated. An increase in the maximum total AFD was observed with a thinner barrier and with the use of the low- κ dielectric. The

observations agreed with the experimental results in literature and hence demonstrated the structural and material modeling capability of the proposed model.

In Chapter 4, the EM performance of the circuit model (i.e. a circuit structure) was compared with the line-via test structure under different conditions. The output stage of a class-AB amplifier was used as an example. It was found that the dominant driving force for the total AFD was different at different temperature. At the EM test temperature of 300 °C, the dominant driving force for the total AFD was the AFD due to temperature gradient induced driving force, and the locations of the maximum total AFD for both the circuit structure and the line-via test structure were at the place with the highest current density. However, at the circuit operation temperature of 90 °C, the AFD due to thermo-mechanical stress gradient induced driving force provided more than 90% contribution to the total AFD, and the current density was longer the main factor that affected EM. As such, the location of the maximum AFD depended on the product of the thermo-mechanical stress gradient and the temperature gradient, and the EM weak spots of the circuit structure were different from the line-via test structure. The normal extrapolation using the line-via test structure was therefore unable to provide an accurate EM prediction for a circuit under the circuit operation condition. This again implied the need for a complete 3D circuit modeling to ensure an accurate simulation result. Modifications to the interconnect structure of the model were performed and the simulation results agreed with the

observations in literature, indicating the accuracy of the proposed model.

In Chapter 5, a REAL circuit structure up to the metal top was constructed with the inclusion of all the circuit components and both intra- and inter-block interconnects. A simple LNA circuit was used as an example. The simulation was conducted at both the global (i.e. the full model) and the local (i.e. the sub-model) levels. The full model modeled the EM reliability for the entire circuit and was able to identify the most severe failure site. However, due to the oversimplification in structure, the full model might miss out some possible EM failure sites. This was a common problem in the 2D simulations for which the thermo-mechanical stress and stress gradient were overlooked due to structural simplification. The sub-model was used to solve this problem and additional EM weak spots due to high thermo-mechanical stress gradient were identified.

Some common practices for enhancing the EM reliability of the circuit were examined using the 3D finite element LNA model, and the results agreed well with the simulation and experimental results in literature. This demonstrated the capability of the proposed model for relating the layout and process modifications with the EM lifetime. The model could be conveniently used to predict the improvement in the circuit EM lifetime based on the EM weak spots identified.

In Chapter 6, an experiment plan with the test temperature, test method, and test

procedures was provided. The possible difficulties and the measures that could help to prevent or alleviate these problems during the experimentation were discussed as well.

7.2 Recommendations: Future Work

This work is a beginning in the research field of the 3D finite element circuit modeling. Due to the complexity of the model and the constraint in computation memory, the microstructure and back stress effects are not included in the model. However, as EM progresses, the voids may move along the grain boundaries of the interconnects and nucleate at another location [23]. Furthermore, under the effect of the back stress, the void may disappear from its original nucleation location. Therefore it is important to include these effects. The dynamic simulation of the void nucleation with the consideration of the microstructure and back stress effects of the 3D circuit model is an interesting area for further study.

The example used for the 3D model construction in this work is a single circuit containing only a few transistors. The circuits used in practical are much more complicated and may consist of hundreds or thousands of transistors and other functional blocks. The way of laying the circuit in a chip and the interactions with other blocks may affect the circuit temperature and hence the circuit reliability. These factors are not considered in the current model. Work is being

done by using the Neural Network method [142, 143] to speed up the computation, so that the proposed model will be able to be applied to large and complex circuits.

The current method does not allow for the inclusion in the design flow, and this is another area of research in the future.

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APPENDIX A

THE VOLTAGE AND CURRENT INPUTS USED IN ANSYS

Load Steps	Time (s)	V_{in} (V)	V_{out} (V)	I_{pd} (pA)	I_{ps} (pA)	I_{nd} (pA)	I_{ns} (pA)
Load Step 1	4.225×10^{-12}	3.161	-4.36×10^{-5}	2.309×10^7	2.598×10^7	-8.335×10^6	5.753×10^7
Load Step 2	1.292×10^{-11}	2.874	-1.85×10^{-4}	3.177×10^7	4.419×10^7	-1.388×10^7	6.355×10^7
Load Step 3	2.344×10^{-11}	2.526	-3.31×10^{-4}	-2.656×10^7	1.365×10^8	2.835×10^7	3.032×10^7
Load Step 4	4.385×10^{-11}	1.853	8.47×10^{-4}	-3.793×10^8	5.105×10^8	2.431×10^8	-1.704×10^8
Load Step 5	5.841×10^{-11}	1.372	4.19×10^{-3}	-6.722×10^8	8.380×10^8	3.270×10^8	-2.398×10^8
Load Step 6	7.486×10^{-11}	0.829	0.014	-9.901×10^8	1.204×10^9	1.468×10^8	-6.372×10^7
Load Step 7	1.000×10^{-10}	0.000	0.044	-1.471×10^9	1.636×10^9	2.226×10^7	9.099×10^6
Load Step 8	1.146×10^{-10}	0.000	0.066	-1.533×10^9	1.538×10^9	1.399×10^6	-1.262×10^1
Load Step 9	1.136×10^{-9}	0.000	1.376	-1.031×10^9	1.034×10^9	5.450×10^5	-1.530×10^1
Load Step 10	2.171×10^{-9}	0.000	2.214	-6.137×10^8	6.153×10^8	2.727×10^5	-1.702×10^1
Load Step 11	3.089×10^{-9}	0.000	2.659	-3.710×10^8	3.720×10^8	1.522×10^5	-1.794×10^1
Load Step 12	4.173×10^{-9}	0.000	2.960	-1.996×10^8	2.001×10^8	7.788×10^4	-1.858×10^1
Load Step 13	5.000×10^{-9}	0.000	3.092	-1.231×10^8	1.234×10^8	4.704×10^4	-1.887×10^1
Load Step 14	5.004×10^{-9}	0.141	3.092	-1.369×10^8	3.756×10^7	-2.628×10^6	-9.315×10^6
Load Step 15	5.015×10^{-9}	0.495	3.094	-1.444×10^8	1.625×10^7	-3.879×10^6	-2.434×10^7
Load Step 16	5.029×10^{-9}	0.949	3.096	-2.515×10^8	7.918×10^7	1.667×10^8	-1.967×10^8
Load Step 17	5.039×10^{-9}	1.289	3.096	-3.338×10^8	1.505×10^8	3.370×10^8	-3.647×10^8
Load Step 18	5.057×10^{-9}	1.876	3.094	-4.073×10^8	1.978×10^8	6.310×10^8	-6.704×10^8
Load Step 19	5.066×10^{-9}	2.192	3.091	-3.441×10^8	1.279×10^8	7.755×10^8	-8.346×10^8
Load Step 20	5.083×10^{-9}	2.745	3.080	-1.499×10^8	-4.341×10^7	1.048×10^9	-1.117×10^9
Load Step 21	5.100×10^{-9}	3.300	3.062	-8.654×10^7	-2.364×10^7	1.329×10^9	-1.392×10^9
Load Step 22	6.138×10^{-9}	3.300	1.772	-1.825×10^6	3.187×10^1	1.045×10^9	-1.046×10^9
Load Step 23	7.185×10^{-9}	3.300	0.925	-7.549×10^5	2.811×10^1	5.966×10^8	-5.971×10^8
Load Step 24	8.152×10^{-9}	3.300	0.489	-3.570×10^5	2.660×10^1	3.265×10^8	-3.268×10^8
Load Step 25	9.256×10^{-9}	3.300	0.230	-1.579×10^5	2.585×10^1	1.567×10^8	-1.568×10^8
Load Step 26	1.000×10^{-8}	3.300	0.138	-9.272×10^4	2.561×10^1	9.427×10^7	-9.434×10^7

* V_{dd} and Gnd are fixed at 3.3 V and 0 V respectively.