Design, simulation and fabrication of silicon nanowire based nanoelectronics devices

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**DESIGN, SIMULATION AND FABRICATION
OF SILICON NANOWIRE BASED
NANO-ELECTRONICS DEVICES**

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**SCHOOL OF ELECTRICAL & ELECTRONIC
ENGINEERING**

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**Design, Simulation and Fabrication
of Silicon Nanowire based Nanoelectronics
Devices**

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Abstract

Silicon nanowire (SiNW) has drawn great research attention in recent years due to its high aspect ratio and unique electrical properties, which arise from quantum confinement effects and changes in the wave function of charge carriers, density of states, effective mass and bandgap. It has the potential to become the building block of next generation electronics devices. SiNW fabricated using the top-down approach is advantageous compared to the bottom-up approach as the process is compatible with silicon CMOS process and can be integrated with conventional silicon devices. It also allows large scale integration and hence is attractive from the prospective of manufacturability. The objective of this work is to design, simulate, fabricate and characterize SiNW based nanoelectronics devices synthesized with the CMOS compatible top-down approach, where silicon fins are patterned with optical lithography and subsequently oxidized and reduced to form SiNWs. Three SiNW based devices have been investigated in this work, which are Schottky barrier diode, single-electron transistor and p-i-n junctions array.

SiNW Schottky barrier diodes (SBDs) were formed between N-type SiNWs and nickel silicide. The top-down approach was used to achieve SiNWs with a cross-sectional dimension of ~120 nm. Ni was deposited and annealed, and reacted completely with the SiNWs underneath to form nickel silicide. The SBDs formed between the SiNWs and nickel silicide reveal strong rectifying characteristic. The devices exhibit a high breakdown voltage of at least 70% of the theoretical ideal value, attributed to the unique structure of the SiNW SBDs which does not suffer

from field crowding, as also confirmed by our simulation results. This is an important advantage compared with bulk devices where complicated termination techniques have to be employed to alleviate field crowding and improve the breakdown voltage.

Top-down SiNWs fabricated from deep-UV lithography and subsequent thermal oxidation have been applied to build single-electron transistors (SETs). The SETs exhibit strong Coulomb oscillation at room temperature due to the extreme small size of the SiNWs with a diameter of 4 nm. Our approach for the fabrication of SETs using optical lithography is advantageous as compared to the most widely used electron beam lithography technique because it offers the possibility of integrating silicon single-electron electronics with CMOS technology. The effects of different oxidation induced tensile strain on the formation of tunneling barriers in SiNW based SET are investigated by designing SiNWs with different lengths, from 200 nm to 500 nm. Coulomb blockade oscillations are found to be more prominent for longer than shorter SiNWs. For the shortest device of 200 nm, no oscillation is observed and the $I_d - V_g$ curve reverts to that of a typical MOSFET. The results are interpreted in terms of the effect of SiNW length on the oxidation induced tensile strain, and consequently the tunneling barrier height developed in the wires. The study reveals that the SiNW length is a crucial parameter in the design of SiNW based SETs.

P-i-n junctions were fabricated along SiNWs via the top-down approach using deep-UV lithography. Each device comprises 500 identical SiNWs connected in

parallel, and each SiNW has a triangular cross-section with dimensions of ~6 nm (base) by ~8 nm (height). The photodiodes exhibit very good rectifying electrical characteristics with a low reverse bias current of ~0.2 fA per SiNW. It is observed that the photocurrent spectral response exhibits three peaks between 400 nm to 700 nm, which arise due to local optical field enhancement associated with diffraction by the periodic SiNW array and interference in an air/SiO₂/silicon structure. Our results suggest that it is possible to engineer light absorption by designing multiple SiNWs in parallel to selectively enhance absorption for specific sensing applications.

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Chapter 1 Introduction

1.1 Motivation

Silicon nanowire (SiNW) has drawn great attention in recent years due to its small dimension, high aspect ratio and quantum confinement effect, which give rise to unique electrical properties that are not available from bulk Si [1-4] . Due to the quantum confinement, the wave function of the charge carriers, density of states, effective mass, energy band structures and bandgap of SiNW are substantially different from those of bulk Si. Dimension plays an important role in determining the properties of a material at nanoscale because electrons behave very differently when they are under physical confinement. Quasi low dimension devices have been shown to exhibit superior electrical, optical, mechanical as well as thermal properties [5-7] which may not be observable in corresponding bulk devices.

SiNW is also considered as an excellent candidate for studying quasi-one-dimension semiconductor since the bulk counterpart is one of the most well studied and understood materials. Besides, quasi-one-dimension SiNW is viewed as the most promising building blocks for nano-scale devices in the future, potentially leveraging on the well-developed silicon complementary metal–oxide–semiconductor (CMOS) process technology. For example, SiNW based Schottky barrier transistors have been demonstrated to exhibit excellent current on–off ratio and reduced leakage current [1]. SiNW fabricated with electron beam lithography has also been applied as the channel for single-electron transistor, with single

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electron memory effect successfully demonstrated at room temperature [8]. In the area of nanophotonics, single SiNW based high resolution p-i-n junction photodiodes have been investigated and the possibility of realization of nanoscale avalanche photodetector using single SiNW has been demonstrated [9]. In addition, other SiNWs based devices ranging from chemical and biological sensors to integrated circuits etc have been successfully demonstrated with improved performance [1, 8, 10, 11]. These results suggest the great potential of SiNW based devices for various applications with improved performance and realization of devices with novel operating principles that are different from those of their bulk silicon counterpart. There is no doubt that SiNWs will be the new focal point of research beyond conventional silicon CMOS devices.

There are several methods that have been used to fabricate high aspect ratio SiNWs. They are mainly grouped under two categories, the top-down [8, 12, 13] approach and the bottom-up [14-17] approach. The top-down approach fabricates SiNWs using methods such as lithography, etching and self-limiting oxidation [8, 12, 13]. It is compatible with silicon CMOS process and can be easily integrated on a large scale with conventional silicon devices. Therefore, it is attractive from manufacturability perspective. On the other hand, the bottom-up approach grows SiNWs using the metal-catalyzed chemical vapor deposition (CVD) technique [16]. Free-standing SiNWs are directly grown from metal catalyst which promises low-cost production of SiNWs. However, the bottom-up approach faces the challenge of exact placement of nanowires to allow high level and large scale integration.

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1.2 Objectives

In this project, the top-down process is adopted to fabricate SiNWs and three types of SiNWs based devices, namely, Schottky barrier diodes (SBDs), single electron transistors (SETs) and p-i-n junctions array. The scope of the research work includes the design, fabrication, characterization and simulation of the above devices. The objectives of this study are summarized as follows:

(i) Study SiNWs fabricated with the top-down approach using conventional optical lithography and CMOS compatible process. The SiNWs formed are subsequently used for the fabrication of three different types of electronic devices with improved performance and functionality.

(ii) Study SiNW based SBDs and investigate their detailed electrical properties. We will specifically focus on the study of their breakdown characteristic, which may be much improved compared to the corresponding bulk devices. The unique structure of the devices with the Schottky barrier junction formed along the longitudinal direction of the SiNWs is expected to alleviate electric field crowding effect that occurs in typical bulk devices, and hence improve the breakdown performance. We will also carry out device simulation to study and compare electric field distributions in the SiNWs based SBDs and corresponding bulk devices of the same doping, and relate them to the physical structures of the devices.

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- (iii) Research on SiNWs based single electron transistors (SETs) and study their electrical characteristics at room temperature and low temperature. We will focus on investigating single electron transport in such devices and its dependency on temperature and the length of the SiNWs. The effects of oxidation induced tensile strain on the characteristics of the SiNWs based SETs will be examined. The origin of the formation of tunneling barriers within the SiNWs that accounts for the operation of the SET will be investigated.

- (iv) Study SiNWs based p-i-n junctions that comprise multiple identical SiNWs connected in parallel. The electrical performance and photocurrent spectral response of the devices will be investigated in detail. Simulation of the device absorption and hence photocurrent response will be carried out and compared with the experimental results.

1.3 Major contribution of the thesis

SiNWs with diameters down to several nanometers have been successfully fabricated by thermal oxidization of silicon fins defined by optical lithography. The process is compatible with conventional CMOS fabrication and thus is advantageous from the perspective of manufacturing. It also provides the possibility to integrate SiNWs based devices with conventional CMOS devices on a large scale, and consequently expand and enhance their functionality. Based on the SiNWs fabricated, three types of SiNWs based devices which include Schottky

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barrier diode, single-electron transistor and p-i-n junctions array have been successfully fabricated and characterized.

SiNWs Schottky barrier diodes (SBDs) have been designed and fabricated using the top-down approach with nickel silicide as the Schottky metal. The SiNW has a cross-sectional dimension of ~ 120 nm. The current-voltage results of the devices exhibit strong rectifying characteristic which confirms that SBDs have been successfully formed. High breakdown voltage of at least 70% of the theoretical value has been achieved for the devices in the absence of complex edge-termination techniques, which are commonly employed in bulk devices to alleviate electric-field crowding near the metal edges. This is attributed to the unique structure of the SiNWs based SBDs with the Schottky metal of comparable or even larger contact area than the SiNWs, resulting in more uniform distribution of the electric field near the Schottky metal contact. The conclusion is also confirmed by device simulation comparing the electric field distributions between the SiNWs based SBDs devices and bulk SBDs of the same doping subjected to the same bias condition.

SiNWs are used to fabricate single-electron transistors (SETs) through the top-down approach using conventional deep-UV lithography. The devices have the same structure as n-type gate-all-around SiNWs MOSFETs, with ~ 4 nm channel width. Attributed to the small dimensions of the SiNWs, pronounced Coulomb oscillation can be observed in the I_d - V_g characteristics of the devices under room

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temperature. Increased peak-to-valley ratio of the drain current oscillations is also noted at lower temperature, which further confirms the presence of single-electron transport.

The effects of oxidation-induced tensile strain on the formation of tunneling barriers in SiNW based SET are studied as well. Different tensile strain was induced in the SiNWs by designing SiNWs with different lengths from 200 nm to 500 nm. The measurement results show that Coulomb blockade oscillation becomes weakened for SiNWs of shorter length, attributed to the lowering of the tunneling barrier as a result of the reduced oxidation induced tensile strain. For the shortest device with a SiNW length of 200 nm, the $I_d - V_g$ characteristic reverts to that of a typical MOSFET. The result confirms the proposition that formation of SET in SiNW device is attributed to a combination of quantum confinement effect and strain induced barrier lowering in extremely small nanowires. Besides, the results indicate that the length of SiNWs is a crucial parameter in the design of SiNW based SETs devices.

SiNW p-i-n junctions with 500 identical SiNWs connected in parallel are fabricated by the top-down approach with deep-UV lithography. The SiNWs have a cross-sectional dimension less than 10 nm. The devices exhibit very good rectifying characteristic of up to 9 orders of magnitude between forward and reverse bias, and very low reverse bias current of ~ 0.2 fA per SiNW as a result of the extremely small SiNW dimension. It is noted that three responsivity peaks exist

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in the photocurrent spectral response of the device between 400 nm and 700 nm. Our simulation results confirmed that the resonant peaks observed are attributed to local optical field enhancement associated with diffraction by the periodic SiNW array and interference in an air/SiO₂/silicon structure. The results suggest it is possible to engineer light absorption at specific wavelengths with the multiple SiNWs p-i-n junctions array structure.

1.4 Organization of the thesis

This thesis consists of seven chapters. The first chapter covers the motivation, objectives and major contributions of this work. The second chapter presents a literature review of the unique properties of SiNW as compared to bulk silicon and SiNW based nanoelectronics devices. The third chapter introduces the techniques used in this work to fabricate SiNWs and characterize SiNWs based devices. Chapter four discusses the fabrication, simulation and characterization of SiNW based Schottky barrier diodes with near ideal break down voltage. A detailed analysis of the high breakdown voltage of the devices is presented and its origin is established. Chapter five details the design, fabrication and characterization of SiNW based single electron transistors operated under room temperature. The mechanism of single-electron transport has been investigated and verified experimentally. Chapter six presents the design, fabrication and characterization of SiNWs based p-i-n junctions array. The electrical and photocurrent properties of the devices have been studied and the latter has been verified using 2-D finite-

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element-method simulation. Chapter seven summarizes the work done in this project and includes recommendations for future work.

Chapter 2 Literature review

This chapter reviews the research work reported in the literature on silicon nanowires (SiNWs), including their synthesis and applications. The chapter begins by examining the unique properties of SiNW that arise owing to its one-dimension structure. Common fabrication approaches to synthesize SiNWs will be discussed and various applications that have been realized with SiNWs with improved performance will be presented.

2.1 Silicon nanowire properties

SiNW offer unique properties compared to its bulk counterpart as a result of its one-dimension structure. As the dimension of SiNW decreases, quantum confinement effect becomes more prominent. This in turn modifies the band structure and effective mass of carriers. Several research groups have reported increased bandgap energy for SiNWs with smaller dimension from the calculation of the electronic density of state (DOS) of silicon nanostructures [18-20]. Fig. 2.1 shows the simulation results of energy band gap as a function of confinement parameter $1/d$ for different silicon nanostructures such as SiNW, Si slab and nanoclusters based on various first principle methods such as density functional theory with self-energy correction, effective mass model and finite barrier effective mass model [19].

Fig. 2.1 Energy gap versus confinement parameter $1/d$ calculated with density functional theory with self-energy correction (Dots); effective mass model (Dash lines) and finite barrier effective mass model (Full lines) [19].

Experimental investigation of SiNWs bandgap has been carried out using scanning tunneling microscopy (SEM) [21]. SiNWs with diameter from 1 nm to 7 nm were prepared by an oxide-assisted growth method [22]. The oxide sheath was subsequently removed and the SiNW surface was terminated by hydrogen through a hydrofluoric acid dip [21]. The experimental results have demonstrated that there was an increase in the bandgap energy from 1.1 eV to 1.3 eV as the SiNW diameter shrank from 7 nm to 1.3 nm [21]. The results are in good agreement with previously reported theoretical predictions [18-20] and provide experimental

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evidence of quantum confinement effect on the DOS of SiNWs, as shown in Fig. 2.2 [21].

Fig. 2.2 Experimental band gap versus diameter of SiNWs [21]. Also shown are the calculated diameter-dependent band gaps of (circles) Read et al.[19] and (triangles) Delley and Steigmeier [20].

Quantum confinement of carriers in SiNWs also affects their optical properties, which has been verified by photoluminescence measurement [23]. The blueshift of the optical absorption edge along with the intense red photoluminescence peak has been observed from SiNWs prepared by pulsed-laser vaporization of heated silicon (mixed with metal catalyst) target. It is also noted that the peak of the red emission centers at different energies for SiNWs of different diameters, which correspond to different bandgap energies as a result of quantum confinement at small dimension [23].

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2.2 Silicon nanowire fabrications

In the last few years, several techniques have been proposed to fabricate SiNWs. These methods can be generally classified under two groups: the top-down approach and the bottom-up approach. The top-down approach employs lithography and etching to define nano-scale silicon fins/SiNWs structure, whose dimension can then be further reduced by thermal oxidation. The lithography techniques used include both electron beam lithography and optical lithography. On the other hand, the bottom-up approach employs vapor-liquid-solid (VLS) technique to synthesize SiNWs. Metallic nanoclusters are often used as catalyst to chemically grow SiNWs from the source material, which can be derived either from a feed gas (such as silane for Si) or from laser-assisted ablation of Si target. The dimension of the SiNWs is controllable by the size of metallic nanoclusters and the length can be adjusted by turning on or off the supply of source material. In the following, a detailed discussion of the two approaches used for the fabrication of SiNWs will be presented.

2.2.1 Top-down approach

Electron beam lithography can be used to define nano-scale SiNW/silicon fin pattern directly on Si wafer. This approach was commonly used in the earlier studies of SiNW fabrication [8, 24]. Silicon on insulator (SOI) wafers were used as the starting substrates so that the SiNWs fabricated will be electrically isolated from the substrates. Fig. 2.3 shows the process flow of SiNW fabrication using inorganic electron beam resist process [8]. The process inherits the capabilities of

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conventional electron beam lithography process but uses an inorganic resist. With the use of inorganic resist, secondary electrons resulting from primary electron beam scattering are much suppressed, leading to higher resolution than the conventional organic electron beam resist process [8]. Besides, inorganic electron beam resist process has high scalability with small deviations in critical dimension (CD). Therefore it is suitable for fabricating silicon nanostructure devices where the design of shape, size, and position demand high precision lithography. SiNW with width as small as 15 nm was demonstrated [8]. Although electron beam lithography enjoys process simplicity as optical mask is not required, inherent low throughput issue of this technique limits its application in mass production.

Fig. 2.3 Silicon nanowire fabrication using inorganic electron beam resist process on SOI substrate.

It is possible to reduce the dimension of silicon fins/SiNWs using thermal oxidation after they are formed [12]. In this technique, the silicon layer on a SOI wafer was first thinned by oxidation and electron beam resist, PMMA, was then spun onto the surface. Following that the wire pattern was defined using electron beam lithography. After resist development, a layer of metal was evaporated onto

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the resist as well as the developed region to serve as a masking layer for the etching. Subsequently, the metal layer on top of the resist was lifted off and an anisotropic silicon plasma etch was carried out at high RF power to form SiNWs [12]. The wires were then oxidized at 875 °C to further reduce the wire diameter in a self-limiting manner. This temperature was chosen because self-limiting oxidation phenomenon is not prominent for temperature higher than 950°C [25]. Stress generated in the SiNWs during the oxidation process prevents them from being oxidized completely. Eventually, at a certain radius, the oxidation process slows down and a thin silicon core is formed. SiNWs down to 8 nm in diameter were successfully achieved by this approach, as demonstrated in Fig. 2.4 [12].

Fig. 2.4 TEM cross section images of SiNW after thermal oxidation [12].

Besides electron beam lithography, it has been demonstrated that SiNWs can be fabricated using optical lithography followed by controlled thermal oxidation [13]. By using alternating phase-shift mask technique, the photolithography resolution is

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greatly enhanced. The photoresist pattern developed can be further trimmed to reduce the silicon fin dimension formed [13]. This process is fully compatible with CMOS technology and allows the possibility of large-scale integration and production. SiNWs based high performance gate-all-around CMOS devices have been achieved by this fabrication technique and the SiNW diameter was reported to be less than 5 nm [13].

Fig. 2.5 Cross section SEM images of SiNW fabricated using NIL technique at different tilting angles [26].

Several groups demonstrate that it is also possible to define SiNW based on nanoimprint lithography (NIL) [26-28]. Fig. 2.5 shows the SEM micrograph of SiNW fabricated by NIL technique on SOI substrate. The average diameter of the SiNW defined is 76 ± 5 nm [26]. The NIL technique allows definition of SiNWs over a large area of wafer with high density and high uniformity. It has two main steps, imprinting and pattern transfer [29]. For imprinting, a thin layer of imprint resist, which is a thermal plastic that deforms readily upon heating, is spin coated onto the substrate. The mold with the SiNW patterns is then brought into close

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contact with the substrate and they are pressed together under certain pressure. When the imprint resist is heated up above its glass transition temperature, it will deform and the pattern on the mold is pressed into the softened polymer film. For pattern transfer, the mold is removed after cooling and an anisotropic etch process, such as reactive ion etching, is used to remove the residual resist in the compressed area. The pattern of the mold is then fully transferred to the imprint resist [29]. The resolution of NIL is not limited by the optical interference or diffraction of light, which is advantageous as compared to conventional lithography. Moreover the process steps involved are also much simpler than optical lithography. However, NIL suffers from drawbacks such as the low throughput of template patterning and accelerated wear of template due to substantial pressure exerted during printing process.

2.2.2 Bottom-up approach

The bottom-up approach generally involves growing SiNWs on metal nanoclusters which serve as catalyst. This approach could be used to fabricate a large amount of SiNWs at relatively low cost. One common technique using this approach to synthesize SiNWs is VLS growth [14-17]. This technique allows the growth of SiNWs with small and controllable diameter without using fine-scale lithography. There are two possible ways to provide the source material silicon to grow SiNWs: from feed gas containing silicon atoms (such as silane) or from laser-assisted ablation of Si target.

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To grow SiNWs from silane or other feed gas containing silicon atoms, metal nanoclusters are first formed on the substrate. This can be achieved by evaporation or CVD deposition of a thin metal film followed by thermal annealing. The metal film will agglomerate after annealing to form nanoclusters. The structure is then exposed to precursor gas, which contains silicon atoms, in a chemical vapor deposition reactor. The vapor phase species, such as silane, are transported between the metal nanoclusters and the underlying surface of the silicon substrate. Dissolution of vapor phase reactants into liquid metallic nanocluster catalyst forms alloys which are eutectic compound. Silicon will precipitate and nucleate upon saturation at an appropriate temperature. Subsequently the metallic nanoclusters are pushed away from the substrate surface, leaving columns of silicon behind to form SiNWs. The whole process is illustrated in Fig. 2.6 [16]. In this process the size of the metallic nanoclusters determines the diameter of the grown SiNWs, and a good control over the SiNW dimension has been demonstrated [30]. Also, the length of the SiNWs can be controlled by the growth time.

Fig. 2.6 Growth of SiNWs using the VLS technique. Metal nanoclusters accelerate the decomposition of a silicon-containing gas. The silicon atoms precipitate between the nanocluster and the substrate, forming a column of silicon [16].

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It is also possible to synthesize SiNWs using the laser ablation-condensation technique [15, 31], in which laser-ablated particles serve as the source material to grow SiNWs. The schematic of the experimental apparatus is illustrated in Fig. 2.7. The target consists of silicon and the catalyst material. A pulse laser is used to produce nano-scale catalyst clusters within the reaction chamber at 1200 °C. The ablated materials are then carried by an argon gas flow. The growth of SiNWs occurs when the catalyst clusters remain in liquid phase and stops once the catalyst particles are moved away from the hot zone. After the growth, SiNWs can be collected at the cold finger. TEM images of SiNWs produced by this technique are shown in Fig 2.8 [31].

Fig. 2.7 Schematic of the laser ablation-condensation technique apparatus for the production of SiNWs [15].

Fig. 2.8 (a) TEM images of silicon nanowires produced after laser ablating a Si_{0.9}Fe_{0.1} target. (b) Diffraction contrast TEM image of a SiNW. The crystalline silicon core appears darker than the amorphous oxide surface layer. The inset shows the convergent beam electron diffraction pattern recorded perpendicular to the wire axis [31].

There are pros and cons of each fabrication approach. As discussed above, the top-down fabrication approach uses optical or E-beam lithography followed by etching to define nano-scale silicon structures. Thermal oxidation can be used to further reduce the dimension of the SiNWs. The top-down approach processes the advantage of better compatibility with CMOS technology and it allows a precise control and integration of SiNWs with devices fabricated using conventional CMOS technology. Thus large-scale integrated circuit which consists of both CMOS transistors and SiNW based devices can be realized on a single chip, and provides great potential in various applications. However, to produce SiNWs with high packing density, high lithography resolution is needed. This will put extreme demand on equipment and hence incur high cost.

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On the other hand, the bottom-up approach can produce large amount of SiNWs at the same time with low cost. SiNWs can be grown from nanoclusters of metal catalyst through exposure to silane or other feed gas containing silicon atoms. It is possible to control the diameter of the SiNW grown by the metal nanocluster size. Also, the length of SiNWs can be adjusted by turning off the supply feed gas. However, it is difficult control the growth orientation of the SiNWs which imposes difficulty for device fabrication with high degree of reproducibility. It is also challenging to place and assemble the fabricated SiNWs with a few nanometers diameter to the desired location and to integrate the SiNW with other devices fabricated using conventional CMOS technology. This greatly impedes the application of SiNWs synthesized using the bottom-up approach in large scale integrated circuit.

2.3 Silicon nanowire applications

2.3.1 Silicon nanowire field effect transistor

SiNWs have been employed as channels of field effect transistors [13, 32-34]. The devices are demonstrated to exhibit many attractive attributes, such as excellent electrostatic control of the channel, near ideal sub-threshold slope, low drain-induced barrier lowering and high I_{on}/I_{off} ratio [13]. Transport characteristics of vertically integrated nanowire field effect transistors have also been investigated by J. Goldberger *et. al* [17]. The devices show transport property which are within the same order of magnitude as horizontal nanowire field effect transistors [17]. Thermal annealing and passivation of oxide defects by chemical modification were found to be crucial in improving the source-drain contact and hence transport characteristics of the SiNW based field effect transistors [25, 30]. The average transconductance of the SiNW field effect transistor was found to increase from 45 nS to 800 nS and average mobility from 30 to 560 $\text{cm}^2/\text{V s}$, with peak values of 2000 nS and 1350 $\text{cm}^2/\text{V s}$ respectively, after thermal annealing. The transport characteristics and key parameters of SiNW field effect transistors have demonstrated many advantages as compared to the corresponding planar silicon devices [25]. Therefore, they have great potential to be the building blocks of future electronics devices.

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2.3.2 Silicon nanowire sensors

SiNW was an appealing candidate for chemical and biological sensing applications [4, 35-37]. X. T. Zhou *et. al* [10] have prepared bundles of SiNWs using the oxide-assisted growth technique and attached them to silver electrode for ammonium gas sensing application. It was observed that the electrical conductance of SiNWs was extremely sensitive to the ammonia gas concentration. The sensitivity could be further increased by removing the surrounding thermal oxide using HF solution, since it acts as a shielding barrier to the NH_3 gas [10]. Besides vapor phase ammonium, SiNWs have also shown high sensitivity to liquid phase solution of nitrobenzene and phenol in cyclohexane [26]. The results indicated that the sensing mechanism was based on charge transfer between the analytes and the SiNWs, which scaled according to the concentration of the organic solutions.

As sensors, SiNWs possess the advantage of high sensitivity such that only a small quantity of analytes is required for the sensing process. They are also miniaturized in size and are also compatible with conventional silicon integrated circuits, which allow large-scale integration of sensor arrays. Hence SiNWs are promising candidate for sensing application. Development of silicon micro-needle with integrated SiNW sensor on SOI wafer for the detection of biochemical within or outside individual live cells has been fabricated by I. Park *et. al* [11]. The SEM image of fabricated SiNW based biomedical sensor is shown in Fig. 2.9. This sensor demonstrates the potential for studying individual cell or localized bioenvironment by revealing the pH level and/or enzyme activities [11].

Fig. 2.9 SEM image of a fabricated silicon nanowire of 50 nm width on a microneedle for intracellular biomedical detection.

2.3.3 Silicon nanowire photonics

SiNWs have also been assembled to form nano-scale photonic devices [9, 38-40]. For example, nanowire avalanche photodiodes (nanoAPDs) have been demonstrated with crossed P-type SiNW and cadmium sulphide (CdS) nanowires, as shown in Fig. 2.10. It was observed that nanoAPDs offer extremely high sensitivity with detection limit less than 100 photons. A multiplication factor of about 5×10^4 was observed for sub-breakdown bias due to impact ionization [38]. As a result of their miniaturized size, it is possible to integrate SiNWs based nanophotonics devices with nanoelectronics devices to offer promising opportunities in various applications such as communication and computing [38].

Fig. 2.10 SEM image of the n-CdS/p-Si nanowire device. The scale bar is 4 μm [38].

Chapter 3 Fabrication and characterization methodology

This chapter presents the experimental techniques to fabricate SiNWs and characterize SiNWs based devices. The chapter starts with a detailed description of the process used for the fabrication of SiNWs applied in all the devices studied in this work. It is based on the top-down approach that involves the patterning of Si-fins by optical lithography and their subsequent thermal oxidation to reduce the size to nanometer range. Following that, the electrical and optical characterization techniques applied to characterize the SiNWs based device are demonstrated.

3.1 Silicon nanowire fabrication

The SiNWs used for the fabrication of all the three types of SiNWs based devices, namely, Schottky barrier diodes, single electron transistor and p-i-n junctions array have been fabricated using the top-down approach based on conventional optical lithography. Si-fins were first defined and transferred to the top layer of SOI wafers, and subsequently oxidized to form SiNWs. The process was carried out without using E-beam lithography, and hence potentially allows the integration of SiNWs based devices with CMOS devices. The Schottky barrier diodes were built based on SiNWs with dimension of around 120 nm. The process was conducted in the Nanyang Nano-Fabrication Center in Nanyang Technological University (NTU). For SiNW based single electron transistors and p-i-n junctions, nanowires with a diameter less than 10 nm were used and the fabrication process was carried out in the Institute of Microelectronics, Singapore (IME). The general steps

Chapter 3 Fabrication and characterization methodology

involved in the fabrication of SiNWs for all the devices will be briefly described in this chapter, whereas the detailed specific steps for individual device built on these SiNWs will be presented in the corresponding chapters in which the devices will be discussed.

3.1.1 Silicon fin patterning

The fabrication process for all the three types of SiNWs based devices fabricated in this work starts off with the use of silicon-on-insulator (SOI) wafers. The buried oxide (BOX) in the SOI wafer serves as an isolation layer between the top silicon layer and the silicon substrate underneath. The BOX isolation also ensures that Si fins defined on top of it will shrink to form isolated SiNW after thermal oxidation.

Optical lithography was used to transfer I-shape silicon island onto the top silicon layer. The silicon island consisted of thin Si-fins which were connected to two big silicon contact pads, as shown in Fig 3.1.

Fig. 3.1 Silicon island pattern used to fabricate Si-fins and hence SiNWs.

Chapter 3 Fabrication and characterization methodology

For SiNWs fabricated in NTU for SBDs, the alignment and exposure were done by the Canon PLA601 contact aligner and the pattern was then developed by AIO resist spin-coat/develop system. The photolithography process has the following steps that include dehydration bake, vapor prime, photoresist spin coat, soft-bake, alignment and exposure, post-exposure bake, develop, hard-bake and develop inspect. Silicon fins with a line width of 1.6 μm were obtained due to the constraint of the lithography limit of the system. LAM Research 4420 Poly/Nitride Etcher was then used for plasma etching of field silicon to achieve the Si-fins.

For the SiNWs fabricated in IME to form SETs and p-i-n junctions, much smaller initial Si-fin size was needed to ultimately achieve SiNWs with diameters less than 10 nm. Alternating phase shift mask lithography was used to define Si-fins and KrF excimer laser with wavelength of 248 nm was used as light source for exposure. Sulfuric acid and hydrogen peroxide mixture (SPM) was used to clean the wafer. After the wafers were dried by spinning, they were baked for 5 mins at 300 °C to drive out moisture. To minimize the reflection at the wafer surface during exposure, a layer of anti-reflecting coating material with thickness of 60 nm was coated on the wafers. After that photoresist with thickness of 320 nm was deposited onto the wafers. Pre-exposure bake was carried out to harden the photoresist by driving out the solvent. After exposure and development, photoresist in the field region was removed. The width of the patterned photoresist was around 120 nm as determined from the critical dimension scanning electron microscope.

Chapter 3 Fabrication and characterization methodology

The width of the patterned photoresist was subsequently reduced further by oxygen plasma etch. During this process, the width of the patterned photoresist was reduced gradually to 40 - 45 nm from the initial ~120 nm. This step is important to achieve a much smaller critical dimension than the optical lithography limit. Silicon etch recipe with a gaseous mixture of octafluorocyclobutane (C_4F_8) and sulfur hexafluoride (SF_6) was applied to etch away the silicon down to the BOX layer, to transfer the pattern to silicon layer of SOI wafer.

3.1.2 Thermal oxidation

After strip of photoresist, thermal oxidation was carried out to reduce the dimension of silicon fins to nano-scale. The structure of Si-fins sitting on top of BOX ensures that the fins are isolated and hence SiNWs are formed after thermal oxidation. For SiNWs fabricated in NTU for SBDs, two rounds of wet oxidation were performed with oxidation time of 340 mins and 85 mins in oxidation furnaces. Wet oxidization was used to accelerate the process because the initial silicon fin has a large dimension of 1.6 μm . The first round of oxidation was carried out at 1100 $^{\circ}C$ for 340 mins with 5 *SLM* flow rate of O_2 and 8 *SLM* of H_2 . Thermal oxide covering the silicon core was removed by isotropic wet etching after first round of oxidation to speed up the subsequent oxidation process. The second round of thermal oxidation was carried out at 950 $^{\circ}C$ for 85 mins with the same flow rates of O_2 and H_2 . The final dimensions of SiNWs fabricated were around 120 nm.

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For SiNWs fabricated in IME for SET and p-i-n junctions, patterned silicon fins were oxidized in dry oxygen ambient at 875 °C for 4 hours. Dry oxidation was used because the initial dimension of silicon fins is quite small of about 40 to 45 nm. Dry oxidation was considerably slower than wet oxidation and hence provided better control of the rate of the oxidation process. The final dimensions of the SiNWs fabricated were less than 10 nm.

The details of the fabrication process of SBDs, SETs and p-i-n junctions array based on SiNWs will be presented from chapters 4 to 6. The morphology characterization results of the SiNWs obtained for each device are presented separately in section 4.2, 5.2 and 6.2.

3.2 Device characterization techniques

3.2.1 Electrical characterization

The current-voltage characteristics of all fabricated devices under room temperature (300K) were measured with a Keithley 4200-SCS semiconductor parameter analyzer connected to SUSS Microtec probe station (See Fig. 3.2 and Fig. 3.3). The equipment is located in Semiconductor Characterization Lab 2, Nanyang Technological University, Singapore. Two-terminal measurements for SBDs and p-i-n junctions as well as three-terminal measurements for SETs were carried out by probing pins onto the contact pads of the respective devices. The measurement precision of the probe station is as low as 10^{-14} A. This is achieved with installation of preamplifier for low current range, which is essential to capture

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the small current signal of our devices due to the extremely small SiNW dimensions. Current limits were also set during the measurement of all devices to prevent electrical breakdown of the devices due to accidental high current.

Fig. 3.2 SUSS Microtec probe system used in this work for sample probing

Fig. 3.3 Keithley 4200-SCS semiconductor parameter analyzer with current measurement precision as low as 10^{-14} A

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Low temperature current-voltage characteristics up to 77 K were measured by connecting a cryogenic prober (PLC50) to the Keithley 4200-SCS semiconductor parameter analyzer in the same lab (See Fig. 3.4). During measurement the sample was placed in a 2-inch chuck and stuck to the chuck by thermally conductive glue. The chuck was first vacuumed by a pump and then the temperature was cooled down by liquid nitrogen until 77 K. A separate heater can be used to heat the chuck such that the chuck temperature can be varied from 77 K to 300 K.

Fig. 3.4 Cryogenic prober (PLC50) used in this work for low temperature I - V characterization up to 77K.

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3.2.2 Optical characterization

For optical characterization of the SiNWs p-i-n junction arrays, it is necessary to measure their behavior under light illumination. Moreover, it is important to characterize their photocurrent spectral response, i.e., the photocurrent generated in the devices under light illumination of different wavelengths. Despite the small dimension of the SiNWs in the p-i-n junctions array, it was found that the devices responded well to illumination because of the large number of identical SiNWs that are connected in parallel.

The optical characterization system was set up in Centre for Advance Nanotechnology, University of Toronto, Canada. The optical characterization of p-i-n junctions array was carried out by our collaborators Mr. Joe Salfi, Christina Souza and Prof. Harry Ruda. The light source used to illuminate the devices was a tungsten-halogen lamp, powered by a radiometric power supply at 170 W. The schematic of the measurement setup is shown in Fig 3.5. The broadband light was spectrally filtered to a narrow band of ~ 1 nm resolution between 400 to 700 nm by a short-path optical monochromator and was focused onto the sample by an objective lens. The sample was mounted on the stage in the prober and the photocurrent was measured by a low noise current preamplifier and the data was read from a digital voltmeter.

Fig. 3.5 System setup for measurement of photocurrent spectral response of SiNW based p-i-n junctions array. Movable beam splitter was inserted into the optical path when illumination spot size was measured.

The power of the incident illumination was measured by replacing the sample with a calibrated optical power meter. To calculate the average intensity of the incident illumination, its spot size has to be known. This was measured by inserting a beam splitter into the optical path to partially direct the reflection from the sample into a CCD camera. The spot size of the beam was measured to be $520 \pm 20 \mu\text{m}$ at normal incident. The incident power on the active device area, which is the vertically projected area of the SiNWs, was then obtained by the product of the average incident intensity and active device area.

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For each wavelength of the incident illumination, the short circuit current of the p-i-n junction device was measured and the incident power on the active device area was calculated. Responsivity, which is defined as photocurrent per unit incident power, was then determined over the range of wavelengths measured.

Chapter 4 SiNW based Schottky barrier diode

This chapter presents Schottky barrier diodes fabricated on SiNWs. The design and fabrication of such devices using the top-down approach will be first described. The electrical characteristic of the SiNWs based Schottky barrier diodes which reveal high breakdown voltage is then demonstrated. Theoretical analysis of the high breakdown voltage attributed to the unique SiNW structure as compared to its bulk counterpart is also discussed.

4.1 Introduction

Schottky barrier diodes (SBDs) use the Schottky barrier formed between the metal and semiconductor to function as diodes. The advantages of SBDs compared to p-n junctions include their high switching speed and low forward voltage drop. SBDs have high switching speed because they are majority carrier semiconductor devices and do not suffer from reverse recovery which limits the device switching speed, as in the case of p-n junction diodes. Besides, SBDs generally have larger current density due to the smaller built-in potential. These have also resulted in a much smaller forward voltage drop compared to p-n junctions [41]. On the other hand, the disadvantages of SBDs include their larger reverse current and lower breakdown voltage [41].

SBDs can be fabricated by various techniques to deposit the metal on the semiconductor surface and form the Schottky barrier. These techniques include evaporation, sputtering and chemical vapor deposition. A typical SBD device

Chapter 4 SiNW based Schottky barrier diode

structure is shown in Fig. 4.1, which is commonly used as a microwave mixer diode [41]. This structure is simple to fabricate but suffers from low operating voltage as the sharp-edge of the electrode will increase the reverse current and reduce the breakdown voltage. To alleviate the electric field crowding effect near the electrode edges, various complex edge termination techniques, such as diffused guard ring, double-diffused guard ring, high-resistivity guard layer and metal-overlap laterally diffused structure, have been employed [41-43]. They have successfully reduced the electric field crowding at the edges and increased the breakdown voltage.

Fig. 4.1 A Typical Schottky barrier diode structure used as a microwave mixer diode [41].

In this work, we have shown that arising from the unique structure of SiNWs based SBDs that eliminates the metal edge effect seen in bulk devices; it is possible to achieve high breakdown voltages without resorting to the use of complicated edge termination techniques. In this study, SBDs are built on SiNWs with nickel silicide as the Schottky metal. Nickel was deposited on top of the SiNWs and reacted with them under high temperature to form nickel silicide. The Schottky barrier is hence formed along the longitudinal direction of the SiNWs and consequently the

Chapter 4 SiNW based Schottky barrier diode

Schottky metal contact has an area that is comparable or even larger than that of the semiconductor. Note that such a structure cannot be achieved in the case of bulk SBDs as the metal contact area is usually smaller than the semiconductor area. This structure eliminates the metal edges and hence the corresponding electric field crowding, leading to very high breakdown voltages that are closer to the ideal values than can be achieved using bulk devices.

4.2 Device fabrication

In this study, the SBDs were fabricated using the top-down approach based on optical lithography. Fig 4.2 summarizes the fabrication process of the SiNW based SBD. Essentially a SiNW was formed between two big silicon contact pads and the whole device was sitting on the top layer of a SOI substrate. Nickel was deposited onto the center part of the SiNW and reacted with it to form nickel silicide during high temperature annealing. Hence two Schottky barriers were formed in the longitudinal direction of the SiNW.

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(a) Starting SOI wafer

(b) Etch Si to define I-shape Si island with mask 1

(c) Oxidation to thin down Si wire to nano-scale

(d) Channel implant

(e) Gate metal deposition with mask 2

(f) Annealing to form NiSi

Fig. 4.2 Major fabrication steps of SiNW based SBD.

Chapter 4 SiNW based Schottky barrier diode

4.2.1 Starting Wafer

As discussed in section 3.1, SiNWs were fabricated on silicon-on-insulator (SOI) wafer. The top layer is <100> silicon that is about 2-3 μm thick with 1-20 $\Omega\text{-cm}$ resistivity, and the buried oxide layer is around 1 μm , which serves as isolation between the fabricated devices on top and the bulk Si substrate below (Fig 4.2a). Thermal oxidation was carried out at 1100 $^{\circ}\text{C}$ for 400 mins to thin the top silicon layer down to 1.4 μm . The SiO_2 formed was removed by dilute HF solution.

4.2.2 Si-fin pattern transfer

Optical lithography was then used to define I-shape silicon islands which consist of silicon fins with a line width of 1.6 μm connected to two silicon contact pads at both ends for electrical probing (Fig 4.2b). Around 1.12 μm thick silicon in the field region was etched by LAM Research 4420 plasma etcher.

4.2.3 Thermal oxidation

Two rounds of wet oxidation, with oxidation time of 340 mins and 85 mins, were subsequently performed to reduce the dimension of the Si fins to nano-scale (Fig 4.2c). The first round of oxidation was carried out at 1100 $^{\circ}\text{C}$ for 340 mins with 5 *SLM* flow rate of O_2 and 8 *SLM* of H_2 . The thermal oxide of 1.33 μm formed on the silicon fins was removed by isotropic wet etching in order to speed up the subsequent oxidation process. The second round of thermal oxidation was then carried out at 950 $^{\circ}\text{C}$ for 85 mins with the same flow rates of O_2 and H_2 to further oxidize the Si fins and reduce the dimension of SiNWs formed. The resulting

Chapter 4 SiNW based Schottky barrier diode

SiNWs fabricated have a triangular cross-section with a height of ~ 120 nm and base ~ 190 nm as confirmed by TEM cross-sectional image shown in Fig 4.3 [44].

Fig. 4.3 TEM cross-section picture of the SiNW fabricated. The cross-section is triangular shape with a height of ~ 120 nm and base ~ 190 nm.

4.2.4 Channel and contact implantation

After the second round of oxidation, about $0.19\ \mu\text{m}$ oxide was etched away before implantation. The SiNW channel was doped with $2 \times 10^{11}\text{cm}^{-2}$ phosphorus by implantation using a Varian EHP-220 ion implanter (Fig 4.2d) with an implantation energy of 80 KeV. An optical mask was then used to expose the contact pad regions. Following that about $0.33\ \mu\text{m}$ thick of thermal oxide on the pads was removed by isotropic etch. A thin oxide layer of 30 nm oxide was left on contact pad to serve as sacrificial oxide and prevent channeling during the subsequent implantation of the contact pads. The phosphorous implantation of the pads was executed with a dose of $5 \times 10^{15}\text{cm}^{-2}$ and energy of 150 keV to heavily

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dope them so as to form good ohmic contacts with metal.

4.2.5 Gate deposition and pattern transfer

A mask was next used to define the gate pattern for metal deposition (Fig 4.2e). A negative photo resist (PR) AR-U4040 was coated on the wafer and the PR in the gate area was removed after development. Isotropic wet etch was performed to completely etch away the oxide around the SiNWs. A 40 nm layer of nickel was then deposited by E-beam evaporation onto the center part of the SiNWs that is fully exposed (Fig 4.2e). The gate pattern was transferred to the metal layer using lift-off technique.

4.2.6 Electrode formation and annealing

A layer of negative PR was coated on the wafer and a mask was used to open contact pads to remove the oxide on top. The oxide on top of contact pads was etched by plasma and PR was stripped after etching. A 400nm layer of Ti was subsequently deposited and pattern on the contact pad to form electrode. After formation of Ti electrodes on the contact pads, the devices were annealed at 425 °C for 30 mins. Nickel reacted completely with the SiNWs underneath to form nickel silicide and SBDs were then formed between the nickel silicide and SiNWs along the longitudinal direction (Fig 4.2f). The SBDs formed can be probed between either one of the two Ti contact pads and the nickel silicide contact. The top view of the fabricated device is presented in Fig.4.4.

Fig. 4.4 SEM micrograph showing the top view of the fabricated device.

4.3 Electrical characteristics and discussions

As demonstrated in the fabrication process in section 4.2, there is a nickel silicide segment in the middle of the SiNW. Hence, Schottky barriers were formed on both side of this nickel silicide segment with the adjacent SiNW. The bandgap diagram of the SBD was shown in Fig 4.5. The device was probed between the nickel silicide segment and one end of the SiNW.

Fig. 4.5 Bandgap diagram of Schottky barrier diode formed between Nickel silicide and SiNW.

Chapter 4 SiNW based Schottky barrier diode

The I - V characteristic of a typical SBD with a nanowire length of 4 μm is shown in Fig 4.6. Strong current rectifying effect can be clearly observed. The I - V characteristic in the forward bias region can be modeled using Eq. 4.1. [41]:

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (4.1)$$

where I_s is the saturation current, k is the Boltzmann's constant, T is the temperature, q is the electronic charge and n is the ideality factor. By fitting the measurement data shown in Fig 4.6 to Eq. (4.1), the ideality factor n is derived to be 1.36 for our SiNW based SBDs.

The Schottky barrier height ϕ_b can be calculated using Eq. 4.2. [41]:

$$I_s = T^2 A A^{**} \exp\left(-\frac{q\phi_b}{kT}\right) \quad (4.2)$$

where A^{**} is the effective Richardson's constant ($110\text{A/K}^2 \text{ cm}^2$ for n-type Si) and A is the contact area which is assumed to be the cross-sectional area of the SiNW. Using the I_s derived from Eq. 4.1, the Schottky barrier height has been found to be 0.33 eV.

The work function of NiSi is 4.6 eV [45]. Hence the Schottky barrier height can be calculated theoretically from the following equation,

$$q\phi_b = q(\phi_M - \chi) = 4.6 - 4.05 = 0.55\text{eV} \quad (4.3)$$

where χ is the electron affinity of Silicon. The experimentally determined Schottky

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barrier height of 0.33 eV is lower than theoretically calculated value of 0.55 eV.

This may be due to the Femi level pinning in the silicon which is induced by surface state or image-force-induce lowering of Schottky barrier height [46].

Fig. 4.6 *I-V* characteristic of a SiNW SBD with a 4 μm length. Strong rectifying effect can be observed.

Fig. 4.7 Reverse-biased characteristic of SiNW SBD at different temperatures. The reverse current was clamped at 100 μA .

Fig. 4.7 shows the breakdown characteristics of the devices at 77 K and 300 K. The breakdown voltages (V_{br}) of the SBDs at room temperature have a nominal value of 32.0V, and range from 29.0 V to 33.5 V for our fabricated devices. From Fig 4.7, it is observed that V_{br} decreases with reducing temperature. A positive temperature coefficient suggests that impact ionization is responsible for the breakdown of the devices [41]. The V_{br} of SBDs due to avalanche breakdown depends strongly on the electric field distribution near the Schottky metal contact. Conventional bulk SBDs suffer from severe field crowding at metal edges and various edge termination structures have been proposed to alleviate the problem. However, such techniques generally complicate the device design and fabrication process substantially [41-43]. In contrast, the small dimension of the SiNWs

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coupled with the Schottky contact formed along the longitudinal direction of the SiNWs leads to the formation of an ideal Schottky structure that is expected to exhibit excellent electrical breakdown characteristics. As the Schottky metal contact area in our devices is comparable or even larger than the semiconductor area, there is no electric field crowding and hence very high breakdown voltage can be expected.

In assessing the V_{br} of the SBDs, it is important to know the doping concentration (N_D) in the SiNWs, which is the most important parameter that determines V_{br} . However, it remains a challenge to determine the exact N_D in the SiNWs after the oxidation process. It should be noted that todate there is no established technique to directly determine the doping concentration in SiNWs due to their small dimensions. Capacitance measurements are not helpful to determine the doping concentration since the capacitance of the SBDs is extremely small due to their small cross sectional area. Thus we have performed simulation to estimate the doping concentrations in our SiNWs.

In this study, the two dimensional semiconductor process simulator *Tsuprem* was used to simulate the fabrication process of SiNW. The simulator allows user to monitor cross-sectional structure of the wafer upon various fabrication process treatment. The specification of SOI wafer listed in section 4.2.1 was input in the simulator to define the starting wafer, as shown in Fig 4.8 (a). Photo resist was subsequently deposited onto the wafer and optical mask was used to define the Si-

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fin with width of 1.6 μm . Around 1.12 μm thick silicon in the field region was etched followed the experimental recipe specified in section 4.2.2 (Fig 4.8 (b)). Wet oxidation, with oxidation time of 340 mins was performed in the simulation to reduce the dimension of the Si-fins. The simulation follows the recipe in section 4.2.3 and the resulting structure is shown in Fig 4.8 (c). The thermal oxide of 1.33 μm formed on the Si-fin was then removed by isotropic wet etching (Fig 4.8 (d)). Following the recipe in section 4.2.3, the second round of thermal oxidation was carried out at 950 $^{\circ}\text{C}$ for 85 mins (Fig 4.8 (e)). About 0.19 μm oxide was then etched and the SiNW channel was implanted with $2 \times 10^{11} \text{cm}^{-2}$ phosphorus and 80 KeV energy.

(a)

(b)

(c)

(d)

(e)

Fig. 4.8 The simulated cross-sectional view of wafer after each process step. Scales are in μm .

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A cross-section that was nearly triangular, as shown in Fig. 4.8 (e), was obtained from our simulation, which is similar to that revealed by the TEM picture (see Fig. 4.3) and with comparable dimensions. Therefore, this affirms the validity of the simulation results. From the full simulation results, the doping concentration in the SiNW as well as the theoretical breakdown voltage (V_{br}) could be determined.

It is noted that dopant segregation, which is prominent in SiNW due to oxidation-enhanced diffusion of dopant during thermal oxidation [47], can affect its doping concentration. In this work, we have considered the effects of dopant segregation on the dopant concentration in the SiNWs and hence the breakdown voltage. N_D was found to be $\sim 1.3 \times 10^{16} \text{ cm}^{-3}$, and corresponding V_{br} was 46 V if phosphorus segregation is ignored. On the other hand, N_D was $\sim 3.3 \times 10^{16} \text{ cm}^{-3}$ and corresponding V_{br} was 25 V if phosphorus segregation was considered in the simulation. The increase in dopant concentration arises because phosphorus tends to segregate into SiNW from the surrounding oxide during the thermal oxidation process. The V_{br} of our SiNW SBDs of 32 V exceeds the theoretical ideal value of 25 V at $N_D = 3.3 \times 10^{16} \text{ cm}^{-3}$ when dopant segregation is considered. This may be because the simulation model overestimated the phosphorus dopant segregation into SiNW. The model simulates the dopant segregation during thermal oxidation based on calculation of the segregation flux and moving-boundary flux at Si-SiO₂ interface. Segregation flux is related to the concentration of the impurity within two materials and moving-boundary flux is due to the consumption of silicon containing impurities. Nevertheless, based on the process simulation without dopant segregation, we conclude that $N_D \geq 1.3 \times 10^{16} \text{ cm}^{-3}$, which means that the

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ideal theoretical $V_{br} \leq 46$ V. Therefore, our SBDs have demonstrated V_{br} of at least 70% of the theoretical value. On the other hand, as reported by M. P. Lepselter and S.M. Sze [48], bulk planer Schottky diode formed between silicide and silicon with no additional edge termination technique showed a breakdown voltage of only 5 V, compared to theoretical value of 36 V with a doping concentration around $2.2 \times 10^{16} \text{ cm}^{-3}$. This suggested that the bulk Schottky diode can only achieve a fraction of the theoretical breakdown voltage. Comparing with the 70% of theoretical breakdown achieved in this work, SiNW based SBD demonstrated great advantage in improving the breakdown voltage.

We have also considered the effect of uncertainty in the SiNW dimension on the dopant concentration and hence the theoretical breakdown voltage. This is important as the cross-sectional dimension of the SiNWs may not be uniform along its length. Our simulation results have shown that when dopant segregation is not considered, the doping concentration in the SiNW is mainly determined by the implantation process and has only weak dependence on its dimension. Thus, the breakdown voltage is also not very sensitive to the dimension of the SiNW. For example, we found that even with a very large variation in the SiNW dimension of 30% from its 120 nm deduced from the TEM picture, the peak dopant concentration changes only by 15%, which translates to a change in the theoretical breakdown voltage of 4 V, or about 8%. Hence, the uncertainty of the SiNW dimension does not critically affect the theoretical breakdown voltage deduced.

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As SiNWs have a large surface to volume ratio, it is expected that the SiNW-SiO₂ interface will exhibit a significant effect on its electric field distribution and hence breakdown voltage. As our process involved annealing at 425 °C in forming gas, it is expected that only positive fixed interface charge will exist at the interface [49]. *Medici* device simulation was carried out to simulate the effect of these positive charges. SiNW Schottky barrier diode devices with/without incorporation of positive fixed charge at the SiNW surface were simulated. The depletion region width at the metal-SiNW interface was extracted and compared. From our simulation, it is found that such positive charge will result in a smaller depletion region, leading to higher electric field and hence lower theoretical V_{br} compared to those without such positive charge. This implies that our SBDs are even closer to the ideal case in terms of breakdown and hence they are very suited for high voltage application. We ascribe the high V_{br} to the unique structure of the SiNW SBD which does not subject to field crowding, in contrast to bulk devices. In essence, the SiNW with a very small dimension completely reacted with nickel to form the Schottky metal. Since the Schottky metal area is comparable or larger than that of the SiNW, electric field crowding at the edges of the SiNW is totally eliminated. Therefore, the device will exhibit a large breakdown voltage that is closer to that of the ideal value for a given doping concentration.

To further understand and verify the origin of the high V_{br} observed, electric field distribution within the SiNW SBD has been modeled using *Medici* simulator by numerically solving Poisson's and continuity equations. For simplicity, a circular

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structure has been assumed for the Schottky metal and SiNW with a diameter of 120 nm, and with a SiNW length of 4 μm . For comparison, conventional bulk silicon SBD with the same length of 4 μm and an edged electrode was also modeled. The widths of the bulk silicon SBD and the edged top electrode have been assumed to be 2 μm and 400 nm respectively. Both devices have been assumed to have the same doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ (phosphorus doped) and are subjected to a same -8V reverse bias voltage. To get better accuracy of simulation, denser mesh grid size was used in the device areas where there were significant electric field variations. The mesh grid size for the bulk SBD near the metal contact edge is 10 nm, and the corresponding value used for the SiNW SBD is 2 nm.

Figs. 4.9 and 4.10 show the electric field distribution in the bulk SBD and SiNW SBD respectively. As can be seen, the electric field near the edge of the contact for the bulk SBD is greatly enhanced due to electric field crowding effect. The peak electric field is observed to be as high as $\sim 8.9 \times 10^5 \text{ V/cm}$ and has exceeded the silicon critical field, which will lead to breakdown of the device. In contrast, the electric field lines in the SiNW SBD are almost parallel to the nanowire and distribute more evenly as compared to the bulk device, with no field crowding effect observed. The peak electric field is only $\sim 1.5 \times 10^5 \text{ V/cm}$, which is about 80% lower compared to that in the bulk device. This suggests that SiNW based SBD device structure is effective in alleviating the electric field crowding effect and hence breakdown voltage of SiNW based SBD is much larger than that of bulk

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SBD. The simulation results are consistent with the experimental results demonstrated in the previous session, which revealed that high device breakdown voltage close to its theoretical maximum value can be achieved in SiNW based SBD devices, while bulk SBD with no edge termination techniques can only achieve a fraction of its theoretical maximum breakdown voltage.

As demonstrated from the electric field distribution simulation above, the main advantage of using SiNW for Schottky barrier diode is the unique device structure that can be achieved with SiNW. The small cross-sectional area of SiNW allows the metal gate to be deposited all round the SiNW. After thermal annealing at 425 °C for 30 min, the section of SiNW surrounded by the nickel gate completely reacted with the nickel to form nickel silicide, which in turn formed Schottky junctions with the other sections of the SiNWs. As a result, the Schottky barrier diode has a metal contact area that is larger than that of the SiNW. This structure avoids sharp metal corners and helps improve the breakdown voltage of the device. This is in contrast to the bulk Si Schottky barrier diode as shown in Fig 4.1, where the area of metal contact is small than that of the Si. Thus, sharp edges of metal contact exist where the electric field is enhanced, leading to early breakdown and hence lower breakdown voltage. Besides, it will induce greater leakage current in the device.

Fig. 4.9 Electric field distribution in conventional bulk SBD when subjected to a -8V reverse bias. The doping concentration is $1 \times 10^{16} \text{ cm}^{-3}$.

Fig. 4.10 Electric field distribution in SiNW SBD when subjected to a -8V reverse bias. The doping concentration is $1 \times 10^{16} \text{ cm}^{-3}$.

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It should be noted that the electrical behavior of nano-scale SBD formed on our 1-dimension SiNW in this work is different from that of a nano-contact formed on a 3-dimension bulk semiconductor. Nano-diode scaling and the formation of nano-contact on a 3D bulk semiconductor have been previously reported [50]. Such work studied the electrical characteristics of SBDs formed with very small Schottky metal (~ 10 nm) on bulk semiconductor. It was found from simulation that the nano-scaling of Schottky metal led to a considerably reduced Schottky barrier thickness, which in turn resulted in substantial tunneling current even when the semiconductor has a low doping concentration [46]. Besides, the dominant transport process is no longer by thermionic emission, as in the case of conventional SBD [50]. As a result, the I - V characteristic showed no rectifying effect and did not conform to that of a conventional SBD. Also, a much higher conductance than expected from down-scaling a conventional diode was observed from the I - V characteristic of such devices, which further indicated the existence of special transport behavior. In contrast to the nano-contact formed on a 3-dimension semiconductor, the semiconductor in our device is also scaled down to comparable dimension as the Schottky metal area. Our device simulation using *Medici* has shown that when both the Schottky metal and semiconductor are scaled down concurrently to nanometer range, the depletion width is not affected by the nano-scaling. As a result, our SiNW SBDs do not have appreciable tunneling current and they exhibit rectifying I - V characteristic that is expected of a SBD dominated by thermionic emission transport mechanism.

4.4 Conclusion

SiNW-nickel silicide SBD has been fabricated using the top-down approach along SiNWs of around 120 nm in cross-sectional dimension. Electrical measurement of the SiNW SBD reveals high breakdown voltage that is at least 70% of the theoretical ideal value. This result is remarkable given that no edge termination techniques have been used. The high breakdown voltage obtained is attributed to the unique structure of our SiNW SBDs that does not suffer from electric field crowding, in contrast to bulk devices. Essentially, the small cross-sectional dimension of the SiNWs and the formation of the Schottky contact along the longitudinal direction of the SiNWs have resulted in the Schottky metal area that is comparable or even larger than that of the SiNWs. Therefore, the structure is similar to that of an ideal SBD and hence accounts for the high breakdown voltage observed. In comparison, this structure is very different from those of conventional planar bulk SBDs where the metal contact area is always much smaller than that of the semiconductor in contact. As a result, such bulk devices suffer from field crowding effect at the Schottky metal edge and complicated termination techniques have to be applied to improve the breakdown voltage.

The electric field distribution in the SiNW SBDs has been simulated using TCAD *Medici* simulator and compared with that of a corresponding bulk Si SBD. It is found that under the same reverse bias voltage, the electric field distribution is more uniform within the SiNW SBD device and the peak electric field is much smaller compared to that in the conventional bulk SBD device. The simulation

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results have verified that the unique device structure of SiNW based SBD renders itself free from electric field crowding effect that is commonly encountered in bulk SBDs. Therefore such SiNWs based SBDs are potentially suited for high voltage applications at nanoscale.

Chapter 5 SiNW based single electron transistor

This chapter focuses on the fabrication and characterization of SiNW based single electron transistors (SETs) using deep-UV optical lithography. The principle of operation of SETs and a review of existing work on SETs are first presented. The design and fabrication of such devices based on SiNWs using the top-down approach will then be discussed in detail. Following that, the electrical characteristics of the SiNW based SETs revealing Coulomb blockade oscillation at room temperature is demonstrated. The effects of oxidation-induced tensile strain on the single-electron transport in the devices are also investigated. Besides, the mechanism responsible for single-electron transport and the effects of SiNW length on the characteristics of the SETs are discussed.

5.1 Introduction and background

As the size of modern transistors continues to reduce, the quantum mechanical property of electrons plays an increasingly important role in determining how devices are designed, fabricated and operated. The wavelike nature of electrons influences the way in which they travel through the channel in a device, when the channel length is comparable to the wavelength of electrons (several nm). The atomic disorder introduced during the fabrication process for devices at the nanometer scale will also greatly affect the transport of electrons. SETs belong to single-electron devices, a class of devices that are built based on the quantum

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mechanical property of electrons, where it is possible for them to tunnel through insulating barriers even though their energy is too low to overcome the potential barrier [41, 51-53]. Such a transport behavior in single-electron devices provides functions and transfer characteristics that conventional electronic devices do not exhibit.

5.1.1 Operating principle

The simplest single-electron device is a single-electron box, which consists of a small conducting island connected to a capacitor and a tunneling junction in series (Fig 5.1 (b)) [52]. To understand the operation of single-electron box, we can compare Fig. 5.1 (b) with a similar system shown in Fig. 5.1 (a) that has the tunnel junction replaced by a resistor. For the system in Fig. 5.1 (a) where the capacitor is charged through the resistor, the charge on the capacitor is proportional to the voltage applied. However, for the charging of the capacitor through the tunnel junction as shown in Fig. 5.1 (b), it becomes staircase-like when the island is sufficiently small, as shown in Fig. 5.1 (c) [52]. This is because the charging energy E_c , which is the energy required to add one electron to the island becomes very large when the island size is very small. As a result, an additional electron is prohibited from entering the island through the tunnel capacitor unless the potential of the island is lowered by an external bias or substantial energy is provided to the electron. This phenomenon is known as the Coulomb blockade effect [54]. With increasing applied voltage it is possible to add on electrons in increment of one

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whenever the voltage is sufficient to overcome the charging energy of the island to introduce an additional electron.

Fig. 5.1 (a) When a capacitor is charged through a resistor, the charge on the capacitor is proportional to the applied voltage (b) When a tunnel junction replaces the resistor, a conducting island is formed between the junction and the capacitor plate. In this case, the average charge on the island increases in steps as the voltage is increased. (c) The steps are sharper for more resistive barriers and at lower temperatures. [52]

There are two criteria that must be fulfilled for the Coulomb blockade effect, or single-electron transport effect to be observed [54]. Firstly, the tunnel capacitor must have a resistance sufficiently larger than the quantum resistance given by

$$R_q = \frac{h}{e^2} \quad (5.1)$$

where h is the Planck's constant and e the electronic charge. This is limited by the uncertainty principle that dictates that electrons have to be treated as particles being clearly on either side of the junction [41]. The second criterion is that the

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energy of the electrons due to thermal fluctuation, which is given by kT , must be much smaller than the charging energy E_c . This energy is calculated as $e^2/2C$, where C is the total capacitance of the gate capacitor and the tunnel junction. A smaller island has a smaller total capacitance and hence a higher E_c . As the temperature increases or the resistance of the tunnel capacitor decreases, then either one of the two criteria will not be obeyed and consequently the steps seen in Fig 5.1 (c) become rounded and eventually reduced to a straight line, similar to that of charging a capacitor through a resistor.

The above described the Coulomb blockade effect in a two-terminal device single-electron box. In the case of a single electron transistor which is a three terminal device, it can be viewed as an single-electron box with two separate tunneling junctions for the entrance and exit of single electrons, as shown in Fig 5.2 [52]. Assuming that the gate is grounded, for an electron to tunnel through the barrier and enter the island, its energy must be equal to $e^2/2C$ due to Coulomb blockade effect. If the bias voltage between the source and drain is greater than e/C , then electrons have sufficient energy to overcome the Coulomb blockade and tunnel through the junction, and hence pass through the island. If the bias voltage between the source and drain is kept below e/C , we can apply a gate voltage to modulate the potential of the island. When a gate voltage is gradually applied, the island potential will increase and likewise the energy of the initial state of the system with no electrons on the island. Simultaneously, the energy of the state with one excess electron on the island gradually decreases [52]. When the energies of the two states

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are equal, they both qualify as the lowest energy state of the system and consequently the island can hold zero or one electron. Therefore an electron is now able to tunnel onto and out of the island readily.

The above process of inducing tunneling of electrons between source and drain through the island can be further illustrated quantitatively. Suppose a voltage V_g is applied on the gate such that the total number of electrons on the island, N , is balanced with those on the gate, that is, $V_g C_g = Ne$. Since the number of electrons N is stable and due to Coulomb blockade effect, no current can flow through the island when a small source-drain bias is applied. However, when V_g is changed such that $V_g C_g = (N+0.5)e$, the energies of the two states of the system, one with N electrons and the other with $N+1$ electrons become equal. In the case, when a small voltage is applied between the source and drain, an electron can tunnel onto the island and increase the number of electrons on the island to $N+1$. Subsequently, an electron can tunnel out of the island and reduce the number of electrons on the island back to N . In this way a current can flow between the source and drain due to single electron tunneling and the Coulomb blockade is lifted. As a result, the source-drain current exhibit conductance peaks with respect to the gate voltage whenever $V_g C_g = (N+0.5)e$, as illustrated in Fig 5.3. That is, conduction occurs whenever the voltage on the gate corresponds to half-integer multiple of e on the island and is suppressed for integer multiple of e [52].

Fig. 5.2 SET structure consists of a small island attached to two tunneling junctions. A gate electrode is used to control tunneling between the source and drain electrodes [52].

Fig. 5.3 Drain current versus gate voltage at small source-drain bias voltage. The drain current is a periodical function of the gate voltage [55].

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5.1.2 Literature review of single electron transistors

The physics, existing work and potential applications of single electron transistors have been extensively reviewed [52-54]. Here we briefly summarize the previous work which demonstrates the single electron transistor.

The first experimental SET was demonstrated by Theodore Fulton and Gerald Dolan [56] at Bell Labs in 1987. All the electrodes were made out of aluminum in this device. On top of an insulating substrate, a long center metal electrode connected to several metal leads by tunnel junctions was fabricated, as shown in Fig. 5.4. The gate electrode made of Au-Cr was placed on the back of the substrate. The Al-Al junctions were formed through a multiple angle deposition-oxidation-deposition cycle. The predicted oscillation was observed through the I - V characteristic of the device at around 1 K.

Fig. 5.4 SEM micro image of the sample fabricated. Junctions labeled a, b, c were formed where the vertical electrodes overlap and contact the longer horizontal central electrode [56].

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Semiconductors based SETs that comprised two layers of GaAs and AlGaAs, as shown in Fig 5.5 [57], has been reported. A two-dimensional electron gas was formed at the interface between the two layers of semiconductors. It was confined in the direction perpendicular to the AlGa and AlGaAs interface and its density could be controlled by the gate voltage V_g applied to the conducting substrate. Electrodes were also deposited on the top surface to control the 2-dimension electron gas. When an electric field was applied on the electrode, the electron gas just beneath it was depleted and hence defined the pattern of the channel. Two constrictions in the electrode gap were formed in order to induce saddle-shaped potential barriers in the channel, which functioned as tunneling junctions in the fabricated SET.

Fig. 5.5 Schematic drawing of the device and SEM micro image of the fabricated sample. The patterned electrode on top define a narrow channel with two potential barriers [57].

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These early work on SET reported were measured at temperatures less than 1 K [56, 57]. This is because the island size formed was not small enough and hence the corresponding charging energy E_c was not sufficiently large for them to operate at room temperature, recalling that for Coulomb blockade effect to be seen, $E_c \gg kT$. To enable practical SETs operating at room temperature, they need to have large E_c , which in turn will require much reduced island sizes down to the nanometer range [53]. Various fabrication methods and materials have been explored to fabricate such islands and junctions, such as cadmium selenide nanocrystal binding to pre-patterned Au electrodes [58], evaporation on a Si_3N_4 membrane with a nanometer scale orifice [59], Ti metal deposition on pre-patterned silicon substrates [60]. Till now room temperature operations of SETs with high E_c have been successfully demonstrated by several groups [61-64].

Fig. 5.6 Schematic of starting device structure to fabricate SET. Silicon fin was defined by E-beam lithography and SiNW was subsequently formed by thermal oxidation [55].

SiNW based SETs fabricated using the top-down approach with the SiNW serving as both the SET channel and tunneling barrier have been demonstrated [55, 64, 65]. Such SiNW based SETs are technologically very important as the fabrication

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process involved is CMOS compatible. Thus they offer the possibility of integrating SETs with conventional silicon devices to substantially enhance the practicality and functionality of SETs. The starting structure used for the fabrication of SiNW based SET was a narrow and thin silicon fin defined by E-beam lithography and connected to two silicon pads, as shown in Fig 5.6 [55]. The entire structure was fabricated on SOI wafer. The fin was then oxidized in dry oxidation ambient to reduce its dimension. It has been proposed that the origin of the tunneling barrier is the bandgap modulation of Si due to quantum confinement and strain developed in SiNW due to thermal oxidation [54]. As shown in Fig. 5.7 [55], quantum size effect of SiNW with diameter less than 10nm leads to an increase in the bandgap of SiNW. Also, the oxidation-induced strain reduces the bandgap in the middle of SiNW. This lowering of the bandgap results in the formation of tunneling barriers in the fabricated SiNW. Oscillation of the drain current versus gate voltage has been observed up to room temperature from these SiNW based SETs [55]. Several applications have also been developed, such as implementation of Exclusive-OR gate using multi-gate SET, multi-value logic operation by combining with MOSFET, and single electron-CCD device [55].

In the previous work on SiNW based SETs reported by other research groups, E-beam lithography was used to achieve SiNWs with dimension less than 10 nm needed for room temperature operation [61, 63, 66, 67]. The E-beam lithography technique, however, is costly and has low throughput, and hence not suitable for mass fabrication of SET devices. In our work we have used the optical lithography

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approach to fabricate SiNW based SETs. It is attractive compared to E-beam lithography because it is compatible with CMOS technology and can be used for large-scale fabrication and integration. Besides, it offers the possibility of integrating silicon single-electron electronic devices with conventional silicon devices to realize a new generation of silicon devices and circuits for a wide range of applications.

Fig. 5.7 Schematic of the SiNW and corresponding energy bandgap along SiNW demonstrating the proposed model of tunneling barrier formation [55].

5.2 Device fabrication

In this work, SiNW based SETs were fabricated based on the top-down approach using conventional deep-UV optical lithography followed by thermal oxidation.

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The SET device structure is based on an N-type gate-all-around SiNW MOSFET with ~3 nm to 4 nm channel width. Similar silicon SETs have been previously fabricated using the optical lithography technique [68]. However, single-electron transport was only observed at very low temperature of ~10 K attributed to the relatively larger cross section of the SiNW of around 45 nm × 30 nm [68]. For our devices based on SiNWs with much smaller cross sectional dimension, pronounced Coulomb blockade oscillation can be observed in the current-voltage (I - V) characteristics even at room temperature [69, 70] .

5.2.1 Starting wafer

The devices were fabricated using 8 inch silicon-on-insulator (SOI) wafers with (100) orientation. The starting SOI wafers have a p-type (boron doped) top silicon layer and a thickness of 200 nm and doping of 10^{15} cm^{-3} . The buried oxide has a thickness of 150 nm. The schematic of the starting wafer is shown in Fig 5.8.

Fig. 5.8 Schematic of starting p-type SOI wafer.

5.2.2 Si-fin pattern transfer

Alternating phase shift mask lithography was used to define Si-fins connected to two big silicon pads on the wafer [69-71]. The masks used and schematic of the

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patterned Si-fins are shown in Fig 5.9. The deep ultraviolet light source used for the patterning was from a krypton fluoride excimer laser (KrF laser) with a wavelength of 248 nm. The width of the patterned resist that defined the Si-fins was around 120nm, whereas their lengths varied from 200 nm to 500 nm and were along the $\langle 110 \rangle$ direction. To reduce the width of the Si-fins that will be formed, the patterned photoresist was trimmed by oxygen plasma and the pattern was then transferred to the top silicon layer by silicon etching using a reactive ions etching process, which consisted of a gaseous mixture of C_4F_8 and SF_6 . Si-fins with widths of 40 nm and 43 nm were obtained after etching of the silicon top layer down to the buried oxide layer, as shown in Fig. 5.10.

Fig. 5.9 Mask used to pattern silicon fin (solid line).

Fig. 5.10 Schematic of the patterned structure by optical lithography. The structure is not drawn to scale.

5.2.3 SiNW formation by thermal oxidation

The patterned Si-fins were oxidized in dry oxygen ambient at 875 °C for 4 hours, resulting in the formation of SiNWs. The wires were subsequently released from oxide by dilute HF solution wash. The schematic of the SiNW formed is shown in Fig 5.11 and the SEM image of a tilted device with a SiNW length of 200 nm is shown in Fig. 5.12 [71]. An encapsulating oxide of 4 nm was subsequently thermally grown around the SiNW to function as the gate dielectric. The final SiNWs have diameters of ~3 nm and ~4 nm, corresponding to starting Si-fins with critical dimensions of 40 nm and 43 nm respectively. TEM cross section image of SiNW taken after completing all process steps will be presented later in section 5.2.6, Fig 5.19.

Fig. 5.11 Schematic of the SiNW formed between two silicon pads after thermal oxidation at 875 °C for 4 hours.

Fig. 5.12 SEM image of tilted SiNW with 200 nm length after release from thermal oxide using dilute HF.

5.2.4 Gate deposition and patterning

A layer of 130 nm amorphous silicon (α -Si) was further deposited around the SiNW as the gate electrode using low-pressure physical vapor deposition technique (LPCVD) [69-71]. The gate electrode was patterned and etched after the α -Si deposition. The mask used for gate patterning is highlighted in dashline in Fig. 5.13. The gate length was defined to be longer than the SiNW length so that

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margins were provided should misalignment occur during the gate patterning. Besides, this design served to protect the SiNW from being broken during the gate etching process. The schematic of the device after gate formation is shown in Fig 5.14. The SEM image of device after α -Si gate deposition and patterning is shown in Fig 5.15.

Fig. 5.13 Mask used to pattern gate (dash line).

Fig. 5.14 Schematic of the structure after gate pattern transfer. The structure is not drawn to scale.

Fig. 5.15 SEM image of the fabricated device after 4 nm thermal oxide grown, 130 nm α -Si deposition and gate patterning. The length of the SiNW between the silicon pads is 200 nm.

5.2.5 Metal contact formation

After gate formation, the process was followed by source/drain implantation to obtain good ohmic contacts between the Si pads and the metal electrode. The source/drain and α -Si gate were implanted using arsenide with a dose of $4 \times 10^{15} \text{ cm}^{-2}$ and energy of 30 keV. A long activation annealing at 950 °C for 15 mins was carried out to promote dopant diffusion throughout the gate and source/drain regions.

Fig. 5.16 Mask used to form contact hole (Solid line).

Fig. 5.17 Schematic of the cross-sectional view of the device structure after metal contact formation. The structure is not drawn to scale.

A layer of 400 nm thick undoped silicate glass (USG) was then deposited onto the wafer to passivate the entire device. Square contact holes were defined on the USG above the silicon contact pads for metallization, as shown in Fig 5.16. The USG was subsequently etched down to the silicon contact pads before metallization. After that 25 nm tantalum nitride (TaN) followed by 750 nm aluminum silicon copper compound were deposited by physical vapor deposition (PVD) to form the metal contacts to the silicon pads. The purpose of the TaN deposition was to

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prevent the diffusion of Cu that is known to diffuse fast in silicon [41]. The metal layers were then patterned into larger contact pads for electrical probing purpose. Fig. 5.17 shows a cross-sectional view of the device structure after metallization. A top view SEM image of the entire device after completing all the fabrication steps is presented in Fig 5.18.

Fig. 5.18 SEM image of the entire device after standard metal contact formation. The SiNW between the source/drain pads with 400 nm length was encapsulated by 4 nm thermal oxide and 130 nm thick LPCVD α -Si gate. The entire device was passivated with USG before metallization.

5.2.6 TEM image of SiNW cross section

Fig. 5.19 TEM cross-sectional images of SiNWs with 4 nm and 3 nm diameter. The difference in the dimensions is attributed to the different starting dimensions of the Si-fins. The inner and outer circles indicate the contours of the SiNWs and the encapsulating thermal gate oxide respectively.

The final dimensions of the SiNWs fabricated were determined by TEM cross section imaging in high-resolution phase contrast mode. As shown in Fig. 5.19, the SiNWs have diameters of ~3 nm and ~4 nm, corresponding to starting Si-fins with

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critical dimensions of 40 nm and 43 nm respectively [69-71]. The inner dotted lines in Fig. 5.19 identify the SiNW regions which exhibit crystalline structure and have roughly circular cross-section. The regions between the inner and outer dotted lines outline the amorphous thermally-grown silicon oxide which has a thickness of 4 nm. The regions outside the outer dotted lines are the poly-silicon gate which was converted from α -Si after activation annealing at 950 °C for 15 mins. It is also noted that the deposited α -Si covered the entire SiNWs across their circumstances uniformly without leaving any gap in all directions.

5.3 Room temperature single-electron transport

The fabricated SiNW based SET devices were characterized at room temperature (300 K). The drain current versus gate voltage ($I_d - V_g$) characteristic of a typical device with a SiNW length of 400 nm and diameter of 4 nm is shown in Fig. 5.20. The most important property of the SET is that the threshold voltage, as well as the source-drain current in its vicinity, is a periodic function of the gate voltage [53]. Hence $I_d - V_g$ of a SET shows a periodical characteristic which is distinctively different from MOS transistors. A small drain-source voltage of 1 mV was applied to ensure that electrons do not have sufficient energy to overcome the Coulomb blockade effect. Clear oscillation peaks are observed from the $I_d - V_g$ characteristic, which indicates that the device is operating in the Coulomb blockade regime [72]. Besides the small drain voltage applied, another condition needed to observe Coulomb blockade and single-electron transport at room temperature is that the charging energy $E_c = e^2/2C$ of the device must be much higher than the thermal

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energy kT . Therefore we deduced that the total capacitance of our device is very small, which is attributed to the extremely small dimensions of our SiNWs that is only a few nanometers in diameter.

Fig. 5.20 Room temperature I_d - V_g characteristic of the fabricated SET device. Clear oscillation peaks can be observed. $V_d=1\text{mV}$.

The devices were also characterized at low temperatures (77 K and 150 K) and the results, including the room temperature characteristics, are shown in Fig. 5.21. Clear Coulomb oscillations are observed across all temperatures, and an obvious increase in the peak-to-valley ratio is noted with decreasing temperature. The result further confirms single-electron transport in the devices as increasing temperature will lead to a higher thermal energy kT and hence an attenuation of single-electron transport. More electrons will possess enough energy to tunnel through the junctions and result in a weaker Coulomb blockade effect [10].

Fig. 5. 21 I_d - V_g of the fabricated SET devices at various temperatures. Clear Coulomb blockade oscillation could be observed and an increase in the peak-to-valley ratio with decreasing temperature is noted. $V_d=1\text{mV}$.

The origin of the observed Coulomb blockade effect in such devices have been proposed to be attributed to an increase in the energy bandgap of the SiNW due to the quantum size effect, and a concurrent decrease in its energy bandgap near the center arising from the high stress developed due to thermal oxidation [68]. As a result, two tunneling barriers are formed along the SiNW sandwiching a Si island [54] (see Fig. 5.7). The bandgap of our SiNW of 4 nm diameter is estimated to be about 1.3 eV [21], whereas bulk silicon has a bandgap of 1.12 eV at room temperature. In terms of bandgap reduction due to strain induced by oxidation, it has been predicted that the bandgap of SiNW in the $\langle 110 \rangle$ direction can decrease by as much as 100 mV for a 1% strain [73]. The stress is expected to peak at the center of the SiNW and will be lower at both ends because of the shear stress

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caused by the oxidation of the silicon pad layers at the Si/buried oxide interface [55, 65]. Therefore, the reduction in the bandgap is expected to be the highest at the center of the SiNW, which hence accounts for the formation of a potential well and two adjacent tunneling junctions [55, 65]. This gives rise to the structure as illustrated in Fig. 5.2 that is needed to give rise to SET operation.

Repeated measurements showed highly reproducible periodicity in the I_d-V_g characteristic, with a period of around 0.7 V at all temperatures, as shown in Fig. 5.21. It is possible to calculate the equivalent gate capacitance as follows [48]:

$$C_g = \frac{e}{\Delta V_g} \quad (5.2)$$

where e is the elementary charge and ΔV_g is the period in the I_d-V_g characteristic. Using Eq. (5.2), the gate capacitance is calculated to be around 0.23 aF for this device. We attribute the small capacitance to the extreme small dimension of the SiNW fabricated. To estimate the effective size of the quantum dot formed in the middle of the SiNW, a cylindrical capacitor model is assumed for our gate-all-around SET device. The structure consists of two co-axial cylinders, which correspond to the SiNW in the center with 4 nm diameter and the surrounding thermal oxide with 4 nm thickness, as shown in Fig. 5.19. The capacitance per unit length of the cylindrical capacitor is given by [74] ,

$$C_g = \frac{2\pi\epsilon_0\epsilon_r L}{\ln\left[\frac{b}{a}\right]} \quad (5.3)$$

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where ϵ_r is the relative permittivity of thermal oxide, ϵ_0 is the permittivity of free space, L is the length of the cylinder and C_g is the gate capacitance. a and b are the diameters of the inner and outer cylinders respectively, which correspond to 4 nm and 12 nm for this device. Using the C_g calculated from Eq. 5.2, L is derived to be around 1.4 nm. This reflects the effective size of the quantum dot formed in the middle of the SiNW. The small effective size deduced is considered reasonable as it has been demonstrated theoretically that the size of the semiconductor island sandwiched between tunneling junctions has to be in the order of 1 nm for Coulomb blockade oscillation to be observed at room temperature [53].

Another signature of single-electron transistor is that drain current is suppressed at low source-drain voltage due to Coulomb blockade. The I_d - V_d characteristic of the fabricated SET device measured at different gate voltages is shown in Fig 5.22. As a result of Coulomb blockade, it is observed that the I_d - V_d characteristic at $V_g = 1.0$ V is suppressed at low drain voltage (0 to 0.2 V) and the magnitude of the current is lower than that at $V_g = 0.7$ V (note that $V_g = 1.0$ V corresponds to the valley of the I_d - V_g characteristic shown in Fig 5.21). This confinement further verified the single-electron transport behavior of the device. However, the current suppression is not so strong and does not lead to near zero current as in an ideal SET [41]. This is attributed to the limited height of the quantum tunneling barriers, which is formed in the SiNW from the combination of stress induced bandgap reduction and bandgap increase due to quantum confinement as explained in section this section

earlier. In an ideal SET device, the tunneling barriers are very high to result in much stronger confinement effect.

Fig. 5.22 I_d - V_d characteristic of the fabricated SET device at different gate voltages.

It is noted that current at low drain voltage for $V_g = 1.0$ V is suppressed due to Coulomb blockade.

5.4 Effect of tensile strain on single-electron transport

As discussed in section 5.3, the mechanism of formation of a quantum dot sandwiched by two tunneling barriers in SiNW based SETs has been proposed to be due to a combination of expansion of bandgap due to the quantum confinement, and shrinkage of bandgap due to the oxide-induced strain [55, 68, 75]. Hence the SET structure is formed in a self-aligned manner. On the other hand, some researchers have proposed that SiNW channel width fluctuation may result in strong local quantum confinement and thus formation of large tunneling barriers [59]. In this

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way quantum dots are formed along the SiNW, which are responsible for the single-electron transport [64]. To better understand and ascertain the origin of single electron transport in the SiNW based SETs, it is important to study the effects of the strain induced in the SiNWs on the characteristics of the SETs. This will help to identify the origin of the tunneling barriers formed in such devices.

Oxidation-induced strain on SiNWs formed by optical lithography and subsequent thermal oxidation has been previously investigated using micro-Raman spectroscopy adapted for nanoscale measurements [76]. The Raman scattering result was translated to absolute value of strain using phonon deformation potentials. The measurement results confirmed significant tensile strain induced in gate-all-around SiNW due to the thermal oxidation process. The strain was also found to be non-uniform along its length, being strongest near the centre of the SiNW and weakest near both ends of the wires [76].

It was also shown that the maximum oxidation-induced strain at the centre part of SiNW is related to its dimensions [76, 77]. Fig 5.23 illustrates the trend of the maximum strain as a function of its length and designed width (i.e. Si-fin width defined by lithography before thermal oxidation) deduced by micro-Raman measurements. The actual SiNW diameter after thermal oxidation is in the order of 100 nm. It was found that the maximum strain increases with increasing wire length and designed width. The above results suggest that it is possible to modulate the oxidation-induced strain in the SiNW by changing its length. Therefore we can

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study the effects of different oxidation-induced strain within SiNW on the SET characteristics by defining SiNWs with different lengths. Such a study will help shed light on the origin of tunneling barriers formation within the SiNWs.

Fig. 5.23 Strain dependence on SiNW length and on the designed width of the silicon fins (lithography) [76]. It is observed that strain increases with the SiNW length. The actual diameter of SiNW is in the order of 100 nm.

We have fabricated SiNW based SETs with different SiNW length from 200 nm to 500 nm. Fig 5.24 shows the $I_d - V_g$ characteristics of the devices characterized at room temperature. The diameters of the SiNWs are 3 nm as confirmed by TEM cross-section image (See Fig. 5.19). The voltage applied on the drain terminal is fixed at 1 mV and the source terminal is grounded. For the device with 500 nm length, clear Coulomb blockade oscillation is observed at room temperature. By comparing the devices with different SiNW lengths but the same diameters, it is interesting to note that Coulomb blockade oscillations are dependent on the length

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of the SiNWs. The amplitudes of the oscillations are reduced with decreasing length from 500 nm to 250 nm. When the length is further reduced to 200 nm, no oscillation is seen and the I_d - V_g curve reverts to that of a typical MOSFET.

Fig. 5.24 I_d - V_g characteristics of the fabricated devices with different SiNW lengths measured at room temperature. V_D is fixed at 1 mV. The SiNWs have the same diameter of 3 nm. Coulomb blockade oscillation is more pronounced for longer SiNWs, which are subjected to larger tensile strain.

Based on the results shown in Fig. 5.23, our devices with shorter wire length such as 200 nm will experience less oxidation-induced strain and hence the bandgaps nearer the center part of the SiNW do not lower as much as those devices with longer wire length, such as 500 nm [76, 77]. As a result, the tunneling barrier formed due to the reduction in bandgap at the center of the SiNW is effectively lowered and more electrons with room temperature thermal energy may be able to cross over the barrier. Consequently the devices increasingly operate in a normal MOSFET mode rather than SET mode. This accounts for the smearing out of the

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oscillations seen for devices with decreasing SiNW length. Therefore, it can be concluded that lower tensile strain tends to deteriorate Coulomb blockade oscillation in SiNW based SET devices. Also, the results shown are consistent with the model [54] which proposes that oxidation-induced strain together with the quantum confinement effect in SiNWs account for the operation of SET, as explained in section 5.3. In putting forth our argument, we have referenced the results shown in Fig. 5.23 [72]. It should be noted that the initial silicon fins shown in Fig 5.23 are in the range of about 1 μm , and the actual SiNWs formed after thermal oxidation are much smaller, in the order of 100 nm [76]. Despite that the dimension is still much larger than our SiNWs, we believe that the trend in the change of strain with respect to their length should be the same, given their similar geometry and the same material and fabrication process involved, i.e., optical lithography defined Si-fins followed by thermal oxidation. We have also attempted to use micro-Raman to measure the strain in our SiNWs, however, the signal was too weak that no conclusions could be drawn. This is not unexpected as it is very difficult to use micro-Raman to characterize SiNWs with diameter of just several nanometers, and it shall remain a great challenge to the scientific community for some time to come.

Though it is found that devices with longer SiNWs exhibit more prominent Coulomb blockade oscillation, however, it is also seen from Fig. 5.24 that such devices have lower drain current as compared to those with shorter SiNWs. This is because the longer SiNWs will give rise to larger resistances and inevitably lower

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the drain current. This is another aspect of the SiNW based SETs which should be taken into consideration in their design.

Despite the above analysis, it may still be argued that the tunneling barriers in the SiNW based SET devices are formed due to non-uniformity in the dimension of the SiNW along its length, instead of oxidation induced strain [64]. For our fabricated SiNWs at dimensions of 3 to 5 nm, it is very difficult to see the non-uniformity along their lengths. SEM resolution is not good enough to capture such dimensions and using TEM to study the non-uniformity along the length is also very challenging at this dimension. Nevertheless, we think non-uniformity is not likely to be the origin of the tunneling barriers formed in our SiNWs for the following reasons. Firstly, due to self-limiting oxidation at such small dimension, any non-uniformity in the initial Si-fin critical dimension will result in a much smaller difference in the final dimension of the SiNWs formed and hence mitigate any non-uniformity that may result along the SiNWs. Secondly, non-uniformity in the dimension along the SiNWs, though may be accentuated for longer SiNWs, should occur in all the SiNWs. Therefore if this is the origin of the tunneling barriers leading to the formation of single electron transistor, the Coulomb blockade oscillation should be seen for all the devices under room temperature. However, this is not the case for our fabricated devices where we found an obvious trend of weaker oscillation with decreasing SiNW length, and almost no oscillation was seen for the shorter wires. Therefore, it can be concluded that the origin of the formation of tunneling barriers in our SET devices is due to the oxidation-induced strain.

Low temperature measurements at 77 K using cryogenic prober were also carried out for shorter SiNW devices with lengths of 200 nm and 250 nm that operate as MOSFET under room temperature. The voltage applied on the drain terminal was fixed at 1 mV and source terminal was grounded. As can be observed in Fig 5.25, Coulomb blockade oscillations start to emerge at 77 K for these devices which did not reveal any oscillation peaks under room temperature, as shown in Fig 5.24. This is attributed to a decrease in the thermal energy of the electrons relative to the barrier height as a result of the low temperature. Hence there is stronger quantum confinement and Coulomb blockade effect emerges leading to the devices operating in the SET mode.

Fig. 5.25 I_d - V_g of the fabricated devices with short lengths measured at room temperature and 77 K. Coulomb blockade oscillations emerge at 77K for short SiNW devices, which operate in MOSFET mode under room temperature. V_d is fixed at 1 mV.

5.5 Conclusion

In conclusion, gate-all-around SiNW based SETs operating at room temperature are demonstrated using the top-down approach. The SiNWs in such SET devices have a diameter of around 3 to 4 nm, which was achieved using only optical lithography with KrF laser and thermal oxidation. We have observed prominent Coulomb blockade oscillation with a periodicity of 0.7 V at room temperature and the single-electron transport in the devices has been further confirmed by low temperature electrical characteristics measured at 77 K and 150 K.

SiNW based SETs with different nanowire lengths ranging from 200 nm to 500 nm were also fabricated and characterized. Coulomb blockade oscillations were found to be dependent on the length of the SiNWs, being more prominent for longer SiNWs than shorter ones. For the shortest device of 200 nm, no oscillation was observed and the $I_d - V_g$ characteristic reverted to that of a typical MOSFET. The results are interpreted in terms of the effect of SiNW length on the oxidation induced tensile strain, and consequently the tunneling barrier height developed in the nanowires. The results are consistent with a model [54] proposed to explain the origin of tunneling barrier formation in SiNW based SETs, which attributes it to a combination of quantum confinement effect and strain induced barrier lowering in extremely small nanowires. Our results also indicate that the length of SiNW is a crucial parameter in the design of such SiNW based SET devices.

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Our process used to fabricate SETs is fully compatible with conventional silicon CMOS technology and bypasses the costly and inefficient electron beam lithography technique that was commonly used in the previous work reported by other groups to achieve room temperature operation of SET. Using our fabrication approach, it is possible to integrate silicon SET devices with CMOS devices on a single silicon platform. Such integration can offer new functionalities beyond traditional CMOS logic circuits, and have enormous potential for practical use in information processing applications.

Chapter 6 SiNW based p-i-n junctions array

This chapter focuses on the fabrication and characterization of SiNWs based p-i-n junctions array. A literature review of the existing work on junctions formed by SiNWs is first presented. The design and fabrication of p-i-n junctions array using SiNWs fabricated based on the top-down approach are then described in detail. Following that, the electrical characteristics of the p-i-n junctions array are investigated and analyzed. The photocurrent spectral response of the devices is also studied as a function of wavelength from 400 to 700 nm. We have observed photocurrent peaks in the spectra, which implies enhanced optical absorption at some specific wavelengths. The results are analyzed and successfully modeled on the basis of diffraction effect arising from the array of SiNWs.

6.1 Introduction and motivation

As the Si technology node shrinks further into the nanoscale, there is a strong interest to integrate nanoscale photonics devices into Si electronics. Such a system has the potential to detect, process and transmit optical signal at nanoscale and hence can give rise to many new potential applications. For example, SiNW based nanophotonics devices, including SiNW junctions, can serve as excellent candidates for ultra-high spatial resolution photodetectors as well as high sensitivity spectroscopic sensing [78].

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Individually doped SiNW in a crossed configuration forming abrupt p-n junctions was among the first NW junction devices demonstrated [30]. The transport characteristic revealed clear rectifying effect similar to that of planar p-n junctions. Crossed Si-CdS NW avalanche photodiodes fabricated using the bottom-up approach were also reported [38]. The electrical transport and optical measurements results of the devices indicated that they exhibit ultrahigh sensitivity in terms of photon detection.

Most of the SiNW junctions were fabricated using the bottom-up approach [38, 79-83]. While this approach of growing SiNWs is able to produce junctions with axial and longitudinal modulations, there are inherent issues related to the exact placement of SiNWs and it remains a challenge to integrate the SiNWs in a scale suitable for practical applications. As such, from manufacturability perspective, the top-down approach for SiNWs fabrication is preferred. This approach also allows a very dense array of SiNWs to be fabricated to provide very high spatial resolution, and the integration of the sensing application with CMOS circuits.

P-i-n junctions formed along SiNWs via the top-down approach have not been widely investigated so there is strong motivation to study their electrical transport and optical property. In this work, p-i-n junctions formed along SiNWs in an array were fabricated using the top-down approach with a wire cross-sectional dimension of less than 10 nm. Each device comprises 500 SiNWs connected in parallel and was fabricated using thermal oxidation of silicon fins defined by optical

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lithography. Strong rectifying characteristics have been observed for the devices, which confirmed that SiNW p-i-n junctions have been successfully formed. Their photocurrent spectral response has been characterized and several distinct peaks have been observed [84]. This suggests enhanced absorption at certain wavelengths that are not observed in bulk silicon devices.

6.2 Device fabrication

In this work, SiNWs based p-i-n junctions array were fabricated based on the top-down approach using conventional deep-UV optical lithography followed by thermal oxidation. The fabrication process is fully compatible with conventional CMOS technology. The SEM image of the device structure fabricated is shown in Fig 6.1. In each device there are 500 parallel SiNWs with length of 1 μm . They are connected between two big silicon pads and the distance between adjacent SiNWs is 372 nm. The SiNWs are not doped and form the intrinsic region of the p-i-n junctions, whereas the two big silicon pads are heavily doped with P and N type to form the p and n regions respectively of the junctions. The whole device is passivated with a layer of undoped silica glass (USG) (not shown in Fig 6.1). Contact holes are etched on the USG and a layer of metal is deposited on the wafer through the contact holes to form ohmic contacts with the two silicon pads. The deposited metal was subsequently patterned and etched to form large square metal contact pad for electrical probing. The size of the metal contact pad is 70 μm . The overview of the device structure after metal contact formation is shown in Fig 6.2. The details of the fabrication steps involved will be presented in the following

sections.

Fig. 6.1 SEM image of the device structure showing the general device layout with 500 SiNWs p-i-n junctions connected in parallel. Intrinsic SiNWs are connected between the heavily doped P and N type silicon pads to form p-i-n junctions. Scale bar: 400 nm.

Fig. 6.2 SEM image of the entire device after metal contact deposition and patterning. The white square region outlines the SiNW array (zoomed view shown in Fig 6.1). The size of the metal pad for probing is 70 μm.

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6.2.1 Starting wafer

The fabrication process of SiNWs is similar to that reported in section 5.2.1 for single electron transistors (SETs). The starting SOI wafers were (100) orientated, boron doped and with a 120 nm thick silicon top layer having a resistivity of between 9 to 18 $\Omega \cdot \text{cm}$. The BOX layer has a thickness of 150 nm. The schematic of the starting wafer is shown in Fig 6.3.

Fig. 6.3 Schematic of starting SOI wafer with a top 120 nm thick silicon layer.

6.2.2 Si-fin pattern transfer

Alternating phase shift mask lithography with KrF scanner was used to pattern photoresist with a width of 120 nm and length of 1 μm . The mask layout is shown in Fig 6.4 The wavelength of the light source used for the patterning is 248 nm derived from a KrF excimer laser. Oxygen plasma resist trimming was then used to further reduce the resist pattern width. Following that the pattern was transferred to the top silicon layer by reactive ion etching. The silicon etching recipe used consisted of a gaseous mixture of octafluorocyclobutane (C_4F_8) and sulfur hexafluoride (SF_6). The typical etch rate was about 21.3 $\text{\AA}/\text{s}$ and about 60 s of etch time was carried out to etch a depth of 120 nm. After etching silicon down to the

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BOX layer, Si-fins with a width of 45 nm, length of 1 μm and height of 120 nm were created. There are 500 Si-fins in parallel and the pitch of the fins is 372 nm.

The schematic of the structure is shown in Fig 6.5.

Fig. 6.4 Mask layout of the designed Si-fins with 500 parallel Si-fins connected in parallel between two big silicon pads.

Fig. 6.5 Schematic of the silicon fins fabricated on the top silicon layer of SOI wafer.

6.2.3 Thermal oxidation

The device subsequently underwent a dry oxidation process for 4 hours at 875 °C. The Si-fins with a straight etch profile were reduced to SiNWs with diameter less than 10 nm after dry oxidation. The oxidation process will result in diffusion of boron between the SiNWs and the surrounding oxide and hence affect the dopant concentration. It is important to know the exact dopant concentration in the SiNWs as it determines the electrical characteristics of the p-i-n junction formed. The entire SiNWs have been designed to be the intrinsic region of the p-i-n junction and the initial doping of the Si-fins is in the order of 10^{15} cm^{-3} as calculated from the resistivity of the starting wafer which is between 9 to 18 $\Omega\cdot\text{cm}$. To determine the dopant concentration upon oxidation, we have used *Tsuprem* to simulate the thermal oxidation process and deduce the boron concentration in the SiNW. The

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simulated SiNW cross section is shown in Fig. 6.7 and a cutline is drawn to extract the boron doping profile inside the SiNW. As seen from Fig. 6.8, the simulation results indicate that the boron doping in the SiNW after oxidation is lower than that in the Si-fins before oxidation. The boron concentration decreases with oxidation time and the final value after 4 hours of oxidation is estimated to be about $3 \times 10^{13} \text{ cm}^{-3}$. This is expected because the segregation coefficient of boron is less than 1 [85]. Segregation coefficient is defined as the ratio of equilibrium concentration of boron in the silicon to equilibrium concentration of boron in the thermal oxide [85]. Hence there will be an outward diffusion of boron into surrounding oxide during the thermal oxidization process, resulting in a drop in the boron doping concentration in the final SiNWs formed.

Fig. 6.6 Schematic of SiNWs formed between two silicon pads after thermal oxidation. SiNWs are separated at a regular distance of 372 nm.

Fig. 6.7 Simulated SiNW profile and a cutline is shown along which the boron doping distribution is extracted. The scale is in unit of micrometer.

Fig. 6.8 Extracted boron doping distribution in the SiNW along the cutline shown in Fig 6.7. An obvious reduction in the boron concentration inside the SiNW can be observed.

6.2.4 Implantation to form P and N regions

Implant windows were opened consecutively at the two silicon pads connected to the two ends of the SiNWs to dope them with phosphorus and boron. Together with the intrinsic SiNW region they form a p-i-n junction. The mask layout for the implantation process is shown in Fig 6.9. The implantation energy and dose for phosphorus were 30 keV and $4 \times 10^{15} \text{ cm}^{-2}$ respectively, and for boron were 35 keV and $5 \times 10^{15} \text{ cm}^{-2}$ respectively. The dopants were subsequently activated using rapid thermal annealing at 1000 °C for 5 seconds. The concentrations for both dopants at the contact pads were estimated to be in the range of 10^{20} cm^{-3} based on *Tsuprem* simulation along the cutline shown in Fig 6.10. The dopant distribution is shown in Fig 6.11. The high dopant concentrations ensure that good ohmic contacts will be obtained between the silicon pads and subsequent deposited metal.

Fig. 6.9 Implantation mask layout to define P and N region in silicon pads.

Fig. 6.10 Simulation of the silicon pads after oxidation, implantation and 5s annealing. The doping concentration of the dopant at each pad (phosphorus or boron) is extracted from the indicated cutline. The scale is in unit of micrometer.

Fig. 6.11 Extracted doping concentration distributions of phosphorus and boron at silicon pads after implantation and 5s annealing. Doping profile is along the cutline indicated in Fig 6.10.

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6.2.5 Metal contact formation

A layer of 400nm thick undoped silicate glass was deposited to passivate the SiNWs before metallization. Contact holes were defined on the USG and etched through the passivation layer down to the silicon pads. The mask of the contact holes is shown in Fig 6.12. A blanket deposition of 25 nm tantalum nitride (TaN) followed by 750 nm aluminum silicon copper compound by physical vapor deposition (PVD) formed the metal/silicon contacts, as shown in Fig 6.13. The metal layers were patterned into larger contact pads for direct probing. The mask used to pattern metal pad is shown in Fig 6.14. The devices were then annealed in a hydrogen and nitrogen ambient at 420 °C for 30 minutes.

Fig. 6.12 Mask layout of the contact holes on P and N type silicon pads

Fig. 6.13 Schematic of the cross-sectional view of the device structure after metal contact formation. The structure is not drawn to scale.

Fig. 6.14 Mask used to pattern metal. Inset: SEM image of the fabricated device after contact metal patterning.

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The dimension of the SiNW fabricated was examined by transmission electron micrograph (TEM). The TEM samples were prepared by chemical vapor deposition of 100 nm thick SiO_2 from tetraethyl orthosilicate precursor and physical vapor deposition of 500 nm thick platinum before dicing the sample with focused ion beam milling (FIB). The deposited materials protect the samples while they were being thinned by FIB. High-resolution phase contrast mode was used to obtain the atomic scale SiNW cross-sectional image with crystalline structure. As shown in Fig 6.15, the TEM image reveals that the SiNWs are crystalline and have a triangular cross-section with a height and base of about 8nm and 6nm respectively. The crystalline SiNW region was outlined by the white dash line, which shows strong contrast to the surrounding material. The amorphous-like surrounding material has been verified by energy dispersive X-ray spectroscopy (EDX) to be SiO_2 , which was produced during the thermal oxidation process.

Fig. 6.15 TEM image of SiNW embedded in SiO_2 . Scale bar: 10 nm. Dotted line outlines the triangular cross section of the crystalline SiNW.

6.3 Electrical characteristics

The setup for electrical characterization has been discussed in detail in Chapter 3. The I - V characteristic of the device with 500 SiNWs p-i-n junctions connected in parallel is shown in Fig 6.16 in semi-log plot. The measurement was carried out in dark and at room temperature. The applied voltage was swept from -2 V to 2 V to study both the forward and reverse bias characteristics. Very strong rectifying characteristic with a rectifying ratio of more than 9 orders of magnitude, defined to be the ratio of the forward current at 2 V to the reverse current at -2 V, can be observed. This verifies that SiNWs p-i-n junctions have been successfully fabricated.

It is also noted that the reverse bias current is very low at around 100 fA, which translates to about 0.2 fA per SiNW, attributed to the small cross-sectional area of the nanowire junction. With such low dark current, they can be potentially used as ultra-small-scale photodiodes with very high sensitivity. Besides, individual SiNWs are found to be able to withstand current density up to 10^6 A/cm² under strong forward bias.

The I - V characteristic of the measured device has been fitted with the ideal diode equation, as shown in Eq. 6.1:

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (6.1)$$

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where I_s is the reverse saturation current, k is the Boltzmann's constant, T is the temperature, q is the electronic charge and n is the ideality factor. Using Eq. 6.1, the best fitted curve to the linear region of the measurement data (absolute value) in log scale under forward bias range is plotted in Fig 6.16. An ideality factor of around 1.8 was extracted from the best fitted curve of the measured device. An ideality factor close to 1 signifies that the transport mechanism is dominated by diffusion while a value of 2 indicates that the transport is dominated by recombination [41]. Therefore the ideality factor deduced that is much larger than 1 suggests that minority carrier diffusion is not the only carrier transport mechanism. The larger ideality factor could arise from high surface recombination rate due to the large surface to volume ratio of the SiNWs p-i-n junctions [86].

Fig. 6.16 I - V characteristic of a p-i-n diode with 500 nanowires connected in parallel, where strong rectifying effect can be seen. The straight line fitting used for deducing the ideality factor is shown in the plot.

6.4 Optical characteristics

The photocurrent spectral response of the SiNWs p-i-n junctions was measured under illumination with wavelengths between 400 nm and 700 nm. The setup has been described in detail in Chapter 3. A tungsten-halogen source was spectrally filtered by a monochromator and focused to a beam. The beam has a spot size with a diameter $520 \pm 20 \text{ }\mu\text{m}$ at normal incidence to the surface of the chip. The photocurrent of the device was measured by a low noise current preamplifier. The p-i-n junctions were unbiased and the short circuit current was measured.

The photocurrent spectral response was normalized to the power spectrum of the excitation source. The latter was measured by replacing the sample with a calibrated silicon detector. The normalized responsivity is defined as

$$\text{Normalized responsivity}(\lambda) = \frac{I_{PC}(\lambda)}{P(\lambda)} \quad (6.2)$$

where $I_{PC}(\lambda)$ is the photocurrent measured at each wavelength λ and $P(\lambda)$ is the power of the incident illumination at λ . It should be noted that the excitation light source is unpolarized and the devices responded well to optical illumination despite the small photon capture area of SiNWs.

To obtain the actual responsivity R of the SiNWs p-i-n junctions, the normalized responsivity has been corrected for the active area of the SiNWs. The responsivity R can be calculated using the equation:

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$$R = \text{Normalized responsivity} \times \frac{A_{illum}}{A_{active}} \quad (6.3)$$

Where

A_{active} = Active device area

A_{illum} = Illumination area

The active device area is considered as the total area of vertical projection of all the 500 SiNWs. The illumination area is measured by directed the beam into a CCD camera as shown in Chapter 3. The responsivity R can therefore be expressed as:

$$R = \text{Normalized responsivity} \times \frac{\pi r_0^2}{d \times N \times L} \quad (6.4)$$

where

N = number of nanowires

L = nanowire length

d = nanowire diameter

r_0 = effective beam radius

The effective beam radius is measured to be 260 μm and the length of the SiNWs is 1 μm . The calculated responsivity of the p-i-n junction device is shown in Fig 6.17.

Fig. 6.17 Photocurrent spectral response of the 500 SiNWs p-i-n junctions. Several distinct peaks can be observed as indicated by the arrows in the graph.

It is noted that the photocurrent spectral response obtained is quite different from that of a bulk silicon photodiode that has a typical spectrum as shown in Fig. 6.18. As can be seen, the bulk responsivity increases from 400 nm till it reaches a peak at ~950 nm and beyond which it drops sharply [83]. Note that the three distinct peaks seen for our devices at 420 nm, 480 nm and 540 nm are not present in the bulk responsivity. Besides, the overall trend of the responsivity which exhibits a continuous decrease with increasing wavelength is also not observed for bulk devices. This is attributed to the very small cross-sectional dimension of the SiNWs resulting in very different absorption characteristics compared to bulk Si.

Fig. 6.18 Spectral response of a bulk silicon photo diode [87]

The differences in overall trend of the responsivity observed between SiNW and bulk silicon can be explained from simulation of a slab of silicon. The responsivity can be calculated by

$$R = \frac{\lambda(\mu m)}{1.24} (1 - e^{-\alpha t}) \quad (6.5)$$

where λ is wave length of the incident light, α is absorption coefficient, t is the thickness of the silicon slab and the internal quantum efficiency has been assumed to be 1 in the calculation. Assuming that $t = 500 \mu m$ for the bulk silicon wafer, the simulated responsivity R of bulk silicon as a function of wavelength λ is shown in Fig. 6.19. The simulated responsivity is very similar to that of experimental results as shown in Fig . 6.18.

Fig. 6.19 Simulated responsivity of bulk silicon

The responsivity of silicon bulk shows a peak around 950 nm. The responsivity decreases at wavelength larger than 950 nm because as absorption coefficient is getting smaller and only a small fraction of incident light can be absorbed. On the other hand, at shorter wavelength, although the absorption coefficient is high, each photon can only create one electron-hole pair. Higher photon energy at shorter wavelength means less number of photon and leads to less electron-hole pair generated. This consequently leads to less photo current.

In the case of SiNW, for a very thin absorbing layer in which $t \ll 1/\alpha$, the responsivity R is approximately given by:

$$R = \frac{\lambda(\mu m)}{1.24} (1 - e^{-\alpha t}) \approx \frac{\lambda(\mu m)}{1.24} \alpha t \quad (6.6)$$

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Absorption coefficient α is a strong function of incident wavelength λ and decays sharply with increasing λ . Therefore the responsivity in such thin layer is dominated by absorption coefficient α and exhibit continuous decay with wavelength. We have plotted the absorption coefficient of silicon [41] and measured responsivity in Fig. 6.20 and as can be seen, indeed the global shape of the responsivity of our devices overlaps very well with the absorption coefficient spectrum of Si.

Fig. 6.20 Silicon absorption coefficient as a function of wavelength compared to measured responsivity of the SiNWs p-i-n diodes.

Cao and coworkers [88] have identified peaks in the spectral response of the photocurrent of germanium nanowires of diameter 220 – 280 nm due to the leaky geometrical resonances of dielectric nanostructures. Resonance enhanced optical

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absorption has been studied theoretically for SiNWs with cylindrical geometry [89]. The calculations employing Lorentz-Mie scattering theory [90] predicted that for absorption within visible-light regime, i.e. from 400 nm to 700 nm studied in this project, $m = 0$ and $m = 1$ mode for Mie resonance do not occur for SiNWs with diameter less than 20 nm [89]. Given that the SiNWs in our p-i-n junctions have diameter less than 10 nm, we conclude that the three peaks observed in the photocurrent spectral response of our devices is not due to Mie scattering.

The periodic array of SiNWs produces a periodic modulation of dielectric permittivity in one spatial dimension, similar to a diffraction grating, and is an example of a one dimensional photonic crystal. The m^{th} order diffracted wave occurs at a wavelength λ and angle θ satisfying Eq. 6.7,

$$m\lambda = nd\sin\theta \quad (6.7)$$

where $d = 372$ nm and $n = 1.46$ are the spacing between adjacent SiNWs and the optical dielectric constant of surrounding passivation USG, respectively. By setting $\theta = \pi/2$, and $m = 1$, the longest wavelength for which the first order diffraction allowed can be calculated to be around 540 nm. This is in excellent agreement with the rightmost peak observed in the photocurrent spectral response as shown in Fig 6.17. Using the same equation by setting $m = 2$, it can be derived that the second order diffraction takes place for wavelengths less than 270 nm, which is outside the spectral range of measurements in this study. The difference in refractive indices between the surrounding USG and the SiNW suggest that the latter will strongly scatter incident light. Reflection of diffracted wave at air/SiO₂ and reflection at

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SiO₂/Si interfaces is expected to produce resonant field enhancement at some wavelengths and suppression at others. This may possibly account for the other two additional peaks observed in the photocurrent response. To investigate further on the absorption peaks observed experimentally, a detailed simulation of electromagnetic wave propagation on a periodic structure, which has a unit cell comprising air/SiO₂/Si-substrate, was carried out with help of our collaborator Mr. Joe Salfi from University of Toronto. The simulation structure is illustrated in Fig. 6.21. Such a periodic structure resembles our actual device configuration. The unit cell has a width of 372 nm, which is the periodicity of the structure, that is, the distance between adjacent SiNWs in the device.

Fig. 6.21 The unit cell comprising air/SiO₂/Si-substrate that is used for the construction of a periodic structure to simulate the spectral responsivity of the SiNWs p-i-n junction device. The axes are in unit of meter.

As shown in Fig 6.21, the incident light was defined as a plane wave with normal incident to the structure. Since the incident light used for the experiment was unpolarized, two polarizations of light with electric field parallel and perpendicular to the SiNW axis exist. For nanowires with diameter much smaller than the electromagnetic wavelength, it has been shown that the electric field inside the nanowire will be essentially suppressed [91], if the external electric field has a polarization that is normal to the nanowire axis. Therefore in our simulation we have ignored the normal polarization and assumed that the incident light is linearly polarized with polarization parallel to the SiNW axis.

The electric field of the electromagnetic wave inside the SiNW as a result of the plane wave incident on the unit cell structure (Fig 6.21) was calculated using finite element method by COMSOL multiphysics simulator for visible light frequency. The optical properties of intrinsic silicon as a function of wavelength [92] that are needed for the simulation, including the real part (n) of the refractive index and the negative of the imaginary part (k , the extinction coefficient) were input into the software. Periodical boundary condition was applied to the structure to simulate our device that consists of a periodic array of SiNWs. Upon determining the electric field distribution in the structure using COMSOL, the power density absorbed at each point W inside the SiNW can be obtained from the electric field using Eq. 6.8 [93],

$$W = \frac{1}{2} \omega \epsilon_0 \epsilon'' |E|^2 \quad (6.8)$$

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where ε_0 is the dielectric constant of free space, ε'' is the imaginary part of the complex dielectric constant of Si, E is the total electromagnetic field inside the SiNW and ω is the angular frequency of the incident plane wave. The total power absorbed by the SiNW P_{abs} was then obtained by integrating the absorbed power density over the entire SiNW volume, as shown in Eq. 6.9,

$$P_{abs} = \int_{V_{SiNW}} W dV \quad (6.9)$$

This equation can be further simplified to Eq. 6.10,

$$P_{abs} = L \int_A W dA \quad (6.10)$$

where L is the length of the SiNW and A is cross section area of SiNW.

The photocurrent generated in our p-i-n junctions can be expressed as the number of electron-hole pairs swept from the depletion region of the p-i-n junction per unit time. Assuming η is the internal quantum efficiency, which is the ratio of the number of electron-hole pairs collected by the electrode to the number of photons of a given energy absorbed by the SiNW, the photocurrent can be expressed as

$$I_{PC} = \frac{e\eta}{\hbar\omega} P_{abs} \quad (6.11)$$

where $\hbar$ is the reduced Planck's constant.

The power density (optical power per unit area) of the incident electromagnetic wave with an electric field E_0 can be expressed as

$$|S| = \frac{1}{2} |E_0|^2 \varepsilon_0 C \quad (6.12)$$

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The responsivity $\mathfrak{R}$ of the SiNW p-i-n junction diode, defined as the ratio of collected photocurrent to the power of incident electromagnetic wave is given by.

$$\mathfrak{R} = \frac{I_{PC}}{P_{in}} = \frac{I_{PC}}{|S| 2RL} \quad (6.13)$$

where R is the radius of the SiNW and the active area of the SiNW is assumed to be the product of its diameter and length L . By substituting Eqs. 6.8 to 6.12 into Eq. 6.13, the responsivity $\mathfrak{R}$ can be obtained as follows:

$$\mathfrak{R} = \frac{e\eta\epsilon''}{2\hbar Rc} \int \frac{|E|^2}{|E_0|^2} dA \quad (6.14)$$

In Eq. 6.14, the electric field E of the electromagnetic wave inside the SiNW can be determined using COMSOL.

Fig. 6.22 Calculated responsivity of SiNWs in the unit cell structure with periodical boundary condition. Several peaks close to those observed experimentally are noted. Inset: experimental responsivity of SiNW.

Responsivity Spectra	1 st peak	2 nd peak	3 rd peak
Simulated	409 nm	472nm	524nm
Experimental	420nm	480nm	540nm

Table 6.1 Comparison of wavelengths of three peaks between simulated and experimental responsivity spectra.

Using Eq. 6.14, the responsivity of the SiNW p-i-n junctions has been calculated and plotted as a function of wavelength in Fig. 6.22. The internal quantum efficiency η is assumed to be 1 in the calculation, meaning that we have ignored recombination of the generated electron-hole pairs in the device. The simulated

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responsivity reveals resonance peaks at 524 nm, 472 nm and 409 nm, which are close to the experimental peak wavelengths of 540 nm, 480 nm and 420 nm respectively as also compared in table 6.1. At these wavelengths, light diffracted by the periodic nanowire array interferes constructively as a consequence of multiple reflections at the SiO₂/air and SiO₂/Si-substrate interfaces, producing an enhancement of local field, and therefore, enhanced photocurrent. Apart from these three peaks, the response generally follows the trend of absorption coefficient α of bulk silicon (See Fig. 6.20). The local field enhancement caused by this combination of grating/cavity effect produces peaks in the absorption spectrum and suggests that it is possible to engineer light absorption by designing multiple SiNWs in parallel to selectively enhance absorption for specific sensing applications.

6.5 Conclusion

In conclusion, SiNW p-i-n junctions with multiple parallel SiNWs connected to two big silicon pads are fabricated by the top-down approach with optical lithography. SiNWs with diameter less than 10 nm form the intrinsic region of the junction and the two big pads serve as the P type and N type of the junctions. The device exhibits very good rectifying characteristic with very low reverse bias current, which is a consequence of the very small SiNW dimension. It is noted that several resonant peaks exist in the responsivity spectrum of the device, which can be attributed to local optical field enhancement associated with the periodic dielectric structure of the nanowires. This has been verified through our simulation

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of the theoretical responsivity spectrum which exhibits resonant peaks at wavelengths that are consistent with those observed experimentally.

SiNW based p-i-n junction devices fabricated in this work demonstrated interesting enhanced absorption at specific wavelengths in the visible range, which can potentially be tuned by controlling the spacing between adjacent SiNWs. Such devices are extremely small in size and hence can be used as an important component in photonic integrated circuit [94] to provide high sensitivity and high spatial resolution. The SiNW based detector demonstrated is also advantageous due to its compatibility with CMOS technology and suitability for large scale integration.

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7.1 Conclusion

In the project silicon nanowires based devices which include Schottky barrier diode, single-electron transistor and p-i-n junctions array have been designed, fabricated and characterized. The SiNWs were formed on Si SOI wafers using the top-down approach based on optical lithography to first pattern silicon fins, which were then thermally oxidized to reduce their dimension to form SiNWs. The top-down approach is advantageous compared to the bottom-up approach as the process is compatible with Si CMOS technology and can be used to fabricate SiNWs based devices that can be integrated with conventional Si CMOS devices. It also allows large scale integration and hence is attractive from the prospective of manufacturability.

For the fabrication of SiNW based Schottky barrier diodes (SBDs), nickel was deposited on SiNWs with a cross-sectional dimension of around 120 nm. The devices were annealed and nickel reacted totally with a section of the SiNWs to form nickel silicide that served as the Schottky gate electrode. The Schottky barrier was hence formed along the longitudinal direction of the SiNW. Strong rectifying *I-V* characteristics have been measured for the devices, which confirmed that SBDs have been successfully formed. The devices were also noted to exhibit a high breakdown voltage that is at least 70% of the theoretical ideal value without the use

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of any edge termination technique. The high breakdown voltage observed is attributed to its unique structure where the area of the Schottky metal is comparable or even larger than that of the SiNWs such that there are no metal edges and hence no electric field crowding. In contrast, bulk Si SBDs are usually formed with the metal contact area smaller than the active area of Si, resulting in enhanced electric fields at the metal corners and hence premature breakdown. Therefore various complicated edge termination techniques have been built into the fabrication of bulk Si SBDs to improve their breakdown voltages. We have also simulated the electric field distribution in the SiNW based SBDs and compared with that in bulk Si SBDs of the same doping. It is found that the peak electric field in the SiNW SBDs is much smaller, and the field distribution is also more uniform, compared with bulk devices when subjected to the same bias voltage.

The device structure of SiNW based single-electron transistors (SETs) are the same as that of a gate-all-around SiNW MOSFET. In order to achieve single-electron transport at room temperature, very small SiNWs with diameters of only 3 nm to 4 nm, as confirmed by TEM images, were fabricated. Prominent Coulomb oscillations have been observed in the I_d - V_g characteristics of the devices at room temperature. The Coulomb blockade in the devices was also confirmed by low temperature measurements under which stronger oscillation was observed as a result of the reduced thermal voltage of electrons. SETs fabricated using SiNWs of different lengths from 200 nm to 500 nm but same diameter were also investigated. It was found that the Coulomb oscillation was monotonically weakened with

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decreasing SiNW length. The device with the shortest SiNW length of 200 nm revealed $I_d - V_g$ characteristic that is typical of a MOSFET and no oscillation was observed. Our results are consistent with a proposition that formation of SET in SiNW device is attributed to the modulation of bandgap along the SiNW due to a combination of quantum confinement effect and oxidation induced strain in extremely small nanowires. The former increases the bandgap of SiNW whereas the latter lowers its bandgap near the center of the nanowire and results in the formation of a confined Si island sandwiched between two tunneling barriers. Our SETs with shorter SiNWs will experience reduced strain and hence less bandgap lowering. As a result, the tunneling barriers formed are lowered leading to a weakened Coulomb blockade effect. The results also indicate that the SiNW length is a crucial parameter in the design of SiNW based SETs. Our process used for the fabrication of SET is fully compatible with Si CMOS technology, and bypasses the costly and inefficient electron beam lithography technique that was commonly used in such work to ensure room temperature operation. Using our approach, it is also possible to integrate Si SET devices with CMOS devices on a single Si platform to offer new functionalities beyond traditional CMOS devices.

SiNWs p-i-n junctions were fabricated with a structure that consists of multiple SiNWs connected in parallel between two big silicon pads. The SiNWs have cross-sectional dimension of around 8 nm, as confirmed by TEM image. The entire lightly doped SiNW formed the intrinsic region of the junction and the two pads were heavily doped with P type and N type to form the p-i-n junctions. The devices

Chapter 7 Conclusion and future work

exhibit very good rectifying characteristic of up to 9 orders of magnitude between forward and reverse bias of 2 V and -2 V respectively. They also possess very low reverse bias current of 0.2 fA per SiNW, attributed to the extreme small dimension of the SiNWs. The photocurrent spectral responses of the SiNWs p-i-n junctions have been characterized and several responsivity peaks have been observed in the spectral range of 400 to 700 nm. These peaks are ascribed to stronger optical absorption at these wavelengths due to local optical field enhancement associated with the periodic dielectric structure of the SiNWs. At these wavelengths, light diffracted by the periodic nanowire array interferes constructively as a consequence of multiple reflections at the SiO_2/air and $\text{SiO}_2/\text{silicon-substrate}$ interfaces, producing an enhancement of local field, and therefore, photocurrent. The enhanced absorption was also confirmed by theoretical simulation using finite element method, where good agreement between the simulation and experimental resonant peaks has been observed. Our results show that besides providing ultra high spatial resolution for light detection, such SiNWs p-i-n junctions can serve as a good candidate in engineering light absorption for nanophotonics applications.

7.2 Recommendation for future research

There are several aspects of the present research work that can be further investigated.

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7.2.1 Surface treatment

The SiNW fabricated in this work could be further treated with hydrogen annealing to improve the interface quality and hence device performance. The surface condition is important for SiNWs given their large surface to volume ratio. It was also reported that hydrogen thermal annealing can be used for three-dimensional profile transformation by rounding up the sharp corners formed during thermal oxidation [95, 96]. The active device crystalline structure was preserved while the surface roughness could be reduced during the annealing process [97, 98].

7.2.2 External Strain on SiNW

External strain can be induced on SiNWs to investigate its effect on the SiNW based devices investigated in this work. It has been previously reported that external induced strain could modulate the bandgap of SiNW and enhance its carrier transport properties such as carrier mobility and transconductance [98-101]. In the case of single-electron transistors, such an experiment will also be able to shed light on the origin of the tunneling junctions formed in the SiNWs. The external strain can be induced by techniques such as elastic strain relaxation of patterned tensile biaxially strained silicon on insulator layer [102].

7.2.3 SiNW orientation

The crystalline orientation of SiNWs plays an important role in determining the electronic property of the devices fabricated, especially for SiNWs with diameter less than 10 nm. The number of atoms within the SiNW cross-section with such a

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small dimension is only a handful. As a result, the symmetry of crystal structure and orientation of bond between atoms become important [103]. The effects of SiNW orientation on device performance have been calculated theoretically, where it was found that the bandgap values strongly depends on both the diameter and orientation [104]. Therefore it is interesting to explore experimentally the effects of different SiNW orientations on the performance of SiNW based devices with very small SiNW dimensions.

Author's publications

Journal Papers

1. **Sun Yongshun** *et al.*, “Effect of oxidation-induced tensile strain on Gate-all-around silicon nanowire based single-electron transistor fabricated using DUV lithography”, *IEEE Transactions on Nanotechnology*, 10 (6), pp. 1214-1216 (2011).
2. **Sun Yongshun** *et al.*, “Electrical Characteristics and Photocurrent Spectral Response of Si Nanowires p-i-n Junctions”, *Optics Express*, Vol. 19 Issue 6, pp.5464-5469 (2011).
3. **Sun Yongshun** *et al.*, “Room-temperature Operation of Silicon Single-electron Transistor Fabricated Using Optical Lithography”, *IEEE Transactions on Nanotechnology*, 10 (1), pp. 96-98 (2011).
4. **Sun Yongshun** *et al.*, “Silicon Nanowire-Based Schottky Diode With Near Ideal Breakdown Voltage”, *IEEE Electron Device Letters*, Vol. 31, Issue: 11, pp. 1187-1189 (2010).

Conference Presentations

5. **Sun Yongshun** *et al.*, “Electrical characterization of Silicon nanowire p-i-n diodes arrays with varying diameters”, *IEEE International Nanoelectronics Conference*, Taiwan (2011). **(Invited)**.
6. **Sun Yongshun** *et al.*, “Room Temperature Single Electron Transistors Based on Silicon Nanowires”, *Nanomeeting*, Minsk, Belarus (2011). **(Invited)**
7. **Sun Yongshun** *et al.*, “Electrical Characteristics and Photocurrent Spectral Response of Si Nanowires p-i-n Junctions”, *Photonics Global Conference*, Singapore (2010).
8. **Sun Yongshun** *et al.*, “Effect of oxidation-induced tensile strain on Gate-all-around silicon nanowire based single-electron transistor fabricated using optical lithography”, *International Conference on Solid State Devices and Materials*, Tokyo, Japan (2010).
9. **Sun Yongshun** *et al.*, “Silicon Nanowire Based MESFET Fabricated Using CMOS Technology on SOI wafer”, *40th European Solid State Device Research Conference 2010*, Seville, Spain (2010).
10. **Sun Yongshun** *et al.*, “Schottky Contacts Formed on Silicon Nanowires”, *International Conference on Materials for Advanced Technologies*, ICMAT 2009, Singapore (2009).

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