Nanoscale characterization of resistive switching phenomena in HFO₂-based stacks using transmission electron microscopy and atomistic simulation

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**NANYANG
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RESISTIVE SWITCHING PHENOMENA
IN HfO_2 -BASED STACKS USING
TRANSMISSION ELECTRON
MICROSCOPY AND ATOMISTIC
SIMULATION**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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ABSTRACT

This thesis presents a comprehensive study combining electrical characterization, physical analysis, and atomistic simulation on the mechanism of resistive switching. The metal-insulator-semiconductor (MIS) stack based on conventional transistor was used in this study as an effective test structure to understand the chemical origin of switching behavior in the metal-insulator-metal (MIM) stack. The objective of this thesis is to understand the fundamental mechanism governing the nucleation and rupture of the nanosized conductive filaments in resistive random-access memory (RRAM).

To study the chemistry of the localized nanoscale conductive path, electrical characterization techniques were employed to pinpoint the location of the conductive path, then advanced nanoscale analysis tools such as transmission electron microscopy (TEM) along with electron energy loss spectroscopy (EELS) were used to study the elemental composition of the conductive path; finally first-principles calculations were used to further understand the band structure change of the switching material. It is found that the conductive filament consists of oxygen vacancies and the metal filament. There are two stages for the formation of the conductive filament: the initial stage, which is commonly referred to as the soft breakdown stage in MIS gate stack reliability study where the oxygen vacancies are the physical defects responsible for the formation of a percolation path; In the second stage, the metal atoms from the top gate electrode migrate along the oxygen deficient breakdown path driven by the high current density and temperature enhanced metal atom diffusion, forming a metal-rich filament at the central core of the breakdown spot. For the ruptured conductive filament, our physical analysis

results show that metal fragments still remain in the dielectric even after the conductive filaments have been electrically switched-off. It is very likely that the residual metal in the dielectric bonds with the O^{2-} ions forming an insulator.

The direct visualization of the time evolution of uncorrelated multiple conductive filaments in ultra-thin HfO_2 -based high- κ dielectric resistive switching device is reported using advanced *in-situ* TEM for the first time. The locations of the multiple filaments were found to be spatially uncorrelated. The evolution of these microstructural changes and chemical properties of these filaments provides a fundamental understanding of the switching mechanism in ultra-thin oxide films and paves a way for investigations into improving the stability and scalability of RRAM for future sub-10nm technology nodes.

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LIST OF ABBREVIATIONS

AFM	Atomic force microscopy
AOI	Area of interest
BD	Breakdown
C	Capacitance
CASTEP	Cambridge sequential total energy package
CF	Conductive filament
CMOS	Complimentary metal-oxide-semiconductor
Cu	Copper
CVS	Constant voltage stress
D	Drain
DFT	Density functional theory
DBIE	Dielectric-breakdown-induced epitaxy
DBIM	Dielectric-breakdown-induced migration
DOS	Density of states
E	Electric field
EELS	Electron energy loss spectrometry
EOT	Equivalent oxide thickness
FIB	Focused ion beam
GGA	Generalized gradient approximation
HAADF	High angle annular dark field STEM
HBD	Hard breakdown
Hf	Hafnium
HfO ₂	Hafnium oxide
HRS	High resistance state

I	Current
I_d	Drain leakage current
I_g	Gate leakage current
I_{gl}	Gate leakage compliance current limit
I_s	Source leakage current
ICSD	Inorganic crystal structure database
IL	Interfacial layer
ITRS	International technology roadmap for semiconductors
L	Gate length
LDA	Local density approximation
LRS	Low resistance state
M	Metal
MIM	Metal-insulator-metal
MIS	Metal-insulator-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
mA	Mili ampere
μA	Micro ampere
μm	Micro meter
nm	Nano meter
Ni	Nickel
O	Oxygen
PBE	Perdew-Burke-Ernzerhof
Poly-Si	Polycrystalline silicon
Pt	Platinum
RRAM	Resistive random-access memory
S	Source
SBD	Soft breakdown

SCF	Self-consistent field
SCVS	Successive constant voltage stress
SEM	Scanning electron microscopy
Si	Silicon
SiO ₂	Silicon di-oxide
SILC	Stress induced leakage current
STEM	Scanning transmission electron microscopy
STM	Scanning tunneling microscopy
T	Temperature
Ta	Tantalum
TaN	Tantalum nitride
TDDDB	Time dependent dielectric breakdown
TEM	Transmission electron microscopy
Ti	Titanium
TiN	Titanium nitride
TMO	Transition metal oxides
V	Voltage
V _d	Drain voltage
V _g	Gate voltage
V _{gstress}	Gate stress voltage
V _s	Source voltage
V _{TRIG}	Triggering voltage of digital-breakdown
VASP	Vienna ab-initio simulation package
W	Gate width

LIST OF SYMBOLS

A	Ampere
eV	Electron-volt
κ	Dielectric constant
K	Kelvin
μ	Micro

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

With continued scaling down of the metal-oxide-semiconductor field-effect transistor (MOSFET) devices into the nanometer regime, the conventional oxide material silicon oxide (SiO_2) has been pushed to its fundamental limits, accompanied by a replacement of the polysilicon (poly-Si) gate electrode based device technology. Many new materials including the high- κ gate dielectric and the metal gate electrode have already been integrated into the conventional complementary MOS (CMOS) process. According to the 2011 edition of the International Technology Roadmap for Semiconductors (ITRS) [1], hafnium-based oxides (HfO_2), whose dielectric constants have a range of values ~ 20 -25, are the preferred state-of-the-art dielectric material for transistors in the 45 and 32nm technology nodes. Although HfO_2 has been identified as the most practical solution for replacing SiO_2 , many reliability issues still need to be addressed for the new material gate stack.

Dielectric breakdown (BD) is one of the critical failure mechanisms in logic devices [2]. It has been widely accepted that the accumulation of intrinsic defects inside the gate oxide under constant voltage stress (CVS) or constant current stress conditions leads to the formation of a percolation path, bridging the gate and substrate through the oxide [3-5]. This causes the gate leakage current to surge to a relatively high level. Once the percolation path is formed, if the device is continually stressed to evolve into the post-BD regime, the percolated region degrades progressively with gradual increase in current during the wear-out. It is well documented that the post-BD regime in ultra-thin

dielectrics prolongs the device lifetime, providing an additional reliability margin for the transistors [6].

Recent reports on NiSi/HfO₂/Si based gate stack show that reversible BD could be observed in the post-BD regime under certain favorable conditions [7]. The conductive BD path can be “switched-off” and “switched-on” repeatedly, which are similar to RESET and SET in the resistive switching material system [8, 9]. In this study, we apply our understanding of the physics of failure in the post-BD regime of HfO₂ dielectric-based conventional logic transistors having metal-insulator-semiconductor (MIS) structure to interpret the mechanism of resistive switching in resistive random access-memory (RRAM) technology metal-insulator-metal (MIM) stacks.

We present the latest findings using nanoscale high resolution physical analysis techniques such as transmission electron microscopy (TEM), together with electron energy loss spectroscopy (EELS), to study the morphology and chemical nature of nanosized structural defects formed in the oxide layer during different phases of the overall resistive switching process.

We also employ atomistic simulations to correlate the physical observations to theoretical explanation. Many properties of the desired materials can be further explored by the laws of quantum mechanics, which are essentially a set of scientific principles describing the known behavior of energy and matter at the atomic scale. With the advancement of computer hardware and the development of theory and efficient computer algorithms, computer simulation for electronic structure modeling is becoming an important tool in materials research. The development of the density functional theory (DFT) [10, 11] has made calculations with hundreds of atoms possible. Currently, DFT

based on the Kohn-Sham formulation, employing a plane-wave basis set and the pseudopotential approximation are among the most successful techniques in use. The benefits of the first-principles calculation are manifolds: (1) it can provide a fundamental understanding of the experimental findings and probe quantities that are either inaccessible or difficult to be measured by experiments, (2) good quantitative predictions can lead experiments in the right direction, and (3) new material system can be designed even before they are synthesized, which is the ultimate goal.

1.2 OBJECTIVE

The main objective of this study is to extend the post-BD study from the metal gate high- κ system with MIS structure, to better understand the physical nature and mechanism of resistive switching with MIM structure. This thesis provides an in-depth analysis of the switching behavior through a coherent comprehensive study involving electrical data, physical analysis and atomic-level simulations. These were achieved in the following four phases:

1. To provide a comprehensive study on the mechanism of resistive switching combining electrical characterization, physical analysis, and atomistic simulations;
2. To understand the chemical nature of the resistive switching transition in ultra-thin transition metal oxides (TMO), especially the role of oxygen vacancy and metal electrode material;

3. To study the effect of material properties of a BD path in gate dielectric with the switching properties of emerging RRAM devices so as to formulate a hybrid model using a MIS structure;
4. To observe the formation and rupture of the nanosized conductive filament in real time, and study the areal correlation (if any) of multiple conductive filaments.

1.3 SCOPE OF THE PROJECT

This project involves the understanding of resistive switching phenomena in TMO system as well as to study the important physical structures or defects that correspond to the formation of the nanosized conductive filament.

TEM was employed to observe the morphology of the nanosized conductive filament. EELS was used to analyze the chemical component of the conductive filament. *In-situ* TEM was applied to study the formation and “rupture” of conductive metallic filaments in real time, while being electrically characterized. The locations of multiple filaments were also investigated to study the spatial correlation.

Using atomistic simulation to calculate the density of states (DOS) in HfO_2 , oxygen vacancies were found to be responsible for the formation of a sub-band in the forbidden band gap region, which affects the triggering voltage for the post-BD current fluctuations and leads to a shrinkage of the HfO_2 band gap. The metal atoms from the gate electrode could diffuse along the oxygen vacancy pathway among the percolated region in favor of the lowest energy configuration, further reducing the band gap and increasing the leakage current. The formed metallic filament could undergo rupture due

to melt down, caused by significant current-induced joule heating.

The novelty of this work is in the area of bridging the mechanism of post-BD to better understand the resistive switching phenomena.

1.4 ORGANIZATION OF THESIS

This thesis is divided into eight major chapters. The organization of the thesis is as follows:

- *Chapter Two* covers a literature review of the research on high- κ gate dielectric BD as well as resistive switching phenomena. The theoretical background on the first-principles calculation is also reviewed.
- *Chapter Three* explains the procedure and the experimental details of the physical analysis techniques and instrumentation utilized in this study.
- *Chapter Four* presents a comprehensive insight into the role of oxygen vacancies in controlling digital-BD, which is a phenomenon typically encountered in the early stage of the progressive BD process.
- *Chapter Five* reveals the role of metal migration and filament and their effects on the BD recovery behavior of the oxide for metal-gate HfO_2 -based dielectric systems. The study of uncorrelated multiple conductive filament nucleation and rupture is also presented.
- *Chapter Six* introduces the idea of using post-BD conduction studies in MIS logic transistor structure as a tool to better understand the resistive switching mechanism in MIM capacitor stack.

- *Chapter Seven* finally summarizes the results achieved and concludes with further recommendations for future work.

CHAPTER 2 LITERATURE REVIEW

2.1 INTRODUCTION

This chapter provides a review of the BD process and resistive switching phenomena reported in the literature. Different analysis methods associated with gate dielectric BD, and conductive filament based resistive switching model are discussed. Subsequently, the basics of the first-principles calculation are introduced.

2.2 BREAKDOWN MODE

The continuous scaling down of semiconductor devices generates the need for a gate dielectric with a lower effective oxide thickness (EOT), to allow high drive current on the one hand, and a low leakage current on the other [12]. A comparison of the leakage current of various oxides with different EOT values at 1V is shown in Fig. 2-1(a) for traditional SiO_2 and SiON , as well as for the high- κ gate dielectric of HfO_2 [13], La_2O_3 [14], and Al_2O_3 [15]. A significant reduction in the leakage current is evident for the high- κ gate stacks as compared to SiO_2 , which has the same EOT as the high- κ dielectric. According to the 2011 edition of ITRS [1], hafnium-based oxides (HfO_2), whose dielectric constants have a value range of ~ 20 -25, have replaced SiO_2 and SiON as the gate dielectric in MOSFETs since 2008. With a large energy bandgap of 6.9eV, HfO_2 is considered as an excellent insulator. Correspondingly, new metals have been investigated to replace the poly-Si gate electrode of the MOSFETs. These new materials, along with the right process recipe, reduce gate leakage by more than 100 times, as shown in Fig. 2-1(b).

Figure 2-1 (a) Comparison of the leakage current of various oxides with different EOT values at 1V, for various high- κ oxides [16]. (b) Leakage current density versus EOT for HfO_2 with poly-Si gates and TiN gates [17].

However, the device performance is strongly affected by the high density of bulk defects present in HfO_2 and the problems caused by the metals with which it is in contact [16]. Therefore, the study of gate dielectric BD reliability has been a focus of attention.

2.2.1 ELECTRICAL CHARACTERIZATION OF BREAKDOWN

In this section, we provide the electrical characterizations corresponding to various stages of the oxide BD. Figure 2-2 shows an overall picture of a BD evolution,

which consists of five stages. The first one is stress-induced leakage current (SILC). When a huge current jump, two or three times greater than the initial leakage current level of the SILC occurs, time-dependent-dielectric BD (TDDB) occurs. TDDB failures occur when the physical traps align to form a percolation path connecting the gate electrode to the substrate. The physical nature of these traps has been attributed to the presence of oxygen vacancies [18, 19]. After TDDB, the BD process moves to the post-BD region (also called the SBD), which in turn consists of digital-BD (Di-BD) and analog-BD (An-BD). As the name implies, digital-BD corresponds to the random gate current fluctuations among certain fixed current levels. In digital-BD, the average gate current stays constant without any significant change. The later regime of analog-BD occurs when the average leakage current starts to increase, usually in an exponential manner (i.e. power law), towards the set compliance value of say $100\mu\text{A}$. After that, a catastrophic failure happens, which is referred to as the hard BD (HBD). The device at this stage is totally malfunction.

Figure 2-2 An overall picture of BD evolution, which consists of five main stages [6].

Figure 2-3 shows an example of the SILC-TDDB failure for a device tested at a stress voltage of $V_{gstress} = 3.8V$ (substrate injection). The device tested was a TaN gate n-type MOS transistor ($W \times L = 0.09 \times 0.65 \mu m^2$) with a low EOT $9.4 \text{ \AA}$ HfO_2 dielectric.

Figure 2-3 Gate current evolution from the SILC towards TDDB failure for a device tested at $V_{gstress} = 3.8V$.

The SILC was first reported for the SiO_2 dielectric in 1982 [20]. Different models have been proposed to explain the SILC, for example interface trap generation, bulk-oxide electron trap generation, non-uniformities or weak spot formation in the oxide films, and injection of trapped holes from the anode. The SILC can be best explained by the generation of neutral electron traps in the oxide, allowing more current to flow through the oxide layer via these traps which act as “stepping stones” by means of trap-assisted tunneling [21]. It has essentially been reported as a reliability monitor [22]. Though gate current evolution from the SILC towards the TDDB has been studied for many decades, the exact physical mechanism still remains elusive. However, it has been widely accepted that the TDDB happens when defects generated during the SILC stage

continue to accumulate over time until a localized conductance path (percolation path) is formed (Fig. 2-4). The percolation path shorts the anode to the cathode, producing a large current surge through the path [23-25].

The post-BD region consists of two regions namely, digital-BD and analog-BD. Figure 2-5(a) shows the digital-BD profile for a high- κ material system – TiN/HfO₂, stressed at voltages ranging from 2.2 – 3.6V. Figure 2-5(b) shows the digital-BD fluctuations of $V_{gstress} = 2.8V$. I_g exhibited an irreproducible, random step-like profile. The stressing time was fixed at 300s. Report showed that even after very long durations of stressing (~ 18 hours), the digital-BD signature continued to exist without any obvious rise in the current [6].

Figure 2-4 Schematic representations of the formation of the percolation path. The figure shows the sequence of defect generation (step 1), defect coalescence (step 2), and percolation path formation (step 3). Here, the empty circles represent neutral traps, blue circle are electron occupied traps, and the red circles are the traps forming the percolation path, respectively [26].

Figure 2-5 Digital-BD current fluctuations for novel high- κ dielectric stacks on TiN/HfO₂. (a) Gate stress voltages from 2.2V to 3.6V. The stressing time was fixed at 300s at each stage. (b) Digital-BD fluctuations of $V_{gstress} = 2.8V$ is shown. In the digital-BD regime, the average gate current stays constant without any significant change.

When stressing a device in a stepwise sequential manner from a low $V_{gstress} = 1.2V$ to higher values of $V_{gstress}$ in steps of 0.2V, it was found that below a certain critical voltage (V_{crit}) [27], it is very hard to induce the occurrence of the analog-BD, while for $V_{gstress} > V_{crit}$, this transition from the digital-BD to the analog-BD regime occurs quickly,

well within the testing period. Figure 2-6(a) shows one such trend for poly-Si gate SiON 22Å n-type MOS transistors ($W \times L = 0.15 \times 0.15 \mu\text{m}^2$), where the value of V_{crit} is $\sim 3.4\text{V}$.

This concept of V_{crit} has an important implication on the duration of the digital-BD regime in the post-BD stage. Lo *et al.* [27] reported that for an ultra-thin SiON dielectric system, the V_{crit} for ultra-thin oxides was found to be much larger than the operating voltage V_{op} , thus making it very hard to induce an analog-BD in the circuit during nominal operating voltage conditions, as shown in Fig. 2-6(b). The prolonged digital-BD regime also implies extended device functionality. It is interesting to note that this still holds true for the high- κ dielectric in the post-BD regime.

There are several explanations for post-BD, including localized damage producing an effectively thinner oxide layer [28]. The presence of noise was explained as a result of electron trapping and detrapping from the damaged BD region. It was also observed that the current fluctuations were due to variable range hopping [29] and post-BD was due to a locally modified energy barrier [30]. Bude *et al.* [31] described the occurrence of post-BD as a result of inadequate energy transfer from the tunneling electrons to the holes that were injected at the anode. Suñé *et al.* [32] modeled the post-BD conductance as a tunneling through a quantum point contact. But still, in-depth study is needed to further understand the nature of the BD path.

Figure 2-6 (a) Leakage current trends for $V < V_{crit}$ and $V > V_{crit}$ during the stepwise constant voltage stress (CVS) period. The transition from digital-BD to analog-BD is found to occur at $V \cong V_{crit}$ [27]. (b) Trend of V_{crit} and operating voltage, V_{op} , for SiON dielectric as a function of its thickness [27].

2.2.2 PHYSICAL FAILURE ANALYSIS OF BREAKDOWN

This section provides a brief insight into the physical nature of the traps and the microstructural defects underlying the evolution trends of leakage current during BD. It is

important to understand and investigate the cause of the different failure regimes existing in oxide BD and the role of the injected electrons and the electric field.

Figure 2-7 shows an overall picture of the MOSFET microstructural changes taking place during BD [33]. Grain boundary, metal filament, dielectric-breakdown-induced-epitaxy (DBIE) and dielectric-breakdown-induced migration (DBIM) are considered as common physical defects that occur during the process of BD. All these defects will be introduced in detail in the following section. Note that the grain boundary here might be the intrinsic defect in HfO_2 dielectric, and will eventually cause high gate leakage current.

Figure 2-7 An overall picture of the MOSFET microstructural changes taking place during BD [33].

Transmission electron microscopy (TEM) along with electron energy loss spectroscopy (EELS) have been used to study the chemical nature of the BD path in SiON ultra-thin gate dielectrics. It has been reported that as compared to an unbroken oxide, the oxide stressed and failed due to the percolation path has a very low oxygen

content. It implies that the local chemical structure of a percolation path is SiO_x , where $x < 2$. Therefore, oxygen vacancies are the precursors for dielectric BD [18, 34]. Furthermore, oxygen vacancy defects are the most likely intrinsic defects in ZrO_2 and HfO_2 in terms of their formation energies. Defects at the metal site would result in greater energy [35, 36]. Further studies on the HfO_2 gate dielectric also indicated that the oxygen atom concentration within the BD path is very low [37].

Grain boundaries will cause higher leakage current and will lead to a possible BD path [16]. It was reported that at higher annealing temperatures ($500 - 1000^\circ\text{C}$), thin HfO_2 film becomes more crystallized, and crystallization makes it more susceptible to leakage, due to the conduction through the grain boundaries [38]. Conduction through the $\text{HfO}_2/\text{SiO}_2$ stack was studied at the nanoscale level using the scanning tunneling microscopy (STM) technique [39]. The current was found to be higher when probed over the grain boundaries (see Fig. 2-8), indicating higher conduction along the grain boundaries.

Figure 2-8 A STM constant current tunneling spectroscopy map of the 5nm $\text{HfO}_2/1\text{nm}$ SiO_2 stack at $V_{\text{stress}} = 3.5\text{V}$. Dotted lines (in green) outline the grain boundaries [39].

In the post-BD regime, the high current density through the percolation path and the thermal gradients surrounding the path serve as the driving forces for the thermomigration phenomenon. This causes silicon from the substrate or gate (whichever is the cathode terminal) to protrude through the oxide layer, leading to an effectively thinner oxide with an increased electric field. This eventually causes the two terminals to short. This epitaxial defect, detected in TEM analysis (Fig 2-9), is called DBIE. DBIE was first reported on the SiON gate dielectric by Tung *et al.* [40]. Further studies suggested that it is a universal microstructural defect signature for dielectric BD [41, 42].

Once the gate oxide is ruptured by the presence of a DBIE, it may subsequently trigger several other severe microstructural damages, DBIM [43-47] being one of them. Figure 2-10 shows a recent observation of the switching behavior during post-BD conduction in NiSi-gated high- κ stacks, which NiSi DBIM acts as an oxygen storage [7]. The migration of Nickel happens on the drain side which is closer to the original BD spot. Ni further migrates into the channel, and makes a metal(NiSi)-insulator(HfO₂)-semiconductor(Si-substrate) structure to a metal(NiSi)-insulator(HfO₂)-metal(NiSi) structure.

Figure 2-9 TEM images of both the grain boundary and DBIE observed in the analog-BD region of a n-type MOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$), tested under $V_{g\text{stress}} = 3.6\text{V}$. DBIE is indicated by dashed lines, while the grain boundary is indicated by dotted lines [48].

Figure 2-10 A NiSi/HfO₂ n-type MOSFET recovered from severe breakdown. DBIM is found near the drain end in the TEM analysis. The insert shows the entire transistor [7].

Another common failure mechanism seen in high- κ gate stacks is the presence of a metal filament. If the gate material is a metal such as TaN/TiN, then the metal atoms have also been observed to migrate into the dielectric in the post BD stage for a large leakage current. This metal filamentation is highly conductive and can cause a very fast catastrophic breakdown of the transients instead of the progressive degradation generally observed in the analog-BD regime [49].

2.3 RESISTIVE SWITCHING IN TRANSITION METAL OXIDE SYSTEM

2.3.1 RESISTIVE SWITCHING

The impressive growth of the portable electronic systems market has been sustained by the availability of successful semiconductor non-volatile memory (NVM) technologies [50]. Charge-based memory containing hundreds of millions of MOSFETs, such as flash memory and dynamic random access memory (DRAM), tends to suffer

from performance degradation issues. One issue is the tunnel oxide scalability limitation, which cannot be further thinned down without impairing data retention. The other issue is the electrostatic interactions between adjacent cells resulting in cross-talk. The development of non-charge-based memory is therefore essential to achieve NVM with high speed, high density, and low power consumption. RRAM is one of the most promising candidates for the next generation of NVM, given its advantages in terms of fast writing/erasing times (< 100 ns), long retention lifetime (> 10 years), low power consumption, and CMOS technology compatibility [9, 51-54]. In addition, RRAM is also suitable for the three-dimension stacking of memory layers, which can prompt the realization of very high-density memory [55].

2.3.2 PHYSICAL STORAGE MECHANISMS

The operational mechanism of RRAM is based on a reversible breakdown of an insulating dielectric. RRAM is a simple two-terminal device in which the resistance of the device can be reversibly and repeatedly switched between a high resistance state (HRS) and a low resistance state (LRS) for different applied voltages, where these states are referred to as ‘0’ and ‘1’ in digital circuits. The device is composed of an insulating layer, sandwiched between two metal electrodes which could be the same or different materials. From a microscopic point of view, a recent review report by R. Waser classified the resistive switching mechanisms into electrochemical metallization mechanism, valence change mechanism, and fuse-antifuse mechanism, as shown in Figure 2-11 [52].

Figure 2-11 Classification of the resistive switching mechanisms with redox-related chemical switching effects (red bracket). The switching mechanisms based on electrochemical, valence change, and thermochemical effects (three classes on the left) are reviewed in the text [52].

Firstly, in the electrochemical metallization mechanism, the migration of the highly mobile electrode metal forms a conductive filament during SET and can be electrochemically dissolved upon a applied voltage with reverse polarity. For example, it is convincingly demonstrated in Refs. [56] and [57] that the electrochemically active electrode metal Ag^+ ions can punch through the insulating layer, setting the device to ON state. The metal filament undergoes dissolution under electrochemical current (also called Faradaic current) when a reverse voltage bias is applied, resetting the system to OFF state. The insulating layer for this mechanism is usually a solid electrolyte layer without oxygen ions, i.e., Ag_2S and Ag-Ge-Se .

Secondly, in the valence change mechanism, specific TMO are chosen as the insulating layer [9, 58-63]. The creation and migration of the oxygen vacancies lead to a redox reaction expressed by the valence state change of the cations. Upon SET, dislodged

oxygen species from the TMO migrate to the electrode material (typically made of Ni, Ti, Ta, etc.), which serves as a good reservoir for oxygen in the ionic form [64]. Under a reverse bias, the O^{2-} ions stored in the gate are driven back to the oxygen-deficient conductive path. The devices driven by electrochemical metallization mechanism and valence change mechanism usually show bipolar behavior, in which SET and RESET voltages are of opposite bias polarity.

Thirdly, in the fuse – antifuse mechanism, the conductive filament fusion is a thermal runaway process by applying an electric field. It is well documented that in all insulating and semiconducting materials, the conductivity of the material is dependent on the temperature exponentially [65-68]. In the anti-fuse process, the conductive filament is ruptured by joule heating-assisted reduction [69, 70]. In this case, resistive switching can be achieved with one bias polarity, and is thus called unipolar switching behavior. Both bipolar and unipolar switching behaviors have been observed in HfO_2 based dielectric stacks [59, 71]. Several materials also show both types of switching behaviors [72, 73].

Among various resistive switching models, the conductive filament theory draws a lot of attention because it is similar to a BD path: a nanosized conductive path is formed connecting the top and bottom electrodes and yielding a drop of resistance. A high resistance is obtained by the RESET operation, where the application of a voltage results in a recovery that breaks the BD path. It is illustrated in Fig. 2-12 [74]:

Figure 2-12 Conductive filament model: (a) RESET state: the conductive filament is electrically “switched-off”. (b) Apply SET voltage results in an electronic conductive filament, causing thermal damage, and (c) A conductive filament forms, switching to a SET state. Alternatively, recovery can restore the RESET state [74].

Szot *et al.* [75] reported defects in SrTiO_3 could act as bistable nanowires that switch between ON and OFF states. Figure 2-13(a) shows the atomic force microscopy (AFM) results of the conductivity map. Figure 2-13(b) shows that the electrical switching depends on localized BD percolation path. However, as AFM directly probed the dielectric layer, this study failed to consider the effect of electrode materials.

Figure 2-13 (a) Conductivity map of the surface of a SrTiO_3 crystal by AFM. Filamentary paths with enhanced conductance are present on the surface. Inset: spot with a dimension of 1 – 2nm, where the main current is concentrated. (b) Line scan across the selected spot showing the dynamic range of the resistance change as a result of the application of voltage bias. Right: Conductivity maps of the selected spot before (n_1) and after forming (n_{15}). The diameter of the filamentary increases from 5 to 10nm [75].

Kwon *et al.* [58] studied the TMO-based RRAM device with electrodes. They chose a sandwich structure of $\text{Pt/TiO}_2/\text{Pt}$, and the thickness of the TiO_2 layer is ~50nm.

High resolution *ex-situ* TEM micrographs in Fig. 2-14(a) and (b) show connected and disconnected nanofilament, respectively. However, the interface between the Pt and TiO_2 is very rough. It remains unclear whether the surface defect plays an important role. Moreover, Pt is a noble metal with high price, limiting the commercial use of RRAM devices with low-cost.

Figure 2-14 High resolution TEM micrographs of (a) a connected Ti_4O_7 phase nanofilament in SET state; and (b) a disconnected Ti_4O_7 nanofilament in RESET state [58].

2.4 FIRST-PRINCIPLES CALCULATION

After understanding the electrical characterization and the physical nature of the BD, it would be interesting to use the atomic scale simulation to unearth the mechanism of BD. DFT is one of the most popular tools in the first-principles calculation.

2.4.1 SINGLE ELECTRON SCHRÖDINGER'S EQUATION AND MANY-BODIED PROBLEM

The fundamental basis for understanding materials and phenomena ultimately rests upon the understanding of electronic structures [76, 77]. Problems in the electronic structure can be addressed by time-dependent Schrödinger's equation. In most cases, we only concern with problems without time-dependent interactions, so we will only deal with the stationary Schrödinger's equation. Single electron time-independent Schrödinger's equation is given as

$$\hat{H}\varphi(r) = E\varphi(r) \quad (2.1),$$

where E is the eigenenergy of the electron and $\varphi(r)$ is the single electron wavefunction description. $\hat{H}$ is the Hamiltonian operator and is given as

$$\hat{H} = -\frac{\hbar^2}{2m}\nabla^2 + V(r) \quad (2.2),$$

where $V(r)$ is the external potential field. It is easy to solve single electron time-independent Schrödinger's equation. However, for a two-electrons system,

$$\left\{ -\frac{\hbar^2}{2m_1}\nabla_1^2 - \frac{\hbar^2}{2m_2}\nabla_2^2 + V(r_1, r_2) \right\} \varphi(r_1, r_2) = E\varphi(r_1, r_2) \quad (2.3),$$

the item $V(r_1, r_2)$ usually can not be separated. There is no analytical solution for Eq. (2.2) nor (2.3) unless the potential was known. This is so called many body problems. The real material bulk is made of a large number of interacting particles.

To solve many body problems, Hohenberg and Kohn formulated the theorems in 1964 that constitute the theoretical basis of DFT, where the electron density $n(r)$ plays the central role [78]. The central ideas of the theorems are the following:

Theorem 1 (Uniqueness) The ground state expectation value of any observable is a unique functional of the exact ground state electron density $n(r)$.

$$E_{Ground\ State}[\Psi(r_1, r_2, r_3, \dots, r_N)] \rightarrow E_{Ground\ State}[n(r)] \quad (2.4).$$

This means that, in the ground state, if the electron density and the wavefunction are known, it is possible to calculate all properties of the system. In particular it is possible to calculate the ground state energy $E[n]$.

Theorem 2 (Variational principle) Ground state electron density $n(r)$ minimizes the total energy functional $E[n]$.

$$E_{Ground\ State}[n(r)] \geq E_{Ground\ State}[n_{Ground\ State}(r)] \quad (2.5).$$

This means that, the expectation value of the ground state energy for the trial wavefunction must be greater than or equal to the actual ground state energy.

It is worth to note that many properties of materials can be exploited based on ground state, such as bond length, crystal lattice constant, band structure, and DOS.

The Hohenberg-Kohn theorems only show the validity of variational principles used in ground state energy and ground state electron density, but does not provide accurate mathematic formula of ground state energy.

The next step is what Kohn and Sham did in 1965 [10], to separate $E_{Ground\ State}[n(r)]$ into four terms.

$$E[n(r)] = T[n(r)] + E_H[n(r)] + E_{ext}[n(r)] + E_{xc}[n(r)] \quad (2.6),$$

where $T[n(r)]$ is the electron kinetic energy

$$T[n(r)] = \frac{1}{2} \sum_i \psi_i^*(r) \nabla^2 \psi_i(r) d^3r \quad (2.7),$$

$$n(r) = \sum_i |\psi_i(r)|^2 \quad (2.8),$$

$$N = \int n(r) d^3r = \sum_i \int \psi_i^*(r) \psi_i(r) d^3r \quad (2.9).$$

Equation 2.9 is the orthonormal constraint. $E_H[n(r)]$ is the classical electrostatic potential :

$$E_H[n(r)] = \int n(r') n(r) |r' - r| d^3r' = \int V_H(r) n(r) d^3r \quad (2.10).$$

$V_H(r) = n(r') |r' - r| d^3r'$ is so called Hartree energy, which is the electrostatic coulomb potential. $E_{ext}[n(r)]$ is external potential effect:

$$E_{ext}[n(r)] = \int V_{ext}(r) n(r) d^3r \quad (2.11).$$

Now three of the four terms can be decided except E_{xc} , which will be discussed in the following section. The most important contribution from the Kohn-Sham theorems is that it proves that $E_{Ground State}[n(r)]$ is universal in the sense that it does not depend on external potential $U_{Ground State}[n(r)]$.

2.4.2 THE LOCAL DENSITY APPROXIMATION (LDA) AND GENERALIZED GRADIENT APPROXIMATION (GGA)

In DFT, the exact form for the exchange-correlation energy E_{xc} as a functional of electron density is not known and has to be approximated. The most common approximation to the exchange-correlation functional $E_{xc}[n]$ is the local density approximation (LDA). Kohn and Sham pointed out that solids can often be considered as close to the limit of the homogeneous electron gas. The idea is that the inhomogeneous

electronic system can be considered locally homogeneous, and exchange correlation for a homogeneous gas of interacting electrons can be used. It can be shown that if $n(r)$ is slowly varying $E_{xc}[n]$ can be written as

$$E_{xc}[n] = \int n(r)\varepsilon_{xc}(n(r))dr \quad (2.12),$$

where $\varepsilon_{xc}(n)$ is the exchange-correlation energy per electron of a uniform electron gas of density n , which has been extensively studied and whose properties were well known. LDA therefore assumes that ε_{xc} is local, and neglects the possible effects from inhomogeneous around the position $\mathbf{r}$. The exchange-energy functional in LDA can be derived in an exact form [76], and the correlation energy for a homogeneous gas involves various approximations and fittings. A popular correlation functional is a parameterization by Perdew and Zunger [79] that fits to quantum Monte Carlo (QMC) calculations by Ceperley and Alder [80].

The LDA, exact for a uniform electron gas, was a priori expected to be useful only for materials with slowly varying densities. Nevertheless the LDA has shown accurate results for most applications, even for some cases with rapidly varying densities. This success can be partially attributed to the fact that the LDA always gives the correct sum rule for the exchange-correlation hole. LDA usually gives ionization energies of atoms, dissociation energies of molecules and cohesive energies with a fair accuracy of typically 10-20%. For the bond-lengths and typical geometries of molecules and solids, an accuracy of ~1% can be achieved.

The Generalized-Gradient Approximation (GGA) uses a functional of the gradient of the density $|\nabla n|$ as well as the density n at each point; typically GGA favors density inhomogeneity more than LDA does. GGA expands and softens bonds, an effect that

sometimes corrects and sometimes overcorrects the LDA prediction. Widely used GGAs can now provide the accuracy required by the chemistry community, but the GGA does not lead to consistent improvement over LDA. One of the popular GGA functional is Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional [81].

The approximations used in many of LDA and GGA functions are often inadequate in materials in which the electrons are localized and strongly interacting. These materials include the TMO and rare earth elements and compounds. For strongly correlated materials such as transition metal oxides where the electrons are highly localized, an additional orbital-dependent interaction can be added to the usual LDA or GGA calculations, termed as “LDA+U” method. In this thesis, “GGA+U” method has been used.

2.4.3 SELF CONSISTENT FIELD

Equation 2.6 is a constrained minimization problem that can be performed using the Lagrange method. Because $\psi_i^*(r)$ is a complex function with the form of $a(r) + ib(r)$ of two free degree, thus we can consider $\psi_i^*(r)$ and $\psi_i(r)$ as two independent functions. The variation results of $\psi_i^*(r)$ are the following:

$$\frac{\delta T(n)}{\delta \psi_i^*(r)} = \frac{1}{2} \psi_i(r) \quad (2.13),$$

$$\frac{\delta E_H(n)}{\delta \psi_i^*(r)} = V_H(r) \psi_i(r) \quad (2.14),$$

$$\frac{\delta E_{ext}(n)}{\delta \psi_i^*(r)} = V_{ext}(r) \psi_i(r) \quad (2.15),$$

$$\frac{\delta E_{xc}(n)}{\delta \psi_i(r)} = \left\{ \frac{\delta E_{xc}(n)}{\delta n(r)} \right\} \left\{ \frac{\delta n(r)}{\delta \psi_i(r)} \right\} \equiv V_{xc}(r) \psi_i(r) \quad (2.16).$$

Lagrange multiplier λ is introduced:

$$\frac{\delta \lambda N}{\delta \psi_i(r)} = \lambda \psi_i(r) \quad (2.17).$$

Summarizing the above equations, we have

$$[H - E_i] \psi_i = \left[\frac{1}{2} \nabla^2 + V_H + V_{ext} + V_{xc} - E_i \right] \psi_i = 0 \quad (2.18).$$

Equation 2.18 is a typical differential equation problem. Because ψ_i is unknown at the beginning, we need to guess a set of ψ_i , subsequently obtain $n(I)$, then get a new set of ψ_i . This procedure repeated until $n(N) = n(N+I)$. The iterative minimization procedure is so called self-consistent field (SCF) method.

2.4.4 SUPERCELL APPROACH AND PLAN WAVE BASIS

The Kohn-Sham equations mapping the interacting many-electron system onto a system of non-interacting electrons in an effective potential created by all the other electrons, along with SCF method, it is possible to solve many body problems. However there are an infinite number of electrons moving in the static potential of an infinite number of nuclei in solid materials. These problems can be tackled by performing calculations on periodic systems and applying Bloch's theorem to the electronic wavefunctions [82].

All crystalline solids can be described in terms of the Bravais lattice, which specifies the periodic array in which the repeated units of the crystal are attached, and the

unit that can be a single atom or a group of atoms. The three-dimensional Bravais lattice consists of all points with position vector $R = n_1a_1 + n_2a_2 + n_3a_3$, where a_1 , a_2 and a_3 are the three basis vectors, and n_1 , n_2 and n_3 are any positive integer values. The reciprocal lattice vector is defined as $G = k_1b_1 + k_2b_2 + k_3b_3$ with the three basis vectors b_1 , b_2 and b_3 in the reciprocal space given by

$$b_1 = 2\pi \frac{a_2 \times a_3}{a_1 \cdot (a_2 \times a_3)}; b_2 = 2\pi \frac{a_3 \times a_1}{a_2 \cdot (a_3 \times a_1)}; b_3 = 2\pi \frac{a_1 \times a_2}{a_3 \cdot (a_1 \times a_2)} \dots \quad (2.19).$$

In periodic solids, Bloch theorem can be applied to find the electronic wavefunctions. With the one electron Hamiltonian $\hat{H} = -\sum_i \frac{\hbar^2}{2m_i} \nabla_i^2 + U(r)$, where $U(r+R)=U(r)$ in a Bravais lattice, each electronic wavefunction can be written as a product of a plane wave and a function with the periodicity of the Bravais lattice:

$$\psi_i(r) = e^{ik \cdot r} u_i(r) \quad (2.20);$$

or in its equivalent form:

$$\psi_i(r + R) = e^{ik \cdot r} \psi_i(r) \quad (2.21),$$

for every R in the Bravais lattice.

The periodic function $u_i(r)$ can be expanded using plane waves as a basis set whose wave vectors are reciprocal lattice vectors of the crystal,

$$u_i(r) = \sum_G c_{i,G} e^{iG \cdot r} \quad (2.22).$$

Thus each electronic wavefunction can be written as a sum of plane waves by substituting Eq. (2.22) into Eq. (2.20),

$$\psi_i(r) = \sum_G c_{i,k+G} e^{i(k+G) \cdot r} \quad (2.23).$$

The Bloch theorem transforms the problem of calculating an infinite number of wavefunctions in real space into one of calculating a finite number wavefunctions at an infinite number of $\mathbf{k}$ points in reciprocal space. In principle, an infinite number of calculations are still needed for these k points. However, the electronic wavefunction at k points that are very close together will be almost identical. Thus, calculations for the electronic states at a finite number of $\mathbf{k}$ points are able to determine the total energy of the solid. Various efficient k -point sampling schemes have been proposed and the Monkhorst-Pack $\mathbf{k}$ -point sampling is the most widely used scheme [83]. The Monkhorst-Pack k -point sampling scheme produces equally spaced discrete k -point mesh in the Brillouin zone. Using efficient $\mathbf{k}$ -point sampling schemes, the electronic potential and total energy can be determined by calculating the electronic states at a small number of $\mathbf{k}$ points. The convergence of total energy with $\mathbf{k}$ -point sampling should always be checked and the magnitude of any error in the total energy due to insufficient k points can be reduced with a denser set of $\mathbf{k}$ points.

The wavefunctions can be expanded using plane waves. Although many different basis sets can be used to expand electronic wavefunctions, such as localized atom-centered orbitals, Gaussian orbitals and Wannier functions, plane waves allow the Hamiltonian to be evaluated efficiently and an easy analytical evaluation of forces and of the stress tensor. Using a vector notation for the basis where $e^{i(k+G) \cdot r} = |k + G\rangle$, the matrix element of the kinetic energy operator is

$$\langle k + G | - \sum_i \frac{\hbar^2}{2m_i} \nabla_i^2 | k + G \rangle = \frac{\hbar^2}{2m} |k + G|^2 \delta_{G,G'} \quad (2.23).$$

It can be seen that this matrix is diagonal and the kinetic energy for a plane wave with wave vector of $k+G$ is simply $\frac{\hbar^2}{2m} |k + G|^2$. The effective potential $V_{eff}(r)$ in the solid is also periodic and after Fourier transformation it becomes

$$V_{eff}(r) = \sum_m V_{Gm} e^{iG_m \cdot r} \quad (2.24),$$

where G_m is the reciprocal lattice vector. Thus the matrix element of the effective potential is

$$\langle k + G | V_{eff} | k + G \rangle = \sum_m V_{Gm} \delta_{Gm, G' - G} \quad (2.25).$$

Now the Kohn-Sham equation in Eq. (2.6) can be written in a simple form when a plane-wave basis set is used. This is given as

$$\sum_{G'} \left[\frac{\hbar^2}{2m} |k + G|^2 \delta_{G,G'} + V_{G,G'} \right] c_{i,k+G'} = \varepsilon_i c_{i,k+G} \quad (2.26).$$

The solution of Eq. (2.26) can be found by a diagonalization of the Hamiltonian matrix. The size of the Hamiltonian matrix is determined by the cutoff energy, which in turn determines the number of plane wave basis. The full diagonalization of the Hamiltonian matrix calculates the Kohn-Sham eigenvalues of all the electronic states. However, only those of the lowest occupied states are required to calculate the total energy. Hence the full diagonalization method is not an efficient way to solve this Kohn-Sham equation [84]. As such, many efficient matrix diagonalization methods, such as the

conjugate gradient algorithm and residual vector minimization scheme, have been developed.

The plane-wave basis set has to be truncated to include plane waves that have kinetic energy $\frac{\hbar^2}{2m}|k + G|^2$ which is smaller than some particular cutoff energy. Too small a cutoff energy will introduce an error in the calculated total energy while too large a cutoff energy will slow down the calculations. Hence it is necessary for any calculations to find a cutoff energy that is sufficient for the convergence of the total energy.

2.4.5 PSEUDOPOTENTIALS

Although in principle any wavefunctions can be expanded using a discrete set of plane waves, a plane wave basis is not suitable to expand the tightly bound core orbitals. At the tightly bounded regions near the nuclei, the wavefunctions for electrons oscillate rapidly, and a large number of plane waves is needed to expand these wavefunctions. Therefore, it is computationally costly to perform an all-electron calculation with a plane-wave basis. The pseudopotential approximation allows the electronic wavefunction to be expanded using a much smaller number of plane waves. Another important consequence is that the total energy with pseudopotential approximation is typically a thousand times smaller than the all-electron calculations while the energy difference between different ionic configurations remains essentially the same because this depends on the energy of the valence electrons. Hence the accuracy required to determine energy differences between different ionic configurations in pseudopotential calculations is much smaller than the accuracy required in all-electron calculations.

Figure 2-15 Schematic illustration of all-electron (solid lines) and pseudo-electron (dashed lines) potentials and their corresponding wavefunctions. The radius at which all-electron and pseudo-electron wavefunction values match is denoted as r_c [85].

It is well known that most physical properties of solids depend more on valence electrons rather than core electrons. In most cases the core electrons are strongly bound and do not respond effectively to the motions of the valence electrons. Thus the pseudopotential approximation removes the core electrons and uses a much weaker potential to replace the strong core potential, which is $-\frac{Ze^2}{r}$ plus the Hartree potential due to the core electrons as well as a component of the exchange-correlation potential related to the valence-core interaction. Thus the electronic wavefunctions (now pseudo wavefunctions) can be expanded using a much smaller number of plane wave basis. An ionic potential, valence wavefunction and corresponding pseudopotential and pseudo wavefunction are shown in Fig. 2-15. A nodeless ground state wavefunction $\psi^{ps}(r)$ from this pseudopotential mimics the all-electron wavefunction $\psi^{ps}(r)$ outside a selected core

radius r_c . For many elements, the pseudo-wavefunctions $\psi^{ps}(r)$ are quite smooth and may be well represented using plane waves with a low wave vector $\mathbf{G}$.

The early accurate, transferable pseudopotentials are norm-conserving, and introduced by Hamann, Schlüter and Chiang. The norm-conserving pseudopotentials require that the all-electron wavefunctions and the soft nodeless pseudo wavefunctions have the same norm within some core radius while outside the core radius the all-electron wavefunctions and the pseudo wavefunctions are identical. However it is computationally costly to treat elements with strongly localized orbitals, such as first-row elements, transition metals and rare-earth elements. For better computational efficiency, one goal of pseudopotentials is to have pseudo wavefunctions as smooth as possible. Vanderbilt proposed an elegant “ultrasoft pseudopotentials” (US-PP) within which the norm conserving requirement is relaxed and to make up for the resulting charge deficit, localized atom-centered augmentation charges are introduced. However, it is rather difficult to construct the US-PP as it involves too many parameters and extensive tests are required in order to obtain an accurate and transferable pseudopotential.

2.5 SUMMARY

Metal gate high- κ gate dielectric BD is one of the most important reliability concerns in MOSFET miniaturization. The process of BD has been discussed in detail. The classes of resistive switching mechanism have also been introduced. To explore the fundamental material properties, the first-principles calculation based on quantum theory has been widely used. We will use the DFT based method to investigate the band structure, density of states, and oxygen-related defect formation energy in a high- κ material like HfO_2 .

CHAPTER 3 METHODOLOGY AND EXPERIMENTAL PROCEDURE

3.1 INTRODUCTION

In this chapter, the details of the electrical characterization and the physical characterization methodologies that were used to study the resistive switching phenomena are discussed. CVS consisting of successive and multi-stage were used to control the evolution of conductive filament. TEM and EELS were then used to pinpoint the localized conductive filament morphology and the chemical component. The physical analysis results are subsequently linked back to the electrical characteristics of the device. With the knowledge acquired from the physical analysis, a comprehensive understanding of the material properties is developed by atomistic simulation as well. The design and fabrication technologies can be improved too. The overall flow of the methodology is illustrated in the schematic diagram in Fig. 3-1.

Figure 3-1 Schematics describing the comprehensive methodologies used in this study.

3.2 ELECTRICAL CHARACTERIZATION

3.2.1 PROBE STATION

The equipment used for the electrical characterization consists of a 8-inch (200mm) CASCADE MICROTECH manual probe station system and a KEITHLEY INSTRUMENTS model 4200-SCS semiconductor characterization system, which is shown in Figs. 3-2(a) & (b). The 8-inch CASCADE MICROTECH manual probe system including a thermo-chuck (0°C to +300°C) serves as the platform to hold the wafer at different temperatures. The stressing and various electrical measurements of a MOSFET device are performed by using the KEITHLEY model 4200-SCS semiconductor characterization system. Figure 3-2(c) shows the KEITHLEY model 4200-SCS consisting of four highly accurate source-monitor units (SMUs) with unique preamplifiers (PreAmp) that extend the current resolution of SMUs to 0.1fA, and the voltage resolution to 1μV. For a 4-terminal MOSFET device, these SMUs are separately connected to CASCADE MICROTECH with four standard 3-lug female triax connectors via standard 3-slot male triax. The probe heads are primarily used to steadily hold Tungsten needles, which are separately connected to the drain terminal, the source terminal, the gate electrode and the substrate of a MOSFET.

Figure 3-2 (a) 8-inch CASCADE MICROTECH wafer probe station. (b) KEITHLEY INSTRUMENTS 4200-SCS semiconductor characterization system. (c) SMUs with PreAmps.

3.2.2 STRESS METHODOLOGIES TO INDUCE A BREAKDOWN

Various stressing methodologies based on CVS have been developed to acquire more insightful data that can improve the understandings on the physical mechanisms governing the post-BD. Figure 3-3(a) shows a general figure of gate current evolution with stressing time obtained through K-cycle multi-stage CVS method. In this method, after TDDB occurs, a staircase pattern CVS is subjected to the test sample. The stress begins with a very low voltage. Subsequently, gate stress voltage is increased in incremental steps. For each stage, the stressing time is fixed around 300s. The purpose of

this stressing method is to investigate the presence of digital-BD at low gate voltages and the eventual transition to analog-BD, as shown in Fig. 3-3(b).

Figure 3-3 (a) Schematics of the K-cycle multi-stage CVS. (b) Example of K-cycle multi-stage CVS in a poly-Si/HfO₂/SiO₂ n-type device for accumulation mode stress condition. Notice the random gate current fluctuations in cycles 1 and 2 (digital-BD), but a monotonic increase in current during cycle 3 for $V_g > 2.8\text{V}$ corresponding to analog-BD evolution. The critical voltage V_{crit} governing the digital-BD $\rightarrow$ analog-BD transition is 2.9V [86].

The other stressing method used in this study is successive CVS (SCVS). This method is to identify the leakage level, so as to study device performance at different BD “hardness”, as shown in Fig. 3-4(a). In this test methodology, a current compliance limit (I_{gl}) is the controlling parameter. At the beginning, a selective $V_{gstress}$ is applied to the device. The stressing is automatically halted when gate current reaches a preset current compliance limit. Then the gate oxide stressing is continued by setting a higher current compliance limit without changing stress voltage. This procedure is repeated until a hard BD is observed or a recovery is initiated, as shown in Fig. 3-4(b).

(Continue on next page)

Figure 3-4 (a) Schematics of the SCVS. (b) Example of successive CVS method. For a NiSi/SiO₂ p-type MOSFET under SCVS with stressing voltage of 2.7V, I_{gl} was pre-set from 10 μ A, 50 μ A, 1mA, and then to 2mA, with I - V measurement (such as I_g - V_g , I_d - V_d and I_s - V_s) taken upon reaching each I_{gl} . After the I - V measurement, very low gate current I_g , similar to the pre-BD leakage was observed, indicating recovery occurred [7].

3.3 TEM LAMELLA PREPARATION METHOD

The details of the TEM lamella preparation method are thoroughly introduced. Precision TEM sample preparation method is used to prepare the lamella of thickness less than 100nm to study the microstructural defects responsible for the nanosized conductive filament. Focused ion beam (FIB) technique is able to meet this requirement as very small devices located at specific locations must be used in our study. The working mechanism of FIB is based on the sputtering of sample material by highly energized Ga⁺ ions (~ 30kV acceleration voltages) in the presence of electric and magnetic field. In order to increase the success rate of catching the nanoscale conductive filament, very narrow transistors consisting of widths of 150nm or less are used. Using this method, the probability

of capturing the defects in a MOSFET in the final TEM lamella of about 100nm of thickness is more than 90 percent.

To identify the location of the small size transistor under scanning electron microscope (SEM), M1 (metal 1) layer of the chip is removed by hand polishing until the contact layer (via) expose, as shown in Figs. 3-5(a) & (b). The area of interest (AOI) is then covered by a protecting material (Pt in this case). Holes are milled on each side of the lamella, as shown in Fig. 3-5(c). Then the lamella is lifted-out *in-situ* by a micromanipulator, and is glued on the pole of a Cu grid, as shown in Figs. 3-5(d)-(f). After pre-thinning (Fig. 3-5(g)), low-kv cleaning technique is used to reduce the damage/amorphization layer on each side of the lamella, which is ~ 20-30nm thick for Si using 30 kV Ga⁺ ion milling. The final TEM lamella is shown in Fig. 3-5(h).

Figure 3-5 SEM micrographs showing the FIB thinning process of a TEM lamella: (a) Overview of the narrow width transistor after removing the M1 layer, exposing the contact layer; (b) Location of the transistor has been identified; (c) Holes are milled on each side of the lamella. (d) Omi-probe and Pt needed used for the *in-situ* lift-off procedure. (e) Cu grid used to transfer the TEM lamella; (f) The lamella is approaching the Cu-grid before Pt-welding. (g) Further thinning of the TEM lamella; (h) Thickness of the TEM lamella after final milling with low-kV cleaning technique.

3.4 PHYSICAL CHARACTERIZATION USING TEM/EELS

3.4.1 TRANSMISSION ELECTRON MICROSCOPY (TEM)

TEM is a widely used technique for the nanoscale physical characterization of semiconductor devices and thin films. TEMs are best known for imaging the morphology of a specimen, but a whole range of additional techniques is available in TEMs to extract chemical, electrical and structural information. By using the parallel electron beam of the TEM for example, local diffraction patterns can be measured, which can provide accurate measurements of the crystal system and parameters. The electron beam could also be converged for diffraction measurements at even smaller areas of a few nanometers in diameter. The thus obtained converged beam electron diffraction (CBED) pattern contains structural information in all three dimensions, as well as a mean to accurately measure the specimen thickness.

A function often found on modern TEM, is the STEM (scanning TEM) option. In this mode, the electron beam is further converged to a small probe with a diameter that can be varied from a few nanometers (for high-current measurements) down to the 0.1nm (low-current) regime.

STEM and TEM are usually performed with the same instrument; in fact, when a specimen can be imaged with TEM, it can also be imaged with STEM, likewise with atomic resolution. A comparison of STEM and TEM is given in Figs. 3-6(a) and (c). In general, it can be said that TEM micrographs reveal rich details on the morphology and crystal structure; STEM micrographs often do not resolve polycrystalline structures. On the other hand, high angle annular dark field (HAADF) STEM micrographs are much more directly interpretable. The contrast reflects the (average local) atomic number, which is also referred as Z-contrast. Therefore, if an area appears bright in a HAADF

STEM micrograph, it is locally contains heavier elements. Figure 3-6(c) for example, immediately shows the presence of the hafnium-containing high- κ layer, which is much less obvious in the TEM micrograph. Another advantage of STEM imaging is the lack of ‘TEM delocalization effects’ at interfaces [87, 88]. Unless most spherical lens aberrations are corrected — which is only the case in high-end, corrected TEMs — the exact location of interfaces will often not be clear in TEM micrographs. STEM micrographs give more accurate information on the location and quality of an interface; they show directly where atom columns are located, in contrast to conventional TEM micrographs.

3.4.2 ELECTRON ENERGY LOSS SPECTROSCOPY (EELS)

Both STEM and TEM can be used for chemical mapping using EELS, as shown in Figs. 3-6(b) and (d). In TEM mode, such an energy-filtered image is recorded for each element separately; for STEM, the whole EELS spectrum is recorded in parallel, but acquired with only one image pixel at a time. Therefore, energy-filtered TEM maps are more efficient for imaging a large area, where many image pixels are needed. STEM on the other hand allows for a much more detailed spectral analysis of small areas or interfaces. Simultaneously with the acquisition of an HAADF STEM image, and EELS spectra can be obtained. The combination of these techniques can give a comprehensive chemical analysis of a critical part of a device, with nanometer resolution. Due to the lateral nature of semiconductor devices, there is usually only one critical dimension for which nanometer-scale analysis is needed. An obvious example on which we will focus in this work, is the chemical analysis of the various layers in gate stacks, for which line scans (or even point analysis) are usually sufficiently conclusive.

When the small STEM probe travels through the specimen at a specific point, some of these fast electrons will interact with the specimen material. One interaction that will take place is the excitation of core-electrons. When this happens, some of the energy from the fast electron is transferred to the specimen electrons in the *s*, *p*, *d*, etc. core shells, which in turn are excited into empty energy states in the conduction band. Nearly immediately, a ‘free’ or conduction electron will fill the empty core state, relieving the energy difference by emitting an X-ray. The fast electron has lost some of its initial energy, and this energy loss is detected with EELS. The peaks that are observed in EELS spectra are typical for each chemical element and core level, and can therefore be used to chemically analyze the small area where the STEM probe is located. EELS has a small energy dispersion, but higher spectral resolution. As a result, EELS can be used to study a few selected elements in much more detail. Not only the presence of these elements can be revealed, but also their bonding nature, since the shape of the EELS peak will be a reflection of the local density of unoccupied electron states. EELS can therefore in some cases be used to measure local changes in bonding type, shifts in the conduction band onset, and changes in valence states. Localized measurements of semiconductor band gap energies are also possible, but with a degraded spatial resolution of $\sim 10\text{nm}$ instead of less than 1nm [89].

Figure 3-6 (a) Conventional TEM micrograph of a MOSFET with near the bottom in the silicon substrate the source and drain, and vertically in the center the high- κ containing gate stack. (b) Energy-filtered TEM micrograph, with some of the chemical elements colour-coded. (c) STEM HAADF micrograph of the same device, with the 3nm thick high- κ layer showing bright. (d) Energy-filtered map similar to (b), but now showing the oxygen distribution in more detail. Spacers and gate oxide become clear, as well as a ~ 2 nm thick oxygen-containing layer between the gate metal and polycrystalline silicon [courtesy of M. Bosman].

3.4.3 IN-SITU TEM

To understand the switching mechanism of MIS structures, *in-situ* TEM study was performed. The *in-situ* TEM analysis was carried out with a Nanofactory single tilt

STM-TEM holder, as shown in Fig. 3-7. The key benefits of *in-situ* TEM probing techniques lie in the abilities to: (1) locate and align a probe to nanoscale objects with high precision; (2) characterize both object and probe by high resolution imaging using TEM; (3) carry out electrical and mechanical probing in situ; (4) study dynamical processes.

Figure 3-7 A picture of Nanofactory single tilt STM-TEM holder.

3.5 SUMMARY

Various electrical device characterization and stressing methodologies have been discussed in this chapter. Precision TEM sample preparation method using *in-situ* lift-up FIB technique was described. To extract the physical information of defects in the gate dielectric layer, STEM and EELS techniques were used. *In-situ* TEM set-up was introduced.

CHAPTER 4 ROLE OF OXYGEN VACANCIES IN ADVANCED HfO_2 - BASED GATE STACKS BREAKDOWN

4.1 INTRODUCTION

Dielectric BD is a process that is observable in natural phenomena such as lightning and thunderstorms, in man-made electrical devices such as smartphones, and in failed electronic components at die level. High resolution TEM analysis results have shown that oxygen vacancies are the physical defects that result in the formation of the BD path in gate oxide [18, 34]. This reveals the chemical nature of the BD path at the atomic scale. However, the band structure of an oxygen deficient path in HfO_2 -based dielectric and its impact on digital-BD remain unclear. This chapter describes the band structure and DOS of multiple oxygen vacancy traps in the percolated dielectric of the digital-BD fluctuations in HfO_2 -based logic transistors through DFT calculations.

4.2 TRIGGERING VOLTAGE OF DIGITAL BREAKDOWN

4.2.1 IMPORTANCE OF DIGITAL BREAKDOWN

The gate leakage current of a CMOS circuit increases significantly as the technology is scaled down, creating a reliability issue in high performance systems. The measurement of digital-BD fluctuations is important for characterizing traps in gate dielectrics. Digital-like fluctuations in I_g or random telegraph noise is directly correlated to stress-induced traps/defects generated in the dielectrics [90]. Moreover, digital-BD

fluctuation is believed to affect the performance stability and reliability of devices, thus presenting a challenge for the scaling of the high- κ metal gate stacks in the future [91]. In addition, digital fluctuations may cause erratic behavior in static random access memory (SRAM) [92]. As a result, digital-BD has become increasingly important in studying the defects and degradation of ultra-thin dielectrics.

Digital-BD measurements have typically been performed within a narrow range of a relatively high V_g , where the signal of digital fluctuations can be observed clearly [93, 94]. For example, Lee *et al.* [93] reported digital fluctuations under gate voltage of $V_g = 1.9 - 2.3\text{V}$, on MOSFET gate oxide with 3nm HfO₂ and 1nm SiO₂. However, the starting voltage or triggering where digital-BD fluctuations begin to occur is yet to be studied in detail. In this study, we investigate the triggering voltage V_{TRIG} in an ultra-thin HfO₂-based dielectric with zero interfacial layer (SiO₂), and the DOS changes with multiple oxygen vacancy traps through first-principles DFT calculation.

4.2.2 ELECTRICAL CHARACTERIZATION OF TRIGGERING VOLTAGE OF DIGITAL BREAKDOWN

The samples tested consisted of a TiN-gated HfO₂ (thickness $\sim 12\text{\AA}$) zero interfacial layer n-type MOS ($W \times L = 0.09 \times 0.065\mu\text{m}^2$) with an equivalent oxide thickness of $4.8\text{\AA}$. The device was subjected to a single cycle multi-stage CVS test at room temperature [86]. In the test, TDDB of the n-type MOS was initiated with a gate stress voltage ($V_{gstress}$) of 3.9V and a gate compliance current I_{gl} of 1 μA . This accelerated test of gate oxide is needed to ensure that the TDDB of the gate oxide can be performed within a reasonable window of time. In the post-BD regime, the single cycle multi-stage CVS began with an initial voltage of 0V. Subsequently, $V_{gstress}$ was increased in

increments of 0.2V. For each stage, the stressing time was fixed at 300s. An example of a complete post-BD I_g evolution with stressing time is shown in Fig. 4-1(a). Figures 4-1(b) and (c) show the I_g evolution at two typical $V_{gstress}$ ranges of 0.2-0.6V and 1.6-2.0V. It is clear that digital fluctuations are triggered at a stress voltage of $V_{TRIG} \sim 1.6\text{V}$. These results have been confirmed by Liu *et al.* [90].

4.3 SELECTION OF SIMULATION METHOD

4.3.1 SIMULATION OF DEFECTS

In Chapter 2, periodic boundary conditions were applied in the first-principles based calculation of the energy of a primitive cell. Although solids with a defect do not exhibit three-dimensional periodicity, a supercell, which is a repeating unit cell of the crystal that contains several primitive cells, can be constructed for a defect, a surface in a bulk solid, or a molecule, as shown in Fig. 4-2. For a surface, the slab must be thick enough to prevent two surfaces within the same supercell from interacting through the bulk regions. For a molecule, the vacuum regions must be wide enough to ensure that the surfaces of adjacent crystal slabs do not interact across the vacuum regions. For the defect calculations, the supercell must be large enough to ensure that the interaction with other defects in neighboring supercells is small. However, the first-principles calculation for a large supercell becomes prohibitively expensive in terms of the computation time required. As the volume and number of atoms increase, the increase in computation time is of the order of n^6 or higher. Thus, the main challenge of defect simulation is finding a compromising between computation time and result accuracy.

(Continue on next page)

Figure 4-1 (a) Evolution of post-TDDB I_g for an n-type MOS ($\text{EOT} = 4.8\text{\AA}$ and $W \times L = 0.09 \times 0.065\text{\AA}$) stressed using a single cycle multi-stage CVS at room temperature [86]. TDDB failure was initiated with $V_{g\text{stress}} = 3.9\text{V}$ and $I_{gl} = 1\text{\AA}$. In the post-BD regime, the initial stressing voltage was 0V. Subsequently, the stressing voltage was increased in increments of 0.2V. For every stage, the stressing time was fixed at 300s. (b) Noisy I_g fluctuations without any digital-BD signals were observed with $V_{g\text{stress}}$ ranging from 0.2V to 0.6V. (c) Digital-BD fluctuations clearly triggered at a gate voltage of $V_{TRIG} \sim 1.6\text{V}$.

Figure 4-2 Schematic illustration of a supercell (a) a vacancy in a bulk solid (b) a surface of a bulk solid (c) a molecule. The boundaries of the supercell are shown in dashed lines. The supercell is the area enclosed by the dashed lines.

4.3.2 ATOMISTIC SIMULATION FLOW AND SOFTWARE PACKAGES

The general flow chart for the first-principles calculation is shown in Fig. 4-3. The program begins by finding the appropriate atomic structure. The Inorganic Crystal Structure Database (ICSD) provides a sufficient number of structures (a 3592 structure subset of the 140,116 inorganic structures in release 2011-1) [95]. By using various first-principles calculation packages, the optimized primitive cell can be constructed. The supercell is then set up accordingly. During optimization of the supercell, a SCF result is obtained when the energy difference between the current run and the previous run meets the convergence criteria. The simulation work was performed in collaboration with D. Migas of the Belarusian State University of Informatics and Radioelectronics, who provided the supercomputer computation required to perform a calculation of large scale.

Figure 4-3 General flow chart for the first-principles calculation.

There are many advanced DFT algorithms. The Vienna Ab-initio Simulation Package (VASP) [84, 96, 97] is a powerful software package based on the first-principles Kohn-Sham DFT, and employs a plane-wave basis set and the pseudopotential approximation. The key features of VASP are as follows:

- Perform first-principles quantum-mechanical molecular dynamics calculations, which are based on the spin-polarized DFT.
- Support the ultrasoft Vanderbilt pseudopotentials (US-PP) and a plane wave basis set, and provides potential files for all the elements.
- Provide efficient matrix diagonalization schemes and employs an efficient Pulay/Broyden charge density mixing scheme.
- Force and the stress tensor can be calculated and used for atomic relaxation calculations.

The Cambridge sequential total energy package (CASTEP) [98, 99] is another state-of-the-art quantum mechanics based program designed specifically for solid-state materials science. Similar to VASP, CASTEP also employs the DFT plane-wave pseudopotential method. The key features of CASTEP software are as follows:

- Provide various advanced exchange-correlation energy functionals (e.g. screened exchange and the weighted density approximation), suitable for transition oxide calculations.
- Provide a user-friendly graphical interface that makes it easy to build the modular structure.
- A user can interact with CASTEP through a Perl scripting environment.
- Provide parallelized computing as well as high efficiency.

In this study, we used both software packages, VASP and CASTEP.

4.4 FIRST-PRINCIPLES CALCULATION ON MULTIPLE OXYGEN VACANCIES

The BD path in both the HfO_2 [37] and SiO_2 [19] dielectric is mainly comprised of oxygen vacancies; this was verified through TEM and EELS studies. First-principles calculation can be useful for understanding the role of oxygen vacancies and their effect on the bandgap of the insulating dielectric layer for HfO_2 -based gate stacks.

4.4.1 SIMULATION PARAMETERS

Bulk HfO_2 has a monoclinic symmetry ($P2_1/c$) at low temperatures, and it transforms to tetragonal phase ($P4_2/nmc$) at 2000K and to the cubic phase ($Fm3m$) above 2870K [100]. Thus we used HfO_2 with a monoclinic crystal structure in this study. For monoclinic phase HfO_2 , the most stable phase was found to have the following lattice parameters: $a = 5.1156\text{\AA}$, $b = 5.1722\text{\AA}$, $c = 5.2948\text{\AA}$ and $\beta = 99.18^\circ$ [97]. The corresponding unit cell consists of 12 atoms. Here we used a supercell that contains 96 atoms, which was constructed by enlarging the dimensions of the original unit cell twice along a , b and c . Thus, the supercell we chose exceeds the minimum supercell size of 48 atom cells as described in other literature reviews [101, 102], which ensure that the results are accurate.

Structural optimization and calculations of DOS for HfO_2 , with and without defects, were performed by implementing the projector-augmented wave method in VASP code [84, 103, 104]. In this study, we employed the exchange and correlation potentials using GGA of PBE [81]. Total energy minimization was performed via an

optimization of the lattice parameters and a relaxation of the atomic positions in a conjugate gradient routine by calculating the Hellmann–Feynman forces and the stress tensor. The convergence in the total energy was better than 5meV/atom for the energy cutoff of 430eV and the $4 \times 4 \times 4$ grid of Monkhorst–Pack points. This dense $\mathbf{k}$ -point mesh was used for the final iterations while initial iterations were carried out on the $1 \times 1 \times 1$, $2 \times 2 \times 2$ and $3 \times 3 \times 3$ meshes. The total DOS was calculated by the tetrahedron method, with Blöchl correction on the $4 \times 4 \times 4$ mesh. The simulation flow is shown in Fig. 4-4.

Figure 4-4 The flow chart for the multiple oxygen vancancies first-principles simulation.

4.4.2 DOS OF HfO_{2-x} WITH MULTIPLE NEUTRAL OXYGEN VACANCIES

We analyzed several HfO_{2-x} compounds for x ranging from 0 to 0.1. To change the stoichiometry, some oxygen atoms were removed from the enlarged cell. Note that the oxygen vacancies are neutral. Thus, the $\text{HfO}_{1.969}$, $\text{HfO}_{1.938}$ and $\text{HfO}_{1.907}$ stoichiometries were obtained by removing one, two and three oxygen atoms from the cell, respectively. We checked several variants, where oxygen vacancies are close to each other (oxygen divacancy) (Fig. 4-5(a)) or apart from each other (Fig. 4-5(b)), in $\text{HfO}_{1.938}$ and $\text{HfO}_{1.907}$. No significant changes were observed in the position of the top of the valence band (E_v) and the bottom of the conduction band (E_c). Changes were observed only for defect levels in the gap, as shown in Fig. 4-6.

Figure 4-5 Schematic image of the $\text{HfO}_{1.938}$ used in the calculation. The left column shows a side view and the right column shows a top view, where (a) shows oxygen vacancies of two traps that are next to each other (b) shows oxygen vacancies of two traps that are not next to each other. The black dotted outline square represents the $2 \times 2 \times 2$ supercell volume. Hf and O atoms are represented as blue and red, respectively. The arrows mark the V_o centers.

Figure 4-6 Total DOS (states/eV/cell) for HfO_{2-x} near the gap region for x ranging from 0 to 0.1. Different stoichiometries are indicated. The vertical dashed lines show the top of the valence band (E_v) and the bottom of the conduction band (E_c). The zero of the energy scale corresponds to the absence of allowed electron states. The left panel shows threefold coordinated oxygen vacancies, and the right panel shows fourfold coordinated oxygen vacancies.

It can be seen that the formation of oxygen vacancies leads to the appearance of narrow peaks in the gap region, which may be associated with the defect energy levels.

The location of the defect level has been studied both experimentally [105, 106] and

theoretically [35, 107]. However, in the latter case only one stoichiometry (one oxygen vacancy in the unit cell) was analyzed. It is evident from the results here that the formation of two or more oxygen vacancies creates multiple defect levels in the gap region.

Figure 4-7 shows the projection of all calculated positions of the defect levels onto the gap for $\text{HfO}_{1.907}$. Although no smearing technique was applied for the DOS calculations, it is evident that a defect sub-band (E_d) of about 1.5eV has evolved from the defect levels. In these calculations, we did not use the hybrid functional, and consequently, the bandgap value is underestimated and the positions of the defect levels are shifted towards the valence band [107]. However, this only affects the quantitative interpretation of the results. Electrons need to overcome the barrier height between E_v and the bottom of E_d to contribute to the post-BD gate leakage current fluctuations between various discrete current levels.

Figure 4-7 Projection of defect levels onto the gap for $\text{HfO}_{1.907}$ for all types of oxygen vacancy combinations. The defect subband (E_d) is also marked.

4.4.3 DOS OF HfO_{2-x} WITH MULTIPLE CHARGED OXYGEN VACANCIES

A charged defective $\text{HfO}_{1.969}$ system was also simulated (Fig. 4-8). A positive charge system, especially when two electrons are absent, gives the most shallow defect levels. The value of this shallow defect level is around 0.5V, which is in close agreement with the experimental data [105]. The positive oxygen vacancies have been suggested likely candidates for intrinsic shallow electron traps in the HfO_2 -based gate stack devices [108, 109].

A similar shallow defect level has been identified in an $\text{HfO}_{1.938}$ system (Fig. 4-9). Again, the positive charge system is responsible for the shallow defect level. Interestingly, the value of the shallow defect level located 0.5V below the bottom of the conduction band E_c is the same as that of the negative charged $\text{HfO}_{1.969}$ system. Thus, the increase in the number of oxygen vacancies does not affect the location of the shallow defect levels, but instead increases of the number of defect levels in the middle of the bandgap region.

Note that for all the simulation, there was no much change on the lattice constant.

Figure 4-8 DOS (states/eV/cell) for a charged $\text{HfO}_{1.969}$ system, showing that the defect level of a positively charged oxygen vacancy is shallow.

Figure 4-9 DOS (states/eV/cell) for a charged $\text{HfO}_{1.938}$ system. Again, positively charged oxygen vacancy gives the shallowest defect level.

4.5 SUMMARY

We studied the influence of multiple oxygen vacancy traps in the percolated dielectric on the post-BD digital fluctuations in HfO₂-based MOS transistors. The electrical characterization results indicate that these digital fluctuations are only triggered beyond a certain gate stress voltage. First-principles calculations suggest that the oxygen vacancies are responsible for the formation of a sub-band in the forbidden band gap region, which affects the triggering voltage for the digital-BD fluctuations and leads to shrinkage of the HfO₂ bandgap.

CHAPTER 5 ELECTRODE MATERIAL DEPENDENT BREAKDOWN AND RECOVERY IN HfO_2 -BASED GATE STACKS

5.1 INTRODUCTION

In recent decades, several studies have tried to explain BD path formation and degradation [110-113] in metal gate HfO_2 -based gate stacks in order to predict the occurrence of BD accurately in a device under operating conditions. Various metal gate materials have been tested. The gate metal is chosen primarily for its work function. The work function of the gate electrode determines the gate threshold voltage for inversion. NiSi [114], TiN [16], and TaN [115] emerged as strong candidates for use as electrode materials in the proposed metal gates. It is generally accepted that defects generated during pre- and post-BD stress are responsible for the various leakage current profiles observed in the accelerated tests. In addition to oxygen vacancies, metal migration from the gate electrode is another important physical cause of ultra-fast BD, causing shrinkage of the post-BD reliability margin [49, 116].

In a recent study, Liu *et al.* [7] have reported recovery in the post-BD regime on a NiSi/ HfO_2 gate stack under favorable conditions. This phenomenon is considered related to the ON/OFF state of the nanosized BD path, which depends on defect transformations. The discovery of BD reversal is important as now the post-BD reliability margin can be enlarged. This chapter discusses the effect of using different gate electrode materials on

reversible BD and thereby explains the physical origin of the insulator to conductor, and conductor to insulator transitions.

5.2 CHARACTERIZATION OF POST-BREAKDOWN RECOVERY

The devices tested included NiSi, TiN, and TaN-gated n-type MOS transistors containing ultra-thin HfO_2 dielectric, where the thickness of HfO_2 ranged from 1.2 to 2.5nm. In the test, a selected gate stress voltage was applied to the transistors until TDDB occurred within the required time period. The compliance current was capped at 1mA. Recovery was observed during the $I_g - V_g$ sweep in the post-BD regime. Figure 5-1 shows the $I_g - V_g$ graphs for the NiSi/ HfO_2 , TiN/ HfO_2 , and TaN/ HfO_2 gate stacks. In the NiSi gate stack test, a significant low resistance state to high resistance state transition corresponding to a change of two to five orders of magnitude was observed as shown in Fig. 5-1(a). Recovery in the TiN gate stack for I_g was less than one order of magnitude (Fig. 5-1(b)). No recovery was observed in TaN gate stacks as shown in Fig. 5-1(c). These results were consistent across over 30 devices that were tested for each gate material. We selected three sets of representative data points labeled as #1, #2, and #3 in Fig. 5-1. The difference in observed recovery trends is attributed to the difference in gate electrode materials used, which will be explained in the following sections.

Figure 5-1 Post-BD $I_g - V_g$ graphs for (a) NiSi- HfO_2 gate stack (b) TiN- HfO_2 gate stack (c) TaN- HfO_2 gate stack. The arrows indicate the start of the recovery stage.

It is important to note that the recovery from BD here is different to digital-BD [27, 86]. Under digital-BD, I_g fluctuates randomly between certain fixed current levels usually of the same order of magnitude. In contrast, the recovery behavior shows that I_g decreased almost instantaneously by one to two orders of magnitude and then remains at a leakage level comparable to the pre-BD leakage. Digital-BD also occurs beyond the triggering voltage and evolves to analog-BD if a critical voltage is exceeded [27]. In contrast, BD recovery is not limited by V_g or I_g .

5.3 PHYSICAL ANALYSIS OF POST-BREAKDOWN RECOVERY

To understand the physical nature of recovery after BD, TEM and EELS techniques were used. The physical analysis method used was *ex-situ* TEM, which is a post-analysis technique for a device under standard freezing conditions. There is no electrical probe in the *ex-situ* TEM machine. Thus, once we had stressed the device electrically using the probe-station, we could not change the device conditions. The *ex-situ* TEM technique is widely used in the study of semiconductors, materials, and in nanotechnology and provides important information about the devices studied. *In-situ* TEM will be discussed in more detail in later chapters. This section discussed device after recovery by *ex-situ* TEM.

Figure 5-2 (a) and (b) show the cross-sectional STEM HAADF micrograph and EELS result for the NiSi gated HfO_2 -based stack. DBIE was observed, as shown in the inset of Fig. 5-2 (a). As was first mentioned in Chapter 2, DBIE is the process where Si atoms from the channel protrude into the oxide layer forming hillocks as a result of thermomigration. This leads to effective oxide thinning, which is a nano-marker (for localized TEM analysis) of the BD location. More details involved in identifying the DBIE and BD location can be found in Refs. [18, 117]. Here, we used EELS analysis to understand the chemical change in the BD path through the dielectrics, as shown in Fig. 5-2 (b). As illustrated in Fig. 5-2 (a), Ni and O EELS line profiles were acquired at three different locations on the sample: the non-BD spot (line 1), the DBIE center (line 2), and the Ni spike (line 3). The DBIE center shows a lower oxygen K-edge count in the BD path compared to a non-BD spot suggesting that the local chemical structure of the percolation path is an oxygen-deficient HfO_x , where $x < 2$. Moreover, comparing with a

non-BD area, the Ni atoms originating from the gate electrode spiked into the dielectrics by an ionic and hole migration mechanism [118], resulting in a metal filament spike of diameter $\sim 2\text{nm}$. The Ni migrates into the Si-substrate along the Si $\langle 111 \rangle$ direction, where surface tension is the lowest [119]. Note that all the EELS spectrums results are repeatable, and therefore statistically meaningful.

Figure 5-2 (a) Cross-sectional STEM HAADF micrograph of a NiSi-gated HfO_2 -based dielectric stack after BD showing a 2nm Ni filament that pierced through the HfO_2 -based dielectric into the Si channel (b) EELS results of Ni spiking from gate to substrate in the gate stack. The Ni composition profile is shifted to the right with respect to the reference fresh device profile indicating Ni punchthrough. The percolated region is O-deficient [71].

Similar oxygen deficiency and metal filament defects were found in the TiN/HfO_2 n-type MOS gate stack. Figures 5-3 (a) and (b) show the TEM/STEM micrographs and EELS results. The STEM HAADF micrograph in Fig. 5-3 (a) shows that the size of the Ti filament was $\sim 5\text{nm}$, which is more than the Ni filament. EELS signals were collected at four different locations: broken-down oxide/gate, and reference non-BD oxide/gate. In the broken-down HfO_2 oxide, the Ti L-edge signal at 456eV was observed, while no N K-edge signal at 401eV could be observed. This indicates that only Ti metal atoms from the gate electrode migrated downwards. Interestingly, in contrast to the non-BD location EELS signal, the oxygen atoms in the broken-down oxide move up to gate electrode and are stored there. This can be explained by the fact that, negatively charged oxygen ions (O^{2-}) migrated into the TiN gate when a positive voltage was applied to the gate, leaving the oxide BD region O-deficient.

(Continue on next page)

Figure 5-3 (a) Cross-sectional STEM HAADF micrograph of a TiN-gated HfO_2 -based dielectric. The broken-down oxide/gate, and reference non-BD oxide/gate are indicated by circles. The inset shows the TEM micrograph, where DBIE is marked as the nano-marker of the BD location (b) EELS results of N K-edge (401eV), Ti L-edge (456eV), and O K-edge (532eV). In contrast to the non-BD spot EELS signal, the oxygen atoms in the broken-down oxide move up to gate electrode and are stored there, while the Ti atoms from the gate electrode migrate down towards the dielectric.

Figure 5-4 (a) reproduces the STEM and EELS results from Li *et al.* [49] using a TaN-gated HfO_2 gate stack. The large amount of Ta atoms diffused from the gate electrode punched through the dielectric layer with the diameter more than 10nm and formed a bowl-shape defect in the Si-substrate. Note that the diameter here is much larger than both the Ni spike ($\sim 2\text{nm}$) and the Ti ($\sim 5\text{nm}$) filament. Figure 5-4 (b) shows the EELS oxygen K-edge spectra at the BD spot, BD edge, and non-BD spot shown in Fig. 5-4 (a). The oxygen count drops significantly at the BD spot. Some oxygen atoms remain at the edge of the BD spot. Therefore, the defects shown as oxygen vacancies spread out radially from the center of the BD path, similar to poly-Si/SiON BD [120]. Table 5-1 lists the recoverability of several electrode materials.

Figure 5-4 (a) HAADF micrograph of a TaN-gated HfO_2 MOS with a Ta metal filament found in the dielectric after BD [49]. The BD spot, BD edge, and the non-BD spot are marked with dotted circles. The inset shows the overall view. (b) EELS oxygen K-edge spectra at the BD spot, BD edge and non-BD spot. The oxygen signal is close to zero at the center of the BD spot, but some oxygen atoms remain the edge of the BD spot. Thus, the oxygen atom distribution in the BD path increases radially outwards [18].

Table 5-1 Degree of recoverability of various electrode materials: NiSi, TiN, and TaN. Both NiSi and Ti gated HfO_2 systems show a tendency to recover, but the TaN system does not. Metal atom migration and filamentation was also identified in NiSi and TaN gated stacks using TEM and EELS.

Gate electrode material	Recoverability	Diameter of the metal filament
NiSi	Large recovery	~ 2nm
TiN	Moderate recovery	~ 5nm
TaN	No recovery	~ 10nm

5.4 FIRST-PRINCIPLES CALCULATION OF ROLE OF THE METAL ATOM

5.4.1 DOS OF DEFECTIVE HfO_2 SYSTEM WITH METAL ATOM MIGRATION

To explain the metal gate dependent dielectric BD and recovery, we analyzed the role of the metal atom from the gate electrode from the perspective of an atomistic simulation, using a first-principles based approach. A neutral V_o is created by removing an oxygen atom from a HfO_2 supercell. Metal migration is represented by placing a metal atom near the V_o site, which is the favored energy minimum location. Figure 5-5 shows the simulated structure.

Figure 5-5 Schematic of a typical defective structure used for the calculations. The black dotted outline cube represents the supercell lattice. Hf and O atoms are represented as blue and red circles, respectively. The dotted outline white circle indicates the V_o center. Metal migration is represented by placing the metal atom near a V_o site, which is the favored energy minimum location.

The calculated DOS for the perfect HfO_2 and for HfO_2 with metal filament induced by Ni, Ti and Ta migration are shown in Figs. 5-6 (a)-(d). Three distinct bands are seen for perfect HfO_2 , corresponding to $2s$ states of oxygen (-20eV to -15eV), the strong-bonding states of oxygen $2p$ orbitals (-5eV to 0eV), and the conduction band of hafnium $5d$ orbitals (3eV to 5eV). The calculated bandgap for perfect HfO_2 is 3.23eV , is close to the previously reported value of 3.25eV [121]. This is substantially smaller than the real bandgap of about 6eV due to the approximation used in the Kohn–Sham equations [122]. V_o induced gap states contributed by the Hf $5d$ orbitals [123] are shown as red dashed lines in Figs. 5-6 (b)-(d). Metal atoms that have migrated induce additional defect states in the gap region, which are shown as blue dashed lines in Figs. 5-6 (b)-(d). These gap states reduce the bandgap of the dielectrics significantly. The Ni $5d$ states form a narrow sub-band close to the top of the valence band, reducing the bandgap to 1.587eV .

The Ta $5d$ states are spread out, causing the bandgap to collapse to zero. The Ti $5d$ states are located between the Ta and Ni states, causing bandgap shrinkage to 0.296eV. Although bandgap reduction in post-BD TaN-gated stacks has been reported previously [124], this work compares the bandgap shrinkage for different gate electrode materials. These simulation results show that recovery is feasible whenever the bandgap of the filamented HfO_2 dielectric is none zero.

Figure 5-6 DOS for (a) perfect monoclinic HfO_2 ; and defective HfO_x ($x < 2$) with (b) Ni, (c) Ti, and (d) Ta atom migration. Solid lines represent the total DOS of the systems and the dotted and dashed lines represent the partial DOS contributed by the $5d$ orbitals of Hf and the migrated metal atoms, respectively. Ni migration results in the largest bandgap margin, while Ta migration shows a 0eV bandgap.

5.4.2 DEFECT FORMATION ENERGY CALCULATION

We also studied the defect formation energy (E_f) required by the HfO₂ dielectrics to remove the metal migration defect. Lower E_f would imply easier and better reversibility of BD. The defect formation energy using the first-principle calculation with the supercell approach is given by [125]:

$$E_f = E_{defect} - E_{perfect} + \frac{E_{O_2}}{2} - E_{metal} \quad (5.1),$$

where E_{defect} , $E_{perfect}$, E_{O_2} , and E_{metal} represent the energy of the defective system, defect-free system, molecular O₂, and a single metal atom, respectively. Table 5-2 summarizes the calculated defect formation energy and bandgap values for the various metal gate HfO₂ dielectrics. The Ta metal filament requires the highest E_f and causes the bandgap to collapse to 0eV, indicating that the BD path inside HfO₂ is highly conductive and the filamentation is irreversible. However, the Ni and Ti metal filaments in HfO₂ show a reasonable bandgap margin and relatively low defect formation energy, implying that the metal filament related BD failure can be recovered. The Ni migration induced defect has the lowest E_f , very close to the E_f of the V_o defect. Thus, Ni-based gate stacks show the best BD reversibility.

Table 5-2 Bandgap and defect formation energy calculated by CASTEP using the GGA exchange potential. The Ta atom migration defect causes the bandgap to collapse to 0eV, indicating that the conductive path inside HfO_2 is fully metallic and is difficult to be turned off. However, the Ni and Ti migrations still show non-zero bandgap values, implying the possibility of recoverable BD.

Gate electrode	Band gap (eV)	Defect formation energy (eV)
HfO_x ($1V_o$)	--	6.22 / 6.40 [35]
$\text{HfO}_x + \text{Ni}$	1.587	6.92
$\text{HfO}_x + \text{Ti}$	0.296	7.53
$\text{HfO}_x + \text{Ta}$	0	9.92

5.5 UNCORRELATED MULTIPLE METAL FILAMENTS

5.5.1 METAL FILAMENTS LOCATIONS ALONG THE CHANNEL

We discussed a single metallic conductive filament in the previous section. Previous studies have not explored the possibility and implications of multiple conductive filamentation events. Consequently, it is still not clear whether the BD process involves the generation of spatially and temporally correlated or uncorrelated defects that are produced by a positive feedback of defect formation and localized current stress. This section describes the in-depth electrical characterization performed, which shows that the conductive filaments are spatially and temporally uncorrelated during formation.

The devices tested were conventional NiSi-gate HfO_2 n-type MOS transistors since they have the best reversal BD behavior. We chose a small area device with long

gate length of $L = 350\text{nm}$ to make it easier to observe multiple metal and the gate width was $W = 150\text{nm}$.

Figure 5-7 (a) shows the BD and recovery I - V graphs recorded using a bipolar switching mode. A positive bias sweep from 0V to 5V was applied on the gate electrode, while the compliance current was capped to 1mA. Both the source and drain terminals were grounded. BD is defined as the occurrence of an instantaneous increase in the current level two or more times during voltage ramping. The first BD and formation of a metal filament occurred at 4.3V, as shown in Fig. 5-7 (b). This was followed by another abrupt increase in the current at 4.8V, as the current reached the compliance value of $I_{gl} = 1\text{mA}$. The relative BD location ($S = \Delta I_d / (\Delta I_d + \Delta I_s)$) along the channel from the source ($S = 0$) to drain ($S = 1$) end was measured in accumulation/inversion mode using the technique proposed by Degraeve *et al.*, where I_d is the drain and I_s is the source terminal currents at $V_d = V_s = V_{sub} = 0\text{V}$ [126]. The structure of the MOS device is advantageous for identifying the BD path (along the length of the channel) precisely. By this method, we found that the first BD path formed at $S_1 = 0.06$, which was near the source. After the second BD, we found that $\Delta I_d \gg \Delta I_s$. S value changed to 0.96, indicating that the location of the second metal filament formed was near the drain. This was verified through the TEM micrograph, which showed physical evidence of metal filament formation at both edges (source and drain) of the transistor. During the negative voltage sweep from 0 V to -2V , the gate leakage current first decreased at -1.3V , and decreased again sharply at -1.7V . The range of voltages for bipolar switching here was -2V to $+5\text{V}$ with ON/OFF ratio of 1000.

Figure 5-7 Breakdown and recovery in a bipolar NiSi/HfO₂ MOS device (a) Electrical data showing the bipolar I - V switching trends when the compliance current was capped to 1mA. Two discrete increases in the current (BD) that accompany the formation of two individual conductive paths can be identified. The first BD occurred at +4.2 V with $S = 0.06$, which indicates the first conductive path was near the source. The second BD occurred at +4.8 V. In this case, $\Delta I_d \gg \Delta I_s$, while S was 0.96, implying that the conductive path location was near the drain. Two discrete recoveries were observed during the negative voltage sweep. The current first decreased sharply from 80 μA to 1 μA at -1.3 V, followed by a second decrease from about 2 μA to 80 nA at -1.7 V. Both the recovery events represent a second order of magnitude change in the gate current. (b) Details of the first BD.

5.5.2 TEM AND STEM ANALYSIS

Our previous work showed that both oxygen vacancies and Ni metal filaments are physical defects corresponding to the formation of the conductive path during the BD process [71]. Figure 5-8 shows the post-recovery HAADF STEM micrograph of the device used in the experiment shown in Fig. 5-7. Two uncorrelated BD paths at the source and drain ends are clearly visible, marked as 'CF-A' and 'CF-B' where CF stands for 'conductive filament'. Here, CF-A corresponds to the first BD path near source, while CF-B corresponds to the second BD path near drain. The bright region in the Si-substrate indicates the presence of heavy atoms that were confirmed to be of Ni by EELS (as shown in Fig. 5-9). Our previous work has shown that the vertical migration of metal atoms from the transistor gate electrode and lateral diffusion of Ni-based silicide compounds from the source and drain into the broken-down HfO_2 gate dielectric cause the physical defects that are responsible for the highly conductive BD path called DBIM [37, 43, 49]. The key driving forces behind DBIM are the Ni concentration gradient between the Ni silicide contacts and the channel near the BD spot, and the temperature gradient induced by the BD path. By monitoring the ΔI_s and ΔI_d during BD, the first BD spot was observed at the source (CF-A) with DBIM, creating an MIM (metal insulator metal)-like sub-structure. The Ni in the dielectric could have come from the gate electrode or the DBIM formed in the substrate. Before CF-B formed, CF-A continued to degrade with stressing, inducing more severe DBIM. Note that the Ni metal filament in CF-A was formed by migration from the gate electrode (anode) and the source NiSi contact.

Figure 5-8 (a) STEM-HAADF micrographs of the MIS device in Fig. 5-7 after RESET showing two ruptured conductive filaments (CFs): CF-A and CF-B. The bright area in the Si-substrate beneath CF-A is the lateral diffusion of Ni-based silicide compounds from the source, known as the dielectric-breakdown-induced metal migration (DBIM) [37, 43, 49]. DBIM can also refer to the vertical diffusion of NiSi from TE (anode) into the BD path in the dielectric. DBIM in both lateral and vertical directions could be the physical defects that caused CF-A and CF-B to form a sub-capacitor like metal/insulator/metal (MIM) structure. High-resolution TEM micrographs of (b) CF-A, and (c) CF-B.

5.5.3 CHEMICAL ANALYSIS BY USING EELS

To obtain a high resolution micrograph of under 1 Ångström, a monochromated probe C_s corrected FEI TITAN CUBED system was used. The use of the probe C_s -corrector is necessary to ensure that the electron beams in STEM mode will be tighter and brighter, yielding a stronger signal, higher imaging contrast, greater analytical sensitivity and unprecedented spatial resolution.

The probe size was set to 0.9 Å in diameter to obtain sub-angstrom level resolution, and the point-to-point distance in the EELS line scan is 1.3 Å. The EELS spectra were collected from the central region of the ruptured filament, a region next to the ruptured filament, and locations free of any filament. Figure 5-9 shows the Ni and O EELS line profiles acquired from the two conductive filaments shown in Fig. 5-8 after RESET. The corresponding STEM HAADF micrographs shown in Figs. 5-9 (b) and (d) illustrate the vertical EELS line scan locations. In CF-A, the oxygen atom signal distribution in the ruptured filament is different to the non-filamentary location and the region absence of the filament. The Ni signal is present in the dielectric of the ruptured filament. The lowest Ni signal intensity point for the ruptured filament EELS signal correlates well with the highest O signal, which may signify the localized discontinuity upon recovery. In CF-B, the localized rupturing point of the conductive filament is in the middle. Metal filament nucleation and rupture are feasible for both CF-A and B because of the formation of metal-insulator-metal (MIM) like stacks due to the formation of DBIM at the Si substrate.

Figure 5-9 (a) Ni (dashed line) and O (solid line) EELS signal profiles for the line scans across the NiSi TE, the dual-layer dielectric of HfO_2 and SiO_2 , and the Si substrate at three different locations near the CF-A region. The horizontal axis represents the position along the stack, while the vertical axis represents the intensity of each chemical element signal. The intensity values are normalized for comparison. The three line scan locations shown in (b) are a ruptured filament (black line), a region free of the ruptured filament above DBIM (blue line), and a non-filament spot (red line). At the ruptured filament location, the intensity O is lower than that in the filament-free region, while Ni diffuses into the dielectrics. (c) & (d) show Ni (dashed line) and O (solid line) EELS line profiles of CF-B acquired at two locations as indicated in STEM micrograph in (d). Ni and O distribution trends similar to CF-A were observed.

Figure 5-10 shows the HAADF-STEM micrographs of CF-B, and the Ni and O EELS mapping results for two locations: the edge of the ruptured filament (Area 1), and a filament-free region (Area 2). Ni fragments remain in the dielectric even after the

conductive filaments have been electrically “switched-off.” Since Ni remains in the ruptured filament, oxidation of Ni to NiO_x (an insulator) would explain the recovery. From the very high resistance and low current seen in Fig. 5-7 after the two recoveries, it is very likely that the residual Ni in the dielectric bonded with O^{2-} ions to form NiO_x , an insulator. The chemical and structural changes after conductive filament formation and rupture in this device may be Ni metal filamentation, oxygen ion drift and storage in the metal electrode, and DBIM. All of these effects favor the formation of a conductive filament. The rupture of the conductive filament in bipolar reset can be explained by a combination of joule heating and oxygen re-passivation from the gate electrode. We will discuss the joule heating effect in details in the next chapter. Oxygen re-passivation mostly happened in the bipolar switching mode. Negatively charged oxygen ions (O^{2-}) migrated into the NiSi gate when a positive voltage was applied to the gate, wherein only the opposite voltage polarity can cause the O^{2-} ions to passivate the V_0 traps. The oxygen re-passivation location may be near the gate or deep inside the dielectric. Note that the role played by O^{2-} ions in the bipolar switching process is clearer at very low switching compliance SET transitions [127].

Figure 5-10 STEM-HAADF micrograph and EELS mapping analysis around the dielectric of CF-B. Ni and O EELS maps were collected at the edge of the ruptured Area (1) and a filament-free Area (2). The Ni signal is indicated in red, and the O signal is green. A NiO_x -based compound was highly possible in the ruptured filament.

5.6 SUMMARY

Post-BD recovery in the advanced HfO_2 -based gate stacks was studied using various gate electrode materials by examining electrical properties and through first-principles based simulation. The roles of metal atom migration and filamentation, and the physics underlying the gate material dependent BD recovery were examined by performing theoretical calculations of the bandgap shrinkage and the defect formation energy. The TiN and NiSi based gate electrodes were found to provide adequate bandgap margin to initiate post-BD recovery enhanced TDDDB reliability, but the TaN-gated devices provided a poor post-BD reliability margin. Furthermore, the locations of multiple filaments were found to be spatially uncorrelated.

CHAPTER 6 USING POST-BREAKDOWN STUDY IN MIS STRUCTURE TO BETTER UNDERSTAND RESISTIVE SWITCHING

6.1 INTRODUCTION

This chapter correlates the current understanding of the physics of failure in the post- BD regime of HfO₂ (HK) dielectric-based conventional logic transistors having MIS structure to investigate the mechanism of resistive switching in RRAM technology MIM stacks. The mechanisms of oxygen vacancies, gate metal migration, and metal filament formation in the gate dielectric describe the chemistry of BD in the post-BD stage of logic gate stacks. These mechanisms are accepted as being responsible for the SET process in RRAM technology. This study attempts to draw an analogy between the study of BD in logic devices and filamentation physics in resistive non-volatile memory.

6.2 BREAKDOWN PHYSICS IN THICK OXIDE AND ULTRA-THIN OXIDE

As the mechanisms behind BD (SET) and recovery (RESET) in the HfO₂-based MOS transistor and memory-MIM stacks are similar, the physics that explains the operation of these devices must also be similar and interrelated. Based on previous studies of the post-BD defect transformation in MOS, we investigate the resistive switching mechanism in MIM capacitors.

The oxide layer used in RRAM devices is relatively thick, usually more than 10nm [58]. This makes it hard to capture the details of defect evolution, as the wear-out process that precedes percolation for these thick films results in a very catastrophic and rapid BD transient at the instant of percolation. This transient is often difficult to control due to the current overshoot problem. However, in this study we use ultra-thin dielectrics in the experimental MIS devices with thickness $\sim 1\text{-}4\text{nm}$, providing better control for arresting the BD transient in a softer (i.e. progressive) stage [112].

The BD process in thick and thin oxides is different because of the differences in trap/defect generation mechanisms. The BD in thick oxide ($\geq 10\text{nm}$) is ultrafast: as soon as the stress voltage applied causes the oxide field to exceed a critical value (usually 10MV/cm), the current increases instantaneously due to a positive feedback process that results from continuous positive charge buildup. However, BD in ultra-thin oxides ($\leq 5\text{nm}$) is progressive [128]. BD does not occur until the injected electrons gain enough energy (usually 2eV) to overcome the kinetic energy barrier between the interface of the electrode and the dielectric, causing defect generation in the gate dielectric. Progressive BD is common in ultra-thin dielectrics. Papanikolaou *et al.* [129] and Shubhakar *et al.* [130] describe two examples of progressive BD in conventional SiO_2 dielectric and advanced high- κ (HK) CeO_2 dielectric, respectively. Their results have been verified through both conventional device level electrical measurements [129] and localized scanning tunneling microscopy (STM) stressing [130].

The difference can also be explained by the percolation model [26]. In thick oxides, by the time a percolative path of traps is formed, a large number of traps are generated all over the oxide layer, making it highly defective. Therefore, at the instant

BD occurs, the oxide suffers catastrophic damage and current overshoot is very likely for such severely degraded oxides. However, a thin oxide layer has very few randomly positioned traps at the time of percolation. In other words, the oxide is still intrinsically undamaged at all locations surrounding the percolated region. As a result, the BD process in ultra-thin oxides tends to be soft with progressive and prolonged, gradual wear-out of the oxide layer before a complete hard BD process if the stress maintains to be low. Figure 6-1 shows the difference between the two.

Figure 6-1 Formation of the percolation path in thin and thick oxide layers. Blue circles are electron occupied traps and red circles are the traps forming the percolation path [26].

MOS devices incorporating ultra-thin dielectrics with thickness $\sim 1\text{-}4\text{nm}$ were used for this study to provide better control for arresting the BD transient at a soft (i.e. progressive) stage [112]. Thus, the mechanism of BD can be investigated more precisely. Table 6-1 lists the ultra-thin gate dielectric-based HK MIS devices with different gate materials used in this study.

Table 6-1 List of MIS devices tested with details of their gate and dielectric materials.

Sample number	Gate material	Dielectric material
S1	Poly-Si	SiON ~ 1.6nm
S2	Poly-Si	HfO ₂ -based HK 4.4nm
		SiO _x interfacial layer (IL) 1.2nm
S3	TaN	HfO ₂ -based HK 2.5nm
		SiO _x IL 1.2nm
S4	NiSi	HfO ₂ -based HK 2.5nm
		SiO _x IL 1.2nm
S5	TiN	HfO ₂ -based HK 1.8nm
		Zero IL

6.3 RESISTIVE SWITCHING IN THE MIS STRUCTURE

The role of several gate electrode materials is also investigated in this work. Poly-Si/SiON, poly-Si/HK/IL, NiSi/HK, TaN/HK, and TiN/HK n-type MOS transistors were subjected to a SCVS test [27] in inversion mode (i.e. substrate injection) at room temperature to identify the leakage level (indicative of the BD hardness) at which recovery (analogous to switching in MIM) is initiated, as shown in Fig. 6-2. For easier interpretation of the BD evolution graphs, the scale of I_g in Fig. 6-2 is not constant. Poly-Si gated stacks show progressive BD behavior, while metal-gated stacks show ultrafast BD behavior. However, there is significant variation in ultrafast BD among different gate materials. Both NiSi and TiN gate stacks show ultrafast transient and rapid increase in I_g followed by a recovery phase.

Figure 6-2 Time evolution of the gate leakage current I_g during the SCVS test. A progressive BD profile of a conventional poly-Si/SiON (S1) gate stack is shown for comparison. The Poly-Si/HK (S2) gate stack I_g (in blue) shows progressive BD after a dielectric BD event, instead of an instantaneous change in I_g . In this case, I_g degrades towards a device failure criterion with a relatively gradual profile. NiSi/HK (S4) gate stack I_g (in red) shows a recovery after ultrafast BD wherein I_g reaches a preset compliance current I_{gl} instantaneously. TiN/HK (S5) gate stack current I_g (in green) shows moderate recovery after an abrupt BD, whereas the TaN/HK (S3) transistor shows no recovery at all.

The NiSi/HK stack also demonstrates very good bipolar resistive switching performance. The switching operation is called bipolar because the SET and RESET voltages have opposite polarities. Figure 6-3(a) shows a typical linear scale I_g - V_g characteristic graph for a dual-sweep voltage cycle (ranging from $-3V$ to $+4V$) with a fixed compliance current, $I_{gl} \sim 100\mu A$. After a slow voltage ramp up from $0V$ to $+4V$, BD (similar to FORMING in resistive switching) was initiated at $V_g = 3.8V$ (equivalent to $V_{FORMING}$). A transition from the HRS to LRS occurred. The device remains in the LRS during the reverse sweep. As the voltage was swept in the negative polarity, a recovery in the gate leakage (analogous to the reversible transition from LRS to HRS in RRAM) was

observed at $V_g = -2.8\text{V}$, which is analogous to V_{RESET} . The device remains in this RESET state until it is subjected to a high $V_g > V_{SET}$ again for further repeated switching (not shown here). In this case, the conductance ratio (resistance memory window) $I_{ON}/I_{OFF} \sim 1000$ in the READ voltage range $0.5 - 1\text{V}$. Fig. 6-3(b) shows switching in a semi-logarithmic plot where the large hysteresis indicates the switching phase. Thus, BD and recovery in the logic device reliability test are analogous to the SET and RESET processes in MIM switching capacitors. Table 6-2 provides a detailed comparison of terminologies used in logic breakdown and resistive switching in RRAM devices. The terminologies used may be different. However, the underlying physics of SET transition (analogous to BD) has to be correlated. Note that SiO_2 layer on Si substrate is negligible, and we consider it as part of the insulator layer as well as HfO_2 layer.

Figure 6-3 A close examination of the recovery after BD in the NiSi/HK (S4) gate stack shows hysteretic bipolar switching I - V curves similar to RRAM capacitive stacks. (a) Starting from a HRS, a ramp voltage was applied starting at 0V, going to a positive value and back to 0V to complete the cycle indicated by the arrows. The SET (HRS to LRS) and RESET (LRS to the HRS) points are marked in the I_g - V_g cycle. LRS and HRS are identified as ON and OFF states, indicating whether a current does or does not flow through the gate stack. (b) Logarithmic scale plot of I_g - V_g showing sharp changes in the conductivity ($I_{ON}/I_{OFF} > 1000$) during BD (SET) and recovery (RESET).

Table 6-2 Comparison of the terminologies used for logic BD and RRAM, and the similarities and differences in their test structure.

LOGIC BREAKDOWN	RRAM SWITCHING
Breakdown	SET (HRS to LRT)
Recovery	RESET (LRS to HRS)
Percolation/BD path	Conductive filament
Gate/Substrate	Top electrode/Bottom electrode
M-I-S	M-I-M
Gate electrode materials: NiSi, TiN, and TiN	Top electrode materials: TiN, TaN, and Pt
Gate dielectric materials: HfO ₂ , ZrO ₂	Insulator materials: HfO ₂ , TiO ₂ , Ta ₂ O ₃
Transistor	Capacitor
Thickness of dielectric: 2 – 4nm	Thickness of insulator: 7 – 10nm
Interface between dielectric and electrode: Ångström-scale roughness (interface roughness between Si and SiO ₂ is ~ 2Å [131])	Interface between dielectric and electrode: nanometer-scale roughness (interface roughness between Pt and TiO ₂ is around 2-4nm [58])
Lifetime	Retention

6.4 MODEL ON RUPTURE OF THE CONDUCTIVE FILAMENT

6.4.1 TWO-STAGE EVOLUTION OF THE CONDUCTIVE FILAMENT IN NiSi/HK MIS DEVICE

We selected the NiSi/HK MIS device for studying the evolution of the conductive path since it has the best switching performance for both unipolar and bipolar operation. As we performed failure analysis on four-terminal MIS devices, the precise BD location along the channel length could be detected electronically, as described in Chapter 5. Furthermore, knowing the BD location, we can perform in-depth elemental mapping very close to and at the BD location even though it may not show any clear microstructural changes for a very soft BD [18, 19, 34]. This is a significant advantage over the two-terminal MIM capacitive stacks, which offer no identification electrically in finding the precise location of the nanosized conductive filament for elemental analysis.

To capture the defect evolution process, we varied I_{gl} to arrest the BD of the logic device at different levels of hardness. Figures 6-4 (a) and (b) show the high resolution TEM micrographs of the NiSi/HK gate stack conductive path evolution, with compliance currents of 1 μ A and 2 μ A. The electronic measurement for the sample in Fig. 6-4 (a) indicates that the BD location is near the source, where Si atoms from the substrate push into the oxide layer forming hillocks. This physical defect known as DBIE is common in a transistor-based dielectric gate stack when BD occurs [112, 132]. DBIE is a nano fingerprint that can be used to identify the location of BD. Previous EELS analyses [18, 19] showed a lower oxygen K-edge count in the dielectric in the vicinity of the DBIE spot (i.e. the dielectric region that underwent BD) compared to a non-BD area. This suggests that the conductive path is comprised oxygen vacancies making the local chemical

structure of the conductive path an oxygen deficient SiO_x , where $x < 2$. Therefore, oxygen vacancies, Si-O bond breakage, and the associated structural relaxation are the chemical changes that result in dielectric BD. Further examination of the HK dielectric also shows that oxygen vacancies are the dominant precursor defects, which form electrically active traps that comprise the percolation path.

In Fig. 6-4 (b) [71], the metal migration and filament formation in the sample are clearly visible in the high resolution TEM micrograph. Ni spiking with diameter as small as $\sim 2\text{nm}$ is observed in the HK layer forming a conductive filament, shorting the top and bottom electrodes. Notably, there is no evidence of metal filament nucleation in the poly-Si HK stack. However, in the MIS based structure, in addition to oxygen vacancies, metal atoms from the gate electrode migrate to the Si substrate through the gate dielectric creating a spike or punchthrough of the HK dielectric, which is probably driven by ion/hole migration [118]. First-principles calculations show that the metal atoms prefer to migrate along the oxygen vacancy sites in the percolated region, favoring the lowest energy configuration.

The study of conductive (metallic) filament formation at different levels of BD hardness or different BD stages is important. Prior to the nucleation of metal filaments at the harder stages of BD (i.e. SET), the oxygen vacancy is the only type of defect corresponding to the initial formation of the percolation (conduction) path. This is similar to percolation path formation in poly-Si/ SiO_x gate stacks [18, 19, 34].

Figure 6-4 High resolution cross-sectional TEM micrographs of three NiSi/HK gate stacks after a first BD capped at different compliance currents (a) $I_{gl} = 1 \mu A$ and (b) $I_{gl} = 2 \mu A$ [71]. The insets show a low magnification view. For $I_{gl} = 1 \mu A$, the BD gate dielectric does not show any obvious structural damage except for DBIE that has a percolated HK layer of oxygen vacancies [18, 19, 34, 41]. For $I_{gl} = 2 \mu A$ a 2nm Ni filament spiking through HK into the Si channel and a DBIE are clearly visible [71]. (c) and (d) The evolution of oxygen ion diffusion and metallic filament formation corresponding to (a) and (b).

To summarize, the conductive filament consists of oxygen vacancies surrounding the Ni filament. The formation of the conductive filament is a two-stage process. The first stage is labeled the soft BD stage in logic gate stack reliability studies (i.e. with low

compliance current of approximately $1\mu\text{A}$). In this stage, oxygen vacancies are the physical defects responsible for the formation of a percolation path, as shown in Fig. 6-4(c). In the second stage, metal atoms from the top gate electrode migrate along the oxygen deficient BD path, driven by the high current density and temperature enhanced metal atoms diffusion [43, 116]. They form a metal filament at the centre of the BD spot that is surrounded by oxygen vacancies, as shown in Fig. 6-4(d). The role of the metal filament is to improve the uniformity of the device switching performance, and to reduce the SET voltage. A recent study by Panda *et al.* [133] found that the SET voltage of RRAM devices with embedded metal nanocrystals inside the dielectric is lower than the one with no nanocrystals present.

Based on the asymmetric MIS structure and filamentation from metal gate electrode, the results suggested that the conductive filaments in RRAM are likely to nucleate from the anode side; in other words, anodic migration is the governing phenomenon [116]. Therefore, the key interface of interest in resistive switching is the anode/dielectric interface.

6.4.2 SIZE EFFECTS ON THE CONDUCTIVE FILAMNET IN NiSi/HK AND TaN/HK DEVICES

As discussed earlier, among the different metal electrode materials tested in this study, NiSi has the best recovery (i.e. switching), whereas no such switching is seen in TaN. The switching behavior appears to be highly dependent on the electrode material. Therefore, the choice of gate electrode material is crucial for obtaining good switching trends. For further comparison, high resolution TEM physical analysis of the hard BD

NiSi/HK and TaN/HK gate stacks is shown in Fig. 6-5 [49, 71]. In the NiSi/HK MIS structure, the diameter of the Ni filament is $\sim 2\text{nm}$. However, the Ta metal filament shows a bowl-shape about 10nm across. As the diameter of the Ta metal filament is large, it cannot be burned-off or ruptured during the RESET process. The size of the Ni spike does not change going from the soft BD stage to the hard BD stage; it is also unchanged going from I_{gl} of $2\mu\text{A}$ shown in Fig. 6-4(b) to I_{gl} of $500\mu\text{A}$ shown in Fig. 6-5(a).

Figure 6-5 High resolution cross-sectional TEM micrographs (a) NiSi/HK [71] (b) TaN/HK [49] gate stacks after BD capped at a very high compliance current $I_{gl} = 500\mu\text{A}$. A 2nm Ni filament spiking through the HK into the Si channel is visible in the NiSi/HK sample. The Ta metal filament shows a bowl-shape about 10nm across. The diameter of the Ni filament ($\sim 2\text{nm}$) is much smaller than Ta ($\sim 10\text{nm}$).

6.4.3 METAL FILAMNET RUPTURE MODEL

Rupture of metal filaments is necessary to initiate an LRS $\rightarrow$ HRS transition through melting, thus high temperature and current density are needed. The rupture of filaments, RESET, is attributed to joule heating in the nanofilament, where the localized temperature may exceed its melting point, causing a phase transition and leading to

rupture (dissolution). We can estimate the temperature in the formed filaments prior to RESET by applying the non-uniform, flawed filament model [134] and the steady state temperature equation given in [135]

$$T_{filament} = \sqrt[4]{T_0^4 + \frac{J^2 \rho r}{2P_w}} \quad (6.1),$$

where $T_{filament}$ is the increased filament temperature due to joule heating, T_0 is the room temperature = 300K, J is the current density, ρ is the sample resistivity, r is the filament radius, and P_w is the radiative loss parameter for the filament, which is approximately $3 \times 10^{-7} \text{ Wm}^{-2}\text{K}^{-4}$ [136].

Equation 6-1 gives a temperature of over 1434K for a current of 200nA in a Ni nanowire with $r = 2\text{nm}$ and $\rho_{\text{Ni-nanowire}} = 5 \times 10^{-4} \Omega\text{cm}$ [137]. This temperature is higher than the melting point of the Ni spike with $T_{melting} \sim 1160\text{K}$ [120]. The melting point of Ta, $T_{melting} \sim 3020\text{K}$ is extremely high [138], while $T_{filament}$ is only $\sim 348\text{K}$. In this case, the temperature in the formed filaments is too low for phase transition.

It is important to note that in this mode, the melting temperature of the Ni nanowire is strongly dependent on its diameter. As the diameter of the Ni nanowire decreases, the melting point of the nanowire also decreases due to increase in the ratio of surface area and volume. Wen *et al.* [120] reported that the melting points of Ni nanowire of diameter 1.23nm and 1.94nm are 880K and 1160K, respectively. From TEM results, we found the diameter of the Ni spike to be $\sim 2\text{nm}$. Thus, 1160K was set as the benchmark temperature. The resistivity of a nanowire also depends on diameter. However, there is no exact formula linking Ni nanowire diameter and resistivity. In this study, we used the resistivity values from Ref. [137]. The calculated temperature of the

filament is significantly higher than the melting point of Ni in the resistivity range 2.5×10^{-4} to $6.7 \times 10^{-4} \Omega\text{cm}$, as shown in Table 6-3. Our filament rupture model explains why the TaN-gate based material is unlikely to show any recovery (switching). Thus, it provides another explanation for the easy dissolution of 2nm Ni spikes, in contrast to the 10nm Ta filament.

Note that a simplified model based on the steady stage temperature equation is used here. Advanced thermodynamic analysis was performed by Raghavan *et al.* in Ref. [139]. We modeled the ruptured conductive filament from the macroscopic perspective (classical physics) by thermal analysis, which complements our previous microscopic atomistic simulation by first-principles calculation (quantum physics). The latter focuses more on the bandgap and DOS changes when recovery of BD occurs.

Table 6-3 Size-dependent Ni nanowire resistivity values and calculated filament temperatures.

ρ (resistivity)	T_{filament}
$2.5 \times 10^{-4} \Omega\text{cm}$ [134]	1206 K > 1160 K [120] (T_{melting})
$6.7 \times 10^{-4} \Omega\text{cm}$ [134]	1543 K > 1160 K [120] (T_{melting})

6.5 CHEMICAL ORIGIN OF FORMING FREE RESISTIVE SWITCHING DEVICES

6.5.1 FORMING PROCESS

Previous TEM/EELS analysis showed that the conductive filament consists of oxygen vacancies surrounding the metal atoms. For a virgin oxide layer, the voltage required to form a percolation path (V_{FORM}) is relatively high, imposing severe constraint for circuit design. For stable RRAM operation, the forming and successive cycle SET

voltages (V_{SET}) should be similar and relatively low. Moreover, if V_{FORM} is large, the oxide may suffer from substantial degradation (trap generation) before reaching the compliance current level, which in turn can affect the endurance behavior of the memory device. This is more likely in thicker (5-10nm) high- κ dielectrics currently being considered for commercial RRAM applications. Thus, new approaches for reducing V_{FORM} and enhancing RRAM performance metrics are needed. To this end, Fang *et al.* fabricated a new multilayer oxide stack containing an additional buffer layer consisting of TiO_x on top of an HfO_x layer. Figures 6-6 (a) and (b) show the TEM micrographs of the single layer and the multi-layer HfO_x RRAM device, respectively. The $HfO_x/TiO_x/HfO_x/TiO_x$ multilayer RRAM shows substantial improvement in the cycle-to-cycle uniformity within one device and device-to-device uniformity. Moreover, electrical characterization results in Fig. 6-7 (b) show that these multilayer devices are free of the forming process [140, 141].

Figure 6-6 (a) Cross-sectional TEM micrograph of a single layer HfO_x RRAM device. The thickness of the HfO_x layer is 9.70nm. (b) TEM micrograph of a multi-layer HfO_x RRAM device. The thickness of the oxide layer was measured by averaging the whole layer based on a full width at half-maximum method. Distinctive multi-layer oxides are clearly visible.

6.5.2 ELECTRICAL CHARACTERIZATION ON FORMING FREE RRAM DEVICES

Figure 6-7(a) shows the typical forming, SET and RESET processes of a single layer HfO_x device followed by five successive cycles. The forming voltage (1.7V) is 0.6V more than the SET voltage (1.1V). The initial (virgin) state resistance (before forming) is 2.5 times the HRS resistance after the RESET process. For the forming-step free multilayer RRAM fabricated in this study, the virgin state resistance is similar to the HRS resistance after RESET, as shown in Fig. 6-7(b). Moreover, the forming voltage (1.5V) is comparable to the subsequent SET (1.4V) voltage, which suggests that the *conventional* high voltage forming process is no longer needed for this device. Figure 6-7(c) shows the SET voltage distribution of the single layer device and multilayer RRAM devices undergoing 500 dc cycles. The distribution of SET voltages in our multilayer RRAM devices is not as wide spread as in the single layer RRAM devices.

(Continue on next page)

Figure 6-7 (a) Forming process followed by five successive bipolar switching cycles (i.e. SET/RESET) for single layer HfO_x device. The ON/OFF ratio is 10. (b) Initial SET/RESET in the forming-free device is followed by five successive bipolar switching cycles. No forming step is needed in the multiple oxide layer RRAM device. The voltage difference between the first forming sweep and the SET voltage is less than 0.1V. The ON/OFF ratio has been increased to 100 from 10 for the single layer HfO_x device shown in (a). (c) SET voltage distribution comparison between single layer and multilayer RRAM devices after 500 dc cycles.

6.5.3 EELS ANALYSIS

For the multilayer RRAM device, it was suspected that Ti atoms from the capping layer have diffused into the HfO₂ layer, causing the forming-free behavior.

To analyze the chemical distribution and origins in the forming-free multilayer RRAM device, EELS measurements were performed at 200kV in STEM mode. The STEM probe diameter was 1.3Å, and the point-to-point distance was 3.0Å in the line scan. We performed physical analysis using TEM-EELS on a statistically meaningful set of 5 devices. For each device, we collected more than 3 sets of EELS data from different locations.

Figure 6-8 shows the EELS results of the N K-edge, Ti L_{2,3}-edge, and the O K-edge of a fresh multilayer RRAM device. The N K-edge is clearly visible in the TiN TE layer, but no such signal is seen in the multi-layer oxide region. The oxygen signal is clear in every oxide layer, but an O-count of zero was recorded in the TiN TE layer. Most importantly, a sharp rise in the Ti L_{2,3}-edge is seen in every oxide layer, indicating that the Ti ions actually diffused/migrated into both HfO_x layers. Thus, our hypothesis was verified successfully.

Figure 6-8 EELS results of the fresh multilayer oxide RRAM device, showing N K-edge at 401eV, Ti $L_{2,3}$ -edge at 453eV, and the O K-edge at 532eV. The sharp rise in the Ti $L_{2,3}$ edge is found in every oxide layer, indicating that Ti diffused into both HfO_x layers. The point to point distance in the EELS line scan is 3.0Å. The N K-edge is visible in the TiN top electrode layer, but no signal was found in the multiple oxides layer. The oxygen atom count is large in every oxide layer, but negligible in the TiN top electrode layer.

6.6 SUMMARY

We investigated the bipolar switching mechanisms in HfO_2 -based dielectrics using traditional MIS logic transistors. A clear correlation between the recovery of dielectric BD and resistive switching was established and current understanding of the physics of dielectric failure and defect chemistry in metal gate high- κ stacks was used to study the microscopic filamentation mechanism in RRAM. Oxygen vacancies and metal filamentation are the two main physical/chemical defects responsible for the switching phenomena in the nanosized conduction path. Their role depends on the compliance

current chosen for the forming/SET process. Forming-free behaviors were also investigated in MIM RRAM devices and the diffusion of metal atoms into the HfO_2 layer was found to be the chemical cause initiating the forming-free process.

CHAPTER 7 CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

This thesis presents a comprehensive study on the fundamental physics governing the resistive switching phenomenon combining the inferences from electrical characterization, physical analysis, and atomistic simulation results. We leveraged on the existing asymmetric MIS stack as a unique test structure to enable us to better understand the role played by the insulator and the metal electrode material in a standard symmetric MIM RRAM stack.

It is found that the conductive filament consists of oxygen vacancies and metal filament. Oxygen vacancies are found to be responsible for the formation of a sub-band in the forbidden bandgap region, which affects the triggering voltage of digital breakdown and leads to a shrinkage of the HfO_2 bandgap on one hand. On the other hand, metal filament, has also been found being responsible for the breakdown in the HfO_2 metal gate stacks. Recovery is possible in the broken-down dielectrics with enough low defect formation energy of metal atoms migration, which can be realized by selecting proper gate electrode materials, such as NiSi and TiN. The anode terminal (gate electrode in our study) material plays an important role.

There are two stages for the formation of the conductive filament: the initial stage, which is commonly referred to as the soft breakdown stage in MIS gate stack reliability study, wherein the oxygen vacancies form the chemical constituents of the percolation path; In the second stage, the metal atoms from the gate electrode migrate along the

oxygen deficient breakdown path driven by the high current density and temperature enhanced metal atom diffusion, forming a metal-rich filament at the central core of the breakdown spot. As for the analysis of the filament after rupture, our physical analysis results still show metal fragments remaining in the dielectric even after the conductive filaments have been electrically switched-off. It is very likely that the residual metal in the dielectric bonds with the O^{2-} ions forming an insulator.

We also demonstrate that multiple conductive filaments can be individually switched-on and switched-off and are spatially uncorrelated. The residual metal in the dielectric layer may affect the retention lifetime and endurance of the memory device. The uncorrelated multiple conductive filament formation has implications on the feasibility of further scaling down the size of future RRAM devices.

7.2 RECOMMENDATIONS FOR FUTURE RESEARCH

We believe that there is scope for this project to be further extended. Some of the possible directions for future investigations and studies are listed below:

- The proposed methodologies, combining electrical, physical characterization and atomistic simulation, can be further applied to thoroughly analyze the new upcoming device technologies under research, especially new device architectures and material systems such as nanowire and graphene-based devices. New mechanisms and defects can be identified using physical analysis techniques and correlated with the electrical characteristics of the device.
- The basic operation mechanism of the RRAM is the switching between the insulating and conducting states of the dielectric material. In recent RRAM

devices, the dielectric layer used is thick ($> 10\text{nm}$), while the interface between the metal electrode and dielectric is rough ($\sim 2\text{nm}$ roughness). Our MIS structure provides atomic flat interface and ultra-thin oxide layer. Furthermore, the MIS structure can be easily integrated for future 3D device structures. It would be interesting to fabricate 3D devices at the wafer level, which potentially can be used for future technologies.

- *In-situ* electron microscopy is a powerful nanoscale characterization tool, which can collect both electrical data and nanoscale results at the same time. This new technique opens the door for future characterization of nanoscale devices.

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