Design of a high speed and power efficient quarter-rate clock and data recovery circuit

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**DESIGN OF A HIGH SPEED AND POWER EFFICIENT QUARTER-RATE CLOCK AND
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Abstract

Due to the advantage in technology and multi-media, the demand for data communication has increased tremendously. More standards for high speed low power communication have been established, i.e. Serial Advanced-Technology Attachment (SATA), Peripheral Component Interconnect Express (PCIe), Universal Serial Bus (USB) and etc. In the receiver design, the clock and data recovery (CDR) circuit is an important block as the clock signal is embedded in the receiving data.

This thesis presents several new circuit designs to improve the performance of the CDR circuit. First, a new quarter-rate linear phase detector (PD) is proposed to reduce the circuit complexity of the reported quarter-rate linear PD design. Besides that, the proposed PD applies UP pulse-widening technique to resolve the issue of small UP pulses. The existing PDs with UP pulse-widening techniques have more output signals, which increases the difficulties in designing the Charge Pump (CP). In the proposed PD, the number of output signals has been successfully minimized.

This thesis also provides propagation delay analysis of the proposed PD. A set of equations is derived from the analysis to predict the characteristic curve of the proposed PD. At the linear region, the accuracy of the prediction results is 98% of the simulation results. The effect on propagation delay at various phase differences is also being discussed.

Second, a quarter-rate de-multiplexer (DEMUX) is proposed to increase the power efficiency. At a data rate of 10-Gb/s, the DEMUX has a phase margin of 72-ps and it consumes 6.98-mW from a 1.8-V supply voltage. The DEMUX also has the advantage of integrating with the PD. The integration not only resolves the systematic offset of the retimed data but also provides the retimed data with a 1:4 DEMUX function.

Third, an unbalanced charge pump (CP) is proposed to compensate for the PD design. Besides compensating for the difference in the UP and DOWN (DN) pulse-widths, the unbalanced CP also compensate for the difference between the number of UP and DN signals. With the unbalanced CP, the PD does not require additional DN signal. Hence, this reduces the number of output signals of the PD.

Fourth, in dual-loop CDR architecture, the lock detector (LD) plays an important role in controlling the switching between the loops. However, the conventional LD has only one required parts-per-million (ppm) or frequency range, which increases the challenge in setting the ppm value. A hysteresis LD is proposed in this thesis to circumvent this issue. It has two different ppms for two different conditions; a smaller required ppm for in-lock condition and a larger required ppm for out-of-lock condition.

Fifth, this thesis also provides methodology in designing the third order loop filter in a dual-loop CDR design. For a given phase margin and unity gain bandwidth, the values of the capacitance and resistance can be calculated through a set of equations presented in this thesis.

Finally, a fully integrated 5-Gb/s quarter-rate linear CDR design is presented. With the dual-loops architecture, the frequency tracking ability of the CDR is enhanced. The CDR design consumes a total silicon area of $1.9 \times 2.3\text{-mm}^2$. Its total power consumption is 71.9-mW at a supply voltage of 1.8-V. It has a 30.4-ps peak-to-peak clock jitter and the power efficiency is 14.38-mW/Gbps.

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1 Introduction

1.1 Motivation

The increasing growth of data transfer over the Internet in recent years has induced a blast in data communication over wide-area networks (WANs) and local-area networks (LANs). The International Technology Roadmap for Semiconductors (ITRS) anticipates that the non-return zero (NRZ) data rate for high speed communication will reach 100-Gbps by the year 2019 [1]. In order to accommodate the increase in data rate requirement, researchers have endeavoured to integrate a low cost, low power and high speed serial-link data transceiver.

Figure 1.1. Block diagram of a generic high speed wire-linked data transmission system.

Fig. 1.1 shows the block diagram of a generic high speed wire-linked data transmission system [2]. At the transmission side, parallel input data will be multiplexed and pre-emphasized with output buffer. The data is then transferred through a transmission medium to the receiving end. In many transmission systems, in order to reduce the cost of the transmission medium used, the system will only transfer the data without transferring the clock. Due to the lack of clock signal in this embedded clock system, at the receiving end, the data cannot be de-multiplexed after the input buffer. Hence, the clock and data recovery (CDR) circuit is implemented and placed before the de-multiplexer (DEMUX) to recover the required clock for the following synchronous process.

In the embedded clock receiver design, the CDR is a critical block as it not only recovers the clock but also retimes the input data for further synchronous processing. During the transmission, the integrity of the input signal will be degraded by crosstalk, attenuation and reflection. With all these effects, the input data becomes noisy and jittery. Hence, it is a great challenge to design CDR circuit.

Besides wire-linked data transmission system, CDR is also crucial for some of the wireless transmission system. In a crystalless wireless transceiver [3], CDR circuit is critical as it provides clock signal for the mixer from the data stream. Besides crystalless wireless transceiver, CDR is also crucial for the wireless optical communication [4, 5] and biomedical implantation [6-8]. Hence, the research on CDR design is essential for transmission system. As the CDR is also being used in portable devices, the power

efficiency of the CDR is also another important aspect. In this thesis, we will be focusing on achieving a high speed power efficiency CDR.

1.2 Organization of the Thesis

This thesis consists of nine chapters. Chapter 1 gives an introduction to multi-giga-bits serial-link systems and the outline of the thesis.

Chapter 2 provides an overview of the clock and data recovery (CDR) circuit. The specifications such as data format and jitter are presented. The discussion of various CDR architectures grants an in-sight on the advantages and disadvantages of each architecture. A more comprehensive study on Phase Locked Loop (PLL) design provides understanding in designing the parameters of the loop filter. The important terms of PLL, i.e. natural frequency, damping factor, loop bandwidth and locking behavior are also defined.

Chapter 3 presents a literature review of the phase detector (PD). Two main types of PD design; linear and binary, are discussed and compared. As the linear type of PD has a superior performance in jitter, a more detailed discussion is provided. Lower-rate linear PD, i.e. half-rate and quarter-rate, are explored to provide more understanding in lower-rate design.

Chapter 4 proposes a quarter-rate linear PD with UP pulse widening technique. The proposed PD reduces the circuit complexity of the quarter-rate linear PD and also minimizes the number of output signal of the PD. In addition to that, a detailed analysis on propagation delay provides equations to predict the characteristic curve of the PD. The propagation delay analysis also explores the changes of UP and DOWN (DN) pulse-widths under various phase difference.

Chapter 5 discusses on the architecture of the DEMUX. Two important architectures, shift register architecture and tree architecture, are presented and compared. This chapter also explores the modification of the important block, D-latch. A novel quarter-rate DEMUX is proposed and it has a good performance in power consumption.

Chapter 6 covers the dual-loops CDR design and two other important building blocks, charge pump and voltage controlled oscillator (VCO). The dual-loops CDR consists of a frequency acquisition loop and a phase tracking loop. With the additional frequency acquisition loop, the capture range of the CDR is increased. An unbalanced charge pump design is proposed to compensate for the PD design. It compensates for the difference in the UP and DN pulse-widths and the number of UP and DN signals. A VCO that provides quadrature phase is also mentioned in this chapter.

Chapter 7 covers the building blocks of the frequency acquisition loops. The first section discusses architecture design and function of the phase frequency detector (PFD). The second section discusses on the frequency divider and the third section discusses on

the proposed hysteresis lock detector (LD). The LD has two different required ppms (or frequency range) under two different conditions.

Chapter 8 focuses on the overall design of the dual-loops quarter-rate CDR circuit. The method to calculate the loop filter parameters is discussed. The measurement results of the CDR are also presented. Lastly, the proposed CDR is compared with other reported CDRs.

Chapter 9 summarizes the results and concludes the thesis. The recommendations for further research on CDR design are also presented.

2 Background

2.1 Introduction to Clock and Data Recovery (CDR)

Figure 2.1. A generic block diagram of CDR's function.

It has been a challenging task to design CDR circuit. When data is transferred through a transmission medium, it suffers from the attenuation of the medium and also the distortion due to noise. The disturbance caused by crosstalk and reflection further degrades the signal integrity. The jittering and distorted input data increases the difficulties for the CDR circuit to recover the clock. As it is also a tough task for DEMUX to de-multiplex the jittering and distorted data, the CDR circuit is required to recover the clock and retim the data so that the signal integrity of the data can be improved.

Fig. 2.1 shows the general concept of the function of a CDR circuit. In essence, it performs two main functions: 1) retim the jittering and distorted input data and 2) recovers the required clock from the input data. As the recovered clock is being used to resynchronize the data, the sampling edge of the clock has to be at the center of data eye to ensure the performance of bit-error-rate (BER). In order to achieve these two main functions, the recovered clock frequency has to be the same as the data rate and the phase

difference between the recovered clock and the retimed data should be kept at half of the data rate. Besides that, the recovered clock is also required to have a minimum amount of jitter because the jitter of the retimed data is influenced by it.

2.2 Data Format for High Speed CDR

Figure 2.2. Data format of NRZ and RZ.

In many of the high speed serial-link data communication system, data is transmitted in the non-return-to-zero (NRZ) format instead of return-to-zero (RZ) format. Fig. 2.2 shows the timing diagrams of these two data formats and they have the same data stream. The data stream in the diagram has a period of T_b which translates to the data rate of $1/T_b$. In RZ format, the signal will return to zero after every half data period while in NRZ format, the signal will remain at the current bit value for each data period. If the data period is T_b , the minimum pulse-width for RZ and NRZ format is $T_b/2$ and T_b respectively. By comparing these two pulse-widths, the required bandwidth for RZ format is twice that for the NRZ format. Hence, NRZ format is preferred in many high speed communication systems as circuit bandwidth is very expensive to trade-off.

Although NRZ format is superior in bandwidth performance, it is trade off with some other properties which are challenging in CDR design. First, no data transition is found in a data stream with long sequence of ONEs or ZEROs. In this situation of inadequate data transition, the CDR must be able to maintain the data rate it acquired previously. Hence, the drifting effect of the recovered clock frequency should maintain within a negligible range.

Figure 2.3. Power Spectrum Density diagram for NRZ and RZ format.

Second, the NRZ format does not carry any frequency component at the frequency equal to data rate. This can be clearly seen from the spectrum of NRZ format. The autocorrelation function of an unipolar NRZ format can be written as follow [9]

$$R(k) = \begin{cases} \frac{1}{2} A^2, k = 0 \\ \frac{1}{4} A^2, k \neq 0 \end{cases} \quad (2.1)$$

where A is the amplitude of the data stream. Hence, the power spectral density, P(f), is obtained as follow

$$P(f) = \frac{A^2 T_b}{4} \left(\frac{\sin f\pi T_b}{f\pi T_b} \right)^2 \left[1 + \frac{1}{T_b} \delta(f) \right]. \quad (2.2)$$

Fig. 2.3 shows that no frequency component is found at the integer multiple of data rate. This disables the direct extraction of the clock from the data stream. Hence, the CDR circuit has to undergo some non-linear operation in order to extract out the clock.

2.3 CDR Specification

2.3.1 Introduction to Jitter

Jitter is the most important parameter in determining the performance of CDR. It is defined as the time domain aberration of the clock or data transition time from their ideal case. The deviation of transition time shown in Fig. 2.4 illustrates the definition of jitter. The source of jitter can generally be categorized into two main portions, random jitter and deterministic jitter.

Figure 2.4. Illustration of jitter in timing diagram.

Deterministic jitter (DJ) generally has a characteristic of non-Gaussian probability density function which is predictable and reproducible. Its peak-to-peak amplitude is restricted within certain range in units of time. There are three basic categories of DJ: 1) data dependent jitter (DDJ) which is caused by duty cycle distortion and inter-symbol

interference (ISI), 2) bounded uncorrelated jitter (BUJ) which is mainly due to crosstalk and some other secondary effects like electromagnetic interference (EMI), and 3) periodic jitter (PJ) which is caused by modulating effects that has a periodic characteristic. In multi-gigabit rate, DDJ becomes more substantial as compared to other categories of DJ.

Random jitter (RJ), as it is called, is a random behaviour and an unpredictable pattern in the time domain. It is caused by device effects such as thermal noise, flicker noise, and some other random modulations and etc. For the case where white noise is the main cause of RJ, it can then be characterized with a Gaussian probability density function.

2.3.2 Jitter Measurement

There are two commonly used units to measure the amplitude of the jitter. The first type of unit is in terms of the absolute time which is in picoseconds in multi-gigabit system. Another type of unit is the unit intervals (UI) and one UI is defined as the period for one bit. For example, 0.1 UI jitter in a 5-Gb/s system means that its jitter amplitude is equal to 20-ps.

Root mean squared (RMS) jitter and peak-to-peak jitter are two common methods to measure the amplitude of jitter. The value of RMS jitter provides the jitter noise power in a given time period and it can be shown by the following equation,

$$Jitter_{RMS} = \sqrt{\frac{1}{T} \int_0^T (j(t))^2 dt} \quad (2.3)$$

As for peak-to-peak jitter, it provides the maximum amount of jitter fluctuation which is the worst case scenario. The value of peak-to-peak jitter can be calculated by finding the difference between the maximum and the minimum jitter amplitude which is as follow,

$$Jitter_{peak-to-peak} = \max(j(t)) - \min(j(t)) \quad (2.4)$$

2.4 CDR Architecture

As more researchers devote in CDR circuit design, there are generally several different types of architecture being reported. In this section, we will briefly discuss and compare some of the popular architectures.

2.4.1 Injection-Locked based CDR

Figure 2.5. Block diagram of Injection-locked based CDR

This is the simplest type of CDR architecture which applied open-loop topology [10, 11]. Fig. 2.5 shows that the input data, D_{in} , is first pass through an edge detector circuit which can be implemented by a delay block and a XOR gate. With this edge detector, the frequency components of the input data can be extracted. By passing through a high-Q band-pass filter, the required clock is extracted out for the purpose of data

retiming which is accomplished with a D-flip-flop (DFF). This high-Q band-pass filter can be implemented with an off-chip surface acoustic wave (SAW) filter, LC tank or dielectric resonator.

With the advantage of having a simple structure, the design cost and time is reduced. Besides that, this architecture has a very short acquisition time. However, the high-Q band-pass filter restrains its integration ability as it is very difficult to implement in monolithic. In order to overcome this constraint, some slight variations of this architecture have been reported. It is achieved by replacing the high-Q band-pass filter with a gated oscillator and a phase locked loop (PLL), which is added to tune the gated oscillator frequency [12, 13].

Although it solved the integration problem, the architecture still faced some other disadvantages. First, the phase margin between the recovered clock and the delayed data at DFF is not maximal which leads to the degradation of BER performance. This phase margin will further reduce due to variation by process, temperature or even data rate. Second, due to its open loop nature, this architecture has no ability to reject input jitter. Third, in the occurrence of long data stream of identical ONES or ZEROS, the CDR will cease its operation and provide no output. These drawbacks abstain the implementation of this architecture in continuous-mode application such as SONET, Fiber Channel and Gigabit Ethernet which have stringent requirement on jitter performance.

2.4.2 Delay Locked Loop (DLL) based CDR

As the open loop architecture does not have the ability to reject input jitter, a feedback loop is implemented in the DLL to resolve this issue. The general block diagram of a DLL based CDR architecture is shown in Fig. 2.6 [14]. It is formed by two main loops: frequency acquisition loop and delay locked loop. The frequency acquisition loop applied phase locked loop (PLL) architecture to generate clock frequency that is the same as the data rate. The clock is then sent to the input of a voltage control delay loop (VCDL) block in the DLL for phase alignment between the recovered clock and the input data. In DLL, after the phase detector detects the phase difference between the recovered clock and the input data, it sends the information to the charge pump and low pass filter to generate a control voltage for VCDL. This control voltage will then adjust the phase of the clock. The loop continues to track the phase so that the clock is able to sample the data at the optimal point.

Figure 2.6. Block diagram of DLL based CDR

The advantage of this architecture is that it does not have the problem of jitter peaking which solves the jitter accumulation issue. Next, as the VCDL block in DLL controls the phase and not the frequency of the clock, it will not generate an extra pole in the loop transfer function. Hence, the stability of the system is improved. In addition to that, as the clock frequency of DLL based CDR is fixed by the F_{ref} , the phase acquisition time becomes much shorter.

However, this improvement is trade-off with the phase tracking range of the loop. This small phase tracking range leads to a low tolerance towards frequency offset. In source-asynchronous system, this becomes a huge issue as the frequency offset between transmitter and receiver is large due to process, temperature, and supply voltage variation.

2.4.3 Phase Interpolator (PI) based CDR

In order to increase the frequency offset tolerance, the VCDL in DLL based CDR is replaced with a Phase Interpolator (PI). Fig. 2.7 shows the block diagram of a PI based CDR [15-17]. In the frequency acquisition loop, a multi-phase VCO is implemented so that it can be fed to the PI in the phase tracking loop. In the phase tracking loop, both the CP and LPF is replaced by a digital LPF (DLPF) and a current digital to analog converter (I.DAC) respectively. The DLPF and I.DAC will help to adjust the current so that the PI will change the phase of the clock according to the phase difference detected by the PD.

Similar to DLL based CDR, PI based CDR has the same advantage in system stability and shorter lock time. In addition, the frequency offset tolerance is being

widened as compared to DLL based CDR. As for jitter peaking, it will depend on the loop latency. If the loop latency is much larger than the PI phase update period, then when the phase shift control signal reaches the PI, the gradient of the fast changing jitter will be in the opposite direction which leads to jitter peaking [18].

Figure 2.7. Block diagram of PI based CDR

As I.DAC is implemented in this architecture, it has the disadvantage of quantization phase error. Although this quantization phase error can be improved through better I.DAC resolution, it is trade-off with circuit complexity and power consumption. Besides that, this architecture also suffers from cycle-to-cycle jitter which will degrade the jitter performance of the CDR. Moreover, routing of high speed multi-phase clock is also another challenging task for the designer.

2.4.4 Phase Locked Loop (PLL) based CDR

PLL based CDR [19-21] is a more common architecture used in CDR and its general block diagram is shown in Fig. 2.8. The main difference between PLL based CDR

and frequency synthesizer (FS) is that the former removed the frequency divider in the feedback loop so that the clock is being compared directly with the input data. Another difference is that the phase frequency detector (PFD) in FS is replaced with the phase detector (PD), which must have the ability to determine transition of the random input data. The PLL based CDR must also generate a retimed data for the following synchronous process.

Figure 2.8. Block diagram of PLL based CDR

As there is an additional pole at the VCO output of the PLL based CDR, the stability issue has to be taken in as a design consideration. Besides that, the jitter peaking which leads to jitter accumulation is also a disadvantage of this architecture. However, these issues can be minimized through a proper loop filter design. Another concern regarding PLL based CDR is its long phase acquisition time. As the PFD is replaced by a PD, the frequency tracking range is greatly reduced. In order to compensate for this reduction, an additional frequency acquisition loop can be added. Fig. 2.9 shows the dual-loops architecture. The additional loop overcomes the problems of long phase acquisition time and small frequency tracking range.

One of the most important advantages in PLL based CDR is its ability to reject input jitter. With this ability, the jitter of the distorted input data will be improved.

Besides that, with the acquisition loop, the PLL based CDR has a very good ability to track input frequency as compared to other architectures.

Figure 2.9. Block diagram of dual-loops PLL based CDR

2.4.5 Summary of CDR architecture

Table 2.1 shows the comparison between different CDR architectures. Although Injection-Locked based CDR has the advantage in circuit complexity as compare to others CDR architecture, it does not have the ability to reject input jitter due its open loop characteristic. With first order system, the DLL based CDR is more stable and circumvent the problem of jitter peaking. However, it is trade-off with a smaller phase tracking range which will be unacceptable in source-asynchronous system. With Phase-Interpolator based CDR, the phase tracking range is improved. Nevertheless, with the interpolation of clock phases, it has the issues of quatization phase error. As for PLL based CDR, it has a good ability to track input jitter and input frequency. This is highly preferred in

asynchronous source system such as SONET, Ethernet etc as the frequency offset maybe large. Due to all these abilities, this thesis focuses on PLL based CDR design and discusses on technique to minimize the effect of jitter peaking and the long acquisition time.

Table 2.1 Comparison table between CDR architectures.

Architecture	Advantages	Disadvantages
Injection-Locked	<ul style="list-style-type: none">• Simple structure• Shorter acquisition time	<ul style="list-style-type: none">• Quantization phase error• No input jitter rejection
DLL	<ul style="list-style-type: none">• No jitter peaking• More stable (first order system)	<ul style="list-style-type: none">• Smaller phase tracking range• Not feasible in source-asynchronous system
Phase Interpolator	<ul style="list-style-type: none">• Shorter acquisition time• Wider frequency offset tolerance than DLL	<ul style="list-style-type: none">• Quantization phase error• Cycle-to-cycle jitter• Routing of multi-phase clock
PLL	<ul style="list-style-type: none">• Good rejection of input jitter• Good ability to track input frequency	<ul style="list-style-type: none">• Jitter peaking• Long Acquisition time

2.5 Modeling and Analysis of PLL based CDR

PLLs are commonly used in the modern data communication, wireless systems and computer systems. It is implemented with a closed-loop feedback system and it provides a stable clock signal for the other parts of the circuit. The idea of PLL started in the 1930s and has been intensively studied since the 1950s [21]. Throughout these years of research, the basics of PLL have been well-defined. However, as PLL is implemented in different aspect of applications, the focus of each application differs from one another. For example, the design requirements of PLL in clock recovery circuit and frequency synthesizer circuit are different.

Monolithic integration of PLL has also been actively research in the past few decades [22]. With the advancement in CMOS technology, the monolithic integration of the PLL becomes feasible and practical [23-25]. On top of this, the speed of the PLL is also another important aspect of the research. In recent reported PLL [26-28], the speed of the PLL can function upto tens of GHz.

In this section, the basic of PLL and its main parameters will be discussed. The important performance of PLL such as natural frequency, damping factor, loop bandwidth, and locking behavior will also be discussed in the following sections.

2.5.1 PLL Fundamental

Figure 2.10. Block diagram of a basic PLL architecture.

The simplified block diagram of a basic PLL architecture is shown in Fig. 2.10. It is composed of a phase detector, a charge pump, a low pass filter, a voltage controlled oscillator (VCO) and a frequency divider. First, the phase detector will compare the phase difference between the reference frequency, f_{ref} , and the output of the frequency divider, f_{div} . The phase detector will then generate a UP or a DN signal to the charge pump. The pulse-width of the UP signal is proportional to the phase error and the pulse-width of the

DN signal is a constant. The charge pump output will be filtered by a low pass filter whose output is used to control the output frequency of the VCO. The frequency of the VCO output will then be divided by a frequency divider and compared again by the phase detector. This loop will continue to change the frequency of the VCO until both the inputs of the phase detector have the same frequency and a constant phase offset.

2.5.2 PLL Linear Model

Figure 2.11. Linear model of a basic PLL architecture.

When the PLL is around locked condition, it can be analyzed with a linear model shown in Fig. 2.11 [29, 30]. The main function of phase detector is to detect the phase difference between both of its inputs and translates it to voltage outputs. With these voltage outputs, the charge pump will convert them to current output and the amount of current flow is proportional to the phase difference detected by the phase detector. Hence, the combined gain of the phase detector and charge pump, K_{PD-CP} , has unit of A/rad. Although the charge pump current is a step function, it can be approximated as a ramp response [31]. Thus, the function of K_{PD-CP} can be expressed as

$$K_{PD-CP} = \frac{I_p}{2\pi} \quad (2.1)$$

where I_p is the amount of charge pump current.

In a basic PLL system, the low pass filter (LPF) can be implemented with just a capacitor. Hence, the transfer function of the LPF, $F_{LPF}(s)$, is just the Laplace transform of the capacitor which is given by

$$F_{LPF}(s) = \frac{1}{sC_s} \quad (2.2)$$

where C_s is the capacitance value and s is the Laplace transform parameter.

As for an ideal VCO, the output radian frequency, ω_{out} (rad/s), is linearly proportional to the control voltage (V_C) and can be written as

$$\omega_{out} = \omega_o + K_{VCO} \cdot V_C \quad (2.3)$$

where ω_o is the free running radian frequency and K_{VCO} is the gain of the VCO (rad/s/V). The radian frequency is the derivative of phase, thus the function of VCO can be expressed as

$$\frac{d\Phi_{out}(t)}{dt} = K_{VCO} \cdot V_C(t) \quad (2.4)$$

where $\Phi_{out}(t)$ is the output phase. Laplace transform Eq. (2.4), we will have

$$\Phi_{out}(s) = \frac{K_{VCO} \cdot V_C(s)}{s} \quad (2.5)$$

Hence, the transfer function of the VCO can be expressed as

$$\frac{\Phi_{out}(s)}{V_C(s)} = \frac{K_{VCO}}{s} \quad (2.6)$$

As the frequency divider is just to divide the input frequency by N , the transfer function of frequency divider in s-domain will be $1/N$.

From Fig. 2.11, through multiplying all the blocks, the open loop gain of the system can be written as

$$H_{open}(s) = \frac{K_{PD-CP} F_{LPF}(s) K_{VCO}}{sN} \quad (2.7)$$

Substituting Eq. (2.1), Eq. (2.2) and Eq. (2.6) into Eq. (2.7), the open loop gain of the system can be rewrite as

$$H_{open}(s) = \frac{I_P K_{VCO}}{2\pi N C_s} \cdot \frac{1}{s^2}. \quad (2.8)$$

The closed loop transfer function of the system is then expressed as

$$H_{closed}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\frac{I_P K_{VCO}}{2\pi C_s} \cdot \frac{1}{s^2}}{1 + \frac{I_P K_{VCO}}{2\pi N C_s} \cdot \frac{1}{s^2}} \quad (2.9)$$

$$\Rightarrow H_{closed}(s) = \frac{\frac{I_P K_{VCO}}{2\pi N C_s}}{s^2 + \frac{I_P K_{VCO}}{2\pi N C_s}}. \quad (2.10)$$

In Eq. (2.10), the two poles of the closed-loop PLL system can be expressed as

$$s = \pm j \sqrt{\frac{I_P K_{VCO}}{2\pi N C_s}}. \quad (2.11)$$

Due to the location of these two imaginary poles at the origin, the system exhibits stability issue as it has a phase shift of 180° . To resolve the stability issue, a resistor is connected in series with the capacitor to generate a zero in the transfer function shown in Fig. 2.12(b). The transfer function of the LPF can then be expressed as

$$F_{LPF}(s) = R_s + \frac{1}{sC_s}. \quad (2.12)$$

By substituting Eq. (2.12) into Eq. (2.7), the closed-loop transfer function of the PLL system can then be expressed as

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\frac{I_P K_{VCO}}{2\pi N C_s} (sR_s C_s + 1)}{s^2 + \frac{I_P K_{VCO} R_s}{2\pi N} s + \frac{I_P K_{VCO}}{2\pi N C_s}}. \quad (2.13)$$

Figure 2.12. Loop filter with (a) a simple capacitor, (b) a stabilizing resistor, (c) a ripple filtering capacitor.

Although the series resistor can resolve the stability issue, it is compromised with an increase in the ripple level for the control voltage of the VCO. This increase in ripple is mainly due to the change of voltage across the resistor. When there is a current flowing into the LPF, there will be an increase in voltage and the amount of increase is given as

$$\Delta V = I_P \cdot R_s. \quad (2.14)$$

For the case of current flowing out of the LPF, a similar voltage change exists. This ripple in the VCO control voltage will greatly deteriorate the output phase which can be translated into jitter. So to compensate for the ripple effect, an additional capacitor, C_p , is connected in parallel with R_s and C_s and it is shown in Fig. 2.12(c) [32].

With this additional C_p , the open loop transfer function can be expressed as

$$H_{open}(s) = \frac{I_p K_{VCO}}{2\pi N} \cdot \frac{1}{C_p s^2} \cdot \frac{s + \frac{1}{R_s C_s}}{s + \frac{1}{R_s \cdot (\frac{C_s C_p}{C_s + C_p})}}. \quad (2.15)$$

The bode plot of this open-loop transfer function is shown in Fig. 2.13. The phase margin, Φ_M , can then be expressed as

$$\Phi_M = \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_{UGB}}{\omega_{p3}}\right). \quad (2.16)$$

where ω_{UGB} is the radian frequency of unity gain bandwidth, ω_{UGB} is the radian frequency of the zero and ω_{p3} is the radian frequency of the third pole.

Figure 2.13. Bode plot of the open-loop transfer function.

With some mathematical calculation shown in [29], the phase margin can be expressed in terms of C_s and C_p ,

$$\Phi_M = \tan^{-1} \sqrt{\frac{C_s}{C_p} + 1} - \tan^{-1} \frac{1}{\sqrt{\frac{C_s}{C_p} + 1}}. \quad (2.17)$$

By rearranging Eq. (2.17), C_s can be expressed in terms of C_p and Φ_M ,

$$C_s = 2C_p \left(\tan^2 \Phi_M + \tan \Phi_M \sqrt{\tan^2 \Phi_M + 1} \right). \quad (2.18)$$

Hence, for a given phase margin, the ratio between C_s and C_p is fixed. There is only one degree of freedom to choose between C_s and C_p .

2.5.3 Natural Frequency and Damping Factor

To inspect the two basic loop parameters, natural frequency and damping factor, Eq. (2.13) can be used if $C_p \ll C_s$. These two parameters can be found by comparing Eq. (2.13) with a well-known equation implemented in control theory as shown

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{2\delta\omega_n s + \omega_n^2}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (2.19)$$

where ω_n is the natural frequency of the system and δ is the damping factor. Hence, ω_n and δ can be expressed as

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi N C_s}} \quad (2.20)$$

and

$$\delta = \frac{R_s}{2} \sqrt{\frac{I_p K_{VCO}}{2\pi N} \cdot C_s} \quad (2.21)$$

respectively.

From Eq. (2.19), the two poles of the closed-loop system can be expressed as

$$s_{1,2} = \omega_n \left(-\delta \pm \sqrt{\delta^2 - 1} \right). \quad (2.22)$$

For an over-damped system, $\delta > 1$, it will have two real poles. The transient response of the system consists of two time constants: $1/s_1$ and $1/s_2$. However, for an under-damped system, $\delta < 1$, overshoot will occur and it will oscillate within a decaying envelope. The critically-damped system occurs when $\delta = 1$. Fig. 2.14 shows the transient response of the closed-loop system under three different damping conditions.

Figure 2.14. Transient response of V_C under different damping conditions.

2.5.4 Loop Bandwidth

The loop bandwidth can be obtained by finding the -3-dB frequency which is $s_B = j\omega_B$, where ω_B is the loop bandwidth. Hence, it can be expressed as

$$\left| \frac{2\delta\omega_n s_B + \omega_n^2}{s_B^2 + 2\delta\omega_n s_B + \omega_n^2} \right| = \frac{1}{\sqrt{2}}. \quad (2.23)$$

By setting $s_B = j\omega_B$, we have

$$\frac{4\delta^2\omega_n^2\omega_B^2 + \omega_n^2}{(\omega_n^2 + \omega_B^2)^2 + (2\delta\omega_n\omega_B)^2} = \frac{1}{2}. \quad (2.24)$$

By rearranging Eq. (2.24), we obtained

$$\omega_B^4 - 4\omega_n^2(2\delta^2 + 1)\omega_B^2 - \omega_n^4 = 0. \quad (2.25)$$

Hence, the loop bandwidth is expressed as

$$\omega_B^2 = \left[(2\delta^2 + 1) + \sqrt{(2\delta^2 + 1)^2 + 4} \right] \cdot \omega_n^2. \quad (2.26)$$

From Eq. (2.26), the loop bandwidth can be changed by changing either ω_n or δ .

However, in a narrow loop bandwidth requirement, the δ cannot be set lower than $1/\sqrt{2}$ as this may induce stability problem. Hence, narrow loop bandwidth can only be achieved by reducing ω_n . From Eq. (2.20) and Eq. (2.21), both I_p and K_{VCO} cannot be reduced further as they will also reduce δ . Thus, narrow loop bandwidth can only be achieved by increasing the value of C_s . In Gb/s CDR system, the loop bandwidth is between the range of hundreds-kHz to tens-MHz [33-35].

2.5.5 Locking Behavior

The two basic parameters for the locking behavior of PLL are its lock range and capture range. The lock range is defined as the range of frequency in which the PLL can remain in lock condition. It is also often known as the tracking range. The capture range is defined as the range of frequency in which the PLL can acquire lock condition. It is

also often known as acquisition range. For Gb/s CDR system, both the lock range and capture range will be in the range of a few-MHz to hundreds-MHz [36-38]. The required time for the CDR to lock, locking time, will be in the range of hundreds-ns to tens- μ s [39-42].

Figure 2.15. Lock range and capture range of PLL architecture.

To illustrate both the lock range and capture range, Fig. 2.15 shows the frequency-to-voltage characteristic of a PLL [43]. The horizontal axis represents the input frequency and the vertical axis represents the loop-error voltage. For the upper diagram, the input frequency is slowly increased. When the input frequency reaches f_1 , the loop locked the input signal and caused a negative value for the loop-error voltage. As the input frequency continues to increase, the loop-error voltage will continue to increase. The lock condition continues until the input frequency is larger than f_2 . Hence, the lock range can be expressed as

$$\Delta f_L = f_2 - f_o \quad (2.27)$$

and the capture range can be expressed as

$$\Delta f_c = f_o - f_1. \quad (2.28)$$

Moving backwards, when the input frequency is slowly decreased, the first frequency, f_3 , which causes the loop to lock, is used for lock range calculation and the second frequency, f_4 , which causes the loop to be out-of-lock, is used for capture range calculation. In general, the lock range is greater or equal to the capture range.

From Eq. (2.19), we can also observe that when an additional static phase error is gradually added to the input, the output phase will follow this addition in static phase error. On the other hand, when the additional static phase error is hastily added to the input, the output phase will not follow this addition in static phase error. Especially when the speed of change in the additional static phase error is close to zero, $s \approx 0$, the transfer function $H(s)$ will be close to one. Hence, the PLL acts like a low pass filter to the additional static phase error.

2.6 Introduction to D-latch and D-flip-flop

This section discusses on the operation of two important blocks, D-latch and D-flip-flop (D-FF), which will be frequently used in this Thesis. The block diagram of a basic D-latch is shown in Fig. 2.16(a) which consists of an input data signal, D_{in} , a clock signal, CLK, and an output data signal, Q. The D-latch is triggered by CLK signal and is known as a level triggered device. Whenever CLK signal is *high*, the output will follow the input. This period is called the reading period and is shadowed with grey boxes in Fig. 2.16(b). Whenever CLK signal is *low*, the output will hold on to the previous input data

until CLK signal changes to *high*. This period is called the latching period. Due to its characteristic, it can be implemented as a temporary buffer.

Figure 2.16 (a) Block diagram and (b) timing diagrams of D-latch.

D-FF is slightly different from D-latch as it is an edge triggered device. It is only active at the edge of the CLK signal and can be generally separated into two main types, rising edge triggered and falling edge triggered. For a rising edge triggered D-FF shown in Fig. 2.17(a), it will only read in input data, D_{in} , at the rising edge of the CLK. Vice versa, the falling edge triggered D-FF will only read in input data at the falling edge of the CLK. The timing diagram of the rising edge triggered D-FF is shown in Fig. 2.17(b). With this characteristic, D-FF can be implemented as a register.

Figure 2.17 (a) Block diagram and (b) timing diagrams of D-FF.

3 Literature Review of Phase Detector

Recently, researchers have endeavoured to design high speed low power PD in CMOS process as CDR performance depends greatly on the characteristic of PD. There are two primary types of PD used in PLL-based CDR architecture, linear PD and binary PD. Due to a continuous increase in the data rate, half-rate, quarter-rate and 1/8-rate PD have also been reported.

Unlike sequential phase detector (PD) in PLL circuit, the PD in CDR circuit not only detects the phase difference between two inputs but also the data transition as the transfer of data in a serial-link data communication system is not periodic. Hence, the design of PD for CDR is much more complicated than normal PD as additional information such as data transition, is required. The literature review on some eminent PDs will be discussed in the following sections.

3.1 Linear Phase Detector

Hogge's phase detector [44] is the classic representation of full rate linear phase detector and its block diagram is shown in Fig. 3.1. It is one of the simplest PD because it only composes two D-flip-flops (D-FFs) and two Exclusive-OR (XOR) gates. Its operation is illustrated by the timing diagrams shown in Fig. 3.2. The first D-FF will sample input data, D_{in} , with full-rate clock and then both its input and output is compared with an XOR gate. The output of this XOR gate, UP, comprises information on the phase difference between D_{in} and clock. Its pulse-width will vary according to the phase

difference which means that its pulse-width increases when the phase difference increase.

Due to this linear property, it is called a linear PD.

Figure 3.1 Block diagram of Hogge's phase detector.

Besides having the ability to determine phase differences, the PD is also required to determine input data transition. From the timing diagrams, the UP signal will only be high when there is a data transition and the average output voltage for the UP pulse is dependent on the data transition density. However, this dependency on the data transition density can cause a false lock if no additional information is given. For example, if the input phase difference is decreased by a factor of two and the data transition density is increased by a similar amount, then the average output voltage of the UP signal will remain the same.

Figure 3.2 Timing diagrams of Hogge's phase detector.

To avert from false lock, an additional signal, DN, is inserted to resolve the dependency of the PD on the input data transition density issue. It is accomplished through connecting the first D-FF output to another D-FF, which is clocked with the opposite clock phase. Through this, the pulse of the DN signal will only appear when there is a data transition and its pulse-width is independent of the data pattern, i.e. half of the clock period for Hogge's PD. If the input data transition density increases, the average output voltage of the DN signal will also increase. Hence, the DN signal helps to store the information on input data transition density.

When the PD locked D_{in} , the rising edge of the clock is required to be at the mid point of each bit to provide a better phase margin for the digital signal processing. The timing diagram shown in Fig. 3.3 is for the situation when the PD locked D_{in} . At this condition, both the UP and the DN signals have the same pulse-width and engender the average control voltage, V_C , of the voltage controlled oscillator (VCO) to remain unchanged. In addition to that, the retimed data can also be directly extracted from Q_1 which changes at the rising edge of the clock.

Figure 3.3 Timing diagrams of Hogge's phase detector under lock condition.

In designing Hogge's PD, there are a few drawbacks that need to take note of. First, in the real world there is a finite delay for D-FF, T_{delay} , and this delay will contribute to an increase in the UP pulse-width by T_{delay} . As a result, a phase offset is introduced. In high speed design, the phase offset becomes more significant due to a reduction in the UP pulse-width. To resolve this problem, an additional delay block, T_{delay} , is inserted to decrease the DN pulse-width [44] or increase the UP pulse-width [45]. However, the implementation of accurate delay block in high speed design is a tough task as it is affected by process variation and device mismatch.

Second, under locked condition, both the UP and DN pulse-widths occupied half of each clock period respectively. This induces a half period skew between the UP and the DN signals to the V_C of the VCO. This can be further explained as follow; the charge pump current will flow into the LPF for the first period when the UP signal is *high* and flow out from the LPF for the second period when the DN signal is *high*. This causes the control voltage, V_C , of the VCO to become a triangle wave whenever there is data transition, as shown in Fig. 3.3. This increase and decrease in V_C will translate as the phase noise of the VCO and further seen as an additional jitter to the CDR system. To ameliorate this issue, a few more stages can be inserted which is reported in [46].

3.2 Binary Phase Detector

Alexander's phase detector [47] shown in Fig. 3.4 is a classic representation of a full rate binary phase detector. It is composed of four D-FFs and two XOR gates and uses

three-point sampling to determine whether the clock leads or lags the data. It is also known as an early-late PD.

Figure 3.4 Block diagram of Alexander's phase detector.

Fig. 3.5(a) shows two possible conditions, clock leads data and clock lags data. For the case of clock lags data, the three point sampling has to satisfy the condition $Q_1 = Q_2 \neq Q_3$. On the other hand, for the case of clock leads data, the three point sampling has to satisfy the condition $Q_1 \neq Q_2 = Q_3$. If no data transition is detected, then the three point sampling has to satisfy the condition $Q_1 = Q_2 = Q_3$. From the above observations, if $Q_1 \oplus Q_2$ is *high*, clock leads data. If $Q_2 \oplus Q_3$ is *high*, clock lags data. However, if both $Q_1 \oplus Q_2$ and $Q_2 \oplus Q_3$ are *low*, that represents no data transition. In summary, the $UP = Q_2 \oplus Q_3$ signal is used to represent clock lags, and the $DN = Q_1 \oplus Q_2$ signal is used to represent clock leads. Fig. 3.5(b) is an example when clock lags data. The retimed data can directly be extracted from Q_3 just like in the linear PD.

Under locked condition, Q_1 and Q_3 will be at the middle of each bit, and Q_2 will be around the transition edge of the data. At this condition, the switching activity of the charge pump will be high as it is switching between clock leads and lags. Hence, it has a very high gain in the vicinity of locked condition. However, this high gain at locked condition creates ripples in V_C which result in a significant jitter at the output of the VCO [45]. Another issue is that under locked condition, FF_3 samples at the transition of the data, causing FF_3 - FF_4 pair to enter meta-stable state [48].

Figure 3.5 (a) Three points sampling and (b) timing diagrams of Alexander's phase detector.

3.3 Comparison between Linear and Binary Phase Detector

Fig. 3.6 shows the characteristic curves of linear PD and binary PD. From Fig. 3.6(a), the average UP signal voltage of a linear PD varies linearly with the phase difference and hence it has a linear gain characteristic. On the other hand, the binary PD (Fig. 3.6(b)) only has a binary UP signal voltage with one representing the clock lags and zero representing the clock leads. This leads to a high phase gain characteristic for binary PD when the phase difference is closed to zero.

Figure 3.6 Characteristic curves of (a) linear PD, and (b) binary PD.

Due to a linear gain characteristic, the linear PD has an advantage in jitter generation as compared to the binary PD. At the locking state, the gain of the linear PD is close to zero and the gain of the binary PD is close to infinity. This leads to a smaller fluctuation in the control voltage, V_C , of the linear PD and a larger fluctuation in V_C of the binary PD. As the fluctuation of V_C will translate into a jitter, the jitter generation for linear PD will be much lesser than that for binary PD.

The advantage of binary PD is that it is much easier to implement as compared to linear PD. This is mainly because binary PD only needs to check whether the clock leads

or lags the input data. It does not need to provide information on the value of the phase difference. The phase difference information will become harder to extract as the data rate is increased. On the other hand, due to this non-linearity property of the binary PD, the analysis of binary CDR system will be much more complicated than linear CDR system [49].

Table 3.1 shows the comparison between linear PD and binary PD. In serial-link communication, the jitter requirement for CDR is very stringent. As linear PD has the advantage of in-lock jitter performance and it can be modeled by a matured loop theory, in the following sections, we will be focusing on linear PD instead of binary PD.

Table 3.1 Comparison between linear PD and binary PD.

	Linear PD	Binary PD
Advantages	<ul style="list-style-type: none">• Linear gain characteristic• Smaller jitter generation	<ul style="list-style-type: none">• High phase gain• Easier to implement
Disadvantages	<ul style="list-style-type: none">• Suffers bandwidth limitation• Static phase offset due to mismatch	<ul style="list-style-type: none">• Larger jitter generation• Static phase offset due to sampling apertures error

3.4 Half-rate Linear Phase Detector

When the data rate increases to a very high speed, full-rate PD becomes malfunction or has reliability problem. Furthermore, at such a high speed, it becomes a big challenge to design the VCO with sufficient tuning range and acceptable jitter. In order to ease the speed requirement of the PD, the reported PD [50] uses a slower clock.

A half-rate linear phase detector shown in Fig. 3.7 uses a clock frequency which is half of the input data rate. It is composed of four D-latches and two XOR gates.

Figure 3.7 Block diagram of J. Savoj's half-rate linear PD.

Fig. 3.8 shows the timing diagrams of the reported half-rate linear PD under locked condition. First, D_{in} is latched by L_1 and L_2 through the clock and its complement. By XORing Q_1 and Q_2 , $Q_1 \oplus Q_2$, it provides the information of the phase difference between the clock and D_{in} . Its pulse-width is directly proportional to the phase difference and hence is set to be the UP signal. As for the reference signal, it can be generated by sampling D_{in} at different edges of the clock. Q_3 is being sampled at the falling edge of the clock and Q_4 is at the rising edge of the clock. Through this, the reference signal, DN, is equal to $Q_3 \oplus Q_4$. Whenever there is data transition, DN will have a pulse-width equal to half of the clock period as shown in Fig. 3.8.

Besides having the advantage of easing speed requirement of the PD, half-rate PDs also have a higher capture range. By multiplexing the outputs of Q_3 and Q_4 , the retimed data, D_{out} , can be extracted. However, one of the drawbacks of this architecture is the deviation of clock duty cycle. This deviation will translate to bimodal jitter. Hence, extra care is needed to ensure the symmetry in layout for clock duty cycle minimization. Besides deviation of clock duty cycle, the reported PD also has another concern. When the phase difference is small, the pulse-width of the UP signal will also be small. This small UP pulse-width is an issue when the data rate continues to increase because the circuit bandwidth limits the performance. In the next section, the reported PD will resolve the issue of small UP pulse-width.

Figure 3.8 Timing diagrams of J. Savoj's half-rate linear PD.

3.5 Half-rate Linear Phase Detector with UP Pulse Widening

When the speed of PD becomes very high, the very narrow generated UP pulses becomes a bottleneck of the circuit. UP pulse widening [51] is a technique reported to resolve this issue. For UP pulse widening, a constant pulse-width will be inserted, i.e. one

data period for this architecture. Due to the insertion of constant pulse-width, one UP signal will not be able to detect all the data transitions. An additional UP signal is introduced. The block diagram of the reported PD architecture is shown in Fig. 3.9(a). It consists of four latches, three XOR gates and two AND gates. The connection of latches is similar to previous half-rate linear PD. However, the extraction of the UP and DN signals are different.

From Fig. 3.9(b), UP₁ detects the transition edge of the even data by connecting Q₂, Q₃ to XOR gate and UP₂ detects the transition edge of the odd data by connecting Q₁, Q₄ to XOR gate. To detect DN, the connection is similar to the previous PD. However, in order to have two pairs of UP and DN signals, the DN signal is further separated into two signals DN₁ and DN₂. DN₁ is generated by connecting DN and the clock's complement to an AND gate and DN₂ is generated by connecting DN and the clock to another AND gate.

Under locked condition, the UP pulse-width is $3/2$ times of the data period, $3T/2$, and the DN pulse-width is one data period, T . In designing the overall CDR system, an unbalanced charge pump is applied to correct this difference. Although the UP pulse-width has been widened, the gap between the pulses has been reduced. Hence, UP pulse widening will only gain advantage when no data edge is detected.

(a)

(b)

Figure 3.9 (a) Block diagram and (b) timing diagrams of Y. Ohtomo's half-rate linear PD.

3.6 Quarter-rate Linear Phase Detector

In order to further reduce the clock rate, a quarter-rate linear phase detector has been reported [52] recently. The block diagram of the reported PD is shown in Fig. 3.10

and it consists of four D-latches, six MUXs, and three XOR gates. The input data is first latched by a four phase clock and these outputs are multiplexed by clocks to produce M_1 to M_6 . This architecture generates two error signals: UP_1 and UP_2 , which they are given by $UP_1 = M_1 \oplus M_3$ and $UP_2 = M_2 \oplus M_4$. The reference signal, $DN = M_5 \oplus M_6$, has a pulse-width equal to one data period.

Figure 3.10 Block diagram of M. Saffari's quarter-rate linear PD.

Figure 3.11 Timing diagrams of M. Saffari's quarter-rate linear PD.

Fig. 3.11 shows the timing diagrams of the reported PD. Under locked condition, the UP pulse-width will be half of the data period and DN pulse-width will be one data period. This unbalance between UP and DN pulse-width at locked condition is compensated through implementing the XOR gate topology reported in [53]. The DN pulse-width is doubled that of the UP pulse-width. In order to achieve compensation, the

current in the XOR gates for the UP signal has to be doubled the current in the XOR gate for the DN signal.

As the UP pulse-width remain as half of the data period, very short UP pulses becomes a drawback in the speed limit. In addition to that, although the clock rate is decreased, the outputs of the latches still have small pulse-width. Hence, the bandwidth requirement for the latches are still very high.

3.7 Quarter-rate Linear Phase Detector with UP Pulse Widening

Figure 3.12 Block diagram of S. Byun's quarter-rate linear PD.

To further ease the speed requirement imposed on the PD, a quarter-rate PD with UP pulse widening has been reported in [54]. The block diagram of this architecture is shown in Fig. 3.12. It consists of four D-latches, four XOR gates and eight AND gates. In

this design, D_{in} is latched by a four phase clock and the adjacent outputs of the latches are passed through XOR gates. These outputs are then passed through AND gates to extract the required UP and DN signals. For this architecture, four pairs of UP, DN signals are extracted.

Figure 3.13 Timing diagrams of S. Byun's quarter-rate linear PD.

The timing diagrams for this architecture are shown in Fig. 3.13. Under locked condition, the UP pulse-width is $3/2$ times the data period and the DN pulse-width is one data period. It resolves the problem of small UP pulse-width and the UP signal is now separated into four parts. Although there are still a few small pulses on the signals Q_1 to Q_8 , they can be neglected as they will be filtered by the following AND gates. Hence, the D-latches and XOR gates do not have stringent speed requirement. Due to the ease of speed requirement, the supply voltage of the circuit can be reduced.

Although this architecture relaxes on speed requirement, there are a few issues to take note. First, the circuit complexity increases significantly. This increase in complexity will cause an increase in the power consumption as more blocks are implemented and may supersede the reduction of power consumption due to the reduction in supply voltage. Second, with consideration of propagation delay, the misalignment of the clock will deteriorate the UP and DN pulse-width. By inserting a clock tree [54] design, misalignment problem can be greatly reduced. However, this will cause circuit complexity to further increase and induce an increase in power consumption. Third, the reported PD has four pairs of UP and DN signals. With these additional pairs of UP and DN signals, more charge pump blocks will be needed. This will lead to a severe mismatch in the charge pump circuit.

3.8 Comparison & Summary

This chapter provides a literature review on the architecture of PD. Two important types of PD, linear and binary, are described and compared. From the comparison, binary

PD is simpler to implement as it only provides information on whether clock leads or lags input data. However, linear PD has to provide the information on the phase difference between input data and clock. On the other hand, the simplicity of binary PD is trade-off with an increase in jitter generation which is an advantage for linear PD. Due to the jitter requirement set by SONET and Ethernet, this work focuses on linear PDs.

Table 3.2. Performance comparison of the reported PDs.

	[44]	[47]	[50]	[51]	[52]	[54]
Technology	-	-	0.18- μ m	0.13- μ m	0.18- μ m	0.13- μ m
Data Rate	565-Mb/s	-	10-Gb/s	12.5-Gb/s	4-Gb/s	10-Gb/s
Type of PD	Linear	Binary	Linear	Linear	Linear	Linear
Supply	-	-	2.5-V	1.5-V	1.8-V	1.2-V
Rate of PD	Full rate	Full rate	1/2 rate	1/2 rate	1/4 rate	1/4 rate
Power Diss.	-	-	-	-	28.8-mW	74.4-mW ^b
Power per Gb/s	-	-	-	-	7.2-mW	7.44-mW ^b
Building Blocks	2 D-FFs ^a 2 XOR gates	4 D-FFs ^a 2 XOR gates	4 Latches 2 XOR gates 1 MUX cells	4 Latches 3 XOR gates 2 AND gates	4 Latches 6 MUX cells 3 XOR gates	4 Latches 8 AND gates 3 XOR gates
Output Signals	1 UP pulse 1 DN pulse	1 UP pulse 1 DN pulse	1 UP pulse 1 DN pulse	2 UP pulses 1 DN pulse	2 UP pulses 1 DN pulse	4 UP pulses 4 DN pulses
UP-pulse widening	No	No	No	Yes	No	Yes

^a A D-FF is composed by 2 D-latches

^b Includes charge pump power consumption

Table 3.2 summarizes and compares all the PDs discussed in this chapter. The first two columns show the full-rate linear and binary PD. In term of their complexity, the binary PD has two additional D-FFs as compared to linear PD. As the rate of linear PD decreases to half-rate and quarter-rate, the complexity of the PD increases. However, this increase in complexity enables the PDs to function at Gb/s range. As for the PDs that implement UP-pulse widening technique, their complexity and output signals increase.

However, this increase in complexity and output signals enable the PDs to function at a higher data rate.

4 The Proposed Phase Detector

In this chapter, we will be focusing on designing a linear PD as it has a superior performance on jitter as compared to binary PD. As discussed in the previous chapter, when the clock rate of the linear PD decreases, the complexity of the circuit will increase. This work endeavours to reduce the circuit complexity of quarter-rate linear PD. Besides that, this work preserves the UP pulse-widening technique to resolve the issue of small UP pulse-width. On top of that, this work also reduces the number of output signals of the PD as more pairs of output signals will deteriorate the current mismatch of the charge pump.

4.1 The Proposed Quarter-rate Linear Phase Detector Architecture

Figure 4.1 Block diagram of the proposed quarter-rate linear PD.

The architecture of the proposed PD is shown in Fig. 4.1. It consists of 4 D-latches, 4 MUXs and 3 XOR gates. The input data, D_{in} , is latched by four phase clock, CLK0, CLK90, CLK180, CLK270 and outputted Q_1 , Q_2 , Q_3 , Q_4 . These four latch outputs are further multiplexed with CLK0 and CLK90 to give output signals M_1 , M_2 , M_3 , and M_4 . At the last stage, (M_1, M_2) and (M_3, M_4) passes through XOR gates to give UP_1 and UP_2 respectively. DN is generated by XORing M_1 and M_4 .

Figure 4.2. Timing diagrams of the proposed PD architecture.

The timing diagrams of the proposed PD are shown in Fig. 4.2. If the period of D_{in} is T_{period} , then the period of the clock is four times T_{period} . In the locking state, clock samples are at the middle of D_{in} . This implies that the phase difference between D_{in} and clock is half of T_{period} . The UP pulse-width consists of two parts: a phase difference, T_{phase} , and a constant fixed pulse-width equal to T_{period} . Hence, the UP pulse-width is equal to $T_{phase} + T_{period}$. It varies linearly with respect to T_{phase} and ranges from T_{period} to $2 T_{period}$. Due to the small increment in the UP pulse-width, a single UP signal is not able to detect all the changes in D_{in} . Hence, another UP signal is added to assist in detecting all D_{in} changes. Both the UP_1 and UP_2 signals detect different set of D_{in} pairs as shown in Fig. 4.2, i.e. UP_1 detects the changes between data (1 and 2), (3 and 4), and so on while UP_2 detects the changes between data (2 and 3), (4 and 5), and so on. As for DN, it can detect all the changes in D_{in} and its pulse-width increases from normal width of $0.5T_{period}$ to T_{period} .

There are several features and advantages of the proposed PD. First, it has a simple architecture and the least number of building blocks among all the reported quarter-rate linear PD [52, 54, 55]. It consumes very low power because the clock tree design implemented in [54], which helps to phase align the clock, is not being implemented here. So, the propagation delay will be critical and it will be analyzed in detail in the next section.

Second, a new UP pulse-widening technique is implemented which overcomes the problems of having narrow UP pulses when the phase difference is very small. As shown in Fig. 4.2, a wide UP pulse will reduce the UP pulse gap. In contrast to narrow UP

pulses, short UP pulse gaps will not happen in every data transition because D_{in} is random data or pseudorandom binary sequence (PRBS) signal. In addition, UP pulse gaps are large as they are fixed around half of the data period at locking state.

Third, beside UP pulse widening, the DN pulse-width is also made wider from $0.5T_{period}$ to T_{period} . With an extended DN pulse-width, the switching of DN signal is reduced so it will not need to switch at every data transition. If D_{in} has a switching activity equal to one, DN will output a constant high instead of switching between high and low. This will further reduce the current mismatch in charge pump due to input switching.

4.2 Analysis of the Proposed PD

As the proposed PD does not use clock tree [54] to achieve low power design, the analysis of propagation delay becomes critical. For the first time, this section provides equations to predict the characteristic curve and analyzes the changes in the UP and DN pulse-widths due to variations in the propagation delay for various phase differences. In this analysis, the propagation delay of D-latch with respect to its input and clock are represented by $T_{I/Q(latch)}$ and $T_{C/Q(latch)}$ respectively. Similarly, $T_{I/Q(MUX)}$ and $T_{C/Q(MUX)}$ are the propagation delay of MUX with respect to its input and clock. $T_{D(XOR)}$ is the propagation delay of the XOR gate.

Figure 4.3. Timing diagrams of the proposed PD with design considerations of propagation delay.

Fig. 4.3 shows the timing diagrams of the proposed PD taking into account the design considerations of propagation delay. The additional delay on the rising edge of UP pulse, T_{r_UP} , is given by

$$T_{r_UP} = T_{I/Q(latch)} + T_{I/Q(MUX)} + T_{D(XOR)} \quad (4.1)$$

and the additional delay on the falling edge of the UP pulse, T_{f_UP} , is given by

$$T_{f_UP} = T_{C/Q(MUX)} + T_{D(XOR)} \quad (4.2)$$

Hence, the pulse-width of the UP signal varies according to the difference between T_{r_UP} and T_{f_UP} and it can be modeled as

$$T_{UP} = T_{period} + T_{phase} + T_{f_UP} - T_{r_UP} \quad (4.3)$$

$$\Rightarrow T_{UP} = T_{period} + T_{phase} + T_{C/Q(MUX)} - T_{I/Q(latch)} - T_{I/Q(MUX)} \quad (4.4)$$

where T_{period} is the period of D_{in} and T_{phase} is the phase difference between the input and clock. The first term in T_{UP} , T_{period} , is the constant pulse-width added to the UP signal for pulse-widening. If T_{r_UP} is larger than T_{f_UP} , the width of the UP pulse will decrease which leads to an increase in the UP pulse gap. As for the DN signal, the additional delays on both edges are the same so its pulse width remains unchanged and can be modeled as

$$T_{DN} = T_{period} \quad (4.5)$$

Thus, the UP/DN ratio changes with respect to the width of the UP pulse.

Fig. 4.4(a) shows the simulated characteristic curve of the proposed PD where the UP pulse-width is divided by the UP/DN ratio. By using Eq. (4.4) and Eq. (4.5), the predicted characteristic curve is plotted with the symbols of triangle and circle for the UP and DN pulses, respectively. Fig. 4.4(b) shows the percentage error between simulated and predicted pulse-width. From the result, the characteristic curve can be categorized

(a)

(b)

Figure 4.4. (a) Simulated and predicted characteristic curves of the proposed PD and (b) the percentage error between simulated and predicted UP/DN pulse-width.

into four regions. For the first region, as the phase difference becomes smaller than the hold time of the latch, it does not have enough time to read in the input data, D_{in} , causing the circuit to be in meta-stable state (Region 1). In this meta-stable region, the simulated UP and DN pulse-widths have significant dips as compared to the predicted UP and DN pulse-widths. It also has the largest percentage error. It is preferred that this region is far away from the crossover point of UP and DN pulses so that there is a larger phase margin available for the next stage.

Next, as the phase difference continues to increase beyond the meta-stable region, the simulated UP/DN pulse-widths are still shorter than the predicted UP/DN pulse-widths. In this region, the percentage errors in the width of the UP and DN pulses are less than 10%. Fig. 4.5 shows the timing diagrams of the proposed PD in this region. The dotted line represents the original output and the solid line represents the output caused by the increase in propagation delay. To further analyze the propagation delay, the delay model in [56] is used and is shown below,

$$T_{delay} = k_{RC} \cdot \frac{\Delta V_{SWING}}{\Delta I_{SWING}} \cdot C_{total} + \frac{\tau}{2} \min\left(\frac{V_{eff}}{\Delta V_{in}}, 1\right) \quad (4.6)$$

where k_{RC} is a constant that depends on the input data rate and time constant of the system, ΔV_{SWING} is the single-ended voltage swing at output, ΔI_{SWING} is the single-ended current swing at one of the loads, C_{total} is the effective capacitance at the output node, τ is the rise time of the input, V_{eff} is the sum of the over-drive voltage of the differential pair transistors, ΔV_{in} is the input voltage swing and “min” is the function that selects the minimum value between the two. Both $T_{I/Q}$ and $T_{C/Q}$ can be approximated by using Eq. (4.6).

Figure 4.5. Timing diagrams of the proposed PD when T_{phase} is small.

In this region, there are generally two main reasons that cause the increase in delay. First, it is mainly due to the latch. It changes from reading to latching state while its output is still in transition. This can be approximated as a decrease in current flowing through its input source-coupled pair, ΔI_{SWING} , and the amount of decrease vary with the phase difference. From Eq. (4.6), a decrease in ΔI_{SWING} will lead to an increase in $T_{I/Q(latch)}$, and hence an increase in rise/fall time of the output. Furthermore, $T_{I/Q(MUX)}$ of the next stage will also increase, as the rise/fall time, τ , of input is increased. Second, it is

due to the close edges between the clock and input of MUX. At the edge of the clock, the bias current of MUX will steer its current from one source-coupled pair to another. The steering of current starts while the input of MUX is still in transition. As a result, $T_{C/Q(MUX)}$ is increased. In summary, the change of $T_{I/Q(MUX)}$, $\Delta T_{I/Q(MUX)}$, affects the rising edge of the UP pulse while the change of $T_{C/Q(MUX)}$, $\Delta T_{C/Q(MUX)}$, influences the falling edge of UP pulse and both edges of the DN pulse. From Fig. 4.5, the width of the UP and DN pulses in this region are modeled as

$$\begin{aligned} T_{UP_new} &= T_{UP} - \Delta T_{I/Q(MUX)} \\ T_{DN_new} &= T_{DN} - \Delta T_{C/Q(MUX)}. \end{aligned} \quad (4.7)$$

Hence, in this region, the simulated UP/DN pulse-width is shorter than the predicted UP/DN pulse-width.

The third region or the linear region is the most important region where the simulated UP pulse is a straight line and coincides with the predicted UP pulse. It has the largest portion in the characteristic curve and shows the linearity of the proposed PD. In this region, the percentage error in width of the UP and DN pulses are less than 2% as shown in Fig. 4.4(b). The last region (Region 4) occurs when the phase difference is very large. The timing diagrams of the proposed PD in this region are shown in Fig. 4.6. The main reason for this decrease in the UP pulse-width is due to the small time difference between the input and clock edges of MUX. The input of MUX changes while the clock is still steering the current. Similar to the previous analysis, the decrease in ΔI_{SWING} will

lead to an increase in $T_{I/Q(MUX)}$. In this region, the width of the UP and DN pulses are modeled as

$$\begin{aligned} T_{UP_new} &= T_{UP} - \Delta T_{I/Q(MUX)} \\ T_{DN_new} &= T_{DN} \end{aligned} \quad (4.8)$$

Hence, the simulated UP pulse-width is smaller than the predicted UP pulse-width and the simulated DN pulse-width is the same as the predicted DN pulse-width.

Figure 4.6. Timing diagrams of the proposed PD when T_{phase} is very large.

The latch plays an important role in this design as it decides the performance and power of the proposed PD. The $T_{I/Q(latch)}$ determines the closeness between the meta-stable region and crossover point of the UP/DN curve. As $T_{I/Q(latch)}$ decreases, the meta-stable region will move away from the crossover point thereby improving the performance of the proposed PD. In addition, it also influences the linear region of the characteristic curve and the region between linear and meta-stable. As for the MUX and XOR design, the speed and power requirements are less stringent as compared to the latch.

4.3 Circuit Implementation of the Proposed PD

In order to achieve high speed, all the building blocks in the proposed PD are implemented with high speed differential MOS current mode logic (MCML) architecture. The schematic diagrams of commonly used MCML gate are shown in Fig. 4.7. It is generally composed by three portions, which are a pull-down network with stacked of source-coupled pairs, a current source and pull-up resistors. The main function of pull down network is to switch the bias current, I_{ss} , to either one of the resistors, R . The resistor will then act as an I-V converter which converts current into voltage. The output voltage can be represented by $V_O = Q - Q$ where output *high* has a value of $I_{ss} \times R$ and output *low* has a value of $-I_{ss} \times R$.

Fig. 4.7(a) shows the schematic diagram of the MCML D-latch. When the CLK signal is *high*, transistor M_1 is on and transistors M_3 and M_4 help to read in input data. This is the reading period of D-latch. When the CLK signal is *low*, transistor M_2 is on and transistors M_5 and M_6 will helps to latch the output. This is the latching period of D-latch.

The schematic diagram of MCML 2:1 multiplexer (MUX) is shown in Fig. 4.7(b). When the CLK signal is *high*, transistor M_1 is on and the output of MUX will follow input signal, A. When CLK signal is *low*, transistor M_2 is on and output of MUX will follow input signal, B. The design parameters for both MCML D-latch and 2:1 MUX are given in Table 4.1. As the performance of D-latch is more critical than 2:1 MUX, the bias current of D-latch is design to have a larger value than 2:1 MUX.

Figure 4.7. Topology of a MCML (a) D-latch, and (b) 2:1 multiplexer.

Table 4.1. Design parameters for MCML D-latch and 2:1 multiplexer.

Devices	D-latch	2:1 multiplexer
	W/L (μm)	W/L (μm)
M_1/M_2	3.74*6/0.18	3.74*3/0.18
M_3/M_4 and M_5/M_6	3.655*6/0.18	3.47*3/0.18
R	200- Ω	400- Ω
I_{SS}	1.8-mA	1.5-mA

Fig. 4.8(a) shows the schematic diagram of a conventional MCML XOR gate. The input signal, A, of the XOR gate is connected to transistors M_1 and M_2 and the input signal, B, of the XOR gate is connected to transistors M_3 , M_4 , M_5 and M_6 . The stacking structure of the conventional MCML XOR gate causes a difference in propagation delays between its two input signals, A and B, with respect to the output. This difference will translate into errors in the UP and DN pulse-widths which will degrade the overall performance of the PD design.

To minimize this difference in the delays, the conventional MCML XOR gate is replaced by a symmetrical MCML XOR gate shown in Fig. 4.8(b) [57, 58]. It is basically implemented through connecting two conventional XOR gates in parallel with their inputs swapped and outputs shorted. The current source of each conventional XOR gate can be reduced to half so that the power consumption will remain the same. As both input signals, A and B, have the same paths to the output, their propagation delay will be the same. Table 4.2 shows the design parameters of the symmetrical MCML XOR gate implemented in this design. As each of the current sources is 0.6-mA, the total current consumed by the symmetrical MCML XOR gate is 1.2-mA.

Figure 4.8. Schematic diagram of a MCML XOR gate; (a) conventional and (b) symmetrical.

Table 4.2. Design parameters for MCML XOR (symmetrical).

Devices	XOR
	W/L (μm)
M ₃ -M ₆ and M ₉ -M ₁₂	5/0.18
M ₁ /M ₂ and M ₇ /M ₈	1.4/0.18
R	600- Ω
I_{ss}	0.6-mA

In the proposed PD, the difference in capacitive load of MUX should also be taken into design consideration. In Fig. 4.1(a), the load of M_2 , M_3 is one XOR gate while the load of M_1 , M_4 is two XOR gates. As difference in load will also cause variation in propagation delay, a dummy XOR gate is added to circumvent this problem. Its inputs are connected to M_2 , M_3 to balance between the loads.

4.4 Simulation Results and Comparisons

The proposed PD is simulated under Cadence SpectreRF environment and implemented using Global-foundries' 0.18- μm RF CMOS process. The transistor sizes of the circuit are chosen to be as small as possible in order to reduce the parasitic load and effect in high speed operation. However, the reduction in transistor sizes should not compromise the linearity and robustness of the proposed PD. Fig. 4.9 shows the layout of the proposed PD and it occupies a total chip area of only $132 \times 155\text{-}\mu\text{m}^2$.

Figure 4.9. Layout diagram of the proposed PD.

Fig. 4.10 shows the full parasitic post-layout simulation results of the new PD with a 5-Gb/s random input data, D_{in} . It consumes 32.55-mW at 1.8-V supply voltage. Whenever there is a change in D_{in} either UP_1 or UP_2 will have a pulse-width equal to the phase difference plus a constant pulse-width. Similarly for DN, the pulse-width is equal to the data period. If D_{in} keeps changing, DN will output a long constant *high*. The small glitches in UP are mainly due to the simultaneous change in the inputs of XOR gate, i.e. M_1 , M_2 changing from zero to one or vice versa simultaneously and causing a small glitch in UP_1 .

Figure 4.10. Post-layout simulation results of the proposed PD.

Figure 4.11. Eye diagrams of the (a) UP₁ and (b) DN pulses.

To ensure the functionality of the proposed PD, it is integrated into a PLL-based CDR system. The circuit is simulated with a 5-Gb/s $2^{31}-1$ PRBS input signal with loop bandwidth equal to 27-MHz. The eye diagrams of UP₁ and DN in locking condition are shown in Fig. 4.11(a) and Fig. 4.11(b) respectively. As UP₂ has a similar eye diagram as UP₁, the eye diagram of UP₂ is not shown here.

To further ensure the robustness of the new design, it is also simulated under fast-fast (FF) and slow-slow (SS) conditions. The simulated characteristic curve of both FF

and SS conditions are shown in Fig. 4.12. In the FF condition, the range of linear region is improved because the propagation delay of each block is reduced. On the other hand, the SS condition is the opposite and shows the worst case scenario for propagation delay. These two conditions define the boundary of the UP and DN pulse-widths due to process variations.

Figure 4.12. Characteristic curves of the proposed PD under FF and SS conditions.

Table 4.3 shows the comparison of the proposed PD with existing lower-rate PDs. From the table, the proposed PD is composed by 4 D-latches, 4 MUXs and 4 XOR gates which has a total number of 12 building blocks. Although the reported PD in [55] is composed by 4 D-latches, 4 D-FFs and 2 4-inputs XOR gates, each D-FF is basically formed by two D-latches which means that the total number of building blocks needed is 14. The total number of building blocks for the reported PD in [52] is 13 which has the least amount of building blocks among all the other existing lower-rate linear PDs. However, the amount of building blocks for the proposed PD is still one less building block than it. Hence, the proposed PD achieves the least amount of building blocks among the best reported lower-rate PDs.

Table 4.3. Performance Comparison of Lower Rate PDs.

	[59]	[37]	[55]	[52]	[34]	[60]	This Work
Technology	0.18- μm	0.25- μm	-	0.18- μm	0.18- μm	0.13- μm	0.18- μm
Data Rate	40-Gb/s	4-Gb/s	-	4-Gb/s	5-Gb/s	10-Gb/s	5-Gb/s
Type of PD	Binary	Linear	Linear	Linear	Linear	Linear	Linear
Supply	2-V	2.5-V	-	1.8-V	1.8-V	1.2-V	1.8-V
Rate of PD	1/4 rate	1/8 rate	1/4 rate	1/4 rate	1/8 rate	1/4 rate	1/4 rate
Power Diss.	-	-	-	28.8-mW	-	74.4-mW ^a	32.55-mW 34.71-mW ^a
Power per Gb/s	-	-	-	7.2-mW	-	7.44-mW ^a	6.51-mW 6.94-mW ^a
Building Blocks	8 D-FF 8 XOR gates	8 Latches DCT ^b Detector ^c DCT ^b Generator	4 2-phase Latches 4 D-FF ^d 2 4-inputs XOR	4 Latches 6 MUX cells 3 XOR gates	16 Latches 16 AND gates 16 XOR gates	4 Latches 8 AND gates 3 XOR gates	4 Latches 4 MUX cells 4 XOR gates
Output Signals	-	1 UP pulse 1 DN pulse	1 UP pulse 1 DN pulse	2 UP pulses 1 DN pulse	8 UP pulses 8 DN pulses	4 UP pulses 4 DN pulses	2 UP pulses 1 DN pulse
UP-pulse widening	-	No	No	No	Yes	Yes	Yes

^a Includes charge pump power consumption

^b Data & Clock Transition (DCT)

^c DCT Detector compose by 4 MUX cells and 8 XOR gates

^d D-FF is formed by 2 D-latches

The proposed PD also has the lowest power consumption per Gb/s. This is achieved through minimizing the total number of building blocks being implemented in the PD. Besides that, from the analysis of the proposed PD, the power consumption can also be reduced by reducing the power consumption of the MUX and XOR gate. This is because the performance of the PD is mainly affected by the D-latch.

To circumvent the problem of very small UP pulse, the proposed PD also implement with UP pulse-widening technique. However, for PDs which implement UP

pulse-widening technique ([34] and [60]), their number of output signals increased. This increase in output signals will require more charge pumps in the clock and data recovery circuit which will further increase the power consumption of the overall circuit. Besides that, the problem of current mismatch will also be further degraded. The proposed PD improves the number of output signals to 2 UP signals and 1 DN signal as compared to [34] and [60]. With this reduction in output signals, only one unbalanced charge pump will be needed for the whole clock and data recovery circuit.

The proposed PD also widens the pulse-width of the DN signal. With wider DN pulse-width, the switching activities of DN signal are reduced. This improves on the current mismatch problem of the charge pump due to input switching.

5 De-multiplexer (DEMUX)

De-multiplexer (DEMUX) is an essential component in the receiver of high speed serial-link data communication system. It performs the necessary functions of extracting the input series data stream into two or more parallel output data channels at the receiver. These output data channels are transmitted for further signal processing.

5.1 Introduction to DEMUX

Figure 5.1 Timing diagrams of a time-division 1:2 DEMUX.

In serial-link data communication system, DEMUX is implemented in time-division method to separate the input data, D_{in} . In time-division DEMUX, it has two basic specifications, input data rate and number of output data streams. Input data rate specifies the length of the time frame to store each data. For example a 5-Gb/s input data rate means that the time frame for each data is 200ps. The number of output data streams in serial-link data communication is mostly in terms of 2^N where N is a positive integer. Fig. 5.1 illustrates the function of a time-division 1:2 DEMUX. The output data streams is stored in-sequence in D_{in} .

There are two main architectures to implement a time-division DEMUX. The first type of architecture is called “shift register” [61] and its block diagram is shown in Fig. 5.2. For the case of N channels DEMUX, N-bits are clocked serially into N-bit shift register and its clock frequency is the same as input data rate. After all data are available for a parallel output dump, data ready flag will be used to output all the data.

Figure 5.2 Block diagram of 1:N DEMUX with “Shift Register” architecture.

The second architecture is called “pair” or “tree” architecture. It uses 1:2 DEMUX as the basic building block. For a 1:N DEMUX operation, the number of 1:2 DEMUX block being used is calculated by using the formula $2^N - 1$. At the beginning stage, D_{in} is de-multiplexed into two parallel outputs by using a 1:2 DEMUX block. These parallel outputs are further de-multiplex into four parallel outputs by using two 1:2 DEMUXs at the second stage. This process will continue until N parallel outputs are being de-multiplexed by using $N/2$ 1:2 DEMUX blocks. Hence, the number of stage needed to complete 1:N DEMUX is given by $\log_2 N$. In each of the stage, the clock frequency will

reduce by half compared to previous stage. Fig. 5.3 shows the block diagram of a 1:8 DEMUX. The total number of stage is 3 and the number of 1:2 DEMUX blocks implemented is 7.

Figure 5.3 Block diagram of 1:8 DEMUX with tree architecture.

The “shift register” architecture has an advantage of having simpler circuit. For example, a 1:4 DEMUX design, “shift register” architecture composed by four registers and one frequency divider. However, the “tree” architecture is composed by three 1:2 DEMUX blocks and one frequency divider. The 1:2 DEMUX block usually consists of five latches. Although “shift register” architecture has advantage in circuit complexity, the main drawback is its stringent speed requirement on each block. In this design, each register has to function at the data rate. As the data rate becomes higher and higher, it becomes a huge challenge in designing the circuit block. In contrast to “shift register” architecture, “tree” architecture eases the speed requirement as the speed requirement of each subsequent stage is reduced by half with comparison to the previous stage. Although

the first stage of “tree” architecture has a stringent speed requirement, it is only required to operate at half of the data rate which is also half of the speed requirement for “shift register” architecture. Hence, “tree” architecture is more preferred in high speed design. In the following section, we will have a more detail discussion on “tree” architecture.

5.2 Building Blocks of “Tree” DEMUX Architecture

Figure 5.4 (a) Block diagram and (b) timing diagrams of 1:2 DEMUX.

In a “tree” DEMUX architecture design, it only consists of two main building blocks, 1:2 DEMUX and frequency divider. The block diagram of a conventional 1:2 DEMUX block is shown in Fig. 5.4(a). It consists of 5 D-latches and they are clocked by a half-rate clock. To ensure the DEMUX has sufficient margin for timing, D_1 is generated by master-slave-master D-latches with a positive clock and D_2 is generated by master-slave D-latches with a negative clock. Hence, D_1 samples D_{in} at the falling edge of the clock and D_2 samples D_{in} at the rising edge of the clock. From Fig. 5.4(a), the additional D-latch found in D_1 path is to add as additional half period phase to D_1 so that both outputs D_1 and D_2 will have the same phase. The function of 1:2 DEMUX can be illustrated by the timing diagrams shown in Fig. 5.4 (b). D_1 samples the even number of the data (falling edge of the clock) and D_2 samples the odd number of the data (rising edge of the clock).

Figure 5.5 (a) Block diagram and (b) timing diagrams of frequency divider.

Frequency divider is commonly implemented with two D-latches and its block diagram is shown in Fig. 5.5(a). From the block diagram, the complement output of the second latch is feed back to the input of the first latch. The timing diagrams of the frequency divider are shown in Fig. 5.5(b). When CLK_{IN} is *high*, the first latch will latch in the complement of CLK_{QOUT} . As CLK_{IN} changes to *low*, the second latch will latch in CLK_{IOUT} . Through this mechanism, the frequency of CLK_{IN} is reduced by half. With the negative feedback topology, the phase of both CLK_{IOUT} and CLK_{QOUT} will change by 180° after a period of CLK_{IN} . The frequency divider not only divides the frequency of the input clock, but also has the ability to provide a four phase clock outputs. This provides designers with choices of different clock phases.

5.3 The “Tree” DEMUX Architecture with D-latch Modification

As D-latch is the basic building block of 1:2 DEMUX, researchers have been endeavoured to improve its performance. Several papers have been reported about the modifications of MCML D-latch design. In this section, we will discuss some of the important design that helps to improve the speed performance of D-latch.

5.3.1 MCML D-latch without Current Source

The first design is called MOS current-steering (MCS) D-latch [62] and its schematic diagram is shown in Fig. 5.6. The main difference between MCS design and MCML design is that the current source in MCML design has been removed in the MCS counter part. With this removal, the source of transistors M_1 , M_2 are directly grounded, which reduces the voltage headroom of the supply voltage. In addition, the parasitic

capacitance of the current source node in the MCML design is also removed by shorting the two sources of M_1 , M_2 to ground. This will enable the D-latch to operate at a higher speed.

Figure 5.6 Schematic diagram of MOS current steering (MCS) D-latch.

However, the main drawback of MCS design is that the removal of the current source increased the toughness in controlling the current flowing through it. As a result, the output voltage swing is harder to predict. As transistors M_1 , M_2 act as variable current sources, the current flowing through it depends on clock voltage level and size of the transistors. To achieve high speed, the channel length of M_1 , M_2 transistors has to be shorter than the channel length of current source transistor. As a result, the current flowing through them is very sensitive to process variation. In addition, any change in the clock voltage level will also change the current flowing through M_1 , M_2 . Hence, the MCS D-latch is not robust.

5.3.2 MCS D-latch with Inductor

Figure 5.7 Schematic diagram of MCS D-latch with shunt-peaking inductors.

To further improve the speed performance of MCS D-latch, shunt-peaking inductors are added and the schematic diagram is shown in Fig. 5.7 [63]. These inductors are inserted between supply voltage, V_{DD} , and load resistance, R , to boost the circuit bandwidth. The bandwidth extension can be achieved by resonating the shunt-peaking inductance with the output capacitance in the proximity of corner frequency. The frequency response of the shunt-peaking architecture is affected by two parameters, the ratio of L/R and the RC time constant where C is the load capacitance. By equating both parameters with a constant, m , the relationship between R , C and L can be expressed as

$$L = mR^2C. \quad (5.1)$$

In order to get the maximum flat response, the value of m has to be equal to 0.41 [64]. In this condition, the bandwidth enhancement for the MCS D-latch is around 72%. As the value of m continues to increase, the bandwidth of the MCS D-latch will also increase. When m is equal to 0.71, the bandwidth enhancement reaches its maximum value which

is around 85%. However, this increase in bandwidth is trade-off with a significant gain peaking. With a given R and C value, the inductance value for the shunt-peaking inductor can be easily calculated through Eq. (5.1).

In order to achieve an even wider bandwidth, capacitive-splitting architecture [65, 66] is another choice. There are mainly two types of capacitive-splitting: near-end (NE) termination network and far-end (FE) termination network. Both of their schematic diagrams are shown in Fig. 5.8. Although the circuit structure of NE and FE termination networks are very similar, their frequency and step responses are quite different. They will only have the same response when both the terminal capacitances of L_s are the same. However, in practical, D-latch does not have same capacitance between these two terminals.

Figure 5.8 Circuits and frequency response of the capacitive-splitting architectures. (a) NE topology. (b) FE topology. [67]

To simplify the derivation of capacitive-splitting architecture, the input is modeled as a current source. The frequency behaviour of capacitive-splitting architecture is shown in Fig. 5.8. For NE topology (Fig. 5.8(a)), the first resonant frequency, $\omega_{1,NE}$, is caused by the resonance of L_s and C_2 . The second resonant frequency, $\omega_{2,NE}$, is the frequency in which the gain is at its maximum because the π -network (C_1 - L_s - C_2) resonates at this frequency. Subsequently, L_p and $C_{eq,NE}$ resonate at frequency $\omega_{3,NE}$. For FE topology (Fig. 5.8(b)), the first resonant frequency, $\omega_{1,FE}$, is caused by the resonance of L_p and C_2 . It is then followed by the resonance of L_s and $C_{eq,FE}$ with resonant frequency of $\omega_{2,FE}$. Finally, the π -network (C_1 - L_s - $C_{eq,FE}$) resonates at $\omega_{3,FE}$ and at this frequency, the gain is at its maximum.

Figure 5.9 (a) Frequency response of different topologies with the maximum achievable bandwidth ($\omega_0 = (RC_L)^{-1}$). (b) Step response of NE and FE topology. [67]

Fig. 5.9(a) shows the frequency response of the four different topologies that have been discussed above. It shows that the capacitive-splitting topology can achieve the widest bandwidth and it validates with the analysis. Besides that, it also shows that FE network has a higher bandwidth extension than NE network. However, this superiority is compromised with the large gain peaking around the corner frequency. From the step response shown in Fig. 5.9(b), the FE network has a smaller damping ratio than the NE

network. Hence, the bandwidth of FE network is trade-off with gain peaking and a smaller damping ratio [67].

The main drawback of D-latch design with inductor is the large silicon area occupied by inductor. As each D-latch will employ two to four inductors, a basic 1:2 DEMUX block will have to employ ten to twenty inductors which are very significant in the area consumption. This will also lead to long interconnection and hence increase the coupling noise.

5.3.3 MCML D-latch with Dual-Clock

To avoid the large area consumption by the inductors, the D-latch reported in [68] employed a dual-clock architecture and its schematic diagram is shown in Fig 5.10(a). It is a modification of the conventional MCML D-latch by adding two more transistors and an additional input signal, CLKD. The additional signal, CLKD, is a delayed version of the clock signal (CLK). This architecture overcomes data distortion caused by data transition and process variation. Fig. 5.10(b) shows the timing diagrams of the modified CML latch. The output, Q, can generally separate into two periods: reading period and latching period. Reading period is where both CLK and CLKD are high. The other portion is the latching period. With the characteristic of a flip-flop, this new circuit structure can replace the master-slave latch used in the 1:2 DEMUX block and reduce the number of transistors used.

misreading issue. This issue decides the upper limit of the reading period. If the reading period is too short, the modified CML latch will not be able to react fast enough to read in the data. As stacking of the transistors increases, longer reading period is needed and this decides the lower limit of the reading period. The range for reading period, T_{READ} , will be the difference between these two limits. However, as the data rate increases, T_{READ} will decrease and more stringent requirements will be imposed on the DLL or PLL which is harder to implement.

5.3.4 MCML D-latch with Dual Current Source

Figure 5.11 Circuit diagrams of MCML (a) coupled latch (CL), and (b) CL + buffer. (c) Frequency response of different latch architectures. [69]

The coupled latch (CL) [69] shown in Fig. 5.11(a) is another architecture reported to widen the circuit bandwidth without using inductors. It uses two separate current sources, I_{read} and I_{hold} . The reading and latching networks are very similar to those in [70]. Both the current sources, I_{read} and I_{hold} , supply a current equals to $I_0 + \alpha$ and $I_0 - \alpha$, respectively. With current reduction in I_{hold} , the transistors' size in the latching network can be reduced. Hence, the loading capacitance is reduced which implies that higher speed can be achieved. In addition, the current I_{read} is also increased to enhance the speed. However, small I_{hold} will cause a voltage swing reduction at latching state which will degrade the speed performance. Hence, an additional buffer is inserted after CL to improve the rise and fall time of CL and also to provide an acceptable voltage swing.

Fig 5.11(c) provides the frequency response of four different types of D-latch architectures in which CL + buffer architecture has the highest gain and bandwidth. However, the achievement in gain and bandwidth is a trade-off with higher power consumption. The current consumption of a CL + buffer is the sum of I_{read} , I_{hold} and I_0 which is equal to $2I_0$. For a basic 1:2 DEMUX block, CL + buffer architecture will consume a total current of $10I_0$. Compared to the conventional D-latch, the CL + buffer has a 2 time increase in current consumption which is not preferred in low power design.

5.4 Modification of “Tree” DEMUX Architecture

Figure 5.12 Block diagram of 1:4 DEMUX (a) conventional tree architecture (b) cascaded buffers and (c) cascaded buffers and DLL.

One of the drawbacks in conventional “tree” DEMUX architecture is that the output of the frequency divider has to drive large capacitive load which is 10 D-latches in the second stage; 2:4 DEMUX block of a 1:4 DEMUX. This large capacitive load will cause sensitivity degradation and has to compensate by increasing the size of frequency divider. As a result, the frequency divider consumes a large amount of power. In order to

reduce the capacitive load seen by the frequency divider, buffers are inserted at the output of the frequency divider in the 1:4 DEMUX shown in Fig. 5.12(b) [63]. The buffers relieve the capacitive load seen by the frequency divider output and enable the frequency divider to operate at a faster speed with smaller size. To ensure that both the 1:2 DEMUX output and frequency divider output are aligned, buffers are also added to both the D_{odd} and D_{even} paths. However, due to process variation, the phase margin between $D_{\text{odd}}/D_{\text{even}}$ and the frequency divider output will still reduce and cause degradation in DEMUX performance.

The 1:4 DEMUX shown in Fig. 5.12(c) [69] includes an additional DLL circuit to improve the phase margin of the DEMUX. The DLL circuit will synchronize the falling edge of the input clock, CLK, with the rising edge of the feedback clock, CLK_{FB} . As the output of the 1:2 DEMUX will experience a clock-to-output delay, $T_{\text{C/Q}}$, CLK_{FB} will need an additional $T_{\text{C/Q}}$ delay to synchronize with the data. Hence, $\text{CLK}/2$ will be able to sample at the mid-point of the data for maximum phase margin.

The main advantage of this architecture is that it relaxes the output load of the frequency divider and ensures that the phase margin is not being trade-off. However, on the other hand, this is being compromised with the circuit complexity and power consumption.

5.5 Lower-Rate DEMUX Architecture

Figure 5.13 Block diagram of the “tree” type quarter-rate DEMUX architecture.

In order to further ameliorate on the performance of DEMUX, researchers have begun to explore on the area of lower-rate DEMUX design recently. In this section, we will mainly discuss the quarter-rate DEMUX architecture.

Fig. 5.13 shows one of the quarter-rate DEMUX architecture and it has two 1:2 DEMUX blocks from Fig. 5.4 [71, 72]. The half-rate clock, CLK_{IN} , is first passed through a frequency divider to generate a four-phase quarter-rate clock, CLK_I and CLK_Q . Both CLK_I and CLK_Q are then used to clock two 1:2 DEMUX blocks. Hence, both the rising and falling edge of CLK_I and CLK_Q , respectively, will cause the input data, D_{in} , to be

read in. The last two latches for D_1 and D_3 are mainly implemented to delay the phase of Q_1 and Q_2 so that the output data, $D_1 - D_4$, will have the same phase.

Figure 5.14 Timing diagrams of the “tree” type quarter-rate DEMUX architecture.

In order to have a better understanding on this architecture, its timing diagrams are shown in Fig. 5.14. The CLK_I will de-multiplex the odd number of D_{in} data and the CLK_Q will de-multiplex the even number of D_{in} data. As there is a 90° phase difference between CLK_I and CLK_Q , the 1:2 DEMUX block outputs will also have a 90° phase difference. Both Q_1 and Q_2 are being latched by CLK_Q , so that they are delayed by 90° to produce D_1 and D_3 , respectively.

The DEMUX architecture shown in Fig. 5.15 is another reported quarter-rate design [60]. A four-phase clock, CLK_0 , CLK_{90} , CLK_{180} and CLK_{270} , is required for this architecture and the 1:4 DEMUX is formed by 16 latches. From the timing diagrams shown in Fig. 5.16, the speed requirement for D-latch is greatly eased as all the short

pulses will be filtered out and can be ignored. The circuit operation is described as follow; D_{in} is first latched by the four phases of the clock and the outputs will be further latched by the next phase of the clock. The following stages are for aligning purposes and the outputs of the DEMUX are aligned at the falling edge of CLK0. Hence, there is a delay of one and a half cycle.

Figure 5.15 Block diagram of the quarter-rate 1:4 DEMUX.

One of the advantages of the quarter-rate DEMUX architecture is that the bandwidth requirement for D-latch design is being reduced. With a reduction in bandwidth, we can implement the D-latch without using inductors. As a result, the silicon area is reduced. Another important advantage of quarter-rate architecture is it reduced circuit complexity. The quarter-rate 1:4 DEMUX reported in [71] uses only 14 D-latches. While the half-rate 1:4 “tree” DEMUX has 17 D-latches. With less D-latches and lower bandwidth requirement, quarter-rate DEMUX architecture can achieve lower power consumption too.

Figure 5.16 Timing diagrams of quarter rate 1:4 DEMUX.

One of the drawbacks for the quarter-rate DEMUX architecture is the use of four phase clock. Besides that, in conventional high speed DEMUX design, the frequency of the clock is normally half-rate instead of quarter-rate. The four phase quarter-rate clock can be generated by passing the half-rate clock through a frequency divider.

5.6 The Proposed DEMUX

Due to the superior performance in power, the proposed DEMUX will be implemented in quarter-rate architecture. The architecture and simulation results of the proposed DEMUX will be discussed in this section.

5.6.1 Architecture of the Proposed DEMUX

Figure 5.17 Block diagram of the proposed quarter-rate 1:4 DEMUX.

The block diagram of the proposed quarter-rate 1:4 DEMUX architecture is shown in Fig. 5.17. It consists of 14 D-latches which are clocked by a four-phase clock, CLK0, CLK90, CLK180, and CLK270. The first two stages of D-latches function as D-FFs. At the first stage, the input data, D_{in} , is first clocked by four different phases of the clock and these outputs are further clocked with the opposite phase of each respective clock at the second stage of D-latch. At this stage, all the required data, $Q_5 - Q_8$, has been read by the

rising edge of each phase of the clock. Next, Q_5 and Q_6 are delayed by latching with CLK180. At the final stage, Q_7 to Q_{10} are latched by the rising edge of CLK0, which aligns the outputs D_1 - D_4 . The proposed DEMUX architecture de-multiplexes D_{in} within a clock cycle with the outputs of D_1 - D_4 .

Figure 5.18 Timing diagrams of the proposed quarter-rate 1:4 DEMUX.

Fig. 5.18 shows the timing diagrams of the proposed quarter-rate 1:4 DEMUX architecture. As the first two stages of D-latch function as rising edge D-FFs, the outputs of the second stage, Q_5 to Q_8 , read in Data 1 to Data 4 at the rising edge of each phase of the clock. The remaining subsequent stages are for phase aligning purpose which shifts the phases of Data 1 to Data 4 to the rising edge of CLK0. Finally, D_{in} is de-multiplexed

into four parallel outputs, D_1 to D_4 , with the required data, (Data 1 to Data 4), (Data 5 to Data 8) and etc. The final pulse-width of each data will be four times the period of D_{in} . This implies that the output data rate decreases by four times.

From Fig. 5.18, it is clear that only the first four D-latches (i.e. L_1 to L_4) have some small pulses at their outputs. However, all these pulses will not affect the speed requirement of the D-latches as they are not being used for the next stage. The speed limiting factor of the proposed DEMUX circuit is mainly affected by the hold time of the D-latches in the first stage. For example, at the falling edge of CLK180, L_1 has to read in Data 5. If the phase difference between D_{in} and CLK180 is smaller than the hold time of D-latch, then L_1 will not have enough time to read in Data 5. As a result, the DEMUX circuit will malfunction. Hence, only the first stage of D-latches (i.e. L_1 to L_4) has to operate at a higher speed. As for the D-latches in other stages, they only need to operate at a lower speed. Hence, their bias currents can be reduced which will lead to lower power consumption.

Table 5.1. Design parameters for the proposed DEMUX.

Devices	$L_1 - L_4$	$L_5 - L_{14}$
	W/L (μm)	W/L (μm)
M_1/M_2	1.9/0.18	1.0/0.18
M_3/M_4 and M_5/M_6	3.8/0.18	3.0/0.18
R	1.6-k Ω	4-k Ω
I_{SS}	500- μA	185- μA

The schematic diagram of the building block, D-latch, can be found in Fig. 4.7.

Table 5.1 shows the design parameters of the proposed DEMUX circuit. As first stage of

D-latches required a higher speed, their current sources are set to be 500- μ A. For the other stages, the current sources are set to be 185- μ A.

5.6.2 Results and Discussions

The proposed DEMUX circuit is simulated in Cadence SpectreRF environment and is implemented with 0.18- μ m RF CMOS process from Global-foundries'. All the D-latches employ in the proposed DEMUX circuit utilizes MOS current mode logic (MCML) technique and its schematic diagram is shown in Fig. 4.7. The proposed DEMUX circuit employs a two-stage output buffer and its schematic diagram is shown in Fig. 5.19. The first stage of this output buffer helps to minimize the bandwidth degradation of the D-latch and provide sufficient amplification. The second stage of the buffer acts as a 50 Ω matching network and has a large bias current to provide adequate voltage swing to drive the output pad.

Figure 5.19 Schematic diagram of the two-stage output buffer.

Figure 5.20 Layout of the proposed DEMUX circuit.

Fig. 5.20 shows the layout of the proposed 1:4 DEMUX circuit, which consumes a total area of $87 \times 108.2\text{-}\mu\text{m}^2$. The front portion of the layout is occupied with 1:4 DEMUX circuit and the portion behind is the output buffers. The proposed 1:4 DEMUX circuit operates at 1.8V supply voltage and its D_{in} is generated from a 10-Gb/s random bit sequence. D_{in} has a voltage swing of 400-mV_{pp} and its rise (fall) time is equal to 100-ps. The circuit is clocked by a 2.5-GHz four-phase clock which has an amplitude of 450mV. Sinusoidal clock is used in this simulation instead of square clock for the purpose of examining the robustness of the circuit.

Figure 5.21 Simulation results of the proposed DEMUX.

Fig. 5.21 shows the results of post-layout simulation with full parasitic extraction. It consists of D_{in} , CLK0 (solid line), CLK90 (dotted line) and the output waveforms D_1 , D_2 , D_3 and D_4 . The complements of all the output waveforms are shown in dotted line. Fig. 5.21 demonstrates the functionality of the proposed DEMUX circuit. The first group of D_{in} shown is “0010” and this group of data is de-multiplexed into four outputs, D_1 - D_4 , which has the value of “0”, “0”, “1”, and “0” respectively. The output voltage swing is 400mV_{pp} and the average power consumption is 6.98mW (without output buffers) and 50.32mW (with output buffers). To ensure that the proposed 1:4 DEMUX circuit is robust enough against process variation, it is also simulated under fast-fast (FF) and slow-slow

(SS) conditions. The average power consumption (without output buffer) under FF and SS conditions is 8.38mW and 6.10mW, respectively.

Table 5.2. Characteristics of the proposed DEMUX circuit.

Supply Voltage	1.8-V
Data Rate	10-Gb/s
Clock Frequency	2.5-GHz
Power Consumption (without buffers)	6.98-mW
Power Consumption (with buffers)	50.32-mW
Input Voltage Swing	400-mV _{p-p}
Output Voltage Swing	400-mV _{p-p}
Phase Margin	72-ps

Table 5.2 shows the characteristics of the proposed 1:4 DEMUX circuit, which has an excellent phase margin of 72-ps. With this phase margin, the circuit is able to tolerate the effects of input jitter and clock jitter in communication system. Fig. 5.22(a) and Fig. 5.22(b) show the input eye diagrams for D_{in} and the clock, respectively, and Fig. 5.23 shows the stressed-eye diagram for the proposed circuit. Due to the limitation of simulation, D_{in} is simulated with $2^{13}-1$ pseudo-random bit sequence with the consideration of input jitter that is composed of random jitter, deterministic jitter. The horizontal and vertical eye openings for D_{in} are around 70-ps and 200-mV, respectively. To further test the robustness of the proposed circuit, a triangular wave with jitter is used instead of sinusoidal wave. As the output of the VCO has smaller jitter than D_{in} , the peak-to-peak jitter amplitude for the clock is set to be around 27-ps. The simulated stressed-eye diagram has horizontal eye opening of 374ps and vertical eye opening of 450mV.

Figure 5.22 Input eye diagrams for (a) D_{in} and (b) Clock.

Figure 5.23 Stressed-eye diagram of the proposed 1:4 DEMUX.

Table 5.3. Comparison between the proposed DEMUX and the existing DEMUXs.

	[73]	[62]	[74]	[68]	[69]	[75]	[71]	This work
Technology	0.18- μ m	0.18- μ m	0.18- μ m	0.18- μ m	0.13- μ m	0.18- μ m	90-nm	0.18- μ m
1:N DEMUX	1:8	1:4	1:4	1:4	1:4	1:2	1:4	1:4
Data Rate	10-Gb/s	10-Gb/s	10-Gb/s	10-Gb/s	20-Gb/s	20-Gb/s	20-Gb/s	10-Gb/s
Supply Voltage	2.0V	1.5V	1.3V	1.8V	1.2V	1.3V	1.2V	1.8V
Power	48-mW 102-mW ^a	54-mW 160-mW ^a	38-mW -	12.2-mW -	- 210-mW ^a	- 140-mW ^a	9.5-mW -	6.98-mW 50-mW ^a
Power Efficiency (mW/Gbps)	4.8 10.2 ^a	5.4 16.0 ^a	3.8 -	1.2 -	- 10.5 ^a	- 7.0 ^a	0.475 -	0.698 5.0 ^a

^aPower consumption with output buffers

Table 5.3 shows the performance of the proposed DEMUX against other reported DEMUXs. The proposed DEMUX has the best performance in power consumption. In terms of power efficiency, the proposed DEMUX is in second place. The main reason for [71] to have the best performance in power efficiency is that it is implemented in 90-nm technology. If the proposed DEMUX is implemented in the same technology, it will also have a better performance in power efficiency.

6 Architecture Components: Dual-Loops CDR design, Charge Pump & VCO

6.1 The Proposed Dual-Loops PLL-CDR Architecture

Figure 6.1. Block diagram of the proposed dual-loops PLL-CDR architecture.

In Section 2.4, different types of CDR architectures have been discussed. As the dual-loops PLL-CDR has a good performance in input jitter rejection and has a wider capture range, the proposed CDR design will be implemented with this architecture. Fig. 6.1 shows the block diagrams of the proposed CDR design. It consists of a frequency acquisition loop (bottom loop) and a phase tracking loop (top loop). The frequency acquisition loop consists of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a quadrature voltage controlled oscillator (QVCO) and a frequency

divider. As for the phase tracking loop, it consists of a phase detector (PD), an unbalanced charge pump, a LPF, a QVCO and a data recovery (DR) circuit.

In Fig. 6.1, both the frequency acquisition and phase tracking loops share a common LPF and a QVCO. The switching between the loops is controlled by the lock detector and a multiplexer (MUX) that acts as a switch. The lock detector detects the frequency difference between the reference frequency and the QVCO frequency. When the recovered clock frequency is within certain frequency accuracy of the reference clock, REF, the lock detector will enable the MUX to switch from the frequency acquisition loop to the phase tracking loop. After switching to the phase tracking loop, the lock detector will continue to track the QVCO frequency. If the QVCO frequency is shifted out of certain frequency accuracy with respect to REF, the lock detector will switch from the phase tracking loop back to the frequency acquisition loop.

The proposed linear PD discussed in chapter 4 will be implemented in the phase tracking loop of this CDR design. The proposed PD has two UP signals and one DN signal. As its output differs from the output of conventional PD, an unbalanced charge pump is proposed to compensate for this difference. Besides that, the proposed CDR design not only retimed the input data but also helps to de-multiplex the retimed input data into four parallel output data for further digital signal processing. The DR block functions as a 1:4 DEMUX circuit and its circuit structure contains part of the proposed DEMUX circuit mentioned in chapter 5. Fig. 6.2 shows the block diagrams of the proposed PD and DEMUX discussed in chapter 4 and chapter 5, respectively. As the first stage of both PD and DEMUX are the same, the first stage is shared by these two circuit

blocks (PD and DEMUX). The sharing of the first stage by both blocks not only results in reducing the total number of circuit blocks but also eliminates the systemic phase offset caused by the retimed data. The recovered data from the 1:4 DEMUX is then multiplexed together for the purpose of BER measurement.

Figure 6.2. Block diagrams of the proposed (a) PD and (b) 1:4 DEMUX.

6.2 Charge Pump Design

6.2.1 Conventional Charge Pump

The main function of the charge pump is to control the current flowing into and out of the LPF. Fig. 6.3 illustrates the functionality of the charge pump. There are three main operating states of the charge pump design. 1) When the UP signal is *high*, switch S_1 will close and the charge pump current will flow into the LPF. 2) When the DN signal is *high*, switch S_2 will close and the charge pump current will flow out of the LPF. 3) When both the UP and the DN signals are *low*, both switches, S_1 and S_2 , will open and no current flows [76].

Figure 6.3. Block diagram of PD, CP and LPF.

The simplest charge pump design is shown in Fig. 6.4(a) [77]. The switch S_1 is replaced by a PMOS transistor and the switch S_2 is replaced by a NMOS transistor. The current sources for pull-up and pull-down transistors can be obtained from current mirrors. Fig. 6.4(b) shows the schematic diagram of the charge pump when the inputs are differential [78].

Figure 6.4. Schematic diagram of conventional charge pump (a) single input, and (b) differential input.

One of the issues arising from this PMOS-NMOS charge pump is the mismatch between the NMOS and PMOS transistors. This mismatch will further translate into the current mismatch of the charge pump. Another issue for this architecture is charge injection. When DN is *high*, the NMOS transistor will turn ON. At the time when DN is *low* and transistor is in the process of switching off, the accumulated channel charges will flow to V_2 and into the LPF. This additional charge injected into the LPF will translate into an error.

6.2.2 Differential Charge Pump Design

In high speed PD design, the output voltage of UP and DN signals are generally differential. So these signals do not have a full voltage swing. As a result, the NMOS and PMOS switches will not be fully opened or closed. This will also lead to the current mismatch. One of the methods to resolve these issues is by using a differential charge pump. The schematic diagram of a differential charge pump is shown in Fig. 6.5 [79].

Figure 6.5. Schematic diagram of a conventional differential charge pump.

Two pairs of NMOS source-coupled transistors are used as switches that are controlled by the UP and DN signals and their complements. Hence, the mismatch between NMOS and PMOS is eliminated. The two current sources at the bottom function as current steering devices. With one of the current sources will steer the source current to one of the output nodes. The truth table of the charge pump is listed in Table 6.1. When both UP and DN are *low*, the net current flowing into the LPF is zero. For the case when UP is *high*, the charge pump current, $2I$, will flow into the LPF. For the case when DN is *high*, the same amount of charge pump current will flow out of the LPF.

Table 6.1. Truth Table of a Conventional Differential Charge Pump.

UP	DN	I_{LPF}	$\overline{I_{LPF}}$	$I_{OUT} = I_{LPF} - \overline{I_{LPF}}$
L	L	0	0	0
H	L	I	-I	$2I$
L	H	-I	I	$-2I$

Fig. 6.6 shows the schematic diagram of a single-ended output differential charge pump [80, 81]. The top two current sources in Fig. 6.5 are replaced with the current

mirrors. These currents are mirrored to the output of the charge pump. The truth table of the charge pump is shown in Table 6.2 and the amount of current flowing is also $2I$.

Figure 6.6. Schematic diagram of a single-ended output differential charge pump.

Table 6.2. Truth Table of a Single-Ended Output Differential Charge Pump.

UP	DN	I_{UP}	I_{DN}	$I_{LPF} = I_{UP} - I_{DN}$
L	L	I	I	0
H	L	$2I$	0	$2I$
L	H	0	$2I$	$-2I$

Fig. 6.7 shows the start-up and biasing circuit for the charge pump design. The left portion is the biasing circuit and the right portion is the start-up circuit. The unit current for the biasing circuit is set to be $16.7\text{-}\mu\text{A}$. Table 6.3 shows the design parameters for the differential charge pump, start-up circuit and biasing circuit. As the current source for the charge pump is $400\text{-}\mu\text{A}$, the W/L ratio of the current source will be 24 times of the transistors M_{13} and M_{14} .

Figure 6.7. Schematic diagram of start-up and bias circuit.

Table 6.3. Design parameters for charge pump, start-up circuit and biasing circuit.

Start-up and biasing circuit		Differential charge pump	
Devices	W/L (μm)	Devices	W/L (μm)
M ₁ , M ₃ , M ₅	10.0/0.5	M ₁ , M ₂ , M ₃ , M ₄	8.0/0.18
M ₂ , M ₄ , M ₆	10.0/0.8	M ₅ , M ₆ , M ₈	10.0*3/0.3
M ₇	2.5/0.8	M ₇	10.0*3/0.3
M ₈ , M ₁₀ , M ₁₃	5.0/0.8	M ₉	5.0*3/0.3
M ₉ , M ₁₁ , M ₁₄	5.0/0.5	M ₁₀	5.0*3/0.3
M ₁₂	1.25/0.8	I	400-μA
M ₁₅ , M ₁₆ , M ₁₈	5.0/0.5		
M ₁₇	1.0/1.0		
R	3.67-kΩ		

This charge pump design is being implemented in the frequency acquisition loop of the proposed CDR circuit and its layout is shown in Fig. 6.8. The charge pump circuit

is on the left portion of the layout and the right portion of the layout is the start-up and biasing circuit.

Figure 6.8. Layout of a single-ended output differential charge pump.

6.2.3 The Proposed Unbalanced Charge Pump Design

As the UP and DN pulse-widths have different duration and the number of UP signals are not the same as the number of DN signal for the phase detector in the phase tracking loop, an unbalanced charge pump is proposed to compensate for the differences. The charge pump must operate in such way that the net current flowing into or out of the low pass filter (LPF) is zero at locking state. As UP controls the current flowing into the LPF, I_{LPF_UP} , and DN controls the current flowing out of the LPF, I_{LPF_DN} , the operation of the charge pump at locking state must satisfy the following equation,

$$T_{H_UP} \cdot I_{LPF_UP} + T_{H_DN} \cdot I_{LPF_DN} = 0 \quad (6.1)$$

where T_{H_UP} and T_{H_DN} is the UP and DN pulse-widths of the proposed PD, respectively. Since T_{phase} is equal to half of T_{period} at locking state, by combining Eq. (4.4) and Eq. (4.5), the relationship between T_{H_UP} and T_{H_DN} is as follow

$$T_{H_UP} = 1.5 \cdot T_{H_DN} \quad (6.2)$$

if $T_{I/Q(latch)} + T_{I/Q(MUX)} = T_{C/Q(MUX)}$. Substituting Eq. (6.2) into Eq. (6.1), the current relationship is given by

$$I_{LPF_DN} = -1.5 \cdot I_{LPF_UP} \quad (6.3)$$

Figure 6.9. Schematic diagram of the proposed unbalanced charge pump.

Fig. 6.9 shows the schematic diagram of the proposed unbalanced charge pump. It uses source-coupled pairs to steer the current source. The current sources for both the UP signals are I and the current source for the DN signal is $1.5I$. The top-left current mirror will mirror the current flowing through the diode connected transistor to the LPF. Table 6.4 shows the truth table of the proposed unbalanced charge pump and it has to satisfy the

condition given by Eq. (6.3). When only one UP signal is high, $I_{LPF} = I_{LPF_UP}$ and this amount of current is set as a unit current, I_o . From Eq. (6.3), $I_{LPF_DN} = -1.5I_o$ and it coincides with the truth table given in Table 6.4. By comparing all the required I_{LPF} s with the values in the truth table, the charge pump accords with the condition imposed by Eq. (6.3).

Table 6.4. Truth Table of the Proposed Unbalanced Charge Pump.

UP ₁	UP ₂	DN	I _{UP}	I _{DN}	0.75I _{DN}	I _{LPF} = I _{UP} - 0.75I _{DN}	I _{LPF_UP1} +I _{LPF_UP2} +I _{LPF_DN} (in terms of I _o)
L	L	L	1.5I	2I	1.5I	0	0
L	L	H	0	3.5I	2.625I	-2.625I	-1.5I _o
L	H	L	2.5I	I	0.75I	1.75I	I _o
L	H	H	I	2.5I	1.875I	-0.875I	-0.5I _o
H	L	L	2.5I	I	0.75I	1.75I	I _o
H	L	H	I	2.5I	1.875I	-0.875I	-0.5I _o
H	H	L	3.5I	0	0	3.5I	2I _o
H	H	H	2I	1.5I	1.125I	0.875I	0.5I _o

*Shaded portions occur in the proposed PD

Table 6.5. The Current Flow of the Proposed Unbalanced Charge Pump at Different States.

State	T _{H_UP}	T _{H_DN}	I _{LPF_UP} × T _{H_UP} + I _{LPF_DN} × T _{H_DN}
Lock	1.5T	T	I _o × 1.5T + (-1.5I _o) × T = 0
Late	1.5T + ΔT	T	I _o × (1.5T + ΔT) + (-1.5I _o) × T = ΔT × I _o
Early	1.5T - ΔT	T	I _o × (1.5T - ΔT) + (-1.5I _o) × T = -ΔT × I _o

Table 6.5 provides the CP current flow at different states of the CDR. In the lock state, there will not be any net current flowing into or out of the LPF. In the case where the clock is late, the net current will flow into the LPF. And when the clock is early, the net current will flow out of the LPF.

Table 6.6 shows the design parameters of the unbalanced charge pump. The current source, I , is set to be $116.9\text{-}\mu\text{A}$. As the current of transistor M_{12} is only 0.75 times of the current of transistor M_{11} , the W/L ratio of transistor M_{12} is also 0.75 times the W/L ratio of transistor M_{11} . Fig. 6.10 shows the layout of the proposed unbalanced charge pump. The right portion of the layout is the start-up and biasing circuits for the current sources and its schematic diagram is shown in Fig. 6.7. The left portion of the layout is the proposed unbalanced charge pump shown in Fig. 6.9.

Table 6.6. Design parameters for the unbalanced charge pump.

Devices	W/L (μm)
$M_1, M_2, M_3, M_4, M_5, M_6$	8.0/0.18
M_7, M_8, M_9, M_{10}	10.0*3/0.3
M_{11}	5.0*3/0.3
M_{12}	3.75*3/0.3
I	$116.9\text{-}\mu\text{A}$

Figure 6.10. Layout of the proposed unbalanced charge pump.

Figure 6.11. I_{LPF} versus V_C with different input logic combinations.

In order to obtain the output current of the charge pump, a low pass filter has been connected to the output of the charge pump. Fig. 6.11 shows the simulation results of the proposed unbalanced charge pump under different input conditions. There are four input conditions, 1) only one UP signal is *high* and the other signals are *low*, 2) all input signals are *low*, 3) one UP signal and one DN signal are *high* and the other signal is *low*, 4) only DN signal is *high* and the other signals are *low*. In this simulation, the unit current of the unbalanced charge pump, I_o , is set to be 200- μ A. The highest curve is the output current, I_{LPF} , under first condition. According to Table 6.4, the amount of current is 200- μ A and the simulation result shows that I_{LPF} is around 200- μ A. The second highest curve is the I_{LPF} under second condition. Under this condition, the current should be 0- μ A as all input signals are *low*. The lowest curve is the I_{LPF} under fourth condition. From Eq. (6.3), the amount of current is -1.5 times the unit current (I_o) which is -300- μ A. The second lowest curve is the I_{LPF} under third condition and the amount of current is -100- μ A which is the

current summation of first condition and fourth condition. The simulation results shown in Fig. 6.11 shows that under different input conditions, the simulated I_{LPF} current is close to the theoretical I_{LPF} current. The simulation results also show that the working range of the output voltage, V_C , is between 0.3-V to 1.5-V.

Fig. 6.12 shows the transient simulation results of the proposed unbalanced charge pump. The top three signals are the input signals, UP_1 , UP_2 and DN respectively and the output signal, I_{LPF} , is shown at the bottom of the diagram. In Fig. 6.12, there are four different input conditions being highlighted. When all input signals are *high*, the simulation result shows that the output current, I_{LPF} , is around 100- μ A. This result matches with the theoretical result obtained from Table 6.4.

Figure 6.12. Transient simulation results of the unbalanced charge pump.

6.3 Voltage Controlled Oscillator (VCO)

6.3.1 Introduction to VCO

The oscillator is a self-sustaining circuit which uses positive feedback topology [82]. It has to generate a periodic signal from amplifying the noise inherent in the system. Fig. 6.12 shows the simple model of a feedback oscillator and its transfer function can be expressed as

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \quad (6.4)$$

Figure 6.12. Simple model of a feedback oscillator.

In order to ensure that the oscillator is able to oscillate at a given frequency, ω_o , it has to satisfy a well-known criterion, Barkhausen's criterion [83]. Its two main conditions are summarized as follow:

1) The open loop gain has to be greater than or equal to unity and it is expressed as

$$|H(j\omega_o)| \geq 1 \quad (6.5)$$

2) The total phase shift of the loop is 0° or 360° and it is expressed as

$$\angle H(j\omega_o) = 0^\circ \text{ or } \angle H(j\omega_o) = 360^\circ \quad (6.6)$$

It should be noted that the Barkhausen's criterion is essential but not sufficient because the observation of this criterion is based on the assumption of a linear model. The stability issues should also be taken into consideration. From the study of [84], it concludes that with Nyquist, root-locus analysis and the steady-state oscillation condition, the oscillator design will be more predictable and reliable. When these conditions are met, the oscillator is able to start its oscillation by the help of noises generated by the switch-on of the power supply or noises generated from the devices.

The VCO is not only capable of oscillating at a given frequency. It is able to oscillate at a range of frequency, depending on its control voltage. Fig. 6.13 shows the basic concept of a VCO [85]. It has an input control voltage, V_C , and an output periodic signal, ω_{OUT} . In an ideal case, ω_{OUT} is linearly dependent on the voltage level of V_C . Their relationship can be expressed as

$$\omega_{OUT} = \omega_o + K_{VCO} \cdot V_C \quad (6.7)$$

where ω_o is the free running frequency and K_{VCO} is the gain of the VCO.

Figure 6.13. Basic concept of a voltage controlled oscillator.

There are two main architectures for VCO: ring oscillator and LC oscillator. In the following sections, we will discuss more on these two architectures.

6.3.2 Ring VCO

Fig. 6.14 shows the block diagram of a single-ended ring VCO formed by N number of inverters. In order to satisfy the Barkhausen's criterion, N has to be an odd number. The frequency of a N-stage ring VCO is given as

$$f = \frac{1}{2NT_d} \quad (6.8)$$

where T_d is the delay of the inverter. Hence, the frequency of a VCO can be tuned by changing the delay of the inverter. For a differential ring VCO, the minimum number of block required is 2 [86, 87].

Figure 6.14. Block diagram of a single-ended ring oscillator.

The schematic diagram of a differential delay block is shown in Fig. 6.15. The two PMOS transistors operate in the triode region and their resistance values are controlled by V_C . As the time delay of the block is affected by the resistance values, by changing V_C , the frequency of the VCO can be tuned.

The advantage of the ring VCO is that it has a wide-tuning range than the LC VCO. Besides that, the ring VCO is able to provide multiphase output because the other outputs of the delay blocks also have the same frequency [88]. However, the phase noise of ring VCOs tend to higher than that of LC VCOs and the switching activities of the ring

VCO will also degrade the jitter performance [89]. Finally, ring VCOs tend to have higher power consumption than LC VCOs.

Figure 6.15. Schematic diagram of a differential delay block.

6.3.3 LC VCO

Figure 6.16. Simple LC tank.

LC tank is one of the core blocks for LC VCO and Fig. 6.16 shows the schematic diagram of a LC tank. The series resistor, R, is the parasitic resistance of the inductor coil and the quality factor, Q, can be expressed as

$$Q = \frac{\omega \cdot L}{R} \quad (6.9)$$

where ω is the frequency. For an ideal case, the inductor does not have any parasitic loss which means that R is equals to zero. Hence, Q is infinite. However, the on-chip inductor normally has a Q value from 3 to 20.

Due to the loss suffered by the LC tank, the oscillator will not be able to sustain its oscillation by the LC tank alone. In order to compensate for this loss, a cross-coupled pair shown in Fig. 6.17 is used together with the LC tank. By using small signal analysis, we can conclude that the cross-coupled pair has a negative impedance of $-2/g_m$ [22]. With a proper design of g_m , the cross-coupled pair will be able to compensate for the loss in the LC tank.

Figure 6.17. Schematic diagram of a cross-coupled pair.

Combining both the LC tank and cross-coupled pair, result in a simple cross-coupled LC VCO as shown in Fig. 6.18. The oscillator will resonate when the impedances of the capacitor and the inductor are the same. That is,

$$\frac{1}{\omega_o \cdot C} = \omega_o \cdot L \quad (6.10)$$

By rearranging Eq. (6.10) and substituting $\omega_o = 2\pi f_o$, the oscillating frequency can be expressed as [90]

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (6.11)$$

Figure 6.18. Schematic diagram of a conventional VCO.

Eq. (6.11) concludes that the oscillating frequency varies with respect to the inductance and capacitance. Hence, the oscillator can be tuned by either changing the inductance or the capacitance. For an on-chip inductor, it is not efficient to change the inductor value so the frequency can only be tuned by changing the capacitor value. In Fig. 6.18, the capacitor is replaced by two variable capacitors, also known as varactors. The control voltage, V_C , is connected between the two varactors so that their capacitance value can be changed. Hence, the frequency of the VCO can be tuned by V_C .

6.3.4 A Quadrature 1.25-GHz LC VCO

A quadrature clock is needed in the proposed CDR design. As the VCO shown in Fig. 6.18 is differential and only consists of two phases, an additional two phases are needed. Fig. 6.19 shows the schematic diagram of the quadrature VCO block. In this design, an additional PMOS cross-coupled pair is added. There is also an input to the circuit. The design parameters of the quadrature VCO block is shown in Table 6.7. The varactors, C_1 and C_2 , are implemented with NMOS varactor and their sizing is also provided in the table.

Figure 6.19. Schematic diagram of the quadrature VCO block.

Table 6.7. Design parameters for the quadrature VCO block.

Devices	W/L (μm)
M_1, M_2	8.0*18/0.18
M_3, M_4, M_5, M_6	8.0*9/0.18
M_7	9.0*16/0.5
C_1, C_2	4.5*8/5.0
L	11.35-nF (@1.25GHz)

The circuit in Fig. 6.19 can be modeled using small-signal analysis and its small-signal model is shown in Fig. 6.20(a) [91], where G_M is the transconductance of the differential pair, Z_T is the impedance of the tank and $-R$ is the negative resistance of the cross-coupled pair. To further analyze the principle of the quadrature VCO, two identical quadrature VCO blocks are coupled together and its block diagram is shown in Fig. 6.20(b).

Fig. 6.20(c) shows the small-signal model of the two coupled VCO blocks. From the small-signal analysis, we have

$$G_{M1}V_{IN1} \cdot (-R // Z_T) = V_{OUT2} \quad (6.12)$$

$$\& \quad G_{M2}V_{IN2} \cdot (-R // Z_T) = V_{OUT1}. \quad (6.13)$$

By equating Eq. (6.12) and Eq. (6.13), the final equation is obtained as

$$G_{M1}V_{IN1}^2 - G_{M2}V_{IN2}^2 = 0. \quad (6.14)$$

Figure 6.20. (a) Small-signal model of a quadrature VCO block, (b) Block diagram of two coupled VCO blocks and (c) Small-signal model of two coupled VCO blocks.

Figure 6.21. Block diagram of a quadrature VCO.

In Eq. (6.14), there are two importance parameters G_{M1} and G_{M2} . For the condition $G_{M1} = G_{M2}$, we have $V_{IN1} = \pm V_{IN2}$. This means that the phase difference between the two VCOs is either 0° or 180° . For the condition $G_{M1} = -G_{M2}$, we have $V_{IN1} = \pm j V_{IN2}$, which means that the phase difference is now either -90° or 90° . Hence, a quadrature VCO can be implemented with this condition. Fig. 6.21 shows the block diagram of a quadrature VCO [92, 93]. The output of the second VCO block is negative feedback to the first VCO block. With this negative feedback, a negative sign is generated and hence the VCO satisfies the condition $G_{M1} = -G_{M2}$.

Figure 6.22. Schematic diagram of the clock buffer.

Fig. 6.22 shows the schematic diagram of the clock buffer [54]. It helps to increase the driving power of the VCO. Besides that, the clock buffer also acts as a band-pass filter to remove the unwanted low frequency noise caused by interference and the high frequency harmonics of the VCO. The biasing circuit in the middle provides bias voltage that is close to the threshold voltage of the inverter. The design parameters of the clock buffer are shown in Table 6.8. Another two stages of inverter are included to ensure the driving capability of the clock buffer.

Table 6.8. Design parameters for the clock buffer.

Devices	W/L (μm)
M_1, M_3, M_5	2.795/0.18
M_2, M_4, M_6	1.0/0.18
C_1, C_2	0.5-pF
C_3, C_4	0.1-pF
R_1, R_2	10-k Ω

6.3.5 Comparisons and Discussions

Figure 6.23. Layout of the quadrature VCO.

Fig. 6.23 shows the layout of the quadrature VCO. It consumes a total area of $500 \times 1200\text{-}\mu\text{m}^2$. The inductors are on both the left and the right sides and the core circuit is at the middle. The clock buffer is located at the bottom of the layout.

Fig. 6.24 shows the tuning range of the quadrature VCO. It has a tuning range of 290-MHz (20%) and it can operate from 1.31-GHz to 1.6-GHz. The VCO is overdesigned to compensate for the additional parasitic that is not modeled in the simulation.

Figure 6.24. Tuning range of the quadrature VCO.

Fig. 6.25 shows the phase noise plot of the VCO at the free running frequency. The VCO has phase noise of -104.4-dBc/Hz at 1-MHz offset. The output waveforms of the VCO after passing through the clock buffer are shown in Fig. 6.26. At a supply voltage of 1.8-V, the core circuit of the VCO consumes 7-mW and the clock buffer consumes 6.6-mW of power.

Figure 6.25. Phase noise of the quadrature VCO.

Figure 6.26. Simulation results of the quadrature VCO.

The comparison table for the VCO design is shown in Table 6.9. The performance of the VCOs in the first three rows is better than the others. This is mainly because the

VCOs in the first three rows are standalone VCO design and the others are the VCO design which is integrated in CDR systems. For the integration, the VCO design has to optimize between its driving capabilities, tuning range, power consumption and phase noise. Comparing among the integrated VCO designs, this work achieves the minimum power consumption with a moderate trade-off in term of phase noise. The tuning range of this work is also fixed around 20%.

Table 6.9. Comparison table for VCO design.

	Technology	Supply Voltage (V)	f_o (GHz)	Power (mW)	Tuning Range	Phase Noise (dBc/Hz) @1-MHz
[94]	0.18- μ m CMOS	1.2	5	6.4	6%	-114
[95]	0.18- μ m BiCMOS	1.3	2	11.05	14%	-120
[96]	0.18- μ m CMOS	1.8	2.18	4.14	7.3%	-117.13
[37]	0.18- μ m CMOS	1.8	6.6	-	15%	-103.18
[97]	0.18- μ m CMOS	1.8	5	30.6	20%	-86
[54]	0.13- μ m CMOS	1.2	2.5	12	19%	-110
This work	0.18- μ m CMOS	1.8	1.45	7	20%	-104.4

7 Architecture Components: Phase Frequency Detector, Frequency Divider & Lock Detector

7.1 Phase Frequency Detector (PFD)

7.1.1 PFD Architecture

The phase frequency detector (PFD) has the ability to detect the phase difference and the frequency difference. The PFD has a supreme performance in lock range as its range is unbounded. Fig. 7.1 shows the block diagram of the phase frequency detector [98, 99]. It is formed by a AND gate and two D-FFs. The two D-FFs are clocked by REF and DIV.

Figure 7.1. Block diagram of the phase frequency detector.

The PFD is triggered by the rising edge of the clock. When the PFD detects the rising edge of REF, the UP signal becomes *high*. When the PFD detects the rising edge of DIV, the DN signal becomes *high*. However, when both the UP and DN signals are *high*, the PFD resets the D-FFs and eventually both the UP and DN signals become *low*. There are four possible states for the PFD and they are listed below:

- 1) UP = 0, DN = 0
- 2) UP = 1, DN = 0
- 3) UP = 0, DN = 1
- 4) UP = 1, DN = 1

The fourth state can be combined with the first state because when both the UP and DN signals are *high*, the D-FFs will be reset and both the UP and DN signals become *low*. The state diagram of the PFD is shown in Fig. 7.2 [100]. The PFD will start with an initial state where both the UP and DN signals are *low*.

Figure 7.2. State diagram of the phase frequency detector.

There are two main operations for the PFD: phase tracking and frequency tracking. First, we will be discussing on its phase tracking operation, in which the frequency of both REF and DIV is the same. For the case of REF leading DIV as shown in Fig. 7.3(a), the rising edge of REF occurs before the rising edge of DIV. The UP signal has a wider pulse-width than the DN signal. Hence, charge pump current will flow into the LPF and causing the VCO control voltage, V_C , to increase. As a result, the frequency of the VCO increases, which also increase the frequency of DIV. The phase difference between REF and DIV will decrease. The opposite of the above effects will take place when REF lags DIV, as shown in Fig. 7.3(b). Fig. 7.4 shows the timing diagrams when

both the frequency of REF and DIV is different. If REF has a higher frequency than DIV (Fig. 7.4(a)), the PFD output will remain in the UP state for a longer period. Hence, the DIV frequency will be increased. In Fig. 7.4(b), the frequency of REF is lower than the frequency of DIV.

Figure 7.3 Timing diagrams of the PFD when (a) REF leads DIV and (b) DIV leads REF.

Figure 7.4 Timing diagrams of PFD when REF frequency is (a) greater and (b) smaller than DIV frequency.

The characteristic curve of the PFD is shown in Fig. 7.5 [101]. The x-axis represents the phase difference between REF and DIV, and the y-axis represents the charge pump current flowing through the LPF, I_{LPF} . The positive phase difference means that REF leads DIV and the negative phase difference means that DIV leads REF. We can see that I_{LPF} is linearly proportional to the phase difference. When there is no phase difference, I_{LPF} will be zero.

Figure 7.5. Characteristic curve of the phase frequency detector.

“Dead zone” is one of the issues for the PFD. It occurs when the phase difference between REF and DIV is very small, as shown in Fig. 7.6. When the phase difference is small, the pulse-width of the UP or DN signal will also be small. If the pulse width of the UP or DN signal is smaller than the reaction time of the charge pump, no current will flow through the LPF.

To circumvent the “dead zone” issue, a delay block can be inserted in to the feedback loop between the AND gate output and the Reset inputs of the D-FFs [102, 103]. Fig. 7.7 shows the block diagram of the modified PFD. With the insertion of the delay block, the pulse-width of the UP and DN signals can be increased. The delay time

of the delay block will determine the pulse duration to be added to the UP and DN signals.

Figure 7.6. Dead zone of the phase frequency detector.

Figure 7.7. Block diagram of the modified phase frequency detector.

7.1.2 Results and Discussion

Fig. 7.8 shows the layout of the PFD. It consumes a total area of $85 \times 135 \mu\text{m}^2$. The D-FF is implemented using NAND gates. In order to have a differential output for the differential input of the CP, all the gates in the PFD are implemented with differential cascode voltage switch logic (DCVSL) architecture [104, 105].

Figure 7.8. Layout of the phase frequency detector.

Fig. 7.9 shows the simulation results of the PFD when both the frequency and phase difference of REF signal and DIV signal are zero. Due to the insertion of delay block shown in Fig. 7.7, the pulse-width of both the UP and DN signals are widened. The increase of pulse-width is proportional to the delay. In this work, the delay block has the delay of two inverters. Fig. 7.9 also shows that the pulse-width of UP and DN signals are the same. Hence, the total charge pump current flowing into the LPF is zero which is the locked condition.

Figure 7.9. Simulation results of the PFD when both the frequency and phase difference are zero.

To further verify the functionality of the PFD, it is also simulated under the condition where REF signal leads DIV signal. The simulation results are shown in Fig. 7.10. In this condition, the pulse-width of the UP signal is wider than the pulse-width of the DN signal. As the UP signal controls the charge pump current flowing into the LPF and DN signal controls the charge pump current flowing out of the LPF, there is a total charge pump current flowing into the LPF under this condition. Hence, the frequency of DIV signal will be increased which will cause a reduction in the phase difference between both REF and DIV signals.

Figure 7.10. Simulation results of the PFD when REF leads DIV.

Fig. 7.11 shows the simulation results of the PFD when the frequency of REF signal is higher than the frequency of DIV signal. Similar to previous condition, the pulse-width of UP signal is larger than the pulse-width of DN signal. However, under this condition, the total pulse-width of UP signal is larger and the pulse-width of UP signal for each cycle is different. This is mainly due to the difference in frequency between REF signal and DIV signal. As the total pulse-width of UP signal is still larger than the total pulse-width of DN signal, there will be a total charge pump current flowing into the LPF. This will cause the frequency of DIV signal to increase which helps to minimize the frequency difference between DIV signal and REF signal.

Figure 7.11. Simulation results of the PFD when REF has a higher frequency than DIV.

Figure 7.12. Characteristic curve of the PFD.

Fig. 7.12 shows the characteristic curve of the PFD. When the phase difference is positive, which is REF signal leads DIV signal, there is a total charge pump current flowing into the LPF. When the phase difference is negative, which is REF signal lags DIV signal, there is a total charge pump current flowing out of LPF. The charge pump current has a linear relationship with respect to phase difference. As there is a delay block inserted into the PFD, there is no dead zone found in the characteristic curve.

7.2 Frequency Divider

7.2.1 Frequency Divider Architecture

Frequency divider is also often known as a prescaler. It divides the input frequency by N where N is an integer. The relationship between the input and output frequency can be expressed as

$$f_{CLK_{OUT}} = \frac{f_{CLK_{IN}}}{N}. \quad (7.1)$$

D-FF is the main building block in the prescaler. The block diagram of a simple divide by 2 prescaler is shown in Fig. 7.13(a) [106]. The input of the prescaler is connected to the clock of the D-FF and the output of the prescaler is the inverted output of the D-FF. In order to reduce the frequency by half, the inverted output of the D-FF must be connected back to the input of the D-FF. Fig. 7.13(b) shows the timing diagrams of the prescaler. CLK_{OUT} will only change its value at the rising edge of CLK_{IN}. Hence, the frequency of CLK_{OUT} is half the frequency of CLK_{IN}.

Figure 7.13. (a) Block diagram and (b) timing diagrams of a divide by 2 prescaler.

A divide by 2^N prescaler can be implemented by cascading N number of divide by 2 prescaler. Fig. 7.14 shows the block diagram of a divide by 16 prescaler. It is formed by cascading four divide by 2 prescaler in series. The first stage divides the frequency of CLK_{IN} by 2 and the second stage further divides the CLK_{IN} frequency by 4. At the third stage output, the frequency will be CLK_{IN} divided by 8 and the frequency of the last stage will be 16 times smaller than the CLK_{IN} frequency.

Figure 7.14. Block diagram of a divide by 16 prescaler.

The D-FF is implemented with true single phase clock (TSPC) architecture. The schematic diagram of the TSPC D-FF is shown in Fig. 7.15 [107]. The last stage of the D-FF is an inverter so that the inverted output can be fed back to the input of the D-FF.

Figure 7.15. Schematic diagram of a TSPC D-FF.

7.2.2 Results and Discussion

The layout of the divide by 16 prescaler is shown in Fig. 7.16. It consumes a total area of $15 \times 115 \mu\text{m}^2$ and its design parameters are shown in Table 7.1. The length of the transistors in the last stage has been increased as compared to other stages. This increase in the transistors length is to increase the output delay of the TSPC D-FF. Without this increase in delay, the D-FF of the last stage is not able to function correctly because the clock of the last stage has longer rise/fall time.

Figure 7.16. Layout of the divide by 16 prescaler.

Table 7.1. Design parameters for TSPC D-FF.

First three stages		Last stage	
Devices	W/L (μm)	Devices	W/L (μm)
M_1, M_2	4.0/0.18	M_1, M_2	4.0/0.30
M_3	1.0/0.18	M_3	1.0/0.30
M_1 to M_9	2.0/0.18	M_1 to M_9	2.0/0.30
M_{10}	2.0/0.18	M_{10}	2.0/0.18
M_{11}	1.0/0.18	M_{11}	1.0/0.18

Figure 7.17. Simulation results of the divide by 16 prescaler.

Fig. 7.17 shows the simulation results of the divide by 16 prescaler. The top waveform is the input signal, CLK_{IN} , and the bottom waveform is the output signal, CLK_{OUT} . The waveforms in between the input signal and output signal are the

intermediate signals. As each stage functions as a divide by 2 prescaler, the output clock period of each consecutive stage will be increased by 2. For the last stage, the CLK_{OUT} signal will toggle after every eight cycles of CLK_{IN} signal.

7.3 The Proposed Lock Detector (LD)

In dual-loop CDR architecture, the lock detector (LD) [108, 109] acts as a vital role to control the switching between the frequency acquisition loop and the phase tracking loop. Initially, as the frequency of the VCO is further away from the operating frequency, the LD will enable the frequency acquisition loop. The frequency acquisition loop will track the VCO frequency so that it can be within a certain range of the required operating frequency. When the VCO frequency falls within the frequency range, the LD will switch to the phase tracking loop. The loop will continue to track the frequency and phase of the VCO and provides a recovered clock. The LD will only switch back to the frequency acquisition loop when the VCO frequency is being interrupted and is out of the frequency range.

One of the problems in the conventional LD architecture is that there is only one required frequency range to switch between the frequency acquisition loop and the phase tracking loop [110-112]. The setting of the required frequency range has been a challenging task for the designer. When the required frequency range is set to be small, the frequency acquisition loop will track the VCO frequency to a closer operating frequency. This helps to shorten the lock time of the CDR. However, when the phase tracking loop is in use, the VCO frequency may easily go out of the required frequency

range if it is set to be too small. The outcome is an inadvertent switching back to the frequency acquisition loop. Instead of having a shorter lock time, the CDR will now take a longer time to lock due to more switchings between the frequency acquisition loop and the phase tracking loop. However, if the required frequency range is set to be large, the phase tracking loop will have a longer lock time as the VCO frequency is further away from the operating frequency.

7.3.1 The Proposed LD Architecture

In order to circumvent the problem of having only one required frequency range, a LD with hysteresis property is proposed in this work. It provides two different required frequency ranges for two different conditions. The first condition is that the proposed LD will have a smaller required frequency range to switch from the frequency acquisition loop to the phase tracking loop (in-lock condition). The second condition is that the proposed LD will have a larger required frequency range to switch from the phase tracking loop to the frequency acquisition loop (out-of-lock condition).

Fig. 7.18 shows the block diagram of the proposed LD architecture. It is composed of two N-bit counters, three D-FFs and a few logic gates. The main purpose of the counter is to count the number of clock cycle of the reference clock (REF) and the output of the prescaler (DIV) respectively. The pass-transistor logic after the counter is to control the hysteresis property of the LD circuit. The decision logic circuit at the bottom of Fig. 7.18 helps to decide whether the frequency is lock or not.

Figure 7.18. Block diagram of the proposed LD.

The main concept of the proposed LD architecture is that during the in-lock condition, both the N-bit counters with REF and DIV inputs will start counting the number of cycles of each clock. The logic circuit will then compare the values of both counters. If either one of the counters reaches the count of $2^{N-1} + 1$ while the other count is still smaller than 2^{N-1} , then the output of the OP gate, C, will become one which means that the frequency of the VCO is still out of the frequency range. A small reset pulse, R,

will then occur and cause the output signal, LOCK, to go low. Both the counters will reset and count the number of clock cycles again. The whole process will repeat until the other count is greater than or equal to 2^{N-1} . The timing diagrams of the in-lock condition are shown in Fig. 7.19.

Figure 7.19. Timing diagrams of the proposed LD under in-lock condition.

As for the out-of-lock condition, the pass transistor logic will then increase the number of cycle count. Instead of comparing the cycle number of $2^{N-1} + 1$, the logic circuit is now comparing the cycle number of $2^{N-1} + 2^k$, where k is an integer. Due to this increase in number, the required frequency range is increased for out-of-lock condition.

Fig. 7.20 shows the timing diagrams for out-of-lock condition.

Figure 7.20. Timing diagrams of the proposed LD under out-of-lock condition.

7.3.2 Analysis of the Proposed LD

For the in-lock condition, the logic circuit compares both cycle number of 2^{N-1} and $2^{N-1} + 1$. In order to obtain a logic *high* for the LOCK signal, the period of the VCO has to satisfy the following conditions,

$$(2^{N-1} + 1) \cdot T_{REF} \geq 2^{N-1} T_{DIV} \quad (7.2)$$

and
$$(2^{N-1} + 1) \cdot T_{DIV} \geq 2^{N-1} T_{REF} \quad (7.3)$$

where T_{REF} and T_{DIV} are the period of REF and DIV respectively. By combining these two conditions, the frequency range of DIV and the VCO for the in-lock state is given as follow,

$$\frac{2^{N-1}}{(2^{N-1} + 1)} f_{REF} \leq f_{DIV} \leq \frac{(2^{N-1} + 1)}{2^{N-1}} f_{REF} \quad (7.4)$$

$$\frac{2^{N-1}}{(2^{N-1} + 1)} f_{lock} \leq f_{VCO} \leq \frac{(2^{N-1} + 1)}{2^{N-1}} f_{lock} \quad (7.5)$$

where f_{lock} is the required range of the VCO frequency. When N is equal to 12, the required ppm for in-lock condition will be around ± 488 -ppm and Eq. (7.5) can be rewritten as

$$0.999512 f_{lock} \leq f_{VCO} \leq 1.000488 f_{lock} \quad (7.6)$$

In order for the lock detector to change its operation from in-lock to out-of-lock, the cycle number of $2^{N-1} + 2^k$, where k is an integer, is used as a reference instead of $2^{N-1} + 1$. Hence, the frequency range will be larger and is given by

$$\frac{2^{N-1}}{(2^{N-1} + 2^k)} f_{lock} \leq f_{VCO} \leq \frac{(2^{N-1} + 2^k)}{2^{N-1}} f_{lock} \quad (7.7)$$

As the value of N has been set by the required ppm of the in-lock state, the ppm for the out-of-lock state is now set by the value of k. If the value of k is chosen to be 2, the required ppm will be around ± 1950 -ppm and Eq. (7.7) can be rewritten as

$$0.99805 f_{lock} \leq f_{VCO} \leq 1.00195 f_{lock} \quad (7.8)$$

7.3.3 Results and Discussion

Fig. 7.21 shows the layout of the proposed LD. It consumes a total area of $120 \times 425 \text{-}\mu\text{m}^2$. The N-bit counter is implemented with the transmission gate architecture and the logic gates are implemented with static complementary CMOS technology.

Figure 7.21. Layout of the proposed LD.

Figure 7.22. Simulation results of the proposed LD under in-lock condition.

Figure 7.23. Simulation results of the proposed LD under out-of-lock condition.

Fig. 7.22 shows the simulation results for the in-lock condition. The REF signal first reaches the cycle number of 2^{11} . After half of the cycle, the DIV signal also reaches the cycle number of 2^{11} . As both signals A_{11} and B_{11} are *high*, a pulse is then occurs in signal C. This will cause a rise in signal R which leads to a *high* for the LOCK signal. Fig. 7.23 shows the simulation results for the out-of-lock condition. The DIV signal first reaches the cycle number of 2^{11} . After four cycle of DIV signal, the cycle number of REF signal still has not reaches 2^{11} . This will also triggered a pulse for signal C. With a *high* in signal C, the signal R will also rise. Under this condition, the output signal LOCK will output a *low*.

Figure 7.24. Simulation results of the proposed LD.

In order to further ensure the functionality of the proposed LD, it is simulated in a dual-loops CDR. The simulation results are shown in Fig. 7.24. Initially, as the VCO frequency is very far away from the operating frequency, the LOCK signal is *low* to enable the frequency acquisition loop to track the VCO frequency. As the frequency of the VCO is being locked, the LOCK signal changes to *high*. The control voltage, V_C , is constant and the phase tracking loop will now take over to track the phase and recover the clock. However, when the control voltage is interrupted, the LOCK signal will go *low* and the frequency acquisition loop will take over to track the frequency again.

8 A Fully Integrated 5-Gb/s Dual-Loops Quarter-Rate CDR

8.1 Loop Filter Design

The loop filter is a crucial part in the CDR design. It determines the stability and loop dynamic of the CDR. A third-order loop filter is implemented in this CDR design and the fundamentals of a third-order loop filter is discussed in section 2.5.2. The third-order loop filter (shown in Fig. 2.12(c)) consists of two capacitors, C_p and C_s , and a series resistor, R_s . Rewriting Eq. (2.13), for a given phase margin, Φ_M , the ratio of C_s and C_p can be found and is expressed as

$$\frac{C_s}{C_p} = 2 \left(\tan^2 \Phi_M + \tan \Phi_M \sqrt{\tan^2 \Phi_M + 1} \right). \quad (8.1)$$

For a phase margin of 70° , the ratio C_s/C_p is approximately 31.16.

From the open loop transfer function, in Eq. (2.10), the zero and the third pole can be expressed as

$$\omega_z = -\frac{1}{R_s C_s} \quad (8.2)$$

and

$$\omega_{p3} = -\frac{1}{R_s \cdot \left(\frac{C_s C_p}{C_s + C_p} \right)}. \quad (8.3)$$

In order to calculate the maximum phase margin, we can differentiate Eq. (2.12) and equate it to zero. With some mathematical manipulation, the condition for maximum phase margin is given as

$$\omega_{UGB} = \omega_z \sqrt{1 + \frac{C_s}{C_p}}. \quad (8.4)$$

By re-arranging Eq. (8.4), we can get ω_z from a given unity gain bandwidth, ω_{UGB} , and in term of the ratio of the capacitances in Eq. (8.1).

Figure 8.1. Bode plot of maximum phase margin.

Fig. 8.1 shows the bode plot of the open-loop transfer function when the phase margin is at a maximum. By equating Eq. (8.2) and Eq. (8.3), the relationship between ω_{p3} and ω_z can be expressed as

$$\omega_{p3} = \omega_z \left(1 + \frac{C_s}{C_p} \right). \quad (8.5)$$

Hence, the third pole of the open-loop transfer function can be found as the ω_z value is determined from Eq. (8.4).

To calculate the value of capacitances and resistance, we have to solve the equation of unity gain bandwidth, which is written as

$$|H_o(j\omega_{UGB})| = 1 \quad (8.6)$$

From Eq. (2.10), we can rewrite Eq. (8.6) as

$$\left| \frac{K_{VCO} I_P}{2\pi} \cdot \frac{j\omega_{UGB} + \frac{1}{R_s C_s}}{(j\omega_{UGB})^2 C_p \left(j\omega_{UGB} + \frac{C_s + C_p}{R_s C_s C_p} \right)} \right| = 1 \quad (8.7)$$

By solving Eq. (8.7), C_p can be expressed as

$$C_p = \frac{K_{VCO} I_P}{2\pi \cdot \omega_{UGB}^2} \cdot \sqrt{\frac{\omega_{UGB}^2 + \omega_z^2}{\omega_{UGB}^2 + \omega_{p3}^2}} \quad (8.8)$$

With C_p , the value of C_s can be found from Eq. (8.1). By rearranging Eq. (8.2), R_s can be expressed as

$$R_s = \frac{1}{\omega_z C_s} \quad (8.9)$$

Hence, with a proper choice of phase margin, Φ_M , and unity gain bandwidth, ω_{UGB} , all the capacitance and resistance values can be calculated.

As the CDR will operate in the phase tracking loop for most of the time, this loop will directly influence the performance of the CDR. Hence, we will look at the parameters of the loop filter in influencing the performance of the phase tracking loop. For loop filter calculation, two additional constants, K_{VCO} and I_p , are required. From section 6.3.4, the gain of the VCO, K_{VCO} , is approximately 0.25-GHz/V. The charge pump current, I_p , is set to approximately 200- μ A. For the condition $\Phi_M = 70^\circ$ and $\omega_{UGB} = 2\pi \times 1.5$ -MHz, the loop filter parameters are calculated as $C_p = 15.8$ -pF, $C_s = 492.3$ -pF and $R_s = 1222$ - Ω . Fig. 8.2 shows the bode plot of the open-loop transfer function of the phase tracking loop. The

phase margin is at its maximum value. To further analyse the system, the bode plot of the closed-loop transfer function phase tracking loop is obtained as shown in Fig. 8.3. The -3-dB bandwidth is 2.07-MHz and the jitter peaking is 1.06-dB.

Figure 8.2. Bode plot of the open-loop transfer function of the phase tracking loop.

Figure 8.3. Bode plot of the closed-loop transfer function of the phase tracking loop.

As the frequency acquisition loop and the phase tracking loop share the same loop filter, the frequency acquisition loop will not be able to change the loop filter parameters that were previously designed for the phase tracking loop. As the frequency acquisition loop has an additional frequency divider block, its open-loop transfer function can be expressed as

$$H_{open}(s) = \frac{I_{p1} K_{VCO}}{2\pi N} \cdot \frac{1}{C_p s^2} \cdot \frac{s + \frac{1}{R_s C_s}}{s + \frac{1}{R_s \cdot \left(\frac{C_s C_p}{C_s + C_p} \right)}}. \quad (8.10)$$

From Eq. (8.10), there are two parameters which we can vary, N and I_{p1} . In this CDR design, N is set to be 16. In order to compensate for the value N , the charge pump current, I_{p1} , for the frequency acquisition loop has to be increased. In this case, its value is increased to four times of the initial value which is 800- μ A.

Figure 8.4. Bode plot of the open-loop transfer function of the frequency acquisition loop.

Fig. 8.4 shows the bode plot of the open-loop transfer function of the frequency acquisition loop. As the overall magnitude of the open-loop is being shifted down, the phase margin of the frequency acquisition loop is being shifted to the left. The phase margin of the frequency acquisition loop is 55.9°. The bode plot of the closed-loop transfer function of the frequency acquisition loop is shown in Fig. 8.5.

Figure 8.5. Bode plot of the closed-loop transfer function of the frequency acquisition loop.

8.2 5-Gb/s Dual-Loops CDR

The proposed dual-loops CDR circuit is fabricated using Global-foundries' 0.18- μm RF CMOS process. Fig. 8.6 shows the microphotograph of the die which it consumes a total area of $1.9 \times 2.3\text{-mm}^2$ including the pads. The top pads of the die are for the input reference signal, REF, which is used in the frequency acquisition loop and the bottom pads of the die are for the input data signal, D_{in} , and the DC biasing voltage. The pads on

the left are for the output signals, CLK0, CLK90, CLK180, CLK270 and the pads on the right are for the output data signals, D_{out} , D_{out1} , D_{out2} , D_{out3} , D_{out4} .

Figure 8.6. Microphotograph of the proposed quarter-rate CDR circuit.

The overall setup for the measurement equipment is shown in Fig. 8.7(a). The probing station is at the middle of the picture and the equipments are on both sides of the picture. Fig. 8.7(b) shows the block diagram of the measurement setup. The inputs of the circuit are generated with Agilent J-BERT N4903A and signal generator. The J-BERT is used to provide a 5-Gb/s input with a data pattern of $2^{31}-1$ PRBS and the signal generator is used to provide a 78.125-MHz reference clock, REF. The outputs of the circuit are measured with JBERT, oscilloscope (LeCroy Wavemaster 8600A) and Agilent Spectrum Analyzer E4407B. The bit-error-rate (BER) is measured by connecting the output of the MUX, D_{out} , to the J-BERT. The eye diagram of the recovered clock and the retimed data are measured with the oscilloscope. The spectrum of the VCO is measured by the spectrum analyzer.

(a)

(b)

Figure 8.7. (a) Probing station and measurement equipment setup, (b) Block diagrams of the measurement setup.

The spectrum of the VCO is shown in Fig. 8.8 and the measured phase noise at 1-MHz offset is -95.2 dBc/Hz. The eye diagram of the recovered clock is shown in Fig. 8.9

and it has a peak-to-peak jitter of 30.4-ps. Fig. 8.10 shows the eye diagram of the recovered parallel data (DEMUX) with a $2^{31} - 1$ PRBS input. Due to the design error in the MUX shown in Fig. 6.1, the output signal of the MUX, D_{out} , is not able to function. Hence, we are not able to measure the BER value.

Figure 8.8. Measured phase noise of the VCO at 1-MHz offset.

The whole CDR circuit consumes a total power of 71.9-mW from a 1.8-V supply. This measured power is close to the simulated power which is 71.28-mW. The PD circuit is overdesigned for a data rate of 6.5Gb/s and its power consumption is 44.4-mW. The VCO consumes 7-mW and its clock buffer driving the PD and frequency divider consumes 6.6-mW. The data recovery circuit and other parts of the circuit consume 8-mW and 6.3-mW respectively.

Figure 8.9. Eye diagram of the recovered clock.

Figure 8.10. Eye diagram of the recovered parallel data (DEMUX).

Table 8.1. Performance Comparison of Lower Rate CDRs.

	[55]	[15]	[37]	[52]	[34]	[54]	[113]	This Work
Technology	-	0.25- μm	0.25- μm	0.18- μm	0.18- μm	0.13- μm	0.18- μm	0.18- μm
Data Rate	-	5-Gb/s	4-Gb/s	4-Gb/s	5-Gb/s	10-Gb/s	6-Gb/s	5-Gb/s
Type of PD	Linear	Linear	Linear	Linear	Linear	Linear	Linear	Linear
Supply	-	2.5V	2.5V	1.8V	1.8V	1.2V	1.8V	1.8V
Rate of PD	1/4 rate	1/8 rate	1/8 rate	1/4 rate	1/8 rate	1/4 rate	1/4 rate	1/4 rate
Building Blocks	4 2-phase Latches 4 D-FFs 2 4-inputs XOR	16 Latches 8 XOR gates 2 4-inputs XOR	8 Latches DCT ^a Detector ^b DCT ^a Generator	4 Latches 6 MUX cells 3 XOR gates	16 Latches 16 AND gates 16 XOR gates	4 Latches 8 AND gates 3 XOR gates	4 Latches 8 AND gates 3 XOR gates	4 Latches 4 MUX cells 4 XOR gates
Output Signals	1 UP pulses 1 DN pulses	1 UP pulses 1 DN pulses	1 UP pulses 1 DN pulses	2 UP pulses 1 DN pulses	8 UP pulses 8 DN pulses	4 UP pulses 4 DN pulses	4 UP pulses 4 DN pulses	2 UP pulses 1 DN pulses
UP-pulse widening	No	No	No	No	Yes	Yes	Yes	Yes
Power (CDR)	-	130-mW	70-mW	-	144-mW	120-mW	210.6-mW	71.9-mW
Power per Gb/s	-	26-mW	17.5-mW	-	28.8-mW	12-mW	35.1-mW	14.38-mW
Frequency Loop	-	No	No	-	Yes	Yes	Yes	Yes
Clock Jitter (peak-to-peak)	-	40-ps	47-ps	-	57.4-ps	15.6-ps	15.57-ps	30.4-ps
DEMUX	-	1:4	1:4	-	1:8	1:4	1:4	1:4
DEMUX Phase Align	-	No	No	-	No	Yes	-	Yes
Active Area	-	1.7 $\times$ 1.4 mm ²	0.9 $\times$ 1.0 mm ²	-	0.6 $\times$ 1.1 mm ²	3 $\times$ 3.4 mm ²	1.0 $\times$ 1.3 mm ²	1.9 $\times$ 2.3 mm ²

^a Data & Clock Transition (DCT)^b DCT Detector is made up of 4 MUX cells and 8 XOR gates

Table 8.1 shows the performance comparison of the proposed CDR with existing CDRs. The total number of building blocks for the proposed PD design is 12 which achieves the least number of building blocks among the best reported lower-rate PDs.

Besides that, among the linear PD with UP pulse widening technique, the proposed PD also has the least number of output signals. This will reduce the number of charge pump circuits needed for the whole CDR circuit which will translate into a reduction in power consumption and current mismatch due to the charge pump circuit.

In terms of power efficiency, the proposed CDR consumes 14.38-mW/Gbps. Compared to other CDRs implemented in 0.18- μ m technology; its power efficiency is improved. In order to ensure the reliability of the CDR circuit, it is also simulated under the fast-fast (FF) and slow-slow (SS) conditions. Under FF condition, the proposed CDR consumes a total power of 78.44-mW which translates to a power efficiency of 15.69-mW/Gbps. Under SS condition, the proposed CDR consumes a total power of 64.7-mW which translates to a power efficiency of 12.94-mW/Gbps. The percentage change of the power efficiency from the typical condition is within 10% for both FF and SS conditions. From the measurement result of 5 dies, all the power efficiency fall within the range of FF and SS conditions.

As the clock jitter performance varies with the data rate, the proposed CDR has the best jitter performance among all the existing CDRs with the same data rate. From the measurement result of 5 dies, the maximum peak-to-peak clock jitter is 32.1-ps and the minimum peak-to-peak clock jitter is 30.4-ps.

9 Conclusions & Recommendations

9.1 Conclusions

This thesis explored on a lower-rate power efficient linear CDR design. The realization of a CMOS 5-Gb/s dual-loops quarter-rate CDR circuit was presented. This section summarizes the key contributions of this thesis.

A new quarter-rate linear PD is proposed in this thesis. The proposed PD has the advantage in reducing circuit complexity. Among the existing quarter-rate linear PDs, the proposed PD has the least number of building blocks which only consists of 4 D-latches, 4 MUXs and 4 XOR gates. In addition, the proposed PD employed an UP pulse-widening technique to circumvent the problem of existing narrow UP pulses. It also has the least number of output signals among all the other linear PDs with UP pulse-widening technique.

A detailed propagation delay analysis of the proposed PD was carried out and equations were derived to predict the characteristic curve of the proposed PD. The percentage error of the prediction in the linear region is about 2%. Furthermore, the effect of propagation delay on the UP and DN pulse-widths at various phase differences was also being explored for a more in-depth study.

We have proposed a quarter-rate DEMUX architecture that has superior performance in power as compared to the conventional “tree” DEMUX architecture. The

proposed DEMUX is composed of 14 D-latches and is able to function at a data rate of 10-Gb/s. It consumes a total power of 6.98-mW at a supply voltage of 1.8-V. The phase margin for the proposed DEMUX at 10-Gb/s is 72-ps. The vertical and horizontal eye opening for the de-multiplexed data is 374-ps and 450-mV respectively.

As the first stage of the proposed PD and the proposed DEMUX is the same, both the first stage circuits were merged together in the CDR design. Besides having the advantage of reduced power consumption, the merging of the circuits also eliminates the systematic phase offset caused by the retimed data.

An unbalanced charge pump is implemented to compensate for the proposed PD. The unbalanced charge pump compensates for the difference in the UP and the DN pulse-widths and also the difference in the number of the UP and DN signals. The analysis and calculation of the unbalanced charge pump and charge pump current is also presented in this thesis.

Besides that, a hysteresis lock detector is also implemented to circumvent the issue of having only one required ppm (or frequency range). It has a smaller required ppm to switch from the frequency acquisition loop to the phase tracking loop (in-lock condition) and a larger required ppm to switch from the phase tracking loop to the frequency acquisition loop (out-of-lock condition).

Finally, all the proposed circuits were tested in a fully integrated quarter-rate CDR design. With the dual-loops CDR architecture, the CDR is able to achieve a wider tracking range. The CDR consumes 71.9-mW a supply of 1.8-V and its peak-to-peak clock jitter is 30.4-ps. The power efficiency of the CDR design is 14.38-mW/Gbps and it has the best performance among all the lower-rate linear CDRs with the same technology.

9.2 Recommendations

By designing the CDR circuit with a more advanced CMOS process such as 90-nm or 65-nm, the CDR will be able to reach a higher data rate [81, 114, 115]. This is because the speed of the CDR design is constraint by the speed of the device. Hence, with a more advanced CMOS process, the speed performance of the CDR can be improved. Besides that, a more advanced process will also bring along the possibility of scaling down the supply voltage. With a reduction in the supply voltage, the power consumption of the CDR circuit can be reduced. This will provide a higher power efficiency for the CDR circuit because the speed of the CDR is increased while the power consumption of the CDR is reduced.

As the CDR circuit has a dual-loops architecture, its frequency tracking ability is increased. With a higher frequency tracking range, the CDR design can be implemented for multi-standard application, i.e. serializer/deserializer (SERDES) structure. With the quarter-rate nature of the proposed CDR, the required VCO tuning range is reduced by four times. For example, if the change in the data rate is 4-Gb/s, the required tuning range

of the VCO is only 1-GHz. Hence, multi-standard application will benefit from the advantage of the quarter-rate CDR architecture.

Another possible future research direction is to build a fully integrated CDR circuit. The current CDR design needed an external reference signal for the frequency acquisition loop. This reference signal can be supplied with a CMOS crystal oscillator. However, research on the frequency accuracy of the crystal oscillator with respect to temperature and supply voltage variation is critical.

Besides that, the integration of the CDR design in a free space optical receiver is also another possible research area. As the receiver is a portable device, the power consumption will be an important aspect to consider. Control circuit can be implemented to fully or partially switch-off the CDR design when no data is being received.

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