Gate-all-around nanowire FET sensors with ultrahigh sensitivity and low noise

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Gate-All-Around Nanowire FET Sensors with Ultrahigh Sensitivity and Low Noise

A Thesis submitted to Nanyang Technological University in
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By

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Abstract

In this thesis, new kinds of field-effect transistor (FET)-based sensing elements were developed to maximize the detection limits of conventional piezoresistors. These sensing elements were able to enhance the piezoresistive sensitivity and to reduce the intrinsic noise, which significantly improved the detection limits and make them adaptable for lower strain detection applications. The FET-based sensing elements were integrated into the cantilever or diaphragm to improve minimum detection limits in force or pressure measurements. After the sensor designs were confirmed by the theoretical analysis, six different kinds of piezoresistive n-type metal-oxide-semiconductor field-effect transistor (MOSFET)-embedded microcantilevers were designed and characterized to systematically study the impacts of different cantilever and transistor channel geometries on the force sensitivity. For point-loading or force sensing applications, FETs with lower channel width were found to be optimal for relative drain current change even though their absolute current output was less. In particular, the embedded nMOSFET exhibited 63.6% higher sensitivity by decreasing the transistor channel width from 300 to 60 μm . The low-frequency noise (LFN) characteristics of the devices showed better resolution for higher aspect-ratio FETs, and the measured drain current noise was in the nanoampere range. Effects of the gate bias on the drain current change and device sensitivities were investigated. Specifically, a wide piezoresistance tuning range above 200% was demonstrated for the pMOSFET with the width/length ratio of 5 within a gate bias span of 6 V. The preliminary results indicated that the MOSFET-embedded microcantilever sensors comprise compact size, moderate sensitivity, lower noise, rapid response and have a potential application as a strain sensor.

To further improve the piezoresistive sensitivity of the planar FET-based sensing element, the gate-all-around (GAA) nanowire field-effect transistor (NWFET) was presented as a novel, miniaturized and lower voltage driven piezoresistive sensing element. With a narrow gate bias span of 0.8 V near the threshold region, the piezoresistive coefficient of the NWFET enhanced up to seven times under both compressive and tensile strain conditions. Results revealed the reduction of the LFN of the NWFET when biased in the subthreshold region, which improved the sensor resolution (minimum detectable strain $\sim 1.5 \times 10^{-7}$) by sixteen times compared to the planar FET-based sensing element. To use the higher piezoresistance and lower intrinsic noise, the nanoelectromechanical pressure sensor based on the GAA NWFET sensing element was demonstrated to enhance the pressure sensitivity and signal-to-noise ratio (SNR). It was observed that the pressure sensitivity enhances from 0.019 to 0.079 (mA/A)/mmHg by changing the NWFET gate bias from 0.2 V (inversion region) to -0.2 V (subthreshold region). The LFN characteristics showed the significant reduction in the drain current noise for the NWFET when biased in the subthreshold region, enhancing the SNR from 2×10^6 (inversion region) to 2.4×10^9 (subthreshold region). Results showed that NWFET-based sensing elements operated at low bias with higher piezoresistance and can be used to measure lower strain values with high SNR.

The development of the GAA channel structure was further implemented to design and fabricate a novel junctionless nanowire field-effect transistor (JL-NWFET). The JL-NWFET exhibited excellent electrostatic control with high ON/OFF current ratio ($>10^7$), low subthreshold slope ($SS < 70$ mV/dec) and ultra-small drain-induced barrier lowering. Higher piezoresistance was obtained for the lower channel doping devices, i.e. a piezoresistance increment of 91% was observed for a JL-NWFET device with a channel doping level of $6.7 \times 10^{18} \text{ cm}^{-3}$, compared to one with a doping level of $6.7 \times 10^{19} \text{ cm}^{-3}$. The JL-NWFET operated by bulk conduction in the on-

state compared to surface conduction in the inversion mode NWFET, and showed significantly lower drain current noise than the NWFET counterpart. In the JL-NWFET, the LFN was found to be nearly insensitive to the gate bias voltage (full depletion to no depletion), doping levels, and operating frequency. The picoampere drain current noise helped to achieve a superior resolution, i.e. the minimum detectable strain of $\sim 3.8 \times 10^{-8}$ achieved for the JL-NWFET, was four times smaller than that of the inversion mode NWFET. The preliminary results achieved in this project indicate that the GAA JL-NWFET-based sensing element has miniaturized size, higher piezoresistive sensitivity and lower intrinsic noise and can be potentially used in ultrasensitive strain sensors.

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List of Abbreviations

ASIC	Application-specific Integrated Circuit
BOX	Buried-oxide
CMOS	Complementary metal–oxide–semiconductor
CNFET	Carbon Nanotube Field-effect Transistor
CVD	Chemical Vapor Deposition
DC	Direct Current
DG	Double Gate
DRIE	Deep Reactive Ion Etching
DUV	Deep Ultraviolet
FET	Field-effect Transistor
GAA	Gate-all-around
GF	Gauge Factor
IM	Inversion Mode
JL	Junctionless
LFN	Low-frequency Noise
LPCVD	Low-pressure Chemical Vapor Deposition
MDF	Minimum Detectable Force
MDS	Minimum Detectable Strain
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal-oxide-semiconductor
MOSFET	Metal–oxide–semiconductor Field-effect Transistor
NW	Nanowire
NWFET	Nanowire Field-effect Transistor
PZT	Lead Zirconate Titanate
RIE	Reactive Ion Etching

SEM	Scanning Electron Microscope
SNR	Signal-to-noise Ratio
SOI	Silicon-on-insulator
TEM	Transmission Electron Microscopy
PZR	Piezoresistance
ZTC	Zero Temperature Coefficient

Chapter 1

Introduction

I began work at NTU for Dr. Miao Jianmin at the beginning of 2008 to learn thoroughly about microelectromechanical systems (MEMS), with an initial topic to enhance the sensitivity of piezoresistive sensors. As a start to the project, I came up with the thought to develop a transistor-based piezoresistive sensing element that could improve the detection limits of conventional piezoresistors. I began my work in designing and fabricating transistors, and integrating them into cantilever and diaphragm structures for actual sensing applications, i.e. force and pressure sensing. After a couple of semesters, I successfully fabricated the planar transistor-integrated sensor devices but the measured piezoresistive sensitivity was found comparable to conventional piezoresistors. The planar transistor characterization was not proficient to obtain higher piezoresistivity, but the dedication for improved piezoresistance was unrelieved. After that, I devoted my time to understand the fundamental issues and improve the transistor designs by reducing the channel dimensions from micro to nano scale to enhance the piezoresistance and reduce the intrinsic noise. The idea to use nanowire as a transistor channel and the carrier confinement by the biasing effect had been successful, and nanowire channel transistor held promise as a higher sensitivity sensing element that could achieve the better resolution we were looking for. The large scale fabrication and convenience of higher piezoresistance also made nanowire transistors as an attractive sensing element for a variety of sensing applications. As a result, the rest of my efforts were focused onto fundamental understanding and improving transistor-based sensing elements. Following sections briefly

present the scientific background and motivations of this work. The background of conventional piezoresistive sensing elements, including configuration, limitations and research trend, is briefly introduced. Extraordinary properties of nano scale nanowires that can be used to enhance the resolution of the piezoresistors are also discussed. At the end of the chapter, the organization of this thesis is presented.

1.1 Background

MEMS are “systems made of very small components”, which are useful in various sensing applications. Micro begins a dimensional scale, electro suggests either electronics or electricity and mechanical implies moving parts of some kind. The advancement of the IC technology with specialized techniques called “micromachining” allows the fabrication of these miniature systems. Most MEMS devices involve some form of lithography-based microfabrication, borrowed from microelectronics industry and the high-volume batch fabrication offers the potential for great cost reduction. MEMS devices are widely used for various sensing applications, such as automobiles, process control and a number of biomedical measurements [1-3]. Biomedical applications, requiring precise measurement of mechanical quantities, such as force, pressure, stress and strain, have a vast domain. With this regard, MEMS sensors with superior resolution, compact size, reduced cost, rapid response, and easy operation are main prerequisites.

MEMS sensors include the sensing element on the micrometer or nanometer scale and it is integrated with the mechanical component such as a cantilever or diaphragm. The mechanical component deforms due to input interactions on the MEMS sensor and the embedded sensing

element converts the measurand of interest into an interpretable output signal, i.e. current, voltage, resistance and optical image. Based on the working principles of the sensing elements, sensors can be categorized into capacitive, optical, piezoelectric and thermal types [4-7]. Nevertheless, the drawbacks of these detection methods lie in the complexity of the testing, lower sensitivity, bulky size of equipment and difficult packaging procedures [8-11]. As an alternative, the piezoresistive sensing element has become the main preference for MEMS designers, mainly because of easier integration with application-specific integrated circuits (ASICs) [12]. However, conventional piezoresistive sensors acquire lower sensitivity and suffer from thermal drift, which limits them to attain superior resolution (minimum detectable signal) [13]. Hence, by optimizing the doping, design and operating conditions, piezoresistive sensing elements need further improvement to fulfill the demands of higher piezoresistance and lower intrinsic noise, especially in the lower strain measurements.

The piezoresistive effect in silicon represents a change in resistance with applied stress and its piezoresistive coefficient is a function of crystal orientation, dopant type and doping concentration [14]. Numerous alternative piezoresistive materials, such as carbon nanotube, metal hybrid structures and polycrystalline silicon, were also investigated in the exploration of higher piezoresistive sensitivity [15-16]. The higher piezoresistive coefficient was obtained, but the non-linear response, higher intrinsic noise and non-compatibility with CMOS-MEMS fabrication techniques have made these sensing elements unrealistic for actual sensing applications. Recently, to enhance the sensitivity of piezoresistive sensors, one-dimensional nanowire-based sensing elements were introduced and showed improved performance in terms of higher piezoresistance [17]. The higher piezoresistive sensitivity of nanowires was reported due to the reduced dimensionality, larger surface/volume ratio and the quantum confinement

effects [18-19]. In addition, higher piezoresistance was also reported for depleted nanowires, which was achieved by using a high substrate bias voltage [20]. The anomalous piezoresistive effect has been interpreted as a combined effect of electric field and mechanical stress on the constricted current channel. Though higher sensitivity was reported, there have been large differences in piezoresistive coefficients obtained by different researchers and giant piezoresistance in nanowires was not successfully reproduced. Milne et. al [21] accounted that the apparent giant piezoresistance [18, 20] was not because of applied stress but due to the charge trapping and subsequent relaxation at the exposed SiO₂ layers on the wire surfaces. It was confirmed with experimental consequences that the true piezoresistance of the nanowire sensing element was comparable to the bulk silicon and giant piezoresistance claims were fictitious [21]. Thus, unfortunately, it is still uncertain whether the reported piezoresistive enhancement is intrinsic, caused by size reduction, or simply due to oxidation. The combined effect of lower dimension and biasing voltage on the nanowire piezoresistance and intrinsic noise is an unknown physical phenomenon, motivating a comprehensive investigation before claiming nanowires as better sensing element. Therefore, in this project, the possibility of utilizing nanoscale silicon piezoresistors as improved strain sensing element will be investigated.

Among many factors that limit the sensing performance, the intrinsic noise is extremely critical since it determines the minimum signal that can be detected by any MEMS sensor. Reducing noise while maintaining or improving device sensitivity will provide enhanced signal-to-noise ratio (SNR) and superior resolution (minimum detectable signal). However, to determine whether the sensor noise is at its theoretical minimum or a better design can achieve lower noise, fundamental noise mechanisms need to be apprehended to improve the sensor performance. By knowing the most dominant noise source in sensors, the sensing element designs and parameters

can be optimized to realize a low-noise sensing element. Noise in MEMS sensors has been studied by many researchers who have focused on specific noise sources, which are believed to limit the device performance. Harley and Kenny [22] showed methods used for fabricating high-sensitivity piezoresistive cantilevers to improve their sensitivity, bandwidth, and noise. It was also suggested that piezoresistive devices have to be biased according to their tolerance on power dissipation to prevent either their destruction or the decrease of their performance. In this work, the prospect of utilizing nanowire transistor-based sensing element with much lower intrinsic noise will be investigated.

Thus, the need to enhance the piezoresistance and reduce the intrinsic noise was the main concern in the development of MEMS sensors, which are required for lower strain detection. As compared to conventional piezoresistors, the field-effect transistor (FET) devices were reported with higher piezoresistance but lower intrinsic noise [23-24]. The increment of the piezoresistive coefficient was due to the electron quantum confinement in the inversion channel region [25]. The FET-based sensing element consists of a silicon channel connected between two terminals (source and drain), and the current flow between these terminals is controlled by a third terminal called gate. Recently, Vandamme and Hooze [26] reviewed the theoretical models in relation to various drain current fluctuation sources, which are accountable for the intrinsic noise in FETs. The intrinsic noise reduction could be achieved by utilizing optimized FET designs and operating conditions.

The undoped silicon nanowire can be used as a channel material to increase the piezoresistance of FET-based sensing elements. With the use of the improved gate structure, the nanowire channel current can be controlled by lower gate bias and piezoresistance might be further

enhanced. Furthermore, lower noise in the FET-based sensing element could offer a superior resolution along with higher SNR. By using CMOS-MEMS technology, planar FET-based sensing elements will be fabricated in the first stage of this project. Furthermore, with nanowire channel, junction-based and junctionless (with no doping gradient) FETs will be demonstrated to further enhance the strain resolution at the end of this project.

1.2 Motivations

Most of MEMS sensors utilize piezoresistive-based detection techniques because of easier fabrication, direct CMOS compatibility and good linearity. The resistance of piezoresistors changes under the stress and therefore gives the information about the applied input (i.e. force, pressure or strain). However, lower sensitivity and higher intrinsic noise limit the usage of piezoresistors for lower strain measurements, especially in biomedical applications. The lower strain detection could be achieved by using an alternating sensing element with higher piezoresistance, but lower intrinsic noise is also required to acquire better resolution. To enhance the sensitivity of piezoresistive sensors, silicon nanowire-based sensing elements were introduced and they showed improved performance in terms of higher piezoresistance [17]. However, the high surface-to-volume ratio in piezoresistive nanowires, which increases sensitivity to any changes, makes them prone to noise and leads to reduced SNR.

Compared to piezoresistors, the FET-based sensing element was reported with higher piezoresistance and lower intrinsic noise. A comprehensive study, considering the impact of the channel material, channel design and gate bias on piezoresistivity and intrinsic noise, has not

been reported for the FET-based sensing element. As the title of this thesis suggests, this research focuses on the development of various kinds of FET-based piezoresistive sensing elements to improve the strain detection limits, i.e. to enhance the performance of piezoresistive FETs in force and pressure sensing. In this work, a gate-all-around (GAA) nanowire FET-embedded sensor is proposed in order to get enhanced piezoresistive sensitivity with higher SNR.

1.3 Objectives

The main objectives of this project can be summarized in the following points:

- Theoretically analyze the piezoresistive behavior of FET-based sensing elements and optimize the sensor design parameters from governing equations to enhance the strain sensitivity in a static mode of stress loading operations.
- Investigation of the drain current noise in FET-based strain sensors. To explore the relationship between the sensor resolution, piezoresistive coefficient and intrinsic noise in FET-based sensing elements. FET sensors will be integrated into cantilevers and diaphragms to carry out force and pressure measurements.
- To develop a novel nanowire FET-based sensing element by using CMOS-MEMS technology. The GAA nanowire FET needs to be fabricated and characterized to confirm the possibility of applying these sensing elements for better force and pressure sensing applications.
- To distinguish the effects of low-dimension and biasing voltage on nanowire FET

piezoresistance and intrinsic noise. All parameters will be optimized through experiments to obtain superior resolution with high SNR.

- Based on optimized process parameters from the nanowire FET, a novel junctionless nanowire FET sensing element will be developed to further enhance the performance, such as sensitivity, limit of detection and the sensor fabrication yield. The main aim is to fabricate miniaturized sensing element that can operate at lower voltages with the best reported strain resolution.

1.4 Organization of the report

This thesis is organized into six chapters and detailed as follows:

Chapter 1 is the preliminary chapter with a concise introduction of the research background and motivations of the project, followed by the objectives and the organization of the thesis.

Chapter 2 presents detailed literature review on the fundamental understanding of working principles and classifications of silicon piezoresistivity. As the focus of this research, reviews on piezoresistive sensing element-based sensors are emphasized. In this chapter, reviews on nanowire piezoresistive properties and noise measurement methods are also included. Furthermore, a theoretical background is presented for the transistor-embedded stress sensors. The importance of piezoresistance and low-frequency noise governing equations is recognized for the MEMS sensor working under the mechanical stress. The stress sensitivity and resolution of the sensor are also reviewed for a variety of piezoresistive sensors. The piezoresistive gauge factor and low-frequency noise are found to be the two dominant factors to affect the sensor resolution and their relationships are also established in this chapter. The novel sensor designs based on transistor-embedded force and strain sensors are proposed at the end of this chapter.

Chapter 3 describes the developments of planar transistor-based sensing elements. The detailed fabrication processes for nMOSFET and pMOSFET transistors are presented and their electromechanical behaviors are investigated by integrating these sensing elements into microcantilevers. Six different piezoresistive nMOSFET-embedded microcantilevers were designed and characterized under strain to systematically study the impacts of different cantilever and nMOSFET channel geometries on the strain sensitivity. In the second part, three different pMOSFET-embedded microcantilevers are presented and their responses to physical displacements are evaluated. The effect of the gate bias on the piezoresistive output is presented. Characterization results demonstrate that MOSFETs comprise lower noise compared to conventional piezoresistors, and can be applied as improved and potential sensing elements in strain sensing applications.

In Chapter 4, the GAA nanowire FET is introduced as the piezoresistive sensing element and its electromechanical properties are characterized. The gate surrounds the nanowire channel in the GAA structure, which provides easier carrier creation/depletion in the nanowire channel with the use of low gate bias. The strain-induced change in the drain current is experimentally verified, and the gate bias effects on piezoresistance and drain current noise are analyzed. The higher gauge factor and lower noise are reported to obtain higher piezoresistance and SNR. Results reveal that the GAA NWFET can be used as a miniaturized, low bias controlled and ultrasensitive sensing element for nanoelectromechanical sensors.

Chapter 5 presents a novel piezoresistive sensing element based on the junctionless nanowire field-effect transistor (JL-NWFET). Effects of various channel doping are presented on the piezoresistance, threshold voltage and low-frequency noise (LFN). The JL-NWFET operates by bulk conduction in the on-state compared to surface conduction in the inversion-mode

NWFET, and shows significantly lower spectral noise than the NWFET counterpart. The channel doping offers wide tunability of the threshold voltage without any influence on the LFN. The superior LFN behavior helps to achieve a superior resolution (minimum detectable strain) and propose the JL-NWFET as an ultrasensitive sensing element for the nanoelectromechanical sensors.

Chapter 6 concludes the thesis with a summary of the research work and achievements that have been accomplished. Recommendations for future research in this project are also included.

Chapter 2

Literature review

A detailed review of piezoresistive sensing elements and strain sensors is presented in this chapter. The working principle of silicon piezoresistors, its physics and related fabrication techniques are introduced. I also summarize the effects of intrinsic noise, design considerations and alternative material choice to enhance the sensitivity of piezoresistive sensors. Since transistor-based sensing elements are the research focus of this project, the piezoresistive response and intrinsic noise results have been summarized to review previous developments in this topic. As smaller dimension nanowires will be incorporated as the channel material to enhance the piezoresistive sensitivity and detection limits, the electromechanical properties of nanowires are also summarized. In the last section of this chapter, the design of a transistor-integrated strain sensor is proposed.

2.1 Piezoresistivity

The piezoresistive effect describes the change in the resistivity of a material due to an applied mechanical strain. In 1856, Sir Thomson reported on the resistance change in strained iron and copper wires, and thereby discovered the first strain gauge sensor [27]. The change in the resistance due to the applied load was much lower for iron and copper wires and many efforts have been carried out on different metals to enhance the strain sensitivity [28]. Cookson introduced the name piezoresistance to the change in the conductivity with strain, as different from the total fractional change of resistance [29]. In 1950, Bardeen and Shockley introduced

larger conductivity change with strain in single-crystal silicon and C. S. Smith confirmed with exceptionally larger piezoresistance in silicon and germanium [30, 31]. The resistance of the homogeneous material is defined as a function of resistivity (ρ)

$$R = \rho \frac{l}{A} \quad (2.1)$$

where l is the length and A is the cross-sectional area. As the material is compressed or stretched in one particular direction, the cross-sectional area expands or contracts in the other two directions perpendicular to the direction of stress, respectively. This phenomenon is called the Poisson effect and the Poisson's ratio (ν) is defined as the fraction of expansion divided by the fraction of compression [32]. The piezoresistive property of a material is usually defined by the gauge factor (GF), which is the ratio of the normalized change of the resistance to the applied strain (ε) [33]

$$GF = \frac{\Delta R / R}{\varepsilon} \quad (2.2)$$

The resistance change in the material is originated mainly due to two reasons: (1) dimensional changes and (2) fractional changes in conductivity. For semiconductors, the change in the conductivity is dominant, while the change in dimensions only has a minor influence [34]. The change in the resistance of the material with strain is given as [35]

$$\frac{\Delta R}{R} = (1 + 2\nu)\varepsilon + \frac{\Delta\rho}{\rho} \quad (2.3)$$

2.1.1 Piezoresistive effect of silicon

Although the piezoresistive behavior has been investigated in many metals and materials, silicon attracted the main focus due to its direct compatibility in CMOS and MEMS-based fabrication

processes. Few aspects of silicon crystal physics, such as atomic and crystalline structure, energy band hypothesis, carrier transport, and carrier trapping at grain boundaries, were key functions in determining the piezoresistive effect in silicon. Photolithography and etching techniques were used to create devices in various crystal directions to access desirable material properties.

As shown in Figure 2.1a, undoped silicon has four valence electrons and it forms a covalently bonded diamond cubic structure. When impurity atoms (n-type or p-type) are doped in the silicon material, free electrons or holes are added to the crystalline silicon lattice. The silicon crystal lattice results from external doping have an important effect on the material's piezoresistive behavior.

Figure 2.1. (a) Covalently bonded diamond cubic structure of silicon. (b) Nine components, σ_{ij} , of stress on an infinitesimal unit element.

To define the state of stress for a unit element, as shown in Figure 2.1b, nine stress components, σ_{ij} , are specified as

$$\sigma = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix} \quad (2.4)$$

The first index i denotes the direction of the applied stress, while the second index j indicates the direction of the force or stress. The stress is normal to the surface, if $i = j$, but indicate a shear stress on face i when $i \neq j$. As static equilibrium requires forces and moments sum to zero, stress tensor is always symmetric ($\sigma_{ij} = \sigma_{ji}$) and thus the stress tensor contains only six independent components. For an isotropic and homogeneous material, the strain (ε_{ij}) is directional and related to the stress by Hooke's law [36],

$$\sigma_{ij} = \varepsilon E \quad (2.5)$$

In the conduction theory of electric charges, the Cartesian current density vector components J_1 , J_2 and J_3 are functions of the Cartesian electric field vector components E_1 , E_2 and E_3 i.e. $J_i = J_i(E_1, E_2, E_3)$, where $i = 1, 2, 3$. For ohmic materials, there is proportionality constant for this linear relation, which is the electrical resistivity. Applying the summation implied in the repeated indices with $r_{ij} = r_{ji}$ yields [37]

$$E_i = \rho_{ij} J_j \quad (2.6)$$

In the case of anisotropic semiconductor materials, the piezoresistive effect is dominated by the geometrical change of the strained filament. Bridgman [38, 39] was the first to experimentally observe this effect in metals under tension and hydrostatic pressure. Experimental observations in semiconductors have followed his work [40, 41] and the piezoresistive effect in semiconductors can be described mathematically using the series expansion

$$\rho_{ij} = \rho^0_{ij} + \pi_{ijkl} \sigma_{kl} + \lambda_{ijklmn} \sigma_{kl} \sigma_{mn} + \dots \quad (2.7)$$

where ρ^0_{ij} are the electrical resistivity components for the unstressed conductor and π_{ijkl} , $\lambda_{ijklmn} \dots$ etc are the components of fourth, sixth and higher order tensors, which characterize the

stress induced resistivity change. For stressed semiconductors, the resistivity components are linearly related to the stress components as

$$\rho_{ij} = \rho_{ij}^0 + \pi_{ijkl} \sigma_{kl} \quad (2.8)$$

To define the piezoresistive coefficient, four subscripts are required because of two second-rank tensors of stress and resistivity. The first subscript refers to the electric field component (measured potential), the second to the current density (current), and the third and fourth to the stress (stress has two directional components). For conciseness, the subscripts of each tensor are also collapsed [42], e.g., $\pi_{1111} = \pi_{11}, \pi_{1122} = \pi_{12}, \pi_{2323} = \pi_{44}$. Kanda later generalized these relations for a fixed voltage and current orientation (ω) as a function of stress (λ) [43]:

$$\frac{\Delta \rho_{\omega}}{\rho} = \sum_{\lambda=1}^6 \pi_{\omega\lambda} \sigma_{\lambda} \quad (2.9)$$

$$\sigma = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{12} & 0 & 0 & 0 \\ \sigma_{12} & \sigma_{11} & \sigma_{12} & 0 & 0 & 0 \\ \sigma_{12} & \sigma_{12} & \sigma_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \sigma_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \sigma_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \sigma_{44} \end{bmatrix} \quad (2.10)$$

Combining the above equations, considering the crystal symmetry in silicon and employing the reduced index notation, the electrical resistivity can be described as

$$\begin{pmatrix} \Delta \rho_1 / \rho_0 \\ \Delta \rho_2 / \rho_0 \\ \Delta \rho_3 / \rho_0 \\ \Delta \rho_4 / \rho_0 \\ \Delta \rho_5 / \rho_0 \\ \Delta \rho_6 / \rho_0 \end{pmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \begin{pmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{pmatrix} \quad (2.11)$$

where ρ_0 and π_{ij} are the isotropic resistivity of the unstressed silicon crystal and component of the piezoresistance tensor, respectively. There were three independent piezoresistive coefficients named as π_{11} , π_{12} and π_{44} . The values of π_{11} , π_{12} and π_{44} for single-crystal silicon under certain doping concentration and dopant types have been experimentally characterized. It was reported that the piezoresistive coefficient of single-crystal silicon was not constant but influenced by the doping concentration [44], type of dopants [45], and temperature of the substrate [46]. Table 2.1 shows the values of piezoresistive coefficients based on the lightly doped silicon (resistivity= 11.7 Ωm).

Table 2.1: Piezoresistivity components for silicon under certain doping values [47, 48].

Piezoresistance Coefficients	n-type Si ($\times 10^{-12} \text{Pa}^{-1}$)	p-type Si ($\times 10^{-12} \text{Pa}^{-1}$)
π_{11}	1020	-66
π_{12}	-534	11
π_{44}	136	-1380
$\pi_s = \pi_{11} + \pi_{12}$	486	-55

Furthermore, Table 2.2 summarizes the effective longitudinal and transverse piezoresistive coefficients for most commonly occurring cases, when the piezoresistor current flows in $\langle 100 \rangle$, $\langle 110 \rangle$ or $\langle 111 \rangle$ directions [49]. The effective piezoresistive gauge factors attributed to each case can be calculated by multiplying the piezoresistive coefficient with Young's modulus in the direction of the applied strain. The resistance (R) change can be calculated in the piezoresistive sensing element-based sensors as a function of applied stress and given as [50]

$$\frac{\Delta R}{R} = \pi_l \cdot \sigma_l + \pi_t \cdot \sigma_t \quad (2.12)$$

where σ_l and σ_t are longitudinal (the stress component is parallel to the direction of the current) and transverse (the stress component is perpendicular to the direction of the current) stress components, respectively. Also π_l and π_t are longitudinal and transverse piezoresistive coefficient, respectively.

Table 2.2: Formula for transverse and longitudinal gauge factors for various commonly encountered resistor configurations.

Direction of strain	Direction of current	Configuration	Piezoresistive coefficient
$\langle 100 \rangle$	$\langle 100 \rangle$	Longitudinal	π_{11}
$\langle 100 \rangle$	$\langle 010 \rangle$	Transverse	π_{12}
$\langle 110 \rangle$	$\langle 110 \rangle$	Longitudinal	$(\pi_{11} + \pi_{12} + \pi_{44})/2$
$\langle 110 \rangle$	$\langle \bar{1}\bar{1}1 \rangle$	Transverse	$(\pi_{11} + \pi_{12} - \pi_{44})/2$
$\langle 111 \rangle$	$\langle 111 \rangle$	Longitudinal	$(\pi_{11} + 2\pi_{12} + 2\pi_{44})/2$

Piezoresistive materials were used to develop piezoresistors and their application was mainly focused to determine the mechanical strain. One of the simplest forms of the piezoresistive silicon sensor was the diffused resistor. It consists of a simply diffused n-well or p-well contact within a p-type or n-type silicon substrate, respectively. The resistance is determined by the diffused area and its value ranges of several hundred ohms. Additional p+ or n+ diffusion was also carried out to provide the ohmic contact to the device. The schematic cross-section of an n-well piezoresistor is shown in Figure 2.2. There is a diode between the p-region and the n-region, but the n-region itself functions as a resistor.

Figure 2.2. Silicon n-well piezoresistor [50].

It can be considered that the diffused resistor is junction-isolated from the substrate. These piezoresistors were embedded in the cantilever or membrane structure and resistivity measurements were performed with the help of the Wheatstone bridge [51]. In order to measure the resistance change, silicon cantilevers should be in a DC-biased Wheatstone bridge as shown in Figure 2.3.

Figure 2.3. Piezoresistive read-out and the Wheatstone bridge configuration [52].

The relation between the applied stress and resistance change clearly suggests that the resistance increases with the applied stress. Under the applied force F , the fractional resistance change of the piezoresistive cantilever is [53]

$$\frac{\Delta R}{R} = \pi_l \sigma_{\max} = \beta \frac{6L_c \pi_l}{W_c t^2} F = \beta \frac{3Et \pi_l}{2L_c^2} \delta \quad (2.13)$$

where δ is the deflection at the free end of cantilever. $\sigma_{\max}$ and π_l are the maximum stress and longitudinal coefficient of silicon, respectively. L_c and W_c are the length and width of the cantilever, respectively. β is the correction coefficient (between 0 and 1). To have the maximum sensitivity, the β value has to be the highest. It has the maximum value when doped resistors are very shallow and the current is flowing close to the surface. Although piezoresistive measurements have been used for many applications, however, the main disadvantages of the piezoresistor were its sensitivity and resolution dependence on the noise level.

2.1.2 Noise in piezoresistors

Noise can be defined as unwanted signals that degrade the desired signal. In the electrical domain, these unwanted signals can originate from the environment or from the electronic device itself via current or voltage fluctuations. The noise signals can be large enough to manipulate the desired signal and thus limits the detection capabilities of the MEMS sensors. Since noise is a random process, analyzing it in the time domain does not give useful information regarding its average magnitude. Therefore, the power spectral density (PSD) function was employed, which presents the noise power (squared magnitude of the random signal) over a range of frequencies for noise measurements [54].

The intrinsic noise inside piezoresistors originates from different sources. It is important to understand the originating sources of the intrinsic noise in piezoresistors to improve the sensing element design parameters and to achieve better resolution. Noise in semiconductors is originated and affected by various parameters such as defect density, conductivity, doping concentration, temperature and biasing voltage. With zero applied bias voltage and no external stimuli (light and thermal gradient), the semiconductor is in equilibrium and its properties remain constant (independent of time). However, when bias or stimuli are applied, the semiconductor properties are no longer constant, and the system is said to be in non-equilibrium. Noise in MEMS sensors can be also classified as equilibrium and non-equilibrium noise. There are some basic parameters that can generate the random variation in the current or voltage in a conductor. The average current in a conductor of length L can be written as

$$I = qNv_d / L \quad (2.14)$$

where q is the electron charge, N is the number of free electrons and v_d is the drift velocity of the carriers. Any change in the number of carriers (ΔN) and carrier velocity (Δv_d) fluctuates the

average current in the conductor. These are two sources of current fluctuations originated from physical processes inside a material. The current fluctuation can be defined as [55]

$$\Delta I(t) = \frac{q}{L} \overline{v_d} \Delta N(t) + \frac{q}{L} \sum_{i=1}^{\bar{N}} \Delta v_i(t) \quad (2.15)$$

where v_i is the drift velocity for an individual carrier. The first term of Equation (2.15) is due to the carrier fluctuation and the second term is due to the fluctuating carrier velocity.

The intrinsic noise in piezoresistors can be classified into four main types that are Johnson noise, shot noise, generation-recombination noise and Hooge noise. The dominant noise types that limit the resolution of piezoresistors are thermal and flicker (1/f) noise. The thermal noise arises from the random thermal motion of electrons in the resistive material. This noise was first discovered by J. B. Johnson and theoretically explained by H. Nyquist in 1928 [56]. For this reason, it is named as Johnson noise and the Johnson noise PSD for a resistance R at a finite temperature T (K) is defined as

$$S_I = 4k_B T R \quad (2.16)$$

where k_B is the Boltzmann constant (1.38×10^{-23} J/K). Because this spectral density function is constant over all frequencies, it is also called white noise. The equation can be rewritten by replacing $k_B T$ with the frequency dependent quantum correction factor [57]

$$S_I = 4 \frac{hf}{e^{hf/k_B T} - 1} \frac{1}{R} \quad (2.17)$$

where h is the Planck's constant (6.63×10^{-34} J.s). The electrical thermal noise was found to be independent of the bias voltage since the agitation of the charge carriers by thermal lattice vibrations presented regardless of the bias voltage. However, an increase in the temperature

induces more agitation of the carriers, hence making the Johnson noise temperature dependent. Furthermore, the Johnson noise was found to be frequency independent because lattice vibrations are random, thus not related to any single time constants.

Secondly, the interface states at the interface between oxide and silicon can trap or emit electrons and holes similar to impurities in silicon. They can exchange charge carriers with the substrate via the tunneling mechanism and, therefore, contribute to stochastic fluctuations of the carrier density in the piezoresistor. It was also called generation-recombination (g-r) noise which is caused due to fluctuation in the number of carriers available for current transport [58]. The PSD of current fluctuation can be calculated by the following expression

$$S_I = I^2 \frac{N_T}{N^2} \frac{\tau}{1 + (2\pi f)^2 \tau^2} \quad (2.18)$$

where τ is the time constant of the transitions, N_T is the total number of traps, N is the total number of carriers and I is the DC current through the resistor. As given in Equation (2.18), the PSD was proportional to the number of traps and inversely proportional to the number of carriers squared. In general, the time constant and relative strength of the traps depend on the trap energy level and spatial position. For certain distribution of time constants, it was found experimentally that the noise currents in piezoresistors have an additional low-frequency component that varies with the magnitude of the DC current and the PSD becomes proportional to $1/f$. It is called flicker noise or $1/f$ noise. Flicker noise arises from the capture and release of charge carriers in the localized trap states in semiconductors. Due to the distribution of the binding energies of such traps, there is a corresponding distribution of capture and release times τ_i . As these times depend on the binding energy, the quantity $\log \tau_i$ is distributed similar to the binding energies

and results in a spectral density fuction. Low-frequency or $1/f$ noise is a frequency dependent non-equilibrium noise, which has higher magnitude at lower frequencies. The mechanism that generates $1/f$ noise in piezoresistors is still an active area of research. The PSD for $1/f$ noise takes the general form

$$S_I = K \frac{I^\beta}{f^\gamma} \quad (2.19)$$

where K is a constant, and β and γ are the current exponent and material dependent function, respectively. This kind of behavior has been observed in the low-frequency part of the spectrum in most conductors and semiconductors. Two main theories that have been proposed to define this behavior are based on number fluctuation and mobility fluctuation. G-r noise from a large number of traps (number fluctuation) is described as [59]

$$S_{tot} \approx \frac{B}{4\ln(\tau_2/\tau_1)f} \quad \text{for } 1/2\pi\tau_2 \ll f \ll 1/2\pi\tau_1 \quad (2.20)$$

here $(\tau_2 < \tau < \tau_1)$, and the factor $1/\ln(\tau_2/\tau_1)$ is for normalization purpose. It was observed that different time constants add up to $1/f^\gamma$ spectrum with γ close to 1[60].

The second reported mechanism that can originate $1/f$ noise was mobility fluctuation. Hooge [61] originally conducted experiments on noise in homogeneous samples at low frequency, which showed inverse frequency dependence. It was proposed that $1/f$ noise at low frequency is a bulk phenomenon and occurs due to fluctuations in the mobility [62]. Hooge gave an empirical formula for the noise PSD of $1/f$ noise in his publications [63] as illustrated in

$$\frac{S_R}{R^2} = \frac{\alpha_H}{fN} \quad (2.21)$$

where S_R is the spectral power density of the resistance, R is the resistance of the sample, α_H is a dimensionless parameter referred as Hooge parameter, N is the number of carriers and f is the frequency. The noise PSD was inversely proportional to the number of carriers N . The PSD of the individual mobility fluctuation was described as [64]

$$\frac{S_\mu}{\mu^2} = \frac{\alpha_H}{f} \quad (2.22)$$

which means that α_H is proportional to the variance of the relative mobility fluctuation for each carrier, independent of the number of carriers. As the intrinsic noise presents in piezoresistive sensors, the output signal was configured with a ratio between desired and undesired signal called the signal-to-noise ratio (SNR).

The SNR was described as the ratio of the mean-square signal to the mean-square noise. If the signal waveform $v_s(t)$ is added to the random noise waveform $v_n(t)$, the SNR can be defined as

$$SNR = \frac{\overline{v_s^2}}{\overline{v_n^2}} \quad (2.23)$$

The ratio was also represented in decibels and can be further expressed in terms of the RMS value of each quantity

$$SNR = 20 \log \left(\frac{v_{s,rms}}{v_{n,rms}} \right) \text{ in dB} \quad (2.24)$$

The variation of the current with the doping concentration, length and thickness of the piezoresistor needs to be optimized to obtain better resolution and higher SNR for specific applications. The existing piezoresistive detection technology suffers from inevitable thermal and conductance fluctuation noise (usually called flicker or $1/f$ noise), nonlinearity in piezo-

response, and inadequate sensitivity to be used in very small strain measurements. Thus, there is a strong requirement to improve the piezoresistive sensitivity and reduce the intrinsic noise to measure lower strain values. As an alternative, piezoresistive sensors based on metal-oxide-semiconductor field-effect transistor (MOSFET) were introduced and it offered lower noise level, high sensitivity and easier integration with ASICs [65, 66]. These FET-based strain sensors were reported for MEMS sensors such as accelerometers, resonators, and parallel cantilevers for scanning probe microscopy, as well as for residual strain measurements.

2.2 MOSFET structure and operation

A basic FET operates as a conducting semiconductor channel with two ohmic contacts (source and drain). The number of charge carrier taking part in the current flowing in the channel is controlled by another terminal called gate. The source and drain regions are heavily doped and the doping is of opposite type to the substrate. For an n-channel MOSFET, source and drain are n^+ -doped when the substrate is p-type. The basic MOSFET structure is shown in Figure 2.4.

Figure 2.4. Schematic design of the standard n-MOSFET. The device can be viewed as a combination of two orthogonal two-terminal devices.

In the vertical direction, the gate-channel-substrate structure is called gate junction and regarded as an orthogonal two-terminal device, which is either a MOS structure or a reverse-biased rectifying device that controls the mobile charge in the channel by capacitive coupling (field-effect) [67]. In normal operation, the gate-channel impedance for all FET type devices has a large value. In the silicon MOSFET fabrication, the gate contact metal is separated from the channel by a high quality insulating silicon dioxide (SiO_2) layer. By applying a voltage to the gate electrode, the charge carriers of the conducting channel form an inversion charge, i.e., electrons in the case of a p-type substrate (n-channel device) or holes in the case of an n-type substrate (p-channel device) are induced in the semiconductor at the silicon-insulator interface. The current conduction is through an inversion layer at the silicon- silicon oxide interface. For instance, in n-channel MOSFET, the substrate is high resistivity p-type silicon (boron doped silicon) and the inversion charge consists of electrons to form the conducting channel between the n+ ohmic source and the drain contacts. Electrons enter and exit the channel at n+ source and drain contacts in the case of an n-channel MOSFET, and at p+ contacts in the case of a p-channel MOSFET. The concentration of inversion charges is controlled by applying the appropriate gate voltage. The threshold voltage (V_{TH}) is defined as the required gate voltage (V_{GS}) for the onset of strong inversion. The threshold voltage equation is given as [68]

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_B - V_{BS})}}{C_{ox}} \quad (2.25)$$

where ε_s is the permittivity of the semiconductor, N_A is the doping concentration of the substrate wafer, C_{ox} is the oxide capacitance per unit area, $2\phi_B$ is the potential drop in the semiconductor at the onset of strong inversion and V_{FB} is the gate voltage with respect to bulk required to

achieve the flat band condition. When a drain-source bias V_{DS} is applied to an n-channel MOSFET at above the threshold ($V_{GS} > V_{TH}$) conducting state, electrons flow inside the inversion layer from source to drain. The variation in the gate-source voltage alters the density of the electron sheet in the inversion layer (channel), changing the channel conductance and the drain current (I_{DS}). The magnitude of the drain current depends on the conductivity and transverse electric field (perpendicular to the direction of the current flow). For the linear region, the drain current is described as [68]

$$I_{DS} = \frac{W\mu_n C_{ox}}{L} \left((V_{GS} - V_{TH})V_{DS} - mV_{DS}^2 / 2 \right) \quad (2.26)$$

where W is the channel width, L is the channel length and μ_n is the electron mobility in the channel. A schematic view of the n-channel MOSFET is shown in Figure 2.5.

Figure 2.5. N-channel MOSFET with conducting channel and depletion region.

The factor m is called the body-effect coefficient (value between 1 and 1.4) and is defined as follows [69]

$$m = 1 + \frac{\sqrt{\epsilon_s q N_A / 4\phi_B}}{C_{ox}} \quad (2.27)$$

which correction for $V_{GS} > V_{TH}$ in an n-channel device. The application of a positive V_{DS} gives a steady voltage increase from source to drain along the channel that causes a reduction in the local gate-channel bias V_{GX} (here X represents a position within the channel). This reduction is the greatest near drain where V_{GX} equals the gate-drain bias V_{GD} . As an example, when $V_{GD} = V_{TH}$, the channel reaches the threshold at the drain and the density of the inversion charge vanishes at this point. This is called the pinch-off condition, which leads to a saturation of the drain current I_{DS} . Hence, the drain current in saturation remains approximately constant. The drain current in the saturation region can be described as [70]

$$I_{DS} = \frac{W\mu_n C_{ox}}{L} \frac{(V_{GS} - V_{Th})^2}{2m} \quad (2.28)$$

Typical current–voltage characteristics of a long-channel nMOSFET, where pinch-off is the predominant saturation mechanism, are shown in Figure 2.6.

Figure 2.6. Current–voltage characteristics of an n-channel MOSFET with current saturation caused by pinch-off (long-channel case). The intersections with the dotted line indicate the onset of saturation for each characteristics.

The drain current is not zero when the gate bias is below the threshold voltage ($V_{GS} < V_{TH}$), called the subthreshold region. The subthreshold current flow in the subthreshold region is defined as [68]

$$I_{DS} = \frac{W\mu_n C_{ox}}{L} (m-1) \left(\frac{kT}{q} \right) e^{q(V_{GS} - V_{TH})/mkT} \left(1 - e^{-qV_{DS}/kT} \right) \quad (2.29)$$

The ability to turn off a MOSFET is described by the subthreshold slope [68]

$$SS = \left(\frac{d(\log_{10} I_D)}{dV_{GS}} \right)^{-1} \approx 2.3 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad (2.30)$$

These parameters play an important role to determine various physical and electromechanical properties in transistors. The piezoresistive effect in the MOSFET inversion layer was investigated by many researchers and the piezoresistive coefficient was found to be different compared to the bulk silicon.

2.2.1 Piezoresistivity in MOSFETs: Quantization effect

The basic idea to use MOSFET as a piezoresistive sensing element came up to utilize the quantum effects in the piezoresistor with thickness below 50 nm. For the quantum mechanical point of view, this is a limit below the quantum confinement that begins to have additional influence on the electrical properties of the piezoresistor. The physical consequence of thin piezoresistor was the confinement of the charge carriers in the direction perpendicular to the piezoresistor surface. The physical phenomenon and modeling of the carrier mobility enhancement due to strain have been extensively studied for both (n and p-type) silicon inversion

layers. It has been shown that the deviation of the piezoresistive coefficient is due to the electron quantum confinement caused by the vertical electric field in the inversion channel region [71]. The quantization of the carrier motion was considered to be perpendicular to the surface in the inversion layer, which reduced the resistivity symmetry and the piezoresistive behavior in the MOSFET was not similar to the bulk material. It has been found that the piezoresistive coefficient in the MOSFET inversion layer depends not only on the surface orientation but also on the magnitude of the gate voltage.

2.2.2 Carrier repopulation and intervalley scattering

The piezoresistance effect in many-valley semiconductors has been interpreted in terms of strain-induced carrier repopulation and carrier scattering. According to the deformation potential theory [72], an applied strain causes the energy of the conduction-band minima to change, and hence, carriers are repopulated among the valleys. In the case of n-channel inversion layers of MOSFETs, because the quantization of surface energy levels has a large contribution on the piezoresistance, the piezoresistance gives us important information on two-dimensional electron states and electron transport properties. It was reported with experimental and theoretical results on the piezoresistance in the *n*-channel inversion layers, and the contributions of the carrier repopulation and the relaxation time anisotropy on the piezoresistance have been observed [73].

It is necessary to understand whether the mobility enhancement results from reduced conductivity effective mass or scattering. Since the valence band dispersion relationship for semiconductors depends on the nearest neighbor atomic spacing, certain stress (in particular shear stress) warps the valence bands (although less so for the conduction band but some warping for shear stress) [74]. The warping of the valence band provides dramatic changes to the

constant-energy surfaces in k space and can lead to the electron mobility enhancement via reduced conductivity mass in the channel direction. Thus, the important physical parameters, which play important roles to determine the piezoresistive behaviour in the MOSFET inversion layer, are strain-induced energy-level splitting, inversion-layer quantum confinement energy-level shifts, average mass change due to repopulation and band warping, two-dimensional (2-D) density of states, and interband scattering changes due to band splitting. Many qualitative models were presented to recognize the electron mobility in bulk-strained silicon by occupation and scattering in the $\Delta 2$ and $\Delta 4$ valleys and can be expressed as [75]

$$\mu_{eff} = q \frac{\left(\tau \Delta 2 \frac{n \Delta 2}{m_t^*} + \tau \Delta 4 \frac{n \Delta 4}{m_l^*} \right)}{(n \Delta 2 + n \Delta 4)} \quad (2.31)$$

where q , n , τ , and m are the electron charge, concentration, relaxation time, and conductivity mass in the MOSFET channel direction, respectively. The strain improves the mobility by increasing the electron concentration in the $\Delta 2$ valley. The repopulation improves the average in-plane conductivity mass (unstressed: $m_t = 0.19 m_0$ versus $m_l = 0.98 m_0$) and some further improvements are possible for stresses that warp the conduction valleys and lower m_t [76]. The carrier scattering also depends on the relative energetical position of valleys. Reduced intervalley scattering by the strain-induced splitting between $\Delta 2$ and $\Delta 4$ valleys plays some roles (enhances long channel mobility) when the splitting becomes comparable or larger than the optical phonon energy.

In addition to a low in-plane mass, a high out-of-plane mass for the $\Delta 2$ valley electron is equally important since the carrier motion perpendicular to the SiO_2 interface was quantized. This quantization in addition to the strain alters the position of the energy levels.

The quantization leads to bands becoming subbands since only discrete wave vectors k_z are allowed. Including quantization, the total inversion-layer electron energy is given by discrete values of energy (E_n) added to the electron energy in the x - and y -directions (in the plane of the MOSFET) [31]. Each step in the energy is called a subband with E_n the energy of the bottom of the subband. As an example, the self-consistent solution of Schrödinger and Poisson equation for 500 MPa of uniaxial tensile stress and an inversion-layer vertical field of 1 MV/cm gives the energy levels, as shown in Figure 2.7 [77].

Figure 2.7. Conduction valley energy-level splitting under 500 MPa of longitudinal uniaxial tensile stress: Bulk and MOSFET inversion layer (1 MV/cm). The energy-level splitting from the inversion-layer confinement is found to be larger than strained bulk silicon.

As the subband separation is greater than $k_B T$, practically all electrons in most cases occupy the bottom two subbands [ground state $n = 0$ typically called E_o (from $\Delta 2$) and E_o' (from $\Delta 4$)]. The ground state energy was significantly lower for the $\Delta 2$ valleys because of the higher quantization mass ($\Delta 2 : m_z = 0.98m_0$ versus $\Delta 4 : m_z = 0.19m_0$) which leads to increased splitting between the

bottom two subbands and confinement and strain splitting being additive (for the common biaxial and uniaxial tensile stress).

Together with higher piezoresistance, the lower $1/f$ noise is the fundamental requirement to introduce the transistor as the improved sensing element in strain sensors. Accurate transistor noise models were therefore necessary for semiconductor manufacturers and sensor designers to understand the factors that originate $1/f$ noise.

2.2.3 Low-frequency noise in MOSFETs

The origin of $1/f$ noise in transistors has been investigated and debated for nearly half a century. The two main theories that attracted the research focus are: (1) number fluctuation (ΔN) noise- $1/f$ noise is caused by electron transitions between the conduction band of the material and the oxide traps in the gate oxide and (2) mobility fluctuation ($\Delta\mu$) noise- $1/f$ noise is due to the mobility fluctuation of free carriers in the conduction channel. McWhorter conducted his experiments on germanium filaments and reported that $1/f$ noise is a surface effect [78]. At the semiconductor surfaces and interfaces, physical defects give rise to electronic traps that capture and emit charge. McWhorter postulated that $1/f$ noise is caused by fluctuations of the number of charge carriers, due to trapping and detrapping of charge carriers at these traps.

The physical mechanism behind the number fluctuation $1/f$ noise in MOSFETs is the interaction between traps in the gate oxide and carriers in the channel. The oxide traps dynamically exchange carriers with the channel causing a fluctuation in the surface potential, giving rise to fluctuations in the inversion layer density. These fluctuations translate to the drain current flowing between drain and source in the MOSFET and generate the drain current noise.

Secondly, since carriers are confined to a narrow region below the oxide/substrate interface and suffer from scattering at the surface, the carrier mobility in the inversion layer is lower than in the bulk. The effective mobility (μ_{eff}) in an inversion layer of a MOSFET can be computed using Matthiessen's rule from individual mobilities [79]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_c} \quad (2.32)$$

where μ_b is the bulk phonon mobility, μ_{ac} the mobility limited by the surface acoustic phonon scattering, μ_{sr} the mobility due to the surface roughness scattering and μ_c the mobility limited by Coulomb scattering mainly from ionized impurities and trapped charge in the gate oxide. Even though both ΔN and $\Delta\mu$ theories predict a low-frequency noise, the key difference between them is the bias dependence of the noise. While the ΔN theory gives a gate-referred noise spectral density that is independent of the gate voltage, the gate-referred noise from the $\Delta\mu$ theory increases in strong inversion.

As the transistor drain current is confined near to the surface under the gate oxide, the carrier transport is affected by traps present at the silicon-silicon oxide interface. The number fluctuation is generally believed to be the dominant $1/f$ noise mechanism in n-channel MOSFETs. However, the mobility fluctuation model tends to be better for explaining $1/f$ noise in p-channel MOSFETs. In an effort to have a “unified” model that applies to both pMOSFET and nMOSFET devices, the correlated number-mobility fluctuation theory ($\Delta N - \Delta\mu$) has been developed [80]. It postulates that the fluctuation in the number of carriers due to trapping can also cause a fluctuation in the mobility, because the trapped carriers act as Coulomb scattering

centers for the mobile carriers. The $(\Delta N - \Delta\mu)$, the ΔN , and the $\Delta\mu$ models have been reviewed to understand the role of oxide traps and charge in the oxide [81].

In the $(\Delta N - \Delta\mu)$ model, the spectral density of the drain current noise can be represented as

$$S_{I_D} = g_m^2 S_{V_G} \quad (2.33)$$

where g_m is the transconductance and S_{V_G} is the spectral density of the gate voltage fluctuations and given by [82]

$$S_{V_G} = S_{V_{FB}} \left[1 + \left(\alpha \mu_{eff} C_{eff} \frac{I_D}{g_m} \right) \right]^2 \quad (2.34)$$

where, μ_{eff} is the effective mobility, C_{eff} is the effective capacitance per unit area, consisting of the insulator layer, α is the Coulomb scattering coefficient, and $S_{V_{FB}}$ is the spectral density of the flatband voltage fluctuations, given by

$$S_{V_{FB}} = \frac{q^2 k_B T N_t \lambda}{f W L C_{eff}^2} \quad (2.35)$$

where N_t is the effective trap density, λ is the so-called McWhorter or tunneling parameter and L is the length of the MOSFET channel. The noise PSD is specified as [82]

$$S_{I_D} = g_m^2 \frac{q^2 k_B T N_t \lambda}{f W L C_{eff}^2} \left[1 + \left(\alpha \mu_{eff} C_{eff} \frac{I_D}{g_m} \right) \right]^2 \quad (2.36)$$

The first term in the parentheses in Equation (2.36) is due to the fluctuating number of inversion carriers and the second term to mobility fluctuations correlated to number fluctuations. The value

of α can be positive or negative depending on whether the mobility increases or decreases upon trapping a charge. In the next chapters, these parameters will be considered to minimize the intrinsic flicker noise to establish a better FET-based sensing element for lower strain detection.

2.3 Piezoresistive effect in silicon nanowires

To enhance the detection limits of the doped piezoresistors, strain engineering was considered as the most promising target for developing high-performance sub 10-nm piezoresistive sensing elements. Interesting electromechanical properties have been observed in carbon nanotubes, but nonlinear response and lower SNR were limiting factors [83]. Also, it was reported that silicon nanowires possess an unusually large piezoresistance (PZR) effect compared with bulk silicon. As shown in Figure 2.8a, the longitudinal piezoresistance coefficient was increased for p-type Si nanowires as high as $3550 \times 10^{-11} \text{ Pa}^{-1}$ in comparison with a bulk value of $94 \times 10^{-11} \text{ Pa}^{-1}$ [17].

Figure 2.8. (a) First-order longitudinal piezoresistance coefficient of p-type Si nanowires and its dependence on diameter and resistivity [17]. (b) Extracted gauge factor (GF) as a function of gate voltage. As V_{GS} increased from -10 to 3.75V, the device changed the behavior from a conventional piezoresistor ($GF \sim 50$) to ultrasensitive piezoresistor ($GF \sim 5000$) [20].

The p-type nanowire diameters were ranging from 50 to 350 nm and the giant piezoresistance was interpreted due to the strain-induced carrier mobility change and surface modification effects. Higher piezoresistance was also reported for n-type silicon nanowire, when the current flow was controlled by an external electric field. With the optimized nanowire doping and biasing conditions, the pinch-off region was formed and the mechanical stress was applied. As shown in Figure 2.8b, by combining the formation of the pinch-off region with mechanical stress, a modulation of the gauge factor by 2 orders of magnitude was achieved and phrased as electrically controlled giant piezoresistance in nanowires [20]. The giant piezoresistivity attracted huge attention [84, 85], due to a potential breakthrough for detecting motion in nanoelectromechanical systems. Moreover, since the mechanical stress is a key element for the performance enhancement of micro-electronic devices, the physical mechanism behind the giant PZR could prove to be an important phenomenon for the design of future nanoscale transistors.

Figure 2.9. (a) Apparent and true PZR for silicon nanowire (extracted at $V_{DS} = 0.5V$). (b) Relative conductance change of various samples under the mechanical stress. It is extracted using the stress modulation technique, together with typical values for n-type and p-type bulk silicon [21].

However, until now, there was no experimental and theoretical agreement regarding the origins of the giant PZR except two models show similar explanation [14, 86]. The first model [14] was based on a surface quantization effect and predicted the giant effect occurrence in the first few silicon monolayers, while the second model [86] was based on a stress-induced shifting of the surface Fermi level in depleted structures resulting from a change in the surface charge. Since the report on the giant piezoresistance, it was experimentally investigated in a large number of depleted silicon nano and microstructures. As shown in Figure 2.9a, it was experimentally verified that the observed resistance change in depleted structures were not true but dominated by electron and hole trapping at the surface [21]. The resistance was shown to vary strongly with time due to electron and hole trapping at the sample surfaces, which was independent of the applied stress. By modulating the applied stress in time, it was confirmed and shown in Figure 2.9b that the true PZR of the structures was comparable with that of bulk silicon [21].

In addition to the expected high sensitivity and superior signal quality due to the on-chip correlation analysis in time and space, silicon nanowire sensors could be mass manufactured at reasonable costs and readily integrated into electronic diagnostic devices to facilitate lab-on-a-chip applications. Finally, their small size makes them an ideal candidate for future sensing devices. Efforts to enhance the nanowire piezoresistive sensitivity and to reduce the intrinsic noise will be presented in the next chapters.

2.4 Surface strain in cantilever and diaphragm-based sensors

Microcantilevers attracted attention due to high sensitivity and their application as physical, chemical and biological sensors [87, 88]. In atomic force microscopy (AFM), use of cantilever as

a force sensor is a well-established application, taking advantage of silicon micromachining techniques to integrate it with integrated circuit (IC) process technology. The two main modes of cantilever operation are static and resonant, and the detection principles take account of changes in the deflection, surface stress, and resonance frequency. In the surface stress mode, the cantilever bends with nanometer deflection and requires an ultra sensitive readout method. The deformation of the cantilever sensor reflects the mechanical stress generated within the device. The radius of curvature of the cantilever after bending can be determined using Stoney's formula [89]

$$\frac{1}{R} = \frac{6(1-\nu)}{Et^2} \Delta\sigma \quad (2.37)$$

where R and t are the radius of curvature and thickness of the cantilever, respectively. $\Delta\sigma$ is the surface stress change, E is the Young's modulus of the silicon substrate. The deflection of the cantilever under the differential stress is defined as [52]

$$\delta = \frac{3L_c^2(1-\nu)}{Et^2} \Delta\sigma \quad (2.38)$$

where L_c is the cantilever length and the deflection is directly proportional to the differential adsorption-induced surface stress.

Figure 2.10. (a) SEM image of five microfabricated silicon rectangular cantilevers of different lengths supported by the same silicon chip. (b) Zoomed image of the cantilever having length=100 μm, width=40 μm and thickness=1 μm. (IMM, Mainz, Germany).

The surface stress is a function of the initial surface free energy of the substrate. Once the radius of curvature is determined, the tip displacement of a microcantilever with length L_c can be determined. The tip displacement can be correlated to the analyte concentration. The effective spring constant k of the uniform beam with a rectangular cross-section, which is fixed at one end and deflected at the other, is given by

$$k = \frac{EW_c t^3}{4L_c^3} \quad (2.39)$$

where W_c and t are the width and thickness of the cantilever, respectively. As the load is applied on the free end of the cantilever in force sensing applications, the sensing element location was near to the cantilever base to get the maximum stress effect. To generate the transverse stress on the cantilever surface, a force was applied on the top end part of the cantilever. After applying force F ($k \times \delta$), the maximum effective stress can be calculated with the relation [53]

$$\sigma_{\max} = \frac{6L_c}{W_c t^2} \cdot F = \frac{3Et}{2L_c^2} \delta \quad (2.40)$$

Under the induced stress, piezoresistor resistance change is proportional to stress [50]

$$\frac{\Delta R}{R} = \frac{\Delta \mu}{\mu} = \pi_l \sigma_l + \pi_t \sigma_t \quad (2.41)$$

where π_l and π_t are parallel and vertical piezoresistive coefficients, respectively. So, the relation between the current change of the piezoresistive transistor and the applied stress can be deduced from the relation [50]

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \mu_0}{\mu_0} = \left(\frac{\pi_s + \pi_{44}}{2} \right) \sigma_x + \left(\frac{\pi_s - \pi_{44}}{2} \right) \sigma_y + \pi_{12} \sigma_z \quad (2.42)$$

where π_{ij} represents the piezoresistive coefficients and σ_x, σ_y and σ_z are the three normal stresses. For lightly doped silicon piezoresistive coefficients, the drain current change for the MOSFET can be determined by using the values given in Table 2.1.

Another possible strain sensor design is based on MEMS diaphragm made of silicon, having additional advantages of better sensitivity, stability and sensor size. Diaphragm-based sensors have attracted attention in the past few years due to many applications in the field of automotive, aerospace and biomedicine. The piezoresistive component, including silicon diaphragm and piezoresistors, is the key element for the whole sensor performance. A lower density material was used to fabricate the diaphragm, which results in a better pressure sensitivity. Diaphragm-based sensors can be classified according to their working principles and each having some advantages to particular applications. The stress analysis of diaphragms is more complex than for cantilevers as the membrane is two-dimensional in nature. The governing equation for the rectangular diaphragm displacement under a uniform pressure loading P is [49]

$$\frac{\partial^4 w}{\partial^4 x} + 2 \frac{\partial^4 w}{\partial^2 x \partial^2 y} + \frac{\partial^4 w}{\partial^4 y} = \frac{P}{D} \quad (2.43)$$

where w is the normal displacement for a point of the diaphragm at a location (x, y) . The term D represents the rigidity of the diaphragm. The sensitivity is the most important parameter to evaluate the performance and superiority of the strain sensor. The sensitivity mainly depends upon the physical structure of the mechanical section and the location of the measurement device in the case of the lab-on-a-chip type sensor. For most cases, these diaphragms, either in circular, square, or rectangular shapes, can be treated approximately as thin plates subjected to lateral

bending by uniformly adsorption-induced stress. The parameter D is the flexural rigidity of the diaphragm, which can be expressed as [49]

$$D = \frac{Et^3}{12(1-\nu^2)} \quad (2.44)$$

where t is the thickness of the diaphragm. In the case of the sensor platform based on the circular diaphragm, if a is the radius of the diaphragm and F is the uniformly applied load, the maximum stress is given as [90]

$$\sigma_{\max} = \frac{3F}{4\pi t^2} \quad (2.45)$$

at the edge, and the maximum deflection occurs at the centre with the value of

$$\delta_{\max} = -\frac{3F(m^2-1)a^2}{16\pi Em^2 t^3} \quad (2.46)$$

where $m=1/\nu$. Once $\sigma_{\max}$ is known, the normalized resistance change can be theoretically calculated by using the piezoresistive values given in Table 2.1.

Figure 2.11. (a) Wheatstone bridge. (b) SEM images of the combined pressure micro sensor having the whole picture with the diaphragm (front side) and diaphragm (backside) [91].

The schematics of the piezoresistive structure and the bridge circuit used for the pressure sensor application are shown in Figure 2.11. A Wheatstone bridge comprises four piezoresistors embedded on the diaphragm and used to measure the pressure information. An electrical circuit is used to measure an unknown electrical resistance by balancing two legs of a bridge circuit. According to the piezoresistive theory, the resistance change after the application of pressure on the diaphragm is expressed as

$$\Delta R / R = \pi \cdot \sigma_{\max} \quad (2.47)$$

where $\sigma_{\max}$ and π is maximum stress and longitudinal piezoresistive coefficient of silicon, respectively. Under no pressure condition, the bridge is in balance and the output of the sensor is zero. However, once a pressure is applied, the bridge becomes unbalanced and the pressure converts to an output voltage signal. The output can be tested to compute the pressure value, which is proportional to the forced pressure. When using a current source I , the output signal becomes

$$V_{out} = I \cdot \Delta R = \pi \cdot \sigma_{\max} \cdot R \cdot I \quad (2.48)$$

Recently, a novel pressure sensor was proposed based on the MOSFET stress sensitive phenomenon, in which the source-drain current of the MOSFET changes with the stress in the channel region due to the application of pressure. A Wheatstone bridge is formed from two MOSFETs and two piezoresistors and this result in a better performance pressure sensor than conventional piezoresistive sensor. The drain current characterization of the MOSFET in the saturation region is described without pressure and given as [91]

$$I_{DS} = \frac{W\mu_p C_{ox} R}{2L} (V_{GS} - V_{Th})^2 \quad (2.49)$$

where μ_p is the hole mobility in the channel. After the pressure application on the diaphragm, the variation of the MOSFET current is proportional to the change of the channel mobility $\Delta\mu_p$ and the change in the piezoresistance is also proportional to the resistor mobility change $\Delta\mu_R$. Output of the sensor after the pressure application can be written as [91]

$$V_{out} = 2 \left(\frac{\Delta\mu_p}{\mu_p} + \frac{\Delta\mu_R}{\mu_R} \right) V_0 \quad (2.50)$$

The output voltage is proportional to the stress as well as the forced pressure. Compared to the traditional piezoresistive pressure sensor, this sensor showed better sensitivity with less power requirements. The proposed design provided a way to use transistors for the strain sensing application and the sensitivity can be further improved with the piezoresistive enhancement. Next chapters will be focused to improve the piezoresistive sensitivity of the transistors while minimizing the noise effects to achieve the best possible strain resolution.

As explained in previous sections, conventional piezoresistive sensors suffer from lower sensitivity and higher intrinsic noise and their usage is limited for measuring small strain differentials. When the strain range reduces and the sensitivity of the sensor increases, the effect of the intrinsic noise on the output signal becomes the limiting factor in the sensor design.

2.5 Proposal for gate-all-around FET-embedded MEMS sensors

Recent advances in technology have made it possible to fabricate nano-structures and to enhance the piezoresistive coefficient by shrinking the dimension. As discussed in section 2.3,

piezoresistive measurements have been carried out on nanowires and giant piezoresistance was claimed due to the reduced dimensions ($70 \text{ nm} < \text{diameter} < 370 \text{ nm}$) and larger surface/volume ratio effects. However, the combined effects of low-dimension, channel doping and biasing-voltage on nanowire piezoresistance and intrinsic noise was an unknown physical phenomenon, motivated a comprehensive study before claiming nanowire as better sensing element.

In this thesis, a novel piezoresistive sensing element based on the gate-all-around (GAA) nanowire transistor is proposed to maximize the strain detection limits. By using quantum-confinement effects, these miniaturized FET-based sensing elements (diameter $< 15 \text{ nm}$, channel length $< 200 \text{ nm}$) will be able to enhance the piezoresistive sensitivity and to reduce the intrinsic noise, which significantly improve the detection limits and make them adaptable for lower strain detection applications. FET-based sensing elements are integrated into cantilever and diaphragm structures to use as force and pressure sensors. In the development of low-pressure sensors, the diaphragm materials will be optimized to improve the diaphragm flatness and to get stable pressure sensitivity.

In the development of FET-based piezoresistive sensors, the piezoresistive sensitivity and intrinsic noise are separately analyzed in the subsequent chapters and experimentally tested with respect to geometric parameters and gate voltage. Flicker ($1/f$) noises are measured, which dominant for piezoresistive FETs are operating at low frequencies. The results presented in this work indicate that the GAA nanowire transistor-based sensing element has miniaturized size, higher piezoresistive sensitivity and lower intrinsic noise, and can be potentially used in ultrasensitive strain sensors.

Chapter 3

Microcantilever sensors with piezoresistive transistor read-out

This chapter introduces transistor-based sensing element for strain sensing applications. The proposed sensing element utilizes the piezoresistive properties of single crystal silicon, which was used as the transistor channel material. Employing the Micro Electro Mechanical Systems (MEMS) technology, high sensor sensitivities and resolutions have been achieved.

Microcantilevers with embedded metal-oxide-semiconductor field effect transistor (MOSFET) sensing element formulate simple and sensitive MEMS sensors. Recent advances in MOSFET as a transducer to detect the molecule binding-induced cantilever deflection has gained extensive attention due to its high sensitivity and direct compatibility with MEMS sensors. The first section of this chapter presents the design, fabrication, and characterization results on the piezoresistive effects of MOSFETs with different channel geometries embedded into cantilevers. Six different piezoresistive nMOSFET-embedded microcantilevers were designed and characterized to systematically study the impacts of different cantilever and transistor channel geometries on the device sensitivity. It was confirmed that the amount of change in the drain current is the same range as reported in the literature. For point-loading applications, transistors with lower channel width were optimal for relative drain current change even though their absolute current output is less. In particular, the embedded nMOSFET exhibited higher sensitivity by decreasing transistor channel width. Furthermore, theoretical equations were established and results were compared with experimental data to optimize cantilever and

transistor geometrical factors to achieve higher stress or force sensitivity. The low-frequency noise (LFN) characteristics of the devices showed better resolution for higher aspect-ratio transistors, and the measured drain current noise was in the nanoampere range. Results reveal useful design guidelines to enhance the MOSFET-embedded microcantilever sensitivity for various applications.

In the last section, three different pMOSFET-embedded microcantilevers are presented and their responses to physical displacements are evaluated. Effects of the gate bias on the drain current change and device sensitivity are investigated. Specifically, a wide tuning range above 200% was demonstrated for the pMOSFET with the width/length ratio of 5 within a gate bias span of 6 V. Such tunable feature can be very useful to compensate process variations and optimize device performance for maximum sensitivity. The preliminary results discussed in this chapter indicated that the MOSFET-embedded microcantilever sensors have compact size, high sensitivity, lower noise, rapid response and have a potential application as a stress sensor.

3.1 Introduction

Microcantilever-based sensors have attracted attention due to their small size and high sensitivity. Generally, microcantilever sensors offer numerous advantages such as simple implementation of sensor array and easy integration with electronic circuitry [92]. Adsorption-induced stress due to bimolecular mass binding on the single surface of microcantilever causes it to deflect [93]. The amount of deflection was detected with sub-nanometer resolution using optical, capacitive and electrical techniques [5, 6, 23]. The optical detection techniques were precise, however, required external devices for deflection measurement, which involves tedious calibration and laser alignment. The second commonly used technique was using piezoresistors

to measure the cantilever deflection. The merit of this technique was easy integration with application-specific integrated circuits (ASICs) [94]. Nevertheless, the major disadvantage of the conventional piezoresistive sensing is the inherent high noise level, which directly limits the resolution and the sensitivity [95]. As an alternative, sensors based on MOSFET offer much lower noise level, high sensitivity and direct integration with ASICs [96]. It has been reported that the piezoresistive coefficient of the piezoresistive nMOSFET is two times higher than the bulk silicon. This increment of piezoresistive coefficient was due to the electron quantum confinement in the inversion channel region [97].

While the piezoresistive effect has been comprehensively studied for bulk silicon from theoretical and experimental points of views, no work has been done on piezoresistive effects for transistors with different channel geometry. For transistors embedded inside microcantilevers, it was difficult to quantify the local stress under the point loading and hence, more data is required to fully understand the effect of stress on the piezotransistor drain current change. In conventional characterization method, stress is induced by bending the whole chip to determine the stress sensitivity of the embedded transistor. For practical force sensing applications, stress is applied non-uniformly within the embedded transistor channel region while the cantilever bends. Because these two different characterization methods have fundamentally different mechanical loading mechanisms, piezoresistive transistor optimized for conventional chip-bending characterization might not be optimal in force sensing applications. This work reports the design, fabrication, and characterization results on the piezoresistive effects of six nMOSFETs with different channel geometries embedded into cantilevers. A PZT-based nano indentation system was used to explore the sensor sensitivity for different channel width-to-length ratios transistors under the applied stress.

3.2 Design of transistor-embedded cantilever platform

Figure 3.1 shows the schematic representation of the device. To apply transverse stress on the MOSFET channel, a force is applied on the free end of the cantilever, and the nMOSFET was placed near the anchor of the cantilever to be exposed to the maximum stress.

Figure 3.1. Schematic of the sensor structure with nMOSFET embedded in the cantilever.

As discussed in Chapter 2, the working principle of this device is based on increase in the drain current of a transistor in response to a force applied on the cantilever free end. It has been demonstrated that the carrier mobility of the piezotransistor is affected by the mechanical stress and the drain current change is proportional to the applied stress [98]. The relationship is described as

$$\Delta I_{DS} \propto \sigma_{ch} \quad (3.1)$$

where ΔI_{DS} and σ_{ch} are the drain current change and effective stress on the whole piezotransistor channel, respectively. The effective spring constant k of the cantilever with a rectangular cross section can be expressed as $k = Ebt^3/4a^3$, where b , t , a and E are width, thickness, length of the cantilever and Young's modulus of silicon (169 GPa), respectively.

Under an applied force F_A at the free end on the cantilever, the surface stress $\sigma(y)$ varies along the length y of the cantilever and can be calculated by [99]

$$\sigma(y) = \frac{6(a-y)}{bt^2} F_A = \frac{3Et}{2a^3} \delta(a-y) \quad (0 \leq y \leq a) \quad (3.2)$$

The maximum stress at the anchor of the cantilever with $y = 0$ can be formulated as

$$\sigma_{\max} = \frac{6a}{bt^2} F_A = \frac{3Et}{2a^2} \delta \quad (3.3)$$

where δ is the deflection at the free end of the cantilever. Equation (3.2) shows that the magnitude of the stress level is significantly different along the cantilever length. However, the expression has no influence on the cantilever width (b). In other words, the stress varies with the MOSFET channel in y direction under the applied force at the cantilever free end. For a MOSFET with channel width W , the effective stress in the channel can be calculated by averaging the point stress across the whole channel region

$$\sigma_{ch} = \frac{1}{W} \int_0^W \sigma(y) dy = \frac{3Et}{2Wa^3} \delta \int_0^W (a-y) dy = \frac{3Et}{2a^3} \delta \left(a - \frac{W}{2} \right) \quad (3.4)$$

The expression for the channel stress, which is the function of the transistor channel width (W) and cantilever length (a) under transverse stress application, neglects the influence of the transistor channel length (L). Since the transistor channel length orientation is along the cantilever width, which makes the stress variation independent of the transistor channel length. The cantilever beam is exposed to tensile longitudinal stress above the neutral plane and compressive stress below it. After the stress is induced, the channel resistance change in the transistor is proportional to the stress applied [89]

$$-\frac{\Delta R_0}{R_0} = \frac{\Delta \mu_{R0}}{\mu_{R0}} = \pi_l \sigma_l + \pi_t \sigma_t \quad (3.5)$$

where π_l and π_t are longitudinal and transverse piezoresistive coefficients, respectively. For the channel in the $\langle 110 \rangle$ direction, the relationship between the current change of the piezoresistive transistor and the applied stress can be deduced from the following equation:

$$\frac{\Delta I_{DS}}{I_{DS}} = \pi_{\langle 110 \rangle} \sigma_{ch} = \left(\frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) \sigma_{ch} \quad (3.6)$$

where π_{11} , π_{12} , π_{44} are the three major piezoresistive coefficients of the cubic structure of lightly doped silicon and σ_{ch} is the effective stress on the MOSFET channel in the transverse direction (drain current direction is perpendicular to the applied stress) as given in Equation 3.3.

The quantitative relationship between the transistor drain current change and the stress is governed by piezoresistance effects. When a uniaxial stress is applied perpendicular to the current flow, the transverse piezoresistive coefficient dominates and the stress sensitivity can be defined as the relative change in the drain current per unit channel stress:

$$\text{Stress sensitivity} = \frac{\Delta I_{DS} / I_{DS}}{\sigma_{ch}} \quad (3.7)$$

3.2.1 Constructing nMOSFET-embedded cantilevers

To study the influence of the stress on the drain current change, cantilevers with long channel nMOSFETs have been fabricated using the standard transistor process flow combined with MEMS fabrication techniques on the 4-inch p-type silicon-on-insulator (SOI) wafers having 5 μm top Si device layer with $\{100\}$ surface and $\langle 110 \rangle$ channel direction, as shown in Figure 3.2. The devices of this work are planar nMOSFETs with the channel length $L=20 \mu\text{m}$ (device A, B, F) and $L=30 \mu\text{m}$ (device C, D, E). The channel width varies and resulting in different channel

width-to-length ratios, as listed in Table 3.1. In all devices, multi-length silicon cantilevers are used with 5 μm thickness (t). A cantilever width of $b=200\text{ }\mu\text{m}$ was selected for all devices.

Table 3.1: Parameters of piezotransistors on cantilevers.

Device	Cantilever $b \times a$ (μm^2)	Channel W (μm)	Channel L (μm)
A	200 $\times$ 500	60	20
B	200 $\times$ 500	200	20
C	200 $\times$ 500	300	30
D	200 $\times$ 250	60	30
E	200 $\times$ 300	90	30
F	200 $\times$ 300	90	20

Since the stress magnitude strongly depends on the specific locations of the cantilever under bending, the piezoresistive transistor channel was positioned near the cantilever anchor to experience the maximum stress concentration during the cantilever bending. By applying the stress on piezoresistive transistors, the change in the drain current was measured and compared for all devices at the same biasing conditions to explore the correlation between the stress sensitivity and device geometries.

3.2.2 Fabrication processes and results

The fabrication process of the transistor-embedded microcantilever was started with a 1 μm field oxide growth on both sides of the wafer in the furnace by using the wet oxidation method. Secondly, the diffusion window was opened for the source and drain via lithography. Thirdly, n-type doping was completed through phosphorus doping by the solid state diffusion process (Figure 3.2a). The diffusion process includes two steps, predeposition and drive-in. The fourth step is the oxide removal and gate oxide formation by dry oxidation at 1000 $^{\circ}\text{C}$ for 36 minutes

(Figure 3.2b). The next step is contact opening (Figure 3.2c) followed by metal patterning for source, drain and gate (Figure 3.2d).

Figure 3.2. Fabrication processes for the proposed piezotransistor-integrated cantilever. (a) Active area patterning on SiO_2 layer followed by N^+ diffusion. (b) N^+ drive-in and gate oxidation. (c) Contact opening for the source and drain. (d) Sputtering Cr/Au on the front side. (e) Cantilever patterning on the top surface followed by deep reactive ion etching (DRIE) silicon etching. (f) Release of device by DRIE.

After the completion of transistor fabrication, the cantilever structure is defined by front side patterning and deep reactive ion etching (DRIE) of the silicon device layer (Figure 3.2e). Next, the release of the cantilever from bulk silicon is achieved by DRIE etching from backside (Figure 3.2f). A layer of 10 μm photoresist serves as an etching mask for DRIE and 1 μm buried-oxide (BOX) layer is used as an etching stop layer. After the BOX layer is removed, the entire piezotransistor-embedded cantilever fabrication process is completed.

Figure 3.3 shows SEM images of the fabricated piezoresistive transistor- embedded cantilever. It is clear that the transistor is placed near to the anchor of the cantilever to experience the maximum stress in the channel region during the cantilever bending to maximize the drain current change.

(a)

(b)

Figure 3.3. SEM images of the piezotransistors (channel length=20 μm) embedded cantilevers. (a) nMOSFET with a channel width =60 μm . (b) nMOSFET with a channel width =200 μm .

After device fabrication, all transistors embedded in the cantilever were characterized under the external applied stress to determine the drain current change and the stress sensitivity for various

transistor channel geometries. For the stress sensing application, the drain current flows along the $\langle 110 \rangle$ direction and the mechanical stress was applied perpendicular to the current flow.

3.3 Electromechanical characterization

A PZT-based nano-indentation system is used to explore the sensor sensitivity for different channel width-to-length ratios transistors under the applied stress. To apply the transverse stress on the channel, the force was applied at the free end of the cantilever using a lead zirconate titanate (PZT)-based nano-indentation system (Physik Instrumente GmbH & Co. KG), which was vertically mounted on the DCM 2000 micro-manipulator (Cascade Microtech, Inc.) as shown in Figure 3.4a. The precise deflections at the free end are obtained by increasing the piezo bias on the PZT actuator. The spring constant of the microcantilever is calculated and it is almost 0.2 % compared to the indenter spring constant. Therefore, the compliance due to the indenter could be considered negligible for loading applications.

(a)

Figure 3.4. (a) Photograph of the PZT actuator-based deflection set-up. (b) Schematic representation of the cantilever beam deflection under an applied force.

Figure 3.4b schematically represents the deflection of the cantilever when the force F is applied at the cantilever free end. The diameter of the stylus pin is about $3\ \mu\text{m}$ and its vertical displacement was controlled with $100\ \text{nm}$ resolution. The stylus was exactly moved down with the movement of the PZT actuator and the cantilever deflection is precisely controlled in steps to measure the transistor drain current changes (ΔI_{DS}) at the pre-set deflection variations (Figure 3.5). The different width-to-length ratio nMOSFET-embedded microcantilevers are designed and characterized under applied stress to study the impacts of transistor channel width on the device sensitivity. Additionally, different cantilever designs are considered with the same width-to-length ratio to analyze the influence of the cantilever length on the sensor sensitivity.

3.3.1 Piezoresistive measurements and discussions

Electrical characteristics of the fabricated devices were measured using a semiconductor parameter analyzer (HP4156B) under the applied stress. The change in the drain current per unit

stress $(\Delta I_{DS}/I_{DS})/\sigma_{\max}$ due to the piezoresistive effect in the nMOSFET was found to be dissimilar for different channel width devices.

Electrical measurements of the transistor drain current change under applied stress were measured by sweeping V_{DS} from 1 to 5 V for $V_{GS} = 1$ V, 2 V and 3 V respectively. Figure 3.5 shows I_{DS} - V_{DS} curves with and without the external stress, exhibiting a significant drain current change after the applied stress. The cantilevers were characterized under the point loading at the free end and the stress difference was distributed along the length of the cantilever. The applied stress is localized near the cantilever base and the piezotransistor sensing element is placed near the cantilever anchor to achieve maximum benefit from the localization of high stress difference during the cantilever bending.

Figure 3.5. I_{DS} - V_{DS} curve for device with width-to-length ratio=3 ($W = 90 \mu\text{m}$, $L = 30 \mu\text{m}$) with and without the applied stress.

The drain current variation versus the applied mechanical stress is presented in Figure 3.6 for all devices. Figure 3.6(a-c) show the transistor drain current change at a fixed gate voltage ($V_{GS} = 3V$) under the transverse tensile stress. It can be seen from the results that the relative drain

current change per unit stress is not constant for different channel width transistors. In particular, the stress sensitivity significantly decreases as the channel width becomes larger.

Figure 3.6. Channel width/length dependence on the drain current sensitivity for microcantilevers with mechanical stress loading: piezotransistor channel width $60 \mu m$ in (a), $100 \mu m$ in (b) & $300 \mu m$ in (c); piezotransistor channel width $60 \mu m$ in (d), $90 \mu m$ in (e), & $90 \mu m$ in (f). $V_{DS} = 5 V$ and $V_{GS} = 3 V$ are used in all measurements.

In Figure 3.6(a) & 3.6(d), the transistor drain current change shows the current change for the devices with same transistor width but having different cantilever lengths. Furthermore, drain current change results are shown for the devices of similar transistor width but different channel lengths in Figure 3.6 (e) & 3.6(f). Some significant implications can be drawn from these results. It has been found that piezoresistive effects dominate the drain current change under the mechanical stress. For the same channel length, the relative current change appears more prominent for the smaller width transistors, clearly indicating the different stress sensitivity of dissimilar channel geometry transistors. Another set of measurements was repeated to ensure the repeatability of the results under a transverse stress. The maximum stress ($\sigma_{\max}$) induced in the cantilevers was extracted from the amplitude of the cantilever's tip deflection. Additionally, effective stress on the channel (σ_{ch}) is calculated by Equation 3.4 and the drain current change (%) is plotted versus $\sigma_{\max}$ and σ_{ch} as shown in Figure 3.6. Experimental and theoretical stress sensitivities of each device are evaluated from the drain current change slopes. The slopes under the stresses illustrate little difference for the lower channel width transistors because of small difference between σ_{ch} and $\sigma_{\max}$ values. However, the slope is largely different for the larger channel width transistors as the channel cover significant distance along the cantilever length and σ_{ch} becomes much lesser compared to $\sigma_{\max}$ (Equation 3.4). Under the same stress, the percentage current change per unit stress (%) was found to be lesser for larger channel width transistors. The observed drain current change is of comparable magnitude to recent literature for the transistors [98]. Figure 3.7 shows the cantilever piezotransistor response to different designs and confirms that the device having the lower channel width shows more drain current change (%) compared to the larger channel width devices.

Figure 3.7. Relative drain current change comparison of nMOSFET devices comprises different channel widths. $V_{GS} = 3$ V in this measurement.

The drain current change of the nMOSFET with 20 μm channel length devices was reduced by about 53 % by increasing W from 60 to 200 μm under similar applied stress. Furthermore, the drain current change of the nMOSFET with 30 μm channel length devices was reduced by about 63.6 % by increasing W from 60 to 300 μm . Since smaller width-to-length ratio device (device A) has the channel position nearer to the cantilever anchor and the minor difference in the values of $\sigma_{\max}$ and σ_{ch} makes its sensitivity higher compared to that of large channel width devices (device B and C). The transistor channel can be considered as a series of short channels. During the cantilever bending, channels near the base experience the maximum stress and subsequent channels have lower stress component in proportion to their specific locations. The total stress then can be integrated as to find the average channel stress (σ_{ch}) on the transistor channel, which is accountable for the drain current change. Furthermore, the effective channel stress (σ_{ch}) is calculated from Equation 3.4 and the theoretical drain current change (%) is plotted and compared to experimental results. It is found that experimental sensitivities for all devices

exhibit comparable values to the theoretical estimate from Equation 3.4. However, the difference in device sensitivities could be due to device dimension variance during the fabrication processes, i.e. slight over etch (or under etch) during the cantilever release and misalignment during the litho processes.

The channel length is oriented along the cantilever width and the induced stress is independent of the cantilever width (b) as specified in Equation 3.2 and Equation 3.4. Cantilever type E and F, with the same transistor channel width and cantilever geometry, show similar sensitivity, despite both devices having different transistor channel length (Figure 3.8).

Figure 3.8. Column plot of drain current change response for microcantilever devices. Each column represents the percentage drain current change response to applied stress (experimental & theoretical). (a) Sensitivity plot of transistors with same channel width but different channel length, (b) Sensitivity plot of transistors with same channel width but different cantilever length. $V_{GS} = 3V$ in this measurement.

Consequently, the stress sensitivity is measured to be independent of channel length. Furthermore, the effect of the cantilever length is analyzed on the device sensitivity. Under the same stress, the drain current change (%) was measured for device A and device D which has the same channel width but different cantilever length. It is found that device A shows slightly

higher stress sensitivity than device D. Experimental results for the sensitivity ratio ($\text{Sensitivity}_{\text{Device-A}} / \text{Sensitivity}_{\text{Device-D}} = 1.10$) are found very close to theoretical calculated sensitivity ratio ($\text{Sensitivity}_{\text{Device-A}} / \text{Sensitivity}_{\text{Device-D}} = 1.07$) as calculated by Equation 3.4. The observed sensitivity change could be due to the fabrication uncertainties (over etching or under etching) during the device fabrication.

Since the cantilever length is not same in all devices, the applied force is normalized and the absolute current is compared as an output. Higher force sensitivity is observed for devices that have higher W/L ratio as shown in Figure 3.9.

Figure 3.9. Force sensitivity response due to an applied point load for six cantilever devices. W and L are transistor channel width and length respectively.

For $L=20 \mu\text{m}$, device B shows more than four times force sensitivity than device A ($W/L=3$) and F ($W/L=3.5$). Similarly for $L=30 \mu\text{m}$, device C has higher sensitivity compared to device D ($W/L=2$) and E ($W/L=3$). For point-loading applications, the long channel length device ($L=30 \mu\text{m}$) exhibits lower force sensitivities compared to their smaller channel length counterparts ($L=20$

μm), despite both having similar channel width and cantilever dimensions (device E and F). Next, device A and D have similar channel width, showing better sensitivity enhancement for device A because of longer cantilever length. By comparing all devices in terms of absolute current output, it is concluded that long cantilevers embedded with short channel length and higher aspect-ratio transistors are better suited for point-loading force sensing applications.

3.3.2 Low-frequency noise characterization

The low-frequency noise measurements are conducted to calculate the drain current noise for all devices. Spectral noise measurements were performed using a battery-powered SR570 low-noise current preamplifier and a HP35670A dynamic signal analyzer. Careful calibration procedures have been taken to reduce the background noise within acceptable range. The drain-current noise spectral density curve in Figure 3.10 shows $1/f$ noise of the nMOSFET (device E) at $V_{DS}=100$ mV and $V_{GS}=3$ V.

Figure 3.10. Drain-current noise spectral density curve of cantilever device E ($W = 90 \mu\text{m}$, $L = 30 \mu\text{m}$) showing $1/f$ noise in the embedded nMOSFET.

The drain current noise amplitude was measured for each device from the spectral density curve shown in the low frequency range as shown for device E. The measured noise amplitude values were 3.5 nA (device A), 6 nA (device B), 7 nA (device C), 4 nA (device D), 5 nA (device E) and 4 nA for device F. For all devices, similar noise amplitude values indicate low noise in the nMOSFET sensing element.

To compare the performance of the force sensors, minimum detectable force (MDF) is used to define the resolution. The MDF is the noise equivalent force, which is defined as the drain current noise amplitude (I_N) divided by the force sensitivity

$$MDF = \frac{I_N}{(\Delta I_{DS} / F_A)} \quad (3.8)$$

where I_N is the drain current noise and ΔI_{DS} is the change in the drain current due to the applied force on the cantilever end. From the measurements of the spectral current noise at 1 Hz, I_N and ΔI_{DS} , the calculated MDF for each device is shown in Figure 3.11.

Figure 3.11. Minimum detectable force sensitivity for six cantilever devices.

With higher ΔI_{DS} and the similar drain current noise, the MDF is found to be higher for devices embedded with higher aspect-ratio transistors. The optimum MDF (70 nN) was found for device B. Similarly, for $L=30\text{ }\mu\text{m}$, the optimum MDF (130 nN) was found for device C.

Other important parameters that can affect the sensitivity are carrier mobility and doping profile in the transistor channel. In all devices, the transistor channel was boron-doped silicon substrate with low doping concentration ranging from 1×10^{15} to $6 \times 10^{15}\text{ cm}^{-3}$. For each device in this work, the carrier mobility was determined by measuring the linear region transfer characteristics and the variation is observed to be less than 3% for all transistors.

3.4 Fabrication of pMOSFET-embedded microcantilever

This section presents the design, fabrication, and piezoresistive testing results of pMOSFETs with different channel geometries embedded into cantilevers. The influences of the gate bias and transistor geometries (i.e. channel width and channel length) are investigated on the device sensitivity. The devices of this work are planar pMOSFETs with the channel length $L=30\text{ }\mu\text{m}$ and varied channel width, resulting in different channel width-to-length ratios, as listed in Table 3.1. In all devices, the multi-length silicon cantilevers were used with $3\text{ }\mu\text{m}$ thickness (t).

To study the influence of stress on the drain current change, cantilevers with long channel pMOSFET transistors have been fabricated using the combined CMOS-MEMS fabrication techniques on the 4-inch n-type silicon-on insulator (SOI) wafers having $3\text{ }\mu\text{m}$ top Si device layer with $\{100\}$ surface and $\langle 110 \rangle$ channel direction. Silicon cantilevers were $300\text{ }\mu\text{m}$ long, $200\text{ }\mu\text{m}$ wide and $3\text{ }\mu\text{m}$ thick. The sensing element was planar pMOSFET with the channel length $L=30\text{ }\mu\text{m}$. The channel width varies and resulting in different channel width-to-length

ratios of 2, 3, and 5. In order to lower the noise level, $3\text{ }\mu\text{m}$ thickness was designed to give better mechanical strength. The fabrication process steps of the pMOSFET-embedded microcantilever were similar to nMOSFET shown in the earlier section (Figure 3.2). However, the pMOSFET fabrication has two different process steps as compared to the nMOSFET: first, the starting wafer was n-type and second, the doping in source and drain was p-type.

After the fabrication of the pMOSFET, the silicon cantilever beams were defined by $3\text{ }\mu\text{m}$ top silicon etching followed by cantilever release from backside silicon etching. Silicon oxide layer (buried oxide in SOI) was used as an etch stop layer during through etching. Figure 3.12 shows the SEM image of the fabricated pMOSFET-embedded cantilever structure. Under the cantilever bending, the stress magnitude was strongly dependent on the specific locations of the cantilever surface along the cantilever length.

Figure 3.12. SEM of the fabricated microcantilever embedded with the PMOSFET. Cantilever is $300\mu\text{m}$ long, $200\mu\text{m}$ wide and $3\mu\text{m}$ thick.

3.4.1 Deflection measurements

To apply the transverse stress on the cantilever, a point force was applied at the free end of the cantilever using a similar PZT-based nano-indentation system as described earlier in Figure 3.3. The drain current was measured at the 5 μm steps in incrementing and decrementing deflection and the difference in the drain current is found to be negligible for both upstroke and downstroke. Results of the drain current change with the sweeping deflections show a nearly linear dependence (Figure. 3.13b) and absence of hysteresis confirms the accuracy of PZT-based indenter.

Figure 3.13. (a) Cantilever beam deflection under an applied force. (b) I_{DS} at different cantilever deflection for up and downstroke.

The channel lengths L_{ch} of the three pMOSFETs were kept the same at 30 μm while the channel widths were different. To apply the desired physical displacement, a PZT nano-indenter (Physik Instrumente P-245.5S) was vertically mounted on a DCM 2000 micro-manipulator (Cascade Microtech, Inc.) with an attached probe pointing at the free end of the cantilever. I-V characteristics of the pMOSFETs were obtained using the HP4156B semiconductor parameter

analyzer. The source-drain voltage V_{DS} was biased at 5 V throughout the testing, which was well below the impact ionization threshold. The normalized drain current change of various devices under the external stress was characterized and transfer characteristics of a pMOSFET transistor with $W_{ch}(90\text{ }\mu\text{m})/L_{ch}(30\text{ }\mu\text{m}) = 3$ are shown before and after mechanical strain in Figure 3.14. Systematic measurements for the dependence of drain current change on the width-to-length ratio were performed.

Figure 3.14. I_{DS} - V_{DS} curve before and after applied strain.

As shown in Figure 3.15, the drain current change of the strained pMOSFET with a W/L of 150 $\mu\text{m}/30\text{ }\mu\text{m}$ was reduced by 87% compared to that of the pMOSFET with a W/L of 60 $\mu\text{m}/30\text{ }\mu\text{m}$ under a gate bias of -4V. Furthermore, the drain current change of the pMOSFET was reduced almost 58% by increasing W from 60 to 90 μm under the same gate bias. Another set of measurements was repeated at $V_G = -7\text{V}$ to ensure the repeatability of the results under a transverse stress. The drain current change was not the same at different gate potential but results follows the similar trend for different aspect-ratio devices. It has been found that piezoresistive effects dominate the drain current change under the mechanical strain. The enhancement of the

carrier mobility under the strained silicon is due to the reduction of an effective mass in the lowest sub-band as suppressed inter-valley scattering attributable to sub-band splitting. Under the biaxial strain along (100) plane, the six-fold degeneracy of the silicon conduction band is lifted, making the effective mass lower and conductivity higher [100].

Figure 3.15. ΔI_{DS} (%) for different W/L ratio transistors; (a) $V_G = -4\text{V}$, (b) $V_G = -7\text{V}$.

The variation in the sensitivity can be explained by the fact that the distance between the transistor channel and the maximum applied strain location on the cantilever is nearer for smaller channel width-to-length ratio devices, and hence experience larger stress, resulting in enhanced piezoresistive effects or drain current. As a result, the maximum drain current change was obtained for a combination of particular gate voltage and aspect ratio.

3.4.2 Gate bias tunable piezoresistance in pMOSFET

As described earlier, the piezoresistivity effect in silicon arises from the change in the carrier mobility due to strain-induced band energy shift, band warping and carrier repopulation. In the case of microcantilevers, the average surface stress σ_{ch} in the pMOSFET channel region is given in Equation (3.4). In response to the physical displacement δ , the drain current of the pMOSFET varies in the form

$$\frac{\Delta I_{DS}}{I_{DS}} = \alpha \pi \sigma_{ch} \propto \pi \left(L - \frac{W_{ch}}{2} \right) \delta \quad (3.9)$$

where π is the piezoresistive coefficient of silicon and α is the correction factor accounting for the carrier concentration and stress dependence normal to the cantilever surface.

In Figure 3.16, the drain current variation at fixed applied mechanical strain is presented for all devices at different gate bias. It is found that the relative drain current change at fixed stress has significantly changed for different width-to-length ratio transistors. For the same channel length, the relative current change appears more prominent for smaller width transistors, clearly indicating the different sensitivity for dissimilar channel aspect-ratio transistors. Figure 3.16 lists the relative drain current change of the pMOSFET in response to the applied displacement. The overall current change was highest in the first pMOSFET due to its smallest channel width W_{ch} and highest channel stress σ_{ch} , as expected from Equation (3.4).

(a)

(b)

(c)

Figure 3.16. Drain current change versus gate bias voltage under different cantilever displacement with pMOSFET having: (a) $W_{ch}(60 \mu m)/L_{ch}(30 \mu m)=2$, (b) $W_{ch}(150 \mu m)/L_{ch}(30 \mu m)=5$ and (c) $W_{ch}(90 \mu m)/L_{ch}(30 \mu m)=3$. V_{DS} was fixed at 5 V during the testing.

It was also observed that the drain current change in the first pMOSFET increases with the gate bias voltage V_{GS} . This can be attributed to the enhanced piezoresistive coefficient π at higher V_{GS} [101]. The source-drain current of a transistor was determined by the carrier transport through its surface inversion layer. In the inversion layer, the carriers were confined in a triangular potential well formed by the source, drain and gate and the carrier energies are quantized into sub bands. The sub-band energy levels are influenced by the transverse electrical field from V_{GS} and changed by the applied mechanical stress. Consequently, the repopulation of the charge carriers among different valleys results in the mobility change in the inversion layer. Hence, the piezoresistive effect depends on V_{GS} as well. However, the second pMOSFET in Figure 3.16b exhibited the opposite trend of the drain current change. This is believed to be due to the

increased inversion layer carrier concentration at elevated V_{GS} . Kanda's classical model predicted that the piezoresistive coefficients vary with the Fermi level as a decreasing function of concentration [43]. Apparently, for this second pMOSFET, the effect of carrier concentration was the dominant factor and the aforementioned enhancement effect becomes less significant. Specifically, under 10 μm displacement, the drain current change decreased from 6.5% at $V_{GS}=-1$ V to 2% at $V_{GS}=-7$ V, manifesting a tuning range of more than 200%. Next, in order to demonstrate the transition of the gate bias effect from enhancement to suppression on the drain current change, the third pMOSFET with a medium W_{ch}/L_{ch} ratio of 3 was characterized and the measurement results clearly show that the drain current change increases at low V_{GS} but decreases at high V_{GS} . Under an applied force F at the free end on the cantilever, the optimum deflection sensitivity obtained was 600 pA/nm for $W_{ch}(60 \mu\text{m})/L_{ch}(30 \mu\text{m})=2$, 730 pA/nm for $W_{ch}(90 \mu\text{m})/L_{ch}(30 \mu\text{m})=3$ and 1.45 nA/nm $W_{ch}(150 \mu\text{m})/L_{ch}(30 \mu\text{m})=5$ devices. It should be clarified that three pMOSFET's different responses to V_{GS} were not due to the threshold voltage. Measured threshold voltages for three pMOSFETs were very close. Their respective values were -0.25 V, -0.23 V and -0.28 V. Hence, other factors such as non-uniform stress distribution in the channel region, should be further investigated and still be the potential topic for future research.

3.5 Conclusion

The stress sensitivity response for various channel geometry transistors was characterized by measuring the micromechanical response of the cantilevers upon bending. Results demonstrated the sensitivity output for a wide range of width/length ratio transistors and found the optimized parameters of channel designs to achieve the maximum sensor sensitivity. A sensitivity increment of 63.6% was observed for embedded transistor devices with smaller width ($W=60$

μm) transistors compared with the larger width ($W=300\text{ }\mu\text{m}$) ones. For force sensing or AFM applications, higher aspect-ratio transistors were optimal for absolute current change, however lower aspect-ratio transistors provided better current change in percentage. The LFN characteristics of the transistors show the drain current noise in the sub-nanoampere range and an optimized resolution (minimum detectable force $=70\text{ nN}$) was obtained for the higher aspect-ratio device. These results, along with previous developments in miniaturized cantilever sensors, make it feasible for these sensors to be used in many sensing applications such as ultra-sensitive stress and force transducers.

Next, the pMOSFET-embedded microcantilevers are reported as displacement sensors. Displacement testing revealed highest overall current change for the smallest pMOSFET due to the high localized mechanical stress. The shrinkage of the channel aspect ratio of the pMOSFET, from 5 to 2 at a fixed channel length at $30\text{ }\mu\text{m}$, enhances the drain current change considerably for different gate voltages. Furthermore, a wide tuning range of more than 200% was achieved for the relative drain current change through the modulation of the gate bias. However, within the same span of the gate bias, pMOSFET with different width to length ratio exhibited different trends due to the adverse effects between the sub-band energy shift and the inversion carrier concentration variation. As sensor dimensions are progressively evolving into sub-micron and nanometer regimes, such tunable feature of the piezoresistive pMOSFETs provides valuable opportunities to compensate process variations and tailor sensor performance for specific applications.

Chapter 4

Piezoresistance and noise in gate-all-around nanowire FET

It was established in Chapter 3 that planar transistors provide increased sensitivity and lower noise compared to doped piezoresistors. The ability to construct nanowire channel transistors will expand the piezoresistive sensitivity in ways that are not possible with bulk transistor devices.

This chapter reports the gate-all-around nanowire field-effect-transistor (GAA NWFET) as piezoresistive sensing element. The detailed fabrication processes and electro-mechanical characterization are discussed. In GAA structure, gate surrounds the nanowire channel, which provides easier carrier creation/depletion with the use of low gate bias. The surrounding gate also provides complete shielding from environmental charges and prevents humidity effects to change the drain current that are independent of stress. With narrow gate bias span of 0.8 V near the threshold region, the piezoresistive coefficient of NWFET enhanced up to seven times under both compressive and tensile strain conditions. Results revealed the reduction of low-frequency noise of NWFET when biased in the subthreshold region, improving the resolution, i.e. minimum detectable strain by sixteen times. Results revealed that GAA NWFET can be used as miniaturized and ultrasensitive sensing element for nanomechanical sensors.

Furthermore, the nanoelectromechanical pressure sensor based on nanowire and NWFET sensing element was demonstrated in the following section to enhance the pressure sensitivity and signal-to-noise ratio. It was observed that the sensitivity of the pressure sensor can be enhanced up to

four times when NWFET operated in the subthreshold mode instead of the inversion mode. The sensitivity enhancement is attributed to carrier confinement inside the nanowire channel, which is obtained by gate bias tuning. The low-frequency noise characteristics showed the significant reduction in the drain current noise for NWFET when biased in the subthreshold region, enhancing the signal-to-noise ratio (SNR) three orders of magnitude in the subthreshold region compared to inversion region. Results showed that NWFET-based pressure sensor operates at low bias with higher piezoresistance and can be used to measure low pressures with high signal-to-noise ratio.

4.1 Introduction

As reviewed in Chapter 2, the piezoresistive effect of silicon has been extensively used for numerous applications in physical transducers. Silicon channel is used in planar MOSFETs and higher piezoresistance and lower noise were demonstrated in Chapter 3. With the progress of scaling down devices, there were rapid developments of micromachining technology and researchers focused on a range of nano-materials, such as silicon nanowires [102] and carbon nanotubes [103], as sensing element due to their smaller size and higher sensitivity. The small diameter and the larger surface-to-volume ratio rendered nanowires as an ideal transducer for piezoresistive sensing applications. Also, the stable and reproducible electrical property of silicon nanowires produced precise and reliable measurement. Piezoresistive measurements have been carried out on nanowires and giant piezoresistance was claimed due to the reduced dimensions ($70\text{ nm} < \text{diameter} < 370\text{ nm}$) and larger surface/volume ratio effects [17, 104]. The higher piezoresistance was also reported in partially depleted nanowires, and the substrate bias voltage is used to reduce the carriers inside the nanowire channel [20]. The anomalous

piezoresistive effect has been interpreted as a combined effect of electric field and mechanical stress on the constricted current channel. Though higher sensitivity was reported, there have been large differences in the piezoresistive coefficient obtained by different researchers and giant piezoresistance in nanowires was not successfully reproduced. It was accounted that the apparent giant piezoresistance was not because of applied stress but due to charge trapping and subsequent relaxation at the exposed SiO_2 layers on the nanowire surfaces [21]. The combined effect of low-dimension and biasing voltage on nanowire piezoresistance and intrinsic noise was an unknown physical phenomenon, motivating a separate study before claiming nanowire as a better sensing element.

Pressure is an important physical parameter in medical diagnostics such as blood pressure measurements. A silicon nanowires-embedded ultrasensitive piezoresistive pressure sensor was fabricated and characterized in the next section which potentially can be used to measure lower pressure especially for biomedical applications. In the next section, results are presented for nanowires integrated into suspended diaphragm and its electrical characteristics were measured under the applied pressure.

4.2 Silicon nanowire embedded pressure sensor

The pressure sensor with piezoresistive silicon nanowires (NWs) of dimension 90 nm x 150 nm was fabricated using p-type $\langle 100 \rangle$ 1170 Å SOI wafer by lithography process followed by resist trimming, dry etching and thermal oxidation. With the advancement of fabrication technology, SiNWs were fabricated using normal CMOS process and successfully embedded within 3.1 μm thick diaphragm. Subsequently, these NWs were doped by implantation of BF_2 with concentration dose of 1×10^{14} ion/ cm^2 . There were 4 pairs of NWs located symmetrically

at the edge of the diaphragm. After the implantation activation, the metal layer of aluminum was sputtered, patterned and sintered on the wafer to have interconnection between NWs and the bonding pads. In the last step, the diaphragm with the diameter of 200 μm was released from backside by DRIE process. The fabrication process flow is shown in Figure 4.1 and the images of fabricated NWs and released pressure sensor are shown in Figure 4.2.

Figure 4.1. Fabrication process flow of the pressure sensor with embedded SiNWs.

Figure 4.2. The images of released pressure sensor diaphragm and fabricated NWs.

SiNWs with cross-section of 90 nm x 150 nm were achieved by the combination of deep ultraviolet patterning and photoresist trimming. The next step was silicon etch process and 4 pairs of SiNWs coupled with a 200 μm diameter nitride diaphragm were successfully fabricated in this study. Figure 4.3a shows the optical image of the released pressure sensor diaphragm and Figure 4.3b shows the TEM cross-section image of SiNW.

Figure 4.3. (a) Optical image of released pressure sensor diaphragm. (b) TEM cross section view of SiNW.

4.2.1 Diaphragm buckling and sensitivity

In order to get improved and steady sensitivity of the pressure sensors, different diaphragm stacking layers were optimized. On top of the device layer, different thicknesses of oxide and nitride layers were deposited to optimize/minimize the diaphragm buckling induced after the DRIE process. After metallization, low-stress nitride with tensile stress was chosen as a passivation layer to balance the film stress within the stack and to minimize the buckling effect after the DRIE process. After the diaphragm release, the surface topography was measured and compared to quantify the deflection of the fabricated diaphragms. Table 4.1 shows the different

thicknesses of oxide and nitride material used in this study for the diaphragm deflection evaluation.

Table 4.1: Different thicknesses of oxide and nitride deposition for deflection evaluation.

Thickness of BOX layer	Thickness of Deposition layer
1 μm	5000 $\text{\AA}$ Oxide
1 μm	1.5 μm Oxide
1 μm	2.5 μm low stress oxide
1 μm	2.5 μm low stress nitride
1450 $\text{\AA}$	2.5 μm low stress nitride

Table 4.2: Comparison of deflection profile for different stacking film released diaphragm.

Thickness of BOX Layer	Thickness of Deposition Layer	Deflection profile
1 μm	5000 $\text{\AA}$ Oxide	6.1 μm , asymmetric membrane
1 μm	1.5 μm Oxide	2.5 μm , non-concentric bending
1 μm	2.5 μm low stress oxide	1.7 μm , symmetric membrane
1 μm	2.5 μm low stress nitride	0.1 μm , symmetric membrane
1450 $\text{\AA}$	2.5 μm low stress nitride	<0.1 μm , symmetric membrane

An optical interferometer (Veeco NT3300) was used to measure the diaphragm deflection after the DRIE process for different layers of film stack. Table 4.2 shows the deflection profile data for different stack material and it is shown that the diaphragm layers with 1450 $\text{\AA}$ BOX and 2.5 μm low-stress nitride have the lowest central diaphragm deflection of < 0.1 μm . In Figure 4.4, the 3D view of different deflection profiles of released diaphragm are shown.

Figure 4.4. 3D view of different deflection profiles of released diaphragm.

The electrical characterization was carried out to determine the piezoresistive sensitivity of NWs, which were embedded within different thicknesses of diaphragm. Figure 4.5 shows the schematic of experimental set-up used for the electrical characterization of pressure sensors. The electrical characterization of sensor was conducted with respect to varying pressure (0 psi to 6 psi). The DC measurements of current flow through the NW was measured by HP 4156A precision semiconductor parameter analyzer.

Figure 4.5. Schematic cross-section view of pressure sensor set-up with embedded SiNWs.

The NW pressure sensor device exhibited a linear increase in resistance under the applied pressure from 0 to 41.4 kPa (6 psi). Consequently, as shown in Figure 4.6, NWs demonstrated a linear increase in normalized resistance change ($\Delta R/R$) under the increasing pressure condition. The change in resistivity of NWs was compared for different diaphragm thicknesses. It is observed that the thin diaphragm was suitable for getting higher sensitivity. The sensitivities ($\Delta R/R$)/ ΔP of 0.0024 Pa^{-1} with $3.1 \text{ }\mu\text{m}$ diaphragm and 0.0018 Pa^{-1} with $3.9 \text{ }\mu\text{m}$ thick diaphragm have been achieved.

Figure 4.6. Normalized resistance change in NWs as a function of applied pressure. Comparison of sensitivity is shown for the relative resistance change of NWs with different thicknesses of diaphragm.

Although nanowire was used as a sensing element in the fabrication of the pressure sensor, the higher intrinsic noise was a major concern to use doped nanowires as a potential candidate for the sensing element. The device sensitivity was limited due to the intrinsic noise and it was necessary to design a better sensing element structure that can comprise higher piezoresistance as well as lower intrinsic noise to realize superior sensing performance.

4.3 Gate-all-around structure

The piezoresistive and noise response of planar MOSFETs were presented in Chapter 3. Subsequently, nanowire-based sensing element was presented in the last section and showed good piezoresistive response with sufficient linearity. However, the intrinsic noise in doped nanowires was a major concern in order to achieve better sensor resolution. As an alternate, nanowire can be used as a transistor channel and the carrier motion in nanowire could be controlled with gate bias to minimize the intrinsic noise. With the advancement in nanoscale

fabrication technology, transistors with a choice of gates, such as double-gate (DG) structure [105], tri-gate structure [106] and gate-all-around (GAA) structure [107], have been developed to improve the gate-channel controllability for better electrical characteristics. Silicon GAA nanowire MOSFETs have attracted much attention owing to their excellent electrostatics and immunity to short channel effects. The gate surrounded the channel body in the GAA structure and thus provided the best possible electrostatic control [108]. The reduction in the channel width and thickness can further increase the effectiveness of the gate control. Therefore, an ultrathin and narrow body nanowire MOSFET combined with the GAA structure is designed as a sensing element for superior strain sensing applications.

In the next section, the gate-all-around nanowire field-effect-transistor (GAA NWFET) is presented as a piezoresistive sensing element and its electromechanical properties are characterized. The gate surrounds the nanowire channel in the GAA structure, which provides easier carrier depletion with the use of low gate bias. The surrounding gate also provides complete shielding from environmental charges and prevents humidity effects to change the drain current that are independent of stress. The strain-induced change in the drain current was experimentally verified, and the gate bias effects on piezoresistance and drain current noise were analyzed.

4.3.1 Fabrication processes of gate-all-around nanowire FET

GAA n-type NWFETs were fabricated on 8-inch (100) SOI wafers with a top device layer of 117 nm and 145 nm BOX. Silicon fins of width 50 nm were defined through deep ultraviolet (DUV) patterning followed by resist trimming. These silicon fins were oxidized at 875 °C for 5 h, which results in twin nanowires (Figure 4.7a inset). After the nanowire formation, 4 nm SiO₂ was

thermally grown followed by 130 nm amorphous silicon (α -Si) by low-pressure chemical vapor deposition (LPCVD). The α -Si was further patterned and used as the gate electrode (Figure 4.7a). Next, source and drain implantation was carried out followed by activation annealing to allow the dopants to diffuse through the gate electrode and thick source and drain regions below the gate. Finally, standard metallization process completed the formation of gate-all-around nanowire FET device.

Figure 4.7. (a) SEM picture of completed GAA NWFET. 120 nm long twin Si NWs attached with source/drain (Inset image before gate formulation). (b) Schematic diagram of the four-point bending apparatus designed for the measurements.

4.3.2 Electromechanical characterization

The piezoresistive properties of NWFET were investigated using a four-point bending set-up equipped with probe station. The fabricated wafer was diced into rectangular wafer slices and the transistors channel direction was placed accordingly to generate the mechanical strain in the desired direction. A wafer slice was positioned on two bottom blades and two identical weights (W) were applied on top of the two blades to bend the chip (Figure. 4.7b). By switching the position of the top and bottom blades, either tensile or compressive strain can be generated while bending the wafer upwards or downwards. Devices (on the test chip) between the inner blades

experienced uniform and uniaxial strain after loading the weight. A strain gauge was attached on the test chip to measure the actual strain during the weight loading.

NWFETs with 120 nm channel length were tested and the dependence of the electrical characteristics on the mechanical strain is investigated using a semiconductor parameter analyzer (HP4156B). When the gate bias (V_{GS}) exceeds the threshold voltage (V_{TH}), an inversion layer forms at the Si-SiO₂ surface and the drain current (I_{DS}) flows once a voltage is applied between source and drain. The electrical characteristics were measured and NWFET devices exhibited subthreshold slopes of ~ 75 mV/dec with $V_{TH} \sim -150$ mV.

4.3.3 Influence of gate bias on piezoresistive sensitivity

Piezoresistive coefficients of the NWFET device were found by applying a sequence of controlled strains and measuring the corresponding changes in the drain current ($\Delta I_{DS}/I_{DS}$). Under the same strain, the drain current change (%) was found to be higher at the lower gate bias (Figure 4.8a). Consequently, the linear square fit slope also increases for lower gate bias, indicating a higher gauge factor ($K = (\Delta I_{DS}/I_{DS})/\epsilon$) in the subthreshold region (Figure 4.8b). The longitudinal piezoresistive coefficient (π_l) is defined as the relative change in the drain current per unit strain:

$$\pi_l = \frac{1}{E} \left(\frac{\Delta I_{DS}/I_{DS}}{\epsilon} \right) = K/E \quad (4.1)$$

where E (169 GPa) is the Young's modulus of silicon. As higher gauge factor was measured in the subthreshold region ($V_{GS} < V_{TH}$), π_l enhances up to seven times to $\sim 207 \times 10^{-11} \text{ Pa}^{-1}$ ($V_{GS} = -0.4\text{V}$) compared to $\sim 29 \times 10^{-11} \text{ Pa}^{-1}$ for the inversion region ($V_{GS} = 0.4 \text{ V}$).

(a)

(b)

Figure 4.8. (a) Drain current variations vs longitudinal strain under different biasing conditions (inversion and subthreshold region). (b) Gauge factor and minimum detectable strain (MDS) variations at different biasing conditions. MDS is minimum detectable strain of the sensor and ε is the applied strain.

Piezoresistance in silicon surface inversion layers has been interpreted to be due to the strain-induced changes in the energy-band structure and inter-valley scattering effects. The energy of conduction-band minima changes under the applied strain and carriers redistribute among the

valleys of dissimilar effective masses. The strain-enhanced electron mobility originates mainly from two factors: (1) the reduction in the average effective mass due to the carrier redistribution and (2) the change in the carrier scattering rate due to the energy-band splitting. With increasing gate voltage, the surface electric field confines the carrier motion perpendicular to the surface, which also influences electron population and scattering of electrons. A reduced gauge factor was observed at higher gate bias (Figure 4.8b) and a possible reason can be the reduction in the effective carrier mobility, which may be attributable to stronger confinement effects at high vertical electric field.

The strain may change the NWFET drain current from two aspects: such as changes in the carrier mobility and threshold voltage. For the inversion region, the drain current change dependence on the carrier mobility and threshold voltage (V_{TH}) is described as [109]

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \mu}{\mu} - 2 \frac{\Delta V_{TH}}{V_{TH}} \left(\frac{V_{TH}}{V_{GS} - V_{TH}} \right) \quad (4.2)$$

where μ represents the effective electron mobility in the channel. Figure 5.9 shows that V_{TH} reduces ~ 4 mV under the strain of $385 \mu\text{m/m}$.

Figure 4.9. I_{DS} - V_{GS} characteristics of n-NWFET for 0 and $385 \mu\text{m/m}$ uniaxial longitudinal tensile strain at $V_{DS} = 100 \text{ mV}$.

As the conduction band structure shifts under the mechanical strain, the V_{TH} reduction is attributable to the reduced band bending required to attain the inversion region. At the onset of strong inversion ($V_{GS} > V_{TH}$), the NWFET drain current becomes linearly dependent on the ($V_{GS} - V_{TH}$) and small variation in the threshold voltage (~ 4 mV) can be neglected for the drain current change. The drain current change was then considered mainly from the mobility variation and the second term in Equation (4.2) can be neglected. However, in the subthreshold region, the drain current increases exponentially ($I_{DS} \approx I_0 e^{\left(\frac{V_{GS} - V_{TH}}{mV_T}\right)}$) with ($V_{GS} - V_{TH}$), where I_0 = drain current at $V_{GS} = V_{TH}$, the thermal voltage $V_T = kT / q$ and m is the slope factor. The drain current change dependence on the threshold voltage can be described as

$$\frac{\Delta I_{DS}}{I_{DS}} = e^{\left(\frac{\Delta V_{TH}}{mV_T}\right)} - 1 \quad (4.3)$$

The calculations from Equation (4.3) indicate that the small reduction in the threshold voltage (~ 4 mV) can enhance the drain current significantly ($\sim 16\%$ for $m=1$ and $\sim 8\%$ for $m=2$) in subthreshold region.

4.3.4 Influence of gate bias on low-frequency noise

Besides the electric field dependence, the spectral noise was measured to investigate the effect of other mechanisms such as thermal and impurity scattering effects at different gate biases. Spectral noise measurements were performed using a battery-powered SR570 low-noise current preamplifier and a HP35670A dynamic signal analyzer. Figure 4.10 shows the frequency dependence of the measured drain-current noise spectral density (S_{ID}) at different gate bias. The noise power spectral density showed significant variation up to five orders of magnitude within 0.8 V gate bias span. Higher gate voltage attracts channel carriers closer to the nanowire surface

in the inversion regime, which results in carriers trapping and detrapping (number fluctuation- ΔN) at the nanowire surface. These trapped carriers generate scattering with channel carriers at the nanowire interface and influence the mobility (mobility fluctuation- $\Delta\mu$), and produce higher low-frequency noise at increasing gate bias [110]. It is shown in Figure 4.10a that S_{ID} exhibits a typical $1/f$ trend for $V_{GS} = 0.4$ V (inversion regime), but not for $V_{GS} = -0.4$ V (subthreshold regime).

Figure 4.10. (a) Drain-current noise spectral density (S_{ID}) versus frequency in the n-NWFET transistor with nanowire width ~ 10 nm and channel length = 120 nm. (b) Comparison of S_{ID} spectra versus frequency measured at $V_{DS} = 0.1$ V for gate voltage varying from 0.2 V to -0.2 V in -0.2 V steps.

In the subthreshold region ($V_{GS} < V_{TH}$), on the other hand, the surface scattering remains low due to the physical separation of carriers from the interface and ΔN has no influence on the low-frequency noise. Figure 4.10b shows that the noise power spectral noise reduces at lower gate bias (subthreshold regime), indicating that the lower drain current noise is caused only due to the $\Delta\mu$ theory [111].

To measure the performance of the strain sensor, the term ‘minimum detectable strain’ (MDS) is calculated. The MDS is the noise equivalent strain, which is defined as the drain current noise amplitude (A) divided by the strain sensitivity

$$MDS = \frac{A}{(\Delta I_{DS} / \varepsilon)} = \frac{A}{KI_{DS}} \quad (4.4)$$

From measurements of the spectral current noise at 2 Hz, I_{DS} and the gauge factor, the MDS was calculated to be $\sim 2.4 \times 10^{-6}$ for the inversion mode ($V_{GS} = 0.4V$) as shown in Figure 4.8b. However, with higher gauge factor and lower $1/f$ noise, the MDS was found to be sixteen times lower $\sim 1.5 \times 10^{-7}$ for the subthreshold mode ($V_{GS} = -0.2V$). For $V_{GS} = -0.4V$, the gauge factor is higher but the A/I_{DS} term also increases, making the MDS bigger compared with its value when $V_{GS} = -0.2$. For small strains, the signal-to-noise ratio (SNR) is defined as the sensor signal power divided by the incorporated noise power [82]

$$SNR = \frac{K^2 \varepsilon^2}{A} \quad (4.5)$$

Results suggest that both the gauge factor and the noise amplitude depend on the applied gate voltage, providing an easier way to enhance the SNR significantly by tuning small gate bias in NWFET.

4.4 Nanowire FET-embedded pressure sensor

In this section, a novel GAA NWFET-embedded pressure sensor was developed to measure the applied pressure with high signal-to-noise ratio. The detailed fabrication processes and characterization results are presented in the following sections.

Most of the pressure sensors use piezoresistive-based detection techniques because of easier fabrication, direct CMOS compatibility and good linearity. However, lower sensitivity and higher intrinsic noise cause a limitation in using piezoresistors for low-pressure measurements, especially in bio-medical applications [112]. Lower pressure detection could be achieved by

using a sensing element with higher piezoresistance, but the intrinsic noise also needs to be considered in the designing of the sensing element, as low noise is necessary to acquire better signal-to-noise ratio (SNR) of the pressure sensor. As discussed in the last section, a FET-based sensing element was investigated with improved piezoresistance compared to piezoresistors along with lower intrinsic noise. A FET-based sensing element consists of a silicon channel connected between two terminals (source and drain), and the current between these terminals was controlled by the third terminal called gate. Undoped silicon nanowire can be used as a channel material in the FET to increase the piezoresistance of the sensing element. With the use of surrounding gate, the nanowire channel can be depleted at lower gate bias and higher piezoresistance can be achieved. Furthermore, lower noise in FET-based sensing element could offer higher signal-to-noise ratio to enhance the detection limits.

As an application, a gate-all-around (GAA) NWFET-embedded pressure sensor is proposed in order to get superior pressure sensitivity and higher SNR. Ultrathin and undoped silicon nanowire was considered as the channel to take advantage of higher piezoresistivity. A NWFET was fabricated with gate-all-around structure, in which the gate surrounds the nanowire to get easier carriers depletion inside the nanowire channel by using low gate bias. The results enabled additional understanding of more effective and miniaturized designs of mechanical to electrical transducers. The optimum gate bias for the NWFET, values of the pressure sensitivity and the signal-to-noise ratio were determined by maximizing the sensitivity of the pressure sensor.

4.4.1 Pressure sensor fabrication

A NWFET-embedded diaphragm-based pressure sensor was fabricated on a 8-inch (100) SOI wafer with a 1170 nm silicon top layer and a 1 μm BOX. The starting silicon film was p-type ($N_A=2\times 10^{15}/\text{cm}^3$). The fabrication process flow of the NWFET is shown in Figure 4.11.

Figure 4.11. The fabrication process flow of NWFET. (a) 3-D view of the fin, source and drain structures. (b) Cross-section after the fin oxidation. (c) Wet etching to remove the oxide. (d) Cross-section after poly-Si gate deposition.

Silicon fins of width 60 nm to 90 nm were patterned by deep ultraviolet lithography and ultrathin silicon fins (~40 nm) were achieved by resist trimming followed by DRIE (Figure 4.11a). Twin silicon nanowires were formed after the oxidation of ultrathin silicon fins in dry O_2 for 5 hrs at 875 °C (Figure 4.11b). The formation of twin nanowires was caused by stress-limited oxidation [113], and the position of the nanowires was one on the top and the other at the bottom of the silicon fin. The complete oxidation of nanowires was prevented because of the stress generated during the oxidation process. Wet oxide etching was used to remove the grown oxide on the silicon and twin nanowires are shown in Figure 4.11c. Next, 4 nm SiO_2 was thermally grown to serve as gate oxide followed by 130 nm amorphous silicon in LPCVD. Amorphous silicon was further patterned by lithography and etched to use as gate electrode (Figure 4.11d). Next, source

and drain implantation was carried out followed by activation annealing at 950 °C for 15 minutes to allow dopants to diffuse through the gate electrode and thick source and drain regions below the gate. Finally, standard metallization process completed the formation of the GAA NWFET device.

The fabricated NWFETs have channel lengths ranging from 100 to 350 nm. When the NWFET channel length was less than 150 nm, the gate patterning step, which involves lithography followed by the photoresist trimming process, was marginal and almost 50% NWFETs were not successfully fabricated because of the limitation in gate patterning. Next, for the NWFETs with channel length > 250 nm, almost 30% nanowires were broken during the oxidation process. However, for NWFETs with channel length from 200 nm to 250 nm, the NWFET fabrication was finished with high yield (> 90%).

As demonstrated in the earlier sections (Table 4.2), low-stress nitride layer was deposited onto the diaphragm to obtain minimum pre-bending. Thus, a 2.5 μm low-stress nitride was deposited after the NWFET fabrication and patterned to open the contacts. A DRIE was then performed on the backside of the wafer in order to release the silicon nitride/silicon oxide diaphragm.

Figure 4.12. (a) SEM image showing NWFET-embedded pressure sensor (b) A pair of silicon NWs before gate formation. NW length is 200 nm and diameter is ~10 nm.

Figure 4.12a shows a SEM image of a NWFET sensing element integrated into a diaphragm-type

pressure sensor. The diaphragm consisted of circular double-layer made of $\text{Si}_3\text{N}_4/\text{SiO}_2$ ($2.5 \mu\text{m}/1 \mu\text{m}$) with a radius of $110 \mu\text{m}$. The low-stress nitride deposition provided a flat diaphragm surface (centre deflection $<100 \text{ nm}$) after the releasing process.

The design of the pressure sensor is presented as the integration of NWFET with the mechanical components such as a diaphragm. This approach offers advantages to apply high pressure in integrating NWFET on a thin diaphragm. A differential pressure applied across the membrane leads to a deflection of the diaphragm, which induces stress (σ) or strain (ε) on the diaphragm and then in the integrated NWFET. The NWFET was positioned near the diaphragm edge to experience maximum stress during the pressure application. By measuring the NWFET distance from the diaphragm edge, it is possible to determine the theoretical dependency of the applied pressure on the transistor drain current. The diaphragm deformation and the corresponding stress distribution were calculated as a function of the applied pressure (P_A). The longitudinal (σ_l) and transverse stress (σ_t) on a circular diaphragm are given by

$$\sigma_l = \frac{3}{8} \left(\frac{P_A}{t^2} \right) [a^2(1+\nu) - r^2(3+\nu)] \quad (4.6)$$

$$\sigma_t = \frac{3}{8} \left(\frac{P_A}{t^2} \right) [a^2(1+\nu) - r^2(1+3\nu)] \quad (4.7)$$

where a is the radius of the diaphragm, r is the radial distance from the center of the diaphragm, t is the thickness of the diaphragm, and ν is the Poisson's ratio.

Bogdan et al. [114] presented results concerning that the maximum stress is obtained at a particular distance ($\sim 35 \mu\text{m}$) from the diaphragm edge (diaphragm diameter = $350 \mu\text{m}$). The less variation of stress value ($\sim 5\%$) around the $30 \mu\text{m}$ maximal stress position gives an additional misalignment tolerance for the sensing element positioning at high stress locations. The resulting

relative drain current variation in the integrated NWFET as a function of the in-plane biaxial mechanical stress can be expressed as

$$\frac{\Delta I_{DS}^{sat}}{I_{DS}^{sat}} = \pi_l \sigma_l + \pi_t \sigma_t \quad (4.8)$$

where π_l and π_t are the longitudinal and transversal piezoresistive coefficients, respectively.

The σ_l and σ_t are the longitudinal and transversal components of the mechanical stress in the diaphragm, relative to the current flow direction in the NWFET channel, respectively.

4.4.2 Tunable pressure sensitivity and signal-to-noise ratio

The fabricated NWFET-embedded pressure sensor was characterized using the pressure sensor measurement system as shown in Figure 4.13. The pressure on the diaphragm was applied by the air flow nozzle of the equipment.

Figure 4.13. Schematics of the pressure sensor with embedded GAA NWFET, showing the testing setup for its characterization.

The applied pressure induces stress at the diaphragm surface and changes the drain current of the integrated NWFET. First, I_{DS} - V_{DS} characteristics of the embedded NWFET were measured at different gate bias (V_{GS}) using a semiconductor parameter analyzer HP4156B. The device

showed good electrostatic control with ON/OFF ratio of six orders of magnitude, low subthreshold slope of ~ 80 mV/dec and threshold voltage ' V_{TH} ' ~ -0.15 V. The gate bias controls the carrier concentration and their position inside the nanowire channel, i.e. carriers accumulation near the nanowire surface in the inversion mode ($V_{GS} > V_{TH}$) and carrier depletion from the nanowire surface in the subthreshold mode ($V_{GS} < V_{TH}$). The current-voltage (I_{DS} - V_{DS}) characteristics of the NWFET were measured with and without applied pressure under different gate bias (Figure 4.14). The change in the drain current was recorded at 6 psi (310.3 mmHg) pressure increment steps.

Figure 4.14. I_{DS} - V_{DS} characteristics for NWFET before and after applied pressure at varying gate bias regimes (Inversion to sub-threshold).

Figure 4.15 shows the results concerning the relative variation of the drain current as a function of the applied pressure for a NWFET. From 0 to 30 psi (1550 mmHg) applied pressure, the NWFET device exhibited an increase in the normalized current change ($\Delta I_{DS}^{sat} / I_{DS}^{sat}$). The gauge

factor of the NWFET was found by applying a sequence of controlled pressure to the NWFET and measuring the corresponding changes in the drain current.

For the same pressure, the normalized current change (%) was found to be higher at lower gate bias. Figure 4.15 shows the device sensitivity extracted from the differentiation of $(\Delta I_{DS}^{sat} / I_{DS}^{sat})$ as a function of P_A , with V_{GS} as a parameter. It is shown that the linear square fit slope increased for lower gate bias, indicating a higher gauge factor $(\Delta I_{DS}^{sat} / I_{DS}^{sat}) / \epsilon$ in the subthreshold regime. At $V_{GS} = -0.2$ V (subthreshold regime), the measurement results revealed a four-times gauge factor increase compared to $V_{GS} = 0.2$ V (inversion region). The measurement was repeated several times (> 10 times) on a single device and the absolute drain current variation was found to be unchanged ($< \pm 0.1\%$) under the same pressure. Additionally, measurements were repeated on several devices (~ 10 devices) to ensure the repeatability of the results. The relative drain current change (%) was found to be similar (variation $< \pm 0.2\%$) under the same applied pressure.

Figure 4.15. Relative drain current change variations versus applied pressure under different biasing conditions (inversion and subthreshold region).

In piezoresistive NWFET, the gauge factor is attributed to small changes in the electronic band gap of the silicon channel under mechanical stress. The carrier's energies in the NWFET channel are quantized into energy sub-bands and the carrier concentration is controlled by the gate bias. The carrier sub-band energy levels modify under the applied mechanical stress/strain, and change the mobility or the drain current of the NWFET. The mechanical stress has an effect on the NWFET drain current from two aspects: such as changes in the carrier mobility or threshold voltage. The variation of the threshold voltage under strain was determined by measuring the intercept of the linear region in the I_{DS} - V_{GS} characteristics. The observed threshold voltage reduced ~ 3 mV under the pressure of 30 psi (1500 mmHg). At the onset of strong inversion ($V_{GS} > V_{TH}$), the NWFET drain current becomes linearly dependent on the $(V_{GS} - V_{TH})$. Thus, the little variation in the threshold voltage (~ 3 mV) can be neglected for the drain current change in the inversion region. The drain current change was then considered mainly from the mobility variation and the contribution from the threshold voltage is neglected. However, the inversion layer charge density and drain current increase exponentially with $(V_{GS} - V_{TH})$ in the subthreshold regime ($V_{GS} < V_{TH}$). For that reason, small reduction in the threshold voltage can significantly enhance the drain current and the contribution of threshold voltage change dominates for providing higher normalized current change in the subthreshold regime.

Next, the drain current noise was measured to observe the biasing effects in analyzing the signal-to-noise ratio of the NWFET pressure sensor. Low-frequency noise measurements were performed using low-noise current preamplifier and dynamic signal analyzer. Figure 4.16 shows the frequency dependence of the measured drain current noise at different operating regimes (subthreshold to inversion) for the NWFET. It was observed that the drain current noise amplitude shows up to two orders of magnitude change within a change of 0.4 V gate bias. Also,

the drain current noise shows the $1/f$ trend for the inversion regime ($V_{GS} > V_{TH}$), but no $1/f$ dependence at the subthreshold regime ($V_{GS} < V_{TH}$). In particular, the drain current noise of 1 pA/ $\sqrt{\text{Hz}}$ at $V_{GS} = -0.2$ V was significantly lower than the reported noise values for piezoresistors and MOSFETs [115, 24].

Figure 4.16. Comparison of drain current noise spectrum versus frequency measured at $V_{DS} = 0.1$ V for gate voltage varying from 0.2 V to -0.2 V.

The low-frequency noise behavior in the NWFET is explained by two main mechanisms. First, the number fluctuation (ΔN) theory suggests that the drain current noise is originated due to fluctuations in the number of carriers in the conduction channel (N), which is caused by trapping and detrapping at the silicon-insulator surface. Second, the mobility fluctuation ($\Delta \mu$) theory assumes that the drain current noise arises due to fluctuations in the carrier mobility originated due to Coulomb or surface scattering events. The scattering mechanism depends mainly on the vertical electric field and the concentration of the inversion charge in the channel, which generates the mobility fluctuation. In actual fact, both phenomenons contribute as low-frequency noise source; however, one of these could dominate depending on the type of device structure and operating gate bias conditions. The ΔN theory presents a noise spectral density that is

independent of the gate voltage while the $\Delta\mu$ theory postulates gate bias dependence with higher noise at higher gate bias.

In the NWFET, increasing gate voltage generates the inversion carriers and attracts them closer to the nanowire surface. Thus, carriers scattering events rapidly increase in frequency with the gate voltage, thereby increasing the mobility fluctuation and then low-frequency noise at higher gate bias. In strong inversion ($V_{GS} > V_{TH}$), the mobility fluctuation ($\Delta\mu$) takes over as the dominant $1/f$ mechanism. However, in the subthreshold regime ($V_{GS} < V_{TH}$), the carriers position is relatively far from the surface of nanowire and therefore the surface scattering is reduced due to the reduced vertical electric field. As the GAA gate architecture surrounds the channel body, it was extremely suitable for depleting the carriers from the nanowire interface and thus the drain current noise is found to be extremely low in the subthreshold regime. It facilitates least scattering events as well as trapping/detrapping at the nanowire interface. Thus, the low-frequency noise in subthreshold regime is dominated by the $\Delta\mu$ theory, which is due to the lattice scattering inside the depleted regions, and shows no $1/f$ dependence.

It was observed in the results that the NWFET gauge factor and the drain current noise change with the applied gate voltage (V_{GS}). Based on these two parameters, a performance factor was described as the SNR that incorporates both the gauge factor (GF) and the drain current noise (I_N). Results suggest that the SNR depends strongly on V_{GS} , setting the aim of finding V_{GS} that maximizing the SNR. The SNR was generally defined as the ratio of signal power to the noise power affecting the signal. The noise power in a NWFET was determined by integrating the current noise over the measurement bandwidth. Thus, the SNR is defined as [82]

$$SNR = \frac{(GF)^2}{I_N} \frac{1}{\ln f_2/f_1} \varepsilon^2 \approx \frac{(GF)^2}{I_N} \varepsilon^2 \quad (4.9)$$

where f_1 and f_2 are corner frequencies and $\ln f_2/f_1$ is considered to be 1 for the sake of certainty. The GF was calculated from Figure 4.15 and its values increase when the gate bias is reduced. The $GF \sim 57$ was observed to be similar to bulk silicon in the inversion regime ($V_{GS}=0.2$ V). But, when the gate bias was reduced to the subthreshold regime, the GF increased and a maximum $GF \sim 250$ was obtained at $V_{GS} = -0.2$ V. Figure 4.17a shows the enhancement of the GF and reduction in I_N at lower V_{GS} .

Figure 4.17. (a) Gauge factor and drain current noise variation at different biasing condition. (b) Pressure sensitivity and signal-to-noise ratio variation at different biasing condition.

The pressure sensitivity ($(\Delta I_{DS}^{sat}/I_{DS}^{sat})/P_A$) and SNR (calculated from Equation 5.9) values from individually measured GF and I_N were plotted against V_{GS} in Figure 4.17b. It was confirmed that the SNR increases significantly with a reduction of V_{GS} . This is because of the NWFET gauge factor enhancement and low-frequency noise reduction with V_{GS} , increasing the overall SNR .

Results suggested that both the gauge factor and the noise amplitude depend on the applied gate voltage, providing an easier way to enhance the SNR significantly by tuning the small gate bias in the GAA NWFET. The SNR was recently reported for carbon nanotubes field effect transistors (CNFETs) and it was found that both the GF and I_N varied independently with the gate bias. Fortunately, in the NWFET, the piezoresistive sensitivity increased at lower gate bias whereas the noise amplitude was found to be minimum. Compared to the recently reported CNFET ($SNR_{max}=10^2$), lower noise amplitude in the NWFET offered higher SNR ($SNR_{max}=10^9$) at low voltages and can be incorporated in application-specific integrated circuits. Results showed that the optimization of the GAA NWFET sensing element and operating bias conditions can provide significant enhancements in the pressure sensitivity and signal-to-noise ratio for the NWFET-embedded pressure sensors.

4.5 Conclusion

Since the report from He & Yang [17], researchers investigated the giant piezoresistance of nanowires. The reported gauge factor values were as high as 6674 for $\langle 111 \rangle$ silicon. Neuzil et al. used the biasing effect to pinch-off the current channel and reported maximum gauge factor of 5400 [20]. Recently, Milne et al. [21] revealed no large gauge factor in nanowires and the previous reported values are most likely due to dielectric surface relaxation effect independent of

applied stress. In our work, using nanowire and gate-controlled nanowire FETs as sensing elements, no giant piezoresistance is measured in nanowires with dimensions as low as 10 nm widths. However, ‘tuning’ effect of piezoresistance and drain current noise is measured and verified for the first time. Because of the low noise, the MDS of the sensor remains as an attractive choice for physical sensors.

In the latter section, the biasing effect has been investigated on the pressure sensitivity of the NWFET-embedded pressure sensor. The NWFET-based sensing element was presented with higher gauge factor and lower noise, and miniaturized size compared to other sensing elements. The NWFET device has been optimized with respect to noise and sensitivity, and the current change to pressure improved by a factor of four within a 0.4 V gate bias span. A figure of merit in terms of signal-to-noise ratio has been calculated to compare the performance of the pressure sensor. The dependence of the *SNR* on the gate bias was significant and the maximum *SNR* is found at $V_{GS} = -0.2$ V (subthreshold regime). Results suggest operating the NWFET sensing element in the subthreshold regime to maximize the sensor resolution and low voltage operation provides promising applications for miniaturized low power pressure sensors. This would allow further optimization of the channel geometry and doping effects to further improve the sensitivity and then pressure resolution.

Chapter 5

Minimum detectable strain improvement in junctionless nanowire FET

This chapter demonstrates a novel piezoresistive sensing element based on junctionless nanowire field-effect transistor (JL-NWFET). The proposed sensing element utilizes the piezoresistive properties of doped single crystal silicon. The effects of various channel doping are investigated on the piezoresistance, threshold voltage and low-frequency noise (LFN). Significant enhancement in the piezoresistance is observed when the channel doping concentration is varied from $6.7 \times 10^{19} \text{ cm}^{-3}$ to $6.7 \times 10^{18} \text{ cm}^{-3}$. The JL-NWFET operates by bulk conduction in the on-state compared to surface conduction in the inversion mode NWFET, and shows significantly lower spectral noise than the NWFET counterpart. The LFN is found to be nearly insensitive to gate bias voltage (full depletion to no depletion), doping levels, and operating frequency. Channel doping offers wide tunability of the threshold voltage without any influence on the LFN. The superior LFN behavior in the GAA JL-NWFET is attributed to the conduction of carriers inside the uniformly-doped nanowire channel. The picoampere drain current noise helps to achieve a superior resolution (minimum detectable strain) and formulate the JL-NWFET as an ultrasensitive sensing element for nanoelectromechanical sensors.

5.1 Introduction

The mechanical strain is extensively used to increase the carrier mobility in the channel of silicon MOSFETs and used to measure various physical quantities [116]. The technique has been used to investigate the piezoresistive response to bulk MOSFETs in Chapter 3 and NWFETs in

Chapter 4. The results established the significance of strain engineering to enhance the piezoresistive performance by changing the architecture and size of MOS devices. For the better piezoresistive sensor, the main requirements were higher gauge factor and lower noise. Piezoresistive response explored in transistor devices, such as nanowires field effect transistors or carbon-nanotubes field effect transistors achieved superior piezoresistance with substantial signal-to-noise ratio [82, 117]. However, the major disadvantage of these transistors was the drain current noise dependence on gate bias and temperature, which degrades the resolution needed for low-strain measurements. The important parameters to evaluate the strain sensor performance are their minimum detectable strain (MDS) and signal-to-noise ratio (SNR) that incorporates both piezoresistance and drain current noise. In Chapter 3, a transistor-based sensing element was demonstrated and the sensitivity was found to be better than conventional piezoresistors. To further improve the detection limits of transistor-based sensing elements, nanowire channel transistors have been investigated in Chapter 4 and superior piezoresistance and lower noise were obtained when the transistor operated in the subthreshold region. However, the drain current magnitude was small in the subthreshold region, which limits the resolution (MDS) of the transistor. It is established that the transistor architectures and smaller channel dimension in NWFETs were responsible on their ability to provide better piezoresistive enhancement comparable to strained-Si planar MOSFETs.

5.2 Junctionless transistor devices

Instead of using undoped silicon channel, a heavily-doped nanowire channel will expand the scope to optimize the piezoresistance and noise for better sensing applications. However, by reducing the transistor dimensions, the doping concentration gradient control becomes

challenging when the distance between the junctions drops below 10 nm. These junctions represent an increasingly difficult fabrication challenge for the semiconductor industry and also degrade the transistor performance. Recently, a new kind of transistor was demonstrated in which there was no junction and no doping concentration gradient [118]. In the JL-NWFET, the channel doping was the same as that of source/drain, which can overcome the challenges of forming junction and minimize the junction-based performance degradation issues. As an alternative to conventional inversion mode transistors, junctionless transistor devices showed full CMOS functionality and were made using silicon fins. Additional advantages were high ON/OFF drain current ratio, near-ideal subthreshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage than conventional transistors [119, 120]. In these devices, the channel doping concentration was high with typical values ranging around 10^{19} atoms/cm³. The absence of doping concentration gradients greatly simplified fabrication and relaxed thermal budget requirement, especially in nano-scale channel devices. Since the channel of junctionless transistors is heavily-doped, the obvious question arises, is strain-induced mobility enhancement techniques can be effectively used in these devices? The aim of the chapter is to experimentally analyze the impact of the mechanical strain on piezoresistance, drain current noise and drive current for n-type junctionless Si nanowire MOSFETs.

Since the channel of the junctionless transistor is doped silicon, it was desirable to explore the channel doping impacts on various parameters, especially important for sensor applications. In terms of piezoresistance, it was reported that lightly-doped silicon outperformed in terms of higher gauge factor [121]. But, higher gauge factor alone cannot be sufficient for sensors operating close to their detection limit, as the drain current noise also becomes extremely important. Results in Chapter 4 confirmed that piezoresistance and the drain current noise in

transistors strongly depend on the applied gate bias (V_{GS}). These two factors suggest that the SNR and MDS also depend on V_{GS} , providing a way to enhance the sensor performance by electric biasing. The impact of channel doping and gate bias on piezoresistive sensing in the JL-NWFET is not reported so far to our knowledge, thus motivating a complete SNR and MDS study.

In subsequent sections of this chapter, JL-NWFET was investigated as strain gauges, which were fabricated and tested to validate their performance as an electrical signal platform for strain sensing. The GAA architecture was used to fabricate the JL-NWFET, in which the gate surrounds the channel body. The GAA structure is extremely suitable for fabricating junctionless devices as the gate will create/remove depletion from all sides to turn off/on the device. The full carrier depletion is possible even in highly-doped nanowire. Thus, the strain gauge consists of pre-doped nanowire channel encapsulated by the surrounding gate structure. Results are presented for piezoresistive measurements on gate-all-around junctionless nanowire field-effect transistor (GAA JL-NWFET) with four different doping levels. The electromechanical properties of the JL-NWFET are characterized and the strain-induced change in the drain current is experimentally measured. Results are presented for the channel doping impacts on the piezoresistance, threshold voltage and low-frequency noise (LFN). Results provide further insights into the role of channel doping and gate bias on the electromechanical performance of JL-NWFET.

5.2.1 Fabrication processes of junctionless nanowire FET

JL-NWFETs were fabricated on 8-inch p-type (100) SOI wafers with a top device layer of 117 nm and 145 nm BOX. The top silicon layer was doped with arsenic (As) using ion implantation to make it n-type. The implant doses were chosen to yield uniform silicon doping concentrations

ranging from 1.3×10^{18} to 6.7×10^{19} atoms cm^{-3} in four different quadrants of the wafer. Silicon fins of width 60 nm ($\pm 10\%$) were defined through deep ultraviolet (DUV) patterning, dry etch and then oxidized at 875 °C for 5 h, which results in twin nanowires of diameter ~ 15 nm (variability up to ± 3 nm), shown schematically in Figure 5.1(a). After the nanowire formation, 4 nm SiO_2 was thermally grown (reducing nanowire diameter to ~ 10 nm), followed by 130 nm amorphous silicon ($\alpha\text{-Si}$) by low pressure CVD and BF_3 doping at a dose of $1 \times 10^{16} \text{ cm}^{-2}$. Gate electrodes were then patterned and standard metallization process completed the fabrication of the JL-NWFET. Figure 5.1(b) shows the tilted view SEM image of the JL-NWFET after the gate definition. Inversion mode GAA NWFETs were fabricated on separate wafers with the process flow described previously in chapter 4.

Figure 5.1. (a) Schematic view of the n-type JLNWFET. Nanowire channels have same doping type and concentration as source/drain. (b) Tilted view SEM image of GAA JL-NWFET after the gate patterning.

5.2.2 Electrical characterization results and discussion

JL-NWFETs with 160 nm channel length were tested and the dependence of the electrical characteristics on the mechanical strain was investigated using a semiconductor parameter

analyzer (HP4156B). The surrounding gate was extremely suitable to create/remove depletion from all sides to turn off/on the transistor and provided a possibility to achieve the full carrier depletion even in highly-doped nanowire channel. JL-NWFETs operated by bulk conduction in the on-state compared to surface conduction in the inversion mode NWFETs counterpart.

Figure 5.2. I_{DS} - V_{DS} characteristics of JL-NWFET devices with different channel doping concentrations at varying gate bias (Subthreshold to on-state accumulation region).

Figures 5.2(a-d) show the I_{DS} - V_{DS} characteristics of JL-NWFET devices fabricated with different channel doping concentration. The device exhibits high on/off ratio of eight orders of magnitude with low subthreshold slope of $\sim 65 \text{ mV/dec}$. Four JL-NWFET devices fabricated with doping

concentration of 1.3×10^{18} , 6.7×10^{18} , 1.3×10^{19} and 6.7×10^{19} atoms cm^{-3} , are named as A, B, C and D, respectively. All devices were characterized to study the impacts of doping on the piezoresistance, threshold voltage (V_{TH}) and drain current noise. Figure 5.3 presents the variation of the threshold voltage of JL-NWFET devices as a function of nanowire doping at $V_{DS} = 0.1$ V. Five devices for each doping were measured and the fluctuations in V_{TH} are represented by a vertical bar in the graph for each doping. As expected, the threshold voltage has decreased linearly with increase in doping concentration. It is worth mentioning here that the actual doping concentrations inside the nanowires may be slightly different from the fin as a result of the segregation effect during oxidation of the ultrathin fin.

Figure 5.3. Threshold voltage of JL-NWFET as a function of fin doping concentration at $V_{DS} = 0.1$ V.

Because of the n-type doping in the substrate, the high work function gate material was used to operate the doped channel device like an enhancement type transistor. Higher doping in the gate material adjusted the V_{TH} value of the transistor even when doping was very high in the substrate. Thus it made it possible to turn off the transistor without any application of the gate bias. It is also to be noted that the fabrication of the junctionless device allows the usage of a gate-last

process, which facilitates the use of a metal gate. In the last chapter, a midgap gate material was used for the classical inversion-mode (IM) nanowire transistor when the V_{TH} adjustment was not needed.

5.2.3 High-temperature performance of junctionless nanowire FETs

Figures 5.4 (a-d) show the measured drain current as a function of the drain voltage at different temperatures for JL-NWFET transistors. The nanowire diameter in all devices was 10 nm.

Figure 5.4. Measured I_{DS} – V_{DS} characteristics with various temperatures of JL-NWFET ($L = 160$ nm, and $d \sim 10$ nm).

It was observed that the junctionless transistor drain current increased at higher temperature, which was opposite to the conventional transistors. Also, the enhancement in the drain current was found to be maximum for the lower doping devices. As the channel doping increased, the relative enhancement of the drain current with temperature was found to be minimum. Furthermore, Figures 5.5(a-d) show the measured drain current as a function of the gate voltage at different temperatures for JL-NWFET transistors.

Figure 5.5. Measured I_D – V_{GS} characteristics with various temperatures of JL-NWFET ($V_{DS} = \pm 1.0$ V, $L = 160$ nm, and $d \sim 10$ nm).

The threshold voltage was measured for different doping devices as a function of temperature at $V_{DS} = 0.1$ V. It was observed that the threshold voltage decreased and the subthreshold slope

increased in all devices as temperature was increased. The use of the GAA NWFET further reduced the temperature dependence of the threshold voltage when narrow silicon nanowires were used due to the reduction in the surface potential variation with the temperature [122]. It was reported for the conventional MOSFET that the reduction of the threshold voltage with temperature tends to increase the drain current, while the decrease of mobility due to increasing phonon scattering with temperature tends to decrease it [123, 124]. There exists a particular gate bias at which these effects balance one another, called the “zero temperature coefficient” (ZTC) point. The ZTC point was reported at $V_{GS} = 1$ V for inversion mode n-channel devices [125]. However, in junctionless transistors, the reduction of mobility with temperature was observed much lower than in other types of transistors. As a result, the current increases in a monotonous manner, and there was no ZTC point observed for the JL GAA NWFET.

5.3 Piezoresistive characterization of junctionless NWFET

A four-point-bending technique was used to apply an external mechanical strain and the piezoresistive properties of the JL-NWFET were investigated using four-point bending set-up equipped with probe station (Figure 5.6). The similar set-up was used in Chapter 4 for the piezoresistive measurements on NWFETs. The interest of this method was to apply a uniform uniaxial strain between the two central fulcrums if the configuration shown in Figure 5.6(a) is referred. The fabricated wafer was diced into rectangular wafer slices and JL-NWFET transistors channel direction was placed accordingly to generate the mechanical strain in the desired direction. A wafer slice was placed between two blades, and two identical weights (W) are applied on both ends to bend the chip. The transistor devices were defined on a (0 0 1) silicon wafer and the mechanical strain was applied along $\langle 110 \rangle$ silicon direction. With the shown four-

point bending setup, both uniaxial tensile or compressive strain can be generated while bending the wafer upwards or downwards. Devices (on the test chip) between the inner blades experienced uniform and uniaxial strain after loading the weight. The induced surface strain is a function of the distance between the inner blades (d) and applied weight (W)/force (F) on the upper blades [126].

Figure 5.6. Schematic diagrams of the four-point bending apparatus designed for measurements: (a) Force applied at the two ends generates tensile stress on the silicon wafer. (b) The fabricated JL-NWFET on the test chip experience the tensile strain when weight (W) is applied on the two ends.

The attached strain gauge on the wafer slice was used to measure the actual strain during the weight loading. The strain value was calculated and compared with the recorded data from the strain gauge. The difference in the values was within $\pm 3\%$ and data obtained from the strain gauge were used in the experimental results.

5.3.1 Influence of doping and gate bias on piezoresistive sensitivity

The tensile strain was applied parallel to the drain current flow in $\langle 110 \rangle$ crystalline direction. The change in the drain current was measured for each device for a gate voltage ranging from on-state to the subthreshold mode of operation. The transistor piezoresistive sensitivities were

obtained by measuring the drain current change as a function of the applied strain. The gauge factor of the devices was found by applying a sequence of controlled strains to the JL-NWFET and measuring the corresponding changes in the drain current ($\Delta I_{DS}/I_{DS}$). The variation in the drain current, $\Delta I_{DS}/I_{DS}$, as a function of tensile strain is plotted for all devices in Figures 5.7(a-c). The slopes of the curves provided the piezoresistive sensitivities in the different doping devices. As expected, the piezoresistance of the devices decreased when the doping concentration was increased. It was also observed under the same strain that the drain current change (%) is higher at lower gate bias for all devices. At least five devices for each doping were measured. The small characteristic fluctuation between devices was found. This fluctuation was pretty low ($\sim \pm 4\%$), especially for higher doping channel devices. However, device A showed higher non-uniformity ($\sim \pm 10\%$) during piezoresistive measurements in different devices. The origin of this non-uniformity might be related to the variability between the doping in a nanoscale channel. Piezoresistive measurements were compared among the devices B, C and D to optimize the effect of channel doping and gate bias on the gauge factor.

Consequently, it is observed that the linear square fit slope increases for lower gate bias, which indicates a higher gauge factor ($G_F = (\Delta I_{DS}/I_{DS})/\epsilon$) in the subthreshold regime (Figure 5.8).

Figure 5.7. (a) Drain current variations vs longitudinal strain for the different channel doping JL-NWFETs under different biasing conditions (inversion and subthreshold region).

The reduction of the gauge factor was observed for higher channel doping and it confirmed the piezoresistive behavior of junctionless devices similar to the doped piezoresistors. Similar to the inversion mode NWFET in the last chapter, the higher gauge factor was measured in the subthreshold regime ($V_{GS} < V_{TH}$) for the junctionless NWFET. In particular, the gauge factor was enhanced in the subthreshold region by four times for device B and two times for device D compared to the inversion region ($V_{GS} > V_{TH}$). The enhancement of the gauge factor in the subthreshold voltage was found to be minimum in the highest doping transistors due to the difficulty in carrier confinement by the gate bias.

Figure 5.8. Gauge factor variations for the different channel doping JL-NWFETs at different biasing condition (on-state to subthreshold region).

The enhancement of the gauge factor can be explained to be due to the effect of the carrier confinement in the energy bands. The carrier energies in the JL-NWFET channel are quantized into energy sub-bands and carrier population is controlled by the gate bias. The carrier sub-band energy levels shift under the applied mechanical strain, leading to the mobility or drain current change of JL-NWFET. The shifting of energy levels is strongly dependent on the channel doping. The energy levels are less discrete for the highly-doped channel and it is difficult to shift these energy levels by the application of the mechanical strain. The strain may affect the drain current from three aspects: such as change in mobility, threshold voltage or dimension. The dimensional changes are considered to be negligible due to silicon's high modulus of elasticity. The relation between the drain current change dependence on the carrier mobility change and the threshold voltage is described in the last chapter. The same relation will be applied in the junctionless devices and the drain current change in the on-state is mainly due to the mobility change. The variation of the threshold voltage under strain was measured for device B by measuring the intercept of the linear region in the I_{DS} - V_{GS} characteristics. The results demonstrate that the threshold voltage reduces ~ 3 mV under the strain of $360 \mu\text{m}/\text{m}$. At the start of on-state conduction ($V_{GS} > V_{TH}$), the NWFET drain current becomes linearly dependent on $(V_{GS} - V_{TH})$. Under the applied strain, small variation in the threshold voltage (~ 3 mV) can be neglected for the drain current change in the inversion region. The drain current change is then considered mainly from the mobility variation. As explained in the last chapter, the charge density and drain current increase exponentially with $(V_{GS} - V_{TH})$ in the subthreshold regime. Small reduction in the threshold voltage can significantly change the drain current and higher gauge factor was obtained in the subthreshold regime.

Also for JL-NWFET device, higher GF near subthreshold regime is attributed due to the variation of effective channel width. The JL-NWFET devices have a thin n-type channel surrounded with depletion regions (created by p++ gate doping) at the Si-SiO₂ interface. The depletion region width depends on the doping profile and increase in nanowire doping concentration results in reduced depletion region width. When gate bias reduces, the width of the depletion region increases from all sides of nanowire and cross-section area of the channel reduces. As higher piezoresistivity was reported for the decreasing nanowire diameter, the reason of GF enhancement in subthreshold regime is due to the reduction of effective channel width. As shown in Figure 5.8, compared to the inversion-region ($V_{GS} = V_{th} + 0.2V$), the GF is enhanced four times for device B and two times for device D in the subthreshold-region ($V_{GS} = V_{th} - 0.2V$). The results supports that the GF enhancement rate depends on the depletion width variation and thus higher enhancement rate is obtained for the lower doping channel (device B). Under the similar gate bias, as depletion width variation is less for the highly doped regions, the high GF enhancement in device B can be explained due to the larger channel width variation compared to the higher doping device C and D.

5.3.2 Influence of doping and gate bias on intrinsic noise

Besides the gate bias dependence on the gauge factor, the drain current noise was measured to investigate the effect of other sources such as thermal and impurity scattering effects at different gate biases. As described in the last chapter, drain current spectral noise measurements were performed using a battery-powered SR570 low-noise current preamplifier and a HP35670A dynamic signal analyzer. For all devices with different channel doping, Figures 5.9(a-d) show

the frequency dependence of the measured drain-current noise spectral density (S_{ID}) at different gate bias.

Figure 5.9. (a) Drain-current noise spectral density (S_{ID}) versus frequency in the different channel doping JL-NWFET transistors with nanowire width ~ 10 nm and channel length = 160 nm. (b) Comparison of S_{ID} spectra versus frequency measured at $V_{DS} = 0.1$ V for gate voltage varying from on-state to subthreshold regime.

It is shown in Figure 5.9 that the S_{ID} exhibits a less $1/f$ trend not only for on-state but also in the subthreshold region. The observed drain current noise was significantly lower compared to the noise reported for piezoresistors and inversion-mode transistors. Also, the noise power spectral density shows very less difference with respect to the variation in the gate bias and channel

doping. The DC characteristics were measured before and after noise measurements to confirm that devices were biased properly during the noise measurement. To confirm the results further, same probe station is used to measure the noise and DC characteristics. For DC measurements, the bias voltages were supplied from the semiconductor parameter analyzer. For noise measurements, bias voltages (V_{GS} , V_{DS}) were obtained from the voltage supply in battery-powered SR570 low-noise current preamplifier. Some changes, though really small, in LFN with frequency and gate voltage confirm that devices were biased. In the last chapter, the same biasing set-up was used in the NWFET noise measurements, which showed more clear changes in the noise spectrum with gate bias and confirm that biasing was accurate. Compared to the inversion mode transistor, lower fluctuation in the drain current noise provides various advantages to use the junctionless transistor for various sensing applications.

Figure 5.10. Signal-to-noise (SNR) ratio variations for the different channel doping JL-NWFETs at different biasing condition (on-state to subthreshold region).

To calculate the SNR for small strains, the same method is used as given in Chapter 4 for the NWFET. The SNR calculation includes the value of the gauge factor, intrinsic noise and applied

strain and shown in Figure 5.10 for all devices. Results suggested that both the gauge factor and noise amplitude depend on the applied gate voltage, providing an easier way to enhance the SNR significantly by tuning small gate bias in the JL-NWFET. Low noise amplitude in the JL-NWFET offers high SNR at low voltages and can be incorporated as promising sensing element in application-specific integrated circuits.

5.4 Performance enhancement in junctionless nanowire FET

It has been demonstrated in the last chapter that nanowire FET in gate-all-around (GAA) architecture is a promising candidate for future CMOS electronics due to its ideal gate controllability, low leakage, and enhanced carrier transport property. Nanowires and back-gated NWFETs have been studied for many sensing applications such as chemical and biochemical sensing elements [127, 128]. They have also been reported to have high piezoresistivity, offering their application as sensing element for physical sensors [14]. However, the high surface-to-volume ratio in nanowires, which improves sensitivity to applied strain, makes them prone to noise and leading to reduced signal-to-noise ratios [129]. Furthermore, in the earlier sections of this chapter, the junctionless NWFET was presented as a promising sensing element and the structure was similar to the NWFET presented in the last chapter. The junctionless transistor is illustrated with significantly lower intrinsic noise and attracted attention to use it for strain sensing applications. Thus, it is a necessity to compare the performance of the proposed junctionless NWFET with the conventional inversion mode NWFET before claiming them as better sensing element for strain sensing applications. In the last section, the device performance is compared between the junctionless and inversion-mode nanowire FET. The comparison included typical device parameters with intrinsic noise and finally, the performance of the

sensing capability was concluded with the minimum detectable strain value obtained for these sensing elements. Both devices were having similar dimensions and operating conditions.

Both the inversion mode NWFET and JL-NWFET were characterized having 160-nm gate length and nanowire diameter $d \sim 10$ nm. DC I - V characteristics were measured using a semiconductor parameter analyzer HP4156B. The low-frequency noise measurements were performed with a battery-powered SR570 low-noise current preamplifier and a HP35670A dynamic signal analyzer. Figure 5.11 shows the transfer characteristics for both devices. They exhibit excellent electrostatic control with high ON/OFF ratio ($>10^7$), low subthreshold slope (SS < 80 mV/dec), and ultra small drain-induced barrier lowering. The threshold voltage (V_{TH}) of the JL-NWFET was tunable and more appropriate to CMOS applications due to p++ doping in polysilicon gate.

Figure 5.11. I_{DS} - V_{GS} characteristics of n -type GAA NWFET and JL-NWFET (doping in the fin was $6.7 \times 10^{18} \text{ cm}^{-3}$).

Shown in Figure 5.12(a) and 5.12(b) are the output characteristics of the NWFET and JL-NWFET devices, respectively. The junctionless device showed improved (1.76 versus 1.7)

velocity saturation index (value of α in $I_{Dsat} \propto (V_{GS} - V_{TH})^\alpha$) as a result of reduced surface scattering due to the bulk conduction and lower vertical electric field.

Figure 5.13 and 5.14 show the frequency dependence of the measured drain current noise spectral density (S_{ID}) at different operating regimes (subthreshold to inversion) for the NWFET and JL-NWFET, both biased in the linear regime, $V_{DS} = 0.1$ V.

Figure 5.12. Output (I_{DS} - V_{DS}) characteristics of n-type GAA (a) NWFET and (b) JL-NWFET.

In the NWFET (Figure 5.13), the noise spectral density showed about two orders of magnitude change within a span of 0.4 V gate bias around V_{TH} . It showed $1/f$ -like trend for the inversion regime ($V_{GS} > V_{TH}$), but less $1/f$ like dependence in the subthreshold ($V_{GS} < V_{TH}$). The low noise in the subthreshold regime is attributed to most of the electrons conducting at the core of the wire, limiting the LFN to be caused mainly by mobility fluctuations [130].

Figure 5.13. Drain-current noise spectral density (S_{ID}) versus frequency for n-type NWFET at $V_{DS}=0.1$ V.

Figure 5.14. Drain-current noise spectral density (S_{ID}) versus frequency for different channel doping n-type JL-NWFET devices at $V_{DS}=0.1$ V. The left inset shows the electric field directions inside the channel with $V_{GS} < V_{TH}$ and $V_{GS} > V_{TH}$. The right inset shows the effect of channel doping on the LFN.

With increasing gate voltage, the carriers move close to the silicon oxide interface, which adds the number fluctuation component to the mobility fluctuation and thus increases the LFN [131].

Figure 5.14 showed the drain-current noise spectral density in JL-NWFETs. As compared to the NWFET, it showed about five orders of magnitude lower power spectral noise. The $1/f$ and gate bias dependence were also weaker. The reduced LFN in the GAA JL-NWFET is attributed to the favorable vertical electric field magnitude and orientation, and bulk conduction. Indeed, the vertical electric field changes sign – passes through zero – while switching the device from OFF to ON or vice versa (inset to Figure 5.14). In the junctionless NWFET, two n-type silicon nanowires were used as channel and the gate material was poly-silicon heavily doped with p++ doping (Figure 5.15). In the subthreshold regime, the carriers travel at the core of the wire and the vertical field assists them to remain away from the channel oxide interface.

Figure 5.15. Cross section and SEM picture of completed JL-NWFET. 160nm-long twin Si NWs attached with source/drain (Inset image showing the twin nanowire formation before gate formulation).

Thus, the LFN in this case is expected to be limited by mobility fluctuations caused by lattice scattering [26], similar to the NWFET discussed above. The similar LFN behavior for devices with different channel doping (inset to Figure 5.14) infers that the dopants inside the channel do

not contribute to the low-frequency noise. Beyond the threshold regime, carriers conduct throughout the channel body with very little (much lower than the inversion mode device) vertical field keeping the LFN low. Although such low LFN values have been reported earlier in buried channel devices [132], extremely weak $1/f$ dependence deserves further investigation.

Further, it is worth discussing here that the LFN behavior presented here for the GAA JL-NWFET is different from recently reported for tri-gate junctionless n-FET in [133]. In a junction-less tri-gate, the channel starts to form at the bottom surface of the fin. Therefore, carriers always remain at the bottom interface (even in the subthreshold regime) and thus get to see the interface scattering and the trapping or de-trapping from that interface. On the other hand, the channel formation in a GAA device starts from the nanowire core and then expands towards the interface, keeping the LFN limited to mobility fluctuations before the device is biased in strong accumulation.

5.4.1 Minimum detectable strain improvement

To measure the performance of the strain sensors, the term minimum detectable strain (*MDS*) is used as described in the last chapter. The *MDS* is the noise equivalent strain, which was defined as the drain current noise amplitude (A) divided by the strain sensitivity. The measurement has been completed for both junction and junctionless NWFET and concluded with the *MDS* value to optimize the best sensing element. It is shown in the last chapter that the *MDS* value was calculated from measurements of the spectral current noise at 2 Hz, drain current I_{DS} and the gauge factor. The *MDS* value was calculated for different region of operation and with the higher gauge factor and lower noise, the best *MDS* $\sim 1.5 \times 10^{-7}$ was reported at the subthreshold region.

It is found that the gauge factor was lower in the junctionless NWFET due to high doping in the nanowire channel. Also, the intrinsic noise was not changed with the gate bias and it helped to get lower noise even at high gate bias. As high gate bias turns out high on-current, superior *MDS* was obtained in on-state for all junctionless devices. The *MDS* value was calculated for the junctionless NWFET, and $MDS \sim 3.8 \times 10^{-8}$ was found almost four times lower than conventional NWFETs. It can be seen from Figure 5.16 that the best value of *MDS* obtained for the junctionless NWFET is 3.8×10^{-8} . The *MDS* value of the Junctionless NWFET was about a factor of four times smaller than that of the inversion mode NWFET when other parameters were identical. Transistors with lower doping showed relatively superior *MDS* as the gauge factor was increased significantly due to lower doping in the channel.

Figure 5.16. Extracted resolution (minimum detectable strain) is found to be superior for higher doping devices and increases when transistor operates at on-state region. Resolution is shown for NWFET (inset) at different biasing condition.

This was obviously due to the similar noise level irrespective of the channel doping concentration. The results imply that the *MDS* relies not only on the mechanical properties of the channel material, structure of the transistor and piezoresistive characteristics of the NWFET but

also on the operating voltages. A relation of the *MDS* versus biased voltages for the NWFET and junctionless NWFET is plotted in Figure 5.16.

It was observed in the JL-NWFET that the *MDS* value decreased as the biased voltage increased, which was opposite to the NWFET. It provides opportunity to obtain higher resolution and signal-to-noise ratio even with higher drain current ($V_{GS} \gg V_{TH}$). As shown in Figure 6.16, lower LFN in the JL-NWFET provides superior resolution (minimum detectable strain) than the reported values of piezoresistors [134] and FET-based sensing elements [135, 136]. Lastly, the performance of different sensing elements has been summarized in Table 5.1 to compare the performance of presented work with state-of-art.

Table 5.1 *Benchmark comparison of different sensing element used for strain sensing.*

Device	Sensing element	Spectral noise	Sensing element Size	Gauge factor
Rasmussen et al. 2003	Doped piezoresistor	2.7 μ V	$5.5 \times 10^9 \text{ nm}^2$	~30
Shekhawat et al. 2006	MOSFET	60 nA	$6 \times 10^8 \text{ nm}^2$	~50
Singh et al. 2011	NWFET	~(1nA-100 pA)	$1.8 \times 10^2 \text{ nm}^2$	~ (50-350)
JL-NWFET-based	JL-NWFET	~(10pA-1 pA)	$1.8 \times 10^2 \text{ nm}^2$	~ (30-175)

5.5 Conclusion

A novel n-type junctionless nanowire field-effect transistor (JL-NWFET)-based sensing element was presented in this chapter to reduce the junction-related degradations in nano scale transistors and to improve the strain detection limits. As an alternative to conventional inversion mode transistors, junctionless transistor devices were made using doped silicon nanowire channel with

no physical junction at the source and drain end. The JL-NWFET transistor showed excellent electrostatic control with high ON/OFF ratio ($>10^7$), low subthreshold slope ($SS < 80$ mV/dec), and ultra small drain-induced barrier lowering. Compared to the inversion mode counterpart, the junction-less device showed improved (1.76 versus 1.7) velocity saturation index as a result of reduced surface scattering due to bulk conduction and lower vertical electric field. The piezoresistance increment was observed for different doping and 91% increment in piezoresistance was observed for a doping level of $6.7 \times 10^{18} \text{ cm}^{-3}$, compared to the device with a doping level of $6.7 \times 10^{19} \text{ cm}^{-3}$. Unlike in conventional transistors, the drain current of the junctionless FET increased with the temperature.

Furthermore, the low-frequency noise was presented for the n-type gate-all-around JL-NWFET with respect to the channel doping and the gate bias voltage. Irrespective of the doping level in the channel, which was the same as that of source/drain, the JL-NWFET showed ~5 orders of magnitude lower spectral noise than the inversion mode counterpart. Unlike the NWFET, the LFN in the JL-NWFET varied less due to change in the gate bias voltage. The LFN in the JL-NWFET was also found to be less sensitive to the gate bias voltage and the frequency. The carriers travel through the whole silicon channel body having less interaction with the interface, resulting in much lower LFN compared to the inversion mode counterpart. The verification of lower noise confirmed the feasibility of the JL-NWFET as a promising sensing element and the picoamperes drain current noise helped to achieve a superior resolution (minimum detectable strain) and formulate the JL-NWFET as an ultrasensitive sensing element for nanoelectromechanical sensors. The observed resolution (minimum detectable strain) $\sim 3.8 \times 10^{-8}$ was found to be at least four times better than the best reported values for piezoresistors and inversion mode transistors in the literature.

Chapter 6

Conclusions and recommendations for future work

This chapter presents a number of key results drawn from this research and proposes recommendations for future work in this area. The focus of this thesis has been to extend and optimize the piezoresistive properties of transistors in the static sensing mode, specifically to enhance the strain detection limits of transistor-based sensors as a prime target. The aim was to enhance the piezoresistance while minimizing the intrinsic noise during sensor operation. Three different kinds of novel transistor-based sensing elements were designed, fabricated, characterized and optimized for piezoresistive measurements in this project. The research work has been done and major contributions during this project are concluded thoroughly in Section 6.1. Recommendations of further study beyond this thesis are outlined in Section 6.2.

6.1 Contributions

In this thesis, a comprehensive study, including the theoretical analysis of piezoresistive effect in nanoscale transistors, various kinds of transistor designs as well as fabrication optimization and electromechanical characterization on the transistor-based sensors, was carried out. In brief, the piezoresistive sensitivity and the drain current noise of transistor-based sensing element were systematically investigated with respect to the transistor geometry, channel material, doping dose and the operating biased voltage. With noise and dimension optimization results, nanowire

channel transistors were designed and fabricated by using single-crystal silicon and doped-silicon as the transistor channel. Measurement results have shown significant enhancement in the piezoresistive coefficient for nanowire transistors and the highest gauge factors were obtained for the gate-all-around nanowire FET. Of the two inversion mode and junctionless transistors, junctionless transistors showed relatively much lower $1/f$ noise. The gauge factor was reduced due to the doped channel in the JL-NWFET; however, lower intrinsic noise improved the minimum detectable strain. The main contributions of this thesis are summarized in the following points:

- To understand the piezoresistive response of the planar FET, the design, fabrication, and testing results were reported for six nMOSFETs with different channel geometries embedded into cantilevers. The stress sensitivity response was characterized by measuring the micromechanical response of the cantilever upon bending, which has not previously been reported for various channel geometry transistors. The observed drain current change was found comparable to the literature for the surface stress on the {100} plane. Sensitivity results have been demonstrated for a wide range of width and length transistors to optimize the parameters of channel designs to achieve the maximum sensor sensitivity. The sensitivity increment of 63.6% was observed for embedded transistor devices with smaller width ($W=60\text{ }\mu\text{m}$) transistors compared with the large width ($W=300\text{ }\mu\text{m}$) ones. In force sensing or AFM applications, higher aspect-ratio transistors were found to be optimal for absolute current change, however lower aspect-ratio transistors provided better current change in percentage. The low-frequency noise (LFN) characteristics of the transistors showed the drain current noise in the sub-nanoampere range and an optimized resolution (minimum detectable force $=70\text{ nN}$) was obtained for higher aspect-ratio transistors. These results, along with previous

developments in miniaturized cantilever sensors, make it feasible for these sensors to be used in real sensing applications such as ultra-sensitive stress and force transducers.

- To understand the electromechanical response in p-type FET, three pMOSFETs were embedded into the cantilever base as piezoresistive sensing elements. The displacement testing revealed the highest overall current change for the small width pMOSFET owing to the high localized mechanical stress. Furthermore, a wide tuning range of more than 200% was achieved for the relative drain current change through the modulation of the gate bias. However, within the same span of the gate bias, the pMOSFET with different width-to-length ratio exhibited different trends owing to adverse effects between the subband energy shift and the inversion carrier concentration variation. As sensor dimensions are progressively evolving into sub-micron and nanometre regimes, such tunable feature of piezoresistive pMOSFETs provides valuable opportunities to compensate process variations and tailor the sensor performance for specific applications.
- Towards the realization of quantum electromechanical effects in the nanostructure devices, the NWFET-based sensing element was demonstrated with a higher gauge factor, lower noise and miniaturized size compared to planar transistors. Since reports published on giant piezoresistance in silicon nanowires, several researchers carefully investigated the giant piezoresistance existence and have not succeeded to reproduce it. In our work, no giant piezoresistance is measured even for nanowires in dimensions as low as 10 nm width. However, by using gate-bias controlled nanowire FETs, ‘tuning’ effect of piezoresistance is measured and the low noise was reported for the first time that changes with the gate bias. The surrounding gate also provided complete shielding from environmental charges and prevented the humidity effects to change the drain current that are independent of stress. The

tunability of the piezoresistance and noise in gate-all-around nanowire FET was investigated with respect to the gate voltage. With narrow gate bias span of 0.8 V near the threshold region, the piezoresistive coefficient of NWFET enhanced up to seven times from $29 \times 10^{-11} \text{ Pa}^{-1}$ to $207 \times 10^{-11} \text{ Pa}^{-1}$ under both compressive and tensile strain conditions. The sensor performance was compared in terms of resolution which includes both gauge factor and electrical noise. Results revealed the reduction of $1/f$ noise in NWFET when biased in the subthreshold region, improving the resolution, i.e. minimum detectable strain, by sixteen times. Because of higher piezoresistance and low noise, the minimum detectable strain (MDS) of the sensor remains as an attractive choice for physical sensors. The NWFET operates at low bias with higher signal-to-noise ratio (SNR), and offers promising applications in low power strain sensors.

- The NWFET-embedded pressure sensor has been demonstrated and the gate bias variation was used to increase the pressure sensitivity. Results showed that the carrier confinement in the NWFET channel was attained with lower gate bias, which enabled the significant enhancement of the pressure sensitivity. The NWFET device has been optimized with respect to noise and sensitivity, and the current change to pressure improved by a factor of 4 within a 0.4 V gate bias span. A figure of merit in terms of the SNR has been calculated to compare as a performance of the pressure sensor. The dependence of the SNR on the gate bias was significant and the maximum SNR value was found at $V_{GS} = -0.2 \text{ V}$ (subthreshold regime). The higher SNR was explained by the gate bias dependency of both higher gauge factor and lower noise amplitude in the subthreshold regime. Results suggest that operating the NWFET sensing element in the subthreshold regime to maximize the sensor resolution and low-

voltage operation provides promising applications for miniaturized low power pressure sensors.

- As an alternative to conventional inversion mode transistors, a novel n-type junctionless FET- based sensing element was reported to overcome the challenges of forming junctions in nano scale transistors and to improve the strain detection limits. The junctionless transistor devices were made using doped silicon nanowire channel and showed full CMOS functionality. With the gate-all-around structure, complete carrier depletion in the nanowire was possible by using heavy p-type doping in the poly-silicon gate. The JL-NWFET exhibited excellent electrostatic control with high ON/OFF ratio ($>10^7$), low subthreshold slope ($SS < 80$ mV/dec), and ultra small drain-induced barrier lowering. Unlike in conventional transistors, the drain current of the junctionless FET increased with the temperature. These devices offered more appropriate threshold voltage (V_{TH}) due to p++ doping in the poly-silicon gate. Compared to the inversion mode counterpart, the junctionless device showed improved (1.76 versus 1.7) velocity saturation index as a result of reduced surface scattering due to the bulk conduction and lower vertical electric field. Results revealed the channel doping and gate bias impacts on the piezoresistance and the threshold voltage. In the JL-NWFET, at a doping level of $6.7 \times 10^{18} \text{ cm}^{-3}$, 91% increment was found in the piezoresistive effect compared to the device with a doping level of $6.7 \times 10^{19} \text{ cm}^{-3}$. The wide threshold voltage variation was achieved for the junctionless transistor with the variation of the channel doping.
- The n-type gate-all-around (GAA) junctionless nanowire field-effect transistor (JL-NWFET) along with LFN was presented with respect to the channel doping and the gate bias voltage. Irrespective of the doping level in the channel, which was the same as that of source/drain,

the JL-NWFET showed ~5 orders of magnitude lower spectral noise than the inversion mode counterpart. The LFN in the JL-NWFET was also found to be less sensitive to the gate bias voltage and the frequency. The superior LFN behavior in the GAA JL-NWFET was attributed to the conduction of carriers inside the uniformly-doped nanowire channel. The channel doping showed a wide tunability of the threshold voltage without any influence on the LFN. It provides an opportunity to obtain superior resolution with high SNR value at higher drain current ($V_{GS} \gg V_{TH}$). The picoamperes drain current noise helps achieve a superior resolution (MDS) and formulate the JL-NWFET as an ultrasensitive sensing element for nanoelectromechanical sensors. The observed resolution (minimum detectable strain) was found to be at least four times better than the best resolution reported for piezoresistors and inversion mode transistors in the literature.

6.2 Recommendations for future work

Although various kinds of transistor-based sensing elements were developed and demonstrated with improved piezoresistance and lower intrinsic noise, the following works are needed and recommended to be studied in future to make them practical for various sensing applications.

- It is suggested to demonstrate the dynamic response of the piezoresistive transistor sensors. A new class of MEMS resonators based on the piezoresistive transistor readout principle can be designed and characterized. In these devices, the strain in the extensional vibration mode will be converted into an electrical signal using the piezoresistive effect of a transistor-based sensing element. This kind of piezoresistive resonator can be designed in different shapes, such as the shape of a ring, to operate in a flexural in-plane mode. These

resonators will be able to operate at larger excitation forces without having the mode-coupling problem, as compared to conventional piezoresistive resonators.

- In this work, all drain current noise measurements have been completed with respect to different doping and biasing voltages and the influence of strain was not considered. The understanding of strain effects on the transistor internal noise is needed to further improve the detection limits. It is difficult to isolate strain effects from the fabrication process as the dominant cause of $1/f$ noise change was measured by simple comparisons of noise measurements at different biasing voltages. In the future work, different kinds of external mechanical stresses can be applied in order to measure strain effects on $1/f$ noise to all kinds of micro and nano transistors reported in this thesis. Experimental results can be obtained by characterizing the transistors with an electrical noise measurement setup integrated with a four-point bending jig for applying the mechanical strain. Measurement results and data analysis will show the extracted average noise power spectral densities under different kinds of applied strain. By concluding the detailed mechanisms of strain effects on noise PSD, parameters can be concluded to minimize the total intrinsic noise and sensors can be designed to further improve the detection limits.
- The temperature dependence on the main electrical parameters of junctionless silicon nanowire transistors has been analyzed. Unlike in conventional FETs, the drain current of junctionless FETs increases when temperature is increased. The nanowire FET device capabilities can be measured under the harsh environments, such as high temperature and high pressure, to find the possibility to propose them as promising sensing element in rugged electronics.

- Higher piezoresistance and lower intrinsic noise may offer promising applications in using nanowire transistors in many biomedical sensing applications such as blood flow measurements. The core sensing mechanism is by measuring the resistance change of a transistor sensing element attached to the moving part of the flow sensor. Variations of blood flow rate cause pressure or flow change, which deflects the moving part, such as a cantilever beam or diaphragm, of the flow sensor. The mechanical deformation further causes strain change on the embedded transistor whose drain current value varies with its internal strain. By accurately measuring the drain current change on the transistor, it will be possible to measure the blood flow variation. Sensitive monitoring of the blood flow rate within the graft can give an early indication of in-situ blood clot, debris, upstream stenosis or subsequent graft failure.
- The piezoresistive coefficient and electronic noise of the proposed GAA-NWFET should be investigated at the elevated temperatures. It will help to understand the stress measurements over a wide range of temperature and to obtain a comprehensive (GAA-NWFET) set of piezoresistive coefficients over a broad range of temperature. Results will demonstrate proper methods for relating coefficients at different temperatures, and to obtain consistent formulation of $R(\sigma, T)$ valid for wide temperature range.
- As GAA nanowire channel dimension is in nanometer dimension and it was separated from bulk silicon layer, the localized heating phenomenon is caused due to contentious current flow in nanowires as there is no pathway to drain the localized heat. The effect of this heat flow can slows down the transistor speed, deteriorates the interconnect delay, and causes reliability issues. These issues should be carefully observed to comment on the electromechanical response under the localized heating.

References

1. W. P. Eaton and J. H. Smith, Micromachined pressure sensors: review and recent developments, *Smart Mater. Struct.* 6 (1997) 530–9.
2. L. Gisela, R. E. Palmer, K. S. Pister and K. P. Roos, Miniature heart cell force transducer system implemented in MEMS technology, *IEEE Trans. Biomed. Eng.* 48 (2001) 996–1006.
3. B. H. Bae, H. S. Kee, S. H. Kim, Y. LEE, T. S. Kim, Y. K. Kim and K. H. Park, In vitro experiment of the pressure regulating valve for a glaucoma implant, *J. Micromech. Microeng.* 13 (2003) 613–619.
4. C. L. Britton, R. Jones, P. Oden, Z. Hu, R. Warmack, S. Smith, W. Bryana and J. Rochelle, Multiple-input microcantilever sensors, *Ultramicroscopy* 82 (2000) 17–21.
5. E.A. Wachter and T. Thundat, Remote optical detection using microcantilevers, *Rev. Sci. Instrum.* 66 (1995) 3662–3667.
6. R. Bashir, BioMEMS: state-of-the-art in detection, opportunities and prospects, *Adv. Drug Deliv. Rev.* 56 (2004) 1565–1586.
7. X. Ting, Z. Wang, J. Miao, L. Yu, C. Li, Micro-machined piezoelectric membrane based immunosensor array, *Biosens. Bioelectron.* 24 (2008) 638–643.
8. N. V. Lavrik, M. J. Sepaniak, P. G. Datskos, Cantilever transducers as a platform for chemical and biological sensors, *Rev. Sci. Instrum.* 75 (2004) 2229–2253.
9. T.E. Schaffer, Calculation of thermal noise in an atomic force microscope with a finite optical spot size, *Nanotechnology* 16 (2005) 664–670.

10. G. Meyer and N. M. Amer, Novel optical approach to atomic force microscopy, *Appl. Phys. Lett.* 53, (1988) 1045-1047.
11. A. V. Chavan and K. D. Wise, Batch-processed vacuum-sealed capacitive pressure sensors, *IEEE J. Microelectromech. Syst.* 10 (2001) 580–588.
12. R. Marie, H. Jensenius, J. Thaysen, C. B. Christensen and A. Boisen, Adsorption kinetics and mechanical properties of thiol-modified DNA-oligos on gold investigated by microcantilever sensors, *Ultramicroscopy* 91 (2002) 29-36.
13. J. K. Otto and T. D. Brown, Static and dynamic response of a multiplexed array piezoresistive contact sensor, *Exp. Mech.* 39 (1999) 317–323.
14. J. X. Cao, X. G. Gong, and R. Q. Wu, Giant piezoresistance and its origin in Si(111) nanowires: First-principles calculations, *Physical Review B* 75 (2007) 233302-5.
15. T.W. Tombler, C. Zhou, L. Alexseyev, J. Kong, H. Dai, L. Liu, C. S. Jayanthi, M. Tang, and S.-Y. Wu, Reversible Electromechanical Characteristics of Carbon Nanotubes under Local Probe Manipulation, *Nature* 405 (2000) 769.
16. A. C. H. Rowe, A. D. Barrera, C. Renner, S. Arscott, Giant Room-Temperature Piezoresistance in a Metal-Silicon Hybrid Structure, *Physical Review Letters*, 100, (2008) 145501-4.
17. R. He and P. Yang, Giant piezoresistance effect in silicon nanowires, *Nature Nanotechnology* 1, (2006) 42-46.

18. Y. P. Shkolnikov, K. Vakili, E. P. D. Poortere, and M. Shayegan, Dependence of Spin Susceptibility of a Two-Dimensional Electron System on the Valley Degree of Freedom, *Appl. Phys. Lett.* 92 (2004) 246804-7.
19. T. Ivanov, T. Gotszalk, T. Sulzbach, I. Chakarov, I. W. Rangelow, AFM cantilever with ultra-thin transistor-channel piezoresistor: quantum confinement, *Microelectronic Engineering* 67 (2003) 534–541.
20. P. Neuzil, C. C. Wong and J. Reboud, Electrically controlled giant piezoresistance in silicon nanowires, *Nano Lett.* 10 (2010) 1248–52.
21. J. S. Milne, A.C.H. Rowe, S. Arscott and C. Renner, Giant piezoresistance effects in silicon nanowires and microwires, *Phys. Rev. Lett.* 105 (2010) 226802-5.
22. J. Harley and T. Kenny, $1/f$ noise considerations for the design and process optimization of piezoresistive cantilevers, *J. Microelectromech. Syst.* 9 (2000) 226-235.
23. G. Shekhawat, S. H. Tark and V. P. Dravid, MOSFET-embedded microcantilevers for measuring deflection in biomolecular sensors, *Science* 311 (2006) 1592–5.
24. S.-H. Tark, A. Srivastava, S. Chou., G. Shekhawat and V. P. Dravid, Nanomechanoelectronic signal transduction scheme with metal-oxide-semiconductor field-effect transistor-embedded microcantilevers, *Applied Physics Letters* 94 (2009) 104101-3.
25. E. T. Scott, S. Guanyu, S. C. Youn and T. Nishida, Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap, *IEEE Transactions on Electron Devices* 53 (2006) 1010-1020.
26. L.K.J. Vandamme and F. N. Hooge, What Do We Certainly Know About $1/f$ Noise in MOSTs?, *IEEE Transactions on Electron Devices*, 55 (2008) 3070-3085.

-
27. W. Thomson, On the electro-dynamic qualities of metals: Effects of magnetization on the electric conductivity of nickel and of iron, *Proc. R. Soc. London* 8 (1856) 546–550.
 28. P. W. Bridgman, The effect of homogeneous mechanical stress on the electrical resistance of crystals, *Phys. Rev.* 42 (1932) 858.
 29. J. W. Cookson, Theory of the piezo-resistive effect, *Phys. Rev.* 47 (1935) 194–195.
 30. J. Bardeen and W. Shockley, Deformation potentials and mobilities in non-polar crystals, *Phys. Rev.* 80 (1950) 72–80.
 31. C. S. Smith, Piezoresistance effect in germanium and silicon, *Phys. Rev.* 94 (1954) 42–49.
 32. D. R. Franca and A. Blouin, All-optical measurement of in-plane and out-of-plane Young's modulus and Poisson's ratio in silicon wafers by means of vibration modes, *Meas. Sci. Technol.* 15 (2004) 859–868.
 33. I. S. Sokolnikoff, *Mathematical Theory of Elasticity*. Malabar, FL: R.E. Krieger Pub. Co., 1983.
 34. W. A. Brantley, Calculated elastic constants for stress problems associated with semiconductor devices, *J. App. Phys.* 44 (1973) 534–535.
 35. H. Rolnick, Tension coefficient of resistance of metals, *Phys. Rev.* 36 (1930) 506–512.
 36. W. C. Young and R. Budynas, *Roark's Formulas for Stress and Strain*, 7th ed. New York: McGraw-Hill, 2002.
 37. A. Boresi, *Advanced mechanics of materials*. 6th ed. John Wiley and Sons: New York, 2003.
 38. P. Bridgman, The Effect of the Transverse and Longitudinal Resistance of Metals, *Proceedings of the American Academy of Arts and Science* 60 (1925) 423–449.

-
39. P. Bridgman, The Effect of Homogeneous Mechanical Stress on the Electrical Resistance of Crystals, *Physical Review* 42 (1932) 858-863.
 40. J. Taylor, Pressure Dependence of Resistance of Germanium, *Physical Review* 90 (1950) 919-920.
 41. W. Paul, G. Pearson, Pressure Dependence of the Resistivity of Silicon, *Physical Review* 98 (1955) 1755-1757.
 42. W. P. Mason and R. N. Thurston, Use of piezoresistive materials in the measurement of displacement, force, and torque, *J. Acous. Soc. of Am.* 29 (1957) 1096–1101.
 43. Y. Kanda, A graphical representation of the piezoresistance coefficients in silicon, *IEEE Trans. Electron Devices* 29 (1982) 64–70.
 44. K. Yamada, Nonlinearity of the Piezoresistance Effect of p-type Silicon Diffused Layers, *IEEE Transactions on Electron Devices* ED-29 (1982) 71–77.
 45. O. N. Tufte, E. L. Stelzer, Piezoresistive Properties of Silicon Diffused Layers, *Journal of Applied Physics* 34 (1963) 313–318.
 46. Y. Kanda, Piezoresistance Effect of Silicon, *Sensors and Actuators A: Physical*, 28 (1991) 83–91.
 47. W. P. Mason and R. N. Thurston, Use of Piezoresistive Materials in the Measurement of Displacement, Force, and Torque, *J. Acoust. Soc. Am.* 29 (1957) 1096.
 48. O. N. Tufte and E. L. Stelzer, Piezoresistive properties of heavily doped n-type silicon, *Phys. Rev.* 133 (1964) A1705.
 49. S.D. Senturia, , *Microsystem Design*, Kluwer Academic Publishers, 2001.

-
50. K. Harafuji, Y. Yamasaki, K. Ishikawa, K. Kuwabara, Effect of three normal mechanical stresses on electrical characteristics of short-channel metal-oxide-semiconductor field effect transistor, *J. J. Appl. Phys.* 47 (2008) 824–832.
 51. M. Tortonese, R. C. Barrett, C. F. Quate, Atomic resolution with an atomic force microscope using piezoresistive deflection, *Appl. Phys. Letters* 62 (1993) 834-836.
 52. L.G. Carrascosa, M. Moreno, M. A. lvarez, L.M. Lechuga ,Nanomechanical biosensors: a new sensing tool, *Trends in Analytical Chemistry* 25 (2006) 196-206.
 53. M. J. Madou, Fundamental of micro fabrication, CRC press, second edition, (2002) 312.
 54. N. Wiener, Generalized harmonic analysis, *Acta Math.* 55 (1930) 117.
 55. M. Haartman and M. Ostling, Low-frequency noise in advanced devices, Springer (2007) 7.
 56. H. Nyquist, Thermal agitation of electricity in conductors, *Phys. Rev.* 32 (1928) 110-113.
 57. A. van der Ziel, Noise in solid state devices and circuits, John Wiley & Sons, New York, 1986.
 58. F. N. Hooge, 1/f noise sources, *IEEE Trans. Elec. Dev.* 41 (1994) 1926-1935.
 59. M. Surdin, Fluctuations in the thermionic current and the flicker effect, *J. Phys. Radium* 10 (1939) 188-189.
 60. F. N. Hooge, On the additivity of generation-recombination spectra, Part 2: 1/f noise, *Physica B* 336 (2003) 236-251.
 61. F. N. Hooge and L. K. J. Vandamme, Lattice scattering causes 1/f noise, *Phys. Lett. A* 66 (1978) 315-316.

-
62. F. N. Hooge, T. G. M. Kleinpenning and L. K. J. Vandamme, Experimental studies on 1/f noise, *Rep. Prog. Phys.* 44 (1981) 479-531.
 63. F. N. Hooge, 1/f noise is no surface effect, *Phys. Lett. A* 29a (1969) 139-140.
 64. F. N. Hooge, Discussion on recent experiment on 1/f noise, *Physica* 60 (1972) 130-144.
 65. S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Y. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, A logic nanotechnology featuring strained-silicon, *IEEE Electron Device Lett.* 25 (2004) 191-193.
 66. Y. G. Wang, D. B. Scott, Y. Wu, J. L. Waller, J. Hu, K. Liu, and V. Ukraintsev, Effects of uniaxial mechanical stress on drive current of 0.13 μm MOSFETs, *IEEE Trans. Electron Devices* 50 (2003) 529.
 67. S. M. Sze, Semiconductor devices, Physics and technology 2nd Ed., John Wiley & sons (2005).
 68. N. Dasgupta and A. Dasgupta, Semiconductor Devices, Prentice-Hall, 264 (2004).
 69. P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, Fourth Edition Ed., New York, Wiley (2001) 66–67.
 70. T. A. Fjeldly, T. Ytterdal, and M. Shur, Introduction to Device Modeling and Circuit Simulation, John Wiley & Sons, New York (1998).
 71. G. Dorda, Piezoresistance in Quantized Conduction Bands in Silicon Inversion Layers, *J. Appl. Phys.* 42 (1971) 2053.
 72. C. Herring and E. Vogt, Transport and Deformation-Potential Theory for Many-Valley Semiconductors with Anisotropic Scattering, *Phys. Rev.* 101 (1956) 944.

-
73. T. Maruyama, S. Zaima, Y. Koide, Y. Kanda and Y. Yasuda, Anisotropy of piezoresistance in n-channel inversion layers of metal oxide semiconductor transistors on (001) Si, *J. Appl. Phys.* 68 (1990) 5687-5691.
 74. H. Mikoshiba, Stress-sensitive properties of silicon-gate MOS devices, *Solid-State Electron.* 24 (1981) 221.
 75. S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap, *IEEE Transactions on Electron Devices* 53 (2006) 1010-1020.
 76. K. Uchida, T. Krishnamohan, K. C. Saraswat, and Y. Nishi, Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime, *IEDM Tech. Dig.* San Francisco CA (2006) 129-132.
 77. F. Stern, Self-consistent results for n-type Si inversion layers, *Phys. Rev. B Condens. Matter* 5 no. 12 (1972) 4891–4899.
 78. A. L. McWorther, Semiconductor surface physics, University of Pennsylvania Press, Philadelphia, 1957.
 79. S. A. Schwarz and S. E. Russek, Semi-empirical equations for electron velocity in silicon: part II-MOS inversion layer, *IEEE Trans. Electron Devices* ED-30 (1983) 1634-1639.
 80. E. P. Vandamme and L. K. J. Vandamee, Critical discussion on unified 1/f noise models for MOSFETs, *IEEE Trans. Electron Devices* 47 (2000) 2146-2152.
 81. J. Koga, S. Takagi and A. Toriumi, A comprehensive study of MOSFET electron mobility in both weak and strong inversion regimes, *IEDM Tech. Dig.* (1994) 475-478.
 82. M.J. Deen, M.W. Shinwari, J.C. Ranuarez, Noise considerations in field-effect biosensors, *J. Appl. Phys.* 100 (2006) 074703.

-
83. T. Helbling, C. Roman and C. Hierold, Signal-to-Noise Ratio in Carbon Nanotube Electromechanical Piezoresistive Sensors, *Nano Lett.* 10 (2010) 3350–3354.
 84. J. Jie, W. Zhang, K. Peng, G. Yuan, C. S. Lee and S. T. Lee, Surface-Dominated Transport Properties of Silicon Nanowires, *Adv. Funct. Mater.* 18 (2008) 3251–3257.
 85. T. Barwicz, L. Klein, S. J. Koester and H. Hamann, Silicon nanowire piezoresistance: Impact of surface crystallographic orientation, *Appl. Phys. Lett.* 97 (2010) 023110.
 86. A. C. H. Rowe, Silicon nanowires feel the pinch, *Nature Nanotech.* 3 (2008) 311.
 87. O. Wolter, T. Bayer, J. Greschner, Micromachined silicon sensors for scanning force microscopy, *J. Vac. Sci. Technol. B* 9 (1990) 1353–1357.
 88. T.R. Albrecht, S. Akamine, T.E. Carver, C.F. Quate, Microfabrication of a cantilever styli for the atomic force microscope, *J. Vac. Sci. Technol. A* 8 (1990) 3386–3390.
 89. G.G. Stoney, The Tension of Metallic Films Deposited by Electrolysis, *Proc. Roy. Soc. (London)*, 82 (1909) 172.
 90. J. A. Pelesko, D. H. Bernstein, Modeling MEMS and NEMS, Chapman & Hall/CRC, 2003.
 91. Z. H. Zhang, Y. H. Zhang, L. T. Liu, T. L. Ren, A novel MEMS pressure sensor with MOSFET on chip, *IEEE Sensors proc.* (2008) 1564 - 1567.
 92. R.G. Rudnitsky, E.M. Chow, T.W. Kenny, Rapid biochemical detection and differentiation with magnetic force microscope cantilever arrays, *Sens. Actuators A: Phys.* 83 (2000) 256–262.
 93. R. Berger, E. Delamarche, H.P. Lang, C. Gerber, J.K. Gimzewski, E. Meyer, H.-J. Güntherodt, Surface stress in the self-assembly of alkanethiols on gold, *Science* 276 (1997) 2021–2023.

-
94. P.A. Rasmussen, O. Hansen, A. Boisen, Cantilever surface stress sensors with single-crystalline silicon piezoresistors, *Appl. Phys. Lett.* 86 (2005) 203502.
 95. X. Yu, J. Thaysen, O. Hansen, A. Boisen, Optimization of sensitivity and noise in piezoresistive cantilevers, *J. Appl. Phys.* 92 (2002) 6296–6301.
 96. Zaima, T. Maruyama, Y. Yasuda, Piezoresistance in n-channel inversion layer of Si MOSFETs, *Appl. Surf. Sci.* 42 (1989) 433–438.
 97. C. Gallon, G. Reimbold, G. Ghibaudo, R.A. Bianchi, R. Gwoziecki, Electrical analysis of external mechanical stress effects in short channel MOSFETs on (0 0 1) silicon, *Solid-State Electron.* 48 (2004) 561–566.
 98. C. Ziegler, Cantilever-based biosensors, *Anal. Bioanal. Chem.* 379 (2004) 946–959.
 99. F. Gamiz, P. C. Cassinello, J.B. Roldan and F. J. Molinos, Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates, *J. Applied Physics* 92 (2002) 288.
 100. R. Schoorner, First- and second-order longitudinal piezoresistive coefficients of n-type metal-oxide-semiconductor field-effect transistors, *J. Appl. Phys.* 67 (1990) 4354–4357.
 101. J.H. Kim, K.T. Park, H.C. Kim, K. Chun. , Fabrication of a Piezoresistive Pressure Sensor for Enhancing Sensitivity Using Silicon Nanowire, *Transducers* June 21-25 (2009) 1936.
 102. T. W. Tombler, C. Zhou, L. Alexseyev, J. Kong, H. Dai, L. Liu, C. S. Jayanthi, M. Tang and S.-Y. Wu, Reversible electromechanical characteristics of carbon nanotubes under local-probe manipulation, *Nature* 405 (2000) 769-772.

-
103. X. Wang, J. Zhou, J. Song, J. Liu, N. Xu, and Z. L. Wang, Piezoelectric Field Effect Transistor and Nanoforce Sensor Based on a Single ZnO Nanowire, *Nano Lett.* 6 (2006) 2768.
 104. D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, FinFET-A self-aligned double-gate MOSFET scalable to 20 nm, *IEEE Trans. Electron Devices* 47 (2002) 2320–2324.
 105. B. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, High performance fully-depleted tri-gate CMOS transistor, *IEEE Electron Device Lett.* 24 (2003) 263–264.
 106. J. P. Colinge, M. H. Gao, A. R. Rodriguez, H. Maes, and C. Claeys, Silicon-on-insulator: Gate-all-around device, in *IEDM Tech. Dig.* (1990) 595–598.
 107. S. Monfray, T. Skotniki, Y. Morand, S. Descombes, P. Coronel, P. Mazoyer, S. Harrison, P. Ribot, A. Talbot, D. Dutartre, M. Haond, R. Palla, Y. Le Fré, F. Leverd, M. E. Nier, C. Vizioz, and D. Louis, 50 nm-gate all around (GAA)–silicon on nothing (SON)–devices: A simple way to co-integration of GAA transistors with bulk MOSFET process, in *VLSI Symp. Tech. Dig.* (2002) 108–109.
 108. T. Bradley, R.C. Jaeger, J.C. Suhling, K.J. O'Connor, Piezoresistive characteristics of short-channel MOSFETs on (1 0 0) silicon, *IEEE Trans. Electron Devices* 48 (2001) 2009.
 109. J. Chang, A. A. Abidi and C. R. Viswanathan, Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures, *IEEE Trans. Electron. Dev.* 41 (1994) 1965–1971.

-
110. K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, A unified model for the flicker noise in the metal-oxide-semiconductor field-effect-transistors, *IEEE Trans. Electron. Dev.* 37 (1990) 654-664.
 111. A. Bid, A. Bora and A. K. Raychaudhuri, $1/f$ noise in nanowires, *Nanotechnology* 17 (2006)152–6.
 112. J. Kedzierski , J. Bokor and C. Kisielowski, Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation, *J. Vac. Sci. Technol. B* 15 (1997) 2825–8.
 113. B. Bercu, L. Mont`es, F. Rochette, M. Mouis, X. Xin and P. Morfouli, Electron mobility increase in submicronic transistors integrated on ultrathin silicon diaphragms subjected to high mechanical stress, *Appl. Phys. Lett.* 96 (2010) 092107.
 114. A. A. Barlian, W.-T. Park, J. R. Mallon, A. J. Rastegar and B. L. Pruitt, Review: semiconductor piezoresistance for microsystems *Proc. IEEE* 97 (2009) 513–52.
 115. S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T.Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. E. Mansy, A 90-nm logic technology featuring strained-silicon, *IEEE Trans. Electron Devices* 51 (2004) 1790.
 116. T. Barwicz, L. Klein, S. J. Koester and H. Hamann, Silicon nanowire piezoresistance: Impact of surface crystallographic orientation, *Appl. Phys. Lett.* 97 (2010) 023110.
 117. J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, I. Blake, M. White, A. M. Kelleher, B. McCarthy and R. Murphy, Nanowire transistors without junctions, *Nature nanotechnology* 5 (2010) 225-229.

-
118. C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, Junctionless multigate field-effect transistor, *Appl. Phys. Lett.* 94 (2009) 053511.
119. C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, Low subthreshold slope in junctionless multigate transistors, *Applied Physics Letters* 96 (2010) 102105.
120. A. Lugstein, M. Steinmair, A. Steiger, H. Kosina and E. Bertagnolli, Anomalous Piezoresistance Effect in Ultrastrained Silicon Nanowires, *Nano Lett.* 10 (2010) 3204–3208.
121. K. Akarvardar, A. Mercha, E. Simoen, V. Subramanian, C. Claeys, P. Gentil, and S. Cristoloveanu, High-temperature performance of state of-the-art triple-gate transistors, *Microelectron. Reliab.* 47 (2007) 2065–2069.
122. P. Aminzadeh, M. Alavi, and D. Scharfetter, Temperature dependence of substrate current and hot carrier-induced degradation at low drain bias, in *VLSI Symp. Tech. Dig.* (1998) 178–179.
123. D. S. Jeon and D. E. Burk, MOSFET inversion layer motilities—A physically based semi-empirical model for a wide temperature range, *IEEE Trans. Electron Devices* 36 (1989) 1456–1463.
124. C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, High-Temperature Performance of Silicon Junctionless MOSFETs, *IEEE Transactions on Electron Devices* 57 (2010) 620-625.

-
125. C-L Huang, H. R. Soleimani, G. J. Gula, J.W. Sleight, A. Villani, H. Ali, Locos-induced stress effects on thin-film SOI devices, *IEEE Trans Electron Dev.* 44 (1997) 646–650.
 126. Y. Cui, Q. H. Park, and C. M. Lieber, Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species, *Science* 293 (2001) 1289-1292.
 127. X. P. A. Gao, G. Zheng, and C. M. Lieber, Subthreshold Regime has the Optimal Sensitivity for Nanowire FET Biosensors, *Nanoletters* 10 (2010)547-552.
 128. Z. Jing, R. Wang, R. Huang, Y. Tian, L. Zhang, D. W. Kim, D. Park, and Y. Wang, Investigation of Low-Frequency Noise in Silicon Nanowire MOSFETs, *IEEE Electron Device Lett.* 30 (2009) 57-60.
 129. C.Wei, Y. Z. Xiong, X. Zhou, N. Singh, S. C. Rustagi, G. Q. Lo and D. L. Kwong, Investigation of Low-Frequency noise In Silicon nanowire MOSFETs in the Subthreshold Region, *IEEE Electron Device Lett.* 30 (2009) 668-671.
 130. N. Park and K. K. O, Body bias dependence of 1/f noise in NMOS transistors from deep-subthreshold to strong inversion, *IEEE Trans Electron Dev.* 48 (2001) 999–1001.
 131. A. Zial, Unified presentation of 1/f noise in electronic devices: fundamental 1/f noise sources, *Proc. IEEE* 76 (1988) 537-571.
 132. D. Jang, J. W. Lee, C.W. Lee, J.P. Colinge, L. Montès, J. Lee, G. T. Kim, and G. Ghibaudo, Low-frequency noise in junctionless multigate transistors, *Appl. Phys. Lett.* 98 (2011) 133502-133504.
 133. P.A. Rasmussen, J. Thaysen, O. Hansen, S.C. Ericsen and A. Boisen, Optimised cantilever biosensor with piezoresistive read-out, *Ultramicroscopy* 97 (2003) 371-375.
 134. J. L. Plumb and E.R. Chenette, Flicker noise in transistors, *IEEE Transactions on Electron Devices* 10 (1963) 5.

135. P. Singh, J. Miao, W.-T. Park and D.-L. Kwong, Gate-bias controlled sensitivity and SNR enhancement in a nanowire FET pressure sensor, *J. Micromech. Microeng.* 21 (2011) 105007(7).

Publications

Research Papers in Peer-reviewed International Journals:

1. Jia Hao Cheong, Simon Sheung Yan Ng, Xin Liu, Rui-Feng Xue, Huey Jen Lim, Pradeep Basappa Khannur, Kok Lim Chan, Andreas Astuti Lee, Kai Kang, Li Shiah Lim, Cairan He, Pushpapraj Singh, Woo-Tae Park and Minkyu Je, “An Inductively Powered Implantable Blood Flow Sensor Microsystem for Vascular Grafts”, ***IEEE Trans. on Biomedical Engineering***, 2012 DOI: 10.1109/TBME.2012.2203131.
2. Pushpapraj Singh, Jianmin Miao, Vincent Pott, Woo-Tae Park, Dim-Lee Kwong, “Channel Doping and Gate Bias Effects on the Piezoresistive Performance of Junctionless Nanowire FET”, ***Applied Physics Letters***, 2012, (Under review).
3. Pushpapraj Singh, Woo-Tae Park, Jianmin Miao, Shao Lichun, Rama Krishna Kotlanka, Dim-Lee Kwong , “Tunable Piezoresistance and Noise in Silicon Gate-All-Around Nanowire Transistors”, ***Applied Physics Letters*** , 100, pp. 063106, 2012.
4. Pushpapraj Singh, Navab Singh, Jianmin Miao, Woo-Tae Park, Dim-Lee Kwong , “Gate-All-Around Junctionless Nanowire MOSFET with Improved Low-Frequency Noise Behavior”, ***Electron Device Letters***, 32 (12), pp. 1752, 2011.
5. Pushpapraj Singh, Jianmin Miao, Woo-Tae Park, Shao Lichun, Dim-Lee Kwong , “Gate-Bias Controlled Sensitivity and Signal-to-Noise Ratio Enhancement in Nanowire FET Pressure Sensor”, ***Journal of Micromechanics and Microelectronics***, 21, pp. 105007, 2011.
6. Li-Shiah Lim, Woo-Tae Park, Liang Lou, Han-Hua Feng, **Pushpapraj Singh** , “Design, Fabrication and Characterization of ultra-miniature piezoresistive Pressure Sensors for medical implants”, ***Advanced Material Research***, 254, pp. 94-98, 2011.
7. Pushpapraj Singh, Jianmin Miao, Rama Krishna Kotlanka, Shao Lichun, Woo Tae Park, Dim-Lee Kwong, “Microcantilever sensors with embedded piezoresistive transistor read-out: design and characterization”, ***Sensors and Actuators: A*** , 171, pp. 178, 2011.
8. Pushpapraj Singh, Jianmin Miao, Lichun Shao, Ramakrishna Kotlanka, and Dim-Lee Kwong, “Tunable microcantilever sensors with embedded piezotransistors”, ***Electronics Letters***, 46, pp.1557, 2010.

Research Papers in International Conferences:

1. **Pushpapraj Singh**, Jianmin Miao, Woo-Tae Park, Dim-Lee Kwong, “*Piezoresistance and low frequency noise study in junctionless nanowire FET*” IEEE MEMS, 29 Jan-2 Feb 2012, Paris France.
2. **Pushpapraj Singh**, Woo-Tae Park, Han-Hua Feng, “*Battery less MEMS Flow Sensor within Prosthetic Vascular Graft*” DSR, 3- 5 August 2011, Singapore.
3. **Pushpapraj Singh**, Jianmin Miao, Woo-Tae Park, Lim Li Shiah, Dim-Lee Kwong, “*Piezoresistance Effects in Junctionless Nanowire Transistors*” ICMAT, 26 Jun-1 Jul 2011, Singapore.
4. **Pushpapraj Singh**, Jianmin Miao, Woo Tae Park, Dim-Lee Kwong , “*Ultrasensitive Pressure Sensor Based on Gate- All-Around Nanowire FET*”, Transducers, 5- 9 June 2011, Beijing China.
5. Li-Shiah Lim, Woo-Tae Park, Liang Lou, **Pushpapraj Singh**, Han-Hua Feng, “*Design, Fabrication and Characterization of ultra miniature piezoresistive Pressure Sensors for medical implants*” ICMAT, 26 Jun-1 Jul 2011, Singapore.
6. **Pushpapraj Singh**, Jianmin Miao, Lichun Shao, Rama Krishna Kotlanka, Woo Tae Park, Dim-Lee Kwong, “*Impact of channel aspect ratio on the sensitivity of transistor-integrated microcantilever biosensor*” , International Conference on Cellular & Molecular Bioengineering, 2-4 August 2010, Singapore.
7. **Pushpapraj Singh**, Jianmin Miao, “*Piezotransistor-Embedded Microcantilever Platform for Strain Sensing Applications*”, IEEE Sensors, 1-4 November 2010, Hawaii USA.