Development of control schemes for power converters and coordinated grid operation

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Development of Control Schemes for Power Converters and Coordinated Grid Operation

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Summary

Power electronic converters can convert electricity from AC to DC form or vice versa in order to supply different types of loads. Among various developed converter topologies, three-phase pulse-width modulated (PWM) converters, built with fully controllable semiconductor devices, have been increasingly adopted by many power electronic applications. Examples include grid-connected inverters for delivering renewable energies into the utility grids, uninterruptible power supplies (UPS) for supporting emergency loads during mains outage, active power filters (APF) for power quality enhancement in distributed generation (DG) systems and active rectifiers for harmonic-free AC / DC power conversion.

Development of proper control schemes for three-phase PWM converters is crucial to achieve intended functions such as high conversion efficiency, low harmonic distortion and accurate control of real and reactive power flows. Undeniably, many control schemes have since been proposed with specific advantages. Although less explicitly stated, all schemes may have disadvantages too, which is the main reason why research for an even better solution is still on-going. Contributing to that effort, a repetitive current control scheme is first presented in the thesis for three-phase PWM inverter interfaced to the ac mains. The proposed controller is designed using complex vector (CV) theory, and can inherently filter off ac grid background harmonics, preventing them from distorting the grid currents.

Based on the developed CV repetitive control algorithm, a double loop control structure is subsequently presented for a three-phase power converter with LC output filter. As its output voltages can be regulated directly, the controlled power converter can provide undisturbed voltages to emergency loads in case of ac mains outage. Because of that, it is classified under UPS with its outer voltage loop capable of

rejecting load harmonics and inner current loop able to guarantee fast dynamic response. The resulting UPS system can therefore function well in both steady and transient states, for unbalanced and nonlinear loads.

Traditionally, a grid inverter is connected to the utility grid through a single inductor. This inductive filter may become very bulky and costly in high power conversion systems as to attenuate switching harmonics. To reduce its overall inductance and hence size, an inductor-capacitor-inductor (LCL) filter is recommended for smoothing the output current of a switching power converter. Although effective, an LCL filter is a higher third-order filter that has its own stability and design concerns to address. Some of these challenges are investigated here, mainly on its inherent resonance damping characteristic and the development of a generalized design methodology. It is shown that in the ideal case, proper damping of LCL resonance can be achieved naturally without incorporating additional damping control techniques. If the ideal design criterion is not fulfilled, a simple compensation method is provided for tuning the damping factor to meet overall system stability.

Besides supplying power to the utility grid and loads, a three-phase PWM converter can also be used for power quality enhancement in distributed generation (DG) systems, especially in weak power systems where the ac grid voltages are not stiff. To reduce system costs and improve its harmonic compensation ability, an LCL-filter is again used for constructing a shunt APF system. Relevant system implementation details are provided in the thesis, along with its generalized design approach and associated control algorithms. The developed shunt APF system covers a wide range of harmonic frequencies, and has some merits over conventional APF systems.

Instead of adding active filter and / or other types of power conditioners, power quality improvement can be achieved by developing more advanced control schemes for an active rectifier performing AC / DC power conversion for a majority of dc power supplies. The resulting rectifier still provides the requested dc power, but injects less

low-order harmonic currents to the ac grid. Since harmonics are explicitly dealt with, the proposed rectifier uses the one-cycle control (OCC) scheme, which is known to be a nonlinear method with fast dynamic response for tracking purposes. The investigation also concentrates on non-ideal operating conditions such as unbalanced and / or distorted input voltages. An improved OCC scheme is proposed for suppressing these non-idealities, while keeping the physical controller simple.

All design methodologies and control algorithms proposed throughout the course of development have been thoroughly verified in simulation using MATLAB / Simulink and PLECS. Suitably scaled experimental prototypes have also been built in the laboratory for validating the practicalities of all theoretical findings.

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List of Abbreviations

APF	Active Power Filter
CCM	Continues Conduction Mode
CSC	Current-Source Converter
CV	Complex-Vector
DCM	Discontinuous Conduction Mode
DG	Distributed Generation
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMF	Electromotive Force
EMI	Electromagnetic Interference
HPF	High Pass Filter
IGBT	Insulated Gate Bipolar Transistor
LCL	Inductor-Capacitor-Inductor
LPF	Low Pass Filter
OCC	One-Cycle Control
PCC	Point of Common Coupling
PFC	Power Factor Correction
PI	Proportional Integral
PLL	Phase-Locked Loop
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse-Width Modulation
SAPF	Shunt Active Power Filter
SHC	Selective Harmonic Compensation
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply

VSC	Voltage-Source Converter
VSI	Voltage-Source Inverter

Chapter 1 Introduction

1.1 Background and Motivation

Led by the rapid development of technology worldwide, power electronics has become an attractive research area for investigation with various converter topologies and semiconductor devices invented for modern applications. The basic functionality of a power converter is to convert electrical energy from one form to another. An illustrative example of energy conversion is an AC / DC converter or rectifier, which can commonly be found in consumer electronic products, such as television sets and personal computers, to provide an appropriate dc power supply. Power levels can range from several watts to hundreds of megawatts. Recent examples are linked to the fast development of renewable energy and the growing adoption of decentralized sources for distributed generation, where the power converters in the range of tens of megawatts are in high demand for safe interfacing to the grid and high efficiency is a basic requirement for these converters.

Besides development of renewable sources, many power system loads in residential and industrial facilities have some degree of nonlinearity. These nonlinear loads may produce or absorb harmonics to or from the grid, where the degraded power quality might affect distant sensitive loads because of the vastness of the grid. The affected equipment would likely be those found in hospitals, defense and critical semiconductor industries, whose shutdown would be lengthy even if not detrimental. To minimize shutdowns and their accompanied economical losses, a number of related standards (IEEE-1547 in the USA and IEC61727 in Europe) have long been in force to govern the amount of harmonics that can be injected into utility grids.

For critical missions, it is also common for custom-power conditioners like active

power filters (APF) and uninterruptible power supplies (UPS) to be installed at the customer end for a fail-safe solution, which may lead to comparatively high cost. A more attractive alternative is to embed power conditioning within renewable grid converters, which are gradually becoming basic necessities because of environmental concerns and growing demands for energy. Such additional functionality might help to encourage faster adoption of renewable energy, which now has even more attractive advantages.

With such impressive and practical developments, it is obvious that power electronics has many important roles to play in the modern world. These roles, whether as power quality enhancers, renewable energy conditioners or industrial drivers, are made possible through appropriate control techniques. Development of control techniques is thus an important pillar supporting research in power electronics with many inventions over the years. Among the common objectives for controller design, one of them is the precise control of current, which represents system power for a strong network with firm voltage. It can be achieved in the stationary or synchronous frame with the latter further divided into the fundamental and harmonic synchronous frames. Examples in the stationary reference frame include the dead beat control [1], [2], hysteresis control [3], [4], and proportional resonant (PR) control [5]-[7], and examples in the fundamental reference frame include linear proportional integral (PI) control [8]-[10] and sliding mode control [11], [12].

Each control method has its own unique features. Some commonly cited references can be found in [13], [14], where hysteresis controller is stated to have better performance than others in both stationary and synchronous frames. However, the hysteresis control is known to suffer from unwanted interaction between phases, and has a variable switching frequency. For a fixed switching frequency, a linear PI controller in the stationary frame is the simplest to implement, but usually has accompanied amplitude and phase tracking errors. The only way to overcome this drawback is to transform the controlled variables to dc quantities in the synchronous

reference frame before applying PI control.

Although effective, compensation of harmonics using the synchronous PI scheme is still extremely complex with multiple harmonic reference frames involved. These complexities translate to higher computational burden, which may lead to degradation in both steady-state and transient responses. Other existing control schemes also have their own shortcomings, which so far have not been promptly addressed. Improvements are therefore possible even though current control of power converters is quite a mature area.

While designing the controller, it is important to consider the filter types at the converter input and output ports since they affect the overall system dynamics. Earlier efforts have mostly focused on a simple inductive (L) filter for current control, which might not be too relevant because of the growing interest in the inductor-capacitor-inductor (LCL) filter. Being a higher third-order filter, the LCL arrangement provides much better harmonic attenuation, while using smaller passive elements. It is thus more suitable for higher power conversion systems, and has already been widely used in wind farms of over hundreds of kilowatts [15]-[17]. Unfortunately, an LCL-filter can trigger stability problems usually linked to higher-order systems. The underlying reason is related to resonance. When it happens, it causes the system to appear as zero or very low impedance.

This stability concern is further complicated by the availability of two possible current feedback variables. Unlike the L filter whose current is the only variable for sensing, current feedback with LCL-filter is more flexible with three options for selection, namely grid current sensing, converter current sensing or computing their weighted sum from a re-organized LCCL arrangement studied in [18]. In [19], grid current feedback is recommended, after it was shown through root locus analysis to be slightly more stable than converter current feedback. An optimized design algorithm for LCL-filter was proposed in [20], based on which a system can be stabilized at certain

switching frequencies even without damping. However, the results in these references show low-order harmonic distortions in their line currents. Even more confusing is the findings by other researchers, who had verified that excellent steady-state and transient performances can be obtained by converter current feedback with some degrees of damping introduced [15]. The question about which type of current feedback control is truly more stable is therefore left unanswered.

With these challenges to explore and the growing importance of power electronics, the theme of this thesis is firmly set on the design of advanced control schemes for commonly used three-phase voltage-source converters (VSCs). The same theories can equally be applied to current-source converters (CSCs) based on duality between the two classes of converters. For more stringent applications, LCL filter is explicitly considered with its accompanied control schemes designed accordingly. Issues like feedback variable selection, stability, damping, harmonic compensation, disturbance rejection and control simplification for industry relevance are promptly discussed, while designing the new control schemes and generalized design methodologies. The relevant contributions to knowledge are now elaborated as follows.

1.2 Major Contributions of the Thesis

A number of original contributions, which have been achieved throughout the course of research, are explained as follows:

1.2.1 Design of Complex-Vector Repetitive Current Control Schemes

A complex-vector repetitive control scheme has been proposed for grid converters to achieve high current tracking precision and good disturbance rejection that are comparatively better than existing schemes. The proposed control scheme was originally based on a mixed combination of stationary and synchronous frames, which could still be complex depending on the processor or microcontroller chosen for implementation. For an even simpler implementation, mathematical derivation was

performed to arrive at an alternative that could fully be implemented in the stationary frame, and hence avoiding the computationally intensive frame transformation. Whether in the mixed or full stationary frame, the proposed control scheme is generally less demanding in hardware requirements since it requires simple arithmetic and only a small amount of memory for storing delayed control variables.

1.2.2 Design of Repetitive Control Schemes for UPS Applications

Based on the proposed complex-vector repetitive control and other existing methods, a number of repetitive control schemes have been proposed for UPS applications, covering both single and double-loop layouts. Although the bulk of this thesis is about current control, repetitive voltage control should not be skipped because of its originality and relevance to the huge power supply industry. Again, the main control building blocks assembled are memory and simple transfer functions formulated with either no or one control zero for cancelling the plant pole. The presented schemes have high compensating gains only at those typical harmonic frequencies, and are therefore more robust and less sensitive to implementation noise. Applying them to UPS application then results in an output voltage that is less affected by load types (nonlinear and / or unbalanced) and load dynamics.

1.2.3 Investigation of Inherent Damping Characteristics of LCL-Filters

A generalized design methodology for an LCL-filter in grid-tied inverter has been proposed. The knowledge discovered is that there is an inherent damping term embedded in the feedback loop when converter current is used for control. Such internal damping can be brought out for use by selecting the grid- and converter-side inductors appropriately. Upon doing so, resonances are damped naturally by feeding back the converter-side current without requirement for an external state observer or active and passive damping. When exposed to tough design conditions, the damping information contained in the converter-side current can also be extracted via a second-order notch filter, before using it for further tuning purposes.

1.2.4 Design of LCL-Filter-Based Shunt Active Power Filter Systems

The design methodology described in Section 1.2.3 has been extended to shunt active power filters (SAPF) with an LCL-filter added at the output. The resulting SAPF has improved switching harmonic suppression and a lower total inductance. The latter is especially important for SAPF, whose current must have high slew rate for tracking the desired harmonic reference. Requirements for SAPF are thus more demanding with a number of them now clarified in the thesis. These requirements are closely related to the selection of LCL-filter parameters, control bandwidth design, filter damping and simplified implementation.

1.2.5 Improved Regulation of One-Cycle Controlled Active Rectifiers

Until now, only linear control is considered. For even better dynamics, nonlinear control is deemed as more appropriate. No doubt different types of nonlinear control are available, but in this thesis, only one-cycle control (OCC) is considered because of its simplicity and hence ease of realization in practice. OCC nonetheless has some performance limitations that are not yet identified and solved. These challenges are discussed in the thesis with an improved OCC scheme eventually proposed for power converter control. Its performance has been verified with a three-phase active rectifier, whose requirements are more demanding on OCC especially at high power rating and low switching frequency.

The proposed system has been shown to solve even-order sideband harmonic problems faced by the traditional OCC scheme via a double-edge integration strategy. Introducing the LCL-filter has also helped to bring down costs, while yet compromising system stability because of two designed damping techniques added for nullifying the LCL resonance. Comparative studies have been performed to show that the improved OCC scheme has better conversion efficiency and lower total harmonic distortion (THD). Consideration is extended to non-ideal ac input for three-phase active rectifier, which may happen in weak ac power systems. Mathematical analysis

has demonstrated how harmonics at the input and output sides of the rectifier can be computed and then reduced using a simple compensation scheme added on to the main OCC core. Analog implementation of the overall OCC scheme has also been discussed to show that simplicity of the original OCC scheme is preserved.

1.3 Organization of the Thesis

The thesis comprises nine chapters organized as follows:

Chapter 1 introduces the background and motivation of this work as well as summarizing all original contributions documented in the thesis.

Chapter 2 reviews existing control techniques for three-phase PWM converters. It discusses the essential relationships among PI, PR and repetitive control schemes and elaborates on the basis of OCC. Recent related developments are also discussed with their benefits and limitations identified. The knowledge gained helps in the understanding of new control schemes and generalized design procedures proposed from Chapter 3 onwards.

Chapter 3 introduces the concept of complex-vector PI control from which the complex-vector repetitive current control scheme is proposed and illustrated on a grid-tied inverter. Mathematical analysis is presented for two equivalent variants in either the mixed synchronous-stationary or fully stationary frame. Both share the same theoretical transfer function, but differ in hardware complexity.

Chapter 4 extends the analysis from Chapter 3 with a double-loop control structure presented for voltage control of a power converter with an output LC filter. The presented scheme is compared with existing alternatives to clearly identify their respective steady-state and dynamic characteristics.

Chapter 5 considers LCL-filter when added to the output of a power converter. Mathematical model of the filter is established, before using it to identify inherent damping characteristics. Two current control schemes are then presented with resonance damping considered.

Chapter 6 extends LCL-filtering consideration to shunt active power filters (SAPF) with a discussion of the design, control and implementation issues. A generalized design procedure is subsequently presented and tested with an analytical design example.

Chapter 7 adds an LCL-filter to an OCC-controlled active rectifier before proposing double-edge integration scheme for solving even-order harmonic problems. Comparative studies show that lower THD and higher conversion efficiency can be achieved by the proposed system.

Chapter 8 improves on Chapter 7 with the performance of active rectifier examined under non-ideal operating conditions. Mathematical proof identifies the dominant system harmonics caused by distorted ac input voltages, from which an improved OCC scheme is presented for minimizing their influences without adding hardware.

Chapter 9 concludes research findings presented in the thesis and suggests some prospective research topics for future investigation.

Chapter 2 Existing Control Techniques for Three-Phase PWM Converters

2.1 Introduction

With rapid growth of energy demand and increasing concern about environmental sustainability, renewable energy sources, like photovoltaic (PV), hydro, biomass and wind power are gaining momentum in place of traditional fossil fuels. Three-phase PWM converters are used to transfer the generated power to the utility grid or loads. To realize this grid-tying function, power converters must operate with closed-loop control so as to follow certain commanded references. Design of proper control schemes is therefore crucial and has in fact been a relevant topic for many power electronic applications in addition to grid-interfacing.

Various control schemes for three-phase PWM converters have been proposed with each claiming some forms of improvement. This chapter briefly reviews fundamental control knowledge and introduces the control schemes that are popular and relevant to the research contributions of this thesis. The essential relationships among proportional-integral (PI), proportional-resonant (PR) and repetitive control are introduced. The basis of one-cycle control (OCC) and its recent developments are also elaborated. Material presented in this chapter is therefore not exhaustive, but would definitely helps with understanding of concepts proposed in subsequent chapters.

2.2 Basic Concepts about Power Converter Control

In this section, some basic concepts related to power converter control are discussed before reviewing existing control schemes for three-phase PWM converters. Understanding of these basic concepts helps greatly with control design targeted at

power conversion systems.

2.2.1 Control Objectives

Fig. 2-1 shows the basic control block diagram applicable to a three-phase PWM converter. The control objective is to force the converter current to follow some predefined reference, which is either obtained from an outer voltage loop or computed from a demanded power. The instantaneous converter current is measured and subtracted from its reference before their error is forwarded to a designed controller to achieve the control objective. The controller produces the required gating signals either implicitly or explicitly using an external modulator. The gating signals are then channeled to the gates of the switching devices for driving the converter. The generated converter current should be able to track its reference as close, and as quickly as possible, and this is usually regarded as one of the most important criteria to judge the performance of designed current controllers. Besides this point, the controller should also be able to suppress system inrush current in the startup of power conversion, which is typically caused by charging of bulky dc side electrolytic capacitors. Moreover, some “green mode” power supplies need to comply with very critical efficiency requirements under light load conditions, and in this case, burst mode operation has to be considered in the controller design to save power losses and to satisfy such requirement. The latter two factors are beyond the scope of this thesis and will not be discussed here.

Fig. 2-1. General control block diagram of a three-phase PWM converter.

As mentioned above, the converter is operating based on switching actions, and its immediate output is pulsating, and hence not possible to produce a smooth continuous current. Even upon filtered, the converter current would still contain harmonics or ripples, whose amount is frequently reflected by single-term performance indicators. One commonly used indicator is the total harmonic distortion (THD), whose expression is written as:

$$THD_{(i)} = \frac{\sqrt{i_{(2)}^2 + i_{(3)}^2 + i_{(4)}^2 + \dots + i_{(h)}^2}}{i_{(1)}} \quad (2.1)$$

where subscript h denotes the order of each harmonic current.

2.2.2 Switching Frequency

Switching frequency represents the rate at which semiconductor switches are commutated within the converter. A higher switching frequency leads to lower current ripple, but increases the overall system losses. A compromise therefore exists, and would usually depend on the system power rating. For higher power systems considered in this work, switching frequency in the range of 5 to 10 kHz is appropriate and is therefore chosen for design and experimentation.

It should further be noted that the switching frequency is not necessarily constant, and it can be varied either intentionally to get a spread spectrum or unintentionally due to the control scheme. An example for the latter is hysteresis current control, whose switching frequency depends heavily on system parameters and might therefore cause electromagnetic compatibility (EMC) problems [13]. Filter design for hysteretically controlled converter might also be difficult even though its dynamic response is fast and implementation is simple.

2.2.3 Limits of DC-Link Voltage

Voltage output of a PWM converter is obtained by switching each phase to two discrete dc-link voltage levels. Multilevel converters are not considered in this thesis,

but if necessary, the developed control schemes can also be extended to them with simple manipulation of their PWM schemes. Regardless of the number of levels, the dc-link voltage must be higher than the line voltage amplitude of the grid or back electromotive force (back-EMF) in order for the converter to have full control over its output. This means modulation index m defined as in (2.2) should always be limited to less than or equal to 1.15 assuming that triplen offsets have been added for modulation.

$$m = 2\hat{v}_{a1} / V_{dc} \leq 1.15 \quad (2.2)$$

where $\hat{v}_{a1}$ represents the peak fundamental voltage of phase a , and V_{dc} represents the dc-link voltage.

Index m can of course rise above 1.15 to produce a larger fundamental voltage, but its modulation would no longer be linear with sizable amount of low-order harmonics produced. This scenario is referred to as over-modulation, and should generally be avoided for control design because of prominent harmonic influences. On the other extreme, m should not be too low since switching harmonics increase with the decrease of m [26]-[29]. A compromise is roughly recommended as between 0.8 and 0.9 for nominal load conditions.

2.2.4 Effect of Phase Interference

If the neutral point N of the three-phase ac source in Fig. 2-1 is connected to the midpoint M of the power converter, a three-phase four-wire system is formed. Each phase of the converter would then be fully independent, allowing zero-sequence current to flow and return through the neutral line. On the contrary, such independence does not exist for three-phase three-wire system without the neutral connection. Current flow in a three-wire system is determined by the states of all phase legs, and not solely by the state of the corresponding phase leg. When that happens, the relevant current controller is said to experience phase interference or dependency, which can have damaging effects like those high frequency limit cycles experienced by hysteresis control [21], [23].

Phase dependency is not always detrimental, and in fact has an important advantage linked to the addition of triplen offsets during modulation to lengthen the linear modulation range by 15% [30]-[32]. More explanations on it can be found in [33]-[35] and [36]-[39], where space vector and discontinuous modulations are respectively introduced. The common principle shared by these modulation schemes is that their added triplen offsets appear only in their phase-leg voltages, and not their fundamental output currents because of the absence of a zero-sequence path. Their output current ripples would however be different because of variations introduced to their commutation state sequences.

2.2.5 Reference Frame Transformations

As mentioned in Chapter 1, for a balanced three-phase three-wire power system, the control variables are normally transformed from abc frame to dq frame so that they become DC quantities. Simplified calculations can then be carried out on these imaginary DC quantities before performing the inverse transformation to recover the real three-phase AC results. In many literatures, such transformations served as the fundamental knowledge to design various controllers, either in the synchronous reference frame or stationary frame, for achieving accurate power flow control, as well as complicated system harmonic compensation. Because of its importance, the mechanism of the associated frame transformation will also be introduced in this section for ease of understanding the contents presented in the following chapters.

Usually, the transformation from abc frame to dq frame is performed in two steps, first from abc to $\alpha\beta$ to create an orthogonal system, and then from $\alpha\beta$ to dq to make the system to be time invariant. The principles of these two transformations are depicted by Fig. 2-2(a) and Fig. 2-2(b), respectively. They can also be mathematically written as (2.3) and (2.4), respectively.

Fig. 2-2. Reference frame transformations from (a) *abc* to $\alpha\beta$ frame and (b) $\alpha\beta$ to dq frame.

$$\begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad (2.3)$$

$$\begin{bmatrix} S_d \\ S_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} \quad (2.4)$$

where S is the transformed signal that can be either the converter voltage or current,

and θ is the angle difference between dq and $\alpha\beta$ reference frames, and the coefficient $\sqrt{\frac{2}{3}}$ on the right-hand side of (2.3) is to keep power balanced during frame transformations.

In order to reconstruct the reference signals that are required for PWM generation, inverse frame transformations can be simply obtained by taking the transpose of the matrices shown in the above equations.

2.3 Linear Controllers

A linear controller normally consists of a current regulator for tracking its reference and a modulator for generating gating signals. The latter can be any existing carrier-based or space vector modulator with a constant switching frequency and a well-defined spectrum. Modulating signal to the modulator comes from the current regulator, which presently has many options. This chapter concentrates only on those related to the thesis.

2.3.1 PI Controllers

Stationary frame PI controllers, also known as ramp comparison controllers, use three independent compensators to produce the required modulating commands. Each compensator has a proportional and an integral gain to set the control bandwidth and steady-state tracking errors, respectively. The latter should preferably be zero, but cannot be achieved because of the finite integral term at non-zero frequencies. A simple remedy is obviously to use larger gains to push down the errors, but doing so moves the system closer to its stability limit, and hence should be avoided. Other recommendations include the use of an additional phase-locked loop (PLL) [40] and voltage feed-forward correction [41], [42], whose effects are not as good as performing PI control in the synchronous frame.

Fig. 2-3. Synchronous reference frame PI control with dq cross-coupling term decoupled.

Unlike the stationary frame, the synchronous frame rotates at the same angular frequency as the control variables, hence making them appear like dc quantities named as d and q components. PI control is then suitable since its infinite integral term at dc would easily force the steady-state d and q errors to zero. Unfortunately, due to the presence of system inductance L , cross-coupling between d and q components exist, whose impact is a longer transient duration. To decouple these components, the scheme shown in Fig. 2-3 can be implemented, where two diagonal L dependent blocks are added. Presence of these blocks however causes the controller to be dependent on system parameters, whose values may vary widely [5], [6].

Adding decoupling blocks, as shown in Fig. 2-3 may, also be viewed as moving the two complex conjugate poles of the system to the real axis, so that they can be cancelled out by the PI controller. Instead of “forward” moving the plant poles, “inverse” shifting of the PI zeros can equally be performed to arrive at the complex-vector (CV) PI controller [43], [44], whose effect is the same as that shown in Fig. 2-3 since they share the same theoretical basis.

2.3.2 PR Controllers

Avoiding frame transformation, PR controller in the stationary frame is an attractive alternative introduced in [5] for ac current regulation. As shown in Fig. 2-4, this concept is simple and simply involves placing an infinite resonant peak at the frequency of regulation. The infinite gain then forces the steady-state error to zero at the frequency of interest. This concept does sound like the inverse of synchronous frame PI since it places resonant peak of controller at signal frequency, while synchronous PI does the reverse of placing signal frequency at the resonant or integral peak. Such inverse equivalence has already been proven in [6], where mathematical procedure has shown how the PR controller can be derived from the synchronous frame PI controller. Because of this relationship, the resonant part of the PR controller

(a)

(b)

Fig. 2-4. (a) The essence of a PR controller and (b) its frequency domain Bode plot.

can be regarded as an ac generalized integrator [45], whose response is different from the controller proposed in [46]. The controller in [46], [47] is in fact more unstable since it creates a 90° phase lag at the frequency of interest even though it has the same denominator in its transfer function.

Another merit of the PR controller is its ability to simultaneously compensate for positive and negative sequence components in an unbalanced three-phase system. To realize the same function using PI controller, the control variables must first be

(a)

(b)

Fig. 2-5. Resonant banks for SHC implemented in the (a) stationary reference frame and (b) synchronous reference frame.

transformed to the positive and negative sequence frames before being processed by PI compensators in the individual frames. Such multi-frame transformation is definitely more complicated.

Because of its simplicity, more functions can be added to the PR controller, while not stressing the digital processor or microcontroller used to implement it. One popular attempt is to connect multiple resonant terms in parallel to realize selective harmonic compensation (SHC) [48]. A diagram showing SHC is given in Fig. 2-5(a) with its transfer function written as:

$$G_{h1(s)} = \sum_{h=3,5,7,\dots} \frac{2K_{ih}s}{s^2 + (h\omega_o)^2} \quad (2.5)$$

In (2.5), h represents the odd harmonic order only since even harmonics are usually absent in a typical power system. Each value of h is also written to have its own resonant gain K_{ih} , which can independently be tuned to produce different compensation performance. The controller thus obtained will not affect the dynamics of the fundamental PR controller so long as the highest harmonic frequency considered falls within the system control bandwidth. This certainly is the case since each resonant peak is limited to only a very narrow frequency range.

In addition to its stationary frame variants, PR controller can be implemented in the synchronous frame to achieve compensation of multiple harmonics with reduced computational efforts. A good example for illustration is to consider the fifth negative-sequence and seventh positive-sequence harmonics typically found in a three-phase three-wire system. These harmonics, when transformed to the fundamental synchronous frame, appear as sixth positive and negative-sequence harmonics. That means a single resonant controller tuned at the sixth harmonic frequency and placed in the fundamental synchronous frame can compensate for the fifth negative-sequence and seventh positive-sequence harmonics in the stationary frame. Other harmonics like the eleventh negative-sequence and thirteenth positive-sequence in the stationary frame

can similarly be compensated by a twelfth resonant term in the fundamental synchronous frame. That then leads to the following SHC expression in the fundamental synchronous frame for compensating even more $(6h \pm 1)$ harmonics.

$$G_{h2(s)} = \sum_{h=1,2,3,\dots} \frac{2K_{ih}s}{s^2 + (6h\omega_o)^2} \quad (2.6)$$

A block diagram illustration of (2.6) is shown in Fig. 2-5(b), which when implemented for three-phase three-wire systems, results in all typical harmonics being compensated. Surely, (2.5) can be used in place, but its computational requirement is two times more since a resonant term is needed for each harmonic frequency. Equation (2.6) is therefore preferred for three-phase three-wire systems if non-characteristic harmonics are absent.

So far, the resonant terms considered have not taken into consideration the decoupling blocks drawn in Fig. 2-3. This is generally fine for standard 50 or 60 Hz since their influences are quite small at those frequencies. For systems with higher order harmonics to compensate or in 400-Hz aircraft power systems, the decoupling term can no longer be ignored. Taking them into consideration, the CV concept is discussed in [48] for modifying the resonant controller after studying the plant model. The modified resonant controller can then neatly cancel out the complex poles of the plant at the chosen harmonic frequencies. Expected outcome would be an improvement in the closed-loop response, as verified by [48]. Also verified in [48] is the ability of the CV resonant controller in compensating for the highest 37th harmonics, while the conventional PR controller can only compensate for the 19th harmonic.

2.3.3 Repetitive Controllers

As discussed in the above section, SHC can be accomplished by cascading multiple resonant controllers in parallel. No doubt, they can function well under most situations, but as the compensation criteria become more stringent like more high frequency

components needed to be attenuated, performance of the basic transfer functions degrades gradually, while their computational burden increases steadily.

Instead of using direct resonant terms, an indirect simplified approach for realizing SHC is to use the repetitive control theory, which is developed from the internal model principle [49]. Conventional repetitive control with only a single positive feedback delay has already been discussed in [50]-[53], whose aim is to compensate for all harmonics found in a UPS subject only to practical implementation constrains. The same repetitive control scheme has subsequently been applied to other common power electronics applications, like APF and DC / DC boost converter, as described in [54], [55]. Other developments can be found in [56] and [57]. In [56], a modified adaptive control scheme has been proposed for achieving better steady-state performance when subject to external disturbances and plant uncertainties. Complementing, [57] merges repetitive and deadbeat control theories to arrive at a faster transient response.

In spite of their differences, those described repetitive schemes have the same positive

(a)

(b)

Fig. 2-6. Hybrid repetitive control with (a) positive and (b) negative feedback and feed-forward paths.

feedback of signal, which may be unfavorable at times because of the likely amplification of noise. To minimize this likelihood, negative feedback repetitive control scheme is recommended as an alternative [58], [59]. Instead of introducing high gains at all harmonics, negative feedback scheme produces high gains only at odd harmonics, which in principle are enough for compensating typical load harmonics. No amplifying of noise at even harmonics is possible since the controller gains there are all zero. Implementation wise, negative feedback scheme may have a slight advantage since its delay time is half of the positive feedback scheme, which in practice translates to a smaller memory requirement for storing delayed data if the same signal resolution is enforced for both schemes.

Other than negative feedback, improvements like adding a single feed-forward delay path [60] or phase lead compensation [61] to the original feedback structure have been proposed with their common objective being to enhance overall tracking accuracy and stability. More specifically, [60] introduces two alternative repetitive control schemes with their control block diagrams shown in Fig. 2-6. This figure clearly shows that the control schemes can be viewed as the cascaded connection of a delayed feedback path and a delayed feed-forward path that represent the classical repetitive and Posicast control [65]-[67], respectively. Mathematical analysis in [55], [60], [62] has already shown their close linkages to the resonant controller with their transfer functions derived as (2.7) for Fig. 2-6(a) and (2.8) for Fig. 2-6(b).

$$\frac{Y(s)}{E(s)} = \frac{1 + e^{-sT_d}}{1 - e^{-sT_d}} = \frac{2}{T_d} \left\{ \frac{1}{s} + \sum_{h=1}^{\infty} \frac{2s}{s^2 + (h\omega_o)^2} \right\} \quad (2.7)$$

$$\frac{Y(s)}{E(s)} = \frac{1 - e^{-sT_d/2}}{1 + e^{-sT_d/2}} = \frac{4}{T_d} \left\{ \sum_{h=1}^{\infty} \frac{2s}{s^2 + ((2h-1)\omega_o)^2} \right\} \quad (2.8)$$

Apparently, (2.7) and (2.8) are multiple harmonic compensators that can be used for eliminating all harmonics and odd harmonics, respectively. The extent of computation needed would be intensive if actual multiple resonant compensators are used. Fortunately, with the schemes presented in Fig. 2-6, only a single delay block is needed

for digital implementation. These hybrid repetitive control schemes are therefore attractive and promising alternatives for industry applications.

More recently, the control scheme shown in Fig. 2-6(a) is smartly shifted to the synchronous reference frame with its delay time shortened to one sixth of the fundamental period ($T_d/6$) [68]. The resulting transfer function is expressed as (2.9), which obviously has a term that looks close to (2.6). This implies that the developed repetitive controller is capable of compensating typical $(6h \pm 1)$ harmonics found in three-phase three-wire systems, while yet avoiding the burden of implementing (2.6). This certainly is an advantage shared by most, if not all, repetitive schemes.

$$\frac{Y(s)}{E(s)} = \frac{1 + e^{-sT_d/6}}{1 - e^{-sT_d/6}} = \frac{2}{T_d} \left\{ \frac{1}{s} + \sum_{h=1}^{\infty} \frac{2s}{s^2 + (6h\omega_o)^2} \right\} \quad (2.9)$$

Equation (2.9) can further be transformed to the stationary frame according to [6] with the same performance preserved. This latest controller, together with all other repetitive controllers, would still face the same problem of performance deterioration at high compensating frequencies. The reason being mismatched pole / zero cancellation of the system plant. This deficiency will lessen the attractiveness of the repetitive control schemes, which fortunately can be solved by adopting the approach contributed in Chapter 3.

2.4 Nonlinear Controllers

For nonlinear current controllers, the on / off states of semiconductor devices in power converters are usually determined by some predefined switching rules and / or logic operations, instead of using modulators. Their dynamics are also much faster because of the absence of bandwidth limits in their control loops. Nonlinear control is therefore at times popular, examples being OCC, neutral networks control, fuzzy logic control and hysteresis control [13]. This section focuses only on OCC because of its proven popularity in commercial power electronic products [69]-[91] and relevance to this

Fig. 2-7. One-cycle control of a buck converter.

thesis.

OCC is often quoted as a large-signal nonlinear control method originally developed for controlling DC / DC power converters. Its basic operating principle, as shown in Fig. 2-7, is to control the switching duty ratio such that integration of a chosen control variable is exactly equal or proportional to its reference in every switching cycle [69], [70]. Due to this precise cycle by cycle regulation, OCC features instant reference tracking, good rejection of source side perturbations and a constant switching frequency. Stability of OCC has been discussed in [70], where it was proven that OCC is globally stable if its chosen control variable is independent of its input signal. For a complex system whose input to its switch is a function of other state variables, OCC can still be stable and produce zero tracking error in both steady and transient states. That however is subjected to certain duty ratio limitations.

Extending its application to AC / DC power converters, OCC is subsequently adopted for single-phase active power factor correction (PFC) in continuous conduction mode (CCM). Relevant control objectives defined are unity power factor operation and sinusoidal input current waveforms even with a front-end diode rectifier bridge [71]-[73]. Unlike linear controllers, OCC achieves these objectives without using any analog multiplier and ac line sensing for reference current generation. It also does not

need a fixed oscillator commonly used for saw-tooth ramp generation. Instead, in OCC, its output error from the differential amplifier is integrated over each clock cycle to generate a variable slope ramp, whose amplitude depends on its loading level.

This ramp signal is then synthesized with the error voltage and current sensing signal to produce the final gating pulses. With these unique features of OCC, the designed PFC circuit uses less external passive components for control implementation and electromagnetic interference (EMI) filtering. Undoubtedly, this translates to a smaller footprint, and hence higher power density. To improve on OCC performance for PFC control, its discontinuous conduction mode (DCM) was investigated in [74], from which a hybrid control technique was derived for achieving smooth transition between CCM and DCM within one line cycle. Again, this hybrid scheme preserves unity power factor, large-signal stability and noise immunity with only very few hardware additions.

Based on the volt-sec balancing equation, OCC can also be applied to three-phase boost rectifiers for PFC control [75]-[78]. Bipolar operation of a typical boost rectifier has in fact been discussed in [75], where the converter output current is shown to follow the ac input voltage without using a PLL circuit for reference current generation. An alternative vector operation of OCC controlled three-phase PFC rectifier has also been discussed in [76]. For that method, the grid three-phase voltages per fundamental cycle are first divided into six sextants. Depending on the sextant that the rectifier is presently residing in, a phase-leg is always clamped to a terminal of the dc-link, while the other two phase-legs modulate their switches between two terminals of the same dc-link. Since one phase-leg is always clamped, switching losses of this method is greatly reduced.

Instead of only a single converter, OCC in vector mode has also been extended to parallel operation of multiple converters in order to meet higher power rating. When applied directly, OCC undesirably results in the converters appearing as low

impedance closed-loop paths for circulating current to flow [78]. The outcomes are output current unbalance and excessive power losses. Moreover, the transition time of these two inverters may not be synchronized, and it may probably cause a current step change at each region-crossing point. Fortunately, for bipolar parallel OCC inverters, this circulating current is naturally eliminated as there will be less likely to form up this freewheeling loop. To limit the circulating current, a hybrid OCC architecture that combines vector operation and bipolar operation is proposed in [78], [79]. That method simply uses bipolar mode at the start of each sextant before transiting to vector mode. To a great extent, circulating current is reduced by such transition.

Other efforts on OCC cover its stability enhancement, harmonic and unbalance compensation for three-phase power converters. One notable improvement is documented in [80]-[82], where a fictitious feedback term is explicitly introduced to the OCC core for altering the slope of a ramp waveform. As a consequence, the modified OCC can regulate the system real and reactive power flow freely without entering unstable zones. Another improvement is shown in [83]-[90], where the harmonic compensation ability of OCC is demonstrated with APF and UPS systems. More recently, ac input voltage unbalance, but not distortion, was taken into consideration in [91]. The results there show that OCC is capable of producing sinusoidal input currents, which unfortunately are unbalanced. In addition, a large capacitor is needed to reduce harmonics at the dc-link, and hence preventing them from distorting the input currents. Such passive solutions are not cost effective and might not have brought out the full advantages of OCC under unbalanced and distorted input conditions. Further discussion about this topic can be found in Chapter 8.

2.5 Summary

This chapter reviews some of the existing control techniques that are popularly employed for regulation of three-phase PWM power converters. Depending on the nature of the control algorithms, they are classified as either linear or nonlinear

controllers. For linear controllers, an insightful review is given to establish basic understanding of the relationships among PI, PR and repetitive controllers, before their advanced variants are described. For nonlinear controllers, basic OCC operating principles are explained before related recent developments are elaborated. While describing the schemes, challenges presently unsolved are also identified, which when summarized, represent problems linked to high frequency harmonic distortions, LCL filters and non-ideal supply voltage conditions. To a great extent, these challenges have already been solved with relevant findings documented from Chapter 3 onwards.

Chapter 3 Complex-Vector Repetitive Control of Power Converters

3.1 Introduction

As discussed previously, repetitive control schemes have gained popularity in power electronic applications because of their simplicity and impressive harmonic rejection. Nevertheless, as the order of harmonics to compensate increases, performances of most repetitive controllers will deteriorate, causing the converter current to stop following its reference closely due to mismatches in pole-zero cancellation. In [92], [93] an attempt to transform individual harmonics to their respective harmonic frames is demonstrated so as to achieve accurate pole-zero cancellation. Although working effectively, this method causes excessive computational burden as the number of harmonics compensated increases. Low pass filter (LPF) introduced in each harmonic frame also slows down the dynamic response of the overall system.

To resolve these complications while preserving the simplicity of repetitive control, this chapter first introduces the concept of complex-vector (CV) PI controllers, and illustrates its essential differences as compared to the traditional PI controllers. After understanding its basic operating principles, a CV repetitive control scheme is proposed, which can either be formulated in the stationary frame or in a mixed combination of stationary and synchronous frames (referred to as mixed frame hereon). The designed controller uses a more precise transfer function for compensating the frequency under consideration and can physically be implemented using simple mathematical functions with a small amount of memory space for storing delayed control variables.

Moreover, its control characteristics are tuned to match harmonics produced by most non-linear loads, hence giving rise to a less noise-sensitive scheme with no raised computational burden for compensating more harmonics. When used with a grid-connected converter, its inherent ability to filter off grid disturbances from distorting the generated current is also appreciated with more accurate control of active and reactive power flows expected. These steady-state control features are attractive which, together with the fast dynamic response of the controller, are tested physically in the laboratory using a digitally controlled experimental setup. The results are presented at the end of this chapter for validation.

3.2 Complex-Vector PI Control in the Synchronous Frame

In principle, the proposed CV repetitive control is designed based on the analytical concept of CV-PI control discussed in [43]. Using the simple example described in [43], where the control scheme is used for controlling a power converter connected to a resistive-inductive (RL) load, the differences between the traditional PI and CV-PI controllers in the synchronous frame are clarified first before extending the latter to give the proposed CV repetitive control scheme. Beginning with the overview block diagram shown in Fig. 3-1 (ignoring $V_{EMF}(s)$ for the time being), where the complex-vector notation $l_{qd} = l_q - jl_d$ has been used for integrating the q and d variables together to form a single variable, the feed-forward transfer expression for the control path is written as:

Synchronous Frame

$$G(s) = H_{syn}(s) \times 1/\{sL + (R + j\omega_o L)\} \quad (3.1)$$

pole at $s = -(R/L) + j\omega_o$ is noted in the second term of (3.1), whose imaginary term explicitly represents the phase coupling introduced by the frame transformation. For a non-zero transformation frequency ω_o , this complex pole is not strictly cancelled by the real zero introduced by the traditional PI controller, whose transfer function and

Fig. 3-1. Simplified control diagram of CV-PI control with an external load.

zero expression are respectively written as $H_{Syn1}(s) = K_p + K_i/s$ and $s = -K_i/K_p$, where K_p and K_i represent the proportional and integral gains. Although partial neutralization can still be attained for reasonably small ω_o , the mismatch in pole-zero cancellation is expected to eventually cause the controller to lose control of the plant as ω_o increases progressively towards the designed controller bandwidth. When that happens, the dominant complex pole of the plant then determines the system oscillatory response, which surely is an unacceptable scenario.

The traditional PI transfer function is therefore not an ideal base entity to rely on for more advanced control development. Instead, for high frequency tracking and disturbance rejection, an alternative CV-PI transfer function is recommended, whose transfer function is written as $H_{Syn2}(s) = K_p + (K_i + jK_p\omega_o)/s$. By explicitly writing down the numerator of $H_{Syn2}(s)$, the zero introduced by controller is undoubtedly determined as $s = -(K_i/K_p + j\omega_o)$, where an imaginary $j\omega_o$ term is added to form a complex root. This complex zero can then be tuned to cancel the plant pole along the feed-forward path shown in Fig. 3-1 by setting $K_i/K_p = R/L$, after setting K_p to produce the desired bandwidth. The final system response is then solely determined by the controller, regardless of the specific frequency used for the synchronous frame transformation.

Although the analysis is performed on an RL load, its application to loads with a back-emf ($V_{EMF}(s)$) shown in Fig. 3-1) is also possible after the influences introduced

by the back-emf are decoupled by feeding forward either its measured or predicted value. The simplified load then resembles an RL load, implying that perfect pole-zero cancellation can still be achieved without much difficulty. Even without back-emf feed-forward (for cases where voltage sensing is not performed due to likely cost constraint), the CV-PI controller is still expected to perform well with only minor deviation from its ideal operating condition expected [43]. It is therefore viewed as the preferred transfer function in the synchronous frame to begin with, while developing the repetitive control scheme presented below.

3.3 Complex-Vector Repetitive Control in a Mixed Reference Frame

As per the transformation of synchronous PI to stationary PR scheme mentioned in Chapter 2, the CV-PI control scheme can also be transformed to the stationary frame by applying the following mathematical frequency shifting operation [6]:

Stationary Frame

$$H_{Stat2}(s) = \frac{1}{2} \left[H_{Syn2}^+(s - j\omega_o) + H_{Syn2}^-(s + j\omega_o) \right] \quad (3.2)$$

where $H_{Syn2}^+(s) = K_p + (K_i + jK_p\omega_o)/s$ and $H_{Syn2}^-(s) = K_p + (K_i - jK_p\omega_o)/s$

represent the positive and negative-sequence versions of $H_{Syn2}(s)$. Substituting H_{Syn2}^+ and H_{Syn2}^- into (3.2) then gives rise to the CV-PR transfer function in (3.3) used for ensuring zero steady-state fundamental tracking error in the stationary frame. In essence, (3.3) represents the optimal transfer function used for designing the CV repetitive control scheme, whose operating principles are discussed shortly. But before doing that, the PR transfer function derived from the traditional PI scheme is also stated in (3.4) for comparison with (3.3), where a noted common feature is that they have infinite gains at the resonant frequencies of $\pm\omega_o$. That means both controllers can simultaneously compensate for positive and negative-sequence components, even though their PI counterparts can only compensate for one sequence depending on the direction of rotation assumed.

Stationary Frame

$$H_{Stat2}(s) = \frac{K_p s^2 + K_i s}{s^2 + \omega_o^2} \quad (3.3)$$

Stationary Frame

$$H_{Stat1}(s) = K_p + \frac{K_i s}{s^2 + \omega_o^2} \quad (3.4)$$

3.3.1 Operating Principles

One of the demanded features of the proposed control scheme involves the precise compensation of only typical harmonics produced by most nonlinear loads. That means the controller gains at those frequencies on interest (negative- $(6k-1)\omega_o$ and positive- $(6k+1)\omega_o$, where $k = 1, 2, 3 \dots$) must ideally be infinite with preferably zero gains sustained at the non-characteristic frequencies, so as to avoid unnecessary noise amplification. An obvious approach to produce the described harmonic gain profile is to use multiple copies of (3.3) tuned at different frequencies in the stationary frame, written as:

Stationary Frame

$$H_{Stat2-a}(s) = \sum_{k=1}^h \frac{K_{pk} s^2 + K_{ik} s}{s^2 + ((6k \pm 1)\omega_o)^2} \quad (3.5)$$

where h , K_{pk} and K_{ik} are the maximum harmonic order considered and respective controller gains. Although effective, an immediate disadvantage observed from (3.5) is that as the number of harmonics selected for compensation increases, the computational resource needed for processing all the CV-PI terms increases proportionally. Upon reaching the processing limit, the converter output degrades noticeably, making the choice of selecting CV-PR over the conventional PR controller less prominent. One method for reducing the number of resonant terms is deduced from the observation that by transforming the $-(6k-1)\omega_o$ and $+(6k+1)\omega_o$ harmonics to the synchronous frame rotating at ω_o , they respectively become $-6k\omega_o$

and $\pm 6k\omega_o$ components. These components can collectively be compensated by the single generic resonant term expressed in (3.6), whose gains are infinite at both $\pm 6k\omega_o$ because of the mathematical squaring operation in the denominator. (Placement of resonant terms in the synchronous frame is first proposed in [93] for the less inferior PR transfer function expressed in (3.4)).

Synchronous Frame

$$H_{Syn2_a}(s) = \sum_{k=1}^h \frac{K_{pk}s^2 + K_{ik}s}{s^2 + (6k\omega_o)^2} \quad (3.6)$$

Although effective in reducing the computational burden by half, (3.6) still has an upper limit, above which the compensation of more harmonics would lead to performance degradation. Therefore, instead of explicitly realizing each resonant term, an alternative method of integrated implementation is needed. This integration form can be deduced by performing the following simple mathematical manipulations with h set to ∞ to compensate for all characteristic load harmonics and an additional $H_{Syn1}(s) = K_{p1} + K_{i1}/s$ term added.

Synchronous Frame

$$\frac{Y(s)}{E(s)} = H_{Syn1}(s) + H_{Syn2_a}(s) = s \left\{ \frac{K_{p1}}{s} + \sum_{k=1}^{\infty} \frac{K_{pk}s}{s^2 + (6k\omega_o)^2} \right\} + \left\{ \frac{K_{i1}}{s} + \sum_{k=1}^{\infty} \frac{K_{ik}s}{s^2 + (6k\omega_o)^2} \right\} \quad (3.7)$$

Upon setting $K_{i1}/K_{p1} = K_{ik}/K_{pk} = R/L$ and $2K_{i1} = K_{ik} = 12\omega_o/\pi$, (3.7) further simplifies to:

Synchronous Frame

$$\frac{Y(s)}{E(s)} = \frac{sL}{R} \left[\frac{6\omega_o}{\pi} \left\{ \frac{1}{s} + \sum_{k=1}^{\infty} \frac{2s}{s^2 + (6k\omega_o)^2} \right\} \right] + \left[\frac{6\omega_o}{\pi} \left\{ \frac{1}{s} + \sum_{k=1}^{\infty} \frac{2s}{s^2 + (6k\omega_o)^2} \right\} \right] \quad (3.8)$$

Synchronous Frame

$$\frac{Y(s)}{E(s)} = \frac{sL}{R} \left[\frac{1+e^{-sT_d}}{1-e^{-sT_d}} \right] + \left[\frac{1+e^{-sT_d}}{1-e^{-sT_d}} \right] = \left(\frac{sL}{R} + 1 \right) \left(\frac{1+e^{-sT_d}}{1-e^{-sT_d}} \right) \quad (3.9)$$

$$T_d = 2\pi/(6\omega_o) = T_o/6$$

where an exponential rational function has replaced the summation of resonant terms. Quite obviously, (3.9) infers that the resonant filters in (3.6) can equivalently be implemented by using only small amount of memory spaces for storing past or delayed values of the input control error without any significant increase in computational burden even when compensating for all characteristic load harmonics. Illustration of this alternative method of implementation is shown in Fig. 3-2(a), where the delay duration T_d is noted to be one-sixth of the fundamental time period $T_o = 2\pi/\omega_o$, as indicated in (3.9). The only minor difference noted between the representations in (3.6)

(a)

(b)

Fig. 3-2. CV repetitive control in the synchronous frame under (a) ideal and (b) non-ideal operating conditions.

and (3.9) is the implicit embedding of a gain K_{p1} and an integral K_{i1}/s term in the latter (explicitly shown in (3.7)), whose influence is to compensate for the positive-sequence fundamental error in the synchronous frame (negative-sequence not compensated), similar to that imposed by the traditional synchronous frame PI controller. In addition to that, the integral term is noted to have an ability to compensate for grid harmonics, which is qualitatively less obvious, but can be proven mathematically as demonstrated in Subsection 3.3.3.

Another observation deduced from (3.9) is that it does not allow independent tuning of the fundamental and individual harmonic gains, which are assumed constant during the simplification from (3.7) to (3.9). This no doubt is a disadvantage, which can be compromised by paralleling the CV repetitive controller with the CV-PR controller expressed in (3.3) to give the system shown in Fig. 3-3, where a mixed combination of stationary and synchronous (rotating at the fundamental frequency) frames is involved. The resulting controller can then be freely tuned to produce the desired dynamic response, fundamental positive-sequence tracking and negative-sequence unbalance compensation, independent of its characteristic load harmonic compensation ability achieved by using only simple delay and mathematical operations.

Fig. 3-3. Representation of integrated CV-PR and CV repetitive control scheme in mixed reference frame.

Note that the adoption of delay block for control has previously been mentioned in [55], but for the scheme discussed there, the summation of multiple PR terms is discussed, which as mentioned earlier, will give rise to poorer compensation when compared with the more advanced CV-PR controllers used for designing the CV repetitive scheme presented here. In addition, the scheme in [55] has resonant peaks placed at all harmonic frequencies including those not typically produced by common nonlinear loads, which can at times cause noise re-injection to the system if disturbing noises at those untypical frequencies exist. Also, it is pointed out in [55] that the embedded integrator in its described scheme is not providing any useful contribution to performance, and is thus intentionally neutralized by placing a high pass filter $\gamma s/(\gamma s + 1)$ along the feedback path of that scheme. Instead of neutralizing it, the integral term of the CV repetitive scheme is used wisely for compensating other harmonics after a simple modification is made to its frame transformation process, as discussed later on.

3.3.2 Robustness and Stability Enhancement

The CV transfer function in (3.9) is noted to consist of the product of a zero with a rational time delayed transfer function. Needless to say, both building blocks are ideal entities derived directly from conceptual studies, which need further refinements before they can stably be realized in practice. For the zero at $s = -R/L$, its realization can be enhanced by adding a pole with properly tuned cutoff frequency for attenuating noises that it might pick up. This modification is explicitly shown in Fig. 3-2(b), where the introduced pole cutoff frequency is located at $s = -1/\tau_1$. Next, to introduce physical stability to the time-delay block, its series of infinite gains at characteristic load harmonic frequencies must be flattened slightly by introducing a damping coefficient to its transfer function (also applicable to most existing resonant controllers). This can be done by shifting the roots to the left by σ on the root locus plot, which in transfer function notation, is written as:

Synchronous Frame

$$TD(s + \sigma) = \frac{1 + e^{-(s+\sigma)T_d}}{1 - e^{-(s+\sigma)T_d}} = \frac{1 + K_f e^{-sT_d}}{1 - K_f e^{-sT_d}} \quad (3.10)$$

where $K_f = e^{-\sigma T_d}$ is viewed as the equivalent damping gain added along the control path of the delay term e^{-sT_d} (also shown in Fig. 3-2(b)). With this modification, the gains at the resonant peaks are now not infinite, but expressed as $(1 + K_f)/(1 - K_f)$, from which, it is deduced that to still keep a reasonably high gain without introducing polarity inversion, K_f should preferably assume a value between 0 and 1. In addition to its gain reduction ability, other influences introduced by the damping gain in (3.10) are more obviously revealed by expanding (3.10) into its resonant series, as demonstrated by:

Synchronous Frame

$$\begin{aligned} & \frac{Y(s + \sigma)}{E(s + \sigma)} \\ &= \frac{6\omega_o}{\pi} \left\{ \frac{1}{s + \sigma} + \sum_{k=1}^{\infty} \frac{2(s + \sigma)}{(s + \sigma)^2 + (6k\omega_o)^2} \right\} \\ &= \frac{6\omega_o}{\pi} \left\{ \frac{1}{s + \sigma} + \sum_{k=1}^{\infty} \frac{2(s + \sigma)}{s^2 + 2\sigma s + [\sigma^2 + (6k\omega_o)^2]} \right\} \end{aligned} \quad (3.11)$$

From (3.11), it is noted that the integral term now has a cutoff frequency σ , which is relatively small, and therefore, would not introduce any significant influence. Also noted in (3.11) is the presence of two additional terms with σ embedded, found in the denominator of each of the resonant functions. For the first term indicated as $2\sigma s$, its duty is to damp the infinite resonant peaks as intended with no unwanted side influence introduced, but for the second term indicated as σ^2 , it undesirably causes the resonant peaks to shift slightly above their nominal frequencies collectively expressed as $6k\omega_o$. Fortunately, that shifting is not expected to impact the controller performance significantly since σ^2 is almost negligible even when compared with the first harmonic resonance located at 300 Hz ($6\omega_o$) in the synchronous frame. For

Fig. 3-4. Variation of the sixth-order resonant term in the synchronous frame when σ changes.

validating that assumption, Fig. 3-4 shows the variation of the sixth-order resonant term in (3.11) with σ increased from 0 to $2\pi \times 10$ rad/s. Clearly, the resonant gain reduces when the damping coefficient σ increases, but with no visible shifting of resonant frequency noted in all three traces, hence justifying the assumption of negligible mistuning even for the “worst case” scenario. Also interesting to note is the comparatively smaller mistuned error associated with the proposed scheme, as compared with the scheme discussed in [55], where the first resonant peak is placed at 100 Hz in the stationary frame.

Other than adding a damping coefficient, a second modification recommended for the time delay block is to place a simple first order LPF with cutoff frequency of $s = -1/\tau_2$ after the delay term, as indicated in Fig. 3-2(b). This LPF term serves to narrow the bandwidth of the system so as to filter off high frequency switching noises that can bring instability, especially to an analog system. For a digital implementation, explicit noise filtering is less stringent since the sampling process, to a favourable extent, has introduced some implicit filtering to the controller.

3.3.3 Integral Term for Grid Disturbance Rejection

As noted in (3.7), the proposed CV repetitive control scheme incorporates an integrator K_i/s in addition to those harmonic resonant peaks. The integrator, besides contributing slightly to the tracking of fundamental reference, also exhibits an additional functionality when the proposed scheme is used for grid converter control, during which the grid voltage is measured and used for synchronous frame transformation [94]. For undistorted grid, transformation to the synchronous frame is straightforward with only a linearly rising angle θ available for affecting it. On the other hand, if the grid is distorted, choices of synchronizing the transformation angle with reference to the positive-sequence or actual grid voltage are available for selection with each having its own unique system impacts. Needless to say, if the angle synchronized with the positive-sequence grid voltage is used, the frequency shifting expression adopted is again similar to that expressed in (3.2), which clearly has no added capability for compensating the grid distortion. Therefore, instead of synchronizing with the positive-sequence voltage, the actual grid voltage should be followed to give an angle $\hat{\theta}$ ($\neq \theta$) needed for affecting an alternative form of frequency-shifting process that is different from (3.2). To be more specific, using $\hat{\theta}$ for transformation gives rise to the new frequency-shifted transfer function of $\hat{H}_{Stat2}(s)$ in the stationary frame, and expressed as:

Stationary Frame

$$\begin{aligned} \hat{H}_{Stat}(s) = & \frac{1}{2} \left[H_{Syn}(s + j\omega_o) + H_{Syn}(s - j\omega_o) \right] \\ & + \frac{a_h}{4} \left\{ \begin{aligned} & \left[H_{Syn}(s + jh\omega_o) + H_{Syn}(s - jh\omega_o) \right] \\ & - \left[H_{Syn}(s + j(h-2)\omega_o) + H_{Syn}(s - j(h-2)\omega_o) \right] \end{aligned} \right\} \end{aligned} \quad (3.12)$$

where a_h is the amplitude of grid distortion introduced for relating the actual and positive-sequence angles by $\hat{\theta} = \theta + a_h \sin[(h-1)\theta]$. Clearly, the first term in (3.12) resembles that in (3.2), used for performing the usual synchronous frame (rotating at ω_o) to stationary frame transformation. Therefore, the $6k\omega_o$ resonant filters embedded

in the proposed scheme can still compensate for the characteristic load harmonics even if $\hat{\theta}$ is used. More interestingly is the added feature introduced by the second term, which infers that the embedded integrator when transformed to the stationary frame resembles a resonant term with its resonant peak centered at $h\omega_b$. That means the embedded integrator in the mixed-frame repetitive controller can compensate for any $h\omega_b$ harmonics in the grid, albeit at a reduced gain of $a_h/4$, in addition to those typical load harmonics at $-(6k-1)\omega_b$ and $+(6k+1)\omega_b$ discussed earlier.

3.4 Complex-Vector Repetitive Control in the Stationary Frame

Although the mixed frame scheme presented in Fig. 3-3 has already been proven to operate well under distorted system conditions, its analysis is still not that straightforward because of its involvement of two reference frames, which definitely is not easy to express mathematically. Therefore for analytical purposes, it would be more convenient to either transform the CV-PR controller to the CV-PI controller in the synchronous frame or the CV repetitive control scheme to the stationary frame. Of these two options, the former is straightforward, but would impose the disadvantage of requiring frame transformation of all control variables at the beginning of each computational step. Therefore, instead of that option, the second option of transforming the CV repetitive block to the stationary frame is now explored by applying the frequency-shifting process illustrated in (3.2) to (3.9). The mathematical manipulations are presented as follows.

Stationary Frame

$$\frac{Y(s)}{E(s)} = \frac{1}{2} \left\{ \left[\frac{(s - j\omega_o)L}{R} + 1 \right] \left[\frac{1 + e^{-(s - j\omega_o)T_d}}{1 - e^{-(s - j\omega_o)T_d}} \right] \right. \\ \left. + \left[\frac{(s + j\omega_o)L}{R} + 1 \right] \left[\frac{1 + e^{-(s + j\omega_o)T_d}}{1 - e^{-(s + j\omega_o)T_d}} \right] \right\}$$

$$\begin{aligned}
 &= \frac{1}{2} \left\{ \left[\frac{sL}{R} + 1 \right] \left[\frac{1 + e^{-(s-j\omega_o)T_d}}{1 - e^{-(s-j\omega_o)T_d}} + \frac{1 + e^{-(s+j\omega_o)T_d}}{1 - e^{-(s+j\omega_o)T_d}} \right] \right. \\
 &\quad \left. - \frac{j\omega_o L}{R} \left[\frac{1 + e^{-(s-j\omega_o)T_d}}{1 - e^{-(s-j\omega_o)T_d}} - \frac{1 + e^{-(s+j\omega_o)T_d}}{1 - e^{-(s+j\omega_o)T_d}} \right] \right\} \\
 &= \frac{1}{2} \{ H_{Int1}(s) + H_{Int2}(s) \}
 \end{aligned} \tag{3.13}$$

Considering $H_{Int1}(s)$ and $H_{Int2}(s)$ separately then gives rise to:

$$\begin{aligned}
 H_{Int1}(s) &= \left[\frac{sL}{R} + 1 \right] \left[\frac{2(1 - e^{-s2T_d})}{1 - e^{-(s-j\omega_o)T_d} - e^{-(s+j\omega_o)T_d} + e^{-s2T_d}} \right] \\
 &= \left[\frac{sL}{R} + 1 \right] \left[\frac{2(1 - e^{-s2T_d})}{1 - e^{-sT_d} (e^{j\omega_o T_d} + e^{-j\omega_o T_d}) + e^{-s2T_d}} \right]
 \end{aligned} \tag{3.14}$$

Noting that $e^{-j\omega_o T_d} + e^{j\omega_o T_d} = 2\cos(\omega_o T_d)$, (3.14) then becomes:

$$H_{Int1}(s) = \left[\frac{sL}{R} + 1 \right] \left[\frac{2(1 - e^{-s2T_d})}{1 - e^{-sT_d} (2\cos(\omega_o T_d)) + e^{-s2T_d}} \right] \tag{3.15}$$

Since $T_d = 2\pi/(6\omega_o)$ from (3.9), (3.15) further simplifies to:

$$H_{Int1}(s) = \left[\frac{sL}{R} + 1 \right] \left[\frac{2(1 - e^{-s2T_d})}{1 - e^{-sT_d} + e^{-s2T_d}} \right] \tag{3.16}$$

Proceeding next to simplify $H_{Int2}(s)$:

$$\begin{aligned}
 H_{Int2}(s) &= \frac{j\omega_o L}{R} \left[\frac{-2e^{-(s-j\omega_o)T_d} + 2e^{-(s+j\omega_o)T_d}}{1 - e^{-(s-j\omega_o)T_d} - e^{-(s+j\omega_o)T_d} + e^{-s2T_d}} \right] \\
 &= \frac{j2\omega_o L}{R} \left[\frac{e^{-sT_d} (e^{-j\omega_o T_d} - e^{j\omega_o T_d})}{1 - e^{-sT_d} (e^{j\omega_o T_d} + e^{-j\omega_o T_d}) + e^{-s2T_d}} \right]
 \end{aligned} \tag{3.17}$$

Replacing the exponential terms in the parentheses of (3.17) by

$e^{-j\omega_o T_d} - e^{j\omega_o T_d} = -j2\sin(\omega_o T_d)$ and $e^{-j\omega_o T_d} + e^{j\omega_o T_d} = 2\cos(\omega_o T_d)$ then gives rise to:

$$\begin{aligned}
 H_{int2}(s) &= \frac{j2\omega_o L}{R} \left[\frac{-j2e^{-sT_d} \sin(\omega_o T_d)}{1 - 2e^{-sT_d} \cos(\omega_o T_d) + e^{-s2T_d}} \right] \\
 &= \frac{j2\omega_o L}{R} \left[\frac{-j2e^{-sT_d} \times \sqrt{3}/2}{1 - e^{-sT_d} + e^{-s2T_d}} \right] \\
 &= \frac{2\sqrt{3}\omega_o L}{R} \left[\frac{e^{-sT_d}}{1 - e^{-sT_d} + e^{-s2T_d}} \right]
 \end{aligned} \tag{3.18}$$

With (3.16) and (3.18) substituted back to (3.13), the required CV repetitive transfer function in the stationary frame is derived as:

$$\frac{Y(s)}{E(s)} = \frac{(sL/R+1) + (\sqrt{3}\omega_o L/R)e^{-sT_d} - (sL/R+1)e^{-s2T_d}}{1 + (e^{-s2T_d} - e^{-sT_d})} \tag{3.19}$$

(a)

(b)

Fig. 3-5. CV repetitive control in the stationary frame under (a) ideal and (b) non-ideal operating conditions.

Fig. 3-6. Bode plot of the proposed CV repetitive controller in comparison to a single PR controller.

Drawing the above equation in block diagram form then gives rise to the configuration shown in Fig. 3-5(a), where only simple delay blocks and transfer functions are used for its implementation in the stationary frame without any frame transformation of control variables needed. Unlike the mixed-frame variant whose resonant peaks compensate for only negative $(6k-1)$ and positive $(6k+1)$ harmonics, the resonant terms introduced by the stationary frame variant can compensate for both positive and negative-sequence $(6k\pm 1)$ harmonics based on the same reasoning explained in Section 3.3, while deriving the elementary resonant expressions. The designed stationary frame controller can therefore also compensate for grid distortion, even though its operating principle is not based on the integral operation. Proceeding on to stabilize the controller in a physical setup, Fig. 3-5(b) shows the controller with gain K_f and time constants $(\tau_1$ and τ_2) added for filtering and damping noises, which would almost always be there. The resulting controller (with a CV-PR term added) is therefore summarized as a robust, dynamically fast entity that can track its positive-sequence reference well, and compensate for negative-sequence unbalance and characteristic load / grid harmonics using only simple building blocks for its realization. The frequency domain response of the designed CV repetitive controller is plotted in Fig.

instead of (3.3), it uses the PR resonant term in (3.4) as the elementary building block.

With the RL load connected and the 2 A reference current set to include an additional 10% each of -5^{th} , $+7^{\text{th}}$, -11^{th} and $+13^{\text{th}}$ harmonics, the controller ability to track these characteristic load harmonics is shown in Fig. 3-8 for both the NCV and CV repetitive schemes. As anticipated, the NCV tracking ability is poorer with its measured current lagging behind its reference. On the other hand, the CV scheme is noted to track well because of its more precise pole-zero cancellation, as discussed earlier. Moving on to confirm its dynamic response, Fig. 3-9 shows the measured converter current tracking its reference closely during the triggered step-up and down events for the CV repetitive scheme. In effect, the observed transients smoothen off in less than a cycle of the highest harmonic frequency tracked by the controller.

With next an undistorted grid of 240 V (line rms) and 50 Hz connected to the setup, and the 2 A reference current set to include a higher percentage (20%) each of the more prominent -5^{th} and $+7^{\text{th}}$ harmonics, denoting the system harmonic currents that need to be compensated. The recaptured experimental waveforms are shown in Fig. 3-10, where the same excellent tracking performance is attained. Proceeding next to emulate a distorted grid with 5% each of atypical positive 5^{th} and negative 7^{th} harmonics included, and the current reference content kept unchanged, Fig. 3-11 again shows the excellent tracking ability of the CV repetitive scheme even when both positive and negative-sequence components of a particular harmonic are now present in the system. As discussed, this compensating ability is contributed by the integral term embedded in the mixed-frame controller and the transformation process used to develop the stationary frame controller.

Fig. 3-8. Experimental steady-state current tracking performances of NCV (TOP) and CV (BOTTOM) repetitive controllers.

Fig. 3-9. Experimental step-up (TOP) and down (BOTTOM) transient current responses of CV repetitive controller.

Fig. 3-10. Experimental three-phase grid voltages (TOP) and current waveforms (BOTTOM) obtained with CV repetitive control and an undistorted grid.

Fig. 3-11. Experimental three-phase grid voltages (TOP) and current waveforms (BOTTOM) obtained with CV repetitive control and a distorted grid.

3.6 Summary

In this chapter, a CV repetitive control scheme is presented, which can either be implemented in a mixed combination of stationary and synchronous frame or solely in the stationary frame. For analytical purposes, the latter is preferred since it allows the full mathematical expression to be formulated more easily, which in effect is the sum of a CV-PR term and the product of a zero with a rational delayed transfer function. The controller can conveniently be implemented using simple memory blocks and transfer functions without compromising any of its excellent steady-state and transient

characteristics, where one of them is its ability to compensate for only typical load harmonics with no unwanted noise amplification observed at atypical frequencies.

When applied to grid converters, the proposed CV repetitive control scheme not only regulates real and reactive powers, it also compensates for system harmonic currents produced by nonlinear loads. Its relatively simple theoretical basis, derived solely from classical control theories and exponential mathematical operations, further facilitates understanding and adoption by the industry especially with its physical realization already confirmed experimentally by a grid-tied converter.

Chapter 4 Repetitive Control of Power Converters with Output LC Filters

4.1 Introduction

In many DG systems, interfacing PWM converters are expected to operate in both grid-connected and autonomous modes. The latter happens during ac mains outages so that power can still be channeled to nearby critical loads to prevent them from abnormal shutdowns. The PWM converter therefore operates like a UPS. To realize such capability, an inductor-capacitor (LC) filter is usually connected at the output of the converter, whose control objective is now to keep a constant capacitor voltage regardless of how the loads change.

With the above stated objective in view, this chapter presents the design of a number of repetitive control schemes for UPS voltage regulation, where the main control entities needed are identified as simple memory blocks and a single resonant filter. The added memory blocks are for enhancing the pivotal role of precise steady-state reference tracking even when the UPS is tasked to supply highly nonlinear and unbalanced loads. These loads generate harmonics, which can be individually compensated by the high control gains introduced at their respective frequencies. In contrast, gains at the other non-characteristic load frequencies are forced to zero by enhancing the selectiveness of the controller. With this load-matching characteristic, the proposed control schemes are expected to be more robust and less sensitive to unwanted noise amplification, which are certainly advantages.

Adding on to its advantages, the resonant filter is intentionally introduced for reinforcing the controller fundamental tracking ability (both positive and negative sequences), and to improve its overall dynamic response so as to virtually keep its output

voltage unaffected even when exposed to a sudden, large load step transients. Unlike past trends where performance enhancement is usually accompanied by a rise in complexity, the proposed control schemes gain their added advantages using virtually the same hardware setup as the double loop controller, inferring that existing double loop controllers can easily be retrofitted to include the new schemes. This simplicity in implementation and the overall performance enhancement of the proposed repetitive control schemes are eventually tested using a digitally controlled power converter, configured as a UPS for powering diode-rectified nonlinear and unbalanced loads.

4.2 Single and Double loop Control Structures of UPS

For UPS control based on classical feedback control theories, the single and double loop configurations, shown in Fig. 4-1(a) and (b) respectively, are the simplest with reasonable output quality obtained under linear load conditions. In Fig. 4-1(a), the output voltage v_o across the filter capacitor C_f is directly fed back to a difference block, where it is subtracted from the voltage reference v_o^* to give the corresponding error e_v . The error e_v is then passed to a voltage controller, usually implemented using a PI controller in either the stationary or synchronous frame, whose output v_{int} , together with the feed-forward voltage v_o , forms the modulating voltage v_{UPS} needed for driving the UPS inverter. It is known from classical control theories that the dynamic response and stability margin of the single-loop structure is poorer and therefore for most cases, a second inner current loop is added, as shown in Fig. 4-1(b).

Instead of producing v_{int} as in Fig. 4-1(a), the output of the outer voltage controller is now a reference signal i_C^* for the inner capacitor current control loop (inductor current i_L can be fed back instead, but the overall system response will be slightly poorer [95]). The current error e_i , expressed as $(i_C^* - i_C)$, is then fed into the inner controller for generating v_{int} , which when added to v_o , gives the modulating voltage v_{UPS} for driving the inverter. For the inner current controller, a proportional controller is considered appropriate since the task of maintaining zero steady-state error for the UPS output

(a)

(b)

Fig. 4-1. General block representations of (a) single-loop and (b) double loop control.

voltage is already taken care of by the outer voltage controller [96]. Therefore, the criterion for tuning the gain of the inner controller should mainly be the increase of its dynamic response to preferably much faster than the outer voltage control loop. If indeed attained, the double loop block representation can then be simplified to that shown in Fig. 4-2, where the inner current control dynamic is ignored when tuning the outer voltage loop.

Under balanced and linear operating conditions, both schemes described above are noted to track their references well with zero error ensured if a simple synchronous

Fig. 4-2. Simplified block representation of double loop control.

frame PI controller is used as the outer voltage controller. Unfortunately, as soon as load distortions or negative sequence components are introduced to the system, the tracking ability of the PI controller may degrade seriously, implying that other advanced techniques need to be used for better performance. Indeed, selective harmonic compensation techniques with satisfactory responses are available [95], but they usually introduce a higher computational burden or more complex implementation. Achieving a better compromise in terms of performance (both steady-state and transient) and complexity, the following section discusses the derivations of a number of simple repetitive controllers, whose advantages and disadvantages are also compared in details. The analyses are tuned mainly towards implementation using the double loop structure with the single-loop configuration only occasionally referenced for clarifying some concepts.

4.3 Operating Principles of Different Repetitive Control Schemes

The generic operating principles of all repetitive controllers discussed in this chapter are based on the use of a properly delayed control block placed in the feedback path of the controller. (In practice, the delayed control block can conveniently be implemented using a small amount of memory from the relatively large data storage space found in most modern digital signal processors (DSPs) or micro-controllers). Indeed, the formulated control principles match those underlying traditional repetitive control, but unlike the latter, where only a single negative feedback loop is used [51], the repetitive controllers discussed below have more features added to better refine the quality of the UPS output waveform. Their specific operating principles are now respectively described as follows.

4.3.1 Repetitive Control with a Single Zero at $s = 0$

As noted in [96], a combination of proportional and resonant controllers (referred as PR controller, $H_{Stat1}(s)$ with a control zero at $s = 0$) in the stationary frame can be used in place of a PI controller $H_{Syn1}(s)$ in the synchronous frame for precise fundamental waveform tracking in a UPS. Theoretically, [45] has proven using frequency-shifting techniques that both controllers are nearly similar in operating principles when viewed from the same reference frame, and they can mathematically be linked by:

$$H_{Stat1}(s) = \frac{1}{2} [H_{Syn1}(s + j\omega_o) + H_{Syn1}(s - j\omega_o)]$$

$$H_{Stat1}(s) = K_p + K_i s / (s^2 + \omega_o^2)$$

$$H_{Syn1}(s) = K_p + K_i / s \quad (4.1)$$

where K_p and K_i are gains, and ω_o represents the fundamental frequency of interest. Clearly, (4.1) shows that $H_{Stat1}(s = \pm j\omega_o)$ has an infinite gain at the fundamental frequency for forcing the steady-state error to zero accordingly to the internal model control principles and the Bode diagram shown in Fig. 4-3. This infinite gain also infers that in addition to its easier implementation in the stationary frame, the PR controller has a second advantage of distinctly compensating for both positive ($+\omega_o$) and

Fig. 4-3. Bode plots of PR controllers with (solid line) and without (dashed line) a control zero at $s = 0$ ($K_p = 0$ and $K_i = 1$).

negative-sequence ($-\omega_o$) components, unlike a synchronous PI controller, where only one of the sequences is compensated [45]. When comparing with those traditional state feedback techniques [98], adding the PR controller to the outer voltage loop also has the advantage of reducing parametric sensitivity of the system since various control paths that depend on the accurate prediction of system parameters are now not needed for inclusion (and thus not explicitly shown in Fig. 4-1).

Moving forward, the idea of using multiple resonant filters centered at selected harmonic frequencies for regulating those chosen harmonics of interest is reported in [95], and when expressed in the s-domain, the control transfer function $H_{SHC1}(s)$ is written as:

$$H_{SHC1}(s) = K_p + \sum_{h=1}^J \frac{K_{ih}s}{s^2 + (h\omega_o)^2} \quad (4.2)$$

where K_{ih} , h and J represent the individual resonant gain, harmonic order and highest harmonic order specified for compensation. For most typical loads, h would assume odd integer values ($h = 2k-1$, where $k = 1, 2, 3 \dots$), and by letting $J \rightarrow \infty$ for compensating all odd harmonics, (4.2) can be rewritten as (4.3) if a constant gain $K_{ih} = 4\omega_o K / \pi$ is used for all the resonant filters.

$$H_{SHC1}(s) = K_p + K \left(\frac{2\omega_o}{\pi} \sum_{k=1}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) = K_p + K \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right) \quad (4.3)$$

Clearly, the expression in (4.3) includes an exponentially delayed term in both its numerator and denominator, which when drawn using block representation, corresponds to the negative delayed feed-forward and feedback paths shown in Fig. 4-4. That configuration definitely represents an easier way of effecting numerous odd harmonic compensations using only a single delay or memory block together with a few simple arithmetic operations. The only compromise noted with the scheme is its lack of freedom in tuning since all harmonic gains K_{ih} must now assume the constant value of $4\omega_o K / \pi$. To resolve that constraint to a reasonable extent, an additional fundamental

Fig. 4-4. Outer voltage repetitive controller $H_{SHCI}(s)$ with a single control zero at $s = 0$.

resonant term is recommended for inclusion to the overall controller to give:

$$\begin{aligned}
 H_{SHCI}(s) &= K_p + \frac{(K_i + 4\omega_o K/\pi)s}{s^2 + \omega_o^2} + K \left(\frac{2\omega_o}{\pi} \sum_{k=2}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) \\
 &= K_p + \frac{K_i s}{s^2 + \omega_o^2} + K \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right)
 \end{aligned} \tag{4.4}$$

where the middle expression indicates that the fundamental resonant gain is changed to $(K_i + 4\omega_o/\pi)$, while the rest of the gains remain at $4\omega_o K/\pi$. Independent tuning of the controller reference tracking and harmonic disturbance rejection abilities is therefore possible, where the focus for the latter is mainly to minimize the prominent fifth and seventh harmonics. It is commented here that control scheme using an exponential term has previously been mentioned in [60] for UPS control, but the precise scheme found there is different from that expressed in (4.4). Moreover, the scheme reported in [60] is mainly for the single-loop configuration with its extension to a double loop scheme producing no favorable response because of the absence of zero from the controller transfer function. Explanation for that and details of the UPS controller used in [60] are described next to provide a basis for comparison.

4.3.2 Repetitive Control without Zero

In [46], an alternative resonant term $H_{Stat2}(s)$ is introduced for forcing the steady-state error to zero, but when compared with $H_{Stat1}(s)$ in (4.1), $H_{Stat2}(s)$ is noted to have no control zero at $s = 0$, meaning that its transfer function is expressed as (4.5), and is not directly derived by frequency-shifting the PI controller from the synchronous to the stationary frame.

$$H_{Stat2}(s) = K_p + K_i / (s^2 + \omega_o^2) \quad (4.5)$$

With the absence of a zero at $s = 0$, the Bode plot of $H_{Stat2}(s)$ in (4.5) shows that its phase response is pushed downwards by 90° , as compared to that of $H_{Stat1}(s)$ in (4.1), to give the distinct levels of 0° and -180° below and above the resonant frequency respectively (Fig. 4-3). For closed-loop operation, the -180° phase-shift can at times give rise to a poor phase margin, and hence a poor transient response [47]. In addition, even though its placement along the voltage control path can give rise to a zero fundamental steady-state error, its output is not fully diminished if harmonics are present in the measured voltage. In fact, by noting that v_o^* is a pure sinusoidal reference at ω_o and that the input to the controller is given as $e_v = v_o^* - v_o$, the individual harmonic outputs of $H_{Stat2}(s)$ are expected to stay in-phase with their driving counterparts in v_o . That would infer that $H_{Stat2}(s)$ is not optimally designed for use as the voltage controller in a double loop configuration since its output, being the capacitor current reference i_C^* , should conceptually lead v_o by 90° rather than staying in-phase with it (see Fig. 4-1(b) for the relevant labeling). On the other hand, $H_{Stat2}(s)$ would function well when used with the single-loop configuration since the intended controller output for that case is v_{int} , used for computing the UPS modulating signal v_{UPS} (see Fig. 4-1(a)), whose phase orientation stays near to that of v_o .

Although predicted to be poorer in performance, the extension of $H_{Stat2}(s)$ to its repetitive variant is still pursued here for building a basis for comparison and for completeness. Effecting that derivation then gives rise to:

 Fig. 4-5. Outer voltage repetitive controller $H_{SHC2}(s)$ without the control zero at $s = 0$.

$$\begin{aligned}
 H_{SHC2}(s) &= K_p + \sum_{k=1}^{\infty} \frac{K_{ih}}{s^2 + ((2k-1)\omega_o)^2} \\
 &= K_p + \frac{K}{s} \left(\frac{2\omega_o}{\pi} \sum_{k=1}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) \\
 &= K_p + \frac{K}{s} \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right)
 \end{aligned} \tag{4.6}$$

where the integral term in the far right expression is noted to cancel out the control zero at $s = 0$ within the exponential rational function. Transferring (4.6) to its block representation then gives rise to the structure shown in Fig. 4-5, which resembles that shown in Fig. 4-4 except for the inclusion of an additional “ $1/s$ ” integral term. Adding again a separate resonant term for independently controlling its fundamental tracking and harmonic rejection, (4.6) is rewritten as (independent control of both objectives has not been discussed in [60] even though it uses (4.6) for its single-loop control):

$$\begin{aligned}
 H_{SHC2}(s) &= K_p + \frac{K_i + 4\omega_o K/\pi}{s^2 + \omega_o^2} + \frac{K}{s} \left(\frac{2\omega_o}{\pi} \sum_{k=2}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) \\
 &= K_p + \frac{K_i}{s^2 + \omega_o^2} + \frac{K}{s} \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right)
 \end{aligned} \tag{4.7}$$

whose overall block representation is drawn in Fig. 4-5.

4.3.3 Complex Vector Repetitive Control with Two Zeros

Instead of transforming a standard synchronous PI controller to the stationary frame, [48] have recommended the processing of a modified PI controller, expressed as $H_{Syn3}(s) = K_p + (K_i + j\omega_o K_p)/s$ and known as complex vector PI. The reason for using the complex integral coefficient is that it more accurately cancels the plant (UPS in this case) pole, allowing the final system dynamic to be solely determined by the controller [43]. Even if precise cancellation is not possible due to likely parametric variations, the insertion of an imaginary $j\omega_o$ term to the control zero is proven in [43] to help retain the controller performance even if the plant parameters vary widely. Therefore, $H_{Syn3}(s)$ does have its advantages, and when shifted to the stationary frame, it gives rise to the transfer function $H_{Stat3}(s)$, expressed as:

$$H_{Stat3}(s) = (K_p s^2 + K_i s) / (s^2 + \omega_o^2) \quad (4.8)$$

where two control zeros are noted at $s = 0$ and $s = -K_i/K_p$. The latter should conceptually be tuned to stay near the plant pole so as to cancel out or minimize its effect, leaving the responsibility of tuning the system dynamic solely to the controller. Proceeding on to derive the time-delay variant using the same odd harmonic compensation approach, the third transfer function being investigated is written as:

Fig. 4-6. Outer voltage repetitive controller $H_{SHC3}(s)$ with two control zeros.

$$\begin{aligned}
H_{SHC3}(s) &= \sum_{k=1}^{\infty} \frac{K_{ph}s^2 + K_{ih}s}{s^2 + ((2k-1)\omega_o)^2} = (K's + K) \left(\frac{2\omega_o}{\pi} \sum_{k=1}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) \\
&= (K's + K) \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right)
\end{aligned} \tag{4.9}$$

where the individual harmonic proportional gain K_{ph} is again assumed constant, and expressed as $K_{ph} = 4\omega_o K' / \pi$. Adding the flexibility of independent tuning to (4.9) then gives rise to:

$$\begin{aligned}
H_{SHC3}(s) &= \frac{(K_p + 4\omega_o K' / \pi)s^2 + (K_i + 4\omega_o K / \pi)s}{s^2 + \omega_o^2} \\
&\quad + (K's + K) \left(\frac{2\omega_o}{\pi} \sum_{k=2}^{\infty} \frac{2s}{s^2 + ((2k-1)\omega_o)^2} \right) \\
&= \frac{K_p s^2 + K_i s}{s^2 + \omega_o^2} + (K's + K) \left(\frac{1 - e^{-s\pi/\omega_o}}{1 + e^{-s\pi/\omega_o}} \right)
\end{aligned} \tag{4.10}$$

whose block representation is shown in Fig. 4-6.

4.4 Experimental Results

To compare the repetitive control schemes proposed in this chapter, an experimental system was built in the laboratory, whose setup is shown in Fig. 4-7. To first illustrate performance limitations of existing control schemes, Fig. 4-8 shows the experimentally captured steady-state waveforms for the case of only a proportional controller used for the outer voltage loop. Clearly, the voltage error e_v features a non-zero steady-state error with a prominent fundamental component produced by the lagging of the actual output voltage v_o behind its reference v_o^* . This steady-state error can smoothly be reduced by adding a resonant filter to the outer voltage loop, whose resulting terminal waveforms are shown in Fig. 4-9. Despite being able to force the fundamental error to zero, the third trace in Fig. 4-9 still shows a nonzero voltage error since unwanted low-order harmonics are not fully eliminated from the UPS output.

This harmonic error can indeed be removed by adding a simple repetitive controller with

Fig. 4-7. Experimental setup used for UPS performance evaluation.

either one or two control zeros to the outer voltage loop, where for digital implementation, it simply refers to the catering of some memory spaces for delay emulation. The improved performances are shown in Fig. 4-10 for the scheme with two control zeros, where it is noted that the measured ac voltage is now more sinusoidal with virtually no fifth and seventh harmonics observed in the computed voltage error. Effectiveness in removing the low-order harmonics is however seriously degraded if the scheme with no control zero is used instead. The degraded time responses are shown in Fig. 4-11, which no doubt appear similar to those shown in Fig. 4-9, where only a single PR controller is used. Obviously, that infers the neutralization of merits introduced by the time delayed block, which as predicted in Subsection 4.3.2, is caused by the unfavorable cancellation of zero.

Proceeding on to test the fast dynamic response of the proposed repetitive control scheme, Fig. 4-12 and Fig. 4-13 show the captured waveforms for the scheme with two control zeros, when the switch S in Fig. 4-7 is turned ON and then OFF. As demonstrated in the figures, the UPS output voltage remains almost unchanged as the nonlinear load resistance R_{NL} is changed. This stable and rapid transient tracking is expected since additional degrees of control freedom (K_p and K_i in (4.10)) are intentionally introduced for gaining independent tuning of dynamic and steady-state tracking, where the former can now be adjusted to more than compensate for the poor dynamic response of the time-delay block.

Fig. 4-8. Experimental waveforms of UPS regulated using outer proportional controller.

Fig. 4-9. Experimental waveforms of UPS regulated using outer proportional + resonant controller.

Fig. 4-10. Experimental waveforms of UPS regulated using outer repetitive controller with two control zeros.

Fig. 4-11. Experimental waveforms of UPS regulated using outer repetitive controller without zero at $s = 0$.

Fig. 4-12. Experimental “step-up” transient waveforms of UPS regulated using outer repetitive controller with two control zeros.

Fig. 4-13. Experimental “step-down” transient waveforms of UPS regulated using outer repetitive controller with two control zeros.

4.5 Summary

In this chapter, a number of repetitive control schemes that can conveniently be added to the dynamically favorable double loop configuration for UPS control are presented. Two of the schemes are proved to track their respective fundamental references well,

and can independently isolate harmonic disturbances caused by nonlinear and unbalanced loads, preventing them from affecting the UPS output voltage. The dynamic responses of these two repetitive control schemes are also proven satisfactory with the UPS output voltage appearing nearly unaffected by external load transients. Implementation wise, the proposed controllers can conveniently be assembled using memory blocks and simple transfer functions, which to a favorable extent, preserves the simplicity of the double loop control approach without compromising any of its performance features, as confirmed experimentally in the chapter.

Chapter 5 Current Control of Power Converters with LCL-Filters

5.1 Introduction

In the earlier two chapters, the studied PWM converters are modeled as low order systems since passive filters used with them are either simple L or LC type. It is therefore relatively easy to ensure their stabilities when designing their closed-loop control. Unfortunately, in higher power applications where switching frequency of converters cannot be high because of accompanied switching losses, such simple filter configurations lead to bulky and costly entities that can slow down the system dynamics. This is especially so if they are designed to comply with stringent grid codes specified by IEEE 519-1992 and IEC 61000-3-12 [15].

In order to overcome the above mentioned issues, this chapter focuses on the design and control of three-phase grid-connected inverters with higher order LCL-filters. Being third-order entities, LCL-filters provide much better current ripple and harmonic attenuation over the higher frequency range, while using only small passive elements. They are therefore more suitable for higher power systems, and have already been used in wind farms of over hundreds of kilowatts [15]-[17]. Despite this prominent advantage which is not possessed by lower order filters, inclusion of LCL-filters with three-phase voltage-source inverters (VSIs) is found to complicate the overall control design because of resonance and its related stability issues.

To provide a solution, this chapter first explores the inherent damping characteristic of an LCL-filter and specifically shows that the current control loop has an inherent damping term embedded when the converter current is sensed for feedback. This inherent damping term can be used for damping of the LCL resonance without the

need for additional passive or active damping, so long as the filter component values are designed appropriately. Such inherent damping unfortunately does not exist when the grid current is measured for feedback control, hence leading to the general conclusion that converter current feedback is more stable than grid current feedback.

Upon drawing that conclusion, the next practical issue to address is the likely deviation of passive element values caused by aging, temperature variation and system uncertainty. The immediate influence brought by such deviation is an elevated difficulty in achieving optimum damping, especially if only the inherent damping characteristic of converter current feedback is relied on. To compensate for such practical reality, a simple approach for tuning the damping factor is proposed, which would preserve the advantage of using only one set of current sensors, but at the expense of a more compromised transient response. Simulation and experimental results for validating those findings are eventually provided near to the end of the chapter.

5.2 System Modeling and Description

For illustration, Fig. 5-1 shows the typical circuit diagram of a three-phase VSI connected to the grid through an LCL-filter, whose equivalent series resistances (ESRs) of its converter-side inductor L_{inv} , grid-side inductor L_g and filter capacitor C_f are all neglected here. Not including ESRs would in principle nullify all internal damping, causing the idealized system to be more unstable. Another assumption made here is

Fig. 5-1. Three-phase grid-connected inverter with an LCL-filter.

that the ac supply voltages contain only positive-sequence fundamental component, which then means that they can be treated as short-circuits with zero impedance when performing system stability and harmonic analyses. With both assumptions incorporated, Fig. 5-1 simplifies to the per-phase equivalent circuit shown in Fig. 5-2, whose s -domain transfer functions, representing the plant model $G_p(s)$ at non-fundamental frequencies, can be readily derived as,

$$G_p(s) = \frac{I_g(s)}{V_{inv}(s)} = \frac{1}{L_{inv}L_gC_f s^3 + (L_{inv} + L_g)s} \quad (5.1)$$

$$\frac{I_c(s)}{I_g(s)} = L_g C_f s^2 \quad (5.2)$$

where v_{inv} , i_g and i_c represent the converter pole voltage, grid current and filter capacitor current in the time domain, respectively, while their capitalized notations are for representing them in the s -domain.

Moving next to the pulse-width modulated (PWM) converter, it is now well-accepted that the power stage can be modeled as a linear amplifier with transport and sampling delays caused by the nonlinear modulation process [19]. One recommended way of modeling the delays is to treat them as first-order low pass terms, whose amplitude falls at 20 dB/dec. Such reduction is however not created by the actual delay terms, which then means that the first-order model is not suitable for analysis performed at higher frequencies. Instead, it is noted that the main impact introduced by delays is to significantly reduce the system phase over the full frequency range, which certainly

Fig. 5-2. Simplified per phase equivalent circuit for stability analysis.

can be accounted by dropping the phase of the open loop transfer function derived with the PWM converter treated as a pure amplifier gain. This gain needs not be drawn explicitly, but can be combined with the current regulator, whose transfer expression in the synchronous dq frame is written in (5.3).

$$G_c(s) = K_p V_{dc} \left(1 + \frac{1}{\tau_c s}\right) \quad (5.3)$$

Equation (5.3) is a proportional-integral (PI) controller with K_p , τ_c and V_{dc} representing its proportional gain, integral time constant and half the dc-link voltage, respectively.

5.2.1 Grid Current Feedback

Fig. 5-3(a) shows the control block diagram of LCL-filter-based three-phase VSIs with grid current feedback. Combining (5.1) and (5.3), it is easy to derive the system open loop gain as,

$$\frac{I_g(s)}{I_e(s)} = G_c(s)G_p(s) = \frac{K_p V_{dc} (s + 1/\tau_c)}{L_{inv} L_g C_f s^4 + (L_{inv} + L_g) s^2} \quad (5.4)$$

where i_e represents the current reference in the time-domain, and its capitalized notation denotes the s -domain. Apparently, the third-order term in the characteristic equation is absent, indicating that the overall closed-loop system is unstable. Even if the ESRs of passive elements are included, they are generally insufficient to guarantee a well-damped plant. The plant response is thus dynamically slow with a small control bandwidth. Improvement to it can only be introduced by adding either external passive or active damping to limit the otherwise infinite gain at the LCL resonance frequency.

5.2.2 Converter Current Feedback

The converter current can alternatively be sensed for feedback control as shown in Fig. 5-3(b). Since the grid current is not directly controlled, the q -axis current reference should be set to $\omega_o C_f \mathcal{V}_g$ instead of zero, where ω_o is the fundamental angular frequency.

This is to again ensure unity power factor operation immediately before the grid terminal. Although Fig. 5-3(b) accurately represents the system, its adoption for open-loop stability analysis is not convenient because the feedback variable is tapped from the middle of the open-loop path rather than at the end. This fortunately can be resolved by noting that the converter current can be expressed as the summation of grid current and filter capacitor current, which upon incorporated, gives rise to the modified control block diagram shown in Fig. 5-3(c). Comparing Fig. 5-3(c) with Fig. 5-3(a) now would reveal that converter current feedback is equivalent to grid current feedback, except for an additional $-i_c$ term added to the forward path of the former.

Using this modified notation, it is easy to obtain the following relationship,

$$\frac{I_g(s)}{I_e(s) - I_c(s)} = G_c(s)G_p(s) = \frac{K_p V_{dc}(s + 1/\tau_c)}{L_{inv}L_g C_f s^4 + (L_{inv} + L_g)s^2} \quad (5.5)$$

Substituting (5.2) to (5.5) and performing slight manipulation then yields,

$$\frac{I_g(s)}{I_e(s)} = \frac{K_p V_{dc}(s + 1/\tau_c)}{L_{inv}L_g C_f s^4 + K_p V_{dc}L_g C_f s^3 + (K_p V_{dc}L_g C_f / \tau_c + L_{inv} + L_g)s^2} \quad (5.6)$$

Comparing the denominators of (5.4) and (5.6), it is clear that the latter has an additional s^3 term, which would provide damping by shifting two of its poles further into the left half plane, while the remaining two poles remain at the origin. The extent of damping introduced can be tuned by adjusting the controller gains and passive parameters to size the coefficient of s^3 found in the denominator of (5.6) appropriately. As an example, to arrive at a damping factor of $\zeta = 0.707$ recommended in most control texts, tuning should be done until the following condition is met.

$$\frac{K_p V_{dc}}{L_{inv}} = 2\zeta\omega_{res} = 2\zeta \sqrt{\frac{K_p V_{dc}L_g C_f / \tau_c + L_{inv} + L_g}{L_{inv}L_g C_f}} \quad (5.7)$$

where ω_{res} , being the undamped resonance frequency, has been replaced by the relatively complex square-root term written on the right of (5.7). Since the integral term of the PI controller usually does not impact the resonance frequency significantly,

Fig. 5-3. Block diagram of (a) grid current feedback control, (b) converter current feedback control, (c) equivalent converter current feedback control and (d) modified equivalent converter current feedback control.

this expression can be further simplified as,

$$\omega_{res} \approx \sqrt{\frac{L_{inv} + L_g}{L_{inv} L_g C_f}} = \frac{1}{\sqrt{L_p C_f}} \quad (5.8)$$

where L_p represents the parallel value of L_{inv} and L_g . Regardless of the expression used, (5.7) and the descriptive text presented here clearly prove that inherent damping does exist when converter current feedback is used for controlling the LCL-filtered system,

hence indicating its superiority over grid current feedback.

The system stability under these two control strategies was also investigated in [99], using discrete root loci plots. However, it is found that the root loci plots under converter current control only concern the response of converter-side current. The filter capacitor C_f and grid-side inductor L_g after converter current may form an LC network, and it can also influence the response of final control output, which is the grid current. So, it might not be a fair comparison if different outputs are defined in the stability analysis. Moreover, as stated in [100], the system stability is very sensitive to the parameters of LCL-filter and its control sampling frequency, so it is very difficult to properly damp the LCL resonance using pole-zero cancellation method. In that case, genetic algorithms can be used to find an optimal active damping solution, which certainly increases the control complexity [100].

5.3 Damping Control of LCL-Filters

Previous research works on LCL-filtered systems have usually made the assumption that the filter can be approximated by an inductor, whose value is written as $L = L_{inv} + L_g$ in the low frequency range towards the left of the resonance frequency. This helps to simplify the PI current controller design, but it unfortunately is true only when considering the magnitude response, as reflected by the Bode plots printed in Fig. 5-4. From those plots, it is clear that the LCL-filter has roughly the same magnitude response as an L filter over the low frequency range and under various damping factors. Their phase response are however quite different with the maximum phase lag of an L filter being $\pi/2$ radius, while that of an LCL-filter always exceeding this value. The amount in excess of the LCL-filter would grow larger as the damping factor and operating frequency increase.

Fig. 5-4. Bode plots of LCL-filters under different damping factors.

Because of the differences in phase, the first design recommendation suggested here is to properly tune the damping factor of LCL resonance. Proper damping control is deemed as important since an under or lightly damped system will lead to serious transient oscillations when excited by a step change, while an over damped system will severely decrease the system phase margin, and hence dynamic response. The second recommendation made here is closely related to the dependency of the system crossover frequency with reference to its damping factor and resonance frequency. In [99], it is suggested that ω_c should be placed around one fifth of the converter switching frequency ω_s , but the understanding deduced from Fig. 5-4 is that ω_c is mainly limited by the phase lag of the LCL-filter, inferring that a better guideline is to select ω_c as a fraction of the undamped resonance frequency ($\omega_c = \alpha\omega_{res}$). This phase lag ϕ_{LCL} is actually the function of its damping factor ζ and the ratio of crossover frequency to resonance frequency α , and can be calculated as follows,

$$\phi_{LCL} \approx \frac{\pi}{2} + \arctan\left(\frac{2\zeta\alpha}{1-\alpha^2}\right) \quad (5.9)$$

Based on the above recommendations, the possible tuning zone for ω_c is marked by the two vertical dotted lines added to Fig. 5-4(b), so it can reserve sufficient phase margins ($>50^\circ$) for the closed-loop control. When optimum damping of LCL resonance is considered ($\zeta = 0.707$), the recommended value of crossover frequency is $\alpha = 0.3$. In this case, the system may have an acceptable bandwidth and the phase lag introduced by the LCL-filter is about 0.64π (115°), which is not very severe degradation compared with that of an inductor filter (90°). Sometimes, the damping factor can be slightly decreased to 0.5 so that higher crossover frequency can be obtained and hence faster current control loop. This fact can be clearly visualized from the 3D plot shown in Fig. 5-5. Another important factor to be considered is that the system delays can considerably drop the phase margin in the high frequency range. In order to ensure a stable closed-loop control system, the proportional gain K_p of forward path controller cannot be high, and this is again the reason why the system control bandwidth must be designed in a relatively low frequency range as depicted by Fig. 5-4.

With ω_c now defined, it is now possible to design the optimum damping control for the LCL-filter. Referring back to Fig. 5-4, it is obvious that the magnitude response of

Fig. 5-5. Phase lag introduced by the LCL-filter as a function of damping factor and the ratio of crossover frequency to resonance frequency.

LCL-filter under various damping factors is basically the same as that of an L filtered system in the low frequency range. Therefore, it is reasonable to approximate this LCL-filter as a single L (where $L = L_{inv} + L_g$) to find the relationship between K_p and ω_c . According to [19], this relationship can be depicted by the following equation,

$$K_p \approx \frac{\omega_c L}{V_{dc}} = \frac{\omega_c (L_{inv} + L_g)}{V_{dc}} \quad (5.10)$$

Combining (5.7) and (5.10) gives the following relationship between L_{inv} and L_g ,

$$2\zeta L_{inv} = \alpha(L_{inv} + L_g)$$
$$\frac{L_{inv}}{L_g} = \frac{\alpha}{2\zeta - \alpha} \quad (5.11)$$

Equation (5.11) suggests a theoretical design criterion based on which resonance damping of LCL-filter can be achieved with its inherent damping characteristic. It should be noticed that the performance of resonance damping will not be affected by the proportional gain of PI controller as long as (5.11) is satisfied. Therefore, the system crossover frequency can be placed at a desired frequency range so that the system dynamic response is fast enough. Moreover, (5.11) also reveals that the filter capacitance will not impact the performance of resonance damping, so this value should be first determined in LCL-filter design as will be presented in a later section. Nevertheless, (5.11) is only used for proving the concept that it is possible to achieve proper damping control of LCL-filter through its own inherent damping characteristic. This design approach is however not recommended for practical implementation. On one hand, (5.11) usually leads to much smaller value on converter-side inductor ($L_{inv} : L_g = 3 : 11$ for $\alpha = 0.3$ and $\zeta = 0.7$), so it will not comply with the optimum design method of LCL-filter proposed in [20], [101], where it has been stated that the grid- and converter-side inductance should be same so as to maximize the filtering capability of inductors. In other words, it may inevitably increase the cost and volume of passive filtering elements. On the other hand, small converter-side inductance

directly translates into significant current ripples on the output of the inverter. This may result in very considerable losses in the inductor and cause serious overheating problem.

Following the design method proposed in [20], the converter-side inductance is then chosen to be equal to the grid-side inductance for a fixed total line inductance. In this case, the LCL-filter may have maximum harmonic attenuation capability but fail to satisfy (5.11). Therefore, additional damping terms must be incorporated to adjust the coefficient of the second term in the denominator of (5.6) such that resonance damping control of LCL-filter can always be fulfilled regardless of the ratio of L_{inv} and L_g . A straightforward method to have a tunable damping factor is to measure the filter capacitor current and feedback to the current reference with a proportional gain k [102]. With this simple modification, the equivalent block diagram with converter current feedback control is shown in Fig. 5-3(d) which gives,

$$\frac{I_g(s)}{I_e(s) - (1+k)I_c(s)} = G_c(s)G_p(s) = \frac{K_p V_{dc}(s+1/\tau_c)}{L_{inv}L_gC_f s^4 + (L_{inv} + L_g)s^2} \quad (5.12)$$

Again, with (5.2) substituted into (5.12), the decoupled system open loop gain will be,

$$\frac{I_g(s)}{I_e(s)} = \frac{K_p V_{dc}(s+1/\tau_c)}{L_{inv}L_gC_f s^4 + (1+k)K_p V_{dc}L_gC_f s^3 + [(1+k)K_p V_{dc}L_gC_f / \tau_c + L_{inv} + L_g]s^2} \quad (5.13)$$

The second term of the denominator in (5.13) dominates the damping factor of LCL-filter and should satisfy the following relationship for optimum damping control.

$$2\zeta\omega_{res} = \frac{(1+k)K_p V_{dc}L_gC_f}{L_{inv}L_gC_f} = \frac{(1+k)K_p V_{dc}}{L_{inv}} \quad (5.14)$$

It should be noted that, in practical implementation, k is usually less than the value computed from (5.14), as the system internal resistance can also provide certain degree of damping to the LCL resonance.

Substituting (5.10) to (5.14) gives (5.15) for computing the feedback gain of i_c .

$$k = \frac{2\zeta L_{inv}}{\alpha(L_{inv} + L_g)} - 1 \quad (5.15)$$

As can be seen, even though the parameters of LCL-filters are predetermined and may fail to satisfy the design criterion specified by (5.11), proper damping of LCL resonance still can be accomplished via proper feedback control of filter capacitor currents as proposed in [103]. Nevertheless, this solution requires another set of current sensors to detect the filter capacitor current, which is a disadvantage. Moreover, since the current sensors are placed at capacitor and grid sides, the output current of the converter cannot be controlled directly, meaning that it is impossible to provide instantaneous over current protection to the PWM converter, while this feature is quite essential in practical implementation. To address these shortcomings, the proposed solution is to obtain the information of filter capacitor current from the measured converter current. Assuming that the LCL-filter is well designed and therefore the ripple currents in i_g are negligible. In this case, it is reasonable to use the filtered i_{inv} to approximate i_c since all the harmonics in i_{inv} are now absorbed by the filter capacitor, leaving only the fundamental component for i_g and this process can be simply realized by a second-order notch filter written as (5.16).

$$H(s) = \frac{s^2 + \omega_n^2}{s^2 + (\omega_n / Q)s + \omega_n^2} \quad (5.16)$$

where ω_n is the nominal angular frequency and Q is the quality factor that mainly determines the dynamic response and selectivity of this notch filter. In order to have a fast transient process without high oscillations, Q factor here is chosen to be 0.7 and its implementation is demonstrated in Fig. 5-6. It should be noted that the filtered i_{inv} is not exactly the same as i_c since i_c also contains a small portion of the fundamental reactive current. Fortunately, this approximation will not cause any problem to its damping performance, since the fundamental current in i_c is usually far away from the resonance frequency, and it will not excite any resonance. Moreover, when such fundamental component in i_c is directly added into the control loop, it may probably

can be adopted for this system is 3 kHz, which is low enough for most high power industrial applications. Moreover, per unit value will be used in the following design procedure so that it can facilitate the system scalability.

The basic electrical parameters of the system studied in this chapter are listed in Table 5-1. In this case, the system base impedance Z_b will be 9.6 Ω , and the base values for inductance L_b and capacitance C_b are found to be 31 mH and 332 μ F, respectively. Then, the per unit values of paralleled inductance x and filter capacitance y can be used for calculating the LCL resonance frequency as follows,

$$\omega_{res} = \frac{1}{\sqrt{L_p C_f}} = \frac{1}{\sqrt{x L_b y C_b}} = \frac{1}{\sqrt{x \frac{Z_b}{\omega_o} y \frac{1}{\omega_o Z_b}}} = \frac{\omega_o}{\sqrt{xy}} \quad (5.17)$$

Equation (5.17) shows that the values of passive elements are only associated with the ratio of fundamental frequency to resonance frequency. Applying $\omega_{res} = 30\omega_o$ to the above equation gives $xy = 0.0011$. Apparently, there are infinite solutions for this

Table 5-1. Specifications of the converter and parameters used for experimental testing.

Elements	Parameters	Values
Converter	Nominal power	1.5 kVA
	Switching frequency	5 kHz
	Deadtime	2 μ s
	Dc-link voltage	260 V
Grid	Grid voltage	120 V
	Line frequency	50 Hz
	Grid impedance + transformer leakage inductance	1.3 mH
LCL-filter	Grid-side inductor	1.3 mH
	Filter capacitor	15 μ F
Controller	Proportional gain	0.06
	Integral time constant	0.005
	Damping gain	1.2

equation, but [15] recommended that the value of filter capacitance should be limited to 5%. In this case, the value of paralleled inductance is 2.2%.

The first set of LCL-filter can then be designed based on (5.11). The converter- and grid-side inductance are calculated as,

$$\begin{aligned} L_{inv} &= \frac{2\zeta}{2\zeta - \alpha} L_p = 2.8\% L_b \\ L_g &= \frac{2\zeta}{\alpha} L_p = 10.3\% L_b \end{aligned} \quad (\text{for } \alpha = 0.3 \text{ and } \zeta = 0.7) \quad (5.18)$$

Finally, the parameters of LCL-filter are determined as $C_f = 15 \mu\text{F}$ (4.5%), $L_{inv} = 0.87 \text{ mH}$ (2.8%) and $L_g = 3.19 \text{ mH}$ (10.3%), and the proportional gain of current controller can also be found using (5.10).

Simulation was then conducted in MATLAB / PLECS environment to verify the effectiveness of the proposed design approach. The simulation software uses piecewise linearization technique to solve the nonlinear problems existing in complex power electronics systems, and dedicated solvers are employed by PLECS to expedite its simulation speed. The power converter models and control blocks are available from PLECS library, and all the parameters in simulation are chosen to be the same as those in the above design.

The simulated result is then presented in Fig. 5-7(a), where it is quite clear that the system can be kept stable under both steady and transient states. When the current reference is forced to jump from 5 A to 10 A, the inverter can response very fast and there is no oscillation or current overshoot observed during current step change, which successfully confirm the concept of inherent resonance damping of LCL-filter. To further prove the correctness of (5.11), another simulation was also performed to show the effect of “mismatch” of the two inductors by simply interchanging the values of L_{inv} and L_g ($L_{inv} = 3.19 \text{ mH}$ (2.8%) and $L_g = 0.87 \text{ mH}$ (10.3%)), while the filter

capacitance and system bandwidth are kept the same as the previous testing for performance comparison. Since this type of LCL-filter no longer satisfy the design criterion suggested by (5.11), the resonance of LCL-filter will be improperly damped, causing serious transient oscillations as can be visualized from Fig. 5-7(b).

(a)

(b)

Fig. 5-7. Simulated results of a three-phase inverter connected to the grid through an LCL-filter with (a) the proposed design method and (b) “mismatched” inductance.

As discussed previously, although this set of LCL-filter exhibits inherent damping characteristic of LCL resonance and gives quite simple current control, which can prove the theoretical analysis presented in this chapter, it is not suited for practical implementation. On one hand, the total inductance of LCL-filter exceeds 10% of the base value, which requires high value and cost of passive elements. On the other hand, small converter-side inductance leads to very large current ripples (approaching 8 A under nominal operation), as revealed by the simulation results shown in Fig. 5-7(a). This may result in significant power losses and even cause overheating of converter-side inductor. Therefore, this set of LCL-filter was not tested in experiment.

The design of the second LCL-filter is relatively simple and the inductance is equalized to achieve maximum filtering of switching harmonics. The final values of passive elements of LCL-filter are chosen as $C_f = 15 \mu\text{F}$ (4.5%), $L_{inv} = L_g = 1.36 \text{ mH}$ (4.4%). Again, only the converter current is measured for implementing the feedback control. Owing to the inherent damping characteristic of LCL-filter, the harmonic components in the converter current can help stabilize the system without relying on any other damping techniques. To achieve an optimally damped system, an additional damping term i_c must be estimated from i_{inv} and subsequently added into the control loop through a gain k to tune the damping factor. The calculation of k can be found by (5.15). Consequently, the simulated waveforms are presented in Fig. 5-8(a), where it is obvious that the grid current is well regulated under both steady-state and transient operations. The total harmonic distortion (THD) of i_g is less than 1%, and there is also no overshoot current observed in its dynamic process, confirming the good damping performance of the proposed control scheme. One observation to be highlighted here is that it takes roughly half line cycle for the grid current to reach the steady-state after current step-up change as shown in the fifth trace of Fig. 5-8(a). This relatively slow dynamic response is solely caused by the notch filter, which is used for extracting the harmonic components of converter current, rather than the current controller and will not raise any stability problem.

(a)

(b)

Fig. 5-8. Simulated results of LCL-filter-based inverter using (a) converter current control and (b) grid current control with insufficient passive damping.

For comparison, the grid current is next measured for feedback control. As explained in Section 5.2, it is now impossible to have a stable system due to the lack of resonance damping. Therefore, a $2\ \Omega$ resistor was intentionally inserted in series with the filter capacitor to perform passive damping. However, this value of resistance is still deemed as insufficient damping and transient oscillations in the grid currents are quite obvious as shown in Fig. 5-8(b).

5.5 Experimental Verification

A laboratory setup has also been constructed to experimentally confirm the performance of the proposed control schemes. The three-phase inverter was comprised of three insulated gate polar transistor (IGBT) modules from *Semikron* (SKM50GB063D), having two switches per module for forming a phase-leg. This type of IGBT can tolerate 600 V blocking voltage and pass continuous current up to 70 A. The inverter was interfaced to the utility grid (415 V line-line rms) through a 63.5 V / 220 V step-up transformer. The leakage inductance of the transformer together with the grid impedance was estimated to be 1.3 mH, using the measurement method described in [105], and it is treated as the grid-side smoothing inductor. The converter-side inductor is also chosen to be 1.3 mH, and a 15 μ F filter capacitor is inserted in parallel with them to form an LCL-filter. Further details about specifications and parameter values used for implementing the laboratory system can be found in Table 5-1 and the overall control implementation is described in Fig. 5-6.

The steady-state experimental results under converter current control are captured and shown in Fig. 5-9. As can be seen, the output current of LCL-filter is well regulated and the LCL-resonance has been successfully suppressed. Its harmonic spectrum is shown in Fig. 5-10, where it is clear that the magnitude of switching harmonics are very small, basically below 0.2% of the fundamental component. This confirms the superior filtering performance of LCL-filters. The THD of line current is measured to be 2.64%, which are mainly caused by the low order harmonics originated from the

Fig. 5-9. Steady-state experimental result of LCL-filter-based inverter using converter current feedback control.

Fig. 5-10. Harmonic spectrum of grid current measured under steady-state operation.

slightly distorted grid. There are commonly two ways to further suppress such background harmonics. A straightforward method is to feed forward grid voltage so that it can cancel out the effects of harmonics, as discussed in [106]. Alternatively, individual harmonic controller can be added in parallel with the PI controller to mitigate line current distortions, as shown in Fig. 5-6. Understanding that the grid voltage in a three-phase three-wire system is usually distorted by 5th and 7th such low order harmonics, which may become 6th order in the synchronous frame, the following resonant controller G_r tuned at the same frequency can therefore be used to simultaneously suppress both of them,

$$G_r(s) = \frac{K_r s}{s^2 + (6\omega_n)^2} \quad (5.19)$$

where K_r is the gain of generalized integrator which is similar to the integral gain of PI controller [5].

Moving on to test the dynamic response of the system, the current reference is now commanded to have a 5 A to 10 A step-up transient, and the captured result is shown in Fig. 5-11. It is observed that the output current can follow the reference jump closely and there is no overshoot current or transient oscillation in the entire dynamic process, which is in good agreement with the simulation result. Next, the current sensors are placed at the grid-side, and as similar to the previous simulation, a 2 Ω resistor is connected to the filter capacitor to help stabilize the system. Again, the same transient testing is conducted to examine its stability. Due to the inadequate damping of LCL resonance, this sudden load change now causes serious transient oscillation as clearly

Fig. 5-11. Experimental result of LCL-filter-based inverter subjected to a step-up load transient, obtained using converter current feedback control.

Fig. 5-12. Experimental result of LCL-filter-based inverter subjected to a step-up load transient, obtained using grid current feedback control with insufficient passive damping.

identified from Fig. 5-12, and moreover, the system appears to be marginally stable in steady state. In fact, if the value of this damping resistor is gradually decreased to zero, the inverter will turn out to be unstable even in steady-state operation, which is consistent with the theoretical analysis presented in this chapter.

5.6 Summary

This chapter provides an in-depth investigation of two different current control schemes for LCL-filter-based three-phase grid-connected inverters. It has been shown that feeding back the converter current will lead to a more stable closed-loop system contributed solely by the inherent damping characteristic of LCL-filter. A general design criterion for LCL-filter has also been derived, which upon fulfilled, will lead to proper resonance damping and the desired control bandwidth. However, if the LCL-filter fails to satisfy the design criterion due to system uncertainties or other design constraints, a simple solution has been presented to estimate the filter capacitor current, which can subsequently be used for tuning the damping factor. The main attractiveness of the overall control schemes designed is that they require only one set of current sensors for feedback control and resonance damping purposes, while yet not demanding for a complex state observer. Simulation and experiment have already confirmed all findings discussed.

Chapter 6 Control of Shunt Active Power Filters with LCL-Filters

6.1 Introduction

In previous chapters, the main functionality of three-phase PWM converters is to supply electrical power to the utility grid and customer loads. With some modifications introduced, these converters can also act as power conditioning devices for solving power quality problems in distributed generation (DG) systems. An attractive possibility is shunt active power filter (SAPF), implemented for eliminating harmonic current and improving power factor. SAPF is certainly not a new thought, but more a well-established conditioner that presently has many different control options like those derived from the well-known instantaneous reactive power theory [109]. However, most of the schemes discussed so far are for an L-filter-based SAPF. Advantages that an LCL-filter can bring to SAPF are therefore not yet properly defined, and control schemes for the resulting LCL-filter-based SAPF are presently not widely available.

Based on the above, the focus of this chapter is to apply concepts from Chapter 5 on LCL-filter to SAPF, whose overall design is expected to be more challenging because of the simultaneous need for resonance damping and harmonic tracking. To smoothen the design process, the basic model for an LCL-filter is first established in this chapter, which takes into account the phase lag introduced by the LCL resonance. Analysis of this model reveals that the maximum achievable system bandwidth is closely linked to the resonance frequency of the LCL-filter. A general design guideline is then proposed to ensure proper placement of the resonance frequency within an appropriate chosen range, so as to simultaneously achieve accurate harmonic compensation and optimum resonance damping without any trade-off noted between them.

Active damping, being more efficient, is also explicitly considered here for embedding within the control loop, so as to alter the plant transfer function to get a more well-damped system. A design example then follows, whose objective is to compensate for harmonic currents up to the 25th order in a 50-Hz three-phase three-wire power system. The designed system is next compared with its L-filter-based correspondence, designed to have equivalent ripple filtering. Through the comparison, an attractive advantage of the LCL-filter-based SAPF is identified for cases where high modulation index (e.g. ≥ 0.9) or low dc-link voltage is demanded, which so far has not been previously discussed. Simulation and experimental results for verifying this advantage, together with other performance improvements, are provided at the end of the chapter.

6.2 Mathematical Model of LCL-Filters

For illustration, Fig. 6-1 shows the typical circuit diagram of a SAPF implemented as a three-phase three-wire system. Between the SAPF and utility grid is an LCL-filter added for current smoothing. As similar to Chapter 5, a few assumptions are made here for simplifying the analysis. Foremost would be to assume that the three-phase voltages at the point of common coupling (PCC) are sinusoidal and balanced. That then means the grid can reasonably be treated as short-circuited when performing stability analysis in the high frequency range. In addition, all equivalent series resistances (ESRs) of passive components, including the converter-side inductor L_{ff} , grid-side inductor L_{gf} and filter capacitor C_f , are neglected, since they provide some degrees of resonance damping, and would thus raise the overall system stability. Ignoring ESRs therefore represents the “worst case” scenario in terms of damping, even though it represents the best case in terms of loss reduction. Applying these assumptions then leads to the model shown in Fig. 6-2(a) for representing the power stage of the SAPF, whose converter bridge has been represented by a gain of $V_{dc}/2$, as per previous practice.

Fig. 6-1. Overall circuit diagram of the proposed SAPF system with an output LCL-filter.

Fig. 6-2(a) can further be written as a set of transfer functions in the frequency-domain, as demonstrated by (6.1) and (6.2):

$$G_p(s) = \frac{I_{gf}(s)}{V_m(s)} = \frac{V_{dc} / 2}{L_{ff} L_{gf} C_f s^3 + (L_{ff} + L_{gf}) s} \quad (6.1)$$

$$\frac{I_{cf}(s)}{I_{gf}(s)} = L_{gf} C_f s^2 \quad (6.2)$$

where V_m is the normalized modulating signal, V_{dc} is the dc-link voltage, I_{gf} and I_{cf} are the currents injected into the grid and absorbed by the filter capacitor, respectively. Applying unity feedback control to (6.1) then results in a characteristic polynomial without the s^2 term. The overall closed-loop system is thus unstable or marginally stable according to the Routh's stability criterion, and would need additional damping to stabilize it.

Fig. 6-2. Plant models of (a) un-damped and (b) actively damped SAPFs.

So far, the mathematical derivations are exactly the same as those presented in Chapter 5, as it actually represents the original plant model of the LCL-filter. However, it should be noted that the damping control proposed in Chapter 5 cannot be applied to the LCL-filter-based SAPF system, because the filter capacitor contains low order harmonic currents which are very difficult to filter out. On the other hand, passive damping is also not considered due to its high power losses caused in the SAPF system. Instead, active damping is focused, which when applied, leads to the actively damped system shown in Fig. 6-2(b). In that figure, the filter capacitor current is sensed and added to the modulating signal through a damping gain K_d . The new transfer function is then written as:

$$\frac{I_{gf}(s)}{V_m(s) - I_{cf}(s)K_d} = \frac{V_{dc} / 2}{L_{ff}L_{gf}C_f s^3 + (L_{ff} + L_{gf})s} \quad (6.3)$$

Upon substituting (6.2) for $I_{cf}(s)$, the new plant model $G_{pd}(s)$ is derived as (6.4):

$$G_{pd}(s) = \frac{I_{gf}(s)}{V_m(s)} = \frac{V_{dc} / 2}{L_{ff}L_{gf}C_f s^3 + (V_{dc} / 2)K_d L_{gf}C_f s^2 + (L_{ff} + L_{gf})s} \quad (6.4)$$

With a finite s^2 term now introduced to its denominator, closed-loop stability of (6.4) can easily be tuned by varying the feedback gain K_d appropriately. Damping factor ζ , representing the extent of resonance damping, can also be tuned as:

$$2\zeta\omega_{res} = \frac{V_{dc}K_d}{2L_{ff}} = 2\zeta\sqrt{\frac{L_{ff} + L_{gf}}{L_{ff}L_{gf}C_f}} \quad (6.5)$$

where ω_{res} represents the LCL resonance frequency, determined solely by the passive component values. Substituting (6.5) into (6.4) then results in the following simplified damped system model:

$$G_{pd}(s) = \frac{V_{dc}}{2L_{ff}L_{gf}C_f} \cdot \frac{1}{s(s^2 + 2\zeta\omega_{res}s + \omega_{res}^2)} \quad (6.6)$$

Bode diagrams of (6.6) under various damping factors can now be plotted as in Fig. 6-3, using parameters listed in Table I. Also drawn are the first-order curves associated with a simple L-filter, whose inductance is set to $L_t = L_{ff} + L_{gf}$. Comparing the curves then leads to the general observation that the magnitude response of the LCL-filter approaches that of the L-filter in the low frequency range (below resonance frequency), regardless of the damping factor chosen. Their phase responses can however be quite different, which may significantly impact the system stability.

Fig. 6-3. Bode plot of (6.6) obtained using parameters listed in Table 6-1.

Table 6-1. System parameters used for simulation and experiment.

Elements	Parameters	Values
SAPF converter	Nominal power	2 kVA
	Switching frequency f_s	10 kHz
	Deadtime	2 μ s
	DC-link voltage V_{dc}	300 V
	DC-link capacitor C_{dc}	2200 μ F
AC power grid	Grid voltage V_g	173 V
	Line frequency f_n	50 Hz
	Grid impedance L_g	0.2 mH
LCL-filter	Grid side inductor L_{gf}	0.5 mH
	Converter side inductor L_{ff}	0.5 mH
	Filter capacitor C_f	5 μ F
Nonlinear load (see Fig. 6-1 for circuit)	Three-phase diode rectifier	---
	AC smoothing inductor L_l	1.5 mH
	DC load capacitor C_l	470 μ F
	DC nominal load R_l	75 Ω

Moreover, it is sensed that the control bandwidth cannot exceed or even be close to the resonance frequency, since it will create a 180° phase lag, whose resulting influence is an insufficient phase margin for closed-loop control. Non-negligible delays caused by sampling and modulation would also constrain the system crossover frequency ω_c , limiting it to be lesser than 0.3 times the resonance frequency ω_{res} , based on the region suggested in Fig. 6-3.

Defining α as $\omega_c/\omega_{res} \leq 0.3$ then leads to a phase lag of ϕ_{LCL} radians for the LCL-filter at ω_c , calculated as:

$$\begin{aligned}\phi_{LCL} &= \angle\{G_{pd}(j\omega_c)\} \\ &= \angle\left\{\frac{V_{dc}}{2L_{ff}L_{gf}C_f} \cdot \frac{1}{(j\omega_c)^3 + 2\zeta\omega_{res}(j\omega_c)^2 + \omega_{res}^2 j\omega_c}\right\} \\ &= \angle\left\{\frac{V_{dc}}{2L_{ff}L_{gf}C_f} \cdot \frac{1}{(j\alpha\omega_{res})^3 + 2\zeta\omega_{res}(j\alpha\omega_{res})^2 + \omega_{res}^2 j\alpha\omega_{res}}\right\} \\ &= \angle\left\{\frac{V_{dc}}{2L_{ff}L_{gf}C_f} \cdot \frac{1}{-2\alpha^2\zeta\omega_{res}^3 + (\alpha - \alpha^3)j\omega_{res}^3}\right\} \\ &= \pi - \arctan \frac{1 - \alpha^2}{2\alpha\zeta}\end{aligned}\tag{6.7}$$

When the damping factor of LCL resonance ζ is chosen to be 0.707 (a very typical value used for second order system), ϕ_{LCL} is calculated as 0.64π or 115° , which is not a very severe degradation, as compared to the value of 0.5π or 90° of an L-filter. Parameter ω_c or $0.3\omega_{res}$ should moreover be chosen much higher than the highest harmonic current compensated by the SAPF, so as to completely eliminate its interaction with the LCL resonance. The desired switching frequency can eventually be set, which according to [99], should be set at least two times of ω_{res} , so as to provide sufficient harmonic attenuation around the switching frequency.

6.3 Control of the Proposed SAPF Systems

Upon figuring out the relationships among system bandwidth, LCL resonance frequency and converter switching frequency, development of control algorithms for the LCL-filter-based SAPF can proceed. The resulting control block diagram is shown in Fig. 6-1, where active damping, harmonic current compensation and dc-link voltage control are all considered. Regarding active damping, it has earlier been demonstrated on LCL-filter-based SAPF in [109], [110], where the filter capacitor current was measured and fed to the inner current feedback control loop to imitate a virtual damping resistor. Although the controlled system can eventually be stabilized in the steady state, its damping gain at resonance frequency was not analytically determined,

Fig. 6-4. Root locus of (6.6) showing trajectories of closed-loop poles.

but rather obtained through trial and error. Proper guide on how to choose the damping gain is therefore absent, implying that optimal damping of the LCL-filter cannot be guaranteed. This is clearly confirmed by the dynamic results presented in [110], where obvious current oscillations and overshoots can be seen. Proper sizing of the damping gain is therefore important, and is precisely determined here by using the plant model in (6.4) and (6.5) to arrive at (6.8):

$$K_d = \frac{4\zeta}{V_{dc}} \sqrt{\frac{L_{ff}(L_{ff} + L_{gf})}{L_{gf}C_f}} \quad (6.8)$$

where K_d is shown to be proportional to the damping factor ζ , whose value can freely be tuned to arrive at the desired damping response.

Referring next to (6.6), the general observation noted is that the damped LCL network has a pair of conjugate complex poles in the left half plane and another pole at the origin. The locations of these poles, and hence the system response and performance, can be varied by applying unity feedback, and then tuning the proportional gain K_{pc} of the current controller. Theoretically, a large proportional gain would force the real closed-loop pole to move further away from the imaginary axis, hence attenuating the

Fig. 6-5. Step responses of closed-loop of $G_{pd}(s)$ and $G_s(s)$.

impact of this real pole and causing the two conjugate poles to dominate. The conjugate poles would also move closer towards the right half plane, causing the system to gradually become unstable. The described pole trajectories are shown by the root locus of (6.6) plotted in Fig. 6-4, which also shows the closeness of the poles, even though they are gradually moving apart, as K_{pc} increases. The impact of the real pole therefore cannot be neglected, but should be understood by comparing the step response of the closed-loop system with the following second-order system $G_s(s)$ at different damping factors:

$$G_s(s) = \frac{\omega_{res}^2}{s^2 + 2\zeta\omega_{res}s + \omega_{res}^2} \quad (6.9)$$

The results are plotted in Fig. 6-5, where a feature noted with the real pole is its slowing down of the overall step response, hence leading to a longer settling time. This real pole however damps transient oscillations more forcefully, leading to smaller overshoots at all damping factors. Based on these observations, a recommended value for ζ with active damping incorporated is 0.7, since it leads to a smooth system recovery with no noticeable overshoot and an acceptably short response time. At times, ζ can also be chosen slightly smaller, like 0.5, to introduce a safer phase margin (see Fig. 6-3), but slightly higher overshoot. Further reduction of ζ is however not recommended, since it will not improve the phase response too much, but only lead to even serious oscillations, as seen in Fig. 6-5. Upon deciding on the value of ζ , K_d can then be determined using (6.8) without much difficulty.

Proceeding on to the inner current control loop, its responsibilities are clarified as power flow regulation and harmonic current compensation. Unlike those methods proposed in [111], where both nonlinear load and SAPF currents were sensed, only the line currents are measured here, and controlled to be balanced and sinusoidal. One set of current sensors, together with the load harmonic extraction module for generating the SAPF reference currents, are therefore eliminated, leading to a simpler control implementation. For unity power factor operation, the reactive grid current reference should further be set to zero, while using the following proportional-integral (PI) controller in the synchronous dq frame for forcing the grid current to track an active reference per phase:

$$G_{cf}(s) = K_{pc} \left(1 + \frac{1}{\tau_c s}\right) \quad (6.10)$$

where K_{pc} and τ_c are respectively the proportional gain and integral time constant. As K_{pc} dominates the bandwidth of the inner current control loop, its value must properly be chosen to ensure that ω_c falls well within the frequency range discussed in Section 6.2, and indicated in Fig. 6-3. For that, the following equation can be used for calculating K_{pc} [19], after deciding on the value of $\omega_c (= 0.3\omega_{res}$, as explained earlier):

$$K_{pc} \approx \frac{\omega_c L_t}{V_{dc} / 2} = \frac{\omega_c (L_{ff} + L_{gf})}{V_{dc} / 2} \quad (6.11)$$

The value of τ_c , on the other hand, mainly determines the fundamental steady-state tracking error, and should therefore be small. A conservative value recommended for it to avoid impacting on system stability, like the reduction of phase margin, is given in (6.12):

$$\angle\{G_{cf}(j\omega_c)\} = 90^\circ - \arctan \omega_c \tau_c \approx 2^\circ \quad \text{and} \quad \tau_c \approx 30 / \omega_c \quad (6.12)$$

It should also be noted that adding this PI controller in the current control loop will introduce an additional pair of zero and pole to the closed-loop response. These added terms are however close to each other, allowing their effects to cancel out. The overall

system response would therefore still be dominated by those three poles indicated in Fig. 6-4.

Adding on to the fundamental current regulation is the compensation for harmonic currents, which can be implemented in the synchronous dq frame by using multiple paralleled resonant controllers, expressed as (6.13):

$$G_{ch}(s) = \sum_{n=1}^k \frac{K_{ih}s}{s^2 + (n\omega_n)^2} \quad (6.13)$$

where ω_n , K_{ih} and k represent the nominal angular frequency, respective resonant gain and highest harmonic order that can be compensated. Rather than (6.13), resonant controllers placed in the stationary frame can also be used, but would result in more terms for summation. This is explained in [7] where it is shown that a resonant controller in the synchronous frame is more effective, since it represents two equivalent resonant terms in the stationary frame for compensating two harmonics. Other details on the discretization and optimization of the resonant controllers can be found in [7], and are therefore not explicitly elaborated here.

Returning back to k in (6.13), its value should rightfully be much smaller than the specified resonance frequency. That then corresponds to the low frequency range shown in Fig. 6-3, where as mentioned earlier, would cause the LCL-filter to behave like a small inductance. Output current produced by the SAPF in this range can therefore be of high slew rate for tracking the harmonic reference accurately. A first-order L-filter, designed to produce the same switching ripple filtering, would not be able to respond that fast because of its larger inductance. A possible solution for it is to tune up its controller proportional gain to maximize the system bandwidth. This however is quite hard to achieve in reality, since it can lead to unwanted noise amplification, and hence instability.

Moving next to the outer voltage control loop of the SAPF converter, the responsibility of this outer voltage control loop is to keep the dc-link capacitor voltage constant by

compensating for active power losses in the system. Its realization can therefore be just the stationary-frame PI controller $G_v(s)$ written in (6.14), whose high dc gain would force the tracking error to zero:

$$G_v(s) = K_{pv} \left(1 + \frac{1}{\tau_v s} \right) \quad (6.14)$$

where K_{pv} is the proportional gain, and τ_v is the time constant of the integral term. $G_v(s)$ here must rightfully be designed to be much slower than the current controller $G_c(s)$ ($= G_{cf}(s) + G_{ch}(s)$), so as to avoid interference between them.

Another feature exhibited by the dc-link control loop is its lower dc voltage requirement. This is possible for the LCL-filter, since its total inductance is much smaller, and hence the unfiltered converter output needs to compensate for only a much smaller voltage drop across it. The dc-link voltage can therefore be reduced, while yet maintaining the same high modulation index that is less prone to over-modulation. This is however not true for the L-filter-based SAPF, which always requires a larger inductance, and hence a larger voltage drop across it. Being applied to SAPF also leads to a more prominent voltage drop, since it deals with sizable harmonic currents flowing through sizable inductive impedance that is k times larger than the fundamental. In contrast, similar effects experienced by grid-tied inverters and rectifiers would likely be less obvious, since they deal with fundamental currents and inductive impedances only.

6.4 Generalized Design Procedure and Example Design

Based on reasons discussed earlier about parameter sizing, the generalized design procedure for LCL-filter-based SAPF is now presented in per-unit terms for easier future system scalability. The procedure would quite expectedly begin by defining the highest order harmonic current k that needs to be compensated. According to Section 6.2, the cutoff frequency ω_c and resonance frequency ω_{res} should then be larger than

$k\omega_n$ and $k\omega_n / 0.3$, respectively (ω_n being earlier defined as the nominal fundamental frequency). To be slightly more conservative so as to fully avoid interference between harmonic current compensation and resonance damping, the resonance frequency can instead be set to:

$$\omega_{res} = k\omega_n / 0.25 = 4k\omega_n \quad (6.15)$$

To cater for sufficient switching harmonic suppression, the desired switching frequency of the converter can be set two times larger than the LCL resonance frequency. Even higher switching frequency can of course be used for better harmonic attenuation, but would incur additional losses, and therefore not firmly recommended. With ω_{res} now decided, the filter component values can follow up be determined, but before progressing ahead, some base inductance L_b and capacitance C_b values need to be defined for per-unit representation. These bases are written as:

$$\begin{aligned} L_b &= Z_b / \omega_n \\ C_b &= 1 / \omega_n Z_b \end{aligned} \quad (6.16)$$

where Z_b is the base impedance calculated by dividing the system rated power from the square of its rated voltage.

Noting also that the grid and converter-side inductances should be set equal to produce the lowest resonance frequency, and hence the maximum switching harmonic attenuation, the set of filter parameters recommended should be:

$$\begin{aligned} L_{ff} = L_{gf} &= xL_b = xZ_b / \omega_n \\ C_f &= yC_b = y / \omega_n Z_b \end{aligned} \quad (6.17)$$

where x and y are the per unit inductance and capacitance, respectively, which are usually chosen below 5% to bring down the system cost. Substituting (6.17) to (6.5), followed by some simple manipulation, then leads to:

$$xy = 2(\omega_n / \omega_{res})^2 = 2(1/4k)^2 \quad (6.18)$$

Apparently, (6.18) has infinite solutions, but it is recommended here that the total per unit value of the two inductors should be chosen equal to that of the filter capacitor,

hence yielding:

$$\begin{aligned} L_{ff} = L_{gf} &= (1/4k)L_b \\ C_f &= (1/2k)C_b \end{aligned} \quad (6.19)$$

The closest commercially available capacitance value should then be chosen, while the inductance value can be wound accordingly. If desired, the actual realized resonance frequency can be calculated using these final chosen reactive values, and should roughly match the value recommended in (6.15) for the design. The reactive values, together with the chosen damping factor ($0.5 \leq \zeta \leq 0.7$), cutoff frequency ω_c and dc-link voltage V_{dc} , can next be substituted to (6.8), (6.11) and (6.12) to determine the important control parameters of K_d , K_{pc} and τ_c , respectively. Other control parameters like K_{ih} in (6.13) for harmonic current compensation, and K_{pv} and τ_v in (6.14) for dc-link voltage regulation can be tuned based on classical outer loop control and zero tracking error operating principles. These are well-established and therefore not explicitly shown here.

The above design procedure can now be applied to an example SAPF, whose objective is to compensate up to the 25th harmonic current ($k = 25$) in a 173-V (line-to-line RMS), 2-kVA, 50-Hz three-phase three-wire system. From (6.15), the resonance frequency should rightfully be chosen as $1250 / 0.25 = 5000$ Hz or a value between $1250 / 0.3 = 4167$ Hz and 5000 Hz. Since the desired switching frequency should be at least two times larger than the resonance frequency, its value should be fixed to 10 kHz or more. Using (6.16), the base inductance and capacitance values can next be calculated as 47.8 mH and 212 μ F, respectively. Substituting these bases and $k = 25$ to (6.19) then leads to the calculated values of 0.478 mH and 4.24 μ F for the LCL-filter. Based on available commercial values, the final LCL parameters are chosen as $C_f = 5$ μ F and $L_{ff} = L_{gf} = 0.5$ mH, giving a re-calculated resonance frequency of $f_{res} = \omega_{res} / 2\pi = 4504$ Hz, which indeed falls within the range from 4167 Hz to 5000 Hz that has earlier been identified. Using these reactive parameters, together with $\zeta = 0.5$, $\omega_c =$

8485 rad/s and $V_{dc} = 300$ V, the corresponding control parameters are eventually determined as $K_d = 0.09$, $K_{pc} = 0.05$, $\tau_c = 0.0035$ s, $K_{ih} = 20$, $K_{pv} = 0.2$ and $\tau_v = 0.04$ s.

6.5 Simulation Results

A simulation study was conducted with Matlab / Simulink and PLECS, based on the system shown in Fig. 6-1. The aim was to examine the performance of the proposed SAPF system, and to compare it with the conventional L-filter-based SAPF. The specifications of the designed SAPF and other system parameters were based on those derived in Section 6.4, and summarized in Table 6-1 for comprehensiveness. The ac line and dc-link voltages stated in Table 6-1 were found to give an approximate modulation index of $141 / 150 = 0.94$ for the SAPF converter, which indeed was a reasonably high value. Such a high value was used for proving the lower likelihood of entering over-modulation by the LCL-filter-based SAPF.

Beginning with Fig. 6-6 where the proposed SAPF was subjected to a 33% to 100% step-up nonlinear load change, the results show a smooth compensation of harmonic currents up to the 25th order. The total harmonic distortion (THD), calculated up to the 100th harmonic) of the full load grid current is in fact only 2.91%, even though the load THD is 44.20%. Modulating references in the last plot of Fig. 6-6 are also noted to vary below unity without entering over-modulation, even with a detected dip in dc-link voltage during the transient.

Fig. 6-6. Simulated results of LCL-filter-based SAPF when subjected to a 33% to 100% step-up load change.

Fig. 6-7. Simulated results of L-filter-based SAPF when subjected to a 33% to 100% step-up load change.

For comparison, the LCL network was next replaced by a 5 mH inductor, followed by a retuning of the current controller gains to produce the same dynamic response, as per the previous simulation. Subjecting the L-filter-based SAPF to the same load transient then results in Fig. 6-7, where a prominent increase in modulation index is observed with larger power flow. The increase is for compensating the larger voltage drop across the L-filter and transient dip in dc-link voltage. That pushes the system into over-modulation like the example illustrated here, whose eventual effect is a set of distorted grid currents with THD as high as 7.79%.

6.6 Experimental Results

To validate the proposed SAPF system practically, a prototype was built in the laboratory, based on the same parameter values listed in Table 6-1 and circuit connection shown in Fig. 6-1, as per earlier used for simulation. The first set of experimental results obtained is shown in Fig. 6-8, during which the proposed SAPF is supplying 100% nominal load power in the steady state. As anticipated, the SAPF compensates the load harmonic currents well, giving rise to smooth sinusoidal currents drawn from the grid with a THD of only 3.49%. This is despite the load currents being heavily distorted with a THD of 40.37%. Also shown in the last plot of Fig. 6-8 is the modulating reference for one phase of the SAPF, being fully within the shaded linear modulation range.

The same demanded performance is shown in Fig. 6-9, where a step load transient from 33.3% to 100% of nominal load is intentionally triggered. This sudden increase in harmonic currents causes the dc-link voltage V_{dc} to drop to 279.2 V, which due to limited channels available on the digital scope, is not explicitly shown here. Experimental waveform for the dc-link voltage will be presented in a later section of the thesis (see Fig. 7-15) to prove that the dc bus voltage of the power converter is indeed supported by electrolytic capacitors rather than simply by a dc power supply or batteries, and the resulting power converter requires a dual loop controller design as

Fig. 6-8. Experimental steady-state results of LCL-filter-based SAPF.

Fig. 6-9. Experimental results of LCL-filter-based SAPF when subjected to a 33% to 100% step-up load change.

discussed earlier in Section 6.3. This voltage drop under an undisturbed ac grid would cause the modulation index to rise to approximately $141/139.6 \approx 1.01$, which although is slightly greater unity, would still not lead to over-modulation problem. The reason is partly due to the low series impedance of the LCL-filter and partly due to the presence of triplen offset that can clearly be seen added to the modulating reference of each phase. Transient events are therefore mostly ridden through smoothly with no obvious harmonic distortion sensed from the line current. For further demonstrating that the proposed SAPF meets international standard, low-order harmonic spectrum of the resulting grid current under nominal load condition is plotted in Fig. 6-10, which undeniably shows that the IEEE 519-1992 standard has been met comfortably.

The output filter of the SAPF was subsequently replaced by a 5-mH inductor, and re-tested under the same experimental conditions. Fig. 6-11 shows the steady-state experimental results, where slight over-modulation is observed under nominal load operating condition. This over-modulation is caused by the need to compensate for a larger voltage drop across the filter impedance, while yet keeping the same low dc-link voltage. Its extent can in fact worsen under transient conditions, like the 33% to 100% load step change shown in Fig. 6-12. The corresponding effect is of course a distorted grid current, whose low-order spectrum under nominal load condition is shown in Fig. 6-10. The spectrum undoubtedly shows poorer performance than the IEEE standard with its THD of 7.86% in excess of the normal 5% limit. Adding on to these

Fig. 6-10. Grid current spectrum versus IEEE 519-1992 standard.

Fig. 6-11. Experimental steady-state results of L-filter-based SAPF.

Fig. 6-12. Experimental results of L-filter-based SAPF when subjected to a 33% to 100% step-up load change.

Fig. 6-13. Harmonic spectrum of grid current in high frequency range.

inferiorities is its poorer switching ripple filtering, even after increasing its filter inductance to be five times larger than that of the LCL-filter. The corresponding results are shown in Fig. 6-13, where the switching and associated sideband harmonics are plotted for both L-filtered and LCL-filtered SAPFs. The results indeed show the former having poorer filtering performance, especially at high frequency.

6.7 Summary

In order to solve power quality problems, this chapter presents the design, control and implementation of an LCL-filter-based SAPF system, which can effectively compensate for harmonic currents produced by nonlinear loads in a three-phase three-wire power system. With an LCL-filter added at its output, the proposed SAPF

offers superior switching harmonic suppression using much reduced passive filtering elements. The output currents of this SAPF system thus have high slew rate for tracking the targeted reference closely. Smaller inductance of the LCL-filter also means smaller harmonic voltage drop across the passive output filter, which in turn minimizes the possibility of over-modulation, especially for cases where low dc-link voltage or high modulation index is desired.

These advantages, together with the overall system stability, are guaranteed only through proper consideration of critical design and control issues, like the selection of LCL parameters, interactions between resonance damping and harmonic compensation, bandwidth design of the closed-loop system, and active damping implementation with fewer current sensors. The formulated design concerns and generalized procedure are eventually applied to an analytical example. Simulation and experimental results provided clearly prove the example and hence excellent performance of SAPF designed by the proposed procedure.

Chapter 7 One-Cycle Controlled Active Rectifiers with LCL-Filters

7.1 Introduction

Unlike earlier chapters where grid-tied inverters are considered, Chapters 7 and 8 deal with nonlinear one-cycle control (OCC) of active rectifiers. OCC can certainly be applied to grid-tied inverters and other applications, but rectifiers are explicitly considered here simply because they present tougher control problems to the OCC controller. The reason being OCC controller requires the processing of dc-link voltage, which is from a dc micro-source or well-regulated front-end DC / DC converter for a grid-tied inverter, and hence almost constant. In contrast, dc voltage for a rectifier is internally regulated, and appears across a dc-link capacitor. That means the sensed dc voltage is likely to have ripples, whose extent depends on the switching frequency, control scheme and dc-link capacitance. Having ripples in the dc voltage is definitely a tougher challenge for the OCC controller to address.

Certainly, linear control algorithms like PI, PR and repetitive control can also be used in an AC / DC rectifier, but a fast digital signal processor (DSP) is usually needed for high-bandwidth performance and hence faster dynamics. Another disadvantage shared by linear controllers is the explicit requirement for a phase-locked loop (PLL) circuit or other complex current phase observers [113]-[115] needed for generating the inner loop current reference. Besides computation burdens, such entities can slow down the system response considerably. For example, a single-phase AC / DC rectifier would take at least two line cycles for the PLL to reach its steady-state when the system is subjected to grid disturbances like frequency deviation, phase angle jump and voltage sag [116]. This delay causes errors during reference generation, which might not be acceptable to sensitive loads. Another concern with linear controllers is that under

unbalanced grid conditions, low pass filters (LPF) should be added to the synchronous reference frame for blocking second order harmonics. This can significantly reduce the system bandwidth [117], causing slow transient response.

To avoid the PLL, this chapter presents an improved OCC scheme tested on an active rectifier with an input LCL-filter. The goal is to present a systematic investigation of OCC, which is especially important for systems in the range of several kilowatts and switching at 5 kHz or lower. The reason being a number of assumptions earlier made for conventional OCC becoming invalid at such a low switching frequency. To ensure that, this chapter begins by reviewing conventional single-edge OCC control when applied to a single-phase active rectifier operating at a high switching frequency and with an inductive filter. While reviewing, a number of OCC features that will likely create problems in a three-phase system are elaborated, before appropriate solutions are proposed for solving them. Techniques for avoiding instability, operating limit and resonance are also discussed in details, before the performances of the proposed OCC schemes are verified experimentally on a scaled-down laboratory prototype.

7.2 Single-Phase OCC PWM Rectifiers

OCC was originally designed for DC / DC converters, operating with a fast dynamic response and robust disturbance rejection [69]. It was subsequently modified for single-phase power factor correction (PFC) circuits and active rectifier control with the main objective being to achieve a unity power factor without requiring PLL circuits. The resulting OCC scheme is therefore simple, and can conveniently be implemented by using either a simple analog circuitry or a low cost microcontroller. These unique advantages of OCC control are now extended to a three-phase active rectifier, preceded by a third order LCL-filter. However, before that can be realized, basic operating principles associated with an OCC-controlled single-phase rectifier must be analyzed with likely problems expected in a three-phase system clearly stated for later reference.

7.2.1 Operating Principles

Beginning with the single-phase full-bridge rectifier shown in Fig. 7-1, [78] has clarified that the overall system can be controlled by classical double loop regulation structure. The dc-link capacitive voltage V_o and input grid current i_g are the two necessary control variables for performing OCC. It should be noted that for enhancing the system stability, especially under light load conditions, an additional voltage sensor is usually used to measure the grid voltage v_g , so that a fictitious current term can be obtained and added into the inner current control loop [80]. The overall control scheme is demonstrated in Fig. 7-2, where the dc-link voltage V_o is subtracted from its reference V_o^* and the voltage error is then passed through a proportional-integral (PI) regulator. Its main functionality is to force the input error to zero, as the system approaches its steady state. The bandwidth of this regulator is usually kept small to adapt to the slow dynamic response of the large dc-link capacitor. Output signal V_m from the PI regulator, representing

Fig. 7-1. Single-phase full-bridge active rectifier.

Fig. 7-2. Block diagram representing conventional single-edge OCC control scheme.

power (represented by character ‘ V ’ because measured electrical quantities are mostly converted to voltage signals in actual control circuits) consumed by the load, is then fed to an integrator, integrating with a time constant of $T_s/2$ and periodically reset by a clock with period of T_s . Depending on the actual integrator circuit adopted, the resulting integrated signal can either be a leading- or trailing-edge saw-tooth wave with a period of T_s , as illustrated in Fig. 7-3(a) and (b), respectively. Although the presence of a saw-tooth wave might at times create the impression that OCC control and traditional carrier-based modulation are similar, there in fact is a difference between them, since the former uses a carrier whose gradient is variable and depends on the current operating conditions, while the latter uses a constant-slope carrier.

In the inner control loop, the integrated signal is then compared with a reference signal expressed in terms of the fictitious current i_f and grid current i_g as follows (detailed derivation of (7.1) can be found in [80]).

$$V_m(1-2d) = R_s(i_f - i_g) \quad (7.1)$$

where R_s is the sensing resistance and d represents the duty ratio of SA’ and SB when the rectifier is commanded to switch in bipolar mode (ac output switches only between $+V_o$ and $-V_o$).

Referring back to the modulation process shown in Fig. 7-3 in slightly more detail, it is noted that the reference signal is drawn with some amount of high frequency switching ripple to be more realistic. The switching ripple is expressed as Δi_g , with the subscript ‘ g ’ used to clearly bring out the observation that ripple of reference $R_s(i_f - i_g)$ comes mainly from i_g , measured directly from the power stage, as illustrated in Fig. 7-2. Current i_f , on the other hand, has much smaller ripple since it is indirectly calculated by measuring the smoother grid voltage (especially for strong grid), before dividing it by the fictitious resistance R_f ($R_f = v_g / i_f$). Using this reasonably acceptable approximation and by noting that the main design criterion of OCC is to ensure that the modulation process is convergent within each switching cycle [78], the maximum value of the raising and

Fig. 7-3. Illustrations of waveform placements for (a) leading-edge, (b) trailing-edge and (c) double-edge OCC schemes.

failing slopes of the reference signals (K_1 and K_2 shown in Fig. 7-3) must be smaller than that of the integrated signal (or carrier). The expression governing stability for both the leading- and trailing-edge scenarios shown in Fig. 7-3 is then derived as,

$$\max(K_1, K_2) = \frac{R_s(\sqrt{2}v_g + V_o)}{L} < K_3 = \frac{2V_m}{T_s} \quad (7.2)$$

where L represents the filter inductance drawn in Fig. 7-1. To find the value of V_m , the following equation can be obtained based on the inductor voltage-second balance [78],

$$V_o(1-2d) = v_g = R_e i_g \quad (7.3)$$

where R_e represents the equivalent load resistance seen by the grid when viewing into the ac terminals of the single-phase rectifier. Substituting (7.3) into (7.1) and rearranging slightly then give rise to the following expression for V_m .

$$V_m = \frac{R_s(i_f - i_g)}{v_g} V_o \quad (7.4)$$

Further substituting $i_f = v_g / R_f$ and $i_g = -v_g / R_e$ into (7.4) then yields (7.5), which when used to replace V_m in (7.2), gives rise to the final stability criterion, expressed in (7.6) in terms of the system loading conditions.

$$V_m = \frac{R_s}{R_f // R_e} V_o \quad (7.5)$$

$$\frac{R_s(\sqrt{2}v_g + V_o)}{L} < \frac{2V_m}{T_s} = \frac{2}{T_s} \cdot \frac{R_s}{R_f // R_e} V_o \quad (7.6)$$

Analyzing (7.6), it is immediately clear that if the fictitious term R_f is not added, the right-hand resistive term simplifies to R_s / R_e , which becomes very small under light load conditions ($R_e \rightarrow \infty$). Satisfying (7.6) is thus not always possible, inferring that the overall system stability is severely degraded under light load conditions. According to [80], this degradation in stability can be resolved by including a finite fictitious term R_f to keep the limit in (7.6) at the non-zero value of $2R_s V_o / (T_s R_f)$, even if $R_e \rightarrow \infty$. Therefore, by properly selecting an appropriate value for R_f , the system can be kept stable at all times and over the full range of variation of R_e .

Although the above remedy does sound logical, its influence should nonetheless be kept small so as to minimize the amount of undesired current distortion caused by the direct feeding forward of grid voltage distortions, if detected in the grid (see control implementation of i_f in Fig. 7-2). Unfortunately, reducing i_f without compromising stability is at present not possible with the simple inductive filter shown in Fig. 7-1,

whose simplicity severely limits the degrees of control freedom available for tuning. This limitation is however not faced by the higher order LCL-filter studied in the next section, which happens to go against the common belief that as the filter order increases, the system stability becomes poorer, mainly caused by the presence of more resonant modes.

7.2.2 Summary of Limitations

From the above discussion of existing OCC control schemes, a few operating limits are sensed, and are respectively summarized as follows.

- The single-edge integrated signals produced by existing OCC schemes will unnecessarily give rise to additional semiconductor switching at all vertical transitional edges. This in fact is a shortcoming experienced by all saw-tooth modulation schemes.
- According to [32], the geometrical-wall-model technique can be used to prove that single-edge signals produce sizable amount of even harmonics in a phase-leg, which can be cancelled in a full-bridge converter if modulated properly. Such cancellation is however not possible in a three-phase system, meaning that some residual even harmonics with frequencies very close to the fundamental still exist, and can be very hard to filter (e.g. 2nd and 4th harmonics). These even harmonics can disturb the system stability, if they are unintentionally fed back for control purposes.
- As explained earlier, the fictitious term of $i_f = v_g / R_f$ in the OCC control equation is for raising the overall system stability, but it unfortunately causes distortion to the input current if the grid voltage happens to be distorted. Therefore, instead of solely relying on large i_f to maintain stability, other appropriate techniques should be explored, where possible.

Although some work on OCC control for three-phase systems can be found in [33], they mostly focus on only a single aspect and only for a simple inductive filter. To meet the

more stringent grid codes, three-phase rectifier with a higher order LCL-filter needs to be considered, which together with the concerns summarized above, formed the themes of investigation for this chapter.

7.3 Three-Phase OCC-Controlled Rectifiers with an Input LCL-Filter

The three-phase rectifier investigated is shown in Fig. 7-4, where an LCL-filter and a parallel dc load arrangement for emulating load step transient are explicitly shown. Surely, three of the existing single-edge OCC controllers can be used for controlling the rectifier, but as mentioned in Section 7.2, single-edge integrated signal is not explicitly optimized, and therefore not recommended, especially for cases where multiple resonant modes are present. To improve the rectifier performance, a few modifications concerning the integrated signal, LCL-filter parameter selection, feedback variable selection and damping techniques are suggested, and elaborated as follows.

7.3.1 Wave Shape of the Integrated Signal and Its Advantages

Instead of only leading or trailing edge, a sequence alternating them to produce the symmetrical double-edge pattern shown in Fig. 7-3(c) is considered an alternative with some favorable advantages in terms of performance and stability [78]. Viewing the three options again in more details in Fig. 7-3, the first difference noted among them is that

Fig. 7-4. Three-phase active rectifier with an input LCL-filter.

each semiconductor for the double-edge case needs to commute only once per leading or trailing time interval, unlike its saw-tooth counterparts where an extra commutation per phase always happens at each of the vertical transitional edges. The double-edge controlled rectifier therefore switches at half the original switching frequency, if the absolute rising and falling gradients are kept unchanged for the three plots shown in Fig. 7-3. If instead the same switching frequency is demanded for all three possibilities, the double-edge integrated signal must now be hastened to give a gradient that is two times the original. Because of its steeper gradient, double-edge OCC control is definitely stable, as long as its single-edge correspondences are proven stable according to (7.6).

Implementation wise, the recommended symmetrical integrated signal can be realized by integrating $(-1)^k V_m$ instead of simply V_m , where k represents a sampling count that will alternate every half switching cycle, and can readily be implemented by a phase-reversal analog switch. The alternated control input is then fed to an integrator, whose reset functionality might now appear redundant at first sight, since any upward accumulation when k is even is automatically followed by a winding-down process when k is odd in the next half cycle. Indeed, that can be the case if only steady-state condition is considered, but not when a transient event is encountered.

For illustration purposes, Fig. 7-5 shows the sequence of events happening when a load step-up transient (or other external disturbance) is triggered at the indicated time instant. Upon detecting the load transient through sensing of the dc-link voltage, the downward falling slope of the integrated signal changes its course immediately to the steeper trajectory path, as indicated in the figure. If not corrected promptly, the change in trajectory path would give rise to a constant (or slowly decaying in a practical circuit) dc offset shown in Fig. 7-5(a). On the other hand, with periodic reset still incorporated, the dc offset would be eliminated at the next immediate instant of reset, as shown in Fig. 7-5(b).

Fig. 7-5. Double-edge waveform illustrations (a) without and (b) with integrator reset during a load step-up transient.

7.3.2 Design of LCL-Filters

As mentioned earlier, a simple L-filter is not adequate for meeting stringent grid codes, especially for higher rated converters operating at reduced switching frequencies. Because of that, interest in LCL-filter is growing fast, especially for applications with direct interfacing to the grid. Following that trend of development, the three-phase rectifier studied here is also conditioned by a third-order LCL-filter, as indicated in Fig. 7-4. To demonstrate its characteristic ripple attenuation, the relevant input-to-output transfer functions are derived for the transfer block representation shown in Fig. 7-6, where the grid is short-circuited when considering harmonic frequencies only.

$$\frac{I_g(s)}{V_{rec}(s)} = \frac{1}{L_g L_{rec} C_f s^3 + (L_g R_{rec} + L_{rec} R_g) C_f s^2 + (R_g R_{rec} C_f + L_g + L_{rec}) s + (R_g + R_{rec})} \quad (7.7)$$

Fig. 7-6. Model of LCL-filter in the frequency domain.

$$\frac{I_g(s)}{I_{rec}(s)} = \frac{1}{L_g C_f s^2 + R_g C_f s + 1} \quad (7.8)$$

where V_{rec} , C_f , L_g , L_{rec} , R_g and R_{rec} represent the converter pole voltage, filter capacitance, grid-side inductance, converter-side inductance, and stray resistances of the respective inductors (capitalized notations are used in the transfer functions for representing variables in the s -domain). Notice that the grid impedance should be considered together with L_g and R_g when designing the LCL-filters and the controllers. This point is especially true for weak ac grid, where the grid impedance cannot be neglected. Analyzing (7.7) with R_g and R_{rec} neglected, the resonant frequency of the LCL-filter can be derived as,

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{L_g + L_{rec}}{L_g L_{rec} C_f}} = \frac{1}{2\pi \sqrt{L_p C_f}}, \quad L_p = L_g // L_{rec} \quad (7.9)$$

Needless to say, (7.7) and (7.9) represent a third order transfer function, whose gain roll-off is -60 dB/dec, which surely is faster than the -20 dB/dec exhibited by the simple

Table 7-1. LCL-filter parameters used for analysis.

Case	C_f (uF)	L_g (mH)	L_{rec} (mH)	R_g (Ω)	R_{rec} (Ω)
(a)	15	1.5	1.5	0.15	0.15
(b)	15	2.0	1.0	0.20	0.10
(c)	15	0.5	2.5	0.05	0.25
(d)	0	1.5	1.5	0.15	0.15

L-filter. This better attenuation however takes place only above the resonant frequency, whose placement is therefore important. In addition to the resonance placement, the total filter inductance adopted for the proposed OCC scheme should also be chosen as small as possible, so as to minimize the reactive power demand, and to reduce the inductor size and cost. On another front, the filter capacitance should mainly be limited by the allowable power factor drop and passive damping losses.

Following the above specified general guidelines, four sets of LCL-parameters are chosen for comparison, whose values and accompanied Bode diagrams for (7.7) are

(a)

(b)

Fig. 7-7. Bode diagrams plotted using (a) (7.7) with LCL parameters listed in Table 7-1 case (a) to case (d), and (b) (7.10) with different passive damping resistances and parameters listed in Table 7-1 case (a).

tabulated in Table 7-1, and drawn in Fig. 7-7(a), respectively. For all four cases, the total filter inductance is kept constant, and their common intention is to suppress the 5 kHz switching harmonic and its associated sidebands. Although the total filter inductance remains unchanged, $L_p (= L_g // L_{rec})$ varies among the cases, and peaks only when L_g equals to L_{rec} . For cases where $L_g \neq L_{rec}$, the smaller computed L_p causes the resonant peak to shift rightwards, as shown in Fig. 7-7(a). The right shifting obviously widens the controller bandwidth, and hence speeds up its dynamic response, but at the expense of allowing more low order harmonics to “slip” to the grid. The choice made would therefore depend on the prioritized requirements brought forward for consideration. It is also clear from this figure that LCL-filters will be much more effective in switching harmonic suppression than single L-filters. Comparing the Bode diagrams of case (a) and case (d) shown in Fig. 7-7(a), it is easy to tell that, to achieve the same filtering of input line currents, the inductance of L-filters should be ten times that used in LCL-filters (34 mH), which is surely impractical for industrial applications.

For the bidirectional three-phase rectifier considered here, the symmetrical filter parameters listed under case (a) might have an additional advantage, since it presents equal filtering action to harmonics produced by the rectifier and those present in the grid (caused by nearby switching converters for example). The consequential resonant frequency based on parameters adopted from case (a) is then calculated as $f_{res} \approx 1.5$ kHz, which is neatly placed between ten times the fundamental frequency and half the switching frequency. As mentioned in [15], such placement of resonant peak would give rise to sufficient ripple attenuation, while at the same time, better avoid resonance problems triggered by low order or switching harmonics. In spite of that, an appropriate damping scheme is still needed for practical circuits, and is discussed in Subsection 7.3.4, after feedback variable selection is addressed in the next section.

7.3.3 Selection of Current Feedback Variables

As discussed in Subsection 7.2.1, a reference signal is needed for comparison with the integrated signal, and for the case of a simple L-filter, the reference is formed by

measuring the inductive current i_g (see Fig. 7-1), which happens to be the only ac current variable available for sensing. Offering more choices, current feedback with an LCL-filter added can be formed by measuring the grid-side current i_g , converter-side current i_{rec} , or even their weighted value for the LCCL-filter studied in [118], where the middle capacitive element is divided into two halves. Generally, it is more straightforward to control the converter-side current, but doing so would slightly degrade the accuracy of the controller, since the current flowing into the grid is not directly controlled [15]. For better accuracy, the grid-side current can be controlled instead, but it generally is more challenging in terms of maintaining system stability, which usually can be reinforced by including an appropriate damping scheme.

Some tradeoffs are also experienced by the proposed OCC scheme, but unlike others, grid current feedback can conceptually raise its stability and lessen its distortion sensitivity, which so far has not been discussed in the literature. Explanation for that can be deduced from Subsection 7.2.1, where it is explicitly stated in (7.6) that the rate of feedback current ripple variation must always be smaller than the limit indicated on the right-hand side of (7.6), which happens to depend on R_f . To better ensure stability, it is therefore tempting to set R_f small, so as to get a corresponding higher limit in (7.6). The tradeoff is a more distorted ac line current caused by harmonic amplification linked to the high gain block of $1 / R_f$ drawn in Fig. 7-2, even if only a slight grid voltage distortion is detected. Therefore, including R_f will definitely stabilize the system, but reducing R_f by a large amount is generally not recommended.

Similarly, increasing the dc-link voltage V_o and decreasing the time period T_s to raise the right-hand term of (7.6) are not practically feasible approaches, meaning that the right-hand term of (7.6) has an upper bound, which is hard to exceed in practice. Therefore, to stabilize the system even more, the left-hand term of (7.6), which represents the rate of current ripple variation, should be minimized instead. That certainly can be ensured by feeding back the grid-side current, which as mentioned before, also has the advantage of more precise active and reactive power control, since

the current flowing from the grid is directly controlled. By feeding back the grid-side current, the rate of variation to be placed on the left-hand side of (7.6) can be written as

$$K_{1,2} = \frac{R_s(v_g - v_c)}{L}, \text{ based on the labeling convention adopted for Fig. 7-4. Since both } v_g$$

and v_c are sinusoids, $K_{1,2}$ is definitely more gradual than the alternative of feeding back the converter-side current, which flows directly into the rectifier chopped voltage. Being more gradual, the right-hand limit in (7.6) then needs not be too high, making it suitable for applications demanding sinusoidal current (R_f present, but not overly small), accurate power control, higher power rating and lower switching frequency.

7.3.4 Resonance Damping Techniques

The simplest way of damping resonance is to add an extra resistor R_c in series with the filter capacitor. Adding a resistor would however increase the overall system losses, and would degrade the attenuation factor of the filter at high frequencies, as demonstrated in Fig. 7-7(b). Because of these conflicting interests, the value of R_c should ideally be chosen on a case-by-case basis, in order to arrive at the optimal tradeoff for each application under consideration. As an example, the system controlled by a classical linear controller with an inner current loop is considered. For this linearly controlled system, the value of R_c is usually tuned relatively high, in order to neutralize the oscillatory effect caused by setting high proportional gains needed for fast dynamic tracking purposes. While determining the value for R_c , it is also important to stress here that the power stage gain of $V_o/2$ must always be considered, if the carrier used for modulation spans between -1 and 1 only.

The same considerations would apply when selecting R_c value for the nonlinear OCC controller, except the open-loop gain now comes solely from the converter, since no inner current regulator is used. Another feature of interest is that the amplitude of the integrated signal in OCC is V_m rather than unity, meaning that the gain of the converter would be $V_o/(2V_m)$ placed in between its input reference signal and ac terminal output. This open-loop gain expression is much smaller than that found in the linear controller,

hence allowing its damping resistance to be much smaller without compromising the fast dynamic response of the nonlinear OCC control core. Upon choosing the appropriate passive damping resistance and adding it in series with the filter capacitor, the input-to-output transfer function for the passively damped block representation shown in Fig. 7-8 is written as (7.10) with all stray resistances ignored ($R_g = R_{rec} = 0$) since they are comparatively smaller than the damping resistance.

$$\frac{I_g}{m} = \frac{V_o}{2V_m} \cdot \frac{R_c C_f s + 1}{L_g L_{rec} C_f s^3 + (L_g + L_{rec}) C_f R_c s^2 + (L_g + L_{rec}) s} \quad (7.10)$$

where m represents the modulation index of the converter and usually ranges from -1 to 1. Using (7.10), the Bode diagrams for different damping resistances are plotted and shown in Fig. 7-7(b). As anticipated, increasing the damping resistance favorably flattens the resonant peak, but it unfortunately causes high frequency attenuation to be less effective. Other than frequency characteristics, the amount of damping losses for different resistive values can also be calculated by using (7.11).

$$P_{loss} = 3(\omega C_f v_g)^2 R_c [1 + THD_{(i_c)}^2] \quad (7.11)$$

where ω represents the angular fundamental frequency, and $THD_{(i_c)}$ represents the total harmonic distortion of the filter capacitive current i_c . Equation (7.11) clearly shows that the passive damping losses are directly linked to the harmonic content of the filter capacitive current, which would definitely be lower for the double-edge OCC scheme. Explanation for that can be drawn from the understanding that double-edge OCC control does not produce even harmonics, unlike its single-edge OCC variants, and therefore would give rise to a less distorted current flowing through the filter capacitor, and hence a lower damping loss. Upon understanding the above criteria, a 7 Ω damping resistance

Fig. 7-8. Control block representation of LCL-filter with passive damping.

is chosen for the three-phase OCC-controlled rectifier, which happens to be close to the capacitive impedance value of 7.07Ω determined at the resonant peak and using parameters decided earlier in Subsection 7.3.2. With these impedance values, it can be shown through simple transfer function analysis that the system is stable, and its attenuation factors at switching frequency and associated sidebands are not severely compromised.

Instead of using a real external resistor for passive damping, active damping can be an alternative, where the damping resistance is virtually emulated within the control scheme. Although the concept of virtual damping resistor has been discussed in [104], the active damping method presented here is essentially a different solution. One feature that can be noted from Fig. 7-9 is that the proposed active damping is regarded as a negative feedback of damping term rather than positive feedback one as adopted in [104]. Moreover, there is no differentiator placed along the active damping path, meaning that noise amplification of the high frequency signals is not an anticipated problem. The implementation of this active damping is shown in Fig. 7-9, where instead of adding a real resistance R_c in series with the filter capacitor, a virtual resistance R_d is now emulated along the feedback path of current i_c . With this additional feedback path, the reference signal is raised by a specific amount, computed using (7.12).

$$m' = I_c R_d \quad (7.12)$$

Knowing that $I_c = I_{rec} - I_g$ and by substituting (7.8) into (7.12) with R_g neglected, the actively damped modulating reference m' is derived as,

Fig. 7-9. Control block representation of LCL-filter with active damping.

$$m' = L_g C_f s^2 I_g R_d \quad (7.13)$$

Referring to the control block representation shown in Fig. 7-9, an intermediate transfer function can also be derived as,

$$(m - m') \cdot \frac{V_o}{2V_m} \cdot \frac{1}{L_g L_{rec} C_f s^3 + (L_g + L_{rec})s} = I_g \quad (7.14)$$

Substituting (7.13) into (7.14), and rearranging slightly, the final input-to-output transfer function with active damping incorporated is derived as,

$$\frac{I_g}{m} = \frac{V_o}{2V_m} \cdot \frac{1}{L_g L_{rec} C_f s^3 + \frac{V_o}{2V_m} \cdot L_g C_f R_d s^2 + (L_g + L_{rec})s} \quad (7.15)$$

If the same damping performance is expected from both passive and active damping, their characteristic polynomials or denominators found in (7.10) and (7.15) must be the same. Based on this similarity and by equating coefficients, their respective damping resistances are found to relate well according to the following equations.

$$(L_g + L_{rec})C_f R_c = \frac{V_o}{2V_m} \cdot L_g C_f R_d$$

$$R_d = \frac{L_g + L_{rec}}{L_g} \cdot \frac{2V_m}{V_o} \cdot R_c \quad (7.16)$$

Although their damping performances can theoretically be made the same, realistic differences still exist between them with the passive option clearly exhibiting higher power losses. The active technique also has its own unique characteristics when used with the nonlinear OCC control core, with the first being its anticipated poorer performance when applied to the leading or trailing-edge OCC control. The reason is because for both existing OCC techniques, sizable amount of even harmonics are produced, and will propagate along the actively damped feedback path to reference m' . It is therefore more difficult to tune the active gain (or resistance), since a high gain

would amplify the unwanted harmonics even more, and hence distort the input current even further. On the other hand, a small gain may lead to an inadequately damped, oscillatory response. Although an additional high-pass filter (HPF) can be added along the relevant feedback loop to remove the even harmonics as suggested in [102], it nonetheless is not an approach recommended for OCC control, since it will unfavorably introduce complex frame transformation and dynamic problems to the otherwise simple, yet dynamically fast OCC control core. Fortunately, the problem can be resolved without much difficulty, as long as the investigated double-edge OCC control scheme is used, since it produces no disturbing even harmonics.

Even after the even harmonics are removed, the actively introduced damping reference m' would still add some amount of high frequency switching ripples to the original reference m , since m' is obtained by feeding back the relatively “noisy” filter capacitive current through a properly tuned gain. The resulting reference $(m - m')$ might turn out to have some amount of ripples that will occasionally over-modulate the rectifier for short periods of time, causing the ac terminal voltage to be distorted slightly. To mitigate this over-modulation problem even though only for very short time periods, the linear modulation range should be extended as wide as possible, which based on past modulation understanding, an increase by 15% is conceptually feasible after an appropriate triplen offset is added to the three-phase references [30]. For OCC control, the same addition of offset is also feasible. As demonstrated in Fig. 7-10, the offset is generated by taking the instantaneous average of the maximum and minimum of the three input reference voltages ($R_s(i_{fx} + i_{gx})$), and the final modulation waveforms can be obtained by subtracting this value from each of the individual reference voltages as depicted by the following equations.

$$\begin{cases} V_{offset} = \frac{\max(R_s(i_{fx} - i_{gx})) + \min(R_s(i_{fx} - i_{gx}))}{2} \\ V_x = R_s(i_{fx} - i_{gx}) - V_{offset} \end{cases} \quad \text{where } x = a, b, c \quad (7.17)$$

Fig. 7-10 also shows the complete OCC core for controlling the three-phase active

Fig. 7-10. Double-edge OCC scheme with triplen offset injection designed for controlling three-phase active rectifier.

rectifier (excluding the damping circuit, which can either be passively added to the power circuit or actively included in the control circuit). After adding the triplen offset, the original signal peaks of the three-phase references are reduced, allowing their amplitudes to be increased further by 15% without causing over-modulation.

Upon resolving the above two complications, active damping should give a better damping performance than a passively damped system, since no physical resistor and losses are introduced on a long term basis. The only cost element is a one-time cost for the additional sensor needed for sensing the filter capacitive current, which can be omitted if provisions are included to predict the capacitive current indirectly from the measured grid voltage v_g and grid-side current i_g . This of course is only feasible if the filter parameters are known to some level of preciseness. Other than cost, active damping also has the advantage of no degradation in gain roll-off even if the frequency increases considerably. Explanation for that can be inferred by comparing (7.10) for passive damping and (7.15) for active damping. Clearly, (7.10) has a zero in its numerator, which will reduce the system roll-off from -60 dB/dec to -40 dB/dec after

crossing its cutoff frequency of $1/R_c C_f$ rad/s. This cutoff expression of the included zero means that with a larger R_c for damping, the degradation in roll-off happens earlier, as demonstrated in Fig. 7-7(b). In contrast, the roll-off problem is not faced by the active damping technique, since no zero is found in its transfer expression in (7.15).

7.4 Experimental Results

To verify the effectiveness of the studied OCC control scheme, a 1 kW three-phase active rectifier was constructed in the laboratory based on the layout shown in Fig. 7-4, and parameters listed in Table 7-2. The rectifier was comprised of three insulated gate polar transistor (IGBT) modules from *Semikron* (SKM50GB063D), having two switches per module for forming a phase-leg. This IGBT module can tolerate 600 V blocking voltage and pass continuous current up to 70 A in normal operating condition. The proposed OCC algorithms were implemented by hybrid control architecture, where its outer voltage loop was regulated by a DSP, and inner current loop was implemented by analog devices. It should be noted that, a low cost DSP can be used for voltage loop regulation because of its slow dynamic response, while for current loop, analog implementation is usually preferred in order to obtain a

Table 7-2. Parameters used for experimental testing.

Parameters	Values
Grid-side inductance L_g	1.7 mH
Converter-side inductance L_{rec}	1.7 mH
Filter capacitance C_f	15 μ F
DC-link capacitance C_o	420 μ F
DC-link voltage V_o	350 V
AC rms line voltage ($\sqrt{3} * v_g$)	174 V
Line frequency f_o	50 Hz
Switching frequency f_s	5 kHz
Dead-time	2.5 μ s
Nominal load	135 Ω
Passive damping resistance R_d	7 Ω

cycle-by-cycle regulation that is required by nature of OCC.

Using the assembled hardware platform, experimental testing was first performed with no damping applied to the single-edge (leading or trailing) and double-edge OCC schemes. As anticipated, the system was unstable with large resonant oscillation, and therefore, the system was not turned up to its full specified operating conditions. The experiment was next performed with passive damping added, whose corresponding results are shown in Fig. 7-11. As seen, the filter capacitive current for the single-edge scheme has much thicker ripple band than the double-edge scheme. To reinforce the comparison, harmonic spectra of the grid current obtained by applying Fast Fourier Transform (FFT) are plotted in Fig. 7-12, where it is clear that the double-edge scheme in general produces a lower harmonic content across the entire frequency range.

Proceeding on to verify the actively damped system with only a virtual damping resistance emulated within the control loop, Fig. 7-13 shows the captured experimental results, where as expected, the double-edge scheme produces lesser ripples, as reflected by the thinner current ripple band of the capacitor in Fig. 7-13(b). More details of the captured waveforms for the actively damped cases are shown in Fig. 7-14, where the relevant grid current spectra are plotted for both high and lower frequency ranges. Other than simply showing that the double-edge OCC scheme produces lesser harmonics than its single-edge counterpart in the actively damped mode, more information would be revealed if the plots in Fig. 7-14 are compared with those in Fig. 7-12.

The first observation is that, as predicted, low-order even harmonics produced by the single-edge scheme are fed to the actively damped OCC core without being filtered, since they are below the filter cutoff frequency. Feeding back undesirably causes those even harmonics to be amplified and therefore appearing much larger than those recorded for the passively damped single-edge case (see Fig. 7-12(a) and Fig. 7-14(a)). The second observation is that the switching harmonics of the actively damped single

or double-edge case are considerably lower than those of their passively damped counterparts. The reason has already been explained in Subsection 7.3.4, and is mainly due to the absence of a zero for the actively damped case, which would then not cause the gain roll-off to drop from -60 dB/dec to -40 dB/dec.

Upon verifying the OCC steady-state performances, testing was next conducted on the OCC schemes when subject to 50% to 100% step-up and 100% to 50% step-down load transients, which are simply created by turning off and turning on the switch S_w shown in Fig. 7-4, respectively. Responses for all the OCC schemes are noted to be similar, since they use the same nonlinear, dynamically fast OCC control core, except with different integrated edges and damping schemes. These latter two features influence only the system steady-state response, and not its dynamic behavior. Because of their close dynamic similarity, only results for the double-edge, actively damped OCC scheme are presented in Fig. 7-15, where it is shown that the dc-link voltage and ac input current vary only slightly and recover fully in less than half a fundamental cycle. The speed of response is in fact solely decided by the dc-link voltage controller shown in Fig. 7-10, which in theory faces only minimal bandwidth restriction. This lack of restriction is of course attributed to the presence of the nonlinear OCC control core, which is dynamically much faster than the inner current loop found in a traditional linear controller.

Table 7-3. Performance comparison of OCC control schemes.

	THD of I_g	Additional Sensor	Calculated Damping Losses	System Efficiency
Single-edge passive damping	4.57%	No	79.3 W	87.3%
Single-edge active damping	6.93%	Yes	0	93.1%
Double-edge passive damping	3.92%	No	33.4 W	91.6%
Double-edge active damping	2.06%	Yes	0	94.5%

In addition to the waveforms and spectra discussed above, other experimentally determined results obtained from the OCC-controlled rectifier are tabulated in Table 7-3, after applying the relevant post-processing computations using parameters listed in Table 7-2. The calculated results shown in the last two columns clearly bring out the main disadvantage of the passively damped scheme, which needless to say is the sizable amount of power losses introduced by the real damping resistor added. The overall system efficiency is therefore lower, as clearly reflected by those numbers presented in Table 7-3. Another comment to be highlighted here is that, when there is reduction in load demand, the efficiency of the proposed OCC rectifier may decrease and its THD of input currents may increase. However, such performance degradation is always less serious than the conventional OCC rectifier regardless of the power level, and this confirms the theoretical findings developed in this chapter.

(a)

(b)

Fig. 7-11. Experimental steady-state waveforms obtained for (a) single-edge and (b) double-edge OCC schemes with passive damping.

(a)

(b)

Fig. 7-12. Grid current spectra of passively damped single-edge (SE) and double-edge (DE) OCC schemes when plotted across the (a) low and (b) high frequency ranges.

(a)

(b)

Fig. 7-13. Experimental steady-state waveforms obtained for (a) single-edge and (b) double-edge OCC schemes with active damping.

Fig. 7-14. Grid current spectra of actively damped single-edge (SE) and double-edge (DE) OCC schemes when plotted across the (a) low and (b) high frequency ranges.

(a)

(b)

Fig. 7-15. Experimental transient waveforms obtained when subjecting the active rectifier to (a) 50% to 100% step-up load change and (b) 100% to 50% step-down load change.

7.5 Summary

This chapter presents a double-edge OCC control scheme for controlling three-phase active rectifier with a front-end LCL input filter. By appropriately choosing the feedback variable and by nature of the double-edge integrated signal, the controlled

three-phase rectifier is more stable without having to rely solely on an introduced fictitious stabilizing term. Because of that, the input current is not severely distorted, since any sensed slight voltage distortion is now not amplified by the introduced fictitious gain. The presence of a higher order input filter for better meeting grid codes also prompts the development of appropriate passive and active damping schemes for use with the double-edge OCC control scheme. Specific findings noted from the investigation can therefore be summarized as:

- Better overall performance of the actively damped rectifier when controlled by the double-edge OCC control scheme.
- Better retention of third order filtering characteristics by the actively damped technique.
- Overall improvement in stability and accuracy when the grid-side current is sensed for feedback purposes.

These findings have been experimentally validated using a 1 kW laboratory prototype.

Chapter 8 One-Cycle Controlled Active Rectifiers under Non-ideal Operating Conditions

8.1 Introduction

That one-cycle control (OCC) scheme designed in Chapter 7 does give rise to a high performance active rectifier, which draws pure sinusoidal currents from the utility grid and produces negligible harmonic distortion. Nevertheless, this finding is valid only under ideal input voltage conditions. In reality, the grid might be distorted and / or unbalanced especially in the absence of a strong source. When that happens, performance of the active rectifier might deteriorate significantly.

One possible solution to mitigate this problem is to use bulky passive filters on both input ac and output dc sides. Unfortunately, this leads to increased system costs and slow dynamic response of the active rectifier. Alternatively, harmonic compensation strategies proposed in [119]-[122] can be used, but they are more for linear control schemes, and hence poorer in dynamics. They also need fast digital signal processors (DSPs), carefully designed phase-locked loop (PLL) and probably multiple frame transformations, which make their physical implementation challenging.

For nonlinear OCC, a set of mathematical proofs has already been derived in [91] to show that the line currents are sinusoidal but unbalanced when the source voltages are unbalanced. A large dc-link capacitor also must be added to the dc-link to hold its voltage constant so as not to distort the line currents excessively. So far, no OCC-based compensation scheme has been proposed to address this unbalance in currents when the active rectifier is operated under non-ideal source voltage conditions.

Offering a possible solution to resolve unbalance and harmonic concerns faced at the

input and output ends of the active rectifier, this chapter proposes an improved OCC control scheme based on the concept of reconstructing the reference signals. The described technique can conveniently be embedded within the inner current loop of a conventional OCC control core, hence representing a simple extension rather than a complex alternative that is hard to realize in practice. With some minor modifications subsequently added to it, the proposed scheme can effectively compensate for all prominent harmonics found in the input currents, and smoothen out voltage ripples detected at the dc-link without using large capacitance.

Previously identified advantages of existing OCC scheme like PLL-less, no frame transformation and constant switching frequency are all preserved by the new OCC control scheme, whose details are now elaborated in this chapter. Theoretical findings related to the improved OCC scheme are all verified via experimental testing on a 1.2 kW three-phase active rectifier, developed in the laboratory.

8.2 Behaviour of an OCC-Based Active Rectifier under Non-Ideal Supply Voltages

Fig. 8-1 shows the circuit diagram of a typical three-phase active rectifier with an input LCL-filter that might be needed for better switching harmonic attenuation in higher power applications or to simply meet the ever more tightened future grid codes. A quick review of the existing literature for this boost type rectifier would reveal that it

Fig. 8-1. Circuit diagram of the three-phase active rectifier.

can be controlled by a number of different control schemes, where OCC is one of them. Like most of the other control schemes, OCC also employs a double loop control structure, where the outer voltage loop includes a simple PI controller for regulating V_{dc} . The output V_m of the PI controller, representing the load power level in principle, is then fed to the nonlinear inner current loop on a cycle-by-cycle basis. In the inner loop, V_m is processed according to the following key control equation, together with the measured ac line currents i_{sx} drawn directly from the grid (derivation of (8.1) can be found in [78]).

$$V_m(1-2d_x) = R_s i_{sx}, (x = a, b, c) \quad (8.1)$$

where R_s is the equivalent current sensing resistance, and d_x is the duty ratio of S_a' , S_b' or S_c' . Despite (8.1) being proven to work fine in a number of applications, it may still cause instability problem under light load conditions. To resolve this instability, a more practically orientated OCC scheme was recommended in [80], whose control equation for inner current regulation is formed by sensing both the source voltages and line currents. For comparison with (8.1), the modified OCC control equation used in [80] is reprinted here as (8.2) with its block diagram realization drawn in Fig. 8-2.

$$V_m(1-2d_x) = R_s i_{sx} + K v_{sx} \quad (8.2)$$

where v_{sx} is the instantaneous ac grid voltages, and K is a constant introduced for flexible tuning, so as to stabilize the system even under no load condition. A further comment raised here about K is that its value is dependent on the adopted switching

Fig. 8-2. Control block diagram of existing OCC scheme.

frequency, filter inductance and modulation index, whose full details are explained in [80], and therefore not duplicated here.

Besides (8.2), the boost type rectifier is also governed by the following equation, describing its ac input end with voltage drops across the filter inductors ignored (because of that, (8.3) should more strictly be referred to as an approximation, which turns out to have an important advantage when developing the modified OCC scheme in Section 8.3).

$$v_{sx} \approx v_{cx} = V_{dc} S_x = V_{dc} (1 - 2d_x) \quad (8.3)$$

where v_{cx} and S_x are the converter immediate terminal voltage and average switching function, respectively. Combining (8.2) and (8.3) then yields,

$$\frac{V_m}{V_{dc}} = \frac{R_s i_{sx}}{v_{sx}} + K \Rightarrow i_{sx} = \left(\frac{V_m}{V_{dc}} - K \right) \frac{v_{sx}}{R_s} = \frac{v_{sx}}{R_e} \quad (8.4)$$

where R_e represents the equivalent per phase resistance of the active rectifier when viewed from the ac input side (see Fig. 8-1). Equation (8.4) clearly informs that the currents drawn from the ac source are proportional to the supply voltages in the steady state, which then means that if the supply voltages are unbalance and distorted, the input currents drawn would also be unbalanced and distorted. This conclusion is in fact consistent with that deduced in [122], where a less generalized concluding statement is drawn by considering only unbalance, but not harmonics.

Moving on to analyze the harmonic effects on the dc output side, the power balance equation with converter losses neglected can first be written to link the ac and dc sides of the rectifier in a single equation, as demonstrated in (8.5).

$$v_{ca} i_{sa} + v_{cb} i_{sb} + v_{cc} i_{sc} = V_{dc} i_{dc} \quad (8.5)$$

Substituting (8.3) into (8.5) subsequently gives rise to the following expression for the dc side current.

$$i_{dc} = S_a i_{sa} + S_b i_{sb} + S_c i_{sc} \quad (8.6)$$

Equation (8.6) can next be processed by the simplified Clarke transformation matrix shown in (8.7) with only phases a and b considered, since phase c is not an independent variable, but simply just the negative summation of the other two phases for three-phase three-wire systems.

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/\sqrt{3} & 2/\sqrt{3} \end{bmatrix} \cdot \begin{bmatrix} X_a \\ X_b \end{bmatrix} \quad (8.7)$$

The transformed equation in the $\alpha\beta$ coordinate frame is then written as,

$$i_{dc} = S_\alpha i_\alpha + S_\beta i_\beta \quad (8.8)$$

where i_α , i_β , S_α and S_β on the right of (8.8) can be further expressed in terms of their individual harmonic components in their respective synchronous rotating dq frames, as follows,

$$i_\alpha + ji_\beta = \sum_{n=-\infty}^{\infty} e^{jn\omega t} (i_d^n + ji_q^n) = \sum_{n=-\infty}^{\infty} (\cos n\omega t + j \sin n\omega t)(i_d^n + ji_q^n) \quad (8.9)$$

$$= \sum_{n=-\infty}^{\infty} [(i_d^n \cos n\omega t - i_q^n \sin n\omega t) + j(i_d^n \sin n\omega t + i_q^n \cos n\omega t)]$$

$$S_\alpha + jS_\beta = \sum_{h=-\infty}^{\infty} e^{jh\omega t} (S_d^h + jS_q^h) \quad (8.10)$$

$$= \sum_{h=-\infty}^{\infty} [(S_d^h \cos h\omega t - S_q^h \sin h\omega t) + j(S_d^h \sin h\omega t + S_q^h \cos h\omega t)]$$

where n and h represent harmonic orders of the line currents and average switching functions, respectively, and their signs determine whether positive- or negative-sequence component is considered. It should also be noted here that h and n are independent harmonic orders, whose different frequency combinations allow harmonic interactions between the line currents and switching functions to be generalized over the full frequency range. Substituting the real and imaginary expressions governing i_α , i_β , S_α and S_β from (8.9) and (8.10) into (8.8) then gives rise to the following closed form expression for calculating i_{dc} .

$$\begin{aligned}
 i_{dc} &= \sum_{n,h=-\infty}^{\infty} \left[(S_d^h \cos h\omega t - S_q^h \sin h\omega t)(i_d^n \cos n\omega t - i_q^n \sin n\omega t) \right. \\
 &\quad \left. + (S_d^h \sin h\omega t + S_q^h \cos h\omega t)(i_d^n \sin n\omega t + i_q^n \cos n\omega t) \right] \\
 &= \sum_{n,h=-\infty}^{\infty} \left[(S_d^h i_d^n + S_q^h i_q^n)(\sin h\omega t \sin n\omega t + \cos h\omega t \cos n\omega t) \right. \\
 &\quad \left. + (S_q^h i_d^n + S_d^h i_q^n)(-\cos h\omega t \sin n\omega t + \sin h\omega t \cos n\omega t) \right]
 \end{aligned} \tag{8.11}$$

Equation (8.11) can in principle be used for computing i_{dc} at the rectifier output when regulated by any chosen control scheme, where OCC is one possibility. In fact, when used for computing i_{dc} under OCC control, (8.11) can be simplified by noting from (8.1) that its average switching function S per phase has similar spectral content as its corresponding line current, hence giving rise to the following equality.

$$\sum_{n,h=-\infty}^{\infty} (-\cos h\omega t \sin n\omega t + \sin h\omega t \cos n\omega t) = 0 \tag{8.12}$$

Substituting (8.12) into (8.11) and simplifying the remaining trigonometric functions then give rise to the following simplified equation in (8.13) for computing i_{dc} .

$$\begin{aligned}
 i_{dc} &= \sum_{n,h=-\infty}^{\infty} (S_d^h i_d^n + S_q^h i_q^n)(\sin h\omega t \sin n\omega t + \cos h\omega t \cos n\omega t) \\
 &= \sum_{n,h=-\infty}^{\infty} (S_d^h i_d^n + S_q^h i_q^n)[\cos(h-n)\omega t]
 \end{aligned} \tag{8.13}$$

Equation (8.13) can be simplified by ignoring terms involving the cross-multiplication of two harmonics with one coming from the line currents and the other coming from the average switching functions. This is a justifiable simplification since the normalized amplitudes of harmonics with respect to their fundamentals are relatively small, which when cross-multiplied, will give rise to even smaller amplitudes that can generally be ignored. When introducing this second simplification, only those cross-multiplied terms in (8.13) involving the fundamentals need to be computed, as summarized in (8.14), which in principle represents the first closed form expression derived for computing i_{dc} in the OCC-controlled rectifier.

$$\begin{aligned}
 i_{dc} = & (S_d^{+1}i_d^{+1} + S_q^{+1}i_q^{+1}) + \sum_{n=-\infty, n \neq 1}^{\infty} (S_d^{+1}i_d^{+n} + S_q^{+1}i_q^{+n})[\cos(1-n)\omega t] \\
 & + \sum_{h=-\infty, h \neq 1}^{\infty} (S_d^h i_d^{h+1} + S_q^h i_q^{h+1})[\cos(h-1)\omega t]
 \end{aligned} \tag{8.14}$$

Obviously, the last two current terms on the right of (8.14) are varying cosine functions, which when fed through the dc-link capacitor, lead to voltage ripples appearing across the rectifier output terminals. For the two terms, it is also easy to prove from the OCC control equation that they are related by the following equality, and therefore need to be computed only once.

$$\sum_{n=-\infty, n \neq 1}^{\infty} (S_d^{+1}i_d^{+n} + S_q^{+1}i_q^{+n})[\cos(1-n)\omega t] = \sum_{h=-\infty, h \neq 1}^{\infty} (S_d^h i_d^{h+1} + S_q^h i_q^{h+1})[\cos(h-1)\omega t] \tag{8.15}$$

A relevant comment linked to (8.14) and therefore raised here is that in [122], it is broadly pointed out that the n^{th} harmonic component found in the supply voltages will lead to harmonics of orders $n-1$, $n+1$ and $2n$ sensed at the dc output, which surely is applicable to OCC too, but it does not spell out their relative amplitudes. This unknown information for OCC control is now filled by (8.14), where it is explicitly shown that only harmonics of order $|n-1|^{\text{th}}$ have dominant influences. That means for an ac input network containing unbalanced negative-sequence fundamental component ($n = h = -1$), only the second harmonic would be prominent at the rectifier dc output, as demonstrated by the experimentally captured waveforms shown in Section 8.4. Similarly, for an ac network polluted by common fifth and seventh harmonics ($n = h = -5, +7$), only the sixth harmonic is likely to be detected at the rectifier dc output, whose correspondingly induced dc voltage value is likely to be three times smaller than that of the second harmonic, because of the inverse relationship found between capacitive impedance and harmonic order.

Other than the above discussed ac to dc harmonic transfer, the inverse flow of harmonic influence from the dc to ac end can also be of concern, especially when it

creates non-zero-sequence triplen harmonic voltages at the rectifier ac input. For a clearer illustration of this inverse cross-interfering process, the second harmonic current ripple sensed at the dc end is considered, which upon flowing through the dc capacitor, will give rise to a second harmonic voltage ripple with amplitude V_{dc2} . This induced voltage ripple when cross-multiplied with the average switching function per phase will give rise to more harmonic voltages at the rectifier ac input. Among the added harmonics, the prominent one is likely to be that produced by multiplying the second dc-link harmonic voltage with the fundamental switching function, which supposedly should have the highest amplitude S_1 for the case of rectifier. Details of this multiplication process are shown in (8.16), where the subscripts of *har* and *fund* represent the harmonic and fundamental components found in each control variable, and ϕ represents the phase difference measured between the fundamental average switching function and second harmonic voltage sensed across the dc-link capacitor.

$$\left\{ \begin{array}{l} v_{ca_har} = S_{a_fund} \cdot V_{dc_har} = S_1 \cos(\omega t + \phi) \cdot V_{dc2} \cos 2\omega t \\ \quad = -\frac{1}{2} S_1 V_{dc2} [\cos(3\omega t + \phi) + \cos(\omega t - \phi)] \\ v_{cb_har} = S_{b_fund} \cdot V_{dc_har} = S_1 \cos(\omega t - \frac{2\pi}{3} + \phi) \cdot V_{dc2} \cos 2\omega t \\ \quad = -\frac{1}{2} S_1 V_{dc2} [\cos(3\omega t - \frac{2\pi}{3} + \phi) + \cos(\omega t + \frac{2\pi}{3} - \phi)] \\ v_{cc_har} = S_{c_fund} \cdot V_{dc_har} = S_1 \cos(\omega t + \frac{2\pi}{3} + \phi) \cdot V_{dc2} \cos 2\omega t \\ \quad = -\frac{1}{2} S_1 V_{dc2} [\cos(3\omega t + \frac{2\pi}{3} + \phi) + \cos(\omega t - \frac{2\pi}{3} - \phi)] \end{array} \right. \quad (8.16)$$

Clearly, (8.16) shows the creation of an additional set of dominant third harmonic components at the ac input end, other than the fundamental negative-sequence voltages expected from the earlier discussion on ac to dc harmonic transfer. A note emphasized here with the created third harmonic voltages is the presence of a 120° phase difference measured between any two phases, unlike traditional third harmonic voltages which are all in phase, and hence forming a zero-sequence set. The third harmonic voltages found in (8.16) are therefore non-zero-sequence by nature, and can lead to harmonic current flow that will further deteriorate the rectifier performance,

even when in a three-phase three-wire system. Being third order, these harmonic currents are also close in frequency to the fundamental components, and are therefore hard to filter at the ac input end. Because of that, addressing the concern at the ac input end is deemed as not feasible. Instead, [91] has suggested the use of a considerably large dc capacitor at the dc-link for filtering purposes, which upon effected, will minimize both the dc-link voltage ripples and their correspondingly induced third harmonic input currents. Like most recommended passive solutions, the likely concerns faced here are the higher overall system cost and wider board size needed for accommodating the larger capacitor.

8.3 Operating Principles of the Proposed OCC Scheme

The objectives defined for the proposed OCC scheme are to provide a balanced set of nearly sinusoidal current waveforms and a smoother dc-link voltage without using large capacitor, even when supplied by a set of non-ideal three-phase voltages. For meeting these objectives, the line currents measured for the inner current loop must be broken down into their fundamental and harmonic components, whose pictorial representation is drawn in Fig. 8-3, and mathematical form is expressed as in (8.17).

$$i_{sx} = i_{sx}^{+1} + \sum_{n=-\infty, n \neq 1}^{\infty} i_{sx}^n \quad (8.17)$$

Fig. 8-3. Decomposition of input currents for (a) unbalanced and (b) distorted cases.

According to (8.4), the harmonic components of the line currents are proportional to their respective harmonic source voltages, inferring that (8.17) can be rewritten as,

$$i_{sx} = i_{sx}^{+1} + \frac{1}{R_e} \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n \quad (8.18)$$

By substituting (8.18) into (8.2), the new OCC control equation with source non-ideal conditions taken into consideration is written as,

$$V_m(1-2d_x) = R_s(i_{sx}^{+1} + \frac{1}{R_e} \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n) + K v_{sx} = R_s i_{sx}^{+1} + (\frac{R_s}{R_e} \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n + K v_{sx}) \quad (8.19)$$

where on the right of (8.19), the scaling factor of R_s/R_e for the harmonic summation term is unknown, and should therefore be replaced by $((V_m/V_{dc}) - K)$, deduced from (8.4), which in turn is derived from the approximation found in (8.3). Effecting this replacement has an important compensating influence, whose reasoning is presented shortly. For the time being, the modified control equation is rewritten as:

$$\begin{aligned} V_m(1-2d_x) &\approx R_s i_{sx}^{+1} + [(\frac{V_m}{V_{dc}} - K) \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n + K v_{sx}] \\ &= R_s i_{sx}^{+1} + [(\frac{V_m}{V_{dc}} - K) \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n + K(\sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n + v_{sx}^{+1})] \\ &= R_s i_{sx}^{+1} + (\frac{V_m}{V_{dc}} \sum_{n=-\infty, n \neq 1}^{\infty} v_{sx}^n + K v_{sx}^{+1}) \end{aligned} \quad (8.20)$$

where it is noted on the right of (8.20) that the reference signals needed for OCC realization have all source harmonic voltages included, together with appropriately scaled positive-sequence source voltages and line currents. Understanding it from another prospective, (8.20) also conveys that a balanced set of undistorted positive-sequence line currents can still be produced under non-ideal voltage conditions, so long as an appropriately scaled combination of positive-sequence (scaled by constant K) and harmonic (by ratio V_m/V_{dc}) source voltages can be formed for feedback control purposes. Upon implementing that control, the line current harmonic and zero-sequence components would be zero, causing the second dc current ripple term on the right of (8.14) to be zero too.

As for the third term on the right of (8.14), its value is non-zero since according to (8.20), duty ratio d_x , and hence its corresponding average switching functions S_d and S_q , are still distorted by the non-ideal supply voltage harmonics, scaled by the multiplier of V_m/V_{dc} . With reference to this multiplier, an important note raised here is that with V_{dc} found in its denominator, some extent of normalization is introduced for compensating the dc-link voltage variation, just like what has always been done in traditional PWM schemes for compensating non-constant or varying dc-link voltage. With the dc-link variation now normalized, its induced ac quantities will no longer have prominent non-zero-sequence third harmonic component, as verified later in the experimental section.

Proceeding next to realize the proposed OCC scheme, its control equation in (8.20) clearly shows the requirement for independent scaling of the source voltage positive-sequence and non-ideal (including harmonic and negative-sequence) components, meaning that a mechanism for extracting the non-ideal components from the source voltages is somehow needed. A common method for effecting the extraction is to first transform the three-phase voltages from the stationary abc frame to the positive fundamental synchronous dq frame, where the positive-sequence component now appears as a dc quantity. The dc quantity is then removed by using (e.g.) the first order high pass filter (HPF) shown in (8.21), leaving only the non-ideal components for independent scaling.

$$H_{dq}(s) = \frac{s}{s + \omega_c} \quad (8.21)$$

where ω_c is the cutoff frequency, which should be chosen small, around 20 rad/s, to avoid attenuating the low order harmonics by too much. Although the dq transformation method works fine, its computational complexity and requirement for a PLL to some extent compromise with the OCC simplicity, and should therefore be avoided, if possible. Because of that, frequency-shifting of the voltage variables is not recommended. Instead, the less complex, and hence more realizable, approach of inversely shifting the HPF from the synchronous dq frame to the stationary $\alpha\beta$ frame is

recommended, whose filtering advantages have already been confirmed in [6]. Mathematically, the inverse shifting process can be initiated by substituting (8.21) into the inverse Clarke transformation matrix of (8.22).

$$H_{\alpha\beta}(s) = \begin{bmatrix} H_{dq}(s + j\omega_o) + H_{dq}(s - j\omega_o) & jH_{dq}(s + j\omega_o) - jH_{dq}(s - j\omega_o) \\ -jH_{dq}(s + j\omega_o) + jH_{dq}(s - j\omega_o) & H_{dq}(s + j\omega_o) + H_{dq}(s - j\omega_o) \end{bmatrix} \quad (8.22)$$

where ω_o represents the fundamental frequency. Upon performing slight mathematical manipulation, the equivalent stationary frame HPF is derived at the far right of (8.23) after noting that $\omega_c^2 \ll \omega_o^2$.

$$\begin{aligned} H_{\alpha\beta}(s) &= \begin{bmatrix} \frac{s^2 + \omega_c s + \omega_o^2}{s^2 + 2\omega_c s + \omega_c^2 + \omega_o^2} & \frac{-\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_c^2 + \omega_o^2} \\ \frac{\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_c^2 + \omega_o^2} & \frac{s^2 + \omega_c s + \omega_o^2}{s^2 + 2\omega_c s + \omega_c^2 + \omega_o^2} \end{bmatrix} \\ &\approx \begin{bmatrix} \frac{s^2 + \omega_c s + \omega_o^2}{s^2 + 2\omega_c s + \omega_o^2} & \frac{-\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_o^2} \\ \frac{\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_o^2} & \frac{s^2 + \omega_c s + \omega_o^2}{s^2 + 2\omega_c s + \omega_o^2} \end{bmatrix} \\ &= \begin{bmatrix} 1 - \frac{\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} & \frac{-\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_o^2} \\ \frac{\omega_o \omega_c}{s^2 + 2\omega_c s + \omega_o^2} & 1 - \frac{\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \end{bmatrix} \end{aligned} \quad (8.23)$$

Equation (8.23) can then be conveniently realized by using an analog universal filtering integrated chip UAF42 [123], which includes on-chip 1000 pF capacitors trimmed to 0.5% tolerance for performing various filtering functions. The overall layout of the chip is drawn in Fig. 8-4, where the same structure can be used for realizing low-pass, high-pass and band-pass filters, whose input-output transfer representations are described by (8.24), (8.25) and (8.26), respectively.

$$H_{LP}(s) = \frac{\omega_o^2 / Q}{s^2 + (\omega_o / Q)s + \omega_o^2} = \frac{2\omega_c \omega_o}{s^2 + 2\omega_c s + \omega_o^2} \quad (8.24)$$

$$H_{HP}(s) = \frac{(1/Q)s^2}{s^2 + (\omega_o / Q)s + \omega_o^2} = \frac{(2\omega_c / \omega_o)s^2}{s^2 + 2\omega_c s + \omega_o^2} \quad (8.25)$$

$$H_{BP}(s) = \frac{(\omega_o / Q)s^2}{s^2 + (\omega_o / Q)s + \omega_o^2} = \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \quad (8.26)$$

where $Q = \omega_o/2\omega_c$ is the quality factor. To achieve satisfactory dynamic response and block interference induced by low order harmonics, Q is chosen as six, implying $\omega_c = 26.2$ rad/s. Calculating using the design equations provided in [123], the external tuning resistance R_Q is then determined as 5 k Ω . To next place the resonant frequency at 50 Hz, the external frequency-setting resistors are chosen as $R_{F1} = R_{F2} = 3.1847$ M Ω , which can be formed by series connecting a 3 M Ω fixed resistor with a 184.7 k Ω adjustable resistor, so as to retain enough accuracy. It is worth mentioning that a dedicated design program FILTER42 for UAF42 is available from *Texas Instruments* (*TI*) website for calculating all external tuning resistances automatically, which no doubt will help to simplify the overall design process.

Upon identifying the UAF42 chip, the demanded fundamental positive-sequence extraction can be implemented by using the chip and some scaling / summing op-amps

Fig. 8-4. Universal active filter used for extracting fundamental positive-sequence component.

to realize the following transfer functions without having to transform to the synchronous frame, while yet retaining the same filtering performance as (8.21).

$$H_{\alpha\beta}(s) = \begin{bmatrix} 1 - \frac{1}{2}H_{BP}(s) & -\frac{1}{2}H_{LP}(s) \\ \frac{1}{2}H_{LP}(s) & 1 - \frac{1}{2}H_{BP}(s) \end{bmatrix} \quad (8.27)$$

A further note raised here with (8.23) and (8.27) is that if the supply grid is distorted but not unbalanced, its cross-diagonal terms can be omitted since the fundamental negative-sequence component is now absent, and therefore does not need to be filtered. The resulting simplified filter for dealing with harmonics only is written as (8.28) ($x = \alpha$ or β), which turns out to be only a simple second order notch filter or only a band-pass filter in the UAF42 chip.

$$H_x(s) = \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} = H_{BP}(s) \quad (8.28)$$

Alternatively, the reference generation block can also be realized by writing a digital modular subroutine for micro-controller programming, where the bilinear (Tustin) transform is likely to be first applied to the s-domain transfer functions to convert them to the discrete-time z-domain. For illustration, (8.28) is processed as an example with

Fig. 8-5. Control block diagram of the proposed OCC scheme.

its resulting z-equivalence written as.

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad (8.29)$$

where a_n and b_n are the coefficients of the digital filter. Equation (8.29) can then be written as difference equations, before coding into the demanded subroutine.

Regardless of which implementation approach is eventually chosen, the overall control block representation of the proposed OCC scheme can be summarized as in Fig. 8-5 for easier visual comparison with the existing scheme drawn in Fig. 8-2. The abc to $\alpha\beta$ frame transformation and its inverse version can be found in Section 2.2.5.

8.4 Experimental Results

To verify the effectiveness of the proposed control scheme, a boost type three-phase active rectifier was built using existing components found in the laboratory. The

Table 8-1. Parameters used for experimental testing.

Parameters	Values
Grid-side inductance L_s	1.7 mH
Converter-side inductance L_c	1.7 mH
Filter capacitance C	15 μ F
DC-link capacitance C_o	420 μ F
DC-link voltage V_{dc}	380 V
AC rms line voltage ($\sqrt{3} * v_s$)	173 V
Line frequency f_o	50 Hz
Switching frequency f_s	5 kHz
Dead-time	2.5 μ s
Nominal dc load	135 Ω
Passive damping resistance R_c	6 Ω

rectifier was assembled using three insulated gate polar transistor (IGBT) modules from *Semikron* (SKM50GB063D), having two switches per module for forming a phase-leg. The three modules were then paralleled to a 420 μF (printed as 470 μF on the capacitor, but measured to be only 420 μF using an LCR meter), 500V dc-link capacitor and a resistive load bank. At the rectifier input end, an LCL-filter was added for better suppressing switching harmonics produced by the rectifier with the overall system powered by a *California Instruments* programmable ac power supply. Further details about specifications and parameter values used for implementing the laboratory system can be found in Table 8-1. A comment raised here is that although the chosen IGBT modules can tolerate 600 V and 70 A, the rectifier power rating is limited to 1.2 kW by passive components used to build the system, which after all is still a reasonably acceptable power rating for testing the proposed OCC technique.

Using the assembled rectifier platform, the first set of experimental tests was conducted to evaluate the performances of both existing and proposed OCC schemes under unbalanced supply voltage condition. Instead of conducting the experiments separately for both schemes, they were tested continuously by first running the existing scheme for the first four cycles from $t = 0$ to 0.08 s, before instantaneously switching to the proposed scheme for the next four cycles from $t = 0.08$ to 0.16 s. Doing so resulted in only a single compact plot for verifying both steady-state and dynamic

Fig. 8-6. Experimental results obtained under unbalanced supply voltage condition.

responses of the proposed scheme, but the total of eight cycles collected was too packed for plotting with full details on the screen of an oscilloscope (suitable for plotting only two to three cycles, as illustrated by some of the figures presented shortly). In addition, seven signals had to be viewed simultaneously at the instant of scheme switchover, which certainly cannot be fulfilled by a four-channel (or even six-channel) oscilloscope. Therefore, for this first set of experimental results, a data acquisition card slotted in a desktop computer was used to collect the recorded data points. The saved experimental data was then plotted in Matlab, and presented as Fig. 8-6, where the uppermost plot shows the unbalanced voltages obtained by adjusting the programmable power supply to include an additional 10% fundamental negative-sequence component with a phase-shift of 180° .

These unbalanced input voltages, together with the existing OCC scheme, cause the dc-link voltage to vary with a prominent 100 Hz ripple during the first four line cycles of Fig. 8-6. Other than the dc-link variation, the input currents captured are observed to be seriously unbalanced in the first four line cycles with the phase a current measured

(a)

(b)

Fig. 8-7. Experimental phase a harmonic spectrum obtained using (a) existing OCC and (b) proposed OCC schemes.

to be 2.55 A lower than the phase b current. As explained earlier, this unbalance is caused by the existing control law forcing the phase currents to follow their corresponding supply voltages closely. Also introduced by the existing control law is a non-zero-sequence third order harmonic, clearly projected by the per phase spectrum plotted in Fig. 8-7(a) for the input currents. As discussed earlier, this third harmonic is created by the interaction between the 2nd dc-link harmonic voltage and fundamental switching function component, and is the main cause for the high 4.66% THD of the phase a current, as reflected by the matching experimental results. Before moving forward, it is commented here that the spectrums in Fig. 8-7, and in fact all spectrums plotted from here onwards, were obtained by collecting a sizable amount of experimental data points using the hardware data acquisition card, and then plotted in Matlab. Plotting in this way is deemed as more accurate than using an oscilloscope, whose main functionality is not really for spectrum plotting. Of course, capturing the spectrums using a spectral analyzer would be the best option, but its cost generally makes this option not too reachable.

To improve the performance of the rectifier, the proposed OCC scheme is enabled at $t = 0.08$ s. As expected, the voltage ripple sensed across the dc-link capacitor is now reduced from 2.23 V to 0.92 V. As a consequence, the non-zero-sequence third harmonic components are no longer prominent in the experimental input currents, as reflected by the phase a current spectrum plotted in Fig. 8-7(b), and the THD of phase a current has now been reduced to 2.78%. The combined effect is then a more

Fig. 8-8. Experimental three-phase input voltages with unbalance and distortion programmed for testing.

balanced set of sinusoidal currents, as demonstrated by the waveforms captured in the next four line cycles, starting from $t = 0.08$ s in Fig. 8-6. In addition to showing the retention of favorable features even under non-ideal input voltage conditions, Fig. 8-6 also shows the smooth dynamic transition at $t = 0.08$ s, during which the proposed OCC scheme is activated with no momentary disturbance (sag or swell) affecting the dc-link voltage and input currents.

The experimental testing was next performed with 10% fifth harmonic (in phase) and 5% seventh harmonic (in phase) added to the supply voltages, in addition to the earlier programmed 10% fundamental negative-sequence component. The combined input voltage waveforms are shown in Fig. 8-8, where the peak of phase a is observed to be 21.4 V lower than those of phases b and c . Using the existing OCC scheme, the three-phase currents drawn from the ac source are severely distorted and unbalanced,

(a)

(b)

Fig. 8-9. Experimental (a) dc-link voltage, ac currents, and (b) phase a harmonic spectrum obtained using the conventional OCC scheme.

as reflected by the waveforms captured in Fig. 8-9(a). To reinforce that observation, Fig. 8-9(b) shows the harmonic spectrum of the phase a current, where the third, fifth and seventh harmonics are observed to be prominent, and summed to give a total harmonic distortion (THD) of 13.10%. The presence of third harmonic current here is again due to its non-zero-sequence nature, and is induced by the 2.87 V of second harmonic measured at the rectifier dc-link. Other than the second harmonic, the dc-link voltage is also measured to have a 0.43 V sixth harmonic, caused by the flow of fifth and seventh harmonics at the ac input end, as explained earlier. The presented results are therefore summarized to match well with those conceptual discussions presented in Section 8.2, hence raising the level of confidence for those mathematical formula derived in that section.

The existing OCC scheme is now replaced by the modified OCC scheme proposed in

(a)

(b)

Fig. 8-10. Experimental (a) dc-link voltage, ac currents, and (b) phase a harmonic spectrum obtained using the proposed OCC scheme.

this chapter, whose control equation is shown in (8.19). As anticipated, the input current waveforms shown in Fig. 8-10(a) are greatly improved with near sinusoidal and balanced wave shape observed throughout the captured time span. This improvement is equally observed in Fig. 8-10(b), where the plotted spectrum clearly shows the reduction of third, fifth and seventh harmonics in the phase *a* current. The measured THD is also lower at 3.46%, which is a sizable improvement, as compared to those non-sinusoidal and unbalanced line currents shown in Fig. 8-9(a). Also observed is a smoother dc-link voltage in Fig. 8-10(a), as compared to that captured in Fig. 8-9(a). Explanation for the smoother dc voltage can be found in Section 8.3, where it is specifically stated that the absence of the second mathematical term in (8.14) is the main reason that causes the dc-link current and voltage to be smoother. In spectral context, the improvement in dc-link voltage quality is attributed to the simultaneous reductions of second and sixth harmonics from 2.87 V to 1.06 V and 0.43 V to nearly 0 V, respectively.

8.5 Summary

In this chapter, the performance of existing OCC-based active rectifier under unbalanced and distorted supply conditions is studied. Specific findings discovered are the unintentional distortions introduced by the existing OCC scheme to the input three-phase currents and output dc voltage when supplied by the set of non-ideal operating voltages. For the ac input end, emphasis is also placed on the flow of non-zero-sequence third harmonic currents, caused by second harmonic sensed at the dc-link, which in turn is caused by negative-sequence component found in the unbalanced ac voltages. Unlike other zero-sequence triplen harmonics, these non-zero-sequence third harmonic currents flow even in a three-wire system, resulting in further distortion at the ac input end.

Mathematical expressions for computing these dominant harmonics have been derived, before using them to subsequently develop a modified OCC control equation that can

produce a smaller dc-link voltage ripple and a more balanced set of sinusoidal three-phase input currents. Relevant concepts on reference reconstruction in the OCC control core, stationary-frame harmonic extraction and experimental testing have all been presented in the chapter to help validate the feasibility and practicality of the proposed OCC control scheme.

Chapter 9 Conclusions and Recommendations

9.1 Conclusions

This thesis began with a review of popular linear controllers and established the relationships among PI, PR and repetitive control. The repetitive control and its many variants appeared to be the most attractive since they each produces a sum of resonant terms at different frequencies for SHC without requiring complex hardware. They however still faced the problem of inaccurate tracking as the frequencies demanded for compensation increase. To overcome that limitation, a new CV based repetitive control scheme in the synchronous frame was proposed and tested with a grid-tied inverter, where precise current regulation at high frequencies might at times be needed. The proposed scheme achieved its performance by taking into account the system complex poles at high frequencies, before nullifying their negative effects by introduced zeros.

To further enhance the stability of the repetitive controller, the poles of the controller were slightly shifted so as to limit its compensation gain and produce a more selective bandwidth. Fortunately, this shifting would not impact the performance of high order current tracking since its influences at those frequencies are negligible. Output current of the inverter was also intentionally synchronized with the unfiltered grid angular frequency, so as to prevent it from being disturbed by background harmonics of the grid. Another contribution related to the CV repetitive scheme was its equivalent derivation in the stationary frame. The resulting controller was definitely easier to implement since it avoids frame transformation.

Without being limited to current control, the proposed CV repetitive scheme could also be used for voltage control, as found in a UPS, for example. The CV voltage controller was implemented as an outer capacitor voltage loop with an inner capacitor current

loop (usually proportional) incorporated for fast regulation purposes. The designed controller was shown to have two control zeros that can be used to accurately cancel out the system complex poles. The dynamics of the system was then solely determined by the controller. Due to the introduction of imaginary terms to the control zeros, this control scheme was also shown to be robust to system parameter variations, whose superiority has already been verified through comparison with existing schemes.

Besides controllers, higher order LCL-filter design and its influence on system stability were adjacently considered. LCL-filter was known to have better switching harmonic filtering, and was recommended for higher power conversion at reduced power losses and system costs. For its studies, special attention was devoted to its influence on system stability caused by resonance. For that, two possible current control schemes were investigated, from which it was found mathematically that converter current feedback yields a more stable system than grid current feedback due to its inherent damping term embedded in the feedback loop.

A theoretical design method for LCL-filter was then presented for choosing the values of passive components so that resonance could be damped solely by feeding back the converter current. The chosen values were usually not the optimum in terms of smallest achievable inductance even though damping is implicitly fulfilled. To produce similar damping for an optimally designed LCL-filter, a compensation strategy was proposed for extracting damping information from the filter capacitor current and then feeding it back to the control loop. With such compensation, appropriate damping coefficient could be freely tuned for minimizing negative effects of LCL resonance.

Next, the LCL-filter was used to construct a SAPF for power quality improvement. Its main advantage was its low line impedance, which then allowed smooth tracking of harmonic currents demanded from a SAPF. Lower voltage drop across the LCL-filter also allowed a smaller dc-link voltage to be sustained. As a consequence, the compensation capacity of the proposed SAPF could significantly be increased without

entering over-modulation zone even for sharp load changes. To further ensure that the system was stable, an active damping method was proposed with its design relationships among system crossover frequency, LCL resonance frequency and converter switching frequency clearly defined. The design procedure was generalized in per unit terms before its application to an analytical example was demonstrated. The designed SAPF was eventually proved in experiment to be operating smoothly, as intended.

Other than linear controllers with LCL-filters, nonlinear controllers with the same LCL-filters should also be considered since the fast dynamic properties of nonlinear controllers were presently unmatchable. For that, OCC was chosen as the base because of its simplicity, robustness and fixed switching frequency in addition to its fast dynamics. Building from this base, the first improved OCC scheme was presented in Chapter 7 for AC / DC active rectifier with an input LCL-filter. Other converter functionalities could certainly be tested, but for this invention, active rectifier was deemed to have the most demanding requirements.

With the input LCL-filter, resonance was again a problem, which was solved here by presenting active and passive damping methods. Instead of the conventional single-edge carrier, a mechanism for producing double-edge carrier was also presented for solving even harmonic problem faced by OCC. This was followed by a way to inject triplen offset to the OCC core so as to extend its operating range. So far, all modifications proposed were for improving the OCC steady-state waveform quality, but only under balanced conditions. To reinforce its performance under non-ideal supply voltage conditions, an extensive set of expressions was derived for analyzing harmonic components found in the ac input current and dc output voltage. Based on this, the inner current reference was broken down into its fundamental and harmonic components, before reconstructing them using calculated scaling factors to compensate for the background grid harmonics. Experimental testing has already confirmed all expected findings.

To conclude, this thesis covered a few challenging topics on control of three-phase PWM converters for modern power electronic applications. All presented schemes can operate with high performances whether with or without grid connection. They can reject external disturbances from the grid and loads, hence providing well-damped power conditioning performances to the systems. Overall costs were reduced, while stability was improved even with higher order LCL-filter considered. Specific findings related to each contribution have already been confirmed in simulation and experimentally with favorable results noted.

9.2 Recommendations for Further Research

This research has generated quite a sizable amount of materials on control and design related issues for power converters. It nevertheless is not exhaustive with some other challenges yet to be explored. These unresolved challenges are briefly discussed here to provide insights for future investigation.

Grid-tied and stand-alone (UPS) modes of operation for three-phase inverters have already been discussed in Chapter 3 and Chapter 4, respectively. During ac mains outage, the inverters may switch to stand-alone mode for ride-through purpose, and after the fault is cleared, it should resynchronize with the grid and switch back to normal grid-tied mode. To ensure safe and seamless transfer between the two modes, the following topics would be of interest for investigation.

- Development of detection methods for grid faults, which might cause under / over-voltage, under / over-frequency, and sudden phase jump. Existing methods can be classified as either passive or active methods with the former representing those schemes that sense for transient events happening in the grid. Active methods, on the other hand, refer to those that probe the grid by sending signals from the inverters. Both methods have their merits, but how they integrate with the repetitive control core might not be that straightforward.

- Design of seamless transfer algorithms that can keep the PCC voltage undisturbed and transfer time short during transition between both control modes. Background harmonics of the grid should be considered during this transient period to minimize disturbances to the local loads. Again, integration of the transfer scheme to the repetitive control core can be explored.

Chapter 5 and Chapter 6 deal with the control of only a single three-phase converter with LCL-filter. Quite often, multiple power converters are connected in parallel for higher power rating or redundancy. Control of such paralleled converters might be much more complicated, and hence is a good topic for future research. The following are some specific aspects to consider.

- Since the converters are connected at some common points, circulating current will flow as soon as a closed circuit loop among the converters is formed due to asynchronous switching. The severity of this current may depend on the PWM strategy adopted, line impedance and switching frequency. Additional control techniques must therefore be added to limit this circulating current.
- Presence of filter capacitors in a multiple-converter grid will lead to a very high order network with various series / parallel resonances. Triggering of these resonances is even more likely when the converters have to cope with harmonics. Proper control scheme must therefore be designed to damp system resonance, and hence gaining stability.

Referring next to those improved OCC schemes presented in Chapter 7 and Chapter 8, they provide precise regulation only for the fundamental and low order harmonic currents. Its application to high order harmonic compensation is presently not pursued, but would be an excellent topic for future research. The following shares some ideas.

- When the ac supply voltage is distorted by higher order harmonics, the

proposed OCC schemes may no longer be applicable. The forward compensation gains should be recalculated by a closed-loop control algorithm so that it can remedy the errors caused by the non-negligible voltage drop across the system impedance.

- Three-phase line impedances are assumed identical for the investigation. Practically, they can be quite different and varying. Depending on the degree of unbalance and amount of uncertainty, inaccuracy might appear with the proposed OCC scheme. Methods to compensate for the unbalance and model the uncertainty are therefore needed, and should be used to adjust the forward compensation gains to nullify the inaccuracy.

Author's Publications

Journal Publications

1. **Y. Tang**, P. C. Loh, P. Wang, and F. H. Choo, "One-cycle-controlled three-phase PWM rectifiers with improved regulation under unbalanced and distorted input-voltage conditions," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2786-2796, Nov. 2010.
2. P. C. Loh, **Y. Tang**, F. Blaabjerg, and P. Wang, "Mixed-frame and stationary-frame repetitive control schemes for compensating typical load and grid harmonics," *IET Power Electron.*, vol. 4, no. 2, pp. 218-226, Feb. 2011.
3. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, and K. K. Tan, "Improved one-cycle-control scheme for three-phase active rectifiers with input inductor-capacitor-inductor filters," *IET Power Electron.*, vol. 4, no. 5, pp. 603-614, May 2011.
4. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, and F. Gao, "Exploring inherent damping characteristic of LCL-filters for three-phase grid-connected voltage source inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1433-1443, Mar. 2012.
5. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Generalized design of high performance shunt active power filters with output LCL-filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1443-1452, Mar. 2012.

Conference Publications

6. P. C. Loh, **Y. Tang**, P. Wang and F. Blaabjerg, "Complex-vector time-delay control of power converters," in *Proc. IEEE-IAS'08*, 2008, pp. 1-8.
7. P. C. Loh, **Y. Tang**, F. Blaabjerg and P. Wang, "Performance evaluation of time-delay control schemes for uninterruptible power supplies," in *Proc. IEEE-ICSET'08*, 2008, pp. 887-892.
8. **Y. Tang**, P. C. Loh, P. Wang, and F. H. Choo, "One-cycle controlled three-phase PWM rectifiers with improved regulation under unbalanced and distorted input voltage conditions," in *Proc. IEEE-PEDS'09*, 2009, pp. 579-584.
9. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, and K. K. Tan, "Improved one-cycle-controlled active rectifiers with high-order input filters," in *Proc. IEEE-ECCE'09*, 2009, pp. 960-967.
10. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, and F. Gao, "Exploring inherent damping characteristic of LCL-filters for three-phase grid-connected voltage source inverters," in *Proc. IEEE-ECCE'10*, 2010, pp. 312-319.

11. **Y. Tang**, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, "Design, control, and implementation of LCL-filter-based shunt active power filters," in *Proc. IEEE-APEC'11*, 2011, pp. 98-105.

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