Advanced control methods and topologies for DC-DC power conversion

Jiao, Yanping

2012

Jiao, Y. (2012). Advanced control methods and topologies for DC-DC power conversion.
Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/50721>

<https://doi.org/10.32657/10356/50721>

ADVANCED CONTROL METHODS AND TOPOLOGIES FOR DC-DC POWER CONVERSION

JIAO YANPING

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University

in fulfillment of the requirement for the degree of

Doctor of Philosophy

2012

Acknowledgment

I would like to express my deepest gratitude to my supervisor, Associate Professor Luo Fang Lin for his invaluable recommendation, guidance, help, and encouragement from the very beginning of my PhD journey to the end. Without his support, I cannot finish my degree.

I wish to express my sincere thanks to Nanyang Technological University. The research work would not be possible without the financial support provided by Nanyang Technological University in the form of a research scholarship.

I am indebted to many people who assisted me in the fulfillment of this research work. Special thanks should be given to Associate Professor Luo Fang Lin's other Ph. D students who are Dr. Zhang Shaoru, Dr. He Yi, Dr. Zhu Miao, Dr. Zhang Jin and Mr. Yu Kun. Thanks are also given to all research students in Electric Power Research Lab (EPRL) for their helpful advice and discussions.

I am also deeply thankful to Mr. Yeoh Tiow Koon, Mr. Lee Ting Yeng, Ms Chew-Sim Annie, Mr. Lim Kim Peow and Ms. Jennifer Tan for the technical support they have given me in the course of my research.

Last but not the least, to my dearest parents and my family, for their unconditional love, unceasing understanding, support and encouragement; to them I dedicate my work.

Table of Contents

TABLE OF CONTENTS	I
SUMMARY	V
LIST OF FIGURES	VII
LIST OF TABLES	X
LIST OF ABBREVIATIONS	XI
LIST OF SYMBOLS	XIII
CHAPTER 1 INTRODUCTION	1
1. 1 DC-DC Converters in Power Electronics	1
1. 2 Motivations	2
1. 3 Organization of the Thesis	4
1. 4 Some Explanations about the Thesis	5
CHAPTER 2 LITERATURE REVIEW	6
2.1 Review of DC-DC Converter Topologies	6
2.2 Modeling Methods for DC-DC Converters	10
2.2.1 State-Space Averaging Method	11
2.2.2 Switching Signal Flow Graph	12
2.2.3 Small-Signal Modeling	14
2.3 Control Methods for DC-DC Converters	16
2.3.1 Linear Control Methods	18
2.3.2 Nonlinear Control Methods	22
2.4 Conclusion	34
CHAPTER 3 MODELING AND CONTROL OF ADVANCED DC-DC CONVERTERS	36
3.1 Introduction	36

3.2	Modeling Analysis of Positive Output Super-Lift Converters	37
3.3	Generalized Improved Sliding Mode Controller	41
3.3.1	Existence Condition	43
3.3.2	Reaching Condition	44
3.3.3	Stability Condition	44
3.4	Case Study: Re-lift Circuit	46
3.4.1	System Description	46
3.4.2	Reduced-Order State-Space Model Verification	48
3.4.3	Stability Performance	51
3.4.4	Regulation Performance with Output Load Variations	52
3.4.5	Regulation Performance with Input Voltage Variations	54
3.5	Conclusion	55
CHAPTER 4 VOLTAGE-LIFT SPLIT-INDUCTOR-TYPE BOOST CONVERTERS		56
4.1	Introduction	56
4.2	Development of Split-Inductor-Type Boost Converter	58
4.2.1	Re-lift Split-Inductor-Type Boost Converter	59
4.2.2	Triple-Lift Split-Inductor-Type Boost Converter	63
4.2.3	N^{th} -Lift Circuit	68
4.3	Modeling and Controller Design	70
4.3.1	Existence Condition	72
4.3.2	Reaching Condition	73
4.3.3	Stability Condition	73
4.4	Simulation and Experimental Results	74
4.4.1	Simulation Results	76
4.4.2	Stability Performance	77
4.4.3	Regulation Performance	78
4.5	Conclusion	80
CHAPTER 5 VOLTAGE-LIFT-TYPE SWITCHED-INDUCTOR CONVERTERS		81
5.1	Introduction	81

5.2	Voltage-Lift-Type Switched-Inductor Cells	82
5.3	Hybrid Boost Converter with Basic SI Cell	86
5.3.1	CCM Analysis	86
5.3.2	DCM Analysis	89
5.4	Hybrid Boost Converter with Self-lift SI Cell	91
5.4.1	CCM Analysis	91
5.4.2	DCM Analysis	92
5.5	Hybrid Boost Converter with Double-Self-Lift SI Cell	93
5.5.1	CCM Analysis	95
5.5.2	DCM Analysis	96
5.6	Hybrid POEL Converter with Basic SI Cell	97
5.6.1	CCM Analysis	99
5.6.2	DCM Analysis	101
5.7	Hybrid POEL Converter with Self-lift SI Cell	104
5.7.1	CCM Analysis	104
5.7.2	DCM Analysis	106
5.8	Hybrid POEL Converter with Double Self-lift SI Cell	107
5.8.1	CCM Analysis	109
5.8.2	DCM Analysis	111
5.9	Summary and Verification	112
5.9.1	Comparison and Discussion of Hybrid POEL Converters	113
5.9.2	Simulation Results	116
5.9.3	Experimental Results	117
5.10	Conclusion	120
CHAPTER 6	N-SWITCHED-CAPACITOR BUCK CONVERTERS	121
6.1	Introduction	121
6.2	Two-Switched-Capacitor Buck Converter	123
6.2.1	Two-Switched-Capacitor Buck Converter in CCM	126
6.2.2	Two-Switched-Capacitor Buck Converter in DCM1	127
6.2.3	Two-Switched-Capacitor Buck Converter in DCM2	128
6.3	Three-Switched-Capacitor Buck Converter	133

6.3.1	Three-Switched-Capacitor Buck Converter in CCM	133
6.3.2	Three-Switched-Capacitor Buck Converter in DCM1	134
6.3.3	Three-Switched-Capacitor Buck Converter in DCM2	136
6.4	N-Switched-Capacitor Buck Converter	137
6.4.1	N-Switched-Capacitor Buck Converter in CCM	141
6.4.2	N-Switched-Capacitor Buck Converter in DCM1	142
6.4.3	N-Switched-Capacitor Buck Converter in DCM2	143
6.5	Case Study	146
6.5.1	CCM Operation of Three-Switched-Capacitor Buck Converter	146
6.5.2	DCM1 Operation of Three-Switched-Capacitor Buck Converter	148
6.5.3	DCM2 Operation of Three-Switched-Capacitor Buck Converter	149
6.6	Conclusion	151
CHAPTER 7 CONCLUSIONS AND RECOMMENDATIONS		152
7.1	Conclusions	152
7.2	Recommendations	153
BIBLIOGRAPHY		155
APPENDIX A MAIN ANALYSIS PRINCIPLES IN DC-DC CONVERTERS		172
A.1	Volt-Second Balance Principle	172
A.2	Charges Balance Principle	173
APPENDIX B ROUTH'S STABILITY CRITERION		174
APPENDIX C AUTHOR'S PUBLICATIONS		176

Summary

Power conversion technology has been used in a great variety of products in modern society, such as industrial equipment, computers, communication devices, aerospace electronics, portable electronics devices and etc.

The corresponding equipment can be divided into four groups, AC-AC converters, AC-DC rectifiers, DC-DC converters and DC-AC inverters. The production of DC-DC converters gets large percentage of the total turnover of all conversion equipment production. Study of DC-DC converters has always been a hot research area due to many reasons which include (1) the technical challenges keep coming due to the wide application of DC-DC converters, and (2) they are highly nonlinear systems which increase the difficulty for modeling and control.

Modeling and control are two important issues when a DC-DC converter is being investigated. In this thesis, generalized state-space modeling, especially reduced-order state-space modeling method, is used to describe the main characteristics of the advanced DC-DC converters. Sliding Mode (SM) control, as a variable structure control, is very suitable for DC-DC converters which are variable structures basically. An improved SM controller is designed and applied to positive output super-lift converter. The theoretical analysis and experimental results show the improved SM controller can largely suppress the output voltage error and get satisfactory steady state and transient performances.

In the traditional DC-DC converters (buck, boost, Ćuk, SEPIC...), the effect of parasitic elements comes into picture at high duty cycle U , so the practical value of U has an upper limit. It is difficult to operate at high duty cycles and hence to achieve high voltage transfer gains in those traditional DC-DC converters mentioned above. A step-down or step-up transformer used in the converters can cause switching surges. Cascade connection of two or more traditional converters has the difficulty of the control because of multiple switches in different stages besides the increased power loss increase. With the fast development of technologies, this disadvantage limits the further applications of those

traditional converters in some areas that require higher voltage transfer gains such as renewable energy systems. Therefore, an in-depth research on advanced DC-DC power conversion topologies used in renewable energy systems is the main part of this thesis. Compared to the traditional converters with simple structures, advanced DC-DC converters are named because they usually have higher-order structures with new techniques involved, such as Voltage-Lift (VL) technique, Switched-Inductor (SI) Switched-Capacitor (SC) structures.

Voltage-Lift (VL) technique is an effective method that is widely applied in electronic circuit design, especially in the radio engineering. It also can be utilized to improve the performance and characteristics of DC-DC converters. A set of Voltage-Lift Split-Inductor-type boost converters is described in this thesis, which can get much higher step-up voltage transfer gain. They can be applied to boost the DC voltage to 400 V DC bus in 3 kW solar power systems, where the output voltage of the solar panels is around 30 V.

Recent years, Switched-Inductor (SI) converters and Switched-Capacitor (SC) converters are developed in DC-DC converter family. In this thesis, a set of Voltage-Lift-type Switched-Inductor cells are designed to get higher voltage transfer gain, which is inspired by the combination of VL technique and SI structure. Hybrid DC-DC converters with these cells can applied to boost the DC voltage to 200 V DC bus in 1kW solar power systems.

N-Switched-Capacitor buck converters can get even higher step-down voltage transfer gain, which are also inspired by VL technique. This series of converters can be used into low voltage and high current situations, like 12 V/100 W automobile power supply.

The advanced DC-DC converters introduced in this thesis enriched the DC-DC converter family and at the same time provided flexible and competent choice when building renewable energy systems or some other applications.

List of Figures

Figure 1-1	The DC-DC converter family tree.....	3
Figure 2-1	The generalized representation of second-order DC-DC converters	6
Figure 2-2	The generalized representation of fourth-order DC-DC converters	7
Figure 2-3	The buck converter.....	12
Figure 2-4	The graphical large-signal model of the buck converter.....	14
Figure 2-5	The small-signal model of the buck converter.....	14
Figure 2-6	A general representation of DC-DC power conversion system.....	18
Figure 2-7	Voltage mode control of buck converter.....	19
Figure 2-8	Peak current mode control of boost converter	21
Figure 2-9	Average current mode control of buck converter	22
Figure 2-10	One-cycle controlled buck converter	24
Figure 2-11	Buck converter phase portraits under SM control	27
Figure 2-12	Buck converter's start-up performance under SM control.....	27
Figure 2-13	Buck converter controlled by SM controller with two state variables' feedback	29
Figure 2-14	Equivalent control version of SM controlled buck converter	31
Figure 3-1	Elementary Positive Output the super-lift converter [35]	36
Figure 3-2	Generalized circuit of the super-lift converters with n-cell cascaded structure	38
Figure 3-3	The logic structure of the improved SM controller.....	43
Figure 3-4	The start-up response comparisons	50
Figure 3-5	The configuration of re-lift circuit with the improved SM controller.....	51
Figure 3-6	The enlarged steady state waveforms	52
Figure 3-7	The experimental curves when the output load varies.....	53
Figure 3-8	The experimental curves when the input voltage varies	54
Figure 4-1	Topologies of the existing Split-Inductor-type boost converters.....	57
Figure 4-2	Topology and equivalent circuits of the re-lift Split-Inductor-type boost converter.....	59

Figure 4-3	Waveforms of the energy components of re-lift circuit in different operation modes	60
Figure 4-4	Topology and equivalent circuits of the triple-lift Split-Inductor-type boost converter.....	64
Figure 4-5	Waveforms of the energy components of triple-lift circuit.....	65
Figure 4-6	Topology and performances of VL Split-Inductor-type boost converters	69
Figure 4-7	Triple-lift circuit with SM controller	76
Figure 4-8	Inductor currents of triple-lift circuit under different operation modes	77
Figure 4-9	Stability performances of triple-lift circuit when $V_{in} = 30\text{ V}$ and $R = 50\ \Omega$..	78
Figure 4-10	Regulation performances of triple-lift circuit	79
Figure 5-1	The basic SI cell	83
Figure 5-2	The self-lift SI cell	84
Figure 5-3	The double-self-lift SI cell	85
Figure 5-4	Hybrid boost converter with the basic SI cell	87
Figure 5-5	Hybrid boost converter with the self-lift SI cell.....	90
Figure 5-6	Hybrid POEL converter with the double-self-lift SI cell	94
Figure 5-7	Topology of the POEL converter.....	98
Figure 5-8	Hybrid POEL converter with the basic SI cell.....	99
Figure 5-9	Hybrid POEL converter with the self-lift SI cell	103
Figure 5-10	Hybrid POEL converter with the double self-lift SI cell	108
Figure 5-11	Relationship between the voltage transfer gain and the duty cycle and the normalized load	115
Figure 5-12	Simulation results of inductor currents for the three cases in CCM and DCM	117
Figure 5-13	Start-up response and transient response from CCM to DCM	118
Figure 5-14	Transient response when then R changes from $30\ \Omega$ to $10\ \Omega$ at 0.035 s and back to $30\ \Omega$ at 0.036 s.....	119
Figure 5-15	Voltage stresses of the main switches	119
Figure 6-1	Operations of two-Switched-Capacitor buck converter.....	124
Figure 6-2	Key waveforms of the energy elements in two-Switched-Capacitor buck converter.....	125
Figure 6-3	Operations of three-Switched-Capacitor buck converter.....	131

Figure 6-4	Key waveforms of the energy elements in three-Switched-Capacitor buck converter.....	132
Figure 6-5	Operations of n -Switched-Capacitor buck converter.....	139
Figure 6-6	Key waveforms of the energy elements in n -Switched-Capacitor buck converter.....	140
Figure 6-7	Three-Switched-Capacitor buck converter performances in CCM with $R = 0.1 \Omega$ and $u = 0.5$	147
Figure 6-8	Three-Switched-Capacitor buck converter performances in DCM1 with $R = 1 \Omega$ and $u = 0.5$	149
Figure 6-9	Three-Switched-Capacitor buck converter performances in DCM2 with $R = 4 \Omega$ and $u = 0.5$	151

List of Tables

Table 3-1 Specifications of the re-lift circuit	49
Table 4-1 Main characteristics of the series of VL Split-Inductor-type boost converters.	70
Table 4-2 Specifications of the triple-lift Split-Inductor-type boost converter	75
Table 5-1 Main characters of hybrid POEL converters with different SI cells	113
Table 6-1 Main characteristics of the n -Switched-Capacitor buck converters	145

List of Abbreviations

AC	Alternating Current
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital signal processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
GM	Gain Margin
GTO	Gate-Turn-Off (thyristor)
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
P	Proportional
PI	Proportional-Integral
PID	Proportional-Integral-Differential

PM	Phase Margin
PWM	Pulse Width Modulation
RP	Representing Point
SC	Switched-Capacitor
SEPIC	Single-Ended Primary-Inductor Converter
SI	Switched-Inductor
SM	Sliding Mode
SMPS	Switch Mode Power Supply
SSFG	Switching Signal Flow Graph
UPS	Uninterruptible Power Supplies
VL	Voltage-Lift
VSC	Variable Structure Control
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

A_1, A_2	State matrixes during switching-on and -off
B_1, B_2	Input matrixes during switching-on and -off
C_n	n^{th} capacitor
d	Input signal
$e(s)$	Error signal
f_c	Effective output filter corner frequency
f	Switching frequency
G_1, G_2	Signal flow graphs
$g(s)$	Compensator
$G_{u(s)}$	Control-to-output transfer function
$G_{vin(s)}$	Input-to-output transfer function or the audio-susceptibility
I	Unity matrix
i_L	Inductor current
L_n	n^{th} inductor
m	Current filling efficiency
M	Voltage transfer gain
M_{Buck}	Voltage transfer gain of buck converter
M_{CCM}	Voltage transfer gain in CCM

M_{DCM}	Voltage transfer gain in DCM
R	Output load
R_+	Output load of the positive conversion path
R_-	Output load of the negative conversion path
$R_{DS(on)}$	ON-state resistance of the active switches
S	Sliding surface function
s	<i>Laplace</i> operator
T	Switching period
T_M	Limited minimum switching period
T_{off}	Switching-off period
T_{on}	Switching-on period
T_{SW}	The desired switching period
U	average duty cycle
u	instant duty cycle
u_{eq}	equivalent duty cycle
v_C	Capacitor voltage
V_D	Reversed voltage on a diode
v_{in}	Source voltage
$\hat{v}_{in}$	Perturbations of the source voltage
V_{in}	Average source voltage

v_o	Output load voltage
$\hat{v}_o$	Perturbations of the output voltage
V_o	Average output voltage
V_s	Voltage stress on a switch
v_X	Instantaneous voltage of the component X
$\hat{v}_X$	Voltage perturbations
V_X	Average voltage of the component X
w	Control input
X	average state vector
x	instant state vector
Z_N	Normalized load
Z_{NB}	Boundary normalized load
$Z_{out(s)}$	Output impedance
ξ	Variation ratio of the inductor current or the diode current
σ	Switching function

Chapter 1 Introduction

The research history on DC-DC converters is introduced, and then the research motivation in this area is explained, different types of DC-DC converters are summarized in the DC-DC converter family tree. The organization of the thesis is described to give a clear and short introduction to the contents of this thesis. Some explanations are made so that it is easier to conduct the analysis in the following chapters.

1. 1 DC-DC Converters in Power Electronics

Advanced power conversion techniques have important applications in modern technology and are now used in a great variety of products [1-10], including industrial controls, electric motor drives, Uninterruptible Power Supplies (UPS), traditional power systems and renewable power systems, regulated power supplies for computers, telecommunication equipment and other electronic devices. The power conversion equipment, which is a major area in the field of power electronics, can be divided into four groups: (1) DC-DC converters; (2) DC-AC inverters; (3) AC-DC rectifiers; (4) AC-AC transformers and converters. Products of the first two kinds of conversions contribute to most of the world Switch Mode Power Supply (SMPS) market, especially the DC-DC converters [11].

DC-DC conversion technique was established in the 1920s. The simplest DC-DC converter is a voltage divider (such as rheostat, potentiometer and so on) which can only transfer output voltage lower than input voltage with poor efficiency. The multiple-quadrant chopper is the second step in DC-DC power conversion. Much time has been spent trying to convert one DC voltage to another DC voltage, as a transformer employed in AC-AC conversion does. Some preliminary types of DC-DC converters were used in industrial applications before the Second World War. Research was blocked during the war, but applications of DC-DC converters were recognized. After the war, communication technology developed very rapidly and required low voltage DC power

supplies. This resulted in the rapid development of DC-DC power conversion techniques, and several preliminary prototypes were derived from choppers. Switching DC-DC converters have been in existence since the 1950s. However, the unavailability of reliable and low-cost power transistors had limited their applications primarily to the military and space applications. The advances and availability of modern power semiconductor devices in the early 1970s have made the switching DC-DC converter a popular choice in power supplies and DC motor drives.

Switching DC-DC power conversion technology is therefore a major subject area in the field of modern power engineering and drives, and has been under development for six decades. Switching DC-DC converters are widely used in industrial applications and computer hardware circuits, and DC-DC conversion techniques have developed very quickly. In addition to its high growth rate, the DC-DC converter market is undergoing dramatic changes as a result of two major trends in the power electronics industry: low voltage and high power density.

1. 2 Motivations

DC-DC converters have been systematically classified into six categories according to their characteristics and development sequence. This classification grades all DC-DC converters and categorizes new prototypes, and it can be referred to in [3]. Following this principle, it is now easy to sort and allocate DC-DC converters and assess their technical features. The simplified family tree of DC-DC converters is constructed and shown in Fig. 1-1. It is seen that development and application of the VL technique resulted in series of converters. Also, the Switched-Capacitor (SC) and Switched-Inductor (SI) converters are new to the DC-DC converter family tree. At present, the research on this area is not enough. Therefore, the exploration of new DC-DC power conversion topologies based on the VL technique and SC and SI technique might be a potential and valuable area for the research on topologies of DC-DC converters.

However it is important to find a good way to model and control advanced DC-DC converter systems so that the performance of the advanced DC-DC converters can be analyzed and controlled satisfactorily.

As modern technology develops, there are more and more situations where even higher voltage transfer gains and better output performance are required. Thus, it is necessary to further research on the topological development of advanced DC-DC converters.

Figure 1-1 The DC-DC converter family tree

1.3 Organization of the Thesis

Existing DC-DC converter topologies are introduced and traditional modeling and controlling methods are given so that the background of this DC-DC converter research area is given, see Chapter 2.

Reduced-order state-space modeling is analyzed and applied to all the advanced DC-DC converters in this thesis. An improved Sliding Mode (SM) controller based on a new sliding surface is designed for advanced DC-DC converters. Thus the dynamic response is improved and steady state error in the output is largely suppressed. Positive output super-lift converter is analyzed to show the reduced-order state-space modeling and the improved SM controller is applied to make the performance satisfactory, which is an effective control method for advanced DC-DC converters, see Chapter 3.

A series of Voltage-Lift Split-Inductor-type boost converter is described. Much higher voltage transfer gain is obtained due to the implementation of VL technique. CCM and DCM analysis are given for re-lift, triple-lift and n^{th} -lift circuit respectively. The main characteristics of this series of converters are verified through the experiments on triple-lift circuit with the improved SM controller which is based on reduced-order state-space modeling, see Chapter 4.

The concepts of the Voltage-Lift-type Switched-Inductor cells are described, which can step up the output voltages of DC-DC converters to higher levels. These SI cells can be widely applied to those circuits where strong DC-DC boost abilities are needed. Examples of hybrid boost converters integrated with this series of SI cells are given to show the application into second-order DC-DC converters. Hybrid POEL converters integrated with the various SI cells are analyzed to show the application in high-order DC-DC converters, see Chapter 5.

A series of n -Switched-Capacitor buck converters are examined. They have the advantages of smaller size and easier controlling algorithm compared to cascade buck converter, higher efficiency compared to the quadratic converter reported in former literature. The most important is that they can provide even steeper step-down voltage to satisfy some extreme low-voltage high-current applications. These converters can work

under different DCM situations with different loads and the voltage transfer gains will be a little higher than that in CCM. A case study of three-switched-capacitor buck converter is conducted to verify the theoretical analysis, see Chapter 6.

Finally, a summary of the research work and some suggestion for further developments are given in Chapter 7.

1. 4 Some Explanations about the Thesis

In the theoretical analysis thereafter, the following two assumptions are made:

- (1) All components are ideal, i.e. the ON-state resistance $R_{DS(ON)}$ of the active switches, the forward voltage drop of the diodes and the Equivalent Series Resistances (ESRs) of the inductors and capacitors are ignored.
- (2) All capacitors are sufficiently large, and the voltage stress across the capacitors can be treated as constant.

For any component X in this thesis, its instantaneous current and voltage are expressed as i_X and v_X , its average current and voltage during a switching cycle in the steady state are expressed in I_X and V_X . All reference directions of currents and voltages can be referred to in the corresponding figures. For general description, each component is ideal and the output power is equal to the input power, $V_o I_o = V_{in} I_{in}$. The normalized load is defined as $Z_N = R / fL$, where f is the switching frequency ($f = 1 / T$). The duty cycle of the switches is denoted as u ($0 < u < 1$). Any parameter with the subscript B indicates the boundary value between CCM and DCM.

Chapter 2 Literature Review

The development of the DC-DC converter topologies is introduced from the basic traditional converters to high performance converters applied in some new technological areas recent years, most of them couldn't provide very high voltage transfer gain as well as having a reasonable cost and good performance. Then the modeling methods are reviewed, different methods have different advantages and disadvantages. Then existing control methods are examined, especially Sliding Mode control and some methods trying to improve its performance are introduced.

2.1 Review of DC-DC Converter Topologies

A simple switching DC-DC converter consists of one active power switch (usually one GTO/MOSFET/IGBT), one passive power switch (diode), one inductor and one capacitor, as shown in Fig. 2-1. Since there are two energy storage elements, they are usually termed as second-order DC-DC converters. The different arrangements of these storage elements and switches generate different topologies of switching DC-DC converters, such as buck converter, boost converter and buck-boost converter.

Figure 2-1 The generalized representation of second-order DC-DC converters

The principle merits of these second-order switching converters are their high conversion efficiency and high power density, which result in significant weight

reduction. However, their voltage transfer gains are limited due to their simple structures. Buck converter is a step-down converter, and the voltage transfer gain M_{Buck} is equal to the duty cycle U . Buck-boost converter is a negative output converter, and the absolute value of the voltage transfer gain $M_{buck-boost}$ is equal to $U / (1 - U)$, which can step down or step up the output voltage. Boost converter can provide a step-up function, and the voltage transfer gain M_{Boost} is equal to $1 / (1 - U)$.

The fourth-order DC-DC converters can be considered as the development of simple second-order topologies. Each fourth-order converter consists of one active power switch, one passive power switch, two inductors and two capacitors, as shown in Fig. 2-2. Different arrangements of these storage elements and switches generate different topologies of switching DC-DC converters. They are SEPIC converter, Ćuk converter and elementary Luo converter [3].

Figure 2-2 The generalized representation of fourth-order DC-DC converters

Applications of fourth-order topologies have been developing very fast in recent years; however, their voltage transfer gains are still not high, which have seriously limited their industrial applications in some areas required high voltage transfer gains. For SEPIC converter and Ćuk converter, both of their absolute voltage transfer gains are equal to $U / (1 - U)$.

Recently high performance converters with high voltage transfer gains have been widely studied for many industrial applications, such as car auxiliary power supplies, medical equipment, high intensity discharge headlamps, battery-discharged DC converter

in UPS system and fuel-cell based DC converter [12-24]. New technologies are requiring a higher voltage transfer gain, which is usually greater than four.

However, high voltage transfer gains cannot be easily realized by conventional step-up converters due to the narrow allowed duty cycle range. For these converters, the voltage transfer gain is a function of the modulating control signal of the active switch. Therefore, the high voltage transfer gains can be obtained using conventional PWM converters by: (1) operating at extremely low or high duty cycles U with the corresponding limitations on the finite commutation times of the switching devices; or (2) using a transformer with the corresponding difficulties in switching surges and operating frequencies; or (3) cascade connection of two or more traditional converters with the loss increase and the difficulty of the control because of multiple switches in different stages.

In theory, higher voltage transfer gains can be obtained by properly adjusting the duty cycle. In practice, the maximum and the minimum attainable voltage transfer gains for the conventional converters are limited by the characteristics of the switching devices. The turn-on time and turn-off time of the active switch now play an important role for the attainable duty cycle and, consequently, in the voltage transfer gain. Also, when the duty cycle is close to 0 or 1, great deterioration on the output voltage and inductor currents occur. For the above reasons, it is better to select an operating point in the midrange, i.e., $U = 0.5$.

One often-used approach is to use step-down or step-up transformers. However, large switching surges are present that may damage the switching devices and make the controller difficult to design. Also, the transformer itself would limit the switching frequency of the converter and the power density.

A scheme that provides high voltage transfer gains is the cascade connection of conventional converters. This scheme is a multistage approach that consists of two or more converters connected in cascade. One of the major advantages of these converters is a high voltage transfer gain; however, a drawback is that the total efficiency may be low if the number of stages is large, mainly caused by losses in the switching devices. Matsuo and Harada [12] introduced the cascade connection of buck and buck-boost converters to

obtain low-voltage in power supplies. Maksimovic and Čuk [13] designed several topologies of quadratic converters and discussed the DC operating conditions. A large voltage reduction can be obtained using two-stage topologies with a buck converter in the first stage, which regulates the output voltage, and an isolated converter in the second stage, which operates with 50% duty cycle like a “DC transformer” to step down the voltage. Additionally, J.A. Morales-Saldana [25] and M. Veerachary [26-28] performed the systematic research on theoretical modeling for the cascade connection. The interesting scheme is to have n converters connected in cascade with a single active switch, which are mainly from F.L. Luo [3] and T.F. Wu [29-31]. This class of converters can be used only when the required number of stages is not very large, as the efficiency will be reduced.

Recent years an advanced DC-DC conversion enhancement method, Voltage-Lift (VL) technique has been developed by F.L. Luo [32-41]. The main objective is to construct novel DC-DC topologies which can reach high efficiency and high power density with simple structures. The positive/negative/double output Luo converters have been successfully constructed and termed by the name of their inventor F.L. Luo. A series of VL Luo converters are developed. What's more, super-lift circuit and its VL series and ultra-lift circuit are developed base on that technique. The VL technique is extended to SEPIC converter and Čuk converter by M. Zhu in recent couple of years [42-43]. Both inductors and capacitors play important roles in the VL technique, and all inner capacitors are fully charged by the power source. Moreover, fewer power switches (usually single switch or two synchronous switches) are included in VL structures and avoid complex multiple-switch control schemes.

Switched-Capacitor (SC) converters can also provide higher voltage transfer gains than the conventional topologies. Some new SC converters were described by A. Ioinovici [44-46] and F.L. Luo [47]. Theoretically, any voltage transfer gains can be achieved by increasing the number of capacitors. Therefore, this type of power electronic circuit may serve as another solution to new challenges of high voltage transfer gains and small size in low-power DC-DC converters. It is well known that the main advantage of SC technique is the absence of inductors, making smaller size and higher power density

possible. But more switches are required in SC converters than in magnetic-based converters. Recently, a systematic, topology-based method of designing new converters was developed by A. Ioinovici in [48], in which the duality principles between the basic Switched-Capacitor (SC) cell and the basic Switched-Inductor (SI) cell [49-51] are used for higher voltage transfer gains.

At the same time, Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) technique can also be applied to all the converter topologies mentioned above to improve the performance. Some active clamp circuits are used to realize ZVS for both main and auxiliary switches and the high voltage transfer gains, in which the voltage stress of main switch can be effectively limited by the active clamp circuit [14].

2.2 Modeling Methods for DC-DC Converters

DC-DC converters are nonlinear, time-variant systems. The straightforward analysis tools such as the Laplace transform and the Nyquist plot cannot be applied directly. Therefore, a major goal in the study of these systems has been the development of modeling techniques. The study is always dealing with nonlinear problems and has attempted to explore methods not normally used in other circuit design areas. The state-space averaging [52-63], sampled data modeling [10, 64], quasi-linear modeling [65], and phase-plane trajectory analysis [66] and some other modeling methods [67-70] are several methods that have been derived.

In fact, different models are needed for different stages or aspects of the controller design. Even for a specific stage of the design, there are likely to be several possible models differing from their explicitness, complexity, accuracy, domain of definition, flexibility, and tractability. Several examples are given here: Energy factor modeling [71] is aimed to approximate high-order DC-DC converters as a second-order system; impedance of non-resistive load is included for exact prediction of circuit performance in [72]; and the parasitic components is included into the averaged circuit models in [73]. Nevertheless, almost all modeling methods, including the most popular one, state-space

averaging, will result in a multi-variable system with state-space equations, ideal or nonideal, linear or nonlinear, in steady state or for dynamic purpose.

Here, three most popular modeling methods for DC-DC converters are reviewed, which are state-space averaging method, switching signal flow graph (SSFG) and small-signal modeling. From the analysis below, it will be seen that different modeling methods have different emphasis, thus will be selected according to various analytical purpose.

2.2.1 State-Space Averaging Method

State-space averaging method is an approximation technique that regards switching converter as a continuous linear system. It was firstly described by R.D. Middlebrook and S. Ćuk. State-space averaging method requires that the effective output filter corner frequency f_c should be much smaller than the switching frequency f (i.e. $f_c/f \ll 1$). The mathematical model derived from the state-space averaging method permits the designer to determine the steady-state performance and small-signal transfer functions of the switching converter.

State-space averaging method has been proven to be a very popular analysis technique to derive various performance characteristics of PWM DC-DC converters. This general method has led to understanding of dynamic performance of PWM converters.

State-space averaging procedure is as follows:

- (1) Identify switched models over a switching cycle. Draw the linear switched circuit model for each sub-mode of the switching converter.
- (2) Identify state variables of the switching converter. Write state equations for each switched circuit model using Kirchoff's voltage and current laws.
- (3) Perform state-space averaging using the duty cycle as a weighting factor and combine state equations into a single state-space averaged equation shown as

$$\dot{x} = [A_1u + A_2(1-u)]x + [B_1u + B_2(1-u)]d \quad (2-1)$$

Where: x is the state vector and d is the input signal;

A_1 and A_2 are the state matrixes during switching-on and -off;

B_1 and B_2 are the input matrixes during switching-on and -off.

For example, the state-space averaging method is illustrated for an ideal buck converter shown in Fig. 2-3. The state-space averaged equations for the buck converter are shown in (2-2).

$$\begin{bmatrix} \dot{v}_o \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{u}{L} \\ 0 \end{bmatrix} v_{in} \quad (2-2)$$

Figure 2-3 The buck converter

2.2.2 Switching Signal Flow Graph

As for the circuit designing, especially when the converter circuit contains a large number of elements or many power stages, the linearized models, derived from these traditional methods, will not be suitable, as they can only predict the small-signal stability rather than the large-signal stability information. Therefore, the Switching Signal Flow Graph (SSFG) method has been introduced by K.M. Smedley and S. Ćuk [74] for modeling some complex DC-DC topologies [74-76, 26-28]. The advantages of this graphical method over other methods are [77]:

(1) The switching converter (two or multi-state) can be converted into a unified dynamic model.

(2) From unified model, large-signal, small-signal and steady-state models can be derived.

(3) Minimum mathematical manipulations can be realized for small-signal models.

(4) When it is combined with TUTSIM and MATLAB simulators, large-signal global behavior can be obtained easily.

(5) Various relationships among the circuit variables can be derived without any difficulty.

(6) The cause and effect relationship of the dynamics can be incorporated.

With the SSFG, a given switching converter can be timely divided into two sub-modes corresponding to the switching states of the active switch. Since the sub-mode is linear, corresponding signal flow graphs G_1 and G_2 can be obtained. These two flow graphs can be combined to form an SSFG by the following:

$$G = \sigma G_1 + (1 - \sigma) G_2 \quad (2-3)$$

Where: σ is switching function

$$\sigma = \begin{cases} 1 & 0 < \sigma < uT \\ 0 & \text{otherwise} \end{cases}$$

Equation (2-3) introduces two basic switching branches in G , σ branch and $(1 - \sigma)$ branch [74-75]. The corresponding transmittance of the σ branch is equal to the duty cycle u while the corresponding transmittance of the $(1 - \sigma)$ branch is equal to $(1 - u)$. Since the switching branches are the only nonlinear components in an SSFG, replacing the switching branches with their models yields the unified steady-state, large-signal, and small-signal models for any given DC-DC converter. For example, the large-signal model of the buck converter in Fig. 2-3 is obtained and shown in Fig. 2-4.

Figure 2-4 The graphical large-signal model of the buck converter

2.2.3 Small-Signal Modeling

The small-signal analysis and frequency domain design method are important since many control objectives are evaluated through them. The DC-DC converter's small-signal model can be represented as in Fig. 2-5. A DC-DC converter may encounter condition variations mainly from three sources: the input voltage, the output load, and the control signal. Three transfer functions can be defined as below regarding the converter performance under these cases.

Figure 2-5 The small-signal model of the buck converter

The system state-space equation is represented as

$$\dot{X} = A(X, u) + B(u) \cdot V_{in} \quad (2-4)$$

Where X is the state vector, u is duty cycle, $A(X, u)$ and $B(u)$ are the state matrices.

The small-signal equation can be written as

$$\delta \dot{X} = A \cdot \delta X + B \cdot \delta V_{in} + B_U \cdot \delta u \quad (2-5)$$

The last variable of X is considered as the output voltage. Therefore, the output equation is written as

$$\begin{aligned} \hat{v}_o &= C \cdot \delta X \\ C &= [0 \quad 0 \quad \dots \quad 1] \end{aligned} \quad (2-6)$$

The control-to-output transfer function $G_u(s)$ is found by setting $\hat{v}_{in}(s)$ and $\hat{i}_o(s)$ to zero, and then the transfer function from control to output is obtained as

$$G_u(s) = \frac{\hat{v}_o(s)}{\hat{u}(s)} = C \cdot (sI - A)^{-1} \cdot B_u \quad (2-7)$$

Where s is the *Laplace* operator and I is the unity matrix. This transfer function describes how the control input variations influent the output voltage. Under the condition of closed-loop control, this is the main concern to controller designs. It specifies the system capability in tracking the reference input.

The input-to-output transfer function $G_{vin}(s)$ is derived by setting $\hat{i}_o(s)$ and $\hat{u}(s)$ to zero

$$G_{in}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = C \cdot (sI - A)^{-1} \cdot B \quad (2-8)$$

It is also called the audio-susceptibility of DC-DC converters. It describes how the input voltage variations influent the output voltage. It is of great interest since there are always some input voltage variations caused by the undesired harmonics sourced from AC power line.

To find the output impedance $Z_{out}(s)$, the output current should be written into the equation in replacement of the load resistance. Then, it is found by setting $\hat{u}(s)$ and $\hat{v}_{in}(s)$ to zero,

$$Z_{out}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} \quad (2-9)$$

The output impedance $Z_{out}(s)$ describes how the load variations influence the output voltage. It is especially important in DC-DC converters used in computer power supplies, where some parts of the loads are switched on and off regularly.

Although the controllers of DC-DC converters are different, their control performance can be evaluated through the above criteria in most conditions. And small-signal perturbations method is often used to analyze the closed-loop system.

2.3 Control Methods for DC-DC Converters

The main challenges existing in the present control systems of DC-DC converters can be classified as [78]: (1) with the development of communication and information technology, lower and lower voltage level is used. The ripple voltages and voltage variations during transients in the output voltage of DC-DC converters should be kept at a relatively low level for stable operations; (2) the efficiency of the conversions should be increased so that smaller heat sinks can be used to increase power-density of DC-DC converters; (3) other requirement for DC-DC conversions such as higher reliabilities and lower costs.

In an ideal condition, the output of DC-DC converters is easily calculated according to the input voltage and duty cycle. However, in practice, open-loop control cannot guarantee high reliability and satisfactory dynamic response. Closed-loop control is often needed. The reasons include:

(1) Due to the uncertainties and power losses of the converters, the desired duty cycle cannot be calculated with high accuracy and output steady state error often exists in open-loop control.

(2) The parasitic effects of passive components and nonideal switches in the circuit are difficult to be measured so that it is not easy to be considered in the open-loop control.

(3) Open-loop properties of DC-DC converters are not acceptable in various aspects, such as the overshoot of output voltage and the stress for electric components during start up are very high.

(4) When the circuit conditions change, such as input voltage variations, load resistance variations and even circuit fault, open-loop control cannot provide acceptable dynamic performance and safe operations.

From the 1960's, the studies of the control systems for DC-DC converters have been attracting much attention. The control issues treated in DC-DC converters fall into two main categories:

(1) Control performance [79]: This issue refers to the accuracy, robustness, and stability of the controller, and also the complexity of the controller in terms of the sensors and computational requirements. It also refers to the dynamic performance of the controller. It includes the disturbance rejection, the ripple content, and the response to an input transient, especially, the disturbances originated from the input voltage variations and the load variations. It also includes the reference-to-output transfer function, which is the controller dynamic performance in tracking a reference change. The rising time, overshoot and settling time in the output voltage waveform are also important indexes when evaluating the performance of a controller.

(2) Nonlinear phenomena [8, 66]: DC-DC converters are nonlinear systems due to the nonlinear components (e.g., the power switches and diodes) and gate signals (e.g., on or off). The nonlinear phenomena includes the bifurcations (sudden changes in operating mode), coexisting attractors (alternative stable operating mode), and chaos (apparently random behavior).

Normally, various controllers for DC-DC converters can be sorted into two groups: linear and nonlinear ones. Linear control methods refer to those based on linearized small-signal models, such as the P, PI and PID compensator. Any controller which incorporates nonlinear theory can be viewed as a nonlinear one. Fuzzy logic control, Sliding mode (SM) control, adaptive control and robust control are the nonlinear control methods often used for DC-DC converters. It is difficult to give clear boundaries for

various control methods. For example, adaptive control can be combined with SM control to gain a better performance. Reference [80] has introduced several nonlinear control methods and shown some possible combinations. The review of these controllers in this thesis is categorized in following groups: (1) traditional linear controllers including voltage mode control, peak current mode control and average current mode control; (2) nonlinear controllers using input voltage feed-forward control, fuzzy logic control, SM control and adaptive control. A general representation of DC-DC power conversion system is shown in Fig. 1-6 for the following introduction.

Figure 2-6 A general representation of DC-DC power conversion system

2.3.1 Linear Control Methods

A. Voltage mode control

A control circuit is required in DC-DC converters for the following reasons: (1) to reduce the DC error; (2) to reduce the sensitivity of the closed-loop gain to component values over a wide frequency range; (3) to achieve a fast transient response to sudden changes in the input voltage and/or the output load; (4) to reduce the input-to-output noise transmission; (5) to reduce the closed-loop output impedance, and (6) to satisfy the sufficient degree of relative stability, that is, to ensure a sufficient gain margin (GM) of the order of -12dB and phase margin (PM) of the order of 45° - 60° [81].

The control loop is set up so that the output voltage is compared to a reference voltage by an error amplifier. This amplified error voltage is then compared to a saw-tooth wave

signal, and the PWM comparator sets the duty cycle for the power switch. A voltage mode control circuit for buck converter [82] is set up as shown in Fig. 2-7.

Figure 2-7 Voltage mode control of buck converter

B. Peak current mode control

The peak current mode control loop is set up so that the output voltage of the error amplifier is not compared to a saw-tooth waveform, but to a ramp signal which represents the inductor current. Here, the output of the voltage error amplifier is the reference current.

In peak current mode control, a constant frequency clock turns the switch on at the beginning of each switching cycle. The switch current starts growing until it reaches the control reference, and then the comparator changes its state and turns the transistor off.

When peak current mode control was first used, an occurrence known as sub-harmonic oscillation was discovered. It causes the switch pulse to toggle between a long and short pulse. This can only happen with duty cycles greater than 0.5. Designs that require a duty cycle larger than or equal to 0.5 can be fixed by adding slope compensation [83], which is to add a bit of a saw-tooth waveform to the sensed current information or equally subtract a bit of a saw-tooth waveform from the current reference. The more slope compensations are used, the more the behavior of the current mode control will be like a voltage mode control. With excessive slope compensation, most of the current information is lost and the controller acts like a voltage mode controller.

The advantages which this control technique offers include the following [84]:

- (1) Since inductor current rises with a slope determined by V_{in} and V_o , this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
- (2) Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the error amplifier, and the ease of providing load sharing when multiple power units are paralleled.

While the improvements offered by peak current mode control are impressive, this technology also comes with its own unique set of problems which must be solved in the design process. A list of some of these is outlined below [85]:

- (1) Slope compensation required. The control loop becomes unstable at duty cycles above 0.5 unless slope compensation is added.
- (2) Poor noise immunity. Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop. A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
- (3) Peak to average current error. The peak to average current error inherent in the peak current mode control is usually not serious problem in conventional buck converters. However, in high power factor boost pre-regulators the peak to average error is very serious because it causes distortion of the input current waveform.

Boost converter with peak current mode control is shown in Fig. 2-8.

Figure 2-8 Peak current mode control of boost converter

C. Average current mode control

In the average current mode control, the inductor current is sensed and fed into a compensation network to obtain its DC information. The output of the compensator is compared with a saw-tooth waveform to generate PWM control. A buck example is shown in Fig. 2-9.

Average current mode control has the following advantages compared to the peak current mode control [85]:

- (1) Average current tracks the current program with a high degree of accuracy.
- (2) Slope compensation is not required, but there is a limit to loop gain at the switching frequency in order to achieve stability.
- (3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from the corresponding current error level at the input of the PWM comparator.

Figure 2-9 Average current mode control of buck converter

The traditional linear control solutions are based on the linearized small-signal models. They are still widely used in industrial applications. However, such models are only valid in a small region around any specified operating point. The valid region of the small-signal perturbation in the state space is unknown. When the perturbations are large, the anti-disturbance capability of traditional linear controllers often deteriorates. Also it is known that the maximum range of the duty cycle is 0 to 1, which is the control input limitation of DC-DC converters. The frequency domain design methods do not always consider such limitations. As a result, the actual system performance is not the same as and most likely worse than the predicted characteristics in the frequency domain.

2.3.2 Nonlinear Control Methods

Since linear controller cannot give satisfactory performance, nonlinear control theory applied on DC-DC converters has gained much attention. In order to apply the linear control techniques on DC-DC converters in large-signal mode, the feedback linearization has been studied in many publications. The main idea of this approach is to algebraically transform a nonlinear system dynamics into a fully or partly linear one so that the linear control techniques can be applied [86-87]. There are inherited disadvantages of such method: the full state variables must be measured. No robustness can be guaranteed in the presence of parameter uncertainty or un-modeled dynamics.

Many references have focused on the application of the state transformation on the control of DC-DC converters. Sira-remirez [88] has developed a so-called pseudo-linearization method which can determine the nonlinear transformations of the state

variables and control inputs. Then the tangent model (small-signal linearization) of the transformed system is in phase with the canonical form. The advantage of this approach is that it can stabilize an entire class of equilibrium. However, the global stability and the large-signal behavior of control system cannot be ensured using this method.

Nonlinear state transformation [89-90] is applied to the state-averaged model in large-signal form. The new state variables are the energy function of the original system and its derivatives. The controller can be obtained by steadily decreasing the energy function to its least value corresponding to the equilibrium point. Lyapunov theory is applied in the derivation of such controllers. Exact dynamical feedback linearization is used to get the nonlinear feedback controller [91-92]. For stability problems, it is by regulation of other state variables such as input current to gain output regulations [93-94]. Since the output voltage with such a strategy is only controlled indirectly, additional effort is required to treat with the load variations. Generally, most methods using nonlinear or linear transformation can get linear relation between the newly defined control input and output. The problems of these methods are that it requires the exact information of the circuit components and large quantity of calculations is also needed. They are not suitable for practical use considering cost, performance, and robustness.

A. Input voltage feed-forward control

A simple nonlinear feedback controller [95] is given below

$$u = \frac{1}{V_{in}} w \quad (2-10)$$

Where w is the control input. The resulted system is a large-signal linear one and independent to input voltage variations. The pole-placement method is used to derive the feedback compensator. To decrease the output impedance, it is also suggested that the output capacitor current is used as the state variable. It is in fact a kind of input voltage feed-forward control. This controller needs to be combined with other possible feedback to gain good output regulation as well.

Input voltage feed-forward in open-loop control is examined. It is shown that input voltage feed-forward significantly decreases the influence of input voltage variations. The

input audio-susceptibility is also reduced. However, the output characteristics are not changed [96-97].

One-cycle control [98-99] is a nonlinear approach to avoid the input voltage variations. It is shown below, that one-cycle control is actually similar to the input voltage feed-forward control. An example of one-cycle controlled buck converter is shown in Fig. 2-10.

Figure 2-10 One-cycle controlled buck converter

In one-cycle control, the switch is turned off when the integration of the diode voltage reaches the reference value.

$$\frac{1}{T} \int_0^{T_{on}} v_D dt = V_{ref} \quad (2-11)$$

Where T is the switching period and T_{on} is the switching-on period. The diode voltage is equal to input voltage V_{in} when switch is turned on. If the input voltage is constant, then (2-11) becomes

$$V_{in} \frac{T_{on}}{T} = V_{ref} \quad (1-12)$$

This is the open-loop characteristic of a buck converter. The one-cycle control actually uses the diode voltage observer instead of the input voltage feed-forward. It can adjust the duty cycle in one switching period in case of the input voltage variations. However, like other input voltage feed-forward controllers, it cannot enhance the converter output performance. If a step change occurs in the input voltage, the duty cycle quickly changes

to a new value. The output performance is the same as the open-loop response, which is not satisfactory in most cases. In addition, the one-cycle control is not globally stable for more complex converters. Then necessary modification is made to limit of the duty cycle and ensure the stability of Ćuk converter [100]. The possibility of applying the one-cycle control on other types of DC-DC converters [101] is examined. To enhance the output characteristic of one-cycle control, a direct reference voltage with a PI controller is used [102-103], whose input is the error between the output voltage and the reference voltage. The resulted closed-loop systems can achieve better response than the original one-cycle control in case of load variations.

B. Fuzzy logic control

As the performance of traditional linear control based on the small-signal model is influenced by the variation of operating point, nonlinear PI controller can be designed to incorporate such changes. A nonlinear PI controller is designed based on the extended linearization theory. This, in structure, is similar to a nonlinear PI controller based on fuzzy logic theory [104].

Fuzzy logic control [105] has also been widely used to design such nonlinear controllers. The error and differential of the error of the output voltage is fuzzified [106] and the Sugeno fuzzy system gives out the change in duty cycle. A practical implementation of a Mamdani type fuzzy controller [107] is developed with micro-processor. For these methods, the changes of duty cycle are directly determined by the de-fuzzifying the output of the controller [108]. The advantages of such fuzzy controller over the traditional PI controller in control of the boost converter are summarized in [109].

Another type of fuzzy PI controller for Ćuk converter is developed [110]. The input of the fuzzy controller is the error and change rate of the output voltage error. The coefficients of the proportional and integral gains are the result of the fuzzy controller. Alternatively, it has been developed using the error of both the output voltage and the input inductor current as the fuzzy base [111].

It is shown that the fuzzier and de-fuzzier are generally needed to implement a fuzzy controller. Micro-processors or other digital storage devices are therefore needed to

implement such complex computation. The analog implementation of a fuzzy logic controller for the boost converter has been reported in [112].

C. Sliding Mode control

The SM control theory was firstly developed in 1970's [113-114] for variable structure systems and it is also a kind of Variable Structure Control (VSC). The most distinguished feature of VSC is that it can achieve robust control system. Currently, VSC is also applied in a wide range [115-120]. DC-DC converters are also one kind of variable structure systems due to their switch properties. SM control has been widely applied to such systems since 1980's [121].

The basic idea of SM control can be explained using buck converter as an example. The phase portraits of buck converter during switching-on and switching-off are shown in Fig. 2-11. The solid lines are the phase portrait of buck converter during switching-on, and the dotted lines are the phase portrait during switching-off. The axes are the error item of the capacitor voltage and the inductor current corresponding to their operating points. A sliding surface is often defined as

$$S(X,t) = 0 \quad (2-13)$$

The sliding surface divides the whole state plane into two separated parts, which are corresponding to the two switch positions: ON and OFF. The system operating state can often be represented as a point in the state space, which is called Representing Point (RP) in this thesis. The state trajectory of buck converter is then decided according to the system RP's position in the state plane. The sliding surface can be selected to achieve different control objectives. There are normally three phases of system motion under SM control: reach phase, sliding mode and steady state. Fig. 2-12 shows the start-up performance of buck converter using the SM control.

If the switching frequency is infinite, the system can be kept on the sliding surface. However it cannot be achieved in reality and a hysteresis is used in practice to limit the switching frequency. The system RP will slide across the sliding surface repeatedly, which is called the system in sliding mode.

Figure 2-11 Buck converter phase portraits under SM control

Figure 2-12 Buck converter's start-up performance under SM control

The analysis of SM control includes examination of three conditions: the reaching condition, existence condition and stability condition in sliding mode [122]. The first two conditions can be examined using derivative of system equations. When in sliding mode, the system performance is guaranteed by the sliding surface. Five methods have been developed to analyze the system performance under sliding mode [115]. All of them describe how to derive differential equation of system under sliding mode.

It has been proven that the SM control has several advantages:

- (1) By forcing the system to stay on the sliding surface, a better dynamic response can be achieved.

- (2) The system is less sensitive to parameter variations. It can ensure stability even under large parameter changes.
- (3) By choosing a second-order sliding surface, SM control can achieve first-order response. This second order sliding surface can be readily applied to higher-order systems, which greatly simplifies the implementation of the controllers.

A lot of papers have been published on applying the SM control to DC-DC converters. The stabilization of the lossless switched power electronic circuits is examined, whose state variables evolve on a generalized sphere [123]. The theoretical background is constructed in this thesis for the use of SM control to govern the system's transition from one state configuration to another in the state plane. The geometric approach [124] is used to analyze the stabilization of such system.

The error of inductor current and output voltage on their operating point [121] has been used to define the sliding surface. The exact linearization technique and the extended linearization in state transformation are used to obtain new state variables [87, 125], a nonlinear state transformation method is addressed in [89]. All these methods require additional computations. The design procedure is therefore complicated and the global stability of the controllers cannot be guaranteed because of state transformation.

Using the original state variables such as the inductor current and the output voltage has been given much attention. The sliding surface with only output voltage is applicable for buck converter. For other DC-DC converters, additional variables are needed. Various sliding surfaces are analyzed [126-127], which include one, two or three state variables for a simplified Ćuk converter under ideal condition. It is then suggested that more state variables can offer more flexibility and more complexity at the same time, to design controller. DC-DC converters can also be controlled by using only one state variable such as the input inductor current, which has been explained from the energy point of view [91, 122]. A SM controller has also been reported which only used the inductor current as the state variable. The stability of the controller is proven through the direct Lyapunov method.

The dynamic performance of a SM controller with inductor current feedback is satisfactory under ideal conditions. In case of parameter uncertainties, additional information is needed. Generally, the output voltage can be sensed to eliminate the steady state error, which is similar to using a PI compensator in the output voltage loop of the current mode control.

There are other versions of SM controllers which use two variables. Output voltage and its derivative, which is the output capacitor current, are used to implement the sliding surface in [121, 129]. High-pass filter is used to get the error signal of the input inductor current, while the error of output voltage is obtained by subtracting output voltage from the reference voltage [130-131]. Therefore, the reference current is not needed. The approach simplifies the design process and the controller is also insensitive to parameter variations. SM controller using the small-signal method is analyzed in [132]. Fig. 1-13 shows the configuration of the SM controller which uses one current sensor and one voltage sensor.

To obtain the switch signal according to the sliding function value, a sign function is introduced

$$s(x) = 0.5[1 + \text{sign}(x)] = \begin{cases} 0 & \text{when } x < 0 \\ 1 & \text{when } x > 0 \end{cases} \quad (2-14)$$

Figure 2-13 Buck converter controlled by SM controller with two state variables' feedback

Under such case, a clock signal is needed to stabilize and limit the switching frequency. There are five methods of implementing the switching function as [133]:

- (1) Hysteresis: A symmetrical or asymmetrical neighborhood of the sliding surface is established. When in the neighborhood, the switching function is kept unchanged. The switching function regulates its output according to the direction when the sliding function goes outside of the neighborhood. The width of the neighborhood determines the switching frequency.
- (2) Constant sampling frequency: The sliding function is captured at constant time instants, and the switch position changes can only be made at the sampled time instant.
- (3) Constant On-Time: Every time the switch is turned on, it will be kept for a constant time period. Then the switching function checks the sliding function and decides when to turn off the switch.
- (4) Constant switching frequency: The switch off action can only happen at time instant uT_{sw} in one switching period when the sliding function is less than zero. T_{sw} determines the desired switching frequency.
- (5) Limited maximum switching frequency: Either switch states will take place at least for a period T_M .

Only methods (1) and (2) can obtain nearly constant switching frequency at steady state. However, in case of parameter changes, the switching frequency will change as well. This is a disadvantage of SM control. Therefore many approaches have been reported in order to limit the switching frequency.

One method is to encode the ramp signal into the discontinuous switching function of the controller [131]. The advantage of this method is that it is straightforward and simple to implement. However, this comes at an expense of additional hardware circuitries, as well as deteriorated transient response caused by the superposition of the ramp function upon the switching function.

Adaptive hysteresis band control [134] has been developed, which can adjust the hysteresis band according to different parameter variations. However, such a band is

sensitive to the inductance and input voltage. In case of a too large or too small band, the control performance will deteriorate and it is also not easy for implementation in practice.

A SM-like controller [110] is designed for buck converter. The error of output voltage and its derivative are used as the input of a fuzzy based controller. The output of the fuzzy controller is incremental value of the duty cycle. By implementing hard-band saturation on the incremental value, the duty cycle is limited between 0 and 1. Therefore, a constant switching frequency can be achieved. However, the controller often needs excessive duty cycle in order to achieve the desired performance. Because the duty cycle is strictly limited, the actual control performance is always worse than predicted.

The concept of equivalent SM control [134-136] is developed. Only output voltage feedback is used in these controllers. Unfortunately, only control output in discrete manner was presented. The switching frequency will also change during transients.

An equivalent control scheme for buck converter is shown in Fig. 2-14. The advantage of this method is that there is no need of additional hardware circuitries since the switching function is replaced by the PWM modulator and the transient response is not deteriorated. The drawback is that the computations to obtain the equivalent control input are very complicated. This method will be analyzed in details in this thesis to show that the above drawbacks can be overcome by choosing adequate sliding surface.

Figure 2-14 Equivalent control version of SM controlled buck converter

Another type of equivalent control methods is presented in [137]. The sliding surface only includes the output voltage and the converging rate is defined as the control objective shown in (2-15), where λ is the coefficient, which controls the converging rate of the output voltage.

$$\begin{aligned} S &= v_o - v_{ref} \\ \dot{S} &= -\lambda(v_o - v_{ref}) \end{aligned} \tag{2-15}$$

The advantage of this method is that the equivalent control is only represented by the output voltage and reference output. During derivation of the equivalent control, other state variables are considered as constant. The disadvantage is that the output voltage response is also limited by the circuit parameters. It cannot change as rapidly as that defined by the converging coefficient. Therefore, overshoot and long period oscillation exist in the output voltage response.

The method described above is actually a kind of typical synergetic control [138-140]. In synergetic control theory, the first step is to define a macro-variable as a function of the state variables.

$$\psi = \psi(x) \tag{2-16}$$

Then, it tries to get the control output by forcing the trajectory of the pre-defined function to follow (2-17), where A is the design parameter specifying the convergence speed to the manifold specified by $\psi = 0$.

$$A\dot{\psi} + \psi = 0 \tag{2-17}$$

The control input can be solved using the state-space equation. The synergetic control can satisfy various requirements by defining a macro-variable, such as adding an integral part. However, it needs much more computations than the traditional SM control. The performance is also not satisfactory due to the limitation of the circuit response speed and saturation problems.

All the sliding functions described above are of first order. A second order sliding function has been developed [141], which can enhance the tangential velocity of the trajectories along the switching surface. The converter therefore exhibits better transient behaviors. However, computation task increases a lot. The SM control technique has also been used for tracking AC reference voltages. The details can be found in [142-144].

D. Adaptive control and other control methods

The normal two-variable SM control is similar to the current mode control with PI compensator in the output voltage loop. The coefficients of PI compensator thus can be modified through a fuzzy based control [145]. This technique can be viewed as varying the sliding surface under different regions of the state space, which is similar to the idea of adaptive control. Fuzzy control can also be treated as SM control with nonlinear adaptive sliding coefficients [146].

Adaptive control is a useful approach to control systems which have unknown or slowly varying uncertain parameters [147]. The basic idea is to estimate the uncertain plant parameters (or, equivalently, the corresponding controller parameters) on-line based on the measured system signals. The estimated parameters are then used in the control input computation. Systems with varying control parameters can be viewed as adaptive controller. Since the loads of DC-DC power supplies are various, adaptive control can be used to estimate the unknown load impedance [111]. The global stability of such control scheme is also analyzed in this reference. The main advantage of this approach is that it can eliminate the steady state error of the output voltage. Control parameters are adjusted to achieve satisfied dynamic performance under the input voltage variations [148]. For the different input voltage, different pole-placement control coefficients are calculated and used to obtain the same dynamic response.

Adaptive control for both the input voltage and load variations [149] is examined. A state plane with x axis as the load resistance and y axis as the input voltage is built. Grid-point theory has been used to divide the state plane into different pieces around the operating point. Then, according to the locations, different control parameters can be designed. PI controller has been chosen as an example in the paper to verify the effectiveness of the control scheme. An adaptive version of fuzzy logic controller [150] is

introduced to achieve the same dynamic performance under various operating points by using a scaling factor as a function of the duty cycle.

Extended linearization and PI control scheme [151] have been used where the output voltage should be adjustable while the load is unknown. An adaptive version of SM control [70] is designed to achieve better dynamic performance under load variations. Through the load estimation and output voltage feedback, gain scheduling scheme [152-153] has been used to determine the slope of the sliding line. It has been shown that the steady state error can be significantly reduced. However, the output voltage needs longer time to reach the desired level in case of step-up change of the load resistance.

A controller design method based on the H^∞ control theory [154-157] is introduced to show that the output impedance of the converter can be set as the direct design goal of the controller. The designed controller is the same order as that of the converter, the advantages of such approach, for example, the output impedance and the audio-susceptibility is analyzed.

The digital control scheme of DC-DC converters can be implemented, most of which are using SM control [158-163]. Since there are parameter uncertainties and immeasurable parasitic effects in DC-DC converters, robust stability analysis has also been examined.

2.4 Conclusion

In this chapter, topology development of DC-DC converters is examined from second-order converters to four-converters. The traditional methods to get high voltage transfer gain are examined and their disadvantages are explained, thus some new techniques to get high voltage transfer gains are desired.

Different modeling methods are then introduced, which have different advantages and disadvantages. If a nonlinear controller like SM controller is to be designed, the state-space modeling is the best choice, for the main characteristics of the converters can be expressed in the form of large-signal equations. But for advanced DC-DC converters

which usually have high-order complexity, it is necessary to reduce the order at the same time the main characteristics are remained and the controller are easier to design based on the reduced-order state space modeling, which will be introduced in the next chapter.

Several control methods are described for DC-DC converters. The linear control methods, although widely used, shall be replaced by advanced control scheme gradually because linear control methods cannot cater with the increasing requirements driven by more and more applications of digital circuits. Nonlinear transformation methods are not applicable as the robustness cannot be guaranteed. The design of Fuzzy logic control scheme is complex and requires a lot of experience. The implementation of a fuzzy logic controller is also of higher cost. Other control methods such as input voltage feed-forward control, one-cycle control and adaptive control can actually be combined with other control schemes to improve the overall system performance.

Among nonlinear control methods, SM control will be a possible direction for the near future as they can offer better performance and simple implementation. The problems of traditional SM control mainly include large surges in transient response and non-zero steady state error which will be solved in the next chapter.

Chapter 3 Modeling and Control of Advanced DC-DC Converters

Modeling and controlling are very important issues for DC-DC converters. There are various modeling and control methods (see Chapter 2). The research work of this thesis describes mainly advanced DC-DC converters, but it is important to find a generalized modeling method and controlling method for advanced DC-DC converters first. In this Chapter, a reduced-order state-space modeling of advanced DC-DC converters is presented. An improved Sliding Model (SM) controller is implemented, which can be generally applied to all advanced DC-DC converters. As a case study, positive output super-lift converter is analyzed to show the reduced-order modeling first, an improved SM controller is designed then, whose performance is satisfactory.

3.1 Introduction

Positive output super-lift converters are a series of attractive DC-DC topologies. The elementary circuit is shown in Fig. 3-1, which is illustrated in detail in [35].

Figure 3-1 Elementary Positive Output the super-lift converter [35]

A series of positive output super-lift converters can be formed by implementing both the n -cell cascade connection and the transformerless single-switch operation to provide very high step-up voltage transfer gains. Each functional cell of the super-lift converters utilizes the Voltage-Lift (VL) technique, which is an effective method widely applied in electronic circuit design [35], especially in the radio engineering, to realize the performance and characteristic improvement. As a new circuit solution, the research on their mathematical modeling and control strategies is important to promote the practical applications of the super-lift converters.

The major modeling methods are reviewed in Chapter 2. In this section, reduced-order state-space modeling method is applied to the super-lift converters, which is suitable for various controller design schemes.

For controlling issues, Sliding Mode (SM) control [113-138] is one of the best choices since DC-DC converters are typical variable structure systems. It is a kind of nonlinear control and can get much better regulation performance especially in some situations when the input signal (input voltage or output load) has a large variation range. Therefore, a general control scheme using the improved SM controller will be designed for super-lift converters.

Re-lift circuit is used in the case study on the modeling and controller performances. Theoretical analysis is verified by satisfactory experimental results. This reduced-order state-space modeling method and the improved SM control method can be applied to advanced DC-DC converter topologies satisfactorily.

3.2 Modeling Analysis of Positive Output Super-Lift Converters

Positive output super-lift converters are a series of DC-DC converters that can get very large step-up voltage transfer gains. According to the number of the functional cell, they can be classified to the elementary circuit (one VL cell), re-lift circuit (two VL cells), triple-lift circuit (three VL cells), etc. The generalized topology (n -cell cascade connection) is shown in Fig. 3-2(a) for reference. It is derived from the elementary circuit

by adding $(n-1)$ VL cells, which are defined by $(L_2-D_2-D_3-D_4-C_2-C_3)$, ..., $(L_n-D_{3n-4}-D_{3n-3}-D_{3n-2}-C_{2n-2}-C_{2n-1})$. By controlling the switch S on and off, the step-up DC output voltage can be obtained.

(a) Topology

(b) Equivalent circuit during switching-on

(c) Equivalent circuit during switching-off

Figure 3-2 Generalized circuit of the super-lift converters with n-cell cascaded structure

During switching-on time, diodes $D_1, D_3, D_4, \dots, D_{3n-3}, D_{3n-2}$ conduct. Capacitor C_1 is charged to v_{in} in a short time and we assume this capacitor voltage is always equal to v_{in} . The voltage across inductor L_1 is v_{in} and the current i_{L1} flowing through inductor L_1 increases. In the second VL part, the capacitor C_2 acts as a DC source providing energy to the inductor L_2 , the current of which is increasing, and the capacitor C_3 , which is quickly

charged to v_{C2} and is assumed always equal to v_{C2} . Similarly in the n^{th} VL cell, the capacitor C_{2n-2} acts as a DC source providing energy to the inductor L_n , whose current is increasing, and the capacitor C_{2n-1} , which is quickly charged to voltage v_{C2n-2} and is assumed equal to v_{C2n-2} all the time. The output capacitor C_o provides energy to output load. The equivalent circuit is shown in Fig. 3-2(b). This process can be expressed by (3-1).

$$\left\{ \begin{array}{l} L_1 \frac{di_{L1}}{dt} = v_{in} \\ L_2 \frac{di_{L2}}{dt} = v_{C2} \\ \vdots \\ L_n \frac{di_{Ln}}{dt} = v_{C2n-2} \\ C_2 \frac{dv_{C2}}{dt} = -i_{L2} - C_3 \frac{dv_{C3}}{dt} \\ \vdots \\ C_{2n-2} \frac{dv_{C2n-2}}{dt} = -i_{Ln} - C_{2n-1} \frac{dv_{C2n-1}}{dt} \\ C_o \frac{dv_{Co}}{dt} = -\frac{v_o}{R} \end{array} \right. \quad (3-1)$$

During switching-off time, diodes $D_2, \dots, D_{3n-4}$ and D_o conduct. The inductor current i_{L1} is discharged in series with capacitor C_1 to provide energy to capacitor C_2 . The second VL branch where inductor L_2 and capacitor C_3 are series connected is providing energy to the capacitor C_4 . Similarly for the n^{th} VL cell, inductor L_n and capacitor C_{2n-1} are series connected to provide energy to the output capacitor and load. The equivalent circuit is shown in Fig. 3-2(c). This process can be expressed by (3-2).

$$\left\{ \begin{array}{l} L_1 \frac{di_{L1}}{dt} = 2v_{in} - v_{C2} \\ L_2 \frac{di_{L2}}{dt} = 2v_{C2} - v_{C4} \\ \vdots \\ L_n \frac{di_{Ln}}{dt} = 2v_{C2n-2} - v_o \\ C_2 \frac{dv_{C2}}{dt} = i_{L1} - i_{L2} \\ \vdots \\ C_{2n-2} \frac{dv_{C2n-2}}{dt} = i_{Ln-1} - i_{Ln} \\ C_o \frac{dv_o}{dt} = i_{Ln} - \frac{v_o}{R} \end{array} \right. \quad (3-2)$$

Using capacitor charge balance rule for $C_3, C_5, \dots, C_{2n-1}$, we can get the below equations for the whole switching period, where u ($0 < u < 1$) is the duty cycle.

$$\left\{ \begin{array}{l} uC_3 \frac{dv_{C3}}{dt} - (1-u)i_{L2} = 0 \\ uC_5 \frac{dv_{C5}}{dt} - (1-u)i_{L3} = 0 \\ \vdots \\ uC_{2n-1} \frac{dv_{C2n-1}}{dt} - (1-u)i_{Ln} = 0 \end{array} \right. \quad (3-3)$$

As there are $2n$ capacitors which are $v_{C1} = v_{in}, v_{C3} = v_{C2}, v_{C5} = v_{C4}, \dots, v_{C2n-1} = v_{C2n-2}$, it is only necessary to choose the second variable of each pair as state variable except v_{in} , besides v_o . Together with n inductor currents, all the state variables are chosen as $x = [i_{L1} \ i_{L2} \ \dots \ i_{Ln} \ v_{C2} \ \dots \ v_{C2n-2} \ v_o]$. Thus we can combine the above three sets of equations and get the state space equation below.

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \vdots \\ \dot{i}_{Ln} \\ \dot{v}_{C2} \\ \vdots \\ \dot{v}_{C2n-2} \\ \dot{v}_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & \dots & 0 & -\frac{1-u}{L_1} & \dots & 0 & 0 \\ 0 & 0 & \dots & 0 & \frac{2-u}{L_2} & -\frac{1-u}{L_2} & \dots & 0 \\ \vdots & \vdots & \ddots & 0 & 0 & \vdots & \ddots & 0 \\ 0 & 0 & \dots & 0 & 0 & \dots & \frac{2-u}{L_n} & -\frac{1-u}{L_n} \\ \frac{1-u}{C_2} & -\frac{2-u}{C_2} & \dots & 0 & 0 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & 0 & 0 & \ddots & 0 & 0 \\ 0 & \dots & \frac{1-u}{C_{2n-2}} & -\frac{2-u}{C_{2n-2}} & 0 & \dots & 0 & 0 \\ 0 & 0 & \dots & \frac{1-u}{C_o} & 0 & \dots & 0 & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{Ln} \\ v_{C2} \\ \vdots \\ v_{C2n-2} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{2-u}{L_1} \\ 0 \\ \vdots \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} v_{in} \quad (3-4)$$

In the steady state, the equivalent switching duty cycle is defined as u_{eq} ($0 < u_{eq} < 1$), and we can get the steady state values of all the state variables below.

$$X = \left[\frac{(2-u_{eq})^{2n-1}}{(1-u_{eq})^{2n}} \frac{v_{in}}{R}, \dots, \frac{(2-u_{eq})^{n+1}}{(1-u_{eq})^{n+2}} \frac{v_{in}}{R}, \frac{(2-u_{eq})^n}{(1-u_{eq})^{n+1}} \frac{v_{in}}{R}, \left(\frac{2-u_{eq}}{1-u_{eq}} \right) v_{in}, \left(\frac{2-u_{eq}}{1-u_{eq}} \right)^2 v_{in}, \dots, \left(\frac{2-u_{eq}}{1-u_{eq}} \right)^{n-1} v_{in}, \left(\frac{2-u_{eq}}{1-u_{eq}} \right)^n v_{in} \right] \quad (3-5)$$

3.3 Generalized Improved Sliding Mode Controller

Sliding mode (SM) control is one kind of nonlinear control method based on large-signal model and it is different from the traditional PI control which is based on small-signal linear model. When there are large variations in input voltage and output load, SM controller can still regulate very well and very quickly. Moreover, being a controller that has a high degree of flexibility in its design choices, the SM controller is relatively easy to implement as compared to other types of nonlinear controllers [164]. Such properties make it highly suitable for control applications in DC-DC converters, which are used in the situations where wide ranges of input voltage and output load exist.

As a kind of variable structure control schemes, the SM controller for DC-DC converters has been investigated recent years by some researchers [164-165]. The most important step for the controller design is to choose an appropriate sliding surface.

A sliding surface composed of the state variable errors and error integrals [164] is implemented and later a double integral term is added to suppress the steady state error. Another kind of sliding surface [165] is using state variables and the integral of the state variable errors. During start-up, this surface is crossing the origin and the system RP (the system operating state can be represented as a point in the state space, this point is named as system representing point) is just on the origin. Thus, a zero reaching time (the reaching time is the time for the system representing point to reach the sliding surface) is obtained and there will be smaller surges in the currents and voltages at hysterious mode.

A new sliding surface combined the advantages of the both above can then be introduced, which is composed of the state variables and the integral and double integral of the state variable errors, which is written as below, where a , b , m and λ are positive coefficients.

$$S = i_L + av_o + b \int (\lambda v_o - V_{ref}) dt + m \int \left(\int (\lambda v_o - V_{ref}) d\tau \right) dt = 0 \quad (3-6)$$

As the SM controller is flexible in design, all the state variables can be added to the sliding surface. On one hand this will improve the dynamic response; on the other hand it will increase the complexity of the controller. Thus a trade-off choice should be considered. For the elementary circuit of super-lift converters, two variables, i_{L1} and v_o , are used to compose the sliding surface. For the generalized n -cell circuit, there are n inductor currents and n capacitor voltages, we also only consider the inductor current of the first VL cell (i_{L1}) and the output voltage (v_o). These two state variables are enough to lead to good dynamic performance as well as good regulation ability. What's more, the controller is not too complicated to be implemented.

On the basis of (3-4) and (3-6), the derivative of S should satisfy the below condition for steady state operation.

$$\dot{S} = \frac{(2-u)v_{in} - (1-u)v_{C2}}{L_1} + a \frac{i_{Co}}{C_o} + b (\lambda v_o - V_{ref}) + m \int (\lambda v_o - V_{ref}) dt = 0 \quad (3-7)$$

The equivalent duty cycle u_{eq} can be obtained from (3-7) and is expressed as (3-8). It is noted that the state variables v_{C2} , v_o and i_{Co} appear in the u_{eq} equation, the feedbacks of

these variables will be needed in the controller. The corresponding logic structure of the improved SM controller is shown in Fig. 3-3.

$$u_{eq} = \frac{v_{C2} - 2v_{in} - \frac{aL_1}{C_o} i_{Co} + bL_1 (V_{ref} - \lambda v_o) + mL_1 \int (V_{ref} - \lambda v_o) dt}{v_{C2} - v_{in}} \quad (3-8)$$

Figure 3-3 The logic structure of the improved SM controller

In this thesis, this improved SM controller is implemented as fixed switching frequency considering the implementation and the performance of the DC-DC converters, the equivalent control input is obtained from the differentiation of the sliding surface, so the advantage of smaller surges in the currents and voltages is not obvious.

According to the basic theory of variable structure control, three conditions should be satisfied to ensure the stability of a SM controller. They are existence condition, reaching condition and stability condition under SM control.

3.3.1 Existence Condition

This condition ensures the system can slide in the vicinity of the sliding surface. In other words, system trajectories of the two substructures should be directed toward the sliding surface. Mathematically, the existence condition can be represented as below, where X is the state vector of the system.

$$\lim_{S \rightarrow 0^+} \dot{S}(X, t) < 0 < \lim_{S \rightarrow 0^-} \dot{S}(X, t) \quad (3-9)$$

When $S > 0, \dot{S} < 0, u = 0$,

$$\frac{2v_{in} - v_{C2}}{L_1} + a \frac{i_{Co}}{C_o} + b(\lambda v_o - V_{ref}) + m \int (\lambda v_o - V_{ref}) dt < 0 \quad (3-10)$$

When $S < 0, \dot{S} > 0, u = 1$,

$$\frac{v_{in}}{L_1} + a \frac{i_{Co}}{C_o} + b(\lambda v_o - V_{ref}) + m \int (\lambda v_o - V_{ref}) dt > 0 \quad (3-11)$$

Thus we get

$$\begin{cases} \frac{v_{in(\min)}}{L_1} + a \frac{i_{Co(\min)}}{C_o} + b(\lambda v_{o(\min)} - V_{ref}) + m \int (\lambda v_{o(\min)} - V_{ref}) dt > 0 \\ \frac{2v_{in(\max)} - v_{C2(\min)}}{L_1} + a \frac{i_{Co(\max)}}{C_o} + b(\lambda v_{o(\max)} - V_{ref}) + m \int (\lambda v_{o(\max)} - V_{ref}) dt < 0 \end{cases} \quad (3-12)$$

3.3.2 Reaching Condition

This condition ensures that the system representing point can eventually reach the sliding surface starting from any point in the state space. Mathematically, it can be represented as

$$\begin{cases} \lim_{t \rightarrow \infty} [\dot{S}(X, t)|_{u=1}] > 0 \\ \lim_{t \rightarrow \infty} [\dot{S}(X, t)|_{u=0}] < 0 \end{cases} \quad (3-13)$$

For the improved SM controller, the reaching condition has been satisfied by the appropriate choice of the sliding surface.

3.3.3 Stability Condition

The condition ensures the system is kept on the sliding surface. For the improved SM controller, the motion equation is nonlinear. We should do a stability analysis on its equilibrium point by knowing the dynamic equations (3-4). In steady state, the state variables should be satisfied by

$$\left\{ \begin{array}{l} L_1 \frac{di_{L1}}{dt} = (2 - u_{eq})v_{in} - (1 - u_{eq})v_{C2} \\ L_2 \frac{di_{L2}}{dt} = (2 - u_{eq})v_{C2} - (1 - u_{eq})v_{C4} \\ \vdots \\ L_n \frac{di_{Ln}}{dt} = (2 - u_{eq})v_{C2n-2} - (1 - u_{eq})v_o \\ C_2 \frac{dv_{C2}}{dt} = (1 - u_{eq})i_{L1} - (2 - u_{eq})i_{L2} \\ \vdots \\ C_{2n-2} \frac{dv_{C2n-2}}{dt} = (1 - u_{eq})i_{Ln-1} - (2 - u_{eq})i_{Ln} \\ C_o \frac{dv_o}{dt} = (1 - u_{eq})i_{Ln} - \frac{v_o}{R} \end{array} \right. \quad (3-14)$$

Next, we introduce perturbations around the operating point as shown in (3-14)

$$\left\{ \begin{array}{l} x = X + \tilde{x} \\ v_{in} = V_{in} + \tilde{v}_{in} \\ i_o = I_o + \tilde{i}_o \end{array} \right. \quad (3-15)$$

In (3-15), we have

$$x = \begin{bmatrix} I_{L1} + \tilde{i}_{L1} & I_{L2} + \tilde{i}_{L2} & \cdots & I_{Ln} + \tilde{i}_{Ln} & V_{C2} + \tilde{v}_{C2} & \cdots & V_{C2n-2} + \tilde{v}_{C2n-2} & V_o + \tilde{v}_o & \int (V_o + \tilde{v}_o) dt \end{bmatrix}^T$$

We can get the linearization of the sliding dynamics around the equilibrium point, which is as follows:

$$\frac{d}{dt} \tilde{x} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1(2n+1)} \\ a_{21} & a_{22} & \cdots & a_{2(2n+1)} \\ \vdots & \vdots & \ddots & \vdots \\ a_{(2n+1)1} & a_{(2n+1)2} & \cdots & a_{(2n+1)(2n+1)} \end{bmatrix} \tilde{x} + \begin{bmatrix} a_{1(2n+2)} \\ a_{2(2n+2)} \\ \vdots \\ a_{(2n+2)(2n+2)} \end{bmatrix} \tilde{v}_{in} + \begin{bmatrix} a_{1(2n+3)} \\ a_{2(2n+3)} \\ \vdots \\ a_{(2n+3)(2n+3)} \end{bmatrix} \tilde{i}_o \quad (3-16)$$

Therefore, the characteristic equation of the linearized system can be written as (3-17) below, where p_i ($i = 1, 2, \dots, 2n+1$) can be represented with a_{ij} ($i, j = 1, 2, \dots, 2n+1$).

$$\begin{vmatrix} s - a_{11} & -a_{12} & \cdots & -a_{1(2n+1)} \\ -a_{21} & s - a_{22} & \cdots & -a_{2(2n+1)} \\ \vdots & \vdots & \ddots & \vdots \\ -a_{(2n+1)1} & -a_{(2n+1)2} & \cdots & s - a_{(2n+1)(2n+1)} \end{vmatrix} = s^{2n+1} + p_1 s^{2n} + p_2 s^{2n-1} + \cdots + p_{2n} s + p_{2n+1} = 0 \quad (3-17)$$

The application of the Routh' stability criterion to the characteristic equation gives the condition under which the system will be stable, for detail see Appendix B.

By analyzing (3-12) and (3-17), we can get the ranges of the parameter values to satisfy the three conditions.

3.4 Case Study: Re-lift Circuit

In this case study, re-lift circuit is taken as an example to verify the foregoing general analysis and the improved SM controller, the detailed explanation is given in the following parts.

3.4.1 System Description

The state variables for re-lift circuit are chosen as $[i_{L1} \ i_{L2} \ v_{C2} \ v_o]$ and the corresponding state-space averaging equation is described by (3-18).

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = 2v_{in} - v_{C2} + (v_{C2} - v_{in})u_{eq} \\ L_2 \frac{di_{L2}}{dt} = 2v_{C2} - v_o + (v_o - v_{C2})u_{eq} \\ C_2 \frac{dv_{C2}}{dt} = i_{L1} - 2i_{L2} + (i_{L2} - i_{L1})u_{eq} \\ C_o \frac{dv_o}{dt} = i_{L3} - \frac{v_o}{R} - u_{eq}i_{L3} \end{cases} \quad (3-18)$$

The steady state variable vector of re-lift circuit can be obtained by the steady state analysis of (3-18) and is shown by (3-19). We can also get the same results from (3-5).

$$X = \left[\frac{(2-u_{eq})^3}{(1-u_{eq})^4} \frac{v_{in}}{R} \quad \frac{(2-u_{eq})^2}{(1-u_{eq})^3} \frac{v_{in}}{R} \quad \left(\frac{2-u_{eq}}{1-u_{eq}} \right) v_{in} \quad \left(\frac{2-u_{eq}}{1-u_{eq}} \right)^2 v_{in} \right] \quad (3-19)$$

Then, the improved SM controller is designed for the triple-lift circuit. The control signal is defined as v_c , and the peak magnitude of the saw-tooth ramp v_{ramp} is equal to V_{pm} . Then, u_{eq} can be expressed in the form below

$$u_{eq} = \frac{v_c}{V_{pm}} = \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{Co} + k(v_{C2} - 2v_{in})}{k(v_{C2} - v_{in})} \quad (3-20)$$

Substitute (3-20) into (3-19), we can get

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = 2v_{in} - v_{C2} + (v_{C2} - v_{in}) \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{Co} + k(v_{C2} - 2v_{in})}{k(v_{C2} - v_{in})} \\ L_2 \frac{di_{L2}}{dt} = 2v_{C2} - v_o + (v_o - v_{C2}) \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{Co} + k(v_{C2} - 2v_{in})}{k(v_{C2} - v_{in})} \\ C_2 \frac{dv_{C2}}{dt} = i_{L1} - 2i_{L2} + (i_{L2} - i_{L1}) \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{Co} + k(v_{C2} - 2v_{in})}{k(v_{C2} - v_{in})} \\ C_o \frac{dv_o}{dt} = i_{L2} - \frac{v_o}{R} - i_{L2} \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{Co} + k(v_{C2} - 2v_{in})}{k(v_{C2} - v_{in})} \end{cases} \quad (3-21)$$

In the above equation, k ($0 < k < 1$) is a factor that is introduced to scale down the equation to conform to the chip level voltage standard. The coefficients are expressed as $K_1 = bkL_1$, $K_2 = bkL_1$ and $K_3 = akL_1/C_o$.

The linearization of the sliding dynamics around the equilibrium point for re-lift circuit is shown in (3-22) where a_{ij} ($i, j = 1, 2 \dots 7$) can be derived from (3-21).

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{L2} \\ \tilde{v}_{C2} \\ \tilde{v}_o \\ \int \tilde{v}_o dt \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & a_{15} \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} \\ a_{41} & a_{42} & a_{43} & a_{44} & a_{45} \\ a_{51} & a_{52} & a_{53} & a_{54} & a_{55} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{L2} \\ \tilde{v}_{C2} \\ \tilde{v}_o \\ \int \tilde{v}_o dt \end{bmatrix} + \begin{bmatrix} a_{16} \\ a_{26} \\ a_{36} \\ a_{46} \\ a_{56} \end{bmatrix} \tilde{v}_{in} + \begin{bmatrix} a_{17} \\ a_{27} \\ a_{37} \\ a_{47} \\ a_{57} \end{bmatrix} \tilde{i}_o \quad (3-22)$$

The characteristic equation of the linearized system can be written as (3-23) below, where p_i ($i = 1, 2 \dots 5$) can be represented with a_{ij} ($i, j = 1, 2 \dots 5$).

$$\begin{vmatrix} s-a_{11} & -a_{12} & -a_{13} & -a_{14} & -a_{15} \\ -a_{21} & s-a_{22} & -a_{23} & -a_{24} & -a_{25} \\ -a_{31} & -a_{32} & s-a_{33} & -a_{34} & -a_{35} \\ -a_{41} & -a_{42} & -a_{43} & s-a_{44} & -a_{45} \\ -a_{51} & -a_{52} & -a_{53} & -a_{54} & -a_{55} \end{vmatrix} = s^5 + p_1s^4 + p_2s^3 + p_3s^2 + p_4s + p_5 = 0 \quad (3-23)$$

The application of the Routh's stability criterion to the characteristic equation gives the condition under which the system will be stable. This re-lift circuit system with the improved SM controller will be stable if the following conditions are satisfied.

$$\left\{ \begin{array}{l} p_i > 0 \quad i = 1, 2, 3, 4, 5 \\ \frac{p_1 p_2 - p_3}{p_1} > 0 \\ \frac{b_1 p_3 - p_1 b_2}{b_1} > 0 \\ \frac{c_1 b_2 - b_1 c_2}{c_1} > 0 \\ \frac{d_1 c_2 - c_1 d_2}{d_1} > 0 \end{array} \right. \quad (3-23)$$

Where $b_1 = \frac{p_1 p_2 - p_3}{p_1}$, $b_2 = \frac{p_1 p_4 - p_5}{p_1}$, $b_3 = 0$, $c_1 = \frac{b_1 p_3 - p_1 b_2}{b_1}$, $c_2 = \frac{b_1 p_5 - p_1 b_3}{b_1}$, $c_3 = 0$,

$$d_1 = \frac{c_1 b_2 - b_1 c_2}{c_1} \text{ and } d_2 = \frac{c_1 b_3 - b_1 c_3}{c_1}.$$

The value ranges for a , b and m , are decided by the existence condition (3-12) and stability condition (3-23). The optimal values we used in this experiment are obtained by try and error.

3.4.2 Reduced-Order State-Space Model Verification

The re-lift circuit descriptions are shown in Table 3-1 for reference to construct a laboratory circuit for system verification. First, we need to verify that the above reduced-order state-space model can be used to describe the real converter. The input voltage is set as 20 V and the output load resistor is 200 Ω , the duty cycle is set as 0.5 at the frequency of 50 kHz. The mathematical model for re-lift circuit is built in MATLAB/SIMULINK

based on the state-space equations in (3-18). The step response of the mathematical model is shown in Fig. 3-4(a). The steady state voltage value of the model is exactly 180 V which accords with the voltage transfer gain shown in (3-18). The step response of the triple-lift converter simulated in PSIM is shown in Fig. 3-4(b). The output voltage is about 180 V, which matches the mathematical model very well. The step response of the real re-lift converter is also tested, the output voltage is about 176 V shown in Fig. 3-4(c), which is a little smaller than the theoretical value due to the parasitic effects and the influence we neglected before. When the input voltage increases to 22 V at 0.3 s and returns to 20 V at 0.31 s, it can be seen clearly that the transient response due to the disturbance for the mathematical model and the simulated circuit are consistent with that of the real converter by comparing Fig. 3-4(a) and (b) with (c). Thus it is verified that the reduced-order state-space model is good enough to describe the converter's main characteristics.

Table 3-1 Specifications of the re-lift circuit

Capacitance of $C_1, C_2, C_3, C_4, C_5, C_o$	230 μ F
ESR of $C_1, C_2, C_3, C_4, C_5, C_o$	25 m Ω
Inductance of L_1, L_2, L_3	200 μ H
ESR of L_1, L_2, L_3	0.12 Ω
Load resistance R	50 Ω (minimum load resistance) 200 Ω (maximum load resistance)
Input voltage v_{in}	15 V ~ 30 V
Desired output voltage V_o	200 V

(a) The output voltage response of mathematical model

(b) The output voltage response of the triple-lift circuit simulated in PSIM

(c) The output voltage response of the real triple-lift circuit

Figure 3-4 The start-up response comparisons

3.4.3 Stability Performance

The parameters of the improved SM controller for the re-lift circuit are chosen as $K_1 = 5$, $K_2 = 100$, $K_3 = 0.3$, $k = 0.1$, $\lambda = 0.01$, $V_{ref} = 2$ V, $f = 50$ kHz. The practical closed-loop re-lift circuit system can be used in the scenario when the output voltage of the solar panel needs to step up and get connected to 200 V DC bus.

A configuration based on the analog components is used as shown in Fig. 3-5. The divider function is implemented with four-quadrant analog multiplier IC AD734. The numerator in equation (3-20) is realized by the fundamental analog PI and adder circuits. The photos of the improved SM controller are shown in Appendix C.

Figure 3-5 The configuration of re-lift circuit with the improved SM controller

Under the condition of load resistance $200\ \Omega$ and input voltage 30 V, the steady state waveforms are observed to verify the stability performance. The waveform of output

voltage ripple is shown in Fig. 3-6(a). It can be seen that the desired voltage is attained with variations less than 1 V, and the voltage variation ratio is close to zero ($< 0.1\%$). Additional, the waveform of the current ripple in inductor L_1 is shown in Fig. 3-6(b) and the ripple of i_{L1} is within the range of 1 A. It can be concluded that with the improved SM controller, the converter performs very stable with little variations and nearly no steady state errors.

(a) Output voltage ripple (AC coupling)

(b) Inductor L_1 current ripple (AC coupling)

Figure 3-6 The enlarged steady state waveforms

3.4.4 Regulation Performance with Output Load Variations

The improved SM controller is a little more complicated; however it has the feed-forward branches of v_{in} and v_{C2} from the high-order power converter, the controller can sense the disturbance faster and make the response quickly. This advantage has been

illustrated in reference [38], the following experiments will be focused on the advantage of the double-integral part which is new in the improved sliding surface.

(a) Inductor current of L_1 (DC coupling) and output voltage ripple (AC coupling) with the traditional SM controller when the load resistance change from 50 Ω to 200 Ω at 0.2s and from 200 Ω to 50 Ω at 0.4s

(d) Inductor current of L_1 (DC coupling) and output voltage (AC coupling) with the improved SM controller when the load resistance change from 50 Ω to 200 Ω at 0.11s and from 200 Ω to 50 Ω at 0.15s

Figure 3-7 The experimental curves when the output load varies

The regulation performances of this converter system under different load conditions are investigated with input voltage 30 V. Here the full load is defined as when the output current is 4 A with load resistance 50 Ω , and the extreme low load is defined as when output current is 1 A with load resistance 200 Ω . In order to verify the good regulation ability of the improved SM controller, traditional SM controller is built for comparison. The waveforms of i_{L1} and v_o with traditional SM controller are shown in Fig. 3-7(a). It can be seen that the voltage steady state error is about 4 V (2%) when the load is 50 Ω , and it is almost 3 V when the load is 200 Ω and the transient time is about 10 ms. The

waveforms of i_{L1} and v_o with the improved SM controller are shown in Fig. 3-7(b). The regulation performance is much better. The voltage steady state error is almost totally suppressed.

3.4.5 Regulation Performance with Input Voltage Variations

Analogously, the regulation performances of this converter system under input voltage changes are investigated with load resistance $200\ \Omega$. The nominal input voltage v_{in} is set as 30 V and the largest drop of the input voltage is set as 15 V . The performance of the improved SM controller is tested by comparison with that of the traditional controller.

(a) Inductor current of L_f (DC coupling) and output voltage ripple (AC coupling) when input voltage is changed from 30 V to 15 V at 0.2 s and from 15 V to 30 V at 0.4 s with traditional SM controller

(b) Inductor current of L_f (DC coupling) and output voltage ripple (AC coupling) when input voltage is changed from 30 V to 15 V at 0.11 s and from 15 V to 30 V at 0.15 s with the improved SM controller

Figure 3-8 The experimental curves when the input voltage varies

With the traditional SM controller, the corresponding waveforms of i_{LI} and v_o are shown in Fig. 3-8(a), respectively. The voltage variation is about 4 V (2%) and the transient time is about 10 ms when the input voltage is 15 V, the output voltage steady state error is about 3 V when the input voltage is 30 V. The waveforms of v_o and i_{LI} with the improved SM controller are shown in Fig. 3-8(b). The regulation performance is much better. The output voltage tracks the reference voltage very well and there is barely steady state error.

3.5 Conclusion

In this chapter, the reduced-order state space modeling and an improved SM controller is described. Re-lift circuit in the series of positive output super-lift converter is used for a case study. It is shown that the reduced-order state space modeling can describe the converter's main mathematical characteristics. The performance of the improved SM controller is compared with the traditional SM controller. It can be seen that with a double-integral part, the improved SM controller can suppress the steady state error in the output voltage largely. Moreover, the excellent consistency in the dynamical behavior of the output response with large output load and input voltage changes clearly demonstrates the superior characteristics of the improved SM controller under large-signal operations.

Chapter 4 Voltage-Lift Split-Inductor-Type Boost Converters

A series of Voltage-Lift (VL) Split-Inductor-type boost converters are described in this chapter. These circuits can get much higher voltage transfer gains due to the implementation of VL technique. They have symmetrical structures, which make them understood easily. What's more, they retain the advantages of the elementary Split-Inductor-type boost converter, which consumes less energy and has lower voltage stresses on active switches and diodes at the same circuit complexity level. Although there are four active switches in the multiple-lift circuits, they operate synchronously which makes the control algorithm much easier. An improved Sliding Mode controller is designed to evaluate the characteristics of the series of converters based on reduced-order state-space modeling. Theoretical analysis is supported by simulation and experimental results.

4.1 Introduction

A systematic, topological-based way of designing new converter structures was described for the first time in [48] to get higher voltage transfer gain by using the duality between a Switching-Capacitor (SC) cell and a Switching-Inductor (SI) cell as well as the duality between a voltage-driven converter and current-driven one.

A transformerless DC-DC high step-up converter is described in [166]. Compared with the converter in [48], this converter has the following merits [166]: (1) Two power devices exist in the current-flow path during the switch-on period, and one power device exists in the current-flow path during the switch-off period; (2) The voltage stresses on the active switches are less than the output voltage; (3) Under the same operating conditions, including input voltage, output voltage and output power, the current stress on

the active switch during the switch-on period is equal to the half of the current stress on the active switch of the converter in [48]. This transformerless DC-DC high step-up converter in [166] is named as elementary Split-Inductor-type boost converter here; it is different from the SI boost converter in [48], because the two inductors are split on either side of the load as shown in Fig. 4-1(a). The third converter in [166] is named as self-lift Split-Inductor-type boost converter as shown in Fig. 4-1(b).

(a) Elementary circuit

(b) Self-lift circuit

Figure 4-1 Topologies of the existing Split-Inductor-type boost converters

Voltage-Lift (VL) technique is an effective method that is widely applied in electronic circuit design [32-43], especially in the radio engineering. It can also lead to performance and characteristics improvement of DC-DC converters. However, it differs from current SC techniques. Both inductors and capacitors play an important role in the VL technique,

and all inner capacitors are fully charged by the power source. Moreover, fewer power switches (usually single switch or two synchronous switches) are included in VL structures and avoid complex multiple-switch control schemes.

In this chapter, VL technique is applied to the elementary Split-Inductor-type boost converter to develop a series of new converters in order to get much higher voltage transfer gain. This series of VL Split-Inductor-type boost converters are different from any other existing DC-DC step-up converters. Re-lift circuit, triple-lift circuit and n^{th} -lift circuits are developed based on the existing elementary circuit and self-lift circuit. All circuits perform positive to positive DC-DC voltage conversion with simple structures, small ripple, high efficiency and high voltage transfer gains.

Reduced-order modeling is reasonable and necessary as there are a lot of energy elements in the series of VL Split-Inductor-type boost converters. General reduced-order state-space model is given in this chapter. It provides enough information of the circuits and convenience for the controller design. For controlling issues, since DC-DC converters are typical variable structure systems, an improved Sliding Mode (SM) controller described in Chapter 3 will be designed for VL Split-Inductor-type boost converters in this chapter.

4.2 Development of Split-Inductor-Type Boost Converter

The circuit configuration of elementary Split-Inductor-type boost converter is shown in Fig. 4-1(a), which consists of two active switches (S_1 and S_2), two inductors (L_1 and L_2) which have the same inductance value, one output diode D and one output capacitor C_O . Switches S_1 and S_2 are controlled on and off synchronously by using one control signal. Self-lift Split-Inductor-type boost converter, which is developed from the elementary circuit, is shown in Fig. 4-1(b). Two VL cells are added in symmetrically, i.e., C_1 , D_1 and C_2 , D_2 , which consist of one capacitor and one diode respectively. The operating principles and steady state analysis of CCM and DCM are presented in detail in [166].

4.2.1 Re-lift Split-Inductor-Type Boost Converter

Fig. 4-2(a) shows the circuit configuration of re-lift Split-Inductor-type boost converter. It is developed from self-lift circuit by adding two VL cells, i.e., C_3, L_3, D_3, S_3 and C_4, L_4, D_4, S_4 , which consist of one capacitor, one inductor, one diode and one active switch respectively. Switches S_1, S_2, S_3, S_4 are controlled on and off synchronously by using one control signal.

(a) Topology

(b) Switching-on time

(c) Switching-off time

Figure 4-2 Topology and equivalent circuits of the re-lift Split-Inductor-type boost converter

Figure 4-3 Waveforms of the energy components of re-lift circuit in different operation modes

Fig. 4-2(b) and Fig. 4-2(c) show the circuits when the switches are on and off respectively during CCM. The general waveforms of the inductors and the capacitors are shown in Fig. 4-3(a). When the circuit works in DCM, the currents in the inductors become zero, the main diode is reversely biased and only the output capacitor C_O provides energy to the output load. The general waveforms of the inductors and the capacitors in this situation are shown in Fig. 4-3(b). The operating principles and steady state analysis of CCM and DCM are presented in detail below.

When the switches S_1, S_2, S_3, S_4 are turned on, inductors L_1, L_2, L_3, L_4 are charged in parallel by the DC source. At the same time, diodes D_1, D_2, D_3, D_4 conduct, capacitors C_1, C_2, C_3, C_4 are charged in parallel by the DC source as well. The energy stored in the output capacitor C_O is released to the load. Thus, the voltages across L_1, L_2, L_3, L_4 and C_1, C_2, C_3, C_4 are given as

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{in} \quad (4-1)$$

When the switches S_1, S_2, S_3, S_4 are turned off, DC source, L_1, L_2, L_3, L_4 and C_1, C_2, C_3, C_4 are series connected to transfer energy to C_O and the load. Thus, the voltages across L_1, L_2, L_3 and L_4 are derived as

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = \frac{V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4} - V_O}{4} = \frac{5V_{in} - V_O}{4} \quad (4-2)$$

By using the volt-second balance principle on L_1, L_2, L_3, L_4 , the following equation can be obtained, where T is switching period and u ($0 < u < 1$) is duty cycle.

$$uTV_{in} + (1-u)T \frac{5V_{in} - V_O}{4} = 0 \quad (4-3)$$

The voltage transfer gain in CCM is then derived as

$$M_{2CCM} = \frac{V_O}{V_{in}} = \frac{5-u}{1-u} \quad (4-4)$$

The voltage stresses on $S_1, S_2, S_3, S_4, D_1, D_2, D_3, D_4, D$ are derived as

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{V_O - V_{in}}{4} \quad (4-5)$$

$$V_D = V_O - V_{in} \quad (4-6)$$

When the circuit operates in DCM, the circuit performance is the same as that in CCM during switching-on period. The peak inductor currents of L_1 , L_2 , L_3 and L_4 can be written as

$$I_{L1p} = I_{L2p} = I_{L3p} = I_{L4p} = \frac{V_{in}}{L} uT \quad (4-7)$$

When the switches S_1 , S_2 , S_3 , S_4 are turned off, there is a time interval $u'T$, during which the circuit operation is also the same as that in CCM. DC source, L_1 , L_2 , L_3 , L_4 and C_1 , C_2 , C_3 , C_4 are series connected to transfer energy to C_O and the load. Inductor currents are decreased to zero after $(1 - u - u')T$ in one switching period. Another expression of the peak inductor currents are given as

$$I_{L1p} = I_{L2p} = I_{L3p} = I_{L4p} = \frac{V_O - V_{in} - V_{C1} - V_{C2} - V_{C3} - V_{C4}}{4L} u'T \quad (4-8)$$

From (4-7) and (4-8), u' is derived as

$$u' = \frac{4uV_{in}}{V_O - 5V_{in}} \quad (4-9)$$

However, after $(1 - u - u')T$ in one switching period, the inductor currents become zero and the switches are still off, then the main diode is reversely biased. At this time, only the output capacitor transfers energy to the load.

The average value of the output-capacitor current in steady state is zero during each switching period in DCM, which is given by

$$I_{co} = \frac{\frac{1}{2} u'T I_{L1p} - I_o T}{T} = 0 \quad (4-10)$$

Substituting (4-7) and (4-9) into (4-10), we can get

$$\frac{2u^2 V_{in}^2 T}{L(V_o - 5V_{in})} = \frac{V_o}{R} \quad (4-11)$$

Thus, the voltage transfer gain in DCM is given by

$$M_{2DCM} = \frac{V_o}{V_{in}} = \frac{5}{2} + \sqrt{\frac{25}{4} + 2u^2 Z_N} \quad (4-12)$$

If the re-lift Split-Inductor-type boost converter works in boundary conduction mode, the voltage transfer gain in CCM is equal to that in DCM. From (3-4) and (3-12), the boundary normalized load can be derived as

$$Z_{2NB} = \frac{2(5-u)}{u(1-u)^2} \quad (4-13)$$

4.2.2 Triple-Lift Split-Inductor-Type Boost Converter

Fig. 4-4(a) shows the circuit configuration of triple-lift Split-Inductor-type boost converter, which is developed from re-lift circuit by adding two VL cells, i.e., C_5, L_5, D_5, D_{01} and C_6, L_6, D_6, D_{02} , which consist of one capacitor, one inductor and two diodes respectively. Switches S_1, S_2, S_3, S_4 are controlled on and off synchronously by using one control signal. Fig. 4-4(b) and Fig. 4-4(c) show the circuits when the switches are on and off respectively in CCM. The general waveforms of the inductors and the capacitors are shown in Fig. 4-5(a). When the circuit works in DCM, the currents in the inductors become zero, the main diode is reversely biased and only the output capacitor C_o provides energy to the output load. The general waveforms of the inductors and the capacitors in this situation are shown in Fig. 4-5(b). The operating principles and steady state analysis of CCM and DCM are presented in detail below.

(a) CCM

(b) DCM

Figure 4-5 Waveforms of the energy components of triple-lift circuit

When the switches S_1, S_2, S_3, S_4 are turned on, inductors $L_1, L_2, L_3, L_4, L_5, L_6$ are charged in parallel by the DC source. At the same time, diodes $D_1, D_2, D_3, D_4, D_5, D_6, D_{O1}, D_{O2}$ conduct and capacitors $C_1, C_2, C_3, C_4, C_5, C_6$ are charged in parallel by the DC source as well. The energy stored in the output capacitor C_O is released to the load. Thus, the voltages across $L_1, L_2, L_3, L_4, L_5, L_6$ and $C_1, C_2, C_3, C_4, C_5, C_6$ are given as

$$v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_{L5} = v_{L6} = V_{C1} = V_{C2} = V_{C3} = V_{C4} = V_{C5} = V_{C6} = V_{in} \quad (4-14)$$

When the switches S_1, S_2, S_3, S_4 are turned off, DC source, $L_1, L_2, L_3, L_4, L_5, L_6$ and $C_1, C_2, C_3, C_4, C_5, C_6$ are series connected to transfer energy to C_O and the load. Thus, the voltages across $L_1, L_2, L_3, L_4, L_5, L_6$ are derived as

$$\begin{aligned} v_{L1} = v_{L2} = v_{L3} = v_{L4} = v_{L5} = v_{L6} \\ = \frac{V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4} + V_{C5} + V_{C6} - V_O}{6} = \frac{7V_{in} - V_O}{6} \end{aligned} \quad (4-15)$$

By using the volt-second balance principle on $L_1, L_2, L_3, L_4, L_5, L_6$, the following equation can be written out as

$$uTV_{in} + (1-u)T \frac{7V_{in} - V_O}{6} = 0 \quad (4-16)$$

The voltage transfer gain in CCM is obtained as

$$M_{3CCM} = \frac{V_O}{V_{in}} = \frac{7-u}{1-u} \quad (4-17)$$

The voltage stresses on $S_1, S_2, S_3, S_4, D_1, D_2, D_3, D_4, D_5, D_6, D_{O1}, D_{O2}$ and D are derived as

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{D6} = V_{D_{O1}} = V_{D_{O2}} = \frac{V_O - V_{in}}{6} \quad (4-18)$$

$$V_D = V_O - V_{in} \quad (4-19)$$

When the circuit operates in DCM, the circuit operation is the same as that in CCM during switching-on period. The peak inductor currents of L_1, L_2, L_3, L_4, L_5 and L_6 can be written as

$$I_{L1p} = I_{L2p} = I_{L3p} = I_{L4p} = I_{L5p} = I_{L6p} = \frac{V_{in}}{L} uT \quad (4-20)$$

When the switches S_1, S_2, S_3, S_4 are turned off, there is a time interval $u'T$, during which the circuit operation is also the same as that in CCM. DC source, $L_1, L_2, L_3, L_4, L_5, L_6$ and $C_1, C_2, C_3, C_4, C_5, C_6$ are series connected to transfer energy to C_O and the load. Inductor currents are decreased to zero after $(1 - u - u')T$ in one switching period. Another expression of the peak inductor currents are given as

$$\begin{aligned} I_{L1p} &= I_{L2p} = I_{L3p} = I_{L4p} = I_{L5p} = I_{L6p} \\ &= \frac{V_O - V_{in} - V_{C1} - V_{C2} - V_{C3} - V_{C4} - V_{C5} - V_{C6}}{6L} u'T \end{aligned} \quad (4-21)$$

From (4-20) and (4-21), u' is derived as

$$u' = \frac{6uV_{in}}{V_O - 7V_{in}} \quad (4-22)$$

However, after $(1 - u - u')T$ in one switching period, the inductor currents become zero and the switches are still off, then the main diode is reversely biased. At this time, only the output capacitor transfers energy to the load.

The average value of the output-capacitor current in steady state is zero during each switching period in DCM, which is given by

$$I_{CO} = \frac{\frac{1}{2} u'T I_{L1p} - I_O T}{T} = 0 \quad (4-23)$$

Substituting (4-20) and (4-22) into (4-23), we can get

$$\frac{3u^2 V_{in}^2 T}{L(V_O - 7V_{in})} = \frac{V_O}{R} \quad (4-24)$$

Thus, the voltage transfer gain in DCM is given by

$$M_{3DCM} = \frac{V_o}{V_{in}} = \frac{7}{2} + \sqrt{\frac{49}{4} + 3u^2 Z_N} \quad (4-25)$$

If the triple-lift Split-Inductor-type boost converter works in boundary conduction mode, the voltage transfer gain in CCM is equal to that in DCM. From (4-17) and (4-25), the boundary normalized load can be derived as

$$Z_{3NB} = \frac{2(7-u)}{u(1-u)^2} \quad (4-26)$$

4.2.3 N^{th} -Lift Circuit

Referring to the former analysis, it is possible to construct n^{th} -lift circuits by repeating adding VL cells (C_5 , L_5 , D_5 , D_{O1}). As they are developed based on the elementary Split-Inductor-type boost converter, in which two inductors exist on either side of the output load and VL cells are added on both sides, so there is always a symmetrical structure in every circuit. There are $2n$ VL cells in n^{th} -lift circuit and each n^{th} -lift circuit has $2n$ inductors, $(2n + 1)$ capacitors and $(4n - 3)$ diodes. Four synchronous switches S_1 , S_2 , S_3 and S_4 are required for each n^{th} -lift circuit when $n > 1$, which only need one simple control scheme and then decreases the complexity and cost significantly. The n^{th} -lift circuit is shown in Fig. 4-6(a).

When the switches are turned on, all the diodes in VL cells conduct, the main diode D is reversely biased. All the inductors and capacitors in VL cells are charged in parallel by DC source. The output capacitor is transferring energy to the load. When the switches are turned off, all the diodes in VL cells are reversely biased and the main diode D conducts. All the inductors and capacitors in VL cell are series connected with DC source and transfer energy to the output capacitor C_O and the load. When DCM happens, only the capacitor C_O provides energy to the load.

Voltage transfer gains of the series of VL Split-Inductor-type boost converters in CCM are illustrated in Fig. 4-6(b). The boundaries between the CCM and DCM for this series

of circuits are illustrated in Fig. 4-6(c). The main characteristics of the series circuits are summarized in Table 4-1, where n ($n = 1, 2, 3 \dots$) is denoted as n pairs of VL cells in n^{th} -lift circuit.

(a) Topology

(b) Voltage transfer gain comparison of this series of circuits in CCM

(c) Boundaries between CCM and DCM for this series of circuits

Figure 4-6 Topology and performances of VL Split-Inductor-type boost converters

Table 4-1 Main characteristics of the series of VL Split-Inductor-type boost converters

	M_{CCM}	M_{DCM}	Z_{NB}	V_D	V_S
Self-lift	$\frac{3-u}{1-u}$	$\frac{3}{2} + \sqrt{\frac{9}{4} + u^2 Z_N}$	$\frac{2(3-u)}{u(1-u)^2}$	$V_O - V_{in}$	$\frac{V_O - V_{in}}{2}$
Re-lift	$\frac{5-u}{1-u}$	$\frac{5}{2} + \sqrt{\frac{25}{4} + 2u^2 Z_N}$	$\frac{2(5-u)}{u(1-u)^2}$	$V_O - V_{in}$	$\frac{V_O - V_{in}}{4}$
Triple-lift	$\frac{7-u}{1-u}$	$\frac{7}{2} + \sqrt{\frac{49}{4} + 3u^2 Z_N}$	$\frac{2(7-u)}{u(1-u)^2}$	$V_O - V_{in}$	$\frac{V_O - V_{in}}{6}$
N^{th} -lift	$\frac{2n+1-u}{1-u}$	$\frac{2n+1}{2} + \sqrt{\frac{(2n+1)^2}{4} + nu^2 Z_N}$	$\frac{2(2n+1-u)}{u(1-u)^2}$	$V_O - V_{in}$	$\frac{V_O - V_{in}}{2n}$

4.3 Modeling and Controller Design

State-space modeling is popular for DC-DC converters, especially when closed-loop control is needed. Energy element states are usually chosen as state variables in state-space equations. For the n^{th} -lift circuit, reduced-order mathematical model is necessary. All the capacitors are same in the VL cells and the capacitor voltages are assumed unchanged, all of which are equal to the input voltage. As all the inductors are the same, only the first inductor current is chosen to be one state variable. The second state variable is the output voltage.

Based the foregoing theoretical analysis results, we write out the equations to describe the switching-on circuit, which are shown in (4-27).

$$\begin{cases} L \frac{di_L}{dt} = v_{in} \\ C_o \frac{dv_o}{dt} = -\frac{v_o}{R} \end{cases} \quad (4-27)$$

Similarly, the switching-off equations can be written out as in (4-28).

$$\begin{cases} L \frac{di_L}{dt} = \frac{v_o - (2n+1)v_{in}}{4} \\ C_o \frac{dv_o}{dt} = i_L - \frac{v_o}{R} \end{cases} \quad (4-28)$$

Equations (4-27) and (4-28) are combined and the general reduced-order state space model of VL Split-Inductor-type boost converters is shown below.

$$\begin{cases} L \frac{di_L}{dt} = \frac{(2n+1-u)v_{in} - (1-u)v_o}{4} \\ C_o \frac{dv_o}{dt} = (1-u)i_L - \frac{v_o}{R} = (1-u)i_L - i_o = i_{co} \end{cases} \quad (4-29)$$

We choose Sliding Mode (SM) control method for the controller design. SM control is a kind of variable structure control and very suitable for DC-DC converters, which have typical variable structures. DC-DC converters can stand wide input voltage changes and large output load variations with SM controller, compared to those with traditional PI controllers [167].

The sliding surface is chosen as below, where a , b , m and λ are positive coefficients.

$$S = i_{L1} + av_o + b \int (\lambda v_o - V_{ref}) dt + m \int \left(\int (\lambda v_o - V_{ref}) d\tau \right) dt = 0 \quad (4-30)$$

The original SM controller is similar to hysteresis control, the switching frequency is variable. However, constant switching frequency is popular in the actual practical adoption of SM controllers in power converters based on Pulse-Width-Modulation (PWM) technique. So we can get the equivalent control signal by differentiating the sliding surface function. Thanks to the double integral part in the sliding surface, an integral part is still here after differentiation to suppress the steady state error. The equivalent duty cycle is derived as

$$u_{eq} = \frac{v_o - (2n+1)v_{in} - \frac{4aL}{C_o}i_{CO} + bL(V_{ref} - \lambda v_o) + 4mL \int (V_{ref} - \lambda v_o) dt}{v_o - v_{in}} \quad (4-31)$$

According to the basic theories of SM control, three conditions should be satisfied to ensure the stability of a SM controller, which are existence condition, reaching condition and stability condition.

4.3.1 Existence Condition

This condition ensures the system can slide in the vicinity of the sliding surface. In other words, system trajectories of the two substructures should be directed toward the sliding surface. Mathematically, the existence condition can be represented as below, where X is the state vector of the system.

$$\lim_{S \rightarrow 0^+} \dot{S}(X, t) < 0 < \lim_{S \rightarrow 0^-} \dot{S}(X, t) \quad (4-32)$$

When $S > 0, \dot{S} < 0, u = 0$,

$$\frac{(2n+1)v_{in} - v_o}{4L} + \frac{ai_{CO}}{C_o} + b(\lambda v_o - V_{ref}) + m \int (\lambda v_o - V_{ref}) dt < 0 \quad (4-33)$$

When $S < 0, \dot{S} > 0, u = 1$,

$$\frac{2nv_{in}}{4L} + \frac{ai_{CO}}{C_o} + b(\lambda v_o - V_{ref}) + m \int (\lambda v_o - V_{ref}) dt > 0 \quad (4-34)$$

Thus we get

$$\begin{cases} \frac{2nv_{in(\min)}}{4L} + \frac{ai_{CO(\min)}}{C_o} + b(\lambda v_o - V_{ref})_{\min} + m \left(\int (\lambda v_o - V_{ref}) dt \right)_{\min} > 0 \\ \frac{(2n+1)v_{in(\max)} - v_{O(ss)}}{4L} + \frac{ai_{CO(\max)}}{C_o} + b(\lambda v_o - V_{ref})_{\max} + m \left(\int (\lambda v_o - V_{ref}) dt \right)_{\max} < 0 \end{cases} \quad (4-35)$$

4.3.2 Reaching Condition

This condition ensures that the system representing point can eventually reach the sliding surface starting from any point in the state space. Mathematically, it can be represented as

$$\begin{cases} \lim_{t \rightarrow \infty} [\dot{S}(X, t)|_{u=1}] > 0 \\ \lim_{t \rightarrow \infty} [\dot{S}(X, t)|_{u=0}] < 0 \end{cases} \quad (4-36)$$

For the improved SM controller, the reaching condition has been satisfied by the appropriate choice of the sliding surface.

4.3.3 Stability Condition

The condition ensures the system is kept on the sliding surface. For the improved SM controller, the motion equation is nonlinear. We should do a stability analysis on its equilibrium point by knowing the dynamic equations. In steady state, the state variables should be satisfied by

$$\begin{cases} C_o \frac{dv_o}{dt} = \frac{2nv_{in} + \frac{4aL}{C_o}i_{co} - bL(V_{ref} - \lambda v_o) - 4mL \int (V_{ref} - \lambda v_o) dt}{v_o - v_{in}} i_L - i_o \\ L \frac{di_L}{dt} = \frac{nv_{in}}{2} - \frac{2nv_{in} + \frac{4aL}{C_o}i_{co} - bL(V_{ref} - \lambda v_o) - 4mL \int (V_{ref} - \lambda v_o) dt}{4} \end{cases} \quad (4-37)$$

Next, we introduce perturbations around the operating point as shown in (4-37)

$$\begin{cases} x = X + \tilde{x} \\ v_{in} = V_{in} + \tilde{v}_{in} \\ i_o = I_o + \tilde{i}_o \end{cases} \quad (4-38)$$

In (4-38), we have

$$x = \begin{bmatrix} I_L + \tilde{i}_L & V_o + \tilde{v}_o & \int (V_o + \tilde{v}_o) dt \end{bmatrix}^T \quad (4-39)$$

The linearization of the sliding dynamics around the equilibrium point for triple-lift circuit is shown in (4-40) where a_{ij} ($i, j = 1, 2, \dots, 3$) can be derived from (4-37).

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_O \\ \int \tilde{v}_O dt \end{bmatrix} + \begin{bmatrix} a_{14} \\ a_{24} \\ a_{34} \end{bmatrix} \tilde{v}_{in} + \begin{bmatrix} a_{15} \\ a_{25} \\ a_{35} \end{bmatrix} \tilde{i}_O \quad (4-40)$$

Therefore, the characteristic equation of the linearized system can be written as (4-41) below, where p_i ($i = 1, 2, 3$) can be represented with a_{ij} ($i, j = 1, 2, 3$).

$$\begin{vmatrix} s - a_{11} & -a_{12} & -a_{13} \\ -a_{21} & s - a_{22} & -a_{23} \\ -a_{31} & -a_{32} & s - a_{33} \end{vmatrix} = s^3 + p_1 s^2 + p_2 s + p_3 = 0 \quad (4-41)$$

The application of the Routh's stability criterion to the characteristic equation gives the condition under which the system will be stable if the following conditions are satisfied.

$$\begin{cases} p_1 > 0 \\ p_2 > \frac{p_3}{p_1} \\ p_3 > \frac{p_1 p_4}{p_2 - \frac{p_3}{p_1}} \\ p_4 > 0 \end{cases} \quad (4-42)$$

The value ranges for a , b and m , are decided by the three SM conditions, which are the existence condition (4-35) and stability condition (4-42). The optimal values we used in this experiment are obtained by try and error.

4.4 Simulation and Experimental Results

Triple-lift circuit with the improved SM controller is investigated in laboratory, the circuit parameters are shown in Table 4-2 for reference.

Table 4-2 Specifications of the triple-lift Split-Inductor-type boost converter

Capacitance of $C_1, C_2, C_3, C_4, C_5, C_6$	230 μ F
ESR of $C_1, C_2, C_3, C_4, C_5, C_6$	10 m Ω
Capacitance of load capacitor C_O	470 μ F
ESR of C_O	15 m Ω
Inductance of $L_1, L_2, L_3, L_4, L_5, L_6$	200 μ H
ESR of $L_1, L_2, L_3, L_4, L_5, L_6$	0.12 Ω
Load resistance R	50 Ω ~ 200 Ω
Input voltage v_{in}	10 V ~ 30V
Desired output voltage V_O	400 V

The equivalent duty cycle u_{eq} can be expressed in the form below, where v_c is the control signal and V_{pm} is the peak magnitude of the saw-tooth ramp v_{ramp} .

$$u_{eq} = \frac{v_c}{V_{pm}} = \frac{K_1(V_{ref} - \lambda v_o) + K_2 \int (V_{ref} - \lambda v_o) dt - K_3 i_{CO} + k(v_o - 7v_{in})}{k(v_o - v_{in})} \quad (4-42)$$

In the above equation, k ($0 < k < 1$) is a factor introduced to scale down the equation to conform to the chip level voltage standard. The coefficients are expressed as $K_1 = bkL$, $K_2 = mkL$ and $K_3 = 4akL / C_O$. As for the parameters a , b and m , the value ranges are decided by the three SM conditions, the optimal values used in this experiment are obtained by evaluating the closed-loop performance described by the reference-to-output, control-to-output, output impedance and audio susceptibility transfer functions. The parameters in the controller are chosen as $K_1 = 10$, $K_2 = 10000$, $K_3 = 0.1$, $\lambda = 0.001$, $k = 0.001$, $V_{ref} = 4$ V. The switching frequency is chosen as $f = 50$ kHz.

The practical closed-loop re-lift circuit system can be used in the scenario when the output voltage of the solar panel needs to step up and get connected to 400 V DC bus. In

the hardware testing circuit, the N-channel MOSFET 2SK2267 is selected as the power switches. The drain-source on resistance is $8\text{m}\Omega$. All the diodes are realized by using MBR6045WT, the forward voltage drop is 0.6 V. Thus, the practical output voltage is smaller than the theoretical values due to the effects caused by parasitic parameters. A configuration of the triple-lift circuit is illustrated in Fig. 4-7.

Figure 4-7 Triple-lift circuit with SM controller

4.4.1 Simulation Results

When the load resistance $R = 100\ \Omega$, the triple-lift circuit works in CCM and inductor current waveform is obtained as shown in Fig. 4-8(a). We can see Δi_{L1} is about 1.5 A. We can calculate the boundary load between CCM and DCM under fixed frequency and inductance from (4-13). Load resistance $R = 4000\ \Omega$ is chosen to make the circuit work in DCM. The inductor current waveform is shown Fig. 4-8(b). It can be seen that the current in inductor L_1 is discontinuous and the peak value is 1.5 A. The results match the theoretical analysis very well.

(a) $R = 200 \Omega$ in CCM

(b) $R = 4000 \Omega$ in DCM

Figure 4-8 Inductor currents of triple-lift circuit under different operation modes

4.4.2 Stability Performance

When the input voltage $V_{in} = 30 \text{ V}$ and load resistance $R = 50 \Omega$, the output voltage and inductor current are shown in Fig. 4-9(a). The triple-lift circuit has a lot of energy elements, it needs time to charge these elements and finally the output capacitor, the start-up operation will be complicated and the start-up response will be slow if starting from zero state. Thus the output capacitor is initially charged to 400 V and the start-up response is fast and smooth. The output voltage can be kept at 400 V with little steady state error because of the integral part existing in the controller. Due to the symmetrical and parallel structure, current in each inductor is smaller.

(a) Inductor current and output voltage

(b) Voltage across the switches and diodes

Figure 4-9 Stability performances of triple-lift circuit when $V_{in} = 30$ V and $R = 50 \Omega$

The voltages across the switches and the diodes in VL cells are shown in Fig. 4-9(b) and the reversed voltage of the main diode is also shown. They are at the same voltage level and a little larger than the theoretical values obtained by (4-18) and (4-19) due to the parasitic elements neglected before. The reversed voltages across the switches and diodes in VL cells are very small thanks to the symmetrical circuit structure. This is a very outstanding advantage of these series circuits.

4.4.3 Regulation Performance

The inductor current and output voltage waveforms are shown in Fig. 4-10(a) when the input voltage increases from 30 V to 15 V at 0.07 s and decreases from 15 V to 30 V at 0.12 s with $R = 200 \Omega$. The largest current overshoot is about 5 A and the largest voltage

overshoot is less than 2 V (<0.5%), both of them happen during the second transient process which lasts less than 10 ms. The transient responses are satisfactory.

(a) When input voltage changes from 30 V to 15 V at 0.07 s and from 15 V to 30 V at 0.12 s with $R = 50 \Omega$

(b) When load resistance R changes from 200 Ω to 50 Ω at 0.07 s and from 50 Ω to 200 Ω at 0.12 s with $V_{in} = 30$ V

Figure 4-10 Regulation performances of triple-lift circuit

The inductor current and output voltage waveforms are shown in Fig. 4-10(b) when the load resistance changes from 100 Ω to 10 Ω at 0.07 s and 10 Ω to 100 Ω at 0.12 s with $V_{in} = 30$ V. The transient overshoot of the inductor current is about 5 A. When the output load changes from 200 Ω to 50 Ω , the output capacitor provides energy to the load, which leads to the output voltage dropping by about 2 V. When the output load changes from 50 Ω to 200 Ω , the extra energy in the circuit will go into the output capacitor, thus the output voltage increases by about 2 V. All the transient time is very short, less than 10 ms.

4.5 Conclusion

A series of Voltage-Lift Split-Inductor-type boost converter is described in this chapter. Much higher voltage transfer gain is obtained due to the implementation of VL technique. CCM and DCM analysis are given for re-lift, triple-lift and n^{th} -lift circuit respectively. Triple-lift circuit is analyzed based on reduced-order state-space modeling and an improved SM controller is implemented. The experimental results show triple-lift circuit can step up the output voltage to an even higher level with satisfactory performance.

Chapter 5 Voltage-Lift-Type Switched-Inductor Converters

The concept of Voltage-Lift-type Switched-Inductor (SI) cells is described in this Chapter. These circuit cells can be used to improve the boost abilities of those traditional transformerless DC-DC converters. More importantly, they can be fabricated as integrated cells and inserted into all the basic converters easily. All newly-developed converters are applicable to those situations where high voltage transfer gains are required. Hybrid boost converters integrated with the described SI cells are analyzed as an example of application in second-order converters. Both CCM and DCM operations are analyzed. Hybrid Positive Output Elementary Luo (POEL) converters integrated with the described SI cells are then described in both CCM and DCM operations as an example of application in four-order converters. All theoretical results are supported by the corresponding simulation and experimental results.

5.1 Introduction

A systematic, topology-based method of designing new converters was described in [48], in which the duality principles between the basic Switched-Capacitor (SC) cell and the basic Switched-Inductor (SI) cell [44-51] were used for higher voltage transfer gains. Analogously, a new SI boost converter was designed in [166]. More active switches are required in this circuit, and it may lead to more power losses and higher cost. On the other hand, this active-switch-based topology cannot be fabricated as a cell and applied to other basic DC-DC converters. Furthermore, the ground points of the input and output voltage in above-mentioned topologies are usually different, which will bring some problems in the applications.

In this chapter, the concept of the Voltage-Lift (VL) technique [32-43] is applied to the traditional SI cell, resulting in a series of new VL-type SI cells with enhanced DC-DC

boost abilities. They can be integrated into all the basic DC-DC converters to provide higher voltage transfer gains. First, boost converter is integrated with the series of VL-type SI cells and these hybrid boost converters are analyzed in both CCM and DCM. POEL converter is then integrated with this series of SI cells as an example for four-order converters to demonstrate the circuit characteristics of the described VL-type SI cells.

5.2 Voltage-Lift-Type Switched-Inductor Cells

The basic SI cell formed by two inductors and three diodes is shown in Fig. 5-1(a) for reference [48], and its switching operations are shown in Fig. 5-1(b) and Fig. 5-1(c). During the switching-on period of the main switch, D_1 and D_2 conduct, while L_1 and L_2 are charged in parallel. During the switching-off period of the main switch, D_0 conducts, while L_1 and L_2 are discharged in series.

The VL technique is then applied to the basic SI cell shown in Fig. 5-1, which can generate new VL-type SI cells with higher voltage transfer gains. As shown in Fig. 5-2(a), a capacitor C_1 and a diode D_3 are added to form a VL branch. For the convenience of analysis, this cell is termed self-lift SI cell, and its switching operations are shown in Fig. 5-2(b) and Fig. 5-2(c). During the switching-on period of the main switch, D_1 , D_2 and D_3 conduct, while L_1 , L_2 and C_1 are charged in parallel. During the switching-off period of the main switch, D_0 conducts, while L_1 , L_2 and C_1 are discharged in series.

(a) Topology

(b) During the switching-on period of the main switch, T_{on}

(c) During the switching-off period of the main switch, T_{off}

Figure 5-1 The basic SI cell

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

Figure 5-2 The self-lift SI cell

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

Figure 5-3 The double-self-lift SI cell

Similarly, on the basis of Fig. 5-2, adding one more VL branch can generate another circuit cell, and the corresponding topology is shown in Fig. 5-3(a). For the convenience of analysis, this cell is termed double-self-lift SI cell, and its switching operations are shown in Fig. 5-3(b) and Fig. 5-3(c). It is noted that an auxiliary unidirectional switch S_0 (e.g., transistor or MOSFET) is added. S_0 is used instead of D_0 that exists in the first two cells, by which the potential short circuit phenomena can be avoided during the switching-on period of the main switch. During the switching-on period, D_1 , D_2 , D_3 and

D_4 conduct, while S_0 is off. L_1 , L_2 , C_1 and C_2 are thus charged in parallel. During the switching-off period of the main switch, D_1 , D_2 , D_3 and D_4 are blocked, while S_0 is on. And consequently, L_1 , L_2 , C_1 and C_2 are discharged in series.

The above three SI cells can be regarded as a family of novel enhanced circuits, and they can be integrated with the traditional boost, buck-boost, Ćuk, SEPIC converters as well as the other developed DC-DC converters such as POEL converters [32].

5.3 Hybrid Boost Converter with Basic SI Cell

The basic SI cell is inserted into basic boost converter, which results in the new hybrid topology as shown in Fig. 5-4(a). The equivalent circuits during switching-on and -off are shown in Fig. 5-4(b) and (c), respectively.

5.3.1 CCM Analysis

When the main switch S is on, D_1 , D_2 conduct, D_0 and D are reversely biased. L_1 and L_2 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$ and $i_{L1} = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, the output capacitor provides energy to the output load. Both the currents i_{L1} and i_{L2} increase, and the charges on C_O decrease.

When S is off, D_0 conducts. L_1 and L_2 are connected in series, and i_L flows through diode D to transfer their stored energy to output capacitor C_O and the output load. The inductor current i_L decreases and the charges on C_O increase.

(a) Topology

 (b) During the switching-on time of the main switch, T_{on}

 (c) During the switching-off time of the main switch, T_{off}

Figure 5-4 Hybrid boost converter with the basic SI cell

During switching-on time uT (u ($1 < u < 1$) is the duty cycle, T is the switching period), L_1 and L_2 are supplied by V_{in} in parallel, so both i_{L1} and i_{L2} increase. During switching-off time $(1-u)T$, they are series and supplied by $(V_{in}-V_O)$. Using the volt-second balance principle, we have

$$uTV_{in} + (1-u)T \frac{V_{in}-V_O}{2} = 0 \quad (5-1)$$

Thus we can get the voltage transfer gain from (5-1)

$$M_{1CCM} = \frac{V_o}{V_{in}} = \frac{1+u}{1-u} \quad (5-2)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-3)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{uTV_{in}}{2L_1 I_{L1}} = \frac{u(1-u)R}{2LM_{1CCM}f} \quad (5-4)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{u(1-u)R}{2LM_{1CCM}f} \quad (5-5)$$

Then we have

$$\xi_1 = \xi_2 = \xi \quad (5-6)$$

The ripple voltage of output voltage V_o is

$$\Delta v_o = \frac{\Delta Q_{Co}}{C_o} = \frac{uTI_o}{C_o} \quad (5-7)$$

The voltage stress of the main switch and the main diode are

$$V_s = V_D = V_o = \frac{1+u}{1-u} V_{in} \quad (5-8)$$

5.3.2 DCM Analysis

When S is off, if the inductor currents in the basic SI cell reach to zero, the current cannot flow reversely due to the existence of D_0 . Thus, the circuit will go to DCM, so there is only the output capacitor provides energy to the output load.

The circuit operates in DCM if the current i_{Ll} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{u(1-u)}{2M_{ICCM}} Z_N \geq 1 \quad (5-9)$$

As a special case, when i_{Ll} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary value of Z_N between CCM and DCM is obtained as below:

$$Z_{INB} = \frac{2M_{ICCM}}{u(1-u)} = \frac{2(1+u)}{u(1-u)^2} \quad (5-10)$$

The circuit will operate in DCM when $Z_N > Z_{INB}$. Under this condition i_{Ll} decreases to zero at $t = t_l = (u + u_l) T$, where $uT < t_l < T$ and $0 < u_l < (1-u)$.

In DCM, current i_{Ll} increases during switching-on and decreases during the period from uT to $(u + u_l)T$. The corresponding voltages across L_l are V_{in} and $(V_{in} - V_O)$. Thus, in DCM, using the volt-second balance principle, we have

$$u_l = \frac{2uV_{in}}{V_O - V_{in}} \quad (5-11)$$

The average value of the output capacitor current during each switching period is given by

$$I_{CO} = \frac{u_l T \left(\frac{V_{in}}{2L} uT \right) - I_O T}{T} = 0 \quad (5-12)$$

Combining (5-11) and (5-12), we obtain the voltage transfer gain in DCM:

$$M_{DCM} = \frac{I}{2} + \sqrt{\frac{I}{4} + u^2 Z_N} \quad (5-13)$$

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

Figure 5-5 Hybrid boost converter with the self-lift SI cell

5.4 Hybrid Boost Converter with Self-lift SI Cell

Fig. 5-5(a) shows the new hybrid boost converter integrating with the self-lift SI cell. The equivalent circuits during switching-on and -off are shown in Fig. 5-5(b) and (c), respectively.

5.4.1 CCM Analysis

When the main switch S is on, D_1 , D_2 and D_3 conduct, D_0 and D are reversely biased. L_1 , L_2 and C_1 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$ and $i_{L1} = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, output capacitor provides energy to the output load. Inductor current i_L and the charges on C_1 increase, the charges on C_O decrease.

When S is off, D_0 and D conduct, D_1 , D_2 and D_3 are reversely biased. L_1 , L_2 and C_1 are thus connected in series to provide energy to the output capacitor C_O and output load. The inductor current i_L and the charges on C_1 decrease, the charges on C_O increase.

During switching-on, L_1 and L_2 are supplied by V_{in} in parallel. During switching-off, they are series connected and supplied by $(V_{in} + V_{C1} - V_O)$. Using the volt-second balance principle, we have

$$uTV_{in} + (1-u)T \frac{V_{in} + V_{C1} - V_O}{2} = 0 \quad (5-14)$$

By assuming $V_{C1} = V_{in}$, we can get

$$M_{2CCM} = \frac{V_O}{V_{in}} = \frac{2}{1-u} \quad (5-15)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-16)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{kTV_{in}}{2L_1 I_{L1}} = \frac{u(1-u)R}{2LM_{2CCM}f} \quad (5-17)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{u(1-u)R}{2LM_{2CCM}f} \quad (5-18)$$

Then we have

$$\xi_1 = \xi_2 = \xi \quad (5-19)$$

The ripple voltage of output voltage V_O is

$$\Delta v_o = \frac{\Delta Q_{Co}}{C_o} = \frac{uTI_o}{C_o} \quad (5-20)$$

The voltage stress of the main switch and the main diode are

$$V_S = V_D = V_O = \frac{2}{1-u} V_{in} \quad (5-21)$$

5.4.2 DCM Analysis

When S is off, if the inductor currents in the self-lift SI cell reach to zero, the current cannot flow reversely due to the existence of D_0 . Thus, the circuit will go to DCM, so there is only the output capacitor provides energy to the output load.

The circuit operates in DCM if the current i_{L1} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{u(1-u)}{2M_{2CCM}} Z_N \geq 1 \quad (5-22)$$

As a special case, when i_{LI} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary values of Z_N between CCM and DCM is obtained as below:

$$Z_{2NB} = \frac{2M_{2CCM}}{u(1-u)} = \frac{4}{u(1-u)^2} \quad (5-23)$$

The circuit will operate in DCM when $Z_N > Z_{2NB}$. Under this condition i_{LI} decreases to zero at $t = t_2 = (u + u_2)T$, where $uT < t_2 < T$ and $0 < u_2 < (1-u)$.

In DCM, current i_{LI} increases during switching-on and decreases during the period from uT to $(u + u_2)T$. The corresponding voltages across L_I are V_{in} and $(2V_{in} - V_O)$. Thus, in DCM, using the volt-second balance principle, we have

$$u_2 = \frac{2uV_{in}}{V_O - 2V_{in}} \quad (5-24)$$

The average value of the output capacitor current during each switching period is given by

$$I_{CO} = \frac{u_2 T \left(\frac{V_{in}}{2L} uT \right) - I_O T}{T} = 0 \quad (5-25)$$

Combining (5-24) and (5-25), we obtain the voltage transfer gain in DCM:

$$M_{DCM} = 1 + \sqrt{1 + u^2 Z_N} \quad (5-26)$$

5.5 Hybrid Boost Converter with Double-Self-Lift SI Cell

The integration of the double self-lift SI cell into the POEL converter generates a new hybrid topology as shown in Fig. 5-6(a). The equivalent circuits during switching-on and -off are shown in Fig. 5-6(b) and (c), respectively. S is the main switch of the converter, and S_0 is the auxiliary switch.

(a) Topology

(b) During the switching-on period of the main switch, T_{on}

(c) During the switching-off period of the main switch, T_{off}

Figure 5-6 Hybrid POEL converter with the double-self-lift SI cell

5.5.1 CCM Analysis

When S is on, S_0 is off. D is reversely biased, while D_1 , D_2 , D_3 and D_4 conduct. And consequently, L_1 , L_2 and C_1 , C_2 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$, and $i_L = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, output capacitor C_O provides energy to the output load. Inductor current i_L increases, the charges on C_1 and C_2 increase, and the charges on C_O decrease.

When S is off, S_0 is on. Main diode D conducts, while D_1 , D_2 , D_3 and D_4 are reversely biased. And consequently, L_1 , L_2 , C_1 and C_2 are connected in series. Inductor current i_L flows through diode D to charge C_O and provide energy to the output load. Inductor current i_L decreases. The charges on C_1 and C_2 decrease, while the charges on C increase.

During switching-on, L_1 and L_2 are supplied by V_{in} in parallel. During switching-off, they are series and supplied by $(V_{in} + V_{C1} + V_{C2} - V_O)$. Using the volt-second balance principle, we have

$$uTV_{in} + (1-u)T \frac{V_{in} + V_{C1} + V_{C2} - V_O}{2} = 0 \quad (5-27)$$

By assuming $V_{C1} = V_{C2} = V_{in}$, we can get

$$M_{3CCM} = \frac{V_O}{V_{in}} = \frac{3-u}{1-u} \quad (5-28)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-29)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{uTV_{in}}{2L_1 I_{L1}} = \frac{u(1-u)R}{2LM_{3CCM}f} \quad (5-30)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{u(1-u)R}{2LM_{3CCM}f} \quad (5-31)$$

Then we have

$$\xi_1 = \xi_2 = \xi \quad (5-32)$$

The ripple voltage of output voltage V_O is

$$\Delta v_o = \frac{\Delta Q_{Co}}{C_o} = \frac{uT I_o}{C_o} \quad (5-33)$$

The voltage stress of the main switch and the main diode are

$$V_s = V_D = V_o = \frac{3-u}{1-u} V_{in} \quad (5-34)$$

5.5.2 DCM Analysis

When S is still off, if the inductor currents in the double self-lift SI cell reach to zero, the current cannot flow reversely due to the existence of D. Thus, the circuit will go to DCM, there is only the output capacitor provides energy to the output load.

The circuit operates in DCM if the current i_{L1} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{u(1-u)}{2M_{3CCM}} Z_N \geq 1 \quad (5-35)$$

As a special case, when i_{L1} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary value of Z_N between CCM and DCM is obtained as below:

$$Z_{3NB} = \frac{2M_{3CCM}}{u(1-u)} = \frac{2(3-u)}{u(1-u)^2} \quad (5-36)$$

The circuit will operate in DCM when $Z_N > Z_{3NB}$. Under this condition i_{LI} decreases to zero at $t = t_3 = (u + u_3)T$, where $uT < t_3 < T$ and $0 < u_3 < (1 - u)$.

In DCM, current i_{LI} increases during switching-on and decreases during the period from uT to $(u + u_3)T$. The corresponding voltages across L_I are V_{in} and $(3V_{in} - V_O)$. Thus, in DCM, using the volt-second balance principle, we have

$$u_3 = \frac{2uV_{in}}{V_o - 3V_{in}} \quad (5-37)$$

The average value of the output capacitor current during each switching period is given by

$$I_{CO} = \frac{u_3 T \left(\frac{V_{in}}{2L} uT \right) - I_O T}{T} = 0 \quad (5-38)$$

Combining (5-37) and (5-38), we obtain the voltage transfer gain in DCM:

$$M_{DCM} = \frac{3}{2} + \sqrt{\frac{9}{4} + u^2 Z_N} \quad (5-39)$$

5.6 Hybrid POEL Converter with Basic SI Cell

To illustrate the high application flexibility, in this section we take the POEL converter as an example to introduce the main principles and integration of fourth-order converters with this series of SI cells. The topology of the POEL converter is shown in Fig. 5-7, and the detailed operation principles can be referred to [32]. As a kind of four-order DC-DC converters, it differs from other existing fourth-order DC-DC converters that have the feature of the output polarity inversion such as the Ćuk converter and the buck-boost converter. The voltage transfer function can be expressed by $u / (1 - u)$, which means this converter performs positive-to-positive DC-DC step-up and step-down voltage conversion.

Figure 5-7 Topology of the POEL converter

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

Figure 5-8 Hybrid POEL converter with the basic SI cell

The basic SI cell is inserted into POEL converter, which results in the new hybrid topology as shown in Fig. 5-8(a). The equivalent circuits during switching-on and -off are shown in Fig. 5-8(b), (c) and (d), respectively. S is the main switch of the converter.

5.6.1 CCM Analysis

When S is on, D_1 , D_2 conduct, D_0 and D are reversely biased. L_1 and L_2 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$ and $i_{L1} = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, L_0 absorbs the energy from the source and C. Both the currents i_L and i_{L0} increase, and the charges on C decrease.

When S is off, D_0 conducts. L_1 and L_2 are connected in series, and i_L flows through the freewheeling diode D to charge C. Both L_1 and L_2 transfer their stored energy to C. At the same time, i_{L0} flows through C_0 -R circuit and D to keep continuous. Both i_L and i_{L0} decrease, and the charges on C increase.

During switching-on, L_1 and L_2 are supplied by V_{in} in parallel, so both i_{L1} and i_{L2} increase. During switching-off, they are in series and supplied by $-V_C$. Using the volt-second balance principle, we have

$$uTV_{in} - (1-u)T \frac{V_C}{2} = 0 \quad (5-40)$$

Similarly for L_0 , we have

$$uT(V_C + V_{in} - V_o) - (1-u)TV_o = 0 \quad (5-41)$$

Thus we can get the voltage transfer gain from (5-40) and (5-41)

$$M_{1CCM} = \frac{V_o}{V_{in}} = \frac{u + u^2}{1 - u} \quad (5-42)$$

Meanwhile, we can get the voltage on the capacitor C,

$$V_C = \frac{2u}{1 - u} V_{in} = \frac{2}{1 + u} V_o \quad (5-43)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-44)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{uTV_{in}}{2L_1 I_{L1}} = \frac{(1 - u)R}{2LM_{1CCM}f} \quad (5-45)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{(1 - u)R}{2LM_{1CCM}f} \quad (5-46)$$

Since L_1 is in series with L_2 , we have

$$\xi_1 = \xi_2 = \xi \quad (5-47)$$

The peak-to-peak current variation of i_{LO} is denoted as

$$\Delta i_{LO} = \frac{uT(V_C + V_{in} - V_o)}{L_o} \quad (5-48)$$

The variation ratio of i_{LO} is

$$\xi_o = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{uT(V_C + V_{in} - V_O)}{2L_O I_{LO}} = \frac{u(1+u)R}{2L_O M_{ICCM} f} \quad (5-49)$$

The ripple voltage of output voltage V_O is

$$\Delta v_o = \frac{\Delta Q_{CO}}{C_o} = \frac{uT(I_{LO} - I_o)}{C_o} \quad (5-50)$$

Because we assume $I_{LO} = I_o$ in the former analysis based on the function of the capacitor, which is to stabilize the voltage, the variation of output voltage V_O is small enough to be neglected.

The voltage stress of the main switch and the main diode are

$$V_S = V_D = V_C + V_{in} = \frac{1+u}{1-u} V_{in} \quad (5-51)$$

5.6.2 DCM Analysis

For L_O , if its current i_{LO} reaches to zero, under the condition that S is off, the energy to the load will be provided by C_O . This situation will not be considered in the paper, and i_{LO} is assumed continuous. Here, we only consider the following DCM situation. When S is off, if the inductor currents in the basic SI cell reach to zero, the current cannot flow reversely due to the existence of D_0 . Thus, the circuit will go to DCM as illustrated in Fig. 5-8(d).

The circuit operates in DCM if the current i_{LI} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{(1-u)}{2M_{ICCM}} Z_N \geq 1 \quad (5-52)$$

As a special case, when i_{LI} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary value of Z_N between CCM and DCM is obtained as below:

$$Z_{INB} = \frac{2M_{ICCM}}{1-u} = \frac{2u(1+u)}{(1-k)^2} \quad (5-53)$$

The circuit will operate in DCM when $Z_N > Z_{INB}$. Under this condition i_{LI} decreases to zero at $t = t_I = [u + m_I(1-u)]T$, where $uT < t_I < T$ and $0 < m_I < 1$.

In DCM, current i_{LI} increases during switching-on and decreases during the period from uT to $m_I(1-u)T$. The corresponding voltages across L_I are V_{in} and $uV_{in}/m_I(1-u)$. Thus, in DCM, the voltage across C is equal to

$$V_C = \frac{2u}{m_I(1-u)} V_{in} \quad (5-54)$$

Thus, using the volt-second balance principle on L_O , we have

$$uT(V_{in} + V_C - V_O) - (1-u)TV_O = 0 \quad (5-55)$$

Additionally, the transferred charges of L_I during switching-off are equal to $m_I(1-u)T\Delta i_{LI}/2$, which compensate the total consumed charges of the load. So we have

$$\frac{1}{2}m_I(1-u)T\Delta i_{LI} = uTI_{LO} \quad (5-56)$$

Combining (5-44), (5-54), (5-55) and (5-56), we obtain

$$m_I = \frac{u + u\sqrt{1+4Z_N}}{(1-u)Z_N} \quad (5-57)$$

Also from (5-44), (5-54), (5-55) and (5-56), we get

$$V_O = \frac{1}{2}m_I(1-u)Z_N V_{in} \quad (5-58)$$

Therefore, substituting (5-57) into (5-58) yields the following voltage transfer gain in DCM:

$$M_{1DCM} = \frac{u + u\sqrt{1 + 4Z_N}}{2} \quad (5-59)$$

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

(d) DCM

Figure 5-9 Hybrid POEL converter with the self-lift SI cell

5.7 Hybrid POEL Converter with Self-lift SI Cell

Fig. 5-9(a) shows the new hybrid topology integrating with the self-lift SI cell. The equivalent circuits during switching-on and -off are shown in Fig. 5-9(b), (c) and (d), respectively. S is the main switch of the converter.

5.7.1 CCM Analysis

When S is on, D_1 , D_2 and D_3 conduct, D_0 and D are reversely biased. L_1 , L_2 and C_1 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$ and $i_{L1} = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, L_O absorbs energy from the source and C, so charges on C decrease. i_L , i_{LO} and the charges on C_1 increase.

When S is off, D_0 and D conduct, D_1 , D_2 and D_3 are reversely biased. L_1 , L_2 and C_1 are thus connected in series. Current i_L flows through the freewheeling diode D to charge C. At the same time, i_{LO} flows through C_O -R circuit and freewheeling diode D to keep itself continuous. Both i_L and i_{LO} decrease. The charges on C_1 decrease and the charge on C increase.

During switching-on, L_1 and L_2 are supplied by V_{in} in parallel, so both i_{L1} and i_{L2} increase. During switching-off, they are in series and supplied by $(V_{C1} - V_C)$. Using the volt-second balance principle, we have

$$uTV_{in} + (1-u)T \frac{V_{C1} - V_C}{2} = 0 \quad (5-60)$$

Similarly for L_O , we have

$$uT(V_C + V_{in} - V_O) - (1-u)TV_O = 0 \quad (5-61)$$

By assuming $V_{C1} = V_{in}$, we can get

$$M_{2CCM} = \frac{V_O}{V_{in}} = \frac{2u}{1-u} \quad (5-62)$$

Meanwhile, we get the voltage across capacitor C

$$V_C = \frac{1+u}{1-u} V_{in} = \frac{1+u}{2u} V_o \quad (5-63)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-64)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{uTV_{in}}{2L_1 I_{L1}} = \frac{(1-u)R}{2LM_{2CCM}f} \quad (5-65)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{(1-u)R}{2LM_{2CCM}f} \quad (5-66)$$

Since L_1 is in series with L_2 , we have

$$\xi_1 = \xi_2 = \xi \quad (5-67)$$

The peak-to-peak current variation of i_{LO} is denoted as

$$\Delta i_{LO} = \frac{uT(V_C + V_{in} - V_o)}{L_o} \quad (5-68)$$

The variation ratio of i_{LO} is

$$\xi_o = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{uT(V_C + V_{in} - V_o)}{2L_o I_{LO}} = \frac{uR}{L_o M_{2CCM}f} \quad (5-69)$$

The ripple voltage of output voltage V_o is

$$\Delta v_o = \frac{\Delta Q_{Co}}{C_o} = \frac{uT(I_{LO} - I_o)}{C_o} \quad (5-70)$$

Similarly, the variation of output voltage V_O is small enough to be neglected.

The voltage stress of the main switch and the main diode are

$$V_S = V_D = V_C + V_{in} = \frac{2}{1-u} V_{in} \quad (5-71)$$

5.7.2 DCM Analysis

The assumption of i_{Lo} is the same as that in Section 5.4.1. When S is off, if the inductor currents in the self-lift SI cell reach to zero, the current cannot flow reversely due to the existence of D_0 . Thus, the circuit will go to DCM as illustrated in Fig. 5-9(d).

The circuit operates in DCM if the current i_{Ll} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{(1-u)}{2M_{2CCM}} Z_N \geq 1 \quad (5-72)$$

As a special case, when i_{Ll} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary values of Z_N between CCM and DCM is obtained as below:

$$Z_{2NB} = \frac{2M_{2CCM}}{1-u} = \frac{4u}{(1-u)^2} \quad (5-73)$$

The circuit will operate in DCM when $Z_N > Z_{2NB}$. Under this condition i_{Ll} decreases to zero at $t = t_1 = [u + m_2(1-u)]T$, where $uT < t_1 < T$ and $0 < m_2 < 1$. Here, m_2 is the current filling efficiency for the circuit.

In DCM, current i_{Ll} increases during switching-on and decreases during the period from uT to $m_2(1-u)T$. The corresponding voltages across L_l are V_{in} and $uV_{in}/m_2(1-u)$. Thus, in DCM, the voltage across C is equal to

$$V_C = \frac{2u}{m_2(1-u)}V_{in} + V_{in} \quad (5-74)$$

Thus, using the volt-second balance principle on L_O , we have

$$uT(V_{in} + V_C - V_O) - (1-u)TV_O = 0 \quad (5-75)$$

Additionally, the transferred charges of L_I during switching-off are equal to $m_2(1-u)T\Delta i_{L_I}/2$, which compensate the total consumed charges of the load. So we have

$$\frac{I}{2}m_2(1-u)T\Delta i_{L_I} = I_{LO}uT \quad (5-76)$$

Combining (5-64), (5-74), (5-75) and (5-76), we obtain

$$m_2 = \frac{2u + 2u\sqrt{1+Z_N}}{(1-u)Z_N} \quad (5-77)$$

Also from (5-64), (5-74), (5-75) and (5-76), we get

$$V_O = \frac{I}{2}m_2(1-u)Z_NV_{in} \quad (5-78)$$

Therefore, substituting (5-77) into (5-78) yields the following voltage transfer gain in DCM:

$$M_{2DCM} = u + u\sqrt{1+Z_N} \quad (5-79)$$

5.8 Hybrid POEL Converter with Double Self-lift SI Cell

The integration of the double self-lift SI cell into the POEL converter generates the new hybrid topology as shown in Fig. 5-10(a). The equivalent circuits during switching-on and -off are shown in Fig. 5-10(b), (c) and (d), respectively. S is the main switch of the converter, and S_0 is the auxiliary switch.

(a) Topology

(b) During the switching-on time of the main switch, T_{on}

(c) During the switching-off time of the main switch, T_{off}

(d) DCM

Figure 5-10 Hybrid POEL converter with the double self-lift SI cell

5.8.1 CCM Analysis

When S is on, S_0 is off. D is reversely biased, while D_1 , D_2 , D_3 and D_4 conduct. And consequently, L_1 , L_2 and C_1 , C_2 are connected in parallel. L_1 and L_2 are designed to be the same (i.e., $L_1 = L_2 = L$, and $i_{L1} = i_{L2} = i_L$). Both inductors absorb energy from the source. At the same time, L_O absorbs energy from the source and C, so the charges on C decrease. Both i_L and i_{LO} increase, and the charges on C_1 and C_2 increase.

When S is off, S_0 is on. D conducts, while D_1 , D_2 , D_3 and D_4 are reversely biased. And consequently, L_1 , L_2 , C_1 and C_2 are connected in series. i_L flows through the freewheeling diode D to charge C. L_1 , L_2 and C_1 , C_2 transfer their stored energy to C. At the same time, i_{LO} flows through C_O -R circuit and freewheeling diode D to keep itself continuous. Both i_L and i_{LO} decrease. The charges on C_1 and C_2 decrease, while the charges on C increase.

During switching-on, L_1 and L_2 are supplied by V_{in} in parallel, so both i_{L1} and i_{L2} increase. During switching-off, they are in series and supplied by $(V_{C1} + V_{C2} - V_C)$. Using the volt-second balance principle, we have

$$uTV_{in} + (1-u)T \frac{V_{C1} + V_{C2} - V_C}{2} = 0 \quad (5-80)$$

Similarly for L_O , we have

$$uT(V_C + V_{in} - V_O) - (1-u)TV_O = 0 \quad (5-81)$$

By assuming $V_{C1} = V_{C2} = V_{in}$, we can get

$$M_{3CCM} = \frac{V_O}{V_{in}} = \frac{3u - u^2}{1 - u} \quad (5-82)$$

Meanwhile, we can get the voltage across capacitor C,

$$V_C = \frac{2}{1-u}V_{in} = \frac{2}{3u - u^2}V_O \quad (5-83)$$

Since the peak-to-peak current variation of i_{L1} is denoted as

$$\Delta i_{L1} = \frac{uTV_{in}}{L_1} \quad (5-84)$$

The variation ratio of i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{uTV_{in}}{2L_1 I_{L1}} = \frac{(1-u)R}{2LM_{3CCM}f} \quad (5-85)$$

Similarly,

$$\xi_2 = \frac{\Delta i_{L2} / 2}{I_{L2}} = \frac{(1-u)R}{2LM_{3CCM}f} \quad (5-86)$$

Since L_1 is in series with L_2 , we have

$$\xi_1 = \xi_2 = \xi \quad (5-87)$$

The peak-to-peak current variation of i_{LO} is denoted as

$$\Delta i_{LO} = \frac{uT(V_C + V_{in} - V_O)}{L_O} \quad (5-88)$$

The variation ratio of i_{LO} is

$$\xi_O = \frac{\Delta i_{LO} / 2}{I_{LO}} = \frac{uT(V_C + V_{in} - V_O)}{2L_O I_{LO}} = \frac{(3u - u^2)R}{L_O M_{3CCM}f} \quad (5-89)$$

The ripple voltage of output voltage V_O is

$$\Delta v_O = \frac{\Delta Q_{CO}}{C_O} = \frac{uT(I_{LO} - I_O)}{C_O} \quad (5-90)$$

Similarly, the variation of output voltage V_O is small enough to be neglected.

The voltage stress of the main switch and the main diode are

$$V_S = V_D = V_C + V_{in} = \frac{3-u}{1-u} V_{in} \quad (5-91)$$

5.8.2 DCM Analysis

The assumption of i_{L0} is the same as that in Section 5.4.1. When S is still off, if the inductor currents in the double self-lift SI cell reach to zero, the current cannot flow reversely due to the existence of S_0 . Thus, the circuit will go to DCM as illustrated in Fig. 5-10(d).

The circuit operates in DCM if the current i_{LI} reduces to zero during switching-off. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi = \frac{(1-u)}{2M_{3CCM}} Z_N \geq 1 \quad (5-92)$$

As a special case, when i_{LI} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary value of Z_N between CCM and DCM is obtained as below:

$$Z_{3NB} = \frac{2M_{3CCM}}{1-u} = \frac{6u-2u^2}{(1-u)^2} \quad (5-93)$$

The circuit will operate in DCM when $Z_N > Z_{3NB}$. Under this condition i_{LI} decreases to zero at $t = t_1 = [u + m_3(1-u)]T$, where $uT < t_1 < T$ and $0 < m_3 < 1$. Here, m_3 is the current filling efficiency for the developed double self-lift circuit.

In DCM, current i_{LI} increases during switching-on and decreases during the period from uT to $m_3(1-u)T$. The corresponding voltages across L_I are V_{in} and $uV_{in}/m_3(1-u)$. Thus, in DCM, the voltage across C is equal to

$$V_C = \frac{2u}{m_3(1-u)} V_{in} + 2V_{in} \quad (5-94)$$

Thus, using the volt-second balance principle on L_O , we have

$$uT(V_{in} + V_C - V_O) - (1-u)TV_O = 0 \quad (5-95)$$

Additionally, the transferred charges of L_I during switching-off are equal to $m_3(1-u)T\Delta i_{LI}/2$, which compensate the total consumed charges of the load. So we have

$$\frac{1}{2}m_3(1-u)T\Delta i_{LI} = uTI_{LO} \quad (5-96)$$

Combining (5-84), (5-94), (5-95) and (5-96), we obtain

$$m_3 = \frac{3u + u\sqrt{9 + 4Z_N}}{Z_N} \quad (5-97)$$

Also from (5-84), (5-94), (5-95) and (5-96), we get

$$V_O = \frac{1}{2}m_3(1-k)Z_NV_{in} \quad (5-98)$$

Therefore, substituting (5-97) into (5-98) yields the following voltage transfer gain in DCM:

$$M_{3DCM} = \frac{3u + u\sqrt{9 + 4Z_N}}{2} \quad (5-99)$$

5.9 Summary and Verification

This series of SI cells with VL technique can be inserted into many DC-DC topologies. It can be easily known that the classical boost converter integrated with the VL-type SI cells will have very large voltage transfer gains that are the same as in [166]. The main characteristics of the hybrid boost converters are similar to those in Chapter 4. Besides, the hybrid boost converters have one more advantage that both the input end and output end have the same grounding point. The characteristics of the hybrid POEL converters will be summarized and verified below.

5.9.1 Comparison and Discussion of Hybrid POEL Converters

The main characters of hybrid POEL converters with different SI cells are shown in Table 5-1, where the corresponding characters of the POEL converter is also given for reference. The relationships of the voltage transfer gains, the duty cycles and the normalized loads are illustrated in Fig. 5-11 for the three hybrid POEL converters. Compared to the basic POEL converter, under the same input and output conditions, the hybrid POEL converters can get larger voltage transfer gains together with smaller current ripples, which can be seen clearly in (5-45), (5-49), (5-65), (5-69), (5-85) and (5-89).

Table 5-1 Main characters of hybrid POEL converters with different SI cells

	M_{CCM}	M_{DCM}	Z_{NB}	$V_S = V_D$
POEL converter	$\frac{u}{1-u}$	$\frac{2+u\sqrt{2Z_N}}{2}$	$\frac{\sqrt{2}}{1-u}$	$\frac{1}{1-u}V_{in}$
With basic SI cell	$\frac{u+u^2}{1-u}$	$\frac{u+u\sqrt{1+4Z_N}}{2}$	$\frac{2u(1+u)}{(1-u)^2}$	$\frac{1+u}{1-u}V_{in}$
With self-lift SI cell	$\frac{2u}{1-u}$	$u+u\sqrt{1+Z_N}$	$\frac{4u}{(1-u)^2}$	$\frac{2}{1-u}V_{in}$
With double self-lift SI cell	$\frac{3u-u^2}{1-u}$	$\frac{3u+u\sqrt{9+4Z_N}}{2}$	$\frac{6u-2u^2}{(1-u)^2}$	$\frac{3-u}{1-u}V_{in}$

(a) Hybrid POEL converter with basic SI cell

(b) Hybrid POEL converter with self-lift SI cell

(c) Hybrid POEL converter with double-self-lift SI cell

(d) Comparison of the voltage transfer gains in CCM

Figure 5-11 Relationship between the voltage transfer gain and the duty cycle and the normalized load

To verify the design and calculation results, PSIM simulation package was applied to simulate these converters. Choosing $V_{in} = 12$ V, $L_1 = L_2 = L = 200$ μ H, $C_1 = C_2 = C = 20$ μ F, $L_O = 1$ mH, $u = 0.5$ and $f = 50$ kHz.

5.9.2 Simulation Results

When the load resistance $R = 10 \Omega$, the hybrid POEL converter with basic SI cell works under CCM and the waveforms of inductor currents are obtained as shown in Fig. 5-12(a). We can see Δi_{L1} is about 0.6 A and Δi_{LO} is about 0.9 A, which match the results calculated from the (5-44) and (5-48) very well.

We can calculate the boundary load between CCM and DCM under fixed frequency and inductance from (5-52). We choose $R = 100 \Omega$ to let the circuit work under DCM. The waveforms of the inductor currents are shown in Fig. 5-12(b). It can be seen that the current in inductor L_1 is discontinuous, but the current in inductor L_O is still continuous and so is the main diode D_0 .

(a) Hybrid POEL converter with basic SI cell when $R = 10 \Omega$ in CCM

(b) Hybrid POEL converter with basic SI cell when $R = 100 \Omega$ in DCM

(c) Hybrid POEL converter with self-lift SI cell when $R = 10 \Omega$ in CCM

(d) Hybrid POEL converter with self-lift SI cell when $R = 150 \Omega$ in DCM

(e) Hybrid POEL converter with double-self-lift SI cell when $R = 10 \Omega$ in CCM

(f) Hybrid POEL converter with double-self-lift SI cell when $R = 150 \Omega$ in DCM

Figure 5-12 Simulation results of inductor currents for the three cases in CCM and DCM

Similarly, we can get the inductor current for hybrid POEL converter with self-lift SI cell working under CCM when $R = 10 \Omega$ and DCM when $R = 150 \Omega$ in Fig. 5-12 (c) and (d). For hybrid POEL converter with double self-lift SI cell, inductor currents under CCM when $R = 10 \Omega$ and DCM when $R = 150 \Omega$ are shown in Fig. 5 -12(e) and (f). All the waveforms match the theoretical results very well.

5.9.3 Experimental Results

In the hardware testing circuits, hybrid POEL converter with double-self-lift SI cell is built with the same parameters as that in the simulation. Basic POEL converter is tested for comparison. The N-channel MOSFET 2SK2267 is selected as the power switches S . The drain-source on resistance is $8m\Omega$. All the diodes are realized by using

MBR6045WT, the forward voltage drop is 0.6 V. Thus, the practical output voltage is smaller than the theoretical values due to the effects caused by parasitic parameters.

Under the zero initial condition of $u = 0.5$, the corresponding experimental curves for the three cases are shown in Fig. 5-13. At the time 0.03 s, the load resistance R is changed from $10\ \Omega$ under CCM operation to $100\ \Omega$ for basic POEL converter and $150\ \Omega$ for hybrid POEL converter with double-self-lift SI cell under DCM operation. It can be concluded that the start-up overshoots of the hybrid POEL converter with double-self-lift SI cell are smaller than that of basic POEL converter. Although the start-up times are a little longer than the latter, they are all less than 10ms.

After careful measurement, we obtained that the practical output voltages V_o of the hybrid POEL converter with double-self-lift SI cell are 29.8 V when $R = 10\ \Omega$ and duty cycle $u = 0.5$, which are close to the theoretical analysis and the simulation results. The boost ability of these cells can be seen apparently by comparison to that of POEL converter, which is equal to the input voltage when duty cycle $u = 0.5$. The corresponding DCM output voltage is larger than that of CCM according to the former analysis. Additionally, the transient response from CCM to DCM is smoothly and quickly, which is close to the dynamics of basic DC-DC converters [168-170].

Figure 5-13 Start-up response and transient response from CCM to DCM

When there is a load disturbance at 0.035 s, which is the load resistance changes from $30\ \Omega$ to $10\ \Omega$ and back to $30\ \Omega$ quickly at 0.036 s, the responses of the POEL converter and the hybrid POEL converter with double-self-lift SI cell are shown in Fig. 5-14. The overshoot for the hybrid POEL converter is around 7.5 V (25%) and that of the basic

converter is around 3 V (25%). The results show that the output voltage of hybrid POEL converter with double-self-lift SI cell can handle transient load disturbance and keep the system stable as well as the basic POEL converter.

Figure 5-14 Transient response when then R changes from 30 Ω to 10 Ω at 0.035 s and back to 30 Ω at 0.036 s

As shown in Fig. 5-15, the voltage stress of the main switch in hybrid PEOL converter is around 60 V, the voltage stress of the main switch in basic POEL converter is 12 V, both of which are in accord with the theoretical analysis.

Figure 5-15 Voltage stresses of the main switches

From the above results, it can be seen that hybrid POEL converter can step up the output voltage and maintain the transient response as well as that of the basic POEL converter. The voltage stress of the main switch in hybrid POEL converters are increased with the step-up output voltage and switches with larger voltage rates are needed, which is a disadvantage for the hybrid POEL converters.

5.10 Conclusion

The concepts of the Voltage-Lift-type Switched-Inductor cells are described, which can step up the output voltages of DC-DC converters to higher levels. Examples of hybrid boost converters integrated with this series of SI cells are given to show the application in second-order DC-DC converters. Hybrid POEL converters integrated with the various SI cells are given to show the application in high-order DC-DC converters. All analysis results in both CCM and DCM have been validated by the simulation and experimental results. This series of SI cells can be widely applied to those circuits where strong DC-DC boost abilities are needed, such as the lower DC voltage from the solar panel is to step up to very high DC bus voltage in the renewable energy system.

Chapter 6 N-Switched-Capacitor Buck Converters

A series of n -Switched-Capacitor buck converters are described in this chapter. The most important feature is that they can provide even steeper step-down voltage to satisfy some extreme applications where low voltage and high current are required. They have the advantages of smaller sizes and simpler controlling algorithm compared to cascade buck converter, higher efficiency compared to the quadratic converter reported in former literature. This series can be applied to on-board aeronautics modern power architectures and solar energy storage systems. Theoretical analysis is supported by simulation and experimental results.

6.1 Introduction

Nowadays, Integrated Circuits (ICs) are drawing their power from less 5 V power supplies. It is estimated that the supply voltage for future microprocessors will decrease from 3.5 V to 1 V, and even lower, in order to decrease the power loss of modern high power consumption CPUs. Power supplies able to reduce the standard voltage of 12 V (or 48 V) to about 1 V are necessary [48]. The output of the solar panel cell is 31 V / 13 A, and then converters with steeper step-down voltage conversion ratio is required when it is necessary to store the energy into batteries whose input usually will be 4.2 V / 96 A. In automobile power supply system, for example the input voltage is 12 V/100 W, there are several devices' required voltage is just 5 V or less. In such conditions, lower voltage and higher current are present. The basic DC-DC converters such as buck, buck-boost, Ćuk, SEPIC and Luo converters [32] cannot provides steep step-down voltage, as required by many modern applications.

In order to provide such an extremely low voltage conversion ratio, these basic converters would have to operate with an extremely small value of the duty cycle,

sometimes smaller than 0.1 in these step-down converters. An extreme duty cycle impairs the efficiency and imposes obstacles for the transient response. The extreme duty cycle may even cause malfunctions at high switching frequency due to the very short conduction time of the active transistors in these step-down converters [171]. What's more, a very good and probably expensive driver circuit is needed when extreme duty cycle is applied. An obvious solution would be the use of transformers to get the desired voltage conversion ratio. However, if the industrial application does not require for DC isolation, a large transformer turns ratio would increase the voltage stress on the primary element, imposing a heavy penalty on the efficiency [48]. Besides, in the on-board aeronautics modern power architectures, smaller-size converters are preferred. The use of a transformer would increase the volume, the losses and the costs. Use of cascade converters for getting the desired voltage ratio is another choice. However, more active switches and diodes are needed, which will increase the controlling complexity and the total cost and decrease the efficiency. Voltage regulators have recently been developed for getting a sub-1 V supply voltage needed in microprocessors [172-175]. These converters, purposely designed for high load current and fast dynamics, are still in the development phase for answering the tough requirements.

The Switched-Capacitor (SC) converters, designed in the 1990s, can provide any step-down voltage conversion ratio [44, 176-177]. However, those converters are complicated, expensive controllers are needed due to many transistors. Large Electromagnetic Interference (EMI) is generated due to large di/dt challenges in the charging path of the capacitors. Switched-Capacitor (SC) and Switched-Inductor (SI) dual structures are defined in [48]. These cells can provide a steeper step-down or step-up voltage ratio. Integration of an SC cell and a classical buck converter comes to correct the drawbacks of the pure SC converters. It contains only one switch which needs a much simpler control circuit and is more adequate for an on-board module. Moreover, the presence of inductors in its structure cancels the large input current ripple of the SC converters and the induced EMI. This new series of SC buck converter, compared with quadratic buck regulator in the terms of conversion ratio and efficiency, are more advantageous [51].

Small volume of capacitors makes it easy to add more capacitors to get even steeper step-down voltage conversion ratio. *N*-Switched-Capacitor buck converter in this chapter can further step down the line voltage, which is inspired by the Voltage-Lift technique [32-43]. The two-Switched-Capacitor buck converter is already analyzed in [51], as for consistency, it is still shown here. The three-Switched-Capacitor and *n*-Switched-Capacitor buck converters will be described and analyzed in this chapter for the first time.

6.2 Two-Switched-Capacitor Buck Converter

The topology of two-Switched-Capacitor buck converter is shown in Fig. 6-1(a). An input inductor is added between the input voltage source and the SC cell to transfer energy and smooth the input current ripple. The two-switched-capacitor cell consists of three diodes (D_1 , D_2 and D_{O1}) and two capacitors (C_1 and C_2) that have the same capacitance value. Fig. 6-1(b)-(e) shows the circuits when the switches are on and off respectively during CCM and DCM. When the circuit works in DCM, there are two situations. The first situation is called DCM1, in which the input inductor current becomes discontinuous. The second situation is called DCM2, in which both the input inductor current and capacitor current become discontinuous [51]. The operating principles and steady state analysis of CCM and DCM are presented in detail below.

(a) Topology

(b) Switching-off time

(c) Switching-on time

(d) DCM1

(e) DCM2

Figure 6-1 Operations of two-Switched-Capacitor buck converter

(a) CCM

(b) DCM1

(c) DCM2

Figure 6-2 Key waveforms of the energy elements in two-Switched-Capacitor buck converter

6.2.1 Two-Switched-Capacitor Buck Converter in CCM

When the main switch S is off, the main diode D and diode D_{O1} in the two-Switched-Capacitor cell conduct. Capacitors C_1 and C_2 are connected in series and charged by the DC source and the input inductor L_{in} , current in inductor L_{in} decreases. The output inductor transfers energy to the load and current in L_O decreases. The operation process is illustrated in Fig. 6-1(b).

When the main switch S is on, the main diode D and diodes D_{O1} in the two-Switched-Capacitor cell are reversed biased, diodes D_1 and D_2 conduct. Input inductor L_{in} absorbs energy from the DC source and current in L_{in} increases. Capacitor C_1 and C_2 are parallel connected and discharge to provide energy together with DC source to output load and output inductor L_O , current in L_O increases. The operation process is illustrated in Fig. 6-1(c). The key waveforms under CCM are shown in Fig. 6-2(a).

As assumed $C_1 = C_2$ we can get

$$V_{C1} = V_{C2} = V_C \quad (6-1)$$

Using the voltage balance technique, currents i_{Lin} decreases and the voltage is $(V_{in} - 2V_C)$ during switching-off. The current decreases and the voltage across the inductor is $(V_{in} - V_C)$ during switching-on. Therefore for inductor L_{in} ,

$$(V_{in} - V_C)uT + (V_{in} - 2V_C)(1-u)T = 0 \quad (6-2)$$

Similarly, for inductor L_O ,

$$(V_C - V_O)uT - V_O(1-u)T = 0 \quad (6-3)$$

Then we can get the voltage transfer gain is

$$M_{2CCM} = \frac{V_O}{V_{in}} = \frac{u}{2-u} \quad (6-4)$$

6.2.2 Two-Switched-Capacitor Buck Converter in DCM1

If L_{in} is discharged completely before the switch turns on, the converter enters a new switching stage as shown in Fig. 6-1(d). The corresponding key waveforms are shown in Fig. 6-2(b). Thus, in DCM1, the converter goes cyclically through three switching stages (Fig. 6-1(b), (d) and (c)). The duration of Fig. 6-1(b) is noted as u_1T .

By using the volt-second balance principles on L_{in} , the following equation can be obtained:

$$(V_{in} - 2V_C)u_1T + (V_{in} - V_C)uT = 0 \quad (6-5)$$

From (6-5), we get

$$V_C = \frac{u + u_1}{u + 2u_1} V_{in} \quad (6-6)$$

By using volt-second balance principles on L_O , the following equation can be obtained:

$$(V_C - V_O)uT - V_O(1 - u)T = 0 \quad (6-7)$$

From (6-7), we can get

$$V_O = uV_C \quad (6-8)$$

The average value of each capacitor current over a full switching period T should be zero, and then we have

$$\frac{I_{in\max}u_1T}{2} + \frac{uT}{2} \left(-\frac{i_O}{2} + \frac{I_{in\max} - i_O}{2} \right) = 0 \quad (6-9)$$

From (6-9), we get

$$I_{in\max} = \frac{2ui_O}{u + 2u_1} \quad (6-10)$$

During switching-on period, the inductor current increase from zero to I_{inmax} , then we have

$$I_{inmax} = \frac{V_{in} - V_c}{L_{in}} uT \quad (6-11)$$

Here we assume

$$i_o = I_o = \frac{V_o}{R} \quad (6-12)$$

From (6-6), (6-8), (6-10), (6-11) and (6-12), we get the voltage transfer gain in DCM1

$$M_{3DCM1} = \frac{V_o}{V_{in}} = \frac{(3uZ_N + \sqrt{3Z_N})u}{3uZ_N + 3\sqrt{3Z_N}} \quad (6-13)$$

The boundary condition for entering switching stage Fig. 6-1(d) after Fig. 6-1(b) is

$$u_1 = 1 - u \quad (6-14)$$

The boundary normalized load between CCM and DCM1 is

$$Z_{3NB1} = \frac{u}{(1-u)(3-2u)} \quad (6-15)$$

6.2.3 Two-Switched-Capacitor Buck Converter in DCM2

At a further reduction of the load current, the circuit can enter DCM2. During the stage Fig. 6-1(c), it can appear a situation in which the three equal capacitor currents drop to zero before the switch S turns off. In other words, after Fig. 6-1(c), it appears the additional switching stage shown in Fig. 6-1(e). The corresponding key waveforms are shown in Fig. 6-2(c). Thus, in DCM2, the converter goes cyclically through four switching stages (Fig. 6-1(b), (d), (c) and (e)). The duration of Fig. 6-1(c) is noted as u_2T .

By using volt-second balance principles on inductor L_{in} , we have

$$(V_{in} - 2V_C)u_1T + (V_{in} - V_C)u_2T = 0 \quad (6-16)$$

From (6-16), we get

$$V_C = \frac{u_2 + u_1}{u_2 + 2u_1} V_{in} \quad (6-17)$$

By using volt-second balance principles on inductor L_O , we have

$$(V_C - V_O)u_2T + (V_{in} - V_O - V_{Lin})(u - u_2)T - V_O(1 - u)T = 0 \quad (6-18)$$

From (6-18), we get

$$V_O = u_2V_C + V_{in}(u - u_2) \quad (6-19)$$

Using again the property that the average capacitor current over a switching cycle is zero

$$I_O u_1 T - \frac{I_O}{2} u_2 T = 0 \quad (6-20)$$

From (6-20), we get

$$u_2 = 2u_1 \quad (6-21)$$

From (6-16) and (6-20), we have

$$V_C = \frac{3}{4} V_{in} \quad (6-22)$$

From (6-19), (6-21) and (6-22), we get the voltage transfer gain in DCM2

$$M_{2DCM2} = \frac{V_O}{V_{in}} = u - \frac{1}{2} u_1 \quad (6-23)$$

The input inductor current decrease from I_O to zero during stage Fig. 6-1(b),

$$I_O = \frac{V_O}{R} = \frac{2V_C - V_{in}}{L_{in}} u_1 T \quad (6-24)$$

From (6-22), (6-23) and (6-24), we get another equation of voltage transfer gain in DCM2

$$M_{2DCM2} = \frac{V_O}{V_{in}} = \frac{1}{2} Z_N u_1 = \frac{Z_N}{1 + Z_N} u \quad (6-25)$$

The boundary condition of DCM1 and DCM2 is

$$u_1 = \frac{u_2}{2} = \frac{u}{2} \quad (6-26)$$

The boundary normalized load between DCM1 and DCM2 is

$$Z_{2NB2} = \frac{3}{2} \quad (6-27)$$

(a) Topology

(b) Switching-off time

(c) Switching-on time

(d) DCM1

(e) DCM2

Figure 6-3 Operations of three-Switched-Capacitor buck converter

(a) CCM

(b) DCM1

(c) DCM2

Figure 6-4 Key waveforms of the energy elements in three-Switched-Capacitor buck converter

6.3 Three-Switched-Capacitor Buck Converter

The topology of three-Switched-Capacitor buck converter is shown in Fig. 6-3(a). An input inductor is added between the input voltage source and the SC cell to transfer energy and smooth the input current ripple. The three-Switched-Capacitor cell consists of six diodes ($D_1, D_2, D_3, D_4, D_{O1}$ and D_{O2}) and three capacitors (C_1, C_2 and C_3) that have the same capacitance value. Fig. 6-3(b)-(e) shows the circuits when the switches are on and off respectively during CCM and DCM. Similar to the two-Switched-Capacitor buck converter in [51], when the circuit works in DCM, there are also two situations. The first situation is called DCM1, in which the input inductor current becomes discontinuous. The second situation is called DCM2, in which both the input inductor current and capacitor current become discontinuous. The operating principles and steady state analysis of CCM and DCM are presented in detail below.

6.3.1 Three-Switched-Capacitor Buck Converter in CCM

When the main switch S is off, the main diode D and diodes D_{O1}, D_{O2} in the three-Switched-Capacitor cell conduct. Capacitors C_1, C_2 and C_3 are connected in series and charged by the DC source and the input inductor L_{in} , current in inductor L_{in} decreases. The output inductor transfers energy to the load and current in L_O decreases. The operation process is illustrated in Fig. 6-3(b).

When the main switch S is on, the main diode D and diodes D_{O1}, D_{O2} in the three-Switched-Capacitor cell are reversed biased, diodes D_1, D_2, D_3 and D_4 conduct. Input inductor L_{in} absorbs energy from the DC source and current in L_{in} increases. Capacitor C_1, C_2 and C_3 are parallel connected and discharge to provide energy together with DC source to output load and output inductor L_O , current in L_O increases. The operation process is illustrated in Fig. 6-3(c). The key waveforms under CCM are shown in Fig. 6-4(a).

As assumed $C_1 = C_2 = C_3$ we can get

$$V_{C1} = V_{C2} = V_{C3} = V_C \quad (6-28)$$

Using the voltage balance technique, currents $i_{L_{in}}$ decreases and the voltage is $(V_{in} - 3V_C)$ during switching-off. The current decreases and the voltage across the inductor is $(V_{in} - V_C)$ during switching-on. Therefore for inductor L_{in} ,

$$(V_{in} - V_C)uT + (V_{in} - 3V_C)(1-u)T = 0 \quad (6-29)$$

Similarly, for inductor L_O ,

$$(V_C - V_O)uT - V_O(1-u)T = 0 \quad (6-30)$$

Then we can get the voltage transfer gain is

$$M_{3CCM} = \frac{V_O}{V_{in}} = \frac{u}{3-2u} \quad (6-31)$$

6.3.2 Three-Switched-Capacitor Buck Converter in DCM1

If inductor L_{in} is discharged completely before the switch turns on, the converter enters a new switching stage as shown in Fig. 6-3(d). The corresponding key waveforms are shown in Fig. 6-4(b). Thus, in DCM1, the converter goes cyclically through three switching stages (Fig. 6-3(b), (d) and (c)). The duration of Fig. 6-3(b) is noted as u_1T .

By using the volt-second balance principles on inductor L_{in} , the following equation can be obtained:

$$(V_{in} - 3V_C)u_1T + (V_{in} - V_C)uT = 0 \quad (6-32)$$

From (6-32), we get

$$V_C = \frac{u + u_1}{u + 3u_1} V_{in} \quad (6-33)$$

By using volt-second balance principles on inductor L_O , the following equation can be obtained:

$$(V_C - V_O)uT - V_O(1-u)T = 0 \quad (6-34)$$

From (6-34), we can get

$$V_o = uV_c \quad (6-35)$$

The average value of each capacitor current over a full switching period T should be zero, and then we have

$$\frac{I_{in\max}u_1T}{2} + \frac{uT}{2} \left(-\frac{i_o}{3} + \frac{I_{in\max} - i_o}{3} \right) = 0 \quad (6-36)$$

From (6-36), we get

$$I_{in\max} = \frac{2ui_o}{u + 3u_1} \quad (6-37)$$

During switching-on period, the inductor current increase from zero to $I_{in\max}$, then we have

$$I_{in\max} = \frac{V_{in} - V_c}{L_{in}} uT \quad (6-38)$$

Here we assume

$$i_o = I_o = \frac{V_o}{R} \quad (6-39)$$

From (6-33), (6-35), (6-37), (6-38) and (6-39), we get the voltage transfer gain in DCM1

$$M_{3DCM1} = \frac{V_o}{V_{in}} = \frac{(3uZ_N + \sqrt{3Z_N})u}{3uZ_N + 3\sqrt{3Z_N}} \quad (6-40)$$

The boundary condition for entering switching stage Fig. 6-3(d) after Fig. 6-3(b) is

$$u_1 = 1 - u \quad (6-41)$$

The boundary normalized load between CCM and DCM1 is

$$Z_{3NB1} = \frac{u}{(1-u)(3-2u)} \quad (6-42)$$

6.3.3 Three-Switched-Capacitor Buck Converter in DCM2

At a further reduction of the load current, the circuit can enter DCM2. During the stage Fig. 6-3(c), it can appear a situation in which the three equal capacitor currents drop to zero before the switch S turns off. In other words, after Fig. 6-3(c), it appears the additional switching stage shown in Fig. 6-3(e). The corresponding key waveforms are shown in Fig. 6-4(c). Thus, in DCM2, the converter goes cyclically through four switching stages (Fig. 6-3(b), (d), (c) and (e)). The duration of Fig. 6-3(c) is noted as u_2T .

By using volt-second balance principles on inductor L_{in} , we have

$$(V_{in} - 3V_C)u_1T + (V_{in} - V_C)u_2T = 0 \quad (6-43)$$

From (6-43), we get

$$V_C = \frac{u_2 + u_1}{u_2 + 3u_1} V_{in} \quad (6-44)$$

By using volt-second balance principles on inductor L_O , we have

$$(V_C - V_O)u_2T + (V_{in} - V_O - V_{Lin})(u - u_2)T - V_O(1-u)T = 0 \quad (6-45)$$

From (6-45), we get

$$V_O = u_2V_C + V_{in}(u - u_2) \quad (6-46)$$

Using again the property that the average capacitor current over a switching cycle is zero

$$I_O u_1 T - \frac{I_O}{3} u_2 T = 0 \quad (6-47)$$

From (6-47), we get

$$u_2 = 3u_1 \quad (6-48)$$

From (6-43) and (6-47), we have

$$V_C = \frac{4}{6}V_{in} \quad (6-49)$$

From (6-46), (6-48) and (6-49), we get the voltage transfer gain in DCM2

$$M_{3DCM2} = \frac{V_O}{V_{in}} = u - u_1 \quad (6-50)$$

The input inductor current decrease from I_O to zero during stage Fig. 6-3(b),

$$I_O = \frac{V_O}{R} = \frac{3V_C - V_{in}}{L_{in}} u_1 T \quad (6-51)$$

From (6-49), (6-50) and (6-51), we get another equation of voltage transfer gain in DCM2

$$M_{3DCM2} = \frac{V_O}{V_{in}} = Z_N u_1 = \frac{Z_N}{1 + Z_N} u \quad (6-52)$$

The boundary condition of DCM1 and DCM2 is

$$u_1 = \frac{u_2}{3} = \frac{u}{3} \quad (6-53)$$

The boundary normalized load between DCM1 and DCM2 is

$$Z_{3NB2} = 2 \quad (6-54)$$

6.4 N-Switched-Capacitor Buck Converter

N-Switched-Capacitor buck converter is shown in Fig. 6-5(a). An input inductor is added between the input voltage source and the SC cell to transfer energy and smooth the

input current ripple. The n-Switched-Capacitor cell consists of $(3n-3)$ diodes ($D_1, D_2, D_3, D_4, \dots, D_{2n-2}$ and $D_{O1}, D_{O2}, D_{O3}, \dots, D_{O(n-1)}$) and n capacitors ($C_1, C_2, C_3, \dots, C_n$) with the same capacitance value. Fig. 6-5(b), (c), (d) and (e) shows the circuits when the switches are on and off respectively during CCM and DCM. Similarly, when the circuit works in DCM, there are also two situations. The first situation is called DCM1, in which the input inductor current becomes discontinuous. The second situation is called DCM2, in which both the input inductor current and capacitor current become discontinuous. The operating principles and steady state analysis of CCM and DCM are presented in detail below.

(a) Topology

(b) Switching-off time

(c) Switching-on time

(c) DCM1

(d) DCM2

Figure 6-5 Operations of n -Switched-Capacitor buck converter

(a) CCM

(b) DCM1

(c) DCM2

Figure 6-6 Key waveforms of the energy elements in n -Switched-Capacitor buck converter

6.4.1 N-Switched-Capacitor Buck Converter in CCM

When the main switch S is off, the main diode D conducts. The diodes D_{O1} , D_{O2} , D_{O3} , ..., $D_{O(n-1)}$ in the n -switched-capacitor cell conduct. Capacitors C_1 , C_2 , C_3 , ..., C_n are connected in series and charged by DC source and input inductor L_{in} , current in inductor L_{in} decreases. The output inductor transfers energy to the load and current in L_O decreases. The operation process is illustrated in Fig. 6-5(b).

When the main switch S is on, the main diode D and diodes D_{O1} , D_{O2} , D_{O3} , ..., $D_{O(n-1)}$ in the n -switched-capacitor cell are reversed biased, diodes D_1 , D_2 , D_3 , D_4 , ..., D_{2n-2} conduct. Input inductor L_{in} absorbs energy from the source and current in L_{in} increases. Capacitor C_1 , C_2 , C_3 , ..., C_n are parallel connected and discharge to provide energy together with DC source to output load and output inductor L_O , current in L_O increases. The operation process is illustrated in Fig. 6-5(c). The corresponding key waveforms are shown in Fig. 6-6(a).

As assumed $C_1 = C_2 = C_3 = \dots = C_n$ we can get

$$V_{C1} = V_{C2} = V_{C3} = \dots = V_C \quad (6-55)$$

Using the voltage balance technique, currents i_{Lin} decreases and the voltage is $(V_{in} - nV_C)$ during switching-off period $(1 - u)T$, where k is the duty cycle. The current decreases and the voltage across the inductor is $(V_{in} - V_C)$ during switching-on period uT , therefore for L_{in} ,

$$(V_{in} - V_C)uT + (V_{in} - nV_C)(1 - u)T = 0 \quad (6-56)$$

Similarly, for inductor L_O ,

$$(V_C - V_O)uT - V_O(1 - u)T = 0 \quad (6-57)$$

Then we can get the voltage transfer gain is

$$M_{nCCM} = \frac{V_O}{V_{in}} = \frac{u}{n - (n - 1)u} \quad (6-58)$$

6.4.2 N-Switched-Capacitor Buck Converter in DCM1

If L_{in} is discharged completely before the switch turns on, the converter enters a new switching stage, as shown in Fig. 6-5(d). The corresponding key waveforms are shown in Fig. 6-6(b). Thus, in DCM1, the converter goes cyclically through three switching stages (Fig. 6-5(b), (d) and (c)). The duration of Fig. 6-5(b) is noted as u_1T .

By using the volt-second balance principles on inductor L_{in} , the following equation can be obtained:

$$(V_{in} - nV_C)u_1T + (V_{in} - V_C)uT = 0 \quad (6-59)$$

From (6-59), we get

$$V_C = \frac{u + u_1}{u + nu_1} V_{in} \quad (6-60)$$

By using the volt-second balance principles on inductor L_O , the following equation can be obtained:

$$(V_C - V_O)uT - V_O(1 - u)T = 0 \quad (6-61)$$

From (6-61), we get

$$V_O = uV_C \quad (6-62)$$

The average value of each capacitor current over a full switching period T should be zero, and then we have

$$\frac{I_{in\max}u_1T}{2} + \frac{uT}{2} \left(-\frac{i_O}{n} + \frac{I_{in\max} - i_O}{n} \right) = 0 \quad (6-63)$$

From (6-63), we get

$$I_{in\max} = \frac{2ui_O}{u + nu_1} \quad (6-64)$$

During switching-on period, the inductor current increase from zero to I_{inmax} , then we have

$$I_{inmax} = \frac{V_{in} - V_C}{L_{in}} uT \quad (6-65)$$

We assume

$$i_o = I_o = \frac{V_o}{R} \quad (6-66)$$

From (6-60), (6-62), (6-64), (6-65) and (6-66), we get the voltage transfer gain in DCM1

$$M_{nDCM1} = \frac{V_o}{V_{in}} = \frac{\left[2Z_N n(n-1)u - Z_N(n-3) + \sqrt{\left[Z_N(n-3) \right]^2 + 8Z_N(n-1)n} \right] u}{2Z_N n(n-1)u - Z_N(n-3) + n\sqrt{\left[Z_N(n-3) \right]^2 + 8Z_N(n-1)n}} \quad (6-67)$$

The boundary condition for entering switching stage Fig. 6-5(d) after Fig. 6-5(b) is

$$u_1 = 1 - u \quad (6-68)$$

The boundary normalized load between CCM and DCM1 is

$$Z_{nNB1} = \frac{2u}{(n-1)(1-u)[n-(n-1)u]} \quad (6-69)$$

6.4.3 N-Switched-Capacitor Buck Converter in DCM2

At a further reduction of the load current, the circuit can enter DCM2. During the stage Fig. 6-5(c), it can appear a situation in which the n equal capacitor currents drop to zero before the switch S turns off. In other words, after Fig. 6-5(c), it appears the additional switching stage Fig. 6-5(e). The corresponding key waveforms are shown in Fig. 6-6(c). Thus, in DCM2, the converter goes cyclically through four switching stages (Fig. 6-5(b), (d), (c) and (e)). The duration of Fig. 6-5(c) is noted as u_2T .

By using volt-second balance principles on inductor L_{in} , we have

$$(V_{in} - nV_C)u_1T + (V_{in} - V_C)u_2T = 0 \quad (6-70)$$

From (6-70), we have

$$V_C = \frac{u_2 + u_1}{u_2 + nu_1} V_{in} \quad (6-71)$$

By using volt-second balance principles on inductor L_O , we have

$$(V_C - V_O)u_2T + (V_{in} - V_O - V_{Lin})(u - u_2)T - V_O(1 - u)T = 0 \quad (6-72)$$

From (6-72), we have

$$V_O = u_2V_C + V_{in}(u - u_2) \quad (6-73)$$

Using again the property that the average capacitor current over a switching cycle is zero, there is

$$I_O u_1 T - \frac{I_O}{n} u_2 T = 0 \quad (6-74)$$

From (6-74), we have

$$u_2 = nu_1 \quad (6-75)$$

From (6-71) and (6-75), we have

$$V_C = \frac{n+1}{2n} V_{in} \quad (6-76)$$

From (6-73), (6-75) and (6-76), we have

$$M_{nDCM2} = \frac{V_O}{V_{in}} = u - \frac{n-1}{2} u_1 \quad (6-77)$$

The input inductor current decrease from I_O to zero during stage Fig. 6-5(b),

$$I_O = \frac{V_O}{R} = \frac{nV_C - V_{in}}{L_{in}} u_1 T \quad (6-78)$$

From (6-76), (6-77) and (6-78), we get another equation of voltage transfer gain in DCM2

$$M_{nDCM2} = \frac{V_O}{V_{in}} = \frac{n-1}{2} Z_N u_1 = \frac{Z_N}{1+Z_N} u \quad (6-79)$$

The boundary condition of DCM1 and DCM2 is

$$u_1 = \frac{u_2}{n} = \frac{u}{n} \quad (6-80)$$

The boundary normalized load between DCM1 and DCM2 is

$$Z_{nNB2} = \frac{n+1}{n-1} \quad (6-81)$$

The main characteristics of the *n*-Switched-Capacitor buck converters are summarized in Table 6-1. It can be seen that they can deeply step down the voltage. Compared with the cascade buck converter, *n*-Switched-Capacitor buck converter only has one active switch, which need simpler controlling algorithm. Also, the total volume will be smaller, which will increase the power density. Apparently, the *n*-switch-capacitor converters are economically and efficiently competitive.

Table 6-1 Main characteristics of the *n*-Switched-Capacitor buck converters

<i>n</i>	M_{CCM}	M_{DCM1}	M_{DCM2}	Z_{NB1}	Z_{NB2}
2	$\frac{u}{2-u}$	$\frac{[(4u+1)Z_N + \sqrt{Z_N^2 + 16Z_N}]u}{(4u+1)Z_N + 2\sqrt{Z_N^2 + 16Z_N}}$	$\frac{Z_N}{1+Z_N}u$	$\frac{2u}{(1-u)(2-u)}$	3
3	$\frac{u}{3-2u}$	$\frac{(3uZ_N + \sqrt{3Z_N})u}{3uZ_N + 3\sqrt{3Z_N}}$	$\frac{Z_N}{1+Z_N}u$	$\frac{u}{(1-u)(3-2u)}$	2
<i>n</i>	$\frac{u}{n-(n-1)u}$	$\frac{[2Z_N n(n-1)u - Z_N(n-3) + \sqrt{[Z_N(n-3)]^2 + 8Z_N(n-1)n}]u}{2Z_N n(n-1)u - Z_N(n-3) + n\sqrt{[Z_N(n-3)]^2 + 8Z_N(n-1)n}}$	$\frac{Z_N}{1+Z_N}u$	$\frac{2u}{(n-1)(1-u)[n-(n-1)u]}$	$\frac{n+1}{n-1}$

6.5 Case Study

To verify the design and calculation results, three-Switched-Capacitor buck converter is set up in laboratory environment and investigated in this case study. The main parameters are chosen as $V_{in} = 12\text{ V}$, $L_{in} = 20\text{ }\mu\text{H}$, $L_O = 20\text{ }\mu\text{H}$, $C_1 = C_2 = C_3 = C_O = 50\text{ }\mu\text{F}$, $R = 0.1\text{ }\Omega \sim 4\text{ }\Omega$ and $f = 50\text{ kHz}$. In the hardware testing circuits, the N-channel MOSFET 2SK2267 is selected as the power switches S , the drain-source on resistance is $8\text{ m}\Omega$. This circuit can be applied to automobile power supply system, for example the input voltage is $12\text{ V}/100\text{ W}$, there are several devices' required voltage is just 5 V or less. Here, we only describe the topology of the basic n -Switched-Capacitor circuits. Experimental results of the case study of three-Switched-Capacitor buck converter in the following parts will verify our theoretical analysis in the former sections.

6.5.1 CCM Operation of Three-Switched-Capacitor Buck Converter

The performances of three-Switched-Capacitor buck converter under CCM with $R = 0.1\text{ }\Omega$ and $u = 0.5$ are investigated. The input inductor current variation is about 3 A and the output inductor current variation is about 200 mA . These match the theoretical results obtained by using volt-second balance principle in (6-29) and (6-30) and the waveforms are shown in Fig. 6-7(a). The three switched capacitors can be regarded as one integrated cell. During switching-on, the three capacitors are parallel connected and the voltage across the cell is equal to single capacitor voltage about 6 V . During switching-off, the three capacitors are series connected and then the voltage across the SC cell is the summation of the three capacitor voltages which is about 18 V . the power switch stress during switching-off is 18 V , which is equal to the voltage across SC cell. The waveforms are shown in Fig. 6-7(b).

(a) Input inductor current and output inductor current

(b) Voltage stresses across the switch S and the whole three-Switched-Capacitor cell

(c) Output voltage when the duty cycle u changes from 0.5 to 0.6 at 0.014s and from 0.6 to 0.3 at 0.022s

Figure 6-7 Three-Switched-Capacitor buck converter performances in CCM with $R = 0.1 \Omega$ and $u = 0.5$

It can be seen from Fig. 6-7(c), the output voltage of three-Switched-Capacitor buck converter is 2.9 V with $R = 0.1 \Omega$ and $u = 0.5$. At $t = 0.014$ s, the duty cycle step up from 0.5 to 0.6, the output voltage then changes to 3.8 V then transient response is smooth and

fast. At $t = 0.022$ s, the duty cycle steps down from 0.6 to 0.3, the respective output voltage then turns to 1.4 V. From these result it can be verified the three-Switched-Capacitor buck converter can step down the voltage by following (6-31) in CCM.

6.5.2 DCM1 Operation of Three-Switched-Capacitor Buck Converter

The performances of three-Switched-Capacitor buck converter under DCM1 with $R = 1 \Omega$ and $u = 0.5$ are investigated. The input inductor current variation is about 2.5 A and the output inductor current variation is about 200 mA. There is a small section with zero input inductor current at the end of each switching-off interval. These match the theoretical results obtained by using volt-second balance principle in (6-32) and (6-34) and the waveforms are shown in Fig. 6-8(a). The three switched capacitors can be regarded as one integrated cell. During switching-on, the three capacitors are parallel connected and the voltage across the cell is equal to single capacitor voltage about 7 V. During switching-off, the three capacitors are series connected and then the voltage across the SC cell is the summation of the three capacitor voltages which is about 21 V. When the input inductor current becomes zero, the voltage across the whole SC cell has a rapid drop to a lower value, about 12 V. The power switch stress during switching-off is equal to the voltage across the SC cell. The waveforms are shown in Fig. 6-8(b).

The three-Switched-Capacitor buck converter output voltage is 3.4 V with $R = 1 \Omega$ and $u = 0.5$. At $t = 0.014$ s, the duty cycle step up from 0.5 to 0.6, the output voltage then changes to 4.1 V then transient response is smooth and fast. At $t = 0.022$ s, the duty cycle steps down from 0.6 to 0.3, the respective output voltage then turns to 1.9 V. the waveforms are shown in Fig. 6-8(c). From these result it can be verified the three-Switched-Capacitor buck converter can step down the voltage by following (6-40) in DCM1.

(a) Input inductor current and output inductor current

(b) Voltage stresses across the switch S and the whole three-Switched-Capacitor cell

(c) Output voltage when the duty cycle u changes from 0.5 to 0.6 at 0.014s and from 0.6 to 0.3 at 0.022s

Figure 6-8 Three-Switched-Capacitor buck converter performances in DCM1 with $R = 1 \Omega$ and $u = 0.5$

6.5.3 DCM2 Operation of Three-Switched-Capacitor Buck Converter

The performances of three-Switched-Capacitor buck converter under DCM2 with $R = 4 \Omega$ and $u = 0.5$ are investigated. The input inductor current variation is about 2.6 A and

the output inductor current variation is about 200 mA. Besides there is an small section with zero input inductor current at the end of each switching-off interval, the input inductor current slope is different from the former value during a small section of the switching-on period. During that time, the capacitors do not provide energy to the load and then there is a drop of the input inductor voltage. These match the theoretical results obtained by using volt-second balance principle in (6-43) and (6-45) and the waveforms are shown in Fig. 6-9(a). The three switched capacitors can be regarded as one integrated cell. During switching-on, the three capacitors are parallel connected and the voltage across the cell is equal to single capacitor voltage about 9 V. During switching-off, the three capacitors are series connected and then the voltage across the SC cell is the summation of the three capacitor voltages which is about 27 V. When the input inductor current becomes zero, the voltage across the whole SC cell has a rapid drop to a lower value, about 12 V. The power switch stress during switching-off is equal to the voltage across the SC cell. The waveforms are shown in Fig. 6-9(b).

The three-Switched-Capacitor buck converter output voltage is 4.3 V with $R = 4 \Omega$ and $u = 0.5$. At $t = 0.014$ s, the duty cycle step up from 0.5 to 0.6, the output voltage then changes to 5.3 V then transient response is smooth and fast. At $t = 0.022$ s, the duty cycle steps down from 0.6 to 0.3, the respective output voltage then turns to 2.9 V. the waveform is shown in Fig. 6-9(c). From these result it can be verified the three-Switched-Capacitor buck converter can step down the voltage by following (6-52) in CCM2.

(a) Input inductor current and output inductor current

(b) Voltage stresses across the switch S and the whole three-Switched-Capacitor cell

(c) Output voltage when the duty cycle u changes from 0.5 to 0.6 at 0.014s and from 0.6 to 0.3 at 0.022s

Figure 6-9 Three-Switched-Capacitor buck converter performances in DCM2 with $R = 4 \Omega$ and $u = 0.5$

6.6 Conclusion

A series of n -Switched-Capacitor buck converters are described in this chapter. They have the advantages of smaller size and easier controlling algorithm compared to cascade buck converter, higher efficiency compared to the quadratic converter reported in former literature. The most important is that they can provide even steeper step-down voltage to satisfy some extreme low-voltage high-current applications. These converters can work under different DCM situations with different loads and the voltage transfer gains will be a little higher than that in CCM. A case study of three-switched-capacitor buck converter is conducted to verify the theoretical analysis.

Chapter 7 Conclusions and Recommendations

7.1 Conclusions

The thesis gives an in-depth research on advanced DC-DC power conversion topologies. In Chapter 1, the background of the research work is introduced. The basic issues of DC-DC power conversion techniques are then reviewed, which are topologies, modeling and control, in Chapter 2. The detailed research work is given in Chapter 3-6, respectively.

In Chapter 3, a reduced-order state space modeling and an improved Sliding Mode controller are described which can apply to advanced high-order DC-DC converters. Positive output super-lift converter is taken as an example. The reduced-order state space modeling can describe the converter's main characteristics satisfactorily. The application of the improved SM controller may be a good alternative in circumstances requiring good regulation properties and excellent dynamical response features. It will be beneficial for enriching the understanding and promoting the practical applications of high-order complex DC-DC converters.

In Chapter 4, a series of Voltage-Lift Split-Inductor-type boost converter is described. Much higher voltage transfer gain is obtained due to the implementation of VL technique. They have symmetric structures, which make them understood easily. This series of converters overcome the effects of parasitic parameters and avoid taking an extremely high duty cycle value. The VL cells can be made into modules and decrease the volume and increase the power density and energy efficiency. The main characteristics of the series of converters are analyzed and then verified through experiments.

In Chapter 5, the concepts of the Voltage-Lift-type SI cells are described, which can step up the output voltages of DC-DC converters to a higher level. Analysis of hybrid boost converters and hybrid POEL converters integrated with this series of SI cells are

given to show that the described VL-type SI cells can be widely applied to those circuits that need strong DC-DC boost abilities.

In Chapter 6, a series of n -Switched-Capacitor buck converters are described. The most important feature is that they can provide even steeper step-down voltage to satisfy some extreme low-voltage high-current applications. These converters can work under different DCM situations with different loads and the voltage transfer ratios will be a little higher than that in CCM. A case study of three-Switched-Capacitor buck converter is conducted to verify the theoretical analysis.

Following the theoretical analysis in Chapter 3 to 6, both simulation and experimental verification have been carried out. It can be seen that all the simulation results are identically matching the theoretical results. The reason is that the theoretical analyses are conducted without consideration of the parasitic parameters and also in the simulation. However, in the practical experimental circuits, the parasitic parameters exists, which affect the performance of the circuits. Nevertheless, the experimental results are quite close to the theoretical and simulation results. All DC-DC topologies described in the thesis could be widely used in the areas of computer peripheral circuits, medical equipment, semiconductor industry, especially in applications that require high voltage transfer gains. They enrich the family of advanced DC-DC switching power converters and are helpful for the practical industrial applications and engineering education. The analytical methods used here provide a useful and convenient way for analyzing and utilizing these advanced DC-DC topologies.

7.2 Recommendations

All DC-DC topologies described in the thesis are circuit prototypes. The discussion in this thesis could explain main fundamental principles of these topologies. More research work needs to be performed in future, and it can be classified into the following parts:

- (1) Protection circuits for complex DC-DC converters including various snubber circuits and soft switching techniques.

(2) Efficiency improvement of complex DC-DC converters.

(3) Advance digital controllers.

All analytical methods and corresponding concepts used in this thesis are based on the averaging techniques, which ignore the nonlinear characteristics of switching circuits.

The following research work could be classified into two parts:

(1) To develop a more convenient analytical method that could unify the CCM and DCM theories.

(2) To analyze nonlinear phenomena in the advanced DC-DC converters.

The DC-DC converters and controllers built in this thesis are only the simple laboratorial version for scientific research. Above-mentioned contents should be considered for practical applications, and they will be carried out step by step in the future. The protection and reliability are critical and need further considerations if the advanced converters and controllers are intended for practical applications. In addition, EMC and EMI are another two factors which need to be investigated.

Bibliography

- [1] M.H. Rashid, "Power electronics: circuits, devices and applications", Prentice-Hall, Englewood Cliffs, NJ, USA, 1993, second edition.
- [2] N. Mohan, T.M. Undeland and W.P. Robbins "Power electronics: converters, applications and design", John Wiley and Sons, Inc., 2004, third edition.
- [3] F.L. Luo and H. Ye, "Advanced dc-dc converters", CRC Press, USA, 2004.
- [4] F.L. Luo, H. Ye and M.H. Rashid, "Digital power electronics and applications", Elsevier Academic Press, USA, 2005.
- [5] F.L. Luo and H. Ye, "Essential dc-dc converters", Taylor and Francis Group LLC, USA, 2005.
- [6] F.L. Luo and H. Ye, "Advanced multi-quadrant operation dc-dc converters", Taylor and Francis Group LLC, USA, 2005.
- [7] C.C. Marouchos, "The switching function: analysis of power electronic circuit", IEE, UK, 2006.
- [8] C.K. Tse, "Complex behavior of switching power converters", CRC Press, USA, 2004.
- [9] J. C. Bennett, "Practical computer analysis of switch mode power supplies", CRC Press, USA, 2005.
- [10] R.D. Middlebrook and S. Ćuk, "Advances in switched-mode power conversion-Vols. I and II", TESLaco, Pasadena, CA, 1981, first edition.
- [11] "World switching mode power supply market", Frost & Sullivan, Mountain View, CA, USA, c1997.
- [12] H. Matsuo and K. Harada, "The cascade connection of switching regulators", IEEE Transactions on Industry Applications, vol. 12, no. 2, pp. 192-198, Mar. 1976.
- [13] D. Maksimovic and S. Ćuk, "Switching converters with wide DC conversion range", IEEE Transactions on Power Electronics, vol. 6, no. 1, pp.151-157, Jan. 1991.
- [14] J.J. Chen and B.R. Lin, "Analysis and implementation of a soft switching converter with high voltage conversion ratio", IET Proceedings on Power Electronics, vol. 1, no.1, Mar. 2008.

- [15] K.W.E. Cheng, "Zero-current-switching switched-capacitor converters", IEE Proceedings on Electric Power Applications, vol. 148, no.5, pp. 403-409, Sept. 2001.
- [16] Y.F. Liu and P.C. Sen, "New Class-E DC-DC converter topologies with constant switching frequency", IEEE Transactions on Industry Applications, vol. 32, no. 4, pp.961-969, Aug. 1996.
- [17] B.G. Dobbs and P.L. Chapman, "A multiple-input dc-dc converter topology", IEEE Power Electronics Letters, vol. 1, no. 1, pp. 6-9, Mar. 2003.
- [18] T. Sato, T. Nabeshima, K. Nishijima, T. Nakano and M. Sekine, "DC-DC converters with ripple cancel circuit", in Proceedings of International Telecommunications Energy Conference (INTELEC'2005), pp. 527-532, Sept. 18-22, 2005.
- [19] I. Barbi and R. Gules, "Isolated dc-dc converters with high-output voltage for TWTA telecommunication satellite applications", IEEE Transactions on Power Electronics, vol. 18, no. 4, pp. 975-984, Jul. 2003.
- [20] H. Tao, A. Kotsopoulos, J.L. Duarte and M.A.M. Hendrix, "Family of multiport bidirectional dc-dc converters", IEE Proceedings on Electric Power Applications, vol. 153, no. 3, pp. 451-458, May 2006.
- [21] David J. Perreault and John G. Kassakian, "Distributed interleaving of paralleled power converters", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol. 44, no. 8, pp. 728-734, Aug. 1997.
- [22] S.K. Mazumder, "Stability analysis of parallel dc-dc converters", IEEE Transactions on Aerospace and Electric Systems, vol. 42, no. 1, pp. 50-69, Jan. 2006.
- [23] K.D.T. Ngo and R. Webster, "Steady-state analysis and design of a switched capacitor dc-dc converter", IEEE Transactions on Aerospace and Electronic Systems, vol. 30, no. 1, pp. 92-101, Jan. 1994.
- [24] G.Y. Zhu and A. Ioinovici, "Switched-capacitor power supplies: dc voltage ratio, efficiency, ripple, regulation", in Proceedings of IEEE International Symposium on Circuits and Systems, 1996, pp. 553-556.
- [25] J.A. Morales-Saldana, E.E.C. Gutierrez and J. Leyva-Ranos, "Modelling of switch-mode dc-dc cascade converters", IEEE Transactions on Aerospace and Electric Systems, vol. 38, no. 1, pp. 295-299, Jan. 2002.

- [26] M. Veerachary, Tomonobu Senju and Katsumi Uezato, "Signal flow graph modelling of interleaved buck converters", *International Journal of Circuit Theory and Applications*, vol. 31, no. 3, pp. 249-264, May 2003.
- [27] M. Veerachary, "Modelling and analysis of cascade step-down converters", *IEE Proceedings on Electric Power Applications*, vol. 151, no. 1, pp. 41-50, Jan. 2005.
- [28] M. Veerachary, "Signal flow graph modelling of multi-state boost dc-dc converters," *IEE Proceedings on Electric Power Applications*, vol. 152, no. 5, pp. 583-589, Sept. 2004.
- [29] T.F. Wu and T.H. Yu, "Unified Approach to developing single-stage power converters", *IEEE Transactions on Aerospace and Electric Systems*, vol. 34, no. 1, pp. 211-223, Jan. 1998.
- [30] T.F. Wu and S.A. Liang, "A systematic approach to developing single-stage soft switching PWM converters", *IEEE Transactions on Power Electronics*, vol. 16, no. 5, pp.581-593, Sept. 2001.
- [31] T.F. Wu, S.A. Liang and Y.K. Chen, "A structural approach to synthesizing soft switching PWM converters", *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp.38-43, Jan. 2003.
- [32] F.L. Luo, "Positive output Luo converters: voltage lift technique", *IEE Proceedings on Electric Power Applications*, vol. 146, no. 4, pp. 415-432, July 1999.
- [33] F.L. Luo, H. Ye and M.H. Rashid, "Multiple quadrant operation Luo-converters", *IEE Proceedings on Electric Power Applications*, vol. 149, no. 1, pp. 9-18, Sept. 2002.
- [34] F.L. Luo and H. Ye, "Positive output cascade boost converters", *IEE Proceedings on Electric Power Applications*, vol. 151, no. 5, pp. 590-606, Sept. 2004.
- [35] F.L. Luo and H. Ye, "Positive output super-lift converters", *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 105-113, Jan. 2003.
- [36] F.L. Luo and H. Ye, "Negative output super-lift converters", *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1113-1121, Sept. 2003.
- [37] F.L. Luo and H. Ye, "Ultra-Lift Luo-Converter", *IEE Proceedings on Electric Power Applications*, vol. 152, no. 1, pp. 27-32, Jan. 2005.
- [38] Y. He, and F.L. Luo, "Sliding-mode control for dc-dc converters with constant switching frequency", *IEE Proceedings on Control Theory and Applications*, vol. 53, no.1, pp. 37-45, Jan. 2006.

- [39] I. Yamamoto, K. Matsui, and M. Matsuo, "A comparison of various DC-DC converters and their application to power factor correction," in Proceedings of Power Conversion Conference (PCC'2002), pp. 128-135, Apr. 2-5, 2002.
- [40] R. Kayalvizhi, S.P.Natarajan, V. Kavitharajan, and R. Vijayarajeswaran, "TMS320F2407 DSP based fuzzy logic controller for negative output Luo re-lift converter: design, simulation and experimental evaluation," in Proceedings of International Conference on Power Electronics and Drive Systems (PEDS'2005), pp.1228-1233, Nov. 28-Dec. 1, 2005.
- [41] R. Kayalvizhi, S.P. Natarajan, and P. Padmaloshani, "Development of neuro controller for negative output self-lift Luo converter," in Proceedings of The first IEEE Conference on Industrial Electronics and Applications (ICIEA'2006), pp.517-522, May 24-26, 2006.
- [42] M. Zhu and F.L. Luo, "Series SEPIC implementing voltage lift technique for DC-DC power conversion", IET Proceedings on Power Electronics, vol. 1, no. 1, pp. 109-121, Mar. 2008.
- [43] M. Zhu and F.L. Luo, "Voltage-lift-type $\hat{C}\hat{u}\hat{k}$ converters: topology and analysis", IET Proceedings on Power Electronics, vol. 2, no. 2, pp. 178-191, Mar. 2009.
- [44] A. Ioinovici, "Switched-capacitor power electronics circuits", IEEE Circuits and Systems Magazine, vol. 1, no. 4, pp. 37-42, 2001.
- [45] B. Axelrod, Y. Berkovich and A. Ioinovici, "Hybrid switched-capacitor- $\hat{C}\hat{u}\hat{k}$ /Zeta/Sepic converters in step-up mode", in Proceedings of IEEE International Symposium on Circuits and Systems, 2005, pp. 1310-1313.
- [46] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched-capacitor (SC)/switched inductor (SL) structures for getting hybrid step-down $\hat{C}\hat{u}\hat{k}$ /Sepic/Zeta converters", in Proceedings of IEEE International Symposium on Circuits and Systems, 2006, pp. 5063-5066.
- [47] F.L. Luo and H. Ye, "Positive output multiple-lift push-pull switched-capacitor Luo-converters", IEEE Transactions on Industrial Electronics, vol. 51, no. 3, pp. 594-602, Jun. 2004.
- [48] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc PWM converters", IEEE

- Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 55, no. 2, pp. 687-696, , 2008.
- [49] J. Chen and A. Ioinovici, "Switching-mode DC-DC converter with switched-capacitor-based resonant circuit", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 43, no.11, pp. 933-938, 1996.
- [50] G. Zhu, A. Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters", Journal of Circuits, Systems and Computers, vol. 7, no. 2, pp. 69-71, 1997.
- [51] B. Axelrod, Y. Berkovich, S. Tapuchi and A. Ioinovici, "Single-stage single-switch switched-capacitor Buck/Buck-boost-Type converter", IEEE Transactions on Aerospace and Electronic Systems, vol. 45, no. 2, pp. 419-430, 2009.
- [52] R. D. Middlebrook and S. Cúk, "A general unified approach to modeling switching-converter power stages", International Journal of Electronics, vol. 42, no. 6, pp. 521 – 550, 1977.
- [53] A. J. Forsyth and S. C. Molloy, "Modeling and control of DC-DC converters", Power Engineering Journal, vol. 12, no. 5, pp. 229 – 236, Oct. 1998.
- [54] R.D. Middlebrook and S. Cúk, "A general unified approach to modeling switching converter power stages", in Proceedings of IEEE Power Electronics Specialists Conference, pp. 18-34, 1976.
- [55] M. Shoyama, Y. Hamafuku, N. Matsuzaki and T. Ninomiya, "Simplification of transfer function in switching converter with general load impedance", in Proceedings of International Conference on Power Electronics and Drive Systems (PEDS' 1995), pp. 155-161, Feb. 21-24, 1995.
- [56] J. Sun, D.M. Mitchell, M.F. Greuel, P.T. Krein and R.M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode", IEEE Transactions on Power Electronics, vol. 16, no. 4, pp. 482-492, Jul. 2001.
- [57] A. Pietkiewicz and D. Tollik, "A unified topological approach to modeling of switching dc-dc converters", in Proceedings of IEEE Power Electronics Specialists Conference, 1985, pp. 535-543.
- [58] J.P. Xu, "An analytical technique for the analysis of switching dc-dc converters", in Proceedings of IEEE International Symposium on Circuits and Systems, 1991, pp. 1212-1215.

- [59] B. Lehman and R.M. Bass, "Switching frequency dependent averaged models for PWM DC-DC converters", *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 89-98, Jan. 1996.
- [60] J.P. Xu and C.Q. Lee, "A Unified Averaging Technique for the Modeling of Quasi-Resonant Converters", *IEEE Transactions on Power Electronics*, vol. 13, no. 3, pp. 556-563, May 1998.
- [61] Q.M. Li, Fred C. Lee and Milan M. Jovanovic, "Large-signal transient analysis of forward converter with active-clamp reset", *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 15-24, Jan. 2002.
- [62] Seth R. Sanders, J. Mark Noworolski, Xianjun Z. Liu and George C. Verghese, "Generalized averaging method for power conversion circuits", *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp.333-340, Apr. 1991.
- [63] J. Mahdavi, A. Emaadi, M. D. Bellar and M. Ehsani, "Analysis of power electronic converters using the generalized state-space averaging approach", *IEEE Transactions on Circuits and Systems*, vol. 44, no. 8, pp.767-770, Aug. 1997.
- [64] A. J. Forsyth, S. H. Ma and Y. T. Leung, "Dynamic characteristics of the class E DC/DC converter using sampled-data modeling", *IEE Proceedings on Electric Power Applications*, vol. 139, no. 4, pp. 409-417, July 1992.
- [65] C. K. Tse and K. M. Adams, "Quasi-linear modeling and control of dc-dc converters", *IEEE Transactions on Power Electronics*, vol. 7, no. 2, pp. 315-323, Apr. 1992.
- [66] S. Banerjee and G. C. Verghese, "Nonlinear phenomena in power electronics attractors, bifurcations, chaos and nonlinear control", the Institute of Electrical and Electronics Engineers, IEEE press, New York, USA, c2001.
- [67] A. K. S. Bhat, "A generalized steady-state analysis of resonant converters using two-port model and Fourier-series approach", *IEEE Transactions on Power Electronics*, vol. 13, no. 1, pp. 142-151, Jan. 1998.
- [68] A. K. S. Bhat and F. D. Tan, "A unified approach to characterization of PWM and quasi-PWM switching converters: topological constraints, classification, and synthesis", *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 719-726, Oct. 1991.

- [69] A. K. S. Bhat, "A unified approach for the steady-state analysis of resonant converters", *IEEE Transactions on Industrial Electronics*, vol. 38, no. 4, pp. 251-259, Aug. 1991.
- [70] A. J. Forsyth, G. A. Ward and S. V. Mollov, "Extended fundamental frequency analysis of the LCC resonant converter", *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1286-1292, Nov. 2003.
- [71] F. L. Luo, "Energy factor and mathematical modeling for power dc/dc converters", *IEE proceedings on Electric Power Applications*, vol. 152, no. 2, pp. 191-198, Apr. 2005.
- [72] P. Li and B. Lehman, "Performance prediction of dc-dc converters with impedance as loads", *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 201 – 209, Jan. 2004.
- [73] D. Czarkowski and M. K. Kazimierczuk, "Circuit models of PWM dc-dc converters", in *proceedings of the IEEE National Aerospace and Electronics Conference (NAECON' 1992)*, vol. 1, pp. 407 – 413, May 18-22. 1992.
- [74] K.M. Smedley and S. Ćuk, "Switching flow-graph nonlinear modeling technique", *IEEE Transactions on Power Electronics*, vol. 9, no. 4, pp. 405-413, Jul. 1994.
- [75] Y.H. Ma and K.M. Smedley, "Switching flow graph nonlinear modelling method for multi-state switching converters", *IEEE Transactions on Power Electronics*, vol. 12, no. 5, pp. 854-861, Sept. 1997.
- [76] C.J. Gajanayake, D.M. Vilathgamuwa and P.C. Loh, "Small-signal and signal flow-graph modelling of switched Z-source impedance network", *IEEE Power Electronics Letters*, vol. 3, no. 3, pp. 111-116, Sept. 2005.
- [77] M. Zhu, "Advanced DC-DC Power Conversion Topologies and Mathematical Analytical Methods", NTU PhD dissertation, 2009.
- [78] Y. He, "Advanced Control Methodologies of DC-DC Converters", NTU PhD dissertation, 2008.
- [79] T. G. Habetler and R. G. Harley "Power electronic converter and system control", in *proceedings of the IEEE Power Electronics Technology*, vol. 89, no. 6, pp. 913- 925, June 2001.

- [80] G. Escobar, R. Ortega, H. Sira-Ramirez, J-P. Vilain and I. Zein, “An experimental comparison of several nonlinear controllers for power converters”, *IEEE Control Systems Magazine*, vol. 19, no. 1, pp. 66 – 82, Feb. 1999.
- [81] Marian K. Kazimierczuk, “Pulse-width modulated DC-DC power converters”, John Wiley & Sons, USA, 2008
- [82] Robert Mammano, “Switching Power Supply Topology Voltage Mode vs. Current Mode”, Unitrode design note, DN-62.
- [83] Lloyd Dixon, “Average Current Mode Control of Switching Power Supplies”, unitrode application note, U-14.
- [84] R.B. Ridley, “A new, continuous-time model for current-mode control [power convertors]”, *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271 – 280, 1991.
- [85] W.Tang, F.C. Lee and R.B. Ridley, “Small-signal modeling of average current-mode control”, *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 112 – 119, Apr. 1993.
- [86] D. Liebal, P. Vijayraghavan and N. Sreenath, “Control of dc-dc buck-boost converter using exact linearization techniques”, in *Proceeding of 24th Annual IEEE Power Electronics Specialists Conference (PESC’93)*, pp. 203 – 207, Jun. 20-24, 1993.
- [87] H. Sira-Ramirez and M. Ilic, “Exact linearization in switched mode dc to dc power converters”, *International Journal of Control*, vol. 50, no. 2, pp. 511 – 524, Aug. 1989.
- [88] H. Sira-Ramirez, “Switched control of bilinear circuits via pseudo-linearization”, *IEEE Transactions on Circuits and Systems*, vol. 36, no. 6, pp. 858-865, Dec. 1989.
- [89] S. R. Sanders, G. C. Verghese and D. E. Cameron, “Nonlinear control of switching power converters”, *Control Theory and Advanced Technology*, vol. 5, no. 4, pp. 601-627, Dec. 1989.
- [90] S. R. Sanders and G. C. Verghese, “Lyapunov-based control for switched power converters”, *IEEE Transactions on Power Electronics*, vol. 7, no. 1, pp. 17-24, Jan. 1992.
- [91] H. Sira-Ramirez, R. Ortega, R. Perez-Moreno and M. Garcia-Esteban, “A sliding mode controller-observer for dc-to-dc power converters: a passivity approach”, in *proceedings of 34th Conference on Decision and Control*, vol. 04, pp. 3379-3384, Dec. 1995.

- [92] H. Sira-Ramirez, M. Rios-Bolivar and A. S. I. Zinober, "Adaptive input-output linearization for PWM regulation of dc-to-dc power converters", in proceedings of American Control Conference 1995, vol. 1, pp. 81-85, Oct. 1995.
- [93] H. Sira-Ramirez and P. Lischinsky-Arenas, "Differential algebraic approach in nonlinear dynamical compensator design for dc-to-dc power converters", International Journal of Control, vol. 54, no. 1, pp. 111-133, Jan. 1991.
- [94] H. Sira-Ramirez, R. Tarantino-Alvarado and O. Llanes-Santiago, "Adaptive feedback stabilization in PWM-controlled dc-to-dc power supplies", International Journal of Control, vol. 57, no. 3, pp. 599-625, July 1993.
- [95] G. Ioannidis, A. Kandianis and S. N. Manias, "Novel control design for the buck converter", IEE proceedings on Electric Power Applications, vol. 145, no. 1, pp. 39-47, Jan. 1998.
- [96] M. K. Kazimierczuk and L. A. Starman, "Dynamic performance of PWM dc-dc boost converter with input voltage feedforward control", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 46, no. 12, pp. 1473-1481, Dec. 1999.
- [97] M. K. Kazimierczuk and A. J. Edstrom, "Open-loop peak voltage feedforward control of PWM converter", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 47, no. 5, pp. 740 – 746, May 2000.
- [98] K. M. Smedley and S. Cúk, "One-cycle control of switching converters", IEEE Transactions on Power Electronics, vol. 10, no. 6, pp. 625-633, Nov. 1995.
- [99] K. M. Smedley and S. Cúk; "One-cycle control of switching converters", in proceedings of 22nd Annual IEEE Power Electronics Specialists Conference (PESC'1991), pp. 888-896, Jun. 24-27, 1991.
- [100] K. M. Smedley and S. Cúk, "Dynamics of one-cycle controlled Cúk converters", IEEE Transactions on Power Electronics, vol. 10, no. 6, pp. 634-639, Nov. 1995.
- [101] Z. B. Hu, B. Zhang and W. H. Deng, "Feasibility study on one cycle control for PWM switched converters", in proceedings of 35th IEEE Power Electronics Specialists Conference (PESC '2005), vol. 2, pp. 3359-3365, Jun. 2005.
- [102] Y. Wang and S. Shen, "Research on one-cycle control for power converters", in proceedings of 5th World Congress on Intelligent Control and Automation, pp. 74- 77, June 15-19, 2004.

- [103] D. S. Ma, W. Ki and C. Tsui, "An integrated one-cycle control Buck converter with adaptive output and dual loops for output error correction", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 140-149, January 2004.
- [104] H. Sira-Ramirez, "Nonlinear P-I controller design for switch mode dc-to-dc power converters", *IEEE Transactions on Circuits and Systems*, vol. 38, no. 4, pp. 410- 417, Apr. 1991.
- [105] K. M. Passino and S. Yurkovich, "Fuzzy control", Addison-Wesley Longman, Inc, Menlo Park, CA, USA, c1998.
- [106] W. C. So, C. K. Tse and Y. S. Lee, "Development of a fuzzy logic controller for dc/dc converters: design, computer Simulation, and experimental evaluation", *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 24-32, Jan. 1996.
- [107] T. Gupta, R. R. Boudraux, R. M. Nelms and J. Y. Hung, "Implementation of a fuzzy controller for dc-dc converters using an inexpensive 8-bit Micro-Controller", *IEEE Transactions on Industry Electronics*, vol. 44, no. 5, pp. 661 – 669, 1997.
- [108] B. R. Lin and C. Hua, "Buck/boost converter control with fuzzy logic approach", in *proceedings of International Conference on Industrial Electronics, Control and Instrumentation (IECON' 93)*, vol. 2, pp. 1342 – 1346, Nov. 15-19, 1993.
- [109] K. Viswanathan, D. Srinivasan and R. Oruganti, "A universal fuzzy controller for a nonlinear power electronic converter", in *Proceedings of the 2002 IEEE International Conference on Fuzzy Systems*, vol. 1, pp. 46-51, May 12-17, 2002.
- [110] A. G. Perry, G. Feng, Y. F. Liu and P. C. Sen, "A new sliding mode like control method for Buck converter", in *proceedings of 35th Annual IEEE Power Electronics Specialists Conference (PESC '2004)*, vol. 5, pp. 3688-3693, Jun. 20-25, 2004.
- [111] P. Mattavelli, L. Rosserro, G. Spiazzi and P. Tenti, "General-purpose fuzzy controller for dc-dc converters", *IEEE Transactions on Power Electronics*, vol. 12, no. 1, pp. 79-86, Jan. 1997.
- [112] L. K. Wong, F. H. F. Leung, P. K. S. Tam and K. W. Chan, "Design of an analog fuzzy logic controller for a PWM boost converter", in *proceedings of the 23rd International Conference on Industrial Electronics, Control and Instrumentation (IECON'97)*, vol. 1, pp. 360 – 363, Nov. 9-14, 1997.
- [113] V. Itkis, "Control systems of variable structure", John Wiley, New York, USA, c1976.

- [114] V. I. Utkin, "Sliding modes and their application in variable structure systems", MIR Publishers, Moscow, c1974, in Russia.
- [115] J. Y. Hung, W. Gao and J. C. hung, "Variable structure control: a survey", IEEE Transactions on Industrial Electronics, vol. 40, no. 1, pp. 2-22, Feb. 1993.
- [116] T. Skvarenina, "Power electronics handbook", CRC Press LLC, NY, USA, c2002.
- [117] J. E. Slotine and W. Li, "Applied nonlinear control", Englewood Cliffs, N.J. Prentice Hall, c1991.
- [118] V. I. Utkin, "Sliding modes in control optimization", Berlin, Germany, Springer-Verlag, c1992.
- [119] V. I. Utkin, "Sliding mode control design principles and applications to electric drives", IEEE Transactions on Industrial Electronics, vol. 40, no. 1, Feb. 1993, pp. 23-36.
- [120] V. I. Utkin and A. Sabanovic, "Sliding modes applications in power electronics and motion control systems", in proceedings of the IEEE International Symposium on Industrial Electronics, ISIE '99, vol. 1, pp. TU22 - TU31, Jul. 12-16, 1999.
- [121] R. Venkataramanan, A. Sabanovic and S. Cúk, "Sliding mode control of dc-to-dc converters", in proceedings of 11th Conference on Industrial Electronics, Control and Instrumentation (IECON'85), pp. 251-258, Nov. 1985.
- [122] H. Sira-Ramirez, G. Escobar and R. Ortega, "On passivity-based sliding mode control of switched dc-to-dc power converters", in proceedings of 35th Conference on Decision and Control, TM17, pp. 2525-2526, Dec. 1996.
- [123] H. Sira-Ramirez, "Sliding motions in bilinear switched networks", IEEE Transactions on Circuits and Systems, vol. CAS-34, no. 8, pp. 919-933, Aug. 1987.
- [124] H. Sira-Ramirez, "A geometric approach to pulse-width modulated control in nonlinear dynamical systems", IEEE Transactions on Automatic Control, vol. 34, no. 2, pp. 184-187, Feb. 1989.
- [125] H. Sira-Ramirez, "Sliding mode control of dc-to-dc converters via extended linearization", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 41, no. 10, pp. 652-661, Oct. 1994.
- [126] M. Oppenheimer, I. Husain, M. Elbuluk and J. A. De Abreu-Garcia, "Sliding mode control of the Cúk converter", in proceedings of IEEE Power Electronics Specialists Conference, vol. 2, pp. 1519-1526, Jun. 1996.

- [127] E. Fossas, L. Martinez, and J. Ordinas, "Sliding mode control reduces audio-susceptibility and load perturbation in the Cúk converter", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 39, no. 10, pp. 847-849, Oct. 1992.
- [128] L. Martinez-Salamero, J. Calvente, and R. Giral, and A. Poveda, and E. Fossas, "Analysis of a bidirectional coupled-inductor Cúk converter operating in sliding mode", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 4, pp. 355-363, Apr. 1998.
- [129] S. P. Huang, H. Q. Xu and Y. F. Liu, "Sliding-mode controlled Cúk switching regulator with fast response and first-order dynamic characteristic", *IEEE Power Electronics Specialists Conference (PESC '1989)*, vol. 1, pp. 124-129, Jun. 26-29, 1989.
- [130] L. Malesani, L. Rossetto; G. Spiazzi and P. Tenti, "Performance optimization of Cúk converters by sliding-mode control", *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 302-309, May 1995.
- [131] P. Mattavelli, L. Rossetto; G. Spiazzi and P. Tenti, "General-purpose sliding-mode controller for dc/dc converter applications", in *proceeding of IEEE Power Electronics Specialists Conference (PESC'93)* pp. 609-615, Jun. 20-24, 1993.
- [132] P. Mattavelli, L. Rossetto and G. Spiazzi, "Small-signal analysis of dc-dc converters with sliding mode control", *IEEE Transactions on Power Electronics*, vol. 12, no. 1, pp. 96-102, Jan. 1997.
- [133] B. J. Cardoso Fo, A. F. Moreira, B. R. Menezes and P. C. Cortizo, "Analysis of switching frequency reduction methods applied to sliding mode controlled DC-DC converters", in *proceedings of Applied Power Electronics Conference (APEC'92)*, pp. 403-410, Feb. 23-27, 1992.
- [134] V. M. Nguyen and C. Q. Lee, "Tracking control of Buck converter using sliding-mode with adaptive hysteresis", in *proceedings of IEEE Power Electronics Specialist Conference (PESC '1995)*, vol. 2, pp. 1086-1093, Jun. 18-22, 1995.
- [135] V. M. Nguyen and C. Q. Lee, "Indirect implementations of sliding-mode control law in Buck-type converters", in *proceedings of IEEE Applied Power Electronics Conference*, vol. 1, pp. 111-115, Mar. 1996.

- [136] L. G. Shiau and J. L. Lin, "Direct and indirect SM control schemes for dc-dc switching converters", in proceedings of the 36th SICE Annual Conference. International Session Papers, pp. 1289-1294, Jul. 29-31, 1997.
- [137] J. Mahdavi and A. Emadi, "Sliding-mode control of PWM Cúk converter", in proceedings of Sixth International Conference on Power Electronics and Variable Speed Drives, pp. 372-377, Sept. 1996.
- [138] J. Mahdavi, A. Emadi and H. A. Toliyat, "Application of state space averaging method to sliding mode control of PWM dc/dc converters", in proceedings of IEEE Industry Applications Society Annual Meeting (IAS '1997), pp. 820-827, 1997.
- [139] A. Kolesnikov, G. Veselov, A. Kolesnikov, A. Monti, F. Ponci, E. Santi and R. Dougal, "Synergetic synthesis of DC-DC boost converter controllers: theory and experimental analysis", in proceedings of 17th Applied Power Electronics Conference and Exposition (APEC'2002), vol. 1, pp. 409-415, Mar. 10-14, 2002.
- [140] E. Santi, A. Monti, D. H. Li, K. Proddutur and R. Dougal, "Synergetic control for dc-dc Boost converter: implementation options", IEEE Transactions on Industry Applications, vol. 39, no. 6, pp. 1803-1813, 2003.
- [141] K. K. S. Leung and H. S. H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converter", IEEE Power Electronics Letters, vol. 2, no. 2, pp. 63-67, Jun. 2004.
- [142] D. Biel, E. Fossas, F. Guinjoan and R. Ramos, "Sliding mode control of a buck converter for AC signal generation", in Proceedings of the 1998 IEEE International Symposium on Circuits and Systems (ISCAS'98), vol. 6, pp. 450-453, May. 31-Jun. 3, 1998.
- [143] D. Biel, E. Fossas, F. Guinjoan and R. Ramos, "Sliding mode control of a boost-buck converter for AC signal tracking task", in proceedings of the 1999 IEEE International Symposium on Circuits and Systems, vol. 5, pp. 242-245, 1999.
- [144] E. Fossas and J. M. Olm, "Generation of signals in a buck converter with sliding mode control", in Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'94), vol. 6, pp. 157-160, May 30 –Jun.2, 1994.
- [145] E. Vidal-Idiarte, L. Martinez-Salamero, F. Guinjoan, J. Calvente and S. Gomariz, "Sliding and fuzzy controller of a Boost converter using an 8-bit microcontroller", IEE proceedings on Electric Power Applications, vol. 151, no. 1, pp. 5-11, Jan. 2003.

- [146] V. S. C. Raviraj and P. C. Sen, "Comparative study of proportional-integral, sliding mode, and fuzzy logic controllers for power converters", *IEEE Transactions on Industry applications*, vol. 33, no. 2, pp. 518-523, Mar. 1997.
- [147] K. J. Astrom and B. Wittenmark, "Adaptive control", Addison-Wesley, Second Edition, c1995.
- [148] C. K. Tse and K. M. Adams, "An adaptive control for dc-dc converters", in *proceedings of 21st IEEE Power Electronics Specialists Conference (PESC'90)*, pp. 213-218, Jun. 11-14, 1990.
- [149] T. C. T. Ng, F. H. F. Leung and P. K. S. Tam, "A simple adaptive control strategy for regulated switching dc-dc converters based on grid-point concept", in *proceedings of the 27th IEEE Power Electronics Specialists Conference (PESC'96)*, vol. 2, pp. 1494-1498, Jun. 23-27, 1996.
- [150] A. Balestrino, A. Landi, and L. Sani, "Cúk converter global control via fuzzy logic and scaling factors", *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 406-413, Mar. 2002.
- [151] S. Hiti and D. Boroyevich, "Control of boost converter with adjustable output Voltage and unknown resistive load", in *proceedings of the 25th IEEE Power Electronics Specialists Conference (PESC'94)*, vol. 1, pp. 294-300, Jun. 20-24, 1994.
- [152] S. C. Tan, Y. M. Lai, M. K. H. Cheung and C. K. Tse, "An Adaptive sliding mode controller for Buck converter in continuous conduction mode", in *proceedings of IEEE Applied Power Electronics Conference and Exposition*, pp. 1395-1400, Feb. 2004.
- [153] S. C. Tan, Y. M. Lai, M. K. H. Cheung and C. K. Tse, "On the practical design of a sliding mode voltage controlled Buck converter", *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 425-437, Mar. 2005.
- [154] R. Naim, G. Weiss and S. Ben-Yaakov, " H_{∞} control applied to Boost power converters", *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 677-683, Jul. 1997.
- [155] B. M. Chen, "Robust and H_{∞} control", Springer Press, c2000.
- [156] R. Naim, G. Weiss and S. Ben-Yaakov, " H_{∞} control of boost converters: comparison to voltage mode, feedforward and current mode controls", in *proceedings of 26th IEEE Power Electronics Specialists Conference*, vol. 2, pp. 1327-1332, Jun. 1995.

- [157] A. Kugi and K. Schlacher, "Nonlinear H_{∞} -controller design for a dc-to-dc power converter", *IEEE Transactions on Control Systems Technology*, vol. 7, no. 2, pp. 230-237, Mar. 1999.
- [158] J. Matas, L. G. Vicuna, O. Lopez, M. Lopez and M. Castilla, "Discrete sliding mode control of a Boost converter for output voltage tracking", in *proceedings of 8th International Conference on Power Electronics and Variable Speed Drives*, pp. 351-354, Sep. 18-19, 2000.
- [159] S. Muthu and J. M-S. Kim, "Discrete-time robust sliding mode control for switching power converters", in *proceedings of 28th Annual IEEE Power Electronics Specialists Conference (PESC'97)*, vol. 1, pp. 210-216, Jun. 22-27, 1997.
- [160] R. Orosco and N. Vazquez, "Discrete sliding mode control for dc/dc converters", in *proceedings of 7th IEEE International Power Electronics Congress (CIEP'2000)*, pp. 231-236, Oct. 15-19, 2000.
- [161] G. Venkataramanan, and D. M. Divan, "Discrete time integral sliding mode control for discrete pulse modulated converters", in *proceedings of 21st Power Electronics Specialists Conference (PESC '90)*, pp. 67-73, Jun. 11-14, 1990.
- [162] D. Czarowski, L. R. Pujara, and M. K. Kazimierzuk, "Robust stability of state-feedback control of PWM dc-dc push-pull converter", *IEEE Transactions on Industrial Electronics*, vol. 42, no. 1, pp. 108-111, Feb. 1995.
- [163] J. Leyva-Ramos, J. A. Morales-Saldana and M. Martinex-Cruz, "Robust stability analysis for current-programmed regulators", *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 1138-1145, Oct. 2002.
- [164] S. C. Tan and Y. M. Lai, "Constant-frequency reduced-state sliding mode current controller for Ćuk converters", *IET Proceedings on Power Electronics*, vol. 4, no. 1, pp. 466-477, 2008.
- [165] Y. He and F. L. Luo, "Design and analysis of adaptive sliding-mode-like controller for DC-DC converters", *IEE Proceedings on Electric Power Applications*, vol. 153, no. 3, pp. 401-410, 2006.
- [166] L.-S. Yang, T.-J. Liang and J.-F. Chen, "Transformerless dc-dc converters with high step-up voltage gain", *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3144-3152, 2009.

- [167] S.-C. Tan, Y.M. Lai and C.K. Tse, "Indirect Sliding Mode Control of Power Converters Via Double Integral Sliding Surface", *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 600-611, 2008.
- [168] M. Zhu, F.L. Luo and Y. He, "Remaining inductor current phenomena of complex dc-dc converters in discontinuous conduction mode: general concepts and case study", *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 1014-1019, 2008.
- [169] M. Zhu and F.L. Luo, "Transient analysis of multi-state dc-dc converters using system energy characteristics", *International Journal of Circuit Theory and Applications*, vol. 36, no. 3, pp. 327-344, 2008.
- [170] M. Zhu, Y. He and F.L. Luo, "A novel modeling method for multi-state boost converters", in *Proceedings of IEEE Conference on Industrial Technology (ICIT'05)*, pp. 1-6, Dec. 2005.
- [171] J. Wei, K. Yao, M. Xu and F.C. Lee, "Applying transformer concept to nonisolated voltage regulators significantly improves the efficiency and transient response", in *Proceedings of 34th IEEE Power Electronics Specialist Conference (PESC '03)*, vol. 4, pp. 1599-1604, June 2003.
- [172] W. Jia and F.C. Lee, "Two novel soft-switched, high frequency, high-efficiency, non-isolated Voltage Regulators-the phase-shift buck converter and the matrix-transformer phase-buck converter", *IEEE Transactions Power Electronics*, vol. 20, no. 2, pp. 292-299, 2005.
- [173] K. Yao, M. Yu and F.C. Lee, "A novel winding coupled-buck converter for high-frequency, high step-down DC/DC conversion", in *Proceedings of IEEE 33rd Annual Power Electronics Specialists Conference (PESC'02)*, vol. 2, pp. 651-656, 2002.
- [174] Y. Panov and M.M. Jovanovic, "Design and performance evaluation of low-voltage/high-current DC/DC on-board modules", *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 26-33, 2001.
- [175] P. Xu, W. Jia, K. Yao, M. Yu and F.C. Lee, "Investigation of candidate topologies for 12 V VRM", in *Proceedings of 17th Annual IEEE Applied Power Electronics Conference and Exposition (APEC'02)*, vol. 2, pp. 686-692, 2002.
- [176] S.V. Cheong, H. Chung, A. Ioinovici, "Inductorless DC-to-DC converter with high power density", *IEEE Transactions on Industrial Electronics*, vol. 41, no. 2, pp. 208-215, 1994.

- [177] G. Zhu, A. Ioinovici, “DC-to-DC converter with no magnetic elements and enhanced regulation”, IEEE Transactions on Aerospace and Electronic Systems, vol. 33, no. 2, pp. 499-506, 1997.

Appendix A Main Analysis Principles in DC-DC Converters

To perform a theoretical analysis for a given DC-DC topology, we usually assume that the circuit is operating in the steady state. This means that: (1) the duty cycle U is held constant at a fixed switching frequency for a long time (over a large number of switching cycles). (2) the current and voltage waveforms become periodic with switching cycle T , i.e. $i((n + 1)T) = i(nT)$ and $v((n + 1)T) = v(nT)$. There are two important principles that describe the steady-state performance of DC-DC converters: *volt-second balance* of the inductor and *charges balance* of the capacitors. These two principles are used throughout the thesis to analyze the steady-state performance of various new DC-DC topologies and a brief introduction will be given below.

A.1 Volt-Second Balance Principle

The steady-state condition imposes a periodic behavior of the current flowing through the inductor. Thus, we have

$$i_{L(nT)} = i_{L((n+1)T)} \quad (\text{A-1})$$

Also,

$$v_L = L \frac{di_L}{dt} \quad (\text{A-2})$$

Integration over one switching cycle yields:

$$i_{L((n+1)T)} - i_{L(nT)} = \frac{1}{L} \int_{nT}^{(n+1)T} v_L(t) dt \quad (\text{A-3})$$

Since the left-hand side of (A-3) is zero, then the right-hand side must be zero too, i.e.,

$$0 = \frac{1}{L} \int_{nT}^{(n+1)T} v_L(t) dt \quad (\text{A-4})$$

Equation (A-4) states that the integral of the voltage across the inductor along a switching cycle must be zero for the steady state. This property is termed *volt-second balance* principle in the steady state.

A.2 Charges Balance Principle

A similar analysis can be applied to the capacitor. The relationship between the capacitor voltage and the current flowing through capacitor is defined by:

$$i_C = C \frac{dv_C}{dt} \quad (\text{A-5})$$

The integration of (A-5) over one switching cycle yields:

$$v_{C((n+1)T)} - v_{C(nT)} = \frac{1}{C} \int_{nT}^{(n+1)T} i_C(t) dt \quad (\text{A-6})$$

Since the left-hand side of (A-6) is zero, then the right-hand side must also be zero, i.e.,

$$0 = \frac{1}{C} \int_{nT}^{(n+1)T} i_C(t) dt \quad (\text{A-7})$$

Equation (A-7) states that the integral of the current flowing through the capacitor along a switching cycle must be zero for the steady state. This property is termed *charges balance* principle in the steady state.

Appendix B Routh's Stability Criterion

Consider a closed-loop transfer function where the a_i 's and b_i 's are real constants and $m \leq n$.

$$H(s) = \frac{b_0 s^m + b_1 s^{m-1} + \cdots + b_{m-1} s + b_m}{a_0 s^n + a_1 s^{n-1} + \cdots + a_{n-1} s + a_n} = \frac{B(s)}{A(s)} \quad (\text{B-1})$$

An alternative to factoring the denominator polynomial, Routh's Stability criterion, determines the number of closed-loop poles in the right-half s plane. The algorithm for applying Routh's stability criterion is described below, like the stability criterion, requires the order of $A(s)$ to be finite.

Factor out any roots at the origin to obtain the polynomial, and multiply by -1 if necessary, which is shown below with $a_0 \neq 0$ and $a > 0$,

$$a_0 s^n + a_1 s^{n-1} + \cdots + a_{n-1} s + a_n = 0 \quad (\text{B-2})$$

If the order of the resulting polynomial is at least two and any coefficient a_i is zero or negative, the polynomial has at least one root with nonnegative real part. To obtain the precise number of roots with nonnegative real part, proceed as follows. Arrange the coefficients of the polynomial, and values subsequently calculated from them as shown below:

$$\begin{array}{c|cccccc} s^n & a_0 & a_2 & a_4 & a_6 & \cdots \\ s^{n-1} & a_1 & a_3 & a_5 & a_7 & \cdots \\ s^{n-2} & b_1 & b_2 & b_3 & b_4 & \cdots \\ s^{n-3} & c_1 & c_2 & c_3 & c_4 & \cdots \\ s^{n-4} & d_1 & d_2 & d_3 & d_4 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ s^2 & e_1 & e_2 & & & \\ s^1 & f_1 & 0 & & & \\ s^0 & g_0 & & & & \end{array} \quad (\text{B-3})$$

Where the coefficients bi 's are generated until all subsequent coefficients are zero. Similarly, cross multiply the coefficients of the two previous rows to obtain the c_i , d_i , etc. until the n^{th} row of the array has been completed, all of which is shown below.

$$\left\{ \begin{array}{l} b_1 = \frac{a_1 a_2 - a_0 a_3}{a_1} \\ b_2 = \frac{a_1 a_4 - a_0 a_5}{a_1} \\ b_3 = \frac{a_1 a_6 - a_0 a_7}{a_1} \\ \vdots \end{array} \right\}, \left\{ \begin{array}{l} c_1 = \frac{b_1 a_3 - a_1 b_2}{b_1} \\ c_2 = \frac{b_1 a_5 - a_1 b_3}{b_1} \\ c_3 = \frac{b_1 a_7 - a_1 b_4}{b_1} \\ \vdots \end{array} \right\}, \left\{ \begin{array}{l} d_1 = \frac{c_1 b_2 - b_1 c_2}{c_1} \\ d_2 = \frac{c_1 b_3 - b_1 c_3}{c_1} \\ \vdots \end{array} \right\}, \dots$$

Missing coefficients are replaced by zeros. The resulting array is called the Routh array. The powers of s are not considered to be part of the array. We can think of them as labels. The column beginning with a_0 is considered to be the first column of the array.

The Routh array is seen to be triangular. It can be shown that multiplying a row by a positive number to simplify the calculation of the next row does not affect the outcome of the application of the Routh criterion.

Count the number of sign changes in the first column of the array. It can be shown that a necessary and sufficient condition for all roots of (B-2) to be located in the left-half plane is that all the a_i are positive and all of the coefficients in the first column be positive.

Appendix C Author's Publications

- [1] Y. Jiao, F. L. Luo and M. Zhu, "Voltage-Lift-Type Switched-Inductor Cells for Enhancing DC-DC Boost Ability: Principles and Integrations in Luo Converter," IET Proceedings on Power Electronics, vol. 4, no. 1, pp. 131-142, January, 2011.
- [2] Y. Jiao and F. L. Luo, "N-Switched-Capacitor Buck Converter: Topologies and Analysis," IET Proceedings in Power Electronics, vol. 4, no. 3, pp. 332-341, March, 2011.
- [3] Y. Jiao, F. L. Luo and B. K. Bose, "Voltage-Lift Split- Inductor-Type Boost Converter," IET Proceedings in Power Electronics, vol. 4, no. 4, pp. 353-362, April, 2011.
- [4] Y. Jiao, F. L. Luo and M. Zhu, "Generalized Modeling and Sliding Mode Control for N-Cell Cascade Super-lift DC-DC converters," IET Proceedings in Power Electronics, vol. 4, no. 5, pp. 532-540, May, 2011.
- [5] Y. Jiao and F. L. Luo, "An improved sliding mode controller for boost converter in solar energy system," in Proceedings of the 4th IEEE Conference in Industrial Electronics and Applications (ICIEA'2009), pp. 805-810, May 2009.
- [6] Y. Jiao and F. L. Luo, "An improved sliding mode controller for Positive Output Luo Converter," in Proceedings of 35th Annual Conference of IEEE Industrial Electronics Society (IECON'2009), pp. 200-205, Nov. 2009.
- [7] Y. Jiao and F. L. Luo, "Quasi Sliding Mode Controller for Single Phase PFC Boost Converter," in Proceedings of the 5th IEEE Conference in Industrial Electronics and Applications (ICIEA'2010), pp. 2099-2103, Jun. 2010.