Power converter systems for wind generation

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POWER CONVERTER SYSTEMS FOR WIND GENERATION

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Summary

Variable speed, direct-drive, multi-pole permanent magnet synchronous generators are becoming popular in modern wind energy conversion systems mainly due to their low maintenance, high efficiency and grid-code compliance. The back-to-back converter arrangement which comprises a generator-side converter, an intermediate dc-link and a grid-side inverter is inevitable for the integration of such systems into the power grid.

A comprehensive review on possible topologies for the generator-side converter is presented at the beginning of the thesis. This study revealed that the full controlled six switch two-level active rectifier is the most suitable topology for implementing the generator-side converter since it makes both dc-link voltage regulation and sinusoidal phase current impression possible. However, the two-level active rectifier does not meet voltage and power requirements of modern multi-mega-watt wind energy conversion systems. Therefore, in this context, multi-level converter topologies emerged as a potential solution. Among the number of multi-level converter topologies diode-clamped and capacitor-clamped three-level converters are the popular choices for implementing the generator-side converter. Moreover, due to the unidirectional power flow of wind turbines, these topologies can be built with less number of switching devices.

Similarly, three-level converter topologies are used to implement the grid-side inverter as well in modern wind energy conversion systems. Furthermore, the diode-clamped topology is becoming the most popular choice for realizing three-level grid-side inverters. The energy storage interfacing capability of this topology has been investigated in detail in this study. Uneven distribution of space vectors is the biggest challenge with this unique approach which complicates the modulation process. A novel space vector modulation technique has been developed to address this issue.

The other alternative way of constructing three-level converters is the use of the capacitor-clamped topology which is believed to be less reliable and bulky. These disadvantages can overcome by replacing conventional clamping capacitors with supercapacitors which are more reliable and compact in size. Furthermore, these

supercapacitors can be used to absorb short-term wind power fluctuations. Similarly, long-term power fluctuations can be mitigated if the conventional capacitors are replaced with batteries. Problems associated with these approaches are analyzed in detail and suitable modulation and control techniques are proposed with simulation and experimental verifications.

The concept of dual inverter has been identified as an alternative approach to build multilevel inverter systems with low voltage switching devices. A dual inverter is formed by cascading two inverters through open ends of the primary winding of the coupling transformer. The two inverters are named as the main inverter and the auxiliary inverter. The dc-link of the main inverter is connected to the rectified output of the wind turbine generator. The dc-link of the auxiliary inverter can be used to interface an energy storage system such as a battery bank or a supercapacitor bank. This particular idea is tested for four different dual inverter configurations namely: 2x2, 2x3, 3x2 and 3x3.

The 2x2 dual inverter found to be suitable for interfacing both battery and supercapacitor energy storage systems. However, the energy storage system should be rated for the total dc-link voltage of the auxiliary inverter which in turn increases the number of cells or modules to be connected in series. As a result, internal resistance gets increased. The 2x3 dual inverter provides a solution to this issue by reducing the voltage of each ESS module to a half.

The 3x2 dual inverter is proposed to increase the power rating of the main inverter while interfacing a supercapacitor bank through the auxiliary inverter. However, this topology is capable of absorbing only short term power fluctuations. Therefore, a 3x3 dual inverter based direct integration scheme is explored for battery/supercapacitor hybrid energy storage systems which can mitigate both short term and long term power fluctuations. Moreover, it improves the power rating and low voltage ride through capability of the inverter system.

A hybrid cascaded multilevel inverter has been investigated for the possible use in wind energy conversion systems as the grid-side inverter. Furthermore, energy storage interfacing capability of this topology is also investigated. A modified carrier based pulse

width modulation method and a novel space vector modulation method are proposed to generate undistorted current even under unbalanced supercapacitor voltage conditions. Efficacy of the proposed scheme, modulation methods and control techniques are validated through simulation and experimental results.

A matrix converter topology for the grid connection of large, direct driven, split winding PMSG based wind turbine generator systems is proposed to eliminate dc-link capacitors and thus to improve the reliability. The proposed matrix converter system consists of large number of low power converter modules which are fed from isolated three-phase generator windings. Outputs of matrix converter modules are connected in series to increase the output voltage and thus eliminate the need of a coupling step-up transformer. Therefore, the proposed system would be an attractive solution for the need of transformer-less, high voltage, highly-reliable and compact converter system for nacelle installation in offshore wind power systems. The modulation process of the proposed modular matrix converter, grid-side controller and proper multilevel voltage waveform generation through modified PWM switching are investigated. Simulation results are presented to show the efficacy of the proposed system, modulation method and the controller.

Power fluctuations caused by random wind changes create serious stability issues on the grid voltage, especially at increased levels of penetration. The solution to this issue lies on reactive power compensation. Modern wind turbine generators, equipped with full scale back-to-back converters, are capable of supplying both active and reactive power to the grid and thus help to stabilize the grid voltage.

However, the reactive power capability of individual wind turbine generator varies with available wind power and has certain limitations such as rated voltage and current of the converter. Therefore, individual turbine cannot supply the total reactive power demand all the time. This makes the conventional centralized reactive power compensation inevitable even in modern wind farms, but at reduced capacity. Therefore, a novel centralized reactive power compensator topology is presented in this thesis with corresponding modulation and control strategies.

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List of Abbreviations

BESS	Battery energy storage system
CBPWM	Carrier based pulse width modulation
CCM	Continuous conduction mode
CMC	Cascaded multilevel converter
DCM	Discontinuous conduction mode
DFIG	Doubly fed induction generator
DG	Distributed generation
DSP	Digital signal processor
EMA	Exponential moving average
EMF	Electromotive force
EMI	Electromagnetic interference
EMS	Energy management system
ESI	Electronic smoothing inductor
ESS	Energy storage system
ETO	Emitter turn-off thyristor
FACTS	Flexible ac transmission systems
FPGA	Field programmable gate array
FSC	Full scale converter
GTO	Gate turn-off thyristor
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
LPF	Low pass filter
LVRT	Low voltage ride through
MER	Magnetic energy recovery
MERS	Magnetic energy recovery switch
MPP	Maximum power point
MPPT	Maximum power point tracking
MW	Mega Watt
NPC	Neutral point clamped
PCC	Point of common coupling
PLL	Phase lock loop

PMSG	Permanent magnet synchronous generator
PV	Photovoltaic
PWM	Pulse width modulation
RSS	Redundant state selection
SESS	Supercapacitor energy storage system
SoC	State of charge
SPWM	Sinusoidal pulse width modulation
STATCOM	Static synchronous compensator
SVC	Static var compensator
SVM	Space vector modulation
SVPWM	Space vector pulse width modulation
THD	Total harmonic distortion
THPWM	Third harmonic injection pulse width modulation
TSR	Tip speed ratio
VAR	Volt ampere reactive
VSI	Voltage source inverter
WECS	Wind energy conversion system
WTG	Wind turbine generator

List of Symbols

A	Area
A_m	Magnitude of the reference voltage vector
C, C_1, C_2, C_3	Capacitor
C_p	Turbine power coefficient
C_f	Filter capacitance
D	Diode
E	Electromotive force
E_k	Kinetic energy of wind
E_x ($x= a, b$ or c)	Induced voltage of PMSG
f	Frequency
f_{sw}	Switching frequency
i_d	d axis current
i_q	q axis current
i_x ($x= a, b$ or c)	Three phase current
i_{xs} ($x= a, b$ or c)	Inverter output current
J	Inertia
L	Inductance
L_d	d axis inductance of the PMSG
L_q	q axis inductances of the PMSG
m	Mass
p	Number of pole pairs
P	Active power
$P_{battery}$	Battery power
P_{in}	Input power
P_{out}	Output power
P_{sc}	Supercapacitor power
P_w	Wind power
Q	Reactive power
r	Amplitude of the reference voltage vector
R	Resistance

R_s	Stator resistance
S	Complex power
S_x ($x= a, b$ or c)	Switching states of inverter/converter legs a, b and c
t_x ($x= 0, 1$ or 2)	Switching time for voltage vectors
T_e	Electrical torque
T_m	Mechanical torque
T_s	Sampling time
v_d	d axis voltage
v_q	q axis voltage
v_{ref}	Reference voltage
v_s	Magnitude of the voltage vector
v_x ($x= a, b$ or c)	Three phase voltage
v_{xs} ($x= a, b$ or c)	Inverter output voltage
V	Voltage
V_{avg}	Average voltage
V_{max}	Maximum voltage
V_{min}	Minimum voltage
V_p	Peak voltage
V_{sc}	Supercapacitor voltage
V_w	Wind speed
X	Reactance
α	Load voltage advance angle
β	Blade pitch angle
δ_α	Delay angle of the reference voltage vector
θ	Rotating angle of reference phase
λ	Tip speed ratio
ρ	Air density
φ_d	Magnetic flux component in d axis
φ_q	Magnetic flux components in q axis
φ_m	Flux produced by the permanent magnets of the PMSG
ω_0	Angular frequency of the grid voltage
ω_e	Electrical rotational speed
ω_m	Mechanical rotational speed

Chapter 1 Introduction

1.1 Background and motivation

The phrase ‘industry rotates around the axis of oil’ was true in the past. It is true even in present times. However, in the future, within 40 years as experts predict, this control will gradually move towards alternative energy technologies, mainly due to two reasons. The first and utmost reason is the depletion of existing fossil fuel deposits. Secondly, fossil fuel burning creates long term environmental issues such as global warming, acidification, air pollution, water pollution, damage to land surface and weakening the protective ozone layer [1]-[10]. Out of these, global warming, which is due to excessive carbon emission, is the major concern among scientists and environmentalists. As a result, carbon reduction commitments were imposed on governments to reduce fossil fuel consumption by 20% by 2020 [7]-[15].

The prevailing strategies to achieve this target are the increased use of nuclear power and renewable energy [1] [2]. However, nuclear power is more controversial than any other source of power due to safety reasons and political issues [3]. Consequently, renewable energy sources such as wind, solar, hydro, biomasses, biofuels and hydrogen fuel cells received enormous attention during the last two decades [1]-[12], [21]-[25]. Each of these energy sources has their own characteristics, advantages and limitations. Therefore, different applications use different sources, and sometimes combinations of two or more sources.

However, in the case of grid connected operation wind energy can play the leading role owing to its vast availability and relatively simple, efficient and matured conversion process. All the other renewable energy sources are far behind wind energy and would require more technological advancements to compete with wind and fossil fuels [10], [24]. And hence, wind energy conversion receives huge attention and support all over the world. As a result, worldwide installed wind power capacity doubles in each year showing an exponential growth. Therefore, wind is considered as the fastest growing and most promising renewable energy source to achieve the 2020 target [8]-[18].

Available power in wind increases as the cube of wind speed, which varies continuously throughout the day. On the other hand, power captured by the wind turbine varies with the tip speed ratio (TSR - speed at the tip of the blade/wind speed). Therefore, for maximum power extraction from the wind, speed of the turbine should vary in proportion to the wind speed in a way that the optimum TSR is maintained all the time [21] [22]. Since the extraction of maximum possible power from the wind is extremely important for the better utilization of wind energy conversion systems, almost all the modern wind turbines operate in the variable speed mode.

The doubly fed induction generator (DFIG) is widely used in variable-speed wind generation systems [22]–[25]. In a typical DFIG based wind energy conversion system (WECS) stator windings are directly connected to the grid. Speed of the rotor is controlled by adjusting the electrical torque via the rotor side converter. Power rating of the rotor side converter can be reduced to 30% of the rated power of the WECS [22] [23]. However, WECSs based on DFIGs still require gearboxes due to the fact that low-speed multi-pole DFIGs are not technically feasible [26] [27]. Moreover, the slip rings and brushes, which need regular maintenance, make the DFIG rather unsuitable for applications where logistic could be a problem, e.g., offshore wind parks [28] [29]. Furthermore, new transmission system operator grid codes pose more stringent requirements in terms of low voltage ride through (LVRT) and even request injection of large amount of reactive power to sustain the voltage profile under fault conditions [28]–[32]. These requirements challenge the use of DFIGs. As a result, DFIG's share in the wind energy market is decreasing.

Nowadays, direct-drive multi-pole permanent magnet synchronous generators (PMSG) are dominating the market mainly due to their low maintenance, high efficiency and grid code compliance [23], [28] [29]. However, back-to-back converter systems are inevitable for grid integration of PMSG based WECSs [23], [28] [29], [33], [34]. As they are required to be rated to the same power level of the generator, full-scale converters with higher ratings are essential for modern multi-megawatt wind generation systems [28] [29]. Since traditional two-level converters do not meet these requirements, high power multi-level converters are essential to realize the back-to-back converter system [33]–[36].

This is the motivation behind the research on new high-power multi-level converter topologies for wind generation.

Power fluctuations caused by random wind changes is another significant issue, especially at increased levels of penetration. A promising solution to this problem is the use of energy storage [37]-[40]. Furthermore, the combination of battery and supercapacitor energy storage systems (ESSs) is greatly appreciated by experts as it provide an excellent match that can cover a wide range of power and energy requirements [41]-[43]. However, additional converters used to interface them to WECSs increase system cost, complexity and power losses [37], [44] [45]. A direct integration method, which is free from these drawbacks and beneficial to both industry and academia, is yet to be reported. This motivated us to research on grid-side inverter based direct integration schemes for battery/supercapacitor energy storage systems.

As wind is random in nature, the power output of wind generators are expected to have short-term and long-term fluctuations. In particular, short-term fluctuations of the wind power output can cause serious voltage variations at the point of common coupling (PCC) in wind farms [46]-[48]. Such voltage variations can effectively be compensated with appropriate injection of reactive power either by individual wind turbine generators (WTGs) or by a centralized unit [46]-[50]. For the centralized unit static synchronous compensators (STATCOMs) are suitable due to their fast dynamic response. Furthermore, a storage element connected at the dc-link of the STATCOM in the form of battery or supercapacitor can also help alleviate such short-term power oscillations [46]. Motivated to address this concern, which is very likely to affect future WECSs, reactive power handling capability of individual WTGs and a centralized unit are also investigated in this research.

1.2 Major contributions of the thesis

Throughout this research, a number of theoretical contributions were reported, and they are summarized as follows.

- *Propose a direct integration of battery-supercapacitor ESS using diode-clamped three-level grid-connecting inverter:* Possibility of replacing ordinary dc-link capacitors of a diode-clamped three-level inverter with a battery bank and a supercapacitor bank is investigated. Unavoidable imbalance in dc-link voltages, which causes uneven distribution of space vectors, is the major problem with this approach. A novel space vector modulation (SVM) method has been proposed to address this issue. In addition to that, small vector selection based power sharing technique has also been developed.
- *Explore the possibility of replacing ordinary capacitors of a three-level flying-capacitor rectifier and inverter by three battery banks or supercapacitor banks:* Unavoidable imbalance in battery or supercapacitor voltages is the major problem with this particular topology as well. Space vector distribution is even more complicated in this system due to the presence of two intermediate voltage levels in each leg of the inverter. A detailed analysis on this issue and a novel SVM method, developed as the solution, are presented.
- *Propose the 2x2 dual inverter topology for grid-side inverter implementation and direct integration of battery/supercapacitor ESSs:* The popular 2x2 dual inverter topology, where two two-level inverters are cascaded through open ends of the coupling transformer primary winding, is used in this study. The dc-link of the first inverter is connected to the rectified output of the WTG while a battery or a supercapacitor bank is directly connected to the dc-link of the second inverter. The first inverter is operated in six step mode to reduce switching losses. Effects of uncorrelated and dynamic variations of dc-link voltages are investigated. Novel modulation and control techniques are proposed as solutions for the problems caused by variable dc-link voltages.
- *Propose a series of combined inverter topologies for grid-side inverter implementation and direct integration of battery/supercapacitor ESSs:* Cascaded operation of 2x3, 3x2 and 3x3 dual inverter systems is investigated. In all three configurations dc-link of the first inverter is connected to the rectified output of the WTG. Furthermore, the first inverter is switched at the fundamental frequency

to reduce switching losses. The low-power second inverter operates at a high frequency and is responsible for suppressing harmonics produced by the first inverter. Battery and/or supercapacitor ESSs are directly interfaced to the second inverter. Modulation, control and power sharing of each configuration are thoroughly investigated in this research.

➤ *Propose a hybrid cascaded multilevel inverter for the grid connection of WECSs:*

This cascaded multilevel inverter system is formed by combining a standard two level inverter and three H-bridge modules. DC-Link of the two-level inverter is connected with the rectified output of the WTG. Three supercapacitor banks are directly connected to the dc-links of H-bridge modules. Furthermore, the two-level inverter is operated in six step mode and hence it can be constructed using high power low speed devices like IGCTs. Harmonics produced by the square wave output of the two-level inverter is compensated by high-speed H-bridge modules. This particular arrangement reduces power losses, improves power handling capability and generates multilevel voltage waveforms. In addition to that, the ability to absorb short term power fluctuation with the help of supercapacitors can be considered as an added advantage of the proposed inverter.

➤ *Propose a matrix converter topology for transformer-less grid connection of multi-pole direct-drive PMSG based WECS:* A matrix converter based transformer-less grid integration topology for high-power, direct driven, split winding PMSG wind turbine generators is proposed. The matrix converter system consists of large number of low-power modules which are fed from isolated generator coils. Outputs of matrix converter modules are connected in series to increase the output voltage and thus eliminate the need of a coupling step-up transformer. Moreover, the absence of dc-link capacitors increases the system reliability. Novel modulation, control and power sharing techniques have been developed for this unique design.

➤ *Propose a cascaded multilevel inverter based static synchronous compensator for wind farms:* The proposed STATCOM needs only four dc-link capacitors and 24

switches to synthesize 9-level operation. In addition to that, switching losses are reduced by splitting the voltage source inverter of the STATCOM into two units which operate at different voltages and switching frequencies. This particular configuration offers high voltage and high power ratings. As a result, it has a high potential of being implemented in future high capacity wind farms for both active and reactive power compensation. Modulation and control techniques required to manage reactive power of the STATCOM and thus suppress voltage fluctuations at the point of common coupling are presented.

1.3 Organization of the thesis

The thesis is organized into eight chapters with the main aim being to present the findings in an organized manner. Chapter 1 introduces the background, motivation and the direction of the research on ‘power converter systems for wind generation’. Major contributions and the organization of the thesis are also summarized in this introductory chapter.

Chapter 2 starts with a brief description and a mathematical model of PMSGs followed by a review on commonly used generator-side converter technologies. A brief description on the control of a conventional two-level back-to-back full scale converter based wind energy conversion system is also presented in this chapter with corresponding simulation results. Limitations of two-level converters at increased power levels are discussed in brief to highlight the importance of high-power multi-level converter systems. Furthermore, the possibility of replacing conventional capacitors of a flying-capacitor three-level rectifier with supercapacitors and making the converter to absorb wind power fluctuations are explored.

The immediate successors of the two-level inverter, i.e. diode-clamped and flying-capacitor three-level inverter systems, are explored in Chapter 3. The possibility of replacing dc-link capacitors of a diode-clamped three-level inverter with battery/supercapacitor energy storage systems is investigated. Similarly, replacement of ordinary capacitors of a flying-capacitor three-level inverter by three battery banks or three supercapacitor banks is also discussed in this chapter. Effects of variable dc-link

voltages on space vector distribution and modified modulation techniques, to produce undistorted outputs even under unbalanced conditions, are presented.

Chapter 4 presents four different dual inverter configurations, namely 2x2, 2x3, 3x2 and 3x3 for high-power multi-MW wind energy conversion systems. Possibility of battery and/or supercapacitor direct connection with these inverter topologies are explored in this chapter. Unavoidable dc-link voltage imbalance and its effects on space vector pattern are also discussed in detail. Novel modulations and control techniques, proposed to address this issue, are presented.

The proposed hybrid cascaded multilevel inverter topology is explained in Chapter 5. The unique feature of this topology is the possibility of direct integration of supercapacitors. This incorporates power smoothening capability to the grid-side inverter. However, the major problem of this particular arrangement is the change of supercapacitor voltages. A detailed analysis on this issue and possible solutions are proposed in this chapter.

A matrix converter topology for transformer-less grid integration of high-power, direct driven, split winding PMSG based wind turbine generators is proposed in Chapter 6. Relevant modulation, control and power sharing techniques, developed for the operation of this unique design, are explained in detail.

Chapter 7 starts with a brief introduction on the possibility of voltage restoration by reactive power injection. This concept is used to suppress voltage fluctuation at the point of common coupling (PCC) of wind farms. The reactive power injection capabilities of individual WTGs and centralized STATCOMs are compared in this chapter. A cascaded 3x3 inverter system is proposed in this chapter to build a low loss high-power centralized STATCOM unit for wind farms. Relevant modulation and control methods are explained in detail.

Finally, Chapter 8 concludes the thesis and recommends a number of possible research areas that can be explored in the future.

Chapter 2 A review on generator-side converter systems

2.1 Introduction

Wind is the bulk movement of air due to changes in its density and pressure. A brief description on the cause of these changes, in other words the origin of wind, is presented in section 2.2 as a basis for subsequent discussions. Thereafter, mathematical models are formulated for the available power of wind and the amount of power that can be captured by a wind turbine to emphasize the need for variable speed operation.

Permanent magnet synchronous generators and back-to-back converter systems are identified as key elements in realization of variable speed wind energy conversion systems. Therefore, an assessment on the trend towards PMSGs, mathematical model for a PMSG in the d - q reference frame and a controller for zero d -axis current control are presented in section 2.3. An outline of the back-to-back converter arrangement, which comprises of a generator-side converter, intermediate dc-link and a grid-side converter, is also presented at the end of this section.

A classification on generator-side converters is given in section 2.4. Mainly, the generator side converter can be a passive rectifier, hybrid rectifier or an active rectifier. A brief discussion on the two popular passive rectifiers, diode-bridge rectifier and multi pulse rectifier, is presented in section 2.5. The hybrid rectifier can either be a combination of a rectifier and an electronic reactance, a combination of a rectifier and a dc-dc converter or a half controlled rectifier. These three categories are explained in detail in section 2.6. The most popular active generator-side converter is the standard six switch two-level converter. Therefore, a detailed discussion on two-level rectifier based WECS is presented with related control techniques and simulation results in section 2.7.

Recently, diode-clamped and capacitor-clamped three-level active rectifiers became popular due to the ever increasing demand for high power converter systems. Brief introduction, advantages and limitations of these two topologies are presented in section 2.7. Moreover, the possibility of absorbing short term wind power fluctuations through clamping capacitors of a capacitor-clamped three-level active rectifier is investigated.

2.2 Basics of wind power

Globally, the two major driving factors of large scale winds are the differential heating between the equator and the poles and the rotation of the earth. Solar irradiance is optimum near the equator and thus the air near the surface in tropical regions get heated more than the air near the surface of the polar regions. This leads to convection currents in the atmosphere. As the earth being a rotating planet, convection currents will be deflected by the Coriolis effect [51]. Atmospheric circulation analysis have shown that the large scale movement of air on the planet can be divided into three cells: the Hadley cell, the Ferrel cell, and the Polar cell as shown in Fig. 2.1(a).

Fig. 2.1. (a) Atmospheric circulation in large scale, (b) (c) zonal air circulation due to disparities of temperature in land and sea [51].

While the Hadley, Ferrel, and Polar cells are major factors in global wind circulation, disparities of temperature in land and sea also drive a set of zonal air circulations. Since water has a higher specific heat capacity than land it absorbs and releases more heat, but the temperature change is less than land. As a result, during the day time land heats more than the sea. This carries the sea breeze into the land as shown in Fig. 2(b). During the night land cools faster than the sea and it carries the land breeze out to sea as shown in Fig. 2(c).

Therefore, in summary, it can be concluded that the ultimate source of wind is the sun and thus wind can be considered as a sustainable energy source.

2.2.1 Power of wind and Betz limit

The kinetic energy of air with mass m and speed V_w is given by the familiar relationship:

$$E_k = \frac{1}{2} m V_w^2 \quad (2.1)$$

Since power is the energy per unit time, the power of air passing through area A can be written as

$$P_w = \frac{1}{2} \rho A V_w^3 \quad (2.2)$$

where P_w is the power in wind (watts), ρ is the air density (kg/m^3) at 15°C and 1atm [21], A is the cross-sectional area through which the wind passes (m^2) and V_w is the wind speed normal to the area A (m/s).

According to (2.2) the power in the wind increases as the cube of wind speed, i.e. doubling the wind speed increases the power by eightfold. Furthermore, wind power is proportional to the square of the blade diameter and thus doubling the diameter increases the power by a factor of four.

Similar to the limitations seen in other energy conversion technologies such as Carnot efficiency for heat engines, band gap for photovoltaic cells, Gibbs free energy for fuel cells, there is an upper limit for the conversion of kinetic energy in the wind to mechanical power, which is known as Betz limit [21].

This limitation can be understood as having two extremes for the downwind velocity [21], [23]. The lower limit is zero which means air comes to a complete stop behind the turbine, which, with nowhere to go, would prevent any more of the wind to pass through the rotor. That means the turbine does not extract energy from wind and therefore the downwind velocity cannot be zero. The upper limit is when the downwind velocity is the same as the upwind speed which means the turbine extracts no energy at all from the wind. These two limits suggest that there must be some ideal slowing of the wind that will result in maximum power extraction by the turbine. What Betz showed was that an ideal wind turbine would slow the wind to one-third of its original speed [21].

2.2.2 Variable speed operation for maximum power capture

The implication of the aforementioned downwind velocity limit is that it is impossible to extract all the available power from wind. Therefore the conversion efficiency is obviously less than 100%. The power coefficient C_p is introduced to the wind power equation as in (2.3) to represent this conversion efficiency. The above Betz limit defines the theoretical maximum for the conversion efficiency as 59.3% which is known as the *Betz efficiency* or the *Betz law* [21].

$$P_w = \frac{1}{2} C_p \rho A V_w^3 \quad (2.3)$$

The power coefficient is a nonlinear function of the wind speed, rotor speed and the blade pitch angle. The effect of rotor speed on the power conversion efficiency can be explained as follows. If the rotor turns too slowly, the blades let too much wind pass by unaffected and thus the efficiency drops. On the other hand if the rotor turns too fast, efficiency is reduced as the turbulence caused by one blade increasingly affects the blade that follows. Furthermore, analysis has shown that instead of taking wind speed and rotor speed as two separate variables it is possible to define a single variable called tip-speed-ratio (TSR) to simplify the expression for power coefficient. The TSR, (also denoted by λ), is defined as the ratio between the rotor tip speed and the wind speed as in (2.4). The generic equation for the power coefficient is defined as in (2.5) [52].

$$\text{Tip speed ratio, } \lambda = \frac{\text{Rotor tip speed}}{\text{Wind speed}} \quad (2.4)$$

$$C_p(\lambda, \beta) = \frac{1}{2} \left(\frac{98}{\lambda_i} - 0.4\beta - 5 \right) \exp \left(\frac{-16.5}{\lambda_i} \right) \quad (2.5)$$

$$\lambda_i = \left[\frac{1}{(\lambda + 0.089)} - \frac{0.035}{(\beta^3 + 1)} \right]^{-1} \quad (2.6)$$

where β is the blade pitch angle.

The characteristic function C_p vs λ , for various values of the pitch angle β , is illustrated in Fig. 2.2(a). The maximum value of C_p , that is $C_{pmax}=0.47$, is achieved for $\beta=0^\circ$ when the TSR, $\lambda=6.75$. This particular value, named as the optimal tip-speed-ratio, λ_{opt} , results in the point of optimal efficiency where the maximum power is captured from wind by the wind turbine.

Fig. 2.2. (a) Variation of the power coefficient, C_p , for various values of the pitch angle, β , (b) captured wind power versus rotor speed curves at various wind speeds [52].

Fig. 2.2(b) illustrates the mechanical power versus the rotating speed of a typical three-bladed horizontal-axis wind turbine at various wind speeds for the blade pitch angle $\beta=0^\circ$. It can be observed that, for each wind speed, there exists a specific point in the wind generator power characteristic, also known as the maximum power point (MPP), where the output power is maximized. The rotor speed at the MPP corresponds to the aforementioned optimal TSR. Therefore, for a given wind turbine and a given pitch angle the optimal TSR should be maintained for maximum power extraction. In other words, rotor speed should vary in proportion to the wind speed for maximum power capture. This operation is known as maximum power point tracking (MPPT)

2.2.3 Back-to-back full-scale converter

The drive towards high efficiency wind energy conversion systems has resulted in almost all the modern wind turbines to operate in the variable speed mode [22] [23]. In such systems amplitude and frequency of the generator output varies with the wind speed and must therefore be decoupled from the grid. This can be achieved by using a back-to-back power electronic converter system.

The back-to-back power electronic converter system can either be partially rated or full-scale as shown in Fig. 2.3(a) and Fig. 2.3(b) respectively. The partially rated converter is usually found in DFIG based WECSs. On the contrary the full-scale converter is applicable for almost all the generator systems. However, the combination of PMSG and full-scale back-to-back converter system seems to dominate in the wind energy market

mainly due to the improved reliability and efficiency [22] [23], [28] [29], [34]. Therefore, this research is focused on PMSG based wind energy conversion systems with full-scale power electronic converter systems.

Fig. 2.3. (a) DFIG with a partially rated back-to-back converter system, (b) PMSG with a full-scale back-to-back converter system.

2.3 Permanent magnet synchronous generator

The absence of excitation winding losses helps PMSGs to reach high efficiency values. Furthermore, the direct-drive capability of multi-pole PMSGs eliminates the gearbox and thus reduces the cost and weight of the drive train. Moreover, the brushless operation of PMSGs reduces the burden of periodic maintenance making the system more robust and reliable. Therefore direct-driven multi-pole PMSGs are becoming the popular choice in modern onshore and offshore multi-megawatt WECSs [28] [29].

2.3.1 PMSG model

The PMSG model in the synchronous reference frame is shown in Fig. 2.4. Based on this model, two expressions can be derived for d - q axis voltages as in (2.7) and (2.8) respectively [53]-[55].

Fig. 2.4. PMSG model in the synchronous reference frame.

$$v_d = i_d R_s - \omega_e \varphi_q + L_d \frac{di_d}{dt} \quad (2.7)$$

$$v_q = i_q R_s + \omega_e \varphi_d + L_q \frac{di_q}{dt} \quad (2.8)$$

where v_d and v_q are d - q axis voltages, i_d and i_q are d - q axis currents, R_s is stator resistance, L_d and L_q are d - q axis inductances and ω_e is electrical rotational speed. φ_d and φ_q are magnetic flux components in d - q axes and their magnitudes are determined using (2.9) and (2.10). φ_m in (2.9) is the flux produced by permanent magnets of the generator. Electric torque produced by the generator is given by (2.11).

$$\varphi_d = L_d i_d + \varphi_m \quad (2.9)$$

$$\varphi_q = L_q i_q \quad (2.10)$$

$$T_e = \frac{3}{2} p (\phi_d i_q - \varphi_q i_d) \quad (2.11)$$

where p is the number of pole pairs.

Angular acceleration of the generator and the relationship between the electrical rotational speed and the mechanical rotational speed are given in (2.12) and (2.13) respectively.

$$\dot{\omega}_m = \frac{1}{J} (T_m - T_e) \quad (2.12)$$

$$\omega_e = p \omega_m \quad (2.13)$$

where J is the inertia, ω_m is the mechanical rotational speed of the generator, T_m is the mechanical torque and T_e is the electrical torque.

2.3.2 PMSG controller

The zero d -axis current control technique is used to control the speed of the generator. In this method d -axis component of the stator current is maintained at zero. As a result d -axis component of the magnetic flux becomes equal to the flux produced by the permanent magnet of the generator as shown in Fig. 2.5. This flux, together with the q -axis current, produces the electrical torque according to (2.14), which is an analogue to the operation of dc machine [55]. Therefore, in the speed controller shown in Fig. 2.6 the q -axis current is controlled to control the speed of the generator [54].

Fig. 2.5. Vector diagram showing zero direct axis current control of the PMSG.

$$T_e = \frac{3}{2} p \phi_m i_q \quad (2.14)$$

$$i_q^* = \frac{2T_e^*}{3p\phi_m} \quad (2.15)$$

$$v_d^* = -\omega_e \phi_q = -\omega_e L_d i_q \quad (2.16)$$

$$v_q^* = i_q R_s + \omega_e \phi_d = i_q R_s + \omega_e \phi_m \quad (2.17)$$

$$v_s^* = \sqrt{v_d^{*2} + v_q^{*2}} \quad (2.18)$$

$$\alpha = \tan^{-1} \left(\frac{v_q^*}{v_d^*} \right) \quad (2.19)$$

Fig. 2.6. Block diagram of the speed controller.

In the speed controller shown in Fig. 2.6, the reference angular speed is compared with the actual speed of the generator and the error is passed through a PI controller. Output of the PI controller is the q -axis current reference. The d -axis current reference is set to zero. These current references are compared with actual currents and the errors are passed through PI controllers to generate required voltage components. Mathematical

formulation for this control action is given in (2.15)-(2.17). Equations (2.18) and (2.19) are used to determine the amplitude and the angle of the inverter output voltage vector.

2.4 Generator-side converter

According to the top-level schematic shown in Fig. 2.3(b) the immediate follower of the PMSG is the generator-side converter. The basic function of this unit is to convert alternating voltage and current of the PMSG into dc quantities for the use of the subsequent grid-side inverter. And essentially this is a unidirectional conversion since the wind turbine is only supposed to supply power to the grid, not the other way around. Therefore, the full spectrum of ac-dc converter topologies, shown in Fig. 2.7, is available for the grid-side converter design. Theoretically, all of these converter topologies should be applicable in WECSs. However, the selection of a suitable topology depends on number of factors such as power rating, power density, reliability/robustness, complexity, cost, dc-link voltage requirements, harmonic distortion, power losses etc. Therefore, the rest of this chapter is planned to give an analysis on each converter category, at least taking one topology from each category. Selected topologies are marked with bolded text.

Fig. 2.7. Classification of ac-dc converter systems [56].

A detailed discussion on passive single bridge and multi-pulse rectifier systems is given in section 2.5. Three hybrid rectifier systems are discussed in section 2.6. The benefits of electronic inductor/capacitor are also discussed in this section. Under the active rectifier category two-level rectifiers, diode-clamped three-level rectifier and capacitor-clamped three-level rectifier are discussed in section 2.7.

2.5 Passive rectifier systems

The most simple generator-side converter is the diode-bridge rectifier shown in Fig. 2.8(a). Furthermore, the natural commutation of diode-bridge rectifiers eliminates the need for sensors, complicated controllers and gate drivers and thus the cost, power losses and failure rate are extremely low compared to any other rectifier arrangement. Moreover, the diode-bridge rectifier is a well matured product and thus high-power off-the-shelf modules are readily available in the market for direct deployment in wind generation systems.

However, it has several drawbacks such as dc-link voltage ripples and phase current harmonics [56]. Ripples in the dc-link voltage can be reduced with the use of a large capacitor. But it introduces torque oscillations and increases the harmonic distortion in phase currents which in turn requires large filters in the generator side for compensation. The absence of voltage boosting is also another disadvantage since the dc-link voltage varies with the speed of the generator. Consequently, modulation index of the grid-side inverter shows large variations which in turn results in poor switch utilization [57].

An improvement suggested to overcome some of the aforementioned drawbacks is the use of multi-pulse rectifiers [58]-[60]. This is basically a series or parallel connection of standard 6-pulse diode-bridge rectifiers [61]. A 12-pulse series connected rectifier is shown in Fig. 2.8(b). More details on multi-pulse rectifiers are given in section 2.5.2.

Fig. 2.8. Passive rectifier systems (a) 6-pulse diode-bridge rectifier, (b) 12-pulse series connected rectifier.

2.5.1 Diode-bridge rectifier

A simulation was carried out to show dc-link voltage ripples and phase current harmonics produced by a diode-bridge rectifier. The simulation setup is shown in Fig. 2.9(a). For the simplicity, a resistive load was assumed in this simulation. The voltage and current waveforms shown in Figs. 2.9(b) and 2.9(c) were obtained without a dc-link capacitor. Therefore, they illustrate the behavior of an ideal diode-bridge rectifier. Supply voltage waveform of the a -phase is shown in Fig. 2.9(b). Maximum and minimum values of the dc-link voltage are also shown in Fig. 2.9(b) which are given in (2.20) to (2.22). As given in (2.23) the percentage of the dc-link voltage ripple is found to be 23.21%. Furthermore, as shown in Fig. 2.9(c), total harmonic distortion (THD) of the phase currents, defined in (2.24), is also very high since only two phases conduct at a time.

$$V_{\max} = \sqrt{3}V_p \quad (2.20)$$

$$V_{\min} = \frac{3V_p}{2} \quad (2.21)$$

$$V_{\text{avg}} = \frac{3\sqrt{3}V_p}{\pi} \quad (2.22)$$

$$\frac{\Delta V}{V_p} = \frac{2\sqrt{3}-3}{2} = 23.21\% \quad (2.23)$$

$$THD = \frac{\text{rms value of the harmonics}}{\text{rms value of the fundamental}} \times 100\% \quad (2.24)$$

Fig. 2.9. Performance of a diode-bridge rectifier (a) simulation setup $R=10\Omega$, (b) supply voltage, v_a (phase a to neutral) and dc-link voltage, V_{dc} , (c) phase current, i_a (a -phase) for $C=0F$, (d) decrease in the dc-link voltage ripples and increase in phase current spikes with the increase of dc-link capacitance (simulation time is one second), (e) shape of the phase current waveform at $C=2.5mF$, (f) increase of THD with the increase of dc-link capacitance (simulation time is one second).

The simplest way of reducing the dc-link voltage ripple is the increase of dc-link capacitance. Even though this reduces the dc-link voltage ripple as shown in Fig. 2.9(d) by the trace marked as V_{dc} the peak current stress on diodes get increased. The corresponding current variation is also shown in the same figure by the trace marked as i_a . An enlarged view of this current waveform for $C=2.5mF$ is shown in Fig. 2.9(e) and it reveals that the converter enters into the discontinuous conduction mode (DCM) at high

values of the dc-link capacitance [56], [62]. Consequently, harmonic distortion of phase currents gets increased as shown in Fig. 2.9(f). Therefore, dc-link capacitor alone cannot improve performance of the diode-bridge rectifier and thus current smoothing inductor(s), either placed in the ac-side or dc-side as shown in Fig. 2.10(a) and Fig. 2.10(b) respectively is(are) compulsory [63].

In order to compare performance of current smoothing inductor(s) two sets of simulations were carried out for the systems shown in Figs. 2.10(a) and 2.10(b). Both rectifier systems were supplied from the same source and the corresponding *a*-phase voltage waveforms are shown in Figs. 2.10(c) and 2.10(d). Phase current waveforms of both systems at five discrete values of smoothing inductance are given in Figs. 2.10(e) and 2.10(f). According to Fig. 2.10(e) phase current becomes smooth and square in shape with the increase of the dc-side smoothing inductance. Consequently, THD gets reduced with the increase of the inductance as shown in Fig. 2.10(g). However, this improvement is far below compared to that of the ac-side smoothing inductance, shown in Figs. 2.10(f) and 2.10(h). Nevertheless, according to Figs. 2.10(i, j, k and l) dc-link voltage ripple reduction is quite similar in both implementations. Therefore, in terms of harmonic distortion and dc-link voltage ripple reduction, ac-side is preferred for the connection of smoothing inductor(s). However, smoothing inductors attached to the ac-side introduce voltage drop and thus the output voltage inevitably gets lowered with the increase of the inductance as shown in Fig. 2.10(n). In fact, in large PMSGs winding inductance is significantly large and it causes the output voltage to drop significantly at high loading conditions. As a solution to this problem an electronic capacitance based magnetic energy recovery system is presented in section 2.6.1.

On the other hand, the inductor attached to the dc-side does not introduce such losses and thus the output voltage is independent of the inductance as illustrated in Fig. 2.10(m). Therefore, dc-side seems to be the much preferred choice over the ac-side to add a smoothing inductor provided that the generator is capable of withstanding phase current harmonics with THD $\approx 28\%$.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)

(j)

Fig. 2.10. Performance of diode-bridge rectifier with smoothing inductors (a) diode-bridge rectifier with a dc-side smoothing inductor, (b) diode-bridge rectifier with ac-side smoothing inductors, (c) (d) supply voltage (phase a to neutral), (e) (f) phase current, i_a , at different inductor values, (g) (h) variation of THD with inductance, L , (i) (j) dc-link voltage at $L=2\text{mH}$, (k) (l) dc-link voltage at $L=20\text{mH}$, (m) (n) variation of dc-link voltage with inductance, L .

As mentioned before, change of the dc-link voltage with the speed of the generator is another drawback of the diode-bridge rectifier. In order to analyze this phenomenon in detail per-phase equivalent circuit of a PMSG and a diode-bridge rectifier, shown in Fig. 2.11, is considered and the corresponding voltage equations are given in (2.25) to (2.27).

Fig. 2.11. Per-phase equivalent circuit of the PMSG and rectifier.

Phase electromotive force (EMF), E , of a non salient pole PMSG is proportional to the generator speed and thus it can be expressed as in (2.25) [64]

$$E = K_e \omega_m \quad (2.25)$$

$$E^2 = (V_s + R_s I_s)^2 + (X_s I_s)^2 \quad (2.26)$$

$$V_{dc} = \frac{3\sqrt{3}(\sqrt{2}V_s)}{\pi} \quad (2.27)$$

where ω_m is the rotor speed of the PMSG and K_e is related to the magnetic flux linkage which can be considered as a constant.

From the above equations it can be deduced that the rectifier output voltage V_{dc} varies with the speed of the generator. In other words, in a variable speed wind turbine generator system with MPPT, the dc-link voltage varies with the generator speed as shown in Fig. 2.12(a). The corresponding power and current variations are also shown in the same diagram. Fig. 2.12(c) and Fig. 2.12(d) show the variations of inverter output voltage and power angle required to transfer the captured wind power into to an infinite ac bus at unity displacement power factor.

Fig. 2.12. (a) Variation of the dc-link voltage, current and power, (b) modulation index, (c) inverter output voltage, (d) power angle.

A simple comparison between the two voltage variations in Figs. 2.12(a) and 2.12(c) reveals that the required inverter output voltage variation is much less than the voltage variation at the rectifier terminal. In numerical terms, the voltage at the rectifier terminal doubles for a wind speed change from 0.5 p.u. to 1.0 p.u., whereas the required increase of the inverter output voltage is less than 10%. The grid-side inverter satisfies both of these voltage changes by varying the modulation index as shown in Fig. 2.12(b) [57].

The modulation index is set to 1.0 for the minimum dc-link voltage at the rectifier terminal which corresponds to the cut-in wind speed of the wind turbine generator. The

modulation index is then reduced with the dc-link voltage. Consequently, a rather low modulation index (about 0.3) has to be used for the rated wind speed. This high power delivery at low modulation indices results in poor switch utilization [57].

2.5.2 Multi-pulse rectifier

Multi-pulse rectifiers have been introduced for both power sharing and dc-link voltage ripple reduction in high power ac-dc converter systems. As mentioned before, multi-pulse rectifiers can be found in both series and parallel combinations of standard 6-pulse diode-bridge rectifiers as shown in Fig. 2.13. These topologies are capable of reducing the dc-link voltage ripple down to 5% and THD in phase currents down to 1% [58]-[61]. Parallel and series connections of two diode-bridge rectifiers are shown in Fig. 2.13(a) and Fig. 2.13(b) respectively. In order to make them multi-pulse rectifiers, Y Δ Y phase shifting transformers are required. With the introduction of these transformers dc-link voltage ripples of the two rectifiers get a phase shift of 30° as shown in Fig. 2.13(e and f). As a result, part of dc-link voltage ripples get cancelled out and end up with a more smooth voltage. Phase current harmonics also get reduced as shown in Fig. 2.12(g and h).

Major differences between parallel and series multi-pulse rectifiers are current sharing and voltage addition. In the parallel connected system only one rectifier conducts at a time whereas in the series connected system both rectifiers conduct simultaneously. Moreover, in the parallel system, output voltage is equal to the output of one rectifier. In the series connected system output voltage is simply the sum of the two voltages and therefore the supply voltage can be reduced to a half compared to the parallel connected system as shown in Figs. 2.13(c) and 2.13(d). Nevertheless, current rating of the supply of the series connected system should be doubled.

(c)

(d)

(e)

(f)

(g)

(h)

(i)

(j)

(k)

(l)

(m)

(n)

(p)

(q)

Fig. 2.13. Multi-pulse rectifiers (a) parallel connected 12-pulse rectifier, (b) series connected 12-pulse rectifier, (c) (d) supply voltage (phase to neutral), (e) (f) individual rectifier voltages and the total dc-link voltage, (g) (h) supply current, i_a , (a-phase), (i) parallel connected 18-pulse rectifier, (j) series connected 18-pulse rectifier, (k) (l) supply voltage (phase to neutral), (m) (n) individual rectifier voltages and the total dc-link voltage, (p) (q) phase current, i_a , (a-phase).

With the results shown in Figs. 2.13(e) to 2.13(h) it is clear that 12-pulse rectifier show significant improvements in the reduction of dc-link voltage ripples and phase current harmonics. Similarly, 18-pulse rectifiers and the corresponding simulation results are shown in Figs. 2.13(i) to 2.13(q). The supply voltage of the series connected 18-pulse rectifier can be reduced to 1/3 of the parallel connected system with the increase of current rating to 3 times. The same analysis can be extended for higher order multi-pulse rectifier systems, such as 24-pulse rectifier, as well. However, this discussion is limited to 12 and 18-pulse rectifier systems and more information on other multi-pulse rectifier systems can be found in [61].

According to these results it can be observed that the increase in the number of diode-rectifier modules would reduce ripples in the dc-link voltage and harmonics in phase current.

2.6 Hybrid rectifier systems

As seen in the previous section multi-pulse rectifier systems show significant improvements in terms of dc-link voltage ripples and phase current harmonics. But the increase in the diode count and, specially, the need of additional phase shifting transformers make multi-pulse rectifiers less attractive in wind generation systems. Therefore, alternative technologies have been developed to address the issues of dc-link voltage ripples and phase current harmonics of conventional 6-pulse rectifiers.

One such technology is the electronic smoothening inductor (ESI) which mimics a large inductor connected in series with the rectifier [56], [62] [63]. It acts as a series connected voltage source that absorbs ripples present in the rectifier output voltage. Therefore, phase currents become constant during conduction time and thus THD gets slightly reduced.

Voltage drop across synchronous reactance is significant in large PMSGs [65]. However, the above topology with an electronic inductance attached to the dc-side does not help to solve this problem. Therefore, instead of the dc-side it is possible to connect three such units at the ac-side in series with generator outputs to function as electronic capacitors. This arrangement is known as magnetic energy recovery (MER) [65]-[68]. A detailed discussion on electronic inductance and MER are presented in section 2.6.1.

Even if ESI and MER are used, aforementioned dc-link voltage variation with the generator speed is still present in all these topologies which results in poor switch utilization of the grid-side inverter. Therefore, an intermediate dc-dc converter stage is essential to regulate the dc-link voltage and improve the performance of the grid-side inverter. The most common intermediate dc-dc converter is the single stage boost converter. Other variants such as buck converter, buck-boost converter and Z-source converter are also proposed in literature [69]. All these topologies greatly reduce dc-link voltage ripples and phase current harmonics. Moreover, with these use of these topologies the large synchronous reactance of PMSGs can effectively be used for voltage boosting [56], [70]. If the synchronous reactance is not large enough additional inductors might be required to achieve dc-link voltage regulation [56]. A detailed analysis on the combination of a 6-pulse rectifier and a boost converter is presented in section 2.6.2

2.6.1 Electronic reactance based hybrid rectifier systems

As discussed before in section 2.5.1 the major drawbacks of the 6-pulse rectifier are dc-link voltage ripples, phase current harmonics and resultant torque ripples on the generator and current stresses on the dc-link capacitor. The same section has emphasized that the solution is based on adding smoothing inductors to the ac-side or the dc-side. However, large smoothing inductors increase cost, weight and volume. Moreover, they reduce the dynamic response of the dc-link voltage.

Therefore, instead of passive smoothing inductor, a small power electronic unit, known as electronic smoothing inductor, can be used to obtain the same performance [56], [62] [63]. The corresponding schematic diagram for the dc-side implementation is shown in Fig. 2.14. The ESI is only supposed to absorb voltage ripples and thus its switches can be

rated only for the ripple voltage and not for the total dc-link voltage. Therefore, power rating of the ESI can be reduced down to 12% of the rated power of the rectifier.

A simulation was carried out with and without the ESI to show its efficacy and the corresponding results are shown in Figs. 2.14(b) to 2.14(d). In the first half of the simulation the ESI was disabled and thus usual current and voltage waveforms appear as shown in the first half of Figs. 2.14(c) and 2.14(d). The ESI was turned on at 20ms and therefore voltage and current waveforms get smoother proving the efficacy of the ESI. Similar analysis can be carried out for the ac-side implementation of the electronic inductance and show that it behaves in the same way and reduces dc-link voltage ripples and current harmonics.

Fig. 2.14. (a) Schematic diagram of the dc-side ESI implementation, (b) supply voltage (phase to neutral), (c) dc-link voltage without and with ESI, (d) phase current (a -phase) without and with ESI.

However, apart from reducing dc-link voltage ripples and phase current harmonics the ac-side implementation of ESI is capable of performing another important functionality in large PMSG based WECSs. That is to realize MER within the same ESI. In more general terms, the ESI connected in series with generator terminals can be used to compensate voltage drop across synchronous reactance of the PMSG [65]-[68]. The corresponding schematic diagram, equivalent circuit and vector representations of MER are shown in Fig. 2.15(a), Fig. 2.15(b) and Fig. 2.15(c, d) respectively. The phasor diagram shown in Fig. 2.15(c) corresponds to a general rectifier without magnetic energy recovery switches

(MERSs). It can clearly be seen from this diagram that the output voltage U is obviously lower than the induced voltage E of the generator. Moreover, power factor is also less than the unity. The MER compensate the voltage drop across the inductor by acting as a series connected capacitor. The corresponding phasor diagram is shown in Fig. 2.15(d).

Fig. 2.15. (a) Schematic diagram of the ac-side ESI implementation, (b) single-line diagram, (c) phasor diagram showing voltage and current vectors without MERS, (d) phasor diagram showing voltage and current vectors with MERS.

In order to evaluate performance of MERSs, simulations were carried out for three systems. The first system contained only a general diode-bridge rectifier. The second system was equipped with MERSs. In the third system, capacitors used in MERSs were connected in series with generator outputs so that it gives a clear comparison between MERS and series compensation with capacitors. The corresponding output voltages for different loading conditions are shown in Fig. 2.16(a).

Fig. 2.16(a) proves the efficacy of MERSs in compensating the voltage drop across synchronous reactance of the PMSG. Furthermore, it shows that series connected capacitors are not as effective as MERSs. Due to the voltage drop across synchronous reactance the amount of power that can be taken out from the generator also drops. In that context MERSs help to increase the output power as well. The corresponding power

variations against different loading conditions are shown in Fig. 2.16(b). Generator voltage and current waveforms of the a -phase are shown in Fig. 2.16(c). An enlarged view of this diagram is given in Fig. 2.16(d) to illustrate the power factor correction feature of MERSs. Based on these results it can be concluded that MERSs significantly improve the power factor as well.

Fig. 2.16. Efficacy of MERSs (a) dc-link voltage, (b) output power, (c) supply voltage and current of the a -phase, (d) enlarged view of the supply voltage and current of the a -phase.

2.6.2 Combination of a diode-bridge rectifier and a dc-dc converter

Even though aforementioned ESI based rectifiers are capable of performing MER, reducing voltage ripples and current harmonics, the problem of unregulated dc-link voltage is still present. As a result grid-side inverter operates at low modulation indices at high power conditions resulting in poor switch utilization. Therefore, all these topologies require an intermediate dc-dc converter stage for dc-link voltage regulation and thus meet requirements of modern WECSs.

The intermediate dc-dc converter can be a buck converter, boost converter or buck boost converter. However, out of these three configurations boost converter is the most popular and therefore, the following analysis is based on the single switch boost converter (also known as boost chopper) topology. Schematic diagram of this particular topology is shown in Fig. 2.17. In general, to implement the boost chopper an inductor, a capacitor, a switch and a diode are required. However, the dc-link capacitor is already there with the conventional rectifier. Furthermore, in some cases the winding inductance of the PMSG itself can effectively be used as the boosting inductor. Therefore, under optimum conditions only an additional diode and a switch would suffice to implement the boost chopper. These two implementations are shown in Figs. 2.18(a) and 2.18(b) respectively. The corresponding voltage and current waveforms at different inductor values are given in Figs. 2.18(c) to 2.18(f).

Fig. 2.17. WECS with a single-switch boost rectifier.

The voltage waveforms shown in Fig. 2.18(c) demonstrate the voltage regulation capability of the conventional boost rectifier. Furthermore, it produces the same output voltage even at increased values of the boosting inductance. In contrast, the boost rectifier with ac-side inductors, shown in Fig. 2.18(b), loses voltage regulation after certain values of the boosting inductance. The corresponding simulation results are shown in Fig.

2.18(d) where the output voltage is regulated at 600V for inductor values up to 2.5mH. Further increase of the inductance decreases the output voltage and the power factor.

Fig. 2.18. (a) Boost rectifier with a dc-side boost inductor, (b) boost rectifier with ac-side boost inductors, (c) (d) supply voltage and output voltage, (e) (f) phase current, i_a , at different inductor values.

A close look on current waveforms shown in Fig. 2.18(e) would reveal that the optimum shape of phase current that can be obtained from the conventional boost rectifier with dc-side inductor is more or less similar to that of electronic smoothing inductance based implementations. The only difference is voltage regulation at the dc-side. On the other hand the boost rectifier with ac-side inductors significantly improves the THD as shown in Fig. 2.18(f). Therefore, this arrangement would be more suitable for PMSG based

WECSs with large synchronous reactance that can effectively be used as boosting inductors [70].

Both arrangements of the boost rectifier, shown in Figs. 2.18(a) and 2.18(b), result in high THD at low inductor values and low loading conditions. Moreover, high peak current loading on semiconductor devices and the large EMI filter effort make these two boost topologies unsuitable for modern multi-megawatt WECSs [56], [71]. A solution has been proposed in [59] with the phase-shifted operation of three interleaved converter units as shown in Fig. 2.19. Each converter unit equally contributes for the output power and thus the stress on power devices drops to 1/3 compared to the arrangements shown in Fig. 2.18(a) and 2.18(b). Furthermore, the phase shifted operation of the converter units reduces the current ripple and as a result THD becomes very low.

Two simulations were carried out to compare performance of the conventional operation and phase shifted operation of the above rectifier in terms of THD in phase currents at low loading conditions. The corresponding simulation results are given in Fig. 2.20. In both cases input voltage, output voltage reference and loading conditions were kept the same as shown in Figs. 2.20(a) and 2.20(b). In the conventional operation the same carrier waveform, shown in Fig. 2.20(c), is used to perform pulse with modulation of each converter switch. As a result of this synchronized operation all three converters conduct at the same time resulting in an increase in phase current ripples. The corresponding individual converter currents and the total current of the a -phase are shown in Figs. 2.20(e) and 2.20(g) respectively.

In contrast to this, the phase shifted operation uses three carriers which are phase shifted by 120° as shown in Fig. 2.20(d). As a result of this carrier phase shift, each converter unit conducts at different intervals and thus helps to reduce ripple in phase currents. The corresponding individual converter currents and the total current of the a -phase are shown in Figs. 2.20(f) and 2.20(h) respectively.

Fig. 2.19. Interleaved three-unit boost rectifier.

Fig. 2.20. (a) (b) Supply voltage and output voltage, (c) single carrier, (d) three phase shifted carriers, (e) (f) phase current, i_a , of individual converter units, (g) (h) total current in the a -phase.

2.6.3 Half controlled diode-bridge rectifier

Even though the interleaved three-unit boost rectifier, shown in Fig. 2.19, is capable of reducing harmonic distortion in phase currents it requires additional boosting inductors diodes and switches and thus would not be feasible for WECSs. In this context, the half controlled diode-bridge rectifier shown in Fig. 2.21(a) can be considered as the alternative solution with reduced component count [72]-[75]. If the winding inductances of the PMSG are large enough they can be used as boosting inductors and thus the component count can be reduced further.

The half controlled rectifier shown in Fig. 2.21(a) can be controlled in two ways. In the first and most simple method all three switches are controlled using a common PWM signal [56], [70], [72] [73]. In other words, they are turned on and off simultaneously. This unified operation reduces the complexity of the controller. In this operation the upper three diodes, D_1 - D_3 act as boosting diodes.

The equivalent circuit is shown in Fig. 2.21(b) for an instance where the a -phase voltage, E_a , is most positive and the c -phase voltage, E_c , is most negative. When both a -phase and b -phase are positive and the switches are turned-on currents build up in all three phases. During the off time, the stored energy in inductors are released to the load at a boosted output voltage. The magnitude of the dc-link voltage can be controlled through the duty cycle of the switches. At this particular instance the diodes D_1 and D_2 act as boosting diodes. The diodes D_3 is in the reverse biased condition. The generator winding inductances act as boosting inductors. The boosting switches S_1 and S_2 complete the structure of the boost converter. When the b -phase voltage is negative it conducts until the inductor L_b gets discharged.

Fig. 2.21. (a) Half controlled diode-bridge rectifier, (b) equivalent boost converter.

Similar diagrams can be drawn for other instances as well to analyze the boosting operation. For low modulation indices the output dc-link voltage shows a linear relationship with a peak at $m=0.65$ as shown in Fig. 2.22. Further increase of the modulation index will reduce the output voltage and collapse near unity due to the short circuit of phase windings. At very low modulation indices, near zero, this rectifier behaves exactly like an uncontrolled rectifier.

Fig. 2.22. Variation of the dc-link voltage with the modulation index.

Simulation results for this unified operation are shown in Figs. 2.23(a) and 2.23(b). The a -phase input voltage and output voltage are shown in Fig. 2.23(a). The corresponding phase current waveforms at different inductor values are shown in Fig. 2.23(b). These current waveforms prove the superiority of the half bridge rectifier in reducing THD compared to aforementioned single-switch boost rectifier shown in Fig. 2.18(b) for a given boosting inductance. However, the problems of voltage drop and power reduction at large inductor values are still common for both.

The second control method provides an answer to the problem of low power factor. In this method the input voltages of the rectifier are measured and the phase angle is derived using a phase locked loop. Phase currents are also measured and converted into $d-q$ axis components. Then they are controlled to bring the power factor to unity. After that conventional space vector or carrier based PWM can be used to control switches. In order to test performance of this control technique a simulation was carried out with same input voltages, output voltage reference and loading condition. The corresponding phase current waveforms are shown in Fig. 2.23(c). These waveforms prove that the supply voltage and current waveforms are in-phase and thus the power factor is close to unity.

Fig. 2.23. (a) Supply voltage and output voltage, (b) phase current, i_a , at different inductor values with control method 1, (c) phase current, i_a , with the control method 2

However, due to the lack of bridge symmetry the half controlled rectifier can impress sinusoidal phase currents only when two phase voltages are positive. Therefore, harmonic distortions in phase currents appear in alternative 60° intervals.

2.7 Active rectifier systems

With the above analysis it can be concluded that bridge symmetry is indispensable if the rectifier is supposed to achieve both voltage regulation and sinusoidal current impression. The traditional approach to obtain bridge symmetry is the use of the standard six switch active rectifier. However, modern WECSs require high power converters and thus the trend is to replace traditional six switch two-level rectifiers with multi-level rectifiers. As a result diode-clamped and capacitor-clamped three-level rectifiers have become popular. Moreover, owing to the unidirectional power flow of WECSs these two topologies can be implemented with less number of switches. This simplifies the controller and also reduces switching losses.

2.7.1 Full controlled two-level active rectifier

Schematic diagram of a WECS employing the standard six switch two-level active rectifier and inverter is shown in Fig. 2.24. The bridge symmetry with six active switches enables this rectifier to achieve both voltage regulation and sinusoidal current impression. This is the most common and well matured converter topology used in low-power and

medium-power WECSs [76]-[78]. Therefore, the complete control of the back-to-back converter system is discussed in detail in the following text with simulation results.

The controller block diagram shown in Fig. 2.25 consists of two controllers namely, the generator-side converter controller and the grid-side inverter controller. The generator-side converter controller is already explained in section 2.3.2 and therefore it will not be discussed here.

Fig. 2.24. WECS with a full controlled two-level active rectifier and inverter.

Fig. 2.25. Generator-side converter controller and grid-side inverter controller.

The two controllers are decoupled and the link between them is the dc-link voltage. The objective of the generator-side controller is to follow the speed reference produced by the maximum power point tracker. On the other hand the objective of the grid-side inverter controller is to regulate the dc-link voltage by controlling the amount of power delivered to the grid. Therefore, in the grid-side inverter controller the d -axis current reference is

derived from the dc-link voltage error [79]. The q -axis current reference is set to '0' to ensure zero reactive power transfer to the grid. However, the grid-side inverter is capable of injecting certain amount of reactive power as well in conjunction with active power delivery. Advantages and limitations of this feature are discussed in detail in Chapter 7.

Simulation results of the complete back-to-back converter system are shown in Fig. 2.26. The wind speed profile shown in Fig. 2.26(a) is used to test the dynamic response of the system for step changes in the input. The dc-link voltage of the back-to-back converter system is shown in Fig. 2.26(b). The corresponding generator side q -axis current reference and actual d - q current responses are shown in Fig. 2.26(c). The q -axis current follows the given reference while the d -axis current is maintained at zero. Mechanical time constant of the wind turbine generator system is neglected in this simulation since the focus is more on the electrical system. If the mechanical time constant is included the rise time of the current response becomes significantly large and thus a long simulation time will be required to show the complete response. Similarly, the grid-side d -axis current reference and actual d - q current responses are shown in Fig. 2.26(d).

The variation of the a -phase current of the generator-side converter and its enlarged view at $t=600\text{ms}$ are given in Fig. 2.26(e) and 2.26(g) respectively. According to Fig. 2.26(g) THD of generator phase current is reduced to 1.38%. This is a significant improvement compared to all the aforementioned rectifier systems. Variations of the a -phase current of the grid-side inverter and its enlarged view at $t=600\text{ms}$ are given in Fig. 2.26(f) and 2.26(h) respectively. THD of grid-side inverter phase currents is also in the same range compared to that produced by the generator-side converter.

The power captured by the wind turbine generator is shown in Fig. 2.26(i). The corresponding variations of the active and reactive power delivered to the grid are shown in Fig. 2.26(j). The reactive power component is maintained at zero while the active power shows a small drop compared to the input which is due to the losses incurred by switches and resistive elements of the system.

Fig. 2.26. Simulations results of the back-to-back full scale converter system employing two-level six-switch active rectifier and inverter, (a) wind speed profile, (b) dc-link voltage, (c) d - q components of the generator phase currents, (d) d - q components of the grid-side phase currents, (e) a -phase current of the generator, (f) a -phase current of the grid-side inverter, (g) zoomed in view of the a -phase generator current, (h) zoomed in view of the inverter a -phase current, (i) power captured by the wind turbine generator, (j) power delivered to the grid.

2.7.2 Full controlled diode-clamped three-level active rectifier

Schematic diagram of the standard diode-clamped three-level active rectifier is shown in Fig. 2.27. Compared to the above two-level converter, this topology can either double the dc-link voltage from a given ac-supply or reduce voltage stress on switching devices to a half if the same dc-link voltage is used [80] [81]. Furthermore, each leg of this converter has three switching states defined as $S_x = \{0, 1, 2\}$, $x = \{a, b, c\}$. The switching state 0 means the lower pair of switches in the corresponding leg is turned on while the other two are turned off. The switching state 1 means only the middle two switches are turned on. The switching state 2 corresponds to a situation where the upper pair of switches are turned on while the other two are turned off. These three switching states produce three voltage levels at the output [82] [83].

Fig. 2.27. WECS with a diode-clamped three-level active rectifier and grid-side inverter.

Fig. 2.28. Possible switch reductions for the generator-side converter.

The three-level diode-clamped converter shown in Fig.2.27 possesses bi-directional power flow capability which is not essential in WECSs. Therefore, it is possible to remove some of the switches as shown in Fig. 2.28 [83]. Even for this system generator-

side and grid-side converter controllers are very much similar to the controllers discussed in section 2.7.1 and hence will not be discussed here explicitly.

2.7.3 Full controlled capacitor-clamped three-level active rectifier

Schematic diagram of the standard capacitor-clamped three-level active rectifier is shown in Fig. 2.29. This converter is capable of producing four voltage levels [84] [85]. However, if the flying capacitor voltages are balanced only three discrete voltage levels are available at the output. Under balanced conditions this inverter behaves exactly similar to the diode-clamped three-level inverter. More details on balanced and unbalanced operations of the capacitor-clamped three-level converter can be found in chapter 3. As seen in the previous section switch reduction is possible for this converter topology as well [83]. The corresponding reduced generator-side converter is shown in Fig. 2.30.

Fig. 2.29. WECS with a capacitor-clamped three-level active rectifier and grid-side inverter.

Fig. 2.30. Possible switch reductions for the generator-side converter.

In comparison to the diode-clamped three-level inverter, component count is low in the capacitor clamped converter. However, drawbacks of clamping capacitors, such as bulkiness and less reliability make this converter not very attractive in WECSs. However,

these drawbacks can be overcome by replacing conventional clamping capacitors with compact and highly reliable supercapacitors and making the converter to absorb short term wind power fluctuation.

When supercapacitors are used to absorb power fluctuations their voltages vary with the stored energy. This variable voltage operation creates three major problems. Unequal blocking voltages and increased voltage slew rates (dv/dt) experienced by some switching devices is the first issue. However, the rapid development of device technologies enables the use of such devices with increased blocking voltage and slew rate and hence this would not be a significant issue. The second problem is the unequal distribution of instantaneous power losses among switching devices. This causes some devices to be heated up more than the others. However, supercapacitor banks are used only as short-term power smoothening elements and hence their average power in a cycle is theoretically zero. That means, on average, power losses get distributed evenly among switching devices. Therefore, in steady state temperature of switching devices vary at the same rate. However, heat sinks should have enough capacity to protect devices from aforementioned instantaneous power losses. The third problem is the uneven distribution of space vectors. A comprehensive analysis on this issue and appropriate modulation techniques are given in chapter 3.

A computer simulation was carried out on the MATLAB/SIMULINK platform for a wind generation system to show the efficacy of the supercapacitor-clamped three-level active rectifier. System parameters of the simulation setup are given in Table. 2.1. The controller discussed in section 2.7.1 is used for this setup as well with minor changes in power references. The modifications suggested are shown in Fig. 2.31. The power reference coming out from the wind turbine generator model, P_{ref}^* is low pass filtered and the output is taken as the reference for the grid-side inverter. This term is slightly changed to regulate the dc-link voltage. The difference between the original power reference and its low pass filtered component is an indicator whether supercapacitors should be charged or discharged. Therefore, based on this signal suitable small vectors are selected with the help of a lookup-table. In this charging discharging process special attention is paid on state of charge (SoC) balancing of supercapacitors. In other words, charging/discharging power is shared between supercapacitors based on their SoCs. In case of charging, the

supercapacitor with the lowest SoC is given the highest priority and is charged at a higher rate than the other two. The supercapacitor with medium SoC is given a medium priority while the lowest priority is set to the supercapacitor with the highest SoC. The opposite happens when there is a discharging situation.

Fig. 2.31. Supercapacitor voltage balancing controller.

Wind speed and input power profiles are shown in Figs. 2.32(a) and 2.32 (b) respectively. Output power, P_{out} , is maintained at a constant level and variations of the input power are absorbed by the supercapacitors. Corresponding supercapacitor voltage variations are shown in Fig. 2.32 (c). An enlarged view of the inverter output voltage, v_{as} , is given in Fig. 2.32 (d) for an unbalanced supercapacitor voltage condition. Inverter output currents, shown in Fig. 2.32 (e) prove the ability of the proposed system to generate undistorted outputs even under unbalanced conditions. Inverter output voltage at the balanced condition is also shown in Fig. 2.32(f) for comparisons.

Table 2.1. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency	$f_s = 5\text{kHz}$
Capacitance of supercapacitors	$C_{scx} = 150\text{mF}$
Range of supercapacitor voltage	$V_{scx} = 400\text{-}800\text{V}$
DC-Link voltage	$V_{dc} = 1200\text{V}$
Resistance of the PMSG	$R = 0.87\Omega$
Inductance of the PMSG	$L = 1\text{mH}$
Rated power of the PMSG	200kW

Fig. 2.32. (a) Wind speed, (b) input, output and supercapacitor power, (c) supercapacitor voltage variations, (d) inverter output voltage when $V_{sc} = 800V$, (e) inverter output current, (f) inverter output voltage when $V_{sc} = 600V$.

2.8 Summary

This chapter provides an overview of generator side converters used in PMSG based WECS. The diode-bridge rectifier is the simplest generator side converter. However, phase current harmonics and unregulated dc-link voltage with high ripple content are the major drawbacks of this converter. Multi-pulse rectifiers fed from phase shifted transformers are proposed to reduce dc-link voltage ripples. However, the need of bulky transformers and increased component count make this solution not suitable for WECSs. Alternatively, electronic smoothing inductors can be used to reduce dc-link voltage ripples. With this solution, phase current harmonics also get reduced slightly as a result of voltage ripple cancellation. The generator side is found to be more suitable to connect those electronic smoothing inductors owing to the possibility of compensating voltage drop across synchronous reactance of large PMSGs.

In order to regulate the dc-link voltage an intermediate dc-dc converter can be placed after the diode-bridge rectifier. However, in terms of phase current harmonic distortion performance of this arrangement is similar to that of electronic smoothing inductor based topologies. Therefore, this cannot be considered as a complete solution. The half controlled boost rectifier can be considered as the next in line which can produce sinusoidal phase currents at alternative 60 degree intervals with dc-link voltage regulation.

The full controlled six switch 2-level rectifier is the ultimate solution which can produce both sinusoidal phase currents and dc-link voltage regulation. Applications of this topology in WECSs are discussed in detail with relevant control techniques and simulation results. However, the standard six switch 2-level rectifier does not meet voltage and power requirements of modern multi-mega-watt WECSs. In this context, diode-clamped and capacitor-clamped three-level converters gained more attention. These two topologies and possible switch reduction techniques are discussed in brief at the end of this chapter. Furthermore, possibility of replacing conventional capacitors of capacitor-clamped three-level converter with supercapacitors and making them to absorb short term wind power fluctuations are also discussed. The effectiveness of this arrangement is justified with simulation results.

Chapter 3 Three-level inverter systems for wind generation

3.1 Introduction

The low voltage and low power (<1kV and <1MW) wind energy market is almost exclusively satisfied by the conventional two-level voltage source converter. However, with the development of modern multi-mega-watt wind turbine generators voltage and current ratings of full-scale converter systems increased up to a few thousands of volts and amperes respectively. Conventional two-level voltage source converters are not suitable for such systems mainly due to the low efficiency of high voltage switching devices [8], [28] [29], [34]. Therefore, three-level converters have been increasingly used as they can be built with low voltage devices. In addition to that, three-level converters reduce the blocking voltage and voltage slew rate (dv/dt) to a half of two-level converters and hence stresses on switching devices get reduced [86]-[88]. Furthermore, reduction of semiconductor losses will reduce the average temperature at the component and thus decrease the failure rate.

A comparison of output voltage and current between the two-level inverter topology and the three-level inverter topology are shown in Fig. 3.1. In the two-level inverter line to dc-link midpoint voltage, e.g. v_{ao} , changes from 300V to -300V at every switching instance resulting in a total of 600V step change. But in the three-level inverter this change is reduced to a half, i.e. 300V. In addition to that, total harmonic distortion of three-level inverter output current and voltage are very low compared to those of the two-level inverter. As a result, size, weight and cost of the output filter can significantly be reduced [22], [28] [29], [34], [61], [86]-[89].

As for the realization of three-level inverters, namely, diode-clamped (also known as neutral point clamped) three-level inverter topology, capacitor-clamped (also known as flying-capacitor) three-level inverter topology, and cascaded multilevel inverter topology have been used [86]-[92]. Out of these three topologies the first two, diode-clamped three-level inverter and capacitor-clamped three-level inverter are discussed in this chapter. A detailed discussion on cascaded multilevel inverter topologies can be found in chapter 4.

Fig. 3.1 Comparison of the two-level and three-level inverter output voltages and currents (a -phase) for an RL load where $R=1\Omega$, $L=0.5\text{mH}$, $V_{dc}=600\text{V}$, $m=0.8$ and $f_{sw}=1\text{kHz}$.

A brief introduction on the diode-clamped three-level inverter topology including its switching states, space vector pattern, vector types and redundant states are presented at the beginning of section 3.2. The later part of this section explores the possibility of battery/supercapacitor direct integration into the dc-link of the diode-clamped three-level inverter. This unique approach eliminates the need for interfacing dc-dc converters for both battery and supercapacitor banks and thus reduces associated power losses, cost, complexity and response time. However, the major problem with this approach is the uneven distribution of space vectors which is due to dynamic changes in dc-link voltages. A novel space modulation method, which can produce undistorted currents even in the presence of unevenly distributed space vectors, is proposed as a solution to this problem.

An introduction to the capacitor-clamped three-level inverter topology is presented at the beginning of section 3.3 followed by a novel supercapacitor direct integration scheme. The proposed scheme incorporates short term power smoothening capability into the

inverter and thus eliminates the need for interfacing dc-dc converters. Even though the operation of this inverter system is very much similar to that of the diode-clamped inverter, space vector distribution under unbalanced capacitor voltage conditions is extremely complex. A simple step-by-step approach is presented in section 3.3 to analyze the effects of variable capacitor voltages. Corresponding modulation, control and voltage balancing algorithms are presented in the latter part of section 3.3.

Section 3.4 proposes a battery-clamped inverter in contrast to traditional diode-clamped and capacitor-clamped inverters. The idea is to replace conventional capacitors of a capacitor-clamped inverter with batteries so that the inverter can absorb wind power fluctuations more efficiently. Imbalance and uncontrollability of battery voltages are the main issues with this unique system. Therefore, the proposed battery-clamped inverter should be able to operate under unbalanced conditions. A modified carrier based PWM method is proposed to achieve this objective.

A summary of the chapter is given in section 3.5.

3.2 Diode-clamped three-level grid-side inverter

Fig. 3.2. (a) Schematic diagram of the diode-clamped three-level inverter, (b) space vector distribution for the balanced condition i.e. $V_{C1} = V_{C2} = V_{dc}/2$.

Schematic diagram of the diode-clamped three-level inverter topology is shown in Fig. 3.2(a). Corresponding space vector distribution is shown in Fig. 3.2(b) for the balanced condition, i.e. $V_{C1} = V_{C2} = V_{dc}/2$. These vectors are referred with their switching states. The vectors 200, 220, 020, 022, 002 and 202 are known as large vectors. Similarly, the vectors

210, 120, 021, 012, 102 and 201 are called medium vectors. Small vectors are divided into two groups called positive (or upper) small vectors (211, 221, 121, 122, 112 and 212) and negative (or lower) small vectors (100, 110, 010 011, 001, and 101). When dc-link capacitor voltages are equal, upper and lower small vectors overlap and thus only a single inner hexagon is visible. This makes a redundancy in small vectors, which plays an important role in capacitor voltage balancing [93]. The three vectors at the origin (000, 111 and 222) are called zero vectors.

3.2.1 Battery/supercapacitor direct integration

The intermittent nature of wind energy can create serious system stability issues, especially at increased levels of penetration [9], [94]. A promising solution to this problem is the use of energy storage. Recently, batteries and supercapacitors have emerged as leading energy storage devices [41], [42], [95]-[97]. Furthermore, the combination of batteries and supercapacitors provides an excellent match that can cover a wide range of power and energy requirements [96], [98]. As a result, power quality enhancement using batteries and supercapacitors is actively pursued in the field of renewable energy as evident from literature [41], [42], [96]-[98].

When it comes to the system integration, the simplest way of adding a battery (or a supercapacitor) bank is the direct connection to the dc-link of the grid side inverter, as shown in Fig. 3.3(a). But it suffers from several drawbacks such as, large internal resistance, fixed current distribution governed by internal resistors and lack of control over the power flow [99]. Effects of these issues can somewhat be reduced if an intermediate dc-dc converter is placed between the battery (or the supercapacitor) bank and the dc-link as shown in Fig. 3.3(b). But it introduces additional cost, complexity and power losses. In addition to that, the low pass filter of the dc-dc converter, comprising of an inductor and a capacitor, degrades the dynamic response. A three-level bidirectional dc-dc converter has been proposed in [100] to reduce voltage stresses on switching devices and to improve the dynamic response with a reduced filter inductance. But it needs four switches and a flying capacitor. Therefore, the interfacing dc-dc converter increases the system cost, power losses and complexity, even if an optimized design is used. Therefore, the possibility of direct connection of battery/supercapacitor into the dc-

link of a diode-clamped three-level inverter was researched as shown in Fig. 3.3(c). Latter part of this section discusses two more cases where dc-link capacitors are replaced with two supercapacitor banks or two battery banks.

Fig. 3.3. Interfaces for battery energy storage systems (a) direct connection to the dc-link, (b) connection to the dc-link through a dc-dc converter, (c) proposed battery/supercapacitor direct integration scheme.

The major problem with this unique approach is the imminent imbalance of the neutral point potential due to unequal states of charge of the battery bank and the supercapacitor bank. Comprehensive analysis on capacitor voltage imbalance and balancing techniques used in standard diode-clamped inverters can be found in literature [101] [102]. But only a few papers have discussed the operation under two independent voltage sources [103] [104]. A similar topology has been proposed in [105] for photovoltaic systems. The solution proposed there is based on SPWM with carrier amplitude modification which is proved in section 3.2.2 to be effective only for small and slow changes in dc-link voltages. Furthermore, the control flexibility over small vector is limited in the above method.

Taking these facts into account, a new SVM method has been developed for diode-clamped three level inverters with variable dc-link voltages. Furthermore, full controllability over small vector selection is available in the proposed SVM method. Relevant equations and diagrams are presented in the section 3.2.3 with detailed descriptions. The proposed SVM technique requires more computations compared to simplified SVM techniques proposed in literature. These computations are unavoidable since the triangles of the space vector diagram deviate from equilateral shape, which is exploited in simplified SVM techniques, into more general triangles without simple relations. However, these calculations do not create significant burdens on new digital

controllers such as FPGA, DSP, and microcontroller etc. Therefore, the proposed SVM technique is not unrealistic.

An analysis on battery changing/discharging process and the effects of small vectors on the charging/discharging process are presented in section 3.2.4. Suitable state of charge (SoC) balancing methods and power sharing controllers are presented in section 3.2.5. Experimental results are presented in section 3.2.6 to verify the efficacy of proposed topologies, modulation and control techniques.

3.2.2 Effects of unbalanced dc-link voltages

For the diode-clamped three level inverter, shown in Fig. 3.3(c), line to ground voltages can be derived from switching states S_a, S_b, S_c and the results are given in Table 3.1. In Table 3.1, S_a, S_b and S_c are the switching states of the inverter legs a, b and c respectively. They can take values of 0, 1 or 2. As an example, the values 0, 1 and 2 for leg a means the lower pair of switches (S_{a3} and S_{a4}), the middle pair of switches (S_{a2} and S_{a3}) and the upper pair of switches (S_{a1} and S_{a2}) of the leg a are turned on respectively. If the inverter is connected to a balanced three phase load, corresponding phase voltages can be derived from line to ground voltages using (3.1). Then these phase voltages are transformed into the $d-q$ reference frame using (3.2) and the resultant coordinates for the vectors in sector 1 are given in Table 3.2.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (3.1)$$

$$\begin{bmatrix} v_d \\ v_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3.2)$$

Table 3.1. Switching states and line to ground voltages

Switching states $S_a S_b S_c$	IGBT Switching Sequence of the leg (Top to Bottom)	Line to ground voltages $v_{ag} v_{bg} v_{cg}$
0	0011	0
1	0110	V_L
2	1100	$V_L + V_U$

Table 3.2. d - q axis coordinates of vectors in sector 1

Vector	Vector type	d axis coordinate, x_n	q axis coordinate, y_n
000	Zero	0	0
100	Negative small	$2V_L/3$	0
110	Negative small	$V_L/3$	$V_L/\sqrt{3}$
211	Positive small	$2V_U/3$	0
221	Positive small	$V_U/3$	$V_U/\sqrt{3}$
200	Large	$2(V_L + V_U)/3$	0
220	Large	$(V_L + V_U)/3$	$(V_L + V_U)/\sqrt{3}$
210	Medium	$(V_L + 2V_U)/3$	$V_L/\sqrt{3}$

According to the values in Table 3.2, locations of small and medium vectors vary with dc-link voltages as shown in Fig. 3.4. However, locations of large vectors depend only on the total dc-link voltage and thus would remain unchanged if it is constant. When capacitor voltages are balanced, positive and negative small vectors coincide and only one inner hexagon is formed as shown in Fig. 3.4(b). Furthermore, medium vectors reach mid points of the outer hexagon. If an imbalance is present, small vectors split and two separate inner hexagons appear as shown in Fig. 3.4(a) or Fig. 3.4(c). Moreover, medium vectors move towards large vectors. Size of the inner hexagon formed with negative small vectors depends on the battery voltage which is nearly constant in the proposed system. Similarly, size of the inner hexagon formed with positive small vectors varies with the supercapacitor voltage. The circles marked with dotted lines in Fig. 3.4 represent the path of the reference voltage vector. In the proposed method, supercapacitor voltage is allowed to vary in a way that this circle will always remain within the outer hexagon and middle inner hexagon.

Fig. 3.4. Space vector diagram for (a) $V_U (=V_{sc}) < V_L (=V_b)$, (b) $V_U = V_L$, (c) $V_U > V_L$.

Modulation and voltage balancing control of diode-clamped three level inverters are well documented in literature [106]-[110]. However, all reported modulation methods such as SVPWM, SPWM, and THPWM are supposed to work under balanced conditions. If an unavoidable imbalance occurs, these modulation methods fail to produce desired outputs. This effect is illustrated in Figs. 3.5(c) and 3.5(d) where the capacitor voltages are purposely changed according to Fig. 3.5(a). If the normal SPWM with two equal carriers as shown in Fig. 3.5(b) is used, a dc offset will be present in the inverter output voltage. This effect is clearly visible in the filtered output voltage shown in Fig. 3.5(d). As a solution to this problem, a feed-forward SPWM method is proposed in [111] where the carriers are modified in proportion to the voltage imbalance as shown in Fig. 3(e).

Fig. 3.5. Effects of dc-link voltage imbalance (a) changes applied to capacitor voltages, (b) symmetric carriers for normal SPWM, (c) inverter output voltage of the a -phase, v_{as} , with equal carriers, (d) filtered output voltage with dc offset, (e) modified carriers, (f) inverter output voltage of the a -phase, v_{as} , with modified carriers, (g) filtered output voltage without dc offset, (h) inverter output voltage of the a -phase, v_{as} , with the proposed SVM technique.

Even though this modified SPWM technique is capable of producing undistorted output voltages as in Fig. 3.5(g), voltage stresses on switching devices goes up for large imbalance conditions as depicted in Fig. 3.5(f). This is mainly due to the absence of full control over small vectors. Therefore, a novel space vector modulation method has been developed, from the scratch, to reduce voltage stresses and produce desired outputs even

at large imbalanced conditions. The result of the proposed SVM technique is shown in Fig. 3.5(h). Its filtered output voltage waveforms are very similar those shown in Fig. 3.5(g) and hence not shown here. A detailed description of the proposed SVM technique is given in the following section.

3.2.3 Proposed space vector modulation technique

A simplified block diagram of the proposed SVM technique is illustrated in Fig. 3.6. The amplitude r and the phase angle θ of the reference voltage vector are generated by the grid side inverter controller. Currently serving sector of the space vector diagram is derived from the phase angle according to the sector selection criterion given in Table 3.3. After selecting the sector, the next step is to select the suitable triangle out of the two candidate triangles, formed with upper and lower small vectors respectively. Selection of the proper triangle is a function of the charge/discharge controller which is discussed in the next section. However, due to the presence of two candidate triangles, four different limit angles, θ_1 , θ_2 , θ_3 , and θ_4 , are needed to calculate for a given sector. First two limit angles, θ_1 and θ_2 , are related to the triangles formed with lower small vectors as shown in Fig. 3.7(a) whereas the other two limit angles, θ_3 and θ_4 , are associated with the triangles formed with positive small vectors as shown in Fig. 3.7(b).

Fig. 3.6. Simplified block diagram of the proposed SVM technique.

Table 3.3. Sector selection criteria

Angle, θ	$0 < \theta \leq 60$	$60 < \theta \leq 120$	$120 < \theta \leq 180$	$180 < \theta \leq 240$	$240 < \theta \leq 300$	$300 < \theta \leq 360$
Sector	1	2	3	4	5	6

Fig. 3.7. Limit angles for sector 1 (a) limit angles for triangles formed with lower small vectors, (b) limit angles for triangles formed with upper small vectors.

For the simplicity of subsequent calculations, dc-link voltages are transformed into two temporary variables x and y using (3.3). They are directly related to the lengths of triangles as marked in Fig. 3.7. Limit angles are calculated using (3.4)–(3.8) where α is an intermediate variable. The limit angles given in (3.5)–(3.8) are valid only for the sector 1. Limit angles for the other sectors can be derived from these values with the help of Table 3.4. Once the limit angles are calculated, the triangle and corresponding three vectors can easily be derived.

$$x = \frac{2}{3}V_U, y = \frac{2}{3}V_L \quad (3.3)$$

$$\alpha = \sin^{-1} \left(\frac{\sqrt{3}y}{2\sqrt{(x+y)^2 - 3xy}} \right) \quad (3.4)$$

$$\theta_1 = \alpha - \sin^{-1} \left(\frac{\sqrt{3}y^2}{2r\sqrt{(x+y)^2 - 3xy}} \right) \quad (3.5)$$

$$\theta_2 = \sin^{-1} \left(\frac{\sqrt{3}y}{2r} \right) \quad (3.6)$$

$$\theta_3 = \frac{\pi}{3} - \sin^{-1} \left(\frac{\sqrt{3}x}{2r} \right) \quad (3.7)$$

$$\theta_4 = \alpha - \frac{\pi}{3} - \sin^{-1} \left(\frac{x}{r} \sin \left(\alpha - \frac{2\pi}{3} \right) \right) \quad (3.8)$$

Table 3.4. Limit angles for sectors 1-6

Sector	θ_1^*	θ_2^*	θ_3^*	θ_4^*
1	θ_1	θ_2	θ_3	θ_4
2	$2\pi/3 - \theta_2$	$2\pi/3 - \theta_1$	$2\pi/3 - \theta_4$	$2\pi/3 - \theta_3$
3	$2\pi/3 + \theta_1$	$2\pi/3 + \theta_2$	$2\pi/3 + \theta_3$	$2\pi/3 + \theta_4$
4	$4\pi/3 - \theta_2$	$4\pi/3 - \theta_1$	$4\pi/3 - \theta_4$	$4\pi/3 - \theta_3$
5	$4\pi/3 + \theta_1$	$4\pi/3 + \theta_2$	$4\pi/3 + \theta_3$	$4\pi/3 + \theta_4$
6	$2\pi - \theta_2$	$2\pi - \theta_1$	$2\pi - \theta_4$	$2\pi - \theta_3$

After finding the three vectors, the next step is to determine switching times. According to the well known volt-second balancing principle, a given reference vector can be synthesized with three adjacent vectors. Equations (3.9) and (3.10) provide the mathematical description of this process. Equations (3.11)-(3.14) are used to calculate corresponding switching times d_1 - d_3 which are expressed as fractions of the sampling time [93], [112]. In (3.11)-(3.14), x_n, y_n ($n = 0..3$) are the coordinates of vector points.

$$\bar{V}_r = d_1 \bar{V}_1 + d_2 \bar{V}_2 + d_3 \bar{V}_3 \quad (3.9)$$

$$d_1 + d_2 + d_3 = 1 \quad (3.10)$$

Where V_r is the reference vector and V_1, V_2 , and V_3 are the three adjacent vectors as shown in Fig. 3.8.

Fig. 3.8. Reference vector, three nearest vectors and their coordinates.

$$\Delta = (x_1 y_2 - x_2 y_1) + (x_2 y_3 - x_3 y_2) + (x_3 y_1 - x_1 y_3) \quad (3.11)$$

$$d_1 = (x_0 (y_2 - y_3) + y_0 (x_3 - x_2) + (x_2 y_3 - x_3 y_2)) / \Delta \quad (3.12)$$

$$d_2 = (x_0 (y_3 - y_1) + y_0 (x_1 - x_3) + (x_3 y_1 - x_1 y_3)) / \Delta \quad (3.13)$$

$$d_3 = (x_0 (y_1 - y_2) + y_0 (x_2 - x_1) + (x_1 y_2 - x_2 y_1)) / \Delta \quad (3.14)$$

According to the block diagram shown in Fig. 3.6, the next step is the generation of switching signals. Since this part is very common for most SVM techniques it is not explained here [113] [114].

3.2.4 Analysis of the charging/discharging process and small vector selection

The key factor which determines whether the battery and/or supercapacitor get charged or discharged is the power difference. If the power captured from the wind is higher than the demand, the surplus power will be directed to the battery and/or the supercapacitor bank. Similarly, if there is a deficit of power it will be replenished by discharging stored energy of the battery and/or supercapacitor. However, power sharing between the battery and the supercapacitor heavily depends on the small vector selection criteria. To describe this in simple terms a set of equivalent circuits, shown in Fig. 3.9, at different vector combination are used. In this analysis front end of the wind energy conversion is modeled as a current source and the power factor (output) is assumed to be 1. According to the equivalent circuit shown in Fig. 3.9(a), both supercapacitor and the battery get charged with the same charging current if the available power is higher than the demand and a large vector is selected. Corresponding current magnitudes are given in Table 3.5 where Z is the equivalent per phase impedance. For the same power condition, current directions for a medium vector are marked in Fig. 3.9(b). According to current equations in Table 3.5 if the supercapacitor voltage is higher than the battery voltage (i.e. $V_U > V_L$) current through the b -phase is positive ($i_b > 0$) at medium vectors. Furthermore, if $i_b > 0$ charging current of the battery is higher than that of the supercapacitor bank. But if the supercapacitor voltage is lower than the battery voltage, current through the load terminal 'b' gets reversed and consequently the battery current gets reduced.

Table 3.5. Phase currents and battery current when there is a surplus of power

Vector	i_a	i_b	i_c	I_B
Large vector 200	$2(V_U + V_L)/3Z$	$V_U + V_L/3Z$	$V_U + V_L/3Z$	i_{sc}
Medium vector 210	$2V_U + V_L/3Z$	$V_U - V_L/3Z$	$V_U + 2V_L/3Z$	$i_{sc} + i_b$
Upper small vector 211	$2V_U/3Z$	$V_U/3Z$	$V_U/3Z$	$i_{sc} + i_a$
Lower small vector 100	$2V_L/3Z$	$V_L/3Z$	$V_L/3Z$	$i_{sc} - i_a$

Fig. 3.9. Equivalent circuits and current directions at (a) (e) large vectors, (b) (f) medium vectors, (c) (g) upper small vectors, (d) (h) lower small vectors.

Equivalent circuits for upper and lower small vectors are shown in Fig. 3.9(c) and Fig. 3.9(d) respectively. Corresponding current magnitudes can be determined using equations given in the last two rows of Table 3.5. According to these equations it can be deduced that the battery current is large at upper small vectors and low at lower small vectors. Therefore, wide use of upper small vectors (method *a* in Table 3.8) produces a large battery current as shown by the trace *U* in Fig. 3.10(a). Similarly, if lower small vectors

are widely used (method *b* in Table 3.8) the battery current becomes low as shown by the trace *L* in Fig. 3.10(a). Therefore, it is possible to change the battery current by changing the small vector composition. Corresponding supercapacitor voltage variations are shown in Fig. 3.10(b). This graph implies that increased use of lower small vectors results in a high rate of charge of the supercapacitor compared to increased use of upper small vectors.

Fig. 3.10. (a) Battery current variations when there is a surplus of power (b) supercapacitor voltage variations for upper and lower small vectors

A similar analysis can be carried out for the situation where available wind power is less than the demand. The corresponding equivalent circuits are shown in Figs. 3.9(e) to 3.9(h). At large and medium vectors both supercapacitor and battery get discharged as shown in Figs. 3.9(e) and 3.9(f). But according to the current equations in Table 3.6 if the supercapacitor voltage is higher than the battery voltage it is possible to let some current to flow into the battery at medium vectors. Furthermore, at upper small vectors battery experiences a charging current as shown in Fig. 3.9(g) and its magnitude can be determined using the equations given in Table 3.5. At lower small vectors, supercapacitor experiences a charging current while the battery gets discharged. Therefore, if more upper small vectors are used, supercapacitor gets discharged rapidly while lowering the discharging current of the battery as shown by trace *U* in Figs. 3.11(a) and 3.11(b). Further analysis of Fig. 3.11 reveals that even if the battery current is low it tends to increase as the supercapacitor voltage drops. The wide use of lower small vectors results in slow discharge of the supercapacitor while the battery gets discharged rapidly as shown by trace *L* in Fig. 3.11. A summary of this analysis is given in given in the Table 3.7.

Table 3.6. Phase currents and battery current when there is a deficit of power

Vector	i_a	i_b	i_c	I_B
Large vector 200	$2(V_U + V_L)/3Z$	$V_U + V_L/3Z$	$V_U + V_L/3Z$	i_{sc}
Medium vector 210	$2V_U + V_L/3Z$	$V_U - V_L/3Z$	$V_U + 2V_L/3Z$	$i_{sc} + i_b$
Upper small vector 211	$2V_U/3Z$	$V_U/3Z$	$V_U/3Z$	$i_a - i_{sc}$
Lower small vector 100	$2V_L/3Z$	$V_L/3Z$	$V_L/3Z$	$i_a - i_{sc}$

Fig. 3.11. (a) Variations of the battery current when there is a deficit of power (b) supercapacitor voltage variation for upper and lower small vectors.

Table 3.7. Charge/discharge rates at upper and lower small vectors

Power condition	Upper small vectors		Lower small vectors	
	Battery current	Rate of change of supercapacitor voltage	Battery current	Rate of change of supercapacitor voltage
$P_{in} > P_{demand}$	Charging High	Charging Low	Charging Low	Charging High
$P_{in} < P_{demand}$	Discharging Low & vary	Discharging High	Discharging High	Discharging Low

With the help of Table 3.7, number of small vector selection methods can be developed to suit different operating conditions. Out of these methods, the most prominent three are listed in Table 3.8 with required dc offsets which should be added to the reference signals of the modulator. In order to test the performance of each method a simulation was carried out with the input power profile shown in Fig. 3.12(a). The corresponding battery current variations and capacitor voltage variations are shown in Figs. 3.12(b) and 3.12(c) respectively.

Table 3.8. Small vector selection methods

Notation	Small vector selection method	DC offset to be added to the reference (m -modulation index)
a	More upper vectors	$1-m$
b	More lower vectors	$-(1-m)$
c	Controlled through a PI controller	Upper limit $(1-m)$ Lower limit $-(1-m)$

Fig. 3.12. Performance of small vector selection methods (a) input power and output power, (b) battery current variations for different small vector selection methods a , b and c , (c) corresponding capacitor voltage variations.

The first method, named as a , uses more upper small vectors and charges the battery at the highest rate as shown by the trace a in Fig. 3.12(b). At the same time supercapacitor experiences heavy discharge as depicted by the trace a in Fig. 3.12(c). This method is suitable for charging the battery when it is at a low SoC or discharging the supercapacitor when it is reaching the upper limit. The second method, named as b , discharges the battery at a high rate compared to the charging rate. As a result, there is a net energy discharge from the battery. Consequently, supercapacitor shows a net increase of its stored energy as shown by the trace b in Fig. 3.12(c). Therefore, this method can be used

to discharge the battery or restore the supercapacitor voltage when it reaches the lower limit. According to the traces in Fig. 3.12(b) it can be concluded that the method *a* and *b* sets the lower and upper limits for battery current respectively. With the change of the dc offset, added to the reference signals, it is possible to change the battery current within these two limits.

The main objective of coupling batteries and supercapacitors is to reduce current stresses in the batteries and thus to reduce their size and improve lifetime. Therefore, fast charging and discharging of the battery should be avoided. In other words battery current fluctuations should be reduced to the minimum possible level under fast changing input conditions. In order to achieve this objective a PI controller is used to generate the dc offset in the third method, which is named as *c*. This method reduces the battery current and diverts input fluctuations to the supercapacitor as shown by the traces marked with *c* in Figs. 3.12(b) and 3.12(c). This implies that the supercapacitor compensates fast changes in the input power. In this simulation battery current reference was set to zero and hence the combined energy storage system suppresses only short term fluctuations. When it is required to handle long term fluctuations it can be achieved by changing the battery current reference to a suitable positive or negative value. In summary, it can be concluded that the method *c* is the main small vector selection criteria which can be used to reduce current stresses in the battery while the methods *a* and *b* can be used occasionally for rapid charging of the battery and the supercapacitor respectively. The above analysis can equally be extended for the remaining two cases where dc-link capacitors are replaced with two supercapacitor banks or two battery banks.

3.2.5 SoC Balancing and power reference adjustment

A. DC-Link capacitors are replaced with two battery banks

When batteries are at different states of charge, power sharing should also be changed accordingly. In other words the battery at a high state of charge should discharge more power when there is a deficit. Similarly, when there is a surplus of power the battery with a low state of charge should be given priority to absorb more power. This can be achieved with the proper selection of upper and lower small vectors. For an example, if the lower battery is at a lower SoC compared to the upper battery, it should be given priority under

charging conditions. This can be done by using more upper small vectors than lower small vectors. Similarly, to charge the upper battery, lower small vectors should be used at a higher rate than upper small vectors. A PWM based SoC balancing controller is proposed to adjust the small vector composition as shown in Fig. 3.13. The PI controller generates an offset based on the SoC difference. If the offset is zero, both upper and lower small vectors are selected at an equal rate. Sign of the PI controller output is altered according to (3.15) to reflect the difference of power.

Fig. 3.13. SoC balancing controller block diagram.

$$Sgn_{power} = \begin{cases} +1 & P_{wind} > P_{demand} \\ 0 & P_{wind} = P_{demand} \\ -1 & P_{wind} < P_{demand} \end{cases} \quad (3.15)$$

B. DC-Link capacitors are replaced with two supercapacitor banks

The same SoC balancing controller, shown in Fig. 3.13, is valid even when dc-link capacitors are replaced with two supercapacitor banks. To protect supercapacitor banks from over charging and over discharging a power reference adjustment can be used as shown in Fig. 3.14 [97]. If the SoC of the supercapacitor bank is above 80%, a gradual increase is introduced to the output power reference. This in turn reduces the charging rate. On the other hand if the SoC of the supercapacitor bank is below 20%, a gradual decrease is introduced to the output power reference. This will slow down the discharging process. In all the other possible situations, the original power reference, calculated using the exponential moving average (EMA) formula [97], is used. This particular power reference adjustment ensures that the supercapacitor bank remains in operation at all times and a sufficient amount of energy to smoothen power fluctuations is securely maintained. Moreover, it protects the supercapacitor bank from over charging and over discharging.

Fig. 3.14. Reference multiplication factor.

C. Lower dc-link capacitors is replaced with a battery bank and the upper dc-link capacitor is replaced with a supercapacitor bank

As mentioned earlier the main objective of coupling batteries and supercapacitors is to reduce current stresses in the battery bank. The same controller, shown in Fig. 3.13, can be used for this particular purpose as well. However, in this case, the two inputs, SoC_L and SoC_U , should be supplied with the battery current and its reference instead of SoC values. A simulation was carried out to show the efficacy of this method in diverting short term power fluctuations to the supercapacitor bank. Circuit diagram of the simulation setup is shown in Fig. 3.15(a).

A programmable dc current source is used to generate the input power profile, P_{in} , as shown in Fig. 3.15(b). Output power is maintained at a constant level, marked as P_{out} , as shown in the same graph. Variations of the battery power and supercapacitor power are shown by the traces marked as P_{bl} and P_{sc} respectively. Corresponding battery and supercapacitor current variations are shown in Fig. 3.15(c) which proves the ability of the proposed method to protect the battery from current pulses. In Fig. 3.15(d) battery and supercapacitor voltage variations are shown to verify the absorption of short term power fluctuations by the supercapacitor bank. Reference voltage and inverter output voltage waveforms are shown in Figs. 3.15 (e) and 3.15 (f) respectively. This waveform, together with the inverter output current waveform shown in Fig. 3.15 (g), proves the ability of the proposed SVM technique to produce undistorted current even under unbalanced conditions.

In this simulation, the method c of Table 3.8 is used for small vector selection. The battery current reference is set to zero and hence the combined energy storage system suppresses only short term fluctuations. If there is a long term fluctuation, that can be suppressed by changing the battery current reference to a suitable positive value or a negative value. A detailed comparison on power losses of the proposed direct integration scheme and the conventional dc-dc converter based approach can be found in [128].

(a)

(b)

(c)

(d)

Fig. 3.15 (a) Schematic diagram of the simulation setup, (b) input, load, supercapacitor and battery power, (c) input, battery and supercapacitor current, (d) battery and supercapacitor voltage, (e) reference voltage for the a -phase, (f) inverter output voltage, (g) inverter output current.

3.2.6 Experimental results

Experimental validations of the proposed power sharing technique for the battery-supercapacitor hybrid energy storage system are shown in Fig. 3.16. Photographs of the experimental setup are shown in Fig. 3.16(a). System parameters of the experimental setup are given in Table 3.9. A variable ac source (California Instruments 4500Ls, 4.5kW) is used to generate an input power profile, P_{in} , as shown in Fig. 3.16(b). Output power level is maintained at a constant level, marked as P_{out} , as shown in the same graph. Battery and supercapacitor voltages are shown in Fig. 3.16(c). Due to the absorption of input power fluctuations, supercapacitor voltage varies from 70V to 95V. The method c in Table 3.8 is used in the experiment as well to select proper small vectors which reduces current stresses on the battery. The corresponding battery and supercapacitor current variations are shown in Fig. 3.16(d). It is evident from the above power and current waveforms that the supercapacitor bank absorbs fluctuations making the battery current small and smooth. Inverter output voltage waveform is shown in Fig. 3.16(e). This waveform, together with the inverter output current waveform shown in Fig. 3.16(f), proves the efficacy of the proposed SVM method to handle dc-link voltage imbalances.

Even though fluctuations are present in the input power, output voltage and current waveforms are not affected.

(a)

(b)

(e)

(c)

(f)

(d)

Fig. 3.16. (a) Photographs of the experimental setup, (b) input, load, supercapacitor and battery power, (c) battery and supercapacitor voltages, (d) input, battery and supercapacitor currents, (e) inverter output voltage, (f) inverter output current.

Table 3.9. System parameters of the experimental setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency	$f_s = 2.5\text{kHz}$
Load resistance	$R = 10\Omega$
Load inductance	$L = 6\text{mH}$
Nominal battery voltage	$V_L = 83\text{V}$
Supercapacitor voltage (maximum)	$V_{sc,max} = 95\text{V}$
Supercapacitor voltage (minimum)	$V_{sc,min} = 70\text{V}$
Capacitance of the supercapacitor bank	$C_{sc} = 34\text{mF}$
Number of capacitors	5

3.3 Capacitor-clamped three-level grid-side inverter

The circuit topology of the capacitor-clamped three-level inverter topology is shown in Figure 3.17(a). The structure of this inverter is similar to that of the diode-clamped three-level inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The corresponding space vector distribution is shown in Figure 3.17(b) for the balanced condition, i.e. $V_{Ca}=V_{Cb}=V_{Cc}=V_{dc}/2$. The space vector diagram of the capacitor-clamped three-level inverter is also similar to that of the diode-clamped three-level inverter under balanced conditions. Therefore, the vector description presented in section 3.2 is equally applicable. But this topology has phase redundancy compared to the line redundancy in the diode-clamped inverter [115]-[119]. This allows charging or discharging a capacitor in one leg without changing switching states of the other two legs. Therefore, capacitor voltage balancing in capacitor-clamped inverters is relatively simple and straightforward. Furthermore, it is possible to change the ratio of capacitor voltages and sacrifice this redundancy in order to improve the power quality by increasing the number of voltage levels [85], [118]. In other words the same inverter shown in Figure 3.17(a) is capable of producing four-level outputs if $V_{Ca}=V_{Cb}=V_{Cc}=V_{dc}/3$.

However, capacitor-clamped inverters are not popular in industry mainly due to the increased cost, size and failure rate of clamping capacitors. This drawback has been turned into an advantage in the following system where conventional clamping capacitors are replaced with supercapacitors to incorporate low voltage ride through and short term power smoothening capabilities to the inverter.

Fig. 3.17. (a) Schematic diagram of the capacitor-clamped three-level inverter, (b) space vector distribution for the balanced condition i.e. $V_{Ca}=V_{Cb}=V_{Cc}=V_{dc}/2$.

3.3.1 Supercapacitor direct integration

This section presents a new direct integration scheme for supercapacitors using the capacitor-clamped grid-side inverter. The proposed system is shown in Fig. 3.18 where conventional clamping capacitors are replaced with three supercapacitor banks. This particular direct integration scheme eliminates the need for interfacing dc-dc converters for supercapacitors and thus reduces the cost, complexity, power losses and response time. With the introduction of supercapacitors stability of the inverter gets improved in the fixed voltage operation. But, to acquire full benefits of supercapacitors they should be operated in the variable voltage mode. In other words, supercapacitor voltages should not be regulated and should be allowed to take any value within the safe operating region.

However, as discussed in section 2.7.3, the aforementioned variable voltage mode operation creates three major problems. Unequal blocking voltages and increased voltage slew rates (dv/dt) experienced by some switching devices as a result of unbalanced voltages is the first issue. Large band gap devices such as SiC, GaN, and thin-film diamond are expected to break the 6.5kV limit of blocking voltage in traditional Si devices and therefore in the long run this would not be a significant issue in future medium voltage wind energy conversion systems [33].

Fig. 3.18. Proposed three-level capacitor-clamped grid-side inverter with supercapacitors.

The second problem is the unequal distribution of instantaneous power losses among switching devices. As a result, some devices tend to heat more than the others. However, supercapacitor banks are used only as short-term power smoothening elements and hence their average power in a cycle is theoretically zero. That means, on average, power losses get distributed evenly among switching devices. Therefore, in the steady state, temperature of switching devices varies at the same rate. However, heat sinks should have enough capacity to protect devices from aforementioned instantaneous power losses.

The third problem is the uneven distribution of space vectors. A detailed analysis on this issue is given in the following section. Furthermore, the space vector modulation method proposed in section 3.2.3 has been improved to suit the proposed system. A supercapacitor voltage equalisation technique has also been developed for this particular system. Detailed descriptions on the proposed modulation and voltage equalization methods are given in section 3.3.3 and 3.3.4 respectively.

Another important issue of the proposed direct connection approach is the exposure of supercapacitors to high frequency switching current spikes. In fact, at high frequencies supercapacitors behave as resistors and thus expected capacitive effect is no longer available. The importance of an intermediate low pass filter stage to support supercapacitors in such situations is emphasized in section 3.3.5. Simulation and experimental results are presented in sections 3.3.6 and 3.3.7 respectively to verify the efficacy of the proposed system in suppressing short term wind power fluctuations.

3.3.2 Effects of capacitor voltage variations

Terminal voltage of a supercapacitor varies with its stored energy as shown in Fig. 3.19. Moreover, 50% reduction of supercapacitor voltage from the maximum value yields 75% discharge of the stored energy. Therefore, in order ensure maximum utilization of supercapacitors they should be allowed to operate at variable voltages, ranging from 200V to 400V for example. As mentioned before, this variable voltage operation creates three major problems and the purpose of this section is to present an analysis on the third problem that is uneven distribution of space vectors.

Fig. 3.19. Change of supercapacitor voltage with stored energy.

First step of this analysis is the definition of possible voltage levels in a capacitor-clamped three-level inverter. Line to ground voltage of each leg of the inverter can have maximum of four voltage levels. These four voltage levels, corresponding gate signals and switching states for the leg 'a' of the inverter are given in Table 3.10. The other two legs also follow the same pattern. If supercapacitor voltages are balanced, the 2nd and 3rd voltage levels (V_{sca} , and $V_{dc} - V_{sca}$) become equal and hence the total number of discrete voltage levels is reduced to three (0, $V_{dc}/2$ and V_{dc}). In this particular situation the switching states '1' and '2' produce the same line-to-ground voltage, $V_{dc}/2$. Therefore, these two states are called redundant states. Under this balanced condition, the proposed system acts as a three-level inverter. Corresponding space vector diagram is shown in Fig. 3.20(a) which is similar to Fig. 3.17(b). Equations (3.16) to (3.18) together with (3.1) are used in calculating coordinates of these vectors. Theoretically, if there are n numbers of voltage levels per leg, there are n^3 numbers of total space vectors. Accordingly, this three level inverter has a total of 3^3 (27) vectors. But due to overleaping, only 19 discrete vectors are visible in Fig. 3.20(a).

Table 3.10. Switching states and line to ground voltages

Switching state (S_a)	Gate signals (G_{a1}, G_{a4})	v_{ag}
0	0011	0
1	0101	V_{sca}
2	1010	$V_{dc} - V_{sca}$
3	1100	V_{dc}

Fig. 3.20. Space vector distribution at different supercapacitor voltage conditions (a) $V_{sca} = V_{scb} = V_{scc} = V_{dc}/2$, (b) $V_{sca} = 0.33V_{dc}$, $V_{scb} = 0.31V_{dc}$, $V_{scc} = 0.35V_{dc}$, (c) $V_{sca} = 0.66V_{dc}$, $V_{scb} = 0.64V_{dc}$, $V_{scc} = 0.68V_{dc}$.

$$\begin{bmatrix} v_{ds} \\ v_{qs} \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \quad (3.16)$$

$$V_{ds} = \frac{2}{3} \left(V_{as}S_a - \frac{1}{2}V_{bs}S_b - \frac{1}{2}V_{cs}S_c \right) \quad (3.17)$$

$$V_{qs} = \frac{1}{\sqrt{3}} (V_{bs}S_b - V_{cs}S_c) \quad (3.18)$$

If supercapacitor voltages are reduced to one third of the dc-link voltage, each leg of the inverter can produce four different voltage levels (0 , $V_{dc}/3$, $2V_{dc}/3$ and V_{dc}). Therefore, in this case, the same system operates as a four-level inverter with a space vector distribution as shown in Fig. 3.20(b). In order to differentiate each and every vector point, without overlapping, slight changes have been introduced to supercapacitor voltages. Out of 64 possible vectors 63 are visible in this diagram. The missing one is overlapped at the origin. However, if supercapacitor voltages are equal, overlapping occurs and hence out of 64 only 37 vectors appear in the space vector diagram. Similarly, if supercapacitor

voltages are increased to two third of the dc-link voltage each leg of the inverter produces same voltage levels (0 , $V_{dc}/3$, $2V_{dc}/3$ and V_{dc}). Therefore, in this case also the system operates similar to a four-level inverter with the space vector distribution shown in Fig. 3.20(c). Even though, this diagram looks very similar to Fig. 3.20(b) positions of some vectors are interchanged.

In the proposed system lower limit for the supercapacitor voltage is $V_{dc}/3$. The space vector diagram shown in Fig. 3.20(b) corresponds to this situation. Similarly, supercapacitor voltage is upper-bounded by $2V_{dc}/3$. The corresponding space vector distribution is shown in Fig. 3.20(c). When supercapacitor voltages increase from the lower limit, the inner most hexagon shown in Fig. 3.20(b), expands while the other inner hexagon shrinks. When supercapacitor voltages reach $V_{dc}/2$ both inner hexagons get overlapped as shown in Fig. 3.20(a). Further increase of supercapacitor voltage would continue the expansion and shrinking of inner hexagons which eventually ends up as in Fig. 3.20(c) at the upper limit.

For the simplicity of analysis and modulation, space vectors of the proposed flying-capacitor inverter are classified into nine groups as in Table 3.11. Out of these nine groups, the last group named as ‘Rest’ is not used in the proposed modulation method due to the complexity of corresponding vector patterns.

Table 3.11. Vector classification

Large	Upper medium	Lower medium	Upper small 1	Upper small 2
003 030 033 300 303 330	023 032 203 230 302 320	013 031 103 130 301 310	113 131 133 311 313 331	223 232 233 322 323 332
Lower small 1	Lower small 2	Zero	Rest	
001 010 011 100 101 110	002 020 022 200 202 220	000 111 222 333	012 021 102 112 120 121 122 123 132 201 210 211 212 213 221 231 312 321	

3.3.3 Modulation strategy

A simplified block diagram of the proposed SVM technique is illustrated in Fig. 3.21. The amplitude r and the phase angle θ of the reference voltage vector are determined by the grid side inverter controller. Currently serving sector of the space vector diagram is derived from the phase angle and the selection criterion is given in Table 3.3. After selecting the sector, the next step is to find a triangle with three nearest vectors. In this particular system, there are four candidate triangles for a given reference vector as a result of the two inner hexagons and two types of medium vectors available on the outer hexagon. It is noteworthy to mention here that the diode-clamped three-level inverter has only two candidate triangles for a given reference. Therefore, modulation process of the capacitor-clamped three-level inverter under unbalanced conditions is more complicated than that of the diode-clamped three-level inverter. Selection of a proper triangle from the four candidate triangles is a function of the power management and supercapacitor voltage balancing controllers which will be discussed later. However, due to the presence of four candidate triangles, eight limit angles $\theta_1.. \theta_8$, need to be calculated for a given sector. However, out of these eight angles, only four have to be calculated exclusively. The other four angles can be derived from these angles.

Fig. 3.21. Simplified block diagram of the proposed SVM technique.

First two limit angles, $(\theta_1$ and $\theta_2)$, are related to the triangles formed with the vectors on the middle hexagon as shown in Fig. 3.22(a) whereas the other two limit angles, $(\theta_3$ and $\theta_4)$, are associated with the triangles formed with vectors on the inner hexagon as shown in Fig. 3.22(b). For the simplicity of subsequent calculations, dc-side voltages are transformed into two variables x and y using (3.19). These two values are directly related to the lengths of triangles as marked in Fig. 3.22. Limit angles are calculated using (3.20)-(3.28) where α is an intermediate variable. In fact some of these equations are

equivalent to the corresponding equations in 3.2.3. However, they are repeated here as well to maintain the continuity of reading.

Fig. 3.22. Limit angles for the sector 1 (a) limit angles for triangles formed with lower small 1 and upper small 2 vectors, (b) limit angles for triangles formed with lower small 2 and upper small 1 vectors.

$$x = \frac{2}{3}(V_{dc} - V_{sc}), y = \frac{2}{3}V_{sc} \quad (3.19)$$

$$\alpha = \sin^{-1} \left(\frac{\sqrt{3}y}{2\sqrt{(x+y)^2 - 3xy}} \right) \quad (3.20)$$

$$\theta_1 = \alpha - \sin^{-1} \left(\frac{\sqrt{3}y^2}{2r\sqrt{(x+y)^2 - 3xy}} \right) \quad (3.21)$$

$$\theta_2 = \sin^{-1} \left(\frac{\sqrt{3}y}{2r} \right) \quad (3.22)$$

$$\theta_3 = \frac{\pi}{3} - \sin^{-1} \left(\frac{\sqrt{3}x}{2r} \right) \quad (3.23)$$

$$\theta_4 = \alpha - \frac{\pi}{3} - \sin^{-1} \left(\frac{x}{r} \sin \left(\alpha - \frac{2\pi}{3} \right) \right) \quad (3.24)$$

$$\theta_5 = \frac{\pi}{3} - \theta_5 \quad (3.25)$$

$$\theta_6 = \frac{\pi}{3} - \theta_2 \quad (3.26)$$

$$\theta_7 = \frac{\pi}{3} - \theta_3 \quad (3.27)$$

$$\theta_8 = \frac{\pi}{3} - \theta_4 \quad (3.28)$$

The limit angles given in (3.21)-(3.24) are valid only for the lower medium vector '310'. The corresponding limit angles for the other medium vector '320' can be derived from these values with the help of equations (3.25)-(3.28).

The aforementioned limit angles are valid only for the sector 1. Limit angles for other sectors can be derived from these angles with the help of Table 3.12. Once the limit angles are calculated the triangle and corresponding three vectors can easily be derived. After finding the three vectors the next step is to determine switching times. This part is exactly similarly to that in the section 3.2.3 and hence will not be discussed here.

Table 3.12. Limit angles for sectors 1-6

Sector	θ_1^*	θ_2^*	θ_3^*	θ_4^*
1	θ_1	θ_2	θ_3	θ_4
2	$2\pi/3 - \theta_2$	$2\pi/3 - \theta_1$	$2\pi/3 - \theta_4$	$2\pi/3 - \theta_3$
3	$2\pi/3 + \theta_1$	$2\pi/3 + \theta_2$	$2\pi/3 + \theta_3$	$2\pi/3 + \theta_4$
4	$4\pi/3 - \theta_2$	$4\pi/3 - \theta_1$	$4\pi/3 - \theta_4$	$4\pi/3 - \theta_3$
5	$4\pi/3 + \theta_1$	$4\pi/3 + \theta_2$	$4\pi/3 + \theta_3$	$4\pi/3 + \theta_4$
6	$2\pi - \theta_2$	$2\pi - \theta_1$	$2\pi - \theta_4$	$2\pi - \theta_3$

3.3.4 Supercapacitor voltage equalisation

Proposed supercapacitor voltage equalisation method is based on redundant state selection (RSS). Overlapping small vectors, shown in Fig. 3.22, provide these redundancies. For an example, small vectors (100, 322) and (200, 311), shown in Fig. 3.22, are redundant vector pairs in sector 1. Similarly, there are ten more redundant vector pairs in the other five sectors. Half of these redundant vector pairs contribute for supercapacitor charging while the other half tend to discharge supercapacitors. In other words, vectors on the middle hexagon, shown in Fig. 3.22, discharge supercapacitors while the vectors on the innermost hexagon charge supercapacitors. In order to explain this phenomena in detail four equivalent circuits, which corresponds to the aforementioned two vector pairs, are shown in Fig. 3.23. By looking at the current direction of the a -phase in Fig. 3.23(a) it can be deduced that the supercapacitor attached to leg ' a ' gets discharged at the small vector '100'. Similarly, the small vector '322'

discharges the other two supercapacitors. Therefore, with the proper combination of these two small vectors discharging rates of supercapacitors can be controlled in sector 1.

Fig. 3.23. Equivalent circuits of small vectors (a) 100, (b) 322, (c) 200, and (d) 311.

The equivalent circuit of Fig. 3.23(c) corresponds to the small vector ‘200’ which is on the innermost hexagon shown in Fig. 3.22. This vector charges the supercapacitor attached to the leg ‘a’ of the inverter. Moreover, the other vector of the pair, i.e. ‘311’, charges the other two supercapacitors as shown in Fig. 3.23(d). This indicates that frequent use of the small vector ‘200’ charges the supercapacitor C_{sca} at a higher rate than that of the other two. Opposite of this happens if the vector ‘311’ is used. The proposed supercapacitor voltage equalization method is based on this particular scenario. The corresponding controller block diagram and the lookup table are shown in Fig. 3.24 and Table 3.13 respectively.

Voltage equalizer, shown in Fig. 3.24, measures supercapacitor voltages at every switching cycle and sort them in ascending order. Output of the min-max sorting block is an index which assigns a priority for the most deviated phase. The most deviated phase is selected as follows. If the supercapacitor C_{scc} attached to the leg ‘c’ of the inverter shows the lowest voltage and the system is in the charging mode, phase ‘c’ is given the priority by setting the index to 3. Then Table 3.13 is used to select suitable small vector for the current sector which in turn increases the charging rate of the supercapacitor C_{scc} .

Similarly, if the system operates in the discharging mode and the supercapacitor C_{scb} , attached to the leg ‘b’ of the inverter shows the highest voltage, it will be discharged at a higher rate compared to the other two. This is done by setting the value of the index to 2. This time small vectors are picked up from the discharging row under index 2 of Table 3.13. If the supercapacitor C_{sca} , is to be given a priority, index should be set to 1.

Fig. 3.24. Block diagram of the supercapacitor voltage equalizer.

Table 3.13. Lookup table for small vector selection

Sector			1	2	3	4	5	6
Phase with priority			<i>a</i>	<i>c</i>	<i>b</i>	<i>a</i>	<i>c</i>	<i>b</i>
Index	1	Charge	200	220	020	133	113	202
		Discharge	100	110	232	233	223	101
	2	Charge	311	220	020	022	113	313
		Discharge	322	332	020	011	223	323
	3	Charge	311	331	131	022	002	202
		Discharge	322	332	232	011	001	101

A computer simulation was carried out to test the efficacy of the proposed supercapacitor voltage equalization method under charging and discharging conditions. Input power to the system was varied as shown in Fig. 3.25(a) by the trace marked as P_{in} . Output power was maintained at a constant level as shown by the trace P_{out} in the same figure. Slight changes have been introduced to the initial voltages of supercapacitors as shown in Fig. 3.25(b) to show the efficacy of the proposed equalisation method. According to Fig. 3.25(b) the supercapacitor C_{scb} has the largest initial voltage and the supercapacitor C_{scc} has the lowest initial voltage. The supercapacitor C_{sca} possesses a mid value as its initial voltage. As shown in Fig. 3.25(a) there is a deficit of power during first 200 ms and thus supercapacitors are discharged to meet the demand as shown in Fig. 3.25(b). However, their discharging rates are not equal. The supercapacitor C_{scb} , which shows the largest

voltage, releases more power than the other two and hence it has the highest rate of decrease of voltage as shown in Fig. 3.25(b). This condition is achieved by setting the index to 2 as shown in Fig. 3.25(c). On the other hand the supercapacitor C_{scc} discharges the least amount of power during first 200ms and hence it shows the lowest rate of decrease of voltage. Voltage of the supercapacitor C_{sca} decreases at an intermediate rate. The corresponding supercapacitor power variations are shown in Fig. 3.25(d). The end result of this operation is the convergence of supercapacitor voltages to a balanced condition as shown in Fig. 3.25(b). This validates the efficacy of the proposed supercapacitor voltage equalization technique under the discharging condition.

Fig. 3.25. Supercapacitor voltage equalization (a) input power and output power, (b) supercapacitor voltage, (c) variations of the index value, (d) supercapacitor power.

There is a surplus of power during the last 200ms period and hence supercapacitors get charged as shown in Fig. 3.25(b). However, supercapacitor voltages are still not equalized. Therefore, their charging rates take different values as depicted in Fig. 3.25(b). Supercapacitor C_{scc} shows the lowest voltage and thus it is given the priority to get charged at an increased rate by setting the index to 3.

When the voltage of supercapacitor C_{scc} , reaches that of the supercapacitor C_{sca} , charging rates of both supercapacitors should be equal. This is done by switching the index value between 1 and 3 as shown in Fig. 3.25(c). Finally, all three voltages become equal as shown in the latter part of Fig. 3.25(b). When that happens index value is switched among 1, 2 and 3 as shown in Fig. 3.25(c) to maintain an equal charging rate. The corresponding supercapacitor power variations are shown in Fig. 3.25(d). This confirms the ability of the proposed method to equalize supercapacitor voltages under the charging condition.

3.3.5 Supercapacitor sizing and implementation issues

The main cause of power fluctuations is the change of wind speed. Therefore, capacity of the energy storage system is also a function of the wind speed variation. In order to analyze this relationship wind is modeled as the sum of a dc quantity and a series of harmonics as in (3.29) [119]. Power captured from wind can be expressed as (3.30).

$$v_w(t) = V_{w0} + \sum \Delta V_{wi} \sin(\omega_i t) \quad (3.29)$$

$$P = 0.5 \rho A C_p v_w^3 \quad (3.30)$$

Where V_{w0} is the mean wind speed, ΔV_{wi} is the harmonic amplitude, ω_i is angular frequency ($f=0.1\sim 10\text{Hz}$), ρ is the density of air, A is the swept area of blades and C_p is the coefficient of power conversion

In the following analysis wind power fluctuation is assumed to be 30% of the mean value. This fluctuation should be compensated by the energy storage system. Therefore, the supercapacitor ESS should be rated according to (3.31). Capacity of the SESS should be determined for the lower frequency of the wind harmonic ($f=0.1\text{Hz}$). Therefore, energy stored in supercapacitors can be expressed as in (3.32). In the proposed system

supercapacitor voltages are allowed to vary between 400-800V. Therefore, minimum capacitance of each supercapacitor is determined using (3.33).

$$P_{sc} = 0.3P_{mean} \quad (3.31)$$

$$E_{sc} = \int_0^5 P_{sc} \sin(0.2\pi) dt \quad (3.32)$$

$$C_{sc} = \frac{20P_{sc}}{3\pi(800^2 - 400^2)} \quad (3.33)$$

In the following simulation mean power of the wind is taken as 500kW. Therefore, the required minimum capacitance of each supercapacitor becomes 0.667F. This capacitance is a feasible value. However, an implementation issue arises with the voltage since the maximum voltage of supercapacitor modules is 2.5V. Therefore, the proposed system requires at least 360 modules to be connected in series per leg of the inverter. In that case size and weight of supercapacitors would not be suitable for in-tower implementation. Furthermore, supercapacitors behave as resistors at high frequencies (typically beyond few tens of Hz) [120]. Therefore, the proposed system requires three electrolytic capacitors as well to support supercapacitors at high frequencies.

3.3.6 Simulation results

The proposed supercapacitor direct integration scheme has been tested using computer simulations on MATLAB/SIMULINK platform for an RL load. System parameters of the simulation setup are given in Table 3.14. Input power profile is shown in Fig. 3.26(a) by the trace marked as P_{in} . This corresponds to the aforementioned worst case scenario. Output power, P_{out} , was maintained at a constant level and variations of the input power are absorbed by the SESS. The corresponding main inverter dc-link voltage and the supercapacitor voltage variations are shown in Fig. 3.26(b). Supercapacitor currents are shown in Fig. 3.26(c). Filtered inverter output voltage, $v_{as,f}$ and current, i_{as} , are shown in Figs. 3.26(d) and 3.26(e) respectively. These waveforms prove the ability of the proposed space vector modulation method to generate balanced and undistorted currents even under unbalanced and dynamically changing conditions. Furthermore, enlarged views of the inverter output voltage v_{as} , are shown in Figs. 3.26(f) and 3.26(g) for unbalanced and balanced supercapacitor voltage conditions respectively. Even though some irregularities

are observable in the inverter output voltage under unbalanced conditions output currents are smooth and sinusoidal as shown in Fig. 3.26(e).

(a)

(b)

(c)

(d)

(e)

(f)

Fig. 3.26. (a) Input, output and supercapacitor power, (b) dc-link voltage variations, (c) filtered supercapacitor currents, (d) inverter output voltage after filtering, (e) inverter output current, (f) inverter output voltage when $V_{sc} = 800\text{V}$, (g) inverter output voltage when $V_{sc} = 600\text{V}$.

Table 3.14. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency	$f_s = 5\text{kHz}$
Load resistance	$R = 0.87\Omega$
Load inductance	$L = 1\text{mH}$
Capacitance of supercapacitors	$C_{scx} = 700\text{mF}$
Range of supercapacitor voltage	$V_{scx} = 400\text{-}800\text{V}$
Inverter output voltage	$v_{abs} = 0.69\text{kV}$
DC-Link voltage	$V_{dc} = 1200\text{V}$
Rated power of the PMSG	1MW

3.3.7 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 3.27(a) and 3.27(b) respectively. System parameters of the experimental setup are given in Table 3.15. A large capacitor bank is used to emulate the high capacitance of the supercapacitor energy storage system. Two sets of experimental results are presented to show the performance of the proposed modulation method and the power smoothing capability in Figs. 3.28 and 3.29 respectively. In the first set of results dc-link voltage was maintained at 160V while the capacitor voltages V_{sca} , V_{scb} and V_{scc} were kept at 80V, 96V and 64V respectively as shown in Figs. 3.28(a) and 3.28(b). The corresponding load voltage and current in the a -phase are shown in Figs. 3.28(c) and 3.28(d) respectively to illustrate the efficacy of the proposed modulation method in generating undistorted outputs even under unbalanced capacitor voltage conditions.

In the second set of results, input power was varied as shown in Fig. 3.29(a) while maintaining a constant output power at the load. Fluctuations present in the input get absorbed by flying-capacitors as shown in Fig. 3.29(b). This diagram shows the power variation of one capacitor bank which is attached to the leg a of the inverter. The other two capacitor banks also follow the same variation. This proves the ability of the proposed system to absorb fluctuations present in the input power and deliver smooth output. Furthermore, initial voltages of flying-capacitors were set to different values as shown in Fig. 3.29(c). The imbalance between capacitor voltages get decreased and eventually become equal as shown in the latter part of Fig. 3.29(c). This proves the efficacy of the proposed capacitor voltage balancing technique. The dc-link voltage was set to 160V for this experiment as well.

(a)

(a)

(b)

Fig. 3.27. (a) Schematic diagram of the experimental setup, (b) photographs of the experimental setup.

Fig. 3.28. Experimental results showing the performance of the proposed modulation method (a) dc-link voltage, (b) unequal capacitor voltages, (c) load voltage of the a -phase, (d) inverter output current of the a -phase.

Fig. 3.29. Experimental results showing the power smoothing capability (a) input power and output power, (b) average power of the capacitor, C_{sca} , attached to the leg a of the inverter (c) capacitor voltage variation.

Table 3.15. System Parameters of the Experimental Setup

Fundamental frequency	$f = 25\text{Hz}$
Switching frequency	$f_s = 2\text{kHz}$
Load resistance	$R = 25\Omega$
Load inductance	$L = 6\text{mH}$
DC-Link voltage	$V_{dc} = 160\text{V}$
Capacitance of electrolytic capacitors	$C_{sca} = 30\text{mF}$ $C_{scb} = 36.8\text{mF}$ $C_{scc} = 26.8\text{mF}$

3.4 Battery-clamped three-level grid-side inverter

This section introduces a new version of the capacitor-clamped three-level inverter topology called battery-clamped three-level inverter. The proposed inverter is shown in Fig. 3.30 where conventional clamping capacitors are replaced with three battery banks. The most advanced feature of the proposed system is the reduced battery voltage compared to the dc-dc converter based system. In dc-dc converter based systems, battery voltage should be kept in the close vicinity of dc-link voltage or else high-gain dc-dc converters have to be used. But in the proposed system, battery voltage is reduced to a half of the dc-link voltage. This reduces the number of series-connected batteries and hence reduces the effective internal resistance as well. As explained below, further reduction of battery voltage is possible with the expense of increased blocking voltage of switching devices. Furthermore, the parallel connection of three battery banks, instead of a single battery bank, increases the reliability. If one battery bank fails the other two can continue operation with the replacement of the faulty battery with a capacitor. Even if two battery banks fail the last one can still continue operation at a reduced capacity.

Fig. 3.30. Proposed battery-clamped three-level inverter.

As seen in sections 3.2.1 and 3.3.1 the major challenge with this inverter is also the unavoidable imbalance in battery voltages and resultant uneven distribution of space vectors. Moreover, battery voltage balancing is not feasible. As a solution to this problem, a novel carrier based pulse width modulation method is proposed in section 3.4.2. A charge/discharge controller is also proposed for power sharing and SoC balancing of battery banks in section 3.4.3. Simulation results are presented in section 3.4.4 to validate the proposed modulation method and power sharing controller.

3.4.1 Space vector distribution

Clamping voltages are assumed to be balanced in conventional flying-capacitor three-level inverters [121] [122]. The term ‘balanced’ means that capacitor voltages are maintained at half of the dc-link voltage. Therefore, in a balanced system capacitor voltages deem to be equal. If an imbalance or a change in capacitor voltages occurs it can be corrected by charging or discharging relevant capacitors within a short period of time. Therefore, in most publications on flying-capacitor inverters balanced clamping voltages are assumed. However, unbalanced equal systems are also proposed in literature [118]. But unbalanced unequal systems have not yet been considered.

However, in the proposed system, clamping voltages are produced by batteries and hence unbalanced and unequal voltages are unavoidable. This happens due to two reasons. The first reason is the possible differences in SoC of batteries. As shown in Fig. 3.31 terminal voltage of a battery varies with the SoC. Therefore, if batteries are at different states of charge their voltages are not equal. Furthermore, battery terminal voltages can take different values due to aging. As a result the proposed converter system is inherently unbalanced and unequal. However, as explained in section 3.4.3, there is a possibility of equalizing battery voltage by charging or discharging them at different rates. But unlike in capacitor based systems, this balancing takes a significant amount of time. Space vectors get distributed unevenly during this period and hence distortions occur in output currents. This large time constant is the second reason for the aforementioned unbalanced and unequal conditions.

Fig. 3.31. Terminal voltage variation of battery banks used in this study.

Based on the above analysis it can be concluded that the success of the proposed battery-clamped inverter heavily depends on the ability to produce desired outputs even under unbalanced and unequal battery voltage conditions. In order to achieve this objective, the

effects of unbalanced and unequal voltages should properly be understood. Therefore, the aim of this section is to present an analysis on the effects of variable clamping voltages.

The first step of this analysis is the definition of possible voltage levels in a battery clamped three-level inverter. Similar to the system discussed in section 3.3.2, this inverter also can have maximum of four voltage levels in the line to ground voltage of each leg. These four voltage levels, corresponding gate signals and switching states for the leg ‘a’ of the inverter can be found in Table 3.10. The other two legs also follow the same pattern. As explained in section 3.3.2, the 2nd and 3rd voltage levels (V_{Ba} , and $V_{dc} - V_{Ba}$) become equal and hence the total number of discrete voltage levels is reduced to three (0, $V_{dc}/2$ and V_{dc}) if battery voltages are balanced. Under this balanced condition, the proposed system acts as a three-level inverter. The corresponding space vector diagram is shown in Fig. 3.32(a). Even though this diagram has already been shown in Figs. 3.17(b) and 3.20(a) it is necessary to repeat here as well to maintain the continuity of reading. Equations (3.16)-(3.18) together with (3.1) are used here as well for calculating vector coordinates.

If the battery voltages are selected to be one third of the dc-link voltage each leg of the inverter can produce four voltage levels (0, $V_{dc}/3$, $2V_{dc}/3$ and V_{dc}). Therefore, in this case, the same system operates as a four-level inverter with the space vector pattern shown in Fig. 3.32(b). Even though it should show 4^3 (64) vectors, only 37 are visible due to overlapping as in the previous case. In the proposed system, battery voltages are assumed to be a half of the dc-link voltage. Therefore, a three level inverter is expected with a space vector diagram as shown in Fig. 3.32(a). But owing to aforementioned reasons, battery voltages can slightly deviate from their balanced operating condition. Consequently, space vectors those were overlapped in Fig. 3.32(a) get split and clusters of vectors form as shown Fig. 3.32(c). At this point the space vector distribution is totally uneven. Out of 64 possible vectors 63 are visible in this diagram. The missing one is overlapped at the origin. If the battery voltage deviations are large, the space vector distribution can reach the pattern shown in Fig. 3.32(b).

Fig. 3.32. Space vector distribution at different battery voltage conditions (a) $V_{Ba} = V_{Bb} = V_{Bc} = V_{dc}/2$, (b) $V_{Ba} = V_{Bb} = V_{Bc} = V_{dc}/3$, (c) $V_{Ba} = 0.54V_{dc}$, $V_{Bb} = 0.46V_{dc}$, $V_{Bc} = 0.38V_{dc}$.

3.4.2 Proposed modulation technique

Modulation and control of flying-capacitor three-level inverters are comprehensively discussed in literature [118], [121]-[126]. But in all these publications, balanced or equal conditions are assumed and some techniques are used to balance capacitor voltages within a few milliseconds. As a result, space vectors get distributed evenly as shown in Fig. 3.32(a) or Fig. 3.32(b). Conventional carrier based pulse width modulation (CBPWM) methods or simplified SVM methods can directly be used as the modulation method in those systems. But, as mentioned before, voltage imbalance is an unavoidable phenomenon in the proposed system. If conventional CBPWM or SVM methods are directly applied in such situations output currents get distorted.

In order to illustrate this fact a simulation was carried out and corresponding results are shown in Fig. 3.33. In this simulation, terminal voltage of the battery B_a was varied purposely from 200V to 400V while the other two are balanced at 300V as shown in Fig. 3.33(a). A simple CBPWM method with two symmetrical carriers was used as the modulation method. Fig. 3.33(b) shows the two carriers. Frequency of the carriers shown in Fig. 3.33(b) is reduced to $1/20^{\text{th}}$ for better illustration. Inverter output voltage of the a -phase is shown in Fig. 3.33(c). This waveform shows some distortions at both ends where the imbalance is significant. These distortions are clearly visible in current waveforms shown in Fig. 3.33(d). This confirms the inability of conventional modulation methods to produce undistorted output under unbalanced conditions.

Fig. 3.33. (a) Battery voltages and the dc-link voltage, (b) symmetrical carriers used in the conventional CBPWM method, (c) inverter output voltage of the a -phase, (d) output currents of the inverter.

A novel CBPWM method is proposed as a solution to this problem. The proposed CBPWM method is summarized in the block diagram shown in Fig. 3.34. The two inputs of the modulator, i.e. magnitude A_m and the angle θ of the reference voltage vector are generated by the grid-side inverter controller [93]. The proposed modulator uses these inputs to calculate corresponding phase voltage references. Equations (3.34)-(3.36) are used in these calculations. These phase voltage references are then converted into line-to-ground voltages using (3.37)-(3.39). Once the line-to-ground references are calculated, the next step is to implement the pulse width modulation. Only two symmetrical carriers, as shown in Fig. 3.33(b) are sufficient to implement CBPWM in a balanced system. But in the proposed system individual sets of carriers should be used for each leg due to dynamic changes in battery voltages. Moreover, each set of carriers should consist of four

carriers as shown in Fig. 3.34. Therefore, altogether there should be 12 different carriers to implement the proposed CBPWM method. The need of four carriers in each PWM unit can be justified as follows.

A given line-to-ground reference voltage can be synthesized by switching between two voltage levels. In the proposed system this can be implemented in two alternative ways. The first method uses the three voltage levels of 0, V_{Ba} , and V_{dc} . Similarly, in the second method the voltage levels 0, $V_{dc} - V_{Ba}$ and V_{dc} are used. Since there are three voltage levels in each method two carriers are required in each case. As a result each leg of the converter requires four different carrier waveforms. Furthermore, amplitudes of these carriers should be varied according to the changes in battery voltages. Relevant mathematical equations are given in Table 3.16.

Fig. 3.34. Block diagram of the proposed CBPWM method.

Table 3.16. Amplitudes of modified carriers

Carrier amplitudes for the leg 'a'		Carrier amplitudes for the leg 'b'		Carrier amplitudes for the leg 'c'	
k_{pa1}	$2(1-V_{Ba}/V_{dc})$	k_{pb1}	$2(1-V_{Bb}/V_{dc})$	k_{pc1}	$2(1-V_{Bc}/V_{dc})$
k_{na1}	$2V_{Ba}/V_{dc}$	k_{nb1}	$2V_{Bb}/V_{dc}$	k_{nc1}	$2V_{Bc}/V_{dc}$
k_{pa2}	$2V_{Ba}/V_{dc}$	k_{pb2}	$2V_{Bb}/V_{dc}$	k_{pc2}	$2V_{Bc}/V_{dc}$
k_{na2}	$2(1-V_{Ba}/V_{dc})$	k_{nb2}	$2(1-V_{Bb}/V_{dc})$	k_{nc2}	$2(1-V_{Bc}/V_{dc})$

$$v_{as}^* = A_m \cos(\theta) \quad (3.34)$$

$$v_{bs}^* = A_m \cos(\theta - \frac{2\pi}{3}) \quad (3.35)$$

$$v_{cs}^* = A_m \cos(\theta + \frac{2\pi}{3}) \quad (3.36)$$

$$v_{ag}^* = \frac{1}{2} (1 + A_m \cos(\theta)) \quad (3.37)$$

$$v_{bg}^* = \frac{1}{2} \left(1 + A_m \cos(\theta - \frac{2\pi}{3}) \right) \quad (3.38)$$

$$v_{cg}^* = \frac{1}{2} \left(1 + A_m \cos(\theta + \frac{2\pi}{3}) \right) \quad (3.39)$$

In order to test the performance of the proposed CBPWM method under unbalanced situation same voltage conditions shown in Fig. 3.33(a) were applied for this simulation as well. Since the voltage of the battery B_a is changing, amplitudes of the carriers attached to the leg a are varied accordingly as shown in Fig. 3.35(b). The first line-to-ground voltage synthesizing method is used in this simulation. Therefore, the other two carriers of the leg a are not shown here. Amplitudes of the carriers attached to the legs b and c are equal and hence they have the same shape as shown in Fig. 3.33(b). Inverter output voltage of the a -phase is shown in Fig. 3.35(c). Compared to the inverter output voltage waveform in the previous case, shape of this waveform seems to be undistorted even at the ends where the imbalance is significant. It can be verified by observing undistorted inverter current waveforms which are shown in Fig. 3.35 (d). This confirms the ability of the proposed CMPWM method to produce undistorted currents even under unbalanced conditions.

(a)

(b)

Fig. 3.35. (a) Battery voltages and the dc-link voltage, (b) modified carriers used in the proposed CBPWM method for leg a , (c) inverter output voltage of the a -phase, (d) output currents of the inverter.

3.4.3 Charge/discharge control of battery banks

Charge/discharge controller for the battery bank B_a , attached to the leg ‘ a ’ of the inverter, is shown in Fig. 3.36(a). The same controller and the following analysis can equally be used for the other two phases as well. The controller output SS_a selects the suitable line-to-ground voltage synthesizing method out of the two methods shown in Fig. 3.34. If SS_a is permanently held at ‘0’ the battery B_a gets discharged during the first half cycle and gets charged in the second half cycle as shown in Fig. 3.36(b). Similarly, as shown in Fig. 3.36(c), the opposite happens when SS_a is held permanently at ‘1’. Therefore, if SS_a is fixed average current flow through the battery is zero and hence state of charge of the battery will not get affected. This indicates that the controller output SS_a should be changed at each and every half cycle to obtain an average charging or discharging current.

(a)

Fig. 3.36. (a) Charge/discharge controller block diagram, (b) battery current waveform IB_a , when SS_a is permanently tied to '0', (c) variation of IB_a , when SS_a is permanently tied to '1', (d), variation of IB_a , when SS_a is '0' at the first half cycle and '1' in the next, (e) variation of IB_a , when SS_a is '1' at the first half cycle and '0' in the next, (f) alternative use of the patterns in (d) and (e) to obtain the desired charging or discharging battery current.

In order to obtain an average discharging current, SS_a should be held at '0' during the first half cycle and '1' at the second half cycle. The resultant discharging current is shown in

Fig. 3.36(d). Similarly, if SS_a is held at '1' during the first half cycle and '0' at the second half cycle a net charging current can be obtained as shown in Fig. 3.36(e). These two settings would produce maximum rates of discharging and charging for the battery B_a respectively. An intermediate rate can be obtained by switching between the above two settings and the resultant battery current waveform is shown in Fig. 3.36(f). This switching is achieved through PWM as shown in Fig. 3.36(a). The reference for the PWM is generated by the battery management system. However, in practice, high frequency current pulses shown in Fig. 3.36(f) should not reach the battery and thus intermediate low pass filters must be used.

3.4.4 Simulation results

The proposed direct integration scheme has been verified using computer simulations on MATLAB/SIMULINK platform. System parameters of the simulation setup are given in Table 3.17. Three step changes were applied for the input power as shown in Fig. 3.37(a), by the trace P_{in} , to test dynamic response of the system. Battery banks are supposed to absorb fluctuations present in the input power and maintain constant power output as shown in Fig. 3.37(a) by traces $P_{battery}$ and P_{out} respectively. According to terminal voltages shown in Fig. 3.37(b) battery B_a has the high state of charge and the battery B_c has the lowest state of charge. Therefore, when there is a surplus of input power battery B_c should be given the priority. Similarly, when there is a deficit of power, the battery B_a should discharge first. This objective is achieved by the proposed controller as evident from the current and power graphs shown in Fig. 3.37(c) and Fig. 3.37(d) respectively.

According to the input power variation, shown in Fig. 3.37(a), initially there is a surplus of power and hence it is absorbed by the battery B_c with a charging current shown in Fig. 3.37(c). Since the battery B_c is capable of absorbing the total amount of surplus power the other two batteries are kept in the neutral mode. Then there is a deficit of power which is supplied by the battery B_a as shown in Fig. 3.37(c) by the discharging current. Here also the battery B_a is capable of supplying the total deficit and hence the other two batteries are kept in the neutral mode. If the deficit is too large and the battery B_a is unable to handle itself the battery B_b is called for support. The battery B_c is the last one to call for support under a deficit since it has the lowest state of charge. Inverter output current of

the a -phase is presented in Fig. 3.37(e) to show the ability of the proposed CBPWM method to produce desired outputs even under unbalanced conditions.

Fig. 3.37. Simulation results (a) input power, output power and battery power, (b) battery voltages and the dc-link voltage, (c) battery currents, (d) battery power, (e) inverter output current of the a -phase.

Table 3.17. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Inverter switching frequency	$f_s = 5\text{kHz}$
Nominal battery voltage	$V_{Bx} = 300\text{V}$
DC-Link voltage	$V_{dc} = 600\text{V}$

3.5 Summary

Traditional two-level converters are not suitable for modern multi MW wind turbine generators. As a result, three-level converters are gradually making their way into the wind energy industry. Diode-clamped topology is becoming the popular choice for implementing three-level converter systems. Energy storage interfacing capability of this topology has been investigated in section 3.2. Major problems of this approach have also been discussed with suitable modulation and control solutions. Simulation and experimental results are presented to prove the ability of the diode-clamped three-level inverter to interface battery/supercapacitor energy storage system directly without additional dc-dc converters.

The other alternative way of implementing three-level converters is the use of capacitor-clamped topology which is believed to be less reliable and bulky. These disadvantages are turned into gains in sections 3.3 and 3.4 by making the inverter to absorb short term and long term power fluctuations. This is achieved by replacing conventional capacitors of the capacitor-clamped three-level inverter with supercapacitors or batteries. Problems associated with these approaches are analyzed in detail and suitable modulation techniques are proposed with computer verifications. A comparison between the aforementioned three-level grid-side inverter based direct integration schemes and the conventional dc-dc converter based approach is given in Tables 3.18 and 3.19.

In summary, it can be concluded that proposed direct integrations schemes help to improve the system efficiency and reliability by eliminating the need for interfacing dc-dc converters. Furthermore, they reduce the cost and complexity of the system. Therefore, proposed schemes have high potential of being implemented in future wind energy conversion systems.

Table 3.18. Comparison between the dc-dc converter based approach and the proposed direct integration scheme for the diode-clamped three-level inverter topology

Topology	Diode-clamped three-level inverter with a dc-dc converter	Diode-clamped three-level inverter with supercapacitors	Diode-clamped three-level inverter with batteries	Diode-clamped three-level inverter with battery and supercapacitor
Components	1-inductor 1-dc-link capacitor rated for V_{dc} 2-dc-link capacitors rated for $0.5V_{dc}$ 12-switches rated for $0.5V_{dc}$ 2-fast switches rated for V_{dc}	1-dclink capacitor rated for V_{dc} 12-switches rated for V_{dc}	1-dclink capacitor rated for V_{dc} 12-switches rated for $0.6V_{dc}$	1-dclink capacitor rated for V_{dc} 12-switches rated for $0.8V_{dc}$
Change in dc-link voltage	Regulated	Large	Slight	Moderate
Transient response	Fast, but includes converter delay	Fast	Slightly low	Fast
Protection against switch faults	Possible to protect the ESS from inverter switch faults	No protection against short switch faults unless fuses are in series with clamping diodes	No protection against short switch faults unless fuses are in series with clamping diodes	No protection against short switch faults unless fuses are in series with clamping diodes
Pros	Modulation is not complicated Well matured technology	Reduce power losses Eliminate bulky inductor Fast response for short term power fluctuations	Reduce power losses Eliminate bulky inductor Able to absorb long term power fluctuations	Reduce power losses Eliminate bulky inductor Fast response for short term power fluctuations
Cons	Introduce additional costs and power losses Inductor is bulky	Require complex modulation and control strategies	Require complex modulation and control strategies	Require complex modulation and control strategies
Applications	Suitable for interfacing both battery and supercapacitor energy systems to the dc-link. Mitigate either short term or long term power fluctuations	Suitable for interfacing supercapacitor energy systems. Mitigate short term power fluctuations	Suitable for interfacing battery energy systems. Mitigate long term power fluctuations	Suitable for interfacing both battery and supercapacitor energy storage systems to the dc-link. Mitigate both short term and long term power fluctuations

Table 3.19. Comparison between the dc-dc converter based approach and the proposed direct integration scheme for the capacitor-clamped three-level inverter topology

Topology	Capacitor-clamped three-level inverter with a dc-dc converter	Capacitor-clamped three-level inverter with supercapacitors	Capacitor-clamped three-level inverter with batteries
Components	1-inductor 1-dc-link capacitor rated for V_{dc} 3-dc-link capacitors rated for $0.5V_{dc}$ 12-switches rated for $0.5V_{dc}$ 2-fast switches rated for V_{dc}	1-dclink capacitor rated for V_{dc} 12-switches rated for V_{dc}	1-dclink capacitor rated for V_{dc} 12-switches rated for $0.6V_{dc}$

Change in dc-link voltage	Regulated	Large	Slight
Transient response	Fast, but includes converter delay	Fast	Slightly low
Protection against switch faults	Possible to protect the ESS from inverter switch faults	No protection against short switch faults unless fuses are in series with supercapacitors	No protection against short switch faults unless fuses are in series with batteries
Pros	Modulation is not complicated Well matured technology	Reduce power losses Eliminate bulky inductor Fast response for short term power fluctuation	Reduce power losses Eliminate bulky inductor Able to absorb long term power fluctuations
Cons	Introduce additional costs and power losses Inductor is bulky	Require complex modulation and control strategies	Require complex modulation and control strategies
Applications	Suitable for interfacing both battery and supercapacitor energy systems to the dc-link. Mitigate either short term or long term power fluctuations	Suitable for interfacing supercapacitor energy systems. Mitigate short term power fluctuations	Suitable for interfacing battery energy systems. Mitigate long term power fluctuations

Chapter 4 Dual inverter topologies for wind generation

4.1 Introduction

Energy storage systems have begun to play an important role in wind energy conversion systems as they help to reduce power fluctuations caused by random wind changes [38]-[40]. From the system integration point of view the most straightforward way of integrating energy storage element is the connection to the intermediate dc-link of the back-to-back converter [127]-[129]. This, however, requires additional dc-dc or ac-dc bidirectional converters which increase the system cost, power losses and response time. If the grid-side inverter itself can be used as the interface for ESSs additional converters and associated drawbacks can be eliminated. Therefore, this chapter explores energy storage interfacing capabilities of dual inverter based grid-side inverter systems.

Four different dual inverter topologies, namely: 2x2, 2x3, 3x2 and 3x3, are considered in this study. The 2x2 dual inverter system is formed by cascading two two-level inverters through open ends of the primary winding of the coupling transformer. One inverter is powered by the wind turbine generator while the other is directly connected to a battery or a supercapacitor bank. Fluctuations present in the captured wind power are absorbed by the energy storage element. Similarly, the 2x3 and 3x2 dual inverter systems are constructed with two-level and three-level inverters where the first number denotes the number of levels in the wind generator side inverter and the second number corresponds to the number of levels in the energy storage side inverter. Likewise, the 3x3 topology consists of two diode-clamped three-level inverters.

In addition to the direct integration of energy storage elements aforementioned dual inverter topologies help to reduce power losses and are capable of producing multilevel output voltage waveforms with less number of switching devices. A detailed analysis of the operation, modulation and control of the 2x2 topology are presented in section 4.2. Similarly, 2x3 and 3x2 topologies are discussed in sections 4.3 and 4.4. The 3x3 topology is presented in section 4.5 for direct integration of a battery/supercapacitor hybrid energy storage system (ESS).

4.2 The 2x2 dual inverter system

The 2x2 dual inverter topology is formed by cascading two two-level inverters through open ends of the primary winding of the coupling transformer as shown in Fig. 4.1. The two inverters are named as the main inverter and the auxiliary inverter owing to their modes of operation. An ESS, either a battery bank or a supercapacitor bank, can be directly connected to the dc-link of the auxiliary inverter without a dc-dc converter and thus drawbacks of interfacing converters can be eliminated.

Fig. 4.1. The 2x2 dual inverter system with ESS interface.

This inverter system has the ability to produce up to 13 voltage levels in the phase voltage waveform whereas the traditional 2-level inverter can only produce 5 voltage levels. Under the optimum dc-link voltage ratio this topology can synthesize a 4-level inverter. Therefore, in literature, this topology has been identified as an alternative approach to develop three-level and four-level inverters without clamping diodes or capacitors. A detailed analysis on the multilevel operation is given in section 4.2.1.

Redundancy and the fault tolerant operation can be seen as additional features of the proposed system where the faulty inverter can simply be disconnected by short circuiting corresponding terminals of the transformer. In such situations the healthy inverter continues to be operational, but with less voltage levels [130]. Furthermore, the 2-level inverter technology is well known and standard modules are readily available in the market. Therefore, the proposed system can easily be implemented using off-the-shelf components.

4.2.1 Effects of variable dc-link voltage ratio

In the proposed system, charging/discharging currents of the ESS are controlled through the main inverter dc-link voltage. And as such it varies with the available wind power. Furthermore, the auxiliary inverter dc-link voltage varies with the state of charge (SoC) of the ESS. If a battery bank is attached to the auxiliary inverter dc-link its voltage is nearly constant for a certain period of time. But if a supercapacitor bank is used as the ESS the auxiliary inverter dc-link would show large variations. However, in both cases, the end result is non-integer dynamic changes in the dc-link voltage ratio. As the voltage ratio varies, space vectors of the combined inverter get distributed unevenly. In order to provide a clear understanding on the space vector distribution under variable dc-link voltage ratios, aforementioned two cases, i.e. interfacing a battery and a supercapacitor bank, are considered separately.

4.2.1.1 Space vector distribution when a battery is used as the ESS

The corresponding space vector distributions at different dc-link voltage ratios are shown in Fig. 4.2. Each and every space vector diagram, shown in Fig. 4.2, contains seven main inverter vectors, called main vectors. They are marked with large dots. The hexagon formed by these main vectors is called the main hexagon. Auxiliary inverter vectors, named as auxiliary vectors, are denoted by attached sub hexagons at each and every main vector point. For Figs. 4.2(a) to 4.2(c) only one sub hexagon is marked to avoid the diagram being too complex. However, scattered dots in these diagrams correspond to the edges of missing sub hexagons. The size of sub hexagons depends on the auxiliary inverter dc-link voltage. As mentioned before, when a battery is used as the ESS, its voltage can be considered as nearly constant and therefore size of sub hexagons are fixed. The circle found in each space vector diagram represents the path of the reference voltage vector which remains unchanged for constant power dispatch into a strong grid.

Fig. 4.2(a) shows the space vector diagram for the dc-link voltage ratio of 0 ($V_{dc} = 0$). At this point, due to the absence of a power source in the main inverter, all the seven main vectors coincide at the origin turning the combined inverter system into a

conventional two level inverter. The corresponding inverter output voltage waveform is shown next to the space vector diagram.

Fig. 4.2. Space vector distributions and output voltage waveforms at different dc-link voltage ratios.

When the main inverter dc-link voltage starts to increase the corresponding main hexagon appears as shown in Figs. 4.2(b) to 4.2(f). At the ratio of 0.25, sub hexagons overlap with each other as shown in Fig. 4.2(b) producing four layers of hexagonal

rings. In other words, the resultant space vector diagram is equivalent to that of a 5-level inverter. But due to the uneven distribution of the sub hexagons and the low resolution between vector points only few voltage levels can be seen in the corresponding waveform. At the ratio of 0.5, vectors get distributed evenly and three layers of hexagonal rings are formed as shown in Fig. 4.2(c). Therefore, this particular state represents a 4-level inverter. The corresponding voltage levels can clearly be seen in the attached waveform in Fig. 4.2(c).

At the ratio of 1, the combined inverter resembles a 3-level inverter (two layers of hexagonal rings) with the space vector pattern shown in Fig. 4.2(d). Further increase of the main inverter voltage would expand the space vector diagram as shown in Figs. 4.2(e) and 4.2(f). At the ratio of 1.5, four layers of hexagons emerge again resulting in a 5-level inverter. But the outermost vectors show large gap compared to inner vectors. However, the resolution between voltage levels is high compared to that in Fig. 4.2(b). As evident from Fig. 4.2(f), the space vector diagram at the ratio of 2 is again equivalent to a 4-level inverter. The attached waveform shows only five levels due to the fact that the reference circle is inside the first layer of hexagon. If the reference circle is extended to the next layer more voltage levels would appear in the output voltage.

Output voltage waveforms shown in Fig. 4.2 are in fact snapshots taken at six discrete dc-link voltage ratios. But as mentioned before, the dc-link voltage ratio can take any value between 0 and 2. Therefore, it is important to see how the output voltage waveform looks like at intermediate values. Therefore, a simulation was carried using the voltage ratio as the independent variable and the result is shown in Fig. 4.3(a).

At the ratio of 0, the output voltage waveform is similar to that in Fig. 4.2(a). The same scenario can be seen at the ratio of 1.125 as well. In between these two points a varying waveform can be seen which gets optimized at the ratio of 0.5. Beyond this point the inverter output voltage waveform gets distorted gradually until the ratio reaches 1. This is due to the decrease of available voltage levels. However, beyond the ratio of 1, the waveform again starts to show continuous improvement as seen in the latter half of the waveform in Fig. 4.3(a). With this result it can be deduced that the

2x2 dual inverter is capable of producing voltage levels similar to that of 2, 3, 4 and 5 level inverters. The filtered output voltage waveform is shown in Fig. 4.3(b).

Fig. 4.3 (a) Inverter output voltage, v_{as} , at different dc-link voltage ratios, (b) fundamental component of v_{as} .

4.2.1.2 Space vector distribution when a supercapacitor bank is used as the ESS

If a supercapacitor bank is used as the ESS, its voltage should be allowed to vary within a certain range for better utilization of the available capacity. This results in variations in the sub hexagon as well which makes the space vector distribution even more complex [73]. Therefore, to obtain the space vector distribution for a given instance, one should consider instantaneous dc-link voltages of both inverters. In other words, two variables are involved in the analysis of the combined space vector diagram. In such situations the usual practice is to vary one variable at a time while keeping the other fixed. The same method is used here as well to simplify the analysis.

In the first step of the analysis auxiliary inverter dc-link voltage is fixed to a certain value and the main inverter dc-link voltage is varied. Therefore, size of the sub hexagon is fixed. The resultant space vector diagrams are shown in Figs. 4.4(a) to 4.4(e). When the main inverter dc-link voltage decreases the space vector diagram shrinks making more overlapping of sub hexagons as in Fig. 4.4(b). The opposite happens when it increases as in Fig. 4.4(e). The corresponding inverter output voltage

variation with varied V_{dc}/V_{dcx} are illustrated in Fig. 4.5(a). Circles marked in Fig. 4.4 indicate the path of the reference voltage vector.

Fig. 4.4. Space vector diagrams at different dc-link voltage ratios, (a)-(e) V_{dc} vary while V_{dcx} is constant, (f)-(i) V_{dcx} vary while V_{dc} is constant.

Fig. 4.5. Variation of the (a) inverter output voltage v_{as} , and (b) supercapacitor current I_{dcx} , for diagrams shown in Figs. 4.4(a) to 4.4(e).

In the second set of space vector diagrams, shown in Figs. 4.4(f) to 4.4(i), the main inverter dc-link voltage is set to a constant value while the auxiliary inverter dc-link voltage varies. Here the circle of the reference vector is inside the main hexagon resulting in a surplus of power. This additional amount of power is absorbed by the supercapacitor bank by charging it. When it does so, sub hexagons get expanded. This results in increased number of overlapping of sub hexagons, as in Fig. 4.4(f). If the charging is not controlled sub hexagons can even extend beyond the origin of the coordinate system. In such a case, the inverter output voltage waveforms get distorted as shown in the first half of the Fig. 4.6(a). But still the fundamental component is controllable as evident from Fig. 4.6(b). A comprehensive discussion on charge/discharge control of supercapacitors at such extremes, through power reference adjustment, can be found in [97].

Fig. 4.6. Variation of the (a) inverter output voltage v_{as} , (b) fundamental component of the inverter output voltage $v_{as,f}$, for diagrams shown in Figs. 4.4(f) to 4.4(i).

4.2.2 Power sharing and MPPT strategies

The per-phase equivalent circuit of the dual inverter system is shown in Fig. 4.7 where the output voltage vector ($\bar{v}_r$), main inverter voltage vector ($\bar{v}_M$), auxiliary inverter voltage vector ($\bar{v}_A$) and the current vector ($\bar{i}$) are also shown. The output voltage vector is equivalent to the addition of the main inverter voltage vector and the auxiliary inverter voltage vector as in (4.1). Real power delivered to the load can be expressed as the dot product in (4.2) [131]. Furthermore, the load power is equivalent to the sum of the main inverter power and the auxiliary inverter power as expressed in (4.3). Equations (4.4) and (4.5) show the relationships between voltage vectors and corresponding switching states. With the help of these five equations, an expression can be derived for the power of the auxiliary inverter, in other words ESS power, as in (4.6). According to (4.6), it can be deduced that the ESS power, P_A , has a linear relationship with the main inverter dc-link voltage, V_{dc} , if the output power is constant (i.e. $\bar{i}$ and $\bar{v}_r$ are constant).

Fig. 4.7. Per-phase equivalent circuit of the dual inverter.

$$\bar{v}_r = \bar{v}_M + \bar{v}_A \quad (4.1)$$

$$P_L = \frac{3}{2} \bar{v}_r \cdot \bar{i} \quad (4.2)$$

$$P_L = \frac{3}{2} (\bar{v}_M + \bar{v}_A) \cdot \bar{i} = P_M + P_A \quad (4.3)$$

$$\bar{v}_M = \frac{2}{3} V_{dc} \left(S_{aM} + S_{bM} e^{j\frac{2\pi}{3}} + S_{cM} e^{-j\frac{2\pi}{3}} \right) \quad (4.4)$$

$$\bar{v}_A = \frac{2}{3} V_{dcx} \left(S_{aA} + S_{bA} e^{j\frac{2\pi}{3}} + S_{cA} e^{-j\frac{2\pi}{3}} \right) \quad (4.5)$$

$$P_A = \frac{3}{2} \left(\bar{v}_r - \frac{2}{3} V_{dc} \left(S_{aM} + S_{bM} e^{j\frac{2\pi}{3}} + S_{cM} e^{-j\frac{2\pi}{3}} \right) \right) \cdot \bar{i} \quad (4.6)$$

where $\bar{v}_M$, P_M and S_{iM} ($i=a, b, c$) represent the main inverter voltage vector, power and switching function while those of the auxiliary inverter are given by $\bar{v}_A$, P_A and S_{iA} ($i=a, b, c$) respectively. $\bar{v}_r$ represents the output voltage vector and P_L represents the real power flow to the grid.

In order to verify this relationship an experiment was carried out using the setup shown in Fig. 4.8(a). A gradually increasing dc voltage was applied to the main inverter while the battery voltage was constant at 25V. These input voltages are plotted in Fig. 4.8(b). The controller was set to maintain constant power dissipation through the load and thus the load current was constant as shown in Fig. 4.8(d). Under this constant power condition, battery current showed a linear relationship to the main inverter voltage with a negative slope as in Fig. 4.8(c). Since the battery voltage is constant, battery current is proportional to the battery power. Therefore, these results confirm that the battery power can be controlled by controlling the main inverter dc-link voltage. The same argument can be extended to develop a MPPT method for the WTG as follows.

According to (4.3), for a given output power, the main inverter power solely depends on the battery power. Therefore, maximum power point of the wind turbine can easily be tracked by changing the battery power. Furthermore, the above analysis reveals that the instantaneous power of the auxiliary inverter can be controlled by controlling the main inverter dc-link voltage. The usual practice is to maintain the main inverter dc-link voltage at a constant level, with the help of a controlled rectifier or a boost rectifier placed between the main inverter and the WTG. The same controlled rectifier or the boost rectifier can be used here to vary the main inverter dc-link voltage and thus indirectly track the maximum power point of the WTG. The controller block

diagram for this indirect MPPT is shown in Fig 4.9. In this controller the WTG model generates a power reference based on the measured wind speed. Then it is compared with the instantaneous power of the main inverter. The error is fed into a PI controller which generates a reference for the main inverter dc-link voltage.

Fig. 4.8. (a) Experimental setup used to verify the linear relationship between main inverter voltage and battery power, (b) dc-link voltage variations, (c) battery current, (d) load current of the 'a' phase.

Fig. 4.9. MPPT controller block diagram.

4.2.3 Modulation strategy

Extensive research has been carried out on modulation of the 2x2 dual inverter system, especially for motor drive applications [130]-[141]. Generally, all the proposed modulation methods can be divided into two groups. The first group employs two independent modulators [140] [141] while the second group consists of composite modulators [130]-[139]. They all consider cases with fixed-integer dc-link voltage ratios. For example, in [135] a SVM method with common mode rejection is presented for the dc-link voltage ratio of 1:1. A PWM scheme is proposed in [136] for both 1:1 and 2:1 voltage ratios. Although a power sharing controller is proposed in [131] for dynamically varying dc-link voltages, it also assumes identical variations thus making the ratio to be 1:1. But, as mentioned in section 4.2.1, this assumption is not valid for the proposed system. Furthermore, existing modulation methods are proposed for systems where both inverters supply power to the load. Therefore, to deal with variable dc-link voltage ratios and bi-directional power flow, a composite modulation method, built upon the six step and space vector modulation methods, is presented in this section.

In the proposed modulation method the main inverter operates in the six step mode producing square wave outputs as shown in the first half of the waveform in Fig. 4.10. The auxiliary inverter operates in the PWM mode and compensates harmonics presents in the square wave output of the main inverter as shown in the second half of the waveform in Fig. 4.10. The six step operation of the main inverter helps to reduce switching losses and thus improves the conversion efficiency.

Fig. 4.10. Square wave output of the main inverter and smoothing effect of the auxiliary inverter.

The modulation method used in the auxiliary inverter is a modified SVM technique and thus the overall modulation can be considered as a combination of the six step mode and SVM. The complexity of this combined modulation process gets further amplified by the dynamic variations present in dc-link voltages. To reduce most of the computational complexities, the three axis coordinate system shown in Fig. 4.11(a) is used [112]. In this coordinate system, each and every vector point is represented by three coordinates which are projections on V_{ab} , V_{bc} , V_{ca} axes. In fact, these three axes represent line to line voltages of a three phase system. If the dc-link voltages of the inverter are fixed, these projections can be normalized to get discrete values such as -1, 0 and 1. But in this particular case they are not fixed and hence the projections can take any value within the operating range. Therefore, instead of normalized values all the calculations are carried out using actual voltages which should be updated at every switching cycle. Hence, apart from the magnitude and the angle of the reference vector, dc-link voltages are used in the proposed modulator as shown in Fig. 4.12.

Fig. 4.11. (a) Space vector diagram with the three axis coordinate system, (b) shaded triangle with dwell times.

Fig. 4.12. Block diagram of the proposed modulation method.

Since the main inverter operates in the six step mode, the main vector selection and gate signal generation units in the modulator would require only the angle information of the reference vector, i.e. α_r . Based on this angle, three normalized coordinates of the current main vector, S_{ab} , S_{bc} , S_{ca} , are defined as temporary variables which are then used to calculate actual projections as expressed in (4.7). At the same time, three axis coordinates of the reference voltage vector v_r are calculated as corresponding line to line voltages v_{ab} , v_{bc} , v_{ca} . According to (4.1), the difference between the reference vector and the main vector is the compensation vector that should be supplied by the auxiliary inverter and thus it becomes the reference for the auxiliary inverter. Projections of this new reference are calculated using (4.8) and subsequently normalized using (4.9) to obtain floor and ceiling values as $\text{floor}(x)$ is the greatest integer $\leq x$ and $\text{ceiling}(x)$ is the smallest integer $\geq x$. Those floor and ceiling values of the normalized reference are then used to locate the triangle in the sub hexagon, for example the shaded triangle in Fig. 4.11(a), where the reference vector falls [93], [112]. The ends of this triangle contain required auxiliary vectors V_1 , V_2 and V_3 . But still they come with three axis coordinates. In order to map three axis coordinates into gate signals the transformation in (4.10) and the lookup table in Table 4.1 are used.

$$\begin{bmatrix} V_{ab} & V_{bc} & V_{ca} \end{bmatrix}^T = V_{dc} \begin{bmatrix} S_{ab} & S_{bc} & S_{ca} \end{bmatrix}^T \quad (4.7)$$

$$S_{ab}, S_{bc}, S_{ca} = \{-1, 0, 1\}$$

$$\begin{bmatrix} v_{abx} & v_{bcx} & v_{cax} \end{bmatrix}^T = \begin{bmatrix} (V_{ab} - v_{ab}) & (V_{bc} - v_{bc}) & (V_{ca} - v_{ca}) \end{bmatrix}^T \quad (4.8)$$

$$\begin{bmatrix} \hat{v}_{abx} & \hat{v}_{bcx} & \hat{v}_{cax} \end{bmatrix}^T = \frac{\sqrt{3}}{V_{dcx}} \begin{bmatrix} v_{abx} & v_{bcx} & v_{cax} \end{bmatrix}^T \quad (4.9)$$

$$S_{sp} = 4x + 2y + z + 3 \quad (4.10)$$

Where the three axis coordinates are assumed to be in the form of $V_n(x,y,z)$, $n=1,2,3$ and the resulting switching state number is denoted by S_{sp} , $p = \{a, b, c\}$.

Table 4.1. Switching signal lookup table

S_{sp}	0	1	2	3	4	5	6
Auxiliary vector	100	101	110	000	001	010	011

Once the three nearest vectors are identified, next step is to find corresponding dwell times (switching times). Usually this part involves multiplications, divisions and trigonometric operations which consume significant amount of processing time. But in the SVM technique adopted in this study dwell time calculations are very simple and straightforward. It is proven in [112] that dwell times are proportional to the distance from the reference vector point to the opposite leg of the triangle. For example, for the vector V_1 in Fig. 4.11(b), dwell time is proportional to the distance d_1 from the reference vector to the V_2 - V_3 leg of the triangle. In other words, it is proportional to the difference between v_{ab} component (projection on V_{ab} axis) of the reference and the corresponding floor value. The other two dwell times, d_2 and d_3 , also can be calculated in the same way. Therefore, to calculate dwell times only subtractions are needed. This yields fast operation and simple implementation in the hardware level. After finding auxiliary vectors and dwell times, five segment switching is used in the auxiliary inverters as described in [139].

4.2.4 ESS interfacing - a battery is used as the ESS

The possibility of direct connection of a battery to the auxiliary inverter is discussed in this section. The corresponding battery charging and discharging process, simulation results and experimental results are presented below.

4.2.4.1 Analysis of battery charging and discharging

Charging and discharging process of the battery can be explained under three different scenarios where the available wind power is less than the demand, equals to the demand, and higher than the demand. In the first case, the battery bank should

discharge to supply the deficit and in the third case it should absorb the surplus of power. However, in the second case, SoC of the battery bank will not get affected. With the help of Fig. 4.2 and Fig. 4.13, an approximate relationship between these three cases and the dc-link voltage ratio can be identified as follows:

Case 1 corresponds to $0 < \text{dc-link voltage ratio} < 1$,

Case 2 corresponds to $\text{dc-link voltage ratio} \approx 1$,

Case 3 corresponds to $1 < \text{dc-link voltage ratio} < 2$.

To understand further, voltage vector additions shown in Fig. 4.13 can be used. The vector additions shown in Fig. 4.13 correspond to $\alpha_r = 60^\circ$. At this angle, and its multiples, both main vector and the auxiliary vector get aligned making the analysis easier. When the dc-link voltage ratio is less than 1, the circular path of the reference voltage vector lies outside the main hexagon as shown in Figs. 4.2(b) and 4.2(c). Hence, the magnitude of the main inverter vector v_M is obviously less than that of the reference vector v_r , as in Fig. 4.13(a). As a result, the auxiliary inverter voltage vector v_A has to be used to fill the gap. Since the same current flows through both inverters, the corresponding share of power depends on the magnitude of the voltage vector. In certain cases, where both inverters should equally share the output power, both main and auxiliary inverter vectors are set to be equal [130]. But in the proposed system, the maximum possible power should be extracted from the main inverter and thus only the balance should be handled by the auxiliary inverter. This automatically happens when the main inverter is operating in the six step mode and hence no special attention is required.

Fig. 4.13. Voltage vector addition for (a) case 1, (b) case 2, (c) case 3.

When both the circle and main hexagon are at the same magnitude, the main inverter vector itself is enough to synthesize the reference vector as in Fig. 4.13(b). This roughly corresponds to the dc-link voltage ratio of 1, as in Fig. 4.2(d). However, it is

noteworthy to mention that the size of the reference circle, and hence the dc-link voltage ratio, where the main hexagon meets the circle, is changed with the power demand. When the dc-link voltage ratio is greater than 1, main hexagon exceeds the reference circle as in Figs. 4.2(e) and 4.2(f). In this case, the direction of the auxiliary inverter vector becomes negative as shown in Fig. 4.13(c). This indicates that part of the available wind power flows into the battery bank.

According to the above analysis it can be deduced that as long as the circle lies outside the main hexagon the battery current is positive (discharge). When the reference circle and the main hexagon are equal in size battery current tends to be zero, which indicates that available wind power is barely sufficient to supply the demand. Further increase of the main inverter dc-link voltage makes the main hexagon to exceed the voltage reference circle and change the direction of the battery current. In other words the battery bank is charged storing the surplus of power.

4.2.4.2 Simulation results

The proposed concept of ESS interfacing with the grid-side inverter has been tested in the MATLAB/Simulink/PLECS digital simulation platform. The wind speed profile shown in Fig. 4.14(a) is used in the simulation, which in turn produce a dc-link voltage variation at the main inverter as shown in Fig. 4.14(b). The corresponding wind power variation, P_w , and dispatch power, P_d , are shown in Fig. 4.14(c). From this graph it can be concluded that the proposed system has the ability to supply the demand amidst fluctuations present in the input power. The surplus or the deficit of power is supplied or absorbed by the battery with the current profile shown in Fig. 4.14(d). Current injected into the grid and the inverter output voltage are shown in Figs. 4.14(e) and 4.14(f) respectively. Although the inverter output voltage shows some fluctuations, once it passes through the LC filter, a smooth waveform can be observed as shown in Fig. 4.14(g). System parameters of the simulation setup are given in the Table 4.2.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Fig. 4. 14. (a) Wind speed, (b) dc-link voltages V_{dc} and V_{dcx} , (c) wind power, P_w , and dispatch power, P_d , (d) battery current, I_b , (e) current injected into the grid, i_a , (f) inverter output voltage before filtering, v_{as} , (g) inverter output voltage after filtering, v_{an} .

Table 4.2. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Filter resistance	$R_f = 0.2\Omega$
Filter inductance	$L_f = 3\text{mH}$
Nominal battery voltage	$V_{dcx} = 600\text{V}$
Range of the main inverter dc-link voltage	0 – 1000V
DC-Link capacitors C_1, C_2	$C = 2200\mu\text{F}$
Peak value of the grid voltage	$V_{pk} = 330\text{V}$
Rated power of the PMSG	$P_{r, PMSG} = 100\text{kW}$
Rated wind speed	$V_{w,co} = 10\text{m/s}$

4.2.4.3 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 4.15(a) and 4.15(b) respectively. System parameters of the experimental setup are given in the Table 4.3. A variable ac source (California Instruments 4500Ls, 4.5kW) is used to power the main inverter and its output was rectified using a diode bridge rectifier. The ac source was programmed in a way that the rectifier output, in other words the main inverter dc-link voltage, varies as shown by the graph marked with V_{dc} in Fig. 4.15(c). During the experiment, the battery voltage remained at 25V as shown by the line V_{dcx} in Fig. 4.15(c). The two inverters were coupled through an RL load and their parameters are given in Table 4.3. The controller was set to maintain constant power dissipation through the load as shown in Fig. 4.15(d) by the graph marked with P_L . The input power and battery power variations are plotted in the same figure and are marked as P_M and P_A respectively. The corresponding battery current variation is shown in Fig. 4.15(e). Shape of this graph is similar to that of the battery power diagram since the battery voltage remained constant. Furthermore, when the main inverter voltage is lower than the battery voltage, the battery current is positive and it is negative when the main inverter voltage exceeds the battery voltage. An

enlarged view of the inverter output current is shown in Fig. 15(f). An enlarged view of the inverter output voltage is given in Fig. 4.15(g) to show the multilevel operation of the proposed dual inverter system.

(c)

(d)

(e)

(f)

Fig. 4.15. (a) Schematic of the experimental setup, (b) photographs of the experimental setup, (c) dc-link voltages V_{dc} and V_{dcx} , (d) main inverter power P_M , battery power P_A , and output power P_L , (e) battery current, I_{dcx} , (f) enlarged view of the output current, (g) enlarged view of the inverter output voltage.

Table 4.3. System parameters of the experimental setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Load resistance	$R = 10\Omega$
Load inductance	$L = 11\text{mH}$
Nominal battery voltage	$V_{dcx} = 25\text{V}$
DC-Link capacitors C_1, C_2	$C = 2200\mu\text{F}$

4.2.5 ESS interfacing - a supercapacitor bank is used as the ESS

The possibility of direct connection of a supercapacitor bank to the auxiliary inverter is discussed in this section. The corresponding supercapacitor charging/discharging process, simulation results and experimental results are presented below.

4.2.5.1 Analysis of supercapacitor charging and discharging

The basic principle of the supercapacitor charging/discharging process is very much similar to the aforementioned battery charging/discharging process. If the main hexagon is large enough to enclose the circle, i.e. the path of the reference voltage vector, supercapacitor bank gets charged. On the other hand, if the circle is larger than the main hexagon, as in Fig. 4.4(b), available wind power is not sufficient to meet the demand. Therefore, the deficit has to be supplied by the supercapacitor bank by

discharging its stored energy.

With the help of the above analysis, a simplified model can be developed for the supercapacitor charging/discharging process as follows. If the wind speed is high, the main inverter dc-link voltage goes up and the main hexagon exceeds the circle. Then the additional power is directed towards the supercapacitor bank resulting in an increase of its voltage. This yields an expansion of sub hexagons. On the other hand if the wind speed is low, the main inverter vector pattern shrinks making the main hexagon to be inside the circle. At this point supercapacitor bank discharges its stored energy to supply the deficit of power. This reduces the supercapacitor voltage and hence sub hexagons get shrunk.

4.2.5.2 Control strategy

As discussed in section 4.2.2, the auxiliary inverter power (in this case supercapacitor power) can be controlled by varying the main inverter dc-link voltage and thereby track the maximum power point of the wind turbine. The corresponding controller block diagram for the 2x2 dual inverter based supercapacitor direct integration scheme is shown in Fig. 4.16. In this controller, the measured wind speed and the parameters of the turbine model are used to derive a power reference for the generator-side converter. The actual generator power is compared with the reference and the error is fed into a PI controller which generates a voltage reference for the boost rectifier. This voltage reference is normalized to produce the modulation index for the boost rectifier.

The grid side inverter controller employs an inner current controller and outer power controller as shown in Fig. 4.16. In this controller the reference for the d -axis current component is obtained by passing the instantaneous active power of the generator-side converter through a low pass filter (LPF) [97]. The q -axis current reference is set to zero to keep the power factor at the grid connection point at unity. These d - q axis current references are then compared with actual currents and the errors are passed through PI controllers to produce voltage references for the subsequent modulation unit.

Fig. 4.16. Controller block diagram for the 2x2 dual inverter based supercapacitor direct integration scheme.

4.2.5.3 Simulation results

The proposed 2x2 dual inverter based supercapacitor direct integration scheme has been tested using computer simulations on MATLAB/Simulink/PLECS digital simulation platform. Schematic diagram of the simulation setup is shown in Fig. 4.17(a) and the corresponding parameters of the setup are given in Table 4.4. The wind speed profile shown in Fig. 4.17(b) with an average speed of 10m/s, 20% harmonic amplitude and 1Hz harmonic frequency, is used to test the performance of the proposed system and control strategy. The corresponding variations of the input power, P_{in} , power injected into the grid, P_{grid} , and the supercapacitor power, P_{sc} , are shown in Fig. 4.17(c). The input power shows a large variation ranging from 30kW to 100kW. The average value of the output power is 60kW with a small variation of ± 5 kW. A simple calculation would reveal that the corresponding input power fluctuation is about 66% while the output power fluctuation is less than 8.4%. This proves the efficacy of the proposed system in mitigating power fluctuations caused by wind changes.

As mentioned in section 4.2.2 the main inverter dc-link voltage is changed to control the supercapacitor power and thus track the MPPT of the WTG. The corresponding

main inverter dc-link voltage and supercapacitor voltage variations are shown in Fig. 4.17(d). According to this diagram, the main inverter dc-link voltage shows a large variation ranging from 400V to 1200V which is far below the upper limit of modern IGCT devices and therefore the proposed system is feasible. Similarly, the supercapacitor voltage varies with a maximum of $V_{sc,H} = 800V$ and a minimum of $V_{sc,L} = 400V$. Therefore, according to (3.33) the required minimum capacitance of the supercapacitor bank found to be 43.75mF which is a realistic value.

The main inverter dc-link current and supercapacitor current variations are shown in Fig. 4.17(e). The main inverter dc-link current is nearly constant due to the six step operation of the main inverter. But the supercapacitor current varies with the main inverter dc-link voltage owing to the PWM operation of the auxiliary inverter.

Change in the modulation index of the generator-side converter (boost rectifier) for the aforementioned wind speed profile is shown in Fig. 4.17(f). The corresponding generator currents are shown in Fig. 4.17(g). Similarly, the variations of the amplitude and power angle of the grid-side inverter output voltage is shown in Figs. 4.17(h) and 4.17(i) respectively. These two values are nearly constant due to the smooth power delivery to the grid. Consequently, $d-q$ axis currents of the grid-side inverter are nearly constant as shown in Fig. 4.17(j). The corresponding three phase currents of the grid-side inverter and their zoomed in view are shown in Figs. 4.17(k) and 4.17(l) respectively to illustrate the low harmonic distortion of the dual inverter arrangement.

Inverter output voltage of the α -phase is shown in Fig. 4.17(m). An enlarged view of the inverter output voltage is given in Fig. 4.17(n) to show the multilevel operation of the dual inverter system. The two figures shown in Figs. 4.17(o) and 4.17(p) depict the six step operation of the main inverter and PWM operation of the auxiliary inverter respectively.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)

(j)

(k)

Fig. 4.17. Simulation results showing the performance of the 2x2 dual inverter based supercapacitor direct integration scheme (a) schematic of the simulation setup, (b) wind speed profile, (c) input power, P_{in} , output power, P_{grid} , and supercapacitor power, P_{sc} , (d) main inverter dc-link voltage V_{dc} , and auxiliary inverter dc-link voltage V_{dcx} , (e) main inverter dc-link current I_{dc} , and supercapacitor current, I_{dcx} (low pass filtered), (f) Modulation index of the generator-side converter, (g) generator current, (h) amplitude of the grid-side inverter output voltage, (i) power angle for the grid-side inverter output voltage, (j) d - q axis components of the grid-side inverter output current, (k) inverter output current, (l) enlarged view of the inverter output current, (m) inverter output voltage, v_{as} , (n) enlarged view of the inverter output voltage, (o) v_{amg} showing the six step operation of the main inverter, (p) v_{axgx} showing the PWM operation of the auxiliary inverter.

Table 4.4. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Boost rectifier switching frequency	$f_{sr} = 10\text{kHz}$
Phase resistance of the generator	$R_g = 0.2\Omega$
Phase inductance of the generator	$L_g = 1\text{mH}$
Capacitance of dc-link capacitors	$C_1, C_2 = 2.2\text{mF}$
Inductance of the boost rectifier	$L_I = 5\text{mH}$
Capacitance of the supercapacitor	$C_3 = 60\text{mF}$
Rated voltage of the supercapacitor bank	$V_{dcx,max} = 1000\text{V}$
Filter resistance of the grid-side inverter	$R_{abc} = 0.1\Omega$
Filter inductance of the grid-side inverter	$L_{abc} = 1\text{mH}$
Grid voltage	$v_{ll,rms} = 400\text{V}$
Rated power of the generator	$P_{r, PMSG} = 100\text{kW}$
Cut-in wind speed	$V_{w, cutin} = 4\text{m/s}$
Rated wind speed	$V_{w, rated} = 12\text{m/s}$
Turns ratio of the coupling transformer	1:1

4.2.5.4 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 4.18(a) and 4.18(b) respectively. The two inverters were coupled through an RL load and their parameters are given in Table 4.5. A large capacitor bank is used to emulate the high capacitance of the supercapacitor.

Fig. 4.18. (a) Schematic diagram of the experimental setup, (b) photographs of the experimental setup.

The controller was set to maintain constant power dissipation through the load as shown in Fig. 4.19(a) by the graph marked with P_{out} . The input power and supercapacitor power variations are also plotted in the same figure and are marked as P_{in} and P_{sc} respectively. In order to obtain the input power profile shown in Fig. 4.19(a), a variable ac source (California Instruments 4500Ls, 4.5kW) is used with a bridge rectifier. The ac source was programmed in a way that the rectifier output, in other words the main inverter dc-link voltage, varies as shown in Fig. 4.19(b) by the trace marked as V_{dc} . The corresponding supercapacitor voltage variation, V_{sc} , is also shown in Fig. 4.19(b). The resultant average supercapacitor current variation is shown in Fig. 4.19(c). An enlarged view of the inverter output voltage is given in Fig. 4.19(d) to show the multilevel operation of the dual inverter system. The inverter output current waveform, shown in Fig. 4.19(e), proves the efficacy of the proposed modulation method in generating outputs with very low distortion under variable dc-link voltage conditions.

(a)

(b)

(c)

Fig. 4.19. Experimental results showing the power smoothing capability (a) input power, output power and supercapacitor power, (b) dc-link voltage variations, (c) dc-link current variations, (d) inverter output voltage of the a -phase, (e) inverter output current of the a -phase.

Table 4.5. System parameters of the experimental setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 2.5\text{kHz}$
Load resistance	$R = 25\Omega$
Load inductance	$L = 6\text{mH}$
Capacitance of dc-link capacitors	$C_1, C_2 = 2200\mu\text{F}$
Capacitance of the capacitor bank	$C_3 = 20\text{mF}$

4.3 The 2x3 dual inverter system

The 2x3 dual inverter topology is formed by cascading a two-level inverter and a three-level inverter through open ends of the primary winding of the coupling transformer as shown in Fig. 4.20. Similar to the 2x2 dual inverter system, the two

inverters are named as the main inverter and the auxiliary inverter owing to their modes of operation. This topology found to be more suitable for interfacing two battery banks through the dc-link of the auxiliary inverter as shown in Fig. 4.20.

Fig. 4.20. The 2x3 dual inverter system with an ESS interface.

Compared to the 2x2 dual inverter, this topology reduces the terminal voltage of each battery bank to a half. As a result, the number of cells and the effective series resistance of each battery bank get reduced. Furthermore, if one battery fails the other can still continue operation at reduced capacity. Also, the auxiliary inverter is capable of accommodating a single switch open circuit fault or a short circuit fault.

The main inverter is a high power low speed inverter which operates at the fundamental frequency producing square wave outputs. Harmonics produced by the square wave output is compensated by the low power high speed auxiliary inverter. This particular power and frequency splitting arrangement reduces switching losses as well as device ratings of both inverters.

This topology is capable of supplying the demanded power even at zero wind speed. Furthermore, redundancy can be seen as an additional feature of this system where the faulty inverter can simply be disconnected by short circuiting corresponding terminals of the transformer. In such situations the healthy inverter continues to be operational,

but with less voltage levels. Furthermore, the 2-level and 3-level inverter technologies are well matured and standard modules are readily available in the market. Therefore, the proposed system can easily be implemented using off-the-shelf components.

In the proposed system, shown in Fig. 4.20, main inverter dc-link voltage varies with the available wind power. Moreover, the auxiliary inverter dc-link voltage varies with the state of charge (SoC) of its batteries. Therefore, as seen in the section 4.2.1, the end result is non-integer dynamic changes in the dc-link voltage ratio, which leads to uneven distribution of space vectors. A detailed analysis on this issue and a modified PWM strategy, which can produce undistorted currents even in the presence of unevenly distributed space vectors are presented in sections 4.3.1 and 4.3.2 respectively.

Another key issue with the proposed inverter system is the unavoidable imbalance of battery voltages due to non-identical batteries and differences in their states of charge. As a solution to this issue a carrier amplitude modification technique is proposed. Furthermore, charging or discharging rates of batteries should vary according to their state of charge. This is done by adding a dc offset to the reference signals of the auxiliary inverter which in turn changes the small vector selection pattern.

4.3.1 Effects of dc-link voltage variations

Space vector distribution of the dual 2x3 inverter system at different dc-link voltage ratios are shown in Fig. 4.21(a) where main vectors are marked with dark dots and auxiliary vectors are represented by attached sub hexagons. Inverter phase voltages take 3 to 8 levels depending on the dc-link voltage ratio as shown in Fig. 4.21(b). By observing the output voltage waveforms shown in Fig. 4.21(b) it can be concluded that the proposed modulation method can produce smooth and controllable output if the dc-link voltage ratio is maintained within the range of 0 to 1.75.

Fig. 4.21. (a) Space vector distribution at different dc-link voltage ratios, (b) phase voltage v_{as} and its fundamental component.

At the ratio of 0, or in other words when wind is absent, all the main vectors coincide at the origin making sub hexagons to overlap and produce a single sub hexagon. Therefore, the output voltage has only three levels. In this case, the battery bank itself supplies the total demand. But as soon as the ratio is increased by a small amount, six different voltage levels begin to appear which gets optimized at 0.25. Later it descends to four levels as the ratio approaches to 0.5. Further increase of the ratio yields a gradually improving 7 level phase voltage pattern with a climax at 0.75. However, it falls to 5 levels when the ratio reaches 1. In Fig. 4.21(a) inner sub hexagons are not shown for the ratios 0.5, 0.75 and 1 as the diagram will become too complex. At the ratio of 1.5 and 2 voltage waveforms can have 6 and 7 levels respectively.

The upper limit of this inverter topology is 8 levels which can be observed near the ratios of 1.25 and 1.75. Beyond 1.75 non overlapping areas emerge, which need fast switching between main vectors to produce undistorted outputs. Therefore, operation is limited to the range of 0 to 1.75.

4.3.2 Modulation strategy

As mentioned earlier, the main inverter operates in the six step mode producing square wave outputs. Fig. 4.22 illustrates this combined operation where the auxiliary inverter is purposely turned off until 30ms. During this period only the main inverter square wave output is available. Harmonic distortion of the output voltage is significant under this operation. After 30ms, auxiliary inverter is turned on and consequently the output voltage becomes smooth with a low harmonic distortion. Therefore, one can consider the auxiliary inverter as an active filter with real power exchange. Usually in harmonic filters, the given waveform is subtracted from the ideal waveform and then the difference is compensated. The same idea is used in the following modulation method.

Fig. 4.22. Square wave output of the main inverter and smoothing effect of the auxiliary inverter.

The relationship between line to ground voltages and switching states of the main inverter is given in (4.11) where S_a , S_b and S_c are the switching states of the main inverter. They can have either 0 or 1 as their values. Phase voltage levels of the main inverter can be obtained from the above line to ground voltages using (4.12). These phase voltage levels can take only four discrete values which are marked along the three axes v_a , v_b and v_c on the main inverter space vector diagram shown in Fig. 4. 23. These three axes correspond to the phase voltages v_{as} , v_{bs} and v_{cs} of the combined inverter.

$$\begin{bmatrix} V_{ag} & V_{bg} & V_{cg} \end{bmatrix}^T = \begin{bmatrix} s_a & s_b & s_c \end{bmatrix}^T \frac{V_{dc}}{2} \quad (4.11)$$

$$\begin{bmatrix} V_{a,\text{main}} \\ V_{b,\text{main}} \\ V_{c,\text{main}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (4.12)$$

Fig. 4.23. Space vector diagram showing vector addition and main inverter phase voltage levels (only one sub hexagon is included to maintain clarity).

A plot of the available phase voltage levels for the a -phase, $V_{a,\text{main}}$, and its reference $v_{a,\text{ref}}$, are shown in Fig. 4.24(a). The difference between the reference and the square wave output of the main inverter is shown in Fig. 4.24(b). Similar waveforms can be obtained for the other two phases using (4.13). These differences are to be compensated by the auxiliary inverter and thus they become references for the auxiliary inverter. Subsequently, these new references are normalized according to (4.14) and pulse width modulation is carried out using two carrier waveforms as shown in Fig. 4.24(c). A 500Hz carrier is used here for the illustration whereas the actual carrier frequency is ten times higher than that. The corresponding inverter controller block diagram is shown in Fig. 4.27. More details about the controller is given in section 4.3.3.

$$\begin{bmatrix} v_{ax} & v_{bx} & v_{cx} \end{bmatrix}^T = \begin{bmatrix} (V_{a,\text{main}} - v_{a,\text{ref}}) & (V_{b,\text{main}} - v_{b,\text{ref}}) & (V_{c,\text{main}} - v_{c,\text{ref}}) \end{bmatrix}^T \quad (4.13)$$

$$\begin{bmatrix} \hat{v}_{ax} & \hat{v}_{bx} & \hat{v}_{cx} \end{bmatrix}^T = \frac{3}{2V_{dc}} \begin{bmatrix} v_{ax} & v_{bx} & v_{cx} \end{bmatrix}^T \quad (4.14)$$

Fig. 4.24. Modulation technique (a) square wave output of the main inverter for the a -phase and the reference voltage waveform, (b) difference between the reference and the square wave output, (c) PWM with two carriers.

4.3.3 Modifications proposed to handle unbalanced battery voltages and SoC

Batteries attached to the dc-link of the auxiliary inverter can be at different states of charge and thus at different voltages. This leads to an inevitable imbalance in the neutral point potential of the auxiliary inverter. As a result of this imbalance, medium and small vectors get scattered unevenly as shown in Figs. 4.25(a) and 4.25(c). However, locations of large vectors depend only on the total dc-link voltage of the auxiliary inverter and would remain unchanged if it is constant. When upper and lower voltages are balanced, i.e. $V_L = V_U$, positive and negative small vectors coincide and only one inner hexagon is formed as shown in Fig. 4.25(b). Furthermore, medium vectors reach mid points of the outer hexagon at this particular state. If an imbalance is present, small vectors split and two separate inner hexagons appear as shown in Figs. 4.25(a) and 4.25(c). In addition to that, medium vectors move towards large vectors.

 Fig. 4.25. Space vector diagram for (a) $V_U > V_L$, (b) $V_U = V_L$, (c) $V_U < V_L$.

Conventional carrier based PWM does not produce desired outputs under such imbalanced conditions. As a solution to this problem carrier waveforms are modified according to (4.15) and (4.16). These modifications are graphically shown in Fig. 4.26(a). These modified carriers are obtained by applying the arbitrary imbalance shown in Fig. 4.26(b)

Fig. 4.26. (a) Modified carriers, (b) arbitrary voltages applied to create an imbalance in battery voltages.

$$A_U = \frac{2V_U}{V_U + V_L} \quad (4.15)$$

$$A_L = \frac{2V_L}{V_U + V_L} \quad (4.16)$$

When batteries are at different states of charge power sharing also should change accordingly. In other words, the battery at a high SoC should discharge more power when there is a deficit. Similarly, when there is a surplus of power the battery with the low SoC should be given a priority to absorb power. This can be achieved by the

proper selection of upper and lower small vectors. For an example, if battery 1 has to be given the priority, lower small vectors should be used at a higher rate than the upper small vectors. A negative dc offset on three reference signals would achieve this goal. Similarly, to give a priority to the battery 2, upper small vectors should be used at a higher rate and it can be done with a positive offset on the reference signals. Magnitude of this dc offset is obtained through a PI controller as shown in the controller block diagram in Fig. 4.27. Sign of the PI controller output is altered according to (4.17) to reflect the power difference in the dc offset. However, this offset should be limited to avoid reference signals being saturated. Corresponding upper and lower limits are given in (4.18).

Fig. 4.27. Controller block diagram.

$$Sgn_{power} = \begin{cases} +1 & P_{wind} > P_{demand} \\ 0 & P_{wind} = P_{demand} \\ -1 & P_{wind} < P_{demand} \end{cases} \quad (4.17)$$

$$\frac{V_{dc}}{2V_{dcx}} - 1 < \delta_{dc} < 1 - \frac{V_{dc}}{2V_{dcx}} \quad (4.18)$$

4.3.4 Simulation results

The proposed scheme including dual inverter and BESS has been simulated for one second on the MATLAB/Simulink/PLECS platform. System parameters of the simulation setup are given in Table 4.6. The wind speed profile used in this simulation is shown in Fig. 4.28(a). The main inverter dc-link voltage is shown in Fig. 4.28(b). The corresponding wind power variation, P_w , and dispatch power, P_d , are shown in Fig. 4.28(c). From this graph it can be concluded that the proposed system has the ability to deliver constant amount of power to the grid amidst random fluctuations of wind. The surplus or deficit of power is supplied or absorbed by the battery with

current profiles shown in Figs. 4.28(d) and 4.28(e). Both waveforms show equal currents proving the effectiveness of the proposed neutral point potential balancing technique. Current injected into the grid and the inverter output voltage are shown in Figs. 4.28(f) and 4.28(g) respectively. Although the inverter output voltage in Fig. 4.28(g) shows fluctuations, once it get passed through the low pass filter a smooth waveform could be observed as in Fig. 4.28(h).

(a)

(b)

(c)

(d)

(e)

Fig. 4.28. (a) Wind speed, (b) main inverter dc-link voltage V_{dc} , (c) wind power, P_w , and dispatch power, P_d , (d) (e) battery currents, I_{b1} , and I_{b2} , (f) current injected into the grid, i_a , (g) inverter output voltage before filtering, v_{as} , (h) inverter output voltage after filtering, v_{an} .

Table 4.6. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Filter resistance	$R_f = 0.2\Omega$
Filter inductance	$L_f = 3\text{mH}$
DC-Link capacitors	$C = 2200\mu\text{F}$
Peak value of the grid voltage	$V_{pk} = 330\text{V}$
Nominal battery voltage	$V_{\text{Battery}} = 300\text{V}$
Rated power of the PMSG	$P_{r, \text{PMSG}} = 75\text{kW}$

4.3.5 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 4.29(a) and 4.29(b) respectively. System parameters of the experimental setup are given in Table 4.7. A variable ac source (California Instruments 4500Ls, 4.5kW) is

used to power the main inverter and its output was rectified using a diode bridge rectifier. The ac source was programmed in a way that the rectifier output, in other words the main inverter dc-link voltage, varies as shown in Fig. 4.30(a). During the experiment, battery voltages remained at 20V. The two inverters were coupled through an RL load and their parameters are given in Table 4.7. The controller was set to maintain constant power dissipation through the load as shown in Fig. 4.30(b) by the graph marked as P_L . The input power and total battery power variations are plotted in the same figure and are marked as P_M and P_A respectively. The corresponding battery current variations are shown in Fig. 4.30(c). Shape of this graph is similar to that of the battery power diagram since the battery voltages remained constant. Furthermore, when the main inverter voltage is lower than the battery voltage, the battery currents are positive and they become negative when the main inverter voltage exceeds battery voltages. An enlarged view of the inverter output current is shown in Fig. 4.30(d). An enlarged view of the inverter output voltage is shown in Fig. 4.30(e) to show the multilevel operation of the proposed dual inverter system.

Fig. 4.29. (a) Schematic diagram of the experimental setup, (b) photographs of the experimental setup.

Fig. 4.30. (a) Main inverter dc-link voltage V_{dc} , (b) main inverter power P_M , battery power P_A , and output power P_L , (c) battery currents, (d) enlarged view of the output current, (e) enlarged view of the inverter output voltage.

Table 4.7. System parameters of the experimental setup

Fundamental frequency	$f = 10\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 500\text{Hz}$
Load resistance	$R = 10\Omega$
Load inductance	$L = 5\text{mH}$
Battery voltage	$V_{B1}, V_{B2} = 20\text{V}$
DC-Link capacitors C , $C1$ and $C2$	$C = 2200\mu\text{F}$

4.4 The 3x2 dual inverter system

Similar to the 2x3 dual inverter the 3x2 dual inverter is formed by cascading a three-level inverter and a two-level inverter through open ends of the primary winding of the coupling transformer as shown in Fig. 4.31. Moreover, the two inverters are named as the main inverter and the auxiliary inverter. This topology is more suitable for interfacing a supercapacitor bank through the dc-link of the auxiliary inverter as shown in Fig. 4.31. Dynamic behavior of the supercapacitor voltage is handled by the proposed controller eliminating the need for a boost converter. The usual frequency and power splitting is incorporated into this topology as well to reduce power losses. Compared to the aforementioned 2x2 and 2x3 dual inverter systems, this topology increases the voltage rating of the main inverter and thus increases the output power.

Fig. 4.31. The 2x3 dual inverter system with an ESS interface.

The issue with non-integer dynamically-changing dc-link voltage ratio is inherent for this topology as well. Therefore, the modulation strategy, proposed in section 4.2.3 is adopted here with minor modifications. The space vector distribution at different dc-link voltage conditions is also very much similar to that of the 2x2 dual inverter system, shown in Fig. 4.4, except the main inverter being three-level. The corresponding space vector distribution is shown in Fig. 4.32. Similar to the space vector diagram in Fig. 4.4, in Figs. 4.32(a) to 4.32(e) auxiliary inverter dc-link voltage is kept constant while the main inverter dc-link voltage changes. In Figs. 4.32(f) to 4.32(j) the main inverter dc-link is kept constant while the auxiliary inverter dc-link voltage changes.

The analysis on supercapacitor charging/discharging is more or less similar to that in section 4.2.5 and therefore will not be repeated here. However, only the outer hexagon of the main inverter space vector diagram is recommended for implementing the modulation process. If vectors of the inner hexagon are selected as main inverter vectors, they are not capable of delivering the required amount of power. As a result supercapacitor bank gets discharged. On the other hand if the inner hexagon is larger than the circle, there is a surplus of power which gets stored in the supercapacitor bank. Further analysis on small main vectors shows that only one capacitor of the main inverter dc-link participates at a time leaving the other capacitor unconnected to the output. That means only a fraction of available wind power is passed in to the grid and the supercapacitor bank. Therefore, the inner hexagon is not desirable for power processing. As a result the only available option is to use large and medium main vectors alternatively as shown in Fig. 4.33. However, small main vectors are occasionally used for voltage balancing of the main inverter dc-link capacitors.

4.4.1 Simulation results

The proposed system has been simulated for one second on the MATLAB/Simulink/PLECS digital simulation platform. System parameters of the simulation setup are given in Table 4.8. The wind speed profile shown in Fig. 4.34(a) is used in this simulation, which in turn produces a dc-link voltage variation of the main inverter as shown in Fig. 4.34(b). The proposed controller maintains the supercapacitor voltage

Fig. 4.32. Space vector diagram at different voltage ratios, (a)-(e) V_{dc} vary while V_{dcx} is constant, (f)-(j) V_{dcx} vary while V_{dc} is constant.

and the dc-link voltage ratio within safe limits as illustrated in Figs. 4.34(c) and 4.34(d) respectively. The corresponding wind power variation P_w , and dispatch power P_d , are shown in Fig. 4.34(e). From this graph it can be concluded that the proposed system has the ability to smoothen short term power fluctuations. The surplus or deficit of power is supplied or absorbed by the supercapacitor bank with the current profile shown in Fig. 4.34(f). The inverter output voltage is shown in Fig. 4.34(g). Although the inverter output voltage shows fluctuations, once it is passed through the low pass filter smooth waveforms could be observed as in Fig. 4.34(h). The current injected into the grid is shown in the Fig. 4.34(i).

Fig. 4.33. Main inverter vector transition pattern.

Fig. 4.34. Simulation results (a) wind speed, (b) main inverter dc-link voltage, V_{dc} , (c) auxiliary inverter dc-link voltage, V_{dcx} , (d) dc-link voltage ratio, V_{dc} / V_{dcx} , (e) wind power, P_w , and dispatch power, P_d , (f) supercapacitor current, I_s , (g) inverter output voltage before filtering, v_{as} , (h) inverter output voltage after filtering, v_{an} , (i) current injected into the grid, i_a .

Table 4.8. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Filter resistance	$R_f = 0.2\Omega$
Filter inductance	$L_f = 3\text{mH}$
Capacitance of the supercapacitor	$C = 0.1\text{F}$
DC-Link capacitors C_1, C_2	$C = 2200\mu\text{F}$
Peak value of the grid voltage	$V_{pk} = 330\text{V}$
Rated power of the PMSG	$P_{r, PMSG} = 40\text{kW}$

4.4.2 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 4.35(a) and 4.35(b) respectively. A variable ac source (California Instruments 4500Ls,

4.5kW) is used power the main inverter and its output was rectified using a bridge rectifier.

Fig. 4.35. (a) Schematic diagram of the experimental setup, (b) photographs of the experimental setup.

The ac source was programmed in a way that the rectifier output, in other words the main inverter dc-link voltage, varies as shown in Fig. 4.36(a) by the trace marked as

(V_{dc}). However, due to the large capacitance supercapacitor voltage remained nearly constant throughout the experiment as shown in Fig. 4.36(a) by the trace marked as (V_{dcx}). The two inverters were coupled through an RL load and their parameters are given in Table 4.9. The controller was set to maintain constant power dissipation through the load as shown in Fig. 4.36(b) by the graph marked with P_L . The input power and supercapacitor power variations are plotted in the same figure and are marked as P_M and P_{SC} respectively. The corresponding supercapacitor current variation is shown in Fig. 4.36(c). Neutral point potential balancing of the main inverter is shown in Fig. 4.36(d). Inverter output current is shown in Fig. 4.36(e).

Fig. 4.36. Experimental results (a) dc-link voltages V_{dc} , and V_{dcx} , (b) main inverter power P_M , supercapacitor power P_{SC} , and output power P_L , (c) supercapacitor current, I_s , (d) main inverter capacitor voltage balancing, (e) inverter output current of the a -phase.

Table 4.9. System parameters of the experimental setup

Fundamental frequency	$f = 10\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 500\text{Hz}$
Load resistance	$R = 3.5\ \Omega$
Load inductance	$L = 5\text{mH}$
Supercapacitor voltage (maximum)	$V_{dcx} = 25\text{V}$
DC-Link capacitors C_1 and C_2	$C = 2200\ \mu\text{F}$
Capacitance of the Supercapacitor bank	$C_s = 100\text{F}$
Number of supercapacitors	10

4.5 The 3x3 dual inverter system

Power handling capabilities of the 2x2 and 2x3 dual inverter systems are limited to several hundreds of kilowatts and hence not suitable for modern multi-mega-watt wind turbine generator systems. On the other hand, even if the 3x2 dual inverter system is suitable for high power systems it can only interface supercapacitors. Therefore, its power smoothing capability is limited to short-term fluctuation. But the mitigation of long-term power fluctuations is also equally important. The 3x3 dual inverter system, shown in Fig. 4.37, is proposed as a solution which can interface both supercapacitor and battery energy storage systems. This hybrid system can mitigate both short-term and long-term power fluctuation. Here also the two inverters are named as the main inverter and the auxiliary inverter. The main inverter is connected to the rectified output of the wind generator. A battery bank and a supercapacitor bank are directly connected across dc-link capacitors of the auxiliary inverter. The operation of the combined inverter is similar to the aforementioned topologies where the main inverter operates at the fundamental frequency to reduce switching losses and the auxiliary inverter is used for harmonic compensation and real power exchange [93], [142]-[144].

Fig. 4.37. Proposed grid-side inverter with battery/supercapacitor hybrid energy storage interface.

A similar direct connection scheme is proposed in [145] for motor drives in large vehicle propulsion with a dc supply attached to the main inverter and two

supercapacitor banks to the auxiliary inverter. In that configuration supercapacitor voltages are balanced using redundant state selection (RSS). But in the proposed system, voltage imbalance between the battery and the supercapacitor bank is inevitable. This imbalance splits small vectors and dislocates medium vector of the auxiliary inverter. Moreover, the main inverter dc-link voltage is purposely varied in order to track the MPP of the WTG. This further complicates the space vector pattern of the combined inverter with dynamically changing and unevenly distributed space vectors. Conventional modulation techniques fail to produce undistorted current under such conditions. Therefore, this section presents a novel SVM technique which can produce desired voltage and current waveforms even in the presence of unevenly distributed space vectors.

4.5.1 Effects of variable dc-link voltages

Generally, it is possible to balance dc-link voltages using RSS when it is connected with two capacitors, which is the case for the main inverter. But in the proposed system, the lower dc-link capacitor of the auxiliary inverter is replaced with a battery bank and hence its voltage is uncontrollable. Furthermore, for the optimum usage of the supercapacitor, its voltage should be allowed to vary within 50-100% of the rated voltage. This creates unavoidable imbalances in auxiliary inverter dc-link voltages.

The combined space vector diagram for an unbalanced condition is shown in Fig. 4.38. The larger dots in main hexagons represent main inverter vectors and small dots in the attached sub hexagons represent auxiliary inverter vectors. In Fig. 4.38, only one set of sub hexagons, with the two inner hexagons, are shown for clarity. In a complete space vector diagram the sub hexagonal pattern shown in Fig. 4.38 repeats at each and every main vector point. Size of the innermost sub hexagon shown in Fig. 4.38 depends on the battery voltage and hence it doesn't vary significantly. In contrast, the size of the other inner sub hexagon varies frequently as the supercapacitor as the supercapacitor gets charged and discharged. This affects the outermost sub hexagon as well since it is the sum of the two inner sub hexagons. The corresponding space vector distribution at different dc-link voltage ratios is very much similar to those presented in sections 4.2, 4.3 and 4.4 and thus won't be discussed in this section.

The operation of the proposed inverter system can be divided to three different modes depending on the way the ESS are used. In the first mode, only the battery is used for power smoothing. In the second mode only the supercapacitor bank is used as the power smoothing element. The third mode uses both ESSs simultaneously.

In the first mode of operation, only the inner sub hexagon 1 is used with the outer main hexagon. The other two sub hexagons are not used. This ensures that only the battery is used for power smoothing. Similarly, in the second mode only the inner sub hexagon 2 is used with the outer main hexagon and thus only the supercapacitor bank is used for power smoothing. In the third mode all three sub hexagons are used simultaneously.

Fig. 4.38. Space vector diagram of the dual 3x3 inverter system.

4.5.2 Modulation strategy

The main vector traversal pattern used in the proposed modulation method is shown in Fig. 4.39. The modulation methods proposed in literature for the 3x3 dual inverter system can be categorized into five groups. A carrier based PWM method is proposed in [143] while a PQ compensation based modulation technique is proposed in [144]. A duty cycle modulation based method is proposed in [146]. An improved SVM technique and a PWM method are proposed in [93] and [147] respectively. All these methods work only for balanced and constant dc-link voltage conditions with integer voltage ratios. The hierarchical modulation method proposed in [145] is capable of

producing undistorted current under non-integer voltage ratios. But even this method is not applicable for the proposed system due to unavoidable imbalance in auxiliary inverter dc-link voltages. Therefore, as a solution to this issue, authors have developed a novel SVM technique from the scratch which can produce desired outputs even under unbalanced and dynamically changing dc-link voltages. The proposed modulation method is three fold in conjunction with the aforementioned three modes of operation and can be described with the use of Fig. 4.38. In the first mode, only the inner sub hexagon 1 with lower small vectors is used in the modulation process. Therefore, the combined inverter becomes equivalent to a cascaded 3x2 inverter system. Similarly, in the second mode, the inner hexagon 2 with upper small vectors is used. But in the third case, all three sub hexagons are used and hence the combined system becomes a cascade 3x3 inverter. However, in all three modes the main inverter vector traversal pattern remains unchanged as shown in Fig. 4.39.

Fig. 4.39. Main inverter vector transition pattern.

4.5.2.1 Modulation process for the operating mode 1

In this mode of operation only the battery energy storage system is used and hence this can only mitigate long-term power fluctuations. A simplified block diagram of the modulation process is shown in Fig. 4.40. First, d - q components of the current main vector are obtained using (4.19). In (4.19), the actual dc-link capacitor voltages of the main inverter (V_u and V_L) are used and hence outputs will not get affected from unbalanced conditions in the main inverter. Difference between d - q components of the reference and main inverter voltage vectors are calculated using (4.20) and they become the compensation vectors which need to be synthesized by the auxiliary inverter. Instantaneous magnitude and angle of the auxiliary inverter voltage vector are

calculated using (4.21) and (4.22) respectively.

$$\begin{bmatrix} v_{ds,M} \\ v_{qs,M} \\ V_0 \end{bmatrix} = \frac{1}{2} [K] \begin{bmatrix} S_a(S_a-1) & S_a(S_a-3) \\ S_b(S_b-1) & S_b(S_b-3) \\ S_c(S_c-1) & S_c(S_c-3) \end{bmatrix} \begin{bmatrix} V_u \\ -V_L \end{bmatrix} \quad (4.19)$$

$$\begin{bmatrix} v_{ds,A}^* & v_{qs,A}^* \end{bmatrix}^T = \begin{bmatrix} (v_{ds}^* - v_{ds,M}) & (v_{qs}^* - v_{qs,M}) \end{bmatrix}^T \quad (4.20)$$

Fig. 4.40. Simplified block diagram showing the proposed SVM process.

$$v_{r,A}^* = \sqrt{v_{ds,A}^{*2} + v_{qs,A}^{*2}} \quad (4.21)$$

$$\alpha_A = \tan^{-1} \left(\frac{v_{qs,A}^*}{v_{ds,A}^*} \right) \quad (4.22)$$

$$T_a = \frac{T}{2V_b} (3v_{ds,A}^* - \sqrt{3}v_{qs,A}^*) \quad (4.23)$$

$$T_b = \frac{\sqrt{3}T}{2V_b} (v_{qs,A}^* + \sqrt{3}v_{ds,A}^*) \quad (4.24)$$

$$T_c = \frac{T}{2V_b} \sqrt{3}v_{qs,A}^* \quad (4.25)$$

$$T_d = \frac{\sqrt{3}T}{2V_b} (v_{qs,A}^* - \sqrt{3}v_{ds,A}^*) \quad (4.26)$$

$$T_0 = 1 - (T_1 + T_2) \quad (4.27)$$

where $[K]$ is the Park's transformation matrix.

Table 4.10. Auxiliary vector identification and dwell time calculation

α_A	Sector	V_1	T_1	V_2	T_2
$0 < \alpha_A \leq 60$	1	011	T_a	001	T_c
$60 < \alpha_A \leq 120$	2	001	T_b	101	T_d
$120 < \alpha_A \leq 180$	3	100	T_a	101	T_c
$180 < \alpha_A \leq 240$	4	100	T_a	110	T_c
$240 < \alpha_A \leq 300$	5	010	T_b	110	T_d
$300 < \alpha_A \leq 360$	6	011	T_a	110	T_c

(Zero vectors of the auxiliary inverter are not included in this table and it should be $V_0 = \{000, 111\}$ with dwell time T_0 .)

Based on the angle of the auxiliary inverter voltage vector and the sector number, three nearest vectors are identified using Table 4.10. The corresponding equations for switching time calculation are given in (4.23) to (4.27). After finding auxiliary vectors and corresponding dwell times, five segment switching is used as described in [139].

4.5.2.2 Modulation process for the operating mode 2

Operation of this mode is very much similar to mode 1. But this time instead of the battery the supercapacitor bank is selected. Therefore, this particular mode is suitable for leveling short term power fluctuations. Equations (4.19) to (4.27) and Table 4.10 can be used in this mode as well. But the battery voltage V_b has to be replaced with the supercapacitor voltage V_{sc} in equations (4.23) to (4.26). Furthermore, lower small vectors in Table 4.10 have to be replaced with corresponding upper small vectors.

4.5.2.3 Modulation process for the operating mode 3

This particular mode of operation is selected in two occasions. The first use occurs when there is a sudden drop of wind speed to the lower limit. Since the main inverter dc-link voltage is varied in proportion to the wind power, it gets lowered in such situations. At this particular situation, both inner sub hexagons would not touch the circle of the reference voltage vector individually. But the outer sub hexagon, i.e. the addition of two inner sub hexagons, can cover the reference circle. Therefore, at this point both energy storage systems are used simultaneously to supply the demand. The duration of discharge is determined by the capacity of the supercapacitor bank. The

second use of this mode happens when there is a need for LVRT. In this case the reference voltage drops down and the outer sub hexagon is used to fill the gap by extending the range of the auxiliary inverter voltage vector. A detailed analysis on LVRT capability of the proposed system is presented in section 4.5.4.

Since all three sub hexagons are used in this particular mode of operation, the modulation process becomes complex. This is mainly due to the uneven distribution of auxiliary inverter vectors as illustrated in Fig. 4.25 [103], [148] [149]. As a solution to this issue, a novel vector selection strategy and a dwell time calculation method are presented below which can produce undistorted current even in the presence of unevenly distributed space vectors. A simplified block diagram of the proposed technique is illustrated in Fig. 4.41. The amplitude $v_{r,A}$ and the phase angle α_A of the auxiliary inverter reference voltage vector are calculated using (4.21) and (4.22). Currently serving sector of the space vector diagram is derived from the phase angle and the sector selection criterion is similar to that in Table 4.10. After selecting the sector, the next step is to select the suitable triangle out of the two possible triangles. Selection of the proper triangle is a function of the EMS which is discussed in the next section.

Fig. 4.41. Simplified block diagram showing vector selection and dwell time calculation for mode 3.

However, due to the presence of two candidate triangles, four different limit angles, θ_1 , θ_2 , θ_3 , and θ_4 , need to be calculated for a given sector. First two limit angles, θ_1 and θ_2 , are related to the triangles formed with lower small vectors as shown in Fig. 4.42(a) whereas the other two limit angles, θ_3 and θ_4 , are associated with the triangles formed with upper small vectors as shown in Fig. 4.42(b). For the simplicity of subsequent calculations, dc-link voltages are transformed into two variables x and y using (4.28).

These two values are directly related to the lengths of triangles as marked in Fig. 4.42. Limit angles are calculated using (4.29)-(4.33) where α is an intermediate variable.

$$x = \frac{2}{3}V_{sc}, y = \frac{2}{3}V_b \quad (4.28)$$

$$\alpha = \sin^{-1} \left(\frac{\sqrt{3}y}{2\sqrt{(x+y)^2 - 3xy}} \right) \quad (4.29)$$

$$\theta_1 = \alpha - \sin^{-1} \left(\frac{\sqrt{3}y^2}{2r\sqrt{(x+y)^2 - 3xy}} \right) \quad (4.30)$$

$$\theta_2 = \sin^{-1} \left(\frac{\sqrt{3}y}{2r} \right) \quad (4.31)$$

$$\theta_3 = \frac{\pi}{3} - \sin^{-1} \left(\frac{\sqrt{3}x}{2r} \right) \quad (4.32)$$

$$\theta_4 = \alpha - \frac{\pi}{3} - \sin^{-1} \left(\frac{x}{r} \sin \left(\alpha - \frac{2\pi}{3} \right) \right) \quad (4.33)$$

$$\bar{V}_r = d_1\bar{V}_1 + d_2\bar{V}_2 + d_3\bar{V}_3 \quad (4.34)$$

$$d_1 + d_2 + d_3 = 1 \quad (4.35)$$

Where V_r is the reference vector and V_1 , V_2 , and V_3 are the three adjacent auxiliary vectors as shown in Fig. 4.38.

The limit angles given in (4.30)-(4.33) are valid only for the Sector 1. Limit angles for the other sectors can be derived from these values with the help of Table 4.11. Once the limit angles are calculated, the triangle and corresponding three vectors are derived from a look up table which is similar to Table 4.10.

After finding the three vectors, the next step is to determine switching times. According to the well known volt-second balancing principle, a given reference vector can be synthesized by three adjacent vectors. Equations (4.34) and (4.35) provide the mathematical description of this process. Equations (4.36)-(4.39) are used to calculate corresponding switching times d_1 - d_3 which are expressed as fractions of the sampling time [112].

Fig. 4.42. Limit angles for sector 1 (a) limit angles for triangles formed with lower small vectors, (b) limit angles for triangles formed with upper small vectors.

Table 4.11. Limit angles for sectors 1-6

Sector	θ_1^*	θ_2^*	θ_3^*	θ_4^*
1	θ_1	θ_2	θ_3	θ_4
2	$2\pi/3 - \theta_2$	$2\pi/3 - \theta_1$	$2\pi/3 - \theta_4$	$2\pi/3 - \theta_3$
3	$2\pi/3 + \theta_1$	$2\pi/3 + \theta_2$	$2\pi/3 + \theta_3$	$2\pi/3 + \theta_4$
4	$4\pi/3 - \theta_2$	$4\pi/3 - \theta_1$	$4\pi/3 - \theta_4$	$4\pi/3 - \theta_3$
5	$4\pi/3 + \theta_1$	$4\pi/3 + \theta_2$	$4\pi/3 + \theta_3$	$4\pi/3 + \theta_4$
6	$2\pi - \theta_2$	$2\pi - \theta_1$	$2\pi - \theta_4$	$2\pi - \theta_3$

Fig. 4.43. Reference vector, three nearest vectors and their coordinates.

$$\Delta = (x_1 y_2 - x_2 y_1) + (x_2 y_3 - x_3 y_2) + (x_3 y_1 - x_1 y_3) \quad (4.36)$$

$$d_1 = (x_0 (y_2 - y_3) + y_0 (x_3 - x_2) + (x_2 y_3 - x_3 y_2)) / \Delta \quad (4.37)$$

$$d_2 = (x_0 (y_3 - y_1) + y_0 (x_1 - x_3) + (x_3 y_1 - x_1 y_3)) / \Delta \quad (4.38)$$

$$d_3 = (x_0(y_1 - y_2) + y_0(x_2 - x_1) + (x_1y_2 - x_2y_1))/\Delta \quad (4.39)$$

where (x_n, y_n) $n = 0..3$, are the coordinates of auxiliary vector points.

4.5.3 Power sharing

In operating modes 1 and 2, only one energy storage system is used at a time. The other one is simply disengaged and hence does not participate in power exchange. Therefore, power sharing between the battery and the supercapacitor bank has to be done through alternative selection as shown in Fig. 4.44(a) where the ESS management algorithm [150] generates a suitable value for the battery/supercapacitor (B/SC) selection control signal. This signal controls the time sharing between the battery and the supercapacitor bank with the aid of a pulse width modulation (PWM) unit. To illustrate this power sharing operation, a simulation was carried out for a situation where the main inverter power is larger than the demand power as shown in Fig. 4.44(b). This surplus of power should be absorbed by the battery, supercapacitor or both. When the value of the B/SC selection control signal is zero only the supercapacitor is given access to absorb the surplus power as shown in Fig. 4.44(c) where the battery current I_b is zero and supercapacitor current I_{SC} is at its maximum. The opposite happens at the other extreme of the control signal. At intermediate values both energy storage devices share the incoming power as shown in Fig. 4.44(c). This simulation was carried out for balanced conditions and hence both ESS devices share an equal amount of power at the midpoint, which is 0.5, of the control signal. If the supercapacitor voltage is larger than the battery voltage this intersection point moves to the left.

Fig. 4.44. (a) Power sharing controller, (b) input power, P_m , and load power, P_l , (c) battery current, I_b , and supercapacitor current, I_{sc} (filtered).

In the third operating mode, both energy storage systems are used simultaneously. Therefore, the power sharing between two energy storage systems is carried out by changing the small vector composition of the auxiliary inverter [151]. In order to illustrate the effects of small vectors on power sharing, a simulation was carried out with two batteries attached to the auxiliary inverter dc-link as shown in Fig. 4.47(b). When there is a surplus of power the increased use of upper small auxiliary vectors increase the charging current of the lower battery as shown in Fig. 4.45(a). Similarly, if lower small auxiliary vectors are used increasingly, the upper battery experiences an increased charging current and the lower battery current gets reduced as shown in Fig. 4.45(b). Therefore, it is possible to change the charging current, and hence power sharing between the two batteries, by changing the composition of small auxiliary vectors.

Similarly, when there is a deficit of power the increased use of upper small auxiliary vectors increases the discharging current of the upper battery as shown in Fig. 4.45(c). If lower small auxiliary vectors are increasingly used, the upper battery gets discharged slowly as shown in Fig. 4.45(d). The above analysis is valid for the remaining two cases where the dc-link capacitors are replaced with two supercapacitor banks and a combination of a battery bank and a supercapacitor bank. A summary of this analysis is given in the Table 4.12. Based on Table 4.12, it can be deduced that the power sharing between the two ESSs can be controlled by controlling the small vector composition. The same controller shown in Fig. 4.44(a) can be used for this purpose.

Fig. 4.45. Battery currents (a) increased use of upper small auxiliary vectors when there is a surplus of power, (b) increased use of lower small auxiliary vectors when there is a surplus of power, (c) increased use of upper small auxiliary vectors when there is a deficit of power, (d) increased use of lower small auxiliary vectors when there is a deficit of power.

Table 4.12. Charge/discharge rates at upper and lower small vectors

Power condition	Upper small vectors		Lower small vectors	
	Lower battery current	Upper battery current	Lower battery current	Upper battery current
$P_{in} > P_{out}$	Charging High	Charging Low	Charging Low	Charging High
$P_{in} < P_{out}$	Discharging Low	Discharging High	Discharging High	Discharging Low

4.5.4 Low voltage ride through capability

LVRT requirements are imposed to avoid disconnection of the WTG after short term voltage sag. A typical LVRT characteristic is shown in Fig. 4.46. In order to meet this requirement, energy produced by the WTG during the low-voltage event should be reduced, dissipated or stored. In the absence of such control, the power produced by the WTG under faulty conditions will remain within the electric machine, resulting in an increase in the rotor speed [29]-[32]. A certain amount of energy can be stored in rotating masses. However, this is finite due to the maximum allowable rotor operating

speed. Furthermore, it is preferable to keep the speed constant at the pre-fault value, in order to minimize transients upon re-closing or reestablishment of the system connection [29] [30].

Options available to handle the energy that the grid cannot absorb are as follows: 1) control pitch angle of rotor blades so that the energy captured from the wind get reduced; 2) dumping the energy in a resistor, which is typically connected to the dc bus of the grid side inverter; 3) storing excess energy in a battery and/or a supercapacitor bank [31]. The proposed system achieves LVRT requirements in three ways. In the first case, the supercapacitor bank is used to absorb excess energy. Once the supercapacitor bank is fully charged battery bank is selected as the ESS element. This is the second option and the last one is the combined use of both energy storage devices. This happens only when the voltage drop is very large and individual inner hexagons are not touching the reference circle.

Fig. 4.46. Typical LVRT characteristic.

4.5.5 Other alternative configurations of the auxiliary inverter

Even though the 3x3 dual inverter system shown in Fig. 4.37 is proposed for interfacing a battery/supercapacitor hybrid energy storage system, it is possible to connect two supercapacitor banks or two battery banks to the dc-link of the auxiliary inverter as shown in Figs. 4.47(a) and 4.47(b) respectively. These two alternative configurations have their own advantages, limitations and control requirements as follows.

4.5.5.1 Interfacing two supercapacitor banks

In this particular configuration, the battery is replaced with another supercapacitor bank as shown in Fig. 4.47(a). The resultant system is suitable for short term power exchange. Capacitor voltage balancing is possible for this configuration and it can be achieved through the same control signal shown in Fig. 4.44(a).

4.5.5.2 Interfacing two battery banks

The other configuration, shown in Fig. 4.47(b), is more suitable for mitigating long term power fluctuations. The controller shown in Fig. 4.47(a) can be used for this particular configuration as well for power sharing between the two batteries. However, voltage imbalance is unavoidable in this configuration since the batteries can be at different states of charge.

Fig. 4.47. Alternative configurations of the auxiliary inverter for ESS interfacing (a) interfacing two supercapacitor banks, (b) interfacing two battery banks.

4.5.6 Simulation results

To illustrate the performance of the proposed modulation method and the power sharing controller, simulations were carried out using the MATLAB/SIMULINK software package. System parameters of the simulation setup are given in Table 4.13. A test voltage profile shown in Fig. 4.48(a), which synthesizes the operation of a wind turbine generator coupled active rectifier, was programmed into the dc-source of the main inverter. The controller was set to maintain a constant power dispatch, P_l , as shown in Fig. 4.48(b). In the first case, the B/SC control signal was set to zero so that

only the supercapacitor is used to absorb fluctuations present in the input power, P_m , shown in Fig. 4.48(b). Corresponding supercapacitor current and voltage variations are shown in Figs. 4.48(c) and 4.48(d) respectively. Since the battery is left unconnected its current remains at zero level.

In the second case, the B/SC control signal was set to 0.5 so that both battery and the supercapacitor should share fluctuations in the same way. The, corresponding current waveforms are shown in Fig. 4.48(e) which illustrates good current sharing between the battery and the supercapacitor. Their voltage variations are shown in Fig. 4.48(f). These current and voltage waveforms show the efficacy of the proposed power sharing controller. Moreover, the range of supercapacitor voltage variation is lower under this power sharing mode of operation than the previous case.

In the third case, the B/SC control signal was set to 1 so that only the battery is supposed to absorb the fluctuations. The corresponding battery current variation is shown in Fig. 4.48(g). Supercapacitor current remains at zero since it is not connected to the system. Similarly, the supercapacitor voltage remains unchanged as shown in Fig. 4.48(h). These results indicate that with the proper use of B/SC control signal it is possible to direct slow fluctuations towards the battery and fast fluctuations towards the supercapacitor bank. The inverter output voltage and its fundamental component of the a -phase are shown in Figs. 4.48(i) and 4.48(j) respectively. The inverter output current is shown in Fig. 4.48(k). These three waveforms confirm the efficacy of the proposed modulation and control techniques in producing undistorted current even in the presence of unevenly distributed space vectors.

Table 4.13. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Auxiliary inverter switching frequency	$f_s = 5\text{kHz}$
Nominal voltage of the battery bank	$V_b = 300\text{V}$
Range of the main inverter dc-link voltage, V_{dc}	0-1000V
DC-Link capacitors C_1, C_2	$C = 2200\mu\text{F}$
Capacitance of the supercapacitor bank	$C_{sc} = 100\text{F}$
Supercapacitor voltage (maximum)	$V_{sc,max} = 400\text{V}$
Peak value of the grid voltage	$V_{pk} = 330\text{V}$

Rated power of the PMSG	$P_{r, PMSG} = 100\text{kW}$
Rated wind speed	$V_{w,co} = 10\text{m/s}$

(a)

(b)

(c)

(d)

(e)

(f)

Fig. 4.48. (a) Main inverter dc-link voltage V_{dc} , (b) input power P_m and dispatch power P_l , (c)(d) battery/supercapacitor currents and voltages for control=0, (e)(f) battery/supercapacitor currents and voltages for control=0.5, (g)(h) battery/supercapacitor currents and voltages for control=1, (i) inverter output voltage, v_{as} , (j) filtered inverter output voltage, $v_{as,f}$, (k) inverter output current, i_{as} .

4.5.7 Experimental results

Schematic diagram and photographs of the experimental setup are shown in Figs. 4.49(a) and 4.49(b) respectively. System parameters of the experimental setup are given in Table 4.14. A variable ac source (California Instruments 4500Ls, 4.5kW) is used to generate an input power profile, P_{in} , as shown in Fig. 4.50(a). Output power

level is maintained at a constant level, marked as P_{load} , as shown in the same figure. The operating mode 2 is used in this experiment and hence all the fluctuations are absorbed by the supercapacitor bank, and the battery is not affected. The corresponding battery and supercapacitor current variations are shown in Fig. 4.50(b). Battery and supercapacitor voltages are shown in Fig. 4.50(c). The main inverter dc-link voltage is shown in Fig. 4.50(d). The inverter output voltage waveform is shown in Fig. 4.50(e). This waveform together with the inverter output current waveform shown in Fig. 4.50(f) prove the efficacy of the proposed SVM method in producing undistorted current even under unbalanced dc-link voltages. Even though fluctuations are present in the input power, output voltage, current and power are not affected.

Fig. 4.49. (a) Schematic of the experimental setup, (b) photographs of the experimental setup.

Fig. 4.50. Experimental results (a) input power P_{in} , input power P_{load} , battery power $P_{battery}$, and supercapacitor power P_{sc} , (b) battery current, I_b , and supercapacitor current I_{sc} (filtered), (c) battery voltage V_b , and supercapacitor voltage V_{sc} , (d) main inverter dc-link voltage V_{dc} , (e) enlarged view of the inverter output voltage, (f) enlarged view of the inverter output current.

Table 4.14. System parameters of the experimental setup

Fundamental frequency	$f = 10\text{Hz}$
Switching frequency	$f_s = 500\text{Hz}$
Load resistance	$R_L = 8\Omega$
Load inductance	$L_L = 6\text{mH}$
Nominal battery voltage	$V_L = 18\text{V}$
Supercapacitor voltage (maximum)	$V_{sc,max} = 25\text{V}$
Capacitance of the supercapacitor bank	$C_{sc} = 100\text{F}$
Number of supercapacitors	10

4.6 Summary

Energy storage interfacing capabilities of four dual inverter topologies namely: 2x2, 2x3, 3x2 and 3x3, are analyzed in detail in this chapter. The 2x2 dual inverter system

is suitable for interfacing both battery and supercapacitor energy storage systems separately. However, the energy storage system should be rated for the maximum possible dc-link voltage of the auxiliary inverter which in turn increases the number of cells connected in series. As a result effective series resistance gets increased. The 2x3 dual inverter system provides a solution to this issue by reducing the voltage of each ESS module to a half.

The 3x2 dual inverter is proposed to increase the power rating of the main inverter while interfacing a supercapacitor bank through the auxiliary inverter. However, this topology is capable of absorbing only short term power fluctuations. Therefore, the 3x3 dual inverter system based battery/supercapacitor direct integration scheme is proposed for mitigating both short term and long term power fluctuations. Furthermore, it improves the power rating and LVRT capability of the inverter.

Chapter 5 Hybrid cascaded multilevel inverter for wind generation

5.1 Introduction

Cascaded H-bridge multilevel inverters have been increasingly used in high and medium power applications [36], [86], [87], [90], [92], [116], [152]. Modularity and linear relationship between the number of inverter elements and voltage levels are the key features which make this topology popular among power electronic engineers. Furthermore, the independence in switching frequency of each module makes it possible to operate high-voltage cells at low frequency and low-voltage cells at high frequency. This unique feature helps to avoid excessive switching losses [90], [153].

However, each H-bridge module requires an isolated dc-source which is not practical in certain applications such as wind generation. Recent researches have demonstrated the possibility of replacing some of the isolated sources with capacitors [153]-[158]. But, these designs still require an isolated source for each phase [154]-[158], or special transformer arrangement to operate from a single dc-source [153].

Hybrid cascaded multilevel inverters have been introduced as an alternative for cascade H-bridge inverters which are less affected from the aforementioned shortcomings. This family of inverters is formed by combining a high voltage traditional two-level or three-level inverter with low voltage H-bridge modules [159]-[164]. H-bridge modules are powered by capacitors while the dc-link of the traditional inverter is powered by a dc-source. This arrangement preserves all the benefits of cascade H-bridge inverters while operating with a single dc-source. Furthermore, to minimize switching losses, the two-level (or three-level) inverter is switched at the fundamental frequency while H-bridges are operated with pulse width modulation (PWM) at high frequency. Number of levels in the output voltage can be increased by increasing the number of H-bridge stages and dc-link voltage ratios.

In addition to the single source operation, the possibility of supercapacitor direct integration into the dc-links of H-bridge modules makes this topology an ideal choice as the grid-side inverter for wind energy conversion systems.

5.2 Hybrid cascaded multilevel inverter with supercapacitor direct integration

This chapter presents a new direct integration scheme for supercapacitors using a hybrid cascaded multilevel grid-side inverter. The inverter used in this study consists of a conventional two-level inverter and three H-bridge modules as shown in Fig. 5.1. In the proposed system, conventional dc-link capacitors of H-bridge modules are replaced with three supercapacitor banks. This approach eliminates the need for additional interfacing dc-dc converters and thus reduces power losses, cost, complexity and response time. The two-level inverter, named as the main inverter, is operated in the six step mode and hence it produces square wave outputs. Harmonics of the square wave output are compensated by H-bridge modules which operate in the PWM mode. Furthermore, H-bridge modules operate at low voltages compared to the main inverter. As a result, main inverter becomes the high power low speed inverter and H-bridge modules become low power high speed units. This particular power and frequency splitting arrangement helps to reduce switching losses and device ratings of the main inverter [90], [165] [166]. Therefore, the main inverter can be built with high power slow devices like GTOs, or IGCTs. On the other hand the H-bridge modules can be built using IGBTs [167].

Fig. 5.1. Proposed hybrid cascaded multilevel inverter based supercapacitor direct integration scheme.

In order to get the maximum use of supercapacitors, they should be operated in the variable voltage mode. And hence, dc-link voltages of H-bridge units are allowed to vary with stored energy in supercapacitor banks. Furthermore, the dc-link voltage of the main inverter is varied with supercapacitor charging/discharging conditions. This variable

voltage operation makes the space vectors distribution uneven. A detailed analysis on this problem is given in section 5.4. In the first half of section 5.4, dc-link voltages of H-bridges are assumed to be equal. This assumption is valid when a balancing technique is used with conventional capacitors. However, due to two reasons, the above assumption is not applicable in the proposed system. The first reason is unequal capacitances due to aging and manufacturing tolerances. The second reason is the large capacity of supercapacitors which takes considerable amount of time to reach a balanced condition. Therefore, dc-link voltage imbalance in H-bridge units is possible and unavoidable. This particular voltage imbalance distorts the hexagonal shape of the corresponding vector pattern. A detailed analysis of this issue is presented in the latter part of section 5.4.

Conventional carrier based modulation methods assume balanced conditions, or at least possible balancing within few milliseconds, and hence they are not capable of producing undistorted current waveforms under dc-link voltage imbalance conditions. Even existing space vector modulation (SVM) methods, which exploit the equilateral shape of triangles, are not developed to work under distorted geometrical shapes. Taking these facts into account, a modified carrier based PWM (CBPWM) method and a novel SVM method have been developed for the proposed supercapacitor direct integration scheme. The modified CBPWM method is presented in section 5.5.1. The proposed SVM technique is built from the scratch and relevant equations and diagrams are given in section 5.5.2. It is obvious that the proposed SVM technique involves inevitable complex computations compared to simplified SVM techniques. However, those calculations do not create significant burdens on present day fast digital controllers such as FPGA, DSP, microcontroller etc. Therefore, the proposed SVM technique can be realistically implemented with the use of such a controller.

A supercapacitor voltage balancing technique is presented in the section 5.6. Control strategies for the proposed supercapacitor direct integration scheme are presented in section 5.7. A power loss comparison between the proposed direct integration scheme and the conventional dc-dc converter based approach is presented in section 5.8 with simulation results to show the usefulness of the proposed system. Experimental results are presented in section 5.9 to show the capability of the proposed system to absorb short-term power fluctuations.

5.3 Supercapacitor charging and discharging

The per-phase equivalent circuit of the hybrid cascaded multilevel inverter is shown in Fig. 5.2 where v_M represents the main inverter voltage vector, v_H represents the voltage vector produced by H-bridges and v_{grid} represents the grid voltage vector. The current injected onto the grid is denoted by i . The output voltage vector of the inverter system is equivalent to the addition of the main voltage vector and the H-bridge voltage vector as in (5.1). Real power output of the inverter can be expressed as a dot product in (5.2). Furthermore, the output power is equivalent to the sum of the main inverter power and the H-bridge power as expressed in (5.3). Equations (5.4) and (5.5) show the relationships between inverter voltage vectors and corresponding switching states. With the help of these five equations, an expression can be derived for the power of the H-bridges, in other words supercapacitor power, as in (5.6).

Fig. 5.2. Per-phase equivalent circuit of the hybrid cascaded multilevel inverter.

$$v_{out} = v_M + v_H \quad (5.1)$$

$$P_{out} = \frac{3}{2} v_{out} \cdot i \quad (5.2)$$

$$P_{out} = \frac{3}{2} (v_M + v_H) \cdot i = P_M + P_H \quad (5.3)$$

$$v_M = \frac{2}{3} V_{dc} \left(S_{aM} + S_{bM} e^{j\frac{2\pi}{3}} + S_{cM} e^{-j\frac{2\pi}{3}} \right) \quad (5.4)$$

$$v_H = \frac{2}{3} \left(V_{sca} S_{aH} + V_{scb} S_{bH} e^{j\frac{2\pi}{3}} + V_{scc} S_{cH} e^{-j\frac{2\pi}{3}} \right) \quad (5.5)$$

$$P_H = \frac{3}{2} \left(v_{out} - \frac{2}{3} V_{dc} \left(S_{aM} + S_{bM} e^{j\frac{2\pi}{3}} + S_{cM} e^{-j\frac{2\pi}{3}} \right) \right) \cdot i \quad (5.6)$$

Where P_M and $S_{iM} = \{0, 1\}$ ($i=a, b, c$) represent the main inverter power and switching states while those of the H-bridges are represented by P_H and $S_{iH} = \{-1, 0, 1\}$ ($i=a, b, c$) respectively. v_{out} represents the inverter output voltage and P_{out} represents the real power

output of the inverter.

According to (5.6), it can be deduced that, for a given output power, H-bridge power (supercapacitor power) varies with the main inverter dc-link voltage, V_{dc} . Therefore, supercapacitor power can be controlled by controlling the main inverter dc-link voltage. The simulation results shown in Fig. 5.3 prove this relationship.

Fig. 5.3. Effects of variable voltages (a) dc-link voltages, (b) input, output and supercapacitor power, (c) inverter output voltage v_{as} , (d) zoomed in view of the inverter output voltage v_{as} , (e) inverter output current, i_{as} .

5.4 Effects of variable dc-link voltages

As a result of the variable voltage operation of H-bridge modules and the main inverter, space vector diagram of the hybrid inverter takes different shapes at different dc-link voltage ratios as shown in Fig. 5.4. Vertices of the main hexagon represent space vectors of the main inverter. If the supercapacitor voltages are balanced, space vectors produced by H-bridge modules can be represented by attached sub hexagons. However, only two such sub hexagons are shown in Fig. 5.4 for clarity. When the main inverter dc-link voltage decreases, the main hexagon shrinks making more overlapping of sub hexagons as shown in Fig. 5.4(a). This increases the number of levels in the inverter output voltage. Overlapping of sub hexagons gets reduced when V_{dc} increases as shown in Fig. 5.4(c). The corresponding inverter output voltage variations are shown in Fig. 5.3(c). It is evident from this waveform that the number of levels in the inverter output voltage varies with the dc-link voltage ratio. An enlarged view of the inverter output voltage of the a -phase is shown in Fig. 5.3(d) to illustrate the multilevel operation of the inverter system. The inverter output current of the a -phase, shown in Fig. 5.3(e), proves the efficacy of the suggested modifications for conventional carrier based PWM, which is explained in section 5.5.1, to generate desired currents even under variable voltage conditions.

Circles marked in Fig. 5.4 indicate the path of the reference voltage vector. When the available wind power is not sufficient to supply the demand, the dc-link voltage of the main inverter will be reduced by the controller [168] [169]. Consequently, the main hexagon becomes smaller than the circle, as shown in Fig. 5.4(a). Then the deficit will be supplied by supercapacitor banks by discharging their stored energy, as shown by the first half of the power variation shown in Fig. 5.3(b). Similarly, when there is a surplus of wind power, the main hexagon exceeds the circle as shown in Fig. 5.4(c). Then the supercapacitor banks get charged as illustrated in the latter part of the power variation shown in Fig. 5.3(b).

Fig. 5.4. Space vector diagram of the hybrid cascaded multilevel inverter at different voltage ratios (balanced supercapacitor voltages are assumed).

In the above analysis dc-link voltages of H-bridges are assumed to be balanced. However, as mentioned before the above assumption is not applicable when supercapacitors are attached to the H-bridges. Unequal voltage in H-bridges move the edges of sub hexagons from their original locations and form a distorted polygon as shown in Fig. 5.5. Equations (5.7), (5.8) and Table 5.1 are used to determine new locations of these space vectors. Switching states and corresponding gate signals of the H-bridge module 1 is given in Table 5.1. Other two modules also follow the same pattern.

Fig. 5.5. Uneven distribution of space vectors produced by H-bridge modules under unbalanced conditions.

$$V_{dsx} = \frac{2}{3} \left(V_{sca} S_{aH} - \frac{1}{2} V_{scb} S_{bH} - \frac{1}{2} V_{scc} S_{cH} \right) \quad (5.7)$$

$$V_{qsx} = \frac{1}{\sqrt{3}}(V_{scb}S_{bH} - V_{scc}S_{cH}) \quad (5.8)$$

where S_{aH} , S_{bH} and S_{cH} are switching states of H-bridge modules.

Table 5.1. Switching states and gate signals of H-bridge 1

Switching state (S_{aH})	Gate signals ($S_{a1}.. S_{a4}$)
-1	1001
0	1100 or 0011
1	0110

5.5 Modulation strategies

Modulation and control of the hybrid cascaded multilevel inverter are extensively discussed in literature [160]-[164]. They all assume balanced conditions or employ some techniques to obtain balanced conditions within a few milliseconds. But as explained in the previous section voltage imbalance is unavoidable in the proposed system. Therefore, conventional modulation methods cannot directly be used in the proposed system. As solutions to this issue, a modified carrier based PWM (CBPWM) method and a novel space vector PWM (SVPWM) method are proposed in sections 5.5.1 and 5.5.2 respectively. The CBPWM method is intended for analog implementation while the SVPWM method is targeted for digital implementation.

5.5.1 Modified carrier based PWM method

The modified CBPWM method is summarized in the block diagram shown in Fig. 5.6. In the proposed system, the main inverter is operated in the six step mode, which produces square wave outputs as shown in Fig. 5.7(a) by the graph named V_{atl} . For this operation the only input required is the angle information, α_m , of the reference voltage vector. The square wave generator uses this angle to determine switching states S_{aM} , S_{bM} and S_{cM} of the main inverter. Equation (5.9) is then used to calculate voltage levels of the square wave output. The difference between the square wave output and the reference voltage is obtained to generate reference voltages for H-bridge modules. This difference is then normalized using (5.10) and pulse width modulated with two carriers as shown in Fig. 5.7(b). The corresponding switching signals of the H-bridge module 1, output voltage and

Fig. 5.6. Block diagram of the modified carrier based PWM method.

Fig. 5.7. (a) Square wave output of the main inverter and the reference voltage, (b) difference between the square wave output and the reference, (c) switching signals for H-bridge 1, (d) inverter output voltage, (e) inverter output current.

current are shown in Figs. 5.7(c) to 5.7(e) respectively. The switching state ‘1’ means a positive addition from the supercapacitor to the phase voltage. Similarly, the switching state ‘-1’ means a negative addition to the phase voltage. The switching state ‘0’ simply bypasses the H-bridge module without adding any value to the phase voltage. In (5.10) actual voltages are used instead of normalized values to take variable voltages into account. This modification handles both variable and unbalanced voltage conditions.

$$\begin{bmatrix} V_{atl} & V_{btl} & V_{ctl} \end{bmatrix}^T = \frac{2V_{dc}}{3} \begin{bmatrix} S_{aM} & S_{bM} & S_{cM} \end{bmatrix}^T \quad (5.9)$$

$$\begin{bmatrix} v_{adiff} \\ v_{bdiff} \\ v_{cdiff} \end{bmatrix} = \begin{bmatrix} \frac{(V_{atl} - v_{a,ref})}{V_{sca}} \\ \frac{(V_{btl} - v_{b,ref})}{V_{scb}} \\ \frac{(V_{ctl} - v_{c,ref})}{V_{scc}} \end{bmatrix} \quad (5.10)$$

In order to test the performance of the modified CBPWM method under unbalanced conditions supercapacitors were given different initial voltages as shown in Fig. 5.8(a). The corresponding inverter output voltage of the *a*-phase is shown in Fig. 5.8(b). Fundamental components of inverter output voltages are shown in Fig. 5.8(c). These waveforms together with output currents shown in Fig. 5.8(d) prove the ability of the modified CBPWM in generating undistorted outputs even under unbalanced conditions.

(a)

(b)

Fig. 5.8. (a) DC-Link voltage variations, (b) inverter output voltage, v_{as} , (c) fundamental components of inverter output voltages, (d) inverter output current, (e) input power, output power and supercapacitor power.

This simulation was carried out for a situation where in the input power is larger than the output power. The surplus of power is absorbed by supercapacitors as shown Fig. 5.8(e). As a result, supercapacitor voltages increase as shown in Fig. 5.8(a). The balancing algorithm, discussed in section 5.6, was disabled in this particular simulation and hence supercapacitor voltages rise at an equal rate.

5.5.2 Space vector PWM method

The space vector diagram of the combined inverter consists of a main hexagon, formed by the vectors of the main inverter, and superimposed seven sub polygons at each main vector point. These sub polygons represent vectors produced by H-bridge modules. Only one such polygon is shown in Fig. 5.9 for clarity. These polygons become hexagons when supercapacitor voltages are equal. A given reference voltage vector, with amplitude A_m and angle α_m , can be synthesized by combining a main vector, V_M , and the three nearest H-bridge vectors, V_1 , V_2 and V_3 , as shown in Fig. 5.9 [93], [170].

As mentioned in the introduction, the main inverter is operated in the six step mode by moving from one main vector to the other as shown in Fig. 5.10(a). The corresponding square wave output voltage waveform is shown in the first half of Fig. 5.10(b). H-Bridge modules are bypassed during this period. Harmonic distortion of the output voltage is significant under this operation. After 20ms, H-bridge modules are turned on and consequently the output voltage becomes smooth with low harmonic distortion as shown by the second half of the waveform in Fig. 5.10(b).

Fig. 5.9. Space vector diagram of the combined inverter.

Fig. 5.10. (a) Two-level inverter vector transition pattern, (b) square wave output of the two-level inverter and smoothing effect of H-bridge modules, (c) simplified block diagram showing the proposed modulation process.

A simplified block diagram of the modulation process is shown in Fig. 5.10(c). Similar to the previous section, the only input required to determine the switching states, S_{aM} , S_{bM} , and S_{cM} , of the main inverter is the angle, α_m , of the reference voltage vector. The corresponding gate signals of the main inverter are derived from the above switching states. Then the d - q axis components of the main voltage vector are calculated using (5.11) and (5.12). In (5.11) and (5.12) actual dc-link voltage of the main inverter is used and hence outputs will not get affected from the changes in the main inverter dc-link voltage. As the next step of the modulation process, d - q axis components of the reference voltage vector are calculated using (5.13). The differences between d - q axis components of reference and main inverter voltage vectors are calculated using (5.14) and they become d - q axis components of the compensation vector which should be synthesized by H-bridge modules. Instantaneous angle of the compensation vector is calculated using (5.15). Based on this, angle sector number and three nearest vectors can be determined. However, due to supercapacitor voltage imbalances, the limit angles which mark the boundary between sectors also vary. Equations (5.16) to (5.21) should be used to calculate new limit angles and thus to determine the sector number. After finding the sector number, corresponding H-bridge vectors can easily be identified with the help of Table 5.2.

$$V_{ds,M} = \frac{2V_{dc}}{3} \left(S_{aM} - \frac{1}{2}S_{bM} - \frac{1}{2}S_{cM} \right) \quad (5.11)$$

$$V_{qs,M} = \frac{V_{dc}}{\sqrt{3}} (S_{bM} - S_{cM}) \quad (5.12)$$

$$\begin{bmatrix} v_{ds} & v_{qs} \end{bmatrix}^T = A_m \begin{bmatrix} \cos(\alpha_m) & \sin(\alpha_m) \end{bmatrix}^T \quad (5.13)$$

$$\begin{bmatrix} v_{ds,A}^* & v_{qs,A}^* \end{bmatrix}^T = \begin{bmatrix} (v_{ds} - v_{ds,M}) & (v_{qs} - v_{qs,M}) \end{bmatrix}^T \quad (5.14)$$

$$\alpha_A = \tan^{-1} \left(\frac{v_{qs,A}^*}{v_{ds,A}^*} \right) \quad (5.15)$$

$$\theta_1 = \tan^{-1} \left(\frac{\sqrt{3}(-V_{scb} + V_{scc})}{2(V_{sca} + 0.5(V_{scb} + V_{scc}))} \right) \quad (5.16)$$

$$\theta_2 = \tan^{-1} \left(\frac{\sqrt{3}(V_{scb} + V_{scc})}{2(V_{sca} + 0.5(-V_{scb} + V_{scc}))} \right) \quad (5.17)$$

$$\theta_3 = \tan^{-1} \left(\frac{\sqrt{3}(V_{scb} + V_{scc})}{2(-V_{sca} + 0.5(-V_{scb} + V_{scc}))} \right) \quad (5.18)$$

$$\theta_4 = \tan^{-1} \left(\frac{-\sqrt{3}(V_{scb} - V_{scc})}{2(V_{sca} + 0.5(V_{scb} + V_{scc}))} \right) \quad (5.19)$$

$$\theta_5 = \tan^{-1} \left(\frac{-\sqrt{3}(V_{scb} + V_{scc})}{2(-V_{sca} + 0.5(V_{scb} - V_{scc}))} \right) \quad (5.20)$$

$$\theta_6 = \tan^{-1} \left(\frac{-\sqrt{3}(V_{scb} + V_{scc})}{2(V_{sca} + 0.5(V_{scb} - V_{scc}))} \right) \quad (5.21)$$

Table 5.2. Sector calculation and H-bridge vector identification

α_A	Sector	V_1	V_2	V_3
$\theta_1 < \alpha_A \leq \theta_2$	1	000	1-1-1	11-1
$\theta_2 < \alpha_A \leq \theta_3$	2	000	11-1	-11-1
$\theta_3 < \alpha_A \leq \theta_4$	3	000	-11-1	-111
$\theta_4 < \alpha_A \leq \theta_5$	4	000	-111	-1-11
$\theta_5 < \alpha_A \leq \theta_6$	5	000	-1-11	1-11
$\theta_6 < \alpha_A$ or $\alpha_A \leq \theta_1$	6	000	1-11	1-1-1

After finding the three vectors, the next step is to determine switching times. According to the well known volt-second balancing principle, a given vector can be synthesized by three adjacent vectors. Equations (5.22) to (5.30) are used to calculate corresponding switching times T_1 - T_3 which are expressed as fractions of the sampling time [171]. After finding auxiliary vectors and corresponding dwell times, five segment switching is used as described in [139].

$$\begin{bmatrix} x_0 & y_0 \\ x_1 & y_1 \end{bmatrix} = \begin{bmatrix} v_{ds,A}^* & v_{qs,A}^* \\ 0 & 0 \end{bmatrix} \quad (5.22)$$

$$x_2 = \frac{2}{3} \left(V_{sca} S_{a2} - \frac{1}{2} V_{scb} S_{b2} - \frac{1}{2} V_{scc} S_{c2} \right) \quad (5.23)$$

$$y_2 = \frac{1}{\sqrt{3}} (V_{scb} S_{b2} - V_{scc} S_{c2}) \quad (5.24)$$

$$x_3 = \frac{2}{3} \left(V_{sca} S_{a3} - \frac{1}{2} V_{scb} S_{b3} - \frac{1}{2} V_{scc} S_{c3} \right) \quad (5.25)$$

$$y_3 = \frac{1}{\sqrt{3}} (V_{scb} S_{b3} - V_{sc} S_{c3}) \quad (5.26)$$

$$\Delta = (x_2 y_3 - x_3 y_2) \quad (5.27)$$

$$T_1 = (x_0(y_2 - y_3) + y_0(x_3 - x_2) + (x_2 y_3 - x_3 y_2)) / \Delta \quad (5.28)$$

$$T_2 = (x_0 y_3 - y_0 x_3) / \Delta \quad (5.29)$$

$$T_3 = (-x_0 y_2 + y_0 x_2) / \Delta \quad (5.30)$$

A computer simulation was carried out to test the performance of the proposed SVPWM method under unbalanced conditions. Initial voltages of supercapacitors were set to different values as shown in Fig. 5.11(a). The corresponding inverter output voltage of the α -phase is shown in Fig. 5.11(b). Fundamental components of inverter output voltages are shown in Fig. 5.11(c). These waveforms together with output currents shown in Fig. 5.11(d) prove the ability of the proposed SVPWM to generate desired outputs even under unbalanced conditions. This simulation was carried out for a situation where input power is less than the output power. The deficit of power is supplied by supercapacitors as shown in Fig. 5.11(e). As a result, supercapacitor voltages decrease as shown in Fig. 5.11(a). The balancing algorithm was disabled in this simulation as well and hence supercapacitor voltages drop at an equal rate.

(a)

(b)

Fig. 5.11. (a) DC-Link voltage variations, (b) inverter output voltage, v_{as} , (c) fundamental components of inverter output voltages, (d) inverter output current, (e) input, output and supercapacitor power.

5.6 Supercapacitor voltage balancing

The proposed supercapacitor voltage balancing method is based on vector timing adjustment of the main inverter. The notations T_a , T_b and T_c are used in the following analysis to denote the time spent on main vectors. Their relationships with main vectors are given in Table 5.3. Supercapacitor voltages are updated at every switching cycle and corresponding vector timings are calculated based on these measured voltages. For an example if the supercapacitor C_{sc} in the H-bridge module 3 shows the lowest voltage it is given the highest priority by allocating the maximum possible value, T_{max} , for the corresponding vector time T_c . Similarly, if the supercapacitor C_{scb} in the H-bridge module 2 shows the largest voltage, it is given the lowest priority by assigning the minimum value, T_{min} , for the corresponding vector time T_b . The remaining time, T_{mid} , is allocated for the vector time T_a . Equations (5.31) to (5.33) are used to calculate maximum, medium and minimum vector times.

Table 5.3. Notations for main vector timing

Main vector	100	110	010	011	001	101
Time	$T_a/2$	$T_c/2$	$T_b/2$	$T_a/2$	$T_c/2$	$T_b/2$

$$T_{\max} = \frac{V_{sc,\max}}{f(V_{sca} + V_{scb} + V_{scc})} \quad (5.31)$$

$$T_{\text{mid}} = \frac{V_{sc,\text{mid}}}{f(V_{sca} + V_{scb} + V_{scc})} \quad (5.32)$$

$$T_{\min} = \frac{V_{sc,\min}}{f(V_{sca} + V_{scb} + V_{scc})} \quad (5.33)$$

where f is the fundamental frequency.

A computer simulation was carried out to test the efficacy of the proposed supercapacitor voltage balancing method with different initial supercapacitor voltages as shown in Fig. 5.12(a). According to Fig. 5.12(a) the supercapacitor C_{scb} has the largest initial voltage and the supercapacitor C_{scc} has the lowest initial voltage. The supercapacitor C_{sca} has an initial voltage in between the maximum and the minimum. Power input to the system was varied as shown in Fig. 5.12(b) so that during first 400ms, the supercapacitors get charged. However, as shown in Fig. 5.12(c), their charging rates are not equal. The supercapacitor C_{scc} absorbs more power than the other two and hence it has the highest rate of increase of voltage as shown in Fig. 5.12(a). This condition is achieved by assigning the maximum value $T_{\max}$ to T_c as shown in Fig. 5.12(d). On the other hand, the supercapacitor C_{scb} absorbs the least amount of power during first 400ms and hence it shows the lowest rate of increase of voltage. This happens due to the assignment of minimum value $T_{\min}$ to T_b as shown in Fig. 5.12(d). The mid value T_{mid} is assigned to T_a and hence supercapacitor C_{sca} 's voltage increases at an intermediate rate. The end result is the convergence of supercapacitor voltages to a balanced condition as shown in Fig. 5.12(a).

There is a deficit of power during the 400ms to 800ms period and hence supercapacitors get discharged. But again their rate of discharge can take different values as depicted in Fig. 5.12(a) and Fig. 5.12(c). In fact supercapacitors C_{sca} and C_{scc} are already balanced at this point and therefore their rate of discharge is equal. The voltage gap between the supercapacitor C_{scb} and the other two are still narrowing as shown in Fig. 5.12(a). This

proves that the proposed balancing technique would work under discharging conditions as well. As illustrated in Fig. 5.12(b) supercapacitors do not absorb or supply power during the last 200ms period. But if there is an imbalance in supercapacitor voltages it can still be balanced using the proposed technique.

Fig. 5.12. (a) Supercapacitor voltage variations, (b) input, output and supercapacitor power, (c) individual supercapacitor power (heavily low pass filtered), (d) variation of main vector timings.

5.7 Control techniques

The controller for the proposed inverter system is shown in Fig. 5.13 which consists of two parts namely, the generator-side converter controller and the grid-side inverter controller. Both controllers are implemented in the synchronous reference frame. A variable three phase ac source is used as the generator in this study and its voltage and frequency are varied according to the wind turbine model [93]. Furthermore, the power

reference for the generator-side converter is derived from the wind turbine model [93]. In the generator-side controller the above power reference is compared with the actual generator power and the error is passed through a PI controller to generate a reference for the d -axis current component, i_{dm}^* . The reference for the q -axis current component, i_{qm}^* , is set to zero. These current references are then compared with actual currents and the errors are passed through PI controllers to generate voltage references for the subsequent PWM unit. Similarly, the grid-side inverter controller is implemented in the synchronous reference frame where the d -axis current component, i_d , is varied in order to control the active power transfer to the grid. The q -axis current component, i_q , is maintained at zero. The power reference for the grid-side inverter controller is obtained by passing the instantaneous output power of the generator-side converter through a low pass filter (LPF) [97]. This makes sure that fluctuations present in the input power are not passed to the grid. The residue power changes the dc-link voltage which in turn changes the supercapacitor power as explained in section 5.3. Furthermore, one charging or one discharging period of supercapacitors contains both charging and discharging of the main inverter dc-link capacitor. Therefore, ideally there is no net energy store or release in the dc-link capacitor in one cycle of supercapacitor charging or discharging. Moreover, the capacitance of the main inverter dc-link capacitor is very low compared to that of supercapacitors. Therefore, at the end, residue power is passed to supercapacitors.

In order to test the performance of this series compensation in terms of power losses the conventional approach of parallel compensation by tapping into the dc-link power is also considered in this study. For this analysis the same schematic diagram shown in Fig. 5.1 is used with the dc-dc converter shown in Fig. 5.14(a) is attached to the dc-link. Similarly, the controller shown in Fig. 5.13 is used together with an additional dc-dc converter controller shown in Fig. 5.14(b). This additional controller controls the dc-link voltage in a way that the dc-link capacitors of H-bridges remain at the specified voltage. As a result of this control action the residue power is directed only towards the supercapacitor attached to the dc-dc converter.

Fig. 5.13. Controller block diagram of the proposed hybrid cascaded multilevel inverter based supercapacitor direct integration scheme.

Fig. 5.14. (a) Interfacing dc-dc converter, (b) controller block diagram for the dc-dc converter.

5.8 Simulation results

The proposed supercapacitor direct integration scheme has been compared with the conventional dc-dc converter based approach using computer simulations on the MATLAB/Simulink/PLECS platform. System parameters of the simulation setups are given in Table 5.4. A variable three phase ac source is used as the generator in this simulation.

Results shown in Fig. 5.15 correspond to the proposed direct integration scheme and the results shown in Fig. 5.16 correspond to the conventional dc-dc converter based system. The wind speed profile used to test and compare the performance of the proposed system and control strategy is shown in both Figs. 5.15(a) and 5.16(a) with an average speed of 10m/s, 20% harmonic amplitude and 1Hz harmonic frequency. The corresponding

variations of the input power, P_{in} , power injected into the grid, P_{out} , and the supercapacitor power, P_{sc} , of the proposed system are shown in Fig. 5.15(b). The dc-dc converter based system also shows similar input/output power variations as shown in Fig. 5.16(b). However, in this system supercapacitor is attached to the dc-dc converter therefore its power is labeled as $P_{sc-dcdc}$. It follows the same pattern of the supercapacitor power variation shown in Fig. 5.15(b). Furthermore, the similarity in supercapacitor voltage variations in both the proposed scheme and the conventional approach which are shown in Figs. 5.15(c) and 5.16(c) respectively validate proposed charging/discharging process. Moreover, in the dc-dc converter based system capacitors in H-bridges do not contribute to the mitigation of power fluctuation and therefore their average power is zero as shown in Fig. 5.16(b) by the trace marked as $P_{cap-Hbridg}$. This is more evident from the regulated H-bridge voltages, V_{cabc} , shown in Fig. 5.16(c).

The major difference between the proposed system and the conventional approach is the change in the main inverter dc-link voltage. In the proposed system the main inverter dc-link voltage varies in a wide range as shown in Fig. 5.15(d). On the other hand the conventional dc-dc converter based system regulates the main inverter dc-link voltage as shown in Fig. 5.16(d). The corresponding dc-link currents, which are nearly constant due to constant power dispatch to the grid, are also shown in Figs. 5.15(d) and 5.16(d). This variable dc-link voltage and constant current operation of the proposed scheme increases the main inverter switching losses as shown in Fig. 5.15(e). Furthermore, in this figure discrete pulses appear as switching losses due to the six step operation of the main inverter. This is clearly distinguishable when compared with the switching losses of the H-bridges which are shown in Fig. 5.15(g). Due to the PWM operation of H-bridges the pulses which show the switching losses are more densely packed in this figure. However, when compared with the conduction losses of the main inverter and H-bridges, shown in Figs. 5.15(f) and 5.15(h) respectively, these switching losses are negligible for the switching frequency used in this study. Furthermore, the conduction loss is independent of the dc-link voltage and it varies only with the current passing through the devices and their turn on voltage drop. Therefore, the aforementioned conduction losses are nearly constant. Moreover the conduction loss of the H-bridges is nearly twice compared to that of the main inverter due to the doubling of the number of switching devices in H-bridges.

Similar power losses can be observed in the main inverter and H-bridges of the conventional dc-dc converter based system as shown in Figs. 5.16(e) and 5.16(f). Therefore, in terms of power losses in the main inverter and H-bridges there are no significant differences between the proposed scheme and the conventional approach. But the dc-dc converter used in the conventional system introduces additional switching and conduction losses as shown in Figs. 5.16(g) and 5.16(h) respectively.

Based on the aforementioned power losses, the amounts of energy losses can be calculated to make an accurate comparison between the systems. The corresponding results are shown in Figs. 5.15(i) and 5.16(i) respectively for the proposed scheme and the conventional approach. At the end of the simulation period the total energy loss of the proposed scheme is found to be 306J. The total energy loss of the main inverter and H-bridges of the conventional system found to be 304J which is very much similar to that of the proposed scheme. Apart from that, the conventional approach includes an additional energy loss of 52.7J which is due to the interfacing dc-dc converter. These results prove that the proposed scheme reduces power losses by 14.3% compared to the conventional dc-dc converter based approach without performance degradation.

Table 5.4. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency of H-bridge modules	$f_s = 5\text{kHz}$
Switching frequency of the dc-dc converter	$f_{sdc} = 15\text{kHz}$
Phase resistance of the generator	$R_m = 0.2\Omega$
Phase inductance of the generator	$L_m = 1\text{mH}$
DC-DC converter Inductance	$L_{dc} = 0.1\text{mH}$
Capacitance of the main inverter dc-link capacitor	$C_l = 1\text{mF}$
Capacitance of supercapacitors in H-bridges	$C_{scabc} = 30\text{mF}$
Capacitance of the supercapacitor in the dc-dc converter	$C_{scdc} = 90\text{mF}$
Filter resistance of the grid-side inverter	$R_{abc} = 0.1\Omega$
Filter inductance of the grid-side inverter	$L_{abc} = 1\text{mH}$
Grid voltage	$v_{ll,rms} = 690\text{V}$
Cut-in wind speed	$V_{w,cutin} = 4\text{m/s}$
Rated wind speed	$V_{w, rated} = 12\text{m/s}$
Main inverter switching device	SKM 145GB176D
H-bridge and dc-dc converter switching device	SKM100GB12T4

Fig. 5.15. Simulation results of the proposed direct integration scheme (a) wind speed profile, (b) input, output and supercapacitor power, (c) supercapacitor voltage, (d) dc-link voltage and current, (e) switching loss of the main inverter, (f) conduction loss of the main inverter, (g) switching loss of H-bridges, (h) conduction loss of H-bridges, (i) total energy loss of the main inverter and the H-bridges.

Fig. 5.16. Simulation results of the conventional dc-dc converter based integration system (a) wind speed profile, (b) input, output and supercapacitor power, (c) supercapacitor voltage, (d) dc-link voltage and current, (e) losses in the main inverter, (f) losses in H-bridges, (g) switching loss of the dc-dc converter, (h) conduction loss of the dc-dc converter, (i) total energy loss of the main inverter, H-bridges and the dc-dc converter.

5.9 Experimental results

Schematic diagram and photographs of the laboratory prototype are shown in Figs. 5.17(a) and 5.17(b) respectively. In this experiment the inverter system is connected to a balanced three phase RL load. System parameters of the experimental setup are given in Table 5.5. A large capacitor bank is used to emulate the high capacitance of the supercapacitor energy storage system. A variable ac source (California Instruments 4500Ls, 4.5kW) is used to power the main inverter and its output was rectified using a bridge rectifier. The ac source was programmed in a way that the rectifier output, in other words the main inverter dc-link voltage V_{dc} , varies as shown in Fig. 5.18(a). The corresponding main inverter dc-link current, I_{dc} , is shown in Fig. 5.18(b). This current is nearly constant due to the constant current demand of the load. Resultant input power, constant output power and supercapacitor power variations are shown in Fig. 5.18(c). At the beginning, the input power is equal to the demand and thus supercapacitor voltages remain unchanged as shown in Fig. 5.18(d). There is a step change in the input power at 250ms which charges the supercapacitor banks. At 1250ms another step change is introduced to the input power as shown in Fig. 5.18(c). This creates a deficit of power and hence supercapacitors discharge as shown in Figs. 5.18(c) and 5.18(d) to match the demand.

An enlarged view of the inverter output voltage of the a -phase, v_{as} , is shown in Fig. 5.18(e) to illustrate the multilevel operation of the cascade H-bridge inverter with the modified CBPWM method. The corresponding inverter output current of the a -phase, i_{as} , is shown in Fig. 5.18(f). These two waveforms prove the ability of the modified CBPWM method to generate undistorted current under unbalanced and changing conditions.

Fig. 5.17. (a) Schematic diagram of the experimental setup, (b) photographs of the experimental setup.

Fig. 5.18. Experimental results (a) main inverter dc-link voltage, (b) main inverter dc-link current (filtered), (c) input, output and supercapacitor power, (d) supercapacitor voltage, (e) enlarged view of the inverter output voltage, (f) inverter output current.

Table 5.5. System parameters of the experimental setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency of H-bridge modules	$f_s = 5\text{kHz}$
Load resistance	$R = 10\Omega$
Load inductance	$L = 6\text{mH}$
Capacitance of the large capacitor bank	$C_{scx} = 50\text{mF}$
Capacitance of the dc-link capacitor	$C_l = 1\text{mF}$

5.10 Summary

A hybrid cascaded multilevel inverter based supercapacitor direct integration scheme for wind power systems is proposed in this chapter. The proposed topology eliminates the need for interfacing dc-dc converters and thus eliminates associated cost and power losses. The elimination of dc-dc converter in interfacing supercapacitors takes away associated power losses. But in this scheme charging and discharging of supercapacitors depend on the main inverter dc-link voltage and therefore, the main inverter dc-link voltage varies in a large range compared to the conventional approach. This makes the space vector distribution uneven. Conventional modulation strategies are not capable of producing undistorted currents under such dynamic situations. Therefore, a modified carrier based pulse width modulation method and a novel space vector modulation method are proposed to generate undistorted current even under unbalanced supercapacitor voltage conditions. A capacitor voltage balancing method has also been presented. Furthermore, it is found that this variable voltage operation does not increase power losses. Simulation results prove that the proposed scheme reduces power losses by 14.3% compared to the conventional dc-dc converter based approach without performance degradation. Experimental results are presented to validate the efficacy of the proposed scheme and modulation method.

Chapter 6 Modular matrix converter for PMSG based wind energy conversion systems

6.1 Introduction

The capacity of modern wind-turbines has increased up to a few MWs and that enables harvesting of increased amount of power from wind and thus reducing the cost per MW of capacity. Power ratings of 3-5 MW per machine are becoming common in areas with large wind potentials, especially offshore wind installations [28] [29], [34], [172]. These multi-megawatt turbines produce large currents which lead to increased I^2R losses in transmission cables. Therefore, the usual practice is to install a step-up grid transformer in the nacelle of the wind turbine [172]. This inevitably increases mechanical loading on the turbine tower. Even though, it is possible to use marginally rated transformers to reduce the weight and size, it degrades the system reliability and thus not suitable for offshore applications [172]. Therefore, a transformer-less, high voltage and compact generator converter system that can be housed in the nacelle would be an attractive solution.

On the other hand, low speed, direct drive, air-cored PMSGs with large number of isolated stator coils gained more attention recently as a suitable generator technology [34], [172]-[174]. The major problem in interfacing such machines to the grid is the limitation imposed by voltage ratings of currently available switching devices in the converter. The conventional two-level back-to-back converter, shown in Fig. 6.1(a), does not meet ratings required for the grid interface of such large machines [34]. This has motivated designers to go for multilevel converters as they provided high voltage levels, low harmonic distortion and low voltage transition rate (dv/dt).

Commonly used multilevel topologies are: diode-clamped, capacitor-clamped and cascaded H-bridge converters. Diode-clamped three-level back-to-back converter is a potential solution for multi-megawatt wind generator systems. However, due to high voltage and current requirements, at present, they can only be implemented using gate commutated thyristors (IGCTs) which operates at very low frequencies compared to IGBTs. An alternative approach for the IGBT based implementation is the increase of the voltage levels. The drawback of this approach is the substantial increase in the diode

count. The capacitor-clamped topology, on the other hand, suffers from inherent drawback of capacitors such as high failure rate, cost, weight and volume.

In this context, cascaded H-bridge multilevel inverters (CHBMLI) has drawn much attention due to their modularized design, absence of clamping capacitors and clamping diodes, possible transformer-less grid connection and low switching losses. The transformer-less cascade H-bridge multilevel modular converter topologies proposed in [34], [172]-[174] consist of a PMSG with isolated coils, controlled rectifiers and dc-link capacitors. However, the major drawbacks of these topologies are the space requirement and less reliability of dc-link capacitors. As a solution to this issue, a modular cascaded matrix converter topology has been proposed in this chapter as shown in Fig. 6.1(b). Internal arrangements of switching devices are shown in Fig. 6.2.

Fig. 6.1. (a) Conventional back-to-back converter system, (b) proposed modular matrix multilevel converter.

A variant of this topology has been proposed in [175] and [176] for motor drive applications. However, the possibility of implementing it in wind energy conversion systems has not yet been investigated. The proposed modular matrix converter eliminates dc-link capacitors with an increase of diode count. This increase, however, can be justified by the improved reliability of diodes over capacitors and their wide availability at low cost. Furthermore, the proposed solution is directly applicable for standard multi-coil PMSGs and thus special machine designs are not required.

A detailed description on the operation of a single converter module is presented in Section 6.2. Section 6.3 explains the circuit arrangement of a single-phase converter with three modules and proper multilevel voltage waveform generation through a modified switching strategy. Grid-side controller for a three phase converter system is presented in Section 6.4. Simulation results are presented in Section 6.5 to prove the efficacy of the proposed modular matrix converter, modulation method and control technique.

6.2 Operating principle of the matrix converter module

Schematic diagram of the matrix converter module is shown in Fig. 6.2. If the switching function of a switch, S_{jk} ($j \in \{a, b, c\}$ and $k \in \{p, n\}$) is defined as ‘0’ when it is open and ‘1’ when it is closed, voltage at the two output terminals (v_p, v_n) of the converter module can be obtained using (6.1). The resultant output voltage is given in (6.2) and it can take both positive and negative values.

Fig. 6.2. Schematic diagram of the matrix converter module.

$$\begin{bmatrix} v_p \\ v_n \end{bmatrix} = \begin{bmatrix} S_{ap} & S_{bp} & S_{cp} \\ S_{an} & S_{bn} & S_{cn} \end{bmatrix} \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \quad (6.1)$$

$$v_{pn} = v_p - v_n \quad (6.2)$$

A given reference voltage can be synthesized with the proper control of switching signals. The corresponding modulation process is explained below. In order to simplify the modulation process, a single cycle of the input three-phase voltage waveform is divided into six sectors as shown in Fig. 6.3. Equation (6.3) relates the output voltage of the matrix converter module to input voltages for the first sector, i.e. $0^0 < \theta \leq 60^0$. For unity power factor control at the input side the condition in (4) should satisfy. Based on (6.3) and (6.4), expressions can be derived for switching times as in (6.5)-(6.7).

Fig. 6.3. Three-phase output voltage from the generator and the sector selection.

$$v_{pn,ref}T_s = (E_a - E_b)t_1 + (E_c - E_b)t_2 \quad (6.3)$$

$$\frac{t_1}{t_2} = \frac{E_a - E_b}{E_c - E_b} \quad (6.4)$$

$$t_1 = \frac{v_{pn,ref}T_s(E_a - E_b)}{(E_a - E_b)^2 + (E_c - E_b)^2} \quad (6.5)$$

$$t_2 = \frac{v_{pn,ref}T_s(E_c - E_b)}{(E_a - E_b)^2 + (E_c - E_b)^2} \quad (6.6)$$

$$t_0 = T_s - t_1 - t_2 \quad (6.7)$$

where T_s is the sampling time and t_1 and t_2 are switching intervals of the two line to line voltages $E_a - E_b$ and $E_c - E_b$. Since the three phase supply voltages coming from the generator are assumed to be balanced, as in (6.8), expressions for switching intervals can be simplified further as in (6.9) and (6.10). Switching times for the remaining five sectors are also calculated in the same manner and a summary is given in Table 6.1.

$$E_a + E_b + E_c = 0 \quad (6.8)$$

$$t_1 = \frac{v_{pn,ref} T_s (E_a - E_b)}{5E_b^2 - 2E_a E_c} \quad (6.9)$$

$$t_2 = \frac{v_{pn,ref} T_s (E_c - E_b)}{5E_b^2 - 2E_a E_c} \quad (6.10)$$

Table 6.1. Switching time calculation

Angle, θ	t_1	t_2
$0^0 < \theta \leq 60^0$	$\frac{v_{pn,ref} T_s (E_a - E_b)}{5E_b^2 - 2E_a E_c}$	$\frac{v_{pn,ref} T_s (E_c - E_b)}{5E_b^2 - 2E_a E_c}$
$60^0 < \theta \leq 120^0$	$\frac{v_{pn,ref} T_s (E_a - E_c)}{5E_a^2 - 2E_b E_c}$	$\frac{v_{pn,ref} T_s (E_a - E_b)}{5E_a^2 - 2E_b E_c}$
$120^0 < \theta \leq 180^0$	$\frac{v_{pn,ref} T_s (E_b - E_c)}{5E_c^2 - 2E_a E_b}$	$\frac{v_{pn,ref} T_s (E_a - E_c)}{5E_c^2 - 2E_a E_b}$
$180^0 < \theta \leq 240^0$	$\frac{v_{pn,ref} T_s (E_b - E_a)}{5E_b^2 - 2E_a E_c}$	$\frac{v_{pn,ref} T_s (E_b - E_c)}{5E_b^2 - 2E_a E_c}$
$240^0 < \theta \leq 300^0$	$\frac{v_{pn,ref} T_s (E_c - E_a)}{5E_a^2 - 2E_b E_c}$	$\frac{v_{pn,ref} T_s (E_b - E_a)}{5E_a^2 - 2E_b E_c}$
$300^0 < \theta \leq 360^0$	$\frac{v_{pn,ref} T_s (E_c - E_b)}{5E_c^2 - 2E_a E_b}$	$\frac{v_{pn,ref} T_s (E_c - E_a)}{5E_c^2 - 2E_a E_b}$

Once the switching times are calculated, the next step is to generate pulse width modulated (PWM) switching signals. The PWM pattern suitable for a single matrix converter module is illustrated in Fig. 6.4. It should be emphasized here that heights and widths of PWM signals vary with time and the diagram shown in Fig. 6.4 corresponds only for a situation where $0^0 < \theta \leq 30^0$. Performance of the modulation strategy proposed for a single matrix converter module has been tested in computer simulations for an RL load where $R=5\Omega$ and $L=1\text{mH}$. The corresponding simulation results are shown in Fig. 6.5. A programmable three-phase ac source, which represents split windings of a wind generator, is used to supply the module.

Fig. 6.4. PWM pattern for the matrix converter module.

Fig. 6.5. (a) Input voltage, (b) output voltage v_{pn} , (c) zoomed in view of the output voltage showing the PWM pattern, (d) output current, (e) input current of the a -phase.

A single cycle of the three-phase input voltage waveforms are shown in Fig. 6.5(a). Frequency of the input voltage is set to be relatively low compared to the grid frequency owing to the slow spin of the direct driven wind turbine generator. The corresponding output voltage of the converter module is shown in Fig. 6.5(b). Even though it looks like a traditional two level waveform it actually consists of five voltage levels. In order to illustrate these voltage levels and the PWM pattern, a zoomed in view of the output voltage is shown in Fig. 6.5(c). It only shows the two positive voltage levels and the zero level. Similarly, there are two negative voltage levels as well. Output current and the corresponding input current of the a -phase are shown Figs. 6.5(d) and 6.5(e) respectively. Power pulsations at twice the grid frequency are inevitably present at the input. An analysis on this issue and possible solution for certain applications can be found in [176] [177].

6.3 Operation of a single phase with three cascaded matrix converter modules

The matrix converter module shown in Fig. 6.2 can be used as a building block to obtain a high voltage cascaded single phase converter as shown Fig. 6.6. Even though only three modules are used in Fig. 6.6 it is possible to extend it with more modules. However, PWM strategy has to be configured accordingly to get proper multilevel voltage waveforms. If an identical PWM pattern, e.g. the pattern shown in Fig. 6.4 is used, output voltage of each module switches at the same time and thus output voltage would still look like traditional two-level waveform. Effect of this unified switching is illustrated in the output voltage waveform shown in Fig. 6.7(b). The shape of this waveform is exactly similar to that in Fig. 6.5(b). The only difference is the amplitude which is three times higher than that in Fig. 6.5(b). This can be explained as the addition of the output voltages of the three matrix converter modules. A zoomed in view of the output voltage, for three sampling periods, is shown in Fig. 6.7(c) to illustrate this summing process. As a result of this unified switching, the load experiences large step changes in voltage which is not desirable in most cases.

Fig. 6.6. Single phase cascaded matrix converter with three modules.

Fig. 6.7. Improper multilevel output voltage waveform generated by unified switching (a) input voltage of a module, (b) output voltage, (c) voltage summing process with unified switching.

Fig. 6.8. PWM pattern for the cascaded matrix converter shown in Fig. 6.6.

The solution to this problem is the distribution of switching times as shown Fig. 6.8. The resultant multilevel output voltage waveform is shown in Fig. 6.9(a). Compared to the waveform in Fig. 6.7(b) step changes in the output voltage is significantly low in this waveform. A zoomed in view of the output voltage is also shown in Fig. 6.9(b) to illustrate the voltage summing process with proposed PWM patterns.

Fig. 6.9. Proper multilevel voltage waveform generated with the proposed switching pattern (a) output voltage, (b) voltage summing process.

6.4 Grid-side controller

The grid-side controller of the three-phase modular matrix converter employs an inner current controller and an outer power controller as shown Fig. 6.10. The grid voltage and current injected into the grid are converted into the synchronous reference frame. The direct component of the current (i_d) controls the active power exchange while the quadrature component (i_q) controls the reactive power. Therefore, to generate a reference for the direct current component, the instantaneous active power P is compared with the reference P_{ref} and then the error is passed through a PI stage. The active power reference is generated by the maximum power tracking controller of the wind turbine generator. The quadrature current reference i_q^* is set to zero to cancel out the reactive power transfer to the grid. These active and reactive current references, (i_d^* and i_q^*), are compared with actual current components and the errors are then passed through PI controllers to produce voltage references v_d^* and v_q^* . Equations (6.11) and (6.12) are then used to calculate the amplitude and angle of the reference voltage vector. Then the corresponding phase voltages references are generated based on the equations (6.13)-(6.15). These phase voltage references are equally divided among converter modules in each phase.

$$A_m = \frac{1}{3} \sqrt{v_{ds}^{*2} + v_{qs}^{*2}} \quad (6.11)$$

$$\alpha_m = \tan^{-1} \left(\frac{v_{qs}^*}{v_{ds}^*} \right) + \theta \quad (6.12)$$

$$v_{a,ref} = A_m \sin(\omega_0 t + \alpha_m) \quad (6.13)$$

$$v_{b,ref} = A_m \sin \left(\omega_0 t + \alpha_m - \frac{2\pi}{3} \right) \quad (6.14)$$

$$v_{c,ref} = A_m \sin \left(\omega_0 t + \alpha_m + \frac{2\pi}{3} \right) \quad (6.15)$$

where θ is the initial phase angle of the voltage vector and ω_0 is angular frequency of the grid voltage.

Fig. 6.10. Grid-side controller.

6.5 Simulation results

The modular matrix converter, proposed for wind energy conversion systems, has been tested in the MATLAB/Simulink/PLECS digital simulation platform. A top level block diagram of the simulation setup is shown in Fig. 6.11(a). System parameters of the simulation setup are given in Table 6.2. Each block in Fig. 6.11(a) represents the matrix converter module shown in Fig. 6.2. The modified PWM switching pattern discussed in section 6.3 is used in each phase of the converter. Programmable three-phase ac sources which represent split-windings of a large direct driven wind generator are used to power each module.

In order to test the dynamic performance of the proposed system and the controller, a step change of 110kW to 220kW was introduced to the output power reference at 125ms. The corresponding variations in the output power and d - q axis currents are shown in Figs. 6.11(b) and 6.11(c) respectively. The output three-phase voltage waveforms and line-to-line voltage v_{ab} of the proposed modular matrix converter are shown in Fig. 6.11(d). Multilevel operation of the proposed converter is clearly visible in the line-to-line voltage waveform. The corresponding output current variation of the a -phase is shown in Fig. 6.11(e).

The input voltage and current of the second module of the a -phase is shown in Figs. 6.11(f) and 6.11(g) respectively. Similar variations are present in other modules as well. The input current contains the second harmonic of the grid-frequency. As a result, power pulsations at twice the grid frequency are present in the input side of this three-phase

converter as well. This is inevitable due to the absence of an energy storage element such as capacitor. The output power variation of a single matrix converter module and the corresponding phase leg are shown in Fig. 6.11(h) to prove the power balancing between converter modules.

Table 6.2. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Switching frequency	$f_s = 2.5\text{kHz}$
Feeder resistance	$R_f = 0.2\Omega$
Feeder inductance	$L_f = 1\text{mH}$
Maximum output voltage of a module	$v_{pn, \max} = 800\text{V}$
Maximum output voltage of a phase	$v_{out, \max} = 2400\text{V}$
Peak value of the grid voltage	$V_{p, \text{grid}} = 1500\text{V}$
Rated power of the wind generator	$P_{r, \text{PMSG}} = 500\text{kW}$

Fig. 6.11. (a) Top level schematic diagram of the simulation setup, (b) dynamic response of the system for a step change in the output power reference, (c) d - q axis currents, (d) output three-phase voltages and line-to-line voltage v_{ab} , (e) output current of the a -phase, (f) input voltage of a matrix converter module, (f) input current of a module, (g) output power of a module and the phase leg showing the power balancing operation.

6.6 Summary

A matrix converter topology for grid connection of large, direct driven, split winding PMSG based wind turbine generators is proposed. The matrix converter system consists of large number of converter modules which are fed from isolated three-phase generator coils. Outputs of matrix converter modules are connected in series to increase the output voltage and thus to eliminate the need of a coupling step-up transformer. Moreover, dc-link capacitors found in alternative approaches are eliminated in the proposed system. Therefore, the proposed system would be an attractive solution for the need for transformer-less, high voltage, highly-reliable and compact converter system for nacelle installation in offshore wind power systems. The modulation process of the proposed modular matrix converter, grid-side controller and proper multilevel voltage waveform generation through modified PWM switching are explained in this chapter. Simulation results are presented to show the efficacy of the proposed system, modulation method and the controller.

Chapter 7 STATCOMs in wind farms

7.1 Introduction

With the continuous growth of individual wind turbine capacity as well as the capacity of wind farms voltage at the point of common coupling (PCC) tends to vary with the wind speed. These fluctuations create serious stability issues and, if not adequately compensated, ultimately result in voltage collapse. Therefore, wind farm operators have been forced to tighten their grid connection rules, also known as grid codes, in order to limit the effects of wind power fluctuations on network quality and stability [178]-[181].

The main reason for voltage instability is found to be the inability to meet the reactive power demand and thus the solution essentially lies on reactive power compensation [47], [147], [182]. The conventional solution for reactive power compensation in a wind farm is the use of a centralized unit dedicated for reactive power compensation. Static synchronous compensators (STATCOMs) have been proved to be the ideal solution for this task due to their extremely fast response, less harmonic distortion and the much smaller reactor requirement. Transient and short-term generator stability conditions can also be improved when a STATCOM has been introduced into the system as a voltage/var supporter [183]-[191].

The introduction of variable speed wind turbine generators, equipped with full-scale converters (FSC), enabled localized reactive power compensation within the generator [192]-[195]. However, complex control and coordination among wind turbine generators within the wind farm are crucial for the proper operation [196]. Furthermore, the reactive power capability of individual wind turbine generators vary with available wind power and has certain limitations such as rated MVA, converter voltage and current limitations. Therefore, individual turbines cannot supply the total reactive power demand all the time [194]-[196]. This makes the centralized reactive power compensation inevitable even in modern wind farms, but their capacity can be reduced. Therefore, this chapter presents a novel centralized STATCOM topology for such systems, its modulation strategy and control technique.

7.2 Reactive power compensation capability of individual wind turbines

Full-scale back-to-back converter equipped wind energy conversion systems are capable of generating reactive power for voltage regulation at the PCC of the wind farm. In fact, in certain countries wind farms are rewarded to be capacitive at peak hours and inductive at low loads, even if it is not generating active power [196]. Therefore, reactive power compensation at individual wind turbines plays an important role in power system stability as well as in income generation.

However, the grid-side converter of a variable speed wind turbine generator has a certain maximum current-carrying capacity, which will impose a limit on the active and reactive power capability of the turbine. In the PQ plane, it will be a circle similar to that of the armature current limit of a synchronous generator, as shown in Fig. 7.1. The relationship between the active and reactive power at the converter current limit is given in (7.1)

$$S^2 = P^2 + Q^2 \quad (7.1)$$

where S is the complex output power, P is the active output power and Q is the reactive output power. The converter voltage V_s will impose another limit on P and Q -capability of the wind turbine, which is similar to that of the field current limit of a synchronous generator. In order to develop a mathematical model for the limit imposed by the converter voltage the power flow diagram and the phasor diagram, shown in Fig. 7.2(a) and Fig. 7.2(b) are used. Based on these diagrams two expressions can be derived for the active and reactive power of the full-scale converter as in (7.4) and (7.7).

These two expressions can be combined as in (7.8) to derive a relationship between P and Q and thus obtain the voltage limit of the converter as in (7.9). A careful analysis on (7.9) would reveal that it represents a circle in the PQ plane with radius r and the centre at the Q axis with an offset c . It is marked in the capability curve shown in Fig. 7.1 and named as the converter voltage limitation. In addition to the aforementioned limitations, there is another limitation imposed by the rated power of the wind turbine generator which is named as the shaft power in Fig. 7.1.

Fig. 7.1. Capability curve of a wind energy conversion system (WECS) with a full-scale power electronic converter.

Fig. 7.2. (a) Single line diagram showing the power flow of the WECS, (b) phasor diagram.

$$P = V_g I_s \cos \varphi \quad (7.2)$$

$$V_s \sin \delta = X I_s \cos \varphi \quad (7.3)$$

$$P = \frac{V_g V_s \sin \delta}{X} \quad (7.4)$$

$$Q = V_g I_s \sin \varphi \quad (7.5)$$

$$V_s \cos \delta - V_g = X I_s \sin \varphi \quad (7.6)$$

$$Q = \frac{V_g V_s \cos \delta}{X} - \frac{V_g^2}{X} \quad (7.7)$$

$$\left(\frac{V_g V_s \sin \delta}{X} \right)^2 + \left(\frac{V_g V_s \cos \delta}{X} \right)^2 = P^2 + \left(Q - \frac{V_g^2}{X} \right)^2 \quad (7.8)$$

$$P^2 + \left(Q - \frac{V_g^2}{X} \right)^2 = \left(\frac{V_g V_s}{X} \right)^2 \quad (7.9)$$

$$c = \left(0, -\frac{V_g^2}{X} \right) \quad (7.10)$$

$$r = \frac{V_g V_s}{X} \quad (7.11)$$

Based on the above analysis it can be concluded that the concept of reactive power generation from WECSs equipped with full-scale converters is practical. However, it has certain limitations and thus a centralized reactive power generator such as a STATCOM should still be available to go beyond these limitations. Therefore, next section proposes a novel STATCOM topology suitable for modern WECSs.

7.3 Proposed STATCOM topology

In the simplest form, STATCOMs employ two-level Voltage Source Converters (VSC) for power processing. However, a multilevel configuration is preferable to achieve higher ac-side voltage levels and improved waveforms with reduced harmonic distortion. Multilevel converter topologies such as diode-clamped converter, flying-capacitor converter and cascading converter have been successfully implemented in STATCOMs [47], [147], [188]-[191], [197]-[199].

Cascaded Multilevel Converter (CMC) topologies have recently become a popular choice for the implementation of high power STATCOM systems. Amongst these topologies the CMC with separate DC sources can be considered as the most popular due to its modularity and flexibility [200]. However, the need for large number of separate DC sources, which is usually supplied with capacitors in STATCOM applications, makes this STATCOM bulky and less reliable. To overcome this limitation, a STATCOM with a combined converter topology, which is formed by cascading two 3-level diode-clamped converters through a coupling transformer, is proposed. This CMC topology needs only four dc-link capacitors and 24 switches to synthesize the 9-level operation [144].

Fig. 7.3 shows the schematic of the proposed STATCOM in which the two inverters, “Bulk inverter” and “Conditioning inverter” are connected at the ends of a coupling transformer secondary winding. The bulk inverter operates at a low frequency producing

square wave outputs while high frequency low power conditioning inverter is used to make output waveforms smoother and closer to sinusoidal in shape. As the high-power bulk inverter operates at a lower frequency, it can be constructed using devices like GTOs, ETOs or IGCTs. On the other hand, the conditioning inverter, which acts to compensate low order harmonics produced by the bulk inverter, can be constructed using more commonly available devices like IGBTs. This particular power and frequency splitting arrangement helps to reduce switching losses of the inverter [143] [144].

Fig. 7.3. Schematic diagram of the proposed STATCOM.

A detailed description on proposed modulation and control techniques for the cascaded multilevel inverter is given in section 7.4. DC-Link capacitor voltage balancing is discussed in section 7.5. The STATCOM controller that is proposed to mitigate potential voltage variations in a wind energy conversion system is discussed in section 7.6. Both simulation and experimental results are presented in sections 7.7 and 7.8 to verify the practical viability of the proposed system, which, according to the results, is suitable for wind power generation systems.

7.4 Modulation and control of the inverter

For the cascaded inverter shown in Fig. 7.3, line to ground voltages of the bulk and conditioning inverters can be derived from the switching states using (7.12) and (7.13). In (7.12), S_a , S_b and S_c are the switching states of the bulk inverter while S_{ax} , S_{bx} and S_{cx} of (7.13) represents switching states of the conditioning inverter. They can take values of 0, 1 or 2. It is assumed in (7.12) and (7.13) that the dc-link capacitor voltages are balanced. The corresponding phase voltages of the coupling transformer secondary winding can be determined using (7.14).

$$\begin{bmatrix} v_{ag} & v_{bg} & v_{cg} \end{bmatrix}^T = \begin{bmatrix} S_a & S_b & S_c \end{bmatrix}^T \frac{V_{dc}}{2} \quad (7.12)$$

$$\begin{bmatrix} v_{agx} & v_{bgx} & v_{cgx} \end{bmatrix}^T = \begin{bmatrix} S_{ax} & S_{bx} & S_{cx} \end{bmatrix}^T \frac{V_{dcx}}{2} \quad (7.13)$$

$$\begin{bmatrix} v_{ast} \\ v_{bst} \\ v_{cst} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} - v_{agx} \\ v_{bg} - v_{bgx} \\ v_{cg} - v_{cgx} \end{bmatrix} \quad (7.14)$$

$$\begin{bmatrix} v_{dst} & v_{qst} & V_0 \end{bmatrix}^T = [K] \begin{bmatrix} v_{ast} & v_{bst} & v_{cst} \end{bmatrix}^T \quad (7.15)$$

Space vector plot of the inverter is shown in Fig. 7.4, which is obtained by transforming phase voltages of (7.14) into d - q components using Park's transformation $[K]$ in (7.15). Darker dots in the space vector diagram represent the switching states of the bulk inverter and are known as “bulk vectors”. They can be categorized into five groups. 1) Large vectors 200, 220, 020, 022, 002 and 202; 2) Medium vectors 210, 120, 021, 012, 102 and 201; 3) Negative small vectors 100, 110, 010 011, 001, and 101; 4) Positive small vectors 211, 221, 121, 122, 112 and 212 and 5) Zero vectors 000, 111 and 222. Therefore, altogether there are 27 bulk vectors marked with darker dots. Each darker dot is the origin of another smaller hexagonal pattern which represents the switching states of the conditioning inverter. They are the vectors of the conditioning inverter and are simply known as “conditioning vectors”. These small hexagons also have the same vector pattern as the bulk inverter. As a result of this, 27X27 different vectors can be identified for this cascaded-3/3 inverter. But some of them overlap as shown in Fig. 7.4 reducing the number of effective vectors. The darker dots are marked with corresponding switching states. The switching state ‘2’ means both upper switches of the corresponding inverter

leg are turned on. Similarly, the switching state '1' means middle two switches are turned on and the switching state '0' means the lower two switches are turned on.

Fig. 7.4. Cascade inverter space vector diagram for $V_{dc} : V_{dcx} = 3:1$.

A given reference voltage vector can be synthesized by combining a bulk vector and three conditioning vectors [93]. As mentioned in the introduction, the bulk inverter produces square wave output by moving from one bulk vector to another slowly. In this process, depending on the amplitude, ($0 < A_m < 8$), of the reference voltage, v_{ref} , different bulk vector traversal patterns have to be used as shown in Fig. 7.5. However, due to operational limitations, caused by the absence of an active power source at the conditioning inverter dc-link, the upper limit of A_m , for steady state operation, gets reduced to 6. When $A_m > 4.58$, the bulk vector traversal pattern consists of large and medium bulk vectors as shown in Fig. 7.5(a). Sub hexagonal vector patterns are omitted in these diagrams as the focus at this point is only on bulk vectors. Bulk inverter output voltage for this range takes the shape as in Fig. 7.5(b). For $3.60 < A_m < 4.58$, medium and small bulk vectors are alternately used as in Fig. 7.5(c) and the corresponding bulk inverter output voltage waveform is shown in Fig. 7.5(d). For the range $1.73 < A_m < 3.60$, only small bulk vectors are used as in Fig. 7.5(e). In that case number of levels in the bulk

inverter output voltage gets reduced as seen in Fig. 7.5(f). However, in the STATCOM operation this range is hardly used. When $A_m < 1.73$, the bulk inverter is turned off and only the conditioning inverter continues its operation. This region is never used in the proposed STATCOM and hence it will not be discussed in this paper. The time spent on each bulk vector is a function of A_m , which varies as depicted in Fig. 7.5(g).

As mentioned above, bulk inverter produces square wave output while the conditioning inverter is used to suppress harmonics. This combined operation is illustrated Fig. 7.5(h) where the conditioning inverter is purposely turned off until 30ms. Harmonic distortion of the output voltage is high under this operation. After 30ms, conditioning inverter is turned on and consequently the output voltage becomes smooth with a low harmonic distortion. Therefore, one can consider the conditioning inverter as an active filter. In the case of harmonic filters, the given waveform is subtracted from the ideal waveform and then the difference is compensated. The same idea is used in the proposed modulation method.

Fig. 7.5. Bulk vector traversal patterns for (a) $A_m > 4.58$, (c) $3.60 < A_m < 4.58$, (e) $1.73 < A_m < 3.60$, (b), (d), (f) corresponding bulk inverter output voltage waveforms, (g) bulk vector timing, (h) effect of the conditioning inverter.

Fig. 7.6 shows the bulk inverter vector diagram with three axes v_a , v_b and v_c which correspond to relevant phase voltages v_{ast} , v_{bst} and v_{cst} . Available bulk inverter phase voltage levels are marked on the v_a axis. For a given amplitude A_m , corresponding bulk inverter phase voltage levels, $V_{ast, bulk}$, can be found in Table 7.1. A plot of these levels and the reference are shown in Fig. 7.7(a) and their difference is shown in Fig. 7.7(b). This difference is the voltage which should be supplied by the conditioning inverter as the compensation voltage. Subsequently, it is pulse width modulated using two triangular carriers as shown in Fig. 7.75(b). A low frequency carrier is used here for clarity. The corresponding switching signals for the leg 'a' of the conditioning inverter are shown in Fig. 7.7(c).

Fig. 7.6. Phase voltage levels of the bulk inverter.

Fig. 7.7. Modulation technique (a) reference voltage and square wave output of the bulk inverter, (b) difference between the square wave output and the reference, (c) switching signals for the leg 'a' of the conditioning inverter.

Table 7.1. Bulk inverter phase voltage levels for different ranges of A_m

Range of A_m	Bulk inverter phase voltage levels $V_{ast, bulk}$						
$4.58 < A_m < 6$	-6	-4.5	-3	0	3	4.5	6
$3.60 < A_m < 4.58$	-4.5		-3	-1.5	0	1.5	3
$1.73 < A_m < 3.60$	-3		-1.5	0	1.5	3

Fig. 7.8. Conditioning inverter controller block diagram.

Fig. 7.8 shows the block diagram of the combined inverter controller where the square wave generator produces bulk inverter switching states S_a , S_b and S_c . Rest of the controller generates suitable conditioning inverter switching states S_{ax} , S_{bx} and S_{cx} based on the above mentioned harmonic filtering technique. A PI controller is used to regulate the conditioning inverter dc-link voltage to 1/3 of the bulk inverter dc-link voltage. This ratio is required for the nine level operation of the combined inverter. The PI controller adds a small delay angle δ_α to the phase angle of conditioning inverter reference voltage which in turns draws some active current from the bulk inverter to charge conditioning inverter dc-link capacitors [144]. This lagging operation is illustrated in the space vector diagram shown in Fig. 7.9. A Redundant State Selection (RSS) algorithm, followed by the PWM process, is used to balance capacitor voltages [93].

Fig. 7.9. Delay angle δ_α .

7.5 Capacitor voltage balancing

The proposed modulation method equally generates both positive and negative small conditioning vectors. Therefore, for a given constant amplitude A_m , conditioning inverter capacitors get charged and discharged equally. In other words they tend to maintain their initial conditions, as shown in Figs. 7.10(a) and 7.10(b), as long as A_m is constant. However, deviations can occur at transients of A_m . The sudden change of the amplitude at $t = 0.2\text{s}$, creates a short term imbalance in the capacitor charging and discharging pattern. Consequently, one voltage goes up while the other goes down. But due to the tight regulation on the conditioning inverter dc-link voltage their addition remains constant. These new voltage levels will remain after the transition period as shown in Figs. 7.10(a) and 7.10(b). Therefore, the proposed modulation method itself is not capable of balancing capacitor voltages, especially in dynamic situations. To address this issue, authors have proposed a Redundant State Selection (RSS) based capacitor voltage balancing method in [93]. Simulation results shown in Fig. 7.11 prove the efficacy of this method in capacitor voltage balancing under steady state and dynamic conditions.

Fig. 7.10. Natural balancing of conditioning inverter capacitor voltages (a) (b) conditioning inverter capacitor voltages, (c) amplitude of the reference voltage vector.

Fig. 7.11. Forced balancing of conditioning inverter capacitor voltages (a) (b) conditioning inverter capacitor voltages.

Fig. 7.12. Bulk inverter capacitor voltages with self balancing (a) (b) main inverter capacitor voltages, (c) amplitude of the reference voltage vector.

The same capacitor voltage balancing technique can be used for the bulk inverter as well by reversing current directions. However, it is valid only for the range of $1.73 < A_m < 4.58$ where small bulk vectors are available. If $A_m > 4.58$, only medium and large bulk vectors are available, this makes capacitor voltage corrections impossible. Large bulk vectors do not have a connection to the dc-midpoint and hence they cannot be used for capacitor voltage balancing. But medium bulk vectors have a single connection to the midpoint while the other two ends connect to the upper and lower points. Because of that, significant ripples can appear on capacitor voltages under unbalanced loads. Even for balanced loads, small ripples appear as shown in Figs. 7.12(a) and 7.12(b).

7.6 STATCOM control

Fig. 7.13 shows the controller block diagram of the STATCOM that controls the active and reactive power transfer between the grid and the STATCOM. The measured PCC voltage V_d in synchronous reference frame is compared with the reference V_d^* and the error signal produced is then fed into a PI controller that generates a current reference i_d^* for the inner current controller loop. The STATCOM's ac side currents are measured and transformed into the synchronous reference frame in the form of direct component, i_d , and quadrature component, i_q . The direct component is related to the real power exchange while the quadrature component is related to the reactive power exchange. Therefore, the bulk inverter dc-link voltage, V_{dc} , can be regulated by controlling the direct component of the STATCOM current.

Fig. 7.13. Controller block diagram of the STATCOM connected to a wind farm.

To regulate the grid voltage, the quadrature component of the STATCOM current is controlled [147], [187]. The current controller outputs, v_{dst}^* and v_{qst}^* are the reference voltages for the inverter. With these reference voltages, amplitude A_m and the phase angle

α_m of the STATCOM output voltage are calculated using (7.16) and (7.17). Then, the STATCOM inverter controller generates output voltages with the required amplitude and phase. The instantaneous angle θ , of the phase voltage vector, is obtained through a Phase Locked Loop (PLL).

$$A_m = \frac{9}{V_{dc}} \sqrt{v_{dst}^{*2} + v_{qst}^{*2}} \quad (7.16)$$

$$\alpha_m = \tan^{-1} \left(\frac{v_{qst}^*}{v_{dst}^*} \right) + \theta \quad (7.17)$$

7.7 Simulation results

Simulation results obtained using the MATLAB/Simulink/PLECS digital simulation platform are presented to verify the effectiveness of the proposed system. Schematic diagram of the simulation setup is shown in Fig. 7.14(a). System parameters of the simulation setup and controller gains are given in Tables 7.2 and 7.3 respectively. In order to test the dynamic response of the STATCOM, two step changes were applied to the supply voltage at $t = 300\text{ms}$ and $t = 700\text{ms}$ as shown in Fig. 7.14(b). If the STATCOM is not present load voltage will deviate from the nominal value as shown by the dashed line in Fig. 7.14(c). When the STATCOM is connected, it detects those deviations and injects appropriate amount of reactive power to bring the voltage back to the nominal value as shown in Fig. 7.14(c) by the continuous line. These results prove that the proposed STATCOM is capable of mitigating voltage fluctuations caused by sudden changes in the supply voltage. The variation of the reactive current reference i_q^* and the actual reactive current i_q of the STATCOM are shown in Fig. 7.14(d). The actual reactive current i_q follows the reference with a small delay. A small amount of active current, i_d , is drawn from the grid to compensate losses in the STATCOM and thereby maintain the bulk inverter dc-link voltage. Variations of the STATCOM a -phase current are shown in Fig. 7.14(e). STATCOM output voltage, load voltage and load current are shown in Figs. 7.14(f), 7.14(g) and 7.14(h) respectively. The bulk inverter and conditioning inverter dc-link voltage regulations are shown in Figs. 7.14(i) and 7.14(j) respectively. Note that the conditioning inverter dc-link voltage is maintained at one third of the bulk inverter dc-link voltage to obtain the 9-level operation. These results prove the efficacy of the proposed modulation and control techniques.

Fig. 7.14. Dynamic behavior of the STATCOM (a) schematic diagram of the simulation setup, (b) magnitude of the supply voltage, (c) variation of the load voltage magnitude with and without the STATCOM, (d) active and reactive currents of the STATCOM, (e) STATCOM a -phase current, (f) STATCOM output voltage, (g) load voltage, (h) load current, (i) bulk inverter capacitor voltages, (j) conditioning inverter capacitor voltages.

7.8 Experimental results

A. Experimental Setup

A laboratory setup of the test system shown in Fig. 7.14(a) was built for experimental verifications. A photograph of the experimental setup is shown in Fig. 7.15. Exaggerated views of both bulk and conditioning inverter modules are also shown in the bottom right

corner of the photograph. System parameters and controller gains of the experimental setup are given in Tables 7.4 and 7.3 respectively. In this experiment both inverters were built using IGBTs. But, as mentioned before the bulk inverter can be built with slow devices as well. The MATLAB/Simulink software platform and the dSPACE hardware interface are used to control the proposed STATCOM. Reactive power control and voltage regulation performances of the experimental setup were tested and the corresponding results are given in the sections 7.8B and 7.8C respectively.

Fig. 7.15. Photograph of the experimental setup.

B. Reactive power Control

Three step changes were applied to the reactive current reference, i_q^* , as shown in Fig. 7.16(a). The corresponding dynamic response of the STATCOM reactive current is shown in the same figure with the graph marked as i_q . Bulk inverter dc-link capacitor voltages are shown in Fig. 7.16(b) which are stable and equal in spite of transients in the STATCOM currents. Similarly, the controller regulates conditioning inverter dc-link capacitor voltages as shown in Fig. 7.16(c). An expanded view of the inverter output voltage is shown in Fig. 7.16(d).

Fig. 7.16. Dynamic response of the system for step changes in reactive power command (a) reactive current command and the response, (b) bulk inverter capacitor voltages, (c) conditioning inverter capacitor voltages, (d) inverter output voltage of the a -phase.

C. Voltage Regulation

The ac source is programmed to generate three step changes in the load voltage as shown in Fig. 7.17(a). At the beginning of this process the system of Fig. 7.14(a) is at steady state and the d -axis component of the load voltage V_d is at its nominal value. Therefore, reactive power injection is not required. Once a change in V_d is sensed the controller starts to inject reactive power as shown in Fig. 7.17(c) to bring V_d back to the nominal value. The result of this voltage restoration attempt is shown in Fig. 7.17(b). The corresponding variations of the STATCOM output currents are shown in Fig. 7.17(d). The variation of modulation index A_m and the power angle are shown in Figs. 7.17(e) and 7.17(f)

respectively. Apart from that, a small amount of active current, i_d , is drawn from the grid as shown in Fig. 7.17(g) to maintain capacitor voltages and replenish power loss due to switching and resistive components of the coupling transformer. The resulting dc-link voltage variations are shown in Fig. 7.17(h). It can be seen from these results that the proposed cascaded multilevel STATCOM and the controllers perform well in transient and steady state conditions.

Fig. 7.17. Experimental results showing voltage regulation (a) load voltage without STATCOM, (b) load voltage with the STATCOM, (c) injected reactive current, (d) STATCOM output current of the a -phase, i_{ast} , (e) amplitude of the reference voltage vector, A_m , (f) power angle, (g) active current drawn by the STATCOM, i_d , (h) bulk and conditioning inverter dc-link voltages.

Table 7.2. System parameters of the simulation setup

Fundamental frequency	$f = 50\text{Hz}$
Conditioning inverter switching frequency	$f_s = 5\text{kHz}$
STATCOM Interfacing Resistance	$R_f = 0.05\Omega$
STATCOM Interfacing Inductance	$L_f = 1\text{mH}$
Line resistance	$R_s = 0.08\Omega$
Line Inductance	$L_s = 1.3\text{mH}$
Load resistance	$R_L = 2.57\Omega$
Load Inductance	$L_L = 5\text{mH}$
Main inverter dc-link voltage	$V_{dc} = 4\text{kV}$
Conditioning inverter dc-link voltage	$V_{dcx} = 1.33\text{kV}$
DC-Link capacitors C_1, C_2, C_{X1} , and C_{X2}	$C = 6800\mu\text{F}$
Nominal value of d -axis voltage	$V_d = 2.4\text{kV}$
Rated power of the STATCOM	3MVA
Turns ratio of the coupling transformer	$n_1 : n_2 = 1 : 1$

Table 7.3. Parameters of PI controllers

PI Controller	Control Variable	Simulation Setup		Experimental Setup	
		Proportional Gain (K_p)	Integral Gain (K_I)	Proportional Gain (K_p)	Integral Gain (K_I)
PI 1	i_d	2 VA^{-1}	$50 \text{ VA}^{-1} \text{ S}^{-1}$	15 VA^{-1}	$500 \text{ VA}^{-1} \text{ S}^{-1}$
PI 2	i_q	30 VA^{-1}	$200 \text{ VA}^{-1} \text{ S}^{-1}$	45 VA^{-1}	$200 \text{ VA}^{-1} \text{ S}^{-1}$
PI 3	V_d	-0.5 AV^{-1}	$-100 \text{ AV}^{-1} \text{ S}^{-1}$	-0.1 AV^{-1}	$-8 \text{ AV}^{-1} \text{ S}^{-1}$
PI 4	V_{dc}	-0.1 AV^{-1}	$-2 \text{ AV}^{-1} \text{ S}^{-1}$	-0.2 AV^{-1}	$-0.2 \text{ AV}^{-1} \text{ S}^{-1}$
PI 5	V_{dcx}	-0.05 radsA^{-1}	$-0.1 \text{ radA}^{-1} \text{ S}^{-1}$	-0.01 radsA^{-1}	$-0.01 \text{ radA}^{-1} \text{ S}^{-1}$

Table 7.4. System parameters of the experimental setup

Fundamental frequency	$f = 50 \text{ Hz}$
Conditioning inverter switching frequency	$f_s = 3.2 \text{ kHz}$
STATCOM Interfacing Resistance	$R_f = 0.8 \Omega$
STATCOM Interfacing Inductance	$L_f = 3 \text{ mH}$
Line resistance	$R_s = 1.1 \Omega$
Line Inductance	$L_s = 18 \text{ mH}$
Load resistance	$R_L = 17 \Omega$
Load Inductance	$L_L = 11 \text{ mH}$
DC-Link voltage	$V_{dc} = 128 \text{ V}$
Conditioning inverter dc-link voltage	$V_{dcx} = 42.6 \text{ V}$
DC-Link capacitors C_1, C_2, C_{X1} , and C_{X2}	$C = 6800 \mu\text{F}$
Nominal value of d -axis voltage	$V_d = 90 \text{ V}$
Short circuit impedance of the STATCOM	$0.8 + j0.942$
Turns ratio of the coupling transformer	$n_1 : n_2 = 1 : 1$

7.9 Conclusions

The proposed STATCOM configuration provides high voltage and power ratings. In addition to that the hybrid structure of the VSC limits the dc-link capacitor count to 4. As a result, it has a high potential of being implemented in future high capacity wind farms for both active and reactive power compensation. Simulation and experimental results show good dynamic responses of the STATCOM for voltage variations at the PCC caused by sudden wind changes. These results indicate that the proposed cascade multilevel STATCOM is capable of suppressing voltage fluctuations caused by random wind changes.

7.10 Summary

Power fluctuations caused by random wind changes create serious stability issues on the grid voltage, especially at increased levels of penetration. The main reason for voltage instability is the inability to meet the reactive power demand and thus the solution lies on reactive power compensation. Modern wind turbine generators, equipped with full scale converters, are capable of supplying both active and reactive power to the grid and thus help to stabilize the grid voltage.

However, reactive power capabilities of individual wind turbine generators vary with available wind power and has certain limitations such as rated voltage and current of the converter. Therefore, individual turbines cannot supply the total reactive power demand all the time. This makes the conventional centralized reactive power compensation is inevitable even in modern wind farms, but at reduced capacity. Therefore, this chapter has presented a novel centralized reactive power compensator topology and its modulation and control for such systems.

Chapter 8 Conclusions and recommendations

8.1 Conclusions

Wind energy conversion is considered as the fastest growing and most promising renewable energy technology that can help to achieve carbon reduction commitments in 2020. Apart from increasing the worldwide installed wind power capacity, extracting maximum possible power from the wind is equally important to reach this target. Therefore, almost all the modern wind turbines operate in the variable speed mode. Nowadays, direct-drive, multi-pole, permanent magnet synchronous generators are dominating in the variable speed wind energy marked mainly due to their low maintenance, high efficiency and grid code compliance. Back-to-back converter systems are inevitable for the grid integration of these wind energy conversion system.

A comprehensive review on possible topologies for the generator-side converter is presented in chapter 2. Furthermore, compared to other topologies, the full controlled six switch two-level rectifier found to be the best solution which can produce both sinusoidal phase currents and dc-link voltage regulation. However, it does not meet voltage requirements, and as a result power requirements, of modern multi-MW wind energy conversion systems. In this context, diode-clamped and capacitor-clamped three-level converters are gaining more attention as the generator-side converter. Moreover, due to the unidirectional power flow of wind turbines, these topologies can be built with less number of switching devices. Furthermore, it is possible to replace conventional capacitors of capacitor-clamped three-level converters with supercapacitors and make them to absorb short term wind power fluctuations. The effectiveness of this arrangement has been justified with simulation results.

Similarly, three-level converters are becoming popular as the grid-connecting inverter in modern wind energy conversion systems. Furthermore, the diode-clamped topology is the most popular choice for implementing three-level converter systems. Energy storage interfacing capability of this topology has been investigated in chapter 3. Uneven distribution of space vectors found to be the biggest challenge in modulation and control of this unique approach. A novel space vector modulation technique, that can generate

undistorted current even in the presence of unevenly distributed space vectors, has been developed to address this issue.

The other alternative way of implementing three-level converters is the use of capacitor-clamped topology which is believed to be less reliable and bulky. These disadvantages can be turned into gains by making the inverter to absorb short term or long term power fluctuations. This can be achieved by connecting supercapacitors or batteries in parallel with clamping capacitors. Problems associated with these approaches are analyzed in detail and suitable modulation techniques are proposed with simulation results and experimental verifications. In summary, it can be concluded that proposed direct integrations schemes help to reduce power losses, cost and complexity by eliminating the need for interfacing dc-dc converters. Therefore, proposed schemes have high potential of being implemented in future wind energy conversion systems.

Energy storage interfacing capabilities of four dual inverter topologies namely: 2x2, 2x3, 3x2 and 3x3, are analyzed in detail in chapter 4. The 2x2 dual inverter system is suitable for interfacing both battery and supercapacitor energy storage systems. However, the energy storage system should be rated for the maximum possible dc-link voltage of the auxiliary inverter which in turn increases the number of cells connected in series. As a result effective series resistance gets increased and the battery management system becomes complex and expensive. The 2x3 dual inverter system provides a solution to this issue by reducing the voltage of each ESS module to a half.

The 3x2 dual inverter is proposed to increase the power rating of the main inverter while interfacing an energy storage system through the auxiliary inverter. However, this topology is only capable of absorbing short term power fluctuations. The 3x3 dual inverter system is capable of interfacing all three combinations of energy storage, i.e. battery only, supercapacitor only and the battery/supercapacitor hybrid. Therefore, this scheme is suitable of mitigating both short term and long term power fluctuations. Furthermore, it improves the power rating and low voltage ride through capability of the inverter.

A hybrid cascaded multilevel inverter based supercapacitor direct integration scheme for wind power systems is proposed in this chapter. The proposed topology eliminates the need for interfacing dc-dc converters and thus eliminates associated cost and power losses. The elimination of dc-dc converter in interfacing supercapacitors takes away associated power losses. But in this scheme main inverter dc-link voltage has to vary in a large range for charging and discharging of supercapacitors. This makes the space vector distribution uneven. A modified carrier based pulse width modulation method and a novel space vector modulation method are proposed to generate undistorted current in such situations. A capacitor voltage balancing method has also been presented. Furthermore, it is found that this variable voltage operation does not increase power losses significantly. Simulation results prove that the proposed scheme reduces power losses by 14.3% compared to the conventional dc-dc converter based approach without performance degradation. Experimental results are presented to validate the efficacy of the proposed scheme and modulation method.

A matrix converter topology for grid connection of large, direct driven, split winding PMSG based wind turbine generators is proposed. The matrix converter system consists of large number of converter modules which are fed from isolated three-phase generator coils. Outputs of matrix converter modules are connected in series to increase the output voltage and thus to eliminate the need of a coupling step-up transformer. Moreover, dc-link capacitors found in alternative approaches are eliminated in the proposed system. Therefore, the proposed system would be an attractive solution for the need of transformer-less, high voltage, highly-reliable and compact converter system for nacelle installation in offshore wind power systems. The modulation process of the proposed modular matrix converter, grid-side controller and proper multilevel voltage waveform generation through modified PWM switching patterns are explained in this chapter. Simulation results are presented to show the efficacy of the proposed system, modulation method and the controller.

Power fluctuations caused by random wind changes create serious stability issues on the grid voltage, especially at increased levels of penetration. The main reason for voltage instability is the inability to meet the reactive power demand and thus the solution lies on reactive power compensation. Modern wind turbine generators, equipped with full-scale

converters, are capable of supplying both active and reactive power to the grid and thus help to stabilize the grid voltage.

However, reactive power capabilities of individual wind turbine generators vary with available wind power and has certain limitations such as rated voltage and current of the converter. Therefore, individual turbines cannot supply the total reactive power demand all the time. This makes the conventional centralized reactive power compensation is inevitable even in modern wind farms, but at reduced capacity. Therefore, Chapter 7 has presented a novel centralized reactive power compensator topology for wind farms, its modulation and control.

Table 8.1 provides a summary on suitability of the converter topologies discussed in this thesis for different application requirements.

Table 8.1. Suitability of the inverter topologies for different application requirements

Application type	Low voltage	Medium voltage	Transformerless operation	Interface supercapacitor ESS	Interface battery ESS	Interface both battery and supercapacitor ESS	VAR support
Two- level inverter with a dc-dc converter	Yes	Need step-up transformer	No	Yes	Yes	No	Yes
Diode-clamped three-level inverter	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Capacitor-clamped three-level inverter	Yes	Yes	Yes	Yes	Yes	No	Yes
Cascaded 2x2 inverter system	Yes	Need step-up transformer	No	Yes	Yes	No	Yes
Cascaded 2x3 inverter system	Yes	Need step-up transformer	No	Yes	Yes	Yes	Yes
Cascaded 3x2 inverter system	Yes	Yes	No	Yes	Yes	No	Yes
Cascaded 3x3 inverter system	Yes	Yes	No	Yes	Yes	Yes	Yes
Hybrid cascaded inverter system	Yes	Yes	Yes	Yes	Yes	No	Yes
Modular matrix converter	Yes	Yes	Yes	No	No	No	No

8.2 Recommendations

Despite the fact that this thesis has covered a wide range of topics, like most other research topics, no firm ending can strictly be placed on the research on power converter systems for wind generation. A number of immediate topics that can be considered for future investigations are briefly summarized below.

1. The switch reduction in multilevel active rectifier systems presented in Chapter 2 has so far been developed only for three-level converters. It is possible to extend the same idea for higher level converters. Surely, that represents a good topic for future investigations. Furthermore, energy storage interfacing capability of higher level generator-side converters would be an interesting area to explore in future since they are gradually entering into the wind energy market.
2. Converter operation within the cut-in and rated wind speed range has been considered in this research. However, the transient operation of the converter at cut-in and rated wind speeds is a major problematic scenario which is an interesting topic for further research and development.
3. Direct integration schemes discussed so far have only used electrolytic capacitors to protect battery/supercapacitor energy storage systems from high frequency current pulses. Although this provides a reasonable low-pass filtering together with internal resistance and inductance of connection wires, properly designed filters would enhance the performance and reduce the capacity and size of filter capacitors. Undoubtedly, this work would push forward the concept of battery/supercapacitor direct integration into practice.
4. All the analysis and discussions presented in this thesis on battery and/or supercapacitor direct integration schemes are based on the steady state operation. The transient conditions at the start up and stop are yet to be explored. This is an important issue which should be addressed to make sure that the battery and/or supercapacitor operate(s) in a comfort zone throughout the operation.

5. The investigation on dual inverter topologies presented in Chapter 4 is limited to the combinations of two-level and three-level inverters. This study can be continued for the combinations of higher level converters as well. Furthermore, similar topologies could be adopted for the generator-side converter as well.
6. Although the concept and topologies proposed in this thesis for the direct integration of energy storage systems are validated through computer simulations and laboratory prototypes a detailed study has not yet been carried out targeting industrial application. This investigation is unarguably challenging since it is expected to promote the concept of direct integration of battery/supercapacitor energy storage systems and introduce a new dimension for low voltage ride through with the converter system.
7. The hybrid cascaded inverter system proposed in Chapter 5 is the simplest combination where the combinations of higher level inverters with H-bridge module are equally possible. These combinations would increase voltage and power ratings of the inverter and thus would be of interest in future wind energy conversion systems. Therefore, this can be recommended as a possible topic for future investigations.
8. Although the technical feasibility of inverter topologies and direct integration schemes proposed in the thesis have already been proven, their economical implementation issues have not yet been addressed to an appropriate extent that justifies their wide-spread application in wind energy conversion systems. Component selection, integration, packaging, efficiency measurements and electromagnetic interference quantification are the key areas to be explored in bringing proposed systems into practical implementation.

Author's publications

International Journal

Published

- [1] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "Cascade multilevel static synchronous compensator configuration for wind farms," *IET Trans. Power Electron.*, vol.4, no.5, pp.548-556, May 2011.
- [2] S.D.G. Jayasinghe, D.M. Vilathgamuwa, U.K. Madawala, "Direct Integration of Battery Energy Storage Systems in Distributed Power Generation," *IEEE Trans. Energy Convers.*, vol.26, no.2, pp.677-685, June 2011.
- [3] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "Diode-Clamped Three Level Inverter Based Battery/Supercapacitor Direct Integration Scheme for Renewable Energy Systems," *IEEE Trans. Power Electron.*, vol.26, no.12, pp.3720-3729, Dec. 2011.
- [4] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Dual Inverter Based Supercapacitor Direct Integration Scheme for Wind Energy Conversion Systems," in press, *IEEE Trans. Ind. Appl.*, 2012.
- [5] S.D.G. Jayasinghe and D.M. Vilathgamuwa, "Flying Supercapacitors as Power Smoothing Elements in Wind Generation," in press, *IEEE Trans. Ind. Electron.*, 2012.

International Conference

Published

- [1] D.M. Vilathgamuwa, S.D.G. Jayasinghe, and U.K. Madawala, "Space vector modulated cascade multi-level inverter for PMSG wind generation systems," in *Proc. Industrial Electronics Conference, IECON '09*, pp.4600-4605, 3-5 Nov. 2009.
- [2] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A cascade multilevel STATCOM for wind generation systems," in *Proc. Power Electronics and Drive Systems Conference, PEDS 2009*, pp.1323-1328, 2-5 Nov. 2009.
- [3] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Dual Inverter with Integrated Energy Storage for Wind Power Systems," in *Proc. IEEE International Power Electronics conference. IPEC-Sapporo 2010*, pp.3182-3187, 21-25 June 2010.
- [4] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Novel DC-Link Voltage Regulation Method for Single Source Hybrid Multilevel Inverters," in *Proc. IEEE Intl. Power Electron. Conf., IPEC-Sapporo 2010*, pp.740-745, 21-25 June 2010.
- [5] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "Grid Side Cascade Inverter System as an Interface for Wind Energy Storage," in *Proc. IEEE Energy Convers. Cong. and Expo, ECCE 2010, Atlanta Georgia*, pp.718-723, 12-16 Sept. 2010.
- [6] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Battery Energy Storage Interface for Wind Power Systems with the use of Grid Side Inverter," in *Proc IEEE Energy Convers. Cong. and Expo., ECCE 2010, Atlanta Georgia*, pp.3786-3791, 12-16 Sept. 2010.
- [7] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "Dual Inverter Based Battery Energy Storage System for Grid Connected Photovoltaic Systems," in *Proc. IEEE Ind. Electron. Conf., IECON '10, Phoenix, AZ, USA*, pp.3269-3274, 7-10 Nov. 2010.

- [8] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "Connecting Two Wind Turbine Generators to the Grid Using Only One Three Level NPC Inverter," in *Proc. IEEE Ind. Electron. Conf., IECON '10*, Phoenix, AZ, USA, pp.3257-3262, 7-10 Nov. 2010.
- [9] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A New Method of Interfacing Battery/Supercapacitor Energy Storage Systems for Distributed Energy Sources," in *Proc. IEEE International Power and Energy Conference, IPEC2010*, Singapore, pp.1211-1216, 27-29 Oct. 2010.
- [10] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Dual Inverter Based Supercapacitor Direct Integration Scheme for Wind Energy Conversion Systems," in *Proc. IEEE International Conference on Sustainable Energy Technologies, ICSET 2010*, Kandy, Sri Lanka, 6-9 Dec. 2010.
- [11] S.D.G. Jayasinghe, D.M. Vilathgamuwa and U.K. Madawala, "A Direct Integration Scheme for Battery-Supercapacitor Hybrid Energy Storage Systems," in *Proc. IEEE Applied Power Electron. Conf. & Expo., APEC 2011*, Texas, USA, pp.1388-1393, 6-10 Mar. 2011.
- [12] S.D.G. Jayasinghe, D.M. Vilathgamuwa, U.K. Madawala, "A hybrid cascaded multilevel inverter with supercapacitor direct integration for wind power systems," in *Proc. Intl. Conf. on Power Electron., ICPE 2011*, pp.638-645, May 30-June 3 2011.
- [13] S.D.G. Jayasinghe, D.M. Vilathgamuwa, U.K. Madawala, "An Analysis on the Possibility of Using Flying Capacitors of a Three-Level Capacitor Clamped Inverter as Power Smoothing Elements for Wind Power Systems," in *Proc. Energy Conversion Congress and Expo, ECCE 2011*, Phoenix, Arizona, USA, pp.2963-2970, Sept. 2010.
- [14] D.M. Vilathgamuwa, S.D.G. Jayasinghe, F.C. Lee, and U.K. Madawala, "A Unique Battery/Supercapacitor Direct Integration Scheme for Hybrid Electric Vehicles," in *Proc. IEEE Industrial Electronics Conference, IECON '11*, Melbourne, Australia, pp.3020-3025, Nov. 2011.
- [15] D.M. Vilathgamuwa, S.D.G. Jayasinghe and U.K. Madawala, "Battery Clamped Three-Level Inverter for Renewable Energy Systems," in *Proc. Industrial Electronics Conference, IECON '11*, Melbourne, Australia, pp.2988-2993, Nov. 2011.
- [16] D.M. Vilathgamuwa, X.N. Zhang, S.D.G. Jayasinghe, King Jet Tseng, B.S. Bhangu, and C. J. Gajanayake, "Virtual Resistance Based Active Damping Solution for Constant Power Load Instability in AC Microgrids," in *Proc. Industrial Electronics Conference, IECON '11*, Melbourne, Australia, pp.3521-3526, Nov. 2011.
- [17] S.D.G. Jayasinghe and D.M. Vilathgamuwa, "A Modular Matrix Converter for Transformer-less PMSG Wind Generation Systems," in *Proc. Power Electronics and Drive Systems Conference, PEDS 2011*, Singapore, pp.474-479, Dec. 2011.
- [18] S.D.G. Jayasinghe, and D.M. Vilathgamuwa, "A Three-Level Flying-Capacitor Rectifier Based Supercapacitor Direct Integration Scheme for Distributed Generation Systems," in *Proc. Intl. Sympo. on Ind. Electron., ISIE 2012*, China, pp.1566-1571, May 2012.
- [19] S.D.G. Jayasinghe, and D.M. Vilathgamuwa, "A Review on Rectifier Systems Suitable for PMSG Based Wind Energy Conversion Systems," in *Proc. Intl. Sympo. on Ind. Electron., ISIE 2012*, China, pp.1058-1065, May. 2012.

Bibliography

- [1] J. Esch, "Prolog to Keeping the Energy Debate Clean: How Do We Supply the World's Energy Needs?," *IEEE Proceedings*, vol.98, no.1, pp.39-41, Jan. 2010.
- [2] D. Abbott, "Keeping the Energy Debate Clean: How Do We Supply the World's Energy Needs?," *IEEE Proceedings*, vol.98, no.1, pp.42-66, Jan. 2010.
- [3] B. Bose, "Global Warming: Energy, Environmental Pollution, and the Impact of Power Electronics," *IEEE Mag. Ind. Electron.*, vol.4, no.1, pp.6-17, March 2010.
- [4] G. Spagnuolo, G. Petrone, S.V. Araujo, C. Cecati, E. Friis-Madsen, E. Gubia, D. Hissel, M. Jasinski, W. Knapp, M. Liserre, P. Rodriguez, R. Teodorescu, and P. Zacharias, "Renewable Energy Operation and Conversion Schemes: A Summary of Discussions During the Seminar on Renewable Energy Systems," *IEEE Mag. Ind. Electron.*, vol.4, no.1, pp.38-51, March 2010.
- [5] M. Liserre, J. Balcells, T. Basso, J.T. Bialasiewicz, C. Cecati, S. Chakraborty, J.M. Guerrero, M. Kazerani, F. Kupzog, A. Nasiri, P. Palensky, J. Rodriguez, P. Rodriguez, T. Sauter, and R. Teodorescu, "Guest Editorial," *IEEE Trans. Ind. Electron.*, vol.58, no.1, pp.2-8, Jan. 2011.
- [6] Xinghuo Yu, C. Cecati, T. Dillon, and M.G. Simões, "The New Frontier of Smart Grids," *IEEE Mag. Ind. Electron.*, vol.5, no.3, pp.49-63, Sept. 2011.
- [7] International Energy Agency. (2011). [Online]. Available: <http://www.iea.org>.
- [8] M. Liserre, T. Sauter, and J.Y. Hung, "Future Energy Systems: Integrating Renewable Energy Sources into the Smart Power Grid Through Industrial Electronics," *IEEE Mag. Ind. Electron.*, vol.4, no.1, pp.18-37, March 2010.
- [9] J.M. Guerrero, F. Blaabjerg, T. Zhelev, K. Hemmes, E. Monmasson, S. Jemei, M.P. Comech, R. Granadino, and J.I. Frau, "Distributed Generation: Toward a New Energy Paradigm," *IEEE Mag. Ind. Electron.*, vol.4, no.1, pp.52-64, March 2010.
- [10] EPRI Discussion Paper, "The power to reduce CO2 emissions—The full portfolio," EPRI Energy Technology Assessment Center, Aug. 2007.
- [11] H. Holttinen, A.G. Orths, P. Eriksen, J. Hidalgo, A. Estanqueiro, F. Groome, Y. Coughlan, H. Neumann, B. Lange, F. Hulle, and I. Dudurych, "Currents of Change," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.47-59, Nov.-Dec. 2011.
- [12] D. Osborn, M.I. Henderson, B.M. Nickell, W. Lasher, C. Liebold, J. Adams, and J. Caspary, "Driving Forces Behind Wind," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.60-74, Nov.-Dec. 2011.
- [13] Liping Jiang, Yongning Chi, Haiyan Qin, Zheyi Pei, Qionghui Li, Mingliang Liu, Jianhua Bai, Weisheng Wang, Shuanglei Feng, Weizheng Kong, and Qiankun Wang, "Wind Energy in China," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.36-46, Nov.-Dec. 2011.
- [14] M.G. Lauby, M. Ahlstrom, D.L. Brooks, S. Beuning, J. Caspary, W. Grant, B. Kirby, M. Milligan, M. O'Malley, M. Patel, R. Piwko, P. Pourbeik, D. Shirmohammadi, and J.C. Smith, "Balancing Act," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.75-85, Nov.-Dec. 2011.
- [15] M. Ahlstrom, J. Blatchford, M. Davis, J. Duchesne, D. Edelson, U. Focken, D. Lew, C. Loutan, D. Maggio, M. Marquis, M. McMullen, K. Parks, K. Schuyler, J. Sharp, and D. Souder, "Atmospheric Pressure," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.97-107, Nov.-Dec. 2011.

- [16] R. Zavadil, N. Miller, A. Ellis, E. Muljadi, P. Pourbeik, S. Saylor, R. Nelson, G. Irwin, M.S. Sahni, and D. Muthumuni, "Models for Change," *IEEE Mag. Power and Energy*, vol.9, no.6, pp.86-96, Nov.-Dec. 2011.
- [17] A.R. Ciupuliga, M. Gibescu, E. Pelgrum, P.G.H. Jacobs, K.P.J Jansen, and W.L. Kling, "Round-the-Year Security Analysis With Large-Scale Wind Power Integration," *IEEE Trans. Sustainable Energy*, vol.3, no.1, pp.85-93, Jan. 2012.
- [18] J.C. Smith, "Wind Power: Present Realities and Future Possibilities [Point of View]," *IEEE Proceedings*, vol.97, no.2, pp.195-197, Feb. 2009.
- [19] C.J. Mozina, "Wind-Power Generation," *IEEE Mag. Industry Appl.*, vol.17, no.3, pp.37-43, May-June 2011.
- [20] Yi Zhang, A.A. Chowdhury, and D.O. Koval, "Probabilistic Wind Energy Modeling in Electric Generation System Reliability Assessment," *IEEE Trans. Ind. Appl.*, vol.47, no.3, pp.1507-1514, May-June 2011.
- [21] Gilbert M. Masters, "Renewable and Efficient Electric Power Systems", *John Wiley & Sons, Inc.* 2004.
- [22] B. Wu, Y. Lang, N. Zargari, and S. Kouro, "Power Conversion and Control of Wind Energy Systems," *IEEE, John Wiley & Sons, Inc.* 2011.
- [23] F. Blaabjerg and Z. Chen, "Power Electronics for Modern Wind Turbines," *Morgan & Claypool Publishers*, 2006.
- [24] David Pimentel, "Biofuels, solar and wind as renewable energy systems: benefits and risks," *Springer*, 2008.
- [25] Tony Burton, David Sharpe, Nick Jenkins, Ervin Bossanyi, "Wind Energy Handbook," *John Wiley & Sons Ltd*, 2001.
- [26] L.H. Hansen, L. Helle, F. Blaabjerg, E. Ritchie, S. Munk-Nielsen, H. Bindner, P. Sørensen, and B. Bak-Jensen, "Conceptual survey of generators and power electronics for wind turbines," *Risø Nat. Lab., Roskilde, Denmark, Tech. Rep. Riso-R1205 (EN)*, Dec. 2001.
- [27] S.K. Hyong and D.D.C. Lu, "Review on wind turbine generators and power electronic converters with the grid-connection issues," in *Proc. IEEE Universities Power Engineering Conference, AUPEC 2010*, pp.1-6, 5-8 Dec. 2010.
- [28] M. Liserre, R. Cárdenas, M. Molinas, and J. Rodriguez, "Overview of Multi-MW Wind Turbines and Wind Parks," *IEEE Trans. Ind. Electron.*, vol.58, no.4, pp.1081-1095, April 2011.
- [29] Z. Chen, J.M. Guerrero, and F. Blaabjerg, "A Review of the State of the Art of Power Electronics for Wind Turbines," *IEEE Trans. Power Electron.*, vol.24, no.8, pp.1859-1875, Aug. 2009.
- [30] C. Abbey, and G. Joos, "Supercapacitor Energy Storage for Wind Energy Applications," *IEEE Trans. Ind. Appl.*, vol.43, no.3, pp.769-776, May-june 2007.
- [31] M.A. Alam, A.H. M.A. Rahim, and M.A. Abido, "Supercapacitor based energy storage system for effective fault ride through of wind generation system," in *Proc. IEEE Intl. Sympo. on Ind. Electron., ISIE 2010*, pp.2481-2486, 4-7 July 2010.
- [32] J.P. Da Costa, H. Pinheiro, T. Degner, and G. Arnold, "Robust Controller for DFIG of Grid Connected Wind Turbines," *IEEE Trans. Ind. Electron.*, vol.58, no.9, pp.4023-4038, Sept. 2011.
- [33] B. Bose, "GLOBAL ENERGY SCENARIO AND IMPACT OF POWER ELECTRONICS IN 21ST. CENTURY," in *Press IEEE Trans. Ind. Electron., Accessed June 2012*.
- [34] J.M. Carrasco, L.G. Franquelo, J.T. Bialasiewicz, E. Galvan, R.C.P. Guisado, Ma.A.M. Prats, J.I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid

- Integration of Renewable Energy Sources: A Survey,” *IEEE Trans. Ind. Electron.*, vol.53, no.4, pp.1002-1016, June 2006.
- [35] R.C. Portillo, M.M. Prats, J.I. Leon, J.A. Sanchez, J.M. Carrasco, E. Galvan, and L.G. Franquelo, “Modeling Strategy for Back-to-Back Three-Level Converters Applied to High-Power Wind Turbines,” *IEEE Trans. Ind. Electron.*, vol.53, no.5, pp.1483-1491, Oct. 2006.
- [36] J. Rodriguez, L. Jih-Sheng, and F.Z. Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp.724-738, Aug. 2002.
- [37] S. D. G. Jayasinghe, D. M. Vilathgamuwa, and U. K. Madawala, “Direct Integration of Battery Energy Storage Systems in Distributed Power Generation,” *IEEE Trans. Energy Convers.*, vol.26, no.2, pp.677-685, June 2011.
- [38] J. Driesen, and R. Belmans, “Distributed generation: Challenges and possible solutions,” in *Proc. IEEE Power Eng. Soc. General Meeting*, pp.1-8, Oct. 2006.
- [39] M. Black, and G. Strbac, “Value of bulk energy storage for managing wind power fluctuations,” *IEEE Trans. Energy Convers.*, vol.22, no.1, pp.197-205, Mar. 2007.
- [40] J.P. Barton, and D.G. Infield, “Energy storage and its use with intermittent renewable energy,” *IEEE Trans. Energy Convers.*, vol.19, no.2, pp.441-448, Jun. 2004.
- [41] P. Thounthong, and S. Rael, “The benefits of hybridization,” *IEEE Mag. Ind. Electron.*, vol.3, no.3, pp.25-37, Sept. 2009.
- [42] A.M. van Voorden, L.M.R. Elizondo, G.C. Paap, J. Verboomen, and L. van der Sluis, “The Application of Supercapacitors to relieve Battery-storage systems in Autonomous Renewable Energy Systems,” in *Proc. IEEE Power Tech 2007*, pp.479-484, 1-5 July 2007.
- [43] Z. Guoju, T. Xisheng, and Q. Zhiping, “Research on battery supercapacitor hybrid storage and its application in microgrid,” in *Proc. IEEE Asia-Pacific Power Energy Eng. Conf.*, pp.1-4, Mar. 2010.
- [44] Shuai Lu, K.A. Corzine, and M. Ferdowsi, “A New Battery/Ultracapacitor Energy Storage System Design and Its Motor Drive Integration for Hybrid Electric Vehicles,” *IEEE Trans. Veh. Technol.*, vol.56, no.4, pp.1516-1523, July 2007.
- [45] J. Cao, and A. Emadi, “A New Battery/UltraCapacitor Hybrid Energy Storage System for Electric, Hybrid, and Plug-In Hybrid Electric Vehicles,” *IEEE Trans. Power Electron.*, vol.27, no.1, pp.122-132, Jan. 2012.
- [46] A. Arulampalam, M. Barnes, N. Jenkins, and J.B. Ekanayake, “Power quality and stability improvement of a wind farm using STATCOM supported with hybrid battery energy storage,” *IEE Proceedings Generation, Transmission and Distribution*, vol.153, no.6, pp.701-710, November 2006.
- [47] B. Ronner, P. Maibach, and T. Thurnherr, “Operational experiences of STATCOMs for wind parks,” *IET Trans. Renewable Power Generation*, vol.3, no.3, pp.349-357, Sept. 2009.
- [48] Wei Qiao, R.G. Harley, and G.K. Venayagamoorthy, “Effects of FACTS Devices on a Power System Which Includes a Large Wind farm,” in *Proc. IEEE Power Systems Conf. and Exposition*, pp. 2070 – 2076, Nov. 2006.
- [49] Chong Han, A.Q. Huang, M.E. Baran, S. Bhattacharya, W. Litzenberger, L. Anderson, A.L. Johnson, and A.A. Edris, “STATCOM Impact Study on the Integration of a Large Wind Farm into a Weak Loop Power System,” *IEEE Trans. Energy Convers.*, vol.23, no.1, pp. 226 – 233, March 2008.
- [50] Z. Saad-Saoud, M.L. Lisboa, J.B. Ekanayake, N. Jenkins, and G. Strbac, “Application of STATCOMs to wind farms,” *IEE Proceedings Generation, Transmission and Distribution*, vol.145, no.5, pp. 511-516, Sept. 1998.
-

-
- [51] Wikipedia Encyclopedia [Online] (2012). Available: http://en.wikipedia.org/wiki/Atmospheric_circulation.
 - [52] M.G. Molina, and P.E. Mercado, "A new control strategy of variable speed wind turbine generator for three-phase grid-connected applications," in *Proc. IEEE Transmission and Distribution Conf. and Expo., PES 2008*, pp.1-8, Aug. 2008.
 - [53] T.H. Nguyen, J. Suk-Ho Jang, P. Hong-Geuk and L. Dong-Choon, "Sensorless control of PM synchronous generators for micro wind turbines," in *Proc. IEEE Power and Energy Conference, PECon 2008*, pp.936-941, Dec. 2008.
 - [54] T. Senjyu, N. Nakasone, A. Yona, A.Y. Saber, T. Funabashi, and H. Sekine, "Operation strategies for stability of gearless wind power generation systems," in *Proc. IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, pp.1-7, 20-24 July 2008.
 - [55] D.M. Vilathgamuwa, S.D.G. Jayasinghe, F.C. Lee, and U.K. Madawala, "A unique battery/supercapacitor direct integration scheme for hybrid electric vehicles," in *Proc. IEEE Industrial Electronics Society Conf., IECON 2011*, pp.3020-3025, Nov. 2011.
 - [56] J.W. Kolar, and T. Friedli, "The essence of three-phase PFC rectifier systems," in *Proc. IEEE Intl. Telecom. Energy Conf., INTELEC 2011*, pp.1-27, 9-13 Oct. 2011.
 - [57] Z. Chen, and E. Spooner, "Voltage source inverters for high-power, variable-voltage DC power sources," *IEE Proceedings Generation, Transmission and Distribution*, vol.148, no.5, pp.439-447, Sep 2001.
 - [58] K. Nishida, T. Ahmed, and M. Nakaoka, "Development of grid-connected wind energy system employing interior PM Synchronous Generator and multi-pulse rectifier," in *Proc. IEEE Energy Convers. Cong. and Expo., ECCE 2010*, pp.3374-3381, Sept. 2010.
 - [59] Li Jianlin, H. Shuju, and X. Honghua, "A kind of direct-driven WECS using single-switch three-phase Boost rectifier," in *Proc. IEEE Intl. Conf. on Ind. Techno., ICIT 2008*, pp.1-6, 21-24 April 2008.
 - [60] B. Wu, Y. Li, and S. Wei, "Multipulse diode rectifiers for high-power multilevel inverter fed drives," in *Proc. IEEE Intl. Power Electron. Cong., CIEP 2004*, pp.9-14, 17-22 Oct. 2004.
 - [61] Bin Wu, "High-Power Converters and ac Drives," *The Institute of Electrical and Electronics Engineers, Inc*, 2006.
 - [62] H. Ertl, and J.W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "Electronic Smoothing Inductor"," *IEEE Trans. Ind. Electron.*, vol.52, no.2, pp.454-461, April 2005.
 - [63] J.W. Kolar, T. Friedli, and M. Hartmann, "Three-phase PFC rectifier and ac-ac converter systems – Part I, Tutorial," *Presented at IEEE Applied Power Electronics Conference and Exposition, APEC '11*, 6-10 Mar. 2011.
 - [64] L. Wei, C. Abbey, and G. Joos, "Control and Performance of Wind Turbine Generators based on Permanent Magnet Synchronous Machines Feeding a Diode Rectifier," in *Proc. IEEE Power Electron. Spec. Conf., PESC '06*, pp.1-6, 18-22 June 2006.
 - [65] T. Takaku, G. Homma, T. Isober, S. Igarashi, Y. Uchida, and R. Shimada, "Improved wind power conversion system using magnetic energy recovery switch (MERS)," in *Proc. IEEE Industry Applications Conference*, vol.3, pp. 2007- 2012, Oct. 2005.
 - [66] R. Shimada, J.A. Wiik, T. Isobe, T. Takaku, N. Iwamuro, Y. Uchida, M. Molinas, and T.M. Undeland, "A New AC Current Switch Called MERS with Low On-State Voltage IGBTs (1.54V) for Renewable Energy and Power Saving Applications," in *Proc. Intl. Sympo. on Power Semiconductor Devices and IC's, ISPSD '08*, pp.4-11, May 2008.
 - [67] J.A. Wiik, A. Kulka, T. Isobe, K. Usuki, M. Molinas, T. Takaku, T.M. Undeland, and R. Shimada, "Loss and Rating Considerations of a Wind Energy Conversion System with Reactive Compensation by Magnetic Energy Recovery Switch (MERS)," in *Proc.*
-

- EPE Wind Energy Chapter 1st Seminar-Wind Power to the Grid, EPE-WECS 2008*, pp.1-6, 27-28 March 2008.
- [68] J.A. Wiik, O.J. Fonstelien, and R. Shimada, "A MERS type series FACTS controller for low voltage ride through of induction generators in wind farms," in *Proc. European Conference on Power Electronics and Applications, EPE '09*, pp.1-10, 8-10 Sept. 2009.
- [69] Z. Shao, T. King-Jet, D.M. Vilathgamuwa, T.D. Nguyen, and W. Xiao-Yu, "Design of a Robust Grid Interface System for PMSG-Based Wind Turbine Generators," *IEEE Trans. Ind. Electron.*, vol.58, no.1, pp.316-328, Jan. 2011.
- [70] J. Yinan, U.K. Madawala, R. Sharma, and D.M. Vilathgamuwa, "A wind generator system with an integrated boost converter," in *Proc. IEEE Intl. Conf. on Sustainable Energy Technologies, ICSET 2010*, pp.1-6, 6-9 Dec. 2010.
- [71] J.W. Kolar, H. Ertl, and F.C. Zach, "Space vector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," *IEEE Trans. Power Electron.*, vol.10, no.6, pp.733-745, Nov 1995.
- [72] D. Krahenbuhl, C. Zwyssig, K. Bitterli, M. Imhof, and J.W. Kolar, "Evaluation of ultra-compact rectifiers for low power, high-speed, permanent-magnet generators," in *Proc. IEEE Industrial Electronics Conference, IECON 2009*, pp.448-455, 3-5 Nov. 2009.
- [73] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "A dual inverter based supercapacitor direct integration scheme for wind energy conversion systems," in *Proc. IEEE Intl. Conf. on Sustainable Energy Techno., ICSET 2010*, pp.1-6, 6-9 Dec. 2010.
- [74] D. Panda, and T.A. Lipo, "A half-power rating improved 3-phase six-switch boost rectifier using two half controlled configurations with a common DC bus," in *Proc. IEEE Power Electron. Spec. Conf., PESC '03*, vol.3, pp.1069-1074, 15-19 June 2003.
- [75] J. Kikuchi, M.D. Manjrekar, and T.A. Lipo, "Performance improvement of half controlled three phase PWM boost rectifier," in *Proc. IEEE Power Electron. Spec. Conf., PESC 99*, vol.1, pp.319-324, Aug 1999.
- [76] S.K.T Miller, and J. Sun, "Comparative study of three-phase PWM rectifiers for wind energy conversion," in *Proc. IEEE Applied Power Electronics Conference and Exposition, APEC '06*, pp.1-7, 19-23 March 2006.
- [77] Y. Fengying C. Fengcai, E. Wang, L. Yonghong, and X. Zhiyong, "Control system of wind power grid PWM rectifier based on DSP," in *Proc. International Conference on Computer Application and System Modeling, ICCASM 2010*, vol.13, pp.V13-530-V13-533, 22-24 Oct. 2010.
- [78] J.R. Rodriguez, J.W. Dixon, J.R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: state of the art," *IEEE Trans. Ind. Electron.*, vol.52, no.1, pp. 5- 22, Feb. 2005.
- [79] J.S. Thongam, P. Bouchard, R. Beguenane, A.F. Okou, and A. Merabet, "Control of variable speed wind energy conversion system using a wind speed sensorless optimum speed MPPT control method," in *Proc. IEEE Industrial Electronics Society Conf., IECON 2011*, pp.855-860, 7-10 Nov. 2011.
- [80] A. Yazdani, and R. Iravani, "A neutral-point clamped converter system for direct-drive variable-speed wind power unit," *IEEE Trans. Energy Convers.*, vol.21, no.2, pp.596-607, June 2006.
- [81] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "Diode-Clamped Three-Level Inverter-Based Battery/Supercapacitor Direct Integration Scheme for Renewable Energy Systems," *IEEE Trans. Power Electron.*, vol.26, no.12, pp.3720-3729, Dec. 2011.
- [82] K.A. Corzine, and J.R. Baker, "Reduced-parts-count multilevel rectifiers," *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp.766-774, Aug. 2002.
-

- [83] M.L. Heldwein, S.A. Mussa, and I. Barbi, "Three-Phase Multilevel PWM Rectifiers Based on Conventional Bidirectional Converters," *IEEE Trans. Power Electron.*, vol.25, no.3, pp.545-549, March 2010.
- [84] T.A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.
- [85] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "An analysis on the possibility of using capacitors of a three-level capacitor clamped inverter as power smoothing elements for wind power systems," in *Proc. IEEE Energy Conversion Congress and Exposition, ECCE 2011*, pp.2963-2970, 17-22 Sept. 2011.
- [86] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Trans. Ind. Electron.*, vol.57, no.8, pp.2581-2596, Aug. 2010.
- [87] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M.A. Pérez, and J.I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol.57, no.8, pp.2553-2580, Aug. 2010.
- [88] J. Rodriguez, S. Bernet, P.K. Steimer, and L.E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol.57, no.7, pp.2219-2230, July 2010.
- [89] A.A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-Filter Design for a Multimegawatt Medium-Voltage Voltage-Source Inverter," *IEEE Trans. Ind. Electron.*, vol.58, no.4, pp.1205-1217, April 2011.
- [90] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol.57, no.7, pp.2197-2206, July 2010.
- [91] F. Defay, A.M. Llor, and M. Fadel, "Direct Control Strategy for a Four-Level Three-Phase Flying-Capacitor Inverter," *IEEE Trans. Ind. Electron.*, vol.57, no.7, pp.2240-2248, July 2010.
- [92] G. Waltrich, and I. Barbi, "Three-Phase Cascaded Multilevel Inverter Using Power Cells With Two Inverter Legs in Series," *IEEE Trans. Ind. Electron.*, vol.57, no.8, pp.2605-2612, Aug. 2010.
- [93] D.M. Vilathgamuwa, S.D.G. Jayasinghe, and U.K. Madawala, "Space vector modulated cascade multi-level inverter for PMSG wind generation systems," in *Proc. IEEE Industrial Electronics Conf., IECON 2009*, pp.4600-4605, 3-5 Nov. 2009.
- [94] G.R. Mohapatra, and A. Kalam, "Dynamic stability analysis of renewable energy sources interconnected to the distribution networks," in *Proc. Power Eng. Conf., AUPEC 2008*, pp.1-4, 14-17 Dec. 2008.
- [95] P.F. Ribeiro, B.K. Johnson, M.L. Crow, A. Arsoy, and Y. Liu, "Energy storage systems for advanced power applications," *IEEE Proceedings*, vol.89, no.12, pp.1744-1756, Dec. 2001.
- [96] Wei Li, and G. Joos, "A power electronic interface for a battery supercapacitor hybrid energy storage system for wind applications," in *Proc. IEEE Power Electron. Spec. Conf., PESC 2008*, pp.1762-1768, 15-19 June 2008.
- [97] S.M. Mueen, R. Takahashi, T. Murata, and J. Tamura, "Integration of an Energy Capacitor System With a Variable-Speed Wind Generator," *IEEE Trans. Energy Convers.*, vol.24, no.3, pp.740-749, Sep. 2009.
- [98] M. Bragard, N. Soltau, S. Thomas, and R.W. De Doncker, "The Balance of Renewable Sources and User Demands in Grids: Power Electronics for Modular Battery Energy Storage Systems," *IEEE Trans Power Electron.*, vol.25, no.12, pp.3049-3056, Dec. 2010.

- [99] A.L. Allegre, A. Bouscayrol, and R. Trigui, "Influence of control strategies on battery/supercapacitor hybrid Energy Storage Systems for traction applications," in *Proc. IEEE Vehicle Power and Propulsion Conf., VPPC 2009*, pp.213-220, Sept. 2009.
- [100] Jin Ke, Yang Mengxiong, Ruan Xinbo, and Xu Min, "Three-Level Bidirectional Converter for Fuel-Cell/Battery Hybrid Power System," *IEEE Trans. Ind. Electron.*, vol.57, no.6, pp.1976-1986, June 2010.
- [101] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibaez, and J.L. Villate, "A Comprehensive Study of a Hybrid Modulation Technique for the Neutral-Point-Clamped Converter," *IEEE Trans. Ind. Electron.*, vol.56, no.2, pp.294-304, Feb. 2009.
- [102] O. Alonso, L. Marroyo, P. Sanchis, E. Gubia, and A. Guerrero, "Analysis of neutral-point voltage balancing problem in three-level neutral-point-clamped inverters with SVPWM modulation," in *Proc. IEEE Ind. Electron. Conf., IECON 2002*, vol.2, pp. 920-925, Nov. 2002.
- [103] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol.49, no.5, pp.1026-1034, Oct. 2002.
- [104] J.H. Seo, and C.H. Choi, "Compensation for the neutral-point potential variation in three-level space vector PWM," in *Proc. IEEE Applied Power Electronics Conference and Exposition, APEC 2001*, vol.2, pp.1135-1140, Mar. 2001.
- [105] M. Galvez, E. Bueno, F.J. Rodriguez, F.J. Meca, and F.J. Rodriguez, "New MPPT algorithm for photovoltaic systems connected to NPC converters and optimized for large variations of solar radiation," in *Proc. IEEE Energy Conversion Congress and Exposition, ECCE 2009*, pp.48-53, 20-24 Sept. 2009.
- [106] Wei-dong Jiang, Shao-wu Du, Liu-chen Chang, Yi Zhang, and Qin Zhao, "Hybrid PWM Strategy of SVPWM and VSVPWM for NPC Three-Level Voltage-Source Inverter," *IEEE Trans. Power Electron.*, vol.25, no.10, pp.2607-2619, Oct. 2010.
- [107] H. Akagi, and R. Kondo, "A Transformerless Hybrid Active Filter Using a Three-Level Pulsewidth Modulation (PWM) Converter for a Medium-Voltage Motor Drive," *IEEE Trans. Power Electron.*, vol.25, no.6, pp.1365-1374, June 2010.
- [108] O. Vodyakho, and C.C. Mi, "Three-Level Inverter-Based Shunt Active Power Filter in Three-Phase Three-Wire and Four-Wire Systems," *IEEE Trans. Power Electron.*, vol.24, no.5, pp.1350-1363, May 2009.
- [109] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of n -Level Three-Leg Diode-Clamped Converters," *IEEE Trans. Power Electron.*, vol.24, no.5, pp.1364-1375, May 2009.
- [110] H. Akagi, and T. Hatada, "Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium-Voltage Transformerless Hybrid Active Filter," *IEEE Trans. Power Electron.*, vol.24, no.3, pp.571-579, March 2009.
- [111] C. Nikola, "Space vector modulation and control of multilevel converters," Ph.D. Thesis, Virginia Polytechnic Institute, Sep. 2000.
- [112] D. Peng, F.C. Lee, and D. Boroyevich, "A novel SVM algorithm for multilevel three-phase converters," in *Proc. IEEE Power Electron. Spec. Conf.*, vol. 2, pp. 509-513, June 2002.
- [113] S. Cheng, Y. Liu, and B. Wu, "SVM algorithm of three-level NPC inverter," in *Proc. IEEE Industrial Electronics and Applications, ICIEA 2008*, pp.2194-2198, June 2008.
- [114] M. Saeedifard, H. Nikkhajoei, and R. Iravani, "A Space Vector Modulated STATCOM Based on a Three-Level Neutral Point Clamped Converter," *IEEE Trans. Power Delivery*, vol.22, no.2, pp.1029-1039, April 2007.

- [115] M.H. Rashid, "Power electronics handbook. devices, circuits, and applications," Elsevier, 2011.
- [116] J.S. Lai and F.Z. Peng, "Multilevel converters – a new breed of power converters," *IEEE Trans. Industry Applications*, vol.32, pp.509-517, May/June 1996.
- [117] F.Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Industry Applications*, vol.37, no.2, pp.611-618, Mar/Apr. 2001.
- [118] J. Huang, and K.A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol.21, no.1, pp.140-147, Jan. 2006.
- [119] T.H. Nguyen, D.C. Lee, S. Seung-Ho, and E.H. Kim, "Improvement of power quality for PMSG wind turbine systems," in *Proc. IEEE Energy Conversion Congress and Exposition, ECCE 2010*, pp.2763-2770, 12-16 Sept. 2010.
- [120] W. Lajnef, J.M. Vinassa, O. Briat, S. Azzopardi, and C. Zardini, "Study of ultracapacitors dynamic behaviour using impedance frequency analysis on a specific test bench," in *Proc. IEEE Intl. Sympo. on Ind. Electron.*, vol.2, pp.839-844, May 2004.
- [121] L. Zhang, and S.J. Watkins, "Capacitor voltage balancing in multilevel flying capacitor inverters by rule-based switching pattern selection," *IET Trans. Electric Power Appl.*, vol.1, no.3, pp.339-347, May 2007.
- [122] K. Dae-Wook, L. Byoung-Kuk, J.H. Jeon, T.J. Kim, and D.S. Hyun, "A symmetric carrier technique of CRPWM for voltage balance method of flying-capacitor multilevel inverter," *IEEE Trans. Ind. Electron.*, vol.52, no.3, pp.879-888, June 2005.
- [123] B.R. Lin, and Chun-Hao Huang, "Implementation of a Three-Phase Capacitor-Clamped Active Power Filter Under Unbalanced Condition," *IEEE Trans. Ind. Electron.*, vol.53, no.5, pp.1621-1630, Oct. 2006.
- [124] Gui-Jia Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol.41, no.3, pp.848-854, May-June 2005.
- [125] K. Xiaomin, K.A. Corzine, and Y.L. Familant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.* vol.19, no.4, pp. 979- 987, July 2004.
- [126] D.W. Kang, W.K. Lee, and D.S. Hyun, "Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter," *IEE Trans. Electric Power Appl.*, vol.151, no.2, pp. 239- 248, Mar 2004.
- [127] Li Wei, and G. Joos, "Comparison of Energy Storage System Technologies and Configurations in a Wind Farm," in *Proc. IEEE Power Electronics Specialists Conference*, pp.1280-1285, June 2007.
- [128] A. Etxeberria, I. Vechiu, H. Camblong, and J.M. Vinassa, "Comparison of three topologies and controls of a hybrid energy storage system for Microgrids," *Elsevier, Energy Conversion and Management*, Vol.54, no.1, pp.113-121, Feb. 2012.
- [129] M. Singh, and A. Chandra, "Control of PMSG based variable speed wind-battery hybrid system in an isolated network," in *Proc. IEEE Power & Energy Soc. General Meeting*, pp.1-6, 26-30 July 2009.
- [130] D. Casadei, G. Grandi, A. Lega, and C. Rossi, "Multilevel Operation and Input Power Balancing for a Dual Two-Level Inverter with Insulated DC Sources," *IEEE Trans. Industry Appl.*, vol.44, no.6, pp.1815-1824, Nov./Dec. 2008.
- [131] G. Grandi, C. Rossi, D. Ostojic, and D. Casadei, "A New Multilevel Conversion Structure for Grid-Connected PV Applications," *IEEE Trans. Ind. Electron.*, vol.56, no.11, pp.4416-4426, Nov. 2009.
- [132] G. Grandi, C. Rossi, A. Lega, and D. Casadei, "Multilevel operation of a dual two-level inverter with power balancing capability," in *Proc. IEEE IAS Annual Meeting*, pp.603-610, 8-12 Oct. 2006.

- [133] G. Grandi, C. Rossi, A. Lega, D. Casadei, "Power balancing of a multilevel converter with two insulated supplies for three-phase six-wire loads," in *Proc. IEEE European Conf. on Power Electron. and Appl.*, pp.1-10, Sept. 2005.
- [134] K.A. Corzine, A.S. Sudhoff, and C. Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. Energy Conversion*, vol.14, no.3, pp.433-439, Sept. 1999.
- [135] M. Baiju, K. Mohapatra, R. Kanchan, and K. Gopakumar, "A dual two level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol.19, no.3, pp.794-805, May 2004.
- [136] M.R. Baiju, K.K. Mohapatra, and K. Gopakumar, "PWM signal generation for dual inverter fed open-end winding induction motor drive using only the instantaneous reference phase amplitudes" in *Proc. IEEE Intl. Joint Conf. SICE-ICASE*, pp.672-677, 2006.
- [137] E.G. Shivakumar, K. Gopakumar, S.K. Sinha, A. Pittet, and V.T. Ranganathan, "Space vector PWM control of dual inverter fed open end winding induction motor drive," in *Proc. IEEE Appl. Power Electron. Conf.*, pp.399-405, March. 2001.
- [138] E.G. Shivakumar, K. Gopakumar, and V.T. Ranganathan, "Space vector PWM control of dual inverter fed open-end winding induction motor drive," *EPE Journal*, vol.12, no.1, pp.9-18, Feb. 2002.
- [139] G. Grandi, and D. Ostojic, "Dual inverter space vector modulation with power balancing capability," in *Proc. IEEE Conf. EUROCON '09*, pp.721-728, 18-23 May 2009.
- [140] B. Welchko, "A double-ended inverter system for the combined propulsion and energy management functions in hybrid vehicles with energy storage," in *Proc. IEEE Ind. Electron. Soc. Conf., IECON 2005*, pp.1401-1406, Nov. 2005.
- [141] J. Kim, J. Jung, and K. Nam, "Dual-inverter control strategy for high-speed operation of EV induction motors," *IEEE Trans. Ind. Electron.*, vol.51, no.2, pp.312-320, April 2004.
- [142] Y. Kawabata, M. Nasu, T. Nomoto, E. C. Ejiogu, and T. Kawabata, "High-efficiency and low acoustic noise drive system using open-winding AC motor and two space-vector-modulated inverters," *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp.783-789, Aug. 2002.
- [143] K.A. Corzine, W. Wielebsk, F.Z. Peng, and J. Wang, "Control of cascaded multilevel inverters," *IEEE Trans. Power Electron*, vol.19, no.3, pp.732-738, May 2004.
- [144] S. Lu, and K.A. Corzine, "Advanced Control and Analysis of Cascaded Multilevel Converters Based on P-Q Compensation," *IEEE Trans. Power Electron.*, vol.22, no.4, pp.1242-1252, July 2007.
- [145] S. Lu, K.A. Corzine, and M. Ferdowsi, "A Unique Ultracapacitor Direct Integration Scheme in Multilevel Motor Drives for Large Vehicle Propulsion," *IEEE Trans. Veh. Tech.*, vol.56, no.4, pp.1506-1515, July 2007.
- [146] K.A. Corzine, and J.R. Baker, "Multilevel voltage-source duty-cycle modulation: Analysis and implementation," *IEEE Trans. Ind. Electron.*, vol.49, no.5, pp.1009-1016, Oct. 2002.
- [147] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "Cascade multilevel static synchronous compensator configuration for wind farms," *IET Trans. Power Electron.*, vol.4, no.5, pp.548-556, May 2011.
- [148] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-Vector Pulse Width Modulation for Three-Level NPC Converter with the Neutral Point Voltage Control," *IEEE Trans. Ind. Electron.*, vol.58, no.11, pp.5076-5086, Nov. 2011.

- [149] J.I. Leon, S. Vazquez, R. Portillo, L.G. Franquelo, J.M. Carrasco, P.W. Wheeler, and A.J. Watson, "Three-Dimensional Feedforward Space Vector Modulation Applied to Multilevel Diode-Clamped Converters," *IEEE Trans. Ind. Electron.*, vol.56, no.1, pp.101-109, Jan. 2009.
- [150] T. Zhou, and B. Francois, "Energy Management and Power Control of a Hybrid Active Wind Generator for Distributed Power Generation and Grid Integration," *IEEE Trans. Ind. Electron.*, vol.58, no.1, pp.95-104, Jan. 2011.
- [151] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "A new method of interfacing battery/supercapacitor energy storage systems for distributed energy sources," in *Proc. IEEE Intl. Power and Energy Conf., IPEC 2010*, pp.1211-1216, 27-29 Oct. 2010.
- [152] F. Khoucha, M.S. Lagoun, A. Kheloui, and M.E.H. Benbouzid, "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives," *IEEE Trans. Energy Convers.*, vol.26, no.1, pp.64-72, Mar. 2011.
- [153] J. Pereda, and J. Dixon, "High-Frequency Link: A Solution for Using Only One DC Source in Asymmetric Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol.58, no.9, pp.3884-3892, Sept. 2011.
- [154] S. Vazquez, J.I. Leon, L.G. Franquelo, J.J. Padilla, and J.M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source," *IEEE Trans. Ind. Electron.*, vol.56, no.7, pp.2513-2521, Jul. 2009.
- [155] Z. Du, L.M. Tolbert, J.N. Chiasson, and B. Ozpineci, "A cascade multilevel inverter using a single DC source," in *Proc. IEEE Applied Power Electronics Conf. and Expo., APEC 2006*, pp.426-430, 19-23 Mar. 2006.
- [156] J.N. Chiasson, B. Ozpineci, and L.M. Tolbert, "A five-level three-phase hybrid cascade multilevel inverter using a single DC source for a PM synchronous motor drive," in *Proc. IEEE Applied Power Electronics Conf. and Expo., APEC 2007*, pp.1504-1507, Feb. 25-Mar. 1 2007.
- [157] Z. Du, L.M. Tolbert, J.N. Chiasson, B. Ozpineci, H.Li, and A.Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," in *Proc. IEEE Power Electronics Specialists Conference, PESC 2006*, pp.1-6, 18-22 June 2006.
- [158] H. Li, K. Wang, D. Zhang, and W. Ren, "Improved performance and control of hybrid cascaded H-bridge inverter for utility interactive renewable energy applications," in *Proc. IEEE Power Electronics Specialists Conference, PESC 2007*, pp.2465-2471, 17-21 June 2007.
- [159] S. Khomfoi, and C. Aimsaard, "A 5-level cascaded hybrid multilevel inverter for interfacing with renewable energy resources," in *Proc. IEEE Intl. Conf. on Elect. Eng./Electron., Computer, Telecom. and Info. Tech., ECTI-CON 2009*, pp.284-287, 6-9 May 2009.
- [160] S. Khomfoi, N. Praisuwanna, and L.M. Tolbert, "A hybrid cascaded multilevel inverter application for renewable energy resources including a reconfiguration technique," in *Proc. IEEE Energy Convers. Cong. and Expo., ECCE 2010*, pp.3998-4005, Sept. 2010.
- [161] N. Praisuwanna, and S. Khomfoi, "A hybrid cascaded multilevel inverter," in *Proc. IEEE Intl. Conf. on Elect. Eng./Electron., Computer, Telecom. and Info. Tech., ECTI-CON 2010*, pp.1041-1044, May 2010.
- [162] H. Sepahvand, M. Ferdowsi, and K.A. Corzine, "A seven-level converter using a combination of staircase and PWM switching methods," in *Proc. IEEE Ind. Electron. Conf., IECON 2010*, pp.2307-2310, 7-10 Nov. 2010.
- [163] H. Liu, L.M. Tolbert, B. Ozpineci, and Zhong Du, "Comparison of fundamental frequency and PWM methods applied on a hybrid cascaded multilevel inverter," in *Proc. IEEE Ind. Electron. Conf., IECON 2008*, pp.3233-3237, 10-13 Nov. 2008.

- [164] Haiwen Liu, L.M. Tolbert, S. Khomfoi, B. Ozpineci, and Zhong Du, "Hybrid cascaded multilevel inverter with PWM control method," in *Proc. IEEE Power Electron. Specialists Conf., PESC 2008*, pp.162-166, 15-19 June 2008.
- [165] B. Venugopal Reddy, V. Somasekhar, and K. Yenduri, "Decoupled Space-vector PWM Strategies for a Four-level Asymmetrical Open-end Winding Induction Motor Drive with Waveform Symmetries," *IEEE Trans. Ind. Electron.*, vol.58, no.11, pp.5130-5140, Nov. 2011.
- [166] A.L. Batschauer, S.A. Mussa, and M.L. Heldwein, "Three-Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules," *IEEE Trans. Ind. Electron.*, vol.59, no.2, pp.668-678, Feb. 2012.
- [167] S. Khomfoi, and N. Praisuwana, "A hybrid cascaded multilevel inverter for interfacing with renewable energy resources," in *Proc. IEEE Intl. Power Electron. Conf. IPEC 2010*, pp.2912-2917, 21-24 June 2010.
- [168] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "A Dual Inverter with Integrated Energy Storage for Wind Power Systems," in *Proc. IEEE Intl. Power Electron. Conf., IPEC-Sapporo 2010*, pp.3182-3187, 21-25 June. 2010.
- [169] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "Grid Side Cascade Inverter System as an Interface for Wind Energy Storage," in *Proc. IEEE Energy Conversion Congress and Expo., ECCE 2010*, pp.718-723, 12-16 Sept. 2010.
- [170] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "A Battery Energy Storage Interface for Wind Power Systems with the use of Grid Side Inverter," in *Proc. IEEE Energy Conversion Congress and Expo., ECCE 2010*, pp.3786-3791, Sept. 2010.
- [171] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, "Connecting Two Wind Turbine Generators to the Grid Using Only One Three Level NPC Inverter," in *Proc. IEEE Industrial Electronics Conf., IECON 2010*, pp.3257-3262, 7-10 Nov. 2010.
- [172] C.H. Ng, M.A. Parker, Li Ran, P.J. Tavner, J.R. Bumby and E. Spooner, "A Multilevel Modular Converter for a Large, Light Weight Wind Turbine Generator," *IEEE Trans. Power Electron.*, vol.23, no.3, pp.1062-1074, May 2008.
- [173] P. Samuel, R. Gupta and D. Chandra, "Grid Interface of Wind Power With Large Split-Winding Alternator Using Cascaded Multilevel Inverter," *IEEE Trans. Energy Convers.*, vol.26, no.1, pp.299-309, March 2011.
- [174] Y. Xibo, L. Yongdong, C. Jianyun and M. Minzheng, "A modular direct-drive permanent magnet wind generator system eliminating the grid-side transformer," in *Proc. European power Electron. and Appl. Conf., EPE '09.*, pp.1-7, 8-10 Sept. 2009.
- [175] Jun Kang, E. Yamamoto, M. Ikeda and E. Watanabe, "Medium-Voltage Matrix Converter Design Using Cascaded Single-Phase Power Cell Modules," *IEEE Trans. Ind. Electron.*, vol.58, no.11, pp.5007-5013, Nov. 2011.
- [176] J. Wang, B. Wu, D. Xu and N.R. Zargari, "Multimodular Matrix Converters With Sinusoidal Input and Output Waveforms," *IEEE Trans. Ind. Electron.*, vol.59, no.1, pp.17-26, Jan. 2012.
- [177] Y. Miura, S. Horie, S. Kokubo, T. Amano, T. Ise, T. Momose, and Y. Sato, "Application of three-phase to single-phase matrix converter to gas engine cogeneration system," in *Proc. IEEE Energy Conversion Congress and Expo., ECCE 2009*. pp.3290-3297, 20-24 Sept. 2009.
- [178] M. Tsili, and S. Papathanassiou, "A review of grid code technical requirements for wind farms," *IET Renewable Power Generation*, vol.3, no.3, pp.308-332, Sept. 2009.
- [179] R. Zavadil, N. Miller, A. Ellis, and E. Muljadi, "Making connections [wind generation facilities]," *IEEE Mag. Power and Energy*, vol.3, no.6, pp.26-37, Nov.-Dec. 2005.
- [180] M.D.I. Alegria, J. Andreu, J.L. Martin, P. Ibinez, J.L. Village, and H. Camblong, "Connection requirements for wind farms: a survey on technical requirements and

- regulation,” *Renewable and Sustainable Energy Review*, Vol.11, no.8, pp.1858-1872, Oct. 2007.
- [181] H.T. Jadhav, and R. Roy, “A critical review on the grid integration issues of DFIG based wind farms,” in *Proc. International Conference on Environment and Electrical Engineering, IEEEIC 2011*, pp.1-4, 8-11 May 2011.
- [182] S. Sayeef, N. Mendis, K. Muttaqi, and S. Perera, “Enhanced reactive power support of a PMSG based wind turbine for a Remote Area Power system,” in *Proc. Australasian Universities Power Engineering Conference, AUPEC 2010*, pp.1-5, 5-8 Dec. 2010.
- [183] STATCOM solutions for Wind Farms (2011). [Online]. Available: <http://www.abb.com>.
- [184] Wei Qiao, R.G. Harley, and G.K. Venayagamoorthy, “Effects of FACTS Devices on a Power System Which Includes a Large Wind farm,” in *Proc. IEEE Power Systems Conf. and Exposition, PSCE 2006*, pp. 2070-2076, Nov. 2006.
- [185] H. Chong, A.Q. Huang, M.E. Baran, S. Bhattacharya, W. Litzenberger, L. Anderson, A.L. Johnson, and A.A. Edris, “STATCOM Impact Study on the Integration of a Large Wind Farm into a Weak Loop Power System,” *IEEE Trans. Energy Convers.*, vol.23, no.1, pp.226-233, Mar. 2008.
- [186] Z. Saad-Saoud, M.L. Lisboa, J.B. Ekanayake, N. Jenkins, and G. Strbac, “Application of STATCOMs to wind farms,” *IEE Proceedings Generation, Transmission and Distribution*, vol.145, no.5, pp.511-516, Sept. 1998.
- [187] S.D.G. Jayasinghe, D.M. Vilathgamuwa, and U.K. Madawala, “A cascade multilevel STATCOM for wind generation systems,” in *Proc. IEEE Power Electronics and Drive Systems Conf.*, pp.1323-1328, Nov. 2009.
- [188] Y. Liu, and F.L. Luo, “Trinary hybrid multilevel inverter used in STATCOM with unbalanced voltages,” *IEE Proceedings Electric Power Applications*, vol.152, no.5, pp.1203-1222, Sept. 2005.
- [189] R. Saha, and B. Singh, “Improved 48-pulse static synchronous compensator for high-voltage applications,” *IET Trans. Power Electron.*, vol.3, no.3, pp.355-368, May 2010.
- [190] M. Saeedifard, H. Nikkhajoei, and R. Iravani, “A Space Vector Modulated STATCOM Based on a Three-Level Neutral Point Clamped Converter,” *IEEE Trans. Power Delivery*, vol.22, no.2, pp.1029-1039, April 2007.
- [191] B. Singh, R. Saha, A. Chandra, and K. Al-Haddad, “Static synchronous compensators (STATCOM): a review,” *IET Trans. Power Electron.*, vol.2, no.4, pp.297-32, July 2009.
- [192] A. Beekmann, J. Marques, E. Quitmann, and S. Wachtel, “Wind energy converters with FACTS Capabilities for optimized integration of wind power into transmission and distribution systems,” in *Proc. CIGRE/IEEE PES Joint Symposium on Integration of Wide-Scale Renewable Resources Into the Power Delivery System*, 29-31 July 2009.
- [193] P. Mitra, G.K. Venayagamoorthy, and K.A. Corzine, “SmartPark as a Virtual STATCOM,” *IEEE Trans. Smart Grid*, vol.2, no.3, pp.445-455, Sept. 2011.
- [194] S.N. Singh, J. Østergaard, and B. Singh, “Reactive power capability of unified DFIG for wind power generation,” in *Proc. IEEE Power and Energy Society General Meeting*, pp.1-7, 25-29 July 2010.
- [195] S.A. Pastromas, “Grid support by wind turbines and future trends,” in *Proc. IEEE PES Transmission and Distribution Conference and Exposition*, pp.1-7, 19-22 April 2010.
- [196] N.R. Ullah, K. Bhattacharya, and T. Thiringer, “Wind Farms as Reactive Power Ancillary Service Providers—Technical and Economic Issues,” *IEEE Trans. Energy Convers.*, vol.24, no.3, pp.661-672, Sept. 2009.
-

- [197] F.Z. Peng, J.S. Lai, J.W. McKeever, and J. VanCoevering, "A multilevel Voltage-Source Inverter with Separate DC sources for Static Var Generation," *IEEE Trans. Ind. Appl.*, vol.32, no.5, pp.1130-1138, Sept./Oct. 1996.
- [198] S. Kincic, A. Chandra, and S. Babic, "Five level diode clamped voltage source inverter and its application in reactive power compensation," in *Proc. Large Engineering Systems Conference Power eng., IEEE-LESCOPE 2002*, pp.86-92, Dec. 2002.
- [199] S. Figarado, K. Sivakumar, R. Ramchand, A. Das, C. Patel, and K. Gopakumar, "Five-level inverter scheme for an open-end winding induction machine with less number of switches," *IET Trans. Power Electron.*, vol.3, no.4. pp.637-647, July 2010.
- [200] S. Sirisukprasert, "The Modeling and Control of a Cascade Multilevel Converter Based STATCOM," PhD Thesis, Virginia Polytechnic Institute, Blacksburg, Virginia, USA, 2004.