Gm-enhanced differential colpitts VCO

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***Gm*-enhanced Differential Colpitts VCO**

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Abstract

This thesis proposes a gm -enhanced differential Colpitts voltage-control oscillator (VCO) that initiates oscillation with a lower biasing current and exhibits a better phase noise performance. The proposed gm -enhanced topology can improve performance of VCO, whereby the oscillator constructed based on the suggested topology demonstrated operation from 1.53 GHz to 2.1 GHz. The tank inductors engaged in the oscillator are each designed with a quality factor of 9. To evaluate the design, a conventional cross-coupled differential LC VCO, a conventional differential Colpitts VCO and the proposed VCO are simulated using 1.5 V supply voltage, under the 0.13 μm standard CMOS process. Biased with a current of 3 mA, the simulation results show that the proposed VCO's phase noise performance is of -128.9 dBc/Hz at 1 MHz offset, which is 3.6 dBc/Hz better than that of the cross-coupled differential LC VCO and 2 dBc/Hz better than that of the conventional differential Colpitts VCO. In the post-layout simulations of the proposed VCO and conventional cross-coupled differential LC VCO, the former has a 2.1 dBc/Hz phase noise better than that of the conventional one.

Based on the developed designed gm -enhanced topology, a gm -enhanced differential Colpitts Quadrature VCO (QVCO) is designed. Operating at 1.8 GHz, the proposed QVCO shows a phase noise of -132.4 dBc/Hz at 1-MHz offset, when biased with 4-mA current and 1.5 V supply voltage. Compared with the conventional Colpitts QVCO, the proposed gm -enhanced differential Colpitts QVCO demonstrates better phase noise of 4 dB under the same operating condition.

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Chapter 1 Introduction

1.1 Thesis Overview

Voltage-controlled oscillator (VCO) plays an ultra important role in radio frequency (RF) systems such as frequency synthesizer. It determines the performance of the whole system since it provides a reference signal by which complex functions are controlled [1]. In wireless communication systems, a steady reference is needed to enable synchronization and carrier recovery between transmitter and receiver modules. Due to the rapidly advancing wireless communication market in this decade, the requests for better VCO performances continue to grow. As a result, VCO topologies have been extensively researched and improved since the last decade [2][3].

The key considerations of VCO design are the phase noise at a certain offset from the carrier frequency [4], the tuning range of the frequency[5][6], and the power consumption [7]. Optimising these key factors seems straight-forward but they do trade-off with one another. Hence, optimally meeting the design specifications means finding the best trade-offs between many interacting variables. Other than the trade-offs approach, a number of VCO topologies have been proposed during the last decade, such as the ring VCOs [8], LC VCOs [9] and Colpitts VCOs [10].

In this thesis, ring VCOs, LC VCOs and Colpitts VCOs will be reviewed and discussed with a focus on the Colpitts VCO topology. This is followed by a review of the *gm*-boosted topologies, filtering techniques, noise cancellation, etc, and a discussion on the related literatures. Based on the differential Colpitts topology, a new *gm*-enhanced differential Colpitts VCO is then proposed.

Based on simulation, using the 0.13- μ m standard CMOS process, a VCO operating at 1.8 GHz with a 1.5 V supply voltage is achieved. The tank inductors attained quality

factors of 9, and when biased at 3 mA current, the proposed VCO has a phase noise of -128.9 dBc/Hz at the 1 MHz offset. To demonstrate the superior performance of the proposed gm -enhanced differential Colpitts VCO, it is compared with both the conventional cross-coupled LC VCO and differential Colpitts VCO. The proposed gm -enhanced differential Colpitts VCO presented phase noise that is 3.5 dBc/Hz better than that of the conventional cross-coupled LC VCO and 1.9 dBc/Hz better than that of differential Colpitts VCO. It is also observed that the proposed VCO calls for a relaxed start up requirements for oscillation. Besides, under the same condition, the tank amplitude provided by the proposed VCO is larger than that of the conventional cross-coupled LC VCO and differential Colpitts VCO, which helps to improve the phase noise performance. The layouts of the proposed gm -enhanced differential Colpitts VCO and the conventional cross-coupled LC VCO had both been completed. Post-layout simulation shows that the proposed gm -enhanced differential Colpitts VCO has a 2.1 dBc/Hz better phase noise than that of the conventional cross-coupled LC VCO.

1.2 Research Goals

The design of a VCO is not a trivial task. The phase noise of the VCO results from multiple sources of noise from different components of the circuit. Since the phase noise performance is the most important indicator of VCO's performance, the improvement of the VCO technique never stop.

The research goals for this project can be summarized in two parts. Firstly, the technical background, such as oscillation theory and design considerations of VCO, will be reviewed in details. The three typical topologies of VCOs, which are ring VCOs, LC VCOs and Colpitts VCOs will be comprehended in depth. Related gm -boosted literatures and typical VCO designs will be reviewed in details. Related

QVCO literatures will be presented as well. The second goal of this project is to propose a novel *gm*-enhanced differential Colpitts VCO and QVCO with central frequency of 1.8 GHz. The proposed VCO should have a superior performance compared with VCOs from mainstream literatures. The reasons for the better performance would then be explained based a thorough evaluation of the VCO.

1.3 Scope

VCO sees a wide range of applications in radio frequency (RF) systems [11][12] and it plays a vital role in many electronic systems. For example, it constitutes the clock generator in microprocessors or carrier synthesis in cellular phones.

Fig. 1.1 A typical transceiver front end.

Fig. 1.1 shows the schematic of a generic transceiver front end. In a frequency synthesizer, an oscillator not only provides the carrier signal for the receive path but also for the transmit path. If the oscillator exhibits a bad noise performance, both the downconversion and upconversion will be distorted. As a result, researches working towards VCOs with superior phase noise performance and lower power consumption never ceased [13][14]. Many reported works on VCOs trying to achieve better

understanding of its noise mechanisms [15][16] and its operation principles [17][18] with the final goal of leading a finer VCO design.

It is obvious that the VCO will still be a popular research subject in the next decade and its significant status in the electronics systems will not change for a long time. As a result, the research goals of this thesis, to design a gm -enhanced differential Colpitts VCO and a quadrature voltage control oscillator, are very meaningful.

1.4 Organization of Report

This report is organized as follows: Chapter Two describes the VCO technical background, including the oscillator theories, general considerations and three typical VCO topologies. The literature reviews are given in Chapter Three. The design of a 1.8 GHz gm -enhanced differential Colpitts VCO is discussed in Chapter Four, along with comparisons between the proposed VCO, conventional LC VCO and differential Colpitts VCO. The negative conductance of the proposed VCO is compared with that of the other five other types of VCOs. The post-layout simulation results have been given as well. Chapter Five presents a novel QVCO based on the gm -enhanced topology described in Chapter Four. The QVCO is then compared with the conventional Colpitts VCO, and simulation results will also be provided. The last chapter concludes the work that has been done and highlights the future directions.

Chapter 2 Technical Background

2.1 Introduction

Generally, when designing a VCO, we need to ensure that whether it can fulfil some requirements, such as attaining a specified central frequency, phase noise at a certain frequency offset or the minimum acceptable tuning range. Same as various circuits, dimensioning of the circuit component, no matter it is active or passive device, is the main challenge of the VCO design. It is obvious that the design variables are the total tank capacitance, the inductance of the tank, the equivalent tank parallel resistance, transistors widths over length ratio, and the supply voltage and biasing current. However, the design parameters have very complex interdependences on each other. Slight change made on any variable will lead to chain reactions on other parameters. This complexity results in multitudinous VCO theories, topologies according to literatures. Although oscillators have been researched for over fifty years, numbers of new theories focusing on phase noise mechanisms and VCO topologies have been continuously proposed. It leads the understanding of the phase noise performance to a deeper level. In this section, oscillator theories will be introduced and general considerations of designing a VCO will be explained in details. Three typical topologies of VCO, that is, ring oscillators, cross-coupled LC oscillators, Colpitts VCOs will be recapitulated in this chapter. Since negative conductance of the topologies plays vital role in generate tank amplitude, the negative conductance of three typical cross-coupled LC VCO topologies has been calculated according to their small-signal model.

2.2 Oscillator Theories

2.2.1 Barkhausen's Criteria

Oscillators are important components of RF circuits. they can provide periodical signals. In [19], a two-port model is put forward by Barkhausen. The model points out that oscillators can be viewed as an amplifier connecting with a feedback network

Fig. 2.1 Barkhausen two-port model.

In Fig. 2.1, the transfer function of the amplifier is represented by $G(V, j\omega)$, with the arguments V represents for the input amplitude and $j\omega$ represents for the angular frequency. With the same arguments, the function of the feedback network is represented by $H(V, j\omega)$.

Assuming the amplifier and feedback network is linear, $G(j\omega)$, instead of $G(V, j\omega)$ can be used in the calculation, and $H(j\omega)$ is used instead of $H(V, j\omega)$. The Barkhausen oscillator criteria is quite straightforward if the transfer function of Fig. 2.1 is analysed.

$$V_{out} = G(j\omega)V_G \quad (1)$$

and

$$V_H = H(j\omega)V_{out} \quad (2)$$

with

$$V_G = V_{in} + V_H \quad (3)$$

The transfer function of the complete network is hence calculated as

$$\frac{V_{out}}{V_{in}} = \frac{G(j\omega)}{1 - H(j\omega)G(j\omega)} \quad (4)$$

which is unstable if

$$|H(j\omega)||G(j\omega)| \geq 1 \quad (5)$$

As long as the left-hand side of the above expression is greater than one, oscillation amplitude will grow. Due to non-linear and saturation effects, the system will arrive at a steady-state amplitude when

$$|H(j\omega)||G(j\omega)| = 1 \quad (6)$$

For the phase

$$\phi_G(j\omega) + \phi_H(j\omega) = 0 + 2\pi k \quad k = 1 \dots n \quad (7)$$

where, $\phi_G(j\omega)$ is the phase of $G(j\omega)$ and $\phi_H(j\omega)$ is the phase of $H(j\omega)$.

Eq. (5) and (7) are well known as Barkhausen oscillator criteria [19]. Assuming a zero degree phase shift over the active part $G(j\omega)$, Eq. (7) reduces to

$$\phi_H(j\omega) = 0 \quad (8)$$

We can also get the equation of the frequency of oscillation:

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \quad (9)$$

2.2.2 One-port View of Oscillators

Because the feedback loop is closed around a two-port network, the above view of oscillators is called the "two-port" model in microwave theory. On the other hand, the oscillator can also be treated as "one-port" model [20]. In "one-port" view, we connect two two-port networks to each other. The Fig. 2.2 shows a schematic of the one-port view of oscillators.

Fig. 2.2 One-port view of oscillators.

When oscillator operates, the energy reciprocates between the tank inductors and capacitors. Some of the energy is dissipated as heat due to the tank equivalent parallel resistor R_p . As a result, if we put a negative resistor equal to $-R_p$ in parallel with the tank, the tank can oscillate indefinitely.

The reason for the oscillation can be expressed as follows:

$$R_p // (-R_p) = \infty \quad (10)$$

As a result, the oscillator has an infinite quality factor, Q .

This is the one-port view of LC oscillators. The concept of negative resistance can be comprehended as follows: with the negative resistance, the current drawn by the circuit will decrease with the applied voltage increases.

2.3 General Considerations

2.3.1 Introduction

A voltage control oscillator (VCO) is an oscillator where its output frequency changes according to its control voltage linearly. Fig. 2.3 illustrates how the frequency of a VCO is affected by the control voltage.

Fig. 2.3 Definition of a VCO.

The relationship between the output frequency and the control voltage can be expressed as follows:

$$\omega_{out} = \omega_0 + K_{VCO}V_{out} \quad (11)$$

where ω_0 is the intercept when setting $V_{cont} = 0$ and K_{VCO} is called the "gain" or "sensitivity" of the circuit with a unit of rad/s/V. $\omega_1 - \omega_2$ is the tuning range of the VCO.

2.3.2 Quality Factor

The quality factor (Q) of the resonant tank significantly determines the phase noise performance of the LC VCO. Basically, the general definition of a component's Q factor is given by the following equation [21]:

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}} \quad (12)$$

In real situation, inductors (and capacitors) are followed by resistive components, which are mostly contributed by the metal wire used in electronics devices. As a result, the inductor can be modelled by an inductor connecting in series with a resistor, which is shown in Fig. 2.4(a). The resistive part of a capacitor can be modelled as Fig. 2.4(b).

Fig. 2.4 A simple inductor and capacitor model with series resistor.

The models of Fig. 2.4 is used to explain definition of Q in depth.

Assuming a sinusoidal current, $i(t) = I_{max} \sin(\omega t)$, passes through the inductor, the maximum magnetic energy stored in the inductor, E_{Lmax} , can be written as

$$\begin{aligned} E_{Lmax} &= \int_0^{\frac{T}{4}} i(t)v(t)dt = \int_0^{\frac{T}{4}} i(t)L_s \frac{di}{dt}dt = L_s \int_0^{I_{max}} idi = \frac{1}{2}L_s I_{max}^2 \\ &= L_s I_{rms}^2 \end{aligned} \quad (13)$$

where $T = \frac{1}{f}$ is the period of the signal.

The energy dissipated in the resistor in series with the inductor per cycle is

$$E_{L_{dissipated}} = \int_0^T i^2(t) R_{sL} dt = I_{rms}^2 R_{sL} T \quad (14)$$

Then, the Q of an inductor is

$$Q_L = 2\pi \frac{L_s I_{rms}^2}{I_{rms}^2 R_{sL} T} = 2\pi f \frac{L_s}{R_{sL}} = \frac{\omega L_s}{R_{sL}} \quad (15)$$

Similarly, the electric energy stored in a capacitor, $E_{C_{max}}$ can be written as

$$\begin{aligned} E_{C_{max}} &= \int_0^{\frac{T}{4}} v(t) i(t) dt = \int_0^{\frac{T}{4}} v(t) C_s \frac{dv}{dt} dt = C_s \int_0^{V_{max}} v dv = \frac{1}{2} C_s V_{max}^2 \\ &= C_s V_{rms}^2 \end{aligned} \quad (16)$$

The energy dissipated in the resistive component of the circuit is

$$E_{C_{dissipated}} = I_{rms}^2 R_{sC} T = V_{rms}^2 \omega^2 C_s^2 R_{sC} T \quad (17)$$

Hence, the Q of the capacitor can be written as:

$$Q_C = 2\pi \frac{C_s V_{rms}^2}{V_{rms}^2 \omega^2 C_s^2 R_{sC} T} = \frac{1}{\omega C_s R_{sC}} \quad (18)$$

Fig. 2.5 presents a simple parallel LC tank. When such a tank oscillates, the electric and magnetic energy are periodically exchanged between the capacitors and inductors, the maximum energy stored in the LC-tank which is denoted as $E_{L_{max}}$ can therefore be

Fig. 2.5 A simple parallel LC tank.

calculated as follows:

$$E_{LC\max} = LI_{rms}^2 = CV_{rms}^2 \quad (19)$$

Meanwhile, the energy also dissipates through the series resistors of the inductors and capacitors.

From Eq. (14) and Eq. (15) , the dissipated energy in one cycle $E_{LCdissipated}$ is

$$\begin{aligned} E_{LCdissipated} &= E_{Ldissipated} + E_{Cdissipated} \\ &= I_{rms}^2 T(R_{sL} + R_{sC}) \end{aligned} \quad (20)$$

Finally, the LC tank Q_{LC} can be determined, where:

$$\begin{aligned} Q_{LC} &= \frac{\omega L}{R_{sL} + R_{sC}} \\ &= \frac{1}{\omega C(R_{sL} + R_{sC})} \end{aligned} \quad (21)$$

The foregoing derivation takes the resistant part of capacitor into consideration. This is for the integrity of comprehension. However, in most of the research paper, the resistive part of the capacitor is neglected. Therefore, the following analysis will follow this routine.

2.3.3 Series to Parallel Tank Conversion

The circuit of Fig. 2.6(a) can be transformed to an equivalent topology of Fig. 2.6(b), which is a model that more adaptable for VCO design.

Fig. 2.6 Oscillator tank converted to parallel equivalent circuit.

Generally, the resistive part of capacitor is neglected. Therefore, the analysis of the inductor connection conversion shown in is of importance. It is possible to convert the circuit to the parallel structure in a narrow frequency range, which is shown in Fig. 2.7.

Fig. 2.7 A series combination to a parallel combination conversion.

For the two circuit to be equivalent:

$$sL_s + R_{sL} = \frac{R_p sL_p}{R_p + sL_p} \quad (22)$$

Considering only the steady state response. Assume $s = j\omega$ and rewrite the Eq. (22) :

$$(L_s R_p + L_p R_{sL}) j\omega + R_{sL} R_p - L_s L_p \omega^2 = R_p L_p j\omega \quad (23)$$

According to the equivalent relationship of the left and right of the Eq. (23),

$$\left\{ \begin{array}{l} L_s R_p + L_p R_{sL} = R_p L_p \\ R_{sL} R_p - L_s L_p \omega^2 = 0 \end{array} \right. \quad (24)$$

$$R_{sL} R_p - L_s L_p \omega^2 = 0 \quad (25)$$

Calculating R_p from the Eq. (25) and substituting into Eq. (24),

$$L_p = L_s \left(1 + \frac{R_{sL}^2}{L_s^2 \omega^2} \right) \quad (26)$$

Recall Eq. (15), which is

$$Q_L = \frac{\omega L_s}{R_{sL}} \quad (27)$$

and the fact that the Q of a typical monolithic inductor is greater than three,

the Eq. (28) can be derived,

$$R_p \approx \frac{L_s^2 \omega^2}{R_{sL}} \quad (28)$$

$$\approx Q^2 R_{sL} \quad (29)$$

2.3.4 Phase Noise

Analog circuits are sensitive to various noises such as flicker noise, white noise, thermal noise, etc. So are the oscillators. Both the frequency and the amplitude can be deteriorated by the noise from various sources. The noise can be injected into an oscillator from its component devices or from external means. For an ideal oscillator

with sinusoidal output, the spectrum should present a shape of an impulse, which is shown in Fig. 2.8(a). However, the fluctuations and variations in oscillation period always exist.

Fig. 2.8(a) Frequency spectrum of ideal oscillators. (b) Frequency spectrum of ideal oscillators.

For the general output of an oscillator, we can write $x(t) = A \cos[\omega_c t + \phi_n(t)]$, $\phi_n(t)$ denotes a small random excess phase which is the variation in the oscillation period. The function $\phi_n(t)$ is called "phase noise". Since $\phi_n(t)$ presents a small fluctuation, $|\phi_n(t)| \ll 1$ is reasonable. As a result, we can get:

$$x(t) \approx A \cos \omega_c t - A \phi_n(t) \sin \omega_c t \quad (30)$$

This implies that the spectrum of $\phi_n(t)$ is translated to $\pm \omega_c$. In other word, the fluctuation introduces sidebands close to $\pm \omega_c$ with symmetrical distribution around $\pm \omega_c$, just like a "skirt" around the carrier frequency [22], which is depicted in Fig. 2.8(b).

"Phase noise" is used to describe the frequency fluctuations in frequency domain. Its corresponded name in time domain is "jitter". Jitter describes the random perturbation of a periodic signal at zero-crossings point. (shown Fig. 2.9).

Fig. 2.9 Time domain: jitter.

The role of a VCO in phase-locked loop (PLL) is to keep the synchronization of the LO signals. Fig. 2.10 shows a simplified phase-locked loop diagram.

Fig. 2.10 Simplified phase-locked loop diagram.

Seen from Fig. 2.10, a PLL is constructed by a phase detector, a loop filter followed by a VCO and a divider. The role of the PLL is to make sure its output frequency to be

a integral multiple of the frequency of input reference [23]. A linear relationship between tuning voltage and frequency can be maintained by a VCO and this function ease the design of PLL significantly.

To illustrate the adverse effect of phase noise in RF communication system, Fig. 2.11 is depicted here to ease the explanation.

Fig. 2.11 Simplified receiver block diagram.

Fig. 2.11 shows a simplified receiver diagram. When a receiver processes the signal, the incoming radio frequency (RF) signal is downconverted by the local oscillator (LO) and the mixer. After downconversion, an intermediate frequency (IF) signal will be generated. If the oscillator is a low-side VCO, in which the oscillator frequency is lower than the RF signal frequency, the resulting intermediate (IF) frequency can be written as:

$$f_{IF} = f_{RF} - f_{LO} \quad (31)$$

In reality, the output signal of local oscillator may contain a noisy spectrum just as what has been shown in Fig. 2.12. Meanwhile, in the adjacent channel of our desired signal, there may be a powerful interfering signal. When the two signals are mixed

with the LO output, the downconverted signals will exhibit two overlapped spectrums. As a result, the wanted signal is suffered by the severe noise due to the tail of the interfere and the signal-to-noise ratio [24] is degraded. This effect is called "reciprocal mixing". Fig. 2.12 shows the real situation of down conversion in receivers.

Fig. 2.12 Reciprocal mixing.

The phase noise spectrum has different component at different offset frequency. Fig.

Fig. 2.13 Phase noise spectrum in a typical LC oscillator.

2.13 shows a typical single side band phase noise spectrum [25].

The corner between the $1/\Delta f^3$ and $1/\Delta f^2$ regions is defined as $\Delta f_{1/\Delta f^3}$ (referred as frequency corner). At low offset frequency to $\Delta f_{1/\Delta f^3}$, a $1/\Delta f^3$ behaviour can be observed and is known as the " $1/\Delta f^3$ region". This region can also be called as the "flicker-noise" region. For the medium offset frequencies, a $1/\Delta f^2$ - dependence behaviour can be observed, and thus the $1/\Delta f^2$ region. This region can also be called as the "white noise" region. Up to the high offset frequency, the constant amplifier noise floor is the dominant.

Generally, phase noise is characterized by the signal sideband noise spectral density normalized to the carrier signal power (Fig. 2.14).

Fig. 2.14 Definition of phase noise.

Phase noise is defined as [26] :

$$\mathcal{L}_{total}\{\Delta\omega\} = 10\log\left[\frac{\mathcal{P}_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})}{\mathcal{P}_{carrier}}\right] \quad (32)$$

where $\mathcal{P}_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})$ represents the single side-band power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz. This definition of $\mathcal{L}_{total}\{\Delta\omega\}$ includes noise results from both of the amplitude and phase fluctuations, $A(t)$ and $\phi(t)$. Thus, one problem of this definition is that it is not able to distinct the effect of amplitude and phase. In fact, the effect of the amplitude and noise can be reduced by some measures. For instant, a limiter applied to the output signal of a VCO can be an effectual one. As a result, in most of the research papers in the last decade, $\mathcal{L}_{total}\{\Delta\omega\}$ is dominant by $\mathcal{L}_{phase}\{\Delta\omega\}$, which is known as phase noise.

In 1966, Leeson first set up the following semi-empirical expression for the phase noise, known as the Lesson-Culter phase noise model [27]. This model is based on an assumption that the oscillators are linear time invariant (LTI) systems.

$$\mathcal{L}_{phase}\{\Delta\omega\} = 10 \log \left\{ \frac{2FkT}{P_s} \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega} \right)^2 \right] \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\} \quad (33)$$

where F is an empirical parameter (often called the "device excess noise number"), k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated when current ones through the resistant components of the tank, ω_0 is the central frequency, Q_L is the effective quality factor of the inductor, $\Delta\omega$ is the offset from the central frequency and $\Delta\omega_{1/f^3}$ is the frequency corner (depicted in Fig. 2.13).

In most of the cases, the flicker-noise portion is described empirically and negligible. To simplify Eq. 33, some extra equations are needed:

$$\left\{ \begin{array}{l} Q_{tank} = \frac{\omega_c L}{R_s} \end{array} \right. \quad (34)$$

$$\left\{ \begin{array}{l} P_{sig} = \frac{V_{sig}^2}{2R_p} = \frac{V_{sig}^2}{2Q_{tank}^2 R_s} \end{array} \right. \quad (35)$$

$$\left\{ \begin{array}{l} \omega_c \gg \Delta\omega \end{array} \right. \quad (36)$$

Together with Eq. 33, the following equation can be written:

$$\mathcal{L}(\Delta\omega) = 10 \log \left(\frac{FkTR_s}{V_{sig}^2} \cdot \frac{\omega_c^2}{\Delta\omega^2} \right) \quad (37)$$

This is the simplified Leeson's model, which is widely used in literatures.

In 1998, Hajimiri proposed a new model of phase noise. Different with Leeson's model, this model was based on the time-varying nature of all oscillators. Hajimiri pointed out that the noise source injected into tank in different time period imposed different impact on the phase noise performance. Based on this idea, Hajimiri proposed a time-domain concept of "impulse sensitivity transfer function"(ISF) to characterize the phase noise over different oscillation period. We can comprehensive the ISF like this: ISF describe the sensitivity to an input charge fluctuation of every point of the output periodic waveform. Hajimiri's equation for phase noise is:

$$\mathcal{L}(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2} / \Delta f}{4\Delta\omega^2} \quad (38)$$

where Γ_{rms} is the mean value of the ISF function, q_{max} is the maximum charge across the tank capacitor. $\overline{i_n^2} / \Delta f$ is the mean square noise current density.

2.3.5 Output Amplitude

From the analysis of phase noise, it is obvious that output amplitude, or the tank amplitude V_{tank} plays a significant role in improving the noise performance.

In 1999, Hajimiri proposed the concepts of "voltage-limited" regime and "current-limited" regime [28] to characterize the behaviour of tank amplitude in oscillation. Based on these two concepts, deeper comprehension of the tank amplitude can be achieved.

In the current-limited regime, a linear relationship holds between the bias current and tank amplitude. That is, the tank amplitude increases with its bias current until the oscillator reaches the voltage-limited regime.

In voltage-limited regime, the tank amplitude will be held to certain amplitude V_{limit} , which is determined by the supply voltage of the oscillator and/or a change in the operation mode of active devices (e.g. MOS transistors entering triode region) [29].

The V_{tank} can be expressed as:

$$\left\{ \begin{array}{l} V_{tank} = \frac{I_{bias}}{g_{tank}} (I - limited) \\ V_{limit} (V - limited) \end{array} \right. \quad (39)$$

Fig. 2.15 depicts the current-limited regime and voltage-limited regime.

Fig. 2.15 Simulated tank voltage amplitude versus tail-current source for the 1.8-GHz CMOS differential oscillator.

2.3.6 Figure of Merit

The phase noise performance can be improved by increasing the biasing current and decreasing the central frequency. Also, when calculating at different offset frequencies, the phase noise has quite a large difference. When compare the phase noise performance of VCOs, the power consumption, frequency offset and the central frequency must be taken in to consideration to make the comparison fair. As a result, the concept of "figure of merit" (FOM) is proposed in [30] and is used in [30,31]. For oscillators operating at different frequencies and with different power consumptions, the FOM can be used to compare the phase noise performance at different offset frequency.

The FOM is defined as follows:

$$FOM = L(\text{offset}) - 20 \log\left(\frac{f_0}{f_{\text{offset}}}\right) + 10 \log\left(\frac{P_{DC}}{1mW}\right) \quad (40)$$

where, $L(\text{offset})$ is the phase noise at certain offset frequency, f_0 is the central frequency, f_{offset} is the offset frequency and the P_{DC} is the power consumption.

2.4 Typical CMOS Integrated Oscillator Topologies

2.4.1 Ring Oscillators

Ring oscillators exhibit better integrability and smaller die areas compared to the conventional LC tank oscillators. This is because of the absence of the inductive elements in ring oscillators. Furthermore, ring oscillators can offer wide tuning range. As a result, the ring oscillators have been widely used in many applications such as in digital phase locked loop (PLL) and in clock recovery circuits. The main parts of a ring oscillator are a number of gain stages. The simplest oscillator can be implemented by putting odd number of inverters (at least three) in series. Fig. 2.16(a) depicts the schematic of such oscillator. Connecting as Fig. 2.16(b), it can provide quadrature output as well.

The ring oscillators achieve frequency tuning by means of changing the number of chain stages or changing the biasing current. The frequency of oscillation can be determined by the following equation:

Fig. 2.16(a) Simple ring oscillator structure. (b) Differential ring oscillator.

$$f_{osc} = \frac{1}{2N \cdot T_d} \quad (41)$$

where, N is the number of stages in the chain, T_d is the delay of the each inverter stage.

2.4.2 Cross-coupled LC Oscillators

Due to the gradually development of monolithic inductors in CMOS topology, it is possible for RF designers to implement VCOs with passive resonant circuits. The central frequency of LC can be written as:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \quad (42)$$

where L_{eq} is the equivalent parallel inductance of the LC tank, and C_{eq} is the equivalent parallel capacitance of the LC tank. At this frequency, the impedance of L_{eq} , which is $j\omega_{LC}L_{eq}$ and the impedance of C_{eq} , which is $1/j\omega_{LC}C_{eq}$ are equal and opposite to each other. In other words, they can cancel each other at the oscillation frequency. As a result, a infinite impedance can be achieved.

The cross-coupled LC oscillator is a typical VCO structure. It is more popular among the RF system design compared with other topologies. This is because that the cross-coupled LC oscillator offers a relaxed start-up condition, differential property and relatively good phase noise [32].

The cross-coupled structure plays a vital role in this type of oscillator because cross-coupled structure provides negative resistance. To illustrate this point, the single-ended structure of negative input impedance Fig. 2.17(a) [33] is discussed.

Fig. 2.17(a) Source follower with positive feedback to create negative input impedance.

(b) Small-signal schematic of (a).

From Fig. 2.17(b), the following equations can be written:

$$I_x = g_{m2}V_2 = -g_{m1}V_1 \quad (43)$$

and

$$V_x = V_1 - V_2 \quad (44)$$

Assuming $g_{m1} = g_{m2}$,

$$\frac{V_x}{I_x} = \frac{-2}{g_m} \quad (45)$$

Connecting the gate of M_2 to the drain of M_1 , a differential structure is constructed, which is the well-known "cross-coupled" structure (Fig. 2.18). This typical structure is also called "negative- gm " structure.

Fig. 2.18 Negative gm generator.

The R_{in} in Fig. 2.18 is equal to $\frac{-2}{g_m}$. The condition for oscillation to start is

$$R_p - \frac{2}{g_m} \geq 0 \quad (46)$$

Fig. 2.19 shows a typical cross-coupled LC VCO schematic. The performance of this VCO will be compared with the proposed gm -enhanced differential Colpitts VCO and differential Colpitts VCO in Chapter Four.

Fig. 2.19 Schematic of a typical cross-coupled LC VCO.

2.4.3 Colpitts VCO

2.4.3.1 Single-end Colpitts VCO

The Colpitts VCO has a brilliant phase noise property. Most of the noise is injected into the tank during the energy transfer process. In the conventional cross-coupled LC VCO, the energy is delivered into the tank at the maximum impulse sensitive point of oscillation. This property significantly deteriorates the phase noise performance of the conventional cross-coupled LC VCO. In Colpitts VCO, the energy is instead delivered to the LC tank at the minimum impulse sensitive point [34] of oscillation. Thus, a better phase noise can be expected in Colpitts VCO as compared to the cross-coupled LC VCO. Fig. 2.20(a) depicts the schematic of a single-ended Colpitts oscillator.

Fig. 2.20(a) Single-ended Colpitts oscillator topology. (b) Small signal equivalent circuit of (a).

From Fig. 2.20(b), the following equations can be written:

$$\omega_R^2 = \frac{1}{L_p \frac{C_1 C_2}{C_1 + C_2}} \quad (47)$$

$$\begin{aligned} g_m R_p &= \frac{(C_1 + C_2)^2}{C_1 C_2} \\ &= \frac{C_1}{C_2} \left(1 + \frac{C_2}{C_1}\right)^2 \end{aligned} \quad (48)$$

where ω_R is the oscillation frequency of single-end Colpitts oscillator, $g_m R_p$ is the voltage gain seen from the source of M_1 to the drain of M_1 (the output).

Setting $C_1/C_2 = 1$,

$$g_m R_p \geq 4 \quad (49)$$

The important conclusion drawn from Eq. 49 is that Colpitts oscillator needs at least a gain of 4 to start up the oscillation while the conventional cross-coupled LC oscillator only needs 1. Leading to a more stringent start up requirement, this is a significant disadvantage of Colpitts oscillator.

From Fig. 2.20(b), the negative small-signal negative conductance of the single-end conventional Colpitts oscillator can be derived.

$$Y_{inA} = \frac{I_x}{V_x} = \frac{-C_1 C_2 \omega^2}{g_m + (C_1 + C_2)s} \quad (50)$$

$$R_e[Y_{in}]_A = \frac{-g_m C_1 C_2 \omega^2}{g_m^2 + (C_1 + C_2)^2 \omega^2} \quad (51)$$

Assuming $C_1 = C_2 = C$,

$$R_e[Y_{in}]_A = \frac{-g_m C^2 \omega^2}{g_m^2 + 4C^2 \omega^2} \quad (52)$$

Since $4C^2 \omega^2 \gg g_m^2$, Eq. 52 can be written as

$$R_e[Y_{in}]_A = -\frac{1}{4} g_m \quad (53)$$

2.4.3.2 Differential Colpitts VCO

Although the conventional Colpitts VCO has better phase noise performance compared with conventional cross-coupled LC oscillator, the single-end nature is a vital limitation for its application. Thus, a differential Colpitts VCO is not only expected but necessary.

Fig. 2.21[35] shows the schematic of a differential Colpitts VCO. A differential output can be achieved by coupling two identical single-end Colpitts oscillators. The source-to-ground capacitors of the two oscillators can be replaced by one capacitor

between their sources, that is C_2 in Fig. 2.21. When the differential Colpitts VCO oscillates, the current flows in one transistor (i.e. M_3) switches to the other transistor (i.e. M_4) at every half oscillation period. The switch has to occur in a synchronized manner and can be achieved by a pair of cross-coupled NMOS, denoted as M_1 and M_2 in Fig. 2.21. The fast current switching between M_1 and M_2 can suppress noise contributions from the active devices during the zero-crossings of the tank voltage and hence improving on the phase noise characteristics. Meanwhile, the tail cross-coupled

Fig. 2.21 A differential Colpitts VCO schematic.

NMOS pair can also provide a negative resistance to improve the small-signal loop gain, relaxing the start-up condition accordingly.

The schematic of the differential Colpitts VCO (Fig. 2.21) will be simulated in Chapter Four and the results will be compared with both the conventional cross coupled VCO and the proposed gm-enhanced differential Colpitts VCO.

It is also necessary to calculate the negative small-signal negative conductance of the differential Colpitts VCO of Fig. 2.21. The small-signal model of the differential Colpitts VCO is shown in Fig. 2.22.

Fig. 2.22 Small-signal model of the differential Colpitts VCO.

According to Fig. 2.22, the following equations can be written:

$$\begin{cases} (V - V_x)sC_1 + (0 - V_x)g_{m3} = I \\ V_x \cdot 2sC_2 + (-V_x)g_{m1} = I \end{cases} \quad (54)$$

$$(55)$$

From Eq. (54) and (55), the small-signal admittance seen from the drain of M_3 of the differential Colpitts VCO can be attained:

$$Y_{inB} = \frac{I}{V} = \frac{sC_1(2sC_2 - g_{m1})}{2sC_2 - g_{m1} + sC_1 + g_{m3}} \quad (56)$$

where, g_{m3} is the transconductance of M_3 , and g_{m1} is the transconductance of M_1 . The real part of Y_{inB} is

$$R_e[Y_{in}]_B = - \frac{\omega^2 (C_1^2 g_{m1} + 2C_1 C_2 g_{m3})}{\omega^2 (C_1 + 2C_2)^2 + (g_{m3} - g_{m1})^2} \quad (57)$$

Letting $g_{m3} = g_{m1}$,

$$R_e[Y_{in}]_B = -\frac{g_m C_1}{C_1 + 2C_2} \quad (58)$$

Assuming $C_1 = C_2 = C$, Eq. (57) can be written as :

$$R_e[Y_{in}]_B = -\frac{1}{3} g_m \quad (59)$$

The differential Colpitts VCO structure proposed in [36] is depicted in Fig. 3.1. The main idea of [36] is that a differential output can be achieved by connecting two identical single-end VCO together. The current only flows in each side of the single-end Colpitts VCO main transistors by less than half of the oscillation period. Therefore, with a current switching mechanism switching the tail current from one side to another, the oscillator can work as well. As a result, an improved VCO structure with a current switching mechanism [Fig. 3.2(a)] is proposed. Meanwhile, [36] has proposed that the current switching mechanism be implemented by a pair of cross-coupled NMOS transistors. The cross-coupled NMOS pair can conduct the current from one side to another side. The usage of the cross-coupled NMOS pair leads to another advantages:

Fig. 3.2 (a) Current switching topology by timed switch implementation.(b) Current switching topology by NMOS transistors implementation.

the negative resistance of the cross-coupled NMOS pair can enhance the small-signal loop gain. As a result, the originally stringent start-up requirement of Colpitts VCO becomes relaxed. This is the beginning of the *gm*-boosted topology of VCO.

The small-signal equivalent circuit of Fig. 3.2(b) is the same as that presented in Fig. 2.22. Thus, the two circuits should have the same negative conductance. Recall the Eq. (59), the small-signal negative conductance Fig. 3.2(b) is $-gm/3$

The oscillator of Fig. 3.2(a) operates at a central frequency of 2.12 GHz and a tuning range of 30.5%. The oscillator is designed with a supply voltage of 2.5 V and 4 mA biasing current and inductors with quality factors of 6. At 3 MHz offset, the phase noise performance is as good as -139 dBc/Hz.

3.2 Low Phase Noise *Gm*-Boosted Differential Gate-to-source Feedback Colpitts CMOS VCO [37].

In [37], a *gm*-boosted differential gate-to-source feedback Colpitts (GS-Colpitts) CMOS VCO was proposed. Fig. 3.3 shows the schematic of the design.

Fig. 3.3 Schematic of *gm*-boosted GS-Colpitts CMOS VCO.

The main breakthrough of the design is that it added a gate to source feedback network while maintaining the cross-coupled structure. The negative small-signal conductance of the proposed VCO can be expressed as:

$$Y_{inC} = \frac{I}{V} = -\frac{g_{m1}\omega^2 C_1 C_2}{g_{m1}^2 + \omega^2 (C_1 + C_2)^2} \cdot \frac{1}{2} \left[1 + \frac{g_{m3}}{g_{m1}} \left(1 + \frac{C_1}{C_2} \right) \right] + j \frac{1}{2} \frac{\omega^3 C_1 C_2 (C_1 + C_2) - g_{m1} g_{m3} \omega C_1}{g_{m1}^2 + \omega^2 (C_1 + C_2)^2} \quad (60)$$

Comparing with that of the single-end Colpitts VCO (Fig. 2.20), a conclusion can be drawn that the negative conductance of the gm -boosted GS-Colpitts VCO has increased by a factor of $0.5[1 + (g_{m3}/g_{m1}) \cdot (1 + C_1/C_2)]$. Assuming $C_1 = C_2 = C$, $0.5[1 + (g_{m3}/g_{m1}) \cdot (1 + C_1/C_2)] = 1.5$. Given the negative conductance of the single-end Colpitts VCO is $-\frac{1}{4}g_m$, the negative conductance of the design can be written as:

$$R_e[Y_{in}]_C = -\frac{3}{8}g_m \quad (61)$$

The proposed VCO consumes a lower start-up current. Meanwhile, the capacitor feedback network of the Colpitts oscillator suppressed the flicker noise and AM-to-FM conversion. The VCO of Fig. 3.3 presents a phase noise of -128dBc/Hz at offsets of 1 MHz with a central frequency of 1.86 GHz.

3.3 Gm -boosted Common-gate LNA and Differential Colpitts VCO/QVCO in 0.18- μm CMOS [38].

In [38], two differential Colpitts VCOs and a quadrature VCO are proposed and discussed, which are depicted in Fig. 3.4 and Fig. 3.5. The main breakthrough of the design shown in Fig. 3.4(a) is that the gate of the NMOS pair is connected to the drain of each other, instead of connected directly to the biasing voltage. This connection saves the blocking capacitors and bias resistor so that the proposed VCO is able to achieve self-biasing.

The small-signal admittance seen from the drain of M_1 can be written as:

$$Y_{inD} = \frac{s^2 C_1 C_2 - g_m s C_2}{g_m + s(C_1 + C_2)} \quad (62)$$

Fig. 3.4 Differential Colpitts VCOs of [38].

The real part of the admittance can then be calculated as follows:

$$R_e[Y_{in}]_D = -\frac{g_m \omega^2 C_2 [2C_1 + C_2]}{g_m^2 + \omega^2 (C_1 + C_2)^2} \quad (63)$$

Compared with the single-end Colpitts VCO, the VCO proposed in Fig. 2.20 has demonstrated increased negative small-signal conductance by a factor of $(2+C_2/C_1)$.

Assuming $g_{m3} = g_{m1}$ and $C_1 = C_2 = C$, the following conclusion can be drawn:

$$R_e[Y_{in}]_D = -\frac{3}{4} g_m \quad (64)$$

In Fig. 3.4(b), an evolution design based on Fig. 3.4(a) is proposed. As depicted in Fig. 3.4(b), another NMOS pair (M₃ and M₄) was inserted below the cross-coupled transistors. The gates of M₃ and M₄ were connected directly to the output of the oscillator. This connection can relax the voltage headroom requirement.

The VCO of Fig. 3.4(a) is fabricated in 0.18- μm CMOS process. The central frequency of the VCO is 1.8 GHz. The phase noise performance is -128dBc/Hz at 1 MHz with a supply voltage of 2.0 V and a current consumption of 3.6 mA.

In [38], a novel quadrature VCO (QVCO) based on Fig. 3.4(b) is proposed. A quadrature outputs can be obtained by coupling two identical oscillators together. Fig. 3.5 shows the schematic of the QVCO proposed in [38].

Fig. 3.5 Colpitts QVCO

Transistor M3 and M4 are used as the coupling devices. The gates of M3 and M4 in the I -phase VCO (marked with Q+ and Q-) are connected to the outputs of Q -phase VCO. The gates of M7 and M8 (marked with I- and I+) are connected to the outputs of I -phase oscillator. The QVCO is fabricated in 0.18- μm CMOS process. The Q of the tank inductor is around 10 when the frequency is tuned to 1.83 GHz. The QVCO

achieves a phase noise of -127 dBC/Hz at 1 MHz offset, with a supply voltage of 2 V and 4.3 mA current consumption.

3.4 A CMOS Colpitts VCO Using Negative-Conductance Boosted Technology [39].

Fig. 3.6 depicts the negative-conductance boosted differential Colpitts VCO. Different from the first three gm -boosted VCO designs, an inductor is deployed to boost the negative-conductance. In Fig. 3.6, two inductors L_{ind} are inserted between the cross-coupled structure (M_1 , M_2) and the Colpitts VCO core. The negative conductance looking from the top of the inductors can be written as:

$$-G_{m2} = \text{Re}\{Y_{IN,2}\} = \frac{R_{ind}C_{m1}\omega^2 + (R_{ind}G_{m1}^2 - G_{m1})}{L_{ind}^2C_{m1}^2\omega^4 + (L_{ind}^2G_{m1}^2 - 2L_{ind}C_{m1} + R_{ind}^2C_{m1}^2)\omega^2 + (1 - R_{ind}G_{m1})^2} \quad (65)$$

Fig. 3.6 Schematic of the negative-conductance boosted differential Colpitts VCO.

where G_{m1} is the negative conductance of the cross-coupled structure (M_1, M_2).

To verify the contribution of the inductors, G_{m2} versus L_{ind} is simulated as shown in the graph of Fig. 3.7. The imaginary part of the input admittance ($Y_{IN,2}$) is also simulated and drawn in the same figure. When the imaginary part has a rapid transition, the small variations on the inductance will induce large phase fluctuations. As a result, it is necessary for the inductance of the L_{ind} to be chosen such that the imaginary part of $Y_{IN,2}$ shows a stable performance as the inductance is varied.

Fig. 3.7 Simulated conductance (G_{m2}) and imaginary part of the input admittance ($Y_{IN,2}$) at 30 GHz versus inductance L_{ind} .

According to Fig. 3.7, although setting L_{ind} at 0.52 nH achieving the largest gm -boosted effect, the $\text{Im}(Y_{IN,2})$ encounters a rapid transition. Therefore, the most suitable inductance for the VCO is 0.3 nH, where even with 30% inductance fluctuation, the imaginary part of $Y_{IN,2}$ only changes by 0.5 mS.

This design provides a new idea on the gm -boost topology of VCO. Implemented with 0.18- μm CMOS process, the negative-conductance boosted Colpitts VCO realises a phase noise of -104.1 dBc/Hz at 1-MHz offset, at a central frequency of 30 GHz. The supply voltage is 1.0 V and the VCO core consumes 2.3-mW dc power.

3.5 Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise [40].

In [40], a concept of "Class-C oscillator" is defined. "Class-C oscillators" are marked by class-C impulse-like current waveforms as shown in Fig. 3.8.

Fig. 3.8 MOS current waveform and amplitude of the fundamental current harmonic in the class-C oscillator.

Starting from a differential Colpitts oscillator with additional feedback from tanks to MOS gate (shown in Fig. 3.9), a new phase noise expression is proposed:

$$L(\Delta\omega) = 10 \log \left(\frac{k_B T}{2 \Delta \omega^2 C^2 I_{bias}^2} \cdot \frac{1}{R^2 (1-n)^2} \cdot \left(\frac{1}{R} + \frac{\gamma}{R} \frac{1-n}{k+n} \right) \right) \quad (66)$$

where $n = C_1/(C_1+C_2)$, is the feedback factor, k_B is the Boltzmann's constant, and γ is the MOS channel noise factor, R is the equivalent parallel tank resistance at resonance, k is the voltage gain from tanks to MOS gate.

With $k = 1$, a illustrating of phase noise performance of the modified Colpitts VCO changing with n is presented in Fig. 3.10. For comparison, the relationship between n

and phase noise of a conventional differential Colpitts VCO is also indicated in the same graph.

Fig. 3.9 Differential Colpitts oscillator with additional feedback from tanks to MOS gates (modified Colpitts).

Fig. 3.10 Calculated (solid line) and simulated (dots) phase noise at 3MHz offset for the standard and modified Colpitts oscillator.

According to Fig. 3.10, it is extremely beneficial to choose n equal to zero since with the decrease of the n , the phase noise performance gets better. With $n = 0$, the phase noise improvement can be as large as 5 dBc and at the same time. The capacitors C_1 are eliminated from the circuit.

Therefore, final designs with $k = 1$ and $n = 0$ are proposed as illustrated in Fig. 3.11(a). With only a large capacitance at the tail, the class-C VCO is similar to that of a standard differential cross-coupled LC-tank oscillator. In fact, they can be viewed as the optimal evolution for either the standard differential cross-coupled LC-tank oscillators or the differential Colpitts oscillators.

Fig. 3.11 Schematic views of the class-C oscillator: (a) MOS gate bias is provided with a low-pass RC filter. (b) centre-tapped secondary winding of a transformer.

The two VCOs in Fig. 3.11 were implemented in a standard 0.13- μm CMOS process. They are tunable over the frequency bands, 4.90 to 5.65 GHz and 4.50 to 5.00 GHz, respectively. The phase noise of the two VCOs is lower than -130 dBc/Hz at 3 MHz. The power consumption of the two VCOs is 1.4 mW.

3.6 Filtering Technique to Lower LC Oscillator Phase Noise [41,42].

In [41], the role of the current source in the oscillators is explained in depth. Recall the Eq. (33), the noise factor F can be expressed as :

$$F = 1 + \frac{4\gamma IR}{\pi V_0} + \gamma \frac{4}{g} g_{mbias} R \quad (67)$$

where γ is the channel noise coefficient of the FET (equal to 2/3 for long-channel FET, and larger than that for shorter channels), I is the bias current, and g_{mbias} is the transconductance of the current-source FET. According to the analysis, the third part of Eq. (67) contributes 75% of the F . In another word, about 75% of the total phase noise is contributed by the tail current bias noise. Furthermore, only two mechanisms in the current source affect the phase noise. The current-source transistors injecting thermal noise around the second harmonic of the oscillation is due to the first mechanism. The second one is the loading of the resonator by the differential-pair FETs in triode mode. For the first mechanism, a high impedance at the tail at around second harmonic can prevent the loading of the resonator. Based on this comprehension, a narrowband circuit to filter out the thermal noise caused by the current source transistors is proposed. Fig. 3.12 shows the schematic of the proposed design.

In Fig. 3.12, a large capacitor is placed in parallel with the current source. The role of this capacitor is to short the noise frequencies around $2\omega_0$ to ground. The next step to improve the circuit is to insert an inductor between the current source and the tail. The inductor is chosen to resonate at a frequency of $2\omega_0$. The inductor provides the high impedance which is needed to prevent the noise injection. The capacitor together with the inductor is named "tail filter".

Fig. 3.12 VCO with noise tail filter.

VCO in Fig. 3.12 is implemented in 0.35- μm CMOS process with a voltage supply of 2.5 V and a tail current of 3.7 mA is consumed. Setting the central frequency to 1.2 GHz, the VCO exhibited a phase noise performance of -153 dBc/Hz at 3 MHz. For comparison, another VCO without the tail filter was implemented. According to the measurement results, the phase noise performance of the VCO with "tail filter" is 7 dB better than that of the VCO without "tail filter".

In [42], a VCO to verify the contributions of tail inductors and capacitors in the tail noise suppression was described (see Fig. 3.13 [42]). In the circuit, L_{flt} and C_{flt} served similar functions as the topology reported in [41]. L_{lf} is an off-chip inductor inserted between the source of M_{src} and the ground. The inductor degenerates M_{src} and reduces the power of the transistor noise current by the a factor of $|1 + jg_m\omega L_{flt}|^2$, where g_m

is the transconductance of M_{src} . Another off-chip capacitor C_{lf} is placed in parallel with C_{flt} to shunt the low-frequency noise generated by M_{src} to ground.

To verify the contributions made by the inductors L_{flt} and L_{lf} , The VCO in Fig. 3.13 is simulated in four cases. In first case, a "plain" VCO design, without on-chip LC filter, off-chip inductor and capacitor, is simulated. In the second case, the VCO is designed with on-chip filter (L_{flt}), but without off-chip inductor and capacitor. In the third case, only an off-chip inductor (L_{lf}) is implemented. In case four, both of the on-chip and off-chip inductors are used.

Fig. 3.13 A VCO with tail current noise filter.

Fig. 3.14 depicts the simulation results of these four cases. To compare the contributions of off-chip inductor and capacitor, VCO with an off-chip inductor and

VCO with an off-chip capacitor were simulated under the same conditions. The simulation results of phase noise are depicted as Fig. 3.15. From Fig. 3.15, it is obvious that an off-chip inductor is more efficient in noise suppression as compared

Fig. 3.14 Simulation results of phase noise for the four cases.

Fig. 3.15 Simulation results of phase noise for VCO with an off-chip capacitor and VCO with an off-chip inductor.

with having an off-chip capacitor. However, the contributions made by the off-chip capacitors cannot be denied because it can be very effective in some cases. Combining with on-chip filter system (L_{flt} and C_{flt}), the off-chip inductors (L_{lf}) and off-chip capacitors (C_{lf}) are able to suppress the dominating noise contribution of the tail current source, hence making them negligible. As a result, any other nonlinear mechanisms which can convert low-frequency noise into phase noise become less significant.

3.7 Design of 1.94-GHz CMOS Noise-Cancellation VCO [43].

In a VCO with a tail current source, any noise voltage presenting at the gate terminal of the tail transistor will be converted to noise current due to the transconductance function of a transistor. Based on this observation, a novel idea of "noise-cancellation" is proposed and the schematic is depicted in Fig. 3.16.

Connecting S_2 , R_1 converts a small fraction of the noise current to a noise voltage. The converted noise voltage is opposite in sign to the initial noise voltage at the gate terminal due to the property of M_1 . After sampling by R_1 , the noise voltage will be fed back to the gate terminal of M_1 through the common drain transistor M_2 . by selecting the value of R_1 and the dimension of transistor M_2 , noise cancellation can be achieved.

A simplified equation indicates the phase noise contribution made by different components of the conventional cross-coupled LC VCO:

$$I_{n,Total}^2 = I_{n,M1}^2 + I_{n,M4}^2 + I_{n,M5}^2 + \left(\frac{g_{m,M1}}{g_{m,M3}} \right) I_{n,M3}^2 \quad (68)$$

According to the Eq. (68), the main contributions of the total phase noise is from current source transistor M_1 , the cross-coupled transistors M_4 and M_5 , as well as the diode-connected transistor M_3 . According to the feedback of the proposed noise-cancellation VCO, these noise sources can be significantly reduced.

Fig. 3.16 1.94-GHz CMOS noise-cancellation VCO.

The VCO of Fig. 3.16 is fabricated in 0.35 μm standard CMOS process with a central frequency of 1.94 GHz. It achieves phase noise of -121.6 dBc/Hz at 500 kHz offset and a FOM of -186 dBc/Hz. The VCO core consumes 2.8 mA current with a supply voltage of 2.4 V.

Connecting S_1 , a conventional cross-coupled LC VCO without the cancellation feedback is attained. Comparing the proposed noise-cancellation VCO with the

conventional one, a phase noise improvement of 10 dB is noted at the central frequency. As this noise-cancellation structure is designed with an aim to lower the noise components, it can be applied with other techniques to get rid of AM-to-PM mechanism and achieve an even greater phase noise performance.

3.8 A 1.8 GHz LC VCO With 1.3-GHz Tuning Range and Digital Amplitude Calibration [44].

In [44], a LC VCO with 1.3-GHz tuning range and digital amplitude calibration is proposed. To achieve a wide tuning range, a switched capacitor array with small varactors is implemented in the LC tank. The schematic of the VCO core is depicted as Fig. 3.17.

Fig. 3.17 Simplified VCO core schematic.

The LC tank is composed of accumulation-mode MOS varactors and a switched capacitor array. The MOS varactors make continuous frequency tuning possible. Together, the LC tank is able to provide several tuning steps. The differential switches

shunt the capacitors in and out of the tank. As a result, the tuning range of the design is able to attain 73%.

However, amplitude fluctuations in wideband VCO lead to an unstable phase noise performance, which may subsequently deteriorate the performance of neighbouring blocks. Therefore, a digital amplitude calibration is inserted to the VCO, as shown in Fig. 3.18.

In Fig. 3.18, a programmable reference is set to the desired amplitude at the beginning. Then, the tank amplitude of the VCO is detected by the peak detector and compared with the reference. A digital state machine analyses the output of the comparator and decides whether or not to change the programmable bias current of the VCO. The power consumption of the digital amplitude calibration system can be neglected because the system is on only during the calibration process.

Fig. 3.18 Calibration-based amplitude control VCO.

The VCO in Fig. 3.18 is implemented in 0.18- μm CMOS process and with a central frequency of 1.8 GHz. A 73% tuning range is achieved. The VCO presents a phase

noise performance of -123.5 dBc/Hz at a 600-kHz offset while drawing 3.2 mA from a 1.5 V voltage supply.

3.9 A 900 MHz CMOS LC-oscillator with quadrature outputs [45].

Quadrature VCO can provide quadrature-phase outputs, which is extremely useful in single-sideband applications. In [45], a novel quadrature VCO is implemented via connecting two identical VCOs in a cross-coupled style.

Fig. 3.19 depicts the schematic of the 900 MHz CMOS LC quadrature oscillator. The basic building block of this design is the MOSFET LC oscillator, consisting a LC tank and a cross-coupled MOS pair. Coupling two identical VCOs via M3 and M4, the design can ensure that the oscillations can only co-exist when the two VCOs synchronize in quadrature. Therefore, quadrature outputs are achieved with phase angles of 0° at M2A, 180° at M1A, 90° at M2B, and 270° at M1B.

The circuit is fabricated in $1\ \mu\text{m}$ CMOS process, with 3 V supply voltage and 10 mA current. The oscillator maintains a linear frequency over a range of 120 MHz centered at 850 MHz, with a phase noise of -85 dBc/Hz at a frequency offset of 100 kHz.

The QVCO proposed in [45] has variable frequency and large output swing. This is in fact the first design based on the idea of coupling two identical oscillators together to generate quadrature outputs. Although the phase noise of the design is moderate due to the structure limitation and CMOS process, the idea itself is very concise and enlightening.

Fig. 3.19 Identical oscillators coupled for quadrature outputs.

3.10 A low-phase-noise low-phase-error 1.8 GHz quadrature CMOS VCO [46].

Based on [45], a low-phase-noise low-phase-error QVCO is proposed by [Error! Bookmark not defined.]. The schematic of QVCO proposed in [Error! Bookmark not defined.] is described as follows.

In Fig. 3.20, the frequency tuning varactors are omitted for readability (and identical components are named only once). Based on the idea proposed in [45], the QVCO in [Error! Bookmark not defined.] is also constructed by coupling two identical VCOs. The coupling between the two VCOs is realized by transistor M2 of each VCO. Transistor M2 is placed on the top of cross-coupled transistor M1, which generate the negative resistance. The main difference in [Error! Bookmark not defined.] is that the transistors M2 are in series with the M1 transistor, rather than in parallel. This change improves the phase noise performance by 10 dB to 20 dB for the same power supply. To optimized the performance, the width of M2 is five times as wide as that of M1.

The QVCO is fabricated in a standard 0.35 μm CMOS process. The tank factor Q is around 6 at the frequency of interest. The VCO is operated from 1.64 GHz to 1.97

Fig. 3.20 Low-phase-noise low-phase-error QVCO proposed in [47]

GHz, with supply voltage of 2 V and 25 mA current consumption. The phase noise is below -140 dBc/Hz at 3 MHz offset across the tuning range.

3.11 A 2 GHz, 17% Tuning Range Quadrature CMOS VCO with High Figure-of-Merit and 0.6o Phase Error [47].

In [Error! Bookmark not defined.], a bottom-series QVCO (BS-QVCO) is proposed. The proposed BS-QVCO is compared with parallel QVCO (P-QVCO) [45] and top-series QVCO (TS-QVCO) [Error! Bookmark not defined.] and BS-QVCO shows the best phase noise performance.

In [45], the coupling transistors M3 and M4 are in parallel with the current switch transistors M1 and M2. So, this parallel style is called P-QVCO. In [Error! Bookmark not defined.], the M2 coupling transistors are placed on the top of the M1 current switch transistors. This idea is motivated by the fact that coupling transistors in

the P-QVCO contribute largely to the phase noise. Connecting coupling transistors in series with switch transistors in a cascade fashion, the phase noise can be improved significantly. This design is known as top-series QVCO (TS-QVCO).

The reference [Error! Bookmark not defined.] presents an alternative way of connecting the coupling transistors (referred as M_{cpl}) and switch transistors (referred as M_{sw}) in series, i.e., the M_{cpl} is placed at the bottom of M_{sw} . This structure is called the bottom-series QVCO (BS-QVCO), and is depicted in Fig. 3.21.

Fig. 3.21 Bottom-series QVCO.

To compare the phase noise performance between the different VCO topologies, the author of [Error! Bookmark not defined.] proposed a variable α , defined as the ratio of the width (W_{cpl}) of transistor M_{cpl} to the width (W_{sw}) of transistor M_{sw} .

$$\alpha = \frac{W_{cpl}}{W_{sw}} \quad (69)$$

Simulations showed that when decreasing α of P-QVCO, the phase error quickly increased while the phase noise decreased greatly. In another word, the phase noise performance of P-QVCO can be improved at the expense of its phase-error

performance. Thus, when comparing the phase noise performance of P-QVCO versus S-QVCO, the same phase-error level should first be clarified. However, the overall phase/amplitude error is not easy to measure directly. As a result, a single-sideband (SSB) upconversion circuit is used to convert the phase/amplitude error into the ratio

Fig. 3.22 Block schematic of single-sideband (SSB) upconversion circuit.

of the wanted upconverted band to the unwanted image band (referred to as Image Band Rejection, IBR). A typical schematic of a single-sideband upconversion circuit is given in Fig. 3.22.

On the other hand, for series-QVCOs, the phase error does not vary with α . That is to say, the phase noise performance of BS-QVCO and TS-QVCO cannot be ameliorated by sacrificing the phase error target. The phase error acts as a design constant, which is solely determined by the mismatch between ideally identical components.

To compare BS-QVCO with P-QVCO and TS-QVCO, all three QVCOs were operated from 1.91 GHz to 2.27 GHz, with a supply voltage of 1.3 V and a biasing current of 16 mA. 0.35 μm standard CMOS process is used in the fabrication. The Q of the tank inductors are all of around 6 at the frequency of interest. Comparing P-

QVCO and BS-QVCO with the same IBR, the BS-QVCO showed better phase noise performance of 7.5 dB/Hz at 1 MHz offset than that of the P-QVCO and BS-QVCO yield a 6 dB/Hz better phase noise performance at 3 MHz offset than that of the TS-QVCO.

3.12 Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS [48].

In [Error! Bookmark not defined.], a method of design and optimizing VCO was reported, where a quadrature VCO is optimized and fabricated to verify the optimization condition.

Since the design specifications of VCOs trade-off with each other, one should have different strategies when aiming for different targets. When reciprocating between inductors and capacitors, some of energy is dissipated due to the resistance part of the tank. As a result, the power consumption of a VCO must be at least larger than the losses of the tank. The loss in the tank can be expressed as:

$$P_{loss} = RC^2 \omega_c^2 V_{peak}^2 = \frac{R}{L^2 \omega_c^2} V_{peak}^2 \quad (70)$$

According to Eq.(70), the power loss decrease linearly for lower tank resistance. If the inductance is increased, the power loss drops quadratically. As a result, if the VCO is designed aiming at achieving least power consumption, the series tank resistance should be minimized and the tank must be maximized.

The phase noise can be expressed using following equation [Error! Bookmark not defined.]:

$$S_{SSB} = F \frac{kT}{2P_{sig}} \frac{R^2}{L^2 \Delta \omega^2} = F \frac{kT}{V_{peak}^2} \frac{R^3}{L^2 \Delta \omega^2} \quad (71)$$

According to Eq. 71, to optimize the phase noise performance of the VCO, the tank inductance and tank amplitude ought to be maximized and the tank series resistance and capacitance is to be minimized. Table I tabulated the design strategy towards achieving low-power and low-phase-noise.

Table I
Low-power low-phase optimization summary

	Low power	Low phase noise
L	Maximize	Minimize
C	Minimize	Minimize
R	Minimize	Maximize

According to the proposed optimization conditions, a cross-coupled quadrature VCO is proposed and fabricated in 0.25 μm CMOS process. The schematic of the proposed QVCO is shown as Fig. 3.23:

Fig. 3.23 Quadrature VCO schematic proposed in [Error! Bookmark not defined.].

The lengths of the transistors are set to minimal length of 0.25 μm to achieve the maximum speed and minimal tank capacitive load. The frequency of the QVCO is from 1.72 GHz to 1.99 GHz, with a supply voltage of 2.5 V and biasing current of 7.8 mA. The phase noise is around -143 dBc/Hz at 3 MHz.

Chapter 4 Design of *Gm*-enhanced Colpitts VCO

4.1 Introduction

In this chapter, a novel *gm*-enhanced Colpitts VCO is proposed based on the former technical background. The proposed design offers a relaxed start-up requirement and larger tank amplitude. Also, it offers a better phase noise performance according to the simulation results. An increased negative conductance is accomplished as compared with the other five types of VCO.

The VCO proposed in the thesis is designed for a phase-locked loop (PLL). PLL is a key building block in many high-speed systems as it accurately generates desired frequency tones. Inside the PLL, the voltage-controlled-oscillator (VCO) is the main block that generates the tone at a specific frequency which is tunable by a control voltage. The central frequency of 1.8 GHz of the proposed VCO is designed to meet the design specifications of PLL. The process used in the thesis is Global Foundry 0.13- μ m standard CMOS process. To meet the frequency specification of 1.8 GHz, the inductance of the inductor should be around 2.5 nH. Considered a pervasive inductor Q used in common VCO design and the library limitation, the inductor of C75N4W6S2-30K is chosen in this research. With a frequency of 1.8 GHz, the inductor presents a Q of 9. The supply voltage is also limited by the library. The supply voltage of Global Foundry 0.13- μ m standard CMOS process is 1.5 V.

4.2 Proposed *Gm*-enhanced Differential Colpitts VCO

Based on the differential Colpitts VCO structure, a gm -enhanced differential Colpitts VCO is proposed in this section and Fig. 4.1 depicts the schematic.

Fig. 4.1 Schematic of the proposed gm -enhanced differential Colpitts VCO.

Transistors M_{cs1} , M_{cs2} , M_{cs3} collectively construct the current source, C_b is used to block the extra noise from the current source, M_1 and M_2 realize the tail current switching mechanism mentioned in Section 3.1, and M_3 - M_4 are the gm -enhanced transistors. According to [39], coupling signal from the source to gate terminal of a transistor can enhance the effective transconductance, to relax the start-up requirement of the Colpitts oscillator. In addition, due to the in-phase relationship between the source and drain voltage, the gate can be alternatively connected to the drain of the transistor.

As seen in Fig. 4.1, instead of directly connecting the gates of M_3 and M_4 to the biasing voltage, the gate of M_3 is joined to the drain of M_4 and the gate of M_4 to the drain of M_3 . Such connection allows M_3 and M_4 to be self-biasing, requiring no biasing resistor. In addition, the cross-coupled structure of M_3 and M_4 can further increase the transconductance of the VCO as well as the tank amplitude and overall small signal loop gain. As a result, a better phase noise performance and a lower start-up current can be expected.

To have more insight into the proposed gm -enhanced differential Colpitts VCO and to derive proofs for its better performance as compared with the differential Colpitts VCO, its small-signal model has been drawn and analysed. The small-signal model of the proposed gm -enhanced differential Colpitts VCO is given in Fig. 4.2.

According to Fig. 4.2, the following equations can be written:

$$\begin{cases} (V - V_x)sC_1 + (-V - V_x)g_{m3} = I & (72) \\ V_x \cdot 2sC_2 + (-V_x)g_{m1} = I & (73) \end{cases}$$

Fig. 4.2 Small-signal model of the gm -enhanced differential Colpitts VCO.

From Eqs. (72) and (73), the small-signal admittance looking into the drain of M_3 of the gm -enhanced differential Colpitts VCO can be written as:

$$Y_{inE} = \frac{I}{V} = \frac{(sC_1 - g_{m3})(2sC_2 - g_{m1})}{2sC_2 - g_{m1} + sC_1 + g_{m3}} \quad (74)$$

where, g_{m3} is the transconductance of M_3 , and g_{m1} is the transconductance of M_1 .

The real part of Y_{inA} is

$$R_e[Y_{in}]_E = -\frac{(2g_{m3}C_2 + g_{m1}C_1)(C_1 + 2C_2)\omega^2 - g_{m3}g_{m1}(g_{m3} - g_{m1})}{\omega^2(C_1 + 2C_2)^2 + (g_{m3} - g_{m1})^2} \quad (75)$$

Assuming $g_{m3} = g_{m1}$,

$$R_e[Y_{in}]_E = -g_{m1} = -g_{m3} \quad (76)$$

Recall the Eq. 60, $|R_e[Y_{in}]_E| - |R_e[Y_{in}]_B|$ can be calculated.

$$|R_e[Y_{in}]_E| - |R_e[Y_{in}]_B| = \frac{\omega^2[4g_{m3}C_2^2 + g_{m1}C_1C_2] - g_{m3}g_{m1}(g_{m3} - g_{m1})}{\omega^2(C_1 + 2C_2)^2 + (g_{m3} - g_{m1})^2} \quad (77)$$

Since $\omega^2[4g_{m3}C_2^2 + g_{m1}C_1C_2] \gg g_{m3}g_{m1}(g_{m3} - g_{m1})$,

$$|R_e[Y_{in}]_E| - |R_e[Y_{in}]_B| > 0. \quad (78)$$

Assuming $g_{m3} = g_{m1}$,

$$\frac{R_e[Y_{in}]_E}{R_e[Y_{in}]_B} = 1 + 2 \frac{C_2}{C_1} \quad (79)$$

If $C_2 = C_1$,

$$\frac{R_e[Y_{in}]_E}{R_e[Y_{in}]_B} = 3 \quad (80)$$

It is obvious that the negative conductance generated in the proposed gm -enhanced differential Colpitts VCO is augmented when compared with the differential Colpitts VCO. If $g_{m3} = g_{m1}$ and $C_1 = C_2$, the negative conductance can be increased by three times. As a result, the biasing current required to ensure a reliable start-up is reduced. Also, the tank amplitude is increased and a better phase noise performance can be expected.

Table II shows the negative conductance of six types of VCO. It is obvious that the proposed VCO is able to vastly boost the gm most.

Table II
Negative conductance (s)

NO.	VCO Type	Negative
A	Single-end Colpitts VCO	$-1/4 g_m$
B	Conventional differential Colpitts VCO	$-1/3 g_m$
C	Gm -boosted differential gate-to-source feedback	$-3/8 g_m$
D	Gm -boosted differential Colpitts VCO	$-3/4 g_m$
E	Proposed Gm -enhanced differential Colpitts VCO	$-g_m$
F	Conventional cross-coupled LC VCO	$-1/2 g_m$

The maximum attainable amplitude of the cross-coupled structure is [46] :

$$A_{max} = \frac{1}{1-n} (V_{DD} - V_{dsat}) \quad (81)$$

The saturation voltage is defined using average values of the gate and source voltages. As a result, the potential drawback of this cross-coupled structure is that a large V_{dsat} limits the maximum amplitude for the VCOs.

The impact of C_{gs3} and C_{gs4} to the proposed design is analyzed as follows. According to Fig. 4.1, C_{gs3} and C_{gs4} is in parallel with C_1 . According to Eqs. 79,

$$R_e[Y_{in}]_E = (1 + 2 \frac{C_2}{C_1}) R_e[Y_{in}]_B \quad (82)$$

$$\text{where, } R_e[Y_{in}]_B = -\frac{1}{3} g_m.$$

C_{gs3} and C_{gs4} 's parallel connection with C_1 leads to a change to the expression $R_e[Y_{in}]_E$:

$$R_e[Y_{in}]_E = (1 + 2 \frac{C_2}{C_1 + \Delta C_{gs}}) R_e[Y_{in}]_B \quad (83)$$

$$\text{If } C_2 = C_1, R_e[Y_{in}]_E < 3.$$

As a result, $R_e[Y_{in}]_E$ decreases if take C_{gs3} and C_{gs4} are taken into consideration.

However, compare with the 2-pF capacitor C_1 , the effect of C_{gs} is minimal and can therefore be neglected.

The capacitors used in the thesis are MIM capacitors. The varactors used in the Chapter 4 and Chapter 5 are based on the model of Global Foundry 0.13- μ m standard

CMOS process. The name of the varactor model is NMOSVAR_1p5v_rf, with a capacitance of 0.773 p, a width of 4 μm and a length of 0.13 μm .

The choice of parameter is described as follows. Among all the components in proposed VCO, the sizing of M1 and M2 is of the most significance. According to the selected tank inductors and varactors, the tank resistance can be evaluated according to the parameter of Global Foundry 0.13- μm CMOS process. Based on calculation, the tank resistance is around 12 $\text{m}\Omega$. The oscillator theory indicates that the oscillator should generate a negative resistance to compensate the tank resistance. Following the conclusion drawn in Chapter 4, the negative resistance of the proposed VCO is equal to $-g_m$. As a result, the proposed VCO should yield a g_m of 12 mS , e.g. the transistors M1 and M2 should present a g_m of 12 mS ., following the following equation:

$$g_m = \sqrt{2\mu C_{ox} \left(\frac{W}{L} \right) I_d} \quad (84)$$

where, I_d is chosen as 3 mA (considering the gain of satisfied phase noise performance), μC_{ox} are constant parameter which depends solely on process. As a result, the W/L ratio can roughly be estimated as 1/300. Refined by simulation, the W/L ratio of the M1 and M2 is finally decided at 0.2 $\mu/60\mu$.

According to Eq. 82, the negative conductance of the proposed VCO is only related to the ratio of the C_2/C_1 , not the absolute value of C_1 . To avoid the fabrication deviation of the capacitors, C_1 is set to a relatively large value, which is 2 pf in thesis.

The parameters of the proposed VCO and the conventional ones are tabulated in Table III. Since all of the three VCOs are based on the same parameter setting, only one set of parameters are presented here.

Table III
Parameters of the proposed differential Colpitts VCO

Component name	Model name (GF 0.13- μ m)	Value	W/L
L	C75N4W6S2_30K	2.54 nH	NA
Cvar	NMOSVAR_1p5v_rf	0.773 pf	4 μ /0.13 μ
Ctune	MIM_DM	120 ff	5.1 μ /5.1 μ
C1	MIM_DM	2 pf	44.275 μ /44.275 μ
C2	MIM_DM	1 pf	44.275 μ /44.275 μ
Cb	MIM_DM	2.25 pf	66.605 μ /66.605 μ
M3&M4	RFNFET_1P5_DW	NA	0.13 μ /90 μ
M1&M2	RFNFET_1P5_DW	NA	0.2 μ /60 μ
Mcs1	NMOS_1P5	NA	1 μ /400 μ
Mcs2& Mcs3	NMOS_1P5	NA	1 μ /200 μ

4.3 Simulation Results

To compare the performances of conventional cross-coupled LC VCO, differential Colpitts VCO and the proposed *gm*-enhanced differential Colpitts VCO, circuits in Fig. 2.19, Fig. 2.21 and Fig. 4.1 are simulated using Cadence SPECTRE, based on the 0.13 μ m standard CMOS process. The two tank inductors each have a quality factor of 9. The supply voltage is 1.5 V. The tanks of the three VCOs are constructed with the same varactors and inductors for fair comparisons. Only C_{tune} is changed in each VCO

to tune the central frequency to 1.8 GHz. The channel length of the NMOS varactors is optimized to maximize the quality factor while maintaining a good tuning range.

We first biased the three VCOs using the same biasing current, i.e., 3 mA, to compare the phase noise performances. The phase noise characteristics of the three VCOs are presented in Fig. 4.3.

Fig. 4.3 Phase noise at 1MHz of three VCOs, with biasing current set at 3 mA.

The phase noise of three VCOs at different offset frequency is tabulated as Table IV.

Table IV
Phase noise (dBc/Hz)

VCO Type	Offset Frequency (Hz)		
	100k	1M	3M
Conventional Colpitts VCO	-104.9	-125.3	-134.9
Differential Colpitts VCO	-106.5	-126.9	-136.5
Proposed <i>gm</i>-enhanced differential Colpitts VCO	-107.3	-128.8	-138.6

Table V shows the tank amplitude of the three VCOs discussed versus their respective biasing currents. As can be seen, the proposed *gm*-enhanced differential Colpitts VCO exhibits amplitudes that are larger than the other two VCOs when the biasing current is varied from 1 mA to 5 mA.

Table V
Tank amplitude (mv) (peak to peak)

VCO Type	Biasing Current				
	1 mA	2 mA	3 mA	4 mA	5 mA
Conventional cross-coupled	308.5	677.4	1008.8	1310.2	1602.0
Differential Colpitts	NA	566.0	835.1	1319.2	1670.4
<i>Gm</i>-enhanced differential Colpitts	309.4	753.8	1125.0	1466.0	1768.8

The phase noises of the three VCOs versus the respective biasing current are tabulated in Table VI. After changing the biasing current from 1 mA to 5 mA, the proposed *gm*-enhanced differential Colpitts VCO is seen to be able to yield a better phase noise performance over the other two VCOs. As seen in Table IV, the conventional cross-coupled LC VCO has a phase noise of -125.3 dBc/Hz at 1 MHz offset while the differential Colpitts VCO attained -126.9 dBc/Hz at 1 MHz offset, and hence a better performance than the conventional one. The proposed *gm*-enhanced

differential Colpitts VCO, however, has the best phase noise performance among the three, achieving a phase noise of -128.9 dBc/Hz at 1 MHz offset.

Table VI
Phase noise (dBc/Hz)

VCO Type	Biasing Current				
	1 mA	2 mA	3 mA	4 mA	5 mA
Conventional cross-coupled	-116.9	-122.5	-125.3	-126.3	-127.1
Differential Colpitts	NA	-122.7	-126.9	-129.3	-130.9
Gm-enhanced differential Colpitts	-119.0	-125.7	-128.9	-130.5	-131.6

Fig. 4.4 Phase noise and tank amplitude versus biasing current.

To have a better insight of the proposed gm -enhanced differential Colpitts VCO, the three oscillators are operated at 1.8 GHz, and varying with biasing current only.

The phase noise at 1 MHz offset is given in Fig. 4.4. The tank amplitude changing with biasing current is also drawn in the same graph.

In Fig. 4.4, the tank amplitude of gm -enhanced differential Colpitts VCO is larger than the other two VCOs. Due to this increased tank amplitude, a better phase noise performance can be achieved. This has been verified by the simulation results. In addition, we also observed that the differential Colpitts VCO call for a 2 mA biasing current to start-up, while the gm -enhanced differential Colpitts VCO requires only 1 mA, which is comparable to the conventional cross-coupled LC VCO. As explained above, this improvement is attributed to the two cross-coupled pairs that help to increase the transconductance of the VCO, hence relaxing the start-up condition.

The proposed gm -enhanced VCO has been compared with other reported design. The following table tabulates the comparison.

Table VII shows that the proposed gm -enhanced differential Colpitts VCO has a state-of-art phase noise performance and a quite good FOM compared with other reported designs.

Table VII
VCO performance comparison

VCO	Power (mW)	Supply (V)	Freq. (GHz)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)	Tech. (μm)
[36]	10	2.5	1.8	-127@1MHz	-182.1	0.18
[38]	7.2	2.0	1.8	-128@1MHz	-184.5	0.18
[47]	1.8	2.67	2.0	-103@100kHz	-182.3	0.18
Cross-coupled LC tank	4.5	1.5	1.8	-125.3@1MHz	-183.9	0.13
Differential Colpitts	4.5	1.5	1.8	-126.9@1MHz	-185.5	0.13
Proposed VCO in this work	4.5	1.5	1.8	-128.9@1MHz	-188.5	0.13

Frequency pushing measures the changing of output frequency corresponding to a given change in the supply voltage at a fix tuning voltage (expressed in MHz/V). To validate how the frequency pushing effect can impact the performance of the proposed VCO, the supply voltage was swept from 1.35 V and 1.65 V to evaluate how the output frequency response. Considering the parasitic capacitance of the circuit layout, the proposed VCO is designed to oscillate at around 2 GHz during schematic simulation. The following figure presents the changes of output frequency corresponding to the supply voltage. The output frequency of the proposed VCO with supply voltage changing from 1.35 V to 1.65 V is plotted as Fig. 4.5.

According to Fig. 4.5, the output frequency of the proposed VCO changes merely by 2 MHz when the supply voltage is varied from 1.35 V to 1.65 V. Therefore, the proposed VCO presents a superior stable output frequency even though the supply voltage is prone to fluctuations.

Fig. 4.6 Output frequency of the proposed VCO with supply voltage changing from 1.35 V to 1.65 V.

Fig. 4.5 Output waveform of the proposed VCO with a supply voltage of 1.35 V (90% of the supply voltage).

To validate that the proposed VCO can still work when V_{dd} is as low as 90% of the designed supply voltage, a transient simulation and a phase noise simulation were performed with a supply voltage of 1.35 V. The proposed VCO presents phase noise performance of -126.97 dBc/Hz, with a decrease of 1.83 dBc/Hz, which is acceptable. The output wave form is given in Fig. 4.6.

Corner simulations, including fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF), were conducted to demonstrate that the proposed VCO can work properly with process variations. The phase noise performance of the proposed VCO under FF, SS, FS, SF are tabulated in Table VIII.

Table VIII
Phase noise performance of the proposed VCO under process variations

Corner Simulation	Phase Noise of proposed VCO (dBc/Hz)
Fast-fast	-124.54
Slow-slow	-124.06
Fast-slow	-126.58
Slow-fast	-125.96

As evident in Table VIII, the proposed VCO can work properly during all corner simulations. Although the phase noise performance is degraded, it is still within the acceptable range.

To validate the performance of the proposed VCO against temperature variation, the VCO is operated with temperature varying from -20°C to 120°C. The simulation result shows that the temperature variation has little impact on the performance of the

proposed VCO. With the temperature changing from -20°C to 120°C , the phase noise fluctuated within a range of 1.3 dBc/Hz, and is acceptable. The phase noise variation with temperature is plotted in Fig. 4.7.

Fig. 4.7 Phase noise performance of the proposed VCO changing with temperature variation.

4.4 Post-layout simulation results.

To validate the performance of the proposed *gm*-enhanced differential Colpitts VCO, the layout of the proposed design of Fig. 4.1 was drawn, together with layout of the conventional cross-coupled LC VCO (Fig. 2.19). The layout is based on Global Foundry $0.13\text{ }\mu\text{m}$ standard CMOS process. Six metal layers are used and the common centroid approach was taken into consideration. To achieve $50\text{ }\Omega$ output matching and to convert differential outputs into a single output to simplify measurement, a buffer was also designed. The schematic of the designed buffer is shown as follows.

Fig. 4.8 Schematic of buffer of proposed design and conventional VCO.

The layout of the two VCOs and their buffers are presented in Fig. 4.9. The tank amplitude and phase noise performance of the two VCOs are simulated in post-layout simulation. The layout area (without pads) of proposed VCO is 0.216 mm^2 . The layout area (without pads) of the conventional cross-couple LC VCO is 0.211 mm^2 .

Fig. 4.9 Layout of proposed gm -enhanced differential Colpitts VCO and conventional cross-coupled LC VCO and their buffers.

Same as schematic simulation, the two VCOs operates at 1.8 GHz, with 1.5 V supply voltage and 3 mA biasing current. The output waveform of the proposed gm -enhanced differential Colpitts VCO is plotted as Fig. 4.10.

Fig. 4.10 Post-layout simulation of output waveform of gm -enhanced differential Colpitts VCO.

When biased with 3 mA current, the peak-peak tank amplitude of the proposed gm -enhanced differential Colpitts VCO is about 905 mV. The output waveform of the conventional cross-coupled LC VCO is plotted as Fig. 4.10 and when biased with 3 mA current, the peak-peak amplitude of the conventional cross-coupled LC VCO is about 870 mV. This is smaller than that of the gm -enhanced differential Colpitts VCO. Since an enhanced tank amplitude can improve phase noise, a better phase noise performance can be expected in the gm -enhanced differential Colpitts VCO.

Fig. 4.11 Post-layout simulation of output waveform of conventional cross-coupled LC VCO

The phase noise performance of the proposed gm -enhanced differential Colpitts VCO and conventional cross-coupled LC VCO is simulated in post-layout simulation. The results are plotted as Fig. 4.12. The post-layout simulation results of phase noise performance are summarized in Table IX.

Table IX
Post-layout simulation of phase noise (dBc/Hz)

VCO Type	Offset Frequency (Hz)		
	100k	1M	3M
Conventional Colpitts VCO	-103.1	-124.7	-134.3
Proposed gm-enhanced differential Colpitts VCO	-106.2	-126.8	-136.2

According to the post-layout simulation results, the phase noise of the two VCO designs are degraded by about 2 dBc/Hz each as compared to the simulation results,

this is acceptable. The phase noise performance of proposed gm -enhanced differential Colpitts VCO in fact, is still better than that of the conventional Colpitts VCO.

Fig. 4.12 Post-layout simulation of phase noise.

Chapter 5 Design of *gm*-enhanced differential Colpitts Quadrature VCO

5.1 Introduction

VCOs that can provide quadrature outputs are referred as Quadrature VCO (QVCO). Due to the popularity of the direct conversion architecture, QVCO has attracted increasing attention especially. This is it plays a key role in direct conversion transceiver and permits low power, low cost and single-chip transceiver.

The Quadrature signals can be generated by three design methods. The first method is to connect the outputs of a non-quadrature VCO to a polyphase filter (or R-C C-R filter), and some output buffers or limiters as used in [48]. However, the buffers consume a lot of power and the filter increase the tank capacitance, leading a larger power dissipation and poorer phase noise performance. The second method is to deploy a frequency divider after to VCO, to achieve oscillation at double the frequency of interest. However, extra circuit, i.e. frequency divider increases the power consumption of the whole system. The third approach is to connect two identical VCOs in cross-coupled style to generate the quadrature VCO outputs [46]. In the following part, a novel QVCO based on the third method is proposed and simulated.

5.2 Proposed *gm*-enhanced differential Colpitts Quadrature VCO

Based on the *gm*-enhanced differential Colpitts VCO proposed in Chapter 4, a *gm*-enhanced differential Colpitts quadrature VCO (QVCO) is proposed in this chapter. Fig. 5.1 shows the schematic of the proposed design.

Fig. 5.3 Phase noise of the proposed Colpitts QVCO (lower curve) and conventional Colpitts QVCO, with biasing current set at 4 mA.

The phase noise of the proposed Colpitts QVCO and conventional Colpitts QVCO are provided as Table X.

Table X
Phase noise (dBc/Hz)

VCO Type	Offset Frequency (Hz)		
	100k	1M	3M
Conventional Colpitts QVCO	-102.7	-128.4	-138.9
Proposed gm-enhanced differential Colpitts QVCO	-108.0	-132.4	-142.6

According to Table X, operating at 1.8 GHz with 4 mA biasing current and 2 V supply voltage, the conventional Colpitts QVCO yields a phase noise of -128.4 dBc/Hz at 1 MHz offset. The proposed Colpitts QVCO has a phase noise of -132.4 dBc/Hz at 1 MHz offset, which is 4 dBc/Hz better than that of the conventional Colpitts QVCO. For the offset frequency 100K Hz and 3M Hz, the phase noise of

proposed Colpitts QVCO is 5.3 dBc/Hz and 3.7dBc/Hz better than that of the conventional Colpitts QVCO, respectively.

To illustrate the amplitude enhancement achieved by the *gm*-enhanced structure, the tank amplitude (peak to peak) of proposed Colpitts QVCO and conventional Colpitts QVCO is simulated, with biasing current changing from 2 mA to 7 mA. The simulation results are shown in Fig. 5.4.

Fig. 5.4. Tank Amplitude (peak to peak) of proposed Colpitts QVCO (higher curve) and conventional Colpitts QVCO, with biasing current changing from 2mA to 7mA.

With the biasing current changed from 2 mA to 7 mA, the tank amplitudes of the proposed Colpitts QVCO and the conventional Colpitts are summarized in Table XI.

Table XI
Tank amplitude (V)

VCO Type	Biasing Current					
	2mA	3mA	4mA	5mA	6mA	7mA
Conventional Colpitts QVCO	0.550	0.984	1.380	1.697	1.907	2.040
Proposed Colpitts QVCO	0.632	1.053	1.446	1.737	1.970	2.154

According to Fig. 5.4 and Table XI, the tank amplitude of the proposed Colpitts QVCO is larger than that of the conventional Colpitts QVCO with biasing current changing from 2 mA to 7 mA. Since phase noise of VCO is inversely proportion to the tank amplitude, the increased tank amplitude can result in better phase noise performance.

To demonstrate the superior performance of the proposed Colpitts QVCO, the two QVCOs are operated at 1.8 GHz, with biasing current changing from 2 mA to 6 mA. The phase noise at 1 MHz offset frequency of the two QVCOs is simulated and shown as Fig. 5.5.

Table XII gives the detailed data of the phase noise of proposed Colpitts QVCO and conventional Colpitts QVCO at 1 MHz offset, with biasing current changing from 2 mA to 6 mA.

Table XII
Phase noise (dBc/Hz)

VCO Type	Biasing Current				
	2mA	3mA	4mA	5mA	6mA
Conventional Colpitts QVCO	-124.6	-127.4	-128.4	-130.7	-132.7
Proposed <i>gm</i>-enhanced Colpitts QVCO	-126.7	-128.3	-132.4	-134.0	-134.0

Fig. 5.5. Phase noise of proposed Colpitts QVCO (lower curve) and conventional Colpitts QVCO at 1 MHz offset, with biasing current changing from 2 mA to 6 mA.

According to Fig. 5.5 and Table XII, the phase noise of proposed Colpitts QVCO is better than that of the conventional Colpitts QVCO when biasing current changing from 2 mA to 6 mA with central frequency of 1.8 GHz and 2 V supply voltage. The proposed gm -enhanced differential QVCO is compared with several typical reported design. The results of comparison is tabulated as follows.

Table XIII
QVCO performance comparison

VCO	Power (mW)	Supply (V)	Freq. (GHz)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)	Tech. (μm)
[49]	0.9	1.8	2.2	-117@1 MHz	184	0.18
[50]	5.17	1	2.18	-140@20 MHz	180	0.18
[51]	4	1.8	2.45	-126@1 MHz	188	0.18
[52]	14.4	1.2	2.33	-130.4@3 MHz	-187.3	0.18
[38]	8.6	2	1.85	-127@1 MHz	-183.2	0.18
Proposed QVCO	8	2	1.8	-132.4@1 MHz	189.1	0.18

According to the Table XIII, the proposed *gm*-enhanced differential Colpitts VCO has superior FOM over the other state-of-art QVCOs.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

This report presents a novel gm -enhanced differential Colpitts VCO and a quadrature VCO. The central frequency of the proposed VCO and QVCO is 1.8 GHz. For the gm -enhanced differential Colpitts VCO, the Q of tank inductors is set to 9 and the supply voltage is 1.5 V. For the gm -enhanced differential Colpitts quadrature VCO, the tank inductors have a Q of 10. The supply voltage of the proposed QVCO is 2 V. The gm -enhanced topology is able to lower the start-up biasing current and enhance the tank amplitude. This has been verified by the improvement of the phase noise performance of the proposed VCO and QVCO in simulations and also the post-layout simulations.

To support the theoretical background of the work, the oscillator theory and general VCO design considerations have been reviewed. Three typical VCO topologies, that is, the ring oscillators, LC oscillators and Colpitts oscillators, are explained in depth. With a focus on the gm -boosted VCOs, the mainstream VCO topologies have been reviewed thoroughly. In addition, each of the negative conductance of gm -boosted VCOs has been calculated. According to calculation, the negative conductance of the proposed VCO has been improved as compared to five VCOs. The five VCOs are: single-end Colpitts VCO, conventional differential Colpitts VCO, gm -boosted differential gate-to-source feedback Colpitts VCO, gm -boosted differential Colpitts VCO, and the conventional cross-coupled LC VCO. The design of proposed gm -enhanced differential Colpitts VCO and QVCO has been discussed in details. The simulation and post-layout simulation results have been provided.

The simulation results proved that when biased at 3 mA, the proposed *gm*-enhanced differential Colpitts VCO can achieve a phase noise of -128.9 dBc/Hz at 1 MHz offset. Under the same condition, the phase noise of the conventional cross-coupled LC VCO is -125.3 dBc/Hz at 1 MHz offset and the phase noise of the differential Colpitts VCO is -126.9 dBc/Hz at 1 MHz offset. In another word, the phase noise performance of the proposed design is 3.5 dBc/Hz better than that of the conventional cross-coupled LC VCO and 1.9 dBc/Hz better than that of differential Colpitts VCO. According to the post-layout simulation results, the proposed *gm*-enhanced differential Colpitts VCO has a 2.1 dB/Hz better phase noise performance than that of the conventional cross-coupled LC VCO.

Based on the *gm*-enhanced topology, *gm*-enhanced differential Colpitts QVCO was also been proposed and simulated. Biasing with 4 mA current, the proposed QVCO presents a phase noise performance of -132.4 dBc/Hz, which is 4 dBc/Hz better than that of the conventional Colpitts QVCO.

6.2 Future Work

Due to the development of the RF technologies and the increasing stringent requirements on oscillators, researches towards more stable oscillation behaviour, better phase noise performance, more relaxed start-up biasing current will continue.

The following possible future work can be conducted to improve on the present work. A verification of the simulation results has to be conducted whereby the two proposed designs, i.e., the *gm*-enhanced differential Colpitts VCO and QVCO must be taped-out. For comparison, the *gm*-enhanced differential Colpitts VCO, conventional cross-coupled LC VCO, and the conventional Colpitts QVCO can be taped-out together. Furthermore, the phase error of the two QVCOs should be measured and

evaluated. Since direct measurement of the phase error is extremely difficult and challenging, a single-sideband (SSB) up-conversion circuit can be included.

Ultra-wide frequency range VCO is continuously being developed due to the vast applications of the variable inductors. Focusing on low power and wide band, VCOs using variable inductors can also be explored in the future work.

List of Publication

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