Analysis, design, and implementation of digital dc-dc converters

Foong, Huey Chian

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ANALYSIS, DESIGN, AND IMPLEMENTATION OF DIGITAL DC-DC CONVERTERS

FOONG HUEY CHIAN

School of Electrical and Electronic Engineering

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Abstract

The trend of pushing signal processing into the digital domain has penetrated into the analog-dominated power management ICs such as DC-DC converters. Researchers from academics and industries have been looking into the core of DC-DC converter, i.e. the controller or compensator, and redesigning it in digital domain to achieve more superior performance. With the continual evolution of CMOS technology and reducing of supply voltage, digital DC-DC converters have the advantages of high signal-to-noise ratio, programmability, and portability while maintaining high efficiency.

This thesis describes the analysis, design, and realization of digitally-controlled (or digital) DC-DC converters. The digital DC-DC converters are targeted for the power management IC for power-critical devices such as portable devices, energy harvesting applications and wireless sensor networks.

To achieve accurate voltage regulation, a high resolution, supply- and process-insensitive 12-bit DPWM is proposed for digital DC-DC converters. The DPWM is realized by a counter and a ring oscillator-multiplexer segmented tapped delay line or hybrid-segmented architecture. The ring oscillator of the segmented tapped delay line is made insensitive to supply and process variation by biasing the differential delay cells with a supply-insensitive replica bias circuit. Using GlobalFoundries CMOS 0.18 μm process models, the simulation results show that the variation of the switching frequency of the DPWM at 1.03 MHz is 0.4% for supply voltage variation between 1.5 V and 2.5 V and 0.95% over the temperature range from -40°C to 90°C . Monte-Carlo simulation was also performed to account for the effect of mismatch between the transistors of the ring oscillator. The worst case delay of the delay cells is 0.87% for $\pm 5\%$ ($3\text{-}\sigma$) mismatch. This design achieves higher resolution and reduces power consumption and area compared to

the prior arts. The design was fabricated in CMOS 0.18 μ m process and the DPWM achieved a supply sensitivity of 0.82% and a current consumption of 14 μ A.

A windowed successive approximation (SAR) analog-to-digital converter (ADC) using an ultra-fast, offset-cancelled auto-zero comparator is proposed for digital DC-DC converters. The ADC has a dynamic reference voltage range to reduce power consumption. The auto-zero scheme of the comparator is realized internally with a preamplifier stage and a latch stage. Post-layout simulation shows that the response time of the comparator from low-to-high and high-to-low is 3.78 ns and 2.47 ns respectively. The resolution of the proposed windowed SAR ADC is 7.5 mV. The ADC is fabricated in standard CMOS 0.18 μ m process and as part of a digital DC-DC converter integrated circuit. Measurement results show that a low power consumption of 0.8 μ W is achieved.

This thesis also presents an integrated digital DC-DC converter with a predictive and feedforward controller, the aforementioned DPWM and the windowed SAR ADC to achieve fast transient response and low overshoot. An additional predictive or jerk component is introduced to the conventional PID controller to speed up the transient response and reduce the settling time by approximately 50%. This predictive term is based on the second derivative of the error signal and introduces zero to the loop response which leads to increased bandwidth and improved phase margin. In addition, a feedforward control is also employed to further improve the transient by evaluating the change in the inductor current during the on and off time of the power transistors. Theoretical analysis and simulations were carried out to analyze the proposed design and algorithm. The proposed design is verified on silicon with a prototype of a digital DC-DC converter fabricated in CMOS 0.18 μ m process. The digital DC-DC converter achieved a settling time of 4 μ s and an overshoot of 15 mV for a step-load transient of 450 mA, which are improved significantly as compared to the prior arts.

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Part I

Introduction and Literature Review

Chapter 1

Introduction

1.1 Motivation

This thesis presents an integrated digitally-controlled or digital DC-DC converter with fast transient response and low overshoot. The digital DC-DC converter could be used in the application of portable electronic devices such as handphones, laptops, mp3 players and e-readers. The motivation of the project is to design a DC-DC converter that has programmable output, optimal response, high accuracy, and efficiency. Compared to linear regulators, DC-DC converters offer higher efficiency over a wider load range. Therefore, they could be employed in a variety of applications that involve mode transition and active load variation.

Traditionally, DC-DC converters are analog-controlled by embodying feedback with analog circuits such as opamps and passive components. However, an analog DC-DC converter has limitations because the opamps have fixed bandwidth and thus the performance is sufficient but never optimal. Furthermore, the controller has to be redesigned every time technology changes. With a digital controller, the DC-DC converter can achieve better performance by using sophisticated control algorithms without physical limitations.

Digital DC-DC converters offer several distinct features such as programmability, flexibility, and portability (Dancy et al., 2000, Wei and Horowitz, 1996, Roh, 2005). Furthermore, it is relatively easier to design advanced control algorithms with digital approach

to achieve optimal transient performance (Trescases et al., 2008, Shirazi et al., 2009, Corradini et al., 2008a). By integrating the digital DC-DC converter onto the IC chip, the switching frequency can be higher and this relaxes the output filter requirements of the power stage, potentially leading to significant simplifications in the complexity of the package and PCB power distribution networks.

The implemented multimode digital DC-DC converter combines the predictive and feedforward control with the conventional PID controller to achieve fast transient response and low overshoot. An additional predictive or jerk component is added to the conventional PID controller to speed up the transient response and reduce the settling time by approximately 50%. This predictive term is based on the second derivative of the error signal and introduces zero to the loop response, which leads to increased bandwidth and improved phase margin. In addition, a feedforward control is also employed to further improve the transient by evaluating the change in the inductor current during the on and off time of the power transistors. Theoretical analysis and simulations were carried out to analyze the proposed design and algorithm. The proposed design is verified on silicon with a prototype of a digital DC-DC controller fabricated in CMOS 0.18 μm process. The digital DC-DC converter achieved a settling time of 4 μs and an overshoot of 15 mV for a step-load transient of 450 mA, which are improved significantly as compared to the prior arts.

1.2 Objectives

The overall objectives of this thesis pertain to design and implement a high performance digital DC-DC converter with CMOS 0.18 μm process. The digital DC-DC converter can be targeted for the power management block for energy harvesting and wireless applications such Wireless Body Area Network (WBAN). In view of the ultimate objective, the specific objectives are:

1. Propose a digital DC-DC converter with dual-mode (PWM/PFM) operation to boost the efficiency over a wider load range. The digital DC-DC converter should also achieve a low quiescent current. The developed DC-DC converter must be designed to meet the requirements of a power management module with a maximum load current of 500 mA.

2. Propose a digital DC-DC converter that features fast transient response and low overshoot under a low voltage process. The digital DC-DC converter should also achieve high accuracy.
3. Propose a high resolution, process- and temperature-insensitive digital pulse width-modulator (DPWM) to achieve the high accuracy requirement of the digital DC-DC converter.
4. Physically realize by means of a prototype IC, a fast-transient, low-overshoot digital DC-DC converter, thereby providing an experimental means to verify the proposed predictive and feedforward control algorithm, and to verify the high resolution, process- and temperature-insensitive DPWM.

1.3 Contributions

The contributions of this project pertain to the design of a high performance digital DC-DC converter in terms of transient response, accuracy, line and load regulation. The specific contributions are

1. Developed a high resolution 12-bit DPWM that is process- and temperature-insensitive. The variation of the switching frequency of the DPWM at 1.02 MHz is 0.4% for supply voltage variation between 1.5 V and 2.5 V and 0.95% over the temperature range from -40°C to 90°C.
2. Designed and implemented a low power windowed successive approximation ADC for the digital DC-DC converter. The developed ADC has an internal compensated ultra-fast comparator to reduce the delay effect of the ADC to the digital DC-DC converter.
3. Designed and implemented an integrated digital DC-DC converter with a predictive and feedforward control. The digital DC-DC converter achieved a settling time of 4 μs and an overshoot of 15 mV for a step-load transient of 450 mA.
4. Designed an alternative noise-reduction ADC. The proposed ADC adopts a robust VCO and a sixth-order delta-sigma modulation to attenuate the phase noise and output ripples of the digital DC-DC converter.

5. Developed a digital DC-DC converter that achieves adaptive optimization based on genetic algorithm (GA). The digital DC-DC converter achieves optimal transient response within four generations and 200 μ s.
6. Developed a digital DC-DC controller based on distributed arithmetic (DA) algorithm to achieve hardware saving of approximately 50%.

1.4 Thesis Organization

This thesis is organized into eight chapters. The first chapter gives an introduction of the Ph.D. project including the motivation, objectives, and contributions. The second chapter reviews the DC-DC converters, introduces the fundamental of digital controlled power systems, compares analog and digital power systems, and reviews modeling and design approaches for digital controlled power converters.

The third chapter presents a high-resolution 12-bit DPWM which is insensitive to supply and process variation. The proposed DPWM is implemented using a differential ring oscillator in a hybrid-segmented topology. This solution is very robust and occupies a smaller silicon area than other reported designs of equivalent resolution.

The fourth chapter presents a low power windowed SAR ADC for digital DC-DC converters. A windowed ADC works within a specific input voltage range, as opposed to full-range ADC. Specifically, the input of the ADC in a digital DC-DC converter is the error signal derived from the difference between the output voltage and the reference voltage. Therefore it does not generally require a full-range ADC. By constraining the quantization range, power consumption can be significantly reduced. Besides, this eliminates the need of a dedicated sample-and-hold circuit. Thus, the proposed ADC also achieves very low power consumption, which leads to a high efficiency DC-DC converter. In addition, an auto-zero comparator with offset-cancellation is proposed to resolve the offset issue in the design of the SAR ADC.

by chopper modulation to boost its SNDR and linearity. Besides, this $\Sigma\Delta$ ADC architecture has a small IC area and low power consumption.

The fifth chapter addresses the problems of dynamic response and complexity with the introduction of a digital DC-DC converter adopting a predictive controller to enhance

the transient performance. The proposed digital controller is based on a novel predictive+feedforward+PID (PFPID) approach to achieve fast settling time and limited overshoot of the integrated DC-DC buck converter during load transient. The PFPID control is realized by combining the predictive and feedforward control with the conventional PID control. The predictive control is based on the second derivative of the error signal and introduces zero to the loop response which leads to increased bandwidth and improved phase margin. To limit the overshoot, the feedforward control is implemented by evaluating the change in the inductor current during the on and off time of the power transistors within a switching cycle. The proposed design has a simple architecture, which leads to a small IC area. Theoretical analysis is further verified on silicon with a prototype of a digital DC-DC converter fabricated in the CMOS 0.18 μm process.

The sixth chapter presents a genetic algorithm controller that investigates optimization of the DC-DC converter in the time domain in terms of the integral of time and absolute error (ITAE). This approach eliminates the need of calibration and reduces the time-to-market. This is made feasible by estimating the model using a state estimator and updating it on-the-fly. Based on the model determined, the proposed genetic algorithm is then being run to achieve optimization by reducing the cost function.

The seventh chapter presents a DC-DC controller based on distributed arithmetic (bit-serial) approach to circumvent the power, IC area and start-up problems. Distributed arithmetic has several advantages over the parallel approach due to its inherent scalability and memory reuse. This will allow the digital controller to operate in different operating modes such as Pulse Frequency Modulation (PFM), Pulse Width Modulation (PWM), pulse-skipping and adaptive control while the same memory is shared and reloaded for different operating modes.

Finally, the last chapter gives a conclusion to the thesis on the design and realisation of a superior performance integrated digital DC-DC converter.

Chapter 2

Literature Review

This chapter provides the background and a literature review of switched-mode DC-DC converters. As a preamble, the review commences with the different types of regulators, and the parameters that are commonly used to qualify a DC-DC converter or switched-mode power supply are presented.

2.1 Overview of DC-DC Converters

Research on DC-DC converters can be traced back to thirty years ago when the analog DC-DC converter was first modelled and analyzed in California Institute of Technology around 1977 to 1978 due to the tremendous efforts made by Slobodan Cuk, R. D. Middlebrook, and other pioneers in an attempt to overcome the low-efficiency problem faced by linear regulators (Middlebrook and Cuk, 1977b). Since then, DC-DC converters have been flourishing in the power management IC market due to their higher efficiency, even though linear regulators are relatively easier to implement. There are essentially three types of DC-DC converters, categorized according to the relative voltage of the input and output, namely, the buck converter, the boost converter and the buck-boost converter. Commercial DC-DC converters are typically analog, which means that they are controlled by analog controllers. Digital DC-DC converters have been conceptualized rather recently and they include the introduction of dedicated digital controller ICs. Since these products have only been around for the past few years, they

Figure 2.1: The linear regulator

have not even achieved a 10% market penetration into the overall power supply market. Nevertheless, they have been made possible mainly due to the advance of semiconductors and the reduction of supply voltage. This chapter reviews the following topics: (1) Classes of regulators, (2) Specifications of DC-DC converters, (3) Fundamental theory of DC-DC converters, (4) Modelling of DC-DC converter, (5) Analog controlled DC-DC converters, (6) Digital controlled DC-DC converters, (7) Design methodology of digital controller, (8) Prior arts of digital DC-DC converters, (9) Prior arts of ADC, and finally, (10) The prior arts in digital pulse-width modulators.

2.2 Classes of Regulators

This section reviews three types of regulators, namely (i) the linear regulator, (ii) the switched capacitor or charge pump regulator, and (iii) the switched-mode DC-DC converter.

2.2.1 Linear Regulator

The linear regulator, as depicted in Figure 2.1, is the earliest solution to the three types of regulator. It typically consists of a high-gain amplifier with a negative feedback. The pass transistor at the output operates in the active region rather than as a switch. A stable voltage reference, V_R , is generated through a bandgap reference and fed to the

non-inverting input of the amplifier, and thereafter it is compared with the output voltage scaled by resistors R_1 and R_2 . The whole system forms a shunt-series feedback loop, and $V_o = (1 + R_1/R_2) * V_R$.

Assuming the quiescent current is negligible, such that $I_{in} = I_o$, the ideal efficiency of a linear regulator can be expressed as:

$$Efficiency, \eta (\%) = \frac{V_o}{V_{in}} \times 100 \quad (2.1)$$

Primarily, the linear regulator has low efficiency, especially when the dropout voltage ($V_{in} - V_o$) is large. Since V_o has to be lower than V_{in} , it can only achieve step-down conversion. If the input voltage drops below a certain threshold, the regulation will be lost and the output will sag below the nominal regulation point.

To achieve low dropout voltage, some commercial linear regulators adopt PMOS as pass transistors. These regulators are generally named as LDO, which stands for low-dropout regulators. These low dropout regulators can achieve high efficiency if the regulated output voltage V_o gets very close to V_{in} . However, there is a limit of $V_{in} - V_{out} > V_{eff}$ to keep the pass transistor in saturated region. (e.g. $V_{in} = 1.8$ V and $V_{eff} = 0.3$ V, the maximum efficiency = $1.5/1.8 = 83\%$). To achieve a greater efficiency, other means of energy conversion such as switched-mode DC-DC converter have to be explored.

In addition to good line and load regulation, state-of-the-art LDOs also exhibit high power-supply-rejection (PSR) that attenuates high frequency supply noise, such as (Patel and Rincon-Mora, 2010). The design is a current-mode LDO that achieves high PSR by increasing the impedance to the supply with a current sampling feedback loop.

A linear regulator is relatively simple to implement. However the major drawback is that the efficiency scales roughly with the ratio of output and input voltage (V_o/V_{in}). As technology development pushes the supply voltage even lower, the supply voltage will pose a challenge in the design of linear regulators. Replacing a linear regulator with a switching regulator for better efficiency is therefore necessary in many cases.

2.2.2 Charge Pump or Switched Capacitor Converter

The second type of regulator is the switched capacitor (SC) converter. Figure 2.2 depicts a typical SC or charge pump power converter. By charging and discharging

Figure 2.2: The switched capacitor converter

the capacitor C_1 in complementary phases, $CLK+$ and $CLK-$, the output capacitor maintains at an output voltage V_o close to $2V_{in}$, therefore it is also known as a voltage doubler.

The operating principle is as follows: During the $CLK+$ phase, the upper plate of the C_1 is connected to V_{in} , while the lower plate is connected to ground. During the $CLK-$ phase, the capacitor C_1 is connected between V_{in} and the intermediate output, V_{o1} , thus boosting the output voltage to $2V_{in}$. To have better regulation and reduce switching noise, the charge pump is generally succeeded by a LDO to generate the final output voltage V_o . It should be noted that $CLK+$ and $CLK-$ must be non-overlapping clock signals to prevent short-circuit current, thereby reducing the power loss.

The same topology can be used as a step-down converter by reversing the direction of power flow. Typically, SC converter can provide moderate output current. It is also used to generate negative output voltage by inverting the nodes of the output capacitor. SC converter is regulated by an LDO or by charge pump modulation circuitry. If it is regulated by an LDO, the drawback is that the efficiency of the switched capacitor converter is also related to the input and output voltage ratio, thereby resulting in low efficiency. In the other case, if it is regulated by charge pump modulation, the switched capacitor regulator has an output resistance described as:

$$R = \frac{a^2}{2fC} \quad (2.2)$$

where C is the value of the capacitor, a is the charge multiplier of capacitor, and f

Figure 2.3: The switched-mode DC-DC converter

is the switching frequency. This output impedance reduces the efficiency of the SC converter. Note that large capacitor arrays are needed to reduce the output impedance to achieve high efficiency.

State-of-the-art integrated switched-capacitor converters aim at achieving high efficiency and high power density with a wide range of output voltage levels. An example is (Le et al., 2010). The design adopts interleaving of clock phases to boost efficiency.

2.2.3 Switched-mode DC-DC Converter

The third type of regulator is the switched-mode DC-DC converter. Switched-mode DC-DC converters are available in many topologies and buck, boost, and buck-boost are fundamentally the simplest. DC-DC converter offers the highest efficiency among the three types of regulators and can generate high output current. Theoretically, the power efficiency is 100% for DC-DC converter. In practice, however, the physical losses of the components limit its efficiency to around 90%. The primary disadvantages of DC-DC converters are the presence of output ripple and switching noise at the output. They are also generally more expensive, due to the fact that they require an external inductor and capacitor. However, recent technological advances push the converter towards higher switching frequencies to reduce the cost and physical sizes (form factor) of the capacitor and inductor. The basic switched-mode dc-dc converters are shown in Figure 2.3, which consists of buck, boost, and buck-boost converters. In Figure 2.3, SW represents the switching signal while the controller is not shown.

State-of-the-art DC-DC converters achieve optimized system performance over a wide range of operating conditions. An example is (Morrone et al., 2009). The design employs

2.3 Specifications of DC-DC Converters

Table 2.1: Comparisons among the three types of regulators

	Linear Regulator	Switched Capacitor Converter	DC-DC Converter
Advantages	Simple Reliable Inexpensive	Moderate efficiency and cost	Variety (step-down or step-up) High efficiency (80% ~ 98%)
Disadvantages	Only step-down Low efficiency	Slow response	Complex Costly
Applications	Low current and input voltage Suitable for sensitive circuit	Medium current operation	High current and input voltage

continuous monitoring of the system frequency response to minimize the errors between the desired and actual crossover frequency and phase margin to achieve good stability and transient performance.

For the remaining of this thesis, the focus will only be on buck converters. To summarize, Table 2.1 lists the pros and cons of the three types of regulators.

2.3 Specifications of DC-DC Converters

2.3.1 Efficiency

Efficiency is defined as:

$$Efficiency(\%) = \frac{Output\ Power}{Input\ Power} \times 100 \quad (2.3)$$

Efficiency is generally measured across different load current and line voltage.

2.3.2 Switching Frequency

This is the fundamental frequency at which the DC-DC converter operates. It is typically the frequency of the pulse-width modulation (PWM) signal.

2.3.3 Line Regulation

When the input voltage is changed from rated maximum to rated minimum while the outputs are at full load, the output voltage will also change. Line regulation is the percentage change in output voltage when the input is varied.

2.3.4 Load Regulation

When the output load is changed from maximum rated current to minimum rated current, the output voltage changes. Load regulation is the percentage change in output voltage. For multiple output supplies, each output is measured while the loads are varied.

2.3.5 Output Ripple

Output voltage ripple refers to the phenomenon where the output voltage rises during the on-state and falls during the off-state. Several factors contribute to the output ripple including the switching frequency, the output capacitance and inductance, load and line current, and any current limiting features of the control circuitry. At the most basic level the output voltage will rise and fall as a result of charging and discharging of the output capacitor.

2.3.6 Dynamic Response

When a load is applied, the output voltage momentarily exceeds its final value. This overshoot is the dynamic response. It is a measure of the converters high frequency output impedance. This specification is generally more important than the settling time of the output, which is also known as the transient response time.

2.4 Modelling of DC-DC Converters

Modelling is the representation of physical circuits by mathematical means. For a power converter, it is desired to design a feedback system such that the output voltage is regulated accurately, and is insensitive to disturbances in input voltage or in the load current. In addition, the feedback system should be stable, and properties such as transient overshoot, settling time, and steady-state regulation should meet specifications. To design a system with the aforementioned requirement, we need a dynamic AC model of the switching power converters.

The basic concept to predict AC behavior is to average the converter waveforms over one switching cycle. Therefore, the desired DC and low frequency AC components of waveforms should be exposed. Since switching power converters are nonlinear systems, by perturbing and linearizing the average model about a quiescent operating point, small-signal linearized models could be constructed.

There are two well-known variants of AC modelling method, state-space averaging, and circuit averaging. Averaged switch modelling as an extension of circuit averaging is also widely used in many applications.

2.4.1 State-Space Averaged Model

The state-space averaging technique generates the low-frequency, small-signal AC equations of switched-mode DC-DC converters (Erickson and Maksimovic). Converter transfer functions and equivalent circuit models can thus be obtained. The converter contains independent state variables such as inductor current and capacitor voltage, which form the state vector, $x(t)$, and the converter is driven by independent sources that form the input vector, $u(t)$. The output vector, $y(t)$, contains the dependent signals of interest. During the first subinterval when the switches are in position 1 for time dT_s , the converter reduces to a linear circuit whose equations can be written in the following state-space form:

$$\frac{dx(t)}{dt} = A_1x(t) + B_1u(t) \quad (2.4)$$

$$y(t) = C_1x(t) + E_1u(t) \quad (2.5)$$

The matrices A_1 , B_1 , C_1 , and E_1 describe the network connections during the first subinterval. The duty cycle, $d(t)$, becomes a time-varying quantity. During the second subinterval, the converter reduces to another linear circuit, and the state space equations are:

$$\frac{dx(t)}{dt} = A_2x(t) + B_2u(t) \quad (2.6)$$

$$y(t) = C_2x(t) + E_2u(t) \quad (2.7)$$

The matrices A_2 , B_2 , C_2 and E_2 describe the network connections during the second subinterval, of length $(1 - d)T_s$. It is assumed that the natural frequencies of the converter network are much smaller than the switching frequency. This assumption coincides with the small ripple approximation, and is usually satisfied in well-designed converters. It allows the high-frequency switching harmonics to be removed by an averaging process. In addition, the waveforms are linearized about a DC quiescent operating point. The converter waveforms are expressed as quiescent values plus small AC variations, as follows:

$$y(t) = Y + \hat{y}(t) \quad x(t) = X + \hat{x}(t) \quad u(t) = U + \hat{u}(t) \quad d(t) = D + \hat{d}(t) \quad (2.8)$$

The state-space averaged model that describes the quiescent converter waveforms is:

$$0 = AX + BU \quad (2.9)$$

$$Y = CX + EU \quad (2.10)$$

where the averaged matrices are:

$$A = DA_1 + (1 - D)A_2 \quad (2.11)$$

$$B = DB_1 + (1 - D)B_2 \quad (2.12)$$

$$C = DC_1 + (1 - D)C_2 \quad (2.13)$$

$$E = DE_1 + (1 - D)E_2 \quad (2.14)$$

The steady-state solution of the converter is:

$$X = A^{-1}BU \quad (2.15)$$

$$Y = (-CA^{-1}B + E)U \quad (2.16)$$

The state equations of the small-signal AC model are:

$$K \frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + (A_1 - A_2)X + (B_1 - B_2)U\hat{d}(t) \quad (2.17)$$

$$\hat{y}(t) = C\hat{x}(t) + E\hat{u}(t) + (C_1 - C_2)X + (E_1 - E_2)U\hat{d}(t) \quad (2.18)$$

The quantities $\hat{x}(t)$, $\hat{u}(t)$, $\hat{y}(t)$, and $\hat{d}(t)$ are the quiescent operating point. These equations describe how the small AC signal variations excite variations in the state and output vectors.

2.4.2 Circuit Averaging Model

The circuit averaging technique also yields equivalent results, but the derivation involves manipulation of circuits rather than equations. Switching elements are replaced by dependent voltage and current sources, of which the waveforms are defined to be identical to the switch waveforms of the actual circuits. This leads to a circuit having a time-invariant topology. The waveforms are then averaged to remove the switching ripple, and perturbed and linearized about a quiescent operating point to obtain a small-signal model.

To be specific, usually the switches in converters can be represented by two-port network with terminal waveforms $v_1(t)$, $i_1(t)$, $v_2(t)$, and $i_2(t)$. With any two-port network, two of these terminal quantities can be treated as independent inputs to the switch network. The remaining two can be viewed as dependant signals. For example, for a boost converter depicted in Figure 2.4, the switch network is replaced with two-port network with independent sources as inductor current $i_1(t)$ and output voltage $v_2(t)$, as shown in Figure 2.5, which correctly represent the dependent output waveforms of the switch network.

Figure 2.4: Boost converter example

Figure 2.5: Replace the switches with independent network

The next step is the averaging circuit. A basic assumption is made such that the natural time constants of the converter are much longer than the switching period, and thus the converter contains low-pass filtering of the switching harmonics. The converters are averaged over the switching period T_s to remove the switching harmonics, while preserving the low-frequency components of the waveforms. Therefore, if the switch dependent waveforms are averaged and the duty cycle are taken into account, the resulting circuit is shown in Figure 2.6. $d'(t)$ represents $1-d(t)$ from the operation of the boost converter. The model in Figure 2.6 is still nonlinear since the dependent source involves the multiplication of $d(t)$, the inductor current, $i_1(t)$, and output voltage, $v_2(t)$. The network can be linearized by perturbing and linearizing the converter waveforms

Figure 2.6: Averaged switch model

Figure 2.7: Linearized circuit-averaged converter model

about a quiescent operating point, assuming:

$$d(t) = D + \hat{d}(t) \quad (2.19)$$

$$d'(t) = D' - \hat{d}(t) \quad (2.20)$$

$$\langle v_g(t) \rangle_{Ts} = V_g + \hat{v}(t) \quad (2.21)$$

$$\langle i(t) \rangle_{Ts} = \langle i_1(t) \rangle_{Ts} = I + \hat{i}(t) \quad (2.22)$$

$$\langle v(t) \rangle_{Ts} = \langle i_2(t) \rangle_{Ts} = V + \hat{v}(t) \quad (2.23)$$

$$\langle v_1(t) \rangle_{Ts} = V_1 + \hat{v}_1(t) \quad (2.24)$$

$$\langle i_2(t) \rangle_{Ts} = I_2 + \hat{i}_2(t) \quad (2.25)$$

From Equations (2.19) to (2.25), the model contains both DC and small signal AC terms. Since the small signal assumption is satisfied, the high-order term such as $\hat{v}(t)\hat{d}(t)$ can be neglected. Then the linearized model is obtained in Figure 2.7. The dependent generator is replaced with an ideal transformer, as in Figure 2.8. Figure 2.8 shows the complete circuit-averaged model, which functions simultaneously as the DC and the small signal equivalent circuits for the boost converter. This model-derived procedure suggests that, only the replacing of the switch network with its averaged model is needed to obtain a small-signal AC converter model. This procedure is called averaged switch modeling.

Figure 2.8: Final linearized circuit-averaged converter model

Figure 2.9: Analog controlled buck feedback model

2.5 Analog-controlled DC-DC Converters

A typical electronic system requires a feedback circuit to stabilize the system and improve the operating characteristics. Analog-controlled DC-DC converters realize the feedback or the controller using analog circuits such as operational amplifiers and other passive devices, such as resistors and capacitors. The models of the power stages derived in Section 2.5 are used to design the controller.

A block diagram of a typical analog-controlled buck small-signal model is shown in Figure 2.9. The output voltage is sensed with gain $H(s)$, which is usually a voltage divider. The sensed output $H(s)\hat{v}_o(s)$ is compared with V_{ref} to generate the error signal $\hat{v}_e(s)$. The objective of the feedback loop is to make $H(s)\hat{v}_o(s)$ equal to V_{ref} regardless of the load and line disturbances. That is to say, if the feedback system works perfectly, the error signal should be zero. To achieve small error signal here is one of the objectives of compensator network $G(s)$. $\hat{v}_c(s)$ is the control signal generated

by the compensator and is fed into the PWM to achieve the duty cycle gate signal for the drivers. Therefore, the system loop gain, $T(s)$, is defined in general as the product of the gains around the forward and feedback paths of the loop as:

$$T(s) = \frac{H(s)G(s)G_{vd}(s)}{V_M} \quad (2.26)$$

where the control-to-output transfer function, G_{vd} is:

$$G_{vd}(s) = \left. \frac{\hat{v}_o(s)}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{V_{in}}{LCs^2 + \frac{L}{R}s + 1} \quad (2.27)$$

The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output as long as adequate phase margin is maintained. Besides, stability and transient performance can be assessed using the phase margin test of loop gain. Specifically, the objective of compensation is to design the feedback network with suitable gain and phase delay to achieve a desirable bandwidth and sufficient phase margin, whereby the system achieves the desired steady state accuracy, transient response, relative stability, and insensitivity to change in system parameters.

There are several typical types of analog compensation consisting of an amplifier and RC network. Lead compensator is also known as the proportional-derivative (PD) controller, which is usually used to improve the phase margin in a system originally consisting of two poles. The possible shortcoming of PD compensation is that the PD compensator is sensitive to noise due to the derivative function.

Lag compensator (also known as proportional-integral, PI) is used to increase the low frequency loop gain, such that the output is better regulated at DC and at frequencies well below the loop crossover frequency. Combined PID compensator is to obtain both wide bandwidth and large DC loop gain for reduced steady-state error.

For the DC-DC converter, there are typically three types of analog controller: Type I, II, and III. For type I, the gain of the controller is:

$$Gain = \frac{1}{sR_1C_1} \quad (2.28)$$

Type I generally does not provide adequate phase margin for DC-DC converter. Type II is more common and its gain equation is:

$$Gain = \frac{1}{R_1C_1} \frac{s + \frac{1}{R_2C_2}}{s(s + \frac{C_1+C_2}{R_2C_1C_2})} \quad (2.29)$$

Figure 2.10: Three types of analog controller (a) Type I, (b) Type II, and (c) Type III

The type II controller has one zero and one pole and thus it is able to provide a 90° phase boost. In general, type II controller can achieve adequate phase margin for the loop response of the DC-DC converter. However, specific DC-DC converters will have different double pole and ESR zero frequencies. For systems with very low ESR of the inductor and capacitor, the phase will experience a very sharp slope downward at the double pole while the gain will have a rather high peak at the double pole. Systems that have such resonant output filters will be more difficult to compensate since the phase will need an extra boost to provide the necessary phase margin for stability. Systems such as this will typically need a type III compensation. The conventional type III PID compensator consisting of an operational amplifier and RC network is realized in Figure 2.10(c) and gain equation is:

$$Gain = \frac{R_1 + R_3}{R_1 R_3 C_1} \frac{(s + \frac{1}{R_2 C_2})(s + \frac{1}{(R_1 + R_3) C_3})}{s(s + \frac{C_1 + C_2}{R_2 C_1 C_2})(s + \frac{1}{R_3 C_3})} \quad (2.30)$$

It is observed that, at low frequency, the integrator pole in the same manner as the PI compensator leads to large low-frequency loop gain and accurate regulation of low frequency component. The type III network introduces two zeros to give a phase boost of 180° . The high frequency zeros prevent the switching ripple from the disturbance of the PWM.

2.6 Digital-controlled DC-DC Converters

Conventional controllers for DC-DC converters are based on duty ratio adjustment for voltage regulation, and most of the commercially available controller products are based on analog techniques. Even though the above-mentioned analog control techniques have

been matured, they are limited by sensitivity to noise and temperature, component parameter variation, and non-flexibility.

Digital controllers for switching power supplies offer a number of advantages as follows:

1. **Programmability, flexibility, and system interface.** In digital control, system parameters are programmable, and can be communicated between the controller and the system. In other words, it is easy to enable digital system interface for programming, diagnostics, monitoring, and other power management functions.
2. **Reusability and portability.** Based on digital control, a design could be reused which could make the entire system design faster and less expensive and reduce the time-to-market.
3. **Easy integration.** In digital control, it is easy to implement the design in custom ICs, taking advantage of the digital process scaling.
4. **New control techniques.** Digital control allows practical implementation of new control techniques such as non-linear control, system identification and auto-tuning.
5. **Reduced sensitivity to process variation.** In digital control, system performance is less sensitive to process variation, which makes digital control more robust.

A digital control system typically contains a sampler to detect continuous analog signal at discrete instances of time. Before a data hold is employed to reconstruct the original signal, a digital compensator block is added to improve system performance.

A commonly used method of data reconstruction is polynomial extrapolation. Using a Taylors series expansion, $e(t)$ can be expressed as:

$$e(t) = e(nT) + e'(nT)(t - nT) + \frac{e''(nT)}{2!}(t - nT)^2 + \dots \quad (2.31)$$

If the first term above is used, the data hold is called a zero-order hold (ZOH), which is expressed as $e_o(t) = u(t) - u(t - T)$. The corresponding transfer function is $G_{h0}(s) = \frac{1 - e^{-Ts}}{s}$, so the frequency response of the zero-order hold can be obtained

Figure 2.11: Frequency responses of ZOH

as $G_{h0}(j\omega) = T \frac{\sin(\pi\omega/\omega_s)}{\pi\omega/\omega_s} e^{-j(\pi\omega/\omega_s)}$, and response in frequency domain of ZOH is shown in Figure 2.11.

According to the Shannon sampling theorem, when the input signal is reconstructed, any frequencies $\omega > \omega_s/2$ will reflect into the frequency range $0 < \omega < \omega_s/2$. This effect is called frequency aliasing. The frequency aliasing can be prevented either by increasing ω_s or by placing an analog antialiasing filter in front of the sampler. The antialiasing filter is a low pass filter that removes any frequency components in $e(t)$ that is greater than $\omega_s/2$, since the low pass filters introduce phase lag. However, the cutoff frequency of the antialiasing filter cannot be made so low as to destabilize the control system.

Applying digital control theory to power converter, compared to analog-controlled system, the digital-controlled power converter is shown in Figure 2.12. The output voltage is sensed, and the sensed output $H(s)\hat{v}(s)$ is sampled by analog-to-digital converter (ADC). The digital sensed output is compared with the reference signal v_{ref} and thus digital error signal is generated. The digital compensator generates the duty cycle control signal according to the input error signal $\hat{v}(z)$ and feeds the control signals into PWM to get the drive signal to the power stage.

Figure 2.12: Digital controlled power converter feedback model

For the digital control loop, the loop gain can be expressed as:

$$T(s) = H(s)G(s)G_{vd}(s)G_{PWM}G_{ADC} \quad (2.32)$$

where $H(s)$ is the voltage divider, G_{ADC} are the gain of DPWM module, and G_{ADC} is the gain of of the ADC. The gain of the DPWM, $G_{PWM}(s)$ is:

$$G_{PWM}(s) = K_{PWM} \cdot e^{-sT_{PWM}} \quad (2.33)$$

where K_{PWM} is:

$$K_{PWM} = \frac{1}{2^{n_{PWM}} - 1} \quad (2.34)$$

The transfer function of the ADC is:

$$G_{ADC}(s) = K_{ADC}e^{-sT_{ADC}} \quad (2.35)$$

where K_{ADC} is:

$$K_{ADC}(s) = \frac{1 - 2^{-n_{ADC}}}{V_{max_{ADC}}} \quad (2.36)$$

Therefore, the DPWM and ADC introduce the gain changes to loop gain over the analog controller, which need to be considered when designing the digital compensator. Meanwhile, the sensitivity of the ADC, the inherent time delay of sampling or the transport delay, and the precision of the numerical value are some factors that will affect the performance of the system. It is, therefore, necessary to give careful consideration to ADC sampling frequency and resolution design.

Generally speaking, ADC resolution is determined by the precision requirements of power stages. Put differently, the least-significant-bit (LSB) value of ADC must be smaller than the minimum required output voltage resolution. The sampling frequency of ADC should generally be 10 or 20 times of system bandwidth to minimize phase delay due to sampling. DPWM acts as a digital-to-analog converter, and generates pulse width modulated switching waveforms for driving power stage switches. Since the discrete change in duty ratio due to the resolution of DPWM, there is a corresponding discrete change in output voltage. It is important that the value of the minimum output voltage change be smaller than the LSB size of the ADC to avoid limit cycle oscillation. Therefore, the DPWM resolution must be greater than the resolution of ADC. This will be further discussed in Chapter 3.

2.7 Digital Controller Design Methodology

In general, there are two design methods for the digital compensator or controller of the DC-DC converter: Digital redesign approach and direct digital design approach. In direct design approach the discrete model of sampled analog components is built. Then, the compensator design is done directly in z-domain including the accurate modeling of sampling functions. With the direct design, the frequency response techniques, such as gain margin and phase margin, can be used as well.

Digital redesign assumes the sampling frequency is much greater than the system crossover frequency so that the design equivalent approach is accurate. This approach first models the discrete components as analog components approximately, and then designs the analog controller with standard analog control technique. Finally, it maps the analog compensator into digital with equivalent mapping methods. Since the techniques of modeling power converter to linear continuous time domain are well known, this thesis will focus on the digital redesign approach. In general, there are three types of digital redesign approach: (1) Bilinear transformation, (2) Pole-zero mapping, and (3) Triangle hold.

Bilinear transformation (BLT) basically performs approximation to integral using the area of a trapezoid between points. It uses pre-warping to map the entire left-half s-plane to inside the unit circle. This perfectly maps the stability axis $j\omega$ to unit circle,

2.7 Digital Controller Design Methodology

and consequently, there is no aliasing. The basic procedures are first to select a critical frequency (e.g. relative to sampling, filter corner or system crossover frequency) ω_{crit} , and subsequently substitute it for s in $H(s)$ to determine $H(z)$:

$$H(z) = H(s) \Big|_{s = \frac{\omega_{crit}}{\tan(\omega_{crit}T/2)} \frac{z-1}{z+1}} \quad (2.37)$$

By employing bilinear transformation (BLT) the number of poles and zeros are equal. If number of poles is more than that of zeros, additional zeros at $s = \infty$ are mapped to $z = -1$, and they represent the highest frequency $f_s/2$ available in the z-domain. If the number of zeros is more than that of poles, additional poles at $s = \infty$ are mapped to $z = -1$, which creates problems in a compensator as it creates significant peaking as f approaches $f_s/2$. Since the BLT maps the entire left-half-plane (LHP) of the s-domain into the unit circle, there is no aliasing for the additional poles.

The Pole-Zero Mapping method maps all poles and finite zeros using the transformation pole or zero at $s = a$ using pole at $z = e^{-aT}$. If there are m more poles than zeros (e.g. zeros at $s = \infty$), then the m poles are mapped to $z = -1$. This requires the ability to apply the current input to the current output. Subsequently, the gain of the filter is determined such that the magnitude of $H(z)$ matches the magnitude of $H(s)$ at a critical frequency (such as the crossover frequency). However, the case when the number of poles and zeros are different must be taken into account. If the number of poles is more than that of zeros, additional zeros at $s = \infty$ are mapped to $z = -1$ and this represents the highest frequency $f_s/2$ available in the z-domain and is a reasonable mapping. However, if the number of zeros is more than that of poles, a direct pole-zero map of pole at $s = \infty$ is to $z = 0$. Therefore, these poles must be added to make the system realizable (causal). Mapping the poles to $z = 0$ represents a z^{-1} unit delay, which corresponds to an effective e_{sT} delay term in the s-domain transfer function. Alternatively, poles can be placed in the z-plane; this requires manual modification of pole/zero mapping. As an additional pole is moved from $z = 0$ to $z = -1$, peaking is introduced in the magnitude response.

Triangle Hold effectively extrapolates samples of the continuous time filter in a straight line, and solves for the z-transform of the samples as in the following equation: $H(z) = \frac{(z-1)}{T_z} Z\left(\frac{H(s)}{s_2}\right)$. Triangle hold always results in the same number of poles and zeros (same as the BLT), however, extra zeros are not mapped to $z = -1$.

2.8 Literature Review of Digital-controlled DC-DC Converter

A number of digital-controlled DC-DC converters have already been developed in the prior arts (Maksimovic and Zane, 2007, Hu et al., 2006, Patella et al., 2003, Carosa et al., 2008, Peng et al., 2004). Modeling and analysis of the digitally controlled DC-DC converters are presented together with the detailed digital circuit implementations (Patella et al., 2003, Carosa et al., 2008). In (Maksimovic and Zane, 2007), an exact small-signal discrete-time model for digitally controlled PWM DC-DC converters is derived and is well suited for directly digital design of digital compensators. In (Peng et al., 2004), the quantization effects in digitally controlled DC-DC converters are analyzed and modeled. The design considerations for avoiding limit-cycling oscillation are given. Some other digital-control techniques (Corradini et al., 2008b, Babazadeh et al., 2009, Yousefzadeh and Maksimovic, 2006, Shirazi et al., 2009, Morroni et al., 2009) focus on the performance improvements of digital DC-DC converters. Two examples are given below where the digital control techniques are implemented to achieve better performance in terms of high efficiency and robust control.

1. Efficiency: the efficiency of switched mode DC-DC converters depends mainly on the switching frequency, which is related to the switching losses, and the series resistances in the power path, which is related to the conduction losses. Normally, the efficiency of a converter is optimized by properly choosing switching frequency and power devices. In synchronous buck converters, another control parameter, dead time, which is defined as the time period when both the high side power MOSFET and the synchronous rectifier are off, also affects the efficiency and can be adjusted to optimize the system efficiency. Too long a dead time results in additional losses due to the body-diode conduction and the body-diode reverse recovery. Too short a dead time will result in simultaneous conduction of the high side power MOSFET and the synchronous rectifier and cause lower efficiency. In the presence of parameter tolerances, temperature variations and different operating points, the optimum dead times are not constant. In (Yousefzadeh and Maksimovic, 2006), a sensorless dead time optimization method is implemented

using digital control techniques. It is proved that the highest efficiency is corresponding to the smallest duty cycle command. In steady state, the dead time is swept from a large value to a small value and the best dead time can be found when the duty cycle command reaches the minimum value. This method takes advantage of the fact that the duty cycle command is directly available in the digital controller and all the parameters such as dead time and duty cycle command can be adjusted and stored precisely in the digital controller.

2. Robust control: in (Shirazi et al., 2009, Morroni et al., 2009), digital adaptive tuning techniques are introduced into switched mode DC-DC converters. The problem is related to the control feedback loops, which are typically designed conservatively so that closed loop regulation and stability margins are maintained over expected ranges of operating conditions and tolerances in power stage parameters. Typical designs often lead to degraded closed-loop performance or loss of stability in the event of significant operating point changes associated with component degradation, input voltage variations, etc. With the increased feasibility of practical digital control for high-frequency switching power converters, new opportunities exist to incorporate intelligent control algorithms into the system to simplify the system design and improve dynamic responses and reliability over a wider range of possible operating points. The approach is based on perturbation of the control signal, duty cycle command, and measurement of the output response. Based on the analysis of the information from the measured output, the system characteristic can be estimated and an autotuning algorithm can be used to modify the control parameters to achieve a stable and desired performance.

A typical digital-controlled synchronous buck converter is shown in Figure 2.13. It typically consists of four blocks, namely an analog-to-digital converter (ADC), a digital controller, a digital pulse-width modulator (DPWM), and a power stage consists of power transistors with gate drivers and output filter. The ADC is employed to sample the output voltage and convert it into a digital code for the controller. The controller then executes the control algorithm and produces a digital command for the DPWM. Based on the digital command, the DPWM generates a pulsewidth modulated (PWM) signal to drive the power transistors. The PWM signal is eventually filtered by the external low-pass filter to produce the output voltage.

Figure 2.13: Block diagram of a digital controlled synchronous buck converter

2.8.1 Analog-to-Digital Converter (ADC)

In a typical digital control system, the analog-to-digital converter (ADC) serves as an interface between the analog world and the digital world. It performs two main tasks on the signals, which need to be processed in digital controllers: sampling and quantization. In digital controlled DC-DC converters, ADC is usually used to sense the output voltage for the output voltage regulation. Two methods have been reported for the application in DC-DC converters: (1) flash ADC, and (2) ring-oscillator or ring ADC.

2.8.1.1 Flash ADC

Flash ADC uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. A 3-bit flash ADC is shown in Figure 2.14. The operating principles of the flash ADC is as follows. As the output voltage of the converter V_o crosses the reference of a comparator, the output state of the comparator is changed, which indicates the position of the output voltage. All comparators outputs are connected to a priority encoder. The priority encoder circuit is used to convert a thermometer codes to a 3-bits digital error signal for the digital compensator. The relation between comparator output codes (thermometer codes) and encoder output codes, $Y[n]$, is shown in Table 2.2. Finally, $Y[n]$ is subtracted from the reference codes to generate the error codes, $e[n]$.

Figure 2.14: Flash ADC circuit

Flash ADCs are extremely fast. However, there are some drawbacks. 2^n resistors and $2^n - 1$ comparators are needed in the design depending on the resolution, n . Thus, it occupies large IC area and consumes huge power. In addition, the resistors must be matched to achieve high accuracy.

Table 2.2: Priority encoder of the flash ADC

Comparator Outputs, $W_{[7:1]}$	Encoder Output, $Y_{[2:0]}$
0000000	000
0000001	001
0000011	010
0000111	011
0001111	100
0011111	101
0111111	110
1111111	111

Figure 2.15: Frequency-current dependency of a differential ring oscillator biased in subthreshold region

2.8.1.2 Ring ADC

The design of the ring ADC (Xiao et al., 2001) is based on the observation that the oscillation frequency in a CMOS ring oscillator, biased in subthreshold region, has a linear dependency on the bias current, as depicted in Figure 2.15. The block diagram of the ring ADC is shown in Figure 2.16. The ADC consists of a simple analog block and a synthesizable digital block. A differential transistor pair M1, M2 drives two identical ring oscillators as a matched load. The bias current is designed such that the voltage swing on the ring oscillator is below threshold. Thus frequency of the ring oscillators is linearly dependent on its supply current. The error voltage v_e develops differential current in the two branches that results in instantaneous differential frequency at the two oscillators. The frequency of each oscillator is captured by a counter that is reset at the beginning of each sampling cycle. At the end of the cycle, one counter output is subtracted from the other, and the result C_e is used to calculate digitized error voltage $e[n]$. Since there is uncertainty in the initial and ending phase, instead of looking at one output per ring, all the M taps on each ring oscillator are observed for frequency information. It can be shown that, ignoring quantization error and assuming good

Figure 2.16: Block diagram of ring ADC

linearity in the input differential pair, C_e is derived as:

$$C_e = Mk_1g_mT_{ADC}v_e \quad (2.38)$$

where M is the number of taps on each ring, k_1 is the ring oscillator frequency sensitivity function to bias current, g_m is the transconductance of the input differential pair, and T_{ADC} is the ADC sampling period, which equals the switching period T_s of the converter. Finally, digitized error voltage, $e[n]$ is calculated by rounding off C_e .

2.8.2 Digital Pulse Width Modulator (DPWM)

A Digital Pulse Width Modulator (DPWM) generates the PWM signal which is analogous to the conventional analog ramp-comparator pulse width modulation scheme. To prevent limit-cycling oscillation, the resolution of the DPWM must be higher than that of the ADC. Several methods to create DPWM have been reported, i.e. (1) Counter-comparator DPWM, (2) Ring-mux DPWM, (3) Hybrid DPWM, (4) Segmented DPWM, (5) Self-Calibrated Segmented DPWM, (6) Dual-Band Switching DPWM, (7) Heterogeneous DPWM, and (8) Feed-forward DPWM. They are reviewed in the following subsections.

Figure 2.17: Counter-comparator DPWM with timing diagram

2.8.2.1 Counter-comparator DPWM

The block diagram of the counter-comparator DPWM, as reported in (Wei and Horowitz, 1996), is depicted in Figure 2.17. The operating principles of the counter comparator DPWM can be explained as follows. At the beginning of each switching cycle, reset is asserted to initiate the counter at the zero state. The zero-state detector is used to detect the zero-state and generate a set signal for the PWM through the SR latch. When the clock signal arrives, the counter begins counting up. Subsequently, the counter counts until its code Q is equal to the reference code D . When $Q=D$, PWM is reset through the comparator. However, the counting process of counter continues until it reaches the final code (111..11) and the counter is reset. After that, a new switching cycle begins.

Counter comparator DPWM takes reasonable amount of die size but the power consumption reported is in the order of milliwatts because of the high clock frequency required for the counters. Therefore, it is only suited for low resolution of DPWM operation.

Figure 2.18: Block diagram of an N-bit ring-mux DPWM

2.8.2.2 Ring-MUX DPWM

To overcome the huge power consumption problem of counter-comparator, ring-mux DPWM was proposed in (Dancy and Chandrakasan, 1997). The block diagram of a ring-mux DPWM is shown in Figure 2.18. Essentially, the main sub-blocks of a ring-mux DPWM are $2^N - 1$ delay stages and a 2^N -to-1 MUX. The $2^N - 1$ differential delay stages will form 2^N taps. A square wave is generated and propagated in the delay stages. When the rising edge reaches the first tap, the PWM makes a transition from low to high. A duty ratio select signal will determine the corresponding input tap to be passed through to the output. The output will then reset the PWM signal. In this case, the switching frequency of the ring-mux DPWM will be equal to the frequency of the ring oscillator.

2.8.2.3 Hybrid DPWM

Since counter-comparator employs a fast clock, the power consumption is considerably high. On the other hand, ring-mux architecture is not area-efficient when the resolution is high as it requires long series of delay stages. Thus, the hybrid approach (Dancy et al., 2000) exploits the advantages of both the approaches by having a solution that can achieve high resolution while maintaining low power consumption. The block diagram of a hybrid PWM is depicted in Figure 2.19.

The operating principles of the hybrid DPWM is elaborated as follows. At the beginning

Figure 2.19: Block diagram of a hybrid DPWM

of each switching cycle, the counter is reset while the output DPWM signal is set. Next, the counter begins to count in coarse discrete steps. Once the counter determines the coarse (MSB) delay required for the DPWM, it initiates a pulse to the delay line instead of resetting the output of DPWM. The finer (LSB) delays of the delay-line are used for the higher resolution bits, and when the pulse has propagated through the selected number of delay cells, the output is reset. Hence, the pulse-width modulated signal is generated. By using this topology, the speed of the clock required for the counter is significantly reduced, as well as the total number of delay cells required for the delay line. Moreover, the clock required is reduced from $2^N \cdot f_{sw}$ to $2^{N_{msb}} \cdot f_{sw}$. For instance, an 8-bit counter comparator DPWM switching at 1 MHz requires a 256 MHz clock. However, if the three most significant bits (MSB) were resolved with a counter, while the rest are implemented with a delay line, the DPWM requires only a 8 MHz clock instead of a 256 MHz clock.

2.8.2.4 Segmented DPWM

A further improvement can be made on the delay-line based DPWM as reported in (Trescases et al., 2007). In the hybrid DPWM, the least significant bits (LSB) are resolved with a delay line, and the MSB bits are resolved using a counter. However, these MSB bits can also be resolved by a more coarse set of delay cells instead of a counter. By segmenting the delay lines, the overall area of the DPWM is much smaller due to the reduced size of the multiplexers. Figure 2.20 depicts the schematic of the segmented DPWM. The delay cells are binary weighted, thus they can be driven directly

Figure 2.20: Block diagram of a segmented DPWM

by the duty ratio digital input. The first MUX is selected through the MSB bits of the $D[n]$, since it is connected to the set of larger delay cells. Similarly, the second MUX is selected through the LSBs of $D[n]$, because it is connected to the set of smaller delay cells.

The advantage of segmenting the delay cells is that it can be realized with much smaller area than the delay lined DPWM. First of all, instead of having a big $2^N:1$ MUX, we logarithmically divide that into two or more MUXs which are much smaller in size than the original MUX. Furthermore, if the delay cells are binary-weighted, the number of total delay cells is much smaller. However, larger delay cells can also be made by stacking individual unit delay cells in series to achieve a delay of 4 units, 16 units etc. Since the delay of these cells depends on the number of unit delay cells stacked in series, the area of the total delay line remains the same as that of a tapped delay-line architecture.

2.8.2.5 Self-calibrated Segmented DPWM

A slightly different version of the segmented DPWM is the self-calibrated segmented DPWM (Trescases et al., 2005), as depicted in Figure 2.21. This version uses a voltage-controlled tunable delay cell such that each of the larger delays can be achieved by using the same delay cell with a different control voltage, thereby saving on the total area of the delay line. In addition, it uses a delay-locked loop to tune the delay such that the non-linear and non-monotonic effects due to delay mismatches are smaller. However,

2.8 Literature Review of Digital-controlled DC-DC Converter

Figure 2.21: Block diagram of a self-calibrated segmented DPWM

Figure 2.22: Dual band switching algorithm

it still requires the use of an external clock and suffers from the non-linear effects due to the multiplexer delay in the signal path of the delay line.

2.8.2.6 Dual-band Switching DPWM

A dual band switching control scheme (Chui et al., 2003) employs the tapped delay line technique. Essentially, a dual band switching control scheme divides the range from 0 to V_g (where V_g is the input voltage) into two regions, as shown in Figure 2.22. A new full range covers $2/3$ of V_g . The low band is from 0 to $2/3$ of V_g while the high band operates from $1/3V_g$ to V_g . To regulate the output voltage, a band selection signal, BC is used to select the appropriate range. As the digital word is assigned to a smaller operating region than the full range, its effective resolution is increased. Figure 2.23 depicts a 6-bit dual band switching PWM generator. The basis block of the PWM generator is a 32-stage line. By looping the PWM generator three times in one switching cycle, 96 taps can be obtained in all, which corresponds to a full range

Figure 2.23: Diagram of a dual band switching PWM generator

Figure 2.24: LUT based auxiliary delay line architecture

of V_g . The band selection signal BC and the most significant bit of the duty cycle command $d5$ control a simple logic to enable the multiplexer in one of the three loops.

Although the number of delay cells is reduced for this approach, the drawback is that extra logic circuits are required to generate the band selection signal and to count the loops.

2.8.2.7 Heterogeneous DPWM

The heterogeneous digital PWM (Foley et al., 2005) extends the hybrid PWM by adding auxiliary delay stages at the output stage of the multiplexer, as shown in Figure

Figure 2.25: Block diagram of Feed-Forward DPWM

2.24. The duty ratio command, for example, $d[m-1:0]$ is categorized into 3 groups: $d[m-1:m-k]$, which sets the coarse time comparator reference, $d[m-k-1:q]$ which selects the appropriate tap of the multiplexer, $d[q-1:0]$, which selects the delay of the auxiliary delay line. The SR-latch is set each time the counter output return to zero, and reset when the specified duty cycle command is reached.

In contrast to the main delay line in the ring oscillator which uses delay cells, the auxiliary delay line uses look-up tables (LUTs) to generate the delays. Compared with the traditional hybrid digital DPWM, the heterogeneous approach uses fewer multiplexers and lower clock frequency.

2.8.2.8 Feedforward DPWM

The feedforward DPWM is a digital PWM controller with feed-forward compensation of the input voltage. The feed-forward compensation is accomplished through a delay-line digital pulse width modulator as depicted in Figure 2.25 where the cell delay is made inversely proportional to the input voltage (Syed et al., 2004). The advantages of feed-forward compensation are improved line regulation and independent loop gain with respect to the input voltage variation.

The output pulse width t_{on} is equal to:

$$t_{on} = D \cdot t_d \quad (2.39)$$

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where D is the numerical value of the duty ratio command and t_d is the cell delay. In the feedforward DPWM, the cell delay should be inversely proportional to V_{in} :

$$t_d = \frac{A}{V_{in}} \quad (2.40)$$

where A is ideally a constant. In a buck converter, the output quantization step V_{step} is:

$$V_{step} = V_{in} \frac{t_d}{T_s} = \frac{A}{T_s} \quad (2.41)$$

Thus the feedforward DPWM has a constant quantization step which is independent of the input voltage, V_{in} .

This chapter discusses the basic topology of a DC-DC converter and shows an analysis of a digital DC-DC converter and its building blocks in prior arts, namely the DPWM, ADC and the digital controller. The analysis in the following chapters will show the design of the proposed building blocks of an integrated digital DC-DC converter, specifically for a buck converter. However, the design and analysis can be extended to other converter topologies.

Part II

Design on the Building Blocks of the Digital DC-DC Converters

Chapter 3

The High Resolution Process and Temperature Insensitive DPWM

3.1 Introduction

A large portion of this chapter is extracted from a paper to be published in the IEICE Transactions on Electronics (Regular Papers) (Foong *et al.*, 2011a) co-authored by the author of this thesis.

A digital DC-DC converter typically consists of four blocks, namely an ADC, a digital controller, a Digital Pulse Width Modulator (DPWM) and an output filter as shown in Figure 3.1. The DPWM is primarily used to generate a PWM signal to drive the power transistors to regulate the voltage at the output. Up to now, several configurations have been reported in literature to realize the DPWM such as the fast clock counter

Figure 3.1: Block diagram of digitally-controlled buck converter

3.2 Overview of Digital Pulse Width Modulator

comparator (Wei and Horowitz, 1996), the tapped delay line (Dancy et al., 2000), the hybrid or ring-mux structure (Xiao et al., 2001), and the segmented tapped delay line (Trescases et al., 2005). However, the DPWM in all these realizations are still susceptible to noise and process variation issues even though the designs have been shifted from an analog to digital regime. The noise generated through digital switching will further degrade the accuracy of the DPWM through feedback and coupling. For instance, the power supply noise will affect the delay of the tapped delay line which will in turn affect the frequency of the PWM signal. Moreover, if the noise is within the passband of the low pass filter, it could be coupled to the output and deteriorate the voltage regulation of the converter. Thus, it is imperative to design a DPWM which is insensitive to supply noise perturbation as well as process variations.

From our analysis, the supply noise and process variation effect will not be significant if low resolution DPWM and ADC are adopted in the digital DC-DC converter. However, a lower resolution PWM will degrade critical specifications such as the line and voltage regulations. High quantization resolution is thus desired to achieve accurate output regulated voltage (Peterchev and Sanders, 2001).

This chapter presents a high-resolution 12-bit DPWM which is insensitive to supply and process variation. The proposed DPWM is implemented using a differential ring oscillator in a hybrid-segmented topology. This solution is very robust and occupies a smaller silicon area than other reported designs of equivalent resolution.

3.2 Overview of Digital Pulse Width Modulator

The DPWM of the digital DC-DC converter can generally be realized in three ways. First, it can be realized using the counter comparator technique which utilizes a counter to count the number of clock cycles required to generate the pulse of the PWM signal. Put differently, the count value is proportional to the input digital codes as well as the duty cycles of the PWM signal. However, one major disadvantage of this technique is that the clock frequency of the counter has to be doubled for every 1-bit increase in resolution. This will increase the power consumption substantially when the DPWM resolution is high. A second way to implement the DPWM is the ring oscillator-multiplexer technique, where the delay of each delay element in the ring oscillator is

3.2 Overview of Digital Pulse Width Modulator

Figure 3.2: Proposed hybrid-segmented DPWM architecture

equivalent to 1 LSB delay. In this technique, the hardware will be doubled for every 1-bit increase in resolution, thereby increasing the IC area substantially if the resolution is high. The third method, also known as the hybrid ring-mux approach, is a combination of the first and second methods. This approach is more prevalent for three primary reasons: a smaller IC area, lower power consumption, and higher resolution.

To achieve even higher resolution and smaller IC area, a hybrid-segmented approach is proposed as depicted in Figure 3.2. In the proposed hybrid-segmented architecture, the input of the DPWM is a pulse width command, $D[11:0]$, derived from the output of the digital controller. The digital controller compares the output of the ADC (detection signal) with the reference and creates the pulse width command $D[11:0]$ through digital processing. The first segment $D[2:0]$ is used to drive the counter comparator while the next segment $D[5:3]$ is used to reset the PWM through a D flip-flop. The last segment $D[11:6]$ is connected as reference code for the counter comparator.

As the supply voltage continues to decrease when technology advances, it is typically required that the output voltage of a DC-DC converter achieves a resolution or accuracy

3.3 Segmented Tapped-Delay Line of the Proposed DPWM

of millivolt or even sub-millivolt range (McGinty, 2005). The resolution of the output voltage, V_o of a digital DC-DC converter depends mainly on the number of bits of the DPWM, n and input voltage, V_{in} according to Equation (3.1).

$$\text{Resolution of } V_o = \frac{V_{in}}{2^n} \quad (3.1)$$

In the design, the resolution of DPWM is chosen to be 12 bits to achieve an output voltage resolution of 0.8 mV for an input voltage of 3.3 V. Note that to prevent limit-cycle oscillation at the output of the converter, the resolution of the DPWM block must be greater than that of the ADC (Peterchev and Sanders, 2001). In this case, the resolution of the ADC is 10 bits.

This hybrid-segmented approach is more area-efficient than the conventional approach because it uses fewer number of delay cells for the same resolution. In this proposed design, the number of delay cells is further reduced by reusing the $1 \times$ delay cells for the second multiplexer input. For a 12-bit DPWM, the 6 LSBs implemented with the proposed architecture requires only 20 delay cells whereas the ring-mux approach would require 32 differential delay cells. This will provide about 37.5% saving in IC area. With the proposed delay cell reused technique, the oscillating frequency is also increased by 75% due to the dual feedback of the segmented ring oscillator. Consequently, this will lead to a proportional increase in the switching frequency and a lower power consumption.

3.3 Segmented Tapped-Delay Line of the Proposed DPWM

In the hybrid-segmented approach, or any approach employing the segmented delay line architecture, the design of the delay cell is very important because any variation in the delay will affect the accuracy and switching frequency of the DPWM. In the proposed DPWM, the 6-bit MSBs are realized by a counter and the 6-bit LSBs are realized by a multiplexer with delay cells as shown in Figure 3.2.

For the design of ring oscillator, a differential delay cell is usually adopted to reduce the phase noise (Hajimiri et al., 1999). The differential structure is also more suitable

3.3 Segmented Tapped-Delay Line of the Proposed DPWM

Figure 3.3: Low-voltage differential delay cell and supply insensitive replica biasing

for low voltage application because the signal swing is doubled compared to that of a single-ended topology. The schematic of a low voltage differential delay cell is shown in Figure 3.3.

The loads at the outputs of the differential delay cells are diode-connected for two reasons. First, it reduces the gain of the delay cell, as shown in Equation (3.2) below, which will reduce the delay of each cell significantly.

$$A_v = -g_{m1} \left(\frac{1}{g_{m3}} // r_{o1} // r_{o3} // r_{o4} \right) \approx -\frac{g_{m1}}{g_{m3}} \quad (3.2)$$

Second, it clamps the maximum swing of the delay cell and enables the ring oscillator to operate at a much higher frequency. Transistors M4 and M5 are used to serve as the delay control or tuning control of the ring oscillator. This decides the upper limit of the output swing, and thus controls the delay of each cell. The maximum swing of the output is derived as follows:

$$(V_{out})_{max} = \max(V_{ctrl} - V_{thn}, V_{eff} + V_{thn}), \quad (3.3)$$

where V_{thn} is the threshold voltage of the NMOS transistors and V_{eff} is the effective gate-source voltage of M3 or M6. Hence, the delay of each stage can be estimated as:

$$t_{delay} = (V_{out})_{max} \frac{C_{par}}{I_{bias}}, \quad (3.4)$$

3.3 Segmented Tapped-Delay Line of the Proposed DPWM

where C_{par} is the parasitic capacitance at the output nodes of the delay cell. From Equation (3.4), note that t_{delay} will be affected by the supply noise since the bias current is sensitive to the variation of the supply voltage. To improve the power supply rejection ratio, the bias current must be insensitive to the supply voltage. This can be achieved by biasing the delay cell with a replica biasing block as depicted in Figure 3.3.

To stabilize the bias current, the replica bias circuit utilizes an op-amp to control the bias current of M8 by means of negative feedback. The dimension of M8 is identical to M7 of the differential delay cell to maintain the same bias current in both circuits. The op-amp can be realized by a single or two-stage design with a proper start-up circuit. Stability can be further improved by connecting a compensation capacitor, C_1 to V_{biasp} . The bias current of M8 and M11 is given as follows:

$$I_{M11} = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_{11} (V_{ctrl} - V_{thn})^2 \quad (3.5)$$

$$I_{M8} = 2I_{M11} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{11} (V_{ctrl} - V_{thn})^2. \quad (3.6)$$

From Equations (3.5) and (3.6), note that the bias current for charging and discharging the output parasitic capacitance of the delay cell is insensitive to the supply voltage variation because it is not a function of the supply voltage. Instead, the bias current is determined by the control voltage, V_{ctrl} , which controls the current of M4, M5, and M10. Thus, the accuracy of the current is only dependent on the matching between transistors M10 and M11. The op-amp employed in the replica biasing cell is a single-stage op-amp with a start-up circuit as depicted in Figure 3.4.

To level-shift the output of the differential delay cell to rail-to-rail swing for the multiplexer, a differential buffer as depicted in Figure 3.5 is inserted between each delay cell and the multiplexer. To further reduce jitter and improve the slew rate, the output of the buffer is cross-coupled.

Two 8:1 multiplexers (MUXs) are also required for the hybrid segmented DPWM. The schematic of the 8:1 MUX is depicted in Figure 3.6. The select signal, $S[2:0]$ is used to control the transmission gates of every branch such that only one of the eight input signals is passed to the output. To reduce the delay mismatch, the two MUXs must be matched in terms of transistor sizes and routing length.

3.4 Counter-comparator of the Proposed DPWM

Figure 3.4: Op-amp with start-up circuit

Figure 3.5: Low jitter differential buffer

3.4 Counter-comparator of the Proposed DPWM

Figure 3.7 depicts the implementation of the counter using negative edge-triggered D flip-flops, XOR and AND gates. Initially, all the flip-flops are reset. Hence, all the bits are 0 and only the output of the first XOR is 1. After that, reset is deasserted. At negative-edge of the clk signal, the D flip-flop is triggered; $A0$ becomes 1 and the output of the XOR changes to 0. Subsequently, $A0$ toggles for every clock cycle whereas $A1$ of the second flip-flop starts to toggle only after $A0$ has become 1. Otherwise, its value is held for the next clock cycle. Likewise, for $A2$, $A3$, $A4$, and $A5$, the flip-flops only trigger when the preceding bit is 1. Consequently, the counter starts counting from 00000 to 11111 and then the cycle will be repeated. As compared to the asynchronous counter proposed in (Xiao et al., 2001), this synchronous counter approach is not affected by

3.4 Counter-comparator of the Proposed DPWM

Figure 3.6: Schematic of 8:1 MUX

the propagation time and, therefore, has a faster speed.

The 6-bit comparator adopted in the counter-comparator segment consists of six one-bit comparators followed by some AND and OR gates as depicted in Figure 3.8. When $A < B$, the output Y is 1. However, when $A \geq B$, Y becomes 0. As compared to the ripple comparator in (Xiao), this dynamic comparator has a faster comparison time as it does not need to wait for the preceding bit decision to ripple through.

Figure 3.9 depicts the design of a negative edge-triggered D flip-flop (DFF). It is based on the master-slave concept. Assuming $RST = 0$; when $CLK = 1$, the input data is sampled on the parasitic capacitances at node X. During this period, the slave stage is in the hold mode. On the negative edge of the clock, the transmission gate T2 turns on, and the value sampled on node X immediately before the rising edge propagates to the output Q . However, as supply variation and leakage current may affect the data stored in the internal and output node, a positive feedback loop embodying two back-to-back connected inverters is added to make the nodes static when they are in the hold mode.

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

Figure 3.7: Schematic of the Counter

Finally, we make use of the asynchronous *SET* and *RST* to set and reset the internal nodes of the DFF, respectively.

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

A 12-bit resolution DPWM embodying the proposed differential delay cell with replica biasing has been designed using CMOS 0.18 μm process. Figure 3.10 shows the simulation results of the DPWM over supply voltage ranging from 1.5 V to 2.5 V. Figure 3.11 shows the simulation results of the DPWM over a wide range of temperature and process corners.

In Figure 3.10, note that the delay variation for the delay cell with replica biasing is only 0.8% over a supply voltage range of 1.5V to 2.5V whereas the variation of the delay cell without replica biasing is 17.3%. The variation of the replica bias delay cell

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

Figure 3.8: Schematic of the comparator

Figure 3.9: Schematic of the negative edge-triggered D flip-flop

is small because the negative feedback of the self-biasing circuit has reduced the effect of supply changes by keeping the bias current constant.

From Figure 3.11, it can be seen that the delay of the ring oscillator varies by 0.95% over different process corners and temperature range from -40°C to 90°C .

In our hybrid DPWM design, the delay variation of the ring oscillator will result in

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

Figure 3.10: Delay variation against supply voltage

Figure 3.11: Delay against process and temperature variation

a change in the switching frequency since the ring oscillator output is fed into the counter-comparator to generate the upper-bits of the digital code before it is compared with the reference digital code. Thus the switching frequency deviation is derived as:

$$\Delta F_{switching} = \frac{1}{t_{period}} - \frac{1}{t_{period} + 2^k * \delta t_{delay_osc}}, \quad (3.7)$$

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

Figure 3.12: Switching frequency against supply voltage

where k is the number of bits for the counter comparator, t_{period} is introduced as the original PWM period and δt_{delay_osc} is the variation of the period of the ring oscillator.

Figure 3.12 depicts the switching frequency of a DPWM embodying the replica biasing and a DPWM with conventional current biasing when the supply varies from 1.5 V to 2.5 V. Note that the variation of the switching frequency of the DPWM with replica biasing at 1.02MHz is less than 0.4% whereas the variation of the PWM with conventional current biasing is 30.4%. This shows that the DPWM with replica biasing is able to maintain a relatively stable switching frequency since the delay variation has been reduced.

Figure 3.13 depicts the switching frequency variation against various process corners. Once again, the DPWM with replica biasing has a much smaller switching frequency variation (0.48%) than that of conventional biasing.

To further validate the process insensitiveness of the delay cell, the mismatch effects of the transistors are simulated and analyzed. This deviation in delay is due to both mismatch in layout as well as process variation. As for the delay cell shown in Figure 3.3, the mismatch effect would lead to a difference in current for the two branches and result in a delay variation of the ring oscillator. Jitter will thus occur and cause a frequency variation in the DPWM. Although this mismatch can be minimized through

3.5 Simulation Results for Supply- and Process-Insensitive DPWM

Figure 3.13: Switching frequency against different process corners

proper layout techniques, mismatch introduced through process variation is inevitable. The effect on delay variation can be further derived from Equation (3.4) as

$$t_{delay} + \delta t_{delay} = (V_{out} + \delta V_{out}) \frac{C_{par}}{(I_{bias} - \delta I_{bias})}. \quad (3.8)$$

Assuming that δV_{out} is small and using Taylor expansion up to first order, the variation in delay is:

$$t_{delay} + \delta t_{delay} \approx (V_{out} + \delta V_{out}) \frac{C_{par}}{I_{bias}} (1 + \Delta I_{bias}), \quad (3.9)$$

$$\delta t_{delay} \approx \frac{V_{out}}{I_{bias}} C_{par} (\Delta I_{bias}), \quad (3.10)$$

where ΔI_{bias} is the ratio of changes in I_{bias} . Thus the delay effect will depend on the current mismatch of the current mirror (M7&M8) matching. In practice, however, the delay variation is mitigated through clamping of the output swing by the diode-connected transistors. For simulation, a $\pm 5\%$ (3σ) current mirror mismatch was introduced to the transistors pairs (M7&M8, M11, M3&M6, and M10, M4&M5), the delay variation was found to be 0.87% for the worst case scenario using Monte-Carlo

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Figure 3.14: Histogram showing the delay variation of the ring-oscillator from 100 runs of Monte-Carlo simulation

Figure 3.15: Linearity of the 12-bit DPWM

simulation (with mean=84.4806 ns and standard deviation=186 ps) at the supply voltage of 1.8 V. Figure 3.14 shows the statistical distribution of the delay for 100 runs of Monte-Carlo simulation.

Figure 3.15 depicts the linearity of the 12-bit DPWM. The correlation r is found to be 0.99. Finally, a comparison of the proposed hybrid-segmented DPWM and the prior arts is given in Table 3.1.

Table 3.1: Comparison of proposed hybrid-segmented DPWM against the prior arts

Implementation of DPWM	Counter Comparator	Ring-MUX	Segmented	Hybrid Ring-MUX	Proposed Hybrid Segmented
CMOS	0.25	0.25	0.6	0.35	0.18
Technology(μm)					
Supply Voltage(V)	2.5	2.5	5	3.5	1.8
Resolution (no. of bits)	8	8	6	10	12
Switching Frequency (MHz)	1	1	1	1	1
Area (mm^2)	0.075	0.084	0.0675	0.16	0.031
Current Consump- tion (μA)	2000	10	111	199.3	14

Figure 3.16: Microphotograph of the DPWM test chip

3.6 Measurement Results

The DPWM was fabricated in the Chartered Semiconductor CMOS $0.18\mu\text{m}$ process. The microphotograph of the test chip, which is encapsulated in a QFP package, is shown in Figure 3.16. The core area of the DPWM is 0.031 mm^2 . The test printed circuit board is depicted in Figure 3.17. The measurement results of the switching frequency variation against supply voltage and temperature are depicted in Figure 3.18. The

Figure 3.17: Printed circuit board for test chip

Figure 3.18: Measured switching frequency against supply voltage and temperature variation

Figure 3.19: Transient PWM waveform with different input codes

measured variation of the switching frequency is 0.82% for supply voltage from 1.5 V to 2.5 V and 0.36% for temperature ranging from -40°C to 90°C.

Figure 3.19 depicts the measured waveform of the DPWM with three different input codes. It can be seen that the pulse width is directly proportional to the input codes.

The PSRR of the DPWM was determined by injecting a sine wave at the supply and measuring the variation of the pulse width, which was then divided by the unit delay of the delay line. The results are illustrated in Figure 3.20.

Figure 3.20: PSRR measurement of the DPWM test chip

Figure 3.21: Load regulation characteristics under different temperature conditions

Finally, the load and line regulation characteristics of the digital DC-DC converter embodying the DPWM under different temperature conditions are depicted in Figure 3.21 and Figure 3.22, respectively. The maximum deviation of the output voltage for a load current change of 500 mA is 0.6 mV whereas the maximum deviation when the input voltage changes from 1.8 V to 3.3 V is 0.7 mV. The temperature coefficient of the proposed digital DC-DC converter is smaller than 0.01%/°C. Note that the output voltage is regulated within a range of ± 0.8 mV around the output voltage of 1.2 V for

Figure 3.22: Line regulation characteristics under different temperature conditions

temperature ranging from -40°C to 90°C , which meets our design specification of an output voltage resolution of 0.8 mV.

This chapter discusses the design and implementation of a supply- and process-insensitive, 12-bit DPWM for a digital DC-DC converter. Theoretical derivations, simulation and measurement results show that the switching frequency of the DPWM with replica biasing can be precisely controlled regardless of process, mismatch and temperature variations. This 12-bit DPWM will be adopted in the integrated digital DC-DC converter in Chapter 5. The next chapter will discuss about another building block of the digital DC-DC converter: the feedback ADC.

Chapter 4

A Windowed SAR ADC with Offset Cancellation for Digital DC-DC Converters

4.1 Introduction

A large portion of this chapter is extracted from a paper published in the journal of Analog Integrated Circuits and Signal Processing (Mixed Signal Letter) (Foong *et al.*, 2011b) co-authored by the author of this thesis.

As discussed in Chapter 3, a digital DC-DC converter consists of four blocks, namely an analog-to-digital converter (ADC), a digital controller, a digital pulse width modulator (DPWM), and an output filter. The ADC is employed to sample the output voltage and converts it into a digital code for the controller. Several architectures have been proposed in the prior arts, such as the windowed flash ADC (Peterchev *et al.*, 2003) and the ring ADC or tapped-delay line ADC (Xiao *et al.*, 2003, Patella *et al.*, 2003). However, the flash ADC needs a large number of comparators and thus it consumes high power. On the other hand, the ring ADC is not area and power efficient due to the long delay chain. Besides, the inherent temperature and process sensitivity of the delay cells degrade the linearity of the ADC. In contrast, the successive approximation (SAR) ADC can typically achieve medium speed with minimal power consumption

(Hong and Lee, 2007, Sauerbrey and Schmitt, 2003). Thus it is an ideal candidate for the application in digital DC-DC converters.

This chapter presents a low power windowed SAR ADC for digital DC-DC converters. A windowed ADC works within a specific input voltage range as opposed to full-range ADC, for example a windowed flashed ADC (Peterchev et al., 2003). Specifically, the input of the ADC in a digital DC-DC converter is the error signal derived from the difference between the output voltage and the reference voltage. Therefore, it does not generally require a full-range ADC. By constraining the quantization range, power consumption can be significantly reduced. Besides, this eliminates the need of a dedicated sample-and-hold circuit. Thus, the windowed ADC also achieves very low power consumption, which leads to a high efficiency DC-DC converter. In addition, an auto-zero comparator with offset-cancellation is proposed to resolve the offset issue in the design of the SAR ADC.

This chapter is organized as follows. An overview of the basic architecture of SAR ADC will be given in Section 4.2. Section 4.2 will also presents the proposed windowed SAR ADC. In Section 4.3, we elaborate the analysis and design of the windowed SAR ADC. An offset-cancelled, auto-zero comparator is also presented with detailed analysis. Section 4.4 shows the simulation results. Section 4.5 demonstrates the measurement results of the test chip of a digital DC-DC converter embodying the proposed SAR ADC. Finally, a summary of the overall findings is given in Section 4.6.

4.2 System Architecture

To understand the importance of a good ADC design to the performance of a digital DC-DC converter, the constraints imposed on the DC-DC converter by the SAR ADC must be determined. There are mainly three factors, namely (1) power consumption, (2) speed or conversion rate, and (3) programmable resolution or quantization step. First, reducing power consumption increases the efficiency of the DC-DC converter. As we know, the power consumption at a switching node is proportional to $(voltage)^2$ and *frequency*. Therefore, to reduce the power consumption, it is essential to design an ADC that operates with a reduced input voltage range as well as lower supply voltage. Second, the ADC should have a fast conversion rate. This is because the delay of the

Figure 4.1: Conventional full-range SAR ADC. Note that *gnd* is the analog ground and V_{ref} is half of the supply voltage

ADC introduces phase lag to the loop response of the DC-DC converter, which will reduce the phase margin and thereby affect the stability and the transient response of the DC-DC converter. Thus, a fast ADC will ease the design of the digital controller. Typically, for a SAR ADC, the delay includes the time for sample-and-hold, the delay of the comparator in track and latch modes as well as the delay of data shifting in registers. Third, the ADC must have programmable resolution to avoid limit-cycle oscillation. Essentially, limit-cycle oscillation occurs when the quantization step of the DPWM is smaller than that of the ADC. For a DC-DC converter that has a wide line voltage range, the quantization step of the DPWM varies largely. Therefore the resolution or the quantization step of the ADC must change accordingly to prevent limit-cycle oscillation.

In a digital DC-DC converter, the input of the feedback ADC is an error signal derived from the difference between the output voltage and the reference voltage. Since this error signal is small most of the time, a full-range-ADC is unnecessary. This is because the output voltage is generally a constant except during transient. Even in the transient period when there are changes in the load or line voltage, the output voltage will typically vary in a limited range around the desired output voltage. A windowed ADC has an input range defined between an upper limit, V_{upper} and a lower limit, V_{lower} . An example is a windowed flashed ADC (Peterchev et al., 2003). Therefore, it suits the application of the feedback ADC in digital DC-DC converters, as high resolution is only needed within a certain voltage range. The windowed ADC also has

Figure 4.2: Architecture of the proposed windowed SAR ADC with an internally auto-zero comparator

the significant advantage of reducing the power consumption as the voltage across the capacitors is smaller. Figure 4.1 shows the conventional charge redistribution SAR ADC whereas Figure 4.2 illustrates the architecture of our proposed 5-bit windowed SAR ADC. Note that the reference voltage, V_{ref} and ground, gnd of the conventional full-range SAR ADC have been replaced with V_{upper} and V_{lower} . The operating principles are elaborated as follows. Initially, during sample mode, all the capacitors are charged to V_{in} and the comparator is auto-zeroed, thus V_x is at V_{lower} . Next, during hold mode, the comparator is taken out of reset, and all the capacitors are switched to V_{lower} . This causes V_x to become $2V_{lower} - V_{in}$. Next during bit cycling, each bit, from the most significant bit (MSB), $b1$ to the least significant bit (LSB), $b5$, is pulsed for one clock cycle sequentially. Specifically, when $b1$ is set, the bottom plate of the largest capacitor is connected to V_{upper} . If V_{in} is larger than $(V_{upper} - V_{lower})/2$ at the end of the sampling mode, then $b1$ is set to 1, which means the largest capacitor will be connected to V_{upper} for the subsequent cycles and the conversion proceeds to determine $b2$. However, if V_{in} is less than $(V_{upper} - V_{lower})/2$ at the end of the sampling mode, then $b1$ is set to 0 and the bottom plate of the largest capacitor is switched back to V_{lower} . This conversion process is repeated five times until the LSB, $b5$ has been determined. Thus the window of the ADC is defined by V_{upper} and V_{lower} . By limiting the reference voltage range, we achieved lower power consumption. In addition, the flexibility in selection of V_{upper} and V_{lower} provides programmability in resolution or the quantization step of the ADC.

Figure 4.3: Flowchart of the proposed windowed charge redistribution SAR ADC

The proposed windowed SAR ADC requires eight clock cycles for data conversion. During the first clock cycle, data are sampled at the input ports. For the second clock cycle, data are being held. Next is the bit cycling process: output bits are being determined for each clock cycle from MSB to LSB. Finally, at the eighth clock cycle, data is being output and the conversion process repeats again. In our case, the clock frequency is 32 MHz and thus the conversion rate is 4 MSPS. Figure 4.3 depicts the flowchart of the operating principles of the windowed SAR ADC.

4.3 Design and Analysis

4.3.1 Dynamic Comparator with Auto-Zeroing

Conventional comparator is connected as a negative feedback opamp during auto-zero (Razavi and Wooley, 2003, Shirai, 2007, Katyal et al., 2006). Thus, the comparator

Figure 4.4: The proposed two-stage (preamp & latch) comparator with an internal auto-zero scheme

needs compensation to avoid stability issue during auto-zeroing. This reduces the bandwidth of the loop response and degrades the speed of the ADC as the response time of the comparator limits the clock frequency and the conversion time of the ADC. Besides, the delay of the comparator introduces phase lag, which results in a smaller phase margin and a longer settling time. To circumvent the delay issue, an ultra-fast comparator with internal auto-zeroing is proposed as depicted in Figure 4.4. The comparator consists of a two-stage preamplifier and a latch. The preamplifier is similar in structure to a dynamic folded cascode amplifier. The capacitances shown at the gate of M8 and M9 are the parasitic capacitances at the nodes. The operating principles of the auto-zero schemes is as follows: When ϕ_1 is high during auto-zero, the output impedance seen at the drain of M9, Z_1 is derived as:

$$Z_{1,az} = \frac{2}{g_{m11} + g_{ds9} + g_{ds11}} \quad (4.1)$$

This represents a low impedance node to ground and thus the output of the preamplifier is auto-zeroed very quickly. Since the time of auto-zero is the limiting factor of the clock frequency, the clock rate can now be increased, which leads to a faster conversion rate of the ADC.

When ϕ_1 is low during comparison, the impedance Z_1 is derived as:

$$Z_{1,comp} = \frac{1}{g_{ds9}} \quad (4.2)$$

Figure 4.5: Timing signals required by the comparator

Therefore, the preamplifier will have adequate gain during comparison. In the derivation, the second order effect of the transistors is neglected. From the timing diagram depicted in Figure 4.5, note that when ϕ_1 drops, ϕ_1' remains high to prevent charge injection affecting the latch stage. This is because the charge injection due to ϕ_1 switches is stored at the coupling capacitors, C . However, as ϕ_1' is high at this time, the latch stage is still in reset. Therefore, this charge will not affect the latch stage. When ϕ_1 is high, the comparator is auto-zeroed by connecting M8, M9 in diode connected configuration while their source terminals are also connected together. This reduces the offset due to the mismatch of the transistors and process variation according to Equations (4.3), (4.4), and (4.5). Assuming A_1 and V_{os1} is the gain and offset of the preamplifier and A_2 and V_{os2} is the gain and offset of the latch, we can derive that:

$$A_1 = g_{m1}r_{ds9} \quad (4.3)$$

$$A_2 = g_{m18}[r_{ds12}^{-1} - g_{m13}^2(r_{ds14} // r_{ds15} // r_{ds17}) + r_{ds16}^{-1}]^{-1} \quad (4.4)$$

The offset voltage can then be derived as:

$$V_{os} = \frac{V_{os1}}{A_1} + \frac{V_{os2}}{A_1 A_2} + \frac{\Delta Q}{A_1 C} \quad (4.5)$$

where ΔQ is the charge injection due to the auto-zero switches. Transistors M10 and M11 serve to control the common mode voltage at V_0 and V_1 . Note that in the track mode, the difference between V_{in} and V_{ref} is amplified first through the preamp stage, and then by the latch stage. This results in a shorter response time and a smaller phase lag.

Figure 4.6: Timing generation block of the windowed SAR ADC

4.3.2 SAR Timing Block

The SAR ADC needs eight clock cycles to perform data conversion. Among the eight clock cycles, five cycles are used to perform code generation, while the rest are for sample, hold and output. Figure 4.6 depicts the timing circuit block. This block serves to generate eight pulses needed to activate each stage of the conversion. In the circuit, D flip-flops (DFF) are connected sequentially, and an RC element is inserted for soft-starting. Initially, the first flip-flop is set while the rest of the flip-flops are reset. After the capacitor, C is fully-charged, all the flip-flops are de-asserted. Subsequently, at the falling edge of the clock, the first pulse at the output of the first flip-flop starts to shift to the right, whereby it operates like the shift registers. Therefore, $b0$ is set at the fifth clock cycle, and $b1$, $b2$, $b3$, and $b4$ are set at the subsequent clock cycles.

4.3.3 SAR Logic Block

SAR logic is used to determine the output code of the analog-to-digital conversion. Figure 4.7 depicts the SAR logic block. Specifically, the SAR logic block determines bit i is 0 or 1 through the feedback from the output of the comparator. When the set signal is asserted, the output of the flip-flop is logic 1. The logic 1 is then used to determine the comparator output. Meanwhile, comparator output is being loaded into the master portion of the flip-flop. When set and reset signal are de-asserted, the value of b_i is determined by the output of the comparator. Each of the flip-flop is sequentially pulsed by the SAR timing block, from $b0$ (MSB) to $b4$ (LSB), where each pulse lasts for one clock cycle.

Figure 4.7: Logic block of the windowed SAR ADC

Figure 4.8: Schematic of the negative edge-triggered D flip-flop

4.3.4 Design of the D flip-flop

Figure 4.8 depicts the negative edge-triggered D flip-flop (DFF) employed in our design. It is based on the master-slave concept. Assuming $RST = 0$; when $CLK = 1$, the input data is sampled on the parasitic capacitances at node X . During this period, the slave stage is in hold mode. On the negative edge of the clock, the transmission gate $T2$ turns on, the value sampled on node X immediately before the rising edge propagates to the output Q . However, as supply variation and leakage current may affect the data stored in the internal and output node, positive feedback embodying two back-to-back connected inverters is added to make the nodes static when they are at the hold mode. Finally, we make use of the asynchronous SET and RST to set and reset the DFF respectively.

Figure 4.9: Timing waveforms of the proposed windowed SAR ADC for $V_{in} = 1.2$ V

4.4 Simulation Results

Figure 4.9 shows the timing waveform of the SAR ADC at an input voltage of 1.2 V. We note that the SAR ADC is sampled at the positive edge of V_{sample} , and it shows the correct output of 01111 and has an input latency of 300 ns.

Figure 4.10: Transient response (low-to-high) of the comparator

The transient behavior of the proposed comparator is depicted in Figure 4.10 and Figure 4.11. Note that the low-to-high response time is 3.78 ns and the high-to-low response time is 2.47 ns.

Figure 4.11: Transient response (high-to-low) of the comparator

Figure 4.12: Layout of the digital DC-DC converter IC embodying the proposed windowed SAR ADC

4.5 Measurement Results

A digital DC-DC converter embodying the proposed windowed SAR ADC was fabricated with GlobalFoundries CMOS 0.18 μm process. The layout of the test chip is shown in Figure 4.12. The core area of the DC-DC converter is $1\text{ mm} \times 1\text{ mm}$ ($= 1\text{ mm}^2$), whereby the area of the ADC is $0.2\text{ mm} \times 0.3\text{ mm}$ ($= 0.06\text{ mm}^2$). The switching frequency of the digital DC-DC converter is 1MHz. The measurement results of the DC-DC converter and the ADC during a load transient from 5 mA to 500 mA and from 500 mA to 5 mA are depicted in Figure 4.13 and Figure 4.14, respectively. Note that in steady-state, the error code $e[4:0]$, derived from the reference voltage minus the

Figure 4.13: Load transient response (high-to-low) of the digital DC-DC converter

Figure 4.14: Load transient response (low-to-high) of the digital DC-DC converter

output voltage, is zero. The results also demonstrate that the ADC responds quickly to the output changes and completes the conversion cycle within 150 ns after the output changes.

A benchmark of the proposed SAR ADC against the prior arts is provided in Table 4.1. A Figure-of-Merit (FOM) is introduced based on the following equation:

$$FOM = \frac{Power}{2^{\frac{SNDR-1.76}{6.02}} \cdot F_{CLK}} (J/Step) \quad (4.6)$$

where SNDR is the signal-to-noise+distortion ratio and F_{CLK} is the sampling frequency.

From Table 4.1, it can be seen that the proposed design shows good linearity with a DNL of $\pm 0.22\text{LSB}$ and an INL of $\pm 0.39\text{LSB}$ due to the offset cancellation effect of the

Table 4.1: Comparison of the proposed ADC design against the prior arts

Implementation	Xiao	Hong	Sauerbrey	Proposed Design
Year of publication	2003	2007	2003	2011
Quantization range	80mV	0V–1V	0V–0.45V	1.08V–1.32V
Step size (mV)	16	7	3.9	7.5
DNL (LSB)	± 1	-0.9/0.26	± 0.7	± 0.22
INL (LSB)	± 5	-0.53/0.5	± 0.9	± 0.39
Sampling frequency	600kS/s	200kS/s	1.5kS/s	4MS/s
SNDR (dB)	–	47.4	51.2	31.1
Power consumption (μ W)	92.5	2.47	0.49	0.8
IC area (mm ²)	0.15	0.23	0.11	0.06
Power supply (V)	2.5	0.9	0.45	1.8
FOM (J/Step)	–	65f	674f	7f

comparator. It also achieves a low power consumption of 0.8μ W. However, due to the switching noise caused by fast sampling, the SNDR is lower than the prior arts. From energy perspective, the proposed design consumes 7fJ for an effective conversion step.

This chapter discusses the windowed SAR ADC for the feedback ADC for a digital DC-DC converter and shows the design and analysis to achieve medium resolution with low power consumption. The windowed SAR ADC will be adopted in the integrated digital DC-DC converter in the next chapter.

Part III

Design on an Integrated Digital DC-DC Converter with Predictive and Feedforward Control

Chapter 5

Fast-Transient Integrated Digital DC-DC Converter with Predictive and Feedforward Control

5.1 Introduction

A large portion of this chapter is extracted from a paper accepted for publication in the IEEE Transactions on Circuits and Systems I: Regular Papers (Foong *et al.*, 2011c) co-authored by the author of this thesis.

A high performance VLSI system requires a fast transient DC-DC converter to frequent load changes due to the nature of a multimode system (Luo and Ma, 2009). Thus, both academics and industries put a lot of effort into the research of the control schemes of the digital DC-DC converter to achieve good transient response and high robustness with a simple architecture. A typical DC-DC converter has a right-half-plane (RHP) zero in its control-to-output transfer function. This property introduces phase lag in the system response and limits the unity-gain frequency of the converters (Erickson and Maksimovic). In addition, the time-delay or latency of the digital controller further increases the phase lag and degrades the robustness of the converter. As such, this in-

creases the difficulty in the design of the controller using the conventional PID approach to achieve stability and fast dynamic response over input and load perturbation.

Many research works have been done in the prior arts on the modeling of the DC-DC converter in the large-signal (Guinjoan et al., 1997) and the small-signal (Middlebrook and Cuk, 1977a) domains. As a DC-DC converter is inherently nonlinear, a feasible approach of designing its controller is to adopt the state-space averaged model (Middlebrook and Cuk, 1977b). Another approach involves applying the Lyapunov stability theory directly to the large signal models such that the closed loop systems possess excellent dynamic properties. Besides, the work in (Naim et al., 1997) uses robust nonlinear control algorithms for the small-signal models to achieve global or semi-global stability. However, these highly nonlinear control methods require high level of computation and logics, thus result in complex digital circuit architecture.

For simple circuit architecture to be realisable, other approaches are primarily based on the cycle-by-cycle control schemes, in which the control switch is controlled by the instantaneous values of the circuit variables. Some examples are the one-cycle control (Ma et al., 2004, Smedley and Cuk, 1995), the sliding mode control (Rossetto et al., 1994), and the bang-bang control (Corradini et al., 2009, Burns and Wilson, 1976). However, the drawback with these control schemes using one-cycle control is that have no information on the output load disturbances. In the sliding-mode control, the trajectory is restricted along the sliding surface and will converge to the operating point after many switching cycles. The bang-bang or hysteresis control has variable switching frequency and non-zero steady-state error (Feng et al., 2007), and therefore it is not suitable in many applications. References (Shirazi et al., 2009) and (Barai et al., 2010, Babazadeh and Maksimovic, 2009, Michal et al., 2010) propose adaptive controllers that limit the overshoot and optimize the transient response for both line and load regulation. However, it is difficult to implement the controllers in digital integrated circuits as they require sophisticated computation or digital processors.

The main objective of this chapter is to address the problems of dynamic response and complexity with the introduction of a digital DC-DC converter adopting a predictive controller to enhance the transient performance. The proposed digital controller is based on a novel predictive+feedforward+PID (PFPID) approach to achieve fast settling time and limited overshoot of the integrated DC-DC buck converter during load

5.2 Architecture of Integrated Digital DC-DC Buck Converter

transient. The PFPID control is realized by combining the predictive and feedforward control with the conventional PID control. The predictive control is based on the second derivative of the error signal and introduces zero to the loop response which leads to increased bandwidth and improved phase margin. To limit the overshoot, the feedforward control is implemented by evaluating the change in the inductor current during the on and off time of the power transistors within a switching cycle. The proposed design has a simple architecture, which leads to a small IC area. Theoretical analysis is further verified on silicon with a prototype of a digital DC-DC converter fabricated in the CMOS 0.18 μm process.

The remainder of this chapter is organized as follows: An overview of the conventional digital DC-DC converter architecture will be given in Section 5.2. Subsequently, the proposed architecture of the digital DC-DC converter is presented. Section 5.3 describes the algorithm of the predictive or jerk control as well as the feedforward control. The implementation of the proposed design is also elaborated. The simulation results are presented and discussed in Section 5.4. Section 5.5 demonstrates the experimental results of the proposed digital DC-DC converter. Finally, Section 5.6 gives a summary of the overall findings.

5.2 Architecture of Integrated Digital DC-DC Buck Converter

5.2.1 Overall Architecture

A digital DC-DC buck converter typically consists of four blocks, namely an analog-to-digital converter (ADC), a digital controller, a digital pulse-width modulator (DPWM), and a power stage consists of power transistors with gate drivers and output filter as depicted in Figure 5.1. The ADC is employed to sample the output voltage and convert it into a digital code for the controller. The controller then executes the control algorithm and produces a digital command for the DPWM. Based on the digital command, the DPWM generates a pulse-width modulated (PWM) signal to drive the power transistors. The PWM signal is eventually filtered by the external low-pass filter to produce the output voltage.

5.2 Architecture of Integrated Digital DC-DC Buck Converter

Figure 5.1: Block diagram of a DC-DC buck converter with its control peripherals

Figure 5.2: Architecture of the proposed digital DC-DC converter with feedforward and predictive/jerk control

Figure 5.2 depicts the architecture of the proposed digital DC-DC converter and its PFPID control scheme. The proposed digital DC-DC converter comprises four main blocks, namely a hybrid-segmented digital pulse-width modulator, a dual-mode (PWM/PFM) PFPID controller, a windowed successive approximation (SAR) ADC and a power stage consisting of power transistors with input buffers and external low-pass filter.

The principles of operation are as follows. First, the hybrid-segmented DPWM generates the PWM signal for the gate drive of the power transistors with a combination of the segmented tapped delay-line and the counter-comparator technique to achieve high resolution. Second, the dual-mode digital controller selects the appropriate mode

5.2 Architecture of Integrated Digital DC-DC Buck Converter

of operation, pulse-width modulation (PWM), which is of fixed-frequency operation, or pulse-frequency modulation (PFM), which is of variable frequency operation to achieve high efficiency. For high load current operation, as the dominant loss is the conduction loss due to parasitic resistances, such as the equivalent series resistance (ESR) of the inductor and the on-resistance of the power transistors, the DC-DC converter should operate in the PWM mode to reduce output ripple and improve efficiency. On the other hand, when the load current is low, PFM is the preferred mode of operation to reduce switching loss. Essentially, the controller compensates the frequency response of the DC-DC converter to achieve stability and fast transient response. Third, the power stage is composed of the parallel power transistors, consist of the on-chip PMOS and NMOS transistors, and the external (off-chip) low-pass filter. For the feedback loop to be closed, an ADC is needed to convert the output voltage into the digital domain. In this case, we propose a windowed SAR ADC that is able to achieve moderate speed with small IC area. This is sufficient for the DC-DC converter application.

Although the dual-mode PWM and PFM control is sufficient to achieve moderately high efficiency, further control strategies are needed to optimize the transient response. Therefore, feedforward control and predictive or jerk control are adopted to achieve ultra-fast transient response. These two control circuits are added in parallel with the original PID control circuits.

The feedforward control augments the feedback control by detecting and processing the input current value from the current detector. This will significantly improve the overshoot performance and the noise disturbance as a desired limit can be imposed directly on the output signal. Another control method, the so-called “jerk control”, is an additional predictive component, which is, in fact, the coefficient of the “derivative of the derivative” of the error signal of the feedback and the reference voltages. It is used to optimize the rate of change of the output voltage so that no abrupt changes in the output voltage are allowed to occur and induce voltage spikes. Similar to the effect of the derivative term, it will generate additional phase lead for the loop response of the system in the frequency domain.

The overall control algorithm is formulated as

$$y[n] = K_I y[n-1] + K_P e[n] + K_D e[n-1] + K_J e[n-2] + K_{ffi}[n] \quad (5.1)$$

5.2 Architecture of Integrated Digital DC-DC Buck Converter

where $e[n]$, $e[n-1]$ and $e[n-2]$ are the digital equivalents of the present value of the output voltage error, the errors of one and two switching cycles before, respectively. K_I , K_P , K_D , K_J and K_{ff} are the gain coefficients of the integral, proportional, derivative, predictive or jerk, and feedforward control, respectively. The selection of the values for the gain coefficients will be explained in Section 5.3.

5.2.2 Digital Pulse-width Modulator (DPWM)

The DPWM of the digital DC-DC converter can generally be realized in three ways. First, it can be realized using the counter comparator technique (Wei and Horowitz, 1996), which utilizes a counter to count the number of clock cycles required to generate the pulse of the PWM signal. Put differently, the count value is proportional to the input digital codes as well as the duty cycles of the PWM signal. However, one major disadvantage of this technique is that the clock frequency of the counter has to be doubled for every 1-bit increase in resolution. This will increase the power consumption substantially when the DPWM resolution is high. The second way to implement the DPWM is the ring oscillator-multiplexer or tapped delay-line technique (Dancy et al., 2000, Xiao et al., 2003), where the delay of each delay element in the ring oscillator is equivalent to 1 least-significant-bit (LSB) delay. In this technique, the hardware will be doubled for every 1-bit increase in resolution, thereby increasing the IC area substantially if the resolution is high. The third method, also known as the hybrid ring-mux approach (Patella et al., 2003), is a combination of the first and second methods. This approach is more prevalent for three primary reasons: a smaller IC area, lower power operation, and higher resolution.

To achieve an even higher resolution and a smaller IC area, the proposed hybrid-segmented approach described in Chapter 3 is adopted, as depicted in Figure 5.3. In the 12-bit hybrid-segmented architecture, the input, $D[11:0]$, is the digital command from the digital PFPID controller. The first segment $D[2:0]$ is used to drive the counter comparator while the next segment $D[5:3]$ is used to reset the PWM through a D flip-flop. The last segment $D[11:6]$ is connected as the reference code for the counter comparator.

5.2 Architecture of Integrated Digital DC-DC Buck Converter

Figure 5.3: High-resolution 12-bit DPWM with delay cell reuse technique

Figure 5.4: Low-voltage differential delay cell and supply insensitive replica biasing

This hybrid-segmented approach is more area-efficient than the conventional approach because it uses fewer delay cells for the same resolution. In the proposed design, the number of delay cells is further reduced by reusing the $1\times$ delay cells for the second multiplexer input. For the 12-bit DPWM, the 6 LSBs implemented with the hybrid-segmented architecture requires only 20 delay cells, whereas the ring-mux approach would require 32 differential delay cells. This will provide about 37.5% saving in IC area. With the proposed delay cell reused technique, the oscillating frequency is also increased by 75% due to the dual feedback of the segmented ring oscillator. Consequently, this will lead to a proportional increase in the switching frequency and a lower power consumption concurrently.

5.2 Architecture of Integrated Digital DC-DC Buck Converter

Figure 5.5: Architecture of the windowed SAR ADC with an internally auto-zero comparator

The schematic of a low voltage differential delay cell adopted in the DPWM is depicted in Figure 5.4. To stabilize the bias current, the replica bias circuit utilizes an op-amp to control the bias current of M8 by means of negative feedback. The dimension of M8 is identical to M7 of the differential delay cell to maintain the same bias current in both circuits. The op-amp is realized by a two-stage design with a proper start-up circuit. Stability is further improved by connecting a compensation capacitor, C_1 to the gate of M8.

5.2.3 Analog-to-Digital Converter (ADC)

The ADC employed in the design is a windowed successive approximation (SAR) ADC using an ultra-fast, offset-cancelled, auto-zero comparator described in Chapter 4 and depicted in Figure 5.5. The SAR ADC has a dynamic reference voltage range to reduce power consumption. The auto-zero scheme of the comparator is realized internally with a preamplifier stage and a latch stage. Since the error signal is small most of the time, a full-range ADC is not necessary. This is because the output voltage is generally a constant except during transient. Even in the transient period when there are changes in the load or line voltage, the output voltage will typically vary in a limited range around the desired output voltage. Therefore, the input range of the ADC is defined

5.2 Architecture of Integrated Digital DC-DC Buck Converter

Figure 5.6: Two-stage (preamp and latch) comparator with an internal auto-zero scheme

between an upper limit, V_{upper} and a lower limit, V_{lower} . This has the significant advantage of reducing the power consumption as the voltage across the capacitors is smaller.

The windowed SAR ADC requires eight clock cycles for data conversion. During the first clock cycle, data are sampled at the input ports. For the second clock cycle, data are being held. Next is the bit cycling process: output bits are being determined for each clock cycle from MSB to LSB. Finally, at the eighth clock cycle, data are being output and the conversion process iterates. In this case, the clock frequency is 32 MHz and thus, the conversion rate is 4 MSPS. This conversion rate is chosen to reduce the delay that causes phase lag to the frequency response while maintaining low dynamic power consumption. This conversion rate is chosen to reduce the delay that causes phase lag to the frequency response while maintaining low dynamic power consumption.

The two-stage comparator with internal auto-zeroing is depicted in Figure 5.6. The comparator consists of a preamplifier and a latch. The preamplifier is similar in structure to a dynamic folded cascode amplifier. The capacitances shown at the gate of M8 and M9 are the parasitic capacitances at the nodes. When ϕ_1 is high during auto-zero, the output impedance of the preamplifier, Z_1 , represents a low impedance node to ground. Thus the output of the preamplifier is auto-zeroed rapidly. However, when ϕ_1 is low during comparison, Z_1 increases to approximately $1/g_{ds9}$. Therefore, the comparator will have adequate gain to achieve fast response.

Figure 5.7: Output voltage precision against DPWM and ADC resolution

To prevent limit-cycle oscillation at the output of the converter, the resolution of the DPWM block must be greater than that of the ADC (Peterchev and Sanders, 2001). Under this condition, simulations are performed to determine the optimum resolution of the DPWM and ADC. The simulation results of the output voltage precision against the resolution of the DPWM and ADC are depicted in Figure 5.7. From system simulation with parasitic components (ESRs of the inductor and capacitor) in HSPICE, it is found that the precision of the output voltage increases significantly as the resolution of the DPWM and the resolution of the ADC increase. The optimum precision is reached when the DPWM is 12-bit and the ADC is approximately 11-bit. Beyond this, there is not much effect on the precision when the resolution increases as the output ripple starts to dominate and becomes the limiting factor for continuous reduction of the step size. The kinks in Figure 5.7 are due to the nonlinearity of the DC-DC converter with the parasitic components. Some parameters of the DPWM and the SAR ADC in the design are summarized in Table 5.1. Note that the high resolution of the DPWM and the ADC leads to high output voltage precision of the digital DC-DC converter.

5.3 PFPID Control for Fast-transient Digital DC-DC Converter

Table 5.1: Parameters of the DPWM and the windowed SAR ADC

Parameter	Value
ADC Quantization Step	2 mV
Window ADC Quantization Range	64 mV
Effective ADC Resolution	10.7 bits
DPWM Step Size	0.8 mV
Effective DPWM Resolution	12 bits

5.3 PFPID Control for Fast-transient Digital DC-DC Converter

In the conventional PID controller, there are three gain coefficients, namely, the proportional gain (K_P), the derivative gain (K_D), and the integral gain (K_I). First, the proportional gain directly affects the loop gain of the DC-DC converter and therefore controls the system stability. The second gain coefficients, the derivative gain, directly influences the settling time and the overshoot. Third, the integral gain reduces the steady-state offset errors. These three gain coefficients are tuned to achieve the desired transient performance. However, there are several limitations associated with PID control. It generally does not provide the optimal transient response, and the overshoot in PID control is typically high if the loop gain is large. Besides, when PID control is adopted in a non-linear system, it is generally overdamped to reduced overshoot which, in turn, increases the settling time. Put differently, the PID control trades off settling-time for reduced overshoot or vice versa in the control of non-linear system. As DC-DC converter is inherently non-linear, the use of PID control in the digital DC-DC converter yields sub-optimal performance. Thus, to circumvent the limitations of the conventional PID control, a PFPID control that is a combination of two control schemes: the predictive PID (PPID) control and the feedforward (F) control, is proposed for the control of DC-DC converter.

5.3.1 Predictive PID Control

In the proposed predictive PID control algorithm, we have introduced an additional predictive or jerk term and the corresponding gain coefficient is K_J . Figure 5.8 depicts

Figure 5.8: Waveforms of the Predictive/Jerk PID control

the waveforms of the output voltage, V_o , and output current, I_o during a load transient. We note that the effect of the jerk term is to push the perturbed waveform of the output voltage back to the original ripple-like waveform. Thus, by introducing the jerk term in addition to the conventional PID, the DC-DC converter is able to achieve a faster settling time. In the continuous time domain, the new control output is:

$$y(t) = K_P e(t) + K_D \frac{de(t)}{dt} + K_I \int e(t) dt + K_J \frac{d^2 e(t)}{dt^2} \quad (5.2)$$

In the s-domain, the new transfer function $T(s)$ is given as:

$$T(s) = K_P + K_D \cdot s + K_I \cdot \frac{1}{s} + K_J \cdot s^2 \quad (5.3)$$

Note that the K_J term introduces left-half-plane (LHP) zero to the control function, $T(s)$, which provides phase lead to the loop response of the system. By using the bilinear transformation where $s = \frac{2}{T} \frac{z-1}{z+1}$, the transfer function $T(z)$ in the discrete domain can be derived as:

$$T(z) = K_P + K_D \frac{2}{T} \frac{z-1}{z+1} + K_I \frac{T}{2} \frac{z+1}{z-1} + K_J \left(\frac{2}{T} \frac{z-1}{z+1} \right)^2 \quad (5.4)$$

Figure 5.9: Implementation of Predictive PID control

The implementation of Equation (5.4) is illustrated in Figure 5.9, where K_1 , K_2 , K_3 , and K_4 are derived as:

$$K_1 = K_P + K_D \frac{2}{T} + K_I \frac{T}{2} + K_J \frac{4}{T^2} \quad (5.5)$$

$$K_2 = K_P - K_D \frac{2}{T} + 3K_I \frac{T}{2} - 3K_J \frac{4}{T^2} \quad (5.6)$$

$$K_3 = -K_P - K_D \frac{2}{T} + 3K_I \frac{T}{2} + 3K_J \frac{4}{T^2} \quad (5.7)$$

$$K_4 = -K_P + K_D \frac{2}{T} + K_I \frac{T}{2} - K_J \frac{4}{T^2} \quad (5.8)$$

where T is the clock period. In Figure 5.9, $u[n]$ is the control input and $y[n]$ is the control output of the PPID controller. The coefficients, K_1 , K_2 , K_3 , and K_4 can be implemented using a look-up table instead of multiplication circuits to achieve lower power consumption and smaller IC area. From Equations (5.5) to (5.8), note that there are four parameters to be designed as opposed to the three gain coefficients of the conventional PID. This introduces one more degree of freedom which can be leveraged to mitigate the settling-time problem of the conventional PID. K_J is typically selected such that the location of the zero is approximately 50 times smaller than the switching frequency. This is because if K_J is too small, the effect of the zero is negligible at the system bandwidth. On the other hand, if K_J is too large, the zero will affect the system stability by allowing noise and ripple to fall into the increased bandwidth, and thus the system becomes noise-sensitive. This will be further explained in Section 5.4.

Figure 5.10: Schematic of the power stage of a synchronous buck converter

5.3.2 Feedforward Control

Figure 5.10 shows the power stage of a synchronous buck converter, which has three possible states. In the first state, the PMOS switch, S_1 is on and the NMOS switch, S_2 is off. The left side of the inductor is connected to the input voltage. The capacitor, C is being charged. Assuming r_L and r_C are small, we have:

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{v_i - v_o}{L} \quad (5.9)$$

$$\frac{dv_o}{dt} = \frac{dv_c}{dt} = \frac{i_c}{C} = \frac{i_L - i_o}{C} \quad (5.10)$$

where i_L is the inductor current, v_C is the capacitor voltage, and i_C is the capacitor current. In the second state, S_1 is off and S_2 is on. The energy stored in L will be released to the load. Thus, we obtain:

$$\frac{di_L}{dt} = \frac{v_L}{L} = -\frac{v_o}{L} \quad (5.11)$$

$$\frac{dv_o}{dt} = \frac{dv_c}{dt} = -\frac{i_c}{C} = \frac{i_o - i_L}{C} \quad (5.12)$$

In the third state, both S_1 and S_2 are off. This occurs during dead time of the power transistors. The inductor current is reduced to zero, and the load current is supplied from C . Thus, we can write:

$$\frac{di_L}{dt} = 0 \quad (5.13)$$

$$\frac{dv_o}{dt} = \frac{dv_c}{dt} = \frac{i_c}{C} = \frac{i_o}{C} \quad (5.14)$$

Figure 5.11: Typical waveform of i_L and i_{S2}

Figure 5.11 shows the typical waveform of i_L and i_{S2} , varying between $i_{L,max}$ and $i_{L,min}$. The feedforward control is done by estimating the area A_1 , when S_1 is on, and A_2 , when S_2 is on. A_1 represents the amount of charge from the inductor that is going to deliver to C to cause the change in output voltage when S_1 is on. Similarly, A_2 represents the charge supplied through S_2 to C . In the analysis, the amount of charge delivered to the load is not taken into account because the proportional change is small compared to that of capacitor, C . Thus, the change in V_o is mostly attributed to the change in the amount of charge delivered to the capacitor. The control scheme is elaborated as follows:

5.3.2.1 Generation of feedforward control when switching S_1 on

Assuming V_{dc} is the desired output voltage. The area of the shade A_1 can be derived as:

$$A_1 = \frac{V_{dc}(T_{on})^2}{2L} \quad (5.15)$$

S_1 tends to be switched off to ensure that i_L will not exceed $i_{L,max}$ in the subsequent switching cycle. Thus, the control output, $y(t)$, is derived as:

$$y(t) = -K_{ff} \cdot (i_{L,max}T_{on} - \frac{V_{dc}(T_{on})^2}{2L}) \quad (5.16)$$

Figure 5.12: Implementation of the feedforward control based on input current

5.3.2.2 Generation of feedforward control when switching S_2 on

The area of the shade A_2 can be derived as:

$$A_2 = \frac{V_{dc}(T_{off})^2}{2L} \quad (5.17)$$

and S_1 tends to be switched on so that i_L will not fall below $i_{L,min}$. Thus $y(t)$ is derived as:

$$y(t) = K_{ff} \cdot (i_{L,min}T_{off} + \frac{V_{dc}(T_{off})^2}{2L}) \quad (5.18)$$

The feedforward coefficient, K_{ff} is selected depending on the desired overshoot or undershoot. The typical range of K_{ff} is within $[1, 5]$. If K_{ff} is too large, the PPID feedback effect will be suppressed, and the error signal cannot be successfully reduced. On the other hand, if K_{ff} is less than one, the overshoot will start to increase as the overshoot limit is relaxed. The Equations (5.15) to (5.18) are implemented digitally. The implementation is depicted in Figure 5.12.

5.4 Simulation Results

Simulation results of the step-load transient of the DC-DC converter with the predictive and feedforward PID controller against the conventional PID are depicted in Figure 5.13. The simulations are run in Simulink, MATLAB with the developed model of the predictive and feedforward controller. Note that the settling time is reduced by approximately 50% and that the new overshoot is one-third of the overshoot of the conventional PID. The improvement can be explained by the Bode plot of the control-to-output transfer function of the DC-DC converter with the PFPID controller against

Figure 5.13: Simulation of the transient response of V_o and I_o

the conventional PID controller, which is depicted in Figure 5.14. In the Bode plot, both the unity-gain frequency and the phase margin have increased due to the additional LHP zero introduced by the predictive control (K_J term) at 20 kHz, which is 1/50 of the switching frequency of 1 MHz. Therefore, a faster transient response can be achieved.

Figure 5.14: Control-to-output frequency response of the DC-DC buck converter with the PFPID control against conventional PID control

In particular, note that in the gain plot, with the present of an additional zero at 20 kHz, the unity gain frequency increases from 100 kHz to 400 kHz. This is because

the additional zero reduces the roll-off of the magnitude plot from -40 dB to -20 dB after 20 kHz, which results in the increase of unity-gain frequency. However, further increase of the unity-gain frequency beyond 400 kHz will result in the the increase of noise due to the output ripple at the switching frequency of 1 MHz being fed back to the system. In the time domain, the increase of the unity-gain frequency to 400 kHz translates to a reduction in rise time during the transient period of the DC-DC converter.

From the phase plot, it is noted that the phase margin increases from 40° to 80° with the additional LHP zero. This yields a faster settling time and a reduced overshoot during transient because the closed-loop Q factor is related to the phase margin. Note that although the zero introduced by the PPID control generates a $+90^\circ$ phase change, the feedforward control cancels part of it in the vicinity of the switching frequency of 1 MHz due to the 180° out of phase of the feedforward signal and the feedback error signal, which results in the overall increase of phase margin of 40° . However, this is sufficient for the DC-DC converter and further increase of the phase margin may result in an overdamped response.

5.5 Experimental Results

The digital DC-DC converter based on the architecture in Figure 5.2 was designed and fabricated with Global Foundries CMOS 0.18 μm process. The microphotograph of the test chip is shown in Figure 5.15. The core area of the digital DC-DC converter including the power transistors is 1 mm^2 ($1\text{ mm} \times 1\text{ mm}$). The values for output filter: $L = 10\text{ }\mu\text{H}$ and $C = 10\text{ }\mu\text{F}$, $\text{ESR} = 1\text{ m}\Omega$. The test printed circuit board is depicted in Figure 5.16. The overall performance of the digital DC-DC converter test chip was measured in terms of (1) efficiency, (2) steady-state response, and (3) dynamic or transient response.

5.5.1 Efficiency

Figure 5.17 depicts the efficiency of the digital DC-DC converter against the load current, I_{out} . When I_{out} is lower than 40 mA, the digital DC-DC converter operates in PFM mode to reduce switching loss which dominates at low load current. The

Figure 5.15: Chip microphotograph of the digital DC-DC converter

Figure 5.16: Printed circuit board of the test chip

resulting efficiency is around 80%. When I_{out} increases beyond 40 mA, the digital DC-DC converter switches to PWM mode to prevent high conduction loss due to the parasitic resistance. The efficiency increases and peaks at 92% at a load current of 200 mA. However, when I_{out} exceeds 200 mA, conduction loss increases and thus the efficiency drops. At maximum load current of 500 mA, the efficiency reduces to 86%.

Figure 5.17: Measured efficiency against load current

5.5.2 Steady-state Performance

5.5.2.1 Load regulation

Figure 5.18: Measured load regulation (output voltage against load current)

Load regulation refers to the change of output voltage against the change of output current. The measurement results of the output voltage of the DC-DC converter against output current for different input voltages are depicted in Figure 5.18. Note that for the proposed design, the output voltage varies within a narrow range of 0.42% of the desired voltage of 1.2 V. In addition, the parabolic characteristic of the curves in Figure 5.18 is

Figure 5.19: Measured line regulation (output voltage against input voltage) at load current of 500 mA

due to the bandgap circuit included in the test chip. This is because the temperature of the test chip rises when the load current increases as the power dissipation increases due to the higher conduction losses. The bandgap reference has a parabolic characteristic with respect to temperature.

5.5.2.2 Line regulation

Line regulation is defined by the change of output voltage against the change in input voltage. The measured output voltage against the change in input voltage ranging from 1.8 V to 3.6 V is depicted in Figure 5.19. Note that the maximum deviation of the output voltage is 0.5%.

The high output voltage precision of the load and line regulation verifies the performance of the high resolution DPWM and ADC embodied in the proposed architecture of the digital DC-DC converter depicted in Figure 5.2.

5.5.2.3 Input and output ripples

The output ripple of the digital DC-DC converter at input voltage of 3.3 V is shown in Figure 5.20. Note that the output ripple is 1.5 mV. The input ripple of the digital

Figure 5.20: Experimental waveform showing the output voltage ripple when $V_{in} = 3.3\text{ V}$

Figure 5.21: Experimental waveform showing the input voltage ripple when $V_{out} = 1.2\text{ V}$

DC-DC converter at the input voltage of 3.3 V is shown in Figure 5.21. The input ripple is approximately 10 mV .

5.5.3 Dynamic Performance

5.5.3.1 Start-up and rise time

Soft-start is needed to prevent excessive current flowing to the load during start-up. The input and output voltages of the digital DC-DC converter during start-up are shown in Figure 5.22. The start-up time is approximately 10 ms and the rise time (from 10% to 90% of final V_o) is approximately 15 ms .

Figure 5.22: Digital DC-DC converter start-up

Figure 5.23: Load transient response of the digital DC-DC converter (load current changes from 500 mA to 50 mA)

5.5.3.2 Settling time and overshoot

The load transient responses of the digital DC-DC converter from 500 mA to 50 mA and from 50 mA to 500 mA are depicted in Fig. 5.23 and Fig. 5.24, respectively. Note that the settling time is $3.5 \mu s$ and the undershoot is 10 mV for high-to-low load transition while the settling time is $4 \mu s$ and the overshoot is approximately 15 mV for low-to-high load transition. The line transient response is shown in Fig. 5.25 when input voltage changes from 2.3 V to 3.3 V. The settling time is $3.5 \mu s$ and the overshoot is 15 mV.

A comparison of the characteristics of the digital DC-DC converter with respect to the prior arts is tabulated in Table 5.2. Note that the proposed design has achieved the fastest transient response of $4 \mu s$, which is comparable to (Trescases et al., 2011). This is because of the increase in the unity-gain frequency and the improved phase margin due to the predictive control. (Trescases et al., 2011) also achieves a very fast transient of $4 \mu s$ due to the mixed-signal current mode control. The proposed digital

Figure 5.24: Load transient response of the digital DC-DC converter (load current changes from 50 mA to 500 mA)

Figure 5.25: Line transient response of the digital DC-DC converter (input voltage changes from 2.3 V to 3.3 V)

DC-DC converter achieves the lowest overshoot of 15 mV as compared to the prior arts, because the feedforward control successfully limits the overshoot and undershoot to the desired values. As the building blocks such as the windowed SAR ADC and the hybrid-segmented DPWM consume low power, the design has an efficiency of 92%. In addition, the proposed DC-DC converter exhibits high output voltage precision and low ripple with a small IC area due to the high-resolution DPWM and ADC. However, the switching frequency is lower than (Trescases et al., 2011) and (Soenen et al., 2010) that allow the use of a smaller output inductor and capacitor. On the other hand, (Xiao et al., 2001) has a low quiescent current of 4 μ A in PFM mode, which allows high efficiency at light-load.

This chapter discusses a digital DC-DC converter with predictive and feedforward control, which has a low overshoot and short settling time. This is because the predictive

term and its corresponding gain coefficient introduce LHP zero to increase the unity-gain frequency and improve the phase margin of the control-to-output response of the digital DC-DC converter. Two alternative digital controllers will be shown in Chapters 6 and 7 to mitigate the performance degradation due to process variation and minimize the resources needed for the controller.

Table 5.2: Comparison of the characteristics of the proposed digital DC-DC converter with respect to prior arts

	This work	Trescases	Soenen	Luo	Xiao	Patella
Year of publication		2011	2010	2009	2004	2003
CMOS process (μm)	0.18	0.18	0.04	0.35	0.25	0.5
Input voltage range (V)	1.8–3.3	3.6	0–3.3	2.2–3.3	2.8–5.5	4–6
Output voltage range (V)	1.2	1	0.1–3.3	1.5	1.0–1.8	2.7
PWM switching frequency (MHz)	1	3	3.125	1	0.5–1.5	1
Maximum load current (mA)	500	500	1000	100	400	1500
Output voltage ripple (mV)	1.5	10	5	12.5	2	25
Quiescent current	20 μA	–	1mA	–	4 μA	–
Load regulation	5/450	45.4/400	20/250	–	16/100	25/700
Line regulation	8/1800	–	15/250	29.1/1000	–	25/1500
Peak efficiency	92%	91.3%	90%	91%	89%	–
Overshoot (mV)	15	50	20	169.4	40	100
Settling time	4 μs	4 μs	1ms	10.2 μs	200 μs	80 μs
Output voltage deviation	$\pm 0.5\%$	–	–	–	$\pm 0.8\%$	$\pm 1.8\%$
(1 - Output voltage precision)						
Active chip area	1mm ²	0.07mm ² *	0.7mm ²	1.31 mm ²	2 mm ²	0.81mm ²

* area for controller only (excluding power transistors)

Part IV

**Design on Adaptive, Hardware-Efficient
Digital DC-DC Converters Based on
FPGA**

Chapter 6

Adaptive Optimal Controller Based on Genetic Algorithm for Digital DC-DC Converters

6.1 Introduction

A large portion of this chapter is extracted from a paper presented in 20th IEEE International Symposium on Industrial Electronics (ISIE 2011) (Foong *et al.*, 2011e) co-authored by the author of this thesis.

Conventional methods of designing the digital controllers adopt manual tuning to optimize the transient response of DC-DC converters. The Ziegler-Nichols method is a widely used online tuning method. However, this method is time-consuming and may not achieve the optimal solution. (Corradini *et al.*, 2008c, Morroni *et al.*, 2009) have proposed the adaptive tuning method of the digital controllers, but they also suffer from the same problems as the Ziegler-Nichols method.

Among other different control algorithms and optimization methods, genetic algorithm (GA) is an appealing choice especially when it is implemented digitally. In most occasions, engineers entail feedback loop compensation to check the stability of a system (Venable). However, little effort is carried out to optimize the control system. Even if the system is optimized during simulation, there is no guarantee that the performance

will match after fabrication. In fact, in the design of a DC-DC converter IC, the loop gain and phase deviate after fabrication due to process variation. Temperature will also affect the frequency response when the chip is in operation. Therefore, an adaptive tuning system is required to achieve the desired transient response by optimizing the controller. One of the adaptive tuning methods is genetic algorithm.

Prior arts of the DC-DC converter optimization adopt GA in the time domain (Kostov and Kyra, 2005, Femia et al., 2002). These involve reducing the error signal over time to optimize the performance. However, this method can only be done off-line, meaning that after fabrication, it will require some manual trials or calibrations beforehand in order for the controller to determine the optimized parameters. This will increase the cost and production time. Furthermore, the trial conditions may differ with the actual operating conditions due to temperature variation.

The proposed genetic algorithm controller investigates optimization in the time domain in terms of the integral of time and absolute error (ITAE). This approach eliminates the need of calibration and reduces the time-to-market. This is made feasible by estimating the model using a state estimator and updating it on-the-fly. Based on the model determined, the proposed genetic algorithm is then being run to achieve optimization by reducing the cost function.

The remainder of this chapter is organized as follows: An overview of the genetic algorithm will be given in section 6.2. Section 6.3 presents the proposed GA controller for digital DC-DC converters. Section 6.4 elaborates the simulation results of the proposed design. Section 6.5 demonstrates implementation and measurement results. Finally, Section 6.6 summarizes the overall findings.

6.2 Background of Genetic Algorithm

Genetic algorithm or GA is a search technique used to find an approximate solution for optimization of a particular problem. The idea of GA is similar to that of evolution in nature. One main advantage of GA is that only objective function evaluations are needed instead of a complete knowledge of the system. Hence, it is useful for complex optimization problems with a large number of parameters that results in difficulty in

obtaining global analytical solutions. In this chapter, a genetic algorithm is proposed to find the optimized coefficients of the PID controller of a digital DC-DC converter in a reasonably short time. A possible solution to a genetic algorithm optimization problem is called a chromosome, and it is an individual of a pool of solutions. Individuals are improved by various operators, especially the fitness function, crossover and mutation. The necessity of employing genetic algorithm in most cases is that we do not have the exact information of the model of the DC-DC converter (Middlebrook and Cuk, 1977b, Sanders and Vergese, 1991) before integrated circuit or printed-circuit board fabrication. Furthermore, the model of a converter deviates after fabrication due to parasitic resistors, capacitors, and inductors. Another advantage is that, by adopting GA, the bandwidth of the controller can be tuned freely such that the system can perform faster during transient.

A new generation is created when fitter individuals reproduce. This is done with operators such as selection, crossover and mutation. Crossover and mutation are sometimes grouped together and termed recombination. The newly created individuals may be fitter than individuals from the previous generation. The cycle is repeated such that the population is continuously updated with new individuals. After a specified number of generations are reached or a particular fitness value is achieved, the iteration stops and the fittest individual will approximate the optimal solution.

A typical GA algorithm consists of the following steps:

6.2.1 Initialization

The chromosomes of individuals in a population can be encoded as a binary string or as a real-value string. (Michalewicz, Huang and Shi, 1996) represent the chromosome as a more precise real-value parameter instead of a binary string. Moreover, it can be directly used to evaluate its fitness value without transforming it from binary value to real value. Therefore, creating the population would require less memory if real-values are used instead of binary values.

Boundaries can be defined for each chromosome so that an optimal solution is found in fewer generations of the GA. However, the range of the boundaries must not be excessively small so that the individual solutions will not be too similar in order to

prevent the solutions to converge quickly to a local minimal without finding the global optimal solution. The range should not be overly large as well, otherwise the population is extremely diverse and many generations are needed before a satisfactory result is achieved.

6.2.2 Fitness Evaluation

Fitness evaluation is largely dependent on the system. In simpler implementation of GA, such as for finding the minimum of a function, the function itself can be used to calculate the fitness value for an individual. Moreover, the fitness values can be normalized, scaled, shared or left unchanged. Often, a cost function, equals to the inverse of the fitness value, is employed. Hence, the aim of the GA would be to find a solution with the lowest cost or highest fitness value.

6.2.3 Selection

Individuals with higher fitness values will have a higher chance of reproducing offspring while individuals with lower fitness may not contribute to the next generation. However, less fit individuals may have a smaller chance of being selected as parents in some selection methods such as the roulette wheel selection and tournament selection (Zhong, 2005). This may be desirable so that the population is diverse and good solutions are not lost before the optimal solution is determined.

In roulette wheel selection, the probability of survival for an individual is equal to its fitness divided by the sum of the fitness of all individuals. For tournament selection, individuals who are the winners of a scheduled tournament would be selected for the next generation.

Another method of selection is truncation selection (Chaiyaratana and Zalzala, 1997), where a certain best proportion of individuals in the population is selected as parents.

6.2.4 Reproduction

Reproduction involves the crossover and mutation of genes from two parents to produce a child. In this way, the child has genes that come from both parents through crossover, with the possibility that it will become fitter, while mutation introduces variety in the solutions to prevent early convergence. Hence, the next generation will be made up of individuals with gradually increased fitness.

There are many other ways that crossover may be done. Common crossover methods include simple crossover, arithmetic crossover and heuristic crossover. In simple crossover, a single point crossover is randomly selected in the form of a cut point, and the chromosomes of the child before the cut will come from one parent while those after the cut will be contributed by the other parent. For arithmetic crossover, an interpolation along the line formed by the two parents is performed. Hence, the child formed will have values that lie somewhere between its parents. The heuristic crossover method performs an extrapolation along the line formed by the two parents outwards in the direction of the better parents. Thus, the child takes values that are closer to the fitter parent.

Mutation may also be performed in a number of ways. Some common mutation methods are boundary mutation, uniform mutation and nonuniform mutation (Kostov and Kyyra, 2005). In boundary mutation, one of the parameters of the parent is changed randomly to either its upper or lower bound. If uniform mutation is performed, one of the parameters of the parent is changed based on a uniform probability distribution. Lastly, in a nonuniform method, one of the parameters of the parent is changed based on a nonuniform probability distribution, such as the Gaussian distribution. The distribution starts broadly and narrows to a point distribution as the current generation tends to the maximum generation.

The crossover and mutation operators come with a probability of occurring. This means that an individual may be subjected to crossover and mutation based on the probability of crossover and mutation. In general, the probability of crossover is high while that of mutation is low.

6.2.5 Termination

The genetic algorithm terminates when the termination condition is satisfied. The condition can be one or more of the following:

1. A maximum number of generations is reached.
2. The fitness value satisfies the predefined required fitness.
3. The solutions converge and further iteration does not result in better solutions.

The first and second termination conditions are normally used in GA as they are relatively easier to implement in code. However, it is noted that a suitable maximum number of generations and an appropriate fitness level must be determined for the GA procedure to terminate.

6.3 Proposed GA Controller for DC-DC Converter

6.3.1 Outline of Genetic Algorithm Program

The GA program begins by randomly initializing the population within specified bounds. Then, the genes of each individual in the population are passed to the model for simulation. The fitness value of each individual is evaluated from the output of the model and stored in the program. Following this, the generation number is incremented and the population is sorted according to the fitness value, with the fittest at the starting index of the array. Parents are then selected from the population to produce children that will constitute the next generation. The parent individuals are also carried forward to the next generation. The fitness of the children is then evaluated and stored. If the termination condition has not been reached, the process continues by incrementing the generation, sorting the population, selecting parents for recombination and forming the new population. Figure 6.1 depicts the flowchart of the proposed GA procedure.

6.3.2 Parameters and Operators in the GA Program

The parameters used for the GA program are listed in Table 6.1. Genetic algorithm parameters such as the crossover probability, the mutation probability, and the elitism

6.3 Proposed GA Controller for DC-DC Converter

Figure 6.1: Flowchart of the proposed GA procedure

Table 6.1: Parameters for Genetic Algorithm

Number of generations	50
Population size	100
Number of best individuals passed on to the next generation (elitism)	40
Crossover probability	0.60
Mutation probability	0.00

probability can be chosen randomly between 0 and 1. However, these parameters will affect the rate of convergence to achieve optimal performance based on the model of a digital DC-DC converter. Thus, in the simulation, it is assumed only crossover exists and there is no mutation in the population to simplify the model. A moderate value of 0.6 has been chosen for the crossover probability and a moderate value of 0.4 (40 out of total population of 100) has been chosen for the elitism probability as these values typically represent the population. The flow of the proposed GA based controller is as follow:

6.3.2.1 Initialization

As mentioned in Section 6.2, real-value strings are chosen to represent the chromosomes as they will reflect more accurately the real-value parameters, in this case the parameters of a PID controller.

Since PID controllers are the main focus in the design of an optimal controller, the parameters to be optimized are identified as the proportional gain, integral gain, and derivative gain. Thus, each solution in the GA population is set to have three chromosomes, will be represented by K_P (proportional gain), K_I (integral gain), and K_D (derivative gain).

K_P , K_I , and K_D for each individual are assigned random values within the bounds $[0, 0.1]$, $[990, 2000]$ and $[0, 0.1]$, respectively. These boundaries are chosen after a few trial simulations as the PID parameters that lie within the stated range were found to provide a fair system response. Using boundaries that contain good solutions can help to achieve better simulation results within a smaller number of generations. The small range of the initial population will later demonstrate that, as the generation increases, individuals may take values that lie outside of the boundaries.

At the start of the program, the fitness value of all individuals is set to zero. This value will be updated when an individuals fitness is determined after fitness evaluation.

6.3.2.2 Fitness evaluation/Cost evaluation

In the case of a digitally-controlled DC-DC converter, it is desirable to have a constant steady-state voltage output. Conversely, it is undesirable for the voltage output to differ largely from the required voltage level. Equation (6.1) shows how the error voltage, v_e is calculated, where v_o is the time-varying voltage output and V_o is the constant desired voltage.

$$v_e = v_o - V_o \quad (6.1)$$

In steady-state v_e is equal to zero. However, when there is any perturbation in the supply or load of a DC-DC converter, v_o is not equal to V_o and thus v_e is non-zero.

6.3 Proposed GA Controller for DC-DC Converter

From the error, the cost function of the GA-based PID controller is defined as in Equation (6.2).

$$Cost = \int_0^T t|v_o - V_o| dt = \int_0^T t|v_e| dt \quad (6.2)$$

From Equation (6.2), it can be seen that the cost is identified as the cumulative sum of the absolute output voltage error v_e , which is also known as integral time absolute error (ITAE). The rationale is that the error has to be minimized. Hence, the controller with the smallest total error in voltage is deemed to be the fittest. In the program, the cost is scaled by a multiple of 1,000 so that the values would be larger and comparison is easier among the individuals.

The cost function, J in the discrete domain is:

$$J = \sum_{k=1}^n k|error(k)| \quad (6.3)$$

Figure 6.2 illustrates how the cost is represented in a plot of the voltage output against time. The solid line in the graph represents a constant voltage of 5 V, which is the desired voltage output, while the area in yellow represents the total difference between the simulated voltage output and the desired value. Hence, the integral function can be used to obtain this area.

The rise in output voltage from 0 V to 5 V is not of concern as the output voltage for a digital DC-DC converter during the start-up time is typically controlled by the soft-start function. Hence, only the cumulative voltage error after the output voltage has reached the required 5 V need to be considered in the fitness evaluation. Thus, in Figure 6.2, only A_2 and A_3 are used to compute the fitness values.

Since the cost function is the inverse of the fitness function, for simplicity of ranking the solutions, the cost function is used instead of the fitness function in the implementation of GA. Hence, the controller with a lower cost has higher fitness and thus a better performance.

Figure 6.2: Area representing cumulative error

6.3.3 Selection

In the GA implementation to design an optimal digital PID controller, the truncation selection method (Chaiyaratana and Zalzal, 1997) is used to select parents for the next generation. The best 40 out of 100 individuals form the parent group. Individuals that form the better half of the parents are assigned as ‘dad’, while their corresponding ‘mom’ is chosen at random from the whole parent group, excluding the particular ‘dad’. Hence, the best 20 individuals have guaranteed parenthood, whereas individuals ranking between 21 and 40 have a random chance of being a parent. Individuals will also not be paired with itself. Equation (6.4) gives the relationship between the population size, N_{pop} , and the number of parents, N_{par} .

$$N_{pop} = \frac{5}{2} \times N_{par} \quad (6.4)$$

The entire parent group is unchanged in the population, and this is known as elitism since the best individuals in one generation are kept in the next generation. The remaining places in the population are then filled by the children. Figure 6.3 illustrates the change in the population from one generation to another.

Figure 6.3: Comparison between the composition of one generation and the next

The reason for choosing this type of selection method is that, when crossover is done, the resulting child may not necessarily be fitter than its parents. Thus, replacing a large proportion of the population with children does not seem practical. Using the aforementioned way of selecting parents and placing them in the next generation ensures that a relatively large percentage (40%) of the new generation is made up of the best individuals from the previous generation. This is opposed to other selection methods that replace almost the whole population with child solutions.

6.3.4 Recombination

For crossover, a variation of the linear crossover method (Kostov and Kyyra, 2005) was used to produce three children by each set of parents. The children are obtained by Equation (6.5) to (6.7), where r is a random number in the interval $[0, 1]$.

$$child_1 = r \times mom + r \times dad \quad (6.5)$$

$$child_2 = (1 + r) \times mom - (1 - r) \times dad \quad (6.6)$$

$$child_3 = (1 + r) \times dad - (1 - r) \times mom \quad (6.7)$$

In the equations, the child inherits a random amount of its genes from its ‘dad’ and ‘mom’. Therefore, mutation is not needed since an amount of variability is already introduced by the random number, r .

The recombination used in the program differs from that in (Kostov and Kyyra, 2005) as r used is a scalar instead of a vector with length equal to the number of genes of the child. From simulation, it was found that using a random vector in recombination results in large variations of the children, such that the children are significantly different from their parents. Hence, a single random number, r , is used in recombination.

If the genes of the child fall below the lower bound after crossover, that particular gene is randomly generated to be within the initial boundary. This step is necessary as the crossover may result in children with unacceptable PID gains, such as negative proportional gain, or small integral gain. Hence, their fitness would be very undesirable and consequently bring down the average fitness of the population. The parameters of the children are not limited by the upper bounds as a combination of proportional, integral and derivative gains can produce optimal system response, regardless of how large the gain is. Despite this, not constraining the child parameters to be within a certain range may cause poor performance for the controller.

6.3.5 Termination

The maximum number of generations was chosen as the termination condition. This is because it is difficult to determine the required fitness to be reached before the GA terminates. In addition, if a required fitness was set, it is undesirable for the iteration to continue searching for too long for an individual to meet the specified fitness, or iterate for too few generations such that the solution found may not be optimal.

In the design, the maximum number of generations was set at 50. After 50 generations, the population had evolved to have significantly fitter solutions than the initial population. Further increase of the number of generations does not increase the best fitness significantly.

Figure 6.4: Area representing total output voltage error

6.4 Simulation Results

Figure 6.4 depicts the transient response of the output voltage. The reason Area 1 is not used for fitness evaluation is that the output voltage does not reach a steady state at $t = 0.002$ s for some combination of K_P , K_I , and K_D . Other combinations of the PID parameters produce a steady state voltage output that is slowly increasing with time. At $t = 0.002$ s, the voltage output may not reach 5 V. It is only after the step load at $t = 0.002$ s and $t = 0.003$ s does the output voltage become more stable at close to 5 V. Hence, only the output voltage response to the step load at $t = 0.004$ s and $t = 0.005$ s are used to measure the fitness of the controller.

The load regulation simulation was done by pulsing the load from 1Ω to 2Ω with a frequency of 500 Hz. In the Simulink model, a step load is used in addition to a constant load of 1Ω . As the load switches, the load current is expected to change from 5 A to 2.5 A.

Simulation is performed to obtain the fittest controller, based on the cost function in Equation (6.3). The fitness graph obtained is given in Figure 6.5. As the number of generations increases, it can be seen that the cost of the best solution in each generation decreases. Hence, the best individual in the generation gradually becomes fitter. Fur-

Figure 6.5: Cost function graph for different generations

Table 6.2: Parameters of four generations from simulations

Generation	K_p	K_I	K_D	Cost
1	3.1721	1.7992e+03	2.1579	0.010215
2	3.9597	2.1663e+03	4.6760	0.010209
3	3.5039	1.9280e+03	15.8160	0.010175
4	3.4856	1.9023e+03	15.9230	0.010123

thermore, the best fitness does not change significantly in the later generations, which signifies that a near-optimal solution has been found such that further evolving of the individuals do not produce much fitter children.

The average fitness of the entire population has a generally increasing trend. However, the average fitness at generation 11 and 13 are considerably poor as compared to the rest of the generation. This could be because the way that the children are produced introduces an amount of variability, thus, the children produced in that those generations may be significantly poorer in performance compared to the previous generation and their parents. Towards the later generations, it can be seen that the average fitness increases and decreases slightly. This indicates that the algorithm is searching for

6.5 Implementation and Measurement Results

Figure 6.6: 1st Generation at $50\mu s$

Figure 6.7: 2nd Generation at $100\mu s$

fitter individuals in a larger space instead of converging about the fittest individual of a generation. The parameters of the three fittest controllers, rounded to the nearest 4 decimal places, are given in Table 6.2.

6.5 Implementation and Measurement Results

The proposed adaptive optimal DC-DC controller based on genetic algorithm is implemented using the Avnet Xilinx Virtex 4VLX25 evaluation board. Due to the frequency constraint of the 100 MHz clock signal from the onboard crystal, the switching frequency is limited to 390 kHz.

6.5 Implementation and Measurement Results

Figure 6.8: 3rd Generation at $150\mu s$

Figure 6.9: 4th Generation (Best Fit) at $200\mu s$

The waveforms showing the transient responses for the four generations are depicted in Figure 6.6 to Figure 6.9. Note that the digital DC-DC converter achieved optimal response within four generations (in $200\mu s$). The efficiency of the generic algorithm-based DC-DC converter is approximately 82% at a load current of 1A and 73% at a load current of 10mA.

This chapter presents the design of an adaptive optimal controller based on genetic algorithm (GA) for digital DC-DC converters. The GA controller has adopted the integral time absolute error (ITAE) of the output voltage as the cost function and achieved an optimal response within four generations and in a very short time.

Chapter 7

A Dual-Mode Digital DC-DC Converter Based on Distributed Arithmetic

7.1 Introduction

A large portion of this chapter is extracted from a paper published in the Proceedings of IEEE International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM 2010) (Foong *et al.*, 2011a) co-authored by the author of this thesis.

The existing controllers for digital DC-DC converters can be categorized into voltage-mode, current-mode, V^2 mode (Goder and Pelletier, 1996), and hysteretic controllers (Corradini et al., 2009). The control structure of the digital controllers is generally parallel in nature. Due to the high computation power required for digital controllers, two major drawbacks which impede the wide-spread use of digital DC-DC converters are the considerable amount of area and power required by the digital controller. This will result in the digital converter having lower efficiency and higher cost than its analog counterparts. (Patella et al., 2003) have proposed means of resolving this issue by adopting limited range of digital codes. However, several other problems will arise due to fewer codes being taken into account by the controller. In addition, the error

code falling outside the range during start-up and perturbation issue will limit the transient response of the DC-DC converter.

To provide high power efficiency for wider load range, a reconfigurable, multi-mode DC-DC converter with sophisticated control is needed to achieve optimum performance. In conventional architectures, the multi-mode digital DC-DC controller usually employs bit-parallel approach (Xiao et al., 2001) and the different controllers are connected in parallel. The controller for each mode is usually realized with several Look-Up Tables (LUTs) in bit-parallel manner. This will result in a large IC chip area which leads to higher cost and in general, lower power efficiency.

To circumvent this issue, a PID controller based on the distributed arithmetic (bit-serial) approach is proposed to circumvent the power, IC area, and start-up problems. Distributed arithmetic (Longa and Miri, 2006) has several advantages over the parallel approach due to its inherent scalability and memory reuse. This will allow the digital controller to operate in different operating modes such as Pulse Frequency Modulation (PFM), Pulse Width Modulation (PWM), pulse-skipping (Paul and Maksimovic, 2008a), and adaptive control (Monica et al., 2005, Acker et al., 1995) while the same memory is shared and reloaded for different operating modes. However, as the data in distributed arithmetic approach are computed 1-bit at a time, the clock speed of the controller has to be increased to maintain the same throughput.

For the same clock frequency, the proposed technique has lower throughput compared to the conventional (parallel computation) technique because of the serial computation. Therefore, the selection of the clock frequency has to be carefully considered to compromise between speed, resources, and power aspects. In the proposed design, the switching frequency is 390 kHz, and the distributed-arithmetic approach can meet the design requirement by having sufficient timing for the serial computation before the next switching cycle arrives when the code from the computation is used to determine the duty cycle of the PWM. The main advantages of the proposed technique are that it requires fewer computing resources and consumes less power.

This chapter is organized as follows: An overview of digital controller architecture will be given in Section 7.2. In Section 7.3, the design and analysis of DA-based controller

Figure 7.1: Proposed memory-reusable PWM/PFM current-mode DC-DC converter

will be elaborated. Section 7.4 presents the design and implementation of digital DC-DC controller. The simulation and measurement results will be presented in Section 7.5. Finally, Section 7.6 gives a summary of the overall findings.

7.2 Digital Controller Architecture

The basic block diagram of the proposed PWM/PFM current-mode DC-DC converter is depicted in Figure 7.1. The proposed controller operates in bit-serial nature with Distributed-Arithmetic Look-Up Table (DA-LUT) and employs memory reuse to optimize the IC area.

For the proposed memory-reusable current-mode DC-DC converter, the average current-mode control (Dixon, Mammano, 1994) is adopted to provide better line regulation, faster dynamic response and noise insensitivity. The operating principles of the proposed current-mode digital DC-DC converter are as follows: The DC-DC converter consists of five blocks, namely, the dual-mode digital current-mode controller, the Digital Pulse Width Modulator (DPWM), the Output Driver Stage, the Analog-to-Digital Converters (ADCs), and the LC lowpass filter. The two ADCs are used to sense the load current (through a current sensing circuit) and the output voltage of the DC-DC

7.3 Distributed Arithmetic Look-up Table (DA-LUT)

converter. In Figure 7.1, the load current and output voltage of the digital controller are denoted as the I information and the V information, respectively in the digital controller. The I information is used by the controller to decide the operating mode (PWM or PFM) and to generate the duty cycle command for the DPWM. On the other hand, the V information is first fed into the serializer before it is processed by the controller based on distributed-arithmetic look-up table. In average current-mode control, the difference between the sensed I information and output of the distributed arithmetic filter is passed through an averaging filter to produce the duty-cycle command for the DPWM. In our design, the sampling frequency of the ADC is four times of the switching frequency and thus allowed four samples of the inductor current to be averaged per switching cycle.

The primary advantage of the distributed arithmetic digital controller is its efficient way of utilizing the IC area and components in FPGA. By sharing the memory (DA-LUT) in the FPGA, the coefficients for PFM or PWM mode which are stored in a ROM (outside the FPGA) will be loaded onto the FPGA when the operating mode is changed. This will reduce the size of the Look-Up Table and save up the resources in the FPGA. This has also added a certain degree of reconfigurability to the compensator. The mode selection block will determine whether PFM or PWM is to be selected to optimize the efficiency of the DC-DC converter. In PFM mode, the peak of the ripple inductor current waveform is chosen as the threshold level for mode selection, as defined in Equation (7.1) where t_{on} is the constant width of the pulse in PFM.

$$I_{threshold} = \frac{t_{on}(V_{in} - V_{out})}{L} \quad (7.1)$$

7.3 Distributed Arithmetic Look-up Table (DA-LUT)

7.3.1 Overview of Distributed Arithmetic

Distributed Arithmetic is a bit-serial computation algorithm that performs multiplication using a Lookup Table-based scheme. Consider a sum of product calculation of

7.3 Distributed Arithmetic Look-up Table (DA-LUT)

order N , the output Y can be expressed as:

$$Y = \sum_{k=0}^{N-1} A_k x_k \quad (7.2)$$

Assuming that A_k are known values, x_k can be represented by:

$$x_k = -2^{B-1} \cdot x_{B-1} + \sum_{b=0}^{B-2} x_b \cdot 2^b \quad (7.3)$$

where x_b represents the b th bit position of the binary number. The binary representation has B bits. By substituting Equation (7.3) into (7.2), the Sum-of-Product can be represented as:

$$Y = \sum_{k=0}^{N-1} A_k (-2^{B-1} \cdot x_{B-1} + \sum_{b=0}^{B-2} 2^b \cdot \sum_{k=0}^{N-1} A_k x_b) \quad (7.4)$$

Hence, the output Y can be defined by:

$$Y = -2^{B-1} \cdot \sum_{k=0}^{N-1} A_k x_{B-1} + \sum_{b=0}^{B-2} 2^b \cdot \sum_{k=0}^{N-1} A_k x_b \quad (7.5)$$

7.3.2 Operation of DA-LUT

The operation of distributed arithmetic Look-up Table is depicted graphically in Figure 7.2. The DA-LUT table-based digital controller has a significant advantage in terms of area compared to other digital control methods. This is due to the application of bit-serial approach at the input and the adder-accumulator at the output.

A proposed state diagram illustrating how the DA-LUT is being controlled for dual-mode (PWM/PFM) operation is shown in Figure 7.3. The dual-mode control consists of five states for the PWM and PFM operation. The error code, Err is the difference of the reference code and the output info code, i.e. $Err = \text{output info} - \text{reference code}$.

The state diagram realizes a control algorithm that will determine the appropriate mode (PWM or PFM) based on the threshold level of the load current, $I_{threshold}$. When the output I information is greater than $I_{threshold}$, the DA-LUT will load in the PWM coefficients from ROM. Furthermore, if $Err < 0$, the controller will be in the up-state

Figure 7.2: Distributed-arithmetic LUT

and force the duty cycle to increase. However, if $\text{Err} > 0$, the controller will be in down-state and the duty cycle will be decreased. If the output I information is smaller than $I_{\text{threshold}}$, the controller will be set to the PFM mode and the DA-LUT will load in the PFM coefficients. Likewise, it will be in up-state when $\text{Err} < 0$ and in down-state when $\text{Err} > 0$. In stable state, $\text{Err} = 0$ and the output voltage will be determined by the reference code. As shown in the state diagram in Figure 7.3, the controller allows bidirectional mode-switching between the PFM and the PWM modes based on the load current condition. This offers the versatility to achieve optimum efficiency.

7.4 Design and Implementation of DC-DC Controller

In the actual design, PID control has to be employed to achieve stability and to improve the transient performance. There are two different methods for designing a PID

Figure 7.3: State diagram of the dual-mode DC-DC controller

controller, namely (1) the indirect method, where continuous-to-discrete conversion is required, and (2) the direct digital design method (Hande and Kamalasadan, 1997).

For fast prototyping, the indirect method is adopted. The PID controller is first designed in continuous domain before it is converted into the discrete domain using bilinear transformation. There are several other transformations such as forward Euler transformation and backward Euler transformation, but bilinear transformation chosen because it is able to preserve the stability of the system. A well-performed DC-DC converter should have an open-loop phase margin of at least 45 degrees to remain stable and to achieve a good transient response.

The controller function in z-domain can be derived as:

$$T(z) = \frac{1.17z - 0.9524}{z^2 - z + 0.0004697} \quad (7.6)$$

The implemented transfer function has two poles and one zero which is typical of type II DC-DC converter (Basso). This results in a phase margin of 90° as shown in the bode plot of the open loop converter system depicted in Figure 7.4. The unity gain frequency is 50 kHz. The z-domain function is implemented using the described DA-LUT in Section 7.3. However, it consists of two sub-tables as depicted in Figure 7.5.

Figure 7.4: Bode plot of the open loop converter system

One table (DALUT-1) is for the input while the other table (DALUT-2) is for the feedback from the output.

7.5 Simulation and Measurement Results

The proposed dual-mode digital current-mode DC-DC controller is implemented using the Avnet Xilinx Virtex 4VLX25 evaluation board. Due to the frequency constraint of the 100MHz clock signal from the onboard crystal, the switching frequency is limited to 390 kHz for an 8-bit DPWM. The DA-LUTs operate at a clock frequency of 1.56 MHz, which is also the sampling frequency. A comparison of the power, speed and area between the proposed dual-mode digital current-mode DC-DC converter based on DA and a reported dual-mode DC-DC converter based on bit-parallel approach (Xiao et al., 2003) are tabulated in Table 7.1.

From Table 7.1, note that the number of FPGA slices and LUTs is reduced by 57% and 45%, respectively. The total area occupied is approximately 50% of the original design without DA. Power consumption is also reduced by 57.6% to 22 mW. The power consumption is reduced since fewer FPGA resources are utilized in the proposed design.

Figure 7.5: PID controller implemented in DA-LUTs

Table 7.1: Comparison of the proposed digital DC-DC converter and prior art at switching frequency of 390 kHz

	Without DA	Proposed approach with DA-LUT
AREA		
Number of slices	196	84
TIMING		
Critical path delay	$3.879\mu s$	$4.112\mu s$
POWER	52mW	22mW

The proposed architecture will also provide the same advantage for full custom IC implementation. The only drawback is that the critical path delay has been increased slightly as a trade-off.

The load transient waveform of the implemented DC-DC converter is shown in Figure 7.6. Note that the settling-time is $20\mu s$ for a maximum load step current change from 500 mA to 0 mA and $25\mu s$ for a maximum load step current change from 0 mA to 500 mA. These two timings include $2.56\mu s$ (4 clock cycles) each for the loading of the coefficients from the ROM to the FPGA during the change between PWM and PFM modes. To verify the dynamic response time of the DC-DC converter, a tracking test was also carried out whereby the reference voltage was changed and the output voltage

7.5 Simulation and Measurement Results

had to follow the reference. The tracking speed of the digital converter is approximately $62.5 \mu\text{s}/\text{V}$. Figure 7.7 shows the line transient response of the output when the input

Figure 7.6: Load Transient Response Waveform

battery voltage (top) changes from 4.2 V to 3.5 V. The output voltage (bottom) varies in a range of 37.5 mV.

Figure 7.7: Line Transient Response Waveform

The efficiency of the dual-mode distributed-arithmetic-based DC-DC converter is 88% at a load current of 500 mA in PWM mode and 81% at a load current of 20mA in PFM mode.

7.5 Simulation and Measurement Results

Table 7.2: Comparison of proposed current-mode converter against voltage mode and hysteretic voltage-mode

	Voltage-mode	Hysteretic voltage-mode	Proposed current-mode
Tracking speed	$100\mu\text{s}/\text{V}$	$\sim 1\text{ms}/\text{V}$	$62.5\mu\text{s}/\text{V}$

Table 7.2 shows a comparison of the tracking speed of the proposed current-mode DC-DC converter against prior arts based on voltage-mode (Dancy and Chandrakasan, 1997) and hysteretic voltage-mode control (Wei and Horowitz, 1999) at switching frequency of less than 1 MHz. From Table 7.2, note that the proposed current-mode converter achieves better load tracking speed than the voltage-mode and hysteretic-mode converters. The detailed hardware resources utilization report for the FPGA is shown in Table 7.3.

This chapter discusses the distributed-arithmetic-based digital DC-DC converter and presents its theoretical analysis. Design and implementation of the digital controller have been realized on the FPGA, and the measurement results have shown savings on resources and low power consumption.

7.5 Simulation and Measurement Results

Table 7.3: Hardware resources utilization report of FPGA

Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	59	21,504	1%
Number used as Flip Flops	16		
Number used as Latches	43		
Number of 4 input LUTs	77	21,504	1%
Number of occupied Slices	84	10,752	1%
Number of Slices containing only related logic	84	84	100%
Number of Slices containing unrelated logic	0	84	0%
Total Number of 4 input LUTs	84	21,504	1%
Number used as logic	77		
Number used as a route-thru	7		
Number of bonded IOBs	10	240	4%
IOB Flip Flops	1		
IOB Latches	5		
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.39		

Part V

Conclusions

Chapter 8

Conclusions

8.1 Conclusions

This thesis has described the proposal, analysis, and realization of the novel design of an integrated digital DC-DC converter with its building blocks. The intended application of the digital DC-DC converter is power-critical and hardware-critical devices like portable devices, such as cell phones and laptops, and wireless devices.

In view of the intended application, the general objectives of the digital DC-DC converter are high efficiency, fast transient response and low overshoot with low hardware complexity. In the case of portable devices, the DC-DC converter also needs to feature low power consumption and high efficiency over a wide load range and different operating modes. The specific building blocks of the digital DC-DC converter are the hybrid-segmented 12-bit DPWM, the windowed SAR ADC, and a predictive and feed-forward digital controller. An alternative sigma-delta ADC is also proposed to reduce the ripple and phase noise generated.

In Chapter 2, classical regulators and analog- and digitally-controlled DC-DC converters have been reviewed. The digital DC-DC converters exhibit a lot of distinct advantages such as its relative portability and short time-to-market. The digital DC-DC converters can achieve optimum transient performance through advanced control algorithms.

In Chapter 2, a comprehensive literature review of the building blocks of the digital DC-DC converter has also been provided. It also includes the small- and large-signal

modeling of the power stage of the converter, the redesign and direct digital design of the controller, and the effect of quantization on the output resolution of the DC-DC converter.

In Chapter 3, the design and implementation of a supply and process-insensitive 12-bit Digital Pulse Width Modulator (DPWM) for digital DC-DC converters has been elaborated. The DPWM is realized by a ring oscillator-based segmented tapped delay line and a counter-comparator. The number of delay cells required is reduced by employing a proposed delay cell reuse technique. The ring oscillator of the tapped delay line is made insensitive to supply and process variation by biasing the differential delay cells with a supply-insensitive replica bias circuit. Simulation results have shown that the variation of the switching frequency of the DPWM at 1.02 MHz is 0.4% for supply voltage variation between 1.5 V and 2.5 V and 0.95% over the temperature range from -40°C to 90°C . Monte-Carlo simulation has also been performed to account for the effect of mismatch between the transistors of the ring oscillator. The worst case delay of the delay cells is 0.87% for $\pm 5\%$ ($3\text{-}\sigma$) mismatch. The design was fabricated in CMOS $0.18\text{ }\mu\text{m}$ process and the fabricated DPWM achieved a supply sensitivity of 0.82% and a current consumption of $14\text{ }\mu\text{A}$.

In Chapter 4, a windowed successive approximation (SAR) analog-to-digital converter (ADC) using an ultra-fast, offset-cancelled auto-zero comparator has been proposed for digital DC-DC converters. It is designed in a standard CMOS $0.18\text{ }\mu\text{m}$ process. The ADC has a dynamic reference voltage range to reduce power consumption. The auto-zero scheme of the comparator is realized internally with a preamplifier stage and a latch stage. Post-layout simulation shows that the response time of the comparator from low-to-high and high-to-low is 3.78 ns and 2.47 ns, respectively. The resolution of the proposed windowed SAR ADC is 7.5 mV. The ADC is fabricated as part of a digital DC-DC converter integrated circuit and measurement results show that an average power consumption of $0.8\text{ }\mu\text{W}$ is achieved. The transient time of the DC-DC converter is within 150 ns for a load current change of 495 mA.

In Chapter 5, a multimode digital DC-DC converter combining the predictive and feedforward control with the conventional PID controller has been introduced to achieve fast transient response and low overshoot. An additional predictive or jerk component is added to the conventional PID controller to speed up the transient response and

reduce the settling time by approximately 50%. This predictive term is based on the second derivative of the error signal and introduces zero to the loop response, which leads to increased bandwidth and improved phase margin. In addition, a feedforward control is also employed to further improve the transient by evaluating the change in the inductor current during the on and off time of the power transistors. Theoretical analysis and simulations were carried out to analyze the proposed design and algorithm. The proposed design is verified on silicon with a prototype of a digital DC-DC converter fabricated in CMOS 0.18 μm process. The digital DC-DC converter achieved a settling time of 4 μs and an overshoot of 15 mV for a step-load transient of 450 mA, which are improved significantly as compared to the prior arts.

Two alternative digital DC-DC converters have also been proposed in Chapter 6 and Chapter 7. In Chapter 6, the digital DC-DC converter achieves adaptive optimization based on genetic algorithm. Chapter 7 presents a dual-mode hardware-efficient digital DC-DC controller. Both the designs were verified on field-programmable gate array (FPGA).

As an overall conclusion, the work described in this thesis pertains to the design and realisation of superior performance digital DC-DC converters. The digital DC-DC converters are targeted for the power management of wireless and portable applications. All the design were verified experimentally and performance improvement have been presented in terms of transient behaviour, power efficiency, and hardware saving.

8.2 Recommendations for Future Research

The following directions are recommended for future research pertaining to the design and implementation of digital DC-DC converters.

8.2.1 Design of Nonlinear Controller for Digital DC-DC Converters

The design of the controller in this thesis mainly focuses on the linear control. However, it is known that nonlinear control is capable of improving the dynamic response of a converter since it is able to quickly react to transient conditions. Furthermore, digital control is well suited for the development of hybrid linear/nonlinear controllers, which

possess the fast reaction of a nonlinear controller during transient conditions with the precision of a linear controller during steady state.

8.2.2 Investigation and Reduction of EMI and Noise Issues for Digital DC-DC Converters

DC-DC converters produce considerable switching noise and electromagnetic interference (EMI). In conventional DC-DC converters, shielding and filtering are employed to reduce EMI. However, these approaches increase the cost and size of the DC-DC converters. With digital controller, it would be desirable to introduce advanced algorithm and complex modulation schemes to reduce EMI and noise.

8.2.3 Applications of Digital DC-DC Converters in Green-Energy Era

In the future green-energy era, digital DC-DC converters will play a significant role in achieving intelligent power control by realizing advance control algorithms, for example, a maximum power point algorithm, dynamic voltage scaling control, adaptive biasing not only for a low-power-consumption system but also for extracting power from renewable energy sources such as solar and wind energy.

Author's Publications

Journal Papers

1. Foong, H. C., Tan, M. T., and Zheng, Y. (2011). A high-resolution and robust 12-bit DPWM for digital DC-DC converters. *IEICE Transactions on Electronics*, vol. e94-c, no. 9, pp. 1455–1463.
2. Foong, H. C., Tan, M. T., and Zheng, Y. (2011). A 0.8- μ W window SAR ADC with offset cancellation for digital DC-DC converters. *Analog Integrated Circuits and Signal Processing*, vol. 70, no. 1, pp. 133–139.
3. Foong, H. C., Zheng, Y., Tan, Y. K., and Tan, M. T. (2012). Fast-transient integrated digital DC-DC converter with predictive and feedforward control. *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 7, pp. 1567–1576.
4. Foong, H. C., Tan, M. T., and Zheng, Y. (2012). High linearity 8-bit VCO-based cascaded $\Sigma\Delta$ ADC for digital DC-DC converters. *Journal of Circuits, Systems and Computers*, doi:10.1142/S0218126612500624.

Conference Papers

1. Foong, H. C., Tan, M. T., and Zheng, Y. Adaptive optimal controller based on genetic algorithm for digital DC-DC converters. In *Proc. IEEE Int. Symp. on Industrial Electronics, ISIE 2011*, pp. 119–124.
2. Foong, H. C., Tan, M. T., and Zheng, Y. Predictive proportional integral controller for digital DC-DC converters. In *Proc. IEEE Conf. on Industrial Electronics and Applications, IEICA 2011*, pp. 2380–2383.

3. Foong, H. C., Tan, M. T., and Zheng, Y. An integrated digital DC-DC converter with adaptive optimal control. In *Proc. IEEE Int. Conf. on Power Electronics, ICPE & ECCE-ASIA 2011*, pp. 2805–2812.
4. Foong, H. C., Tan, M. T., and Zheng, Y. A dual-mode digital DC-DC converter based on distributed arithmetic. In *Proc. IEEE Int. Symp. on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM 2010*, pp 1146–1149.
5. Foong, H. C., Tan, M. T., and Zheng, Y. A supply and process-insensitive 12-bit DPWM for digital DC-DC converters. In *Proc. IEEE Int. Midwest Symposium on Circuits and Systems, MWSCAS 2009*, pp. 929–932.
6. Foong, H. C. and Tan, M. T. An analysis of THD in class D amplifiers. In *Proc. IEEE Asia Pacific Conf. on Circuits and Systems, APCCAS 2006*, pp. 724–727.

Book Chapters

1. Tan, Y. K., Zheng, Y., and Foong, H. C. Ultra low power management circuit for optimal energy harvesting in wireless body area network, In Kris Iniewski, editor, *CMOS circuits for emerging technologies*, Wiley, 2011.

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