Flip chip joint-in-via architecture on flexible substrates with Au-Sn interdiffusion bonding

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FLIP CHIP JOINT-IN-VIA ARCHITECTURE ON FLEXIBLE
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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

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FLEXIBLE SUBSTRATES WITH Au-Sn
INTERDIFFUSION BONDING**

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2006

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Flip Chip Joint-in-Via Architecture On Flexible Substrates with Au-Sn Interdiffusion Bonding

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ABSTRACT

Pad pitch on substrate has been identified as a difficult flip-chip, which makes it a challenge to keep up with the microelectronic packaging revolution. This study proposes a joint-in-via architecture to meet this challenge but this research is hindered by the flux residues of conventional soldering. This study conceptualises the joint-in-via architecture and develops a fluxless bonding technique with its mechanism and reliability uncovered. The success of this research will provide the mainstream consumer electronics market the benefits of flip-chip packaging.

The joint-in-via architecture has been conceptualised on a flex substrate at a 70 μ m pitch with only 20 μ m pad spacing using laser-via technology. This pitch capability is smaller than any existing copper metallizations and has satisfied the requirement of flip-chip till the year 2018. On bonding, the conventional soldering is found to be not compatible due to its wetting properties. Further bonding attempts using solid-state thermocompression bonding failed to form a reliable bond because the multiple micro-weld joints breaks off during cooling. The solid liquid interdiffusion bonding by compressive force (SLICF) has been developed as a new instantaneous fluxless bonding for Au with eutectic PbSn and lead free solder SnAgCu in ambient environment. My studies reveal that the SLICF bonding utilises a mechanical force to break the Sn oxide layer and allow the submerged body to interact with fresh molten solders to form bonds through solid liquid interdiffusion. This fluxless bonding is found to be compatible with the joint-in-via architecture with robust assembly.

In the study of kinetics of Au with molten PbSn solder, the Au consumption rate is found to be a better yardstick to describe the kinetics of solid liquid interdiffusion than the intermetallic layer growth due to the interaction complexity at the bonding interface. The

Au consumption in solid liquid interdiffusion can be described as a two-stage kinetics; the instantaneous dissolution of Au into molten solder with the formation of a diffusion barrier followed by a diffusion kinetics through the diffusion barrier with time i.e. $x = d_o + k_o \exp\left(-\frac{Q}{RT}\right) t^{0.5}$. The growth and shift of this diffusion barrier interfaces are governed by a $t^{0.5}$ relationship as per suggested by the Kidson's interdiffusion model. Through the conservation of mass, significant amount of Au is found to dissolve in the solder even with the formation of the diffusion barrier. For Au with Sn based solder, the rate of the solid liquid interdiffusion is found to be at least two orders of magnitude faster than solid-solid interaction, suggesting the importance of instantaneous SLICF bonding for the joint integrity. The increase of Sn in SnAgCu solder forms a thin diffusion barrier and increases the diffusion kinetics through the diffusion barrier. The initial kinetics of SnAgCu is lower than PbSn but it overtakes the PbSn interaction through the diffusional kinetics with time.

Field applications using existing packaging infrastructure has demonstrated the robustness of applying the SLICF bonding with the joint-in-via architecture for fine pitch flip-chip applications, inclusive of heat sensitive devices. Although the Au with Sn based solder joints are weak due to extensive intermetallics, the joints passed the JEDEC reliability testing in T/C B, T/S D, Autoclave C and MST L2 through proper material selections. In fatigue testing, Au with PbSn performed marginally better than Au with SnAgCu due to its better joint geometry and lower kinetics of forming intermetallic with time.

Future works in this area include research into SLICF bonding for other interconnect systems and verifying the two-stage kinetics for solid-liquid interdiffusion model with established binary phase diagram. This research will help to drive a wider adoption of flip-chip technologies inclusive of the optoelectronic and MEMS packaging.

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LIST OF SYMBOLS AND ABBREVIATIONS

SLICF	Solid liquid interdiffusion bonding by compressive force
RDL	Redistribution Layer
MCM	Multi-chip Modules
Pb	Lead
ITRS	International Technology Roadmap for Semiconductor
PRC	Package Research Centre
NSF	National Science Foundation
Cu	Copper
Ni	Nickel
Au	Gold
Ag	Silver
α	Primary phase
β	Intermetallic phase
γ	Primary phase
W_{β}	Growth of the intermetallic layer
CFCs	Chlorofluorocarbons
CO ₂	Carbon Dioxide
PADS	Plasma Assisted Dry Soldering
Ar	Argon
H ₂	Hydrogen
CF ₄	Tetra-carbon
LAFS	Laser Ablative Flux-less Soldering
In	Indium
UBM	Underbump Metallization
SMT	Surface Mount Technology

IBM	International Business Machines Corporation
PCB	Printed Circuit Board
LTCC	Low Temperature Co-fired Ceramic
CSP	Chip Scale Package
SMD	Soldermask Define
NSMD	Non-soldermask Define
Nd: YAG	Neodymium:Yttrium Aluminum Garnet
ICA	Isotropic Conductive Adhesive
ACA	Anisotropic Conductive Adhesive
X_K	Distance due to Kirkendall shift
J	Flux
D	Diffusion Coefficient
C_{LM}	Maximum solubility of M in L
C_{ML}	Maximum solubility of L in M
J_{LM}	Diffusion flux advancing from L into M
J_{ML}	Diffusion flux advancing from M into L
D_{LM}	Interdiffusion coefficient at interface of phase L into phase M
D_{ML}	Interdiffusion coefficient at interface of phase M into phase L
W_β	Growth of the intermetallic layer
α	primary phase
β	intermetallic phase
γ	primary phase
dC/dx	Concentration Gradient
d^2C/dx^2	Rate of Change in Concentration Gradient
C_s	Concentration at the surface
C_x	Concentration at depth (x)

Erf	Error Function
C_o	Initial Concentration of Diffusing Species
D_o	Diffusion constant
Q	Activation Energy
R	Gas Constant
F	Force in Kgf
T	Absolute Temperature in Kelvin
b	Rate constant for power law
n	time exponent
d_o	Initial Au consumption thickness
k	Rate constant at temperature T
k_o	Rate coefficient
t	Time
SEM	Scanning Electron Microscope
EDX	Energy Dispersive X-ray Spectroscopy
δ	AuSn
ϵ	AuSn ₂
η	AuSn ₄
α -Au	6.8 at % Sn in Au at 498°C
β	Au ₁₀ Sn
ζ	Au Sn eutectoid composition
ζ'	Au ₅ Sn
Ni-P	Nickle phosphorous
WEEE	European Union's Waste in Electrical and Electronic Equipment
CTE	Coefficient of Thermal Expansion

ε	Total strain
σ_{xx}	Axial plastic strain
DNP	Distance of the Neutral Point
$\Delta\alpha$	Expansivity Mismatch between Chip and Substrate
ΔT	Temperature Range for Cycling
h	Joint Height
C4	Controlled Collapse Chip Connection
σ_{xx}	Axial plastic strain
$\Delta\varepsilon$	strain range
ΔW	strain energy density
N_f	No of Cycles to Failure
ε_p	Plastic Strain Range
FEM	Finite Element Method
2D	Two Dimensional
T_g	Transition Temperature
BT	Bismaleimide Triazine
PCB	Printed Circuit Board
TMA	Thermomechanical Analysis
T_g	Transition Glass Temperature
FC-CSP	Flip Chip Chip Scale Package
LCP	Liquid Crystalline Polymer
JIV	Joint-in-via
SAC	SnAgCu
IMC	Intermetallic compound
JEDEC	Solid State Technology Association

(Joint Electron Device Engineering Council)

MEM	Micro-Electro-Mechanical System
FC	Flip Chip
TGA	Thermogravimetric Analysis
DMA	Dynamic Mechanical Analysis
FR4	Flame retardant 4
T/C	Thermal cycling
T/S	Thermal shock
MST	Moisture sensitivity test
Sn	Tin
ITRS	International Technology Roadmap for Semiconductors
TAB	Tape automated bonding
CFC	Chlorofluorocarbons
EPA	Federal Environmental Protection Agency
OSHA	U.S. Department of Labor Occupational Safety and Health Organization
RCRA	Resource Conservation and Recovery Act
x'	Intermetallic layer
P	Circumference of the stud tip
F_R	Insertion force
γ_g	Surface tension of the eutectic solder with air
α_l	Tangential angle of the solder meniscus with the vertical
W	Weight of the soldering body
s	no of stud
s'	the no of tallest studs in equilibrium with a insertion force F_T
F_T	Threshold force to overcome the surface tension
γ	Sum of the surface tension of solder with air and the oxide layer

γ_o	Surface tension of the oxide layer
α_m	Tangential angle of the oxidized solder surface before the oxide layer break
F_b	Insertion force greater than the threshold force
γ_{ls}	Surface tension of the solder with an Au surface
θ	Contact angle between the Au surface and the solder
ρ	Density of solder
g	Mass of acceleration
A	Cross-section of the submerged body
x_o	Equilibrium submersion depth into the solder
F_w	Resultant force at any depth in solder
T_i	Bonding temperature
T_s	Solidified temperature of solder
T_∞	Ambient temperature
m	Mass
c	Heat capacity
h	Convection heat transfer coefficient
A_s	Surface area for convection cooling of the submerged body
t_s	Time taken for solder solidification
W_i	Width of the intermetallic layer
b	Rate constant at temperature T
n	Time exponent
x	Au thickness consume
d_o	Instantaneous Au consumption upon contact with molten solder
k	Rate constant of Au dissolving into molten solder through the diffusion barrier

k_o	Rate constant of Au dissolving into molten solder through the diffusion barrier at absolute temperature
E_i	Activation energy
C_i	Rate constant
RH	Relative humidity
UF	Conventional underfill
NF	Non flow underfill
SDRAM	Synchronous dynamic random access memory
FC-CSP	Flip-chip Chip Scale Package
η'	characteristic life at 63.2 percent of the failures
β'	shape parameter
ξ_{ij}	Shift of the phase i, j interfaces from Matano interface
C_{ij}	Maximum solubility of j in i
J_{ij}	Diffusion flux advancing from i into j
D_{ij}	Interdiffusion coefficient at interface of phase i into phase j
M1	Metal 1
M2	Metal 2
CALPHAD	Computer Coupling of Phase Diagrams and Thermochemistry
c_0	Average height of Au stud bump
c_1	Average Au of stud height left after bonding
c_i	Average thickness of individual IMC thickness
c_{1a}	Average Au of stud height after thermal ageing condition
c_{ia}	Average thickness of individual IMC thickness after thermal ageing condition

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The interconnection technologies in the microelectronics industry have long been challenged to provide faster, smaller, and denser electronic components. To address these challenges, electronic packages have evolved from peripheral lead approach to current area array technology. Flip-chip in a chip-scale package (CSP) is able to address these challenges by providing area bonding, miniaturization, and standardization of footprint with high thermal and electrical performance. This is achieved through its direct flip-chip interconnection bump structures to the substrate carrier.

Flip-chip technologies require the substrate pads to have a corresponding die pad pitch for bonding. Current bumping technologies are sufficient to meet the die pad pitch without the use of a redistribution layer (RDL). A RDL is a wiring circuitry cum dielectric layer deposited on the surface of the chip to redistribute the die pads to a larger pad pitch for accommodating the substrate [1].

The 2003 International Technology Roadmap for Semiconductors: Packaging and Assembly [2] had identified substrate as a difficult challenge for flip-chip packaging because the substrate pitch is not able to meet the die pad pitch. This is due to the inability of the substrate technologies to keep up with the advancement of the flip-chip applications. Consequently, a serious geometry mismatch exists between the die pads and the substrate receiving pads. For manufacturability, a costly RDL is currently used to fan out the die pads to accommodate the substrate design rule. In particular, the organic substrate design rule must be matched as it offers a lower packaging cost as compared to

ceramic or silicon substrates. The organic substrate is clearly the choice for flip-chip packaging. Even with the application of fine-pitch polymer flip-chip technologies such as conductive particle and conductive adhesive bonding, RDL is still required to fan out the die pads in order to meet the organic substrate design rule. The challenges of flip-chip soldering are summarized in Figure 1.1. Thus, advancement in organic substrate pad pitch is important for the wider adoption of flip-chip technologies by providing a cost-effective solution.

Figure 1.1: Challenges in Flip-chip Technologies

1.2 OBJECTIVES AND SCOPE OF WORK

The objectives of the project are to resolve the compatibility of the die pad pitch with the organic substrate through a new substrate's architecture. The unique interconnect architecture aims to offer a fluxless flip chip bonding with a reliable interconnect system at fine pitch

This project proposes a joint-in-via architecture with the use of Au and solder as the interconnect system in this study. The joint-in-via architecture consolidates the landing pads, through via and flip-chip joints into one common element as illustrated in Figure 1.2. The advantages of the proposed architecture and the selection of the Au-solder interconnect system will be discussed in Section 3 of the report. This section identifies the challenges faced in this proposed architecture and suggests the various research areas to enable the fluxless bonding on the joint-in-via architecture.

Figure 1.2: Via architecture consolidates both the landing pads and through-via with the use of current micro-via technologies

First, the joint-in-via architecture needs to be conceptualized with a fine pad pitch capability. The architecture aims to have a better pad pitch capability as compared to current advanced substrate technologies. For example, the joint-in-via architecture needs

to achieve a via opening of 85 μ m with a pad pitch of 150 μ m or less in order to have an equivalent or better pad pitch capabilities than existing pad architecture. With such a fine pitch capability, the proposed joint-in-via architecture will be able to compete with existing substrate technologies to match the die pad pitch and eliminate the need of RDL layer.

The proposed joint-in-via architecture capitalizes on the use of current micro-via technologies. Various micro-via technologies on organic substrate materials must be assessed to generate a large receiving micro-via structure with narrow inter-via spacing. This includes assessing both the micro-via size and its inter-via spacing capability on different organic materials. Capability assessments include the use of chemical, mechanical and laser micro-via formation techniques on organic substrate materials such as FR4, BT, LCP and polyimide etc. The joint-in-via architecture will be fabricated and its pad pitch capability compared with existing subtractive and semi-additive metallization techniques on the organic substrates.

The success of the joint-in-via architecture needs to be coupled with a fine pitch solder bumping technique. Depositing of solder paste into the micro-via by stencil printing at fine pitch needs to be realised for joint assessment. This bumping process needs to be automated and solder bumped with no solder bridging at a fine pitch. Good bump coplanarity needs to be achieved for subsequent flip-chip bonding. With all these developments in place, the joint-in-via architecture with the fluxless flip-chip bonding can then be pursued.

As discussed above, flip-chip soldering using gold studs with solders are selected as the interconnect system for this study. Conventional soldering with the joint-in-via

architecture was characterized as the first reference for flip-chip bonding. This can be carried out by inserting the gold studs into corresponding micro-vias containing solder paste. The bonding process can be accomplished with a conventional reflow process. Conventional soldering generates flux residues that are known to degrade the mechanical properties of underfill and reduce the package reliability of components. The flux residues further restrict the use of soldering for optoelectronic device assembly, micro-electro-mechanical system, fiber optic components, and microwave as the flux residues contaminate the devices. Thus, a fluxless bonding technique with solder is desired for wider adoption of flip-chip packaging.

The review of existing fluxless soldering reveals the difficulties in the implementation of the controlled atmosphere for oxide removal in production. The poor assembly yields and the controlled atmosphere restrict the adoption of the fluxless bonding for flip-chip soldering. As such, this project attempts to develop a fluxless bonding on the joint-in-via architecture in open ambient environment. Thermocompression and solid-liquid interdiffusion are chosen as the potential candidates for the fluxless bonding development. The thermocompression bonding plastically deforms metals in their solid phases under pressure and temperature, thereby allowing interdiffusion between metals to form a bond. The soft nature of the solder will be able to dissipate the residual elastic stresses and provide a good interface bond. Solid-liquid interdiffusion bonding was chosen for assessment because of its success in fluxless die bonding in ambient environment with the additional of gold surface finish to prevent oxidation. In this research, the uses of solid-liquid interdiffusion of gold stud with different molten solders are explored to achieve a fluxless bonding solution in ambient environment. This bonding technique is ideal with the joint-in-via architecture as the micro-via architecture allows a solid-liquid bonding without solder bridging.

The mechanisms for the different bonding are studied to ensure a robust assembly and a reliable joint for flip-chip applications. A hypothesis will be formulated and field tests conducted to understand the fluxless soldering mechanism. This study aims to uncover the mechanism of the fluxless bonding with the joint-in-via architecture. It will investigate how the bonding removes the oxide layer to enable a fluxless joint formation. Analysis tool such as Scanning Electron Microscope (SEM) and Electron Dispersion X-ray spectrometry (EDX) will be used as tools to verify the proposed hypothesis. Macroscopic analysis of the joint will be performed to characterise its geometrical structure and to provide further evidences on this fluxless bonding technique. With the growing environmental concern, lead-free solder such as SnAgCu will also be included as part of the research for future packaging. The fluxless bonding of Au with SnAgCu will be assessed and characterised to ensure robust assembly of the fluxless bonding with the joint-in-via architecture.

With the use of Au and solder as the flip-chip interconnect system, the microstructure and its kinetics at the solid-liquid interface need to be further understood. This is especially important with the introduction of a new fluxless bonding technique. From the literature review, it was found that Au with eutectic solder is known to form extensive embrittlement phases, which affects its joint integrity. Thus, the kinetics of Au interacting with PbSn and SnAgCu solders during bonding need to be researched upon to enhance their joint reliability. The interaction of Au with molten PbSn at different bonding temperatures will be studied with the interface morphologies identified. The kinetics during bonding will be quantified through the measurement of the activation energy and the diffusivity constant. Together with the morphology analysis, this will provide critical information about the joint integrity for subsequent assembly processes and reliability

tests. As reliability tests and assembly processes promote intermetallic growth under solid diffusion, the solid diffusion kinetics will needed to be measured and compared with the kinetics during bonding. Since the extent of Sn may affect the kinetics in SnAgCu, similar kinetics studies will be extended to Au with SnAgCu. This will help to provide insights into the joint-in-via architecture integrity for Au with both PbSn and SnAgCu solders.

Once the joint-in-via architecture is enabled, assembly and reliability tests will be carried out to assess the joint. The assembly tests include assembly checkout for bonding with the joint-in-via architecture at fine pitch. This is done through the use of existing die bonder infrastructure for flip-chip bonding. These tests help to verify the assembly robustness of the proposed joint-in-via architecture. For reliability assessment, characterization of packaging materials will be performed to select the best flex and underfill candidates for reliability assessment. Material characterization such as thermal analysis and shear tests will be performed to obtain the underfills material properties and their interfacial performance respectively. The joint-in-via architecture will be assessed under standard reliability conditions governed by the JEDEC (Solid State Technology Association). These include thermal cycling (T/C), thermal shock (T/S), moisture sensitivity test (MST) and autoclave. The Au-PbSn and Au-SnAgCu systems will be subjected to thermo-mechanical stresses with failure analyses conducted to reveal their failure mechanisms.

In summary, a fluxless bonding in the joint-in-via architecture is conceptualized to address flux residues and pad pitch challenges for flip-chip advancement as shown in Figure 1.3. The bonding mechanism and the kinetics of Au with Sn based solders during bonding and reliability will be studied to ascertain the interaction and reliability. Both assembly and reliability tests will be conducted to assess the claims and joint integrity. Special attention will be made on the joint-in-via architecture of Au with PbSn and Au

with SAC for thermo-mechanical stresses. Figure 1.4 summaries the key milestones of the research project.

Figure 1.3: Proposed joint in via approach to addresses flux residues and pad pitch constraints for advancement in flip-chip technology

1.3 ORGANISATION OF REPORT

This report begins with a literature review of the challenges faced in flip-chip and substrate technologies. This overview assists in revising a strategy in proposing fine pad pitch architecture. A literature review on the kinetics and interactions of Au with Sn based solders are presented to understand the growth of the intermetallic and their effects in

joint integrity. Chapter 3 discusses the advantages and summaries the works involved in conceptualizing the joint-in-via architecture. The fluxless flip-chip bonding mechanism known as solid liquid interdiffusion bonding by compressive force (SLICF) bonding is uncovered in Chapter 4. Chapter 5 discusses the kinetics and the interactions between Au and Sn based solders while Chapter 6 summaries its reliability of this fluxless bonding technology on the joint-in-via architecture. Lastly, Chapter 7 concludes the development of the studies and recommends future research areas.

Figure 1.4: A Simplified Project Flow-chart

CHAPTER 2

LITERATURE REVIEW

The geometry mismatch between silicon die and substrate has been considered as the fundamental challenge for flip-chip technologies in the fine pitch arena. This chapter begins with a literature review of current flip-chip and substrate technologies inclusive of their bonding mechanisms. The kinetics of Au with eutectic PbSn solder and lead free SnAgCu are also reviewed to provide an understanding of their interactions in bonding and their impact to joint integrity. Lastly, thermo-mechanical stresses to packaging will be reviewed to revise a reliable joint.

2.1 FLIP-CHIP OVERVIEW

The wirebond technologies have been the most commonly used interconnect system in microelectronic packaging. This is due to their ability to offer a fluxless and ultra fine pitch solution for microelectronic interconnection. The precision capillary tool with the vision aided ball placement enables the wirebond technologies to achieve a die pad pitch of 35 μ m [3]. Its wire bond loop fan-out the fine die pad pitch to accommodate a larger pad pitch on the substrate. This long loop increases the form factor of the package and affects its electrical performance. Thus it motivates the use of flip-chip technologies for miniaturization and achieving a good electrical performance.

Flip-chip technologies refer to the use of different interconnect systems which connects an integrated circuit chip to a substrate with its active surface of the chip facing the substrate. Figure 2.1 shows a typical flip-chip interconnect system. The solder bump sits on an underbump metallization (UBM) layer and connects to the substrate pad by a

conductive bonding material [4]. The substrate pads receive the bumps and redistribute the electrical signals to the designated locations for external communications. The following sections review the bumping technologies, the RDL processes and the different flip-chip interconnect systems.

Figure 2.1: Typical Flip-chip Interconnect system

2.1.1 Bumping and RDL

Bumping is key to flip-chip technologies. It determines the assembly techniques, infrastructures and the type of interconnect systems for flip-chip packaging. Metal or solder alloy is normally deposited on the die as bumps for interconnection. The 5 mainstream bumping technologies (stencil bumping, evaporation, electroless, electroplating and mechanical stud bump) will be discussed in this section with the emphasis on their pad pitch capabilities.

The stencil bumping uses a precision stencil or photo-resist mask to deposit solder paste on the UBMs through squeegee printing. Fine stencil openings are aligned with UBM for solder paste deposition [5-6]. A simplified processing flow in Figure 2.2 illustrates that the making of the stencil limits its bumping pitch capability. The stencil bumping technology achieves a pad pitch of 200 μm , with an average standoff of 70 μm on a pad diameter of 75 μm [5]. This technology has difficulties in achieving fine pitch bumping of below 200 μm at reasonable yield due to the following limitations [7-9]

- stencil materials and processing technologies challenges
- slumping of paste which resulted in solder bridging
- poor position registration of printer
- availability and print-ability of fine solder paste

However, the stencil bumping offers the lowest bumping cost as it capitalises on a well-established printing technology in surface mount technology (SMT).

Figure 2.2: Stencil fabrication technique restricts a minimum pad pitch of 200µm

Evaporation bumping is the most mature wafer bumping method used by International Business Machines Corporation (IBM) since the 1970s [6, 10-11]. The evaporation bumping takes place in a vacuum chamber for an efficient, uncontaminated and uniform deposition. Evaporation of the solder is performed either by resistive heating of tin and lead or by bombarding the tin and lead with an electron beam. A molybdenum mask is aligned on the wafer to aid the solder deposition on the bond pad as shown in Figure 2.3. The best capability offers in mass production by IBM [10] is a 200µm pitch with an 80µm standoff on a pad diameter of 75µm.

Figure 2.3: The molybdenum mask in evaporation bumping determines the pad pitch

Electroplated bumping is the most widely adopted bumping approach due to its fine pitch and high pin count capability. The bumps are formed through a pattern defined photo-resist mask by electroplating. The bumps are then reflowed after electroplating to homogenize the solder microstructure as illustrated in Figure 2.4. The composition of the electroplated solder bump is determined by current density, electrolyte composition and the additives added in the plating solution [12-14]. The electroplating process is capable of achieving a fine pitch pattern with the use of wafer fab equipment. A $150\mu\text{m}$ fine pitch with a pad size and standoff of $75\mu\text{m}$ and $80\mu\text{m}$ respectively has been reported. An ultra fine pad pitch of $75\mu\text{m}$ with a low standoff of $20\mu\text{m}$ has also been demonstrated using electroplating.

Figure 2.4: The patterned photo resist determines the pitch in electroplated bumping

Electroless plating [6] is a selective metal deposition process that uses a chemical exchange reaction between the metal complexes in the solution and the particular metal electrode. The mask-less bumping process is illustrated in Figure 2.5. The bumping starts by activating the bond pad surfaces with a zincate treatment, followed by electroless plating of Ni and Au [15]. The isotropic growth of the nickel limits the pad pitch capability. It is recommended that an inter-spacing of at least $20\mu\text{m}$ is needed to prevent shorting by overgrowing Ni [16]. It has been reported by Thorsten et al. [17] that electroless bumping offers a fine pad pitch of $50\mu\text{m}$ with an inter-pad spacing and standoff of $10\mu\text{m}$ and $5\mu\text{m}$ respectively. As such, the bump height obtained by electroless bumping is small and can only be considered as a thin film coating.

Figure 2.5: Isotropic plating determines the bump pitch in electroless bumping

Mechanical stud bump maximizes the use of existing wire bond infrastructure for bumping. The bumps are formed by mechanically depositing the Au wires by thermosonic bonding as shown in Figure 2.6. This point-to-point sequential bumping process is not economical for high pin count devices but it provides flexibility for bumping. The rapid advancement in wirebonding has improved tremendously the throughput for stud bumping. This is the only available bumping technique that does not require any UBM metallization for bumping and hence simplify the need of infrastructure investment. The mechanical stud bump is able to meet a fine pitch capability as per wire bonding technologies [18-23]. A pad pitch of $80\mu\text{m}$ with a base and standoff of $60\mu\text{m}$ and $40\mu\text{m}$ respectively has been reported. The coplanarity of the stud bumps has been highlighted as a concern but a mechanical coiling process can be applied to improve the bump coplanarity.

Figure 2.6: Positional accuracy of capillary determines the pitch in stud bumping

Currently, most of the existing bumping technologies offer a pitch capability of $80\mu\text{m}$. This satisfies most of the current die pitch requirement but its substrate pad pitch capability is not able to meet this requirement. This is attributed to the slow advancement in the substrate technologies in keeping up with the advancement of die pad pitch. Thus, it has resulted in a serious geometry mismatch between the die pads and the substrate pads for flip-chip packaging. This problem has been identified by the industry, and consolidated by the ITRS 2003 Roadmap: Packaging and Assembly, as a difficult challenge for flip-chip packaging [2].

Due to this constraint, an existing redistribution layer (RDL) is used to bridge this technological gap between the die and the substrate. The RDL is a wiring circuitry cum dielectric layer that are deposited on the surface of the chip (Figure 2.7) using obsolete wafer fab equipment [24]. This layer fans out the die pads to a larger pad pitch for accommodating the current design rule of the substrate. It acts as an intermediate and temporary solution for packaging but this technology is not a drop in solution for all flip-chip technologies. For example, the RDL is a significant cost adder to flip-chip packaging due to the wafer yield [25-26]. The use of chemical solutions and residues in RDL also contaminates and damages the optical and MEMS devices in its processes. Hence, RDL hinders the growth of flip-chip packaging. Thus the advancement of the substrate technologies is important to meet the advancement of the die pad pitch for the wider adoption of flip-chip technologies.

Figure 2.7: RDL process flow

2.1.2 Flip-chip Interconnect System

Flip-chip technologies can be broadly classified into metallurgy and polymer flip-chip technologies, which can be further broken down into 5 main interconnect systems as shown in Table 2.1. They are controlled collapse, solid state, cap reflow, conductive adhesive and conductive particle bonding. The details of these different interconnect systems will be reviewed to revise a robust flip-chip architecture and bonding technique.

Table 2.1: Summary of the architectures and applications of different flip-chip technologies

		Processes					
		Material					
		Types		Metallurgy		Joints	
						Polymer Joints	
Bumping	Evaporation	Solder / Metal	Metal	Solder / Metal	Metal	Metal	Metal
	Plating	Solder		Solder			
	Printing						
						Stud directly on Al pad	
Bonding material	Chemical / Plating			Solder	Solder		
	Printing					ICA	
	ICA						Anisotropic
Flip-chip structure
		Controlled collapse	Solid state bonding	Cap Reflow	Conductive adhesive	Conductive particle	
Companies Supporting Technologies		IBM, AT&T, Oki, Sharp, HP, Intel	Panasonic, NEC, Delphi, U-Berlin	IBM, Casio, Motorola, Fujitsu	Shinko, Intel, IBM, Fujitsu, Raychem	Panasonic, Fujitsu, MCC, Sun, Lucent, Agilent	Toshiba, Casio, Fujitsu, Hitachi, SMM, Mitsubishi, Samsung, Seiko,
Applications		Consumer, U-processor, Telecom	Automotive, MAP, memory, ASIC	Consumer, Memory, PC,	Consumer, Memory, PC,	Opto devices memory, LCD, RFID	FCOG for TFT, LCD for watches, handheld TV etc

The controlled collapse structure refers to a fully wetted controlled collapse solder interconnection where the entire solder bump is placed and raised above its liquidus temperature. During the molten state, the solder is self-aligned with the whole pad, wets and reacts with the substrate metallization. Therefore, this flip-chip structure offers a high throughput, as it does not require a large bonding force and high precision bonding. At fine pitch, solder bridging between bumps is the main assembly challenge due to the poor assembly placement, the slumping of the solder paste and the flux activity. Thus, it requires a large inter-pad spacing for assembly. Intermetallic, fatigue failures and the solder joint geometry are the commonly blamed failures. Other than the studies of the intermetallic failures by the different interconnect systems to enhance the joint, its stand-off height, lower/upper contact angles of the joint, solder pad diameter and pad shape have also been studied to affect its joint performance [27].

The solid state bonding is commonly referred to as thermocompression, ultrasonic or thermosonic bonding techniques such as wirebond or TAB bonds. In flip-chip context, these interconnections are gang-bonded, forming multiple interconnections at one go. A high force with precise bonding alignment is necessary as it utilizes the top pad width for bonding. The electrical shorting at fine pitch can be prevented as the metal bumps are deformed slightly during bonding. Similar to control collapse structure, the reliability is dependent on its intermetallic and fatigue failure. The challenge of this bonding technique lies in the difficulty of obtaining co-planarity between bonding tool and the set of bumps [28].

The cap reflow structure consists of a bump bonded onto a conductive material for material compatibility. A high melting point bump is normally bumped on a die pad and bonded to a lower melting point solder on the substrate pad. The most common configuration is the use of high lead solder bumps bonded with eutectic solder caps coated over substrate pads. There is an increasing trend of using this configuration for Au stud with lead free solder [29]. The drive is associated with lead-free solder, which offers a higher strength and more resilience to fatigue failure while Au stud bumping enables a fine pitch bumping with the removal of the UBM layer. The bonding technique still undergoes high temperature reflow where the self-alignment of solder kicks in to ease the placement accuracy. Similar to control collapse structure, a large inter-pad spacing is required for cap reflow structure.

Polymer flip-chip consists of conductive adhesive bonding and conductive particle bonding. These flip-chip bonding techniques have no self-alignment mechanism like solder. Therefore, they require a high precision placement equipment to align and bond the bumps onto the receiving pads. The conductive adhesive bonding uses isotropic

conductive adhesive to adhere the bump to the substrate pad, allowing a low temperature for assembly. The gold stud bump consists of a 2-step profile, restricting the conductive adhesive from spreading to the vicinity. This enables a fine pitch bonding of about 100 μ m. This bonding technique has a penalty in assembly throughput [20-22, 30] with the additional processing time by the vision system to achieve a precise alignment. In the aspect of reliability, the conductive adhesive joint is brittle and sensitive to moisture, resulting in junction instability and fatigue failure [19, 31].

The conductive particle bonding [32-33] uses compressed conductive particles captured between the bumps and substrate pads for electrical conducting purposes. The filler particles are deformed, thereby forming a strong inter-atomic bond through atomic diffusion for conducting. This approach offers a fine pitch solution as it accommodates smaller spacing for bonding with the use of conductive particle fillers. The bonding has the advantages of eliminating underfilling and meeting environmental compatibility issue such as a lead-free and fluxless bonding. The conductive particle bonding does not self-align and therefore, it requires a higher bonding accuracy as compared to solder technology. It needs both temperature and high bonding pressure, which is applied concurrently to snap cure the resins and freeze the interconnection. This bonding technique is unfavourable due to the need of special infrastructures and slow bonding processes to snap cure the resins [32]. Similar to conductive adhesive, the joints are sensitive to moisture, which will result in joint instability. Table 2.2 summarises the degradation mechanisms of the conductive adhesive bonding and polymer bonding [34] while Table 2.3 summarizes the assembly considerations and failing mechanisms for different flip-chip interconnect systems.

Table 2.2: Failure mechanism of isotropic conductive adhesive (ICA) and anisotropic conductive adhesive (ACA) bonding

	Failure source	Failure mode
ICA, ACA	Ionic impurities, insufficient curing	Corrosion
ICA	Ionic impurities combined with high moisture absorption	Silver migration
ICA	$T_g < T_{\text{operation}}$	Crack formation in polymer bump
ACA	Unmatched CTE resulting in high shear forces in thermal cycling	Crack formation, delaminating
ACA	High moisture absorption	Swelling of adhesive layer, degradation of elastic strength
ACA	$T_g < T_{\text{operation}}$	Relaxation of bond strength
ACA	Unsuitable combination of bump and particle material	Separation of particles from contact pads

Table 2.3: Assembly consideration and joint failure between different flip-chip structures

Joint Formation	Solid Welding	Soldering		Adhesive Bonding	
FC structure	Solid-state bonding	Recap reflow	Control collapse	ACF (conductive particle bonding)	Conductive adhesive
Processing temperature	Low temp (ultrasonic) High temp (thermocompression)	High temp reflow	High temperature for reflow	Low temperature	Low temperature
Bond width	Top	Bottom	Bottom	Top	Top
Alignment	Precision	Self-alignment	Self-aligned	Precision	Precision
Force	Low/High	Low	Low	High	Low
Throughput	High	High	High	Very slow	Slow
Reliability	Intermetallic and fatigue failure	Extra interface for IMC. Reduce fatigue with high standoff and high melting material	Intermetallic and fatigue failure	Sensitive to moisture and junction instability	Sensitive to moisture and junction instability
Pitch	Small	Large	Very large	Very small	Large

The stumbling block for flip-chip assembly has been identified as the need for a high precision flip-chip bonder for assembly [6,35]. This requires high capital start-up cost as well as large investment since most of the existing die bonders are not able to meet the placement accuracy specification. Furthermore, the differences in flip-chip technologies would require unique bonding specifications [36] and thus makes investment decision even more difficult. The flip-chip bonding throughput is significantly slower with the use of fluxing station and longer vision processing time for precise alignment. Thus, all these

assembly challenges increase the flip-chip packaging cost and hinders the progress of adopting the flip-chip technologies.

2.2 SUBSTRATE TECHNOLOGY OVERVIEW

In flip-chip technologies, the substrate plays an important role as follow [37]:

- a geometrical translation of die pad design rule at $0.1\mu\text{m}$ to match the design rule of printed circuit board (PCB) at $100\mu\text{m}$
- a structure to reduce the thermal mismatch between the die and PCB
- a power distribution and ground to improve the package performance by matching its impedance and noise reduction

The substrate acts to de-couple the die from the PCB, allowing a standardization of the package footprint. For economic reasons, the industry needs a low-cost and high-density substrate for flip-chip packaging which otherwise requires the use of RDL to redistribute the die pads to a larger pitch to accommodate the substrate. The organic substrates and the low temperature co-fired ceramic substrates (LTCC) have been used as candidates for flip chip. This is a result of their unique copper metallizations and micro-via techniques that offer further miniaturization, good electrical performance and cost advantages for flip-chip packaging.

LTCC allows a thick film technology to deposit gold, silver, copper or silver-palladium as conductors on glass ceramics using a low co-firing temperature of 900°C [38]. The high dielectric constant of glass ceramics and its poor routing capability through printing limit its electrical performance as compared to organic substrates. The high cost of LTCC further hinders its wide adoption.

The organic substrates such as rigid or flex laminates are commonly used for packaging. The rigid laminates have similar multi-layer structures as per standard printed circuit board (PCB). It capitalizes on existing PCB infrastructures to produce higher wiring density substrates through the use of copper metallizations and micro-via technologies. The rigid laminate uses an epoxy-glass weave core material laminated with copper foils. This core peripheral provides rigidity for handling and relative high transition temperature for flip-chip applications. The flex refers to a copper circuitry deposited on a flexible dry film, predominantly polyimide. It offers a low dielectric constant for electrical performance enhancement [39] and a temperature of up to 300°C for assembly. The flex is thin and compliant, rendering it suitable as chip carriers, three-dimensional carriers or flip-chip assembly substrates. With its smooth surface texture, the flex offers a better surface for copper metallization than rigid substrate. Thus, a thinner application of photosensitive resistance can be applied for copper patterning; thereby achieving finer lines and spaces. Polyimide material, being mechanical and chemical processable, offers a wide variety of micro-via formation techniques, which no other peripheral base materials have offered. This allows the formation of unique packaging structures for chip scale packaging (CSP) and three-dimensional packaging [23,40]. Table 2.4 summarizes the advantages of the polyimide flex as compared to a rigid substrate.

Table 2.4: Comparison between rigid and flex

Description	Rigid laminates	Flexible laminates
Dielectric (1MHz)	4.7	<3.5
T _g (°C)	~ 190	>300
Line / space (μm/μm)	65/65	25/25
Via /Via land (μm/μm)	150/350	100/200
Ball pitch (mm)	>0.5	0.3-0.5
Core Thickness (mm)	0.1	0.05

2.2.1 Copper Metallization Technologies

Figure 2.8 illustrates the three copper metallization processes (subtractive, semi-additive, full-additive). Subtractive etching is the most commonly used approach for copper circuitry due to its simplicity, high yield, and good reliability. The copper pattern is generated by forming a negative pattern mask on the photo-mask and followed by an isotropic chemical etching. This subtractive approach achieves a fine-pitch design rule of $50\mu\text{m}/50\mu\text{m}$ and $25\mu\text{m}/25\mu\text{m}$ for rigid and flex respectively. The isotropic etching results in trapezoidal traces and pad structures for routing and flip-chip bonding respectively. This trapezoidal pad architecture structure has an impact on its flip-chip pitch capability and its joint reliability. The design rule of the subtractive etching is dependent on the copper thickness i.e. a thinner copper will achieve a fine line and space for routing. Under reliability testing, a minimum copper thickness would be required. Otherwise, a crack would develop and result in functional failure. Thus, subtractive etching restricts the pad pitch capability for flip-chip packaging.

Figure 2.8: Schematic flow of different copper pattern processes

Alternatively, advanced processes such as additive and semi-additive can be used for copper circuitry formation with better profile and the line/space design rules. These

advanced processes offer a larger selection of peripheral materials, such as base substrates and dielectric materials. Instead of removing copper, they deposit copper using a pattern-defined photo-mask. Thus, these techniques provide an avenue for implementation in high-density substrates.

The disadvantage of a fully additive process lies in the complex chemistry needed to achieve a seed layer for subsequent plating, as shown in Figure 2.8. Even if this obstacle is overcome with the use of sputtering, it still exposes the peripheral materials to the harsh chemical environment leading to potential reliability issues. As electroless plating is slow, it increases the chemical exposure of the base peripheral and increases the possibility of reliability issues. In addition, the adhesion between the peripheral and the seed layer is another reliability concern. The complex nature of the additive process also impacts yields, reliability, and thus, cost. The complexity increases significantly as the number of layers increase [41], which hinders its adoption by substrate suppliers.

Semi-additive processes utilize a uniform coating of thin conductive material for circuit formation. A material deposition process is achieved by electroplating with a patterned defined photo-resist, as shown in Figure 2.8. The electroplating process is relatively fast and reduces the chemical exposure of the base peripheral [41]. The inherent adhesion problem of the catalyst electroless copper seed layer to the peripheral still exists. Both additive and semi-additive copper formation processes offer a fine-pitch circuitization with traces having almost vertical profiles. The fine-pitch circuitization is typically achieved at the expense of copper thickness. The thin copper thickness may not be able to withstand the thermo-mechanical stresses during reliability testing. A circuitization line/space of 40 μ m/40 μ m and below can be achieved with these approaches.

In summary, all these copper metallization technologies are dependent on the copper thickness to achieve better design rules but this increases the possibility of trace crack during package reliability. Additive and semi-additive processes offer vertical profile walls with higher routing density for packaging than subtractive processes. This is a result of their copper deposition process as compared to the isotropic etching of copper. However, this does not directly translate to pad pitch as the pad architecture and types of flip-chip interconnect topple the line/space advantages offered by additive and semi-additive processes.

2.2.2 Micro-via Technologies

The redistribution of the signals from the die pads to a customized layout for packaging is performed through the substrate routings and via connections. Blind micro-via, smaller than 0.15mm, allows a layer-to-layer interconnection for substrate build-up. Although, the micro-via with the sequential-build-up technology increases the packaging density of the substrate for signal distribution, it does not resolve the pitch challenge. A summary of the micro-via technologies is reviewed in this section to capitalize on these established technologies.

The micro-via technologies can be broadly classified based on their via formation techniques, namely mechanical, chemical and laser via technology as shown in Figure 2.9. Mechanical techniques such as drilling and punching are limited in its micro-via applications due to their difficulties in blind via formation. Blind via formation is commonly generated by plasma, chemical etched and photo-via techniques. Dry etching utilizes plasma ablation on dielectric while chemical etching uses wet etchant solution on the dielectric. These micro-via techniques have less flexibility in terms of via architecture

due to their isotropic etching nature. They are also limited in their base peripheral for processing.

<i>Mechanism</i>	<i>Mechanical</i>		<i>Laser</i>			<i>Chemical</i>		
	<i>Drilling</i>	<i>Punching</i>	<i>CO₂</i>	<i>UV</i>	<i>Excimer</i>	<i>Plasma</i>	<i>Chem Etch</i>	<i>Photo-via</i>
Material options	Rigid Flex	Flex LTCC	Rigid Flex			Flex	Flex	Flex
Through hole
Blind via
Mask
Without mask
Via flexibility	Poor	Poor	Fair	Good	Good	Fair	Poor	Poor
Throughput	Slow	Fast	Fast	Slow	Fast with conformal mask	Fast	Fast	Fast
Hole size min (μm)	100	100	50	25	10	70	70	70
Equipment	Cheap	Cheap	Moderate	High	Expensive	Expensive	Moderate	Moderate
Tooling cost	Low	High	Low	Low	Low/High	Low	Low	Low
Actual Via structure

Figure 2.9: Comparison between different micro-via formation techniques [6]

A laser-fired micro-via is formed by laser ablation of the dielectric with the use of conformal mask or by a direct focused beam. This can be formed either by an Excimer, Nd: YAG or a CO₂ laser. The laser drilling technique offers flexibility in generating different via structures with different sizes and various degree of taper via wall. The high infrastructure cost and low throughput hinder its applications. However, in recent years, the reduction in cost and increase in throughput have made CO₂ laser drilling a clear lead with economical saving for micro-via fabrication [42].

Aside from the variety of methods utilized in micro-via formation, the metallization of these vias must be accomplished for inter-layer connection. This is commonly accomplished by electro-deposition a copper layer on the sidewall. The drawback is the potential cracking of the thin copper layer (10μm) over the sidewalls due to thermal

fatigue stresses [43]. This is especially apparent for copper plated at the corners of the via edges, where a substantial amount of stress can be generated depending on the types of dielectric and the shapes of the micro-via. [41]. Other significant drawbacks are the difficulties in filling the micro-via to achieve a good planarity for subsequent build-up. This is a result of registration problems on subsequent layers, which then limits the number of build-up layers.

The apparent limitation lies in the complexity of generating a micro-via with multiple processing steps to create a conductive sidewall that is sufficiently robust and adherent to the dielectric for assembly and reliability. All these substrate constraints need to be considered with the pad architecture inclusive of the choice of flip-chip interconnect system for flip-chip packaging.

2.3 FLIP-CHIP PAD PITCH CHALLENGES

As the die size shrinks and reduces, the devices encounter a “pad limited design” phenomenon where the die size cannot be further reduced because of the assembly limitation of bond pad size and pad pitch. This is especially apparent for high pin count devices with pads on all four sides of the die. For low pin count devices such as memory, the bond pad configuration is faced with the pad pitch constraints, as the die pads are commonly laid out in the center of the die. This layout is for electrical performance. Therefore, it is extremely important to reduce bond pad pitch in order to minimize the die size and achieve a maximum cost reduction and good performance. Due to the limitations of the substrate technologies, it has been difficult to obtain substrates for flip-chip assemblies that have bonding pads pitch smaller than 150 μm . This is a result of poor substrate yield due to the limitation of the copper metallizations.

The designs and material properties for substrates are critical to the reliability of flip-chip joints [44]. The types of flip-chip interconnect systems, pad designs, and the assembly techniques need to be coupled together to meet the pad pitch and the reliability requirements. For solder flip-chip application, the registration accuracy of the copper pads with the soldermask pattern must match with the solder bumping on the die. The receiving soldermask defined (SMD) pad or non-soldermask defined (NSMD) pad defines the shape of the joint structure for reliability and determines its pad pitch for bonding. The function of soldermask is to arrest solder wicking and prevent solder bridging between neighboring joints. The soldermask, with its poor registration tolerance, occupies real estate and limits the reduction of the bond pad pitch, as shown in Figure 2.10 [8]. Since copper metallization offers a better resolution than soldermask, the SMD pad offers a finer bond pad pitch for flip-chip applications, as illustrated in Figure 2.10. Assuming a minimum spacing of $30\mu\text{m}$ for copper, the SMD reduces the pad pitch by almost $40\mu\text{m}$. However, this pitch reduction is not significant enough for fine-pitch applications. Moreover, its joint reliability is weaker, as indicated by the low shear strength for SMD ball pad [45].

Figure 2.10: Flip-chip pad pitch architectures

The presence of soldermask plays an important role for flip-chip soldering. For fine pitch application of less than 200 μm , it has been recommended by Baggerman et al. [46] that a thicker soldermask layer is required to avoid short circuits between neighboring bumps. However, the increase in soldermask reduces the physical gap and hinders the underfilling [47]. The accessibility of these pads requires a higher standoff, which further limits the pad pitch for bumping.

As the pad pitch decreases, the inter-spacing between pads must be minimized to maintain sufficient pad width for joint reliability. This poses a difficult challenge for soldermask application. Even if the soldermask can meet the requirement, the narrow spacing will result in bridging due to either the slumping of the solder paste, the wetting of the solder during reflow, or the placement accuracy of the die bonder. This creates challenges in flip-chip assembly, as it requires more accurate die placement by the flip-chip bonder [48].

Polymer flip-chip technologies consist of conductive adhesive and conductive particle bonding. These technologies require high precision alignment to bond the bumps onto the substrate pads. The bondings are achieved at the expense of throughput [32]. For assembly robustness, the top pad width has to account for the equipment placement accuracy and reliability. As the pitch decreases, the contact area of the bumps and pads need to be maintained to ensure reliable joints. In addition, a conductive adhesive joint needs a minimum contact area to withstand thermo-mechanical stresses for conductivity while a conductive particle joint needs a threshold contact area that can capture sufficient conductive particles for conducting.

From a substrate perspective, these polymer flip-chip technologies offer a better pitch capability than flip-chip soldering as the soldermask layer is eliminated (Figure 2.11). Without the soldermask layer, the copper metallization on the substrate will be the only limiting factor for pad pitch. Assuming that a top pad width of 80 μm is needed for reliability, the subtractive process will provide a pad pitch of 160 μm for applications due to the trapezoidal profile. To further improve the pad pitch, the copper thickness has to be reduced using a half-etching process but this does not result in significant increase in pitch, as shown in Figure 2.11. Even with the use of advanced metallization techniques, such as the semi-additive process, a pad pitch of only 145 μm is achieved. Due to this limitation in the copper metallization processes, it is difficult and expensive to obtain substrates for flip-chip assembly with a pad pitch smaller than 150 μm . Consequently, substrate technologies remain as the limiting factor for flip-chip packaging.

*Subtractive Copper Foil : 12 μm Copper Plating : 10 μm min.

**Half Etch Copper Foil : 6 μm Copper Plating : 10 μm min

*** Semi-additive Copper Foil : 3 μm Copper Plating : 10 μm min
Ni/Au Plating : 5-13 μm /0.5-1.3 μm

Figure 2.11: A comparison of the minimum top pad width and inter-pad spacing achieved by different copper metallization techniques

The joint-on-via has been a recent pad architecture on the organic substrates to ease the routing for the 2nd level interconnect system. This architecture consolidates the joint and the copper pad onto the via land, thereby saving real estate on the substrate for routing. This architecture eliminates the need of neighboring via land at the expense of the routing design. This architecture requires an additional copper plating step to generate a copper layer over the via as the receiving pad (Figure 2.12). This additional plating increases the overall copper thickness and hence, decreases the routing density of the substrate. Thus, this technology is not commonly adopted by the industry. The joint-on-via enables the use of via as the receiving pad for flip chip and as an interlayer connection for substrate. Since the via land is larger than the existing flip-chip pad size, it has a larger pad pitch than existing flip-chip architecture. As such, the joint-on-via architecture is not applicable as a flip chip pad.

Figure 2.12: Typical fabrication flow of joint-on-via architecture on organic substrate

In summary, the pad pitch for flip-chip soldering is limited due to the need of soldermask in arresting the solder wicking. Polymer flip-chip technologies remove these soldermask layers and improve the pad pitch but these technologies are still limited by the substrate copper thickness to achieve a fine pad pitch. Hence, a new emerging copper metallization

technology or architecture is required to advance the substrate technologies in order to meet the fine pad pitch requirement for flip-chip packaging.

2.4 BONDING TECHNIQUES

Bonding is a process that assembles two different materials or parts together for economy and manufacturability. The different bonding techniques are discussed in this section in order to capitalise on the assembly techniques. Fig 2.13 classifies the different bonding processes into fusion welding, solid state welding, brazing, soldering, adhesive bonding and mechanical joining [49]. Fusion welding involves partial melting and fusion of the joint between two members when they are in liquid states. Flux or shield gases are commonly applied in a welding process to reduce oxides for bonding. The solid state welding is a fluxless bonding approach that joins two materials in their solid state through heat and movement of mating surfaces by plastic deformation. Brazing is a joining process, which uses a filler material with flux or shield gas to clean the surfaces before being joined. The brazing processing temperature is raised above 450°C to melt the filler metal while the base material remains in solid form. Soldering differs from brazing with the use of solder filler that melts below 450°C. The solder helps to fill the joints by capillary action between closely placed components with its superior wetting ability. Adhesive bonding refers to a joint or assembly with the use of a polymeric adhesive while mechanical joining refers to mechanical means of fastening materials temporarily together.

In semiconductor, the types of solid-state welding, soldering and adhesive bonding are commonly used as flip-chip bonding but faced with assembly constraints. This can be simply classified into the 5 main flip-chip interconnect systems as illustrated in Table 2.1. Soldering is seen in controlled collapse and cap reflow configuration. Solid state welding

is commonly applicable in thermocompression or thermosonic bonding techniques through wirebonds, TAB, gold-gold interconnect bonds in semiconductor packaging. As there is no self-alignment mechanism like solder, adhesive bonding is seen in conductive adhesive bonding and conductive particle bonding for flip-chip applications that require high precision placement to bond the bumps onto the pads of a substrate. As discussed in Section 2.1, flip-chip soldering technology is the preferred interconnect technique due to its high assembly yield, ability to eliminate probe mark by reflow, allowing rework after assembly, electrical stability and ease of accuracy placement with self-alignment effect. This bonding technique faces limitations due to the use of flux and its residues. This will be elaborated in the next section.

Figure 2.13: Types of bonding processes

2.4.1 Mechanism of Soldering

Soldering is defined as the process of joining metallic surfaces using solder without the melting of the base metal [50]. It forms interconnection between the various levels of an electronic package. The spreading of molten solder on solderable metallized surfaces such as Copper (Cu), Nickel (Ni), or Gold (Au) involves many complex physical processes. Poor solder-ability of the electronic components has resulted in significant manufacturing

difficulties when the current electronic packaging has an assembly performance of less than one failure in 10^6 joints. Figure 2.14 illustrates the various processes, which occur during the spreading of a solder droplet on a copper surface [51]. The initiation of the solder spreading depends on the heat flow and the melting of the solder. Subsequent solder spreading involves the fluid motion within the droplet. The flow patterns can be driven by capillary (reduction of surface energy), buoyancy (density) and liquid surface tension gradients (at a rate limited by the viscosity of the liquid solder) and the kinetics of the moving contact line. Thus, this makes the soldering mechanism complex.

Figure 2.14: Schematic representations of possible processes occurring during the spreading of a molten solder droplet on a Cu substrate

A bond between materials is formed as a thin layer of the substrate metallization dissolves by dissolution mechanism. A certain amount of bulk diffusion occurs, which diffuses the metal finish into the liquid solder and tin into the metal pad (a very thin, perhaps undetectable layer). These have resulted in the formation of the intermetallic compounds. The formation of the intermetallic provides a reduction in the free energy of the system and plays an important role in the overall dynamics.

The surface finish of a pad is typically contaminated with oxides, hydrocarbons, and other materials. This is due to the extended exposure of the surface finish in the manufacturing

environment. Likewise, the solder is contaminated by tin oxide due to its thermodynamic stability. With all these contaminants present, the pad cannot wet well with solder to form a good joint. Hence, flux is commonly used to assist soldering by [52]:

- (1) Removing the oxides from the metallization
- (2) Removing the oxides on the molten solder, hence reducing the surface tension
- (3) Inhibiting subsequent oxidation of the clean metal surfaces during soldering
- (4) Assisting in the transfer of heat to the joint during soldering

The flux consists of active agents (such as acids or salts) dissolved in suitable solvents such as alcohol. The flux removes the oxides and contaminants, leaving behind flux residues as by-products. If these flux residues are not removed, they are deleterious to the long-term reliability of an electronic package. These flux residues absorb moisture from the atmosphere and become an ionic conductor, promoting electrical shortening and corrosion. Entrapped flux residues in solder joints cause gross solder voids and premature failures. For flip-chip, these residues reduce the adhesion strength of the underfill with substrate interfaces and lower the moisture performance of a package [53-55]. Thus, if these flux residues are not removed, they are deleterious to the long-term reliability of an electronic package. Even with cleaning, there has been reported that metals still electro-migrated and resulted in current leakage [56]. Current practice is to remove these flux residues to its minimum using solvents that dissolve the flux and its by-products. Many of these solvents are chlorofluorocarbons (CFCs), which work well in removing these residues. However, the solvents are found to be environmentally hazardous as they deplete the stratospheric ozone layer [57]. In addition, the process effluents are toxic and need to be chemically pre-treated before disposal. This is to comply with the Federal Environmental Protection Agency (EPA), OSHA and RCRA regulations [58]. Thus, the

flux residues are not only nuisance to the bonding processes but also increase the operational costs.

For optoelectronic device assembly, the requirement of fluxless soldering is even more critical. The use of flux results in organic contamination on the optically active surface [59], which deactivates the device due to chemical interaction. Similar constraints are seen in the packaging of micro-electro-mechanical systems, fiber optic components, and microwave semiconductor devices [60]. Hence, there are strong economic and environmental incentives to develop a fluxless soldering methodology to eliminate the need of hazardous solvents in flux and its residues.

2.4.2 Fluxless Bonding

There are a variety of fluxless soldering technologies but none of these offers a robust flip-chip assembly process. These technologies can be classified in terms of their mechanisms as shown in Figure 2.15. These fluxless technologies are classified in terms of their mechanisms such as shield gases, solid liquid interdiffusion and solid state bonding. The technologies are discussed to leverage upon their mechanisms and devise a new strategy for fluxless bonding with a new pad architecture.

Figure 2.15: Types of fluxless bonding

The use of shield gases is the most common approach used in fluxless bonding. It consists of inert atmosphere soldering, acid-vapor soldering, hydrogen soldering and plasma-assisted dry soldering (PADS). All these fluxless bonding techniques use some means of controlled atmosphere such as shielding atmosphere or plasma, to reduce oxidation for better solderability. In inert-atmosphere soldering, the soldered areas are heated in an oxygen-free atmosphere to prevent oxidization. The challenge lies in the immediate operation after cleaning; otherwise the oxide will be re-formed on the surface. Acid-vapor soldering [51] replaces the flux with a diluted, vaporized acid that chemically removes the oxide layer. This technique is unfavorable as its reactive vapor causes corrosion in the assembly line and leaves residue that requires cleaning.

In hydrogen soldering, atomic and ionic hydrogen gas is introduced in a reactive atmosphere to reduce the thermodynamically stable oxides prior to the reflow process. However, this reactive gas is not easily controlled and is inefficient in breaking down the oxides at low temperatures [52]. The fluxless laser soldering achieves fluxless bonding by performing laser soldering in a controlled atmosphere such as hydrogen atmosphere [51-52]. The hydrogen atmosphere chemically reduces the oxide layer and enhances its solderability surface. The fluxless laser soldering involves the melting of a solder pre-formed with a directed Carbon Dioxide (CO₂) or Nd: YAG laser beam. This localized heating by laser allows the use of solder alloys with high melting temperature without damaging the neighboring materials.

In plasma-assisted dry soldering, the argon and hydrogen (Ar+H₂) plasma roughen and enhanced the solderable surfaces, but does not effectively prevent damage to the die passivation film [61]. This technique requires special handling and storage to prevent re-

oxidation of the surfaces [62]. The incorporation of controlled atmospheres in acid-vapor fluxless soldering, fluxless laser soldering, ionic hydrogen soldering techniques and PADS are to reduce or breakdown the oxide layer so as to enhance the solderability of the substrate pads. The difficulties in these fluxless approaches lie in the implementation and maintaining of the controlled atmosphere during production.

A fluxless die bonding technique uses solid-liquid interdiffusion for Sn-In [60, 63-64] and Au-In [65-66] solder in a controlled atmosphere. This bonding technique utilises a solid liquid interdiffusion with a unique layer structures as shown in Figure 2.16. The external layer of the structure is coated with a gold flash to prevent oxidation. The bonding is formed by raising the temperature beyond the eutectic melting temperature of the alloy, resulting in a liquid phase layer at the multi-layer interfaces. The liquid layer quickly dissolves the rest of composite by means of solid-liquid diffusion until full thickness and equilibrium composition are reached. This bonding technique is compatible with modern SMT processes and can potentially provide a high-density connection in electronic packaging [67-68]. Unfortunately, to achieve a good bond, this bonding technique requires a unique and costly layer structure with a controlled atmosphere for oxide reduction.

Figure 2.16: Layer structure for solid liquid inter-diffusion [60-64]

The methods of solid-state bonding (thermocompression, thermosonic bonding, or ultrasonic bonding) have been reviewed for fluxless flip-chip bonding, but individual method has its own limitations. Solid-state bondings are fluxless bonding through thermocompression, thermosonic or ultrasonic bonding techniques. These bonding are formed with their materials in solid states. Thermocompression bonding works on the principles of adhesion and friction. When two relatively flat surfaces are placed together, high pressure will be experienced at the contact zones due to the undulating surface. This produces deformation and plastic flow, which promotes the formation of numerous minute welded joints under thermal diffusion [4]. These micro-bonds are weak and easily fractured by the residual elastic stresses as the load force is removed. The thermocompression requires a relatively “clean” material that can withstand high processing temperature for bonding. The presence of any contaminants weakens its bonds, which are easily fractured by residual elastic stresses.

Ultrasonic bonding works on the fundamentals of friction and plastic deformation for bonding [4,69]. The ultrasonic energy allows the materials to be plastically deformed at a much lower stress as compared to pure thermal or mechanical energy. As the material plastically deforms, microscopic slip planes are formed and sheared across one another. As the slip planes slide over one another, new surfaces that are cleaned and highly energetic are formed. These clean metallurgical surfaces promote a solid-state diffusion of molecular species across interface boundary, promoting joint formation [70]. Ultrasonic bondings are limited by the damage of ball-bond interconnects during ultrasonic coupling; the co-planarity between the bonding tool and the set of bumps [71]; and the availability of ultrasonic transducers for high acoustic energy. The precision alignment and coplanarity of this technique further hinders its bonding capability for wide acceptance in flip-chip technologies. Ultrasonic bonding of Au and Cu/Ni/Au bumps with SnAgCu

solder have been reported by Lee et al., but this technique requires the pre-application of film to reduce porosity and dispersion time [72]. Thermosonic bonding combines both the thermal and ultrasonic energy into a bond formation. The ultrasonic frequency increases the strain rate and promotes plastic deformation with clean surfaces while the thermal energy enhances the joint formation through thermal diffusion. As thermosonic bonding employs both the thermocompression and ultrasonic bonding, it shares their challenges.

2.5 Au INTERACTIONS WITH Sn BASED SOLDER

Interdiffusion between metals forms intermetallic compounds and this impacts the reliability of the joints. Gold is commonly used in electronic packaging as interconnect and surface finish. This is because of its ductility and protection over corrosion. Due to the high solubility of Au, its initial thickness with reflow profile and thermal history will affect the joint microstructure and composition for joint reliability. Hence, it is important to study the interaction between Au with Sn based solders for use in flip-chip soldering. This section begins with an introduction of interdiffusion mechanism, followed by the equipment used for microstructure and ends with a morphology analysis. A summary on the kinetics of Au-PbSn and Au-SnAgCu interconnect systems by other researchers are also summarized in this section.

2.5.1 Interdiffusion

When two metals or alloys are in intimate contact with one another, there exists an interdiffusion between one or more of the species of each alloy into the other. In general, diffusion is a mass transport process at atomic scale while interdiffusion is a mutual mass transfer process between species at an interface. Interdiffusion may be discerned from a macroscopic perspective by a change in concentration over time as a result of net drift of atoms from a high to a low concentration region. Interdiffusion is of great importance in

the enhancement of an interface bond. A loss of control over the interdiffusion process can cause physical failure of an electronic device by degrading its electrical, chemical, mechanical or thermo mechanical properties.

Diffusion, including interdiffusion, is a mass transport phenomenon arising from atomic or molecular motion. The macro-scale motion of the matter observed in any diffusion process is a result of many small movements of individual atoms or molecules. Diffusion mechanisms are categorized based on the diffusion paths such as lattice diffusion, grain boundary diffusion, dislocation diffusion and surface diffusion as shown in Figure 2.17.

Figure 2.17: Schematic of Interdiffusion Path [74]

Lattice diffusion is also known as volume diffusion or bulk diffusion. It refers to the diffusion process in the interior of crystals [73-74]. In crystalline materials, there is a regular array of lattice sites, which are energetically favored positions for atoms. Each diffusion atom makes a series of jumps between various equilibrium lattice sites. These jumps allow the atoms to migrate through the point defects in the crystal. This is either done through vacancy or interstitial mechanism. Vacancy mechanism is a popular mechanism in lattice diffusion. It involves the interchange of an atom from a normal lattice position to an adjacent vacant lattice site or to a vacancy site generated by thermal instability. Interstitial diffusion involves small atoms diffusing into interstitial positions of large atoms.

The grain boundary diffusion refers to diffusion through the interfacial region separating two adjacent grains in a polycrystalline material [73-74]. Grain boundary diffusion dominates at low temperature where atomic diffusion in lattice becomes progressively more difficult. Atoms at the grain boundaries are less closely packed with high mobility. This is the result of large vacancies that existed along the boundaries. Therefore, atoms diffuse at a much higher rate along the grain boundaries. Hence, for metals, the activation energy by grain boundary diffusion is much lower, roughly about 0.6-0.8 times the activation energy of lattice diffusion mechanism [74].

The dislocation mechanism is a result of lattice disorder around the dislocation core providing loosely packed paths for atoms to diffuse through. Dislocation density is an important parameter in the diffusion processes, which are dominated by the dislocation pipe mechanism [75]. The dislocation density increases under stress by generating more dislocation source and decreases if it is annealed at high temperatures. Surface diffusion occurs at free surface of crystals due to the free paths of atomic diffusion. Surface diffusion can be driven by surface tension generated by the natural tendency of vapor-solid interfacial area.

Interdiffusion is important in the enhancement of interface bonds. However, it also forms intermetallic compounds that are brittle and undesirable. A layer of oxide, intermetallic compound or metal with low diffusion coefficient is often introduced to act as a diffusion barrier. The intermetallic compounds are mechanically brittle and may cause joint failure at elevated temperature because of the thermal expansion differences between the surrounding metals. Another failure mechanism seen in interdiffusion are the voids caused by Kirkendall shift after long thermal ageing. The Kirkendall shift is an effect of

interdiffusion when two originally homogeneous individual are put together. This has resulted in A atoms diffusing to the right and B atoms diffusing to the left across the interface as illustrated in Figure 2.18. If A diffuses faster than B, more atoms accumulate on the right side while atoms A are depleted on the left side of the interface after diffusion. If there is no change in lateral dimensions of the specimen, a mass invariant crystal plane (Matano interface) located originally at the interface will appear to move to the left at a distance X_K as shown in Figure 2.18. If the interface motion fails in a local region due to defect barriers, vacancies can accumulate at the location on the left side of the interface and gradually form the Kirkendall voids, which will accelerate the joint failure.

Figure 2.18: Schematic of the mass invariant Matano interface with the Kirkendall shift

2.5.2 Diffusion Models

Diffusion and interdiffusion models are based on Fick's First Laws. The law was originally generated from empirical observations. Fick's First Law represents the steady state diffusion driven by the concentration gradient across a pair of parallel planes separated with a distance dx as shown in Figure 2.19. Fick's First Law states that the flux J of a diffusing species passing through a plane normal to the x -direction is proportional to the concentration gradient, dC/dx , of the species [73-74]. This can be expressed as Eq. (2.1)

$$J = -D \frac{dC}{dx} \quad \text{----- (2.1)}$$

where J is the diffusing flux, D is the diffusion coefficient and dC/dx the concentration gradient

Figure 2.19: Rectangular volume of unit cross-sectional area between a pair of parallel plane separated with a distance dx

It is assumed that the concentrations at the interfaces are constant and equal to the equilibrium values. If we consider the flux of material from left to right is considered, the rate of advance of the interface at X_K is given by Eq. (2.2) [74-76].

$$(C_{LM} - C_{ML}) \frac{dX_K}{dt} = J_{LM} - J_{ML} \quad \text{----- (2.2)}$$

where t is the time, C_{LM} denotes the maximum solubility of M in L , C_{ML} denotes the maximum solubility of L in M , J_{LM} denotes the diffusion flux advancing from L into M and J_{ML} denotes the diffusion flux into M into L . Substituting Eq. (2.1) into Eq. (2.2) and $\lambda = x/\sqrt{t}$, the distance X_K of the Matano interface motion is derived as per Eq. (2.3) based on the Fick's First Law

$$X_K = 2 \left(\frac{DK_{ML} - DK_{LM}}{C_{LM} - C_{ML}} \right) \sqrt{t} \quad \text{----- (2.3)}$$

where D_{ML} is the interdiffusion coefficient at interface of phase M into phase L , D_{LM} is the interdiffusion coefficient at interface of phase L into phase M , $K_{ML} = \sqrt{t} \left(\frac{dC}{dx} \right)_{ML}$ and

$K_{LM} = \sqrt{t} \left(\frac{dC}{dx} \right)_{LM}$. Equation (2.3) represents a pair of metals L and M that are not fully miscible where a 2-phase layer is generated during the interdiffusion [74, 76-77]. The concentration depth profile after a certain time and annealing temperature are shown in Figure 2.20 with a concentration discontinuity between C_{LM} and C_{ML} .

Figure 2.20: Concentration-Depth Profile and Phase-Diagram of a Partially Miscible Couple, Metals L and M [74,76]

Figure 2.21 shows the C-x curve and corresponding equilibrium diagram for a system in which a single intermediate phase occurs in addition to the two primary phases α and γ . A single layer of β phase is formed with concentration limits $C_{\beta\alpha}$ and $C_{\beta\gamma}$. Applying Fick's law as per Kidson's equations with a diffusion layer in-between the primary phases α and γ phases the shift of the $\xi_{\alpha\beta}$ interface, $\xi_{\beta\gamma}$ interface and W_β , the growth of the intermetallic layer with respect to the mass invariant Matano interface are expressed in Eq. (2.4) to (2.6) respectively [74-76].

$$\xi_{\alpha\beta} = 2 \left(\frac{(DK)_{\beta\alpha} - (DK)_{\alpha\beta}}{C_{\alpha\beta} - C_{\beta\alpha}} \right) \sqrt{t} \quad \text{----- (2.4)}$$

$$\xi_{\beta\gamma} = 2 \left(\frac{(DK)_{\gamma\beta} - (DK)_{\beta\gamma}}{C_{\beta\gamma} - C_{\gamma\beta}} \right) \sqrt{t} \quad \text{----- (2.5)}$$

$$W_\beta = \xi_{\beta\gamma} - \xi_{\alpha\beta} = 2 \left[\left(\frac{(DK)_{\gamma\beta} - (DK)_{\beta\gamma}}{C_{\beta\gamma} - C_{\gamma\beta}} \right) - \left(\frac{(DK)_{\beta\alpha} - (DK)_{\alpha\beta}}{C_{\alpha\beta} - C_{\beta\alpha}} \right) \right] \sqrt{t} \quad \text{----- (2.6)}$$

Figure 2.21: Concentration-Depth Profile and Phase-Diagram of a Partially Miscible Couple with Intermetallic Compound Formation [74,76]

As the growth is diffusion controlled, the growth of the intermetallic layer x' for solid interdiffusion is commonly represented by Eq. (2.7) [78-79].

$$x' = \sqrt{Dt} \quad \text{----- (2.7)}$$

where D denotes the coefficient of diffusion.

The diffusion coefficient D in Eq. (2.7) can be described by the Arrhenius equation. Past-published studies have established that the diffusion rates in metals such as Ni and Au in eutectic solder [73-74] follow the Arrhenius relationship as seen in Eq. (2.8)

$$D = D_0 \exp\left(-\frac{Q}{RT}\right) \quad \text{----- (2.8)}$$

where D_0 is the diffusion constant in cm^2/s , Q denotes the activation energy in J/mole, R the gas constant in $\text{J/mol}^\circ\text{K}$ and T the absolute temperature in $^\circ\text{K}$. The diffusion constant D_0 and activation energy Q are material properties, which vary with composition but are independent of temperature. Q and D_0 can be obtained experimentally. Applying natural

logarithm to both sides of Eq. (2.8), the expression offers a straight line to be plotted between $\ln D$ vs. $1/T$ as shown in Figure 2.22. From this plot, Q and D_0 can be determined from the gradient and y-intercept respectively.

Figure 2.22: Coefficient of diffusion D versus a function of temperature T

2.5.3 Equipment for Analysis

The scanning electron microscope (SEM) produces an image with the use of an electron beam that scans the specimen's surface. The sample preparation is relatively simple since SEM requires only a conductive sample for the electron beam. The electron beam produces a very high magnification and resolution image of the specimen under examination. With a large depth of field, the SEM allows a large amount of the sample to be in focus for examination.

Energy dispersive x-ray spectroscopy (EDX) is an elemental microanalysis technique performed in conjunction with a scanning electron microscope. When the electron beam bombards the specimen, electrons are ejected from the atoms comprising of the sample's surface. An electron from a higher shell fills the resulting electron vacancy and an X-ray is emitted to balance the energy difference between the two electrons. This discrete X-

rays are used as the element's unique 'finger print' for identification. Features or phases as small as $1\mu\text{m}$ can be analyzed with EDX.

2.5.4 Au with PbSn Solder

In eutectic solder, Sn is the active element with Pb acting as filler. The primary function of Pb is to lower the melting point of pure Sn from 232°C to 183°C for soldering purposes. Pb is added to Sn to lower the cost, ease manipulation, enhance corrosion resistance and lower the surface tension of Sn for manufacturability. The use of the solder in modern microelectronic technology is ubiquitous due to its indispensable role in stencil printing, good thermal performance, reliable joints and robust assembly processes [51-52]. Au is commonly used with solder in a flip-chip interconnect system [80-82]. However, being a tin-based solder, a poor reliability with Au may result due to rapid kinetics in the formation of brittle intermetallic compounds (IMCs). The formation of IMC gives rise to decrease joint reliability, dampening the prospect of Au with solder in flip-chip applications. Thus, the kinetic of Au with eutectic solder is studied to enhance the joint reliability.

The binary section of the Au-Pb-Sn ternary phase diagram is presented in Figure 2.23 [83-85]. The phase diagram can be visualized as the addition of lead lowering the peritectic and eutectic point. From the phase diagram, the $\text{AuSn}_4+\text{Pb}+\text{Sn}$ will be stabilized below 177°C up to 15.5 at% Au. This is 6°C lower than the eutectic point of $63\text{Pb}37\text{Sn}$ [83]. As the temperature increases, the solid liquid phase stabilizes in the form of AuSn_4+L for small amount of Au up to 208°C . Once above 208°C , the thermodynamics shift with the formation of new solid liquid phase of AuSn_2+L .

Figure 2.23: Binary Section of the Au-Pb-Sn ternary phase diagram [83-85]

As Au comes into contact with molten solder, this initiates a solid-liquid interdiffusion at the bonding interface. Researchers found that solutes in noble metals, such as Au, diffuse very rapidly in Sn [86-88]. This rapid diffusion is attributed to the interstitial diffusion mechanism via a bulk diffusion mechanism to form Au-Sn intermetallic compounds. This has resulted in the formation of Sn rich phases. Likewise, a slow substitution of solid solution of Sn in Au will occur. A large difference in the interdiffusion rate of Au in liquid Sn versus Sn in solid Au is observed.

Both dissolution and reaction play an important role during solid liquid interfacial interaction [83]. The total chemical driving force arises from the dissolution of metal pad finish into molten solder and interacts to form intermetallic compounds [89]. According to the thermodynamic principles, Tu et al. reported [90] that the dissolution of Au into molten solder must occur first when the molten solder is in contact with Au. Assuming a

local equilibrium concept at the interface [91], the concentration of the Au can be assumed to be somewhere on the metastable substrate + PbSn liquid phase boundary. Thus, the Au dissolves into molten solder and reaches its solubility limit of Au at the interface. This initiates the growth of IMC formation at the interface. However, it is unnecessary for the entire molten solder to reach the solubility limit. Rather, a boundary layer of the molten solder next to the Au interface becomes saturated and slightly super-saturated, which thereafter the intermetallic compounds can nucleate heterogeneously and grow. The IMC nucleates and grows by interfacial reaction at the boundary layer while the dissolved Au diffuses easily from the boundary layer to the rest of the molten solder to avoid super-saturation. The boundary layer eventually grows into a continuous layer and becomes a diffusion barrier to the subsequent dissolution. The IMC layer of AuSn_4 and AuSn_2 were reported at the interdiffusion interface after solidification.

Ho et al. [92] reported different findings for Au/Ni/Cu with eutectic solder at reflow. Their study suggests that the Au layer reacts with Sn to form AuSn_4 . The AuSn_4 then breaks off and falls into molten solder. During reflow, the solder balls partially melt along the ball/pad interface at the ternary eutectic reaction at 177°C instead of the eutectic PbSn temperature. This is a result of good heat transfer by flux and high thermal conductivity of Cu. The dissolution of Au atoms into eutectic PbSn solder induces a partial melting at the interface, and the reaction of Au and solder produces Au-bearing intermetallic compounds of AuSn_4 and AuSn_2 at the bonding interface. Due to the eutectic point of Au with eutectic SnPb, the formation of AuSn_4 occurs at 177°C [83] after solidification. As a result of the thermodynamic instability of AuSn_4 with Au, the AuSn_2 layer is formed in-between the Au and AuSn_4 layer. Once the barrier is formed, it retards the rate of Au dissolving into solder [88]. When the Au-layer is consumed, the AuSn_2 is converted into $(\text{Au}_x\text{Ni}_{1-x})\text{Sn}_4$, which breaks off from the interface and falls into

the solder. The Ni then starts to react with Sn to form Ni_3Sn_4 at the interface. The growth rate of Ni_3Sn_4 is slower in comparison to the Au-bearing compounds.

Besides the continued dissolution of Au, the IMC layer is also consumed in the molten solder through the spalling of AuSn_4 intermetallics from the interface [83, 90]. The AuSn_4 residing inside the solder is precipitated as needle-like AuSn_4 intermetallic structure upon cooling. This phenomenon is explained from the lowering of its free energy by forming agglomerations of AuSn_4 as suggested by the phase diagrams. The precipitation of the AuSn_4 phase led to the depletion of Sn in the surrounding matrix, thus resulting in the formation of Pb-rich islands [88]. The AuSn_4 appears to migrate onto the interface during solid-state aging at high temperature as reported by Ohriner et al. [93]. With aging, the Ni_3Sn_4 layer also increases. The reconfiguration of Au to the interface is a consequence of the availability of Ni to form thermodynamic $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ ternary compound [94].

The morphologies and kinetics at the interface produce a profound effect on assembly and joint reliability. As Au diffuses into solder rapidly [86, 88], the formation of brittle Au-containing IMC is a serious concern for reliability. According to Kim et al. [88], Au has an interdiffusion coefficient of $6 \times 10^{-7} \text{ cm}^2\text{s}^{-1}$ in molten solder at 240°C . The other researcher quantified the kinetics by the dissolution rate of Au wire in eutectic solder to be $1.33 \mu\text{ms}^{-1}$ at 209°C [84, 95-96]. This fast kinetic is due to the fast dissolution of Au in molten solder, forming coarse, anisotropic, and brittle Au-Sn compounds which weaken the interface between the Au-Sn compounds and the solder matrix.

2.5.5 Au-PbSn joint reliability

The Au and PbSn kinetics at the solid liquid interface determine their phase morphologies and hence affect the joint reliability [97-98]. The AuSn compounds precipitated led to the

embrittlement of the solder joint due to a weak interface between the Au-Sn compound and the solder matrix. However, for a smaller amount of Au content, the Au-Sn compounds are dispersed in the solder as a minor phase. Hence, this will not cause failure. As a result, the thickness of Au film on pad must be minimised to reduce embrittlement. It has been recommended that the Au concentration in the eutectic 37Sn63Pb, pure Sn, 96Sn4Ag molten solder is not greater than 5, 10 and 10 wt% respectively [97] for solder joint. This will require very tight process controls on the part of the assembler to ensure long-term reliability of these joints on the PCB [97].

Past literatures [99-100] have attributed the brittle interfacial fracture of the joint to the adhesion between Ni_3Sn_4 and Ni-P for electroless nickel and gold finish. This is a result of phosphorous segregation at the interface between the Ni_3Sn_4 intermetallic and the Ni-P layer. During soldering, the molten SnPb solder dissolves the Au layer and contacts the underneath Ni-P alloys. Since phosphorous atoms do not take part in the Ni_3Sn_4 formation, they segregate at the interface between the Ni_3Sn_4 and Ni-P. Due to the brittleness of Ni_3Sn_4 intermetallic and Ni-P alloy from the electroless nickel and immersion gold finish, the brittle interfacial failure occurs between the interfaces.

Ferguson [97] and Darveaux [101] et al. have reported that upon thermal aging, the AuSn_4 migrates from the bulk of the solder joint to the solder interface adjacent to the Ni intermetallic, resulting in both decrease in the peel strength and the shear strength of the solder joints. Both the peel strength and the shear strength decrease with subsequent increase in Au thickness. The coexistence of these two phases, with poor adhesion properties between them, is held responsible for the deterioration of the joint. The Au related interfacial fracture might be eliminated by reflow after aging as it moves the AuSn_4 phases back to the solder joint interior. Once reflow, the AuSn_4 intermetallic is

dissolved from the interface back into the solder joint and the weakest interface in the as-reflow structure is transferred to the Ni_3Sn_4 and the Ni-P layer.

Zribi [68] and Minor [94] et al. attributes the joint failure on an electrolytic gold finish, to the brittle $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ intermetallic after thermal ageing. The growth of $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ in thermal ageing is due to its kinetic preference as shown in Au-Ni-Sn ternary phase diagram. This growth depends on the bulk diffusion of Au towards the solder/substrate interfaces and the coarsening effect of the precipitates. The interfaces between the intermetallics and the bulk solder become smoother as a result of the thermodynamic driving force. Hence, the growth of the ternary $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ at the Ni_3Sn_4 /PbSn interface decreases the joint toughness upon thermal ageing and eventually results in joint failure.

To minimize failure, multiple reflow processes and reduction of Au content are recommended to enhance the Au with PbSn joint reliability [102-103]. The use of reflow decreases the disposal of intermetallic by redistributing the intermetallic compounds back to the solder. This reduces the intermetallic formation and improves the solder joint reliability.

2.5.6 Au with SnAgCu Solder

Lead-free soldering has become a global trend in the microelectronic packaging due to the registration and implementation of taxes for lead containing solders for electronic, automotive, and aircraft industries [88,104-106]. This legal ban is due to lead being poisonous as its uses are resulting in environmental pollution and impairing workers' health. The most aggressive and well-known effort is the European Union's "Waste in Electrical and Electronic Equipment" (WEEE) directive that proposed a ban on lead in electronics by the year 2006. The Japanese electronics industry has been aggressive in

developing technologies and processes that produce products that are Pb-free, halogen-free and recyclable. Current research has shown that there are no drop-in replacements for eutectic 63Pb37Sn solder due to its reflow temperature and joint reliability.

Recent studies have shown that SnAgCu (SAC) solder is a promising Pb-free solder [104-106] as it possesses excellent wettability and good compatibility with existing assembly processes. This is due to SAC having a low melting temperature (217°C) and better interfacial properties than binary Pb free alloys [107]. SAC also offers good resistance to migration [108] and superior mechanical properties [109-110] for interconnections. Being a tin-dominant lead-free solder, SAC suffers poor reliability with Au due to its rapid formation of brittle Au-Sn intermetallics [97-98]. This dampens the prospect of Au with SAC for low-cost, fine-pitch, flip-chip interconnect systems [29].

Due to its high Sn content, it is expected to form excessive reaction and growth of intermetallic during reflow and thermal ageing processes. Recent studies have indicated that the intermetallic growth rates increase as a function of increasing Sn content in the solder alloys [68]. Due to the lack of available phase diagram for Au with SAC, AuSn phase diagram [111-112] is the closest available equilibrium phase diagram for reference. The gold—tin system shown in Figure 2.24 presents one of the most complicated and intriguing binary systems.

The basic reason for complexity is that gold and tin not only form several intermetallic compounds but also form solid solution with up to 18.5 at% of tin in Au. The gold tin binary diagram contains two eutectic transformations; one occurs at 278°C (Au-30Sn at%) while the other at 217°C (Au-94Sn at%). The former eutectic composition is widely used for soldering which consists of two phases, AuSn(δ) and Au₅Sn(ζ'). The other Au-

94Sn at% eutectic occurring at 217°C, which is a mixture of AuSn₄ compound and β-Sn. Au-Sn offers a lower bonding temperature but it forms brittle phases of AuSn₄ that are deleterious to packaging applications.

Figure 2.24: Gold-tin equilibrium phase diagram. Stable intermetallic compounds are

δ: AuSn, ε: AuSn₂ and η: AuSn₄ [85]

Both dissolution and reaction play important roles at the interface during the solid liquid interdiffusion. These mechanisms have yet to be quantified. The Au dissolves and diffuses throughout the molten solder. Shin et al. reported that the dissolution of Au with molten SnAg occurs first as AuSn₄ intermetallics are seen throughout the molten solder [29]. Simultaneously, the Au reacts with molten solder [113], which appears as an instantaneous dissolution. This eventually forms a diffusion barrier, which retards the rate of Au dissolution. Au continues to dissolve into solder either by diffusing through the layer or spalling off from the interface [29]. During cooling, the saturated solution then precipitates as AuSn₄ [29]. Since silver (Ag) has little solubility with the phases at the

interfaces, Ag has no role in forming any intermetallic [114]. Thus, the only thermodynamic layer of AuSn, AuSn₂ and AuSn₄ are formed as Au interacts with molten SnAg.

There is limited literature on the kinetics of Au with molten SAC. When Au dissolves in SnAg, the small amount of Ag resulted in extremely fast dissolution of Au into molten solder to form AuSn₄ compounds. Using the relationship of $(x')^2 = Dt$, it is estimated that the dissolution requires a diffusivity about $4 \times 10^{-5} \text{ cm}^2\text{s}^{-1}$ at 230°C for 10s [88]. This is in the same order of magnitude as atomic diffusion in molten metals ($10^{-5} \text{ cm}^2\text{s}^{-1}$). This shows that Au has a fast dissolution rate with molten Sn base solder. In solid diffusion, researchers found that solutes in noble metals, such as Au, diffuse rapidly in Sn [86] with a $t^{0.5}$ growth rate. The IMC growth rate can be expressed as the square root product of diffusivity and time [115]. The high Sn content in SAC promotes excessive reaction and growth of IMC [110] than eutectic solder. These intermetallic compounds tend to be brittle at ambient temperature and are considered a potential cause of crack initiation and growth in electronic assemblies.

Baggerman et al. [46] reported that oxidation of tin is a major challenge in achieving quality bonding and hence limit its uses [51-52]. This is a result of thermodynamic principle, which prefer a tin oxidation than intermetallic growth. The tin oxidation has an activation energy of $Q = 33 \text{ kJ}$ and diffusivity $D = 3.7 \text{ nm}^2/\text{s}$ versus that of the intermetallic growth $Q = 70 \text{ kJ}$ and $D = 3.0 \times 10^{10} \text{ nm}^2/\text{s}$ [46]. Another disadvantage of the Au-Sn interconnection system is the formation of pores in the Au-Sn alloy. These Kirkendall voids are mainly found at the interface between the substrate finish and the Au-Sn alloy. These voids are caused by the segregation, formation of oxides and carbons on the molten solder [85]. Design and process optimization are needed to achieve a

relatively good joint with minor gaps. Even with the use of flux, these gaps are not avoidable in all process optimization cases. These voids and the brittle intermetallic compounds in the interconnection layer reduce the bond strength remarkably. Typical fatigue failure for AuSn solder is due to crack propagation or fracture.

2.6 THERMO-MECHANICAL STRESSES AND ITS FAILURE MECHANISMS

In most microelectronics applications, the prominent damage mechanisms on solder joints may be due to elastic deformation (vibration loads), time independent plastic deformation (thermal shock) or time dependent creep deformation (thermal cycle) [116]. These failures are a result of stresses and strain induced by the differences in coefficient of thermal expansion (CTE) between the silicon chip and the substrate [117-119]. Without underfilling, the mismatch creates a high shear strain in the solder joint during thermal cycling and hence, results in initiation and propagation of creep fatigue crack. The total strain ε in the solder joint is directly proportional to the distance from the neutral point (DNP) [117,120] as shown in Eq. (2.9)

$$\varepsilon = \Delta\alpha \cdot \Delta T \cdot (\text{DNP}/h) \quad \text{----- (2.9)}$$

where $\Delta\alpha$ is the expansivity mismatch between chip and substrate, ΔT denotes the temperature range for cycling, h is the joint height and DNP denotes the distance from the neutral point of the chip. From Eq. (2.9), a strong dependence of the shear strain and DNP is observed i.e. the amount of shear strain decreases with increasing solder joint height [121] or decreasing DNP. When more solder bumps exist at any given DNP, the fatigue life improves as the overall stresses are distributed across the structure [122].

An important technique to dramatically increase the fatigue life of the flip-chip solder joints is to underfill the chip with an epoxy resin as shown in Figure 2.25. This helps to

constrain the expansion mismatch between the chip and substrate [123]. The encapsulation material acts to mechanically couple the die and substrate together and constrain the CTE mismatch. The filled epoxy encapsulant matches the CTE of the bumps and minimizes the stresses on the solder joints. Therefore, it helps to increase the joint fatigue life. This technique has added a new dimension to flip-chip packaging by enabling the flip-chip packaging of larger chips. The underfill has improved the life of controlled collapse chip connection (C4) joints by a factor of 5-20 times over conventional un-encapsulated joints [124-125].

Figure 2.25: Schematic illustration of underfill flip-chip on board

Although the presence of underfill material improves the reliability of the solder joints, it transfers the thermo-mechanical stresses to the chip, substrate and the encapsulant. When the temperature is lowered after the curing of underfill material, the mismatch in thermal expansion coefficient between the chip and the substrate will lead to device bending and shear deformation in the underfill layer. Because of this dissimilarity in CTE between the underfill and the solder, the joints are also strained in the direction of their z-axis [120,126] with reference to Figure 2.25. The stiffness of the underfill is so great that the deformation mode is changed from shear dominated without underfilling to a uniform strain with package warpage for underfilling [119].

The Coffin Manson equation is widely used to predict and relate the maximum plastic strain to the solder bump fatigue lifetime [117-119] as shown in Eq. (2.10). The thermal

fatigue crack occurs in the region with maximum plastic strain range and Eq. (2.10) can be used for package with and without underfill. In Eq. (2.10), N_f denotes the number of cycle to failure, ϵ_p the plastic strain range, $C = 2.332$ and $n = -1.475$ are material constants [119].

$$N_f = C \cdot \epsilon_p^{-n} \quad \text{----- (2.10)}$$

As the solder joints deform due to cyclic loading, the underfill results in both in-plane and out-of plane displacement, introducing normal and shear strains in the solder joints. The out-of-plane strains are greater than the in-plane strains [116]. The out-of-plane strains result in a doming effect due to the CTE of the silicon die dominates a thinner substrate. The accumulated strain range per cycle weakens the solder joints and eventually leads to fatigue failure. The strain range ($\Delta\epsilon$) directly relates these normal or shear strain components in one thermal cycle to the fatigue life of the solder joint. Both the shear and axial (σ_{xx}) plastic strain contribute to the mechanical wear out of the bumps [127]. To calculate the combined effect of the z components in the underfill flip-chip package, the effective plastic strain ϵ_p must be calculated, as the elastic strain is only a small part of the total strain ϵ defined by Eq. (2.9).

Underfilling is a delicate assembly process, which is likely to generate voids. Some studies [128-129] have suggested that most flip-chip joints fail due to the presence of voids in underfilling. This is attributed to the propagation of underfill delamination. A good adhesion between the underfill material, the substrate, and chip surface is needed to act as a stress compensating function [115]. The use of flux during soldering reduces its interfacial adhesion and affects its reliability performance [76-77]. Thus, a fluxless soldering technology for flip-chip assembly is desirable.

The underfill decreases the plastic strain range in the solder by approximately one order of magnitude. This enhances the solder joint reliability. The effectiveness of the underfill also depends on its material properties. The underfill reduces the dependence of the standoff height and its die size on the fatigue performance. The underfill material properties are important to enhance flip-chip fatigue. Popelar [116] and Gektin [124] et al. reported that underfill with a CTE of 14-18 ppm/°C helps to minimize the total damages in the solders, resulting in an optimal fatigue life. This can be achieved through the addition of fillers; which decreases the CTE and increases the Young modulus for reliability [126]. In doing so, the high filler loading affects the processibility of underfilling and thus, the loading of filler needs to be optimized. High glass transition temperature for underfill is also desired as it impacts its operating temperature. When the joints operate above T_g , the elastic modulus decreases by an order of magnitude [120] while the CTE increases by a factor of three. This impairs the performance of the underfill due to extra degrees of rotational in the cross-linked polymer which losses its benefits of coupling the die and the substrate. Underfill in its rubber state may even damage the solder joints [123].

Other than its material underfill properties, the geometry of the package structure and its substrate also affects its joint reliability. The increase in die size and board size increase the plastic work in bumps. This results in early fatigue. On underfill gap, simulation model concludes that the increase in solder height will increase the interface stresses but decrease the inelastic strain in the solder [130]. However, the gap determines the quality of related assembly parameters such as underfill flow and voids while the higher joints are more flexible and cause less plastic deformation for a given amount of chip to board displacement [123]. The substrate material has an effect on the thermo-mechanical stresses and affects its joint reliability. Compliant substrates help to improve the

reliability of solder joints as well as of the whole module [118]. These substrates allow cycling bending and movement due to thermal and power cycling. For example, flex helps to dissipate the energy and minimizes the energy absorption for fatigue [116]. Mathematical calculations and finite element modelings have shown that the hourglass-shaped solder [131] and stacked solder bump [132] also help to relax the stresses. The geometry of the joint helps to reduce the cyclic strain and thereby, enhances the solder joints performance. This section suggests that proper selections of material through material characterization with good underfill processes are required to enhance the solder joint performance.

2.7 SUMMARY ON LITERATURE REVIEW

The bumping technologies satisfy the advancement of die pad pitch. The challenge in flip-chip packaging lies in the geometry mismatch of substrate technology and the die pad pitch. This has been attributed to the lagging substrate technologies; especially in the area of copper metallization and pad architecture for flip-chip interconnect systems. In flip-chip soldering, the pad pitch is limited due to the need of a soldermask in arresting solder wicking. The advanced polymer flip-chip technologies help to minimise this challenge by removing the need of a soldermask but this enhancement is still not sufficient to meet the pad pitch advancement. This limits the quest of flip-chip technologies for miniaturisation and increase functionality. The dependence of the pad pitch by copper metallization and its pad architecture on substrate are being challenged for the advancement of flip-chip technologies.

Due to the instability and poor reliability of polymer flip-chip, flip-chip soldering remains as the preferred candidate for flip-chip packaging. This is driven by the use of soldering which offers a high throughput, high assembly yields and electrical stability. The use of

flux and its residues in soldering contaminate the devices and restrict the use flip-chip technologies in optoelectronic, micro-electro-mechanical system and microwave semiconductor devices. Current fluxless bonding techniques face individual challenges and cumbersome in production implementation. Therefore, a fluxless flip-chip bonding on a fine pitch organic substrate is seen as a cost-effective solution that enables a wide adoption of the flip-chip packaging.

A review of Kidson's equations based on Fick's First law is presented to revise a model for solid liquid interdiffusion. The kinetics and interactions of Au with PbSn and SnAgCu solders are reviewed to understand the growth of their intermetallics and their effects on the joint integrity. A summary of past literatures of the interfacial reactions between Au and Sn based solder is presented. The mechanical reliability of intermetallic compounds at the interface influences the mechanical integrity of the solder joint. These intermetallics tend to be brittle at ambient temperatures and are considered a potential cause of crack initiation and growth in electronic assemblies. AuSn_4 has been noted for its particular deleterious effect on both bulk and interface properties for solder joint performance. The high Au concentration is shown to impair the mechanical strength of the joint. The thermo-mechanical stresses in flip-chips are also reviewed to devise material selection criteria for assessing the joint reliability. Underfill helps to increase the fatigue life of the solder by mechanically coupling the die and the substrate together. The underfill properties such as CTE and good adhesion ability are important to enhance the joint fatigue. The package structure and joint geometry also affect the fatigue life. Proper selection of packaging materials through characterizations with good underfilling processes are required to enhance the flip-chip fatigue life.

CHAPTER 3

JOINT-IN-VIA ARCHITECTURE

The substrate technologies are identified as the stumbling block to meet the advancement of die pad pitch. The high routing density of the substrate is currently achieved by the advanced copper metallization techniques couple with micro-via and build-up technologies. However, with these advanced technologies, the pad pitch remains as an obstacle for flip-chip applications due to the limitations in the pad bonding architecture and the copper metallization techniques. Currently, RDL is used to bridge the technology gap between the wafer and substrate technologies by redistributing the pad pitch to accommodate the substrate. However, this increases the overall packaging cost and restricts the flip-chip applications to optoelectronic and micro-electro-mechanical systems. This is due to its bonding techniques and the chemicals used in RDL. A new substrate architecture without depending on copper thickness and soldermask registration is required to meet this challenge. This architecture is still required to meet low cost, high routing density and good electrical performance for flip-chip packaging. This ideal architecture should be coupled with a robust, fine pitch, fluxless assembly process for flip-chip advancement. This project proposes the use of a joint-in-via architecture that consolidates the landing pads, through via and flip-chip joints into one common element. The joint-in-via architecture relies on the use of current micro-via technologies on organic laminates. This architecture capitalizes on the current substrate copper metallization technologies and versatile micro-via technologies for fabrication.

3.1 ADVANTAGES OF THE JIV ARCHITECTURE

Figure 3.1 compares the conventional pad architecture versus the proposed joint-in-via architecture in terms of package height and performance. Physically, the joint-in-via

architecture offers a lower package height with shorter electrical path for better electrical performance. The joint-in-via architecture consists of an overhanging copper trace beneath the via opening. It helps to re-distribute the electrical signals from the joint in the via to the designated I/O of the package. This architecture allows the overhanging trace width to be smaller than the via, easing design rules for copper metallization and patterning tolerances.

Figure 3.1: Schematic comparison of conventional flip-chip architecture (left) vs. joint-in-via architecture (right). The joint-in-via architecture offers a lower packaging profile and shorter electrical path for communication

The joint-in-via architecture relaxes the design rule such that the subtractive etching can be used for fine pitch applications. The architecture removes the dependence of the top pad width and the copper thickness, thereby allowing the substrate to have a thicker copper finish for better electrical performance and package reliability. The architecture removes the need of via land and free out more space for routing. Figure 3.2 illustrates the physical routing area for SMD, pad define with and without soldermask and the joint-in-via architecture for a receiving pad diameter of 80 μm . These designs are based on the state-of-the-art technology from existing substrate suppliers' capability using a 30/30 μm design rule, 80 μm via capability and a 50 μm soldermask registration. For example, Design 3 for polymer flip-chip is designed with a larger copper pad to accommodate for its bonding accuracy and its bond strength as it utilizes only the top pad for bonding.

Figure 3.2: Joint-in-via saving on routing spaces based on illustration drawn to size for 80 μm bonding pad using advanced 30/30 μm design rule, 80 μm via capability and 50 μm soldermask registration

The reduction in length, width and routing area on the different pad architectures are summarized in Figure 3.3 for analysis. The joint-in-via architecture is found to occupy less real estate as compared to current architecture. It has an 80% reduction in routing area as compared to the SMD pad. The micro-via architecture does not contain any wall metallization and thus, eliminates additional processing steps, wastage of via land or reliability concerns over electrical discontinuity. The architecture eases the routing design rule for fabrication and enhances the robustness of the substrate for reliability.

Figure 3.3: Comparisons between different pad architecture showing JIV having reduction in length, width and routing area

The proposed joint-in-via architecture migrates the bond pad pitch design rule from the copper metallization and soldermask registration to the micro-via capability. The micro-via assists in arresting solder wicking and prevents solder bridging, thereby removing the need of a soldermask. This enables the flip-chip soldering to have similar pad pitch capability as the polymer flip-chip as well as allowing a solid-liquid bonding. The proposed joint-in-via architecture relies on micro-via capability instead of the copper metallization for pitch improvement. The micro-via techniques may have the potential of

narrowing the inter-spacing and further reducing the pad pitch as illustrated in Figure 3.4. If the proposed joint-in-via architecture is able to match the die pad pitch, it potentially removes the need for RDL processes and reduces the overall packaging cost significantly.

Figure 3.4: Joint-in-via architecture reduces pad pitch for packaging

Bonding material is deposited into the micro-via to join the bump and the routing trace together. The micro-vias, which act as aperture openings for stencil printing, guide the bonding materials into the micro-vias for bumping. The joint-in-architecture makes dual use of via for interlayer connections and flip-chip soldering. Thus, allowing a shorter electrical path with lower resistance and inductance as compared to a conventional flip-chip package. This enables a direct electrical path from die to the PCB, thereby enhancing the integrity of the electrical signal.

The proposed joint-in-via architecture helps to enhance the robustness of the flip-chip assembly. The joint-in-via architecture improves the assembly yield by enabling a fine pitch bonding. The architecture arrests the solder wicking and prevents solder bridging during bonding with narrow inter-spacing. With a large receiving pad, the joint-in-via architecture has the potential of using current packaging infrastructure for flip-chip assembly since it relaxes the placement accuracy. This in turn improves the assembly

throughput, as high accuracy alignment by vision is not required. Since the joint sits into the micro-via of the organic substrate, the joint-in-via architecture increases the overall standoff without any compromise in the package height. Without underfilling the joint, the increase in standoff is expected to reduce the shear strain and improve the joint fatigue performance. With underfilling, the gain in standoff height provides more flexibility and less plastic deformation for a given amount of substrate displacement. Thus, the additional margin allows a wider choice of interconnect systems. Six United State patent applications (listed in the Appendix) have been filed on the joint-in-via architecture, demonstrating its commercial values and innovations.

The proposed joint-in-via architecture aims to resolve the pad pitch challenge for substrate and offers a robust flip-chip assembly process with the use of existing packaging infrastructure. This technology leverages on the use of current packaging infrastructures and substrate technologies to resolve the flip-chip pad pitch challenge.

3.2 INTERCONNECT SYSTEM

The joint-in-via architecture aims to resolve the pad pitch limitation but it needs to integrate with an interconnect system for packaging. Conductive adhesive and particle bonding are still in their infancy stage with on-going studies to resolve the junction instability and reliability concerns for polymer flip-chip bonding. The slow throughput and high material cost further hinder the acceptance of polymer flip-chip interconnect systems for high volume production. Large capital investment is needed to purchase new flip-chip bonder with specific bonding capability. Hence, metallurgy flip-chip interconnect system is still the preferred choice of interconnect system with the joint-in-via architecture as it offers a high throughput with proven assembly yield and electrical stability. However, further research works are required to enable the bonding by

eliminating the flux residues and enhancing the joint reliability against intermetallic growth and thermo-mechanical stresses.

In Section 2.1, we have discussed that the bumping materials are either Au or solder. The solder bump is formed by stencil printing or electroplating. The stencil bumping is not able to meet the standoff and pad pitch requirement due to the challenges in stencil fabrication, printing processes and solder paste formulation. The flux residues after soldering, further limit its use for optoelectronic, micro-electro-mechanical system, fiber optic components, and microwave semiconductor devices. Bumping by plating technology contaminates the devices with the use of patterned photo resist mask. It also increases the overall packaging cost, as the yield is sensitive to wafer processing. Therefore, the mechanical gold stud bumping is the preferred bumping solution with the joint-in-via architecture. It eases the bumping infrastructure with the use of current wire-bond infrastructure and offers a low cost, fine pitch solution without the need of the UBM layer on the die pad. The mechanical gold stud bumping provides a good standoff for joint reliability. It also eases the joining process as the gold surface does not oxidize easily.

For assessing the micro-via easier, solder is deposited into the joint-in-via architecture for bonding. Solder is chosen as the bonding material because of its widely accepted properties by industry such as good thermal performance, reliable joints and robust assembly processes. Stencil bumping technology is capitalized to deposit solder in the micro-via for bumping. The solder deposition is done using the micro-vias as stencil apertures for bumping as shown in Figure 3.5. This removes the need of stencil for printing. It helps to save the processing time for stencil alignment and remove any solder loss through stencil registration error. More consistent solder volume is deposited as there

is no further loss of solder through the removal of the stencil after printing. The micro-via helps to contain the solder paste and prevents solder slumping, thereby achieving a fine pitch printing capability. The Au and solder combination is known to cause extensive embrittlement, which helps to magnify the joint failure for better characterization. The increase in stand off by the joint-in-via architecture may enhance the joint integrity and reduce the effect of intermetallic and fatigue failure.

Figure 3.5: Solder bumping using the micro-via as stencil apertures

3.3 EXPERIMENTAL PROCEDURES

In enabling the fluxless bonding on the joint-in-via architecture, following areas are assessed:

- Micro-via fabrication technologies on the organic substrates
- Solder bumping in the joint-in-via architecture
- Flip-chip bonding assessment on the joint-in-via architecture

Organic materials for both rigid and flex are assessed in terms of their micro-via fabrication techniques with substrate suppliers' infrastructures. These organic materials include standard epoxy composite FR4 and high T_g multi-function epoxy for rigid substrates (BT), liquid crystalline polymer (LCP) and polyimide materials for flex. The different micro-via fabrication techniques such as mechanical punching, chemical etching and laser ablation were used to fabricate fifty 100 μ m micro-vias at a pitch of 150 μ m on the thinnest available core materials.

As the rigid materials (FR4 and BT) are available with double cladded copper on a 100 μ m core thickness, only laser ablation technique can be assessed through a blind micro-via structure. CO₂ laser was evaluated for laser ablation due to its high throughput with lower infrastructure cost as a comparison to Nd: YAG and the excimer laser. Moreover, the CO₂ laser has the least flexibility in making the via. Once the desired via profile can be achieved, the Nd: YAG and the excimer laser should have no difficulties in generating these joint-in-via architectures. In addition, the Nd: YAG and excimer laser are not evaluated due to the availability of the infrastructure with suppliers' sites. A lithographic patterning process was carried out to form patterned copper foils, which acted as a laser-firing mask for micro-via fabrication. The process flow is illustrated in Figure 3.6. The LCP flex material was assessed next. As the material was available in the double cladded copper, laser ablation was also employed on the 50 μ m LCP.

Figure 3.6: Laser ablation micro-via techniques

Polymide material, being mechanical, chemical and laser processable, is compatible with a wide variety of micro-via formation techniques. All these micro-via techniques were characterized on polymide flex with a core thickness of 50 μ m. Flex with a tape adhesive layer, denoted as Flex A, was used to evaluate the mechanical punch micro-via technique. The vias were mechanically punched using a numerical control system before laminating the copper foil onto the flex for copper patterning. The vias were generated using a 100 μ m diameter punch tool. A 50 μ m chemical etchable polymide core was evaluated

with chemical etching for Flex B. A CO₂ laser ablation was also assessed on the adhesiveless polyimide Flex C using a 12µm clad copper foils.

Water-soluble type 5 solder paste was then manually deposited into the micro-vias with these vias acting as stencil apertures for printing. The solder paste was then reflowed and flux residues cleaned off. Macroscopic analysis was carried out using optical microscope with observations recorded. A simplified process flow is illustrated in Fig 3.7. For pad pitch assessment, the most preferred micro-via fabrication technologies was further assessed to understand its pad pitch capability. All experimental works were done by the author except for the micro-via formations that were carried out by various suppliers.

Figure 3.7: Process flow for micro-via characterization

Next, the automation of the bumping in the joint-in-via architecture was carried out. The printing concept was translated to a self-design, customized make reel-to-reel printing equipment as shown in Figure 3.8. The printing head consisted of two-stage printing as shown in Figure 3.9. The 1st squeegee deposited a continuous layer of solder paste on the surface while the 2nd squeegee followed through to plug the solder paste into the micro-via and scrubbed away excessive solder paste. Water-soluble type 5 solder paste (15-

25 μ m solder particle size) was then deposited into the 100 μ m micro-via followed by reflow and flux cleaning. The bumping process optimization was carried out by performing studies on the different printing angles at 45°, 35° and 15°. Macroscopic analysis was carried out using optical microscope with observations recorded. The filled solder paste was then reflowed to form bump and the undesirable flux residues were cleaned off. A 2-dimensional laser profiler was then used to measure the profile of the solder paste into the joint-in-via architecture and its bump standoff after reflow.

Figure 3.8: Equipment customized to plug the solder paste into micro-via of flex

Figure 3.9: Illustrating the concept of solder bumping in the micro-via through the use of two squeegees. Actual squeegee printing head fabricated on the right

With the conceptualisation of the joint-in-via architecture, flip-chip bonding assessment using conventional soldering, thermocompression and solid-liquid interdiffusion were

studied. These studies were carried out on dies consisting of fifty $110\mu\text{m}$ -diameter micro-vias fabricated at an inter-via pitch of $130\mu\text{m}$. Based on ITRS 2003 roadmap, this die pad pitch has sufficient margin for application up to the year 2006. The micro-via had a base pad width of $90\mu\text{m}$ cover with a soldermask as shown in Figure 3.10. Au studs with $25\mu\text{m}$ diameters were mechanically bumped on a $9\text{mm} \times 10\text{mm} \times 0.25\text{mm}$ metallized die and then inserted into the corresponding micro-via for joint formation. The Au stud bumps had a base of $75\mu\text{m}$ with a mean standoff of $60\mu\text{m}$. A spacer was introduced in-between the die and the substrate to provide a consistent submergence depth for the studies. Figure 3.11 illustrates a schematic view of the joint-in-via architecture for bonding characterisation.

Figure 3.10: Joint-in-via architecture at a pad pitch of $130\mu\text{m}$ with a diameter of $110\mu\text{m}$ and base $90\mu\text{m}$

Figure 3.11: Schematic illustration of an Au stud bonding with the joint-in-via architecture

Conventional soldering with the JIV was characterized as a reference for fluxless soldering. This was carried out by inserting the Au bumps into the solder pastes and then

followed by a reflow process. In fluxless bonding, the solder plugged in the JIV architecture was solidified and evaluated under different conditions. A design-of-experiment matrix consisted of temperatures T_0, T_1, T_2 , and T_3 ($T_0 < T_1 < 183^\circ\text{C} < T_2 < T_3 < 260^\circ\text{C}$ where T_2 and T_3 were above the melting point of solder); pure mechanical insertion forces F_0 and F_1 ($F_0 < F_1 < 10$ Kgf; and times t_1, t_2 ($t_1 < t_2 < 3$ s). The temperature was applied by local contact heating on the substrate and the die. The matrix was used to characterize the bonding conditions ranging from thermocompression to solid-liquid interdiffusion. A set of 20 units was assembled in each leg. Assembly yield, based on the continuity of the 50 joints, was collected as a metric for assessment. The bonded sample was then embedded in epoxy and sectioned for analysis using a diamond cut-off wheel. The cross sections of the joints were prepared for macroscopic and metallographic analysis. Macroscopic analysis was carried out with a high-magnification optical microscope, and morphologies analysis was performed using a scanning electron microscope (SEM) with an energy dispersive x-ray detector (EDX). Figure 3.12 summaries the experiment flow in the conceptualization of the fluxless bonding with the joint-in-via architecture.

Figure 3.12: Experimental flow to conceptualise the bonding the JIV architecture

3.4 MICRO-VIA CHARACTERIZATION

Cracks were observed between adjacent vias for both rigid materials with typical failures shown in Figure 3.13. This is a result of poor laser drill-ability on the rigid materials due to the presence of reinforced glass fibers. This generated a poor via profile as shown in Figure 3.14. The cracks were frequently found between the via spacing, which resulted in solder bridging after the printing. Rigid materials with laser ablation are not suitable for the joint-in-via concept.

Figure 3.13: Solder bridging due to via cracking on FR4 materials

Figure 3.14: Poor laser profile on FR4 materials

Similarly cracks were observed on the LCP as shown in Figure 3.15. Poor wet-ability of solder was also observed in the micro-via. This is likely due to the LCP residues re-depositing themselves after laser firing. The poor adhesion of copper for LCP also leads

to peeling off the overhanging copper traces as shown in Figure 3.16. The joint-in-via architecture requires the core material to have good adhesion with copper for subsequent copper metallization processes.

Figure 3.15: Cracks between adjacent via and residue seen in micro-via

Figure 3.16: Overhanging copper trace peeling off from LCP after processing

100 μ m diameter punch tool was the smallest available in the industry. The punched micro-via on Flex A has well defined vertical walls. During fabrication, high breakage of the punching tool was recorded, suggesting a vulnerable punch tool. As the numerical punching system has a positional tolerance of $\pm 75\mu$ m, this technique limits the joint-in-via pitch at 175 μ m for a micro-via size of 100 μ m as shown in Figure 3.17.

Figure 3.17: Micro-via mechanical punch at 175 μ m pitch with a via size of 100 μ m

Chemical etched micro-via technique was assessed on the adhesiveless polyimide Flex B. The isotropic chemical etching will result in gentle via wall profile of about $60^\circ \pm 15^\circ$ as shown in Figure 3.18. It required a large inter-via spacing of $50\mu\text{m}$ undercut on the copper mask. Thus, for a via size of $100\mu\text{m}$, a $230\mu\text{m}$ pad pitch was achievable with a $30\mu\text{m}$ inter-via spacing. It had a poorer micro-via pad pitch capability than current copper metallization technologies. The inconsistency in via size by chemical etching also generated design and assembly difficulties. As such, the chemical etching technique was not pursued.

Figure 3.18: Schematic illustration of micro-via isotropic etching

A typical laser firing for micro-via is shown in Figure 3.19. A taper profile with 2 laser shots was taken as the micro-via process baseline due to its high productivity yield. The slope of the via was well controlled as there was no glass woven fibre cloth to complicate the heat ablation during laser firing. This technique allows a $20\mu\text{m}$ inter-via spacing without any cracks between the micro-vias.

The copper metallization was then carried out to suspend the copper trace over the via with solder paste deposited into the micro-via. The final structure is shown in Figure 3.20 for a pad pitch of $150\mu\text{m}$ with a micro-via size of $100\mu\text{m}$. Laser ablation on polyimide flex was found to ease manufacturability and was chosen as a suitable candidate to assess its pad pitch capability. The joint-in-via architecture was successfully conceptualised on the polyimide flex substrate using a CO_2 laser ablation micro-via technique.

Figure 3.19: Laser firing (a) 1 shot (b) 2 shots and (c) 3 shots to generate the blind micro-via structure using patterned copper mask with 20μm inter-via spacing

Figure 3.20: Optical and SEM picture showing a pad pitch of 150μm with a micro-via size of 100μm

3.5 PAD PITCH ASSESSEMENT

The pad pitch for the joint-in-via architecture was determined by the via size and inter-via spacing capability. The copper mask for laser firing was generated using existing copper metallization techniques. In order to obtain fine features with narrow spacing, the copper was thinned down to a few microns, thereby reducing the isotropic etching effect. This thin copper layer serves as a laser-firing mask for fine pitch via fabrication. Alternative, the quartz mask on a projection laser can be used to generate micro-vias with high throughput for production. By using subtractive etching on thin copper foil, a minimum

inter-via spacing of $20\mu\text{m}$ can be achieved. The laser micro-via process allows a narrow via spacing and further pitch reduction as illustrated in Figure 3.21. The micro-via architecture removes the trapezoidal metallization constraints and further eases the copper metallization by the tapered nature of the laser-fired micro-via.

Figure 3.21: Schematic illustration of joint-in-via architecture, which has a finer pad pitch as compared to existing pad designs

The joint-in-via architecture offers a finer pitch as compared to existing pad architecture. Due to the limitation of CO_2 laser beam size, a minimum micro-via diameter of $50\mu\text{m}$ was fabricated with an inter-via spacing of $20\mu\text{m}$ as shown in Figure 3.22. This joint-in-via architecture migrates the bond pad pitch design rule from copper metallization and soldermask registration to laser-firing micro-via capability. The laser-fired joint-in-via architecture offers a better finer pad pitch capability than advanced semi-additive metallization processes as shown in Figure 3.23. The joint-in-via pad pitch capability is far smaller than any current copper metallization process. It helps to eliminate the RDL processes for pad pitch larger than $70\mu\text{m}$. Thus, it reduces the overall packaging cost of flip-chip packaging.

Figure 3.22: SEM and cross-section picture of a micro-via structure for a joint-in-via architecture with 70µm pad pitch with 20µm inter-via spacing

Figure 3.23: Joint-in-via architecture offers a better pad pitch design rule as compared to advanced copper metallization techniques

3.6 SOLDER BUMPING IN MICRO-VIA

The printing optimization was carried out and it was found that the squeegee printing angle was critical to ensure complete filling of the micro-via. Different squeegee angles were evaluated and a 15° squeeze angle was found best in depositing consistent volume of solder paste into the micro-via as shown in Figure 3.24. A lower face angle helped to

generate a larger vertical deposition force on the solder paste assisting more solder particles to plug into the micro-via.

Figure 3.24: Quality of solder paste in micro-via for 45°, 30° and 15° squeegee angle

It was found that the solder paste was not flushed with the flex surface but with a gently gradient of 13° from the flex surface as shown in Figure 3.25. This was estimated to be 75% of the micro-via volume. Based on a 60% shrinkage after solder reflow, a solder volume height of 44μm was achieved. This tallies with the actual measurement of 42.3μm for reflowed bump as shown in Fig 3.25.

Coplanarity of the micro-via was quantified by the 2D laser profiler and found to have a mean standoff of 41.63μm with a standard deviation of 1.92μm. A good bump coplanarity of about 4μm or +/-5% of the bump height was achieved. This minimum stud bump height of 60μm allows a physical overlap of 25μm if the underfill gap is kept at 25μm. This was to ensure good physical connectivity between the stud and the solder.

Figure 3.25: Solder paste deposited with a gentle slope of 13° in micro-via with a standoff height of 42.3μm after reflow

The joint-in-via architecture was successfully conceptualised with a minimum pad pitch of 70 μm . In summary, the solder bumping using the micro-via as stencil apertures was demonstrated to achieve a good bump coplanarity of $\pm 4\text{ }\mu\text{m}$ using a customized reel-to-reel equipment.

3.7 BONDING ASSESSMENT

3.7.1 Conventional Soldering

An assembly yield of 80 percent was achieved for conventional soldering. The cross section analysis is shown in Figure 3.26. For well-aligned joints, the solder wicked up and engulfed the Au stud, forming a fusion joint as shown in Figure 3.26(i). This good wetting behaviour was assisted by the flux from the solder paste. Physical discontinuity was observed in Figure 3.26(iii) for some joints where offset was observed between the Au stud and the micro-via. This offset was a result of bump registration tolerance, via tolerances and placement tolerance. The offset between a series of bumps cannot be avoided in production as the tolerances cumulatively added up. As such, the solder engulfed the Au stud and via pad because their surface energies were minimised during solidification, thus forming two separate hemispheres.

Figure 3.26: Cross section of the solder joint formed by conventional soldering of Au with eutectic solder in the JIV architecture

Further evidence included a “necking” phenomenon, as shown in Figure 3.26(ii), where the Au stud and the micro-via had a smaller offset. The conventional soldering technique was sensitive to tolerances and placement offset with the use of joint-in-via architecture. Thus, the wetting behavior was undesirable for joints with the via architecture. The solder paste was cumbersome for assembly as it increased difficulties in handling and storage during processing.

3.7.2 Solid State Bonding

In all the solid-state bonding, thermocompression, ($T < T_1$), a poor assembly yield ranging from 0 to 60% was recorded. A typical failure mode was seen with the die tilted with respect to the flex interposer. A physical discontinuity was observed at the die edge due to the Au stud, which sat loosely on a deformed solder bump, as shown in Figure 3.27. This was a result of solder softening with respect to the Au stud under bonding conditions.

Figure 3.27: Physical discontinuity between Au stud and solder for bonding condition F_1, T_1, t_1

A microstructure analysis revealed that interdiffusion occurred between Au and Sn during thermocompression. As shown in Figure 3.28 for bonding condition F_0, T_0, t_1 , multiple microscopic welding joints existed between the Au stud and the solder interfaces. These micro-weld sites are formed as the undulating contact surfaces mate together in the presence of Sn. As a result of small contact areas, extremely high pressure was generated. This interfacial shear produced deformation and plastic flow which resulting in

microscopic slip planes shearing over one another. As the slip planes slid over one another, it removed the undesired tin oxide on the solder surface. These clean metallurgical surfaces at these contact zones were high energetic and promoted the interdiffusion of Au and Sn. The applied temperature energized the Au and Sn atoms and thus helped to promote the interdiffusion between them.

Figure 3.28: Micro-weld joints observed in bonding condition F_0, T_0, t_1

Several dark shaded spots were observed in these minute welded joints and they were identified by EDX that $AuSn_4$ intermetallic regions were on the Au stud interface (point A). These intermetallic regions with Au less than 10 atomic percent were identified by EDX in the corresponding Sn matrix (point B). The low content of Au may be due to the availability of Sn at local sites for interdiffusion. The formation of thermocompression joint for Au with eutectic solder was likely due to the interdiffusion between Au and Sn. As these bonds were made of multiple micro-welds instead of a continuous bond, they were weak and broke easily by thermal mismatch during cooling. Thus, this resulted in the discontinuity of joints around the die edges.

Increase in bond force did not extensively improve the joint as it deformed the solder more significantly. Similar extent of micro weld joints were seen for condition F_1, T_0, t_1 .

Furthermore, the increase in bond time promoted thermal diffusion with more intermetallic seen but this did not significantly improve the joint reliability as shown in Figure 3.29 for condition F_2, T_0, t_2 .

Figure 3.29: Joint in via formation by the thermo-compression bond in condition F_2, T_0, t_2

At the condition of F_0, T_2, t_1 (Figure 3.30), it was observed that the increase in bond temperature increased the AuSn intermetallic formation as per Arrhenius relation. The increase in temperature lowered the activation energy and increased the diffusivity constant to promote interdiffusion. But this did not improve the joint to withstand the material mismatch during cooling.

Figure 3.30: Joint in via formation by the thermo-compression bond in condition F_0, T_2, t_1

Even with bonding condition F_1 , T_1 , t_1 , as shown in Figure 3.31, a combination of time, temperature, and force did not seem to improve the joint performance significantly against the thermal mismatch force during cooling.

Figure 3.31: Joint-in-via formation by the thermo-compression bond at bonding condition F_1, T_1, t_1

Similar observations were seen for all bonding conditions with different extent of AuSn intermetallics. During cooling, the flex substrates contract significantly, resulting in the discontinuity of the joints around the die edges. This evaluation demonstrates that thermocompression bonding allows joint formation but the micro-bonds are weak and unreliable. Thermocompression bonding is not suitable with solidified solder on the joint-in-via architecture. Nevertheless, an important experience has been acquired in this study that the solder in the joint-in-via architecture assists in resolving coplanarity in gang bonding which hinders the TAB bonding process in the 1980's.

3.7.3 Solid-Liquid Bonding

With the bonding temperature above the melting point of the molten solder, solid-liquid bonding occurred. A significant increase in assembly yield was observed in solid-liquid bonding as compared to solid-state bonding. From the leverage plot in Figure 3.32, there was no significant response with temperature and bond time. The macroscopic analysis on

the failure units for bond force F_0 at temperature T_2 and T_3 revealed a partial interconnection between the 50 joints. An almost 100 percent yield was observed with a larger bond force of F_1 for a temperature of T_2 or T_3 . The bonding temperature was around the lead free temperature of 260°C and thus no degradation in device performance. The macroscopic analysis revealed that the solder did not wick up the Au stud. The contact angle between the meniscus of the Au and solder was more than 90°. This observation suggests poor wetting between Au and the solder but further tests would be necessary to understand the bonding mechanism.

Figure 3.32: Level plot of the assembly yield with respect to bond temperature, force, and time for solid-liquid bonding

Figure 3.33 shows the back-scattering image of the intermetallic bond formed under solid-liquid interdiffusion. It was observed that a layer of AuSn_4 was formed along the bond interface with multiple rod-like AuSn_4 fragments spalling off from the interface into the bulk solder. The observations suggested that the mechanical force broke through the oxide layer and promoted a rapid solid-liquid interdiffusion between the Au and fresh molten solder, forming an almost instantaneous bond. The fast intermetallic growth was due to the high solubility of Au in molten solder and precipitation upon cooling [88]. During cooling, the saturated solution precipitated needle-like AuSn_4 fragments, which eventually spalled off into the solder due to stresses [83].

In the back scattering images, the increase in bond time had resulted in an increase in Au-Sn phases with no physical differences in the joint architecture. This was a result of the increase of Au content in molten solder with prolonged bonding time. The extensive intermetallic phases were expected to affect the joint reliability [74, 97]. An increase in standoff was observed with higher bonding temperature that may require further study. This instantaneous, fluxless bonding mechanism is based on applying a mechanical force to break the tin oxide layer over molten solder to activate a solid-liquid interdiffusion between Au and fresh molten solder. Thus, this bonding technique has been termed solid liquid interdiffusion bonding by compressive force (SLICF).

Figure 3.33: Phase morphology analysis of Au and eutectic solder after solid-liquid interdiffusion

3.8 SUMMARY ON JIV

Different micro-via technologies on organic substrates were assessed and it was found that the material is susceptible to the micro-via processing technique. Mechanical punching and chemical etching are not able to achieve a fine pad pitch capability due to the limitations in tooling and isotropic etching respectively. Laser ablation on polyimide flex has been identified as the preferred technology in the fabrication of the joint-in-via architecture. This joint-in-via architecture migrates the bond pad pitch design rule from the copper metallization and soldermask registration to the laser-firing micro-via

capability. This eases the copper metallization process and enhances the robustness of the substrate for reliability. The JIV architecture achieves a 70 μ m pad pitch with a 20 μ m inter-via spacing. It offers a better pitch capability than any advanced copper metallization processes. The innovative solder bumping approach of using the micro-vias as stencil apertures enable a 70 μ m pitch bumping. The bumping technique also achieves a good bump coplanarity of ± 4 μ m through a customized reel-to-reel equipment.

The conceptualization of the JIV architecture enables the assessment of different flip chip bonding. The conventional soldering is not compatible with the joint-in-via architecture due to its wetting properties. In solid-state thermocompression bonding, the Au diffuses to eutectic solder to form multiple micro-weld joints that break during cooling. An instantaneous fluxless bonding on the JIV is achieved using solid-liquid bonding. The bonding is visualized as utilizing a mechanical bonding force to break the tin oxide layer over molten solder for Au to interact with fresh molten solder for joint formation. This bonding is termed solid liquid interdiffusion bonding by compressive force (SLICF). The bond is weak but sufficient to survive the thermal mismatch stresses in assembly. This bonding technique is sensitive to bonding force rather than temperature and time. These peculiar bonding behaviors encourage further studies on this unique bonding mechanism.

CHAPTER 4

SOLID-LIQUID INTERDIFFUSION BONDING BY COMPRESSIVE FORCE

The SLICF bonding is constructed by force inserting the Au studs into corresponding molten solder baths with the use of the micro-vias in an ambient environment. The molten solder baths are achieved through contact heating of the solder above the melting point of solder. Once the Au studs are forced submerged into molten solder, the assembly is released and left to cool. A good preliminary assembly yield depends on its bonding force rather than the temperature and bonding time, which called for further study into this bonding mechanism.

4.1 PROPOSED HYPOTHESIS

This ambient, fluxless bonding technique is hypothesized to work on the principle of using a mechanical force to break the tin oxide layer over the molten solder, enabling a solid liquid interdiffusion bonding as shown in Figure 4.1. A mechanical insertion force is applied on the soldering body to help overcome the surface tension of the molten solder and the strength of the oxide layer (stage I). With sufficient force applied (stage II), the soldering body breaks the oxide layer and contacts with fresh molten solder. Thereafter, a rapid solid-liquid interdiffusion occurs between the submerged body and the fresh molten solder. The submerged body is protected from oxidation during bonding. The forced submerged body sinks into the solder until a position of equilibrium is reached. At stage III, the mechanical insertion force is released, and the assembly cools down by natural convection. The submerged body then experiences an upward, thrusting force due to buoyancy. The body ascends while the saturated solder solution solidifies, precipitating

thermodynamically stable phases. An intermetallic bond is formed between the submerged body and the solder. This bond acts as a mechanical interlock to prevent the soldering body from floating out of the molten solder.

Figure 4.1: Principle of solid liquid interdiffusion bonding by compressive force

4.2 EXPERIMENT PROCEDURES

In this bonding study, Au was chosen as the soldering body due to its rapid dissolution rate and its inertness to oxidation. Wetting balance tests were performed to characterize its behavior with solder, as it is a common standard for solderability. This test has a similar insertion motion as the proposed SLICF bonding and, therefore, enables the quantification of the insertion force necessary for bonding. A series of fifty gold studs with a tip diameter of 25 μm were mechanically bumped on aluminium metallized dies using a thermosonic wire bonder. A corresponding fifty 110 μm -diameter micro-vias fabricated at an inter-via pitch of 130 μm were applied for fluxless bonding characterization. The Au-bumped die was then bonded using a conventional lead-on-chip bonder with an upward mounting motion. A spacer with a thickness of x_{10} was introduced between the die and the substrate to provide a constant submerging depth for this study as shown in Figure 4.2. A set of different bonding forces, F_{10} , F_{11} , F_{12} , and F_{13} ($F_{10} < F_{11} < F_{12} < F_{13}$), were applied at temperature T_{11} (above the melting point of eutectic solder)

and bond time t_{11} . The temperature was applied to the assembly by local contact heating of the die and the flex assembly.

Figure 4.2: Schematic illustration of the bonding setup for SLICF bonding studies.

A set of 20 units was assembled in each leg. Assembly yields based on resistance continuity were used as a yardstick for assessment. This evaluation matrix was designed to determine whether a threshold force was necessary to break the oxide layer and overcome the surface tension for bonding. Macroscopic examination was performed on the cross-section of the assembled unit for further analysis of the contact angle and the standoff. Microstructure analyses were also carried out using SEM and EDX to identify the thermodynamic phases. The instantaneous SLICF bonding was studied with varying bond times from t_{10} to t_{13} , where t_{13} was well before the wetting time. Both the impact of the soldering time with the joint architecture and its microstructures were uncovered. The buoyancy effect in stage III was studied with varying bonding temperatures from T_{11} to T_{15} at a fixed submerging depth x_{10} with the use of a spacer. This experiment aims to verify the hypothesis that the body experiences “rejection” while the saturated solder solidifies. Figure 4.3 summarizes the experimental flow.

Figure 4.3: Experimental flow conducted to investigate the fluxless soldering mechanism

4.3 BONDING PHENOMENON

The wetting balance test results are plotted in Figure 4.4. The curves representing samples without flux initially registered a large negative counter-balance force; then they increased gradually and eventually ended up in the negative-force region. The curves representing samples with flux registered a higher counter-balanced force and then passed through the zero-force line. The presence of the thin oxide layer with flux registered a similar initial counter-balance force, while a large negative buoyancy force was recorded without flux. The initial counter-balance force was a result of the surface tension and oxide layer attempting to “reject” the submerging body. Once this was overcome, a reaction between the Au and solder took place and wetting initiated. This wetting force decreased the counter-balance force, but it was not sufficient to overcome the buoyancy force due to the displacement of the solder. Hence, a negative counter-balance force was registered, depicting a poor wetting of Au with molten solder. In the presence of flux, the oxides on the solder were removed where it reduced the initial counter-balance force. As wetting was initiated, the wetting force dominated and generated a positive resultant force over the zero line.

Figure 4.4: Force vs. time data from wetting balance tests

Figure 4.5 plots the assembly yield at temperature T_{11} at different bond forces. The bonding yield increased with respect to the bond force applied. A 100 percent yield was observed for a bond force larger than F_{12} . The cross-section in Figure 4.6 reveals a partial interconnects between the joints. The left joint revealed a physical discontinuity between the Au and solder with some presence of solder remaining on the tip of the Au stud. The right joint had a good contact between the Au and solder, but a relatively high standoff compared to the thickness of the spacer.

Figure 4.5: Assembly yield collected with different bond force depicting a threshold force required for a good joint

Figure 4.6: Partial joint connection for a lower bond force of F_0

The macroscopic analysis of a typically good SLICF joint is seen in Figure 4.7 in comparison with a conventional soldering joint in Figure 4.8. The SLICF joint did not have solder wicking up the Au stud and had a contact angle larger than 90° between the meniscus of the Au and solder, depicting poor solderability per the wetting balance test. The joint architecture differed from conventional soldering, which the solidified solder fully engulfed the Au stud with a good contact angle.

Figure 4.7: SLICF bonding joint at F_1, T_2, t_1

Figure 4.8: Conventional solder joint using solder paste with 220°C reflow

Figure 4.9 shows the intermetallic regions formed under the instantaneous SLICF bonding. It was observed that a layer of AuSn_2 and a layer of AuSn_4 were formed along the bond interface, and the bulk solder contained multiple occurrences of rod-like AuSn_4 . These intermetallic regions appeared to be radiating from the interdiffusion interface between the Au and solder. The microstructure analyses on the SLICF joint showed no sign of tin oxides between the Au and solders interface.

Figure 4.9: Microstructure of AuSn phases after SLICF bonding

As the bond force F_{12} offered a good assembly yield, it was used to study the joint architecture with time and temperature. Figure 4.10 shows the SEM pictures for the different bond time of t_{10} and t_{13} for bond force F_{12} . A 99 percent yield was achieved for t_{10} in a split second, well below the wetting time of a conventional soldering. The macroscopic examination showed similar standoff, while the SEM showed significant increase in the AuSn phases precipitated.

Figure 4.10: Effect of longer bonding time on microstructure of AuSn phase after SLICF bonding at temperature T_{12}

Figure 4.11 shows the assembly yields with different joint standoffs as a result of different bonding temperatures. All the samples had a standoff greater than the spacer thickness. An increasing standoff trend was seen with higher bonding temperature, and this affected the assembly yield accordingly. With a high bonding temperature of T_5 and above, a “bottleneck” joint architecture was noted as shown in Figure 4.12. It appeared that the joint attempted to withdraw from the molten surface while the surface tension of the solder restrained its motion.

Figure 4.11: Standoff and assembly yield of SLICF bonding for different temperatures

($T_{17} > T_{16} > T_{15} > T_{14} > T_{13} > T_{12} > T_{11}$) with bond force F_{12}

Figure 4.12: Cross-section revealing increase with standoff for higher bonding

temperature for bond force F_{12}

4.4 BONDING MECHANISM

4.4.1 Stage I: The Insertion Mechanism

The series of wetting balance tests suggest the need for a threshold force to overcome the surface tension and the oxide layer before the soldering body submerges into molten solder to initiate a wetting mechanism. With respect to the assembly, the 1-dimensional force analysis, prior to the insertion of the soldered body into the molten PbSn solder is shown in Figure 4.13, where F_R is the insertion force, $P\gamma_{lg}\cos\alpha_l$ is the surface tension of the molten solder, and W is the weight of the soldering body. In $P\gamma_{lg}\cos\alpha_l$, P is the circumference of the stud tip, γ_{lg} is the surface tension of the eutectic PbSn solder with air and the α the tangential angle of the solder meniscus with the vertical [133-134]. The surface tension inclusive of the strength of the oxide layer and the weight of the soldering body combine to act against the insertion force F_R . Ignoring the strength of the thin oxide layer, an equilibrium force balance is achieved for s studs (Eq. (4.1)) with an increase in the surface tension force as α_l decreases.

Figure 4.13: Mechanical forces acting on the soldered body prior to submerging into solder

$$F_R - sP\gamma_{lg}\cos\alpha_l - W = 0 \quad \text{----- (4.1)}$$

The surface tension of the solder is analogous to a frictional force restricting the soldering body from submerging into the molten solder. As a larger force is applied, α decreases until the surface tension is overcome. As shown in the wetting balance test for oxide without flux, a larger negative counter-balance force was registered as compared to the curve without oxide and flux. This implies that the presence of the oxide layer may have increased the surface tension with an additional term γ_o against the insertion force. Therefore, a larger insertion force F_T (threshold force) was required to overcome the self-weight and the surface tension of the solder. The F_T is the threshold force to break the oxide layer before the soldering body is submerged. Thus, the balanced force is denoted by Eq. (4.2), where α_m denotes the tangential angle of the oxidized solder surface before the oxide layer breaks. For simplification, γ is termed the sum of the surface tension of solder with air (γ_{lg}) and the oxide layer (γ_o). (i.e., $\gamma = \gamma_{lg} + \gamma_o$ in Eq. (4.3))

$$F_T - sP(\gamma_{lg} + \gamma_o)\cos\alpha_m - W = 0 \quad \text{----- (4.2)}$$

$$F_T - sP\gamma\cos\alpha_m - W = 0 \quad \text{----- (4.3)}$$

As such, when the insertion force F_b greater than the threshold force was applied (i.e. $F_b > F_T$ where F_b denotes the insertion force greater than F_T), the surface tension and the self-weight of the insertion body are overcome. The soldered body breaks the oxide layers and submerges into the molten solder. From that moment, the interdiffusion of Au and solder begins and the solid liquid bonding starts. The assembly yields shown in Figure 4.5 provides strong evidence for the necessary condition of SLICF fluxless bonding. The cross-section in Figure 4.6 further supports the hypothesis. Partial joint formation was seen when a lower bond-force F_{10} or F_{11} was applied for a series of joints. When the Au studs and the molten solder were placed together, a moderate force was sufficient to break the solder oxide due to the high pressure generated by the small contact area. Since the fifty Au studs have a standoff distribution on the die, the tallest Au stud will be the first stud to be in contact with molten solder and forced submerges into solder. This is then followed by the next tallest stud bump. This will continue until an equilibrium condition is reached for s' studs. The equilibrium condition for b studs can be expressed as $\sum_1^{s'} P\gamma \cos \alpha + W + F_T = 0$. As the equilibrium condition is reached, the $(s' + 1)$ stud has insufficient force to overcome the surface tension and break the oxide layer. Hence, partial joints are seen with a low bond force.

4.4.2 Stage II: Submerging into Solder

Once the soldering body submerges into fresh molten PbSn solder, a rapid solid-liquid interdiffusion occurs between the Au and the solder. The microstructure analyses by SEM and EDX showed no signs of tin oxides between the Au and solder interface. As the oxide layer breaks, rapid solid-liquid interdiffusion between the Au and fresh molten solder takes place to form a joint. The Au-Sn phases appears to radiate from the interface. The Au diffuses rapidly into the molten PbSn solder. During cooling, the saturated molten solder precipitates to form the rod-like AuSn_4 phases. The precipitation of AuSn_4 leads to

the depletion of Sn in the surrounding matrix, resulting in the formation of Pb-rich islands, as shown in Figure 4.9.

As the soldering body submerges into the solder, the buoyancy and the wetting forces kicked in, as shown in Eq. (4.4). The buoyancy and wetting forces can be visualized from the gradual increase in the counter-forces during the wetting balance test. The soldering body sinks into the molten solder until the spacer thickness.

$$F_b - \rho g A x_o + s P \gamma_{ls} \cos \theta - W > 0 \quad \text{----- (4.4)}$$

The wetting force is represented by $s P \gamma_{ls} \cos \theta$ where γ_{ls} is the surface tension of the solder with an Au surface, and θ is the contact angle between the Au surface and the solder. In this equation, a $\rho g A x_o$ term is introduced as the buoyancy as a result of the solder volume displacement [133-134]. According to Archimedes' principle, the buoyancy is expressed as the product of the density of solder (ρ), the mass of acceleration (g), the cross-section of the submerged body (A), and the equilibrium submersion depth into the solder (x_o). As a sufficient insertion force F_b is applied, the soldering body will achieve a physical equilibrium position with the use of the spacer.

An instantaneous SLICF bonding is demonstrated in Figure 4.10 with a bond time of t_{10} , which is well below the wetting time of solder. The cross-section of the joints revealed poor solderability of Au with solder and, hence no self-alignment forces for bonding as demonstrated by the wetting tests. The increase in the bond time does not physically affect the joint architecture but merely increased the amount of Au dissolving into molten solder, forming more AuSn phases as per the solid liquid interdiffusion. The bonding time does not affect the joint architecture but promotes the extensive formation of intermetallic compounds.

4.4.3 Stage III: Solidification of Solder

As the bond-force is released in stage III (in the non-wetting state of solder), the soldering body will experience “rejection forces” generated by the buoyancy and the weight of the soldering body. This phenomenon is seen in Figure 4.11 where all the joint standoffs are larger than the spacer assembly. The resultant forces on the submerged soldering body are illustrated in Figure 4.14 as the insertion force is released. By equating the vertical force component of a single stud, the resultant force F_w at any depth in solder can be estimated by Eq. (4.5), where x is the ascending displacement from its equilibrium position x_0 .

$$F_w = \rho g A(x_0 - x) + W - P\gamma_l \cos\theta \quad \text{----- (4.5)}$$

Figure 4.14: Forces acting on a submerged body

Equation 4.5 can be expressed as a second-order linear differential equation as in Equation 4.6, where it depicts the motion of the soldering body as bond forces are released from the submerged body. This is analogous to an external, excited, undamped mass-spring system of stiffness $\rho g A$ by a force of $\rho g A x_0 - P\gamma_l \cos\theta - W$ [135].

$$\frac{d^2 x}{dt^2} + \frac{\rho g A}{m} x = \frac{\rho g A x_0 - P\gamma_l \cos\theta + W}{m} \quad \text{----- (4.6)}$$

Assuming θ as constant, a general solution for Eq. (4.6) gives rise to Eq (4.7) where

$K_1 = \frac{\rho g A}{m}$ is the stiffness of the system contributed by the buoyancy force and

$K_2 = \frac{\rho g A x_0 - P \gamma_i \cos \theta + W}{m}$ is the initial acceleration given to the submerged body. The constants C_1 and C_2 can be determined by the boundary conditions at the equilibrium position where $t = 0$, $x = 0$, and $dx/dt = 0$. The solution for the motion of the submerged body is shown in Eq. (4.8).

$$x = C_1 \cos \sqrt{K_1} t + C_2 \sin \sqrt{K_1} t + \frac{K_2}{K_1} \quad \text{----- (4.7)}$$

$$x = \frac{K_2}{K_1} (1 - \cos \sqrt{K_1} t) \quad \text{----- (4.8)}$$

To estimate the standoff, instantaneous freezing by solder solidification is assumed. The time taken for solder solidification, t_s , can be estimated by Eq. (4.9) using the lumped capacitance model [136] where T_i is the bonding temperature, T_s the solidified temperature, and T_∞ the ambient temperature. The time to reach solidification is based on the assumption of spatial uniformity in all instances during the transient process.

$$t_s = \frac{mc}{hA_s} \ln \left(\frac{T_i - T_\infty}{T_s - T_\infty} \right) \quad \text{----- (4.9)}$$

In the above equation, m denotes mass, c denotes heat capacity, h denotes convection heat transfer coefficient, and A_s denotes the surface area for convection cooling of the submerged body. Substituting Eq. (4.9) into Eq. (4.8) gives rise to Eq. (4.10), which is the estimation of the ascending displacement of the forced submerged body. Hence, an increase in standoff is seen in the SLICF bonding for a particular temperature. The increase in standoff estimated by Eq. (4.10) matches the increase experimentally obtained in Figure 4.11.

$$x = \frac{K_2}{K_1} [1 - \cos \sqrt{K_1} t_s] \quad \text{----- (4.10)}$$

The drop in assembly yield is due to an increase in standoff. For bonding, the body needs to be physically in contact with the solder. Hence, the allowable displacement must be

smaller than the equilibrium position x_o ($x_o > x$) (i.e. $x_o \geq \frac{K_2}{K_1} [1 - \cos \sqrt{K_1} t_s]$). By simplifying the relationship, the following equation was obtained: Eq. (5.11) where $K_3 = \frac{nP\gamma_l \cos \theta - W}{\rho g A}$

$$x_o \geq K_3 \left[\frac{\cos \sqrt{K_1} t_s - 1}{\cos \sqrt{K_1} t_s} \right] \quad \text{----- (4.11)}$$

As such, a minimum submerged distance would be necessary for a specific bonding temperature for the soldering body to be submerged in solder. Therefore, the assembly yield decreases with an increase in bonding temperature for a specific submerged depth. This is a result of longer cooling time t_s where the buoyancy and its weight component are attempting to reject the soldering body as per Eq. (4.11). This is more apparent with high bonding temperature of T_{15} where a “bottleneck” joint architecture is seen. Thus, the bonding temperature and the submerged distance are inter-related parameters in SLICF bonding and, therefore, these parameters have to be optimized to achieve a successful SLICF joint.

4.5 SUMMARY ON SLICF BONDING

The SLICF bonding technique uses a mechanical force to break the oxide layer and overcomes the surface tension and weight of the insertion body. Once inserted, the submerged body interacts with fresh molten solder to form bonds via solid-liquid interdiffusion. The bonds are mechanically interlocked upon cooling. This fluxless bonding technique does not rely on the wetting behavior, thus allows instantaneous soldering, and thereby eliminates the need for fluxing and the reflow process. Due to poor wetting, the buoyancy of the molten solder and the weight of the insertion body tend to “reject” the insertion; therefore, a sufficiently deep submerging is necessary to achieve good joints at any particular temperature.

CHAPTER 5

KINETICS OF Au WITH MOLTEN Sn BASED SOLDERS

The Au and solder interconnect enables a fluxless interconnect system known as SLICF bonding. This bonding works on the principle of solid-liquid interdiffusion of Au with fresh molten solder for bonding. As Au comes into contact with molten Sn based solder, both dissolution and reaction occur at the interface resulting in the formation of thermodynamically stable intermetallic compounds. However, being a tin-based solder, poor reliability with Au may result in failure due to the rapid kinetics in the formation of extensive brittle intermetallic compounds (IMCs). Thus, the formation of this IMC gives rise to a decrease in both peel strength and shear strength, dampening the prospect of Au and solder in the flip-chip solution. In addition, the SLICF bonding has significantly more Au-Sn intermetallic with increase in bond time. Thus, it emphasizes the importance of the kinetic studies. The kinetics of Au and its interface morphologies with eutectic PbSn and SnAgCu solder are examined and summarized in this chapter to leverage on their findings to enhance the reliability of the fluxless SLICF bonding on the joint-in-via architecture.

5.1 PROPOSED KINETICS OF SOLID LIQUID INTERDIFFUSION

The instantaneous SLICF bonding depends on the kinetics of solid-liquid interdiffusion at isothermal condition between Au and molten Sn based solder. When Au comes into contact with molten solder, both dissolution and reaction compete against each other at the solid-liquid interface. The dissolved Au at the interface reaches its solubility and initiates the growth of intermetallic compounds. The intermetallic compounds nucleate and grow by interfacial reaction at the boundary layer while the Au dissolves easily from the boundary layer to the rest of the solder to avoid saturation. The IMC layer acts as a diffusion barrier layer and retards the rate of Au dissolving into solder. Even with the

diffusion barrier, the Au continues to dissolve into molten solder through the diffusion barrier. This can be done through dissolving Au directly into molten solder or spalling off from the interface into molten solder. During cooling, the dissolved Au then precipitates as thermodynamic phases.

At the solid-liquid interface, Kidson's [76] et al. equations are proposed to describe the kinetics of the solid liquid interdiffusion. These equations are derived through the application of the Fick's First Law to polyphase diffusion in the binary systems. It leads to a simple physical interpretation of various possible types of behavior in the growth of the diffusion layer. As the solid metal (Metal 1) comes into contact with another molten metal (Metal 2), the initial interaction can be described as the interdiffusion between partially miscible metals. The shift of the interface $\xi_{Au,Sn}$ with respect to the mass invariant Matano interface is expressed in Eq. (5.1)

$$\xi_{M1,M2} = 2 \left[\left(\frac{(DK)_{M2,M1} - (DK)_{M1,M2}}{C_{M1,M2} - C_{M2,M1}} \right) \right] \sqrt{t} \quad \text{----- (5.1)}$$

where D_{ij} is the interdiffusion coefficient at interface of i and j, $K_{ij} = \sqrt{t} \left(\frac{dC}{dx} \right)_{ij}$, $\xi_{i,j}$ is the displacement from the Matano interface between i and j interface, $C_{i,j}$ denotes the maximum solubility of j in i and vice versa.

For solid liquid interdiffusion, the diffusion in molten metal is about four orders of magnitude faster than solid diffusion [90]. Thus, Eq. (5.1) can be simplified to Eq. (5.2) as $(DK)_{M2,M1} - (DK)_{M1,M2} \approx -(DK)_{M1,M2}$.

$$\xi_{Au,Sn} = 2 \left[\left(\frac{-(DK)_{M1,M2}}{C_{M1,M2} - C_{M2,M1}} \right) \right] \sqrt{t} \quad \text{----- (5.2)}$$

This suggests that the rate consumption of Metal 1 is proportional to the square root of the bonding time with the bond surface moving toward Metal 1. The dissolved Metal 1 forms the saturated solution at the interface, which reacts to form intermetallic phases at the interface to lower the system energy. These thermodynamic phases nucleate heterogeneously and eventually grow into a diffusion barrier layer while the dissolved metal diffuses easily from the boundary layer to the rest of the molten solder to avoid super saturation. Once the diffusion layer is erected, it retards the rate of metal dissolving into molten metal 2 as the kinetics change from a solid-liquid interdiffusion to a solid-solid-liquid interdiffusion. The diffusion barrier produces discontinuities in the concentration-versus-depth curves as shown in Figure 5.1. The shift of its intermetallic interface and growth of the layer can be described by Eq. (5.3) to Eq. (5.5) for a three-phase system base on Kidson's et al. derivation. The rate of advancement of the interfaces $\xi_{M1,M1-M2}$ and $\xi_{M1-M2,M2}$ can be expressed as Eq. (5.3) and Eq. (5.4) respectively while the width of the intermetallic layer growth can then be obtained in Eq. (5.5).

Figure 5.1: Discontinuities in the concentration-versus-depth as a result of the diffusion barrier

$$\xi_{M1,M1-M2} = 2 \left[\left(\frac{(DK)_{M1-M2,M1} - (DK)_{M1,M1-M2}}{C_{M1,M1-M2} - C_{M1-M2,M1}} \right) \right] \sqrt{t} \quad \text{----- (5.3)}$$

$$\xi_{M1-M2,M2} = 2 \left[\left(\frac{(DK)_{M2,M1-M2} - (DK)_{M1-M2,M2}}{C_{M1-M2,M2} - C_{M2,M1-M2}} \right) \right] \sqrt{t} \quad \text{----- (5.4)}$$

$$W_{M1-M2} = 2 \left[\left(\frac{(DK)_{M2,M1-M2} - (DK)_{M1-M2,M2}}{C_{M1-M2,M2} - C_{M2,M1-M2}} \right) - \left(\frac{(DK)_{M1-M2,M1} - (DK)_{M1,M1-M2}}{C_{M1,M1-M2} - C_{M1-M2,M1}} \right) \right] \sqrt{t} \quad \text{----- (5.5)}$$

Equation 5.3 and Equation 5.4 describe the movement of the respective interfaces with respect to the mass invariant Matano interface. The interface $\xi_{i,j}$ will move to one side, remain stationary or move to the other side in accordance with the sign of the rate constant i.e. a negative $\xi_{i,j}$ value suggests that the interface moves toward i. This set of equation suggests that the IMC thickness growth rate and its interface move as a relationship to $t^{0.5}$ once the diffusion barrier has been formed. Figure 5.2 summarizes the proposed 2-stage kinetics of solid-liquid interdiffusion where the initial kinetics of Metal 1 consumed at a faster rate due to the formation of the diffusion barrier while a second kinetic grows with time as Au dissolves through the diffusion barrier.

Figure 5.2: Proposed two stages kinetics of solid-liquid interdiffusion

5.2 EXPERIMENT PROCEDURES

The proposed kinetics for solid-liquid interdiffusion was tested using Au with molten eutectic PbSn solder through the SLICF bonding. A series of fifty gold studs with a tip diameter of 25 μ m were mechanically bumped on aluminium metallized dies using a thermosonic wire bonder. The Au-studs were then bonded into corresponding via

containing eutectic 63Sn37Pb solder [82]. These 110 μ m via were spaced at a 130 μ m pitch. A 25 μ m tape adhesive was introduced between the die and the substrate to provide consistency in the standoff height for characterization. The height of the Au studs was measured using a high magnification 2D-microscope. The bumps for thirty units were measured and the average height (c_0) was used for analysis. The via consisted of a base pad with electrolytic Ni/Au surface finish with solder filled in the via. The base had a Au surface finish of 0.3 μ m over a 0.5 μ m nickel for soldering purposes. The interaction of Au with molten eutectic solder was investigated at bonding temperatures of 190°C, 230°C and 260°C at the intervals of 0.3 second, 1 second and 3 seconds. Each leg consists of five units for assessment. The bonding temperatures melt the solder and enable a mechanical force to break the oxide layer and form a bond under solid liquid interdiffusion. The setup was of similar configurations as illustrated in Figure 4.2.

The bond samples were directly encapsulated in epoxy and sectioned using a diamond cut-off wheel for analysis. The cross-sections of the joints were prepared for metallographic analysis by grinding and polishing. The microstructure characterization was carried out in scanning electron microscope (SEM) with an energy dispersive X-ray detector (EDX). For better phase contrast, the SEM images were captured in back-scattering mode and each intermetallic layer was identified by EDX. At every condition, the Au thickness and individual IMC thickness was measured for five bumps equally space out across the die. For each bumps, three different measurements were made across the interface using a digitized SEM micrograph. The average thickness of individual IMC layer of a unit (c_i) was taken for analysis. Similarly, the Au stud height after bonding was measured using a high magnification scope for these five bumps. The average Au stud height of the unit (c_1) was taken for computation. $c_0 - c_1$ estimated the thickness of the Au consumed for a specific bonding condition. The c_1 and $c_1 - c_i$ estimate the movement

of the interfaces with time. The movements of these interfaces were plotted for analysis. The Au consumption ($c_0 - c_1$) and the individual IMC thickness (c_i) were plotted for different bonding temperatures of 190°C, 230°C and 260°C at the time intervals of 0.3 seconds to and 3 seconds. Fig 5.3 illustrates the measured parameters used for the studies. The number of moles of Au in each intermetallic layer and Au consumed were estimated by subtracting the initial conical volume of the bumps from the remaining conical bump after bonding. These volumes were then divided by molar volume of their phases to estimate the no of moles of Au used. The molar volume of AuSn_2 , AuSn_4 and Au were taken as $42.8\text{cm}^3/\text{mol}$, $75.0\text{cm}^3/\text{mol}$, $10.2\text{cm}^3/\text{mol}$ respectively for computation.

Figure 5.3: Schematic illustration of the measured parameters for computation of the solid-liquid kinetics

For characterising the kinetics of solid diffusion for Au with eutectic solder, 60 units were assembled at a condition of 230°C at 0.3 second. To begin with, the remaining Au thickness (c_1) and the individual IMC thickness (c_i) were measured. Similar measurement approaches as above were adopted for thermal ageing measurement. The bonded samples were then annealed at 125°C, 150°C, and 165°C for 100 hours, 200 hours, 300 hours, and 500 hours. These thermal ageing temperatures were selected based on the thermal reliability test conditions. Each leg consisted of 5 units for measurement.

Similar morphology characterisations were carried out in SEM with EDX on the cross-section of the bonded samples for analysis. After subjecting to the specific conditions, the remaining Au thickness and its individual IMC thickness of the unit were measured for the five bumps through the digitized SEM micrograph and high magnification scope respectively. The average Au thickness (c_{1a}) and individual IMC thickness (c_{ia}) of a unit were used for analysis. Similar measurement approaches as Au-PbSn were adopted for Au-SAC measurement. The growth of individual IMC layers (c_{ia}) and the thickness of the Au consumption ($c_0 - c_{1a}$) were plotted with time for analysis.

The interaction of Au with molten SAC was investigated with similar die and substrate configuration. Due to higher melting point for SAC, its kinetic was studied at temperatures of 230°C, 260°C and 290°C at the time intervals of 0.3 second, 1 second and 3 seconds. For thermal aging growth studies, the bond samples were heated at 125°C, 150°C, and 165°C for duration of 100 hours, 200 hours, 300 hours, and 500 hours. Similar phase morphologies characterization, Au consumption and intermetallic thickness measurements were carried out on the cross-section of the bonded samples for characterizing Au-SAC kinetic.

5.3 Au WITH PbSn SOLDER

5.3.1 Phase morphologies under different bonding conditions

Figure 5.4 is the SEM image of the solid/liquid interface after bonding at 190°C for 0.3 seconds. A thin layer of AuSn₄ was observed at the interface after solidification. The AuSn₄ phases were seen to radiate from the interface. The sequence of the IMC formation can be traced using the concept of local equilibrium [91] and the binary section of the ternary phase diagram. As such, the AuSn₄ appeared to be the first phase at 190°C as

estimated by the isothermal line in Figure 5.5. This phase eventually formed a continuous AuSn_4 intermetallic layer as seen at the boundary interface in Figure 5.4. During cooling, the saturated Au solution precipitated as AuSn_4 according to the Au-PbSn phase diagram. Due to its orthorhombic crystal structure, this resulted in needle-like AuSn_4 intermetallic seen throughout the solder.

Figure 5.4: Interfacial microstructures showing AuSn_4 formation at 190°C for 0.3s

Figure 5.5: Isothermal at 190°C , 230°C and 260°C on the binary section of the ternary phase diagram Au-Sn-Pb showing thermodynamic favor phases of AuSn_4 and AuSn_2 respectively

At the bonding interface, the intermetallic regions also broke off and fell into the molten solder since they were brittle and further stressed by the precipitation cooling. As such, it appeared as though they had spalled off from the interface. That was similar to the observations by Ho et al. [83] for Au with eutectic solder.

Figure 5.6 shows the precipitation of AuSn_4 phases at the base of the joint. The AuSn_4 phases were ascertained from the dissolved Au, as there was no sign of AuSn_4 formation with eutectic PbSn after thermal aging for filled joint-in-via architecture. This suggests that Au diffuses through the molten solder and deposits at the base of the solder. The drive of these AuSn_4 phases may be caused by the difference in the concentration gradient between the barrier interface and the base of the joint or through the lowering of the free energy by forming the ternary thermodynamics phases $\text{Au}_{0.5}\text{Ni}_{0.5}\text{Sn}_4$ [94] at the base of the joint. For samples prepared at 190°C for 1 second and 3 seconds, similar AuSn_4 phases were observed with thickening IMC layer with larger extent of rod-like AuSn_4 phases spalling off the interface into the solder (see Figure 5.7). Identical phases were observed for the samples after 1 second and 3 seconds. This was a result of more Au dissolving into molten PbSn over a longer bonding time.

Figure 5.6: Interfacial microstructures showing AuSn_4 phases at the base of the Au-PbSn joint after bonding

Figure 5.7: Thickening of AuSn_4 layer and rod-like AuSn_4 phases spalling off the interface at 190°C for 3 seconds

Figure 5.8 is the back-scattered SEM images for bonding at 230°C for 1 second. It was identified by EDX analysis that a thin layer of about $1\mu\text{m}$ of AuSn_2 phase was formed at the interface followed by an AuSn_4 layer of about $5\mu\text{m}$ at 0.3 second. Large rod-like AuSn_4 phases appeared as dendrites encroaching into the bulk solder. The formation of the AuSn_2 layer is thermodynamically favored at 230°C as per phase diagram in Figure 5.5. This suggests that AuSn_2 forms at the bonding interface while Au simultaneously dissolves into molten PbSn . Due to the higher bonding temperature, the diffusivity of Au increases and helps to promote more Au to dissolve into the solder. During cooling, the saturated solution precipitates as AuSn_4 with Pb-rich phases around the vicinity. At higher bonding temperatures, the amount of AuSn_4 phase at the base increases. Similarly, thickening intermetallic layer and growth of AuSn_4 formations were observed with increasing time.

At a bonding temperature of 260°C , the AuSn_2 and AuSn_4 layers were detected with thickening of the AuSn_2 layer. Larger chunks of rod-like AuSn_4 phases were observed to spall off from the interface as shown in Figure 5.9. Table 5.1 summarizes the IMC

morphologies at the solid-liquid interfaces. Similarly, thickening phenomenon and rod-like AuSn_4 phases were seen to extend into bulk solder as the bonding time increased.

Figure 5.8: Interfacial microstructures showing AuSn_2 and AuSn_4 formation at 230°C for

1 seconds

Figure 5.9: Larger chunks of rod-like AuSn_4 phases spalling off from the bond interface at

260°C for 1 second

Table 5.1: Summary of morphologies present with different SLICF bonding at different temperatures and time

Time	0.3s	1s	3s
----- Temperature			
190°C	AuSn_4	AuSn_4	AuSn_4
230°C	AuSn_4 & AuSn_2	AuSn_4 & AuSn_2	AuSn_4 & AuSn_2
260°C	AuSn_4 & AuSn_2	AuSn_4 & AuSn_2	AuSn_4 & AuSn_2

5.3.2 Diffusion barrier at bond interface

Figure 5.10 plots the growth of AuSn₄ layers at 190°C with reference to the base of the Au stud. The AuSn₄ layer appeared to move into the Au stud. After a time of 0.3 seconds, it appeared that Au was consumed by simply replacing the Au by a similar thickness of AuSn₄ layer. The Au/AuSn₄ interface was 1.57μm away from the initial bonding interface. The Kirkendall interface shifted to the left, suggesting that Au dominated the kinetics of solid-liquid interdiffusion between Au and molten solder. This is expected, as the solid-liquid interdiffusion is at least 4 orders of magnitude faster than solid diffusion [90].

Figure 5.10. Au and AuSn₄ thickness at 190°C with reference to the base of the Au

At the interface, the local equilibrium can be assumed, where the concentration of the Au can be assumed to be the metastable substrate + PbSn liquid phase boundary. Due to the high solubility of Au, the Au dissolved into molten PbSn and diffused easily to the rest of the solder. At the initial bonding interface, the Au concentration reached a thermodynamic stability, where it precipitated the AuSn₄ phases according to the binary section of the Au-Pb-Sn ternary phase diagram [74, 137] as in Figure 5.5. The AuSn₄ phases eventually nucleated heterogeneously and grew into a diffusion barrier layer, retarding the rate of Au dissolving into the molten solder as early as 0.3 second. As the

dissolved Au solution precipitates AuSn_4 phases during cooling, it contributed to the thickening of the AuSn_4 layer due to the saturated Au concentration at the interface. Since the AuSn_4 layer consists of both the diffusion layer and the precipitation, the thickness of the AuSn_4 diffusion layer cannot be distinguished and used for further analysis.

At a higher bonding temperature of 230°C after 0.3 seconds, a sequential layout of the AuSn_2 layer with the AuSn_4 layer is observed in Figure 5.8. This new AuSn_2 phase was formed as a result of higher bonding temperature. Large rod-like AuSn_4 phase appeared as dendrites encroaches into the bulk solder. Similarly, thickening intermetallic layers and growth of AuSn_4 formations were observed at a longer bonding time. Figure 5.11 shows the intermetallic layers growing at 230°C with reference to the base of the Au stud. It was observed that for a bonding time of 0.3 second, a sequential layer of $1.1\mu\text{m}$ of AuSn_2 followed by a $5.1\mu\text{m}$ AuSn_4 layer was formed in between the Au and solder. These intermetallic layers replaced the Au consumed. The $\text{AuSn}_4/\text{PbSn}$ interface was $0.6\mu\text{m}$ away from the initial solid liquid interface while $\text{AuSn}_2/\text{AuSn}_4$ interface was another $6.2\mu\text{m}$ away from the initial solid-liquid interface. Thus, a total of $6.8\mu\text{m}$ of Au was consumed to form the IMC layers and dissolved into the molten solder.

At 230°C , the dissolved Au reacted to precipitate AuSn_2 next to the Au stud interface. The formation of the AuSn_2 was in agreement with the lowering of the Gibbs free energy according to the binary section of the Au-Pb-Sn ternary phase diagram. The AuSn_2 phases eventually nucleated heterogeneously and grew into a layer. Meanwhile, the Au dissolved rapidly into molten solder and diffused throughout the solder. As these interactions and dissolution consumed Au, the Au/ AuSn_2 interface moved toward Au.

Figure 5.11: Au, AuSn₂ and AuSn₄ thickness at 230°C with reference to the base of the Au

The formation of AuSn₄ layer can either be part of the diffusion barrier formed by reaction or merely precipitated by the saturated Au solution at the interface during cooling. If the AuSn₄ layer was part of the diffusion barrier during solid-liquid interdiffusion, it will either dissolve or spall off into molten solder due to its thermodynamic instability as per depicted by the Au-Pb-Sn phase diagram. Thus, the AuSn₄ precipitates did not have the opportunity to build up into a diffusion barrier. Therefore, the AuSn₂ layer is likely to be the only diffusion barrier during the solid liquid interdiffusion at 230°C. This diffusion barrier was seen as a layer of AuSn₂ as early as 0.3 second, suggesting an instantaneous reaction. Once the diffusion barrier is formed, the rate of Au dissolving in molten solder slowed down with the thickening of AuSn₂ diffusion barrier.

At 260°C, similar AuSn₄ and AuSn₂ phase morphologies and growth phenomenon were observed at the solid-liquid interface. This is a result of similar kinetics and thermodynamic stability at 260°C as compared to 230°C. A thickening of the AuSn₂ layer was observed as a result of higher diffusivity and solubility of Au at 260°C. Rod-like

AuSn₄ phases were seen to spall off from the interface into molten solder. As Au is consumed by molten solder, Figure 5.12 shows the Au/AuSn₂ and AuSn₂/PbSn interfaces move toward Au. Similar to the behavior at 230°C, the AuSn₂ acted as the only diffusion layer at 260°C. Similar amounts of AuSn₄ precipitation were observed for bonding temperatures of 230°C and 260°C (Figure 5.13). This suggests that a gradual Au concentration gradient exists at the AuSn₂/solder interface. Thus, this provides further evidence that AuSn₄ layer was precipitated by the dissolved Au rather than acting as the diffusion barrier during solid-liquid interdiffusion. Therefore, AuSn₂ acts as the only diffusion barrier at 230°C and 260°C.

Figure 5.12: Au, AuSn₂ and AuSn₄ thickness at 260°C with reference to the base of the Au

Figure 5.13: Similar AuSn₄ precipitation trend at 230°C and 260°C

5.3.3 Rate of Kinetics for Au with molten solder

The kinetic of Au with molten eutectic solder is affected by the concentration of Au in solder. The estimation of Au consumption for 260°C at 3 seconds was found to be only 7.2 at.% of the solder. This suggests that the Au concentration in the solder is far from the saturation value. A generic power law as shown in Eq. (5.6) is used to establish the relationship of Au consumed and its IMC growth in the Au - eutectic PbSn solder system. In this equation, x is the intermetallic thickness, b the rate constant at temperature T , t the time of bonding and n the time exponent. Since the rate of Au diffusion in molten solder dominates the reaction, this equation had similar empirical expression as that of Ghosh et al. [89, 138] for growth kinetics. They discussed that n is an indicator of time-dependent diffusivity (i.e. $n < 0.5$ diffusivity increase with time vice versa) while k is the rate constant with temperature (i.e. diffusivity higher with increase in temperature) in their equations.

By plotting natural logarithm form for Eq. (5.6), a regression line can be plotted over the individual growth of Au-Sn intermetallic layers. The b and n can be computed from Figure 5.14 as shown in Eq. (5.7).

$$x = bt^n \quad \text{----- (5.6)}$$

$$\ln x = n \ln t + \ln b \quad \text{----- (5.7)}$$

Figure 5.14 shows the growth of AuSn_4 layers and the consumption of Au at 190°C. The Au thickness was consumed at a rate constant of $3.27 \times 10^{-4} \text{ cms}^{-0.575}$ with a time exponent of 0.575. The rate of Au thickness consumption appears to reduce with time. This is likely due to the formation and growth of the AuSn_4 layer that acts as the diffusion barrier for Au to dissolve into molten solder. As the diffusion barrier thickness increases with time, the rate of Au dissolves into molten solder decreases. The AuSn_4 thickness seen at 190°C

was closed to the Au thickness consumed. As discussed previously, AuSn₄ layer contained the diffusion barrier as well as the precipitated AuSn₄ during cooling.

Figure 5.14: Growth of AuSn₄ layers and Au thickness consumed at 190°C

As shown in Figure 5.15, positive IMC growths were also observed for AuSn₂ and AuSn₄ intermetallic layers at bonding temperature of 230°C. It was difficult to quantify the growth of the Au-Sn IMC layers in solid-liquid interdiffusion by examining the growth of an individual IMC layer. The individual IMC layers grew at different rates with time due to changes in atomic volume of diffusing species [89], different IMC layers formation, [89] and different layers formed by precipitation. The sum of all the IMC layer thickness does not equal to the thickness of the Au consumption. This is because a significant amount of Au dissolves into molten solder during solid-liquid interdiffusion, which is not accounted in the intermetallic layers.

Figure 5.15: Growth of AuSn₂, AuSn₄, total IMC layer and Au consumed at 230°C

The kinetics of solid-liquid interdiffusion is a complex process and the intermetallic growth cannot fully account for their kinetics. The rate of gold consumption appears to be a better representation in the solid-liquid interdiffusion than the yardstick measurement by the IMC growth. Figure 5.16 shows the rate of Au consumed at different temperatures. The Au consumption rate does not follow a $t^{0.5}$ relationship for the solid-liquid interdiffusion of Au with molten eutectic solder. This is likely due to the reaction of Au with molten solder in the formation of the diffusion barrier. The b and n of the consumed thickness of Au for bonding temperatures of 190°C, 230°C and 260°C are computed and summarized in Table 5.2. The coefficient of the time exponent n varies for 0.575 for 190°C and around 0.28 for a bonding temperature of 230°C to 260°C. The n for temperature 230°C to 260°C are noted to be in a similar range.

Figure 5.16: Au consumption at 190°C, 230°C and 260°C are non-parabolic with time

Table 5.2: Summary of the rate constant b and the time component constant n

Temperature	190°C	230°C	260°C
Rate constant k (μms^{-n})	3.27	9.79	15.36
Time exponent n	0.575	0.276	0.287

In Figure 5.16, the diffusion barriers were seen to build up as early as after 0.3 seconds for temperature ranging from 190°C to 260°C. Thus, this suggests that the diffusion barrier is formed almost instantaneously with some amount of Au consumption. Once the diffusion barrier is formed, the kinetics change as the law of diffusion must be obeyed with Au diffusing through the diffusion barrier before dissolving into molten solder. As per Eq. (5.3), based on the fundamentals of Fick's First Law, the Au consumption rate follows a $t^{0.5}$ relationship. As re-plotted in Figure 5.16 with the proposed hypothesis, Figure 5.17 shows $t^{0.5}$ fitted regression line with specific y-intercepts for different bonding temperatures. A good correlation factor of at least 0.95 can be obtained for the different bonding temperatures. This provides evidence to support the proposed two-stage kinetic with the formation of an instantaneous diffusion barrier.

Figure 5.17: A $t^{0.5}$ time relationship with a good correlation factor of at least 0.95 can be obtained for bonding temperature of 190°C to 260°C once an instantaneous diffusion layer is assumed

The y-intercepts account for the amount of Au consumed instantaneously upon contact as Au dissolves into molten solder with the formation of the diffusion barrier at the different bonding temperature. The Au consumptions are found to increase with the increasing bonding temperatures. The regression line at 190°C records near to zero Au consumption thickness as the bonding temperature is near to the melting point of the solder. 4.64μm and 7.21μm Au thicknesses are consumed instantaneously for 230°C and 260°C respectively. Assuming no Au consumption at the melting point of solder, a linear relationship of Au consumption with respect to absolute temperature T is obtained as shown in Figure 5.18.

Figure 5.18: Plot showing instantaneous diffusion barrier thickness d_0 vs. the bonding temperature

The set of data suggests that the Au consumption follows a $t^{0.5}$ relationship as it obeys a diffusion law once an instantaneous diffusion barrier is formed. The Au consumption x can be described by Eq. (5.8) where d_0 denotes the instantaneous Au consumption upon contact with molten solder. The d_0 accounts for the instantaneous dissolution of Au into molten solder with the formation of a diffusion barrier. Once the diffusion barrier is formed, the Au dissolves through the diffusion barrier into the molten solder with a $t^{0.5}$ relationship.

$$x = d_0 + kt^{0.5} \quad \text{----- (5.8)}$$

The k in Eq. (5.8) represents the rate constant of Au dissolving into molten solder through the diffusion barrier. This goes through a series of complex interactions that include Au reacting with the diffused Sn at the Au and diffusion barrier interface. It also involves the Au diffusing through the diffusion barrier and dissolving into molten solder directly or through the spalling at the interface. The dissolved Au then diffuses throughout the molten solder and precipitates as IMCs. These complex processes appear

to be diffusion controlled through the diffusion barrier. In addition, these processes depend on prior processes and thus they take the diffusion time exponent of 0.5 second.

As shown by the gradient in Figure 5.17, the rate constant k increases with increasing bonding temperature. This is a result of the higher reaction and dissolution rate of Au into molten solder with increasing temperature. Assuming the interaction is rate-limited by the diffusion processes, the rate constant k takes the form of the diffusion coefficient (i.e., Arrhenius relationship) as shown in Eq. (5.9) where Q is the apparent activation energy and k_0 is the net diffusivity rate constant at absolute temperature. By applying the natural logarithm on both sides of Eq. (5.8), an Arrhenius plot can be used to estimate k_0 and Q for the diffusion kinetic as shown in Figure 5.19.

Figure 5.19: Plot showing $\ln k$ vs. $1/T$ to estimate K_0 and Q

$$k = k_0 \exp\left(-\frac{Q}{RT}\right) \quad \text{----- (5.9)}$$

The rate constant k_0 and activation energy Q for Au consumed in molten eutectic solder is computed to be $1.12 \times 10^3 \mu\text{ms}^{-0.5}$ and 22.26 kJ/mol respectively. The initial Au consumption by solder is estimated to be 3.15 μm for the initial 1 second at 183°C and this decelerated with the formation of the intermetallic layer. This is a much higher dissolution rate than the 1.3 $\mu\text{m/s}$ at 209°C reported by Zribi [95-96]. The difference in the

dissolution rate is due to the nature of Au consumption kinetics governed by a function of $t^{0.5}$. Thus, this results in a higher Au consumption at the initiation of the solid liquid kinetic.

This study suggests that the solid-liquid interdiffusion can be simply described as a two-stage kinetics using the Au consumption. The initial kinetics can be described by the instantaneous dissolution of Au into molten solder couple for the formation of the diffusion barrier. Once the diffusion barrier is formed, it involves a diffusion kinetic of the Au dissolving into the molten solder through the diffusion barrier with time.

5.3.4 Migration of the interfaces

The diffusion barriers were seen to build up as early as after 0.3 seconds for temperature ranging from 190°C to 260°C. Once the diffusion layer was erected, the kinetics changed. As the diffusion layer is formed instantaneously, the rate of Au consumption appeared to be rapid and cannot be quantified. Once the diffusion barrier is formed, interdiffusion through the layer needs to kick in to lower the Gibbs free energy. The Matano interface at the Au and diffusion barrier is not valid after the formation of the diffusion barrier. Figure 5.20 plots the AuSn₂ thickness vs. $t^{0.5}$. Linear regression lines with good correlation values were observed for the growth of the AuSn₂ diffusion barrier at 230°C and 260°C. The thickness of the diffusion barrier was estimated by the back extrapolation of the AuSn₂ growth in Figure 5.20. A diffusion barrier of 0.70μm and 2.33μm was estimated to form at time zero for temperature at 230°C and 260°C as the Au comes into contact with molten solder. This result further supports the hypothesis that a two-stage kinetics exists for Au with molten eutectic solder. At the initial stage, there is an instantaneous Au consumption as Au dissolves into molten solder to form a diffusion barrier. The movement of the interfaces $\xi_{\text{Au,Au-Sn}}$ and $\xi_{\text{Au-Sn,Sn}}$ with respect to the mass invariant

Matano interface can be described by Eq. (5.10) and Eq. (5.11) respectively. The width of the AuSn_2 growth can also be obtained from Eq. (5.12).

$$\xi_{\text{Au-Sn,Sn}} = 2 \left[\left(\frac{(DK)_{\text{Sn,Au-Sn}} - (DK)_{\text{Au-Sn,Sn}}}{C_{\text{Au-Sn,Sn}} - C_{\text{Sn,Au-Sn}}} \right) \right] \sqrt{t} \quad \text{----- (5.10)}$$

$$\xi_{\text{Au,Au-Sn}} = 2 \left[\left(\frac{(DK)_{\text{Au-Sn,Au}} - (DK)_{\text{Au,Au-Sn}}}{C_{\text{Au,Au-Sn}} - C_{\text{Au-Sn,Au}}} \right) \right] \sqrt{t} \quad \text{----- (5.11)}$$

$$W_{\text{Au-Sn}} = 2 \left[\left(\frac{(DK)_{\text{Sn,Au-Sn}} - (DK)_{\text{Au-Sn,Sn}}}{C_{\text{Au-Sn,Sn}} - C_{\text{Sn,Au-Sn}}} \right) - \left(\frac{(DK)_{\text{Au-Sn,Au}} - (DK)_{\text{Au,Au-Sn}}}{C_{\text{Au,Au-Sn}} - C_{\text{Au-Sn,Au}}} \right) \right] \sqrt{t} \quad \text{----- (5.12)}$$

Figure 5.20: Estimation of AuSn_2 diffusion barrier at origin for a bonding temperature of 230°C and 260°C

Once the diffusion barrier was formed, both Au and Sn species interacted as a solid-solid-liquid. As the diffusion barrier is thin, the Matano interface located at the center of this instantaneous diffusion barrier at time zero was taken as ease of analysis. Figure 5.21 and Figure 5.22 show $\xi_{\text{Au,Au-Sn}}$ and $\xi_{\text{Au-Sn,Sn}}$ with respect to the Matano interface at 230°C and 260°C respectively.

Figure 5.21: Displacement of $\xi_{\text{Au,Au-Sn}}$ and $\xi_{\text{Au-Sn,Sn}}$ with respect to Matano interface at 230°C

Figure 5.22: Displacement of $\xi_{\text{Au,Au-Sn}}$ and $\xi_{\text{Au-Sn,Sn}}$ with respect to this Matano interface at 260°C

At 190°C, the thickness of the diffusion barrier was unknown and hence the AuSn₄/PbSn interface during the molten state cannot be determined. Based on the Au-Pb-Sn ternary phase diagram, the AuSn₄ + L exists in the thermodynamic equilibrium at the AuSn₄/PbSn interface. Due to the difference in concentration gradient, the dissolved Au

at the interface boundary diffused into the rest of the solder. In order to resort the equilibrium stability at the interface, the AuSn_4 will continuously dissolve into molten solder. For the purpose of discussion, at the Au/AuSn_4 interface, the rate constant $2\left(\frac{(DK)_{\text{Au,AuSn}_4} - (DK)_{\text{AuSn}_4,\text{Au}}}{C_{\text{AuSn}_4,\text{Au}} - C_{\text{Au,AuSn}_4}}\right)$ is computed to be -3.46 with respect to the initial bonding interface. The negative rate constant suggests that there is a net flux of Au converting to AuSn_4 . The availability of Sn for this conversion is likely due to Sn atoms present at the interface during the solid liquid interdiffusion or Sn diffusing through the AuSn_4 diffusion barrier. The Sn then thermodynamically reacts with Au to form the AuSn_4 phases. This formation consumed Au and hence the Au/AuSn_4 layer moved towards the Au stud.

In Figure 5.11, the Au/AuSn_2 and $\text{AuSn}_2/\text{AuSn}_4$ interfaces at 230°C moved towards the Au stud. Since AuSn_2 is the only diffusion barrier, the gradient of Au/AuSn_2 and $\text{AuSn}_2/\text{solder}$ in Figure 5.21 represents the rate constant at $\text{AuSn}_2/\text{PbSn}$ i.e. $2\left(\frac{(DK)_{\text{AuSn}_2,\text{PbSn}} - (DK)_{\text{PbSn,AuSn}_2}}{C_{\text{PbSn,AuSn}_2} - C_{\text{AuSn}_2,\text{PbSn}}}\right)$ and Au/AuSn_2 interfaces i.e. $2\left(\frac{(DK)_{\text{Au,AuSn}_2} - (DK)_{\text{AuSn}_2,\text{Au}}}{C_{\text{AuSn}_2,\text{Au}} - C_{\text{Au,AuSn}_2}}\right)$ during solid-liquid interdiffusion respectively. As the diffusion in molten metal is about four orders of magnitude faster than solid diffusion [90], the rate constant at $\text{AuSn}_2/\text{PbSn}$ is simplified to $2\left(\frac{-(DK)_{\text{PbSn,AuSn}_2}}{C_{\text{PbSn,AuSn}_2} - C_{\text{AuSn}_2,\text{PbSn}}}\right)$. The rate constant at the $\text{AuSn}_2/\text{PbSn}$ interface is estimated to be $-3.87 \mu\text{ms}^{0.5}$. The negative sign suggests that the AuSn_2 dissolves into molten solder with $\text{AuSn}_2/\text{PbSn}$ interface moving toward Au. This is a result of AuSn_2 dissolving continuously into molten solder to maintain the equilibrium stability at the $\text{AuSn}_2/\text{PbSn}$ interface.

At the Au/AuSn_2 interface, the rate constant is estimated to be $-5.10 \mu\text{ms}^{0.5}$ in Figure 5.21. The value suggests that the rate of Au converting to AuSn_2 is at a faster rate than AuSn_2 dissolving into molten solder. Therefore, Au is consumed while the Au/AuSn_2 interface moves towards Au. The delta in the rate constant between the interfaces suggests that the diffusion barrier AuSn_2 was growing at $1.23 \mu\text{ms}^{0.5}$.

At 260°C, with a similar analogy as 230°C, the interfaces shifted towards Au as shown in Figure 5.22 with similar interdiffusion. The AuSn₂ diffusion barrier layer was growing at 1.91 μm s^{0.5} while the rate constant for Au/AuSn₂ and AuSn₂/PbSn was at -6.51 μm s^{0.5} and -8.42 μm s^{0.5} respectively. The rate constant for Au/AuSn₂ and AuSn₂/PbSn at 260°C has a ratio of about 1.65 with respect to their rate constant at 230°C, suggesting that the rate of Au consumption and the movement of the Au/AuSn₂ and AuSn₂/PbSn interfaces at 260°C is faster than at 230°C by about 65%. This is likely due to the decrease in the energy barrier as a result of higher solubility and increase diffusivity of Au into molten solder as the bonding temperature increases.

5.3.5 Dissolving of Au in Solid liquid interface

During bonding, the dissolution and reaction mechanisms compete with each other to reduce the free energy of the system. As solid-liquid interdiffusion is three to four orders of magnitude faster than solid interdiffusion, the consumption of Au was used to estimate the interaction of Au with molten solder. The Au interacted with Sn in molten PbSn solder to form AuSn₄ or/and AuSn₂. Simultaneously, the Au dissolves into molten solder. Thus, the difference between the amount of Au consumed and the amount of Au in the diffusion barrier layers can be used to estimate the amount of Au dissolved in molten solder. Assuming that the thickness of the intermetallic layers is the same as the diffusion barriers, the number of mole of Au atoms were computed for 190°C, 230°C and 260°C as shown in Figure 5.23 to Figure 5.25 respectively. It is noted in Figure 5.23 to Figure 5.25 that the amount of Au consumed was found to be significantly higher as compared to the growth of the Au-Sn layers. During solid-liquid interdiffusion, a significant amount of Au dissolved into molten solder even in the presence of the diffusion barrier.

Figure 5.23: Au consumption in solder and in AuSn₄ at 190°C

Figure 5.24: Au consumption in solder and in AuSn₂ and AuSn₄ at 230°C

Figure 5.25: Au consumption in solder and in AuSn₂ and AuSn₄ at 260°C

Figure 5.26 summarizes the percentage of Au dissolved into molten solder with time. It is noted that a significant amount of Au dissolves into molten solder instantaneously followed by the retardation in the rate of Au dissolved. This can be explained by the high solubility of Au dissolving into the molten solder. The dissolved Au forms an instantaneous diffusion barrier that drastically retards the rate of Au dissolving into molten solder. As seen in Figure 5.26, the amount of Au continued to be consumed steadily with time, suggesting the continuous dissolution of Au into the molten solder even with the formation of the diffusion barrier. It is also noted that the increase in bonding temperature increases the amount of Au dissolving into molten solder as the diffusivity of Au increases with temperature. This study shows that the amount of Au dissolving into molten solder is significant and thus the Au consumption appears as a better yardstick to quantify the kinetics for solid-liquid interdiffusion.

Figure 5.26: Au dissolution in molten solder at different bonding temperatures

5.3.6 Kinetics of Au with solid eutectic solder

The kinetic of the IMC growth during solid diffusion needs to be studied as it provides important information about the joint behaviour as it undergoes assembly processing steps

and reliability testing. Thus, it is important to study the growth kinetics of the IMC to determine its vital role as compared to its bonding.

At 125°C, Figure 5.27 shows that the microstructure under thermal aging conditions appeared to have similar morphologies in the solid-liquid interdiffusion. No increase in IMC was observed in the bulk solder except for the growth in IMC layers. With the aging temperature increases to 150°C, the AuSn layer appears next to the Au interface.

Figure 5.27: SEM picture at interface of SnPb-Au thermally aged at 125°C for (a) 100 hours (b) 200 hours (c) 300 hours (d) 500 hours

A complex growth in the intermetallic layers at 150°C was observed in Figure 5.28. The growth of the AuSn₄ and AuSn₂ appeared to slow down while the AuSn intermetallic layer had thickened with time (Figure 5.29). Similar complex growths were also observed in the intermetallic layers in 165°C. It appears that the growth kinetics of each IMC layer is dependent on its neighboring layers. Based on these erratic growths, it is difficult to

determine the diffusivity due to the declining portion of one IMC layer while the thickening of another layer. Thus, the rate of Au consumption was used to estimate the kinetic rate of Au diffusing into solid eutectic solder under thermal aging conditions.

Figure 5.28 SEM picture at interface of SnPb-Au thermally aged at 150°C for (a) 100 hours (b) 200 hours (c) 300 hours (d) 500 hours

Figure 5.29: Relation AuSn₄ and AuSn₂ layers retarded with increasing AuSn layer with time for thermal aging condition at 150°C

Eq. (5.8) was also applied to account for the kinetics in solid diffusion. In solid diffusion, a $t^{0.5}$ relationship can be adopted with d_0 representing the initial IMC layer before solid diffusion. Figure 5.30 summarizes the Au consumption at 125°C, 150°C and 165°C. The kinetics of Au consumed by the eutectic solder for thermal aging was computed to have a rate constant of $0.521 \mu\text{ms}^{-0.5}$ with an activation energy of 13.81 KJmol^{-1} . At the melting temperature of eutectic solder (183°C), the rate at which Au was consumed in solid diffusion was at least two orders of magnitude slower than the Au consumption in solid-liquid interdiffusion. Similar results have been reported by Kim et al [88] with at least two orders of magnitude between solid-liquid interdiffusion and solid diffusion for Au with near-eutectic PbSn solder.

Figure 5.30: Au consumption with square root of time for Au with PbSn for thermal aging condition at 125°C, 150°C and 165°C

5.4 Au WITH SnAgCu SOLDER

Lead-free soldering has become a global trend in microelectronic packaging due to the registration and implementation of taxes for lead containing solders for electronic,

automotive and aircraft industries by the year 2006 [105]. Recent studies have shown that SnAgCu (SAC) solder is a promising Pb-free solder [104] as it possesses excellent wettability, superior mechanical strength and good compatibility with existing assembly processes. Being a tin dominant lead-free solder, SAC suffers poor reliability with Au due to its rapid formation of brittle Sn-Au intermetallics [97-98]. This dampens the prospect of SAC as the bonding material with Au studs for low-cost, fine-pitch, flip-chip interconnect systems with the underbump metallization removed [29,82]. This encourages more research in order to understand the kinetics of Au with SAC and compare it with Au and eutectic PbSn solder in its performance.

5.4.1 Microstructures at different bonding conditions

At a bonding temperature of 230°C for 0.3 second (Figure 5.31), intermetallic layers of AuSn₂ and AuSn₄ were formed at the interface with needle-like AuSn₄ phases projected from the bonded interface into the solder. Upon contact, the Au dissolves and diffuses throughout the molten SAC while reacting with Sn to form a thin diffusion barrier of AuSn₂, AuSn₄ or their combinations. Since the Au-SnAgCu phase diagram is not available, the type and number of diffusion barriers present at the interface cannot be determined. The formation of the diffusion layer retarded the dissolution rate of Au into molten SAC. During cooling, the saturated Au solution precipitated as AuSn₄ phases, in accordance with the Au-Sn binary phase diagram. Thus, needle-like AuSn₄ phases were seen throughout the SAC. No traces of Ag₃Sn or Cu contained intermetallic were observed which was similar to Kim's et al. finding [88]. Similar microstructures were observed for the 1 second and 3 second samples with thickening IMC layers and growth of needle-like AuSn₄ precipitates as more Au dissolves into molten SAC.

Figure 5.31: Interfacial microstructures by EDX showing AuSn₂ and AuSn₄ formation at 230°C at 0.3 second

Figure 5.32(a) shows the microstructures at 260°C after 0.3 second. The Au tip was no longer apparent but with layers of AuSn, AuSn₂ and AuSn₄ sequentially laid out from Au into SAC. At 0.3 second, the AuSn₄ phase appeared to radiate from the bond interface into SAC. As the bonding time increased to 1 second (Figure 5.32(b)), the AuSn and AuSn₂ layers thickened with growing AuSn₂ dendrites into the SAC. In bulk solder, AuSn₄ precipitates were observed with few needle-like structures. As the time increased to 3 seconds (Figure 5.32(c)), chunks of AuSn₂ were surrounded with AuSn₄ phases in SAC.

Figure 5.32: Interfacial microstructures showing AuSn, AuSn₂ and AuSn₄ formation at 260°C at (a) 0.3 second (b) 1 second and (c) 3 seconds

The IMC layers formed were similar to the IMC layers for Au with SnAg [90]. This is a result of thermodynamic constraints. The AuSn₄ phases throughout the SAC were likely

due to the precipitation of the saturated solution as Au dissolved and diffused throughout SAC. As the bonding time increased, more Au dissolved and generated a thickening of AuSn and AuSn₂ layers. Dendritic AuSn₂ was seen to grow from the interface and eventually formed spherical chunks of AuSn₂ in the middle of the bond interface. This was likely due to the shape of the Au stud that accelerated interactions at the tip. The spheroid structure minimized the adhesion and with its brittleness, self-weight and stresses, the chunks of AuSn₂ phases spalled off from the interface into the bulk SAC during cooling. During solidification, non-equilibrium cooling existed and thus promoted segregation. This resulted in precipitation of high melting AuSn₂ phases followed by low-melting AuSn₄ phases during cooling as seen in Figure 5.32 and Figure 5.33.

A similar phenomenon was observed for all bonding occurring at 290°C. Thickening AuSn and AuSn₂ layers with more chunks of AuSn₂ were observed in the SAC (Figure 5.33). This was a result of higher diffusivity of Au into molten SAC with the increase in bonding temperature. A similar segregation phenomenon was also observed.

Figure 5.33: Interfacial microstructures showing AuSn, AuSn₂ and AuSn₄ formation at 290°C at 0.3 seconds

5.4.2 Kinetics of solid liquid interdiffusion

Similarly, a generic power law according to Eq. (5.6) was used to estimate the rate of IMC growth for Au with SAC. This is to confirm whether the two-stage kinetics is

applicable for Au with SnAgCu. The regression power law curve was then fitted over the individual growth of Au-Sn intermetallic layers and the rate of Au thickness consumed over time. The aim was to estimate the time exponent of the interactions. Figure 5.34 shows the growth of individual Au-Sn layers and the consumption of Au at 230°C. With the best-fitted curves, the Au consumption, layer thickness of AuSn₂ and AuSn₄ all increased with a positive time exponent varying from 0.68-0.71. Positive growths were also observed for AuSn and AuSn₂ intermetallic layers (Figure 5.35) at a bonding temperature of 260°C. A faster Au consumption was observed with no change of AuSn₄ thickness for the different bonding duration, which suggests the precipitation of AuSn₄. Similar observations were also seen at a bonding temperature of 290°C.

Figure 5.34: IMC growth and Au consumption at 230°C

Figure 5.35: IMC growth and Au consumption at 260°C

Similarly for Au with eutectic PbSn, it is difficult to quantify the growth of the Au-Sn IMC layers in solid-liquid interdiffusion by examining the growth of an individual IMC layer. The individual IMC layers grew at different rates due to changes in the atomic volume of diffusing species [89], different IMC layer formation [89], and different layers formed by precipitation. Lumping all of the Au-Sn intermetallics into a single IMC layer (Figure 5.36) did not appear to be a good representation of IMC growth for solid-liquid interdiffusion. For example, the total IMC layer formed at 260°C appeared to be thinner than the layer formed at 230°C as time increased. This was associated with the formation of additional AuSn (26.8 cm³/mol [139]) layer which was denser than the AuSn₂ (42.8 cm³/mol) and AuSn₄ layers (75.0 cm³/mol) [29]. In addition, the quantification of intermetallic growth did not account for the amount of Au dissolving in molten SAC. The amount of Au in molten solder is significant and needs to be accounted for as in the study of Au in eutectic PbSn. As the solid-liquid interdiffusion is 4 orders of magnitude faster than solid diffusion [90], the rate of Au consumed dominates the interaction and thus, appears to be a better representative variable in estimating the IMC growth.

Figure 5.36: Growth of total Au-Sn intermetallic layer

The n and b of the Au consumption for temperatures 230°C, 260°C and 290°C were computed and summarized in Table 5.3. It is noted that the time exponent varied from 0.41 to 0.68, ranging around a time exponent of 0.5. The two-stage kinetics for solid-liquid interdiffusion was put to test for Au with SnAgCu. A good correlation factor of at least 0.98 was observed in Figure 5.37 for different bonding temperatures, which suggests that the rate of Au consumes in SAC follows a function of $t^{0.5}$. This has similar behavior for Au with PbSn except for a thin instantaneous diffusion layer observed in SnAgCu. The initial Au consumption accounts for the Au dissolving into molten solder with the formation of the instantaneous diffusion barrier. It can be estimated by a linear function of absolute temperature (i.e. $0.032T - 15.556$ where T is the absolute temperature in Kelvin). The thin diffusion barrier is likely driven by the increased availability of Sn atoms at the bonding interface. Thus, abundant IMCs are formed at the solid-liquid interface, which easily nucleated and grew by the interfacial reaction to become a thin diffusion barrier. Once the diffusion barrier is formed, the diffusion kinetic kicks in with time and dominates the solid liquid interdiffusion. The rate constant k in Eq. 5.9 accounts for the rate of Au dissolving through the diffusion barrier into SAC.

Table 5.3: Summary of the rate constant k and the time exponent for Au consumption thickness at temperatures 230°C, 260 °C and 290 °C

Bonding temperature	230°C	260°C	290°C
Time exponent n	0.68	0.41	0.50
Rate constant k (μms^{-n})	5.07	11.28	17.42

By applying the natural logarithm in Eq. (5.9), a regression line can be plotted to determine k_0 and Q . The rate constant k_0 and activation energy Q for Au consumed in molten SAC were thus estimated to be $2.45 \times 10^4 \mu\text{ms}^{-0.5}$ and 34.63 kJ/mol, respectively. The dissolution rate of Au with SnAgCu was estimated to dissolve 4.98 μm for the initial 1 second at 217°C and then decelerated due to the formation of the diffusion barrier. At

the melting point of the solder, a higher dissolution rate of Au in SnAgCu is computed as compared to Au in eutectic solder.

Figure 5.37: Au consumption with square root of time for Au with SnAgCu for solid liquid interdiffusion at 230°C, 260°C and 290°C

5.4.3 Kinetics during thermal aging

The microstructure under thermal aging appeared to be similar to the microstructures in solid-liquid interdiffusion except that it had developed thickening intermetallic layers. As a result of the complex growth of IMC layers in solid-liquid diffusion, the growth of the individual intermetallic layers was different (Figure 5.38). With similar treatment for the solid-liquid diffusion, the rate of Au consumption was used to estimate the growth of the IMC layers during aging. Figure 5.39 shows the rate at which Au is consumed at 125°C, 150°C and 165°C. The kinetics of Au consumed by SAC for thermal aging was computed to have a rate constant of $2.15 \times 10^{-1} \mu\text{m}^{-0.5} \text{s}^{-0.5}$ with an activation energy of 26.56 kJmol^{-1} . The rate at which Au was consumed in solid-liquid interdiffusion was at least two orders of magnitude higher than the Au consumption rate by diffusion in the solid near the melting point of SAC (217°C). This is similar to the studies of Au with near-eutectic

PbSn. Thus, it suggests a change in the kinetics and mechanism as we moves from a solid-liquid interdiffusion to a solid diffusion during aging.

Figure 5.38: Growth of intermetallic layers during aging at 125°C, 150°C and 165°C

Figure 5.39: Au consumption with square root of time during thermal aging at 125°C, 150°C and 165°C

5.5 COMPARISON BETWEEN THE KINETICS OF PbSn AND SnAgCu

Due to the complexity of various IMC layers interacting and growing at the interface of the diffusion barriers, the thickness of the Au consumption was used to estimate the rate of intermetallic growth. Figure 5.40 shows the total Au consumption for Au with PbSn and SnAgCu for the initial 1 second. It was observed that higher Au consumption was observed for PbSn than SnAgCu for a specific bonding temperature below 320°C. The difference in the Au consumption between PbSn and SnAgCu was lower as the temperature increased. As the temperature moved beyond 320°C, the Au consumption for SnAgCu overtook PbSn. This phenomenon differs from published reports that the increase in Sn content in SnAgCu causes more intermetallics formation [68,140]. This called for further analysis of the instantaneous Au consumption for the diffusion barrier and the rate of Au consumed by the diffusion kinetics.

Figure 5.40: Plot of the Au consumption of Au with molten PbSn and Au with molten SnAgCu for initial bonding of 1s at different bonding temperature.

As shown in Figure 5.41, the consumption of Au in SnPb is much higher than Au in SnAgCu. This phenomenon can be accounted by the kinetics at the solid-liquid interface. Upon Au contact with molten solder, the reaction and dissolution compete against each

other to consume Au. The Au dissolves and diffuses throughout the solder while the Au reacts to form intermetallics, which eventually nucleate heterogeneously to form the instantaneous diffusion layer. With a higher Sn content in molten SnAgCu solder, more Sn is available for reaction at the solid-liquid interface. This increases the rate of Au reacting to form the intermetallics, which easily nucleates rapidly to form the thermodynamic diffusion barrier. Thus, a thin diffusion barrier is observed for SnAgCu due to the increase in Sn content.

Figure 5.41: Estimation of Au consumption for the formation of instantaneous diffusion barrier with bonding temperature

With the formation of the diffusion barrier, the Au needs to diffuse through the diffusion barrier in order for it to dissolve into molten eutectic solder. The rate constant and the activation energy for Au to dissolve through the diffusion layer for molten SnPb are estimated to be $1.12 \times 10^3 \mu\text{ms}^{-0.5}$ and 22.26 KJ/mol respectively; while that of SnAgCu are estimated to be $2.45 \times 10^4 \mu\text{ms}^{-0.5}$ and 34.63 KJ/mol respectively. Figure 5.42 plots the rate of Au dissolving through the diffusion barrier for eutectic SnPb and SnAgCu with respect to temperature. It is shown that the rate of Au consumption dissolving through the diffusion barrier for SnAgCu is higher than that of SnPb. This is expected as the increase

in the Sn content promotes dissolution and reactions at the solid-liquid interface. The thin diffusion barrier also eases the diffusion mechanism through the diffusion barrier, which results in higher rate constant. The AuSn or combination of AuSn and AuSn₂ phases as the diffusion barrier for SnAgCu also resulted in higher and activation energy than AuSn₂ or AuSn₄ phases in SnPb. This agrees with the finding that AuSn has a higher activation energy [141] than diffusion barrier of AuSn₂ or AuSn₄ in Au-PbSn case [11].

Figure 5.42: Larger amount of Au consumed in molten for SnAgCu and PbSn through the diffusion barrier for different bonding temperature

From Figure 5.43, the PbSn consumes more Au than SnAgCu upon contact while Au dissolves faster into molten SnAgCu through the diffusion barrier. This is likely a result of the increase in Sn content for SnAgCu that promotes the formation of a thin diffusion barrier. Thus, it modifies the behaviour of the diffusion barrier formation and the rate of Au diffusing through the barrier. As the Au consumption through the barrier is time dependent, Figure 5.43 plots the Au consumption thickness for the bonding temperature of 230°C and 260°C as a function of time. It can be observed that at initial bonding, PbSn has a higher Au consumption than in the SnAgCu. With time, the amount of Au consumed by SnAgCu overtook PbSn. The result agrees with literatures that higher Sn

content will result in higher Au consumption in reflow soldering process. The initial kinetics in solid-liquid interdiffusion appears to differ with increased in Sn content.

Figure 5.43: The Au consumption of Au with SnAgCu overtakes Au with PbSn due to the increase in the diffusion kinetics with time.

In solid diffusion, k_0 and Q with eutectic solder are found to be $0.528 \mu\text{ms}^{-0.5}$ and 13.81 KJ/mol respectively. In the same temperature range, the k_0 and Q for Au with SnAgCu are found to be $21.5 \mu\text{ms}^{-0.5}$ and 26.56 KJ/mol respectively. The Au consumption thickness with respect to the bonding temperature is plotted in Figure 5.44. It is noted that SnAgCu consumes more Au than the eutectic PbSn. Thus, it suggests that more IMC will be formed in SnAgCu than SnPb for solid diffusion. This may be a result of the increased in Sn content, which promotes more diffusion in thermal ageing. Thus, a higher rate constant is observed for SnAgCu than in PbSn. Higher activation energy is also computed for SnAgCu than PbSn. This discrepancy is likely caused by the different IMC layers in-between the Au-SnAgCu and Au-PbSn interconnect systems.

Figure 5.44: Larger amount of Au consumed in solid diffusion in SnAgCu and PbSn solder

5.6 SUMMARY ON THE KINETIC STUDIES

The studies suggest that when Au comes in contact with molten solder for SLICF bonding, Au will dissolve and react instantaneously with molten solder. This forms an instantaneous diffusion barrier as Au continues to dissolve into molten solder. At the interface, the saturated solution forms favourable thermodynamic phases, which can be predicted by the binary section of the ternary Au-PbSn phase diagram. The first thermodynamic phase is expected to form at the bond interface by reaction mechanism as the dissolution reached a certain concentration on the isothermal line. The Au-Sn thermodynamic phases then precipitated and nucleated heterogeneously and grew into a diffusion barrier layer. The diffusion barrier was formed instantaneously as the Au competes to dissolve into molten solder.

As the diffusion barrier is formed, the kinetics changes, as Au needs to diffuse through the barrier before dissolving into molten solder. This barrier retards the rate of Au dissolving into molten solder. The Au/Au-Sn and the Au-Sn diffusion barrier/solder

interfaces move inward as Au continues to dissolve into solder as per Kidson interdiffusion model. These interfaces move with a $t^{0.5}$ relationship with reference to the Matano interface. The thickness of the Au-Sn diffusion barrier also grows with a time exponential of 0.5. The two-stage kinetics was verified for Au with molten PbSn where the initial stage involves instantaneous dissolution and formation of a diffusion barrier followed by the diffusion kinetics of Au dissolving through the diffusion barrier. This can be quantified by expressing the Au consumption as a linear function of $x = d_o + k_o \exp\left(\frac{Q}{RT}\right)t^{0.5}$ where d_o follow an empirically linear equation with temperature (i.e. $0.094T - 42.84$) while k_o and Q are computed as $1.12 \times 10^3 \mu\text{ms}^{-0.5}$ and 22.26 KJ/mol respectively.

The Au diffuses through the diffusion barrier and dissolves into molten solder either through dissolution or spalling from the diffusion barrier. Simultaneously, it also reacts and increases the growth of the diffusion barrier. Due to high diffusivity of Au, the dissolved Au diffuses throughout solder in an attempt to lower the system energy. During cooling, the saturated solution then precipitates as needle-like AuSn_4 phases throughout the solder. The amount of Au dissolving into solder is significant and needs to be accounted for in solid-liquid interdiffusion. In solid diffusion of Au-PbSn, the growth kinetic is found to be dependent on the neighboring IMC layer and suggest that Au consumption as a better yardstick to quantify its kinetic. A rate constant of $0.521 \mu\text{ms}^{-0.5}$ and 13.81 KJmol^{-1} was computed for Au-PbSn in a temperature of 125°C to 165°C . The kinetics of Au consumed by Pb-Sn under thermal aging was found to be two orders of magnitude slower than solid-liquid inter-diffusion.

The microstructures and kinetics of Au with SAC under solid-liquid diffusion and thermal aging were studied. Different Au-Sn phase morphologies were strongly dependent on the bonding temperature. At 230°C , only AuSn_2 and AuSn_4 were found at the interface layer

with precipitation of AuSn_4 phases in SAC. An additional of AuSn phase appears at the interfacial interface with AuSn_2 spalling off from the interface for 260°C and 290°C . During solidification, segregation of AuSn_2 and AuSn_4 were observed due to non-equilibrium cooling. The rate of individual IMC layer's growth during solid liquid inter-diffusion was found to be intricate due to competing reaction and dissolution mechanism. The Au consumption was adopted to quantify the kinetic of Au in molten SnAgCu and found to agree with the proposed two stages kinetics. It was found that the rate of Au consumed obeyed an Arrhenius relationship with a $t^{0.5}$ relationship. The activation energy and the rate constant of Au with molten SAC were estimated to be 34.63 KJmol^{-1} and $2.45 \times 10^4 \mu\text{ms}^{-0.5}$ respectively. The kinetics of Au consumed by SAC under thermal aging was found to be two orders of magnitude slower than solid-liquid interaction with a rate constant of $21.5 \mu\text{ms}^{-0.5}$ and activation energy of 26.56 KJmol^{-1} .

From the studies, it was concluded that in solid-liquid diffusion, the reaction kinetics dominates with the diffusion kinetics kicking in with time as Au dissolves through the diffusion barrier. Thus, the increases in Sn content for SnAgCu promotes the formation of a thinner thermodynamic diffusion barrier with a rapid diffusion kinetics than eutectic PbSn. This also explains that the initial kinetic of Au-SAC is slower than Au-PbSn and with time, the Au-SAC kinetic overtakes Au-PbSn kinetic in reflow soldering.

CHAPTER 6

QUALITY AND RELIABILITY ASSESSMENTS

The joint-in-via architecture on the flexible substrate delivers high routing density and fine pad pitch suitability for flip-chip applications. Its pad pitch for flip-chip is improved through the removal of soldermask and the use of laser ablation techniques in reducing the inter-via spacing. This architecture enables a fine pad pitch capability of 70 μ m pitch that satisfies the flip-chip pitch requirements up to the year 2018. Together with SLICF bonding, it offers a fluxless flip-chip bonding for the wide applications of electronics and MEMs packaging. This chapter focuses on the assessing its assembly robustness and the material characterization to select the best material candidates for packaging and joint reliability assessment with the joint-in-via architecture.

6.1 EXPERIMENTAL PROCEDURES

In order to verify the assembly robustness of SLICF bonding for a fine pitch application, a series of fifty gold studs with a tip diameter of 25 μ m were mechanically bumped on 8mm x 9mm aluminium metallized dies at a pad pitch of 150 μ m and 130 μ m. The bumps are then bonded to corresponding joint-in-via architectures on the substrate with a narrow 20 μ m inter-via spacing using eutectic 63Sn37Pb solder. A conventional lead-on-chip bonder with a $\pm 40\mu$ m accuracy was used for the flip-chip assembly. This experiment aims to verify the placement margin for flip chip assembly using the conventional die bonder. It also verifies the hypothesis that the joint-in-via architecture prevents solder bridging through its via cavity at a 20 μ m inter-pad spacing during assembly. A set of 100 units was assembled in each leg and assessed using an open-short test for the 50 joints on each die. An x-ray image was also taken to confirm the placement accuracy. Further SLICF bonding was also carried out with only local contact heating on the substrates for 30 units.

This is to assess the applicability of this bonding technique for heat-sensitive devices such as optical and micro-electro-mechanical systems. The continuity of the joints is used as a yardstick for assessment.

A new FC-CSP has evolved with the SLICF bonding on the joint-in-via architecture for flip-chip packaging on flex. In order to characterize the reliability of the joint-in-via architecture, material characterizations were carried out to select flex and underfill materials for FC-CSP. The characterisation of the flex materials include their flex materials properties, their moisture absorption content and their copper peel strength. Flex properties such as degradation temperature, flexure modulus, T_g , and CTE were captured with the use of thermal analysis tools. The flex were subjected to 25°C/60%RH for 125 hrs and simple weight gain analyses were performed to characterize their moisture absorption properties. A simple shear test was also performed to assess the flex adhesion strength with copper. This was done by shearing thirty 0.4mm eutectic solder balls on a 0.35mm pad defined ball structure on the flex.

As the joint strength is weak due to intermetallic formation, underfill is necessary to encapsulate the joints between the die and the flex. To obtain a good package performance for assessment, a good interfacial adhesion between the underfill and the flex material is desired. The adhesion strength between the flex and the underfill materials were assessed with the use of two conventional underfill materials (UF1, UF2) and two nonflow underfill (NF1, NF2) materials. The die shear tests were performed at room temperature and 100°C for comparison.

With proper material characterization, a 128Mb SDRAM in a 8mm x 9mm CSP package with a die pitch of 130µm was used to assess the reliability of the joint-in-via architecture.

The best candidate flex material was routed with a 35 μ m/35 μ m line/space design rule and a series of 110 μ m diameter via was generated for package assessment. The bumped die was then assembled using a lead-on-chip bonder with eutectic solder in the micro-via of the flex. The die was then assembled with the recommended underfill material and subjected to a series of reliability tests, as shown in Table 6.1. These reliability tests are base on JEDEC industry standard. Each test consists of 15 units for reliability assessment using open short test as a yardstick for failure.

Table 6.1: Reliability assessment based on continuity resistance and C-sam for 8mm x 9mm package for Au-PbSn

No	Test Description
1	MST L2 85°C/60% RH with 3IR reflow 260°C based on J-STD-020
2	MST L3 30°C/60% RH with 3IR reflow 260°C based on J-STD-020
3	Temperature cycling condition A –40 to 85°C for 1000 cycles based on EIA/JESD22-A105-B
4	Temperature cycling condition B –40 to 125°C for 1000 cycles based on EIA/JESD22-A105-B
5	Thermal Shock Condition D –65 to 150°C for 700 cycles based on JESD22-A106-A
6	Accelerated Moisture Resistance – Unbiased autoclave condition C 121°C/100% RH 96hrs based on JESD22-A102-B

The joints integrity is significantly affected by the growth of the intermetallic, and thus the joint-in-via architecture using Au-PbSn and Au-SnAgCu need to be further assessed. A series of shear tests was done on thirty bonded dies for Au-PbSn and Au-SnAgCu. This is to characterize their mechanical strength. The shear strength obtained were then normalized with the cross sectional area of the joints for comparison. Thermo-mechanical stresses using a T/C B condition of –40 to 125°C based on EIA/JESD22-A105-B was used to assess their fatigue life. 10 units of Au-PbSn and Au-SAC with similar

configuration were subjected to the testing condition and the joints resistance monitored at every 250 cycles until they are opened. Failure analysis was done to identify the location of the failures. Cross-sections were carried out at the failure regions. Macroscopic and morphology analyses were performed on these failure joints to understand their failure mechanisms.

6.2 ROBUSTNESS OF FLIP-CHIP ASSEMBLY

A 100 percent and 99 percent assembly yield was achieved in the assembly for a pad pitch of 150 μm and 130 μm respectively. Figure 6.1 shows the planar view using x-rays of a unit after assembly using an existing lead-on-chip bonder. The x-ray image at 150 μm pitch confirms the claim that the joint-in-via architecture was sufficiently to accommodate the die placement accuracy of a conventional die bonder for flip chip packaging. This is not achievable in conventional pad architecture. The assembly robustness of the JIV eases the dilemma of specific infrastructure for flip chip packaging. The throughput for flip chip assembly using existing die bonder is two times faster than a flip-chip bonder. The time saving is derived from the removal of the fluxing station as well as the time saving from the precise alignment through the vision system.

A 1 percent assembly drop was observed for the 130 μm pitch assembly. This drop in assembly yield is significant and suggests that 110 μm via size is at the cliff for flip-chip assembly using the lead-on-chip bonder. This experiment also demonstrated that the joint-in-via architecture enables a robust assembly yield by arresting solder wicking and preventing solder bridging during SLICF bonding at an inter-pad spacing of only 20 μm . An inter-pad spacing of 20 μm is not achievable in conventional flip-chip soldering because of design, substrate and assembly challenges.

Figure 6.1: X-ray pictures illustrating stud bump (black dot) aligned onto via architecture (circular ring) using lead-on-chip bonder

In the bonding assessment for heat sensitive devices, a 100 percent assembly yield was collected for the 30 units. This demonstrates the feasibility of using SLICF bonding as a heat isolation bonding for heat-sensitive devices such as optical and MEMS devices for bonding. This further encourages the use of the bonding technique for wider adoption of flip-chip technologies.

6.3 MATERIAL CHARACTERIZATION

6.3.1 Flex Material Characterization

The data obtained is summarized in Table 6.2. Different polyimide materials tested had distinct property differences. In TGA, the adhesiveless Flex A and Flex B had a higher degradation temperature, enabling the interposer to process up to 400°C. The T_g of flex is approximately 300°C, which is higher than the assembly processing temperature and reliability testing conditions. Hence, CTE2 can be ignored in the material selection criterion. By comparison of CTE1, adhesiveless Flex A and C are preferred as they offer a lower packaging stress.

Table 6.2: Flex material properties from thermal analysis

Flex Material		Flex A	Flex B	Flex C
DMA	Storage Modulus (MPa)	4000	4592	5750
	T_g (°C)	315.4	402.3	344.0
TGA	Degradation Temp (°C)	490.4	478.1	392.1
TMA	CTE1	23.2	33.7	10.1
	CTE2	366.5	525	16.8

Flex packages are known for their poor moisture performance. Therefore, a simple weight gain analysis was done to identify the lowest moisture absorption of flex material. The result obtained is summarized in Figure 6.2. Among the materials tested, adhesiveless Flex A and C offered a lower moisture saturation point with higher diffusivity. Thus, Flex A and C were preferred because of the lower moisture content absorbed by the package.

Figure 6.2: Weight gain analysis on different flex materials

The shear test data is presented in Figure 6.3. Flex A and C offered a higher copper adhesion strength than Flex B. All flex materials failed at the copper and flex interfaces. This set of data agreed with the material supplier's data sheet.

Figure 6.3: Adhesion strength of copper foils with flex materials

6.3.2 Underfill Characterization

At room temperature, the non-flow underfill exhibited higher adhesion strength but upon the application of heat, there was a distinct reduction in adhesion strength. The predominant cohesive failure mode at room temperature had also shifted to adhesive-cohesive mixed mode. This may be due to the weakening of the high epoxy resin in the non-flow underfill. Due to the drastic changes in the strength and failure modes for non-flow underfill, heat die shear strength was used as criteria for material selection. The heated die shear strength data with the flex materials is presented in Figure 6.4. In general, UF1 demonstrated higher adhesion strength with cohesive failure mode for all the flex materials tested. Therefore, conventional underfill UF1 on Flex A was selected for joint reliability assessment.

Figure 6.4: Interfacial adhesion strength assessment between underfill and flex materials using heated die shear test

6.4 JOINT RELIABILITY ASSESSMENTS

Conventional underfill material UF1 on Flex A was selected for joint reliability assessment. Figure 6.5 shows the FC-CSP package after assembly. A package height of 0.6mm was obtained with the use of 0.25mm die thickness for reliability assessment.

Figure 6.5: A new FC-CSP package using joint-in-via architecture

Table 6.3 summarizes the reliability data obtained for the FC-CSP using Au-PbSn. The joint survived JEDEC thermal cycling condition B and thermal shock condition D for

1,000 and 700 cycles respectively. This demonstrates the robustness of the joint-in-via architecture against thermal stress. With proper material selections, the FC-CSP package achieved MST L2 and passed the autoclave test condition C. The FC-CSP proved assembly robustness and passed the standard reliability test requirements.

Table 6.3: Package reliability tests based on resistance and C-sam for 8mm x 9mm packages.

No	Test Description	Reliability Result
1	MST L2 85°C/60% RH with 3IR reflow 260°C based on J-STD-020	0/15
2	MST L3 30°C/60% RH with 3IR reflow 260°C based on J-STD-020	0/15
3	Temperature cycling condition A –40 to 85°C for 1000 cycles based on EIA/JESD22-A105-B	0/15
4	Temperature cycling condition B –40 to 125°C for 1000 cycles based on EIA/JESD22-A105-B	0/15
5	Thermal Shock Condition D –65 to 150°C for 700 cycles based on JESD22-A106-A	0/15
6	Accelerated Moisture Resistance – Unbiased autoclave condition C 121°C/100% RH 96hrs based on JESD22-A102-B	0/15

The joint-in-via architecture enhances the joint reliability by increasing the overall joint standoff through embedding the joints in the micro-vias as shown in Figure 6.6. This helps to enhance the joint reliability without compromising the package height and passed the standard reliability tests.

Figure 6.6: Cross-section of the FC-CSP using joint-in-via architecture.

6.5 COMPARSION BETWEEN Au-PbSn AND Au-SnAgCu JIV

6.5.1 Mechanical assessment

The normalised strength of the joint is then tabulated in Figure 6.7. Au-SAC recorded a higher shear strength than Au-PbSn. Similar trend of SAC having a better shear strength than SnPb was reported by Frear et al. [105]. The shear failure occurred at the joint interface as shown in Figure 6.8. The shear failure of Au-PbSn produced a relatively smooth and dull surface at the intermetallic and solder interface. It appeared as a ductile failure mode. For Au-SAC, a brittle failure mode appeared in-between the intermetallics. This may be a result of a significantly higher intermetallic regions formed during the SLICF bonding of Au with SnAgCu.

Figure 6.7: Au-SAC with a higher normalized shear strength than Au-PbSn

Figure 6.8: Failure mode of Au-PbSn and Au-SAC observed under shear test

6.5.2 Thermo-mechanical assessment

Figure 6.9 shows the Weibull plots of Au-PbSn versus Au-SAC for T/C B condition. In the plot, the lifetime parameter η' represents the characteristic life at which 63.2 percent of the samples show failures while shape parameter β' gives the slope of the graph and measures how the failure frequency is distributed around the average lifetime. It is observed that Au-SAC has η' of 973.1 hours (1500 cycles) with a β' of 9.923, while Au-SnPb has η' of 1524 hours (2285 cycles) with a β' of 5.443. This data suggests that the average lifetime of Au-SnPb is about 550.9 hours better than Au-SnAgCu. The Au-SAC has a bigger spread around the average lifetime than Au-SnPb. From the data, the first failure in Au-SAC occurs at about 800 hours while Au-PbSn has a slightly better performance with first known failure at about 900 hours.

Figure 6.9: Weibull plot of Au-PbSn and Au-SAC

As expected, the joint at the extreme corner of the package failed. This coincides with the largest stress where the DNP is largest. Macroscopic analysis on the failure mode for Au-PbSn and Au-SAC also revealed cracks between the AuSn_2 and the solder matrix containing AuSn_4 precipitated as shown in Figure 6.10 and Figure 6.11 respectively. The

failure mode suggests a weak interface exist between the AuSn_2 and the solder matrix. Since both Au-PbSn and Au-SAC have the same interface morphologies after processing, both Au-PbSn and Au-SAC have almost a similar number of cycles of T/C B condition before the first failure. As Au has better wetting behavior on PbSn than SAC, the contact between Au-PbSn is much gentle and thus reduces stress concentration. Together with a significantly less intermetallic component than Au-SAC, Au-PbSn offers a better joint reliability margin than Au-SAC.

Figure 6.10: Failure mode of Au-SnPb occurs in-between the AuSn_2 and the solder matrix

Figure 6.11: Failure mode of Au-SnAgCu occurs in-between the AuSn_2 and the solder matrix

6.6 SUMMARY ON RELIABILITY AND QUALITY ASSESSMENTS

The joint-in-via architecture provides additional mileage for organic substrates to be used for flip-chip packaging. At a pad pitch of $150\mu\text{m}$, the joint-in-via architecture offers a

sufficient pad width for robust assembly process using a conventional die bonder at 40 μ m placement accuracy. The joint-in-via architecture is also proven to prevent solder bridging with a narrow inter-pad spacing of 20 μ m during flip-chip assembly. The SLICF bonding on the joint-in-via architecture also enables heat isolation for flip-chip bonding for heat sensitive devices.

A new FC-CSP using flex has evolved with the use of the joint-in-via architecture. The material characterization identified Flex A with UF 1 as the best material candidate for assessing the joint reliability. Adhesiveless Flex A is selected as it offers a lower moisture absorption with good adhesion strength with underfill material UF1. With proper material characterisation, the joint-in-via architecture using Au with eutectic solder passes the standard reliability tests such as T/C B, T/S D, MST L2 and Autoclave. This reveals the potential of the joint-in-via architecture for flip-chip assembly.

The mechanical strength of Au-SnAgCu is higher than the Au-PbSn for SLICF bonding on the joint-in-via architecture. However, in thermo-mechanical assessment by thermal cycling, the Au-PbSn provides a better reliability margin due to a preferred joint architecture and less intermetallics as compared to Au-SAC.

CHAPTER 7

CONCLUSION AND RECOMMENDATIONS

7.1 CONCLUSION

An evolutionary approach using the joint-in-via architecture has been proposed and conceptualized to meet the pad pitch challenge for flip-chip packaging. The joint-in-via architecture consolidates the landing pads, micro-vias, and flip-chip joint into one common element, thereby saving valuable substrate area for high-density routing. This approach overcomes the challenges by shifting the current copper pad designs to the micro-via architecture using existing substrate technologies. The pad pitch resolution is improved through the elimination of soldermask and reduction of inter-pad space using the laser micro-via technologies. As the pitch now relies on the micro-via, it removes the dependence of the pad pitch design rule to the finished copper thickness.

Through the assessment of different micro-via techniques on different organic materials, laser ablation on polyimide is identified as the best candidate for the generating of the joint-in-via architecture. The joint-in-via architecture is enabled with this micro-via technique down to 70 μ m pitch with a flip-chip receiving via pads of 50 μ m on a polyimide flex. This pad pitch is more superior than the advanced copper metallization technologies such as semi-additive and half-etching technologies. An innovative solder bumping through the use of micro-via as apertures has achieved a good bump coplanarity of 4 μ m or $\pm$ 5% for flip-chip bonding. The bumped micro-via conceptualizes the joint-in-via architecture at fine pitch in elimination of the costly RDL process.

Conventional soldering on the joint-in-via architecture is not compatible with the JIV architecture due to its wetting properties. A physical separation exists between Au stud

and solder bump due to solder wicking between offset bumps. In thermocompression bonding, the increase in temperature softens the solder, thereby allowing the Au stud to plastically deform the solder. This action breaks the oxide layer at contact zones and promotes thermal diffusion to form multiple micro-welds of Au-Sn intermetallic regions. These joints are weak and unable to withstand the material mismatch during cooling.

An instantaneous fluxless bonding on the JIV is achieved using solid-liquid interdiffusion bonding by compressive force (SLICF). It uses a mechanical force to break the oxide layer and overcome the surface tension of the molten solder. Once inserted, the submerged body interacts with fresh solder to form bonds by solid-liquid interdiffusion. The bonds are then mechanically interlocked upon cooling. This new fluxless bonding technique does not rely on its wetting behaviour, thus allows instantaneous soldering, and thereby eliminates the need of fluxing and reflow process. Due to its poor wetting behaviour, the buoyancy of the molten solder and the weight of the insertion body tend to “reject” the insertion; therefore, a sufficiently deep submerging is necessary to achieve good joints at a particular temperature. This bonding method is applied successfully on the JIV substrate architecture.

The Kidson’s three phase model is used to describe the solid liquid kinetics of Au with eutectic solder. The kinetics and thermodynamic studies of Au with molten eutectic PbSn reveal different Au-Sn intermetallic layer at different bonding temperatures. This can be determined through the concept of local equilibrium by using the binary section of the ternary Au-Pb-Sn phase diagram. At 190°C, a continuous AuSn_4 intermetallic layer is formed with needle-like AuSn_4 precipitated in the bulk solder. At 230°C and 260°C, a new intermetallic layer of AuSn_2 is observed with rod-like regions of AuSn_4 precipitated in the bulk solder.

In avoidance of saturation at the interface, the dissolved Au diffuse throughout the rest of the solder while the IMCs nucleate heterogeneously and grow into a diffusion layer. The formation of the diffusion barrier retards the rate of Au dissolving into molten solder. Using kinetics and thermodynamic principle, the AuSn_2 and AuSn_4 are identified as the diffusion barrier for 190°C and $230 - 260^\circ\text{C}$ respectively. Due to the complex interactions at the interface and Au continues to dissolve into molten solder, the Au consumption is recommended as a better yardstick to quantify the kinetics of solid-liquid inter-diffusion. The kinetics can be estimated by a two-stage kinetic. The initial stage involves the instantaneous dissolution and formation of a diffusion barrier followed by the diffusion kinetics of the Au dissolving into the molten solder through the diffusion barrier. The kinetic of Au with molten eutectic solder is measured by the Au consumption which can be expressed as $x = d_o + k_o \exp\left(-\frac{Q}{RT}\right)t^{0.5}$, where d_o follows an empirically linear equation with temperature (i.e. $0.094T - 42.84$) while k_o and Q are computed to be $1.12 \times 10^3 \mu\text{ms}^{-0.5}$ and 22.26 KJ/mol respectively. At 230°C to 260°C , the AuSn_2 diffusion barrier interfaces are found to move with $t^{0.5}$ as governed by the Kidson interdiffusion model. This finding agrees with Kidson model and verifies the two-stage kinetics of solid-liquid interdiffusion. In solid diffusion, k_o and Q for the Au consumption in the eutectic PbSn solder is found to be $0.528 \mu\text{ms}^{-0.5}$ and 13.81 KJ/mol respectively. The rate of Au consumption by solid-liquid interdiffusion is at least two orders of magnitude higher than the solid diffusion.

In Au-SAC study, the different Au-Sn phase morphologies are strongly dependent on the mounting temperature. AuSn_4 phases are found throughout the SnAgCu with AuSn_2 and AuSn_4 presence at the interface layer for 230°C . At 260°C and 290°C , an additional AuSn layer appears at the interfacial interface. Segregation of AuSn_2 and AuSn_4 are observed

due to non-equilibrium cooling. With similar interactions of Au with PbSn, the Au consumption are measured and found to agree with the two-stage kinetics for solid liquid interdiffusion. The d_0 for Au-SAC can be expressed by $0.032T-15.56$ with k_0 and Q estimated as $2.45 \times 10^4 \mu\text{ms}^{-0.5}$ and 34.63 KJ/mol respectively. In solid diffusion, k_0 and Q for Au consumption in SnAgCu is found to be $21.5 \mu\text{ms}^{-0.5}$ and 26.56 KJ/mol respectively. The Au consumption by solid-liquid interdiffusion for SnAgCu is also at least two orders of magnitude higher than the solid diffusion. The comparison studies between Au-PbSn and Au-SnAgCu shows that the initial kinetic of Au-PbSn is faster than the Au-SnAgCu in solid-liquid interdiffusion. This phenomenon is caused by the erection of a thin diffusion barrier due to the abundant Sn availability in SnAgCu. This thin barrier helps to slow down the initial kinetic of Au but eases the Au in diffusing through the diffusion barrier and dissolving into molten SnAgCu. Thus, with time, the kinetics changes with Au consumption of Au-SnAgCu overtaking PbSn.

Actual SLICF bonding on the joint-in-via architecture demonstrates that it allows a robust assembly with only $20\mu\text{m}$ inter-pad spacing. For a current pad pitch of $130\mu\text{m}$, the joint-in-via architecture enables a flip-chip assembly using conventional die bonder. This fluxless SLICF bonding technique is found to be applicable to heat-sensitive devices through local heating. The joint-in-via architecture passes reliability tests such as T/C B, T/S D, Autoclave C and MST L2 conditions as governed by the JEDEC specification. The Au-PbSn interconnect system has a better joint reliability than Au-SnAgCu due to its joint geometry and lower kinetics in the formation of brittle intermetallics.

The fluxless SLICF bonding on the joint-in-via architecture offers a fine pitch solution using the micro-via technologies on organic substrate. This eliminates the need of RDL and encourages a wide adoption of flip-chip technologies in microelectronics,

optoelectronic and micro-electro-mechanical systems. A summary of the achievement is presented in Figure 7.1. All publications are listed in the Appendix for reference.

7.2 RECOMMENDATIONS

The SLICF bonding on the joint-in-via architecture has been successfully demonstrated in this study. This study has shown that there are several technology gaps that call for further research. The recommendations are categorized into three main areas as follow:

- Applications of the SLICF bonding
- Verification of the solid-liquid kinetic models
- Reliability enhancement through finite element modeling

Applications of the SLICF bonding for the different interconnect systems need to be assessed inclusive of the joint reliability. The drive is to enhance the joint reliability without the formation of extensive intermetallics by Au and Sn based solders. Further research works include assessing the SLICF bonding for different Sn based solders with Ni and Au flash over Cu studs. The use of the Cu bumps help to reduce the rate of interdiffusion with Sn as compared to Au. Thus, it may help to enhance the joint reliability. The drives for a green packaging solution also motivates the study of the Cu stud with lead free solders such as SnAg, SnAgCu, SnCu etc.

The kinetic models of solid-liquid interdiffusion may need further verification. This can be achieved by generating the quaternary phase diagram of Au-SnAgCu through the use CALPHAD (Computer Coupling of Phase Diagrams and Thermochemistry). Alternatively, a known binary phase system such as Au-Sn can be used to verify the solid-liquid kinetic models. The local equilibrium at the interfaces can be verified by the phase morphologies formed at the interface for different bonding temperatures. Further

verification includes the formation of the diffusion barrier at the solid liquid interface based on the available phase diagrams as governed by the thermodynamics principle. The kinetics of Au in Sn also helps to verify the two-stage kinetics. This can be quantified by the amount of Au consumption and verified that it follows a $t^{0.5}$ relationship after the formation of the diffusion barrier. Further verification includes the continuous diffusion of Au through the diffusion layer and into the molten solder. The Au-Sn study also provides further evidences that the increase in Sn content promotes rapid interactions, resulting in more intermetallic regions being formed.

The preliminary reliability analysis reveals that the amount of intermetallics and the joint geometry weaken the joint. Finite element modeling should be extended to study the effect of the joint geometry to its reliability. Variables such as stud base, stud height, stud diameter, contact angle between the stud and solder, insertion depth etc should be included in the study. A parametric study is also recommended to capture the response of the different package materials and its package geometries to the joint-in-via architecture. This includes assessing the impact of the die size, die thickness, underfill gap, underfill materials, substrate materials, etc on the joint integrity. To make the simulation model more accurate in its prediction, the growth of the intermetallic layers and their properties should also be included in the finite element model.

These recommended research areas will help to enhance the joint-in-via reliability for a wider adoption of the flip-chip technology. The in-depth understanding of its kinetics at the solid-liquid interface and the joint reliability through the finite element modeling will enhance the joint-in-via architecture for flip-chip advancement.

Figure 7.1:Summary of the project achievements

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APPENDIX

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5. T.K Lee, Sam Zhang, C.C. Wong, A.C. Tan (2006). Fluxless Flip Chip Bonding with Joint-in-Via Architecture. Journal of Thin Solid Film. (504): 436-440
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