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**NANYANG
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**SCHOTTKY BARRIER ENGINEERING ON DOPANT-
SEGREGATED SCHOTTKY SILICON NANOWIRE
MOSFETs**

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING
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SCHOTTKY BARRIER ENGINEERING ON DOPANT- SEGREGATED SCHOTTKY SILICON NANOWIRE MOSFETs

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ABSTRACT

Silicon nanowire with Gate-All-Around architecture is considered as one of the most promising candidates for CMOS scaling beyond 11 nm technology node due to its superior gate to channel electrostatic control. However, due to the one dimensional nature of nanowire, the resistance at the nanowire source/drain (S/D) extension is inherently high. Nickel silicide (NiSi) Schottky S/D is introduced to address this issue. 2 potential challenges associated with NiSi Schottky S/D are: (1) rapid NiSi intrusion into the silicon nanowire channel during silicidation and (2) the existence of a Schottky barrier which leads to increased contact resistance.

In this work, to address issue (1), a two-step rapid thermal annealing (RTA) silicidation was introduced to control the NiSi intrusion into nanowire. TEM imaging was used to characterize intrusion lengths into silicon nanowires. A low temperature first RTA was found to be desirable to control the intrusion length while the Ni thickness was a less critical factor if the proposed first RTA was employed. Consistency in electrical characterization of the devices suggests that the intrusion length using the two-step RTA is indeed repeatable.

To address issue (2), dopant segregated Schottky (DSS) contact was employed. By using silicidation induced dopant segregation (SIDS), boron or phosphorus was implanted into the S/D before silicidation took place to segregate the dopants at the NiSi/Si interface through a phenomenon known as 'snow plow'. The fabricated DSS nanowire MOSFETs demonstrated good electrical characteristics with high drive currents

and low leakages, as well as improved short channel effect immunity compared to its conventional counterpart.

The low temperature (450 – 550°C) activation of the segregated dopants at the NiSi/Si interface has long been attributed to the generation of intrinsic point defects during silicidation. Based on this hypothesis, excimer laser annealing (ELA) was utilized to introduce additional point defects prior to silicidation on doped silicon for an enhanced segregation. Indeed, photoluminescence results on ELA samples showed higher defects density counts. After silicidation, it was found that the segregation concentration at the interface increased by 2 to 3 multiples where the ELA was employed. Electrically, back contacted diodes with the ELA also demonstrated superior ohmic contacts to the ones without. Finally, the ELA method was integrated into DSS nanowire MOSFETs. The DSS devices with the ELA method exhibited improved electrical characteristics than the control DSS devices. The improved electrical performance was attributed to the higher segregation level at the metal-semiconductor junction which substantially reduced the effective Schottky barrier height at the junction.

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2. G. Zhu, X. Zhou, Y. K. Chin, K. L. Pey, J. Zhang, G. H. See, S. Lin, Y. Yan, Z. Chen, "Subcircuit compact model for dopant-segregated gate-all-around Si-nanowire MOSFETs", *IEEE Transactions on Electron Devices*, vol. 57, n 4, p 772-781, April 2010.
3. E. J. Tan, K. L. Pey, N. Singh, G. Q. Lo, D. Z. Chi, Y. K. Chin, K. M. Hoe, G. Cui, P. S. Lee, "Demonstration of Schottky barrier NMOS transistors with erbium silicided source/drain and silicon nanowire channel", *IEEE Electron Device Letters*, vol 29, n 10, p 1167-1170, 2008.

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2. Y. K. Chin, K. L. Pey, N. Singh, G. Q. Lo, G. Zhu, X. Zhou, X. C. Wang, H.Y. Zheng, L. H. Tan, "Excimer Laser-Annealed Dopant Segregated Schottky (ELA-DSS) Si Nanowire Gate-All-Around (GAA) pFET with Near Zero Effective Schottky Barrier Height (SBH)," *International Electron Devices Meeting*, p 935, 2009.
3. Y. K. Chin, K. L. Pey, N. Singh, W. J. Lu, G. Q. Lo, L. H. Tan, X. C. Wang, H.Y. Zheng, L. Chan, "Excimer Laser-Annealed Dopant Segregated Schottky (ELA-DSS) Si Nanowire Gate-All-Around (GAA) pFET," *International Symposium on Integrated Circuits*, special session 9, B2-5, 2009.

Chapter 1 INTRODUCTION

1.1 Background

The semiconductor industry has been a successful one in the past in providing continued improvement in system performance that the Semiconductor Industry Association (SIA) has been publishing roadmaps for semiconductor technology since 1992 [1]. These roadmaps act as guides and present outlooks of industrial trends. The most significant guide for the roadmaps is perhaps the Moore's Law [2], which stated that the number of transistors on a chip is being quadrupled and the performance of the transistor is being doubled every three years. This phenomenon has been achieved in the past through scaling of physical dimensions of the metal-oxide-semiconductor field-effect transistor (MOSFET), hence gaining the density and speed. Over the past few decades, little changes had been introduced in the basic MOSFET design.

However, challenges arise as we approach smaller technology node. As conventional MOSFET scales beyond 65 nm technology node, it requires innovations in design to solve issues due to fundamental physics that imposes certain constraints. Perhaps the fundamental limits most cited [3-11] are 1) quantum mechanical tunneling of carriers through the thin gate oxide; 2) short channel effects; 3) statistical fluctuation in the number and location of dopant atoms in the MOSFET channel, and 4) increased parasitic series resistance due to ultra shallow junction significantly limits the gain by channel mobility enhancement techniques. All these fundamental limits have led to the

prediction of 22 nm technology node as the end of the semiconductor roadmap for conventional device architecture [12].

Due to severe short channel effects, MOSFET is losing its ability as a switching device due to strong electric field from the drain. In preserving the function of a MOSFET as a switching device, it is of utmost importance the gate remains as the terminal that controls the turn-on or turn-off characteristic more than the drain. This can be realized by having a strong gate electrostatic field on the channel. For conventional devices with a planar architecture, this means a constant scaling down of the gate dielectric thickness. However, the scaling of the gate dielectric will ultimately arrive at a fundamental barrier of a thickness of an atomic layer. Moreover, the quantum mechanical tunneling of carriers through the gate dielectric forms another challenge manifests as gate leakage and heat dissipation before the barrier of an atomic layer is reached.

Multiple gate MOSFETs have been proposed as a method to improve drive current, and to reduce short channel effects by enhancing transistor gate-to-channel coupling [13]. Examples of multiple gate MOSFETs include double gated FinFET [14], π -gated [15] and Ω -gated FETs [16]. MOSFETs with ultra-thin body (UTB) have also been proposed to provide improved electrostatic control of the channel [17]. It also relaxes the need for channel doping resulting in reduced short channel effects. Multiple gate FETs usually incorporate thin channel bodies with an increase in the effectiveness of electrostatic control with decreasing channel width and thickness.

A special example of combination of UTB MOSFET and a multiple gated FET structure is the gate-all-around (GAA) MOSFET in which the gate is completely surrounded by an ultra narrow Si nanowire channel [18]. This architecture provides the best possible electrostatic control resulting in greatly reduced short channel effects and

improved drive current. A schematic of a MOSFET having a GAA narrow channel body is shown in Figure 1.1.

Figure 1.1. Schematic of a generic multiple gated MOSFET with GAA structure and a nanowire channel.

However, there are some fundamental issues associated with nanowire transistor. The external series resistance is one of them due to its very narrow source and drain contact to the nanowire channel. The schematic shown in Figure 1.2 (b) is along AA' in the SEM micrograph shown in Figure 1.2 (a) where the external resistance consists of several parts: 1) source/drain extension (SDE) resistance under the spacer (R_{SDE}), 2) nanowire curved extension resistance from the edge of the spacer (R_{curve}), 3) source/drain (S/D) sheet resistance (R_{sh}) and 4) metal to S/D contact resistance (R_{con}). For doped S/D nanowire FETs, the biggest challenge in the external resistance comes from R_{SDE} and R_{curve} due to their narrow dimensions of down to $\sim 10\text{nm}$. Recently, it is proposed that by metalizing the S/D to the edge of the spacers using thin silicide, the R_{con} and R_{curve} can be greatly reduced [19]. As shown in Figure 1.2 (c) the overall external resistance can be reduced and larger drive current can be obtained. However, R_{SDE} remains one unsolved challenge that seriously impacts the performance of a nanowire transistor.

Figure 1.2 (a) Top view SEM micrograph of a Si nanowire MOSFET. Schematics showing AA' cross-sectional view of (a) for (b) a doped S/D MOSFET and (c) a fully silicided S/D MOSFET.

Potential techniques such as dopant segregation with fully silicided S/D have been proposed to alleviate the R_{SDE} [20]. The dopant segregation effectively reduces the Schottky barrier height of the metallic S/D [21, 22]. This leads to very low S/D resistance, improved short channel effect immunity as well as enhanced carrier injection [23, 24]. This motivates us to integrate the dopant segregation technique with nanowire transistor.

Dopant segregation is piling up of dopants at the silicide/silicon interface during silicidation [25, 26]. Following electrical characterization of diodes formed by dopant segregation, the contacts are found to be ohmic which indicates low temperature dopant activation at the interface [27]. There is a lack of understanding of dopant activation mechanism during segregation but early work explored the possibility of point defects in affecting the activation at the interface [26]. Recently, it has been found that excimer laser annealing (ELA) can be used to generate defects in crystalline Si by rapid heating of the

Si beyond its melting point followed by a fast quenching back to ambient temperature [28]. These have led us to study the application of ELA in defect generation for dopant segregation.

1.2 Objectives

The project aims to study and analyze the effect of ELA on Schottky barrier Si nanowire MOSFETs with dopant segregation at the S/D. This will be achieved in the following 4 phases:

- 1) To fabricate fully silicided S/D Schottky barrier MOSFETs with Si nanowire as basic device architecture.
- 2) To investigate the effect of various silicidation parameters on the intrusion of silicide into nanowire channels of Si nanowire MOSFETs.
- 3) To study and analyze the electrical characteristics of the fabricated back contacted dopant segregated Schottky diodes and Si nanowire MOSFETs.
- 4) To incorporate ELA into the fabrication of dopant segregated Schottky diodes and Si nanowire MOSFETs and to investigate the effect of ELA on the electrical characteristics of the fabricated devices.

1.3 Scopes of the project

This project involves the understanding of dopant segregation as well as the important parameters that affect the segregation using exclusively nickel silicide for material studies as well as the S/D material for device fabrication. The silicide phase that is most desirable in this project is the nickel mono-silicide due to its lowest sheet resistance of all known nickel silicide phases.

Pulsed excimer laser was employed to study the effect of ELA on the Si substrate after implantation and various material characterization techniques were used to investigate the effect of ELA on the material properties. Defects are hypothesized to play an important role in the mechanism of dopant segregation. Hence, the effect of ELA on defect formation in the substrate was also investigated.

Si nanowire MOSFET as a basic device architecture was fabricated using top down CMOS technology. Transmission electron micrograph (TEM) was employed to study the intrusion of silicide into the nanowire channel to successfully fabricate fully silicided S/D nanowire MOSFETs for the subsequent electrical studies.

By using simulation of heat transfer in Si substrate, ELA with appropriate energy density or fluence was incorporated into the device fabrication to realize the generation of additional defects in the device S/D. This was followed by the electrical characterization and analyses to elucidate the effect of defect enhanced dopant segregation on device performance as well as the understanding of effective Schottky barrier height and its importance to Schottky barrier MOSFETs.

1.4 Organization of thesis

The organization of various chapters of this thesis is provided as follows.

Chapter 1 provides the introductory overview pertaining to the background and motivation of this project which leads to the definition of the objectives and scope of this project.

Chapter 2 gives a review covering the physics of Schottky barrier and the basic operating principles of the Schottky barrier MOSFET. In addition, the formation methodologies of silicon nanowires and their device applications are also discussed.

Chapter 3 describes the experimental methodology that includes experimental setup, sample preparation, device fabrication, materials and electrical characterization techniques used in this project.

Chapter 4 presents the investigation of nickel silicide intrusion into the channel of Schottky barrier Si nanowire MOSFETs.

Chapter 5 presents the material and electrical characteristics of dopant segregated Schottky diodes and Si nanowire MOSFETs. The concept of gate bias modulated effective Schottky barrier height is introduced to elucidate the electrical performance of the nanowire MOSFETs.

Chapter 6 presents the study of ELA induced defects in dopant segregation and its incorporation in device fabrication. The material and electrical characteristics of the fabricated devices are presented.

Chapter 7 summarizes the major results and findings in this project. Recommendations for future research direction based on the results of this project are also proposed.

Chapter 2 LITERATURE REVIEW

2.1 Schottky barrier

A Schottky diode is formed when a metal makes an intimate contact with a semiconductor where the Fermi levels in the two materials are aligned at thermal equilibrium. The potential barrier, i.e. the Schottky barrier formed at the metal-semiconductor (MS) interface can be identified in the energy diagram shown in Figure 2.1 for a Schottky diode formed on n-Si. According to Schottky and Mott, the SBH Φ_b can be defined as the difference between the metal work function (Φ_m) and the electron affinity (χ_s) of the semiconductor shown in Figure 2.1 and can be expressed as follows [29]

$$\Phi_b = \Phi_m - \chi_s. \quad (\text{Equation 2.1})$$

Figure 2.1. Φ_b band diagram of an arbitrary MS Schottky contact.

Note that the Φ_b is strongly influenced by the Fermi level pinning caused by metal-induced gap states (MIGS) or interfacial states such as dangling bonds and

impurities [30-32]. Under the influence of the Fermi level pinning, the general form of Φ_b is given by [33]

$$\Phi_b = \Phi_m - \chi_s + qV_{int} \quad (\text{Equation 2.2})$$

where V_{int} is the voltage drop accounted for the effect of dipoles and/or charge rearrangement between metal and semiconductor upon the formation of the interface, and q is the electronic charge.

The MIGS concept was first conceived by Heine who proposed that the wave function of electrons in the metal decaying into the adjacent semiconductor leading to forbidden gap states in the semiconductor [34]. Mönch explained that the dependence of the SBH of a MS junction could be calculated by adding a charge density caused by the MIGS into the charge neutrality equation across the junction as [30]

$$Q_m = Q_s + Q_{migs} \quad (\text{Equation 2.3})$$

where Q_m is the charge density on the metal side, Q_s is the semiconductor space charge density and Q_{migs} is the charge density caused by MIGS. Also, by assuming a charge neutrality level where the MIGS above and below this level are acceptor-like and donor-like, respectively, the SBH of any MS junction can be very well correlated with the electronegativity difference between the metal and the semiconductor. The relationship between the SBH and the electronegativity difference is given by

$$\Phi_b = \Phi_{CNL} + S_X(X_m - X_s) \quad (\text{Equation 2.4})$$

where Φ_{CNL} is the charge neutrality level, X_m and X_s denotes the electronegativity for the metal and the semiconductor respectively, and S_X is a fitting parameter called the slope parameter. The basic assumptions for this correlation with the SBH and the MS electronegativity difference are the MS junction must be intimately in contact, abrupt, defect-free, and laterally homogeneous.

Tung, on the other hand, proposed that chemical bonding to achieve thermodynamic equilibrium at the MS interfaces is the cause of Fermi level pinning [33, 35]. When a MS junction is formed, one can account for the chemical effect which takes place at the MS interface by assuming that the Schottky dipole can be identified with the polarization of the chemical bonds. By assuming a uniform density of chemical bonds, N_B , each with a dipole of $qx d_{MS}$ (q = electronic charge, x = normalized atomic energy-level mismatch and d_{MS} = distance between metal and semiconductor atoms at the interface) at the MS interface and an appropriate interfacial dielectric constant ϵ_{int} , the theory has a SBH in the form of

$$\Phi_b = I_S - \phi_M + \frac{q^2 x N_B d_{MS}}{\epsilon_{int}} \quad (\text{Equation 2.5})$$

Experimentally, the effect of interface structure has been observed as the dependence of the SBH on the epitaxial orientation NiSi₂. The morphology of the interface is also an important factor to consider in SBH measurements. Planar NiSi₂/Si(100) interfaces show a SBH which is significantly lower on *n*-type Si as compared to faceted, rough interfaces.

2.2 Carrier transport across a Schottky diode

The forward current of a Schottky diode can be modeled by a combination of carrier transport mechanisms across the MS junction. The carrier transport mechanisms are:

1. thermionic emission;
2. quantum mechanical tunneling; and
3. recombination of electrons or holes in the semiconductor space charge region.

In a high quality semiconductor with a very low density of defects, recombination of carriers within the space charge region can be neglected as it only contributes to a very small component of the overall current.

In a Schottky diode with a lowly doped semiconductor (N_A or $N_D < 10^{17} \text{ cm}^{-3}$), thermionic emission is the dominant transport mechanism. The equation governing the mechanism is given by [29]

$$I_{TE} = I_S \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (\text{Equation 2.6})$$

with

$$I_S = AA^{**}T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \quad (\text{Equation 2.7})$$

where I_S is the saturation current, V is the voltage across the diode, A is the Schottky diode area, A^{**} is the effective Richardson-constant, T is the temperature, k is the Boltzmann constant and n is the diode ideality factor. The ideality factor is defined as

$$n = \frac{q}{kT} \frac{\partial V}{\partial \ln(I_{TE})} \quad (\text{Equation 2.8})$$

The ideality factor is a measure of deviation of a Schottky diode from an ideal diode with $n = 1$. There are a few reasons that contribute to the deviation from an ideal diode. One of them is the existence of defects in the semiconductor that serve as generation and recombination sites of carriers. In a good quality semiconductor, this contribution should be small and often negligible. Another reason is the dependence of the SBH on the applied voltage. As the semiconductor doping increases, the Schottky barrier becomes thin enough such that quantum mechanical tunneling of carriers across the thin barrier is possible. In this case, the thermionic emission theory alone is not enough to describe the total current and the quantum mechanical tunneling component has to be accounted. The tunneling component has a form of [29]

$$I_T \propto \exp\left(\frac{-q\phi_b}{E_{00}}\right) \quad (\text{Equation 2.9})$$

with

$$E_{00} = \frac{q\hbar}{2} \sqrt{\frac{N}{\epsilon_{Si} m^*}} \quad (\text{Equation 2.10})$$

where $\hbar$ is the reduced Planck constant, N is the interfacial doping concentration, ϵ_{Si} is the Si dielectric constant and m^* is the carrier effective mass. Note that I_T increases exponentially with $\sqrt{N}$.

2.3 Capacitance-Voltage (C-V) Characteristics of Schottky Diode

The electrostatic analysis of a MS junction is required to obtain the C-V characteristics of the diode. The general analysis begins with the Poisson equation:

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\epsilon_s} = -\frac{q}{\epsilon_s} (p - n + N_D - N_A), \quad (\text{Equation 2.12})$$

where ϕ is the potential, ϵ_s is the semiconductor permittivity, q is the unit charge and the charge density, ρ , is a function of the electron density n , the hole density p and the donor N_D and acceptor densities N_A . A second order non linear differential equation can be obtained from Equation 2.12, which cannot be solved analytically. Instead, by making assumption that the depletion region is fully depleted and the adjacent neutral regions contain no charge, a simple analytic model can be obtained.

Based on the full depletion model, the capacitance per unit area of a Schottky diode on a p-type semiconductor is given by

$$\frac{C}{A} = \sqrt{\frac{\pm q \epsilon_s (N_A - N_D)}{2(\pm V_{bi} \pm V - \frac{kT}{q})}} \quad (\text{Equation 2.13})$$

where C is the junction capacitance, A is the junction area, V_{bi} is the built-in potential, V is the reverse-bias voltage applied across the Schottky junction, k is the Boltzmann constant and T is the temperature in Kelvin. The “+” sign applies to p-type and the “-” sign to n-type substrates. The kT/q in Equation 2.13 accounts for the majority carrier tail in the space-charge region which is omitted in the full depletion approximation. The built-in potential is related to the SBH by

$$\phi_b = V_{bi} + V_0, \quad (\text{Equation 2.14})$$

with

$$V_0 = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right), \quad (\text{Equation 2.15})$$

where N_C is the effective density of states in the conduction band. By plotting $1/(C/A)^2$ versus V , one obtains a curve with the slope $2/[q\epsilon_s(N_A - N_D)]$. The SBH can be determined from the intercept on the V -axis,

$$V_i = -V_{bi} + kT/q, \quad (\text{Equation 2.16})$$

and substituting V_{bi} from Equation 2.XX gives

$$\phi_b = -V_i + V_0 + kT/q. \quad (\text{Equation 2.17})$$

2.4 Schottky barrier MOSFETs

Several challenges are associated with the aggressive down scaling of conventional MOSFETs. One of the challenges is the S/D scaling, which include issues such as

1. requirements for ultra shallow S/D junction formation, which result in increasing of R_{sh} ,
2. the need for sharp lateral doping techniques to control the lateral steepness of the S/D extensions, and

3. thermal budget constraint in order to maximize dopant activation and minimize dopant diffusion as well as integration with high-k/metal gate.

Schottky barrier MOSFET is one of the non-classical technologies proposed to solve the problems associated with the conventional MOSFET.

In the conventional MOSFETs, there exist several components of the external resistive path. They are contact resistance (R_{co}) at the silicon/silicide interface, sheet resistance (R_{sh}) of the heavily doped p⁺ or n⁺ deep S/D region, spreading resistance (R_{sp}) in the S/D extensions (SDE) region and accumulation resistance (R_{acc}) accounting for the gate to S/D overlap region. These resistances are schematically depicted in Figure 2.2 (a).

Figure 2.2. Schematic of (a) a conventional MOSFET and (b) a Schottky barrier MOSFET.

In the Schottky barrier MOSFET, the heavily doped deep S/D and the SDE are replaced by metals or metal silicides [36] as shown in Figure 2.2 (b). The Schottky barrier MOSFET architecture removes the limitations of the conventional MOSFET by removing R_{co} , R_{sp} associated with silicide/doped S/D interface and SDE respectively. R_{acc} is removed due to the non-overlapping (to gate) MS junction. R_{sh} is also minimized as common metals or silicides have approximately one order or magnitude lower R_{sh} values as compared to the state-of-the-art doped S/D [1].

2.5 Operating principles of Schottky MOSFETs

The operating principles of a Schottky barrier MOSFET are illustrated in Figure 2.3. For the purpose of illustration, a fictitious metal with a Fermi level pinned to the mid-gap of a semiconductor is used in the following example. The semiconductor is intrinsic i.e., the Fermi level is positioned exactly at the mid-gap. The energy band diagram of the Schottky barrier MOSFET in equilibrium is shown in Figure 2.3 (a).

Figure 2.3. Band diagrams of the surface of a Schottky MOSFET at (a) equilibrium, (b) a positive gate voltage, and (c) a positive gate and drain voltages. (E_c , E_v , E_i and E_F denote the conduction band edge, valence band edge, semiconductor intrinsic level and metal Fermi level respectively.)

As shown in Figure 2.3 (b), when the gate is positively biased, the semiconductor channel is bent downward. This creates a triangular barrier for the electrons at the conduction band while a built-in potential V_{bi} is formed at the valence band [37-39]. Similar to a conventional MOSFET, the channel of a Schottky barrier MOSFET can be

inverted by biasing the gate with large enough voltage to create a conductive path for carriers, in this case electrons.

As shown in Figure 2.3 (c), when the drain is positively biased, a potential difference exists across the channel and current is conducted by thermionic emission and tunneling of electrons from the source metal. Electron tunneling current at the source side is enhanced as compared to the equilibrium due to the Schottky barrier thinning as a result of the band bending under the effect of drain bias. In theory, hole current can also be conducted by the same transport mechanisms from the drain side. However, due to the V_{bi} created by the gate bias the effective SBH experienced by holes at the drain side is higher. Since both I_{TE} and I_T are exponentially dependent on SBH, the total hole current is suppressed to a few orders of magnitude smaller than the electron current conducted in the channel. By increasing the gate and/or the drain bias, the effective SBH for electrons can be reduced due to image force barrier lowering [40, 41]. Also, as a result of the high electric field at the source to channel junction, the barrier width experiences significant thinning also enhances tunneling of electrons [42, 43]. As a result, current is increased by increasing gate and/or drain bias.

The above example shows that under NFET biasing conditions i.e., positive gate and drain biases, the Schottky barrier MOSFET behaves as a NFET. The same arguments hold true where the Schottky barrier MOSFET behaves as a PFET when biased at negative gate and drain biases. This characteristic is termed ambipolar conduction. Whether or not the device behaves as N- or PFET depends solely on the bias conditions and not on the Fermi level of the semiconductor (i.e., n- or p-type) or the SBH of the MS junction. The SBH and the semiconductor Fermi level only affect the flatband voltage V_{fb} of the channel, hence the threshold voltage V_{th} of the Schottky barrier MOSFET [44]. The SBH has more influence on whether the device can perform better as N- or PFET [38, 39,

43]. This can be explained with an example of a Schottky barrier MOSFET with a low electron SBH favours electron transport as oppose to a high hole SBH suppresses hole transport, thus the device should perform better as a NFET.

2.6 Schottky barrier tuning

In theory, SBH is an intrinsic property of a specific MS contact. However, due to Fermi level pinning, many MS contacts have SBH pinned close to the mid-gap of the semiconductor with mostly slightly larger electron barrier height, n-SBH than hole barrier height, p-SBH [30, 35]. In the previous section, we have discussed the operation principles of a Schottky barrier MOSFET and it is important to have a low n-SBH for NFET and a low p-SBH for PFET. In this section, various SBH tuning methods will be discussed.

2.6.1 S/D material

For complementary performance in Schottky barrier MOSFETs, both PFET and NFET are required. This has been achieved by using complementary silicides, i.e., two different silicides, one having low p-SBH for PFET, and one having low n-SBH for NFET. ErSi_{2-x} with n-SBH of $\sim 0.27 - 0.32\text{eV}$ [42, 43, 45, 46] and PtSi with p-SBH of $\sim 0.15 - 0.24\text{eV}$ [27, 39, 41, 42, 47, 48] are typically used for NFET and PFET, respectively. Zhu *et al.* used YbSi_{2-x} as the S/D material for NFET and the device was reported to have better drive current and lower leakage compared to ErSi_{2-x} S/D [49]. The improved performance was attributed to a lower n-SBH and a smoother $\text{YbSi}_{2-x}/\text{Si}$ interface.

The major drawback of utilizing 2 different materials for the N- and PFET separately is the additional processing steps. Silicide for the NFET/PFET has to be

formed first followed by the formation of the PFET/NFET. For e.g., PtSi S/D is formed first for the PFET followed by the formation of ErSi_{2-x} S/D for the NFET. This imposes the use of additional masking layer(s) for NFET and PFET.

Recently, there has been a revived interest of using mid-gap silicides with SBH $\sim 0.6\text{eV}$ i.e., TiSi_2 , CoSi_2 , NiSi for both the NFET and the PFET due to the simplicity involved in CMOS processing [20, 50-53]. As a result, some n-SBH tuning methods must be used in conjunction with these mid-gap silicides in order to achieve low effective n-SBH.

2.6.2 Dopant segregation

When silicidation is carried out on a doped silicon substrate, dopants are found to be ‘pilling up’ at the interface of the silicide/silicon interface to form a high concentration doping layer with a very steep profile [25, 27, 54, 55]. This phenomenon is known as dopant segregation or ‘snow plow’. A typical dopant segregation SIMS profile is shown in Figure 2.4. There are currently two methods to generate dopant segregation. The first one is by silicidation induced dopant segregation (SIDS) which has been described above. The second one is termed silicide as diffusion source (SADS) where dopants are implanted into preformed silicide followed by a drive in annealing for dopants to diffuse to the interface [27]. The occurrence of dopant segregation is commonly perceived as a result of the difference of solid solubility and diffusivity between the silicide and silicon. Common dopants (i.e., B, P and As) are found to diffuse along the silicide grain boundaries with diffusivities in a few order of magnitudes higher than that of crystalline Si at relatively low temperatures ($450 - 650^\circ\text{C}$) [25, 26, 56-58]. Coupled with low solid solubility in some silicide materials, most dopants diffuse to the silicide surface or the silicide/silicon interface [25, 59]. For the dopants that diffuse to the interface, due to the

high solid solubility and the low diffusivity of dopants in Si, the dopants eventually slow down and ‘pile-up’ at the interface near Si.

Figure 2.4. Typical SIMS profile of a boron doped Si substrate before and after NiSi formation. Significant dopant segregation is observed at the NiSi/Si interface. Image taken from ref [27].

It is also found that the segregated dopants at the silicide/silicon interface modify the electrical properties of the MS contact. This can be observed through simple I - V measurement where the MS contact is found to be more ohmic if the segregated dopants are of the same type as the silicon substrate i.e., n-type segregated dopants on n-type substrate. Figure 2.5 shows an example of diode I - V characteristics of arsenic segregation by silicidation [22]. The modified electrical property implies that the segregated dopants at the interface must be electrically activated. In fact, recently it has been shown by first principles calculation that boron and arsenic preferentially occupy substitutional sites at the NiSi/Si interface due to smaller formation energies [60]. This implies that dopants are stable only when they are electrically active. Thus, the most interesting part of dopant segregation is the activation of dopants at the silicide/silicon interface during silicidation at relatively low temperature range, typically 450-650°C. There is not much work that

accounts for the exact mechanism responsible for this. However, Wittmer *et al.* proposed that the generation of point defects i.e., self-interstitials and vacancies at the interface during silicide formation could be the reason for enhanced dopant activation at low temperature [26].

Figure 2.5. *I-V* characteristics of NiSi/n-Si(100) Schottky diodes with and without As segregation [22]. The silicidation process was done by RTA at 500°C for 90 s.

Recent work has shown that dopant segregation can be used to lower the SBH of a MS junction and it is possible to be integrated into transistor devices to achieve improved drive currents with lower leakages. This was first attempted by Kinoshita *et al.* for CoSi₂ NFET and the term dopant segregated Schottky (DSS) MOSFET was coined [51]. The DSS MOSFET architectures are illustrated in Figure 2.6. In order to achieve SBH modulation without losing the merits of Schottky junctions, the dopant layer must be sufficiently thin to be fully depleted, with a concentration $> 1 \times 10^{20}$ atoms.cm⁻³. Dopant segregation has been applied to NiSi based Schottky barrier MOSFETs [20, 21, 50-52, 61] as well as PtSi based Schottky barrier MOSFETs [23, 39, 41, 48], with the most

commonly used dopants being As and Sb for DSS NFET [21, 52, 62], and B for DSS PFET [21, 52, 61].

Figure 2.6. Illustration of (a) an ideal DSS MOSFET with ultra thin segregation regions and (b) a practical DSS MOSFET with finite but fully depleted segregation regions [51].

The working principles of the DSS MOSFET are fundamentally similar to the Schottky barrier MOSFET. However, what is attractive of utilizing the dopant segregation technique at the S/D is it creates an additional contact potential at the metal-semiconductor junctions, which effectively increase the barrier height for OFF state carrier and reduces the barrier width for ON state carrier [21, 61]. The band diagrams showing the mechanisms of ON and OFF states carrier transport are illustrated in Figure 2.7.

The device shown in Figure 2.7 is p-doped with a concentration in the order of 10^{19}cm^{-3} . This high concentration narrow dopant segregation region distorts the energy band of the semiconductor channel near the S/D. When the device operates in the ON state as shown in Figure 2.7 (a), the dopant segregation region effectively reduces the depletion width of the Schottky barrier between the source and the channel so that holes can tunnel through the barrier more easily. The drain receives an additional built-in potential from the distorted energy band. Hence, electrons experience a higher effective barrier. Thus, the overall effect is an improve drive current transported by holes injection from the source side.

Figure 2.7. Energy band diagrams during (a) ON state and (b) OFF state of a DSS and a Schottky barrier PFETs [61].

On the other hand, as illustrated in Figure 2.7 (b) when the device is in OFF state, electron tunneling from the drain contributes to a reverse current in the Schottky barrier MOSFET. However, in the DSS MOSFET the additional built-in potential behaves as a barrier that effectively blocks out electron tunneling. The overall effect is a suppressed OFF state leakage.

With dopant segregation, the On/Off current ratio can reach an astonishing 10^8 - 10^9 compared with the commonly obtained 10^3 - 10^5 from an unoptimized Schottky device.

Similar On/Off ratio has been demonstrated in ref. [21]. The transfer characteristic of the DSS PFET reported in [61] is shown in Figure 2.8.

Figure 2.8. I_D - V_G characteristics for DSS MOSFET reported as Modified Schottky Barrier (MSB) FinFET, conventional MOSFET (CN FinFET) and Schottky barrier MOSFET (SB FinFET) in [61]. The On/Off current of the DSS MOSFET is 10^9 .

2.7 Nickel Silicide

In CMOS devices, parasitic capacitances and resistances should both be minimized to achieve low resistive capacitive (RC) delay and hence increase the clock frequency [63]. Self-aligned silicide (SALICIDE) process forms the metal silicide at the gate and S/D simultaneously [64, 65]. The metal silicide thin films are an essential part in semiconductor IC technology. They are often used as S/D ohmic contacts and local interconnects to reduce the series resistance of devices so as to improve the speed of electronic circuits.

TiSi₂ was used in the SALICIDE process for technology nodes down to 0.25 μm in the early 1990s due to its low resistivity (10 – 15 $\mu\Omega\text{-cm}$) and high thermal stability. Conversion of the C49 to C54 phase became increasingly difficult at the sub-0.25 μm node as agglomeration of TiSi₂ occurs during the phase transformation at high

temperatures. This is a result of the reduction of nucleation sites when the linewidth reduces [63]. Subsequently CoSi_2 was used up to the 90nm node due to its smaller linewidth dependence than TiSi_2 . However, Co consumes ~25% more Si to form CoSi_2 as compared to Ti. More recently, NiSi is being used at the sub-90 nm nodes due to its low silicidation temperature, linewidth independence, low Si consumption, and non-bridging nature etc. [65].

As compared to TiSi_2 and CoSi_2 , the use of NiSi for contact metallization shows a number of technological advantages such as, very low formation temperature ($\sim 400^\circ\text{C}$), least silicon consumption, smooth silicide/Si interface, lowest achievable specific resistivity, relatively insensitive to substrate doping, and no “fine-line effect” [66-68]. As can be observed in the binary phase diagram for Ni-Si shown in Figure 2.9, there are six stable Ni-Si phases at room temperature namely, Ni_3Si , $\text{Ni}_{31}\text{Ni}_{12}$, Ni_2Si , Ni_3Si_2 , NiSi, and NiSi_2 . In a bulk reaction between Ni and Si, all of these stable phases formed simultaneously with the exception of the most Ni-rich (Ni_3Si) and the most Si-rich (NiSi_2). Though Ni_3Si_2 was found to be the dominant phase formed it exhibited irregular growth [69].

Figure 2.9. Equilibrium binary phase diagram for Ni-Si. Redrawn from ref. [70].

However in the case of a thin film reaction of Ni and Si, a sequential phase formation is usually observed. Typically, the sequence is described as follows, in the case where $t_{\text{Ni}} \ll t_{\text{Si}}$, the silicides formed will be in the order of $\text{Ni}_2\text{Si} \rightarrow \text{NiSi} \rightarrow \text{NiSi}_2$. In the case where $t_{\text{Ni}} \gg t_{\text{Si}}$, the silicides formed will be in the order of $\text{Ni}_2\text{Si} \rightarrow \text{Ni}_5\text{Si}_2 \rightarrow \text{Ni}_3\text{Si}$ [71]. For the interest of microelectronics fabrication, the reaction takes place between thin Ni with bulk Si substrate only, which is the first scenario described above. In the initial reaction process, the Ni film reacts with Si forming Ni_2Si until all the Ni is consumed. Further annealing at higher temperatures, NiSi phase begins to form at the expense of Ni_2Si through a layer by layer reaction process [72]. Both Ni_2Si and NiSi formation are diffusion controlled processes. The activation energy of Ni diffusion through NiSi has been reported to be about 1.5 eV, [73-76] which makes its formation in narrow lines straight forward and independent of the line width [67, 68, 77-80]. NiSi formation in a narrow Si line down to 100 nm width can be achieved using annealing temperature as low

as 400°C within 30 seconds, [80] There is no need of a second annealing step as in the formation of C54 TiSi₂ or CoSi₂.

Figure 2.10. Silicide degradation temperature vs. (a) silicide formation temperature and (b) deformation temperature for six silicides. Redrawn from ref. [81].

However, despite of its advantages, NiSi was not considered a serious candidate until recently mainly due to its low morphological and thermal stability. As shown in Figure 2.10, NiSi presents the poorest morphological stability on poly-Si amongst silicides of interest. Also, NiSi is reported to have agglomeration issue at 550-600°C [81, 82]. On top of that, the NiSi phase becomes unstable at 700°C which transforms to NiSi₂ phase with a specific resistivity three times higher than that of NiSi [83]. Furthermore, the formation of NiSi₂ is accompanied by a 1.7 times volume expansion which means larger Si consumption [84]. The growth of NiSi₂ from NiSi is a nucleation-controlled process and typically yields a rough surface and interface, [85] which is undesirable to junction integrity.

2.8 Silicon Nanowires

When the scaling of MOSFET becomes so aggressive that the channel is reduced to less than 1 μm, transistors exhibit short channel effects. Short channel effects are 'side effects' of aggressive scaling at small dimension where a transistor no longer behaves like

a perfect switch; rather it becomes ‘leaky’ where the transistor leaks more current when it is turned off. At smaller dimensions, the switching of a transistor has higher influence from the drain voltage as compared to that of a larger transistor. In other words, the gate now has less control on the channel. This phenomenon is known as Drain Induced Barrier Lowering (DIBL).

Researchers have gone so far in modifying the structure of a MOSFET such that the final structure could provide the best performance with scalability reaching far beyond a planar device can ever do. To allow the gate to have exclusive control on the channel, double-gated MOSFET have been conceived where the channel is a layer of Si sandwiched between two gates, one at the bottom and the other on top [11]. The coupling of electrostatic field of the two gates will dominate the control of the channel from that of the drain voltage. The change in structural architecture does not end here. Eventually, the concept of tri-gate MOSFET is introduced, where the channel is now protruding out from the silicon substrate and the three sides of the channel are surrounded by a poly-silicon gate. The transistor now looks like a ‘fin’ standing on the silicon substrate, hence the name FinFET [14, 86, 87]. With three sides covered by the gate, what would be considered as the ‘ultimate’ MOSFET would be one that has the gate wraps around the channel providing the strongest coupling of gate electrostatic field. This ultimate structure has the look of a wire and the diameter can be fabricated to as small as 5nm, hence the popular name of nanowire [86, 88-92].

The motivations behind silicon nanowire fabrication are due to its superior electrical performance over the conventional planar devices [89, 93-95], the small dimension that allows aggressive scaling and realization of ultra high density circuits [90, 96, 97] and also the compatibility of using silicon as the substrate or channel material in the semiconductor industry.

2.9 Synthesis Methods

2.9.1 Bottom-up Approach

The bottom-up approach is considered as a potential method to fabricate complex and high aspect ratio nanowires. The basic idea of this method is to use nanoscale building blocks to initiate directly the growth of nanosize structures at desired positions and with designed dimensions and properties. In short, the nanowires are formed in a self-organized fashion. Development of the different methods for the growth of nanowires has been reported by many research groups. In general, these methods include [98]: (a) the vapor-liquid-solid (VLS) process, (b) vapor-solid (VS) process, (c) template-directed synthesis, (d) electrochemical deposition [99] and (e) solution growth. In this section, only the most commonly used VLS method will be discussed as it is considered as one of the most promising bottom-up method.

VLS method was originally developed in 1964 by R.S. Wagner and W.C. Ellis to study the morphology and the unidirectional micrometers Si whisker growth involving impurities [100]. In general, nanowires are grown on a clean, defect-free surface of a substrate. The substrate material can be semiconductors or insulators such as sapphire or glasses. Small metal clusters are deposited on the surface to work as catalyst. The substrate is then heated until the cluster melts and form liquid droplets. The diameter of the droplets is affected by the initial thickness of the deposited metal layer. The larger the thickness, metal droplets of larger diameter will be obtained [101].

VLS process starts with the dissolution of gaseous reactants into nano-size liquid droplets and forms alloy with a decreased melting temperature as compared to the pure metal. The liquid alloy acts as a preferred sink for arriving atom, due to the much larger sticking coefficient than the solid substrate [98]. For example, in the case of growing Si

nanowire, the Si atom enters the liquid alloy. When the Si concentration in the liquid alloy reaches the super saturation point, which can be referred from the binary phase diagram, Si freezes out and forms solid crystalline structure at the solid-liquid interface. This process is schematically illustrated in Figure 2.11. Basically it can be broken down into four main steps [102]: (1) the adsorption of reactant species on both the catalyst droplet surface and the side surface of growing nanostructures; (2) the dissolution of the species at the droplet surface; (3) the diffusion of the species inside the droplets; and (4) precipitation, incorporation, and crystal growth at the liquid-solid interface.

Thus, it can be seen that there are two mass diffusion processes regarding the VLS growth of nanostructures: the first one is inside the catalyst droplet toward the liquid-solid interface; the second one is from the side surface of the growing nanostructures or from the substrate toward the catalyst droplet for dissolution. Modify the mass diffusion procedure can be achieved by modulating experimental conditions, for instance temperature, pressure, gas flow and etc. Hence, different phase structures of nanowires can be obtained. As the process continues, there is more precipitation of Si from the liquid alloy and eventually single crystal nanowire is formed. The droplet usually remains at the tip of the nanowire which causes the succeeding growth of the nanowire. The nanowire grows in length by this mechanism until the metal catalyst is consumed or the growth conditions are changed.

Figure 2.11. Schematic illustration of continuous VLS growth steps for 1D nanostructure [102].

Metal catalyst is one of the major requirements in VLS growth process. The selection of an appropriate catalyst that will work with the target material to be processed into 1D nanostructure is one of the challenges faced by VLS process. Typically, this is done by analyzing the phase diagrams. Ideally, metals that can form eutectic alloys with the target material at low temperature are desired from economic and process integration point of view. Besides, the metal catalyst droplets should not wet the nanowire sidewalls, as this will consume the droplets continuously and will cause the growth of tapered shape nanowires as the droplets becomes smaller with the length of the nanowires. The VLS growth is terminated once the catalyst is completely consumed. Another concern for the selection of metal catalyst is the incorporation coefficient of metal atoms in the target material. The incorporated metal in the nanowires will produce unwanted deep level defects, which will seriously affect the material electric properties and limit the application of the nanowires fabricated by this method.

Figure 2.12. The binary phase diagram of (a) Au-Si and (b) Au-Ge.

Metals that have been demonstrated as catalyst in VLS process include Au, Ag, Cu, Pt, Fe, Ga, Ti, Al and etc. Among them, gold is the most frequently used metal to synthesize Si and Ge nanowires, probably due to the relatively low eutectic temperature with Si (~363°C) and Ge (~361°C) compared to other metals. In additions, gold is chemically inert and has small incorporation coefficient with Si and Ge compared with other metals. The binary phase diagrams of Au-Si and Au-Ge are shown in Figure 2.12.

Table 2.1. Different semiconductor/metal combinations and growth methods for nanowires.

NW	Source	Catalyst	Growth process	Reference
Si	SiCl ₄	Au	CVD	[103-105]
Si, Ge	SiH ₄ , GeH ₄	Fe	PLD	[106]
Si	SiH ₄ or SiH ₂ Cl ₂	Ti	CVD	[107]

Si	SiH ₄	Al	CVD	[108]
Si	Silyl radicals	Ga	Microwave plasma etching	[109]
n-type Si	SiH ₄ , Sb	Au	CVD	[110]
Ge	Ge particles	Au	evaporation	[111]
Doped Ge	GeH ₄ , PH ₃ , B ₂ H ₆	Au	CVD	[105]
InP	PH ₃ , TMIIn	Au	MOVPE	[112]
InAs		Au	CBE	[113-116]
InAs/InAsP	TMIIn, TBAs, TBP	Au	CBE	[117]
ZnO	ZnO, C	Au	Carbothermal reduction	[118, 119]

MOVPE: metal-organic vapor phase epitaxy

PLD: pulsed laser deposition

CBE: chemical beam epitaxy

The problem with gold is that it is not a CMOS compatible material and can be a source contamination in CMOS technology. The incorporation of gold is known to result in deep-level defects near the mid gap of Si, which drastically reduces the minority carrier lifetime and thus should be avoided in the contact of active devices. Besides this, gold can wet or diffuse on the surface of growing Si nanowires in an ultra high vacuum (UHV) environment [98]. It is also extremely difficult to remove the gold catalyst at the tip of semiconductor nanowires after VLS growth process. In Table 2.1, some semiconductor/metal combinations and the growth process for VLS growth nanowires are listed. Another issue facing the bottom up approach is the self-assembly nature of this method. The challenges lie in both the growth and control of position, dimension and large scale ordering of the nanowires. Thus far, there is no convincing breakthrough in the bottom up approach to replace the current top down semiconductor technology in manufacturing.

2.9.2 Top-down Approach

Top-down approach essentially uses the conventional ULSI technology to fabricate 1-D nanostructures, which is based on a combination of photolithography, thin-film deposition, and etching steps. The first demonstration of 1-D nanostructure was done by Randall and Reed at Texas Instruments in the 1988 in order to study the discrete electronic states in semiconductor quantum dots [120]. The heterostructure layers were deposited by molecular-beam-epitaxy (MBE), while the AuGe/Ni/Au ohmic metallization dots were defined by electron-beam (e-beam) lithography. Due to the fabrication induced damage and poor lateral control, the device properties were rather unsatisfied.

The diameter of the nanowire using top-down method is rather limited by the wavelength of the exposure source using in the lithography. Liu *et al.* has obtained single crystal Si nanowires with sub-5 nm diameter by using a combination of e-beam lithography, Cr lift-off, NF_3 reactive ion etching (RIE) and thermal self-limiting oxidation [121-123]. After that, other research groups were also using the thermal self-limiting oxidation technique to obtain small diameter nanowires [124, 125].

The method used by Liu *et al.* is as follow. First, e-beam lithography was used to form patterns on photoresist coated Si wafer. After that, Cr film was evaporated for a lift-off process to produce Cr dot patterns on top of the photoresist. After lift-off process, NF_3 RIE was then performed to obtain columns with high aspect ratio. The critical step in producing the sub-5 nm Si nanowires is the thermal oxidation.

Self-limiting Oxidation

Some interesting observations are obtained from Liu's experiment. The self-limiting effect leads to a more uniform nanowire diameter as oxidation progresses; this is clearly indicated in Figure 2.13.

Figure 2.13. TEM micrographs of the bottom non-uniform portions of Si nanowires going through (a) 0 h, (b) 8h and (c) 16h of dry oxidation at 850°C [122].

Figure 2.14. TEM micrographs show an identical Si nanowire going through (a) 3h, (b) 4h, and (c) 5h of dry oxidation at 850°C [123].

The tapered vertical nanowires have larger diameters near the substrate and the diameters gradually become smaller toward the tip. The lower part of the nanowire oxidizes faster than the upper part. This shows that the oxidation rate depends on the diameter of the wire. The larger the diameter, the faster it is oxidized. In addition to the core radius dependence, the oxidation rate is also found to be dependent on the column

oxide thickness. For a given core curvature, thicker oxide reduces the oxidation rate. Here, it can be seen that for an initially non-uniform nanowire as shown in Figure 2.14(a), the final profile of the self-limiting nanowire has the thinnest diameter at its center portion. The final diameter of the nanowires saturate at different values depending on the initial diameter of Si nanowires, as pointed out in Figure 2.15.

As the temperature of the oxidation process increases, the time to achieve the limiting value decreases. The self-limiting effect is only observed for oxidation temperatures below 950°C, and above this temperature the Si nanowire will be fully oxidized after several hours.

Figure 2.15. Oxidation duration of Si nanowires with different core diameters at 850°C [122].

Self-limiting oxidation is believed to be caused by the stress built up at the Si/SiO₂ interface due to the growth of new oxide and the associated volume expansion at the interface. The smaller the core, the greater the oxide layer has to expand, which causes a greater stress normal to the interface. This retards the process of further oxidation. It was observed that the self-limiting oxidation is due to the increase in the activation energy of oxygen diffusivity in a highly stressed oxide. The Si-Si bond breaking and O insertion energy are functions of the stress level at the Si/SiO₂ interface.

Using Deal-Grove's oxidation model[126] (diffusion limited) with cylindrical boundaries, the oxidation rate dx_o/dt can be expressed as follows

$$\frac{dx_o}{dt} = \frac{1}{N} \frac{C^*}{(x_o / D)r_c \ln(r_c / r_o)} \quad (\text{Equation 2.18})$$

where N is oxide density, C^* is oxidant solubility in oxide, r_c is the Si core radius, r_o is the outer radius of oxidized column, and D is the activation energy of diffusion. Using experimental oxidation rate data, the activation energy of diffusivity were plotted against r_o/r_c . It was found that as r_o/r_c increases, D increases. Recent theoretical and experimental work suggested that the self limiting oxidation is strongly suppressed by stress during oxide growth. Cui *et al.* explained the self limiting oxidation by offering a 2D model that is governed only by the diffusion of the oxidizing species, ignoring the interface oxidation reaction limiting step [127]. They found that by modeling the cross section of a Si nanowire, the diffusion activation energy increases monotonically as the ratio of the outer radius (oxide surface) to the inner radius (Si/SiO₂ interface) of the wire increases as shown in Figure 2.16. The increase in the diffusion activation energy is explained by the building up of stress due to the non-uniform deformation of the oxide during oxide growth where 'old' oxide is pushed out by newly grown oxide while conserving the old oxide's volume, hence creating a stretch on the convex surface. Again, the results are in good agreement with early work done by Liu.

Figure 2.16. Diffusion activation energy and the oxidation rate (dx_0/dt) in the SiO_2/Si interface as the function of the ratio of the outer radius (b) to the inner radius (a) [127].

In another work done by Ma et al., a model on oxidation that takes into account of the viscosity of oxide is provided [128]. The model has also been improved with the support of extensive studies from TEM micrographs. Experimentally, beams of free standing Si fins with various sizes were prepared. Subsequently, these Si fins were subjected to different oxidation conditions and cross sectional TEM were taken and compared to process simulation results that have been incorporated with the improved viscosity model. In their model, the oxide viscosity is not only temperature dependent but also shear stress dependent. When the total shear stress is low, the oxide viscosity is almost constant. However, as the total shear stress is increased beyond a certain threshold, namely the critical shear stress, the oxide viscosity reduces exponentially. Interestingly, they also observed that the self-limiting effect is indeed diffusion-limited as was observed by Liu. From simulation, the diffusivity reduces as the compressive hydrostatic pressure in the vicinity of Si/SiO_2 interface builds up. Regardless of the oxidation temperature used, the pressure builds up with time and the oxidant diffusivity is significantly retarded

as shown in Figure 2.17 (a). Using their model, they successfully simulated and predicted the size and shape of the final Si nanowire embedded in thermally grown oxide as shown in Figure 2.17 (b).

Figure 2.17. (a) Simulated hydrostatic pressure at Si/SiO₂ interface is plotted against oxidation time and (b) TEM micrographs and simulated results of thermally oxidized Si fins at different temperatures [128].

Although the top-down method is compatible with CMOS technology, there are still disadvantages of growing nanowires by this approach. First of all, the initial dimension of the nanowires fabricated by the top-down method fundamentally depends on the lithography technology. Clearly electron beam lithography could define a nanowire with linewidth as narrow as 5 nm but the intolerably low throughput would not make e-beam lithography an industry option to be considered. Further minimization of the nanowire diameter requires higher resolution processes, which will then incur higher production costs for future production lines.

2.9 Silicon Nanowire Devices

2.9.1 Simple Circuits and Logics

In 2000, Cui *et al.* reported the doping (p and n-type) of Si nanowires by controlled introduction of boron or phosphorus during the vapor phase growth of the nanowires [129]. By using a back gated transistor structure and Al/Au contacts to either end of the doped nanowires, they verified that the wires were electrically p- or n-type by conductance measurements and observed ohmic current conduction whose magnitude depended on the amount of doping.

In 2001, Huang, Cui and Lieber *et al.* reported nanowire junctions arrays that have been configured as OR, AND, and NOR logic gate structures with substantial gain and have been used to implement some basic computation [90]. The nanowire arrays are all fabricated by the bottom-up approach, into crosses of p-nanowire and n-nanowire junctions, resembling functional p-n junctions. Nanowire transistors were made by the same crossed junctions but showed drive currents 10x lower ($\sim 50 \mu\text{A}/\mu\text{m}$) than conventional MOSFETs (with 50 nm gate length) but with comparable $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $\sim 10^5$. The logic array of an OR gate is shown in Figure 2.18. Si nanowires grown by laser

assisted catalytic growth was suspended in ethanol solution. The solution was then passed through fluidic channels in molds on a flat substrate. By pre-patterning the substrate chemically, nanowires were preferentially assembled at positions defined by the chemical pattern.

Figure 2.18. (a) Schematics of logic OR gate constructed from a 2 by 1 crossed NW p-n junction. (Insets) An example SEM (bar: 1 μm) of the assembled OR gate and symbolic electronic circuit. (b) The output voltage versus the four possible logic address level inputs: (0,0); (0,1); (1,0); (1,1), where logic 0 input is 0 V and logic 1 input is 5 V (c). The experimental truth table for the OR gate [90].

They subsequently assembled multiple AND and NOR gates together to form a XOR gate, and with this XOR gate a half adder was built and some simple computations were implemented. The simplicity of these circuits is perhaps the most striking advantage that nanowires can offer. With the implementation of these extremely tiny circuits, it is possible to achieve very high density logics as compared to the conventional logics. However, in this work, the authors have not studied the off state leakage of the p-n junctions and hence no static power consumption calculation or estimation can be deduced. Another important aspect of logic gates is the switching delay, which was not reported in this work too.

2.9.2 Silicon Nanowire Field Effect Transistor

By using either the bottom-up or the top-down method, silicon nanowire transistors have been successfully fabricated. In 1999, using the self-limiting oxidation

method, Kedzierski *et al.* fabricated Si nanowires with doped poly gate over the nanowire channel and measured a I_{ON} of $800\mu\text{A}/\mu\text{m}$ [92]. However, a high series resistance of $100\text{ k}\Omega$ is measured and this is due to the uncovered region of the nanowire by the gate. A nearly ideal subthreshold swing of $60.3\text{mV}/\text{decade}$ is achieved. The nanowire transistor is shown in Figure 2.19.

Figure 2.19. (a) SEM micrograph of a wraparound phosphorus doped polysilicon gate 200 nm wide and $1200\text{ \AA}$ tall. (b) Cross-sectional TEM micrograph of a $5\text{--}7\text{ nm}$ Si nanowire. This wire was formed by a $925\text{ }^{\circ}\text{C}$ stress-limited oxidation of a 45 nm wide 40 nm tall silicon line drawn in the $\langle 100 \rangle$ direction. The black region is a metal layer used to protect the wire during sample preparation. Images reproduced from ref. [92]

In 2002, Cui *et al.* fabricated silicon nanowire transistor using the bottom-up approach to study their electrical performances as compared to the conventional transistor [88]. The transistors were fabricated on SOI wafers and the silicon substrate below the 600 nm thick buried oxide (BOX) layer was used as a back gate. With a diameter of $10\text{--}20\text{ nm}$ and a gate length of 500 nm , the back gated silicon nanowire transistor did not outperform the conventional one because the BOX layer was obviously too thick to provide good control of the gate voltage on the nanowire channel. Hence the poor subthreshold swing of $174\text{--}609\text{ mV}/\text{decade}$ was observed. The on-state current was $50\text{--}200\text{ }\mu\text{A}/\mu\text{m}$, as compared to the ball park value of $600\text{ }\mu\text{A}/\mu\text{m}$ of the conventional MOSFET. However, the author suggested that when the thick BOX is further reduced and

optimization can be applied, the converted result would outperform the conventional MOSFET.

However the first top-down approach in fabricating silicon nanowires that uses a standard industry CMOS technology only started after 2000 by the research groups of Samsung and Institute of Microelectronics of Singapore (IME). In 2006, Singh *et al.* fabricated the world smallest diameter silicon nanowire with a diameter as small as 3 nm [130]. Again, the electrical performance of the nanowire transistor is remarkably higher than the conventional MOSFET. Apart from the electrical result, the effect of diameter on the threshold voltage was also studied. It is found that as the diameter of the wire reduces, the magnitude of the threshold voltage increases due to quantum mechanical confinement effects.

Figure 2.20. (a) Top view SEM micrograph of nanowire after SiGe removal. Nanowire $d = 10\text{nm}$ and damascene-gate $L_G = 30\text{nm}$. (b) Cross-sectional SEM micrograph of nanowire. Images reproduced from ref. [131].

By using sophisticated process steps involving SiGe, Samsung managed to obtain the world first twin silicon nanowires on a horizontal plane, with a diameter of 10nm each [131]. The twin nanowires with a plan view and a cross-sectional view is shown in Figure 2.20. The measured performance of this transistor showed remarkably results with drive current of $1110\text{ }\mu\text{A}/\mu\text{m}$ and $2640\text{ }\mu\text{A}/\mu\text{m}$ from PFET and NFET respectively. The other striking results were the extraordinarily low off state current and near perfect

subthreshold swing of 66 mV/decade and 71 mV/decade on PFET and NFET respectively. The DIBL measured was less than 20 mV/V for both devices, which implies that the nanowire transistor is indeed superior in short channel effect to its conventional counterpart. This was followed in 2006 by more aggressive scaling of L_G down to 15 nm, as well as nanowire diameter down to 4 nm [132]. The PFET I_{ON} was found to be larger than that of the NFET due to the enhanced hole mobility as the nanowire diameter is reduced. The gate delays reported were within the ITRS requirements for $L_G = 16$ nm devices. Subsequently, improved PFET performance by 85% using embedded SiGe S/D stressors as well as an 80% improvement by using <110> orientation on the substrate were demonstrated by the same group in 2007 [133].

Besides SiGe S/D stressors reported by Samsung as strain enhancement technique for nanowire MOSFETs, Tezuku *et al.* have reported strained Si nanowire NFETs and strained SiGe nanowire PFETs utilizing strained SOI and silicon germanium on insulator (SGOI) as starting substrates [134]. The NFET mobility enhancement is 1.9, while the PFET mobility enhancement is 1.6 against unstrained Si nanowire MOSFETs.

Enhanced carrier mobility was also reported in GAA Si nanowire MOSFETs in 2007 due to oxidation induced tensile stress [135]. The tensile stress ranges from 200 MPa to 2 GPa as a result of bending of Si nanowires due to oxidation induced stress and subsequent removal of SiO_2 by wet etching. The bended Si nanowire transistors showed a maximum transconductance ~ 2 orders higher than the non-bended Si nanowire transistors.

GAA Si nanowire transistors have also been fabricated from bulk wafers without the use of SOI [136-139] or selective epitaxial processes [131-133] which greatly reduce cost and complexity [140]. The electrical characteristics are comparable with previously

reported Si nanowire transistors with $I_{ON} = 1039 \mu\text{A}/\mu\text{m}$, $SS = 72 \text{ mV/decade}$, and $DIBL = 4 - 12 \text{ mV/V}$.

Non-volatile flash memory based on semiconductor-oxide-nitride-oxide-semiconductor (SONOS) has recently been investigated using Si nanowire MOSFETs. In 2007, Suk *et al.* reported for the first time GAA twin Si nanowire SONOS memory with diameter $\sim 3 \text{ nm}$ [141]. A threshold voltage shift of 5V (between program-erase (P/E) states) was observed with a P/E speed of $100 \mu\text{s}/10 \text{ ms}$ and P/E voltage of 10 V/-11 V. In addition, faster program speed was observed as Si nanowire diameter decreased which contribute to larger vertical electric field. Lee *et al.* reported a SONOS non-volatile memory using GAA Si nanowire MOSFET with a diameter of $\sim 8 \text{ nm}$ [142]. The threshold voltage shift was $\sim 1.7 \text{ V}$ with a 12 V/80 μs program and a -12 V/1 ms erase time. Fu *et al.* reported a GAA Si nanowire SONOS with Si nanocrystals on nitride as the trap layer with Si nanowire diameter of 5 nm [143]. The threshold voltage shift was $\sim 3.2 \text{ V}$ with a 11 V/1 μs program and a -10 V/1 ms erase time. More recently, vertical Si nanowires have been fabricated to further increase the memory packing density [144].

2.10 Summary

The relevant concepts in MS Schottky barrier have been covered, together with the operation and architecture of Schottky barrier MOSFET. Also, the formation of Si nanowires by bottom up and top down methods has been discussed. In addition, state-of-the-art Si nanowire based MOSFETs are summarized and presented. Further discussion with regards to the Schottky barrier Si nanowire MOSFETs will be made in the following sections.

Chapter 3 METHODOLOGY

3.1 Introduction

In general, this work studies the effect of dopant segregation first with diodes, and subsequently followed by a demonstration on Si nanowire transistors. This chapter describes the experimental methodologies employed for the fabrication of diodes and Si nanowire transistors with the introduction of some key equipment used, as well as the key characterization and simulation methods for analyses. Since laser processing is the key process employed in the device integration, a description of the analytical simulation used for laser processing in the fabrication of the devices is provided.

3.2 Key device fabrication equipment

3.2.1 Metal deposition

Sputter deposition is a method based on physical vapor deposition (PVD) and involves the sputtering of atoms from a source target which then deposits onto a substrate as a thin film [132]. It is one of the most commonly used techniques for thin metal films deposition for vias and lines, diffusion barriers, and metal contacts etc [133].

Highly energetic and chemically inert ions, in our case Ar^+ , are used as the bombardment species of metal targets. Ar gas is ionized by electrons trapped in helical paths in a magnetron which utilizes strong electric and magnetic fields. As a result of the bombardment, the neutrally charged target atoms are ejected and subsequently deposited on the surface of the Si substrate located below the metal target. The advantages of sputtering as a deposition technique is that firstly, the deposited films have the same

composition as the source material and secondly, the deposition rate is high. The higher rate of deposition would result in lower impurity incorporation because fewer impurities are able to reach the surface of the substrate in the same amount of time.

A Discovery 18 DC/RF Research Magnetron Sputter Deposition System was used with standard features such as automation, DC and RF power supply, base vacuum of 3×10^{-7} Torr and 3 confocally-mounted cathodes which provide better than $\pm 5\%$ uniformity. The targets used for the deposition were 99.99 at. % pure.

3.2.2 Rapid thermal annealing

RTA is a process that rapidly increases the temperature of the wafer and maintains it at set temperatures (up to 1200°C or greater) for short periods of time (typically less than 60sec) [6]. Normally, the process includes three stages, which are the ramping up to the set temperature, the main annealing stage at the set temperature for the set period and the ramping down to the room temperature. Thermal shock can be minimized by slowly bringing down the temperature of the wafer temperature. The rapid heating is accomplished using high power halogen-quartz lamps. Due to the selective absorption of radiant energy from the lamps by the wafers but not by the quartz chamber, RTA is able to achieve clean and short processing times.

For our purposes, RTA was carried out for silicidation, i.e., the solid state reaction of the metal and Si into a thermodynamically more stable state. Silicidation by RTA is a fast method to obtain silicides with good film uniformity [134]. All RTA experiments were carried out by a XM80 rapid thermal annealing system.

3.2.3 Excimer laser annealing

A Lambda Physik laser was used to generate the KrF excimer pulsed LA with a wavelength of 248 nm and a FWHM of each pulse of 23 ns. The generated spatial laser energy profile has a weak Gaussian distribution. A beam homogenizer, made of 8 x 8 cylindrical lens array, was installed to convert this initial profile to a flat top profile such that the intensity of the laser energy was uniform across the laser beam size. The temporal profile of the laser measured by a high speed detector exhibits a weak “three-finger” shape that can be approximated as a “trapezoidal” shape as shown in Figure 3.1.

Figure 3.1. The temporal profile of the laser (measured at 250 Hz at 400 mJ) showing an approximated trapezoidal shape.

To ensure that every area in the sample was annealed at the same energy density, a mask was placed after the beam homogenizer to further block out the edge of the laser beam where the laser intensity fall off might still exist. A sensitive joule meter was used to measure the laser energy on the sample (after passing the beam homogenizer and focusing lenses). The measurements were repeated every hour during annealing process to monitor any fluctuation in the laser energy output. The energy fluctuation was usually

in the range of ± 3 to 7% (depending on the laser energy used) during normal operation. The laser fluence used to anneal the sample was obtained by dividing the measured laser energy by the area of the laser beam size. The beam size measured on the sample, after passing the mask and the focusing lens, was $2 \times 2 \text{ mm}^2$. Since the laser pulse duration cannot be changed, the only parameter which can be varied during LA process are the laser fluence and the number of pulse. During the LA process, the sample was placed inside a small chamber enclosed with a quartz window, which was coated by an anti-reflective coating. A continuous purified N_2 purging was performed throughout the annealing process. With the fact that the sample size was $10 \times 10 \text{ mm}^2$ and the laser beam size after the focusing lens was $2 \times 2 \text{ mm}^2$, the definition of single-pulsed LA is that a particular area ($2 \times 2 \text{ mm}^2$) of the sample was only being irradiated with particular laser fluence before exposing the adjacent area. An overlap of $50 \text{ }\mu\text{m}$ between irradiated areas was imposed to further ensure a uniform laser irradiation. This process, which is similar with “step and scan” technology in photolithography, was repeated until the whole sample surface received a maximum coverage of laser beam to facilitate further characterizations.

3.3 Physical and Chemical Characterization

3.3.1 Scanning electron microscopy (SEM)

SEM is a type of electron microscopy capable of producing high-resolution micrographs of a sample surface. SEM images have a characteristic three-dimensional appearance and are useful for judging the surface structure of the sample. In a typical SEM, focused electron beams of energy $\sim 5 - 30 \text{ KeV}$ are scanned on a sample. The reflected secondary and backscattered electrons are used to form a magnified image. Due to the much smaller electron wavelength and higher depth of field compared to the photon,

the resulted SEM image can have better resolution and depth of field compared with the image from an optical microscope.

Secondary electrons which are emitted from the surface atoms form the conventional SEM image whose contrast is determined by the sample morphology. In field emission SEM (FESEM), the micrographs are brighter due to the greater number of electrons emitted per unit area than the traditionally used thermal emitters of tungsten or lanthanum hexaboride. The system is capable of high resolution imaging as well as high quality real time image display at all scan speeds, enabling observation and recording of superior images even in a bright room. Interaction of electron beam with atoms in the sample can also cause shell transitions resulting in the emission of x-rays which have energy characteristics of the element under study. Detection and measurement of the x-ray energy permits elemental analysis and is known as energy dispersive x-ray spectroscopy (EDS). A JEOL FESEM JSM 6700 was used in our experiments.

3.3.2 Transmission electron microscopy (TEM)

TEM is an imaging technique whereby a beam of electrons is transmitted through very thin specimens. An image is formed, magnified and directed to appear on a fluorescent screen. The main strength of the TEM technique lies in its extremely high resolution $\sim 0.08\text{nm}$. The three primary imaging modes are bright field, dark field, and high resolution TEM (HRTEM). Images formed with only the transmitted electrons are bright field images and images formed with a specific diffracted beam are dark field images. HRTEM gives structural information on the atomic size level and has become very important for interface analysis. A FEI FETEM CM200 and a Philips Tecnai F20 TEM with 200 keV acceleration voltage, and 0.2 – 0.15nm spot size were used in our experiments.

3.3.3 Secondary ion mass spectroscopy (SIMS)

The basis of SIMS is a destructive removal of material from a sample by sputtering and the analysis of the removed material by a mass analyzer. A small fraction of the atoms are ejected as positive or negative ions, which are referred to as secondary ions. The mass/charge ratio of the ions is analyzed, detected as a mass spectrum, as a count, or displayed on a fluorescent screen or on a CRT. Quantitative depth profiling, i.e., one selected mass plotted as secondary ion yield versus sputtering time, is a major strength of SIMS. In our experiments, an Ion time-of-flight SIMS (ToF-SIMS) system was used. The incident beam consists of pulsed ions from a liquid Ce^+ gun with beam diameters as small as $0.3\mu\text{m}$. For pulse widths on the order of ns, ions are sputtered in a brief burst and the time for these ions to travel to the detector is measured. The kinetic energy of secondary electrons,

$$KE = \frac{1}{2}mv^2 = qV \text{ (Equation 3.1)}$$

where v is the ion velocity given by L/t_t , V is the accelerating voltage, t_t is the transit time, and L is the distance to the detector. Thus by rearranging the above equation, the mass/charge ratio = $\frac{2Vt_t^2}{L^2}$, which gives the relation of mass/charge to time of flight. A major advantage of ToF-SIMS is the absence of narrow slits in the spectrometer, increasing the ion collection by 10 - 50%. The sputtering rate can be reduced and is so low that it may take an hour to remove a fraction of a monolayer which allows for more accurate depth profiling. Since mass/charge is determined by time of flight, both large and small ion fragments can be detected.

3.3.4 Photoluminescence Spectroscopy

Photoluminescence spectroscopy is a contactless, nondestructive characterization method for the analysis of materials electronic structure. The working principle photoluminescence involves a process in which a material absorbs photons of certain wavelength and then re-radiates photons. Typically, laser is illuminated onto a material where excess energy from the absorbed photons is transferred into the material in a process called photo-excitation. The excess energy can be dissipated by the sample through the emission of light, or luminescence. The combination of photo-excitation and luminescence is termed photoluminescence. The intensity and spectral content of this photoluminescence contain the information of various important material properties.

During photo-excitation, electrons within a semiconductor material are excited from the valence band by absorbing excess energy from the photons to move into excited states in the conduction band. Typically, the excited electrons have more energy than the semiconductor energy band gap. Usually, the electrons go through a non-radiative relaxation process and lose some energy before they settle at lowest state of the conduction band. At this point, the electrons ultimately fall back to the equilibrium state i.e., the valence band by emitting photons. This form of energy transition involving the emission of photons is particular useful in the determination of direct band gap semiconductor materials.

Radiative transitions in semiconductors also involve localized defect levels. The photoluminescence energy associated with these levels can be used to identify specific defects, and the amount of photoluminescence can be used to determine their concentration.

3.3.5 Current-voltage measurements

The I - V characteristics were extracted from the devices using an Agilent 4157B modular semiconductor parameter analyzer. For the temperature dependent measurement, a Temptronic ThermoChuck System was used. A high resolution of 10^{-14} to 10^{-15} A can be achieved at properly maintained condition.

3.4 Fabrication of diode

The diodes studied in this work are back-contacted diodes fabricated on 8 inch Si substrate. There are 3 splits of the diode of interest, namely Schottky diode (without any additional implant), Dopant Segregated Schottky (DSS) diode, and Excimer Laser Annealed Dopant Segregated Schottky (ELA-DSS) diode.

3.4.1 Baseline process for diode fabrication

Si (100) substrate was used as the starting material in all the splits. A layer of 400 nm high density plasma (HDP) oxide was deposited by an Applied Materials plasma enhanced chemical vapor deposition (PECVD) tool. A backside implantation and activation were employed before subsequent steps to ensure an ohmic back contact in the final device. The back contact implantation condition was BF_2 $1 \times 10^{15} \text{ cm}^{-2}$ at 30 keV for p-type substrate and P $1 \times 10^{15} \text{ cm}^{-2}$ at 30 keV for n-type substrate. The activation condition for back contact implant was 1000°C for 30 seconds. Next, an array of $90 \mu\text{m}$ by $90 \mu\text{m}$ square openings was patterned by a KrF 248 nm lithography tool to define the diode areas. This was followed by the etching down of the HDP oxide within the defined openings using an Applied Materials P5000 reactive ion etch (RIE) tool. By timing the etch rate of the HDP oxide, the etching was designed to stop by leaving a 20 – 30 nm oxide layer in order to prevent plasma damage on the Si surface. This remaining oxide

layer was removed in a diluted hydrogen fluoride (DHF 1:25) solution. The wafer was immediately loaded into a sputtering chamber to minimize contamination and native oxide growth. A layer of 30 nm thick nickel film was sputtered on the DHF cleaned Si surface by PVD at a base pressure of 3×10^{-7} Torr. Argon was used as the sputtering gas to knock off the Ni atoms from a pure Ni target. Thermal annealing process was done by a RTA process to react the Ni with the Si within the diode openings. The RTA was done under a flowing nitrogen gas of 100 sccm in the temperature range of 200°C to 650°C. A well calibrated thermocouple was used to measure the temperature during RTA processes. The unreacted Ni on the HDP field oxide was removed by dipping the wafer in a 130°C heated sulphuric acid and hydrogen peroxide solution ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 4:1$) for 30 seconds. Finally, aluminum was deposited on the backside of the wafer to provide ohmic contact before diode measurement.

3.4.2 DSS diode split

For the DSS diode split, an additional implantation step was inserted into the baseline process. It is important to note that during the thermal annealing process, the reaction between the 30 nm deposited Ni and the Si substrate resulted in 54 nm (1 nm Ni consumes 1.8 nm Si to form 2.2 nm NiSi) of the Si being consumed to form 66 nm of NiSi. The implant condition for the DSS split was to ensure that the implanted dopant profile fell within the consumed Si. By simulating the implant range using SRIM on a Si substrate with a 10 nm sacrificial oxide layer, an implant energy of 15 keV using BF_2 and P resulted in a range of approximately 40 - 50 nm. Hence, after the HDP oxide removal in a DHF solution, a 10 nm new sacrificial oxide film was deposited and the simulated implant conditions were employed prior to the Ni deposition in the baseline process.

3.4.3 ELA-DSS diode split

An additional excimer laser annealing (LA) was employed in the ELA-DSS split compared to the DSS split in the previous section. The additional ELA step was introduced into the baseline after the DSS split implantation took place. As oxide layer imposed additional reflectivity to the LA, the 10 nm sacrificial oxide was removed in DHF after the DSS implant but prior to the LA step.

3.4.4 Summary of diode fabrication

A summary of different diode fabrication processes is shown in Figure 3.2 for comparison.

Figure 3.2. Process flow of the baseline, DSS and ELA-DSS diodes.

3.5 Si nanowire device fabrication

This section gives an overview of the CMOS processing of the silicon nanowire devices used in this work. In the following sub-section, a baseline device fabrication flow will be outlined. The subsequent integration of various performance enhancement techniques will be added into the baseline fabrication flow.

3.5.1 Baseline Schottky Si nanowire MOSFET fabrication flow

Active area definition

Si nanowire MOSFETs were fabricated on 8 inch silicon-on-insulator (SOI) wafers. The wafer specifications are as follows: 200-mm *p*-type (100) SOI wafers with resistivity of 5 – 10 Ω -cm and a top silicon thickness of 70nm sitting on a 150nm buried oxide. The SOI wafers were thinned down to 50nm by thermal oxidation in furnace. After the grown oxide was removed in a DHF solution, the active area was patterned by using KrF lithography in conjunction with an alternating phase shift mask. Each device consists of a thin fin (~120nm fin width) connected to two wider S/D extension regions which are in turn connected to 100 μ m by 100 μ m pads (for electrical probing). The target critical dimensions (CD) of the thin fins are 40nm to 60nm and can be achieved after photoresist (PR) trimming. The Si was etched by RIE to the endpoint until the BOX layer was exposed. Figure 3.3 shows the transferred PR pattern onto the SOI layer achieved by RIE of the 50nm top SOI layer down to the BOX layer.

Figure 3.3. Titled view SEM micrographs of active area of a single device showing the defined fin and S/D area (a) as patterned photoresist by lithography, and (b) after RIE Si etching to the BOX layer.

Si nanowire formation

Using self-limiting oxidation, the Si fins were oxidized and converted into Si nanowires. The oxidation of the Si fins was done using dry O_2 at 975°C in a furnace tube which results in a stressed limited Si nanowire formed from the Si fin. Depending on the size and ratio of the starting fin, stacked twin Si nanowires can also be formed using the self-limiting oxidation. However, only single Si nanowire or multiple Si nanowire in parallel horizontally will be used throughout this work for the reason that stacked Si nanowires often resulted in larger size discrepancy during fabrication. Figure 3.4 shows the XTEM micrographs of Si fins and Si nanowires before and after self-limiting oxidation. The Si nanowires were ‘released’ from the thermally grown oxide around them by dipping the wafer in a DHF (1:25) solution. Depending on the timing of the oxide removal in the DHF solution, the Si nanowires can be designed to be ‘fully released’ into a free standing structure as shown in Figure 3.5.

The final nanowire shape is determined by a few factors such as the shape of the Si fin before oxidation and oxidation conditions. The shape of the starting fin is not perfectly square but is slightly tapered as shown in Figure 3.4 (a). This is due to the Si

etching process that inherently produces a tapered fin profile. Moreover, top and side surfaces of the fin are exposed directly to oxygen during oxidation while the bottom surface of the fin is protected by the bottom oxide. On top of that, there is a difference in oxidation rate for the Si surface at the top, both sides and corners of the fin. It is well known that the oxidation rate of the (111) surface is larger than that of the (110) surface, which is in turn larger than the (100) surface. The faster oxidation rate at the (111) corners of the fin smoothen out the sharp corners as the oxidation process continues. All these contribute to the asymmetric oxidation rate to the various part of the Si fin. A simple illustration is given in Figure 3.4 (c) to describe how the oxidation affects the shape of the final Si nanowire. From the experiment, it is suspected that the narrow-top-wide-bottom profile of the Si fin (A) coupled with a thick bottom oxide is the main reason of obtaining a triangular shape Si nanowire (C) as the dimension of the Si fin becomes smaller. Shorter oxidation duration results in narrow-top-wide-bottom fin with rounded corners (B).

In Chapter 4, all the nanowires used were processed with shorter oxidation duration. Hence structure B was obtained and all the transistors studied in Chapter 4 were based on this structure. However, longer oxidation duration was employed in Chapter 5 and 6 nanowire transistor. Hence structure C was mostly obtained. As mentioned, the size and shape of the final nanowire is very dependent on the initial size and shape of the Si fin. While oxidation is a relatively stable process, the variation in the Si fin dimensions stems from lithography, photoresist trimming and etching is relatively large compared to the final Si fin width. It is observed that the fin width variation is in the range of ± 5 nm for a mean width of 50 nm. Due to this reason, some transistors with a slightly larger Si fin can result in nanowires with structure B, albeit at comparable dimensions/diameters as structure C.

Figure 3.4. (a) XTEM micrographs of Si fins before self-limiting oxidation, (b) after self-limiting oxidation and (c) a simple illustration of the shape of the final Si nanowire after oxidation.

Figure 3.5. (a) Tilted SEM micrograph of a released free standing Si nanowire. (b) XTEM micrograph of the Si nanowire in (a) showing the width of the Si nanowire estimated to be approximately 10 nm.

Gate stack formation

After the formation of the Si nanowires, a gate stack was formed by formation of a layer of 60 Å thermally grown silicon dioxide dielectric followed by a layer of 600 Å polysilicon gate. The polysilicon was then P doped to a dose of 5×10^{15} atoms cm^{-2} at 15 keV or BF_2 doped to a dose of 4×10^{15} atoms cm^{-2} at 15keV for N and P-MOSFET respectively. The gate doping was done by 4 quadrant implantation with 45 degrees tilt to maximize the reach of the implanted dopants to the bottom of the gate. After which, the diffusion process during RTA would ensure better coverage of dopants at the bottom of the nanowire. Then, the gate activation was performed at 950°C for 30 seconds to activate the dopants in the polysilicon gate. Gate lithography was then carried out followed by etching using Cl_2 and HBr chemistry in a RIE etcher which utilizes end point detection.

Due to the free standing nature of the Si nanowires, polysilicon stringer was formed by shadow effect of the Si nanowire S/D extensions connecting to the gate. Note that the source/drain implantation for the DSS transistor is done after the spacer has been defined. In the case of non-optimized process, there will be poly stringer left beneath the Si nanowire that is exposed and extended to the source/drain pads. After nitride deposition the poly stringer will be covered and protected from the subsequent spacer etching. The polysilicon stringer beneath the Si nanowire extensions behaves as parasitic gate which increases the overall effective gate length. Thus, meaningful analyses are difficult due to the existence of the parasitic polysilicon stringer which renders the physical gate length to be unreliable as the effective gate length. Therefore, an improved two-step gate etching was designed to first etch anisotropically to reach end point of the polysilicon gate and then to etch isotropically to remove the residual polysilicon stringer beneath the Si nanowire extensions caused by shadow effect. In the isotropic etching, an

optimized mixture of SF₆, HBr and O₂ was employed as the etchant. A low platen power was applied to reduce the directionality of the etchant ions to promote isotropic etching. Figure 3.6 shows the tilted SEM micrographs of the gate with and without employing the second isotropic etching step. A layer of 100Å LPCVD SiO₂ was then deposited followed by a layer of 100Å LPCVD Si₃N₄ which serves as the self-aligned spacer. The Si₃N₄ and SiO₂ were then etched using CF₄ chemistry in a plasma etcher utilizing end point detection which resulted in a 200Å spacer.

Figure 3.6. (a) Tilted SEM micrograph of an etched polysilicon gate with poly-Si stringer, and (b) without poly-Si stringer. (c) Schematics of a GAA Si nanowire MOSFET with (left) and without (right) poly-Si stringer.

Source/Drain silicidation

After spacer formation, self-aligned silicidation was performed. The S/D silicide films were formed by sputter depositing Ni on the devices followed by rapid thermal annealing. Silicide was formed concurrently on the polysilicon gate as well due to the blanket deposition of Ni which covers the gate. The Ni deposition and RTA conditions used for the devices were similar to the fabrication of diodes described in Section 3.4.1. The unreacted nickel on the spacers and the field area was removed by dipping the devices in a sulphuric acid and hydrogen peroxide solution ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 4:1$) for 30 seconds.

3.5.2 Si nanowire DSS MOSFET split

Generally, the DSS split for Si nanowire MOSFET fabrication was similar to the baseline, except that there was an additional S/D implantation before the S/D silicidation was performed. The S/D implant conditions for N and P-MOSFETs were P at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ at 5 keV and BF_2 at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ at 10 keV, respectively.

3.5.3 Si nanowire ELA-DSS MOSFET split

For the ELA-DSS split, a laser annealing was added after the S/D implantation similar to the sequence employed by the diode fabrication in Section 3.4.3. The experimental setup for the laser annealing was the same as explained in Section 3.2.3.

3.5.4 Summary of Si nanowire MOSFET fabrication

A summary of different Si nanowire MOSFET fabrication processes is shown in Figure 3.7 for comparison.

Figure 3.7. Process flow of the baseline, DSS and ELA-DSS Si nanowire transistors.

3.6 Analytical Simulation of Laser Annealing (LA) Process

3.6.1 Introduction

The temperature generated by interaction of laser and the irradiated material is of great importance and interest as the outcome of a thermal annealing process is generally governed by temperature. However, due to the unavailability of real time temperature measurements during the LA process, it is difficult to predict the temperature profile generated by laser irradiation. As a result, COMSOL Multiphysics® Modeling software was utilized to simulate the temperature generated in the sample during LA process. COMSOL Multiphysics® Modeling is a finite element analysis and solver package for applications in physics and engineering especially for coupled phenomena. As such, the software can be utilized to simulate heat transfer by laser irradiation onto materials.

The software can be used to simulate the generation and flow of heat in any form in its dedicated heat transfer module. As such, heating, melting and cooling of a material by laser irradiation can be simulated by incorporating temperature and phase-dependent thermo-physical and optical properties of the material. Hence, by taking into account the thermal properties (thermal conductivity, heat capacity and etc.) and optical properties (reflectivity and absorption coefficient) of different materials, the interaction of multi-layered thin films under laser irradiation can also be simulated.

The software creates an output data of the generated temperature profile in the sample as a function of time. By analyzing the temperature profile at the irradiated surface, one can tell the onset of melting by comparing the generated temperature to the material's melting point.

3.6.2 COMSOL simulation: Assumptions and accuracy

Several assumptions were made in the COMSOL algorithms and the input data. These assumptions were made to simplify the simulation problem and to save computational time. The first assumption made is that the interaction of a laser beam with materials is treated as a one-dimensional heat flow problem. In reality, the heating effect of laser irradiation on materials constitutes a three-dimensional heat flow problem. However, due to the shallow thermal diffusion distance (typically less than 1 μm) of the nanoseconds pulsed laser and the relatively large beam spot size (2 mm x 2 mm) used in the experimental setup, heat flow parallel to the surface within the laser beam spot can be neglected thus making the one-dimensional assumption valid.

The second assumption made in the simulation is that thermal conduction is responsible for local heat transfer in the irradiated material. Heat losses due to radiation or convection at the surface are neglected. In the case of nanosecond laser processing, given the time scale of interest is typically in nanoseconds, it is too short to allow substantial loss through convection from the surface.

The third assumption is the back side of the simulated material has a boundary condition set to a constant temperature. Hence the boundary acts as an infinite heat sink. Again, the assumption is valid within the short duration of the nanosecond laser processing. In addition, the thickness of the simulated material can be made much larger than the thermal diffusion length occurring within the time scale of interest.

The thermal and optical properties of the materials of interest were obtained from the literature and are shown in Appendix A. Both thermal and optical properties are functions of temperature. In other words, a material displays different thermal and/or optical properties when it is heated. Particularly, the reflectivity of a material is one of the important parameters since a slight change of the reflectivity is able to affect the incident

irradiation in percentage term. Experimentally, the reflectivity can be affected by uncleaned sample surface or native oxide.

3.6.3 Governing Equations

During the LA process, the laser light is absorbed by electron excitations in the near-surface layer of the material. The absorbed energy is converted to heat and diffuses into the inner layer of the material by thermal conduction. The equation describing the heat flux is in the form

$$\rho C_p \frac{\partial T}{\partial t} + \frac{\partial}{\partial z} \left(-k \frac{\partial T}{\partial z} \right) = Q \quad (\text{Equation 3.2})$$

where ρ is the mass density (in Kg/m³), C_p is the heat capacity (in J/Kg·K), T is the temperature of the solid materials (in Kelvin), t is time (in second), z is the depth in the solid material (in meter) with $z=0$ defined as the surface, k is the thermal conductivity (in W/m·K), and Q is the volume heat source (in W/m³).

The heat source Q in Equation 3.2 is generated by the laser and is described by

$$Q = I(z,t)\alpha \quad (\text{Equation 3.3})$$

where I is the laser intensity (in W/m²) absorbed by the solid material which is a function of time and depth, α is the absorption coefficient of the laser in the solid material (in m⁻¹). The α of a material is a function of the laser wavelength.

However, due to part of the incident laser is reflected at the material surface during LA, the amount of reflected light is governed by the reflectivity, R of the material. By taking into account of R , the absorbed laser intensity can be described by

$$I = (1 - R)I_0(t) \exp(-\alpha z) \quad (\text{Equation 3.4})$$

where $I_0(t)$ is the incident laser intensity which is a function of the time that describes the temporal profile of the laser. As it is easy to measure the strength of laser in energy

density or fluence, the measured laser fluence can then be converted to laser intensity by dividing the fluence by the FWHM of the laser pulse, t_p :

$$I_0 = \frac{F}{t_p} \quad (\text{Equation 3.5})$$

where F is the laser fluence (in J/m^2).

The initial boundary conditions at the surface where $z=0$ is defined by $T=300$ K at $t=0$. The heat flux on the boundary can be expressed by

$$q_0 = -\vec{n} \bullet \vec{q} \quad (\text{Equation 3.6})$$

where q_0 is the inward heat flux normal to the boundary, $\vec{n}$ is the normal vector of the boundary and $\vec{q}$ is the heat flux vector and can be expressed by

$$\vec{q} = -k \frac{dT}{dz} \vec{z}. \quad (\text{Equation 3.7})$$

The surface to air loss is assumed to be negligible and thus it is assumed $\frac{dT}{dz} = 0$ at $z=0$.

Since the thickness of the simulated sample is set to be greater than $10 \mu\text{m}$ which is sufficiently larger than the thermal diffusion length during the LA process. Hence the heat flux q_0 at the back of the sample is set to zero with $T = 300$ K at any time.

3.7 Summary

Various topics in fabrication equipment as well as materials and electrical characterization techniques of the diodes and the transistors of the research project were briefly discussed. The device fabrication processes for the diodes and the transistors were also described with emphasis on several key process steps. An analytical simulation of the laser annealing process to predict the temperature of the irradiated surface was also

introduced and discussed. Unless otherwise stated, the subsequent chapters follow the experimental and simulation procedures described in this chapter.

Chapter 4 NICKEL SILICIDE INTRUSION IN SI NANOWIRE SCHOTTKY BARRIER MOSFET

4.1 Motivation and objectives

The continued scaling of S/D junction depth in conventional MOSFETs results in several limiting factors including increased sheet resistance and limitations in doping or activation techniques to achieve sharp lateral doping profiles. Schottky barrier MOSFET has an architecture in which the metallic S/D regions are in direct contact with the transistor channel can essentially eliminate the S/D parasitic resistance and provide abrupt junction interfaces [20, 50, 52]. Recently, the effect of gate modulation on Schottky barrier thickness at source/drain has been shown to increase tunneling current [145]. However, this effect is significant when the intruded silicide into the channel overlaps with the gate [21], but controlling the distance of silicide intrusion in nanowire proves to be more challenging than in a 2-D planar transistor [146, 147].

While work on silicide intrusion on bottom-up nanowires has been investigated [146], nickel silicide intrusion in gated nanowires and its impact on Schottky transistor's performance on top-down nanowire transistor by method of lithography are not well studied. In this chapter, we aim to study and demonstrate controllable silicide intrusion using different RTA conditions in top-down nanowire transistor. The d.c. performance of the fabricated device is presented.

4.2 Experimental

By using the baseline fabrication process for Si nanowire MOSFET described in Chapter 3, different silicidation schemes have been carried out to study the amount of silicide intrusion into the Si nanowire channel as well as the silicide phase formed at the

S/D. The silicidation splits with various Ni thicknesses and RTA conditions are summarized in Table 4.1.

Table 4.1. Summary of different silicidation splits used for fabricating Schottky barrier MOSFETs with Si nanowire and thin body architecture.

Split	Ni thickness (nm)	RTA1 275 °C		Unreacted Ni removal after RTA1	RTA2 450 °C 30 s
		30 s	60 s		
1	14	•		•	•
2	14		•	•	•
3	30	•		•	•
4	30		•	•	•
5	14				•

In this experiment, a two-step silicidation scheme was introduced. The first RTA (RTA1) was aimed to control the diffusion speed of Ni during silicidation at a relatively low temperature of 275 °C and the second RTA (RTA2) was aimed to transform the silicide into a lower resistivity phase by fully consuming the remaining Si at the S/D after the unreacted Ni is removed between RTA1 and RTA2. Split no. 5 was a control sample of only one RTA at 450 °C for 30 s with 14 nm deposited Ni. The choice for Ni thickness of 14 nm as control was selected because the remaining S/D Si thickness was approximately 30 nm, where silicidation to form NiSi will need a thickness ratio of Ni:Si = 1:1.8 [64, 65, 148]. To fully consume the 30 nm S/D Si, a Ni film with a thickness of 16.7 nm is required. 14 nm is chosen as it allows discrepancies resulted from the non-uniformity of the SOI substrate used as well as the fluctuation of the sputter deposition rate of the sputtering tool.

The fabricated wafer contained nanowire as well as thin body devices. For the thin body devices, the Si thickness was the same as the nanowire diameter, and differed from the nanowire with a width (W) of 1 μ m. The SEM micrograph of the fabricated device and the XTEM micrographs of the Si nanowire channel are shown in Figure 4.1. The XTEM micrograph of the device shows a Ω -shaped gate structure around the Si nanowire channels. This is due to incomplete separation between the released Si nanowires in DHF solution, resulting in the Si nanowire connected to the underlying BOX layer.

Figure 4.1. (a) Tilted SEM micrograph of a twin Si nanowire omega-gate Schottky barrier MOSFET. (b) XTEM micrograph showing an omega shape gate with Si nanowires with diameter of approximately 30nm. The dashed lines are guide to eyes.

4.3 Silicide intrusion

4.3.1 Silicide intrusion in silicon thin body

Figures 4.2 (a) and (b) show the X-TEM micrographs of a thin body Schottky barrier MOSFET after RTA1 for 30 s of Split no. 1 (see Table 4.1) was performed and the unreacted Ni was removed. From the dark contrast region labeled as Ni_xSi_y in Figure 4.2 (a) the S/D region appears to be fully silicided after RTA1 but the high magnification TEM micrograph shown in Figure 4.2 (b) reveals that the silicide layer does not fully consume the S/D Si. The observation correlates well with the fact that the Ni thickness used by Split no. 1 is 14 nm. The TEM/EDX analysis results as shown in Figure 4.2 (b) show that the ratio of Si to Ni is approximately 1.2 – 1.3.

Figure 4.2. (a) XTEM micrograph showing a thin body device after annealing at RTA1 30 s with 14 nm Ni. (b) A high magnification micrograph near the gate edge showing the nickel silicide formed at the S/D region with the associated EDX analysis results included. The dashed white lines are guide to eyes on the silicide-silicon interface.

The previous studies [64, 73, 149-151] on nickel silicide confirmed that at 275°C, the first silicide phase to form is Ni_2Si , which has a Si to Ni ratio of 0.5. Since Ni_2Si and NiSi phases are formed sequentially (i.e., the Walser and Bene’s rule [152] for first phase

formation and the Tsaur's rule [153] for subsequent phase formation), NiSi cannot be formed before all Ni atoms are reacted to form Ni₂Si. With a ratio of 1.2-1.3 between Si and Ni, the result suggests that the silicide formed at the S/D is not Ni₂Si because its Ni to Si ratio is smaller than unity. Entirely single phase NiSi is also less likely for a low annealing temperature at 275°C for only 30 s. Other studies [73, 148-150] pointed out that silicide formed at this temperature is diffusion limited and the silicide formed is always Ni₂Si first although NiSi formation at low temperature (270-370°C) has also been reported elsewhere [154], but it is only possible if annealing is prolonged when all Ni atoms have completely reacted with Si atoms to form Ni₂Si. NiSi₂ is ruled out from the consideration because thermodynamically, NiSi₂ only forms above 750°C [64, 65, 148]. Thus, the most plausible explanation is a mixture of Ni₂Si, NiSi and Si. The EDX analysis of locations near the silicide edge might also detect the Si signal from nearby Si, hence it slightly increases the Si ratio.

Also shown in Figure 4.2 (b), the silicide-silicon interface at the S/D is right below the spacer, near the poly-Si gate edge. Since the oxide beneath the 20nm-thick silicon nitride spacer was removed in DHF before Ni sputtering, in the worst case scenario, Ni atoms did not fill the void beneath the spacer. Therefore, the maximum silicide intrusion in the thin body device is approximately 20nm, determined from the spacer edge to the silicide-silicon interface beneath the spacer.

Figure 4.3. XTEM micrograph showing a thin body device after annealed at RTA1 30 s with 30 nm Ni. (a) TEM/EDX analysis at the S/D region. The dotted white lines indicate silicide-silicon interface. (b) Magnified TEM micrograph at the gate edge showing silicide intrusion length of approximately 40 nm.

Next, a 30 nm-thick Ni was used for silicidation for 30 s (Split 3). The XTEM micrograph of the silicided device is shown in Figure 4.3. Full consumption of silicon by Ni is observed. This is a direct result of having more Ni atoms to react with Si. The TEM/EDX analysis at the S/D silicide reveals that the ratio of Si to Ni is 0.7-0.8 which suggests that the silicide consists of Ni_2Si and NiSi . It is worth to point out that Ni_3Si_2 also has a Si to Ni ratio 0.67, which is close to the ratio of 0.7. However, Gas *et al.* suggested that Ni_3Si_2 formation is dominated by nucleation and there is a nucleation barrier to the formation of Ni_3Si_2 below 470°C [155]. Recently, Lavoie *et al.* also concluded the absence of Ni_3Si_2 below 300°C [156, 157]. Thus, we strongly believe the silicide at the S/D region is a mixture of Ni-rich silicides such as Ni_3Si , Ni_2Si and NiSi . Figure 4.3 (b) clearly indicates that the length from silicide-silicon interface to the nitride spacer edge is approximately 40 nm. This result is consistent with the use of thicker Ni layer for silicidation, which should form thicker silicide.

4.3.2 Impact of RTA temperature on silicide intrusion in Si nanowire

Figure 4.4. XTEM micrograph showing silicide intrusion in Si nanowire devices annealed at different RTA conditions. (a) Si nanowire device annealed at RTA2 only, (b) Si nanowire annealed at RTA1 only. 14 nm Ni was used for silicidation for both cases.

Figure 4.4 shows the cross-sectional TEM micrograph along the wire direction of Si nanowire devices annealed at 2 different RTA conditions, namely RTA1 (275°C) 30 s and RTA2 (450°C) 30 s, both with a layer of 14 nm Ni (Split 1 vs. Split 5). It is evident in

Figure 4.4 (a) that silicide intrusion lengths into the Si nanowire channel from both sides of the gate are different and severe, with 170 nm at one side and 260 nm at another. The significant difference in the silicide intrusion lengths at 450°C suggests that silicidation is rapid and sensitive to variations e.g. Si nanowire diameter, S/D Si thickness or Ni thickness.

As opposed to 450°C, Figure 4.4 (b) shows that RTA1 at a low 275°C produces intrusion of about 30 nm as mentioned in the previous section and has consistent electrical performance, which will be shown in the subsequent sections. This also implies that the intrusion length is consistent and reproducible.

Figure 4.5. XTEM micrograph showing the cross-sectional view of a fully silicided Si nanowire i.e., electrically short from source to drain, after silicidation at RTA2. TEM/EDX analysis was performed at the center of the silicided nanowire.

As the EDX analysis on the TEM sample with an embedded Si nanowire in Figure 4.4 may yield inaccurate result, a TEM sample perpendicular to the fully silicided Si nanowire would give better accuracy. In some cases where intruded silicides from both ends meet in the middle of a Si nanowire, the device is electrically shorted. Cross sectional TEM/EDX analysis at the center of the fully silicided Si nanowire shown in

Figure 4.5 shows that the Ni to Si ratio is about 1.4. This is interesting as the 14 nm Ni is expected to fully consume the 30 nm Si at the S/D to form the preferred NiSi phase. However, with a Ni:Si close to 1.5, the silicide phase is nickel-rich and is likely to be Ni_3Si_2 . Ni_3Si_2 is a metastable phase that only forms under the condition of an initial Ni:Si atomic ratio of 3:2 and annealed at temperature higher than 300°C [156, 157]. As silicidation takes place at 450°C, Ni reacts with Si at the S/D region to form Ni_2Si , then NiSi. Subsequently, Ni atoms diffuse into the Si nanowire and react with the Si atoms there. It is believed that due to the limited Si source in the Si nanowire, the effective ratio of Ni to Si will be larger than 1. In the case of Figure 4.5, the ratio is 1.5 and a metastable nickel silicide phase is formed in the Si nanowire.

4.3.3 Impact of Ni thickness on silicide intrusion in Si nanowire

The effect of Ni thickness on silicide intrusion into Si nanowire was also studied by using two Ni film thicknesses, namely 14 nm and 30 nm. The corresponding conditions used are Split no. 2 and Split no. 4 in Table 4.1.

In Figure 4.6, the TEM micrograph depicts the cross-sectional view of a Si nanowire Schottky barrier MOSFET. The TEM sample was prepared along the Si nanowire with the Si nanowire embedded within the sample. With a layer of 14 nm Ni used for silicidation, an atomically abrupt silicide-silicon interface in the Si nanowire was observed at the spacer to poly Si interface, approximately 20-30 nm from the outer spacer edge, implying the worst case intrusion of about 30 nm. This value is slightly more than the intrusion length observed in the thin body device, i.e., 20 nm. With a layer of 30 nm Ni, the intrusion length of silicide as measured from the spacer edge is 40 nm, similar to that of the thin body device. Silicidation on Si nanowire is believed to be much more complicated as compared to the case of thin film or bulk Si due to its 1-dimensional

nature. Silicidation rate and hence, the intrusion length in Si nanowire is closely related to its volume, or diameter.

Unlike the case of the thin body device, EDX analysis at the region near the silicide-silicon interface is not possible because the Si nanowire is embedded in SiO₂ and some amorphous Si (from poly-Si) resulted from the TEM sample preparation by the Focus Ion Beam (FIB) technique. If EDX analysis is performed here, the Si signals from the surrounding SiO₂ and amorphous Si can be detected as well and can render misleading ratio between Ni and Si.

Figure 4.6. XTEM micrograph showing a Si nanowire device after annealed at RTA1 30 s with (a) 14 nm Ni and (b) 30 nm Ni. The insets show a magnified views of the silicide-silicon interface at the gate edge.

4.4 Electrical Characterization

4.4.1 Intrusion by measurement

Silicide intrusion in Si nanowire or thin body devices can be observed roughly by measuring the device's DC performance. This can be done by observing the device with a low resistive path between source and drain ($I_S = I_D$ and having an ohmic I - V

characteristic), and without shorting to the gate (I_G in the range of less than a pico ampere). As the fabricated devices have physical gate lengths of larger than 60 nm and a 20 nm-spacer at each side, accurate determination of a low resistive path between source and drain for the low temperature RTA annealed devices is difficult because:

1. The variation of the gate length is in the range of ± 10 nm as confirmed by SEM measurement for device critical dimensions (CD).
2. The silicide intrusion length is in the range of 30-40 nm on each side which implies a combined intrusion length of 60-80 nm, a value close to the smallest gate length CD.
3. There is an estimated ± 10 nm variation in silicide intrusion length. However, due to the nature of the XTEM which is both challenging and costly as a characterization technique, only one XTEM was performed on each experimental split.

However, for the higher temperature RTA (450°C) annealed devices, as the intrusion length can range from 170 - 260 nm as shown in Figure 4.6 (a), an array of devices with increasing gate length provide a qualitative observation of the intrusion. By examining the RTA condition at which a nanowire channel of a certain length is electrically shorted from source to drain, one can have a gauge of how much the silicide has encroached or intruded into the nanowire from the S/D.

As shown in Table 4.2, there are shorted as well as working devices annealed at RTA1 for the smallest gate length. The physical CDs shown in Table 2 are the average CD from measuring several devices on different dies of the same wafer. The results are consistent with the intrusion lengths of 30 – 40 nm mentioned in the previous section. In fact, during the measurement of other devices with the same silicidation conditions and for the 70 nm gate length, it was found that some devices were working while others were

shorted. However, for the devices with a 110 nm gate length, it is obvious that no devices were shorted. With the variations in CD of about ± 10 nm across the wafer, it is apparent that the variation in silicide intrusion length is small and the intrusion is reproducible at low temperature anneal. In the case of a single step annealing at RTA2 (450°C), the longest shorted device has a physical gate CD of 320 nm. All the 700 nm-gate devices did not suffer the problem. From the previous section, the estimated total silicide intrusion at RTA2 is about 430 nm (170 nm + 260 nm). Again, this result is consistent with the observation obtained from the TEM analysis.

Table 4.2. Summary of an array of devices indicating shorted and working devices for various silicidation splits.

Physical CD (Poly + spacer) nm	RTA1 (275°C)				RTA2 14 nm Ni 450°C 30 s
	14 nm Ni		30 nm Ni		
	30 s	60 s	30 s	60 s	
70	✓	✓	X	✓	✓
110	X	X	X	X	✓
160	X	X	X	X	✓
200	X	X	X	X	✓
240	X	X	X	X	✓
320	X	X	X	X	✓
700	X	X	X	X	X
1700	X	X	X	X	X

✓ indicates a short from source to drain.
X indicates no short and device is working.

4.4.2 Thin body against Si nanowire

This section analyzes the differences in the electrical performance between thin body and Si nanowire devices. The I_D - V_G and I_D - V_D characteristics of these devices are compared and analyzed.

The I_D - V_G characteristics shown in Figure 4.7 (a) confirm the ambipolar characteristic of a Schottky barrier MOSFET. If the barrier heights for holes and electrons are the same, the I - V curve will be symmetrical about the flatband voltage. The asymmetry I - V characteristics observed in Figure 4.7 (a) proves that the hole barrier height is lower than the electron barrier height, as the hole current at negative gate bias is larger than that of the electron current at the same positive gate bias. As a result, the fabricated Si nanowire Schottky barrier MOSFETs here will be treated as p-MOSFETs.

Figure 4.7 Si nanowire Schottky barrier MOSFETs annealed at RTA1 30 s with 30 nm Ni. (a) I_D - V_G and (b) I_D - V_D for the two devices. I_D - V_D in step of $V_G = 1V$.

The carrier transport mechanism across a Schottky barrier can be approximated by a combination of thermionic and tunneling current (i.e. $I = I_{TE} + I_{TN}$) and can be expressed in the forms of

$$I_{TE} = AA^* T^2 \exp\left(-\frac{q(\phi_b + \psi_c)}{kT}\right) = I_s \exp\left(-\frac{q\psi_c}{kT}\right) \quad (\text{Equation 4.1})$$

and

$$I_{TN} = \frac{Aq^2 E^2}{8\pi h \phi} \exp\left[-\frac{8\pi}{3hqE} \{2m^* (q\phi_b)^3\}^{1/2}\right] \quad (\text{Equation 4.2})$$

where ϕ_b is the SBH, Ψ_c is the channel potential (conduction band across the channel modulated by the external gate voltage), k is the Boltzmann constant, T is the temperature, q is the electronic charge, A is the diode area, A^* is the Richardson constant, E is the electric field across ϕ_b , h is the Planck's constant and m^* is the effective mass.

The relative contributions from I_{TE} and I_{TN} are dependent on the shape of the Schottky barrier. An energy value E_{00} , defined as diffusion potential of an electron across a Schottky barrier can be used to determine the dominant current contribution [40, 158]. Quantitatively, $E_{00} = q\hbar / 2\sqrt{N/m^*\epsilon_s}$, where $\hbar$ is the reduced Planck's constant, m^* is the effective mass of the electron, ϵ_s is the semiconductor permittivity, and N is the carrier density in the semiconductor.

At small gate bias (V_G), $E_{00} < kT$, thermionic emission dominates the carrier transport across the ϕ_b . Hence, I_{TE} dominates the current flow and only carriers with energy greater than $\phi_b + \Psi_c$ contribute to the current flow. From Equation 4.1, I_{TE} varies exponentially with Ψ_c and the Schottky barrier MOSFET behaves like a conventional MOSFET with a subthreshold slope $\approx \ln 10(kT/q)$.

At higher V_g values, $E_{00} > kT$, tunneling dominates the carrier transport across the Schottky barrier. Hence, I_{TN} dominates the current flow. From Equation 4.2, I_{TN} is dependent on E and hence the shape of the Schottky barrier. E is a function of the gate oxide thickness and it implies that the rate of increase in I_{TN} will be sensitive to both V_G and the gate oxide thickness. For approximation, the 2-dimensional cross-sectional view along the direction of a nanowire can be considered as a thin body. The subthreshold slope of a thin body Schottky barrier MOSFET in this region can be expressed as subthreshold slope $\approx \ln 10(kT/q)(1 - \exp(-d/(\epsilon_{si}t_{si}t_{ox}/\epsilon_{ox})^{1/2}))^{-1}$ where d is the thickness of the Schottky Barrier beyond which the tunneling current can be neglected, ϵ_{si} and ϵ_{ox} are

the Si and SiO₂ dielectric constants, respectively, and t_{si} and t_{ox} are the Si and SiO₂ thicknesses respectively. Thus, the subthreshold slope in the tunneling region will be larger than that in the thermionic region, as shown in Figure 4.7 (a).

It is generally agreed that Si nanowire has a superior gate-to-channel electrostatic control than thin body device, provided the gate dielectric thicknesses are the same. As a gate voltage is applied, the Si nanowire drives significantly more current than the thin body device as shown in Figure 4.7 (b). Note that the I_D - V_G and I_D - V_D are plotted using absolute drain current which has not been normalized. The average diameter of the Si nanowires is approximately 30 nm while the width of the thin body is 1 μ m. Equation 4.2 shows that I_{TN} can be increased with an increased electric field across the Schottky barrier. The Ω -shaped gate structure in the Si nanowire device provides enhanced transverse gate-to-channel electric field as compared to the top gate structure of the thin body device. The vector component of the enhanced electric field adds on to the field across the Schottky barrier which increases the I_{TN} component and hence the total current. In other words, as V_G is applied on the gate, the gate-to-channel electric field at the source side reduces the Schottky barrier width. The thinning in the barrier width results in a higher tunneling current. Therefore, the major contributing factor for higher drive current with the Si nanowire architecture is the improved gate bias modulation on the Schottky barrier width in a Schottky barrier MOSFET. However, such modulation on the Schottky barrier width is a phenomenon that applies to both electron and hole. Barrier width thinning causes the tunneling probability of both electron and hole to increase. Therefore, it accounts for the higher drive current in Si nanowire than in thin body. Also, note that at $V_D = -0.05$ V and under positive V_G , the Si nanowire device has a steeper increment of the electron current than the thin body. This is due to a more effective Schottky barrier width thinning in the Si nanowire than that of the thin body.

Based on Figure 4.7 (a), at a low V_D of -0.05 V, it is apparent that Si nanowire also outperforms the thin body device in terms of short channel effect immunity. The subthreshold slope of the Si nanowire device is 150mV/decade whereas that of the thin body device is 210mV/dec. Peng *et al.* suggested using subthreshold slope of a Schottky barrier MOSFET as a robust indicator for carrier injection efficiency [159]. Under the effect of a strong external electric field, band bending occurs in the semiconductor near the metal-semiconductor contact results in thinning of the barrier. The magnitude of external electric field acting on the semiconductor channel is highly dependent on the architecture of the device as it means how effective the gate bias is modulating the Schottky barrier thinning. The steeper subthreshold slope shown in a Si nanowire MOSFET is an evidence that it has improved carrier injection compared to the thin body MOSFET.

The leakage current in the Si nanowire device is observed to be one order of magnitude lower than that of the thin body device at $V_G = 0$ V. The lower leakage observed in Si nanowire is believed to be due to a smaller contact area and the enhanced short channel effect immunity from the omega shape gate, as compared to thin body that has a larger contact area and the top gate design.

4.4.3 Impact of RTA temperature (RTA1 vs. RTA2)

This section examines the effect of low temperature (RTA1, 275°C) against the control temperature (RTA2, 450°C) annealing on the electrical performance of Si nanowire Schottky barrier MOSFETs.

Figure 4.8 (a) shows the subthreshold slope for the Si nanowire devices annealed at the two RTA conditions with the 14 nm Ni. The data point for the devices annealed at RTA2 only started at 700 nm due to the mentioned silicide intrusion that shorts the source

to the drain at shorter channel length. However, it is significant that from 700 nm onwards, the subthreshold slopes for both devices annealed at RTA1 and RTA2 are almost identical. Figure 4.8 (b) compares the I_D - V_G for the 700 nm gate length devices annealed at RTA1 and RTA2, respectively.

Figure 4.8. Electrical characteristics of Si nanowire Schottky barrier MOSFETs annealed at RTA1 and RTA2 with a 14 nm Ni. (a) Subthreshold slope vs. gate length and, (b) I_D - V_G for the 700 nm gate length devices annealed at two RTA conditions.

It is noticeable at low gate and low drain (-0.05 V) biases, the subthreshold regions are closely resembled. However, as the V_G increases, the current of the device

annealed at RTA1 is always lower than that of the device annealed at RTA2. This observation is reasonable as a 700 nm physical gate length device annealed at RTA2 should have an intrusion in the Si nanowire channel of about 400 nm. In other words, this gives only an effective channel length of about 300 nm. In addition, for the device annealed at RTA2, the location of the Schottky barrier is deeply beneath the gate, which means a better gate modulation from the coupling of the gate electric field. Hence, the RTA2 device drives more current than the RTA1 device when a same V_G is applied.

4.4.4 Impact of 2-step RTA

Figure 4.9 (a) shows the changes in the short channel performance after RTA2 of the pre-annealed Si nanowire Schottky barrier MOSFETs at RTA1. The 4nm-Ni devices show a remarkable improvement in the sub-threshold slope, whereas the 30 nm-Ni devices show only minimal improvement at gate lengths larger than 200 nm. The degradation in the sub-threshold slope at a shorter gate length observed in the 30 nm-Ni devices might be due to the slight silicide intrusion after RTA2 anneal. However, this intrusion length is observed to be very small during electrical measurement as almost all of the smallest working devices (not shorted from source to drain) as shown in Table 4.2 measured after RTA1 anneal still functional after the RTA2 anneal.

Figure 4.9 (b) compares the I_D - V_G characteristics of a RTA1 pre-annealed Si nanowire Schottky barrier MOSFET before and after a second RTA2 anneal. It is very clear that after RTA2, the subthreshold region shows improvement although there is minimal improvement in the drive current at higher drain bias ($V_D = -2.5V$). Overall, the I - V characteristics of the Schottky barrier MOSFET before and after the second RTA2 anneal are similar due to minimal changes in the intrusion length.

Figure 4.9. Effect of a 2-step RTA on Si nanowire Schottky barrier MOSFETs. (a) subthreshold slope before and after RTA2 anneal for devices pre-annealed at RTA1 60 s. (b) I_D - V_G of a device with a 4 nm Ni before and after RTA2 second anneal.

4.5 Summary

A repeatable silicide intrusion of sub-40 nm into a 30 nm diameter Si nanowire was developed and demonstrated by using a proposed 2-step silicidation at 275°C and 450°C. It is found that the effect of the RTA temperature is the dominant factor in the silicide intrusion length. The intrusion can be controlled by using a relatively low RTA1 temperature at 275°C as compared to a severe intrusion with large and different intrusion lengths from S/D at 450°C. By using the proposed RTA1, the choice of the Ni thickness

used is rather less critical which was found to be differed by only 10 nm in the intrusion length by increasing the Ni thickness from 14 nm to 30 nm. Furthermore, with RTA1 the intrusions in Si nanowire and in Si thin body are found to be almost identical.

Electrical characterization was also performed and the 2-step annealing was found to be effective in fabricating silicided S/D Si nanowire Schottky barrier MOSFET with reproducible d.c. characteristics. The findings suggest that the silicide intrusion into Si nanowires can be well controlled and is repeatable by employing the proposed 2-step annealing process.

Chapter 5 DOPANT SEGREGATED SCHOTTKY (DSS) DEVICES

5.1 Introduction

Schottky barrier MOSFETs have been proposed to replace conventional MOSFETs due to their lower sheet resistance and abrupt junction usually formed by metal silicides. Schottky Barrier MOSFETs, however, suffer from relatively high contact resistance which is related to the SBH formed at the MS junction. Hence, two approaches have been proposed to reduce the contact resistance. Firstly, by using noble or rare earth metals such as Pt, Er, Dy or Yb, lower SBH can be achieved [43, 45, 48, 49, 160]. Secondly, metal silicide can be formed on an ultra shallow doped region to pile up the dopants at the MS interface or commonly known as dopant segregation [23, 27, 51]. In this chapter, dopant segregation is proposed to be implemented in CMOS due to its compatibility in Si process. In the first stage, dopant segregation on simple back contacted diodes is studied and analyzed electrically and chemically. Subsequently, dopant segregation is incorporated in Si nanowire MOSFETs with a GAA structure free of poly-Si stringer. The devices are electrically characterized and exhibit excellent performance in terms of I_{ON}/I_{OFF} , subthreshold swing as well as showing a much reduced series resistance as compared to Schottky barrier MOSFETs due to the shallow dopant layer formed at the interface that effectively lowers the SBH.

5.2 DSS diode

To study the electrical and chemical properties of DSS contact, DSS diodes were fabricated using methodology as described in Section 3.4.2 where p- and n-type DSS diodes were implanted with BF_2 and phosphorus respectively. I - V measurement and

characterization on the chemical profiles of dopants were performed to investigate the relationship between the electrical and chemical characteristics.

5.2.1 Electrical characterization

Table 5.1 shows the conditions employed to achieve dopant segregation of boron and phosphorus. Electrical characteristics of the DSS diodes were studied.

Table 5.1. Split table for boron, phosphorus and arsenic segregation.

<div>RTA2 Silicidation temperature</div> <div>Dose</div>	$1\times10^{14}\text{ cm}^{-2}$ (low)	$1\times10^{15}\text{ cm}^{-2}$ (high)
450°C (low)	✓	✓
650°C (high)	✓	✓

Figure 5.1 shows the I - V characteristics of the BF_2 implanted p-type DSS diodes. First we examine the effect of BF_2 dose by comparing the triangle and square markers. The I - V results show that diodes with higher dose drive larger forward and reverse currents across the MS junction. Intuitively, by increasing the BF_2 dose one would expect an increase in the segregated boron concentration which leads to a lower contact resistance of the MS junction. Also, the low dose diodes behave in a way that is almost independent from silicidation temperatures used at least in the study. This can be seen as the overlapping between the solid and open square curves. However, as the dose is increased to $1\times10^{15}\text{ cm}^{-2}$, deviations between different silicidation temperatures can be observed. Clearly, the solid triangle curve which represents the diode silicided at 650°C is more symmetrical than the one with 450°C. The results suggest that to achieve better linearity in an ohmic contact, boron segregation should be done at higher doses with

higher silicidation temperatures so that the nickel silicide film morphology is not compromised i.e., transformation into NiSi₂ or agglomeration into silicide islands.

Figure 5.1. *I-V* characteristics of p-type diodes implanted with BF₂ at various doses and annealing conditions. p-sub in black line denotes the reference Schottky diode fabricated by NiSi/p-Si.

Figure 5.2 shows the *I-V* characteristics of phosphorus implanted n-type DSS diodes. It is noticed that the patterns are different from the BF₂ implanted DSS diodes. The phosphorus implanted DSS diodes exhibit a stronger temperature dependent behavior and a weaker dependence on the dose. The dependence on the dose can only be observed at a lower silicidation temperature of 450°C where the *I-V* curve of the high dose diode (open triangles) is significantly more symmetrical than that of the low dose diode (open squares). Once the silicidation temperature is raised to 650°C, the *I-V* curve of high and low dose diodes are almost indistinguishable from one another. Furthermore, the reverse currents of the diodes processed at the high temperature are consistently higher than that processed at the lower temperature. A stunning example is the low dose diode silicided at 650°C (solid squares) is a better ohmic contact than the high dose diode silicided at 450°C (open triangles). The result also show that both the dose and silicidation temperature play

critical roles in obtaining a good ohmic contact. However, the difference from the boron segregation is that the impact of silicidation temperature on the phosphorus segregation is more dominant than the dose used, at least within the parameters used in this study.

Figure 5.2. *I-V* characteristics of n-type diodes implanted with phosphorus at various doses and annealing conditions. n-sub in black line denotes the reference Schottky diode fabricated by NiSi/n-Si.

Figure 5.3 shows a cross-sectional TEM micrograph of a nickel silicide film formed on the BF₂ implanted Si. The deposited Ni was 30 nm and 15 nm for BF₂ and phosphorus sample, respectively while the silicidation condition was 650°C for 30 seconds and the silicide formed was NiSi as shown by the EDX analysis. Phase transformation to NiSi₂ was not observed until 700 – 750°C on the boron or phosphorus doped Si. The silicide film formed on the BF₂ sample is clearly smoother than that on the phosphorus sample.

Figure 5.3. Cross-sectional TEM micrograph of a nickel silicide film formed on (a) BF_2 implanted and (b) phosphorus implanted Si. EDX analysis result for the phosphorus sample is shown in inset of (b).

5.2.2 Chemical characterization

Since it is found that p-type diodes with boron and n-type diodes with phosphorus are beneficial in obtaining ohmic contact with good linearity at a higher dose of $1 \times 10^{15} \text{ cm}^{-2}$, SIMS profiles on these two doped samples have been performed.

Figure 5.4 shows the boron profiles before and after silicidation at 450°C for 30 seconds. The 30 nm Ni reacted with Si to form 66 nm of NiSi shown in the cross-sectional TEM in Figure 5.3 (a) is also confirmed by the SIMS analysis where the Ni signals decrease remarkably at the NiSi/Si region marked as the shaded area in Figure 5.4. Also, the most unique feature is seen as a hump on the red colour boron profile after silicidation, indicated as DS for dopant segregation. The hump relating to a ‘pile up’ of boron atoms is observed to overlap the NiSi/Si interface. This observation is consistent with the previously reported dopant segregation work [21, 27]. The segregated boron concentration is approximately $1 \times 10^{19} \text{ cm}^{-3}$, which is almost about one order of magnitude higher than the as-implanted concentration at the same depth.

Figure 5.4. Boron and nickel profiles of BF_2 implanted samples. Segregated boron appears as a hump around the NiSi/Si interface region. Silicidation condition was 450°C , 30 seconds.

Figure 5.5 shows the phosphorus profiles before and after silicidation. Ni signals are also shown for reference. There appears to be a double-hump feature for phosphorus profiles after silicidation. This is explained by the rough NiSi formed on the phosphorus implanted Si shown in Figure 5.3 (b). The first hump (~ 20 nm from the NiSi surface) may be due to the phosphorus segregation around the thinner NiSi while the second hump (~ 40 nm from the NiSi surface) is formed around the thicker NiSi. Since it is electrically observed that the phosphorus implanted diodes have stronger dependence on temperature, it is of interest to investigate the impact of silicidation temperature on the phosphorus profile. It is found that silicidation at 450°C and 550°C yield no significant difference in the phosphorus profiles. Both profiles have a phosphorus concentration of approximately one order of magnitude higher than the as-implanted profile at the NiSi/Si interface. Thus, it is convinced that the electrical improvement associated with the higher silicidation temperature at 550°C is a consequence of a higher electrically active phosphorus concentration, given that the chemical concentrations determined by the SIMS analysis are the same.

Figure 5.5. Phosphorus and nickel profiles of phosphorus implanted samples. Segregated phosphorus appears as a hump around the NiSi/Si interface region. Silicidation conditions were 450°C and 550°C, 30 seconds.

Although there is work reported in the literature that shows higher dopant segregation concentration with higher silicidation/annealing temperature [27, 60], it is important to note that the electrically active dopant concentration should be limited by the solubility at the interface. Also, the I - V characterization method using back contacted diode may not reflect the exact nature of the MS contact as it encompasses both the contact as well as the series resistance from the substrate. As the contact resistance becomes much lower than the series resistance, the I - V characteristic ultimately shows only the series resistance of the substrate. Other than that, the bulk sample used to study the chemical concentration is inherently one dimensional in nature. When this is being translated into silicon nanowire which is three dimensional (dopants can diffuse along and perpendicular to the wire axis), the Si is no longer semi-infinite. It is known that dopants tend to out segregate to the wire surface due to minimization of surface energy [161, 162]. The out segregation inevitably reduces the concentration in the wire [163]. Nevertheless,

the simple back contacted diodes provide ample information on the impact of dose and silicidation temperature, when combined with the SIMS analysis, will aid in the analysis of the DSS nanowire transistor in the next section.

5.3 Si nanowire DSS transistor

By capitalizing on the electrical and chemical analyses of the DSS diodes, DSS transistors were fabricated using methods as described in Section 3.3 and the device performance was carefully studied. The S/D implant species were BF_2 and phosphorus for PFETs and NFETs, respectively.

The SEM micrograph of a twin nanowire DSS MOSFET is shown in Figure 5.6 (a). The smallest gate length achievable in this study was approximately 30 to 50 nm using extreme photoresist trimming technique described in Chapter 3. Cross-sectional TEM micrographs reveal that DSS PFETs have slightly narrower nanowires compared to NFETs as shown in Figure 5.6 (b) and (c). Typically, PFET's nanowire width is about 10 nm while NFET's is about 20 nm. The difference in the nanowire width is a result of the fabrication of P- and NFETs on different wafers. In this case, the PFETs underwent a longer thermal oxidation for nanowire formation.

Figure 5.6. (a) Tilted SEM micrograph of a twin Si nanowire channel MOSFET after poly-Si gate etch. The L_G is approximately 50nm. The top-right-corner inset shows the enlarged view of the Si nanowire extension from the GAA channel free of poly-Si stringer. Cross-sectional TEM micrograph of nanowire channel for (b) PFET and (c) NFET.

5.3.1 Electrical transfer characteristics

Figure 5.7. I_D - V_G characteristics of the DSS and Schottky barrier PFETs.

Schottky barrier MOSFETs fabricated with NiSi as the S/D usually have a slightly lower SBH for holes than the SBH for electrons due to Fermi level pinning nearer to the valence band edge. Though it is ambipolar in nature, the Schottky barrier MOSFET with NiSi S/D is treated as a PFET in this study for its slightly lower SBH for holes.

Figure 5.7 shows the I_D - V_G characteristics of the DSS and Schottky barrier PFETs with a similar gate length of 50 nm. It is remarkable that the DSS PFET shows significant improved transistor characteristics compared to the Schottky barrier PFET. The Schottky barrier PFET's I_D - V_G curve indicates a typical ambipolar characteristic commonly seen in Schottky barrier devices. This is due to the near mid-gap SBH at the S/D, which has a SBH of 0.67 eV for electrons and a SBH of 0.45 eV for holes by using NiSi. The channel is a lightly doped ($1 \times 10^{15} \text{ cm}^{-3}$) p-type Si nanowire. When the gate overdrive is negatively biased ($V_G - V_{T,\text{sat}} < 0$), the channel is in accumulation mode and current is conducted by the transport of holes from the source side to the channel. When the gate overdrive is

positively biased ($V_G - V_{T,\text{sat}} > 0$), the channel is inverted and current is conducted by the transport of electrons from the source to the channel.

Figure 5.8. I_D - V_D characteristics of the DSS and Schottky barrier PFETs. Note that the y-axis scale for Schottky barrier PFET is 10 times smaller than that of the DSS PFET.

As shown in Figure 5.8, compared with the Schottky barrier PFET, the DSS PFET achieves a higher drive current of $319\mu\text{A}/\mu\text{m}$ while the Schottky barrier PFET having an exponentially increase in the drain current I_D with V_D , shows a much lower drive current of $11.2\mu\text{A}/\mu\text{m}$ at a gate overdrive of -0.6V and $V_D = -1.0\text{V}$. The drive current has been normalized to the Si nanowire diameter for fair comparison. The results show that the DSS PFET drive current is more than one order of magnitude higher while its off state leakage is about 5 orders of magnitude lower than that of the Schottky barrier PFET at $V_D = 1.0\text{V}$ (approximately $10^{-4}\mu\text{A}/\mu\text{m}$ for the DSS PFET vs. $10\mu\text{A}/\mu\text{m}$ for the Schottky barrier PFET). The remarkable enhancement of DSS PFET over the Schottky barrier PFET is due to the existence of a thin layer of segregated boron at the NiSi/Si point contact of the Si nanowire at the S/D-to-channel interface. It is widely believed that the fully depleted boron results in the distortion of the Schottky barrier depletion region, thus giving rise to an enhanced hole carrier injection at the source side and a suppressed

electron injection from the drain side as compared to the Schottky barrier junction without dopant segregation. It is worth noting that the effect of poly-Si stringer on the Schottky barrier thinning in the silicon nanowire has been removed in our GAA devices. Hence, the modulation of the Schottky barrier depletion region is the result of the GAA electrostatic field modulation on the SBH at the NiSi/Si point contact.

Figure 5.9 shows the short channel performance of the DSS PFETs plotted as a function of the physical gate length. Setting this as a benchmark, the subthreshold slopes of the Schottky barrier PFETs are compared against the DSS PFETs in Figure 5.9 (a). It is clear that the trend for both the Schottky barrier and DSS PFETs assumes an exponentially decaying pattern. However, the subthreshold slope of the Schottky barrier PFETs increases more rapidly than that of its DSS counterpart, reaching 280mV/decade at a gate length of 110 nm. Whilst for the DSS PFETs, the subthreshold slope stays more or less the same at about 80mV/decade at longer gate lengths and eventually begins to increase at less than 100 nm. Even for shorter gate lengths e.g. 30 nm, the subthreshold slope ultimately did not exceed 200mV/decade. Due to the nature of the I_D - V_G curve of the Schottky barrier transistor that is exponentially rising, the criteria to determine the threshold voltage is not straight forward. Furthermore, the threshold voltage is sensitive to the SBH at the S/D which results in large variation between devices [44, 164]. Thus the threshold voltage change and DIBL of the Schottky barrier PFETs are not extracted. Figure 5.9 (b) and (c) show the DIBL and saturation threshold voltage change of the DSS PFETs against the gate length. A long channel DSS PFET with 400 nm gate was arbitrarily chosen as the reference point.

Figure 5.9. (a) Subthreshold slope, (b) DIBL and (c) Saturation threshold voltage change, $\Delta V_{T,sat}$ plotted as a function of the physical gate length, L_G , of the DSS PFETs.

It is easy to notice similarities in the trends between all three plots that below gate length of 100 nm. The short channel performance begins to deteriorate. Though not shown, the DIBL of the Schottky barrier PFETs is much higher than the DSS PFETs, in the range of about 500-1000 mV/V, as can be approximately gauged from the I_D - V_G shown in Figure 5.7.

The series resistance of the Si nanowire PFETs is also characterized for both DSS and Schottky barrier devices as shown in Figure 5.10 (a). The series resistance of a Si nanowire MOSFET is of particular interest which is expected to be higher than planar device due to the small dimensions of the NiSi/Si point contact and the extension of the Si nanowire from the channel to the S/D. The total series resistance, R_{Total} (indicated in data points) is plotted against the applied gate voltage, V_G at $V_D = 50$ mV. The series resistance, R_{SD} is normalized to the Si nanowire diameter and is extracted by extrapolating an exponentially decaying curve to $V_G = 10$ V [165]. The R_{SD} difference for both devices is significant, with $R_{SD} = 6467 \text{ } \Omega\text{-}\mu\text{m}$ for the Schottky barrier PFET as compared to approximately 40 times lower $R_{SD} = 153 \text{ } \Omega\text{-}\mu\text{m}$ for the DSS PFET. For a Schottky barrier device, the series resistance consists of 2 major components, which are the S/D silicide

sheet resistance and the contact resistance due to the SBH. As both devices are silicided with the same condition, the silicide sheet resistances are assumed to be similar. Hence the main contributor to the R_{SD} reduction is attributed to the much lower S/D contact resistance of the DSS PFET as a result of the high doping level at the NiSi/Si interface.

Figure 5.10. (a) R_{TOTAL} of the DSS and Schottky barrier PFETs with $L_G = 50\text{ nm}$ measured at $V_D = -50\text{mV}$ for various applied V_G . The indicated series resistance, R_{SD} is normalized to the Si nanowire diameter. (b) Total resistance, R_{TOTAL} as a function of L_G of the DSS PFETs. The solid triangle indicates the DSS PFET used in (a).

To examine the average R_{SD} of the DSS PFETs, the R_{Total} of each DSS PFET is plotted against respective gate length. The R_{Total} in Figure 5.10 (b) is defined as the total resistance by dividing $V_D = -50\text{ mV}$ by the I_D at a gate overdrive of $V_G - V_{T,lin} = -1.5\text{V}$. By

curve fitting the data points of the DSS device population, the y-intercept yields a mean $R_{SD} = 260 \, \Omega\text{-}\mu\text{m}$ which is a better representative than individual device.

5.3.2 Impact of silicidation temperature

The investigation of the electrical analyses on the DSS diodes in Section 5.2 shows that for both P- and N-type DSS diodes, increasing the silicidation temperature from 450°C to 650°C can improve the linearity of the $I\text{-}V$ characteristic. Therefore, it is of interest to investigate the impact of the silicidation temperature on the Si nanowire DSS MOSFETs.

Figure 5.11. (a) $I_D\text{-}V_G$ and (b) $I_D\text{-}V_D$ characteristics of DSS PFETs silicided at various annealing temperatures, which are 450°C, 550°C and 650°C denoted as DSS 450, DSS 550 and DSS 650, respectively.

Figure 5.11 show the transfer characteristics of DSS PFETs processed at various silicidation temperatures. Figure 5.11 (a) shows the $I_D\text{-}V_G$ of three DSS PFETs with three silicidation temperatures, namely 450°C, 550°C and 650°C, henceforth briefly represented as DSS 450, DSS 550 and DSS 650 PFETs. It is clear that the DSS 450 and DSS 550 PFETs have almost identical $I_D\text{-}V_G$ characteristic while the DSS 650 PFET shows a

deteriorated performance with significant degradation in the short channel properties. While the drive current of the DSS 650 PFET is almost identical to the other PFETs, its off state leakage, subthreshold slope and DIBL are greatly degraded by the higher silicidation temperature. The reason to this is due to the well-known transient enhanced diffusion (TED) [166] of boron at the processing temperature which results in the broader and less abrupt doping profile of boron at the S/D junction. This normally translates into severe short channel effects manifest as an increase in DIBL and subthreshold slope. Hence, it is appropriate to put more emphasis on the comparison on the DSS 450 and DSS 550 PFETs.

Close examination of the I_D - V_D characteristics of the DSS 450 and DSS 550 PFETs reveals that the I - V curves are indeed identical as shown in Figure 5.11 (b). As discussed previously in Section 5.2.1, the diode I - V curves of the boron segregation has more dependence on the implant dose than the silicidation temperature. The dependency is expected to be observed as well in the transistor device. Though a slight improvement in the device electrical performance is expected with the DSS 550 PFETs given its higher processing temperature, the results shown in Figure 5.11 prove otherwise.

The effect of the annealing temperature on the boron chemical profiles is well reported in the literature – with higher temperature, more boron atoms segregate and pile-up at the NiSi/Si interface. By using first principles calculation, Yamauchi *et al.* also reported that segregated boron atom are energetically favoured at substitutional site in the Si crystal near the NiSi/Si interface which they concluded that in principle, all segregated boron atoms are electrically active [60]. This leads to the belief that boron segregation in the NiSi/Si point contact of Si nanowire is not entirely identical to the boron segregation on planar junction. One possibility of such deviation from the planar junction is attributed to dopant surface segregation observed in nanowires. Dopant surface segregation is a

phenomenon where P- or N-type dopants experience a tendency to reside at the nanowire surface due to the preferable lower energy states there. Björk *et al.* showed that nanowires with diameter of less than 20 nm dramatically experience an increase in the resistivity [163]. Other work shows that surface segregation is generally valid for both boron and phosphorus [161, 167, 168]. Hence, surface segregation of boron atoms is expected in the PFETs as the nanowire diameter is only 10 nm. On the one hand, raising the silicidation temperature increases the boron segregation at the interface. On the other hand, higher temperature promotes out segregation of available boron in the Si nanowire to the surface which nullifies the boron at the surface. Hence, the competition between the two mechanisms is believed to neutralize the advantage of having a higher silicidation temperature for further device improvement in the case of boron segregation in NiSi/Si point contact.

The results are different in the case of NFETs. Figure 5.12 depicts the transfer characteristics of DSS NFETs processed at various silicidation temperatures. Figure 5.12 (a) shows the I_D - V_G of three DSS PFETs with three silicidation temperatures, namely 450°C, 550°C and 650°C, henceforth briefly represented as DSS 450, DSS 550 and DSS 650 NFETs. The DSS 450 NFET clearly is the inferior one compared to the DSS 550 and DSS 650 NFETs. The DSS 450 NFET has a threshold voltage shift of 0.26V, a large DIBL of 170mV/V as well as significantly lower drive current and higher off state leakage compared to the DSS 550 and DSS 650 NFETs. Figure 5.12 (b) compares the I_D - V_D characteristics of the DSS 450 and DSS 550 NFETs where the drive current of the DSS 500 NFET is about two times larger than that of the DSS 450 NFETs. This is consistent with the diode I - V results in Section 5.2.1 where the phosphorus segregated diode I - V linearity displays greater dependency on the silicidation temperature as compared to the boron segregation. The diode silicided at 450°C has a worse linearity

signifying the electrically active phosphorus concentration at the NiSi/Si interface is insufficient to result in a lowering of SBH close enough to the conduction band edge. The existence of the SBH results in the need for a larger gate voltage to modulate the SBH to a smaller ‘effective’ SBH and causes the large threshold voltage shift in the DSS 450 NFET.

Figure 5.12. (a) I_D - V_G and (b) I_D - V_D characteristics of DSS NFETs silicided at various annealing temperatures, which are 450°C, 550°C and 650°C denoted as DSS 450, DSS 550 and DSS 650, respectively.

By increasing the process temperature to 550°C, the DSS 550 NFET begins to show conventional like electrical behaviour. At higher temperature, the DSS 650 NFET generally only shows an improvement in the off state leakage at high V_D while keeping the drive current and short channel performance unaltered. Surface segregation of phosphorus is expected to have less impact in the NFETs as the nanowire width is approximately 20 nm, which is not considered small enough for the phenomenon to be as critical as compared to the PFETs with smaller diameters. Also, recall the SIMS analysis from Figure 5.5 that the phosphorus chemical concentration does not increase with increased silicidation temperature from 450 to 550°C. Hence, the electrical improvement

for the DSS 450 NFET over the DSS 550 NFETs is attributed to the enhanced activation of phosphorus atoms at the NiSi/Si interface. Similarly, by further increasing the annealing temperature from 550 to 650°C, it is believed that the surface segregation could undermine, if not neutralize the increased activation of phosphorus atoms.

To successfully fabricate CMOS using the dopant segregation technique, it is crucial to achieve the process window that results in optimal performance for both N- and PFETs. Therefore, dopant segregation achieved by silicidation at 550°C is most desired for the fabrication of Si nanowire DSS CMOS.

5.3.3 Fermi level pinning in N-type DSS transistor

Figure 5.13 shows typical I_D - V_G characteristics of DSS P- and NFETs silicided at 450°C and 550°C, respectively. The drain voltages used were 50mV and 1.0V for linear and saturation current characteristics. By assuming a constant channel resistance at large V_G where the Si nanowire channel is fully inverted, the nanowire channel would behave as a resistor in this regime. Provided the external resistance is constant, then the increase in V_D should result in a proportional increase in the I_D by Ohm's Law. The saturation to linear I_D ratio of the PFET is 17 which is reasonably close to the saturation to linear V_D ratio of $1.0\text{V}/50\text{mV} = 20$. However, this ratio is 67 for the NFET which is a significant deviation from the supposed value. Thus, the origin of the large current ratio is attributed to the reduction of the external resistance at $V_D = 1.0\text{V}$. It is well known that an increase in the electric field across the MS junction results in additional Schottky barrier lowering due to image force. In the case of Schottky or DSS transistor, the electric field across the MS junction at the S/D is influenced by the electric field introduced by the V_D . In other words, by increasing the V_D , the SBH is expected to be lowered in addition to the SBH lowering by the dopant segregation. The V_D induced SBH lowering manifests as a

decrease in the junction resistance of the MS contact which directly translates into a decrease in the external resistance. Such behaviour is more noticeable for the NFET as compared to the PFET.

Figure 5.13. Typical I_D - V_G characteristics of DSS P- and NFETs silicided at 450°C and 550°C, respectively. Note that the NFET has a higher saturation to linear current ratio than that of the PFET.

In principles, dopant segregation is beneficial to both P- and NFETs. However, the degree to which the SBH is modified is largely governed by the behaviour of boron and phosphorus atoms at the NiSi/Si interface as well as the intrinsic SBH for electrons and holes. The general agreement on dopant segregation is that the magnitude change in the SBH is observably related to the concentration of segregated dopants at the interface. In a more precise context, the change in the SBH is related to the electrically active dopant concentration at the interface because one cannot simply assume all dopants at the interface are active. As mentioned previously, first principles calculation on boron segregation suggests that all boron atoms situated at the interface are thermodynamically most stable at substitutional sites provided the concentration does not exceed the solid

solubility limit. However, this is not the case for phosphorus where the SIMS analyses and electrical characteristics of the phosphorus segregated diodes shown in Section 5.2 reveal that even with the same chemical concentration, the electrically active phosphorus concentrations are different with elevated silicidation temperature.

Figure 5.14 shows the R_{TOTAL} of the DSS NFETs plotted as a function of physical gate length. The measurement criterion for gate overdrive is kept constant at 1.5V which is the same as that of the PFETs. As the extraction is done within the linear region ($V_D=50\text{mV}$), it is an indirect measurement of the NFETs SBH with minimal influence from the Schottky barrier lowering induced by the V_D . The NFETs data points are remarkably different from that of the PFETs. While not only there is an absence of a clear trend, the R_{TOTAL} of the NFETs are also scattered over one order of magnitude even within the same gate length. This suggests that the NFETs SBH is relatively larger than that of the PFETs. Since the current across the MS junction is exponentially related to the SBH, a small variation in the SBH can result in a large variation in the current, which is inversely proportional to the junction resistance.

Figure 5.14. Total resistance, R_{TOTAL} plotted as a function of L_G of the DSS NFETs optimally silicided at 550°C.

The significant difference between the R_{TOTAL} plots for the DSS N- and PFET is explained by the intrinsic difference of the SBH for electrons and holes. Due to Fermi level pinning, the NiSi n-SBH is always pinned at about 0.6 - 0.7 eV below the conduction band edge while the p-SBH is 0.4 - 0.5 eV above the valence band edge [30]. By assuming that both the boron and phosphorus segregation achieve the same magnitude of change in eV, the resulted n-SBH would still be larger than the p-SBH.

5.3.4 Fermi level de-pinning

As discussed in Chapter 2, according to Tung [35], Fermi level pinning of a Schottky barrier height in a MS junction is caused by the difference in electronegativity which dictates the distribution of electrons in chemical bonds formed between the metal and semiconductor atoms. The electron distribution in the bonds results in dipole moments within the bonds. Hence, it is reasonable to deduce that by replacing the silicon atom at the interface with a foreign atom, the new electronegativity difference between the metal and foreign atoms should result in a different dipole moment [169]. The SBH can be modified based on the magnitude and the direction of the new dipole moment. Apart from that, foreign atoms with additional (e.g. Group V) or the lack of (e.g. Group III) a valence electron induce image charges on the metal side. Thus, when Si atoms are substituted by Group III atoms, the Si crystal becomes positively charge due to the lack of electrons. This induces negative charges on the metal side which leads to an electrostatic field between the induced charge pair that tends to reduce the p-SBH. The same is true for Group V atoms where positive charges are induced in the metal which tends to reduce the n-SBH.

The phenomenon of the deviation in the commonly observed SBH of a MS junction is generally known as Fermi level de-pinning. Based on the theory, the proper

choices of element that would result in large Fermi level de-pinning are those with the dipole moment and image charge that are changing the SBH in the same direction.

By using boron for PFETs and phosphorus for NFETs, Fermi level de-pinning is expected to take place as dopant segregation is a low temperature process that ensures only the dopants very near to the NiSi/Si interface are activated. It is of interest to examine the SBH at the S/D of these nanowire transistors. However, due to the effect of the gate electrostatic field, there would be an additional influence from the gate terminal. Thus, an ‘effective SBH’ is described as a function of the gate bias will be extracted and presented in the next section.

5.3.5 Effective Schottky barrier height

In Section 4.4.2 the electrical characteristics of planar thin body and Si nanowire transistors have been studied and compared. The total current injected from the drain can be approximated by the summation of thermionic, I_{TE} and tunneling current, I_{TN} . To evaluate the SBH, one would be required to find out the I_{TE} or I_{TN} and solve for the SBH. Practically, it is much easier to measure the total current and solve for an ‘effective’ SBH using the thermionic equation (see Equation 4.1). Hence there is no need to separate out the I_{TE} from I_{TN} as the effective SBH using the total current across the MS junction accounts also for the I_{TN} component.

The measurement of the effective SBH from a Schottky transistor was proposed by Calvet *et al.* [47]. The thermionic equation is modified to adapt to the 2D nature of the planar transistor and is shown as follow:

$$I = wA^{**}T^{3/2} \exp\left(\frac{-q\phi_{eff}}{kT}\right) \left[\exp\left(\frac{qV_D}{kT}\right) - 1 \right] \quad (\text{Equation 5.1})$$

where w is the physical channel width, A^{**} is the 2D effective Richardson constant, k is the Boltzmann constant, T is temperature, Φ_{eff} is the effective SBH and V_D is the drain bias. However, in Calvet's context the effective SBH is a measure of the true SBH under the influence of the gate voltage, which is why he suggested that the equation is strictly valid only if the tunneling component is negligible.

The method was modified to lump in the tunneling component by Zhang *et al.* [170] to evaluate the effective SBH of a DSS transistor fabricated on SOI and Peng *et al.* [159] to compare the effective SBH of Schottky barrier transistors of different architectures i.e., nanowire vs. SOI. In this study, we have applied the modified method by Zhang and Peng to evaluate the effective SBH of DSS Si nanowire transistors. Equation 5.1 is modified by Peng to adapt to the 1D nature of nanowire, which is also used in this study. The modified equation is expressed as:

$$I = wA^{**}T^2 \exp\left(\frac{-q\phi_{eff}}{kT}\right) \left[\exp\left(\frac{qV_D}{kT}\right) - 1 \right] \quad (\text{Equation 5.2})$$

where w is a suitable geometric factor e.g. the nanowire diameter. Note the change in the temperature exponent from 3/2 to 2 from Equation 5.1 to 5.2.

The main concept employed by the proposed method is to measure the device I_D - V_G at a relatively low V_D at several temperatures where the I_D is simply the total current across the MS junction. The reason for the measurement to be done with a low V_D is to minimize the impact of the drain electrostatic field which would result in an additional SBH lowering due to image charges. For every point of V_G , a corresponding effective SBH is extracted as the activation energy from the Arrhenius plot using Equation 5.2.

A typical Arrhenius plot is shown in Figure 5.15 (a) where the measurement was done between 180K down to 77K. Typically, low temperatures are favored due to small effective SBH in the multiple of kT . The corresponding I_D - V_G is shown in Figure 5.15 (b).

Only the region which is shaded is used for the extraction of the activation energy due to a good linearity. The extremely low temperatures of 90K and 77K exhibit significant deviation from the linear region, which could be due to the reduction of silicon channel resistivity at cryogenic temperatures.

Figure 5.15. (a) Activation energy/effective SBH for each V_G is extracted from the linear region of the Arrhenius plot which is extracted from the corresponding (b) low temperature I_D - V_G of a typical DSS PFET from 77K-180K.

The extracted effective SBHs for the DSS P- and NFETs are plotted as a function of the gate overdrive as shown in Figure 5.16. Generally, the DSS 450 PFET effective SBH rapidly decreases at the beginning of a raising V_G . Upon reaching the linear threshold voltage, $V_{T,lin}$ the modulation of the effective SBH becomes more gradual and eventually converges to a small value of 0.03 eV. In the case of DSS 550 NFET, the trend is similar to the DSS 450 PFET. The convergence value of the effective SBH for the NFET has a relatively larger value of 0.16 eV. This observation is consistent with the expectation that the intrinsic SBH for electrons is always 0.1 - 0.2 eV larger than the SBH for holes. The effective SBH for a DSS 450 NFET is also shown in comparison to the DSS 550 NFET. As expected, the effective SBH converges to a higher value of 0.22 eV and the modulation by V_G is less rapid. The larger effective SBH value of the DSS 550

NFET as compared to the DSS 450 PFET is also consistent with the R_{TOTAL} values shown in the respective R_{TOTAL} against L_G plot where the PFETs show a lower R_{SD} extracted using the plot. In fact, the extraction of R_{SD} for the NFETs is impractical as the variation is too large. Though there is only one DSS 550 NFET effective SBH curve shown in Figure 5.16 (b) but the variation in the R_{TOTAL} seen in Figure 5.14 suggests that the R_{TOTAL} could be a result of variation in the effective SBH in the NFETs.

Figure 5.16. Effective SBH plotted as a function of gate overdrive, $V_G - V_{T,lin}$ for (a) a DSS PFET silicided at 450°C and (b) DSS NFETs silicided at 450°C and 550°C.

The modulation of the effective SBH by V_G is a measure of the gate electrostatic control on the channel potential. The modulation of the effective SBH under V_G can be easily understood from the band diagram in Figure 5.17. As shown in Figure 5.17 (a), when the gate is biased to zero potential, the built-in potential, V_{bi} of the channel behaves as a barrier in addition to the intrinsic Schottky barrier, thus making the effective SBH larger than the intrinsic SBH. Figure 5.17 (b) illustrates the band diagram when the V_G is increased. The channel potential is lowered and does not create any extra barrier to carriers. Further increase in the negative V_G distorts the space charge region and acts to reduce the Schottky barrier space charge thickness, thus making the effective SBH lower

than the intrinsic SBH. Hence, the effective SBH can also be viewed as a measure of the degree of Schottky barrier transparency to tunneling.

Figure 5.17. Schematics of band diagrams describing the electron transport when the gate is (a) turned OFF, and (b) turned ON. ϕ_{eff} in the diagram represents the effective SBH.

How rapid an effective SBH is modulated by the gate at the early stage of raising the V_G can also provide some insight into the SBH at the S/D. Assuming the gate-to-channel electrostatic control is the same for every DSS transistor, the modulation curve should ideally have a steep slope limited only by the drift-diffusion carrier transport mechanisms if the Schottky barrier does not exist. However, with the existence of the Schottky barrier the slope begins to deviate from the ideal slope. It is reasonable to believe that a larger deviation from the ideal slope originates from a larger SBH. The effective SBH can be modulated lower or higher depending upon the gate-to-channel potential. However, there is an asymptotic value of which the effective SBH can no longer be further lowered. The asymptotic effective SBH at very large V_G shows that the channel potential is inverted and no longer creates any barrier for injected carriers from

the drain. The effective SBH at this point is believed to be a good measurement of the Schottky barrier at the drain side.

As discussed in Section 5.3.4, the introduction of boron or phosphorus at the NiSi/Si interface causes Fermi level de-pinning which can result in a lower SBH value by itself. Bearing in mind that the calculation of the effective SBH lumps in the thermionic and tunneling components, the effective SBH of the DSS barrier modified by Fermi level de-pinning is expected to yield a smaller value. The larger effective SBH of the DSS NFET of 0.16 eV shows that it is still not sufficiently low to obtain good electrical characteristics, at least in the linear region, as compared to the DSS PFET. This can be attributed to the inadequate activation of phosphorus atoms at the NiSi/Si interface as well as the intrinsically higher electron SBH than the hole SBH due to Fermi level pinning. Since the SBH is a material property, it is crucial that the activation of phosphorus atoms at the interface can be improved so as to generate lower effective SBH which is much desired.

5.4 Numerical simulation with a sub-circuit approach

In this section, 2-D numerical simulations of DSS nanowire MOSFET were done using Medici. A numerical GAA n-channel MOSFET with the nominal parameters shown in Figure 5.18 was used for the simulation. The S/D is assumed to be perfectly aligned with the gate i.e., without any overlap/underlap.

Previous studies show that the carrier transport mechanisms change when the Schottky S/D is replaced by the DSS S/D [12]. The leakage is changed from Schottky barrier tunneling (SBT) to gate-induced drain leakage (GIDL) current due to band-to-band tunneling (BTBT). The ON state transport, on the other hand, changes from the ambipolar thermionic-tunneling (TT) current to the unipolar drift-diffusion (DD) current.

Carrier transport could be DD or TT dominant, or a combination of both, depending on the parameters related to dopant segregation.

Figure 5.18. Schematic of an ideal DSS GAA Si nanowire MOSFET: (a) Cross-section along S/D and (b) along radius. The n-channel DSS subcircuit model is shown in the lower right side. The nominal device parameters are $L_G = 100$ nm, $R = 10$ nm, $T_{ox} = 2$ nm, segregated dopant concentration, $N_{seg} = 10^{20}$ cm⁻³, and length of segregated dopant, $L_{seg} = 10$ nm, which are the default physical parameters values, unless otherwise stated. The work function Φ_M at S/D is 4.7 eV, corresponding to a SBH Φ_B of 0.53 eV for electrons.

5.4.1 Model formulation

The DSS MOSFET can be conceptually separated into three components, namely, a gated Schottky diode (GSD) at the source side where the anode potential V_s' is dependent on the gate voltage V_G , an intrinsic Si channel and a resistor at the drain side as shown in Figure 5.18. The GSD is reverse biased because the electrons are injecting from the silicide to the (n-type) semiconductor in normal operations. Internal nodes (V_s' and V_d') are introduced where the voltages at these nodes can be solved by a circuit simulator in the subcircuit model.

A. DD Model

The DD current in conventional MOSFETs is given by [171, 172]

$$\begin{aligned}
 I_{DS} &= I_{Drift} + I_{Diff} \\
 &= -\mu_s W Q_i(y) \frac{d\phi_s}{dy} + \mu_s W v_{th} \frac{dQ_i(y)}{dy}. \quad (\text{Equation 5.3})
 \end{aligned}$$

In the case of nanowire MOSFETs, the DD formulation is modified to accommodate for the surface potential that is wrapping around the nanowire channel. The DD current is given by [173-175]

$$\begin{aligned}
 I_{DS} &= 2\mu C_{ox} \frac{\pi R}{L} (V_{GF} - \phi_s + 2v_{th}) \Delta\phi_s \\
 &\approx 2\mu C_{ox} \frac{\pi R}{L} (V_{GF} - \phi_s + 2v_{th}) V_{DS,eff} \quad (\text{Equation 5.4})
 \end{aligned}$$

where μ is the carrier mobility, $V_{GF} \equiv V_G - V_{FB}$ is the flatband-shifted gate voltage, $C_{ox} = \epsilon_{ox}/[R\ln(1 + T_{ox}/R)]$ is the cylindrical gate capacitance, and $v_{th} = k_B T/q$ is the thermal voltage. $V_{DS,eff}$ is the effective terminal drain-source voltage including velocity saturation/overshoot effects. ϕ_s in Equation 5.4 is the V_G -dependent surface potential without the lateral-field effect.

$$\phi_s = V_{GF} - 2v_{th} L \left\{ \frac{Y_i}{2\sqrt{v_{th}}} e^{(V_{GF} - V_c(y))/2v_{th}} \right\} \quad (\text{Equation 5.5})$$

where $Y_i = (2q\epsilon_{Si}n_i)^{1/2}/C_{ox}$ is the intrinsic body factor. $V_c(y)$ is the channel voltage, which equals the difference between the internal V'_s at the source end and V'_d at the drain end. $L\{w\}c$ is the Lambert W function.

All major second-order effects, such as S/D series resistance, channel-length modulation, DIBL, velocity saturation/overshoot, and vertical/lateral-field mobility degradation, have been built into the core model as given in [173] and [174]. The detailed

model validation with experimental data can be found in [175], which shows that the unified model to match the drain current as well as its higher order derivatives.

B. Schottky diode model

The Schottky diode at the source side is at the heart of the simulation. Thus, it deserves an important treatment and must be physically modeled. The diode current consists of both thermionic and tunneling currents in series. The thermionic current is given as [176]

$$I_{th} = AA_n^* T^2 \exp\left(-\frac{\phi_{eff}}{V_{th}}\right) \left[\exp\left(\frac{V_A - R_S I_{th}}{n V_{th}}\right) - 1 \right] \quad (\text{Equation 5.6})$$

where $V_A = V_s' - V_s$ is the voltage drop across the GSD. A is the area of the Schottky barrier/channel interface. A_n^* is the electron Richardson constant. ϕ_{eff} is the effective SBH at the source junction and is a fitting parameter in the simulation. n is the ideality factor, which is an adjustable model parameter. V_s' is the internal node voltage between the source Schottky junction and intrinsic Si channel. The tunneling current is given as [177]

$$I_m = A \frac{q^2 F_s^2}{8\pi h \Phi_{B,s}} \exp\left(-\frac{8\pi}{3hq|F_s|} \sqrt{2m_n^* (q\phi_{eff})^3}\right) \quad (\text{Equation 5.7})$$

where h is the Planck constant. m_n^* is the electron effective mass. F_s is the electric field at the source-end metal/semiconductor interface, which is expressed as

$$F_s = \frac{V_s' - V_s}{\lambda_{dep,s}} \quad (\text{Equation 5.8})$$

in which $\lambda_{dep,s}$ is the depletion width induced by the source end Schottky barrier. The relationship between the $\lambda_{dep,s}$ and the segregation dopant concentration at the source-end, $N_{seg,s}$ is given by

$$\lambda_{dep,s} = \sqrt{2\epsilon_{Si}\phi_{eff} / qN_{seg,s}}. \quad (\text{Equation 5.9})$$

The current continuity requires that the total GSD TT current across the junctions to be equal to the transistor DD current in the channel, assuming no leakages from the gate terminal. The GSD TT and the channel DD models are separately implemented in Hspice using Verilog-A, which is simulated to obtain the internal node voltage V'_s .

C. GIDL

A high electric field is induced by the gate in the gate-to-drain overlap region when $N_{seg,d}$ is high or $L_{seg,d}$ is long in the segregation region. The high electric field leads to GIDL, which is due to BTBT or trap-assisted tunneling. Usually, the BTBT is assumed to be the dominant factor. The BTBT current can be approximated by [178]

$$I_{GIDL} \propto 2\pi RL_{seg,d} E_{seg,d}^2 \exp\left(-\frac{B_{GIDL}}{E_{seg,d}}\right) \quad (\text{Equation 5.10})$$

where B_{GIDL} is a physics-based parameter with a theoretical value of 21.3 MV/cm. $E_{seg,d}$ is the electric field in the gate-to-drain overlap region, given as

$$E_{seg,d} = \frac{C_{ox}}{\epsilon_{Si}} \sqrt{V_{seg,d}^2 + (C_{GIDL} V_{DS})^2} \quad (\text{Equation 5.11})$$

in which C_{GIDL} is a fitting parameter and $V_{seg,d}$ is the gate-drain voltage across the oxide.

Figure 5.19. Illustration of the GIDL mechanism and the band diagram of a Schottky barrier nanowire transistor.

GIDL occurs when the transistor is biased such that the V_G is low, typically grounded and the V_D is high, typically at V_{DD} . Figure 5.19 illustrates the band diagram of the Schottky barrier transistor (shown here a NMOS with p-type channel) along the channel direction under the biasing conditions as mentioned. The silicon band bending at the drain side is large that it causes BTBT to take place. Hence, the larger the band bending at the drain side, the higher I_{GIDL} can be expected. This is possible by biasing the V_G further to the negative side (positive for PMOS) and/or increasing the magnitude of the V_D . The BTBT occurs between the drain and the channel/substrate. For bulk transistor, the current path of I_{GIDL} is from the drain to the substrate where it is typically grounded. However, for floating body devices such as the nanowire transistor, there is no way the I_{GIDL} can complete the current path. Thus, there is a net positive potential building up in the channel as BTBT occurs between the channel and the drain. Eventually, the potential is high enough to forward bias the channel/source junction such that the current path can be completed from the drain to the channel and finally to the source where it is grounded.

5.4.2 Simulation results

Figure 5.20 shows the simulation results of both Schottky and DSS nanowire PFETs using the subcircuit approach which are in good agreement with the measurement results.

Figure 5.20. Measured I_D - V_G of both Schottky (triangles) and DSS (circles) nanowire PFETs at $V_{DS} = -0.05$ V and -1.0 V. The inset shows the p-channel DSS subcircuit model conceptualized as a Schottky diode in series with the channel and a resistor at the drain end.

Figure 5.21 shows the energy-band diagram at the Si nanowire surface along the intrinsic nanowire channel of the DSS MOSFET. For both the source and drain, the L_{seg} is 10 nm and the N_{seg} is $1 \times 10^{20} \text{ cm}^{-3}$. Transport mechanisms for the MOSFET can be identified by studying the potential profiles across the channel. Due to the Schottky barrier at the source side, electron injection is governed by the TT model. The electrons obey the DD model in the channel after being injected from the source. Due to the dopant segregation induced band distortion at the drain side, hole injection is basically blocked and the leakage is mainly due to BTBT in the gain-drain overlap region. The BTBT is modelled as the GIDL current.

Figure 5.21. Extracted energy-band diagram from Medici simulations for a DSS MOSFET at various VG from -0.4 to 2.0 V with a step of 0.2 V and VD = 1.2 V.

To better understand the leakage mechanism of DSS MOSFETs, the drain side segregation parameters, $N_{seg,d}$ and $L_{seg,d}$ are varied separately to investigate their impact on the leakage current. The source side segregation parameters are fixed at relatively large values ($L_{seg,s} = 10$ nm and $N_{seg,s} = 1 \times 10^{20} \text{ cm}^{-3}$) to ensure partial depletion such that it does not become an additional factor that contributes to the change in leakage current.

Figure 5.22 shows the effect of $N_{seg,d}$ on the leakage current. For $N_{seg,d}$ greater than $5 \times 10^{19} \text{ cm}^{-3}$, the segregation layer is partially depleted which results in the hole injection being blocked. The leakage current at the drain side is essentially due to BTBT. However, it is undesirable to have a very high $N_{seg,d}$ as it induces large electric field which leads to larger GIDL current. $N_{seg,d}$ smaller than $5 \times 10^{19} \text{ cm}^{-3}$ would result in fully depleted segregation layer that has an energy-band profile independent of the doping concentration which is ineffective in suppressing hole injection. Thus an appropriate value for $N_{seg,d}$ is required in order to optimize the leakage performance of the device.

Figure 5.22. (a) Leakage current characteristics with various dopant concentrations in the drain side segregation region and (b) the corresponding energy-band diagrams of the simulated DSS MOSFETs.

Figure 5.23 shows the effects of $L_{seg,d}$ on the leakage current. The $N_{seg,d}$ is now kept constant at 1×10^{20} cm^{-3} . The segregation layer is partially depleted for $L_{seg,d}$ longer than 4 nm. The leakage mechanism with $L_{seg,d}$ longer than 4 nm is dominated by BTBT. A longer $L_{seg,d}$ is undesirable as it gives a longer overlap region between the gate and drain which leads to a higher GIDL current. Similar to the previous analysis with various $N_{seg,d}$, there exists an appropriate $L_{seg,d}$ where the leakage is kept at the minimum level.

Figure 5.23. (a) Leakage current characteristics with various segregation lengths in the drain side segregation region and (b) the corresponding energy-band diagrams of the simulated DSS MOSFETs.

It should be emphasized that the analyses are based on n-SBH of 0.53 eV. The simulations with Medici do not take into the account of Fermi level de-pinning caused by the dopant atoms at the MS interface which would result in a lowering in the intrinsic SBH. With different SBH values, the corresponding optimum $L_{seg,d}$ and $N_{seg,d}$ values should be different since the onset of partial depletion could be changed. However, it is clear that the aforementioned analyses still holds.

Figure 5.24. (Lines) Model comparison with (symbols) measurement data for two DSS devices in (a) and (b), respectively.

The analyses also infer that the drain side behaviour is especially sensitive to $L_{seg,d}$ and $N_{seg,d}$. A small change in these parameters near the onset values of partial depletion may have dramatic impact on the leakage current transport mechanism as well as the effective SBH where the ON state current is an exponential function of the effective SBH.

The subcircuit model is verified with the device measurement results as shown in Figure 5.24. Two DSS MOSFETs from the same wafer were selected. The DSS MOSFET in Figure 5.24 (a) shows the conventional behaviour whereas the one in (b) shows a convex curvature, particularly at low V_{DS} and high V_{GS} . The interesting difference between the two devices is believed to be due to process variations. One possible source

of variations is the SBH, which is extremely sensitive to the interfacial states, traps or dopants at the MS junction. Moreover, due to the exponential relation on the SBH, a small fluctuation in the SBH can result in a huge variation in the device characteristics. In this example, device (b) is believed to be due to either insufficient $L_{seg,d}$ or $N_{seg,d}$, or both.

5.5 Summary

DSS diodes with boron and phosphorus segregation have been fabricated and analyzed. The results show that by increasing the dose and silicidation temperature resulted in better linearity in the diode I - V curves. The effect of temperature is found to be more critical for the phosphorus segregation. Furthermore, the combination of electrical and chemical analyses shows that the DSS diode I - V characteristic is dependent on the electrically active dopants at the interface.

Using top down technology, true GAA Si nanowire DSS MOSFETs without parasitic poly-Si stringer has been successfully demonstrated and characterized. The results show that the DSS MOSFETs are superior to Schottky barrier MOSFETs. The DSS MOSFETs exhibit better electrical performance in term of I_{ON} and I_{ON}/I_{OFF} ratio, good short channel performance with small subthreshold slope, DIBL and threshold voltage change down to $L_G = 100\text{nm}$ as well as a significant reduction in series resistance. The improvement was attributed to the thin layer of segregated dopants piling up at the NiSi/Si interface of the Si nanowire DSS MOSFET which results in Fermi level depinning of the SBH closer to the conduction/valence band edge.

The activation energy extracted from low temperature measurement reveals that the effective SBH of the DSS PFET is lower than that of the DSS NFET by approximately 0.1 eV. The higher effective SBH of the DSS NFET is a result of the higher intrinsic SBH as well as the incomplete activation of phosphorus at the NiSi/Si

interface, compared to the DSS PFET. Simulation on DSS MOSFETs verified the effect of both L_{seg} and N_{seg} on the device electrical performance which shows that there are no simple solutions as to what L_{seg} and N_{seg} should be. Instead, there exists an optimum condition for a unique combination of the material's SBH, as well as the L_{seg} and N_{seg} of the device. However, the simulation did not take into the account of the effect of SBH lowering by Fermi level de-pinning. With smaller SBH value after accounting for the Fermi level de-pinning, it is possible that the L_{seg} and N_{seg} (particularly N_{seg}) values needed would be significantly lower than those with a larger SBH.

Chapter 6 EXCIMER LASER ANNEALED DOPANT SEGREGATED SCHOTTKY (ELA-DSS) DEVICES

6.1 Introduction

In Chapter 5 we found that the electrically active dopant concentration at the NiSi/Si interface is the key factor in contributing to the Fermi level de-pinning which results in a lower SBH. Thus, it is of great importance to study the origin of low temperature activation of dopants. The understanding of the mechanism could lead to useful applications such as improvement in contact resistance which is critical in advanced CMOS technologies.

The understanding of dopant activation at low temperature typically 400 - 600°C at the silicide/silicon interface is not well understood. Using NiSi as an example, Wittmer *et al.* [26] argued that during silicide formation excess Si point defects i.e., self-interstitials and vacancies are generated at the interface. These point defects are hypothesized to produce a lower energy path for dopant diffusion or activation. This suggests the amount of segregation is correlated to the amount of point defects available during silicide formation. Hence this also leads to the supposition that by incorporating more defects in the Si, more sites with lower energy path are available during dopant segregation which should give rise to higher electrically active dopant concentration at the interface.

In this chapter, ELA is proposed to be implemented as a mean to defect engineering in the Si substrate prior to dopant segregation. Photoluminescence is utilized to characterize defects in the Si. Characterization on diodes and Si nanowire transistors was conducted to study and analyse the effect of defect engineering.

6.2 Defect engineering by ELA

Following the work done by Wittmer *et al.*, we make use of the hypothesis and broaden the assumption that not only point defects (self-interstitial and vacancy) but defects in general, contribute to a lower energy path for dopants to be activated. However, defects on the other hand are detrimental to Schottky junction if located within the depletion region. Thus, it is of interest to engineer a shallow region of defects such that they will be consumed by the silicide layer upon silicidation and the depletion region is free from any defects.

ELA has been a subject of interest for many years due to its transient and ultra fast nature which is capable of transferring energy within an extremely short time frame, elevating the temperature of a material to its melting point or higher and quenching down to the ambient within micro or nanoseconds. Mannino *et al.* [179] showed that by using ELA, defects in particular vacancies are generated in the melt region due to the creation of point defect deformation between the liquid/solid interface during recrystallization of molten Si. Recently, Tan *et al.* [180] showed that transient enhanced diffusion (TED) of boron can be alleviated using defect engineering by ELA. In another work [181], it was shown that even laser with non-melt fluence is capable of generating a substantial amount of defects near the surface. Hence, in this chapter, ELA is employed to engineer a shallow layer of defects to provide a more effective activation at the NiSi/Si interface. The application of ELA is incorporated into device fabrication and the electrical results are discussed.

6.2.1 Analytical simulation of laser annealing process

As the process of defect engineering involves heavy usage of ELA, it is crucial to understand how the ELA interacts with the Si substrate. Perhaps the most important

aspect of the ELA-Si interaction is the substrate temperature generated by the heat transferred from the laser photons to the Si lattice. The choice of excimer laser used throughout the study is a KrF laser with a characteristic wavelength of 248 nm which is equivalent to photon energy of about 5 eV. Generally, crystalline Si absorption coefficient, α of incident wavelength of such energy (5 eV) is very high. The commonly reported value of α for Si is in the order of 10^6 cm^{-1} for 248 nm [182, 183]. Such high α value translates into very shallow absorption depth in the order of tens of nanometers. Hence, the interaction of excimer laser with the Si involves heat transfer at a very shallow depth from the Si surface.

Figure 6.1 (a) shows the simulation result of the surface temperature generated as a result of a heat transfer by the laser-Si interaction as a function of elapsed time. The details of the method of the simulation are discussed in Section 3.6. By increasing the laser energy density or fluence, an increase in the Si surface temperature is observed. The surface temperatures peak at about 22 to 23 ns after the laser irradiation has elapsed which is almost the same as the FWHM of the laser pulse width. As the laser fluence is increased to 550 mJ/cm^2 , a plateau is formed at 16 ns and remains until 26 ns. The temperature of this plateau coincides with the melting point of crystalline Si at 1687 K which signifies that melting occurs at this laser fluence. The temperature plateau is explained by the large latent heat of melting of about 1800 kJ/kg as well as the high thermal conductivity of crystalline Si of $22 \text{ Wm}^{-1}\text{K}^{-1}$ at about 1600 K [184]. A great amount of heat is required to melt the crystalline Si. Furthermore, the generated heat from the laser is quickly transferred from the molten Si to the crystalline Si without involving a rise in temperature of the molten Si. For the simulation to be matched with the experimental results, the onset of melting is calibrated to be at 520 mJ/cm^2 which is also the commonly reported melting threshold of Si determined by experiment [185]. Figure

6.1 (b) shows the simulated result plotted as a function of the distance from the Si surface at 23 ns when the surface temperature peaks. As expected from the large α , most of the laser energy is absorbed at a shallow depth from the Si surface and the generated heat is quickly transferred into the substrate by conduction. This can be seen as large temperature gradients which begin at about 40 to 50 nm to 1 μm beneath the surface.

Figure 6.1. The generated Si surface temperature as a result of heat transfer by the laser as a function of (a) the elapsed time and (b) the distance from the surface.

6.2.2 Photoluminescence (PL) analysis

PL spectroscopy has been an indispensable tool in the characterization of optically active defects in semiconductor. Recently, the technique has also been used to study implantation related defects in Si. Much of the PL work dedicated to the study of defects in semiconductor has been done at low temperature but more recent work has shown that room temperature defect characterization is also plausible [181, 186, 187].

Monakhov *et al.* showed that the diffusion and activation of implanted boron in Si could be affected by a pre-annealing ELA [28]. They concluded that ELA induced defects such as excess vacancies played a critical role in altering the diffusion and activation properties of the implanted boron. Also, Bao *et al.* [188] demonstrated a sub-bandgap

light emitting diode (LED) based on the introduction of point defects by ELA which improved the radiative recombination rate. Using PL analysis, they showed that the excess self-interstitials were responsible for the zero-phonon emission line at 1218 nm. With room temperature PL, Timoshenko *et al.* [181] showed that the yield of PL intensity is reciprocal to the defect surface density of the sample after being irradiated with XeCl₂ laser.

Figure 6.2. PL spectra of Si samples with different annealing conditions.

Figure 6.2 shows the PL spectra of three samples characterized using a 532 nm laser at room temperature. The samples are the as-implanted sample, RTA annealed sample and laser annealed sample. The as-implanted sample displays a very low intensity region at 1100-1200 nm range indicating a high defect density near the surface. The defective region caused by the implant damage is repaired after subjected to a RTA at 950°C for 60 seconds which shows up as a high intensity broad peak around the 1100-1200 nm region. However, by subjecting the as-implanted sample to ELA with a fluence of 550 mJ/cm² the PL spectrum is hardly modified. This shows that ELA is capable of retaining, if not creating defects in Si.

Figure 6.3. Normalized PL intensity of a pristine crystalline Si before and after processed with ELA.

To qualitatively compare the PL intensities among the samples, the associated noise level was first subtracted from each spectrum and the maximum peak within the 1100-1150 nm range of each of the samples were then extracted and compared. Figure 6.3 shows the PL intensities of a pristine crystalline Si before and after being irradiated by laser. The normalized intensity of the sample after subjected to ELA is lower, indicating the creation of some defects near the Si surface due to the shallow heating of the ELA.

The same method was applied to the BF_2 and phosphorus implanted Si and the results are shown in Figure 6.4. For the BF_2 samples, it is clear that the samples with ELA show a decrease in the PL intensity as compared to the as-implanted sample, particularly the sample with a fluence of $440\text{mJ}/\text{cm}^2$. Similar trend can be observed with the phosphorus implanted samples suggesting high defect density region near the surface after processed with ELA. However, it is found that by further increasing the laser fluence exceeding $550\text{mJ}/\text{cm}^2$ (approximately the melting threshold for Si), the PL intensity begins to rise again. This could be due to the competing mechanisms coming from the re-crystallized Si lattice from the molten region which repairs much of the implant damage.

Figure 6.4. PL intensities of (a) BF₂ and (b) phosphorus implanted Si samples processed with different annealing conditions.

The difference in the PL intensities between the BF₂ and phosphorus samples could be due to a slight difference in the optical properties e.g. absorption coefficient and reflectivity as a result of different impurities. Nonetheless, the PL analysis confirms the existence of a defective region near the Si surface by irradiation of laser. Similar results have been reported by Timoshenko *et al.* where surface defect density is increased even below a melting threshold [181]. This could be due to the dislodging of Si atoms from the crystal lattice by the intense heating and quenching process related to ELA.

6.4 ELA-DSS diodes

To study the electrical and chemical properties of ELA-DSS contact, diodes were fabricated using the methodology as described in Section 3.4.3. P-type and n-type ELA-DSS diodes were implanted with BF_2 and phosphorus respectively before laser annealing was conducted. I - V measurement and characterization on the chemical profiles of dopants were performed to investigate the relationship between the electrical and chemical characteristics. The results are also compared to the DSS diodes and the differences are discussed in this section.

6.4.1 Electrical characterization

This section presents the I - V characteristics of the ELA-DSS diodes. As shown previously in Chapter 5, the minimum silicidation temperatures to achieve optimal transistor performance are 450°C for DSS PFETs and 550°C for DSS NFETs. It is of interest to fabricate diodes at these temperatures as it is also the actual fabrication condition of transistor devices. Hence, in this section, we have adopted silicidation temperatures of 450°C and 550°C for P-type and N-type diodes, respectively. Figure 6.5 shows the I - V results of the ELA-DSS diodes compared to the DSS diodes. Schottky diodes without any implant are also presented for reference.

As shown previously in Figure 5.1 and 5.2 in Chapter 5, the P- and N-type diode I - V curves are much more symmetrical compared to their Schottky diode references shown in a logarithmic scale. However, it is found that in a linear scale the I - V is not entirely linear as shown in Figure 6.5. The linearity of the P-type DSS diode is relatively better compared to that of the N-type, which is reasonable as the SBH is expected to be lower for the P-type DSS diode due to its lower intrinsic SBH compared to the N-type diode.

Figure 6.5. I - V characteristics of (a) BF_2 implanted and (b) P implanted diodes. The silicidation temperatures were 450°C for P-type and 550°C for N-type diodes, respectively. The laser fluence used was 550 mJ/cm^2 for the ELA-DSS diodes. Schottky diodes on respective substrate are shown as black diamonds.

With the incorporation of ELA prior to silicidation, the ELA-DSS diodes show better linearity in the I - V curves. The improvement mainly comes from the reverse bias region of the diodes where the majority carriers are required to surmount the SBH of the MS junction to be injected into the Si substrate. Hence the increase in the reverse current is attributed to the reduction in the SBH due to the enhanced Fermi level de-pinning by increasing the electrically active dopants at the interface. Due to the inherently higher electron mobility, the N-type substrate resistance is usually 2-3 times lower than that of the P-type since the substrate doping is almost at the same doping level of $1 \times 10^{15} \text{ cm}^{-3}$. However, the diode current of the P-type diode is approximately 5 times higher than the N-type diode. This suggests that the contact resistance of the P-type diode must be substantially lower.

6.4.2 Chemical characterization

Chemical analyses were also performed on blanket samples to investigate the depth profiles of boron and phosphorus under the effect of ELA. Figure 6.6 depicts the

boron profiles obtained using SIMS for the as-implanted reference and other samples annealed by various laser fluencies. Evidently, the boron profile for the samples irradiated with laser fluencies less than or equals 480 mJ/cm^2 overlaps with the as-implanted dopant profile while a minor diffusion of about 5 nm is noted for annealing with a fluence of 550 mJ/cm^2 . This result is consistent with the reported melting threshold of approximately 520 mJ/cm^2 for bulk silicon by a 248 nm excimer laser.

Figure 6.6. (a) Boron concentration of the as-implanted and the laser annealed diodes prior to silicidation. (b) Magnified view of the boron profile shown in (a).

Figure 6.7. Boron concentration of the as-implanted and the laser annealed diodes after silicidation.

The doping profiles after silicidation are presented in Figure 6.7. Clearly, the samples annealed with laser show a higher doping concentration at the NiSi/Si interface compared to the reference sample. Furthermore, with higher laser fluencies, the segregated boron concentration is seen to increase. The sample annealed at 550 mJ/cm^2 has a segregated boron concentration of approximately 3 times higher than that of the reference sample without ELA.

Based on the hypothesis that point defects provide low energy path for dopant activation at the interface, it is reasonable to deduce that the higher segregated dopant concentration is contributed by the introduction of more point defects. This is also shown to be consistent with the PL analyses in Section 6.2.2 where ELA indeed incorporated defects in the Si lattice. The higher segregated boron at the interface is believed to be fully active, as pointed out by Yamauchi *et al.* using first principles calculation [60].

Figure 6.8. Phosphorus concentration of the as-implanted and the laser annealed diodes prior to silicidation.

The response of phosphorus doped N-type samples to ELA is slightly different from the P-type samples. Figure 6.8 shows the phosphorus profiles obtained using SIMS for the as-implanted reference and other samples annealed by various laser fluencies. Unlike the boron samples, the phosphorus samples do not show any clear sign of

diffusion even at 550 mJ/cm^2 . This is clearly consistent with the PL analyses where the phosphorus doped samples have a higher threshold than the boron doped samples presumably due to some differences in the reflectivity and absorption coefficient between the phosphorus and boron doped Si substrates.

Figure 6.9 (a) shows the phosphorus profiles after silicidation. The difference in the segregated phosphorus concentrations at the interface is observed to be less significant than the boron samples. The segregation peaks of the laser annealed samples are also retreated by about 5 to 7 nm. There is also another prominent peak within the NiSi laser observed only with the laser annealed samples. The reason to this could be due to formation of larger silicide grain size. Most of the dopants in the silicide are situated at the silicide grain boundaries. With smaller grain size, the peaks origin from grain boundaries detected by SIMS profiling would superimpose and show up as variation in the concentration. However, with larger grain size, the individual peaks are further apart and would be easily distinguished from one another.

Figure 6.9. (a) Phosphorus concentration of the as-implanted and the laser annealed diodes prior to silicidation. (b) Magnified view of the boron profile shown in (a).

What is more critical from the SIMS profiling is the relationship between the chemical concentration at the interface and the I - V characteristics of the phosphorus doped diodes. As shown in Figure 6.9 (b), the increase in the segregated concentration after ELA is only marginally higher than the reference sample without ELA. This certainly does not justify the remarkable improvement in the I - V linearity. Hence, the observation supports that with almost the same phosphorus concentration at the interface there must be more electrically active phosphorus atoms at the interface in the laser annealed diodes.

The generation of additional defects by ELA does not modify the activation energy of individual dopant. Rather it should be analogous to increasing the probability of dopants being activated as statistically speaking there are more defects in the Si to provide lower energy path.

6.5 ELA-DSS transistors

ELA-DSS transistors were fabricated as described in Section 3.5. ELA was performed prior to silicidation of S/D. ELA-DSS P- and NFET were fabricated on separate SOI wafers but employing the same processing steps except the poly silicon gate and S/D implant that defined the transistor type. The PFETs and NFETs were then silicided at 450°C and 550°C to form NiSi S/D. Figure 6.10 shows the cross-sectional TEM micrographs of the Si nanowire channel of typical P- and NFET. The PFET has a triangular shape with about 8 nm of width while the NFET has a rectangular shape with a dimension of 15 x 25 nm.

Figure 6.10. Cross sectional TEM micrograph of nanowire channel for (a) PFET and (b) NFET. Dotted lines are guide to the eyes.

The characterized results on the diodes in Section 6.4 are obtained from bulk silicon substrates. However, the interaction of excimer laser on bulk and SOI wafers are very different due to the shallow absorption coefficient of the 248 nm excimer laser on silicon coupled with the existence of a buried oxide (BOX) layer in SOI wafers. The heat which is generated rapidly by the laser at the shallow depth of the SOI layer is dissipated into the substrate by conduction. However, due to its low thermal conductivity, the BOX effectively slow down heat dissipation to the substrate and acts as a heat confinement layer which. The implication of the ELA on a heat confinement layer means that equal temperature on SOI can be generated by smaller amount of heat compared to bulk Si. Hence, to correlate the diode data obtained from the bulk wafers for nanowire devices built on SOI wafers, surface temperatures for both bulk and SOI substrate (20 nm Si on 150 nm BOX used for nanowire device fabrication) are simulated for various laser fluencies using COMSOL simulator. The simulated results depicted in Figure 6.11 show that by using fluencies as low as 100 mJ/cm^2 the surface temperature of the SOI can reach as high as the Si melting point. Remarkably, this is only about one fifth of the minimum fluence (520 mJ/cm^2) that is required to melt the Si surface. For the laser to have minimal impact on the gate stack integrity, laser fluencies used in this study was from non-melt regime i.e., less than 100 mJ/cm^2 . The laser fluence used for the PFETs was 70 mJ/cm^2

while it was 80 mJ/cm² for the NFETs. Maintaining the excimer laser fluence below 100 mJ/cm² involves stringent control of the stability of the source power. Due to newly refilled gas source for the NFETs experiment, the lowest stable fluence achievable was 80 mJ/cm² while the PFETs experiment was carried out after the gas source has been partially depleted. The calculated maximum surface temperature on the PFETs and NFETs are approximately 1290 K and 1420 K, respectively. Due to the assumptions and limitations of the simulation mentioned in Section 3.6.2 such as the GAA structure of the nanowire acting as additional factor of heat confinement, the simulated temperatures are always underestimation of the corresponding real temperatures. However, for the simplicity of simulation, we found that the simulated temperatures provide relatively satisfying accuracy which serves the purpose as a guide for device fabrication.

Figure 6.11. Simulation of surface temperature due to heating upon ELA of SOI wafer. The simulated top Si layer is 20 nm and the BOX layer is 150 nm in thickness.

6.5.1 Electrical transfer characteristics

Figure 6.12. (a) I_D - V_G and (b) I_D - V_D characteristics of the DSS 450 and ELA 450 PFETs.

Figure 6.12 shows the I_D - V_G and I_D - V_D characteristics of the fabricated DSS 450 and ELA-DSS Si nanowire PFET silicided at 450°C (henceforth referred to as ELA 450 PFET). From the I_D - V_G curves, the most significant difference between the two devices occurs at the subthreshold region where the ELA 450 outperforms the DSS 450 PFET with a steeper slope, indicating a swifter turn-on response of the transistor. The ELA 450 PFET also shows improvement in the drive current as compared to the DSS 450 PFET as shown in the I_D - V_D curves. The drive current improves by a remarkable 54% with an additional ELA step prior to silicidation.

To better examine the improvement brought about by the ELA, an I_{ON} - I_{OFF} plot is shown in Figure 6.13. The I_{ON} and I_{OFF} were extracted using a 1.2 V window with the I_{ON} extracted at $V_{T,sat} - 0.9$ V and I_{OFF} at $V_{T,sat} + 0.3$ V. The ELA 450 split is clearly shifted to the right relative to the DSS 450 split. By taking a reference leakage current as a horizontal line in the plot, the ELA 450 split clearly outperforms the DSS 450 split in drive current. The I_{ON} - I_{OFF} plot shows an average I_{ON} improvement of 37% for the ELA 450 PFETs over the reference DSS 450 PFETs at an I_{OFF} of 10^{-7} A/wire.

Figure 6.13. I_{ON} - I_{OFF} plot of the DSS 450 and ELA 450 PFETs. I_{ON} extracted at $V_{T,sat} - 0.9V$ and I_{OFF} at $V_{T,sat} + 0.3V$.

Figure 6.14 shows that similar to the nanowire transistors, the ELA 450 PFETs fabricated on the SOI substrates with a planar structure also shows an improvement in the drive current and subthreshold slope. The subthreshold region for the ELA 450 planar PFET also shows better turn-on compared to the DSS 450 PFET by comparing the I_D - V_G of both splits as shown in Figure 6.14 (a). In addition to the subthreshold improvement, the average I_{ON} of the ELA 450 planar PFETs also shows a 22% gain over the reference DSS 450 planar PFETs as shown in Figure 6.14 (b). Greater improvements in the nanowire transistors could be possibly due to the higher surface temperature generated in the wire than planar structure for the same laser fluence as a result of the confinement effect in GAA nanowire, leading to more defects formation in the Si. However, it is clear that the effect of ELA is significant in both nanowire and planar transistors.

Figure 6.14. (a) I_D - V_G characteristics of the DSS 450 and ELA 450 PFETs with planar structure. (b) I_{ON} - I_{OFF} plot of the DSS 450 and ELA 450 PFETs with planar structure. I_{ON} extracted at $V_{T,sat} - 0.9\text{V}$ and I_{OFF} at $V_{T,sat} + 0.3\text{V}$.

The effect of ELA is straight forward in PFETs where the incorporation of ELA effectively enhances the drive current over the reference PFETs without ELA. However, the effect of ELA is not entirely similar in NFETs. Figure 6.15 shows typical I_D - V_G characteristics of the DSS 550 and ELA 450 NFETs. It is observed that the drive current at low V_D (0.05V) for the DSS 550 NFETs is lower than the ELA 450 NFETs by approximately one order of magnitude. In Section 5.3.3 the effect of the Fermi level pinning in DSS NFETs is revealed as the main reason contributing to low drive current in the linear region (low V_D). The origin of the incomplete Fermi level de-pinning by dopant segregation is due to the insufficient electrically active phosphorus at the NiSi/Si interface. By using ELA, Fermi level de-pinning can be realized through introduction of additional defects which increases the amount of activated phosphorus from the available phosphorus atoms near the interface region. This is remarkable as ELA permits silicidation temperature as low as 450°C to be effective in the Fermi level de-pinning.

Figure 6.15. I_D - V_G characteristics of the DSS 550 and ELA 450 NFETs.

To understand the interaction between the effect of silicidation temperature and ELA, it is crucial to compare the I - V characteristics of NFETs with various annealing conditions as shown in Figure 6.16. The I_D - V_G curves of DSS 450, DSS 550 and ELA 450 NFETs at a low V_D of 0.05 V are compared to minimize the influence from the drain on the SBH. As mentioned in Chapter 5, the DSS 450 NFET has a large threshold voltage shift, severe short channel effects and large off state leakages which indicate the existence of a relatively large SBH. This is evidently pointed out in Section 5.3.5 where the effective SBH of the DSS 450 NFET is indeed relatively higher at 0.22 eV as compared to that of the DSS 550 NFET.

Without the incorporation of ELA, the effective SBH of NFET can be reduced by elevating the silicidation temperature from 450°C to 550°C. The DSS 550 NFET has a lower effective SBH of 0.16 eV which manifest in the low V_D I - V curve as having superior short channel effects immunity as well as lower off state leakages. However, attention should be paid to the drive current as V_G is increasingly larger. The drive current of the DSS 450 and DSS 550 NFETs do not show signs of significant disparity.

Figure 6.16. Low V_D (0.05V) I_D - V_G of NFETs with various annealing conditions.

However, with the incorporation of ELA, even at subsequent silicidation temperature of 450°C , the ELA 450 NFET displays both superior short channel effects immunity and higher drive current. In this example of Figure 6.16, the improvement gained by employing ELA without increasing the silicidation temperature is evidently larger than by only implementing higher silicidation temperature. Hence, to take one step further, it is interesting to investigate the combined effect of implementing both the ELA and elevated silicidation temperature.

The effect of post ELA silicidation temperature is compared in the I_D - V_G characteristics shown in Figure 6.17. The ELA-DSS NFET with an elevated silicidation temperature at 550°C is referred to as ELA 550 NFET. In this example, the difference is relatively small judging from the I_D - V_G curves. However, judging from the result it is obvious that the short channel performance and the off-state leakages are closely matched.

Figure 6.17. I_D - V_G characteristics of the DSS 550 and ELA 450 NFETs.

The drive current of both the ELA 450 and ELA 550 NFETs is compared in Figure 6.18. Both the ELA 450 and ELA 550 NFETs have linear regions with fast turn-on that resemble conventional MOSFETs, unlike the linear region of DSS 550 NFET which shows sign of gradual turn-on with convex curvature usually seen in Schottky barrier MOSFETs. In addition, the ELA 550 NFET shows further improvement in the drive current from the ELA 450 NFET. This suggests that there is an additive effect of the ELA and silicidation temperature on the transistor performance.

Figure 6.18. I_D - V_D of NFETs with various annealing conditions.

Figure 6.19. I_{ON} - I_{OFF} plot of NFETs with various annealing conditions. I_{ON} extracted at $V_{T,sat} + 0.7V$ and I_{OFF} at $V_{T,sat} - 0.3V$.

As shown in Figure 6.19, by plotting the I_{ON} - I_{OFF} of individual devices, the performance of each split can be statistically better represented. The I_{ON} and I_{OFF} were extracted using a 1.0 V window with the I_{ON} extracted at $V_{T,sat} + 0.7V$ and I_{OFF} at $V_{T,sat} - 0.3V$. The lines in the figure are best fit linear lines of each split. The result is consistent with the results shown previously where the DSS 550 NFETs prevail with the best electrical performance in term of on/off current ratio. However, we note that there is some overlaps of data points and a crossover of best fit lines between the DSS 550 and ELA 450 NFETs within the range of interest. This is an indication of close resemblance of device performances. The result may seem contradicting to the claim that the ELA 450 NFETs perform better than the DSS 550 NFETs. However, Figure 6.15 clearly shows that at a higher V_D of 1.0 V, the difference in the drive current between both splits is in fact marginal. The crossover of the two splits show that the ELA 450 NFETs drive relatively larger currents in smaller devices while the DSS 550 NFETs perform better in longer devices. The reason to the I_{ON} - I_{OFF} performance similarity between the ELA 450 and

DSS 550 NFETs is due to additional SBH lowering induced by the drain. When the V_D is larger, the influence of V_D induced SBH lowering would also be larger such that the difference between the SBH becomes smaller.

It is now clear that in order for PFETs and NFETs to perform optimally, ELA together with optimal silicidation temperature are desired i.e., ELA 450 for PFETs and ELA 550 for NFETs. However, it is also critical to reap maximum benefit from the ELA such that maximum defects can be generated in the exposed Si without compromising the integrity of the device structure.

Figure 6.20. I_G of the DSS and ELA-DSS PFETs extracted at $V_G = -1V$.

Figure 6.20 shows the gate leakage, I_G of the DSS and ELA-DSS PFETs extracted at $V_G = -1V$. For the ELA-DSS PFETs, two laser fluencies were employed namely 70 mJ/cm² (which is the fluence used throughout the study of ELA-DSS PFETs) and 100 mJ/cm². As shown in Figure 6.11 for the simulation work on SOI substrate, 100 mJ/cm² is at the threshold which is sufficient to induce surface melting. The simulation is based on S/D Si thickness of 20 nm. With a poly-silicon gate of 60 nm thick, the capacity to heat generated by the laser is slightly larger. Hence, the temperature of the gate should be

slightly lower than the melting threshold which should not compromise the integrity of the gate dielectric layer directly beneath the poly silicon gate. With a measurement performed on 200 nm long transistors and an average nanowire diameter of about 10 nm, it is observed that the DSS PFETs have a mean I_G of approximately 1.5×10^{-14} A. The mean I_G of the ELA-DSS PFETs with a laser fluence of 70 mJ/cm² is also at about the same value. However, as the laser fluence was increased to 100 mJ/cm², it is found that not only the mean I_G has increased by more than 100% to 3.2×10^{-14} A but the spread of the individual I_G has also expanded. The fluctuation indicates a large distribution of generated temperature in the gate among the devices, possibly compounded by the fluctuation in the laser fluence.

Figure 6.21. (a) I_D - V_G and (b) I_D - V_D of the ELA 450 PFETs with different laser fluencies. The split with 100 mJ/cm² has significantly higher GIDL compared with the reference split of 70 mJ/cm².

Although I_G is considered tolerable at the level of 10^{-14} A, it is also crucial to examine the influence of the elevated laser fluence on the device performance. Figure 6.21 shows the I_D - V_G and I_D - V_D of two ELA 450 PFETs processed with laser fluencies at 70 and 100 mJ/cm². It is found from the I_D - V_G that by increasing the laser fluence from 70 to 100 mJ/cm² the leakage current at $V_D = 1.2$ V increases remarkably by approximately 3

orders of magnitude. The I_D-V_D also shows that the drive current increases by an astounding 75%. The high leakage ‘tail’ at positive gate bias is attributed mainly to gate induced drain leakage (GIDL) where the high temperature near melting threshold results in diffusion of dopants in the S/D towards the nanowire channel. This is consistent with the SIMS analysis shown in Figure 6.6 where boron atoms begin to diffuse at melting threshold. The severe overlap of the gate to the S/D region is the main reason behind the observed GIDL. Furthermore, the diffusion of dopants towards the channel reduces the effective channel length which may be the main reason of the extremely high improvement in the drive current.

It is expected that further optimization of PFET can be realized by fine tuning the laser fluence between 70 and 100 mJ/cm² to maximize defects generation and to minimize GIDL effect. However, the proof of concept of the ELA in nano-scaled device performance is demonstrated in this study.

6.5.2 Short channel performance

Figure 6.22 depicts the comparison of the DIBL, subthreshold slope, and $\Delta V_{T,sat}$ plotted as functions of L_G between the DSS 450 and ELA 450 PFETs. It is found that for devices longer than 100 nm, the two splits of PFETs do not show any significant difference among themselves. For L_G smaller than 100 nm, the ELA 450 PFETs show a significant improvement over the DSS 450 PFETs in term of DIBL, subthreshold slope and $\Delta V_{T,sat}$. This is attributed to the higher active boron concentration at the NiSi/Si interface which contributes to a lower effective SBH.

Figure 6.22. (a) DIBL, (b) Subthreshold slope, and (c) $\Delta V_{T,sat}$ plotted as a function of physical gate length, L_G of the DSS 450 and ELA 450 PFETs.

Figure 6.23. (a) DIBL, (b) Subthreshold slope, and (c) $\Delta V_{T,sat}$ plotted as a function of physical gate length, L_g of the DSS 550 and ELA 550 NFETs.

Figure 6.23 compares the short channel performance between the DSS 550 and ELA 550 NFETs in terms of DIBL and subthreshold slopes. Similar to PFETs, the NFETs also show improvement in short channel effects immunity with reduced DIBL at short channel devices. The NFETs subthreshold slopes, however, has a different pattern from that of the PFETs. The subthreshold slopes are improved overall from short to long channel NFETs. This may be due to the slightly higher SBH of NFETs compared to PFETs before and after laser annealed, which shall be discussed in a subsequent section.

6.5.3 Series resistance

In Section 6.5.1 and 6.5.2, the I - V characteristics and the short channel effects immunity of the ELA-DSS transistors are shown to be superior to the DSS transistors. The improved performance is attributed to the enhanced active dopant concentration at the NiSi/Si interface which ultimately reduces the SBH of the MS junction of the Schottky S/D junctions.

Figure 6.24. R_{TOTAL} vs. L_G plot of the DSS 450 and ELA 450 PFETs. Mobility is not affected by the ELA as it can be seen from both splits having the same slope.

To qualitatively examine the SBH of the transistors, R_{TOTAL} of individual transistor is plotted as a function of L_G . The y -intercept of the best fit line describing the split shows the average parasitic external resistance. As discussed in Section 2.3 the external resistance of a Schottky barrier transistor consists of the metal sheet resistance and the MS contact resistance. Transistor with a lower S/D SBH should translate into a lower MS contact resistance. This manifests as an overall decrease in the total external resistance provided the sheet resistance of the silicide is the same. In the case of DSS or ELA-DSS transistors, the silicidation temperature is kept constant. Hence, the assumption of constant silicide sheet resistance should be valid. Figure 6.24 shows the R_{TOTAL} of the

DSS 450 and ELA 450 PFETs. The R_{TOTAL} plot shows a clear trend of the ELA 450 PFETs having a smaller external resistance compared to the DSS 450 PFETs. The extracted average external resistance of the DSS 450 and ELA 450 PFETs are 260 and 127 $\Omega\text{-}\mu\text{m}$, respectively. In addition, the parallel slopes of the two split of devices in Figure 6.24 also indicate that there is negligible or no change in the mobility before and after the incorporation of ELA. This shows that the Si nanowire channel is well protected when non-melt laser fluence is properly utilized.

Figure 6.25. R_{TOTAL} vs. L_G plot of the DSS 550 and ELA 450 NFETs.

In Section 5.3.3, the DSS 550 NFETs have been shown to have a trendless R_{TOTAL} distribution when plotted against the L_G . This has been attributed to insufficient Fermi level de-pinning of the electron SBH due to a low active phosphorus concentration at the NiSi/Si interface. By incorporating ELA, however, the active phosphorus concentration has been increased which is expected to enhance the Fermi level de-pinning in the NFETs. Indeed, a trend is now observed with the ELA-DSS NFETs as shown in Figure 6.25. Notice that the laser annealed device was silicided at 450°C. This indicates that ELA

plays a more critical role than the silicidation temperature in the Fermi level de-pinning of the NFETs, at least within the temperature range that is used within this study.

6.5.4 Defect enhanced dopant activation

To better understand the influence of ELA on dopant activation at the NiSi/Si interface, the mechanism of defect enhanced dopant activation has to be understood. Assume that there is an activation energy required by dopant atoms to be electrically activated at or very near the interface. The activation energy may be arbitrarily defined as the lowest energy required to activate X percent of the chemically available dopants at the interface. The activation energy at the interface is lower than that in the bulk due to the generation of point defects. During silicidation, Ni atoms diffuse through NiSi into Si substrate and weaken the Si-Si bonds. As a result, Si bonds at the Ni/Si or NiSi/Si interface can be broken at a much lower temperature as compared to the bulk Si. The Si-Si bond breaking can be seen as generation of Si self-interstitial and vacancy pair.

In Section 6.2, a hypothesis is made which states that these point defects provide a lower activation energy path than the bulk value and as a result, it effectively lowers the overall dopant activation temperature. The activation energy involving the individual dopant atom is the microscopic activation energy which refers to the energy difference between an initial state and an activated complex during a transition. The energy barrier must be overcome in order to achieve the final state or the product of the reaction. However, in describing the overall dopant activation, macroscopic activation energy is preferred. Macroscopic activation energy is the apparent energy usually obtained in an Arrhenius plot describing the reaction rate as a function of reaction temperature. The concept of micro- and macroscopic activation energy is illustrated in Figure 6.26. The macroscopic activation energy is collectively contributed by factors such as the lower

energy barrier defect enhanced activation as well as the higher energy barrier bulk activation. The explicitly relationship between the macro- and microscopic activation energies shall not be investigated here. However, it is reckoned that as the amount of defects with lower microscopic activation energy is increased, the overall or macroscopic activation energy should be lower.

Figure 6.26. Illustration of (a) macroscopic activation energy, and (b) microscopic activation energy. Reproduced from ref. [189].

For simplicity, by treating the dopant atoms using Maxwell-Boltzmann distribution in solid state kinetics [190], one can describe the macroscopic activation energy, E_a as a vertical line separating the activated dopants (area under the curve to the right of E_a) and the inactivated dopants (area under the curve to the left of E_a) in the distribution as shown in Figure 6.27. By increasing the amount of defects in the Si, the macroscopic activation energy is lowered or shifted leftward in the distribution which means more activated dopants.

Figure 6.27. Illustration of an energy distribution of dopant atoms in Si during thermal processing according to Maxwell-Boltzmann theory. The distribution is not drawn to scale. The mean energy is represented by E_{mean} .

Figure 6.28. Illustration of energy distributions of boron in Si. The distributions are not drawn to scale.

Figure 6.28 illustrates the case of boron activation at the interface, where E_a is arbitrarily placed to the left of the peak of the boron energy distribution curve. As the mean dopant energy, E_{mean} of the boron atoms is increased from 450°C to 550°C, the distribution is ‘flatten’ and the E_{mean} is shifted to the right. This results in more boron atoms being activated. However, due to the relatively low E_a which already included most of the area under the distribution curve at 450°C, an increase in temperature or a shift of

E_{mean} only increases a relatively small percentage of activated boron. This explains the DSS PFET results in Chapter 5 where the DSS 550 PFETs do not show much improvement in the device performance as compared to the DSS 450 PFETs.

Figure 6.29. Illustration of energy distributions of phosphorus in Si. The distributions are not drawn to scale.

Experimentally, the electrical results show a slightly different pattern for the phosphorus doped samples. It is thought that the E_a required for phosphorus activation at the interface is higher than that of boron. For illustration purposes, Figure 6.29 shows that the E_a for phosphorus is placed arbitrarily at the right of the peak. At 450°C, clearly only a fraction of the dopants to the right of the E_a is activated. This could be used to explain the Schottky behaviour seen in the DSS 450 NFETs in Figure 5.12 in Chapter 5. By elevating the silicidation temperature to 550°C, the rightward shifted E_{mean2} now engulfs more area to the right of E_a under the distribution curve which means more dopants are activated.

Figure 6.30. Illustration of the effect of lower E_a on energy distributions of phosphorus in Si. The distributions are not drawn to scale.

Even though the exact E_a values and the explicit distribution curves for boron and phosphorus are not quantitatively determined, the above qualitative model provides necessary information on the importance of E_a in affecting the dopant activation. There are two methods to increase the active dopants based on the model namely, 1) increase the silicidation temperature and 2) reduce the E_a . To obtain the optimal sheet resistance value, NiSi is the most desirable silicide phase. This sets a boundary for the maximum allowable silicidation temperature which is typically less than 700°C (phase transformation to NiSi₂ beyond this temperature occurs). Therefore, it is desirable to achieve low E_a through defect engineering by ELA. Additional defects are created during ELA prior to silicidation induced dopant segregation. These additional defects, as proven by the PL analysis, increase the total amount of defects in the Si which substantially reduces the E_a . As shown in Figure 6.30, with the introduction of ELA induced defects the E_a is reduced from E_{a1} to E_{a2} . Hence, even at 450°C, E_{a2} is sufficient to activate a larger fraction of dopants as compared to E_{a1} . In addition, by increasing the temperature from 450 to 550°C, a further gain in activation can be attained. However, the gain from

450 to 550°C with E_{a2} (with ELA) is arguably less than the gain obtained with E_{a1} (without ELA).

6.5.5 Effective SBH

Figure 6.31. Effective SBH as a function of gate overdrive of typical DSS 450 (nanowire) and ELA-450 (nanowire and planar SOI) PFETs.

By performing the effective SBH extraction method described in Section 5.3.5, the effective SBH of ELA-DSS N- and PFETs are obtained and compared to the DSS N- and PFETs. Figure 6.31 shows the effective SBH as a function of gate overdrive of typical DSS 450 and ELA 450 PFETs. At large overdrive, the DSS 450 PFET already has a low effective SBH of 0.03 eV. However, the laser annealed device clearly shows a further reduction in the effective SBH with value approaching 0 eV. This shows that the series resistance reduction in the ELA 450 PFETs observed in Section 6.5.3 is indeed contributed by a lower contact resistance through reduction in the effective SBH. An ELA 450 PFET with planar structure built on SOI substrate is also compared to the nanowire DSS 450 and ELA 450 PFETs. The planar ELA 450 PFET obviously has the highest effective SBH among the devices, higher than the nanowire DSS 450 PFET. In addition, the modulation by gate voltage of the planar PFET is less rapid as compared to the

nanowire PFETs. This is attributed to the enhanced gate-to-channel electrostatic control by GAA structure in the nanowire PFETs. The observation shows that both GAA structure and the incorporation of ELA are important to achieve excellent device performance.

Figure 6.32. Effective SBH as a function of gate overdrive extracted from NFETs with various annealing conditions.

In Section 6.5.4, the concept of E_a in Maxwell-Boltzmann distribution was discussed which pointed out the interesting results observed with the NFETs with silicidation temperature at 450 and 550°C. The interaction of the temperature with ELA suggests that not only should the laser annealed NFETs improve from the non laser annealed NFETs, the laser annealed NFETs with higher silicidation temperature should also improve slightly against the ones with lower temperature. Indeed, by employing ELA, the ELA 450 NFET achieves a lower effective SBH of approximately 0.07 eV, less than half of the effective SBH value of the DSS 450 NFET of 0.16 eV. Although the effective SBH value of the ELA 450 and ELA 550 NFETs are almost identical at 0.07 eV, arguably the ELA 550 NFET is relatively superior to the ELA 450 NFET by examining the low

gate overdrive region. At a lower gate overdrive of 0.5 V, the effective SBH of the ELA 550 NFET is lower.

Figure 6.33. R_{TOTAL} of the ELA 450 and ELA 550 NFETs compared at (a) high gate overdrive of 1.5V and (b) low gate overdrive of 0.5V.

By comparing R_{Total} of the ELA 450 to the ELA 550 NFETs at high gate overdrive (1.5 V) as shown in Figure 6.33 (a), it is found that both splits display the same external resistance. However, as shown in Figure 6.33 (b), by using a lower gate overdrive (0.5 V) two different external resistances are obtained. The ELA 450 NFETs have slightly higher external resistance than the ELA 550 NFETs. This is indeed consistent with the effective SBH analysis. Typical device operating voltage of advance technology as recommended by the ITRS roadmap is usually less than or equal to 1.1 V. With a threshold voltage of 0.2 to 0.3 V, the common gate overdrive would be 0.7 to 0.8 V. Thus, it is meaningful to examine the effective SBH at this voltage range. Certainly, the ELA 550 NFET is preferred in order to deliver the best performance.

6.6 Summary

ELA is shown to be capable of inducing defects in the Si substrate which is confirmed by PL analyses. During segregation, the laser induced defects provide a lower activation energy for dopant activation near the NiSi/Si interface which increases the active dopant concentration there. ELA-DSS diodes have been fabricated to confirm that the diodes behave with better linearity by the incorporation of ELA prior to dopant segregation.

Si nanowire ELA-DSS MOSFETs have also been fabricated and analyzed. The performance of the ELA-DSS MOSFETs was found to improve over the DSS MOSFETs in term of I_{ON} as well as short channel effects immunity i.e., subthreshold slopes and DIBL. The improvement is attributed to the reduced effective SBH by a more effective Fermi level de-pinning which is in turn contributed by a higher active dopant concentration at the S/D NiSi/Si interface.

A qualitative model based on the E_a and Maxwell-Boltzmann distribution of dopants is employed to explain the interaction and importance of the E_a and silicidation temperature to interfacial dopant activation. The results suggest that a high silicidation temperature and a low E_a are desired to yield the best electrical results for device performance.

Chapter 7 CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

Fabrication of Schottky barrier MOSFETs using Si nanowire as channel material involves the silicidation of nanowire S/D extensions. Thus, it is of great importance that a repeatable silicide intrusion into Si nanowire is developed. In this research project, a repeatable and consistent silicide intrusion of sub-40 nm into a 30 nm diameter Si nanowire was developed and demonstrated by using a proposed 2-step silicidation at 275°C followed by 450°C respectively. It is found that the effect of the RTA temperature is the dominant factor in the silicide intrusion length. The intrusion can be controlled by using a relatively low RTA1 temperature at 275°C for 30 s as compared to a severe intrusion with large and different intrusion lengths from S/D at 450°C for 30 s. By using the proposed RTA1, the effect of the Ni thickness becomes less critical and the resulted intrusion length differs by only 10 nm by increasing the Ni thickness from 14 nm to 30 nm. In addition, with RTA1 the intrusions in Si nanowire and in Si thin body are found to be almost identical. Electrical characterization confirmed that the 2-step annealing is effective in fabricating controllable silicided S/D Si nanowire Schottky barrier MOSFET with reproducible and stable I - V characteristics. The findings indicate that the silicide intrusion into Si nanowires can be well controlled and is repeatable by employing a 2-step annealing process.

To investigate dopant segregation, back contacted DSS diodes with boron and phosphorus segregation have been fabricated and analyzed. The linearity of the diode I - V characteristic is improved by increasing the dose and silicidation temperature. Phosphorus requires higher temperature above 550°C in order to make the dopant segregation effective compared to boron segregation at 450°C. Furthermore, the electrical and

chemical analyses show that the DSS diode I - V characteristic is dependent on the electrically active dopants at the interface.

With the knowledge of silicide intrusion and dopant segregation, GAA Si nanowire DSS MOSFETs have been successfully demonstrated and characterized. The results show that the DSS MOSFETs are superior to Schottky barrier MOSFETs. The DSS MOSFETs exhibit better electrical performance in term of I_{ON}/I_{OFF} ratio, good short channel performance with small subthreshold slope, DIBL and threshold voltage change down to $L_G = 100\text{nm}$ as well as a significant reduction in series resistance. The improvement is attributed to the thin layer of segregated dopants piling up at the NiSi/Si interface which results in Fermi level de-pinning of the SBH closer to the conduction/valence band edge. Activation energy extracted from low temperature measurement reveals that the effective SBH of the DSS PFET is lower than that of the DSS NFET by approximately 0.1 eV. The higher effective SBH of the DSS NFET is a result of the higher intrinsic SBH as well as the incomplete activation of phosphorus at the NiSi/Si interface, compared to the DSS PFET.

To further improve the dopant segregation, ELA induced defects has been employed. The generation of defects by ELA is confirmed by PL analyses. During segregation, the defects provide lower activation energy for dopant activation near the NiSi/Si interface which simultaneously increases the active dopant concentration there. ELA-DSS diodes have been fabricated to confirm that the diodes behave with better linearity with the incorporation of ELA.

Si nanowire ELA-DSS MOSFETs have also been fabricated and analyzed. The ELA-DSS MOSFETs are found to improve over the DSS MOSFETs in term of I_{ON} as well as short channel effects immunity i.e., subthreshold slopes and DIBL. The

improvement is attributed to the reduced effective SBH which is contributed by a higher active dopant concentration at the S/D NiSi/Si interface.

A qualitative model based on the activation energy, E_a and Maxwell-Boltzmann distribution of dopant energies has been used to illustrate the importance of the E_a and silicidation temperature to interfacial dopant activation. The results suggest that a high silicidation temperature and a low E_a are desired to yield the best electrical result for DSS MOSFETs. A low E_a can be achieved by employing ELA with appropriate fluencies to induce defects in the Si substrate without melting which causes adverse effects such as GIDL and gate dielectric degradation.

Finally, Table 7.1 summarizes the important factors that affect the effective SBH of the various devices discussed in this project in a simple and qualitative manner.

Table 7.1. Summary table illustrating the important factors effecting the effective SBH in Schottky barrier, DSS and ELA-DSS devices with planar or GAA architecture.

Factors affecting the Effective SBH	Planar			GAA		
	Schottky barrier	DSS	ELA-DSS	Schottky barrier	DSS	ELA-DSS
gate electrostatic	<i>Weak</i>	<i>Weak</i>	<i>Weak</i>	<i>Strong</i>	<i>Strong</i>	<i>Strong</i>
Fermi level de-pinning	<i>None</i>	<i>Strong</i>	<i>Stronger</i>	<i>None</i>	<i>Strong</i>	<i>Stronger</i>
Band bending of S/D depletion region due to doping concentration	<i>Weak</i>	<i>Strong</i>	<i>Stronger</i>	<i>Weak</i>	<i>Strong</i>	<i>Stronger</i>

7.2 Recommendations for future research

Several areas of research related to Si nanowire Schottky barrier MOSFETs could be studied for possible integration into the process in the semiconductor industry. These include:

1) *First principles study of dopant activation at the NiSi/Si interface.*

The interaction of dopant atoms with Si defects such as self-interstitial and vacancy can be studied by employing first principles calculation. The activation energies of different interactions can be quantitatively calculated and compared. Furthermore, various dopants can be simulated before experiments to determine the effectiveness of various dopant segregations at low RTA temperature.

2) *Dopant activation and diffusion in Si nanowire.*

Dopant activation and diffusion have been studied extensively in bulk Si substrate but it is still a relatively new topic in nanowires. Due to the large surface to volume ratio of the cylindrically shaped nanowire, the effect of surface states can no longer be neglected. In addition, the diffusion lengths of dopants are in the same order of magnitude as the nanowire radius. This aggravates the issues brought about by the nanowire surface. Hence, it is of great interest to investigate the surface effects and to explore the choices of dopants that are beneficial for semiconductor devices built by nanowires.

3) *SBH engineering using other methods or elements.*

Many SBH engineering methods have been proposed and demonstrated previously in the literature such as the use of rare earth silicides or thin insulators for Fermi level de-pinning. There is also research work on using unconventional elements such as sulfur, selenium, or chlorine as segregation species. As mentioned previously, dopant activation and diffusion between bulk and nanowire structure could have a large difference. Conventional semiconductor elements like boron, phosphorus and arsenic may not be the best choice of doping for nanowires. This opens up opportunities for the research of the most beneficial doping elements for nanowire MOSFETs.

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APPENDIX A THERMAL AND OPTICAL
PROPERTIES OF SILICON

1. Si thermal conductivity

Thermal conductivity for Si is fed into the COMSOL simulator as a function of Si temperature. The thermal conductivity between the input temperatures is estimated by the simulator using linear extrapolation between the values. The thermal conductivity of liquid Si is maintained at 0.22 regardless of the molten Si temperature.

Temperature (K)	Thermal conductivity (Wm ⁻¹ K ⁻¹)
273.2	1.68
300	1.48
350	1.19
400	0.989
500	0.762
600	0.619
700	0.508
800	0.422
900	0.359
1000	0.312
1100	0.279
1200	0.257
1300	0.244
1400	0.235
1500	0.227
1600	0.221
1685	0.22

2. Si heat capacity

The heat capacity between the input temperatures is estimated by the simulator using linear extrapolation between the values. The heat capacity of liquid Si is maintained at 1084 regardless of the molten Si temperature.

Temperature (K)	Heat capacity (Jkg ⁻¹ K ⁻¹)
295.2	716
315.7	771
335.4	805
364.8	826
375.5	830
412.1	855
440.2	859
471.7	902
512.2	876
559.4	910
602.9	914
673	877
709.6	926
746.9	959
800	946
849	954
973	924
1073	938
1173	952
1200	994
1273	968
1300	1004
1373	991
1400	1014
1500	1025
1600	1035
1690	1043
1700	1084
1800	1084
1900	1084

3. Reflectivity at 248 nm

$$R(\text{solid}) = 0.66$$

$$R(\text{liquid}) = 0.70$$

4. Absorption coefficient at 248 nm

$$\alpha(\text{solid}) = 1.8 \times 10^8 \text{ m}^{-1}$$

$$\alpha(\text{liquid}) = 1.56 \times 10^8 \text{ m}^{-1}$$

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