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Reduced Semiconductor Energy Conversion Systems

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Summary

Power converters are extensively used in energy conversion systems for converting electrical energy from one form to another. With the development of advanced semiconductor devices, modern power converters are also usually constructed with fully controllable switches, making them suitable for driving a wide range of loads. Some example applications of power converters are Uninterruptible Power Supplies (UPSs) for supporting critical loads during voltage outages, Universal Power Quality Conditioners (UPQCs) for power quality enhancement, renewable energy interfacing converters for green energy delivery and Dynamic Voltage Restorers (DVRs) for regulating load voltages.

Presently, most applications use a few types of proven traditional converter topologies. These converters have long historical records, and are therefore more trusted by the industry. However, relying on the traditional converters only does not guarantee better efficiency, lower cost and innovativeness. That prompts many researchers to propose new converter topologies usually with lower component counts. Lesser components are however almost always accompanied by some performance tradeoffs. A few commonly quoted tradeoffs are loss of independency between multiple driven loads, limited amplitude and phase-shift, and much higher stresses experienced by the remaining components. These tradeoffs can be expensive at times even though components are saved. It is therefore important to note that not all reduced component topologies are rewarding. Even for those proven useful, they cannot be generalized as suitable for all applications. A detailed application study needs to be conducted before a sound judgment can be made for the considered topology especially with reduced components.

The same principle applies to the nine-switch converter recently proposed for replacing the more generalized twelve-switch back-to-back converter found in many ac-ac energy conversion systems. As their names implied, the saving expected is three semiconductor switches or 25% in percentage term. This surely is an attractive saving if no severe limitation in performance is accompanied. Unfortunately, the nine-switch

converter is presently burdened by high dc-link voltage and heavily limited phase-shift between its terminal outputs even though it has been proven to work in motor drives and UPSs. These limitations are however not always severe. They are application-related even though it has presently not been clarified in the literature. It is therefore the intention now to study the nine-switch converter in greater details, believing that it can bring sizable advantages if controlled, designed and applied properly.

The investigation planned for the thesis is thus to revisit the nine-switch modulation principles and its existing ac-ac converter applications with an intermediate dc-link. The intention is to identify areas where modulation can be improved and quantify limitations faced by the nine-switch topology. Understanding those enables new modulation schemes to be proposed for the nine-switch converter before trying them with two suitable energy conversion systems. The first system is an UPQC chosen to represent an example series-shunt ac-ac system. The term “series-shunt” is used here for representing any system with two sets of three-phase ac terminals. One set of terminals is connected in series with the grid, while the other is connected in shunt. The analysis shows that with UPQC or most series-shunt systems, limitations faced by the nine-switch converter can greatly be reduced without affecting terminal performances. The saving of 25% semiconductor is thus less burdensome, and hence more attractive.

The second system investigated is an integrated renewable energy conversion system that can either be single or three-phase. It uses the same concepts as the UPQC, but is not confined to only ac sources and loads. It is in fact the first attempt to merge different ac and dc sources, storages and loads with a single integrated converter rather than multiple independent converters usually with more switches. The latter of course allows each converter to be controlled as per it is operating individually without interfering with the others. That is certainly an advantage, but because of the intermittent nature of most renewable sources, having multiple individual converters might not be a cost effective solution since most of them will not operate continuously. Using a single integrated system might therefore be more attractive especially when performance analysis proves that the saving in switches is not accompanied by burdensome limitations.

Although the two studied energy systems have demonstrated improvements, they nonetheless use the same nine-switch converter as other existing ac-ac applications mostly in ac motor drives. To gain further improvements, modifications to the basic converter topology must be done, where one possible area is to generate more than two switching levels per phase. The reduced switch concept is thus modularized, multiplied and then cascaded to form a new reduced switch multilevel converter. The proposed converter has been tried as an online UPS and an interline DVR, which so far have been proven to function well with no or minimized limitations.

Together, the four presented energy systems form an enriching guide for designer's reference. They help to clarify the real application scopes, advantages and disadvantages of the reduced semiconductor topologies. This information can then be weighed against the 25% saving in semiconductor, before making a sound decision on whether to pursue it. Practicality wise, all modulation schemes, converter topologies and energy systems presented have already been tested in the laboratory.

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List of Abbreviations

CF	Common Frequency
CSR	Current-Source Rectifier
DF	Different Frequency
DVR	Dynamic Voltage Restorer
DG	Distributed Generation
EV	Electric Vehicle
HVDC	High Voltage Direct Current
IMC	Indirect Matrix Converter
IDVR	Interline Dynamic Voltage Restorer
PR	Proportional-Resonant
PI	Proportional-Integral
PLL	Phase-Lock-Loop
SMC	Sparse Matrix Converter
SHE	Selective Harmonic Eliminator
USMC	Ultra-Sparse Matrix Converter
UPS	Uninterruptible Power Supplier
UPQC	Unifier Power Quality Conditioner
VSR	Voltage-Source Rectifier
VSI	Voltage-Source Inverter

Chapter 1 Introduction

1.1 Background and Motivation

Modern semiconductor devices have made possible the development of various power converters for converting energy from one form to another that better suits the load profiles. They can be found in a wide range of applications including mobile phone, television, refrigerator, computer, automobile and high voltage direct current (HVDC) to name only a few [1]-[5]. The power range of these applications spreads from a few milliwatts in the consumer market to hundreds of megawatts usually targeting at the utility. With the growing interest in renewable energy generation, demand for power converters as conditioning interfaces would continue to grow further, bringing along more investment in research and development [6].

Broadly, power converters can be categorized as ac-dc converters (rectifiers), dc-ac converters (inverters), ac-ac converters and dc-dc converters. Among them, rectifiers and inverters might be the most wide-spread in the industry since they are the most viable interfaces for connecting equipment to the utility grid. They can be programmed to regulate the load power and / or raise the input power quality. In many cases, rectifiers and inverters are also tied back-to-back to form ac-ac converters with double conversion and an intermediate dc-link. The simplest can be the twelve-switch configuration formed by cascading two standard six-switch converter bridges. Other more recent options include those indirect matrix and Z-source configurations found in [7]-[9]. The created ac-ac converters are usually used as Uninterruptible Power Supplies (UPSs), Unified Power Quality Conditioners (UPQCs) and Dynamic Voltage Restorers (DVRs) to name only a few [10]-[12].

Although there are presently a few standard converter topologies that have commonly being recommended, developmental trend in creating new untested converter topologies is still aggressively ongoing, especially in the academia. Most of the effort has been directed at reducing the number of passive and / or active components needed in order to lower the system costs. For passive components, the best known examples

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are probably direct and indirect matrix converters [13][14], whose layouts do not have an electrolytic dc-link capacitor. Reduced active component wise, two examples can be found in [15] and [16], where the four- and five-leg converters are presented with two sets of three-phase terminals each. The four-leg converter is designed with its third phase per terminal set drawn from the midpoint of a split dc-link. It is structurally no different from two four-switch B4 inverters [17] connected back-to-back. The total saving is thus four switches as compared with the usual twelve-switch or six-leg converter. The five-leg converter, on the other hand, has one phase-leg more than the four-leg converter. Instead of connecting to the split dc-link, the third phase per terminal set is connected to the fifth phase-leg. The number of switches saved is thus two.

A saving in components is unarguably attractive, but only if no significant tradeoff is introduced. This is unfortunately not the case with some commonly quoted tradeoffs being an increase in component stresses, a more limited terminal phase-shift and amplitude variation range, and a loss of independence between multiple driven loads. Some of these performance tradeoffs are also applicable to the recently proposed nine-switch converter, which was initially proposed for dual motor drives, rectifier-inverter systems and UPSs [18]-[20]. Despite producing the demanded terminal functions, nine-switch converters in these applications are heavily burdened by limited phase-shift and amplitude sharing between their two three-phase terminal sets.

They also need a much larger dc-link capacitance and a doubled dc-link voltage for producing the same two sets of ac voltages as the traditional back-to-back converter. Obviously, the requirements for larger dc-link capacitance and voltage would raise the system cost, and overstress the components. These constraints are however not always severe. They are application-related, which has so far not been clarified. Clarifying this belief is thus set as the first theme of the thesis, using an integrated UPQC as an example. Upon understanding the nine-switch converter better, the second theme planned is to widen its application range by including ac and dc sources, storages and loads to build a few more comprehensive integrated energy systems. Again, tradeoffs experienced by these systems must be kept low. The third theme then diverts temporarily away from applications to concentrate on creating a new cascaded

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multilevel converter with 25% reduction in semiconductors. This cascaded converter is then tested as an online UPS and an interline DVR, which respectively form the fourth and fifth themes of the thesis.

1.2 Major Contributions of Thesis

A number of original contributions have been proposed in the thesis. Their details, relevance and importance are elaborated as follows:

1.2.1 Optimal Pulse-Width Modulation Schemes

Optimal pulse-width modulation schemes have been proposed for the nine-switch converter with either better spectral performance or lower commutation count achieved. The specific objective aimed for depends on the converter operating modes, which for the nine-switch converter can either be the common frequency (CF) or different frequency (DF) mode. To understand these modes, it should again be emphasized that the nine-switch converter has two sets of three-phase output terminals controlled by two sets of three-phase modulating references. CF and DF modes then refer to the two references having the same and different frequencies, respectively.

For the CF mode, it is recommended that dc offset should only be added to the smaller reference. The other larger reference should be left centered within the vertical carrier band. The outcome would be one set of terminals experiencing slight performance degradation, while the other retains its optimal waveform quality related to centered space vector modulation. This recommendation is however not applicable to the DF mode, whose references cannot be centered by nature. A modified 120°-discontinuous modulation scheme is thus proposed for it to lower the converter commutation count by 33%. This modified 120°-discontinuous scheme can equally be applied to the CF mode if spectral quality is not the main concern.

1.2.2 Integrated Series-Shunt Power Conditioners

After evaluating the shortcomings experienced by previous applications of the nine-switch converter, a conclusion drawn is that it is not an attractive alternative for

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replacing two back-to-back connected shunt bridges at different operating frequencies. Such replacement is referred to as “shunt-shunt” in the thesis, and would usually require its dc-link voltage to be doubled. In the long term, it can easily shadow the semiconductors saved. Therefore, instead of such replacement, the thesis recommends that the nine-switch converter should more appropriately be used for replacing a series and a shunt converter like in a universal “series-shunt” power conditioner. For that, a UPQC has been chosen here as an example “series-shunt” conditioner for study. The goal is to quantify the advantages and minimized tradeoffs faced (e.g. 5% increase in dc-link voltage, not doubled), so as to better strengthen the reduced-switch solution provided by the nine-switch converter.

1.2.3 Compact Integrated Energy Systems for Distributed Generation

Nine-switch converter is so far always used to produce two sets of three-phase terminal voltages. Its applications can thus be quite limited. To further broaden the usefulness of the nine-switch converter, the next aim of the thesis is to generalize it to dc systems or a hybrid combination of ac and dc systems. A few integrated energy systems is eventually developed for tying various ac and dc sources, storages and loads to either a dc or an ac grid. The latter can either be single-phase or three-phase. The same 25% saving in semiconductors is achieved when compared with the straightforward practice of connecting multiple well-known converters at their common dc-link [21]-[23]. Performance tradeoffs, although present, are also minimized like in the UPQC.

1.2.4 Reduced Semiconductor Multilevel Converter and Its Applications

As per past trend, the next thought is to extend the reduced semiconductor concept to multilevel converter. For that, a modularized six-switch converter bridge is proposed. It has two sets of three-phase terminals, which can appropriately be cascaded to form a multilevel converter. Comparing to a normal back-to-back cascaded converter formed by H-bridges, the number of switches saved is again 25%, which can be a sizable amount for multilevel converter. The developed converter is then recommended for online UPS and interline DVR application, where either no real or minimized tradeoffs are introduced.

1.3 Organization of Thesis

The thesis comprises eight chapters organized as follows:

Chapter 1 introduces the background and motivation of the research, and summarizes the original contributions documented in the thesis.

Chapter 2 reviews power converters with reduced passive and / or active components. It describes their advantages and disadvantages, and elaborates more on the recently proposed nine-switch converter in terms of its modulation principles and performance constraints. The understanding gained helps with the subsequent creation of new modulation schemes, converter topologies and appropriate energy systems with reduced semiconductors. Relevant details can be found from Chapter 3 onwards.

Chapter 3 describes a few optimal modulation schemes for the nine-switch converter in various operating modes. Particularly, a 120° -discontinuous modulation scheme has been recommended for the nine-switch converter to allow it to reduce its commutation count by 33%. Mathematical and spectral analyses have been included for verifying the presented theory.

Chapter 4 presents control schemes needed for operating the nine-switch converter as a UPQC. UPQC is chosen here as an example series-shunt system, where one set of ac terminals is connected in series with the grid, while the other is in shunt. It is unlike earlier ac motor drive and UPS applications of the nine-switch converter, where both terminals are connected in shunt. Analysis shows that the nine-switch converter can maintain the same performance standard with lesser semiconductors and limitations in a series-shunt rather than shunt-shunt system.

Chapter 5 continues to show how the nine-switch converter can be used in integrated renewable energy generation systems. Instead of handling only ac sources and loads, the reduced semiconductor concept has now been broadened to include ac and dc

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sources, storages and loads. The created system, when multiplied, forms multiple distributed nodes for more reliable energy generation.

Chapter 6 modularizes the reduced semiconductor concept to create multiple six-switch modules for cascading. The resulting converter formed has better multilevel terminal characteristics, and uses lesser semiconductors than a traditional back-to-back cascaded multilevel converter. It however faces limitations, which fortunately can be reduced for certain applications. One prospective system is an online UPS, whose control and implementation are discussed in the chapter.

Chapter 7 continues with the findings presented in Chapter 6 by evaluating a second application for the proposed six-switch module with three-level phase switching characteristics. The system investigated is an interline DVR, which uses three six-switch modules to form a three-phase voltage restorer for protecting two independent ac grids. Voltage restoration of the grids is however constrained by the tighter reduced-switch operating range under ideal and non-ideal supply-load operating conditions. These constraints can better be managed through understanding the system, which is the theme of the chapter.

Chapter 8 concludes all findings, and suggests a few research topics for future investigation.

Chapter 2 Literature Review

Before elaborating on the original contributions of the thesis, this chapter reviews power converters with reduced passive and / or active components. It describes their pros and cons, and elaborates more on the recently proposed nine-switch converter in terms of its modulation principles and performance constraints. This understanding gained will help with the subsequent creation of new modulation schemes and integrated energy conversion systems with reduced semiconductor counts.

2.1 Introduction

Power electronic converters, assembled with diodes, thyristors and / or transistors, can be found in many systems, where conversion of electrical energy from one form to another is needed. Among them, three-phase ac-ac converters with or without an intermediate dc-link have found wide usage in the industry because of the popularity of ac motor drives and others linked to the ac grid. The simplest configuration at present would probably be a dc-ac voltage-source inverter (VSI) tied to an ac-dc diode rectifier. It has so far been used as a DVR, UPS, adjustable speed drive and others [24] because of its low cost and high reliability. It however draws highly distorted current from the grid and does not have regenerative capability. To resolve these shortcomings, a pulse-width modulated voltage-source rectifier (VSR) can be used instead [25] like in Fig. 2-1. Being controllable, the VSR can guarantee sinusoidal input current with or without unity power factor depending on requirement. It also allows energy to be returned to the grid instead of dissipating it unnecessarily.

The back-to-back arrangement in Fig. 2-1 has so far operated well, but is at times

Fig. 2-1 Back-to-back ac-ac converter

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discredited by premature failures caused by its dc-link electrolytic capacitor. Its switch count is also not minimized. An obvious ongoing trend is therefore to develop converter topologies with either no or reduced passive and / or active components. Some of these reduced converters are now reviewed to study their developmental theories before leading to the nine-switch converter. The nine-switch converter is a reduced semiconductor topology, whose operating principles form the background of the thesis. It is therefore reviewed thoroughly near to the end of the chapter.

2.2 Matrix Converters

To avoid the dc-link capacitance, direct and indirect matrix converters are probably the most commonly stated “all-semiconductor” examples [13][14]. They usually convert a fixed ac input voltage to an adjustable ac output voltage, whose amplitude is always lower than the input. They are therefore voltage-buck converters, whose similarities and differences between the direct and indirect variants are described as follows.

2.2.1 Direct Matrix Converter

Fig. 2-2 Direct matrix converter

Fig. 2-3 Indirect matrix converter

Fig. 2-2 shows the direct ac-ac matrix converter with no intermediate dc-link storage unlike the back-to-back converter shown in Fig. 2-1. Instead, it uses more semiconductors arranged as nine bidirectional switches for blocking voltage and conducting current in both directions [26][27]. Alternatively, reverse-blocking switches can be used if they are not too costly, and are of the right ratings. Irrespective of the switch type though, operating principles of the direct matrix converter remain the same, and can be explained with reference to Fig. 2-2. Quoting output phase *A* as an example, it is tied to the input phases through three switches, which at any one time can only have one of them turned on to avoid short-circuiting the input. The output voltage value can therefore be equal to the phase *a*, *b* or *c* value depending on which switch is turned on. Because of this, the output voltage waveform switches among various discrete voltage values, unlike just two found in a VSI. The same applies to the other two output phases, which together form the demanded three-phase output voltages.

Although the direct matrix converter has been proposed a couple of decades back, its actual deployment is not too impressive because of a couple of disadvantages. They include high switch count, limited harmonic and unbalance compensation, only voltage-buck operation, requirement for dc-link clamping circuit, and high sensitivity to input voltage disturbances [27]. These disadvantages will likely keep the direct matrix converter away from reach for many more years.

Fig. 2-4 Sparse matrix converter

Fig. 2-5 Ultra-sparse matrix converter

2.2.2 Indirect Matrix Converter

An alternative indirect matrix converter (IMC) can be found in [28][29], and shown in Fig. 2-3. The same eighteen unidirectional switches are used, even though arranged differently to give various topological differences. One noticeable difference is the possibility of dividing the IMC into a current-source rectifier (CSR) and a VSI tied at a fictitious dc-link. Current through the dc-link can be bidirectional, but voltage across it can only be unipolar. This topological difference has, to no extent, burdened the IMC from producing the same terminal performance as the direct matrix converter when driven by the same modulation scheme. Detailed verification has already been presented in [30].

Although the topological differences of an IMC produce no terminal difference, they do allow the IMC to be simplified with lesser switches used. One possibility is directed at the four-quadrant CSR shown in Fig. 2-3, which strictly is not necessary since the fictitious dc-link voltage can only be unipolar. It can therefore be simplified, leading to

Fig. 2-6 Four-leg converter

the fifteen-switch sparse matrix converter (SMC) shown in Fig. 2-4 [13][31]. When compared with the IMC, the SMC can appropriately be derived from the IMC in Fig. 2-3 by combining switches S_{app} and S_{anp} of phase-leg a into one. This merging is possible because both switches share the same gating signal, and will hence not affect the input and output performances of the SMC (remain the same as the IMC) [30]. The SMC however has a drawback caused by its higher conduction losses at some states.

The reduced SMC can further be simplified if only unidirectional power flow ($i_{dc} \geq 0$) is required. The resulting ultra-sparse matrix converter (USMC) with only nine switches is shown in Fig. 2-5 [32], which when compared with the SMC, is just the removal of switches S_{ap} and S_{an} from Fig. 2-4. The removal will not affect the converter performance since the switches carry no current during unidirectional power transfer. It will only limit the input power factor to above 0.866, which to a great extent, means wide-range reactive power compensation is not possible. Other mentioning of the reduced-switch matrix converters can be found in [33]-[35], which will probably not be elaborated here since they are based on the same topological concepts.

Although the IMC, SMC and USMC appear to be more advantageous than the direct matrix converter, their practical deployment is similarly not far reaching, probably because of the same reasons faced by the direct matrix converter. Research in them will however still continue, but is unlikely to outshine the back-to-back ac-ac converter formed by cascading two VSIs like in Fig. 2-1. Reduced-switch topologies of the back-to-back configuration are therefore more likely to draw interest with a few example circuits reviewed now, as follows.

2.3 Reduced-Switch Back-to-Back Converters

The usual back-to-back ac-ac converter is formed by cascading two six-switch bridges at their common dc-link like in Fig. 2-1. The total numbers of phase-legs and switches needed are thus six and twelve, respectively, which in theory are the maximum needed for completely independent operation at the two ac terminals. If such flexibility is not needed or a slightly compromised performance can be accepted, some switches can appropriately be saved like those possibilities proposed in [17]-[20] and introduced as follows.

2.3.1 Four-Leg Converter

A reduced-switch four-leg converter shown in Fig. 2-6 was proposed in [36] to replace the six-leg converter shown in Fig. 2-1. The new converter uses eight switches, and is no different from cascading two standard B4 converters at their common dc link. The resulting converter can therefore produce two sets of three-phase terminal voltages or currents that are sinusoidal, of unity power factor and of bidirectional power flow. Its spectral performances and terminal amplitudes can however be compromised because the third phase from each terminal set is drawn from the midpoint of a split dc-link, which then cannot be controlled independently. The saving of four switches, although attractive, should therefore be accessed carefully, depending on whether the tradeoffs can be tolerated.

To understand slightly more on how its tradeoffs are introduced, switching states of one B4 converter are considered, as illustrated in Fig. 2-7. Compared with the six-

Fig. 2-7 Voltage vectors of B4 inverter

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switch VSI which has six nonzero vectors and two zero vectors, the B4 converter only has four nonzero vectors, whose corresponding switch signals are also shown in Fig. 2-7. Mathematically, the vectors can be represented by the following complex expression:

$$\bar{u} = \frac{2}{3}(v_1 + \bar{a}v_2 + \bar{a}^2v_3) \quad (2.1)$$

where

$$\bar{a} = e^{-j2\pi/3}.$$

Substituting the terminal voltage values v_1 , v_2 and v_3 to (2.1) then leads to the following four individual vector expressions for the B4 converter:

$$\begin{aligned} v_1 = +V, v_2 = +V, v_3 = 0, & \Rightarrow \bar{u}_1 = V\left(+\frac{1}{3} + \frac{1}{\sqrt{3}}j\right) \\ v_1 = +V, v_2 = -V, v_3 = 0, & \Rightarrow \bar{u}_2 = V\left(+1 - \frac{1}{\sqrt{3}}j\right) \\ v_1 = -V, v_2 = +V, v_3 = 0, & \Rightarrow \bar{u}_3 = V\left(-1 + \frac{1}{\sqrt{3}}j\right) \\ v_1 = -V, v_2 = -V, v_3 = 0, & \Rightarrow \bar{u}_4 = V\left(-\frac{1}{3} - \frac{1}{\sqrt{3}}j\right). \end{aligned} \quad (2.2)$$

To produce sinusoidal waveforms, the four vectors should sequentially be used to track a circular path, whose maximum radius is 0.866 after normalized with V . That is undeniably smaller than the conventional six-switch VSI, whose modulation range can further be stretched by 15% after introducing triplen offsets. The same stretching cannot be done for the B4 converter whose third phase cannot be controlled independently. Terminal voltage of the B4 converter is therefore smaller than that of the six-switch VSI if they are given the same dc input. Alternatively, if they are

Fig. 2-8 Five-leg converter

demanded to produce the same ac output, dc voltage supplied to the B4 converter must be higher, which means higher switching stresses and losses created by its components [17].

Another compromise endured by the B4 converter is its requirement for larger dc-link capacitance, which in theory is needed to keep its split dc-link voltage variation and sensitivity to non-ideal ac load conditions low. Other comparative details can be found in [37]-[40], which are probably not repeated here since those mentioned are enough to show that compromises exist with reduced components.

2.3.2 Five-Leg Converter

A second back-to-back converter with reduced semiconductors is shown in Fig. 2-8, where ten switches or five phase-legs are used in total [15]. Unlike the four-leg converter, the third phase from each ac terminal set is now tied to a fifth phase-leg instead of a split dc-link. Its spectral performance and amplitude range are therefore improved, while yet retaining its bidirectional power flow and flexible power factor control. There are however still some tradeoffs to consider when compared with the twelve-switch converter shown in Fig. 2-1. Relevant comparative details are discussed after viewing through the operating details of the five-leg converter.

Referring again to Fig. 2-8, input (v_{i1} , v_{i2} and v_{i3}) and output voltages (v_{o1} , v_{o2} and v_{o3}) of the five-leg converter can respectively be written as:

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$$v_{ij} = v_{ij0} - v_{n0} = (2s_{ij} - 1) \frac{E}{2} - v_{n0}, \text{ for } j = 1, 2$$

$$v_{i3} = v_{30} - v_{n0} = (2s_3 - 1) \frac{E}{2} - v_{n0}$$

$$v_{oj} = v_{oj0} - v_{m0} = (2s_{oj} - 1) \frac{E}{2} - v_{m0}, \text{ for } j = 1, 2$$

$$v_{o3} = v_{30} - v_{m0} = (2s_3 - 1) \frac{E}{2} - v_{m0} \quad (2.3)$$

where E is the dc-link voltage, v_{i10} , v_{i20} , v_{30} , v_{o10} and v_{o20} are the input and output voltages measured with reference to the dc-link midpoint p (pole voltages), v_{n0} and v_{m0} are the node voltages at n and m measured with reference to p , and s_{i1} , s_{i2} , s_3 , s_{o1} and s_{o2} are the conduction states of the corresponding switches shown in Fig. 2-8 ($s = 1$ when ON and $s = 0$ when OFF). The switch signals are generated from the input and output voltage modulating references designated as v_{i1}^* , v_{i2}^* , v_{i3}^* , v_{o1}^* , v_{o2}^* and v_{o3}^* . From (2.3), the reference pole voltages can follow up be expressed as:

$$v_{ij0}^* = v_{ij}^* + v_{n0}^*, \text{ for } j = 1, 2$$

$$v_{30}^* = v_{i3}^* + v_{n0}^* = v_{o3}^* + v_{m0}^*$$

$$v_{oj0}^* = v_{oj}^* + v_{m0}^*, \text{ for } j = 1, 2 \quad (2.4)$$

Fig. 2-9 Nine-switch converter

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References in (2.4) can then be used with a carrier- or space-vector-based modulation scheme presented in [41]-[45] to produce the required gating signals for driving the five-leg converter. If modulated properly, the five-leg converter should in general be able to drive two loads with different requirements at its two ac terminals. However, because of its shared fifth phase-leg, it faces the limitations of higher dc-link voltage and higher current flowing through its fifth phase-leg. Unlike the four-leg converter though, the five-leg converter faces no severe low-order dc-link voltage variation even if its dc-link capacitance is small. This is of course gained at the cost of two additional switches.

2.3.3 Nine-Switch Converter

Table 2-1 Switch states and output voltages per phase

S_1	S_2	S_3	V_{AN}	V_{RN}
ON	ON	OFF	V_{dc}	V_{dc}
ON	OFF	ON	V_{dc}	0
OFF	ON	ON	0	0

The nine-switch converter shown in Fig. 2-9 was earlier proposed for dual motor drives and rectifier-inverter systems [18]-[20]. Unlike a normal two-switch phase-leg, the nine-switch converter uses three three-switch phase-legs, which together form two three-phase terminal sets sharing a common dc-link. Like those earlier mentioned reduced-switch topologies, the nine-switch converter faces some limitations created by its fewer switching states, when compared with the twelve-switch converter shown in Fig. 2-1. The allowed switching states can in fact be found in Table 2-1, which when decoded, leads to the following three possibilities.

- Both output terminals per phase tied to the upper dc rail P ($= V_{dc}$).
- Both output terminals tied to the lower dc rail N ($= 0V$).
- Upper terminal tied to the upper dc rail P and lower terminal tied to the lower dc rail N .

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Fig. 2-10 Arrangements of references having (a) the same frequency but different amplitudes (CF mode), and (b) different frequencies but the same amplitude (DF mode).

The last combination of connecting the upper terminal to N and lower terminal to P is not realizable, hence constituting the first limitation faced by the nine-switch converter. That limitation is however not a concern since it can be solved easily by placing modulating reference for the upper terminal above that of the lower terminal. Two diagrams showing the described placement can be found in Fig. 2-10 with a single common triangular carrier shown.

Imposing this basic rule of thumb on reference placement then results in those gating signals drawn in Fig. 2-10 for the three switches S_1 , S_2 and S_3 per phase. Equations for describing them can also be written here as:

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$$S_1 = !S'_1 = \begin{cases} ON, & \text{if upper reference is larger than carrier,} \\ OFF, & \text{otherwise} \end{cases}$$

$$S_3 = !S'_3 = \begin{cases} ON, & \text{if upper reference is larger than carrier,} \\ OFF, & \text{otherwise} \end{cases}$$

$$S_2 = S'_1 \oplus S'_3. \quad (2.5)$$

where $\oplus$ is the logical XOR operator.

Signals obtained from (2.5), when applied to the nine-switch converter, lead to those voltage waveforms V_{AN} and V_{RN} per phase shown at the bottom of Fig. 2-10. Together, they show that the forbidden state of $V_{AN} = 0V$ and $V_{RN} = V_{dc}$ is never produced, but at the expense of more limited reference amplitudes and phase-shift. These limitations can clearly be seen in Fig. 2-10(a) and (b), where the former shows two references of common frequency facing a limited phase-shift. The latter, on the other hand, shows two references of different frequencies limited by a maximum modulation ratio of only 0.5. This value can be raised by 15% if triplen offset is added, but is still lower than the usual of 1.15 permitted by the back-to-back converter shown in Fig. 2-1. To get a certain ac terminal voltage, the dc-link voltage for the nine-switch converter must therefore be doubled as compared to the back-to-back converter shown in Fig. 2-1. This is in fact the limitation faced by the nine-switch drive systems proposed in [18][19] when their two terminal sets are approximately at the same rated voltage, but at different operating frequencies.

Summarizing in brief, the major pros and cons of existing nine-switch applications are listed in Table 2-2. They do not appear attractive since the intended semiconductor

Table 2-2 Advantages and disadvantages of existing nine-switch applications

Advantages	Disadvantages
<ul style="list-style-type: none"> Reduced semiconductor count and driver circuits Same complexity in implementation, control and modulation schemes Lower system costs (application-related) 	<ul style="list-style-type: none"> Increase in dc-link voltage (maximum doubled) Oversized and stressed components Limited amplitude sharing and constrained phase-shift

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saving can easily be shadowed by those unintended disadvantages listed in Table 2-2, especially for cases where different terminal frequencies are required. Instead of accepting these tradeoffs as hurdles, the intention of the thesis is to concentrate on a few prospective energy conversion systems, where effects of the tradeoffs are either eliminated or reduced to make the saving of semiconductors more attractive. The same reduced semiconductor concept and application studies can then be extended to back-to-back cascaded multilevel converter. The proposed energy systems found in the thesis can therefore be used as a useful guide for judging the application scope, pros and cons of using reduced semiconductor topologies.

2.4 Summary

This chapter reviews some reduced component topologies that have recently been studied as alternatives for the traditional back-to-back ac-ac converter. For those that use reduced passive components, matrix converters with no dc-link storage are probably the best known examples claimed to be more compact and have a longer lifespan. Active component reduction wise, the four-leg, five-leg and nine-switch converters have been reviewed. These reduced component topologies generally look attractive, but should be considered more thoroughly with their accompanied tradeoffs. A balance exists, which unfortunately is application-related. It is therefore important to focus on applications to identify prospective energy conversion systems where the reduced converters can have real advantages. This is the challenge structured for the thesis with reference to the newly proposed nine-switch converter.

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

This chapter proposes a few optimal modulation schemes for the nine-switch inverter under various operating conditions. Quantitative analysis, in terms of modulation constraints, has been presented together with the proposal of a few optimal carrier-based modulation schemes. Particularly, a 120°-discontinuous modulation scheme has been recommended for the nine-switch inverter, which when implemented, will reduce its commutation count by 33%.

3.1 Introduction

As discussed in Chapter 2, a summarizing observation noted for the component-saving topologies is that performance tradeoffs are almost always unavoidable. To name some, common tradeoffs would include loss of independency between multiple driven loads, limited amplitude and phase-shift, and usually much higher stresses experienced by the remaining components, which can at times be expensive to compromise, even if components are saved. Therefore, before a sound judgment can be made with regard to the adoption of a certain simplified topology, its limitations and gains must first be properly quantified (in addition to qualitative reasoning), so as to help bring fore relevant details needed for making a sound decision. On another frontier, the development of modulation schemes for operating the converters at their respective optimal points is also judged as important, since these optimal points are already compromised, and therefore should not be further deteriorated, if attractiveness of the simplified topologies is to be preserved.

The same concerns shared above are equally applicable to the nine-switch inverter with two sets of three-phase interfacing terminals. The nine-switch inverter is structurally similar to the back-to-back converter, except with three lesser active switches used, and is therefore burdened by some performance tradeoffs. In spite of that, the nine-switch inverter has so far been proven to work well in dual motor drives

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

with different terminal frequencies (DF mode) [18][19], and ac-ac converters like an online uninterruptable power supply (UPS) with a single common terminal frequency (CF mode) [46]. These examples have already confirmed the practicality of the nine-switch inverter, and the possibility of using it in place of the back-to-back converter. However, its quantitative tradeoffs in relation to relevant modulation constraints have not yet been fully studied, which is now attempted in this chapter.

Based more on carrier-based realization rather than the space vector approach recommended in [47], the candidate (under the direction of his supervisor and Gao et al) has proposed a few improved modulation schemes for the nine-switch inverter. The same modulation schemes have been used for the subsequently discussed nine-switch applications found in later chapters. These schemes take advantages of the different operating scenarios encountered during the two operating modes, whose performances

Fig. 3-1 Back-to-back converter with twelve switches in total

Fig. 3-2 Nine-switch inverter

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have already been confirmed in simulation and experimentally using a scaled down laboratory prototype.

3.2 Operation Principles of Nine-Switch Inverter

To better understand differences exhibited by the back-to-back converter and nine-switch inverter, both of them are drawn again in Fig. 3-1 and Fig. 3-2 with their switches properly labeled to conveniently show how the latter is derived from the former. Beginning with the back-to-back converter shown in Fig. 3-1, twelve switches are noted in total with six of them independent and the other six dependent. For the independent switches labeled as SX and SY (X = A, B or C, and Y = U, V or W), their gating signals are obtained by comparing two sets of three-phase independent modulating references with either a single carrier or two different carriers. The ON-OFF pulse signals obtained can then be diverted to drive SX and SY independently, while their logical inversions can be used for driving the dependent switches labeled as SX' and SY' ($SX' = !SX$, $SY' = !SY$, where ! is the logical NOT operator). Merging of SX' and SY' then gives rise to the nine-switch inverter shown in Fig. 3-2, whose gating signals for the middle switches, labeled as SXY, are obtained by simply applying the logical XOR operator to those signals earlier derived for SX' and SY'. Inserting of dead-times to protect the nine-switch inverter against any accidental short-circuit is also automatically taken care of by the XOR-ing process, so long as proper dead-times are inserted to {SX, SX'} and {SY and SY'}, as per controlling a normal VSI [18].

Other than the simple XOR modification, gating signals to the remaining switches in the upper and lowermost rows of Fig. 3-2 remain unchanged, hence making it sensible to label them with the same SX and SY symbols. Labeling with the same symbols however does not mean that they are fully independent, and can be controlled by any independent three-phase modulating references like those found in the back-to-back converter. To illustrate the presence of dependency and hence a resulting forbidden state in the nine-switch inverter, phases A and U from the same phase-leg are considered, where it is noted that tying of phase A to the lower dc rail and phase U to the upper dc rail cannot occur simultaneously. That then leaves only three valid states

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

for each phase-leg of the nine-switch inverter, whose switching details per phase-leg are drawn in Fig. 3-3 and described as follows.

- State {1}: Both phases from the same phase-leg tie to the upper dc rail by turning $SX = SXY = ON$. Since they are both positive, this state is represented by a normalized positive 1.
- State {0}: Phase X ties to the upper rail while phase Y ties to the lower rail by turning $SX = SY = ON$. Since phase X is positive while phase Y is negative, the resulting state is represented by the neutral number of 0.
- State {-1}: Both phases tie to the lower dc rail by turning $SXY = SY = ON$. Since they are both negative, the resulting state is represented by a normalized negative 1.

In total, only three out of eight possible gating combinations are used by the above three states, where two ON signals are distributed among the three switches of SX , SXY and SY per phase-leg. The other three combinations with only one ON signal can happen during dead-time, inserted to protect the converter against the short-circuit combination of accidentally turning ON all three switches. Although not damaging like the all-ON combination, the last all-OFF combination should generally be avoided too,

Fig. 3-3 Switching states obtained in CF mode using two in-phase references.

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

since it leads to uncontrollable phase outputs, whose values are passively determined by the directions of current flows. This non-actively defined behavior can at times cause normalized volt-sec error, but is fortunately avoided by the nine-switch inverter, whose modulation constraints inhibit it from happening, as demonstrated in Fig. 3-3 and all other modulation diagrams shown in the chapter.

3.3 Continuous Modulation

As explained in section 3.2, a forbidden state exists for the nine-switch inverter, and corresponds to the case, whereby an attempt is made to simultaneously tie the upper phase to the lower dc rail and the lower phase from the same phase-leg to the upper dc rail. To avoid this forbidden state, the method recommended in [18]-[20] is to arrange the two modulating references per phase-leg such that the phase X reference (Ref X) is always higher than the phase Y reference (Ref Y), like what is shown in Fig. 3-3. Also noted in Fig. 3-3 is that only a single common carrier can be used, unlike the back-to-back configuration where a second phase-shifted carrier can be added, if intended [25]. These constraints to a sizable extent limit the amplitudes and phases that can be obtained from the two terminal sets of the nine-switch inverter, whose details for CF and DF modes are now discussed, as follows.

3.3.1 CF Mode

CF mode occurs when the inverter is commanded to output two sets of three-phase voltages at the same frequency, but not necessarily the same amplitude and phase. Examples, where this mode can be of interest, include the driving of dual motors in an EV in the straight-line regime [15], and online UPS tasked to output a more stabilized amplitude at the same grid frequency [46]. Despite their different operating objectives, CF mode for both applications is initiated by assigning the same frequency to the two modulating references per phase-leg, while still ensuring that the upper reference is always placed above the lower reference with no crossover intersection. Their amplitudes can be different, but for cases where their total sum exceeds the peak-to-peak vertical band of the triangular carrier, only limited amount of phase-shift can be introduced between them.

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

Fig. 3-4 Switching states obtained in CF mode using two references with a finite phase-shift.

An example illustrating this limit is shown in Fig. 3-4, where the lower modulating reference Ref Y is phase advanced to the extent that its trough touches the carrier negative peak, and its side touches the upper reference Ref X. Of course, Ref X can be shifted upwards until its peak touches the carrier positive peak, to allow for more phase advance to be inserted, but to a reasonable extent, Fig. 3-4 has clearly highlighted the presence of a phase limit, whose value depends on the relative amplitudes of the two references.

Expressing in another way, the above compromise can also be spelled as for a given phase-shift, there is a limit on the maximum amplitude sum that can be divided among the two references. Quite obviously, the biggest amplitude sum occurs at zero phase-shift, like the two references drawn in Fig. 3-3, with its value determined as two times the carrier peak. When this happens, the two references are effectively superimposed on each other with their modulation ratios set to the common value of either unity or 1.15 if proper triplen offsets are added to them [48]. The nine-switch inverter then acts no different from a single three-phase bridge powering two independent loads in parallel. Surely, this is only an equivalence made at the maximum possible point, and does not hold true at all other operating points, where the standard three-phase bridge would have no freedom to supply different voltages to the paralleled loads.

Faced by the above amplitude limitation, it generally is advisable for the nine-switch inverter to operate in CF mode with zero phase-shift, where in EV, it is ensured by adding a compensating angle to one of its modulating references [15]. If unfortunately

Chapter 3 Optimal Pulse-width Modulation of Nine-Switch Inverter

in-phase operation cannot be enforced, the following mathematical analysis would provide some quantitative measures to inform users about the extent of amplitude compromise to expect, when using the nine-switch inverter. Assuming now that the modulating references are expressed as:

$$\begin{cases} V_A(t) = M_1 \sin(\omega_1 t + \varphi_1) + V_{offset1} \\ V_B(t) = M_1 \sin(\omega_1 t + \varphi_1 - 2\pi/3) + V_{offset1} \\ V_C(t) = M_1 \sin(\omega_1 t + \varphi_1 + 2\pi/3) + V_{offset1} \end{cases} \quad (3.1)$$

$$\begin{cases} V_U(t) = M_2 \sin(\omega_2 t + \varphi_2) + V_{offset2} \\ V_V(t) = M_2 \sin(\omega_2 t + \varphi_2 - 2\pi/3) + V_{offset2} \\ V_W(t) = M_2 \sin(\omega_2 t + \varphi_2 + 2\pi/3) + V_{offset2} \end{cases} \quad (3.2)$$

where ω_1 and ω_2 are angular frequencies, φ_1 and φ_2 are relative phases, M_1 and M_2 are normalized amplitudes or modulation ratios, and $V_{offset1}$ and $V_{offset2}$ are appropriate triplen offsets added to gain some performance benefits like improved waveform quality associated with “centered space vector” equivalent modulation [48]. In case of CF mode, $\omega_1 = \omega_2$ and the shift in phase between the reference sets can be written as $\theta = |\varphi_1 - \varphi_2|$, where $0 \leq \theta \leq \pi$. To then find the maximum relative amplitudes that can be set, V_A , V_B and V_C are shifted vertically upwards until they just touch the positive carrier peak, by adding a dc offset of $1-M_1$ to (3.1) with $V_{offset1}$ set to zero for clearer illustration purposes for the time being. Similarly, V_U , V_V and V_W are shifted vertically downwards until they reach the negative carrier peak, by adding M_2-1 to (3.2) with $V_{offset2}$ again set to zero. The modulation constraint of Ref X always higher than Ref Y then requires:

$$M_1 \sin(\omega t + \theta) + 1 - M_1 \geq M_2 \sin \omega t + M_2 - 1 \quad (3.3)$$

If M_1 and θ (or any two out of M_1 , M_2 and θ) are set, the inequality governing M_2 is then determined as:

$$M_2 \leq \frac{2+M_1(\sin(\omega t+\theta)-1)}{1+\sin \omega t} \quad (3.4)$$

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Using (3.4), the maximum of M_2 can be determined by differentiating the right hand expression, and then setting it to zero, so as to determine the specific value of ωt that will give rise to a maximum M_2 value. This maximum must satisfy (3.4) at all time, even while ωt varies between $-\pi$ and π in a fundamental period. Instead of $M_1 \neq M_2$, the subset case of $M_1 = M_2 = M$ can next be considered for verifying an earlier finding, which upon proven, will provide confidence to the mathematical derivation presented here. Upon substituting M for M_1 and M_2 in (3.4) and rearranging, the simplified inequality is then written as:

$$M \leq \frac{2}{2 - 2\sin\frac{\theta}{2}\cos\frac{2\omega t + \theta}{2}} \quad (3.5)$$

where the cosine term in the denominator varies between -1 (when $\omega t = -\pi - \theta/2$ and $\pi - \theta/2$) and 1 (when $\omega t = -\theta/2$) as ωt changes from $-\pi$ to π . Writing its right hand term as M_{RH} and substituting in the limits of the cosine term then cause (3.5) to become $M \leq 1/(1 + \sin(\theta/2)) \leq M_{RH} \leq 1/(1 - \sin(\theta/2))$, which can simply be written as $M \leq 1/(1 + \sin(\theta/2))$. Noting that $0 \leq \theta \leq \pi$ and hence $0 \leq \sin(\theta/2) \leq 1$, maximum M would occur when $\sin(\theta/2) = 0$, during which the denominator is the smallest. The maximum value of M is then determined as unity, and the corresponding value of θ is zero, representing the in-phase case. This finding no doubt agrees with the earlier judgment that the maximum modulation ratios that can be set for both modulating references without triplen offsets added are one for in-phase CF mode of operation. On the other extreme, if θ is fixed to 180° out of phase, then the maximum of M would be lowered to 0.5 , which again is correct with the trough of the upper reference now just touching the peak of the lower reference. In other words, the total amplitude sum of the two references is now either lesser than or equal to unity, which indeed is also the constraint faced when operating in the DF mode, as explained in the next subsection.

The same analysis can be repeated for the case with triplen offsets added to the two sets of modulating references, so as to gain an improvement in overall waveform quality and an increase in modulation ratios to 1.15 [47][48], like commonly associated with the “centered space vector” equivalent modulation. The modified

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Fig. 3-5 Modified references with centered SVM triplen offsets added for controlling the nine- switch converter under continuous CF mode of operation.

references obtained can be drawn like in Fig. 3-5 for illustration purposes, and their corresponding limiting equations can be derived as:

$$M_2 \leq \frac{2+M_1(\sin(\omega t+\theta)-\frac{\sqrt{3}}{2}+V'_{offset1})}{\frac{\sqrt{3}}{2}+\sin(\omega t)+V'_{offset2}} \quad \text{for } M_1 \neq M_2 \quad (3.6)$$

$$M \leq \frac{2}{\sqrt{3}-2\sin\frac{\theta}{2}\cos\frac{2\omega t+\theta}{2}+V'_{offset2}-V'_{offset1}} \quad \text{for } M_1 = M_2 = M \quad (3.7)$$

where $V'_{offset1}=V_{offset1}/M_1$, $V'_{offset2}=V_{offset2}/M_2$, $V_{offset1}=-0.5(\max(V_A, V_B, V_C)+\min(V_A, V_B, V_C))$ and $V_{offset2}=-0.5(\max(V_U, V_V, V_W)+\min(V_U, V_V, V_W))$ for “centered space vector” equivalent modulation (centered SVM in short). Note from (3.7) that for the subset case of $\theta=0$, $V'_{offset1}$ and $V'_{offset2}$ would be equal, and by replacing the cosine term with -1, as explained earlier, the maximum value of M would then be determined as 1.15, which again agrees well with the judgment made earlier.

Although the equations above clearly spell the modulating limits, in many instances, the actual operating conditions are some distance away from these limits, inferring that those equations merely served as guidelines for the users to determine that over-modulation with its accompanied distortion will not occur. If the actual modulation ratios set for a particular phase-shift are indeed smaller than the maximum, like those examples shown in Fig. 3-3 and Fig. 3-4, the modulation approach recommended here is to appropriately manage the references until the amount of performance degradation experienced by the connected sources or loads is the smallest. This is deemed as necessary, since any sizable degradation will further worsen the tradeoffs, making the saving of three switches less and less attractive.

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For the method recommended here, the dominant reference is first determined, where in Fig. 3-3 and Fig. 3-4, it is Ref X since $M_1 > M_2$. The dominant reference Ref X is then kept unchanged, meaning that no dc offset is added to it for vertical shifting. Ref X is therefore still symmetrically placed along the horizontal time axis within the vertical carrier band. By further introducing an appropriate triplen offset $V_{offset1}$ to it, the loads or sources connected to the upper three phases A, B and C will experience the same optimal waveform quality as per centered space vector modulation. For Ref Y, the same centering effect cannot be introduced even if an appropriate triplen offset $V_{offset2}$ is added to it. The reason is attributed to the need to always keep Ref Y below Ref X, which then means that a dc offset must always be added to the former to shift it vertically downwards until it just touches Ref X at only one point per fundamental cycle, as again reflected in Fig. 3-3 and Fig. 3-4.

Because of that downward shifting, Ref Y is no longer vertically centered within the carrier band, inferring that loads or sources connected to the lower three phases U, V and W will now experience a slight degradation in switching quality. In contrast, performing shifting in this way has an advantage when $\theta=0$ in the sense that the overall active duration “sees” by the converter dc-link is still centrally placed, in fact determined solely by the dominant Ref X. The overall slight degradation introduced to the converter is therefore solely shouldered by the lower loads or sources, which unfortunately cannot be avoided. The same procedure can equally be reversed for the other case of $M_1 < M_2$, where now only Ref X needs to be shifted upwards by adding a dc offset to it, while Ref Y remains centrally placed within the vertical carrier band. In this second case, only the upper loads or sources are burdened by the slight quality degradation, which again cannot be avoided, but is certainly minimized by the proposed approach.

If the above recommended approach of centralizing the dominant reference in the vertical band is adopted, limitation imposed on the amplitude of the non-dominant reference can be calculated using the inequality in (3.8), where $M_1 (\geq M_2)$ is assumed to be the amplitude of the dominant reference. A note raised with regard to (3.8) is that it should only be used for the centralizing method, where it is earlier emphasized that the

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approach is only valid for cases where the actual modulation ratios set for a particular phase-shift are smaller than those maximum values calculated using (3.6) or (3.7).

$$M_2 \leq \frac{1+M_1(\sin(\omega t+\theta)+V'_{offset1})}{\frac{\sqrt{3}}{2}+\sin(\omega t)+V'_{offset2}} \quad (3.8)$$

Fig. 3-6 Complete three-phase sequence obtained in CF mode.

So far, the modulation scheme has been discussed with references shown only for one phase-leg. For completeness and to better view the overall three-phase modulation process, the full switching sequence produced per carrier period is included in Fig. 3-6 for illustration purposes. As seen, the three reference sets of {A, U}, {B, V} and {C, W} are all drawn with Ref X above Ref Y, which would then give rise to the sequence shown at the bottom with two full null states $\{-1, -1, -1\}$ and $\{1, 1, 1\}$ placed at the start and end of the considered half carrier cycle.

Fig. 3-7 Complete three-phase sequence obtained in DF mode.

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In the full null states, both sets of three-phase terminals are in their respective nulls, unlike in states $\{0, -1, -1\}$ and $\{1, 1, 0\}$, where only one terminal set is tied to null, while the other has already entered its active state. These two latter states are therefore referred to as partial active states, since current is still flowing from the dc-link capacitor to at least one of the external loads or sources. For the remaining three states of $\{1, -1, -1\}$, $\{1, 0, -1\}$ and $\{1, 1, -1\}$, they are no doubt full active states, since both terminal sets are tied to their respective individual active states. To summarize, a sequence produced in the CF mode with reference amplitudes of $M_1 + M_2 > 1$ would have a majority of full active states, unlike the DF mode discussed next.

3.3.2 DF Mode

DF mode corresponds to the setting of different frequencies for the two terminal sets to which either loads or sources are connected. It is at times needed for driving two motors at different speed in EV during turning regime or aircraft supply where the input land frequency and output onboard frequency are different. To initiate this mode, the two sets of modulating references listed in (3.1) and (3.2) are again used, but with their angular frequencies set to $\omega_1 \neq \omega_2$. It is also clear that their amplitudes must satisfy $M_1 + M_2 \leq 1$ or 1.15 if proper triplen offsets are added, in order to avoid crossover of references, which indeed is the same constraint experienced in the CF mode when $\theta = 180^\circ$. Detailed reference-carrier placement and switching sequence generated under this constraint is shown in Fig. 3-7, where the first obvious feature noted is the placement of lower references U, V and W below the upper ones, notated as A, B and C.

In total, three full null states, notated as $\{-1, -1, -1\}$, $\{0, 0, 0\}$ and $\{1, 1, 1\}$, are produced per half carrier cycle, within which both terminal sets are tied to their respective nulls. The remaining four states are partial active states, where only one set of terminals is active, while the other set is in null. For $\{0, -1, -1\}$ and $\{0, 0, -1\}$, the upper terminals are active, while the lower terminals are in null. The reverse happens in the other two partial active states $\{1, 0, 0\}$ and $\{1, 0, 1\}$, which when summarized with the other states, would lead to the conclusion that only full null and partial active

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states are involved in DF mode of operation. Full active states are not involved here, even though they have a dominant influence in CF mode.

Also unlike CF mode, none of the references in DF mode can be centered within the vertical carrier band, which is clearly reflected in Fig. 3-7, where references A, B and C are shifted vertically upwards, while references U, V and W are shifted vertically downwards. Since none of the modulating references can now be centered, it makes no sense to continue aiming for optimal waveform quality. Instead, it is recommended in the next section that a better objective set for the DF mode is to reduce the converter switching losses by using an appropriate discontinuous modulation scheme. This makes logical sense since the references are already shifted upwards or downwards by some amount, and it surely is not difficult to shift them slightly more upwards or downwards to gain some loss minimization advantages through proper dc-rail clamping.

3.4 Discontinuous Modulation

Observing Fig. 3-3 and Fig. 3-4, the upper and lower switches (SX and SY) of the nine-switch inverter are noted to commute once each per half carrier period, while its middle switch SXY is noted to commute twice. The total commutation count is therefore still four per phase-leg, like in the back-to-back converter. Note that the number of four does not include additional commutations that can occur between the switch and its anti-parallel diode during terminal current reversal, which in principle is load-dependent, and therefore not definite enough for quantifying as a single number. In spite of whether the current reversal commutations are taken into consideration or not, the commutation count can likely only be reduced by applying discontinuous modulation theories [48]-[54].

While applying discontinuous modulation theories, double checking should be performed, since not all discontinuous methods are directly applicable to the nine-switch inverter, as demonstrated shortly. But before doing so, it is commented here that although the nine-switch inverter uses three lesser semiconductor switches, it does not necessarily translate to lower switching losses. For the nine-switch inverter, what

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Fig. 3-8 Modified references per phase-leg for (a) 60° and (b) 30°-discontinuous modulation when in CF mode with $M_1=1 \times 1.15$ and $M_2=0.8 \times 1.15$.

Fig. 3-9 Modified references per phase-leg for 120°-discontinuous modulation of nine-switch inverter when in (a) CF and (b) DF modes.

really happened is that the switching losses remain unchanged, but simply distributed among a smaller pool of switches with the middle switches SXY taking the major share. Of course, these losses can be reduced by adopting discontinuous modulation schemes, which is the main topic of discussion for the following subsections.

3.4.1 CF Mode

As an initial attempt, popular 30° and 60°-discontinuous methods for standard three-phase VSI control are evaluated to check for their suitability for nine-switch inverter control. To do that, relevant offset equations found in [48] are first applied to the two

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modulating references per phase-leg with their amplitudes set to $M_1=1.15$ and $M_2=0.92$ (only an example) for illustrating CF mode of operation. The resulting modified waveforms are then shown in Fig. 3-8 with the upper two for 60°-discontinuous and the lower two for 30°-discontinuous. These waveforms unquestionably show that 30° and 60°-discontinuous schemes can occasionally cause Ref X to fall below Ref Y, which unfortunately is not allowed by the nine-switch inverter. Therefore, 30° and 60°-discontinuous schemes are both not suitable for the nine-switch inverter, even though they are popular methods for the traditional VSI. The reason for failing for the two schemes is attributed to their alternate positive and negative dc rail clamping, which can cause the references to shift in directions opposite to those demanded. More precisely, they cause Ref X to wrongly shift downwards in the negative half fundamental cycle, and Ref Y to wrongly shift upwards in the positive half cycle.

To guarantee that Ref X is only shifted upwards throughout the full fundamental cycle, only the 120°-discontinuous scheme that causes positive clamping for a third of the fundamental cycle per phase is applicable. The same 120°-discontinuous scheme can also be applied to Ref Y, but it should now be negative, and not positive, clamping. The offset equations needed for both cases are summarized in (3.9) with their resulting modified references per phase-leg shown in Fig. 3-9(a). Clearly, the constraint of $\text{Ref X} \geq \text{Ref Y}$ is not breached by the proposed modulation scheme, even while it realizes positive clamping for Ref X and negative clamping for Ref Y for a third of the fundamental period. The eventual outcome would then be a saving of two commutation counts per half carrier cycle per phase-leg, as compared to those continuous modulation snapshots shown in Fig. 3-3 and Fig. 3-4. Among the two commutations saved, one comes from SXY, while the other comes from either SX or SY. The same would happen in all phase-legs, and at any instance, there would only be one upper phase (A, B or C) and one lower phase (U, V or W) clamped. Because of that, the net saving in commutation can be summarized as 50% per phase-leg or 33% when the full three-phase converter is considered.

$$\begin{cases} V_{offset1} = 1 - \max(V_A, V_B, V_C) \\ V_{offset2} = -1 - \min(V_u, V_v, V_w) \end{cases} \quad (3.9)$$

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Another comment raised here is that with the 120°-discontinuous modulation implemented, the advantage gained is solely a reduction in commutation count, and not a removal of amplitude and phase limits between the two modulating references per phase-leg. The same limiting equations from (3.4) to (3.7) are therefore still applicable here, except with $V_{offset1}$ and $V_{offset2}$ substituted by the two expressions listed in (3.9), rather than those for continuous “centered space vector” modulation. Performing the relevant substitution then results in the following inequality for governing the 120°-discontinuous modulation scheme:

$$M_2 \leq \frac{2+M_1(\sin(\omega t+\theta)-V'_{offset-d1})}{\sin(\omega t)+V'_{offset-d2}} \quad (3.10)$$

where $V'_{offset-d1}=\max(V_A, V_B, V_C)/M_1$ and $V'_{offset-d2}=\min(V_U, V_V, V_W)/M_2$.

Fig. 3-10 Variations between maximum M_1 and M_2 values when θ is set to 30° for continuous scheme (a) without and (b) with centered SVM offset, (c) continuous centralizing scheme, (d) discontinuous scheme, hybrid scheme (e) without and (f) with centered SVM offset.

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3.4.2 DF Mode

While discussing the DF sequence shown in Fig. 3-7, the general observation noted is that both modulating references cannot be centered within the vertical carrier band, inferring that all loads and sources connected to the nine-switch inverter are expected to experience a drop in switching quality. Because of that, the objective set for DF mode should not be an improvement in waveform quality, but should rather be a reduction in switching losses, achieved through 120°-discontinuous modulation. For illustrating discontinuous modulation in DF mode, Fig. 3-9(b) shows the modified references at different frequencies, obtained through applying the same offset equations listed in (3.9). The sum of reference amplitudes in this case is still lesser than or equal to 1.15, inferring that no major changes are introduced to the nine-switch inverter, except for a significant reduction in switching losses.

3.5 Hybrid Modulation Schemes and Other Comparative Issues

Fig. 3-11 Variations of maximum M_2 value as θ changes along the horizontal axis with M_1 fixed at 0.75 for continuous scheme (a) without and (b) with centered SVM offset, (c) continuous centralizing scheme, (d) discontinuous scheme, hybrid scheme (e) without and (f) with centered SVM offset.

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Instead of choosing only continuous or discontinuous modulation for its two terminal sets, a mix of both is possible with the resulting schemes referred to as hybrid modulation. In total, two combinations are possible with the first being the upper terminals controlled by continuous modulation with or without centered SVM triplen offset, and the lower terminals controlled by 120°-discontinuous modulation with negative dc-rail clamping. The second is of course the reverse with the upper terminals now controlled by 120°-discontinuous modulation with positive dc-rail clamping, and the lower terminals controlled by continuous modulation with or without triplen offset added. Both schemes are applicable to the CF and DF modes with their maximum modulation ratios governed by the following two limiting expressions, derived for comparison with (3.4), (3.6), (3.8) and (3.10).

$$M_2 \leq \frac{2+M_1(\sin(\omega t+\theta)-1)}{\sin(\omega t)-V'_{offset-dz}} \quad (\text{without triplen offset}) \quad (3.11)$$

$$M_2 \leq \frac{2+M_1(\sin(\omega t+\theta)-V'_{offset1}-\frac{\sqrt{3}}{2})}{\sin(\omega t)-V'_{offset-dz}} \quad (\text{with triplen offset}) \quad (3.12)$$

For a clearer visual comparison of all schemes described in the chapter, Fig. 3-10 plots the six governing equations (3.4), (3.6), (3.8), (3.10), (3.11) and (3.12) for the specific example case of $\theta=\pi/6=30^\circ$ (for (3.11) and (3.12), it is assumed that the upper terminals are controlled by continuous modulation, while the lower terminals are controlled by discontinuous modulation). From the plots, an observation noted is that the hybrid modulation technique without centered SVM triplen offset added and governed by (3.11) provides a slightly larger amplitude sum, as modulation index M_1 approaches unity. This conclusion is however not always true since it depends on the specific phase shift θ .

To illustrate the influence imposed by θ , Fig. 3-11 re-plots the six governing equations, showing now the variations of maximum M_2 as θ increases from 0 to π with M_1 fixed at 0.75 for example. This figure clearly shows that for $\theta \geq \pi/2$, modulation schemes governed by (3.6), (3.10) and (3.12) have an amplitude sum that is slightly larger than

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Table 3-1 The values of various discussed modulation schemes
(computed up to the 500th harmonic with the switching frequency at 10kHz)

	Original method documented in [20][46] and governed by (3.4)				Proposed continuous centralizing method governed by (3.8)				Proposed discontinuous method governed by (3.10)			
	In phase		30°phase-shift		In phase		30°phase-shift		In phase		30°phase-shift	
	Upper terminal	Lower terminal	Upper terminal	Lower terminal	Upper terminal	Lower terminal	Upper terminal	Lower terminal	Upper terminal	Lower terminal	Upper terminal	Lower terminal
$M_1=1$ $M_2=0.65$	52.47	90.78	N.A.	N.A.	52.47	90.78	N.A.	N.A.	56.18	93.90	N.A.	N.A.
$M_1=0.65$ $M_2=0.65$	90.78	90.78	90.78	90.78	86.22	86.22	86.22	90.37	94.71	93.90	94.71	93.90
$M_1=0.65$ $M_2=0.55$	90.78	98.87	90.78	98.87	86.22	97.80	86.22	93.40	94.71	106.29	94.71	106.29
$M_1=0.8$ $M_2=0.4$	75.33	121.38	75.33	121.38	67.76	96.75	67.76	103.87	79.51	133.44	79.51	133.44

that of (3.11), which in effect is the reverse of that observed earlier with θ set to $\pi/6$ ($< \pi/2$).

Other than the amplitude sum variations, another feature that needs verification is the

Fig. 3-12 Line voltage harmonic spectrums produced by nine-switch inverter with $M_1=0.8$, $M_2=0.4$ and $\theta=0$. (a) upper and (b) lower terminal spectrums produced by scheme documented in [20][46], (c) upper and (d) lower terminal spectrums produced by centralizing scheme; (e) upper and (f) lower terminal spectrums produced by discontinuous scheme.

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improved waveform quality produced by the continuous centralizing scheme, recommended in Section 3.3 for use when the amplitude sum is lower than its maximum calculated using (3.4) or (3.6). To preliminary verify that improvement, Table 3-1 lists down the total harmonic distortion (THD) values computed for both terminal sets for the existing modulation scheme documented in [20][46] and governed by (3.4), proposed centralizing scheme governed by (3.8) and discontinuous scheme governed by (3.10). Quite expectedly, the discontinuous scheme produces the worst THD values under all the tested conditions, while the proposed continuous centralizing scheme always produces the lowest THD values.

To further strengthen the comparative finding, Fig. 3-12 shows the plotted harmonic spectrums for the same three studied modulation schemes with their upper and lower modulation ratios set to $M_1=0.8$ and $M_2=0.4$ respectively and θ set to zero. The illustrated plots clearly show that the discontinuous scheme produces higher harmonic strength at the first carrier multiple and its surrounding sideband, which are generally harder to filter than those at higher carrier multiples. In contrast, the continuous centralizing scheme always produces lower harmonic strength at the first carrier multiple and its associated sideband, and is therefore proved to have a better waveform quality.

3.6 Simulation and Experimental Results

The proper functioning of continuous modulation has already been verified in [20][46] for the nine-switch inverter, and will therefore not be duplicated here since the recommendation proposed in subsection 3.3.1 is simply to add a dc offset only to the less prominent reference with its companion left unchanged. Instead, the purposes of including results here are to verify the practicality of those discontinuous findings discussed in Section 3.4 for both CF and DF modes. To achieve that, a nine-switch inverter was preliminary simulated in Matlab / Simulink with PLECS libraries coupled. The converter was configured to operate like a dual output dc-ac inverter with its dc source set to 200 V. The powered inverter, switching at 10 kHz, was then connected to two RL loads with $R = 30 \Omega$ and $L = 5 \text{ mH}$.

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Fig. 3-13 Simulated waveforms under in-phase CF mode.

Fig. 3-14 Simulated waveforms under CF mode with $\theta = 30^\circ$.

Fig. 3-15 Simulated waveforms under DF mode.

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Fig. 3-16 Experimental waveforms under in-phase CF mode.

Fig. 3-17 Experimental waveforms under CF mode with $\theta = 30^\circ$.

Fig. 3-18 Experimental waveforms under DF mode.

Fig. 3-19 Experimental waveforms under in-phase CF mode. Top to bottom – upper line voltage, 200V/div; lower line voltage, 200V/div; upper line current, 5A/div; lower line current, 5A/div.

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Fig. 3-20 Experimental waveforms under CF mode with $\theta = 30^\circ$. Top to bottom – upper line voltage, 200V/div; lower line voltage, 200V/div; upper line current, 5A/div; lower line current, 5A/div.

Fig. 3-21 Experimental waveforms under DF mode. Top to bottom – upper line voltage, 200V/div; lower line voltage, 200V/div; upper line current, 5A/div; lower line current, 5A/div.

With the modulation ratios set to $M_1 = 1 \times 1.15$ and $M_2 = 0.7 \times 1.15$ for the upper and lower references respectively, Fig. 3-13 shows the corresponding 50 Hz waveforms obtained for the in-phase CF mode. In the figure, positive 120° -clamping of the upper terminals and negative 120° -clamping of the lower terminals of the phase voltages (measured with reference to the negative terminal of the dc-link for all simulated and experimental plots presented in the chapter) are clearly observed from the upper two traces. On the other hand, the lower two traces show two sets of three-phase sinusoidal output currents, whose amplitude ratio matches that obtained by dividing M_2 from M_1 .

Next, with the modulation ratios set to $M_1 = M_2 = 0.68 \times 1.15$ and phase-shift set to $\theta = 30^\circ$, Fig. 3-14 shows the corresponding simulated waveforms obtained when in the CF mode, but now with a finite phase-shift. The results again show that the phases are properly clamped with no low order distortion observed since the limit in (3.7) is not yet exceeded. Also observed in the third and fourth traces are two balanced sets of

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three-phase currents, having the same amplitude and a phase-shift of 30° between them. This is expected since the modulation ratios are set equal and a phase-shift of 30° is intentionally introduced. Moving fore to verify the performance in DF mode, Fig. 3-15 shows the simulated waveforms obtained with $M_1 = M_2 = 0.5 \times 1.15$, $\omega_1 = 100\pi$ and $\omega_2 = 60\pi$. The same proper phase clamping and current amplitude ratio are again produced with no low order distortion observed, since the bounding limits have not yet been exceeded.

Upon proven in simulation, an experimental nine-switch inverter was subsequently built in the laboratory using the same system and control parameters, as earlier used for the simulation studies. For improved flexibility, the implemented inverter was controlled by a digital signal processor (DSP), whose on2-chip modulator was programmed to output some preliminary gating signals. These signals were suitable for driving a back-to-back converter with two standard VSI bridges, but not the nine-switch inverter. To convert them to appropriate gating signals, XOR gates were added for processing them, before channeling them to the nine-switch inverter through proper gate drivers.

Using the assembled prototype and with the earlier simulated test conditions repeated, Fig. 3-16 to Fig. 3-18 show the matching experimental waveforms, which are found to agree well with those simulated from Fig. 3-13 to Fig. 3-15. Because of the close similarities observed, the same concluding remarks spelled earlier are equally applicable here for the experimental plots, and are therefore not duplicated for conciseness. To further show that the converter is switching properly, corresponding line voltage waveforms are plotted from Fig. 3-19 to Fig. 3-21, where neat three-level switching is clearly observed for the upper two traces. The lower two traces represent the line currents, which are no different from those plotted in Fig. 3-16 to Fig. 3-18, and are therefore not further discussed here.

3.7 Summary

This chapter evaluates physical constraints experienced by the nine-switch inverter, before proposing modulation schemes for optimizing its performance. In particular, for

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the CF mode, it is recommended that dc offset should only be added to the smaller reference per phase-leg with the other prominent reference left centered within the vertical carrier band. Doing so would subject only one set of loads or sources to slight performance degradation with the other set and dc-link still experiencing waveform quality equivalent to centered space vector modulation. This centering principle is however not achievable in the DF mode, inferring that the DF objective should be set to lower the switching losses, rather than to optimize the overall waveform quality. To achieve this revised DF objective, an appropriate 120°-discontinuous modulation scheme is proposed, after concluding that popular 30° and 60°-discontinuous schemes are not feasible choices for the nine-switch inverter. The proposed 120°-discontinuous scheme is equally applicable to the CF mode, as verified in simulation and experimentally for both the CF and DF modes.

Chapter 4 An Integrated Nine-Switch Power Conditioner

An integrated power conditioner with reduced semiconductors for power quality enhancement and voltage sag mitigation is discussed in this chapter. Relevant control schemes are presented, which when implemented, demonstrate that the nine-switch converter can maintain nearly the same performance standard even with lesser semiconductors used. This conclusion is however limited to series-shunt applications, and not shunt-shunt systems. It is hence a useful guide spelling out the pros and cons of applying the nine-switch topology.

4.1 Introduction

As introduced in chapter 2, the nine-switch inverter was first recommended for dual motor drives, rectifier-inverter systems [18][19]. Despite functioning as intended, these existing applications are burdened by the limited phase shift and strict amplitude sharing enforced between the two terminal sets of the nine-switch inverter.

More importantly, a much larger dc-link capacitance and voltage need to be maintained, in order to produce the same ac voltage amplitudes as for the back-to-back converter. Needless to say, the larger dc-link voltage would overstress the semiconductor switches unnecessarily, and might to some extent overshadow the saving of three semiconductor switches made possible by the nine-switch topology. The attractiveness of the nine-switch inverter, if indeed any, is therefore not yet fully brought out by those existing applications. Although follow-up topological extensions can subsequently be found in [55], where a Z-source network and alternative modulation schemes are introduced, they did not fully address those critical limitations faced by the nine-switch inverter, and not its traditional back-to-back counterpart.

Investigating further by taking a closer view at those existing applications, a general note observed is that they commonly use the nine-switch inverter to replace two shunt converters connected back-to-back. Such replacement will limit the full functionalities

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Fig. 4-1 Representations of (a) back-to-back and (b) nine-switch power conditioners.

of the nine-switch inverter. In this chapter, an alternative concept is discussed, where the nine-switch inverter is chosen to replace a shunt and a series converter found in an integrated power conditioner, instead of two shunt converters. Underlying operating principles are discussed comprehensively to demonstrate how such “series-shunt” replacement can bring forth the full advantages of the nine-switch inverter, while yet avoiding those limitations faced by existing applications. Details explaining smooth transitions between normal and sag operating modes are also provided to clarify that the more restricted nine-switch inverter will not underperform the more independent back-to-back converter even for sag mitigation.

Later, the chapter proceeds to compare the ratings and losses of the back-to-back and nine-switch conditioners. Also presented afterwards is two sets of higher level control schemes with the first used for controlling one set of three-phase outputs so as to compensate for harmonic currents, reactive power flow and three-phase unbalance caused by nonlinear loads. The grid currents drawn from the utility are then sinusoidal, having only fundamental component. In synchronism, the second set of outputs is controlled to compensate for any detected grid voltage harmonics and unbalance, so that only a set of balanced three-phase voltages appears across the loads under normal operating conditions [56]. During voltage sags, the second set of control schemes also has the ability to continuously keep the load voltages within tolerable range. This sag

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mitigation ability, together with other conceptual findings discussed in the chapter but not in the open literature, has already been verified in experiment with favorable results observed. The proposed nine-switch conditioner is operated with the discontinuous modulation scheme developed in Chapter 3 for reducing the commutation count, and hence its switching losses.

4.2 System Description and Operating Principles of Nine-Switch Conditioner

4.2.1 Conventional Back-to-Back Limitations and Recommendations

Fig. 4-1(a) shows the per-phase representation of the common back-to-back unified power quality conditioner (UPQC), where a shunt converter is connected in parallel at the point-of-common-coupling (PCC) and a series converter is connected in series with the distribution feeder through an isolation transformer. The shunt converter is usually controlled to compensate for load harmonics, reactive power flow and unbalance, so that a sinusoidal fundamental current is always drawn from the utility grid, regardless of the extent of load nonlinearity. Complementing, the series converter is controlled to block grid harmonics, so that a set of three-phase fundamental voltages always appears across the load terminals [57]. Rather than the described, the inverse assignment of functionalities with the shunt converter regulating voltage and series converter regulating current is also possible, as demonstrated in [58]. Being so flexible, the UPQC is indeed an excellent “isolator”, capable of promptly blocking disturbances from propagating throughout the system.

Despite its popularity, the back-to-back UPQC is nonetheless still complex and quite underutilized, even though it offers independent control of two decoupled converters. Its underutilization is mainly attributed to the series converter, whose output voltages are usually small, since only small amount of grid harmonics need to be compensated by it under normal steady-state conditions, especially for strong grids ($\vec{V}_{SUPPLY} \approx \vec{V}_{LOAD}$). Some typical numbers for illustration can be found in [56], where it is stated that the converter modulation ratio can be as low as 0.05×1.15 with triplen offset included, if the converter is sized to inject a series voltage of 1.15 p.u. during sag

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occurrence. Such low modulation ratio gives rise to computational problems, which fortunately have already been addressed in [57], but not its topological underutilization aspect.

Resolving the topological aspect is however not so easy, especially for cases where the dc-link voltage must be shared and no new component can be added. Tradeoffs would certainly surface, meaning that the more reachable goal is to aim for an appreciable reduction in component count, while yet not compromising the overall utilization level by too much. Offering one possible solution then, this chapter presents an integrated power conditioner, implemented using the nine-switch inverter, rather than the traditional back-to-back converter. Before the nine-switch inverter can be inserted though, its impact should be thoroughly investigated to verify that there would not be any overburdening of system implementation cost and performance. This recommendation is advised as important, since earlier usages of the nine-switch inverter for motor drives and rectifier-inverter systems have so far resulted in some serious limitations, which would be brought up for discussion shortly to highlight certain insightful concepts.

4.2.2 Proposed Nine-Switch Conditioner

The operating principles of the nine-switch inverter are explained clearly in chapter 3. From its existing applications, the general impression formed is that the nine-switch inverter is not too attractive, since its semiconductor saving advantage is easily shadowed by tradeoffs, especially for cases of different terminal frequencies. Such unattractiveness is however not universal, but noted here to link only with those existing applications reported to date, where the nine-switch inverter is used to replace two shunt-connected converters. References demanded by these shunt converters are usually both sizable, inferring that the carrier band must be shared equally between them, and hence giving rise to those tradeoffs identified earlier. Therefore, instead of “shunt-shunt” replacement, it is recommended here that the nine-switch inverter should more appropriately be used for replacing a series and a shunt converter like those found in a power quality conditioner or any other “series-shunt” topological applications. Explanation for justifying that recommendation is provided in the following contents with all relevant advantages and residual tradeoffs identified.

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Fig. 4-2 Transitions of modulating references and control schemes between normal (left) and sag mitigation (right) modes.

Under normal operating conditions, the output voltage amplitude of the shunt converter is comparatively much larger than the voltage drop introduced by the series converter along the distribution feeder. That indirectly means the modulating reference needed by the shunt converter is much larger than that associated with the series converter, which might simply consist of only the inverse harmonic components for grid voltage compensating purposes. Drawing these details in the carrier range would then result in a much wider vertical range h_1 in the left diagram of Fig. 4-2 for controlling the upper shunt terminal, and a narrower h_2 for controlling the lower series terminal ($h_1 \gg h_2$). Other operating details like logical equations used for generating gating signals for the three switches per phase would remain unchanged, as per (2.5).

For h_2 , a comment raised here is that it can be set to zero, if an ideal grid with no distortion and rated sinusoidal voltage is considered. In that case, the lowest three switches, labeled as S_3 for each phase in Fig. 4-1(b), should always be kept ON to short out the series coupling transformer, and to avoid unnecessary switching losses. If desired, the series transformer can also be bypassed at the grid side to remove unwanted leakage voltage drop without affecting the compensating ability of the shunt converter. Tailored operation with an ideal grid is therefore possible, as described, but for modern grids with abundant distributed nonlinear loads, voltage distortion is relatively common, since any amount of harmonic load current flowing through a finite

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line or transformer impedance would have caused voltage at the PCC to be distorted. Series harmonic compensation of the grid or PCC voltage is therefore technically needed, and hence included here for discussion, if a smoother load voltage is demanded.

Referring back to the h_1 and h_2 carrier band division shown in the left illustration of Fig. 4-2, it would still need a higher dc-link voltage as a tradeoff in the UPQC, but the increase is much reduced, and definitely not anywhere close to doubling. Quoting [56] as an example, where modulation ratio of the series converter can be as low as 0.05×1.15 with triplen offset included, the increase in dc-link voltage is merely about 5%, before the same maximum shunt voltage amplitude, like in a back-to-back converter, can be produced by the nine-switch inverter. This maximum is however arrived at a reduced maximum modulation ratio of 0.95×1.15 , instead of 1.15 with triplen offset considered. The scenario would somehow be improved slightly, if an ideal grid is considered instead, in which case, h_2 is set to zero, as explained in an earlier paragraph. No increase in dc-link voltage is then needed, and the maximum shunt voltage amplitude can be produced at a modulation ratio of 1.15. Replacing of “series-shunt” converter by the nine-switch inverter is therefore an acceptable option with its saving of three semiconductor switches viewed here as more profound, since they represent heavily underutilized switches found in the back-to-back converter for series compensation purposes.

Yet another issue to address, before the nine-switch inverter can be confirmed as a favorable topology for “series-shunt” power conditioner, is to study its compensating ability under voltage sag condition. For that purpose, the PCC voltage in Fig. 4-1(b) is assumed to dip by some amount, which would then subject the higher shunt terminal of the nine-switch inverter to a reduced voltage level. In contrast, the lower series terminal must respond immediately by injecting a sizable series voltage at the fundamental frequency ($\vec{V}_{SERIES} = \vec{V}_{LOAD}^* - \vec{V}_{SUPPLY}$, where $\vec{V}_{LOAD}^*$ is the demanded load voltage reference), so as to keep the load voltage close to its pre-fault value.

Updating this sag operating scenario to the carrier domain then results in the shunt terminal using a reduced reference, and the series terminal widening its reference range

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to include a sizable fundamental component, regardless of whether h_2 is initially zero for an ideal grid or taking a small value for a distorted grid. Since both references are now predominantly fundamental with sizable amplitudes, their placement can ended up like the example drawn on the right of Fig. 4-2 with the same earlier mentioned phase-shift limitation imposed. Fortunately, this limitation will not hinder the operation of the nine-switch conditioner, since large injected series voltage with a demanding phase-shift is usually accompanied by a severe sag at the PCC, and hence a much reduced shunt modulating reference. The compressed shunt reference would then free up more carrier space below it for the series reference to vary within, as easily perceived from the example drawn on the right of Fig. 4-2.

In conclusion, the proposed nine-switch power conditioner can indeed operate well under both normal and sag operating conditions, owing to its auto-complementary tuning of shunt and series references within the single common carrier band. Suitability of the nine-switch inverter for “series-shunt” replacement is therefore established without any stringent practical limitations encountered, unlike those existing “shunt-shunt” replacements.

4.3 Per Unit Comparative Details

Last section provides a qualitative justification for using the nine-switch inverter as a UPQC or other series-shunt conditioners. This justification is now reinforced here by some numerical values calculated for determining the semiconductor losses and component ratings of the back-to-back and nine-switch power conditioners. For the latter, it is further divided into three subcategories without modifying the context of series-shunt power conditioning. The following now describes each of the four cases in details, before summarizing their features in Table 4-1.

4.3.1 Back-to-Back UPQC

Back-to-back UPQC allows independent control of its shunt and series converters, and hence does not need to divide its carrier band into two, like in Fig. 4-2. That means h_2 is zero, and its dc-link voltage can be set to the minimum of $V_{dc-BB} = 2\sqrt{2}/1.15$ p.u.

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Table 4-1 U.P. component rating and losses normalized to nominal grid voltage and load current

UPQC type	Capacitor voltage rating	Semiconductor voltage rating *** With Series Compensation ***	Semiconductor current rating	Total semiconductor losses (conduction & switching)
Back-to-back UPQC	$2\sqrt{2}/1.15$	$2\sqrt{2}/1.15$	$1+k$	4.62% Normal; 5.40% Sag ¹
Proposed nine-switch UPQC	$1.05 \times 2\sqrt{2}/1.15$	$1.05 \times 2\sqrt{2}/1.15$	$1+k$	3.24% Normal; 5.19% Sag ¹
Nine-switch UPQC with equally divided carrier	$2 \times 2\sqrt{2}/1.15$	$2 \times 2\sqrt{2}/1.15$	$1+k$	9.26% Normal; 11.27% Sag ¹
*** Without Series Compensation ***				
Back-to-back UPQC	$2\sqrt{2}/1.15$	$2\sqrt{2}/1.15$	$1+k$	0.62% Normal; 5.40% Sag ¹
Nine-switch UPQC with CF control	$2\sqrt{2}/1.15$	$2\sqrt{2}/1.15$	$1+k$	0.71% Normal; 4.94% Sag ¹

¹ Evaluated with a 40% in-phase sag

(subscript BB stands for “back-to-back”), if the nominal RMS grid voltage is chosen as the base. Voltage ratings of the dc-link capacitor, series and shunt switches would thus have to be higher than this value, after adding some safety margin. Current rating of the series switches also has to be higher than $(1 + k)$ p.u., after adding some safety margin, and treating the nominal sinusoidal RMS load current as the base. The term k then represents the amount of load current “polluted” by low-order harmonic and reactive components, whose negation $-k$ represents the current flowing through the shunt switches, while performing load current compensation.

Rating of the shunt switches must however be larger than k p.u., so as to allow the shunt converter to channel enough energy to the series converter for onward transferring to the load during period of sag compensation, as would also be shown later through experimental testing. For that, the raised shunt value can be set equal to the series value of $(1 + k)$ p.u. for uniformity, or any other higher value that is deemed appropriate. Using these identified values, the overall losses of the back-to-back conditioner are determined using the same simulation approach and parameters for the 600V/50A insulated gate bipolar transistor (IGBT) presented in [20]. Other IGBT parameters can certainly be used, but by using the same parameters as in [20], a firm foundation for result verification is formed without compromising generality. Results obtained are subsequently tabulated in Table 4-1 for later comparison purposes.

4.3.2 Proposed Nine-Switch UPQC

As shown in Fig. 4-2, the proposed nine-switch UPQC operates with its carrier band divided into h_1 and h_2 . The latter, being much narrower, is for blocking small grid harmonic voltages from propagating to the load, which from the example described in [56], is only about 5% of the full carrier band. The minimum dc-link voltage, and hence voltage ratings of components, must then be chosen based on $V_{dc-NS} = 1.05 V_{dc-BB}$, where subscript *NS* is used to represent “nine-switch”. Current rating wise, analysis of the nine-switch UPQC is slightly different, because of its merging of functionalities to gain a reduction of three switches.

Focusing first at the upper S_1 switch, maximum current flowing through it would be the sum of shunt ($-k$) and series ($1 + k$) currents per phase when S_1 and S_2 are turned ON, and hence giving a final value of 1 p.u. Being slightly higher, the common maximum current flowing through S_2 and S_3 is $(1 + k)$ p.u., which flows when S_1 and S_2 are turned ON for the former, and S_1 and S_3 are turned ON for the latter. Note however that these maximum currents are only for sizing the switches, and should not be exclusively used for computing losses. The reason would be clear after considering S_1 as an example, where it is noted that the maximum current of 1 p.u. does not always flow. In fact, when S_1 and S_3 are turned ON, the current flowing through S_1 is smaller at $-k$ p.u., whose duration depends on a number of operating parameters like modulation ratio, phase displacement and others. Analytical computation of losses is therefore nontrivial, as also mentioned in [20], whose simulation approach is now practiced here for computing the UPQC losses. Obtained results for both normal and sag operating modes are subsequently summarized in Table 4-1 for easier referencing.

4.3.3 Nine-Switch UPQC with Only Common Frequency Control

Nine-switch UPQC, constrained to operate with the same common frequency (CF) at its shunt and series terminals, is not able to compensate for harmonic grid voltages. Parameter h_2 in Fig. 4-2 is therefore redundant, and can be set to zero, whose effect is a minimum dc-link voltage that is no different from that of the back-to-back UPQC. The series transformer, being no longer used, can also be bypassed to avoid unnecessary

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leakage voltage drop, and to divert the large load current away from the UPQC, leaving the three switches per phase to condition only the $-k$ shunt current. Among the switches, the lowest S_3 switch behaves differently in the sense that it is always turned ON, as explained in Section 4.2, and therefore produces only conduction losses. It will only start to commute when a sag occurs, and the transformer exists its bypassed state. When that happens, the load current again flows through the switches, inferring that their current rating must still be chosen above $(1 + k)$ p.u., as reflected in Table 4-1, together with some calculated loss values.

4.3.4 Nine-Switch UPQC with Equal Division of Carrier Band

Although not encouraged, the nine-switch UPQC can also be implemented with its carrier band divided into two equal halves, like the different frequency mode studied previously in [18]-[20]. The maximum modulation ratio per reference is then 0.5×1.15 , whose accompanied effect is the doubling of dc-link voltage and switch voltage rating without affecting their corresponding current rating. Such doubling is of course undesirable, which fortunately can be resolved for UPQC and other series-shunt applications, by simply dividing the carrier band appropriately with h_1 being much wider than h_2 , instead of making them equal. Results for the latter, although not recommended, are still added to Table 4-1 for comprehensiveness.

4.3.5 Comparative Findings

Analyzing all results tabulated Table 4-1, it is clear that the higher voltage requirement of the nine-switch UPQC can be as much as doubled, if not implemented correctly. This doubling can fortunately be reduced by narrowing the half, labeled as h_2 in Fig. 4-2, to only 5% of the full carrier band. Another observation noted is the slightly lower losses of the nine-switch UPQC, as compared to its back-to-back precedence, when both schemes have their series compensation activated. The same lower losses are also observed with voltage sag mitigation, but not with equal carrier division. The latter in fact causes losses to more than doubled, because of the doubled dc-link voltage and higher rated IGBT used for implementation.

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The same calculation can again be performed with no series compensation included. For the nine-switch UPQC, it just means the CF mode discussed in Section 4.3 with h_2 set to zero and the transformer bypassed. The former leads to a smaller dc-link voltage, while the latter causes losses to be smaller, since large load current now does not flow through the nine-switch UPQC. For comparison, values calculated for the back-to-back UPQC operating without series compensation are also included, which clearly show it having slightly lower losses under normal operating condition. The lower losses here are attributed to the back-to-back UPQC using only six modulated switches for shunt compensation, while the nine-switch UPQC uses six upper modulated switches (S_1 and S_2 per phase) and three lower conducting switches (S_3). This finding would reverse when sag occurs, during which the back-to-back UPQC uses twelve modulated switches, while the nine-switch UPQC uses only nine, and hence producing lower losses. It might be argued that most sag durations are short, and hence have lesser concern with regard to losses. However, it should not be ignored that sag durations, even though short, are critical to the overall system operation, and should hence be better protected by a less stressed conditioner in terms of losses.

4.4 Modulation and Control

Fig. 4-3 Series control block representation.

The discontinuous modulation schemes expressed as (3.9) that are developed in chapter 3 are incorporated for controlling the nine-switch UPQC with reduced switching losses and roughly same performance standards as its back-to-back

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Fig. 4-4 Bode representation of the selective harmonic regulators found in the series control scheme.

counterpart. Additionally, high-level control schemes are also developed and presented as follows.

4.4.1 Series Control Principles

The series terminals of the nine-switch UPQC are given two control functions that can raise the quality of power supplied to the load under normal and sag operating conditions. For the former, the series terminals of the conditioner are tasked to compensate for any harmonic distortions that might have originated at the PCC. Where necessary, they should also help to regulate the load voltage to compensate for any slight fundamental voltage variation. This second functionality is however more relevant under voltage sag condition, where a sizable series voltage ($\vec{V}_{SERIES} = \vec{V}_{LOAD}^* - \vec{V}_{SUPPLY}$) needs to be injected to keep the load voltage nearly constant. The overall control block representation realized is shown in Fig. 4-3, where the subsystem responsible for voltage harmonic compensation is distinctly identified within the rectangular enclosure.

As seen, the harmonic compensation subsystem is realized by including multiple resonant regulators in the stationary frame for singling out those prominent low-order load voltage harmonics, including the 5th, 7th, 11th and 13th components, for elimination. Transfer functions representing these resonant regulators $H_n(s)$ and their illustration in the Bode diagram are given in (4.1) and Fig. 4-4, respectively [59].

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$$H_n(s) = 2K_I\omega_c \frac{s+\omega_c}{s^2+2\omega_cs+\omega_n^2+\omega_c^2} \quad (4.1)$$

where K_I , ω_n and ω_c represent the gain parameter, chosen harmonic resonant frequency and cutoff frequency introduced for raising stability, but at the expense of slight transient sluggishness.

From Fig. 4-4, it is certainly verified that the regulators introduce multiple high gain resonant peaks only at those chosen harmonic frequencies, with gains at the other frequencies close to zero. Selective harmonic compensation is therefore realizable, and has the advantage of reducing the burden shouldered by the power conditioner, given also that not all harmonics in the load voltage error need to be eliminated in the first place [56] [60]. Another advantage gained by realizing the regulators in the stationary frame is linked to the internal model concept, which hints that a single resonant regulator tuned at a certain frequency can process both positive- and negative-sequence components located at that frequency [61]. In contrast, if realized in the synchronous frame, two control paths per harmonic would generally be needed for processing positive- and negative-sequence components separately. Depending on the number of harmonics considered, such separate paths might end up overstressing the control circuit or microcontroller unnecessarily. To avoid these unwarranted complications, implementation in the stationary frame is therefore preferred, and would in fact suit the carrier-based modulation scheme presented in chapter 3 better.

Upon next detecting the occurrence of voltage sag, the series control focus should rightfully switch from harmonic compensation to fundamental voltage restoration. Spontaneously, the series modulating reference fed to the pulse-width modulator would change from a small harmonic wave pattern to one with fundamental frequency and much larger amplitude, determined solely by the extent of voltage sag. This “normal-to-sag” reference transition has earlier been shown in subsection 4.2.2 to be smooth, so long as the proper higher level control scheme for producing the demanded series modulating reference is in place.

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Moving forward to explain the higher level control operation during sag, Fig. 4-3 is referred to again, where those sag compensating blocks shown above the harmonic regulators are now discussed. Upon analyzing those blocks, the sag compensator is noted to have two degrees of control freedom with the first primary degree formed by subtracting the PCC voltage from the demanded load voltage along the feedforward path to give $\vec{V}_{LOAD}^* - \vec{V}_{SUPPLY}$. Feeding forward of control signal is however not capable of compensating for voltage drops appearing across the filter and transformer. Because of that, a secondary feedback loop is added to act on the load voltage error, derived by subtracting the load voltage from its reference ($\vec{V}_{LOAD}^* - \vec{V}_{LOAD}$). The computed voltage error is then fed through a PI regulator in the synchronous frame, whose effect is to force the steady-state error to zero, and hence compensating for those unaccounted voltage drops appearing across the inductive elements.

Note that for the control presented here, the synchronous-frame is chosen simply because the load voltage reference can then be represented by a single dc constant. If frame transformation is not preferred, resonant regulator in the stationary frame [62] can be used instead, so long as three-phase sinusoids are also used as the load voltage references.

4.4.2 Shunt Control Principles

Fig. 4-5 Shunt control block representation.

As per previous power conditioners, the shunt terminals of the nine-switch power conditioner are programmed to compensate for downstream load current harmonics, reactive power, and to balance its shared dc-link capacitive voltage. To realize these

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Fig. 4-6 Experimental setup and parameters used for testing.

control objectives, an appropriate control scheme is drawn in Fig. 4-5, where the measured load current is first fed through a high-pass filter in the synchronous frame. The filter blocks fundamental d-axis active component, and passes forward the harmonics and q-axis reactive component for further processing. In parallel, a PI regulator is also added to act on the dc-link voltage error, forcing it to zero by generating a small d-axis control reference for compensating losses, and hence maintaining the dc-link voltage constant. The sum of outputs from the filter and PI regulator then forms the control reference for the measured shunt current to track. Upon tracked properly, the source current would be sinusoidal, and the load harmonics and reactive power would be solely taken care of by the proposed power conditioner.

4.5 Experimental Verification

To validate its performance, a nine-switch power conditioner was implemented in the laboratory, and controlled using a dSPACE DS1103 controller card. The dSPACE card was also used for the final acquisition of data from multiple channels simultaneously, while a 4-channel Lecoy digital scope was simply used for the initial debugging and verification of the dSPACE recorded data, but only four channels at a time. The final hardware setup is shown in Fig. 4-6, where parametric values used are also indicated. Other features noted from the figure include the shunt connection of the upper UPQC terminals to the supply side, and the series connection of the lower terminals to the load side through three single-phase transformers. Reversal of terminal connections for the setup, like upper $\rightarrow$ series and lower $\rightarrow$ shunt, was also effected, but was observed

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to produce no significant differences, as anticipated. For flexible testing purposes, the setup was also not directly connected to the grid, but was directed to a programmable ac source, whose purpose was to emulate a controllable grid, where harmonics and sags were conveniently added.

With such flexibility built-in, two distorted cases were programmed with the first

Fig. 4-7 Experimental supply, series injection and load voltages captured during normal power conditioning mode.

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Table 4-2 Load voltage compensation results

	5 th	7 th	11 th	13 th	5 th	7 th	11 th	13 th
No compensation	2.58%	2.79%	0.85%	1.35%	9.13%	5.59%	3.16%	2.39%
	THD=4.18%				THD=11.43%			
With compensation	0.11%	0.34%	0.06%	0.46%	0.01%	0.39%	0.11%	0.70%
	THD = 0.92%				THD = 1.12%			

having a lower total harmonic distortion (THD) of around 4.18%. This first case, being less severe, represents most modern grids, regulated by grid codes, better. The second case with a higher THD of around 11.43% was included mainly to show that the nine-switch UPQC can still function well in a heavily distorted grid, which might not be common in practice. Equipped with these two test cases, experiments were conducted with the shunt compensation scheme shown in Fig. 4-5 always activated, so as to produce the regulated dc-link voltage needed for overall UPQC operation. The series compensation scheme shown in Fig. 4-3, on the other hand, was first deactivated, and then activated to produce the two sets of comparative load voltage data tabulated in Table 4-2. The data obviously shows that the proposed nine-switch UPQC is effective in smoothing the load voltage, regardless of the extent of low order grid harmonic distortion introduced.

Fig. 4-8 Experimental source, shunt injection and load currents captured during normal power conditioning mode.

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Fig. 4-9 Experimental supply, series injection and load voltages during (a) normal-to-sag and (b) sag-to-normal transitions.

To strengthen this observation, Fig. 4-7 shows the supply, series injection and load voltages for the second test case with a higher grid THD, and with both series and shunt compensation activated. The supply voltage is indeed distorted, and would appear across the load if series compensation is deactivated and the transformer is bypassed. The distortion would however be largely blocked from propagating to the load, upon activating the series compensation scheme with the shunt compensation

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Fig. 4-10 Experimental grid, shunt injection and load currents during (a) normal-to-sag and (b) sag-to-normal transitions.

scheme still kept executing. Example load voltage waveform illustrating this effectiveness can be found at the bottom of Fig. 4-7.

Roughly the same results were also obtained when the nine-switch inverter was replaced by its back-to-back precedence with all other system parameters and control schemes kept unchanged. This finding is certainly expected, since both converters differ only by their high frequency switching harmonics produced, which will not be prominent in those filtered quantities of interest, shown in Table 4-2 and Fig. 4-7. Producing the same results is however still an advantage for the nine-switch inverter,

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since it achieves that with three lesser semiconductor switches, and hence a lower system cost. To next verify its shunt compensating ability, Fig. 4-8 shows the source, shunt injection and load currents conditioned by the nine-switch UPQC. Although the load current is heavily distorted, the shunt control scheme Fig. 4-5 is capable of compensating it, so that the grid current drawn is always sinusoidal, as intended.

With the programmable source now configured to introduce a 20% sag, Fig. 4-9 shows the correspondingly sagged grid voltage, series injection voltage, and compensated load voltage during the normal to sag transition and its inverse recovery. These waveforms collectively prove that the sag has been blocked from propagating to the load, while yet using lesser semiconductor switches. Complementing, Fig. 4-10 shows the grid, shunt injection and load currents during the same normal to sag transition and its recovery. The grid current is obviously sinusoidal throughout the whole transitional process with an increase in amplitude noted during the period of grid sag. This increase in grid current is transferred to the shunt terminal of the nine-switch power conditioner, whose absorbed (negative of injected) current now has a prominent fundamental component, as also reflected by the second row of waveforms plotted Fig. 4-10. Upon processed by the nine-switch power stage, the incremental power associated with the higher shunt current is eventually forced out of the series terminal as an injected voltage, needed for keeping the load voltage and power unchanged.

Yet another feature verified through the testing is the dc-link voltage needed by the nine-switch power conditioner, whose value is always higher than that of the back-to-back conditioner, if series compensation is demanded. This increase can however be kept small by adopting the carrier division scheme shown in Fig. 4-2. To confirm that, Fig. 4-11 shows the conditioner dc-link voltage regulated at only 270 V throughout the whole sag and recovery process. This dc-link voltage is merely 8% higher than that of the back-to-back case, hence verifying those theoretical reasoning discussed in Sections 4.2 and 4.3.

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Fig. 4-11 Experimental dc-link voltage during (a) normal-to-sag and (b) sag-to-normal transitions.

4.6 Summary

This chapter evaluates shortcomings experienced by previous applications of the newly proposed nine-switch inverter. With a better understanding developed, the conclusion drawn is that the nine-switch inverter is not an attractive alternative for replacing back-to-back converter with two shunt bridges. Instead, the nine-switch inverter is more suitable for replacing back-to-back converter in “series-shunt” systems, where one good example is the UPQC. As a further performance booster, the modified 120° -discontinuous modulation scheme developed in Chapter 3 is also incorporated here for reducing the overall commutation count by 33%. Following up next with proper shunt and series control, harmonics, reactive power and voltage sags are compensated promptly with no appreciable degradation in performance. To summarize, the proposed power conditioner has the following anticipated advantages, which have been verified in simulation and experimentally:

- Doubling of dc-link voltage is not necessary, unlike existing “shunt-shunt” applications.
- Lower component stress and hence implementation cost as compared to existing “shunt-shunt” configurations.

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- Nearly the same performance (harmonic mitigation and voltage sag compensation) achieved even with 25% lesser semiconductor;
- Same implementation complexity and no significant increase in operating losses as compared to its back-to-back precedence;

Chapter 5 Compact Integrated Energy Systems for Distributed Generation

This chapter shows how the nine-switch converter can be used as an integrated renewable energy generation system. Instead of handling only ac sources and loads, the integrated concept has been broadened to include ac and dc sources, loads and storages. The created system, when multiplied, forms multiple distributed nodes for more reliable energy generation.

5.1 Introduction

So far, the nine-switch inverter and its derived topologies are always used in ac/ac conversion systems, where the output terminals are always divided into two sets for handling either two ac three-phase outputs or a single ac input and output, as described in previous chapters and existing applications reported in [18][19][46][55].

Instead of only three-phase ac conversion, the distributed generation (DG) systems proposed in this chapter generalize the nine-switch inverter as an entity that can support a hybrid combination of dc-dc, dc-ac and other forms of energy conversion requirements in a single integrated unit with multiple sources, storages and loads connected to it. Moreover, through the proper design of the system and modulation requirements, those shortcomings associated with existing ac applications of the nine-switch inverter reported in [18][19][46][55] can also be dismissed, hence offering a real competitive integrated solution for consideration with minimized tradeoffs.

Distributed generation (DG) by local green energy sources has gained worldwide attention because of the ever-growing energy demand, gradual depletion of fossil fuels and environmental concerns linked to the burning of fossil fuels. Accompanying this interest is an equally intensive effort devoted to energy storages like batteries, ultra-capacitors and flywheels [63]-[65]. Energy stored in these mediums can appropriately be used for smoothing variations linked to most green (usually renewable) sources,

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which at present are major shortcomings [66]. Another way of smoothing the variations is to design the DG systems with different types of sources, whose generation characteristics must complement each other [67]. There is however no guarantee that a continuous stream of energy will always be produced if the sources are mostly uncontrollable like renewable sources.

For greater controllability, energy storages appear to be unavoidable even though their capacities can be reduced if there are more source types in the systems [68]. The installed energy storages also need not be of the same type. They should instead be designed with a variety like for example a combination of ultra-capacitors and batteries for fulfilling the power and energy density requirements of the considered system [63][64]. In short, that means a typical comprehensive energy system would unlikely be a single-source system. Rather, it would include many entities needed for meeting the local generation, storage, utilization and grid-tied requirements.

Almost always, these entities would have their own power converters for processing energy to a form suitable for storage or consumption. This is no doubt the most flexible arrangement, which certainly is an advantage [69]. Other advantages can also be thought of, but for certain, including too many individual converters to a system might at times introduce too much costly redundancy. This might be the case for renewable systems, whose energy generations are usually intermittent. Power converters connected to them might therefore operate below their rated capacities for a sizable period of time. It might hence be of interest to perform some integration rather than using multiple individual converters as per existing practice.

For that, a number of integrated energy systems using 25% lesser semiconductors are proposed here for distributed generation. Operating principles and advantages of the systems proposed are first clarified before considering their likely performance tradeoffs. These tradeoffs cannot be avoided by most (if not all) reduced semiconductor topologies, but can surely be minimized for the systems proposed. Relevant explanation can be found in a later section, together with experimental results for proving the practicalities of the systems proposed.

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Fig. 5-1 Example (a) block diagram and (b) circuit layout of non-integrated energy system.

5.2 Energy Generation Systems with Non-Integrated Power Converters

Fig. 5-1(a) shows the typical block representation of a common solar energy generation system drawn here for example. Each source or storage included is accompanied by its own dc-dc boost or charging converter tied to a common dc-link. The harnessed energy is then forwarded to a dc-ac inverter for conditioning before channeling it to the grid. The inverter can either be single- or three-phase, even though the latter is explicitly drawn in the diagram. It is also not necessary for the dc-ac inverter to tie to the grid if the energy generated is meant for immediate load consumption in an islanded local microgrid. The dc-ac inverter in an islanded microgrid can also be replaced by a dc-dc converter if the loads are dc by nature. DC

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network is certainly a possibility, but based on present advancement, ac output would probably continue to dominate for many more years.

To reveal more details of Fig. 5-1(a), its individual blocks are filled with some simple representative circuits. The resulting circuit drawn in Fig. 5-1(b) uses twelve semiconductor devices in total. Eleven of the devices are controllable switches with the remaining one being an uncontrollable diode. The diode S'_c can be replaced by a controllable switch if the indicated solar panel in Fig. 5-1(b) is replaced by another type of source that can absorb backward flow of energy. Regardless of that, the system shown in Fig. 5-1(b) clearly lacks integration. Its formation is simply by connecting individual well-known converters to a common dc-link. The system is thus fully decoupled with each converter having virtually no influence on the others. Surely, this is an advantage, but because of the intermittent nature of the solar source (in fact most renewable sources) and battery charging process, most of the converters would likely not operate continuously at their rated capacities [70]. The resulting system built with multiple individual converters is hence neither cost effective nor compact.

The suggestion is then to introduce some amount of integration to the system to cut down on its number of semiconductors. The integrated system must produce comparable input and output performances as the fully decoupled system. Like all reduced semiconductor topologies though, some tradeoffs like higher voltage stresses and control limitations would likely surface [71][72], but can surely be minimized if designed appropriately. Approaches to realize the minimization for the proposed single- and three-phase energy systems are now described as follows.

Fig. 5-2 Illustration of (a) non-integrated four-switch and (b) integrated three-switch topologies.

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Table 5-1 Switching states and output voltages of Fig. 5-2(a)

S_A	S_A'	S_a'	S_a	V_A	V_a
ON	OFF	ON	OFF	V_{DC}	V_{DC}
ON	OFF	OFF	ON	V_{DC}	0
OFF	ON	OFF	ON	0	0
OFF	ON	ON	OFF	0	V_{DC}

Table 5-2 Switching states and output voltages of Fig. 5-2(b)

S_A	S_{Aa}	S_a	V_A	V_a
ON	ON	OFF	V_{DC}	V_{DC}
ON	OFF	ON	V_{DC}	0
OFF	ON	ON	0	0

5.3 Integrated Energy Generation Systems

5.3.1 Method of Integration

The integration principles are better explained by referring first to the non-integrated energy system shown in Fig. 5-1(b). For easier viewing, two of its phase-legs with switches $\{S_A, S_A', S_a', S_a\}$ are drawn separately, as shown in Fig. 5-2(a). For each of the illustrated phase-legs, its two switches must be switched in complement, meaning that when one switch is on, the other must be off. Terminal voltage of the considered phase-leg can then produce two discrete values identified as V_{DC} and 0V. The same applies to the other phase-leg drawn in Fig. 5-2(a). Terminal voltages of the two phase-legs can then be any of the four sets of values indicated in Table 5-1.

Instead of two independent phase-legs, the switches can be rearranged as shown in Fig. 5-2(b), while still providing two terminal voltages. Instead of four switches, only three switches labeled as $\{S_A, S_{Aa}, S_a\}$ are used. That represents a saving of 25%, which can be sizable if more switches are considered. Among the three switches, two of them will be turned on to tie the terminal voltages to either the same or different dc rails at any instant. The three possibilities are summarized in Table 5-2, which when compared with Table 5-1, tells a constraint faced by the three-switch topology. To be more precise, terminal voltages of the three-switch topology cannot produce the fourth combination of $V_A=0V$ and $V_a=V_{dc}$, which certainly is a tradeoff incurred by saving one

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Fig. 5-3 Integrated three-phase energy system with multiple sources and storages.

switch. The overall system design should therefore be planned such that influences from this tradeoff on the terminal voltages are kept to a minimum. Discussion on this issue can be found in the next subsection.

Applying the same integration to the remaining two pairs of phase-legs with switches $\{S_B, S_B', S_b', S_b\}$ and $\{S_C, S_C', S_c', S_c\}$ then results in the integrated energy system shown in Fig. 5-3. The system in Fig. 5-3 uses nine switches as compared to twelve for the non-integrated system shown in Fig. 5-1(b). The same six terminal voltages are retained with the upper three produced by the dc-ac inverter formed by the upper three switches $\{S_A, S_{Aa}, S_a\}$ and middle three switches $\{S_B, S_{Bb}, S_b\}$. On the other hand, the lower three voltages are produced by three dc-dc converters formed by the middle three switches $\{S_B, S_{Bb}, S_b\}$ and lower three switches $\{S_C, S_{Cc}, S_c\}$. The middle three switches are obviously shared by the inverter and converters, which will surely introduce some constraints as already identified (fourth combination of $V_A=0V$ and $V_a=V_{dc}$ cannot be produced).

Before progressing forward, it is appropriate to share here that the same nine-switch topology has earlier been used as an ac-ac converter for dual motor drives, rectifier-inverter systems and uninterruptible power supplies (UPSs) [19][20][46]. In those attempts, the six converter terminals are organized as either two sets of three-phase ac outputs or one set of three-phase ac input and one set of three-phase ac output. They

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have so far been proven fine, but with serious limitations imposed. The limitations can be summarized as either a very limited phase-shift between the two sets of ac terminals or a doubling of dc-link voltage caused by strict amplitude sharing [19][20][46]. These constraints would make the 25% saving in semiconductors not so attractive. Methods for minimizing them are therefore of interest, and are discussed here in the context of energy systems. Concentrating on energy systems also has the merit of merging ac and dc circuits using the nine-switch topology, which so far has not been tried by other researchers.

5.3.2 Modulation Principles

Referring again to those two simplified illustrations shown in Fig. 5-2, making them produce the same terminal voltages would demand that they share the same modulation theories. Some constraints would however be accompanying the three-switch topology shown in Fig. 5-2(b) since it uses lesser switches. A convenient way of explaining the three-switch modulation is hence to focus on the more established independent phase-legs shown in Fig. 5-2(a) first, before shifting the knowledge with constraints added to Fig. 5-2(b).

With the circuit shown in Fig. 5-2(a), the phase-leg tied to the dc source is in theory controlled by a dc reference and a triangular or saw-tooth carrier. The second phase-leg tied to a phase of the three-phase ac grid is similarly controlled by a sinusoidal reference and a triangular carrier (saw-tooth carrier not considered here since it has no spectral benefit [73]). Strictly, carriers of the two phase-legs need not be the same, but in practice, using one carrier has the benefit of involving only one timer. It is hence

Fig. 5-4 Carrier band division and gating signal generation per phase-leg.

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advisable to use a common carrier and two independent references for the circuit shown in Fig. 5-2(a). The same independence cannot be introduced to the integrated topology shown in Fig. 5-2(b), whose sinusoidal reference for the upper terminal must always be placed above its linear reference for the lower terminal. Such placement helps to avoid the fourth restricted state of $V_A=0V$ and $V_a=V_{dc}$.

An example illustrating the three-switch modulation is shown in Fig. 5-4, where a single carrier band is clearly divided into h_1 and h_2 . The upper sub-band h_1 is assigned to the upper terminal, and hence confines the sinusoidal reference. Similarly, the lower sub-band h_2 is assigned to the lower terminal, and hence encompasses the linear reference. Comparing the references with the single common carrier based on the following rules then leads to those gating signals for S_A and S_a shown at the bottom of Fig. 5-4.

$$S_A = \begin{cases} 1, & \text{reference} \geq \text{carrier} \\ 0, & \text{reference} < \text{carrier} \end{cases}$$

$$S_a = \begin{cases} 0, & \text{reference} \geq \text{carrier} \\ 1, & \text{reference} < \text{carrier} \end{cases} \quad (5.1)$$

To ensure that only two switches are on and hence produce any of the three combinations shown in Table 5-2, gating signal for the middle switch S_{Aa} must be derived from the earlier two based on the following.

$$S_{Aa} = S_A \oplus S_a = (!S_A) \oplus (!S_a) \quad (5.2)$$

where $\oplus$ is the logical XOR operator, $!S_A$ and $!S_a$ are the complements of S_A and S_a with dead-time added. Operating on $!S_A$ and $!S_a$ is recommended since it automatically creates the dead-time needed by S_{Aa} to avoid shorting the three switches simultaneously [74]. The full set of gating signals obtained (e.g. bottom of Fig. 5-4) is thus always in agreement with the allowed states summarized in Table 5-2. Another concern noted with the modulation process is the dc offset added to the sinusoidal reference for centering it within h_1 . Like triplen [50][73][74], this offset is added to all

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phases of a three-phase system, and will therefore be cancelled in the line-to-line voltages.

5.3.3 Parameters and Constraints

As mentioned earlier, the lower sub-band h_2 in Fig. 5-4 is assigned to the lower terminal of the three-switch topology shown in Fig. 5-2(b). Given that it is tied to a dc source, the usual parameter of interest would be the duty ratio d or fractional on time of the lower switch S_a . The range of variation of d and its accompanied gain G_{dc} ($= 1/(1 - d)$) can accordingly be determined as:

$$(1 - 0.5h_2) \leq d \leq 1; \quad 2/h_2 \leq G_{dc} < \infty \quad (5.3)$$

For interfacing the dc source to the ac grid, G_{dc} must usually be high so as to minimize the number of dc sources or storages connected in series. With fewer entities in series, problems like shading and unbalanced charging [75] are less prominent, inferring that mechanisms for preventing them might not be necessary. The overall system is hence simplified, which certainly is a strong reason for keeping h_2 small and G_{dc} high.

Referring now to the upper terminal of the three-switch topology shown in Fig. 5-2(b), since it is tied to an ac source, its parameter of interest would be the modulation index M . Referring to Fig. 5-4, M represents the amplitude of the sinusoidal reference, which in theory, is also equal to the resulting buck gain G_{ac} . Its value can vary within the range spelled in (5.4), where the factor of 1.15 is added for representing triplen insertion [73][74].

$$0 \leq M \leq 1.15 \times h_1/2 \quad (5.4)$$

Value of M is also known to vary inversely with the dc-link voltage V_{DC} ($M \propto 1/V_{DC}$) in the case of a fixed ac grid voltage. Lowering V_{DC} therefore requires M and hence h_1 to be high. That means $h_2=2-h_1$ in Fig. 5-4 must be low, which for the proposed energy system, is fine since a high dc gain G_{dc} is needed, as explained earlier. The proposed energy system is therefore a more suitable system for applying the three-switch

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Fig. 5-5 Other integrated configurations for (a) three-phase and (b) single-phase grid-tied energy conversion.

topology shown in Fig. 5-2(b) rather than those ac-ac converters suggested in [19][20]. In those references, V_{DC} is doubled because M is set to a maximum of only 0.5.

5.3.4 Other Integrated Configurations

Instead of the system shown in Fig. 5-3, the three-switch topology shown in Fig. 5-2(b) can be used to form other energy systems. Two proposed examples are given in Fig. 5-5(a) and (b), where again three three-switch phase-legs are shown. In general, the number of three-switch phase-legs connected in parallel can be any positive integer number. It depends on the number of sources, storages and loads connected together. Where needed, traditional two-switch phase-legs can also be added in parallel to the three-switch phase-legs. This extension is relatively straightforward, and will hence

Fig. 5-6 Illustration of dc-link voltage increase for three-switch topology.

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not be explicitly shown in the chapter.

Rather, the intention for including Fig. 5-5(a) is to show the additional possibility of connecting a solar panel (indicated only as an example) to the dc-link through its dc-dc converter. Unlike Fig. 5-3, no source is now connected to the lower three dc terminals, which are instead tied to three storages (two batteries and an ultra-capacitor). The system however retains its three-phase ac grid interfacing like in Fig. 5-3. For illustrating single-phase grid interfacing, Fig. 5-5(b) is referred to instead, where two of its upper terminals are used for single-phase grid interfacing. The same dc offset as in Fig. 5-4 must still be added to the two 180° -phase-shifted sinusoidal references for the two upper terminals, which when subtracted, will not appear in the ac voltage ($V_A - V_B$). Since the third upper terminal is now not used for grid interfacing, it can either be removed together with switch S_C or tied to a dc load, as demonstrated in Fig. 5-5(b). Other connections to the lower three dc terminals in Fig. 5-5(b) remain unchanged as in Fig. 5-3.

5.4 Three-Switch versus Four-Switch Topologies

5.4.1 DC-Link Voltage

As described earlier, the four-switch topology shown in Fig. 5-2(a) is divided into two independent phase-legs with no restriction on their modulation parameters. Choosing the ac terminal voltage V_A as the base ($= 1p.u.$), the minimum dc-link voltage V_{DC} is then given by $1.74p.u.$ if V_A is assumed to be a phase of a three-phase ac grid. This value is obtained by substituting the maximum modulation index of $M=1.15$ to the standard definition of $M=V_A/((V_{DC}/2))$. On the other hand, if a single-phase ac system is considered, the minimum V_{DC} would change to $2p.u.$ since the maximum M is now 1. Converting from three-phase to single-phase system is thus a simple multiplication by 1.15, which is also applicable to the three-switch topology shown in Fig. 5-2(b).

Unlike the four-switch topology, maximum modulation index of the three-switch topology in a three-phase system is not $M=1.15$, but rather given by the expression in (5.4). The minimum dc-link voltage V_{DC} of the three-switch topology is thus computed

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Table 5-3 Currents through switches at different output voltages for four-switch topology

S_A	S_A'	S_a'	S_a	V_A	V_a
I_{ac}	0	$-I_{dc}$	0	V_{DC}	V_{DC}
I_{dc}	0	0	I_{dc}	V_{DC}	0
0	$-I_{ac}$	0	I_{dc}	0	0
0	$-I_{ac}$	$-I_{dc}$	0	0	V_{DC}

Table 5-4 Currents through switches at different output voltages for three-switch topology

S_A	S_{Aa}	S_a	V_A	V_a
$-(I_{dc} - I_{ac})$	$-I_{dc}$	0	V_{dc}	V_{dc}
I_{ac}	0	I_{dc}	V_{dc}	0
0	$-I_{ac}$	$I_{dc} - I_{ac}$	0	0

as $(3.48/h_1)p.u.$ for the three-phase systems shown in Fig. 5-3 and Fig. 5-5(a). (As mentioned earlier, a multiplication factor of 1.15 needs to be included for the single-phase system shown in Fig. 5-5(b)). In percentage term, it represents an increase given by (5.5).

$$\Delta V_{DC} = \frac{(3.48/h_1) - 1.74}{1.74} \times 100\% = \left(\frac{2}{h_1} - 1 \right) \times 100 \quad 1 \leq h_1 \leq 2 \quad (5.5)$$

Variation of (5.5) is shown in Fig. 5-6, from which it is read that the increase is 100% or doubled when $h_1 = 1$ or $M = 0.5$. This doubling of dc-link voltage is experienced by those ac-ac converters proposed in [19][20], which conceptually can be reduced here by increasing h_1 . For example, if h_1 is raised to 1.6 and 1.8, the increase ΔV_{DC} would respectively be 25% and 11%. It is hence important to keep one sub-band much wider than the other ($h_1 \gg h_2$ shown in Fig. 5-4), which fortunately is a requirement enforced by the proposed energy systems. This identification has so far not been discussed in the open literature.

When dividing the carrier band, it is also of concern to mention here that the upper sub-band h_1 must include all upper references and the lower sub-band h_2 must include all lower references. That indirectly means the highest modulating references in both sub-bands will decide on the appropriate level to divide in the full carrier band. These references correspond to the highest upper and lower terminal voltages that the inverter can manage.

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5.4.2 Switch Current and Overall System Losses

Instantaneous current stresses experienced by the switches can be found by considering the individual terminal currents and converter states summarized in Table 5-1 and Table 5-2 for the four-switch and three-switch topologies. For clarity, positive reference currents for the terminals are defined here as those of I_{ac} and I_{dc} drawn in Fig. 5-2(a) and (b). Positive current through a switch is also defined as current flowing through its transistor, which then means negative current flows through its anti-parallel diode.

With these definitions, the four-switch topology shown in Fig. 5-2(a) can easily be analyzed by considering which switches from its two phase-legs are turned on. The turned-on switches will carry the respective terminal currents, which then lead to those entries shown in Table 5-3 for each pair of corresponding terminal voltages. The table shows that each switch of the non-integrated four-switch topology carries a terminal current, which is not true for the integrated three-switch topology. For example, to produce $V_A = V_a = V_{DC}$, the first row of Table 5-2 indicates that the upper two switches S_A and S_{Aa} of the three-switch topology must be turned on, which then lead to currents $-(I_{dc} - I_{ac})$ and $-I_{dc}$ flowing through them. Current flowing through S_A is obviously decided by two terminal currents and not one. The same determination can be applied to the other two states listed in Table 5-2 with their resulting current expressions summarized in Table 5-4. Table 5-4 is in principle applicable to the three systems shown in Fig. 5-3, Fig. 5-5(a) and (b) since they use the same three-switch topology and the same three operating states.

The currents obtained in Table 5-3 (first three rows only) and Table 5-4 can then be compared for each pair of terminal voltages produced. The conclusions drawn are summarized below.

- By eliminating one switch, the middle switch S_{Aa} of the three-switch topology carries the same current as either S_A' or S_a' of the four-switch topology, depending on the state presently being assumed.

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- Current through S_A of the three-switch topology has an interval over which its current is $-(I_{dc}-I_{ac})$. Otherwise, it is closely similar to the current flowing through S_A of the four-switch topology.
- Current through S_a of the three-switch topology is similar to that flowing through the same switch of the four-switch topology, except for an interval over which current is $(I_{dc}-I_{ac})$.

It should be noted here that absolute amplitude of the current $(I_{dc}-I_{ac})$ depends on the amount of boosting introduced and the individual current polarities (e.g. charging or discharging, terminals connected to sources, storages or loads). Instantaneous current stresses might therefore be raised, but that does not imply the same for the overall system losses. On average, if a good mix of different entities is tied to the integrated system, its losses should either be comparable or slightly raised as compared to its non-integrated correspondence. The slightly higher losses are mainly caused by the slightly higher dc-link voltage needed by the integrated system, as understood from Fig. 5-4.

To demonstrate, overall losses of the non-integrated and integrated energy systems shown in Fig. 5-1(b) and Fig. 5-3 have been computed based on the simulation approach proposed in [76]. Switches used for the simulation are 600V/50A insulated gate polar transistors (IGBTs), whose parameters can be found in [20]. For both systems, energy flow has been tuned to flow from the solar source to the ac grid and storages. Results obtained are tabulated in Table 5-5 for small $h_2 \leq 0.4$, which is in accordance to the earlier suggested band sizing requirement. The results show that for smaller h_2 , losses of the non-integrated energy system increase because of the lower dc terminal voltages, and hence higher dc terminal currents if the system power is kept constant. The integrated system, on the other hand, has its losses reduced because of the lower dc-link voltage associated with a smaller h_2 . This trend is applicable to both three-phase systems shown in Fig. 5-3 and Fig. 5-5(a), except for higher loss values anticipated with Fig. 5-5(a) because of its additional switch S, diode D and other passive components.

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Table 5-5 Losses of energy systems with three-phase grid

h_2	Non-Integrated System		Integrated System	
	DC-Link Voltage (p.u.)	Losses (% Rating)	DC-Link Voltage (p.u.)	Losses (% Rating)
0.2	1.74	1.65	1.93	1.41
0.3	1.74	1.53	2.05	1.65
0.4	1.74	1.41	2.17	1.91

Table 5-6 Losses of energy systems with single-phase grid

h_2	Non-Integrated System		Integrated System	
	DC-Link Voltage (p.u.)	Losses (% Rating)	DC-Link Voltage (p.u.)	Losses (% Rating)
0.2	2.0	1.55	2.22	1.11
0.3	2.0	1.43	2.36	1.22
0.4	2.0	1.41	2.50	1.41

The evaluation is next performed with the three-phase grid in Fig. 5-1(b) replaced by a single-phase grid and a resistive load like those shown in Fig. 5-5(b) for the single-phase integrated system. Results obtained for both systems can be found in Table 5-6, which upon compared, show lower losses for the integrated system. The reason might probably be linked to the third upper terminal supplying a positive current to the dc load. The earlier notated upper current I_{ac} is thus always positive, which when subtracted from I_{dc} , will always lead to a smaller ($I_{dc}-I_{ac}$) for the third three-switch phase-leg. Since its currents are reduced, its losses will reduce accordingly too.

5.5 Control Principles

In this section, only the control schemes for the integrated energy system shown in Fig. 5-3 are explained in details. This does not compromise generality since the other two discussed systems in Fig. 5-5(a) and (b), and the non-integrated system shown in Fig. 5-1(b) share the same control principles. The same control schemes were in fact used for single and three-phase experimental testing, whose results are shown in a later section. It is hence appropriate to consider only Fig. 5-3 with its upper dc-ac inverter control discussed now with reference to the upper half of Fig. 5-7. In that representation, the dc-link voltage V_{DC} is first measured, before being regulated by a classical proportional-integral (PI) controller to follow a defined command V_{DC}^* . Parameters of this PI controller are designed based on [77], where the inner current loop, being much faster, is replaced by a time-lap and a low-pass-filter block for

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Fig. 5-7 Per-phase illustration of overall control schemes.

representing computational delay and capacitor charging dynamics. The proportional and integral gains are then chosen as $K_{pi}=0.1$ and $K_{il}=10$ to give enough phase margin for maintaining overall system stability.

The PI output, being the active current amplitude needed for keeping V_{DC} constant, is then multiplied with a unit sine synchronized with the ac grid voltage V_{grid} by a

Fig. 5-8 Bode plot of PR controller $G_{PR}(s)$.

Fig. 5-9 Per-phase ac inner current loop.

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standard phase-lock-loop (PLL). The resulting ac signal I_{ac}^* represents the in-phase active current reference fed to the inner current loop. The inner current controller can no longer be a PI controller, whose steady-state error is not zero because of its finite gain at the ac frequency of interest [61][78][79][80]. A proportional-resonant (PR) controller is used instead, whose transfer expression is written as:

$$G_{PR}(s) = K_{p2} + \frac{2K_{i2}\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (5.6)$$

where K_{p2} and K_{i2} are the controller gains, ω_c and ω_0 are the angular cutoff and fundamental frequencies, respectively. Bode diagrams of (5.6) are plotted in Fig. 5-8, where a high resonant peak at the 50Hz frequency of interest can clearly be seen. This peak will gradually tend towards infinity as $\omega_c \rightarrow 0$.

Fig. 5-10 Bode plots of feedforward path of Fig. 5-9.

The final tracking performance of the inner current loop can be verified by referring to its control block diagram drawn separately in Fig. 5-9. Filter impedance ($R+sL$) and grid voltage V_{grid} have now been included in the figure for arriving at its closed-loop transfer function written in (5.7). The derived transfer function clearly has two terms

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for informing that if the controller gains are chosen high enough, I_{ac} will follow its reference I_{ac}^* exactly with little influence from V_{grid} .

$$I_{ac} = \frac{G_{PR}(s)V_{dc}}{G_{PR}(s)V_{dc}+sL+R} I_{ac}^* - \frac{1}{G_{PR}(s)V_{dc}+sL+R} V_{grid} \quad (5.7)$$

The controller gains, on the other hand, cannot be too high if the system is to be kept stable. To balance the tradeoff, Bode diagrams of the open-loop transfer function of Fig. 5-9 are plotted in Fig. 5-10. In addition to those obtained with the PR controller, relevant plots obtained with a proportional (P) controller are also included in Fig. 5-10 for the design. The design procedure read from [80] then suggests choosing a proportional gain K_{p2} for the P controller so that the system is stable with good transient response. For that, $K_{p2}=0.1$ is chosen, which gives more than 90° of phase margin at the system crossover frequency (instant at which magnitude response drops to 0dB). The system is thus stable.

The second step is to design the resonant gain so that acceptably small steady-state errors are produced, together with a satisfactory phase margin. The chosen resonant gain here is $K_{i2}=10$, which will alter only the magnitude response around 50Hz, and not at the crossover frequency. The final phase margin is thus still more than 60°, which needless to say, represents a stable system. Cutoff frequency ω_c can next be chosen, whose purpose is mainly to lessen selectiveness by widening the bandwidth around the resonant peak. This can be helpful if the 50Hz resonance frequency varies slightly, but should not be excessive since the resonant peak amplitude drops significantly as ω_c increases.

The resulting signal from the properly designed PR controller then forms the required ac modulating reference (upper sinusoidal reference in Fig. 5-4) needed for switching pulse generation. For that, a timer counting from 0 to 1 and then back is used for realizing a positively displaced triangular carrier, unlike that drawn in Fig. 5-4. The ac modulating reference should therefore be changed according to (5.8), whose effect is still to place the reference centrally within the upper sub-band h_I .

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$$V'_{ac_PWM} = 0.5V_{ac_PWM}h_1 + 1 - 0.5h_1 \quad (5.8)$$

Attention should next be focused on the control scheme shown at the bottom of Fig. 5-7 for the dc-dc converters. In that scheme, a power reference (or voltage reference in some cases) is first created by an algorithm linked to the source or storage. For the case of a solar module, the power reference is usually decided by an appropriate maximum-power-point-tracking algorithm [81][82]. The determined power reference can then be divided by the measured input voltage to create a current reference I_{dc}^* for tracking by the dc boost current I_{dc} . Tracking is enforced here by a simple PI controller, whose high dc gain helps to force zero dc steady-state error. Tuning of this PI controller is presently well established, and can in fact be done in Matlab after setting the desired closed-loop bandwidth to be a fifth of the switching frequency or lower. The final parameters obtained are summarized here as $K_{p3}=0.301$ and $K_{i3}=2131$.

The output from the PI controller is then added to the feedforward source voltage V_{dc} , before being normalized by half the dc-link voltage ($V_{DC}^*/2$) to form the linear dc modulating reference M_{dc} . This modulating reference, according to Fig. 5-4, is placed within the lower sub-band h_2 . Since the carrier is realized with a timer counting between 0 and 1 as mentioned earlier, no dc offset needs to be added to M_{dc} , unlike the ac reference V_{ac_PWM} .

In general, the presented control schemes function well with the same steady-state responses produced by the non-integrated and integrated energy systems, if controlled

Fig. 5-11 Experimental setups and parameters used for (a) single-phase and (b) three-phase energy systems.

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by the same control schemes. Their transient responses are however different caused by coupling introduced by the integrated energy system. To illustrate, a transient step decrease in dc source current reference I_{dc}^* is assumed as an example. To make the actual dc source current I_{dc} track rapidly, the on time of the lowest switch (e.g. S_a in Fig. 5-3) should be shortened, which according to (5.1) and Fig. 5-4, requires the dc modulating reference M_{dc} to increase. The amount by which M_{dc} can increase, is however limited to h_2 for the integrated energy system. Its current response is therefore slower than the non-integrated system whose modulating reference is not confined to h_2 . Slower response is however not experienced during transient step increase in current, which based on the reverse reasoning, requires the on time of the lowest switch to be lengthened. This requires lowering M_{dc} , which according to Fig. 5-4, is not restricted by the integrated system.

The above-explained slower current decrease of the integrated system is undeniably a disadvantage. But, when compared with the usually slow maximum-power-point-tracking, storage charging and discharging, its impact might not be significant. The proposed energy system is therefore still competitive as compared to its non-integrated counterpart.

5.6 Experimental Results

For verification of practicality, scaled-down prototypes shown in Fig. 5-11(a) and (b) were assembled in the laboratory using parameters indicated in the figures (values chosen from those available in the laboratory, and hence not optimized). Fig. 5-11(a)

Fig. 5-12 Modulating references for single-phase system in Fig. 5-11(a) and three-phase system in Fig. 5-11(b) before transient.

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Fig. 5-13 Experimental waveforms of single-phase system in Fig. 5-11(a).

was clearly a single-phase grid-tied system with two of its upper terminals connected to one phase of a 155-V (line-to-line rms), 50-Hz three-phase ac grid and a local single-phase ac load of 30Ω . The third upper terminal was tied to a local dc load of 13Ω , while the lower three terminals were connected to three separate dc sources of 30V each.

Two 180° phase-shifted sinusoidal and four linear references were thus needed, as reflected by Fig. 5-12(a). In the figure, two upper sinusoidal references and a single linear load reference at $M_{dc} = 0.33$ were shown occupying the upper sub-band with width of $h_1/2 = 0.8$. Also shown in the figure were three lower linear references clustering around $M_{dc} = 0.15$ for the dc sources. They occupy the lower narrower sub-band with width of $h_2/2 = 0.2$.

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Fig. 5-14 Experimental waveforms of three-phase system in Fig. 5-11(b).

Corresponding waveforms of the single-phase power stage were then measured and plotted in Fig. 5-13 for two intentionally created transient events triggered at $t = 100\text{ms}$ in each plot. For the event shown in Fig. 5-13(a), all three dc sources were initially generating positive powers with their respective values read from the fourth to sixth traces as 100W, 150W and 200W before $t = 100\text{ms}$. The generated powers were for local dc load consumption and injection to the ac grid. The former was reflected by the positive dc load current in the last trace, while the latter was reflected by the 180° phase-shifted ac voltage and current in the first two traces before $t = 100\text{ms}$. At $t = 100\text{ms}$, dc source 1 was interrupted with the local dc load demand kept unchanged. Power output from dc source 1 therefore dropped to zero in the fourth trace, while the dc load current in the last trace remained constant. The amount of surplus energy injected to the grid was thus reduced, causing the ac supply current in the second plot of Fig. 5-13(a) to drop.

The same initial conditions in Fig. 5-13(a) were repeated in Fig. 5-13(b), whose transient event at $t = 100\text{ms}$ was triggered by turning off dc sources 1 and 2 with the dc load demand kept unchanged. Power values in the fourth and fifth traces of Fig. 5-13(b)

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therefore dropped to zero with the load current in the last trace kept constant. The remaining dc source 3 was not able to power the load fully, hence causing the ac grid current in the second trace to reverse. The ac grid current was now in phase with the ac grid voltage, representing energy drawn from the grid.

Testing was next performed on the three-phase system shown in Fig. 5-11(b) with its upper three terminals tied to the three-phase ac grid and a local ac load of 20Ω per phase. The lower three terminals were connected to two 50V dc sources and a 7Ω dc load, respectively. The references needed were therefore three upper sinusoidal references with triplen offset added and three lower linear references, occupying sub-bands h_1 and h_2 in Fig. 5-12(b). The common dc-link voltage produced was 350V, as seen from the third trace in Fig. 14. This value could be reduced further by narrowing h_2 or widening h_1 , as illustrated in Fig. 5-6. Two transient events were also emulated here with the first shown in Fig. 5-14(a). Throughout the illustrated duration, both dc sources were producing positive powers, as read from the fourth and fifth traces in the figure. Part of the generated powers was for local dc load consumption reflected by the last trace in Fig. 5-14(a). The rest was for ac grid injection reflected by the 180° phase-shifted ac voltage and current in the first two traces. Power from dc source 2 was subsequently lowered at $t = 100\text{ms}$ with the local dc load kept constant. Lesser power was hence injected to the grid, causing the ac current in the second trace to drop in magnitude after $t = 100\text{ms}$.

A second transient event was repeated in Fig. 5-14(b) with the same initial system conditions and constant dc load assumed. The transient was triggered by turning off both dc sources at $t = 100\text{ms}$, causing the fourth and fifth traces to collapse to zero. The grid eventually had to reverse its energy flow to supply the local dc load. This was reflected by the ac grid current reversal in the second trace, to be now in-phase with the grid voltage in the first trace. These results clearly prove the effectiveness of the proposed integrated energy systems, which in principle, can also be produced by the non-integrated energy systems like the example shown in Fig. 5-1(b). The integrated systems however have the following anticipated features, which have now been proven experimentally.

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- The same compact integrated configuration can be used for single and three-phase energy systems, which is particularly advantageous for renewable systems, whose energy generations are usually intermittent;
- Doubling of dc-link voltage is not necessary, unlike those ac-ac converters found in [18][19].
- No significant deterioration of transient responses when applied to energy systems.
- Energy flows through all terminals are not impeded by the converter merging, hence giving rise to no damaging surge or dip in voltage across the dc-link. The dc-link voltage in fact remains nearly constant throughout the experiments.
- Virtually the same performance achieved with 25% lesser semiconductor.

The proposed systems might also appear to have some limitations, which are practically not major concerns because of the following reasons:

- Implementation complexity is not raised because of the same single timer / carrier and some simple dc offsets needed (dc offsets easily added together with triplens);
- Despite the slight increase in dc-link voltage, calculation shows that the proposed energy system is still competitive in terms of efficiency, as compared to its non-integrated precedence;
- Operating tradeoffs linked to the lower switch count can easily be avoided through proper modulation, and hence does not contribute to major operating problems.

5.7 Summary

This chapter proposes a number of integrated energy systems based on a compact converter topology. Through proper design, the proposed systems are shown to output

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equally good terminal waveform quality, while yet gaining advantages like reduced switch count and compactness. Surely, some tradeoffs cannot be avoided, but can be minimized through proper modulation planning, and hence does not constitute a major problem. Experimental testing has already confirmed their conceptual validity and practicality, regardless of whether implemented in single- or three-phase form.

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This chapter proceeds to modularize the reduced semiconductor concept, creating multiple six-switch modules in turn for cascading. The resulting converter formed has better multilevel terminal characteristics, and uses lesser semiconductors than a traditional back-to-back cascaded multilevel converter. It however faces limitations, which fortunately can be reduced for certain applications. One prospective system is an online UPS, whose control and implementation are discussed in the chapter.

6.1 Introduction

Uninterruptible Power Supply (UPS) is extensively used to produce an undisturbed flow of power even during periods of voltage outages, sags or swells. Therefore it is highly suitable for protecting loads found in hospitals, defense infrastructures, server rooms, and most manufacturing industries [83]. Besides protecting loads, UPS can also be programmed for reactive power compensation and harmonic isolation [84][85], hence raising the power quality of the input line. These features are of course not always needed, and the level of protection demanded can vary over different loads. Because of that, different types of UPS are available for selection with the final choice made only after reviewing the current cost constraint, space limitation, functionalities needed and comfortable level of protection, which almost always are the main deciding factors.

The different types of UPS can however be divided into three broad categories, commonly known as offline, line interactive and online types [86]. The offline UPS is normally not connected to the loads but kept on standby. It would switch in to power the loads only when the input line disconnects due to upstream faults. The critical concerns related to an offline UPS is its ability to sense line tripping fast, and the promptness of the UPS switching in mechanism. Delays are therefore unavoidable, however, it is still preferred sometimes, given its unmatched low conversion losses.

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The interactive UPS, unlike the offline counterpart, is always connected to the loads. However, the loads are also connected to the input line. Normally, the loads draw their energy from the input line, while the UPS compensates for line disturbance, if controlled to do so. Upon detecting a fault, the input line trips, and hence the UPS switch in to be the sole source powering the loads. Unlike the offline type, the interactive UPS experiences a shorter switchover delay. It however has a drawback linked to the tying of loads to the input line, which certainly would subject them to fault during the switchover period. It is therefore not the preferred, if even higher level of protection is demanded, as compared to an online UPS.

The Online UPS is presently recognized as offering the best protection with virtually no switchover time [87]. It will not subject the loads to line fault, since there is not any direct link between the input line and loads. An online UPS will first rectify energy from the input line to dc, before inverting it to a well-regulated ac for feeding the loads. At its intermediate dc stage, energy can also be diverted to storage mediums like batteries for charging. The stored energy would subsequently be released to the loads upon sensing a failure, and tripping the input line from the rectifier stage of the online UPS. Obviously, the online UPS is the most protected, but its always actively double-conversion stage would significantly bring down the overall system efficiency. Such low efficiency appears to be unavoidable, though slight improvements is at times possible. Because of that, it would generally be more meaningful to single out other aspects of an online UPS for improvement, while still retaining its safety features. Bearing this in mind, an online UPS is now formed with the proposed semiconductor-reduced configuration. A number of advantages are now shown like improved redundancy, better waveform quality, higher power capability and 25% lesser semiconductor usage, compared to the traditional approach of implementing a cascaded system. Through the analysis, it is shown that the proposed UPS does also not suffer from any noticeable performance trade-offs, unlike most other reduced semiconductor attempts for either UPS or other power conditioners. Facilitated with these improved features and being generally a safer online alternative, the proposed UPS is likely to be used in the critical loads where reliability and high premium power are basic necessities. The conceptual discussion about proposed UPS and its verification in hardware setup is also presented.

6.2 Cascaded Online Topology

Fig. 6-1 Block diagram representation of an online UPS

The basic diagram representing an online UPS is shown in Fig. 6-1, where a rectifying and an inverting stage are placed back-to-back with an energy storage added at their common dc-link. Transformer isolation can be placed at the input end, or both input and output ends for protection purposes. To raise redundancy and waveform quality, the circuit blocks in Fig. 6-1 can be constructed with cascaded multilevel converter, formed by using single-phase H-bridges [88]. In order to make this cascaded configuration to work, isolation between modules is needed for at least one of its end (rectifying and / or inverting).

Another concern associated with the cascaded H-bridge topology is its high switch number, especially at a large number of modules cascaded. It would therefore be attractive to reduce the semiconductor usage, if the performance is not compromised to any noticeable extent. Meeting this expectation would be to replace the standard eight-switch module in Fig. 6-2(a) with the six-switch module shown in Fig. 6-2(b), whose rectifying and inverting stages are now not distinctly separated. The saving in semiconductor is thus 25% per module, which can be sizable, if a long stream of modules is cascaded. This new topology in Fig. 6-2(b) is derived from the nine-switch inverter. Different from the nine-switch inverter, each phase in Fig. 6-2(b) consists of two legs, with each leg formed by tying three switching devices in series. The eventual generalized cascading configuration is given in Fig. 6-2(c) with the module block replaced by the Fig. 6-2(b). It is also advisable to mention that the nine-switch inverter has been used as an UPS in [46], but without considering its control issues related to non-ideal supply and loads. However, the non-ideal conditions are tested for the proposed UPS configuration.

Fig. 6-2 Illustration of the (a) eights-switch module, (b) six-switch module, (c) generalized cascading concept

Taking Fig. 6-2(b) for explanation, its two sets of outputs are grouped as {AC1+, AC1-} and {AC2+, AC2-}. The principles to generate the gating signals for each leg in Fig. 6-2(b) are consistent with those for nine-switch inverter, which are detailed in chapter 3. An example of references arrangement is given in Fig. 6-3, where the peak of upper reference and the trough of lower references are shifted to upper and lower carrier bounds by adding offsets d_1 and d_2 , respectively. Gating signals thus generated for showing the absence of the forbidden switching state is shown at the bottom of Fig. 6-3(a). The same would apply to the other phase-leg, in addition to the usual H-bridge modulating principle, which is to use two 180° phase-shifted references to control its two phase-legs. The resulted references arrangement for the second phase-leg are then shown in Fig. 6-3(b), where its upper and lower references are the negation of their correspondences in Fig. 6-3(a). The upper reference is for controlling the upper terminal AC1- of the second phase-leg while the lower reference is for its lower terminal AC2-. Following these principles, the resulting reference between AC1+ and

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Fig. 6-3 An example of the references arrangement per phase for the derived topology

AC1- would then be the subtraction of just two 180° phase-shifted references as intended, since the upward shifted offsets for the phase-legs are similar, and would cancel each other. The same reasoning would apply to the two terminals AC2+ and AC2- as well, hence demonstrating that the basic H-bridge modulation principles are met, while yet fulfilling the constraints faced by each phase-leg. In addition, It's advisable to mention that the optimized modulation schemes proposed in the chapter 3 are also applicable to the derived topology here. For the cascaded configuration in Fig. 6-2(c), as per its H-bridge cascaded multilevel precedence, modulation carriers used for the N modules would be phase-shifted by $180^\circ/N$, in order to achieve harmonic cancellation [62].

For the UPS, the two sets of terminals operate at the common frequencies (CF) mode. Therefore, phase-shift limitation may become a concern for the proposed online UPS. For example, if the two references are largely displaced in phase angle, their maximum index will decrease accordingly to avoid crossover. Consequently, the dc voltage has

to increase to compensate for such effect, resulting in a higher rating of the semiconductors and dc devices needed. Obviously, the dc voltage could be doubled at the worst case when two references are 180° displaced. Undoubtedly, the requirement of higher dc voltage will increase the overall cost and therefore overshadow the component-saving merit brought by proposed six-switch module. To check on whether online UPS requires two largely displaced references or not, Fig. 6-1 is referred to again, where attention is now placed on the bypass switch. This switch is normally off, and will only be turned on when the UPS needs to be isolated for maintenance, repair or other reasons. For the turning on process to be fast and safe, voltage at both ends of the switch must be the same, which then means that the voltage references for the input and output of an online UPS are relatively close. More specifically, the output reference should be controlled to lead by a small amount to the input reference, in order to compensate the voltage drop along the filter inductances at both sides of terminal. If assuming that both input and output power factors are unity, the leading angle is then mainly decided by the filter inductances. If both filter inductances are 0.1 per unit, the output reference will lead the input reference approximately by 11.42° under the rated operating condition, which translates into an increase in dc voltage by up to 10% [46]. Fortunately, this slight increase in dc voltage is less likely to be a problem for online UPS and can actually be compensated with added triplen in the modulation, which is exclusively developed for the six-switch module to increase the maximum modulation index without breaching any operating constraint. The simplified six-switch module with 25% saving in semiconductor is therefore an uncompromised alternative for consideration, and can certainly be cascaded to form the proposed multilevel UPS topology shown in Fig. 6-2(c) with modules in series per phase.

6.3 Per-Unit Comparison

Now a qualitative justification for using the six-switch module as an online UPS application is done. The justification is extended to perform a numerical analysis on the component ratings of the eight-switch and six-switch module online UPS. For simplification, the following analysis assumes the online UPS is assembled using one

module per phase ($N=1$) and in the same way, the analysis is also applicable for high-level cascaded online UPS ($N \geq 2$).

6.3.1 Eight-Switch Module

For the eight-switch module, the input and output converter can operate independently, and hence there is no need to divide the carrier band into two sections. In this way, the dc-link voltage can be set to the minimum of $V_{dc-ES} = \sqrt{2}/1.15$ p.u. (subscript ES denotes “eight-switch”), if the nominal RMS grid voltage is chosen as a base value. Voltage ratings of the dc capacitor, semiconductors in both converters would therefore have to be set above this value, with some safety margin added. Current ratings of the semiconductors of the input converter have to be higher than 1 p.u., with safety margin considered, if the sinusoidal RMS load current is set as base and the input converter is under unity power factor control. In reality, this current rating has to be higher if the charging current flowing into energy storage device at dc side is considered. For semiconductors in output converter, given the nonlinear loads at end, current rating has to be higher than $(1+k)$ p.u. with safety margin added. The term k represents the amount of current polluted by the harmonic and reactive components in the load current.

6.3.2 Six-Switch Module

As discussed in section 6.2, for six-switch module, the output reference has to lead by a small amount to the input reference to compensate for the voltage drops along the filter inductances. Therefore the dc-link voltage has to be slightly higher than the minimum of $\sqrt{2}/1.15$ p.u and based on the assumption in section 6.2, it is reasonable to set the displacement angle at 15° with some margin added, which gives a 13% increase to the minimum dc-link voltage. Thus, the voltage ratings of the dc capacitor and semiconductors have to be chosen based on $V_{dc-SS} = 1.13 \times V_{dc-ES}$, where the subscript SS denotes “six-switch”.

For the current rating, the analysis for the six-switch module is a little different. Focusing first at the upper S_I switch in Fig. 6-2(b), the current flowing is either I_{acI}

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Table 6-1 Maximum P. U. voltage and current handled by the switches in each module

Eight-Switch Module	Voltage	Current		Mean	
		Input switch	Output switch		
	$\sqrt{2}/1.15$	1	$1+k$	$(2+k)/4$	
Six-switch Module	Voltage	Current			Mean
		Upper switch	Middle switch	Lower switch	
	$1.13 \times \sqrt{2}/1.15$	k	$1+k$	k	$(1+3k)/3$

when S_1 and S_3 are ON, or $(I_{ac1}+I_{ac2})$ when S_1 and S_2 are ON, assuming that both I_{ac1} and I_{ac2} are indicated as flowing out of the converter. If consider it a little more, I_{ac1} in the second term should be negative because it is essentially a rectifier, while I_{ac2} is positively transferring energy to the load. According to subsection 6.3.1, the current ratings of the upper switch S_1 would be $I_{ac1}+I_{ac2} = -1+1+k = k$ p.u.. Obviously, the S_3 would experience the same scenarios as S_1 . The current flowing through S_2 is either I_{ac1} when S_2 and S_3 are ON, or I_{ac2} when S_1 and S_2 are ON. Thus, the current rating of the middle switch S_2 would be based on $(1+k)$ p.u. Not difficult to understand, the semiconductors in the second leg per phase would have the same scenarios.

6.3.3 Comparison

Based on the analysis, the maximum p.u. voltage and current handled by the switches in both modules are listed in the Table 6-1. Due to the small phase displacement between two references, the maximum voltage experienced by switches in six-switch module is slightly higher, but this increase is not dominated as it is in [18][19]. The maximum current handled by every switch is different, Table 6-1 averages the current over switches for each module. Clearly, for both modules, the overall current rating goes up in respect to k . When $k \leq 23\%$, the six-switch module has smaller current ratings compared to the eight-switch module. This situation is opposite when $k \geq 23\%$.

6.4 Control Formulation

The control objective defined for the proposed online UPS is to always maintain a constant sinusoidal output voltage and sinusoidal input current, regardless of the extent of unbalance and distortion detected in the line input and loads, even when less

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semiconductor count is used. With the objective in view, suitable control schemes are developed for each terminal to optimize the performance.

6.4.1 Output Control Principles

Fig. 6-4 Control diagram for proposed cascaded online UPS

Fig. 6-4 is shown that the an output reference voltage phase $V_{o,abc}^*$ is deduced from a set of sinusoidal waveforms synchronized with the input line (see also labels used in Fig. 6-2(c)).

Tracking of this voltage is ensured by using a combination of a proportional-resonant (PR) controller and selective harmonic eliminator (SHE), whose expressions can be written as:

$$G_{PR}(s) = K_P + \frac{K_RS}{s^2 + \omega_c s + \omega_1^2} \quad (6.1)$$

$$G_{SHE}(s) = \sum \frac{K_{Rx}s}{s^2 + \omega_{cx}s + \omega_x^2}; x = 5, 7, 11 \text{ and } 13 \quad (6.2)$$

where K_P , K_R and K_{Rx} are the controller gains, ω_c and ω_{cx} are the cutoff frequencies, and ω_l and ω_x are the fundamental and harmonic frequencies, respectively. The proportional-resonant (PR) controller alone introduces an infinite gain at the

Fig. 6-5 Bode diagram of selective harmonic eliminator (SHE) in the output control scheme

fundamental frequency, but it is unable effectively to attenuate the low-order harmonic components in $V_{o,abc}$ coming from nonlinear loads. To illustrate that, Fig. 6-6(a) is given to show the experimental waveforms of the load voltage $V_{o,abc}$ under a diode rectifier as the load. Thanks to the PR controller, the load voltage $V_{o,abc}$ follows its references $V_{o,abc}^*$ quite well, but still contains a certain amount of low-order harmonic components, as indicated by its THD level of 5.26%. To further attenuate the components, the selective harmonic eliminator (SHE) is added as shown in Fig. 6-4.

As seen in (6.2), the selective harmonic eliminator (SHE) is realized by including multiple resonant regulators in stationary frame for eliminating those prominent low-order load voltage harmonics, including 5th, 7th, 11th and 13rd components. The illustration of SHE in Bode diagram is given in Fig. 6-5 and it is certainly verified that the eliminators introduce multiple high gain resonant peaks only at those chosen harmonic frequencies, with gains at other frequencies close to zero. Therefore, selective harmonic compensation is realizable. Fig. 6-6(b) shows the load voltage with SHE added in the control scheme under the same load condition in Fig. 6-6(a). Obviously, the harmonic components are further attenuated, as verified by a THD level of 1.02%. Before being sent to PWM block for modulation, the signal after the PR controller and SHE is added with a feed forward loop to enhance its transient performance [87].

Fig. 6-6 Load voltage without (a) and with (b) selective harmonic eliminator (SHE) added in output control scheme.

6.4.2 Input Control Principles

The output voltage and current are also multiplied and filtered by Low-pass Filter (LPF) to give the active power P_L^* demanded by the loads, which then divided by $3N$ gives the load power handled per module. This value, when added to the charging

power command P_S^* issued by the storage management system, would be the total active power P_T^* by the positive-sequence input voltage amplitude and accounting from system efficiency ζ , the desired active current amplitude is computed for generating the reference current phasor $I_{i,abc}^*$. In parallel, a PI regulator is also added to act on the dc-link voltage error, maintaining it within a safety range by generating a current command $(I_{i,abc}')^*$ synchronized with supply voltage. The sum of $I_{i,abc}^*$ and $(I_{i,abc}')^*$ is then tracked by the rectifier of each module using the same PR controller, as depicted in (6.2). In order to provide safe shutdown of the rectifying side during power outage,

the actual input voltage $|V_i|$ is sensed, and upon it is falling below a specific trip level V_{trip} , the input current command is set to zero. Simultaneously, the discharging resistor shown in Fig. 6-2(c) would be switched in to dissipate the residual input energy with the upper two switches of each module permanently kept on. Another control issue to address is the switching offline of the UPS for (e.g.) maintenance purposes during period when the input line is distorted and / or unbalanced.

The input and output references are then added with offset d_1 and d_2 , respectively to avoid crossover in PWM generation block. The d_1 and d_2 are calculated instantaneously, based on the amplitude of each modulation reference.

6.5 Experimental Results

A hardware setup was built to verify the proposed online UPS in Fig. 6-2(c) which was assembled using two modules per phase ($N=2$). The ac supply voltage and dc-link voltage across each six-switch module were set at 121V(line-to-line, RMS) and 60V, respectively. The load was assembled using a diode rectifier with a dc load of 60 Ω and 220 μ F in parallel. The online UPS was controlled using a *dSPACE ACE1006* control card and the gating signals were produced with the programmable DS5101 boards.

In Fig. 6-7(a), a voltage outage was introduced at 40ms and as intended, the output voltages were kept sinusoidal and constant throughout the illustrated duration with no noticeable transient dip even at the instant of interruption. The line current is also kept sinusoidal and in phase with the supply voltage to give a unity power factor before the outage, and was driven to zero after the outage, during which the storages took over the responsibility to meet the load demand. Fig. 6-7(a) gives the same illustrations of the reversed process, where the supply voltages were restored from an interruption from 40ms and the load demand was taken over by supply from the storages. The load voltages were still sinusoidal and constant throughout the testing duration. In both scenarios, the dc-link voltages were kept at 60V, indicating that the proposed online UPS with 25% lesser semiconductor does not require an increased dc voltage, as opposed to these existing switch-saving power applications [18][19].

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The next step was to test the performance of the online UPS under non-ideal supply and loads. In Fig. 6-8, the phase a in the supply voltage was dipped by 30% and an additional load of 60Ω was introduced between phase a and phase b of the diode rectifier to create an unbalanced and distorted load. An interruption was also introduced at 40ms in Fig. 6-8(a) and the load voltages were kept in phase with supply

(a)

(b)

Fig. 6-7 Experimental responses from (a) normal-to-interruption and (b) interruption-to-normal condition.

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voltage and maintained constant all the time even though the load was unbalanced and distorted as illustrated. Like in Fig. 6-8(b), the reversed duration was also tested and the results are given in Fig. 6-8(b), and it behaved as expected. In comparison to [46], the proposed online UPS was extended to be able to function under the unbalanced supply and loads conditions, while still maintaining a reasonable dc-link voltage.

Fig. 6-8 Experimental responses under the non-ideal supply and loads: (a) normal-to-interruption and (b) interruption-to-normal condition.

6.6 Summary

The chapter proposes an online UPS using the proposed semiconductor-reduced multilevel configuration. Its semiconductor count is hence reduced by 25%. Unlike other reduced component topologies though, no compromise in performance is experienced by the proposed UPS upon controlled appropriately, as verified through experimental testing. Advantages of the proposed UPS can therefore be broadly summarized as reduced cost, better waveform quality, higher power handling capability and improved redundancy, while still maintaining a high level of online protection for the critical loads.

Like those earlier discussed applications too, the proposed UPS does not face any significant increase in control and modulation complexities when compared with its conventional counterpart. In terms of voltage rating, Section 6.3 has also proven that a minimum of 13% increase in dc-link voltage is needed to cater for the usual phase-shift found between the two UPS's references. This can easily be met in reality for UPS whose two references are usually set to have high modulation ratios ranging from 0.8 to 0.9. The intention is to avoid poor dc-link utilization, while yet providing a safe margin to avoid over-modulation, regardless of whether a reduced or non-reduced topology is used. The level of dc-link voltage demanded by both options is thus roughly the same with no expected increase in switching losses especially when their switch currents are also kept the same for most common load power factor. The proposed UPS is thus an attractive alternative if lesser switches are preferred.

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This chapter continues with the findings presented in Chapter 6 by evaluating a second application for the proposed six-switch module with three-level phase switching characteristics. The system investigated is an interline DVR, which uses three six-switch modules to form a three-phase voltage restorer for protecting two independent ac grids. Voltage restoration of the grids is however constrained by the tighter reduced-switch operating range under ideal and non-ideal supply-load operating conditions. These constraints can better be managed through understanding the system, which is the theme of this chapter.

7.1 Introduction

Voltage sags are one of the most severe power-quality issues that can cause substantial damage to consumers with critical loads [89]. These disturbances are usually caused by faults, load variations and energizing of large loads. Custom power solution is a range of technology-driven products to provide power-quality enhancement. Among these custom power products, dynamic voltage restorer (DVR) [90] is the most advanced and economically accepted devices for voltage sag mitigation in distribution system. The DVR is usually series-connected at the upstream of where an industrial factory or a group of sensitive loads is supplied by distribution feeder. The DVR functions against voltage sags by injecting a set of compensating voltages in series with supply voltage.

The operation of dynamic voltage restorer requires both active and reactive power injection into distribution feeder. The reactive power can be easily generated within the voltage source inverter of DVR while the active power injection can be met with external energy storage devices, such as battery, flywheel or super capacitor [90]. Therefore, the amount of real power that can be transferred to sensitive load is a decisive factor for DVR compensation capability, especially for long-term, deep

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voltage sags. A couple of energy optimization techniques were then proposed to minimize the real power injection from DVR, as described in [91]. However, these techniques are less effective under certain scenarios, such as deep and/or long-term sags. The interline dynamic voltage restorer (IDVR) concept connects two or more DVRs to a common dc-link, enabling the dc-link to be dynamically replenished and therefore removing the necessity of installing bulky energy storage devices [92][93].

However, having multiple voltage source inverters (VSI) grouped together, the IDVR structure employs a large number of semiconductor switches, making it rather costly and complicated. In order to improve this aspect, the chapter uses the derived six-switch configuration for IDVR system, using 25% lesser switching devices, and minimizes the compromise in performance through proper design.

A high-level voltage control scheme, including forward and feedback loops, is incorporated with the proposed structure to achieve optimal tracking performance. In addition, reference voltage generator is respectively developed for sag compensation and power flow control functionality, along with the high-level voltage tracking scheme, enabling the whole system fast response to various transient scenarios and re-stabilize at steady-state point. Last, hardware results are given as verification.

7.2 Operating Principles of IDVR System

Fig. 7-1 Representation of interline dynamic voltage restorer (IDVR) structure with 'n' inverters

Fig. 7-1 represents an interline dynamic voltage restorer (IDVR) configuration with n inverters connecting to a common dc link. All the feeders in Fig. 7-1 are assumed to be

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Fig. 7-2 Representation of the derived topology with 25% lesser switching device count

supplied from electrically independent grid substations and therefore voltage sag appearing in a feeder has no impact on any other feeders. When one of the DVRs in Fig. 7-1 compensates for the voltage sag by transferring active power from dc-link, the rest DVRs dynamically replenish dc-link and maintain V_{dc} at a specific level [92][93]. A number of VSI topologies are available to replace the inverter block in Fig. 7-1, but most always, H-bridge is commonly preferred per phase in order to mitigate various types of voltage sags [56]. In this way, for three-phase system, a total of twelve switching devices, or three H-bridges are needed in each inverter block in Fig. 7-1. A typical concern raised with H-bridge per phase based IDVR configuration is its high semiconductor count, which makes the overall system rather complicated and unreliable, particularly with a large number of n .

Thus, it would be attractive to reduce the semiconductor usage, while performance is not compromised to a noticeable extent. Meeting this expectation would be to merge Inverter block 1 and 2 in Fig. 7-1 into new topology shown in Fig. 7-2, which reduces switching counts by 25%. This topology has already been introduced in chapter 6. As shown in Fig. 7-2, two sets of output are not distinctly separated as in Fig. 7-1, where inverter blocks are fully decoupled by dc-link. The 25% saving in component count is sizable, particularly if a large number of feeders are involved.

The principles to generate the gating signals for each phase in Fig. 7-2 have already been explained in chapter 6, which will not be repeated here again. For IDVR, operating under the modified H-bridge modulation principles results in a prime

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concern in the proposed IDVR structure. As pictured in Fig. 6-3, the maximum magnitudes of two references within the common carrier band are determined by their phase displacement angle θ . When two references are in phase, the maximum modulation ratio for both can reach unity. With the increase in the phase-shift between two references, the maximum modulation index for both starts to reduce until hitting its lowest value of 0.5 when two references are 180° phase shifted. As a result, to be able to generate the same output voltage, the dc-link voltage has to increase accordingly as the maximum modulation index decreases. This increase in dc-link voltage, which is obviously unfavorable, would overstress dc bus and switching devices, hence if possible, should be minimized through proper design. However, because of uncontrollable and unpredictable nature of feeders within an IDVR structure, it is always necessary to prepare enough space for both references to vary in horizontal direction, thus incurring a relatively high increase in dc-link voltage. A reduction in this increased dc-link voltage is possible only at the expense of compromised voltage sag compensation range and capability. In the following section, a thorough analysis on the relation of minimum dc-link voltage and voltage sag compensation capability is presented.

7.3 Analysis of the Proposed IDVR Configuration

For the sake of illustration, an IDVR system having two independent feeders is pictured in Fig. 7-3, in which the supply voltages, V_{s1} and V_{s2} , are assumed same in magnitude and their phase displacement angle is indicated by α . Many practical power flow studies show that α seldom exceeds 10° between any two feeders, provided the transmission line length between them is not more than a few hundred kilometers. Since the feeders within an IDVR system are commonly geologically close to each other, it is reasonable to assume in the following analysis that the phase displacement

Fig. 7-3 Representation of an IDVR system with two independent feeders

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Fig. 7-4 maximum magnitude of (a) angle γ and (b) V_{dvr2} with respect to the power factor $\cos\Phi$ varying from 0.6 to 0.8.

angle α between any two feeders are less than 10° , or $|\alpha| < 10^\circ$.

Another important issue which also requires careful consideration is the possible ranges for phase shift values in supply voltage during voltage sag. Phase shift are different under different fault types, and according to [84], 95% of recorded voltage sags of various types have a phase shift of less than $\pm 20^\circ$. In the following analysis, the phase shift value in supply voltage during voltage sag is denoted by θ , and assumed, $|\theta| < 20^\circ$.

In Fig. 7-3, feeder 1 is assumed as a faulty feeder while feeder 2 is considered healthy and transfers power to dc-link when sag appears in feeder 1. For simplicity, only balanced voltage variations are considered and its corresponding analysis can be extended to other types of voltage variations. For voltage sag, the in-phase compensation technique is adopted to compensate for voltage sag, which means that load voltage V_{L1} is always kept in phase with V_{s1} [92][93]. In this way, V_{dvr1} will also be in phase with V_{s1} . Line impedances are neglected in both feeders to result in a more comprehensive investigation without introducing significant error. The analysis is performed in a per-unit basis, with the *rated* load voltage / supply voltage as the base voltage. The phase angle of V_{s1} at normal condition is assumed as zero.

To define the extent of the voltage sag, voltage sag factor a is introduced as:

$$a = \frac{V_{s1}}{V_{L1, rated}} = \frac{V_{s1}}{1} = V_{s1} \text{ (p.u.)} \quad (7.1)$$

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Fig. 7-5 Minimum V_{dc} and maximum modulation ratio m_{max} versus displacement angle ε

In the practical power system, power factor $\cos\Phi$ usually ranges from 0.6 to 0.8. In addition, according to the power flow theory proposed in [92][93], the DVR 2 absorbs real power from feeder 2 by advancing the load voltage V_{l2} to V_{s2} by a phase angle β . The maximum power transfer can be attained when this advance angle β equals power factor angle Φ [92][93]. At the meantime, despite the advance angle β , V_{l2} must be controlled to be same with V_{s2} in magnitude to avoid disturbing normal operation of load in feeder 2. In this way, when sag appears in feeder 1, the injection voltage should be $\bar{V}_{dvr2} = \bar{V}_{s2} - \bar{V}_{l2}$, and thus V_{dvr2} is lagged from V_{s2} by angle γ . The actual magnitude of V_{dvr2} and angle γ is determined by the amount of real power needed for replenishing the dc-link, but their maximum values are limited by the power factor $\cos\Phi$. Fig. 7-4 shows the maximum magnitude of angle γ and V_{dvr2} with respect to the power factor $\cos\Phi$ varying from 0.6 to 0.8. Clearly, if feeder 2, with a power factor of 0.8, transfers the maximum real power to dc-link, V_{dvr2} would be lagged from V_{s2} by maximum angle γ of 71.56°. Fig. 7-4(b) shows that with $\cos\Phi$ from 0.6 to 0.8, the magnitude of V_{dvr2} is always below 0.9 p.u.

To summarize, in order to cover common voltage sag scenarios, it is necessary to prepare enough space within carrier band for two modulating references' variation in horizontal direction. According to above discussion, depending on various scenarios, the phase shift between two modulating references at power factor $\cos\Phi$ of 0.8 should range within:

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$$|\alpha|+|\beta|+|\gamma|\leq 10^\circ+20^\circ+71.56^\circ\approx 101^\circ \quad (7.2)$$

According to Fig. 7-4(a), with decrease in $\cos\Phi$, the phase shift between modulating references would be always within above range. Therefore, setting 101° maximum possible phase shift between two modulating references is enough to cover all the common voltage sag conditions. However, this phase shift margin between two references reduces their maximum modulation ratios, causing an increased dc voltage in order to maintain same output levels. Since all the feeders within an IDVR structure are equally subject to voltage sags, it is desirable that maximum modulation ratios for both references are kept same all the time. In this way, the minimum dc voltage V_{dmin} with respect to modulating references displacement angle ε should be:

$$V_{dmin}=1+\sin(\varepsilon/2) \text{ (p.u)} \quad (7.3)$$

Fig. 7-5 depicts the maximum modulation ratio m_{max} and minimum dc voltage V_{dmin} in relation with displacement angle ε , with ε varying from 0° to 180° . It clearly shows that dc voltage would increase to 1.77 p.u. at $\varepsilon=101^\circ$, caused by a reduction in maximum modulating ratios to 0.56. When two references are 180° shifted, the dc voltage would be doubled and maximum modulating ratio is 0.5. At this condition, the carrier band is actually equally divided for two references, which provides full flexibility for two references to vary in horizontal directions at the cost of a double dc voltage.

Above discussion shows a 101° phase margin between two references are enough for proposed IDVR structure to cover almost all the common voltage sag scenarios, based on published practical statistics on voltage variations in power system [84]. This phase margin however increases dc voltage by 77% if the IDVR is designed to be able to compensate for a 100% dip in supply voltage, i.e. voltage sag factor $\alpha=0$. However, for the system whose cost is the dominant in the design process, the increase in dc voltage might be reduced further, but, at the expense of a compromised compensation capability. For example, as depicted in Fig. 7-5, a smaller modulation displacement angle ε causes a smaller increase in dc voltage, but it also means that certain voltage sag scenarios would not be able to be compensated properly. Or, the dc voltage could

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be maintained low simply by sacrificing the IDVR's ability to compensate for some sags with small a .

7.4 Control Scheme

Fig. 7-6 Representation of the output voltage regulation control scheme

A high level control scheme is used to regulate the output voltage to follow its reference, as shown in Fig. 7-6. The scheme is noted to have two degrees of control freedom with the first primary degree formed by subtracting supply voltage from demanded load voltage to give $\vec{V}_{load}^* - \vec{V}_{supply}$. Feed forwards path is however not capable of compensating for voltage drops appearing across the filter and transformer. Because of that, a secondary feedback loop is added to act on the load voltage error, derived by subtracting measured load voltage from its reference $\vec{V}_{load}^* - \vec{V}_{load}$. The computed error then is fed into a P+Resonance controller in stationary frame to force its zero-state error to be zero, and hence can compensate for those unaccounted voltage drops appearing across the inductive elements [56]. In addition, the control scheme can further incorporate a separate loop to prevent any harmonic component in supply voltage from propagating to load side. For a feed subject to voltage sag, the load voltage reference is set in phase with supply voltage but at rated magnitude value. The load voltage reference for terminal in power flow mode is generated in the same way as proposed in [92][93].

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7.5 Experimental Results

Fig. 7-7 Representation of the hardware setup for two-line IDVR structure with system specifications

For verification, a laboratory prototype of two-line IDVR structure has been constructed as depicted in Fig. 7-7 with the implementation of the control schemes. The specifications used for hardware setup are illustrated in Fig. 7-7 as well. Two feeder sources in Fig. 7-7 are emulated by two three-phase AC programmable power sources which supply power to two R - L load of same rating and power factor of approximate 0.8. The transformer ratio between proposed inverter and feeders are adjusted at 1:1 for both feeders. Implementation of control algorithms is completed by dSPACE 1006 controller board which sends the 12-channel shifted modulating references through a Lattice LC4128V chip for XOR logical operation and then the gating signals are generated through a driver board before going to act on IGBT switches.

Consistent with above description, a 20% three-phase balanced sag is emulated in feeder 1 from 1s, as shown by left V_{grid1} in Fig. 7-8(a). The compensated load voltage in left V_{load1} is accurately maintained at its rated value from 1s onward. It is noted that in the initial instant after 1s, the power needed for compensation is first taken from dc-link, which is illustrated by a voltage drop starting from 1s in right V_{dc} in Fig. 7-8(b). After the power is replenished progressively from feeder 2, the dc-link voltage is going back to its set point as well. In addition, the bottom plot in left half plate of Fig. 7-8 indicates the grid voltage and load voltage in feeder 2 before and after the sag appears.

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Fig. 7-8 Experimental responses from (a) normal-to-interruption and (b) interruption-to-normal condition

Before 1s, the grid voltage V_{grid2} and load voltage V_{load2} is almost in phase and identical in magnitude. From 1s, V_{load2} is progressively advancing the V_{grid2} to pump power from feeder 2 to replenish the dc voltage which is being depleted by ongoing sag compensation in feeder 1. Contrarily, Fig. 7-8(b) illustrates the inverse process in which the supply voltage V_{grid1} is restored from 20% three-phase balanced voltage sag to rated value from 1s. Fig. 7-8 clearly shows that the control algorithms provide fast dynamic performances. In addition, it can be seen that the dc-link voltage is approximately 1.7 times higher, which is considered the worst case for proposed structure. Of course, the dc voltage can be further reduced at an expense of certain compromise for its compensation capability.

7.6 Summary

This chapter continues with the findings proposed in Chapter 6 by evaluating a second application for the proposed six-switch module with three-level phase switching characteristics. The investigated system here is IDVR, which uses three six-switch modules to form a three-phase voltage restorer for protecting two independent ac feeders. Although shared performance trade-offs exist, they can be effectively minimized through appropriate design and modulation. There are therefore advantages demonstrated by the reduced-switch IDVR, which can be summarized as reduced semiconductor count, better compensation quality, and higher power handling, while

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yet maintaining a high level of protection to the critical loads. These findings have already been tested with an experimental prototype.

Chapter 8 Conclusions and Recommendations

8.1 Conclusions

The thesis begins by reviewing existing reduced component topologies for ac-ac energy conversion. They include the “all-semiconductor” matrix converters, whose attractiveness is not strong because of their number of switches, complexity in control, and lack of harmonic and unbalance compensation. They are therefore not the focus of the thesis. Review is next done for the four-leg, five-leg and nine-switch converters, which in common save some switches but face some tradeoffs. Knowledge on four-leg and five-leg converters would generally be not too complex since they use the same two-switch phase-leg. Nine-switch converter, on the other hand, is newer, and uses a more unique three-switch phase-leg to form two ac terminals. These two terminals are however not fully independent, whose side effects are limited phase-shift and doubled dc-link voltage experienced by existing applications of the nine-switch converter. These limitations are however application-related, which means they can be removed or diluted if the correct energy systems are identified for application. This is the challenge clarified in the thesis with the help of an example UPQC system.

A UPQC, in general, is a “series-shunt” system with one set of ac terminals tied in series with the grid and the other in shunt. It is unlike existing ac-ac motor drive and rectifier-inverter applications of the nine-switch converter, where both terminal sets are tied in shunt, and hence refer to as “shunt-shunt” systems. Through studies, it is clarified that the nine-switch converter is not suitable for “shunt-shunt” systems, where tradeoffs can easily overshadow the saving in semiconductors. Instead, the nine-switch converter should be used with “series-shunt” systems, where impacts from tradeoffs can more easily be neutralized or diluted. This claim has already been verified by an appropriately controlled UPQC, whose commutation count can further be reduced by 33% when controlled by the newly designed 120°-discontinuous modulation scheme. Alternatively, the designed continuous modulation scheme with better spectral performance can be used instead.

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The knowledge created is not just applicable to ac-ac conversion systems with an intermediate dc-link. It can in fact be used to merge multiple ac and dc sources, storages and loads together to form various integrated energy systems. Control and implementation of two example integrated systems have already been demonstrated to show their feasibility in either single- or three-phase form. Although interesting, these generalized integrated systems still use the nine-switch converter with two-level terminal voltage switching. The next challenge is thus to develop a new reduced-switch cascaded multilevel converter, whose semiconductor saving is still 25% as compared to a normal back-to-back cascaded converter. Attractiveness of this saving is again application-related because of the accompanied tradeoffs. It is therefore important to recommend a few prospective applications for the reduced-switch cascaded converter. For that, an online UPS and an interline DVR have been tested with appropriate control schemes recommended for them to ride through voltage dips and other non-ideal supply-load conditions.

To conclude, this thesis presents a rich study of the nine-switch converter with many prospective energy conversion systems explained and a topological extension recommended. All systems explained have already had their practicality verified in experiments.

8.2 Recommendations for Future Research

This research has contributed to the better understanding of the nine-switch converter and its related applications. The findings are however not exhaustive with many future challenges available for investigation. Some of them are discussed below.

- Chapter 5 presents a few integrated energy systems studied and controlled as individual entities. Multiple copies of the integrated systems distributed to the grid have not been tried. Relevant control and management issues are interesting, but yet to be explored.
- Chapter 6 presents a reduced semiconductor cascaded converter tested as an online UPS. Each module has its own dc source, which is fine for a UPS. In

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cases where dc capacitors are used instead, relevant control schemes have to be studied, which again is an area for investigation.

- Interline DVR has been studied in Chapter 7. Its ability to compensate for other power quality concerns without incurring heavy tradeoffs can be a nice knowledge to learn.
- All chapters in the thesis have considered single-phase and three-phase systems. Although it is clarified in Chapter 5 that the concept can be generalized to more phases, a real multi-phase example has not been explicitly considered. There might thus be issues related to multi-phase systems that need further consideration.

Author's Publications

Premium Journal Publications

- [1] Feng Gao; **Lei Zhang**; Ding Li; Poh Chiang Loh; Yi Tang; Houlei Gao; , "Optimal Pulsewidth Modulation of Nine-Switch Converter," *Power Electronics, IEEE Transactions on* , vol.25, no.9, pp.2331-2343, Sept. 2010.
- [2] **Lei Zhang**; Poh Chiang Loh; Feng Gao; , "An Integrated Nine-Switch Power Conditioner for Power Quality Enhancement and Voltage Sag Mitigation," *Power Electronics, IEEE Transactions on* , vol.27, no.3, pp.1177-1190, March 2012.
- [3] Poh Chiang Loh; **Lei Zhang**; Feng Gao;, "Compact Integrated Energy Systems for Distributed Generation," *Industrial Electronics, IEEE Transactions on (early access)*.

Premium Conference Publications

- [1] Feng Gao; **Lei Zhang**; Ding Li; Poh Chiang Loh; Yi Tang; , "Optimal pulsewidth modulation of nine-switch inverter," *Power Electronics and Drive Systems, International Conference on*, pp.718-723, 2-5 Nov. 2009.
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