Electrical properties and memory applications of Al-rich Al-based dielectric thin films

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ELECTRICAL PROPERTIES AND MEMORY APPLICATIONS OF AL-RICH AL-BASED DIELECTRIC THIN FILMS

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This thesis is dedicated to my parents.

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Summary

Summary

An *Al*-rich Al_2O_3 thin film was deposited on a p-type silicon substrate by rf sputtering to form *Al/Al*-rich Al_2O_3 /p-Si diodes. The current–voltage (I – V) characteristics of the diodes were determined by carrier injection from either the Si substrate or the *Al* gate and by carrier transport along the tunneling paths formed by *Al* nanocrystals distributed in the oxide layer. The reverse I – V characteristics were greatly affected by the charge trapping in the oxide layer, i.e., the electron trapping significantly reduced the reverse current while the hole trapping enhanced the current significantly. However, the charge trapping did not produce a large change in the forward I – V characteristic.

A write-once-read-many memory (WORM) device was realized based on the charging-controlled modulation in the current conduction of *Al/Al*-rich Al_2O_3 /p-Si diode. A large increase in the reverse current of the diode could be achieved with a negative charging voltage, e.g., charging at –25 V for 1 ms resulted in a current increase by about four orders. Memory states of the WORM device could be altered by changing the current conduction with charge trapping in the *Al*-rich Al_2O_3 layer. The memory exhibited good reading endurance and retention characteristics.

Metal-insulator-metal (MIM) structure was fabricated by partially anodizing aluminum film followed by deposition of another aluminum film. Unipolar resistive switching between a high-resistance state and a low-resistance state with a high resistance ratio ($>\sim 10^4$) was observed from the structure. The switching occurred without the requirement of a forming process, which was attributed to the pre-existing conductive filaments in the *Al*-rich Al_xO_y layer formed by the anodization. Each resistance state exhibited ohmic behavior which could be explained by the

Summary

metallic conduction and electron hopping from one isolated state to the next in the *Al*-rich Al_xO_y layer. The MIM structure showed good memory characteristics.

AlO_xN_y dielectric thin films have been synthesized with rf sputtering of *Al* target in the presence of a mixture of oxygen and nitrogen. The electrical properties of the MIM and MIS structures based on the AlO_xN_y dielectric thin films have been studied. It was observed that the MIM structure showed multiple resistive switching. The resistive switching strongly depended on the oxygen concentration, and it did not occur if the oxygen concentration was very low, highlighting the important role of oxygen. On the other hand, the current conduction in the MIS structure was found to be affected by the charge trapping in the dielectric films.

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Chapter 1 Introduction

This thesis presents the studies of electrical properties and memory device applications of *Al*-rich *Al*-based dielectric (Al_2O_3 and AlO_xN_y) thin films. The *Al*-rich *Al*-based dielectric thin films have been synthesized with either reactive sputtering or anodization process, forming metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) structures. Electrical properties of these devices, including current transport, charging effect, conduction modulation/conduction switching, and memristive behaviors of the *Al*-rich *Al*-based dielectric thin films have been investigated. The memory applications including Write-Once-Read-many (WORM) memory and resistive switching memory have been demonstrated based on the *Al*-rich *Al*-based dielectric thin films. Memory performance and reliability of the memory devices which are important in real applications also examined. This chapter will introduce the background, motivation, objective and major contributions of this thesis. Details of this study will be presented in the following chapters.

1.1 Background and motivation

1.1.1 Non-volatile memory devices

There are various types of nonvolatile memories (NVMs) such as flash memory, ferro-electric random access memory (FeRAM), magnetic random access memory

Chapter 1: Introduction

(MRAM), phase change memory, etc.. Flash memory was first reported in 1984 by Fujio Masuoka, *et al* from Toshiba [1]. Now it is the prevailing memory segment, which allows data to be stored and erased with a single action, i.e., a flash, by means of electrical pulse. Flash memory takes the advantages of highest chip density, multi-bit per cell capability and full compatibility with CMOS technology. A popular design of flash memory is the floating gate structure, in which the charge is stored in a metal or semiconductor layer (i.e., the floating gate) that is surrounded by a dielectric material, such as SiO₂. The floating gate structure was first proposed by D. Kahng and S. M. Sze in 1967 [2].

As a conventional continuous floating gate memory device must have a thick tunnel oxide (e.g., 8 nm) to prevent charge loss, a higher programming/erasing voltage and a longer programming/erasing time are expected. The requirements on device performance and reliability issues have limited the scalability of the flash memory device. Conventional floating gate technology scaling is expected to face the technical and physical limit in the near future. In order to overcome this problem, new memory structures and new materials, such as nanocrystal floating gate memory device, resistive memory device, etc., have been proposed in recent years.

S. Tiwari, *et al* first proposed a nanocrystal floating gate memory device in 1996 [3]. It is one of possible methods for overcoming scaling limitation of conventional flash memory device by employing a nanocrystal floating gate. Since each nanocrystal is electrically and physically separated in the gate stack, the leakage path formed by defects in the tunnel oxide may only cause the charge loss of single/few nanocrystals, maintaining the stored charges in the rest of the other nanocrystals. In contrast, in a

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conventional floating gate memory device, a single defect in the tunnel oxide can cause loss of all charges stored in the continuous floating gate.

NVMs based on silicon nanocrystal (nc-*Si*), which were first introduced in early 90s [5,6], are promising candidate to overcome the above mentioned limitations and to continue the scaling of NVM devices. In a nanocrystal-based NVM device, the continuous floating gate polycrystalline-silicon layer, but instead on a layer of discrete, mutually isolated, crystalline *Si* nanocrystals or “dots” [3-7]. As compared to conventional floating gate NVM devices, nanocrystal-based NVM devices offer several advantages. First, nanocrystal-based NVM devices provide the possibility to reduce the thickness of the tunnel oxides without sacrificing non-volatility. Reducing the tunnel oxide thickness is the key to lowering operating voltages and/or increasing operating speeds. Secondly, nanocrystal-based NVMs use a more simplified fabrication process as compared to conventional floating gate NMVs by avoiding the fabrication complications and costs of a dual-poly process. Further, due to the absence of drain to floating gate coupling, nanocrystal-based NVMs suffer less from drain-induced barrier lowering (DIBL) and therefore have intrinsically better punchthrough characteristics [3]. On the other hand, the nanocrystals with sub-5 nm dot diameter offer the possibility of single-electron memory devices operating at room temperature [8].

1.1.2 Dielectric materials for non-volatile memory device applications

It is well known that the scaling merit of flash memory will enable it to be the main player in the nonvolatile memory technology because of its potential high density data storage applications. As the density of transistors increases on a chip, the dimensions of

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MOSFET decrease drastically to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). Following the scaling rule, it is known that the channel length, gate oxide thickness and depletion width must be simultaneously reduced to keep device performance. However, gate oxide thickness reduction will introduce an exponential increase of gate leakage current. To decrease the gate leakage current and increase the gate capacitance, high dielectric constant (high- k) materials have been explored to replace the conventional SiO_2 as the gate dielectric. High gate capacitance or low equivalent oxide thickness (EOT) together with low gate leakage current is desired for high- k gate dielectrics.

The Al -based dielectric thin film (Al_2O_3 and AlO_xN_y) should be worthy to investigate as potential candidate to meet such scaling requirements. Al_2O_3 is a potential high- k material. It has the merits of similar bandgap and band alignment with SiO_2 , a dielectric constant of about 10, the heat of formation of 399 Kcal/mol, crystallization temperature higher than 900 °C [9-11] and negligible oxygen diffusivity. Many attempts have been made to keep high- k materials amorphous even after high-temperature post deposition annealing, in order to suppress the surface roughness formation and the grain boundary induced leakage current [12]. Al_2O_3 deposited by sputtering is thermally stable and mechanically hard [13-15] and simulation results indicate that sputtered Al_2O_3 may be useful in the gates of flash memory circuits. Its higher dielectric constant enhances the capacitance coupling and therefore improves the circuit speed by three orders of magnitude in comparison with the SiO_2 circuit [16].

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Except for NVM, the nc-based dielectric thin films can be used in write-once-read-many (WORM) memory devices also. WORM memories are used for permanent data storage and non-editable databases with their advantages of low-power consumption, high-density storage, high flexibility, simple structure, and low cost are desirable with the rapid development of portable storage market, such as wireless RFID tags, smart cards, and personal data storage. Some kinds of materials have been widely studied for WORM memory applications [17-19]. One of their working mechanisms is also based on the resistive switching as described in ReRAM. However, once the memory is switched from one resistance state to another resistance state, normally the device cannot be reset and only reading operations are applicable. The device showed electrical bistability in its current-voltage characteristics. A WORM device based on AlN thin film containing Al nanocrystals (nc- Al), which is compatible with the silicon CMOS technology, has been demonstrated [20].

Beside the WORM device, it has been shown in recent years that resistive random access memory (ReRAM) based on an insulating layer such as a transition metal oxide in a metal-isolator-metal (MIM) structure has good potential to serve as a possible replacement for conventional floating gate memory due to its simple structure, low operation voltages, simple sensing circuits, low power consumption, and especially due to its suitability for crossbar structures that enable the realization of ultra-high density memory arrays [21, 22]. Most of the isolator layers in the MIM structures are stoichiometric metal oxides such as NiO and Al_2O_3 . However, it has been also reported that some dielectric films containing nanocrystals or nanoparticles show resistive switching and thus have the potential in the resistive switching memory applications [23-

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28]. For examples, an *Al*-rich Al_xO_y film (i.e., an aluminum oxide film containing *Al* nanoparticles) in a MIM structure exhibits resistive switching phenomenon without a forming process [25], and a polystyrene film with gold nanoparticles capped with conjugated 2-naphthalenethiol in a MIM structure shows resistive switching also [26].

AlO_xN_y films possess unique properties of high dielectric strength, high resistivity, low loss, high decomposition temperature, chemical inertness and good thermal conductivity. These properties make these films encouraging for use in manufacturing high energy density capacitors for pulse power and other extreme environment applications. In this work, the *Al*-rich Al_2O_3 and AlO_xN_y thin films with different fabrication methods and device structures will be investigated.

In view of the important roles of metal-dielectric nanocomposite film in memory devices, the electrical properties of *Al*-rich *Al*-based dielectric films based metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM) structure deserve more investigation. Nc-*Al* embedded in AlO_xN_y or Al_2O_3 can be synthesized by many techniques, which have their own advantages and disadvantages. Among them, the sputtering is one of the most popular methods for producing metal-dielectric nanocomposite film. Such technique is fully compatible with the existing CMOS technology.

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1.2 Objective and scope of research

In this study, the sputtering and anodization methods have been used to synthesize nc-Al embedded in AlO_xN_y or Al_2O_3 thin films. The main objective of this thesis is to investigate the electrical properties and memory applications of the Al-rich Al-based dielectric thin films. The scope of the research and the approach are as follows:

- (1) Synthesis of nc-Al embedded in AlO_xN_y and Al_2O_3 thin films using rf sputtering. The different oxygen concentrations of Al-based AlO_xN_y dielectric thin films can be achieved by varying the sputtering power.
- (2) Synthesis of Al-rich anodized aluminum oxide thin film based MIM structured memory device. The targeted thickness of anodized film is around 30-50 nm.
- (3) Characterization of the Al-rich AlO_xN_y and Al_2O_3 thin films embedded with nc-Al using Transmission Electron Microscopy (TEM), Scanning Electron Microscope (SEM) and X-ray Photoelectron Spectroscopy (XPS). The obtained structural and chemical properties are used for the analysis of electrical and optoelectronic properties.
- (4) Investigation of the current transport behavior of the Al-rich Al_2O_3 thin films embedded with nc-Al by using the current-voltage (I - V) measurement under various elevated temperatures.
- (5) Study of current conduction mechanisms in the dielectric thin films and examination of influences of the charge trapping in thin films on the current conduction.

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- (6) Study of charge storage behavior including charge trapping and charge retention of the *Al*-rich Al_2O_3 thin films with the conventional capacitance-voltage ($C-V$) method.
- (7) Development of the charge-controlled WORM device based on nc-*Al* Al_2O_3 thin film. The data retention properties and the temperature dependence of memory behaviors are investigated.
- (8) Investigation of the unipolar resistive switching in *Al*-rich Al_2O_3 thin film which is fabricated by anodization method with MIM structure. As the film contains excess *Al* will form pre-exist conductive paths through the dielectric film, the forming process should be not necessary.
- (9) Study of the conduction mechanisms of the high-resistance state (HRS) and the low-resistance state (LRS) and the temperature dependence of resistive switching. From the temperature dependence study, the relationship between the set and reset process and the electrochemical / thermochemical reactions may be established.
- (10) Study of oxygen concentration effect on the current conduction and resistive switching properties of *Al*-rich AlO_xN_y thin film. By adjusting the sputtering power during the deposition, the resulted thin film will contain different oxygen concentrations.
- (11) Examination on the difference in the oxygen concentration effect between the MIS and MIM structures.

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1.3 Major contributions of the thesis

The major contributions of the thesis are listed as follow:

(1) Current transport behavior and conduction modulation in the *Al*-rich Al_2O_3 thin film based metal-insulator-semiconductor (MIS) device have been investigated.

a) The *Al*-rich Al_2O_3 thin films have been synthesized by using rf sputtering method, and the MIS memory device has been fabricated.

b) The current transport under positive and negative biases has been investigated.

A modulation of current conduction has been observed.

(2) Charge trapping and charge retention behavior of the *Al*-rich *Al*-based dielectric thin films has been investigated.

a) The dependences of the amount of trapped charges on the polarity and magnitude of the charging voltage as well as the charging time have been investigated. The retention behavior of trapped charges after charging has also been studied.

b) The temperature effect on the charge trapping and charge retention behavior has been investigated. At high temperature environment, the device showed significant degradation in charge retention as releasing of trapped charges increased.

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c) The effect of charge trapping on current conduction has been determined. The potential memory applications of this *Al* based MIS device as WORM device and charge-controlled memristor have been investigated.

(3) The unipolar resistive switching properties of *Al*-rich anodized aluminum thin films have been investigated.

a) *Al*-rich Al_xO_y dielectric thin film on p-type silicon substrate has been fabricated using aluminum anodization method.

b) The resistive switching properties of the *Al*-rich anodized aluminum oxide thin film based MIM structured have been investigated. It is observed that the forming process is not required for this material.

c) The temperature effect on the set/reset voltage and current conduction has been investigated.

(4) The oxygen concentration effect of *Al* based AlO_xN_y dielectric thin films have been investigated.

a) The *Al*-rich AlO_xN_y thin films with different oxygen concentrations have been fabricated by using rf sputtering method. Different oxygen concentrations of the deposited film different have been achieved by varying the sputtering power. The XPS result indicates that the oxygen concentration increases with the sputtering power.

b) The electrical properties of the MIS devices with different oxygen concentrations have been investigated. The samples with medium and high

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oxygen concentrations exhibit the conduction switching phenomenon. However, such conduction switching could not be observed from the low oxygen concentration sample.

c) Resistive switching properties of the MIM structures with different oxygen concentrations have been investigated. The samples with medium and high oxygen concentrations exhibit resistive switching; in contrast, the low oxygen concentration sample behaves like a resistor without any resistive switching.

1.4 Organization of the thesis

This thesis mainly focused on the studies of electrical properties of nc-*Al* embedded in AlO_xN_y or Al_2O_3 thin films and their applications. **Chapter 1** briefly introduces the roles of *Al*-based dielectric thin film in memory device applications. The motivation, objective and scope of the research and the major contributions of this thesis are also given in this chapter.

Chapter 2 presents a literature review of the research on fabrication and characteristics of *Al*-based dielectric film memory devices with both MIS and MIM structures. It begins with discussion of the ion implantation technique and other common techniques for the synthesis of *Al*-rich in AlO_xN_y and Al_2O_3 dielectric thin film. After that, the common techniques used to characterize the structural, material, electrical and optoelectronic properties of nc-*Al* embedded in AlO_xN_y and Al_2O_3 are reviewed. Finally,

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the applications of nc-Al in non-volatile (NVM) memory devices, WORM devices and memristor devices are discussed in detail.

In **Chapter 3**, the current transport behavior of the nc-Al Al_2O_3 thin films MIS structure based memory device is investigated. The characteristics of current conduction at various temperatures are obtained and the different transport mechanisms dominating in the different oxide field regions are discussed. Appropriate models are proposed to explain the current transport behavior. The modulation and charge trapping effect of the nc-Al in Al_2O_3 thin films is investigated. The dependences of trapped charges on the charging voltage and the charging time are studied. Besides, the influences of environment temperature on the charge trapping and charge retention behavior are investigated. This memory device could be potential application in WORM devices and NVM devices. In addition, the charge loss caused by the charge leakage to the Si substrate is also studied.

In **Chapter 4**, the unipolar resistive switching property in anodized aluminum film based memory devices with MIM structure has been investigated. The switching property of metal oxide thin film must be revisable and could be explained by using conductive filament model which may relate to electrochemical and thermochemical reactions. This device could be potential applications of memristor, which is called as the forth element of electrical circuits. In the end, the retention and endurance properties of this memristor device are investigated.

In **Chapter 5**, oxygen concentration effect on the current conduction of AlO_xN_y dielectric thin film based MIS device and resistive switching property of MIM device are

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investigated. There are three samples fabricated by sputtering with power 100 W, 150 W and 250 W. The oxygen concentrations will increase as 11 %, 18 % and 25 % for 100 W, 150 W and 250 W sputtering samples respectively. For low oxygen concentration samples, there is no conduction switching and resistance switching observed in its MIS and MIM structure devices. The I - V properties of low oxygen concentration samples exhibit charging and memory effect in MIS structure and behave like resistor in MIM structure. For the medium and high oxygen concentration samples, they exhibit conduction switching and resistance switching in their MIS and MIM structure devices respectively. The oxygen effect could be explained by oxygen vacancy model.

Finally, **Chapter 6** summarizes the research work carried out in this thesis and gives recommendations in the future work.

Chapter 2 Literature Review

2.1 Introduction

The scaling of Complementary Metal Oxide Semiconductor (CMOS) transistors has reached ultra-thin (~ 1.4 nm) silicon dioxide layer as a gate dielectric but the consequence of the thin film has a large gate leakage current. One approach to solve the large gate current is to replace the SiO_2 with a physically thicker layer of gate dielectric with a higher dielectric constant, such as hafnium oxide or hafnium silicate. It was found that such “high k ” gate dielectrics have inferior electronic properties compared to SiO_2 , such as a tendency to crystallize and a high concentration of electronic defects. Intensive research is underway to develop these oxides into higher quality electronic materials. Among these high k materials, Al -based dielectric film (Al_2O_3 or AlN) was chosen to be a popular candidate gate dielectric material. However, it has obvious disadvantage with a rather low dielectric constant. To overcome this problem, introducing metal nanocrystals into dielectric thin film can enhance its dielectric constant. The Al nanocrystals (nc- Al) based dielectric film seems to be a proper candidate with several advantages, including low cost, easy fabrication and good compatibility with existing technology. To introduce of nc- Al into a dielectric film, fabrication of Al -rich dielectric film is deemed to be a more practical approach.

In this chapter, the synthesis technique of Al -rich dielectric film containing nc- Al will be introduced in section 2.2, followed by the characterization techniques of its

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chemical and electrical properties in section 2.3. In section 2.4, the current conduction mechanisms commonly found in such dielectric film will be reviewed. Lastly, in section 2.5, the applications that include ReRAM memory, WORM device and memristor of such dielectric film will be reviewed in detail.

2.2 Synthesis techniques of *Al*-based dielectric thin film

The deposition process can be broadly classified into Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD). The PVD process can be carried out at lower deposition temperatures and without corrosive products, but deposition rates are typically lower. On the other hand, in CVD process, the film growth takes place at high temperatures, leading to the formation of corrosive gaseous products and may leave impurities in the film.

In this section, the techniques used to fabricate *Al*-based dielectric thin films are briefly reviewed. For the current study of metal-dielectric nanocomposite film based device study, sputtering technique is employed and such process is fully compatible with modern CMOS technology. Besides sputtering, the anodization is another possible method to deposit the metal-dielectric nanocomposite film. The anodization process is quite popular nowadays in fabricating metal oxide on flexible substrate.

2.2.1 Sputtering deposition

Sputtering is a physical process whereby atoms in a solid target material are ejected into the gas phase due to bombardment of the material by energetic ions. It is commonly

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used for thin-film deposition, as well as analytical techniques as shown in Fig. 2-1. The ions for the sputtering process are supplied either by a plasma that is induced in the sputtering equipment. In the plasma sputtering devices, a variety of techniques are used to modify the plasma properties, especially ion density.

Fig. 2-1: The basic set-up for sputtering deposition system (from Ref. [29]).

To achieve the optimum sputtering conditions, the usage of radio frequency (RF) alternating current, utilization of magnetic fields, and application of a bias voltage to the target are very important. Metal nanocrystals embedded in dielectric films can be prepared by co-sputtering from two electrodes, one with metal target and the other with a dielectric film material target. This method enables controlled composition on the production of alloyed materials. An entire series of mixed compositions with different microstructures can be obtained by varying the RF power applied to the targets. In a sputtering process, the energetic Ar ions are accelerated toward the target surface by

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high-voltage bias between anode and cathode. Hence, this causes the target material to be sputtered out as gaseous form and then deposited onto the sample surface as a thin film.

2.2.2 Anodization: solution-based method

The history of electrochemical oxidation of aluminum dates back to the beginning of the last century [30-33]. Anodic treatment of aluminum was intensively investigated to obtain protective and decorative films on its surface. More recently, applications of porous alumina with a huge surface area and a relatively narrow pore size distribution have been exploited. For example, several attempts to fabricate inorganic membranes have been reported [34,35]. Nowadays, porous alumina is one of the most prominent template materials for synthesis of nanowires or nanotubes with controllable diameter and high aspect ratios. The set up for anodization system is shown in the Fig. 2-2.

- A: motor-controlled rotator for agitating the electrolyte
- B: Pt mesh working as counter electrode
- C: isolator consisting of an outer styrofoam layer and inner brass layer
- D: electrolyte container made of teflon
- E: screw for fixing the electrolyte container to the brass plate
- F: aluminum sheet
- G: brass plate working as electric conductor connected with a positive electric source
- H: potentiostat/galvanostat
- I: computer to operate the potentiostat/galvanostat and the cooling
- J: peltier cooling element

Fig. 2-2: Schematic diagram of the apparatus used for the anodization (from Ref. [36]).

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After anodization, an oxide film can be grown on certain metals – aluminum, niobium, tantalum, titanium, tungsten, zirconium – by an electrochemical process called anodizing. For each of these metals there are process conditions which promote growth of a thin, dense, barrier oxide of uniform thickness. Aluminum is unique among these metals, in addition to the thin barrier oxide, anodizing aluminum alloys in certain acidic electrolytes produces a thick oxide coating, containing a high density of microscopic pores. This coating has diverse and important applications which include architectural finishes, prevention of corrosion of automobile and aerospace structures, and electrical insulation. In fact, it is this porous coating that is most often thought of as the product of anodizing.

Based on a two-step replicating process, a self-ordered porous alumina membrane with 100 nm inter-pore distance was synthesized by Masuda and Fukuda in 1995 [37]. This discovery was a breakthrough in the preparation of 2D-polydomain porous alumina structures with a very narrow size distribution and extremely high aspect ratios. Two years later, they combined the aluminum anodization method with nano-imprint technologies, which allowed for the first time the preparation of a monodomain porous alumina structure. The standard two-step aluminum anodization procedure is shown in Fig. 2-3:

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Fig. 2-3: Stages of the formation of self-ordered alumina: a) annealing at 500°C for 3h; b) electro-polishing in a solution of $1/4 \text{ HClO}_4 + 3/4 \text{ C}_2\text{H}_5\text{OH}$ for 4 min at 8 V with agitation; c) first anodization (typically 1~2 days); d) selective dissolution of the formed oxide layer; e) second anodization under the same conditions as the first anodization; and f) isotropic etching in 1 M phosphoric acid at 30 °C to widen the pores (from Ref. [36]).

In an anodizing cell, the aluminum workpiece is made as the anode by connecting it to the positive terminal of a dc power supply. The cathode is connected to the negative terminal of the supply. The cathode is a plate or rod that is either a carbon, lead, nickel, stainless steel or any electronic conductor that is unreactive in the anodizing bath. When the circuit is closed, electrons are withdrawn from the metal at the positive terminal, allowing ions at the metal surface to react with water to form an oxide layer on the metal. The electrons return to the bath at the cathode where they react with hydrogen ions to make hydrogen gas. However, the pore formation should have relationship with current flow as shown in Fig. 2-4:

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Fig. 2-4: Schematic diagram of the pore formation at the beginning of the anodization. regime 1: formation of barrier oxide on the entire area; regime 2: local field distributions caused by surface fluctuations; regime 3: creation of pores by field-enhanced or/and temperature-enhanced dissolution; regime 4: stable pore growth (from Ref. [36]).

The overall reaction that takes place during anodization is:

This is the sum of the separate reactions at each electrode. The reactions at the anode occur at the metal/oxide and oxide/ electrolyte interfaces. The ions that make up the oxide are mobile under the high field conditions. At the metal/oxide interface the inward moving oxygen anions react with the metal:

At the oxide/electrolyte interface outward moving aluminum cations react with water:

After anodization, a porous structure will be formed as shown in Fig. 2-5:

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Fig. 2-5: Schematic diagram for barrier type alumina and porous type alumina. The aluminum metal, an inner oxide consisting of pure alumina and an outer oxide consisting of an anion-contaminated alumina are indicated (from Ref. [36]).

As shown in Fig. 2-5, both the barrier-type and the porous-type alumina films consist of an inner oxide of high purity alumina and an outer oxide layer comprised of alumina which has incorporated anions. The inner oxide is adjacent to the oxide/metal interface, while the outer oxide is adjacent to the electrolyte/oxide interface. The porous structure could be seen in SEM image as shown in Fig. 2-6. The following figures are bottom view of anodized aluminum film with different electrolyte. The porous structure could be seen after removing the bottom aluminum.

Fig. 2-6: SEM micrographs of the bottom view of anodic alumina layers. Anodization was conducted in 0.3 M (~1.7 wt %) sulfuric acid at 10 °C at 25 V (a), 0.3 M (~2.7 wt %) oxalic acid at 10 °C at 40 V (b), and 10 wt % phosphoric acid at 3 °C at 160 V (c). Pore opening was carried out in 5 wt % phosphoric acid at 30 °C for 30 min (a), 35 °C for 30 min (b), and 45 °C for 30 min (c). The thickness of the oxide films was approximately 120 nm (from Ref. [38]).

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2.3 Characterization of *Al*-rich and *Al*-based dielectric thin films

Most of the techniques to characterize *Al*-rich dielectric thin films are based on the existing semiconductor characterization techniques. However, the emphasis has to be shifted from the bulk properties to the properties associated with particles with nanometer scale. In section 2.3.1, the chemical and structure characterizations which provide essential information for the analysis of experimental results obtained from the electrical characterizations are reviewed. As far as the semiconductor nanocrystals are concerned, the main objectives of structural and material characterizations are to describe the physical dimensions, shape and crystal orientation of the nanocrystals and to reveal the atomic and chemical composition of the films embedded with nanocrystals. In section 2.3.2, the common electrical characterization techniques are discussed. The main purpose is to analyze the charge trapping, charge retention and current transport behavior associated with the *Al*-based dielectric thin film.

2.3.1 Chemical and structural characterization techniques:

2.3.1.1 Transmission Electron Microscope (TEM)

Transmission Electron Microscopy (TEM) in Fig. 2-7 is a microscopy technique whereby a beam of electrons is transmitted through an ultra-thin specimen, interacting with the specimen as it passes through. There are a lot of papers about TEM study of *Al* based dielectric film [39-44]. An image is formed from the interaction of the electrons transmitted through the specimen; the image is magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor.

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Fig. 2-7: Schematic of transmission electron microscopy system (from Ref.[45]).

TEM is capable of imaging at a significantly higher resolution than light microscopes. This enables the instrument's user to examine fine detail—even as small as a single column of atoms, which is tens of thousands times smaller than the smallest resolvable object in a light microscope. TEM forms a major analysis method in a range of scientific fields, in both physical and biological sciences. TEM finds application in cancer research, virology, materials science as well as pollution, nanotechnology, and semiconductor research. At smaller magnifications, TEM image contrast is due to absorption of electrons in the material and due to the thickness and composition of the material. At higher magnifications complex wave interactions modulate the intensity of the image, requiring expert analysis of observed images. Alternate modes of use allow for the TEM to observe modulations in chemical identity, crystal orientation, electronic

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structure and sample induced electron phase shift as well as the regular absorption based imaging.

2.3.1.2 Scanning Electron Microscope (SEM)

A Scanning Electron Microscope (SEM) is a type of electron microscope that images a sample by scanning it with a high-energy beam of electrons in a raster scan pattern. The SEM study of *Al* based dielectric thin film has been reported [42,46-50]. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition, and other properties such as electrical conductivity.

The types of signals produced by an SEM include secondary electrons, Back-Scattered Electrons (BSE), characteristic X-rays, light, specimen current and transmitted electrons. Secondary electron detectors are common in all SEMs, but it is rare that a single machine would have detectors for all possible signals. The signals result from interactions of the electron beam with atoms at or near the surface of the sample. In the most common or standard detection mode, the SEM can produce very high-resolution images of a sample surface, revealing details less than 1 nm in size. Due to the very narrow electron beam, SEM micrographs have a large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. A wide range of magnifications is possible, from about 10 times to more than 500,000 times, about 250 times the magnification limit of the best light microscopes. Back-Scattered Electrons (BSE) is beam electrons that are reflected from the sample by elastic scattering. BSE are often used in analytical SEM along with the spectra made

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from the characteristic X-rays. Because the intensity of the BSE signal is strongly related to the atomic number of the specimen, BSE images can provide information about the distribution of different elements in the sample. For the same reason, BSE imaging can image colloidal gold immune-labels of 5 or 10 nm diameter which would otherwise be difficult or impossible to detect in secondary electron images in biological specimens. Characteristic X-rays are emitted when the electron beam removes an inner shell electron from the sample, causing a higher energy electron to fill the shell and release energy. These characteristic X-rays are used to identify the composition and measure the abundance of elements in the sample.

Fig. 2-8: Schematic of scanning electron microscope system (from Ref.[51]).

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2.3.1.3 X-ray Photoelectron Spectroscopy (XPS)

A typical X-ray Photoelectron Spectroscopy (XPS) spectrum is a plot of the number of electrons detected versus the binding energy of the electrons detected. Each element produces a characteristic set of XPS peaks at characteristic binding energy values that directly identify each element that exist in or on the surface of the material being analyzed. The XPS study realte to *Al* based dielectric thin film has been investigated in some papers [52-57]. These characteristic peaks correspond to the electron configuration of the electrons within the atoms, e.g., 1s, 2s, 2p, 3s, etc. The number of detected electrons in each of the characteristic peaks is directly related to the amount of element within the area irradiated. To generate atomic percentage values, each raw XPS signal must be corrected by dividing its signal intensity (number of electrons detected) by a "relative sensitivity factor" (RSF) and normalized over all of the elements detected. The basic components of XPS system is shown in Fig. 2-9.

Fig. 2-9: Basic components of a monochromatic XPS system (from Ref.[58]).

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X-ray Photoelectron Spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 to 10 nm of the material being analyzed with required Ultra-High Vacuum (UHV) conditions. XPS is a surface chemical analysis technique that can be used to analyze the surface chemistry of a material in its "as received" state, or after some treatment.

2.3.2. Electrical characterization techniques

2.3.2.1 Capacitance-voltage (C - V) measurement

Capacitance-Voltage (C - V) testing is widely used to determine semiconductor parameters, particularly in MOSCAP and MOSFET structures. However, other types of semiconductor devices and technologies also can be characterized with C - V measurements, including bipolar junction transistors, III - V compound devices, photovoltaic cells, MEMS devices, organic thin film transistor (TFT) displays, photodiodes, and carbon nanotubes.

For a metal-oxide semiconductor (MIS) capacitor, properties such as gate oxide thickness, substrate doping concentration, threshold voltage and flat-band voltage can be determined from the C - V measurement [59]. The C - V curve is usually measured with a C - V meter which applies a DC bias voltage and a small sinusoidal signal to the MIS capacitor and measures the capacitive current with an AC ammeter. The flat-band voltage

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(V_{FB}) of the MIS capacitor is sensitive to the existence of charges at the Al / Al -based oxide interface or in the bulk dielectric film. Thus, the behavior of various traps present can be investigated based on the flat-band voltage shift (ΔV_{FB}). Fig. 2-10 shows the typical C - V characteristics of a MIS capacitor with nc- Al embedded in the AlN dielectric thin film. After the charge injection, the ΔV_{FB} can be clearly observed for the usage to estimate the amount of charges trapped in the oxide. The positive/negative ΔV_{FB} shifts indicate electron trapping /de-trapping occur at the layer which closes to substrate side.

Fig. 2-10: The typical C - V measurement of Al -based dielectric films. The flat band voltage shift should be got from C - V measurement (from Ref.[128]).

In wafer processes, C - V measurements can reveal oxide thickness, oxide charges, contamination from mobile ions, and interface trap density. These measurements continue to be important after other process steps such as lithography, etching, cleaning

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dielectric and poly-silicon deposition and metallization. After devices are fully fabricated on the wafer, $C-V$ is used to characterize threshold voltages and other parameters during reliability and basic device testing for modeling the performance of these devices.

2.3.2.2 Current-voltage ($I-V$) measurement

The MIS capacitor is also frequently studied using a current-voltage ($I-V$) measurement. However, for an actual gate oxide, the leakage current is non-zero, and the conduction mechanisms identified from the $I-V$ measurements reveal the properties of the interfaces (i.e., metal / oxide interface and oxide / Si interface) as well as the bulk oxide itself [60]. From the $I-V$ measurements of MIS capacitors with nanocrystals embedded in the gate oxide, the hysteresis effect due to charging and discharging of nanocrystals has been observed [61-63]. Fig. 2-11 is the typical $I-V$ measurement example for Al-based dielectric thin film with MIS device structure.

Fig. 2-11: The typical $I-V$ measurement for Al-based dielectric thin film (from Ref. [128]).

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2.4 Review of conduction mechanisms

Due to the variation in the material, fabrication process, film thickness, and trap density of the dielectric layer, there are many conduction mechanisms for the current transport in the *Al* base dielectric thin film systems which are important for the ultra-large-scale-integration (ULSI) processes. This section briefly reviews the conduction mechanisms used for the analysis of current transport behavior in this study.

2.4.1 Interface-limited conduction mechanisms

2.4.1.1 Tunneling

Due to constant downscaling of gate-dielectric thicknesses in modern MIS devices the effect of tunneling has drastically gained relevance. Quantum mechanical tunneling describes the transition of carriers through a classically forbidden energy state. This can be an electron tunneling from the semiconductor through a dielectric, which represents an energy barrier, to the gate contact of an MIS structure. Even if the energy barrier is higher than the electron energy, there is quantum mechanically a finite probability of this transition. The reason lies in the wavelike behavior of particles on the quantum scale where the wave function describes the probability of finding an electron at a certain position in space. As the wave function penetrates the barrier and can even extend to the other side, quantum mechanics predict a non-zero probability for an electron to be on the other side.

In recent years it has been observed that the tunnel conductance varies rapidly for voltage biases up to about 0.1 V. These observations had attributed to the excitation by the tunneling electrons of internal degrees of freedom in the barrier or the electrodes.

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Hence the tunneling electrons may act as spectroscopic probes of the tunnel junction. Lenzlinger and Snow [64] studied tunneling in the silicon-silicon oxide-*Al/Mg* system in which the oxide was relatively thick (60-500 nm). Thus it was necessary to apply high-voltage biases to the system to reduce the barrier thickness at the negatively-biased Fermi level to a sufficiently thin value (less than 50 Å) in order to observe the Fowler-Nordheim type tunnel effect. In Figure 2-12, the energy band conditions for the tunneling regime are shown. Here, the electrons from the inverted silicon surface can tunnel directly through the forbidden energy barrier formed by the dielectric layer to the poly-gate. Direct tunneling is strongly gaining significance when the dielectric layer gets thinner.

Fig. 2-12: Schematic of the tunneling processes in a silicon-dielectric-silicon structure. The different tunneling processes are indicated by arrows and described in the text. The abbreviations EED and HED denote the electron and hole energy distribution function (from Ref. [65]).

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The energy band condition for Fowler-Nordheim tunneling is a special case of direct tunneling as shown in Fig. 2-13. The electrons do not tunnel directly to the other side of the barrier. Instead they tunnel from the silicon inversion layer to the conduction band of the layer from where they are transported to the gate contact. The Fowler-Nordheim regime is significant for thicker dielectrics and sufficiently high electric fields.

Fig. 2-13: Energy-band diagram of a MIS structure (a) at zero bias, (b) with a large positive gate bias, and (c) with a large negative gate (from Ref. [64]).

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The expression of FN tunneling current (J_{FN}) through the SiO_2 is given by [60]

$$J_{FN} = A_{FN} E^2 \exp\left(-\frac{B_{FN}}{E}\right) \quad (2.1)$$

where E is the external applied electric field across the dielectric layer, and A_{FN} and B_{FN} are two constants given by

$$A_{FN} = \frac{q^3}{16\pi^2 \hbar \Phi_{FN}}$$

$$B_{FN} = \frac{4}{3} \frac{(2m^*)^{1/2}}{q\hbar} \Phi_{FN}^{3/2} \quad (2.2)$$

where q is the electronic charge, m^* is the effective mass of electrons (or holes) in the oxide layer, $\hbar$ is the Planck constant, and Φ_{FN} the tunneling barrier height for electrons or holes. From Eq. (2.1), it is obvious that $\ln J_{FN} / E^2$ is a linear function of $1/E$ with a slope of $-B_{FN}$. Therefore, the barrier height Φ_{FN} can be determined from the slope of the straight line in a FN plot. It should be noted that a standard FN tunneling current is independent of the measurement temperature. This allows one to quickly distinguish FN tunneling from other temperature-dependent current conduction mechanisms. In typical flash nonvolatile memory devices based on floating-gate design, FN tunneling is a common programming mechanism.

As the reduction of the applied voltages does not keep up with the miniaturization of actual devices, the electric fields across dielectric layers are constantly increasing. Especially for non-volatile memory cells, high electric fields are necessary in order to achieve quick write and erase cycles. Due to the repeated high-field stress, defects can arise in the dielectric leading to tunneling currents even at low fields.

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There are many approaches to model Trap-Assisted Tunneling (TAT). One is to model the defect assisted tunneling process including a single trap. For each trap position tunneling from the cathode to the trap and further to the anode is considered. From this the trap occupancy function can be calculated which is used to compute the tunneling current [66]. This single-TAT approach works very well for slightly degraded devices or devices with thin gate dielectrics. For thicker dielectrics with a high defect density it is reasonable to assume that also the interaction of two or more traps in the tunneling process takes place [67].

For the modeling of multi-Trap Assisted Tunneling (multi-TAT) approaches like a two-trap process [68,69] or a multi-trap process considering hopping of carriers between distinct defects [70] have been presented. Recently, anomalous charge loss in floating-gate memory cells has been reported [67], where a two-trap model was used to reproduce the measured data.

2.4.1.2 Schottky emission

Schottky emission is usually considered to be thermionic emission of electrons over a reduced work-function barrier resulting from the combined effects of image potential and applied electric field [60,71,72]. Ematage and Tantraporn first reported experimental observation of Schottky emission from metals into dielectric contact layers [71]. Typical experimental conditions are temperatures of the order of 300 K or higher, electric fields of the order of 10^5 V/cm. Schottky emission is less likely to occur in oxides, which are extremely small band-gap intrinsic or extrinsic semiconductors, than in larger band-gap oxides and insulators, for which the metal-oxide work function is more likely to be the

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smallest energy gap for electronic conduction in the system. Schottky emission, however, depends strongly on the barrier between metal and insulator and should vary with the metal work function. Such dependence does not appear experimentally. The energy band diagram of SE is shown in Fig. 2-14.

Figure 2-14: Energy band diagram showing the schottky emission of electrons over the potential barrier in the presence of an electric field (from Ref.[71]).

If the potential step (with respect to the Fermi level) at a neutral barrier with attendant image potential as a function of the distance from the interface and in the presence of an electron is given by [60]:

$$J = AT^2 \exp\left(-\frac{\phi_0}{kT}\right) \exp\left(\frac{\beta_s \sqrt{E}}{kT}\right)$$

$$\beta_s = \sqrt{\frac{q^3}{4\pi\epsilon_i\epsilon_0}} \quad (2.3)$$

which is called the Richardson-Schottky equation. The ϵ_i and ϵ_0 are dielectric constant of dynamic dielectric material and vacuum permittivity separately.

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The Richardson-Schottky effect at a neutral contact in insulators appears to have been first observed by Emptage and Tantraporn [71] who reported $\ln I$ against $\sqrt{E}$ relationship in their samples; since then there have been many other similar observations reported. However, Mead has pointed out that $\ln I$ against $\sqrt{E}$ relationship does not necessarily imply the Richardson-Schottky effect and has reported convincing evidence of the effect. The schottky emission is quite often seen in metal-dielectric nanocomposite thin films. From the expression of SE, the I - V and Arrhenius plot could be used to analyze the current conduction as the example shown in Fig. 2-15.

Fig. 2-15: The a) I - V and b) Arrhenius plot of Schottky emission of Al-based dielectric film with MIS structure.

2.4.1.3 Space charge limited current

Space charge is a concept in which excess electric charge is treated as a continuum of charge distributed over a region of space (either a volume or an area) rather than distinct point-like charges [72-74]. This model typically applies when charge carriers have been emitted from some region of a solid: the cloud of emitted carriers can form a

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space charge region if they are sufficiently spread out, or the charged atoms or molecules left behind in the solid can form a space charge region. For a trap-free insulator, the J - V characteristic is [73]

$$J = \frac{9\mu\epsilon_i\epsilon_0 V^2}{8d^3} \quad (2.4)$$

where μ is the effective carrier mobility, ϵ_i is the dynamic dielectric constant, ϵ_0 is the vacuum permittivity, d is the thickness of the insulator film. Conduction in such structures is due to electrons injected into the insulator base. The uncompensated charge of injected electrons limits the current. The energy band diagram is shown in Fig. 2-16.

Fig. 2-16: The energy band diagram of space charge limited current (from Ref.[72]).

Space charge usually only occurs in dielectric media because in a conductive medium the charge tends to be rapidly neutralized or screened. The sign of the space charge can be either negative or positive. This situation is perhaps most familiar in the area near a metal object when it is heated to incandescence in a vacuum.

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2.4.2 Bulk-limited conduction mechanisms**2.4.2.1 Poole-frenkel emission**

For the Schottky effect, the emission will occur from the respective electrodes depending on the polarity of the applied field. However, for the Pool-Frenkel effect the barrier-height density will be independent of the direction of field. The Poole-Frenkel effect is often used to explain conduction in thin dielectric films [75-80]. Frenkel's original model incorporates the Boltzmann approximation for the electron energy distribution, and assumes a midgap Fermi level. Despite these approximations, this model has been used to predict conduction through dielectrics with reasonable accuracy [75]. The Poole-Frenkel effect or field-assisted thermal ionization is the lowering of a coulombic potential barrier when it interacts with an electric field, as shown in Fig. 2-17. This process is the bulk analogue of the Schottky effect at an interfacial barrier. To experience the Poole-Frenkel effect, a trap is required to be positively charged when empty and uncharged when filled. Hence, the interaction between the positively charged trap and the electron giving rise to the coulombic barrier.

Fig. 2-17: Energy band diagram showing the PF emission of an electron from a trap in the dielectric layer in the presence of an external electric (from Ref.[76]).

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However, Mead has suggested that since traps abound in an insulator and a trap having a coulombic-type barrier would experience the Poole-Frenkel effect at high fields. Thereby increasing the probability of escape of an electron immobilized therein, the current density in thin-film insulators containing shallow traps is given by [60]:

$$J = CE_0 \exp\left(-\frac{q\Phi_B}{\xi kT}\right) \exp\left(\frac{\beta_{PF} \sqrt{E_0}}{\xi kT}\right) \quad (2.5)$$

where C is a constant, E_0 is electric field, ξ is a constant between 1 to 2. The example of PF conduction is shown in Fig. 2-18.

Fig.2-18: The I-V a) and Arrhenius plot b) of poole-frenkel emission in Al based dielectric film with MIS structure.

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It will be apparent that a plot of $\ln I$ against T^{-1} at constant voltage should yield a straight line. Such plots are normally observed in wide-band at sufficiently high temperature indicating that the conduction is by free electrons in the conduction band. At low temperature, when the majority of electrons are condensed in traps and/or donor centres and if the centres are very closely spaced, the conduction process is by electrons tunneling between nearest neighbor sites tunnel hopping and is a thermally activated process. Fig. 2-18 is the example of PF emission based on *Al*-rich *Al*-based dielectric thin film.

2.4.2.2 Ohmic conduction

For a given conductor, the current I in the conductor and the potential difference V between its ends are directly proportional follows relationship $V = IR$, where the proportionality constant R determined by physical and electrical properties of the conductor, is the “resistance”, measured in “ohms”. (The unit of resistance, the ohm, is such that when one ampere of current exists between potential differences of one volt, the conductor has a resistance of one ohm.) The linear relationship embodied in equation $V=IR$ is known as “Ohm’s law”, and any device, which exhibits this type of electrical behavior, is said to be ohmic. When the potential difference across an ohmic device is reversed in polarity, the current reverses direction, but the proportionality constant R in Ohm’s law remains constant. This is shown in Fig. 2-19 below.

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Fig. 2-19: Linear relationship of V and I in ohmic conduction

At low applied electric field, the current transport of an insulating film can be ascribed to the hopping conduction of thermally excited electrons from one isolated state to another [81]. The ohmic conduction current (J_{ohmic}) is given by [60]

$$J_{ohmic} = CE_0 \exp\left(-\frac{\Delta E_a}{k_B T}\right) \quad (2.6)$$

where C is the a constant, E_i is the electric field across the dielectric layer, ΔE_a is the activation energy of electrons, k_B is the Boltzmann constant, T and is the temperature in Kelvin indicates that the ohmic conduction current exponentially depends on the measurement temperature with an activation energy of ΔE_a . From the linear relationship between $\ln J/E_i$ and $1/T$, the activation energy ΔE_a can be determined.

2.5 Emerging non-volatile memory devices

Knowing the limitation of conventional FG-based non-volatile memory design, the semiconductor manufacturers and researchers are exploring alternative structures for non-volatile memory applications. Tiwari *et al.* proposed the nanocrystal-based non-volatile memory structure using a threshold voltage shift induced by the charge storage in isolated

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nanocrystals [82]. Due to the smaller bandgap of the nanocrystal material, the long-term charge storage in the nanocrystals is achieved. Although each nanocrystal only stores a few electrons, the collective effect of many charged nanocrystals shifts the threshold voltage of the device.

Memory effect is an alleged effect observed in rechargeable batteries that causes them to hold less charge. It describes one very specific situation in which certain batteries gradually lose their maximum energy capacity if they are repeatedly recharged after being only partially discharged. The battery appears to “remember” the smaller capacity. The source of the effect is changes in the characteristics of the underused active materials of the cell. The term is commonly misapplied to almost any case in which a battery appears to hold less charge than was expected. These cases are more likely due to battery age and use, leading to irreversible changes in the cells due to internal short-circuits, loss of electrolyte or reversal of cells. The advantage of *Al* dielectric based memory is the potential to use a thinner tunnel oxide without sacrificing the charge retention performance. Moreover, due to the nature of discrete charge storage as well as the Coulomb blockade effect which limits the removal of an electron from the nanocrystals, the nanocrystal-based non-volatile memory is more robust [82].

2.5.1 Charging effect and memory applications

The charging effect could be observed in several kinds of metal-dielectric nanocomposites materials which are quite similar with situation of nc-*Si* embedded in *SiO*₂. The defects or nanocrystals may act as trap centers. The charging/discharging effects are related to the electrons trapping/de-trapping in dielectric film or interface

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between nc-*Al* and dielectric which could be studied from *C-V* measurement as shown in previous section of Fig. 2-10. Normally the shifts in the *C-V* characteristic after the application of a constant charging voltage to the gate electrode were used to study the charge trapping behavior of the *Al* based dielectric thin film. A clear flat-band voltage shift (ΔV_{FB}) with respect to the initial *C-V* curve indicates the memory effect of the device structure. The ΔV_{FB} can be related to the density of charges trapped in the nc-*Al*. The charging/discharging effects are very important for the development of new devices as floating point memories [83] and floating gate transistors.

Based on the charging effect mentioned before, a Write-once-read-many (WORM) memory device could be developed as potential candidate for future NOM application. The WORM refers to computer data storage systems, data storage devices, and data storage media that can be written once but read for multiple times. These drives are used in applications where the same information is read at large number of times, but still must be rewritten occasionally. Write-once-read-many memory (WORM), in which the data storage in WORM is permanent and cannot be modified, has extensive application for archival storage of video images and non-editable database. WORM feature is found in Al_2O_3 films deposited on silicon substrates and test results from devices of such structure were tested will be shown and discussed in Chapter 3. Devices consist of two resistive states, high (OFF) and low (ON). Resistive switching from high to low is controlled by applying external bias and the process is not reversible. Experiment data is mainly consisting of *I-V* characteristics, endurance, retention and thermal stability of the devices. Results were also obtained for devices with different metal contact/substrate, and

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comparison will be made. Lastly, the theory behind the resistive switching mechanism and current behavior of the devices will be explained.

The example of WORM device is shown in Fig. 2-20.

Fig.2-20: From left to right: a schematic view of the fabricated Al/PI/MLG/PI/Al memory device and the structure of the memory unit cell; a cross-sectional TEM image of the assembly and (shown in the inset) an HRTEM image of the multilayer graphene (MLG) film in the device; I–V characteristics of an Al/PI/MLG/PI/Al memory device and (shown in the inset) the I–V curve for a device assembled without MLG (from Ref.[84]).

The WORM can be an inconvenient property when it comes to re-using recorded media, which was discovered as a desirable property for data backups and archives, to prevent erasure and tampering. Therefore, WORM capability has been intentionally added to otherwise rewritable media such as magnetic tape data storage and hard disk drives. The media can be written to, but the written portion immediately becomes read-only.

Modern WORM systems overcome most problems by building a tested software solution into the cartridges, drives, controllers or operating system. For removable media, the high-capacity drives are new enough that no available drive will violate the rules.

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Other features ensure that any data somehow overwritten in spite of restrictions will be detectable [85-88].

2.5.2 Switching effect and memory applications

2.5.2.1 Bipolar switching and unipolar switching

The bipolar switching means that the bias voltage must change the polarity to switch between different resistance states. After the injection of compliance current, the sample starts in the LRS when sweeping the voltage from zero to negative voltage. By applying negative voltage above a critical value, the sample switches from the LRS to the HRS. By applying a positive voltage, the sample resistance switches back to the LRS. An example of bipolar switching is shown in Fig. 2-21.

Fig. 2-21: Bipolar switching characteristics of a Ni/NiO/NiO_x ReRAM memory element (from Ref.[89]).

The unipolar switching means the set and reset processes are independent on voltage polarity. This unipolar switching mechanism of binary oxide materials might be explained in terms of the formation of a conduction path which was generated by the

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movement of oxygen vacancies under an electrical field during the forming and set process. The example of unipolar switching is shown in Fig. 2-22.

Fig. 2-22: Unipolar switching characteristics of a Ni/NiO/NiO_x ReRAM memory element (from Ref. [89]).

2.5.2.2 Resistive switching memory

Recently, the switching property is a hot topic being observed in several kinds of materials which is an essential physical effect in the resistive random access memory (ReRAM) operation. The resistance switching effect has been studied for more than 40 years [90-94]. Large negative resistance was first observed in the current-voltage (I - V) characteristics of five materials: SiO_x , Al_2O_3 , Ta_2O_5 , ZrO_2 and TiO_2 . The resistance switching phenomenon could be explained by different mechanisms including conductive filament model or solid diffusion model. Generally, the resistive switching cells are based on Metal-Insulator-Metal (MIM) structure. By applying appropriate voltage pulse, the MIM device could switch between High Resistance State (HRS) and Low Resistance State (LRS) with on-off ratio larger than 3 orders of magnitudes. The Al-rich Al-based

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dielectric film with MIM structure is observed to exhibit switching property at both room and elevated temperature which will be introduced in Chapter 4.

With recent progress in material science, Resistive Random Access Memory (ReRAM) devices have attracted interest for nonvolatile, low-power, nondestructive readout and high-density memories. The resistance switching behaviors have been extensively reported in a wide variety of materials such as perovskite oxides [95-97], transition metal oxides [97, 98], organic compounds [99, 100] and even graphene oxide [101]. Normally, the device is using capacitance-type or cross bar structures which are shown in Fig. 2-23:

Fig. 2-23: a) Capacitance-type and b) crossbars type of RERAM is built as a sandwich of metal oxide between two arrays of electrodes.

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It has a regime of operation with an approximately linear charge-resistance relationship as long as the time-integral of the current stays within certain bounds [104-107]. These devices are being developed for application in nanoelectronic memories, computer logic and neuromorphic computer architectures [103]. The model of memristor could be shown in Fig. 2-24.

Fig. 2-24: The coupled variable-resistor model for a memristor. A) Diagram with a simplified equivalent circuit; b) and c), the applied voltage (blue) and resulting current (green) as a function of time t for a typical memristor (from Ref.[108]).

More generally, a memristor is a two-terminal component in which the resistance depends on the integral of the input applied. Since the element “remembers” the amount of current that has passed through it in the past, it was tagged by Chua [103] with the name “memristor.” Another way of describing a memristor is that it is any passive two-terminal circuit elements that maintains a functional relationship between the time integral of current (called charge) and the time integral of voltage (often called flux, as it

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is related to magnetic flux). The slope of this function is called the memristance and is similar to variable resistance. Batteries can be considered to have memristance but they are not passive devices. The definition of the memristor is based solely on the fundamental circuit variables of current, voltage and their time-integrals, just like the resistor, capacitor and inductor. However, unlike those three elements, memristors of interest have a nonlinear function and may be described by any of a variety of functions of net charge. There is no such thing as a standard memristor. Instead, each device implements a particular function, wherein the integral of voltage determines the integral of current, and vice versa. A linear time-invariant memristor is simply a conventional resistor.

Memristors can retain memory states and data in power-off modes. Non-Volatile Random Access Memory (NVRAM) is pretty much to be seen as the first to-market memristor application will be seeing. There are already 3 nm memristors in fabrication currently. The fab prototypes resistance is read with alternating current; therefore the stored value remains unaffected.

Memristor can be fashioned into non-volatile solid-state memory, which would allow greater data density than hard drives with access times potentially similar to DRAM, replacing both components. HP prototyped a crossbar latch memory using the devices that can fit 100 gigabits in a square centimeter and has designed a highly scalable 3D design (consisting of up to 1000 layers or 1 petabit per cm^3). HP has reported that its version of the memristor is currently about one-tenth the speed of DRAM [100]. The devices' resistance would be read with alternating current so that the stored value would not be affected [110]. Some patents related to memristors appear to include applications

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in programmable logic [111], signal processing [112], neural networks [113] and control systems [114].

2.6 Summary of chapter

In this chapter, we reviewed the technology, characterization and electrical property measurement methods of *Al*-based dielectric thin film and their memory applications which are usually used in semiconductor industry nowadays. A table 2.1 could be used to summarize the current state-of-the-art performance of three oxide-based MIS and MIM memory devices. In our study, the *Al* based *Al*-rich dielectric film was fabricated by using sputtering and anodization methods. Also, the most common characterization techniques for the structural, material, electrical properties of *Al* based dielectric thin film have been reviewed. The applications of *Al* based dielectric film have also been discussed in details. Charging effect and switching effect are two important memory effect found in *Al* based dielectric thin film which make this material to be potential candidates of memory application. The biggest advantage of these dielectric thin film based device is compatibility with recent CMOS technology. Lastly, several kinds of important devices, including ReRAM, WORM and memristor have been reviewed.

	MIS structure			MIM structure		
	Power Consumption	Operation Speed	Retention & Endurance	Power Consumption	Operation Speed	Retention & Endurance
SiO ₂	High	10 ⁻⁹ s	Good			
TiO ₂				High	10 ⁻⁹ s	Good
Al ₂ O ₃	Low	10 ⁻⁶ s	Good	Low	10 ⁻⁶ s	Good

Table 2-1: Memory performance of three type devices.

Chapter 3 Electrical properties and memory applications of *Al/Al-rich Al₂O₃/Si* structure

3.1 Introduction

Aluminum oxide (Al_2O_3) has a high dielectric constant ($k = \sim 8 - 10$) and similar band gap and band alignment as compared to silicon oxide. As such, it has been proposed to be used in nonvolatile memory devices as a blocking layer or a charge storage layer [115-118]. Recently, *Al*-rich Al_2O_3 thin film synthesized with sputtering at a reduced oxygen gas flow rate was shown to be a promising candidate for the charge storage layer [117]. In our previous work [119], we also observed that the *Al*-rich Al_2O_3 thin film synthesized by radio frequency (RF) sputtering had a good charge storage capability, and the charge storage behaviors are similar to that of *Al*-rich *AlN* thin films [120].

In this chapter, it will be shown that charge trapping in the *Al*-rich Al_2O_3 thin films can cause a significant change in the reverse current-voltage (I - V) characteristics of the *Al* / *Al-rich Al₂O₃* / *p-Si* metal-insulator-semiconductor (MIS) structure while there is no significant change in the forward I - V characteristics. Such charging effect could be used to realize a two-terminal charging-controlled memory device. To form the MIS structure, the *Al*-rich Al_2O_3 thin film was deposited on a p-type silicon substrate by RF sputtering. The I - V characteristics of the device are determined by the carrier injection from either the *Si* substrate or the *Al* gate as well as by the carrier transport along the

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tunneling paths formed by the *Al* nanocrystals (nc-*Al*) distributed in the oxide layer. The reverse *I-V* characteristics are greatly affected by the charge trapping in the oxide layer (i.e., the electron trapping significantly reduces the reverse current while the hole trapping enhances the current significantly). However, the charge trapping does not produce a large change in the forward *I-V* characteristic. The conduction modulation caused by the charging/discharging effect has been investigated. The MIS structure clearly shows a memory effect. The flat-band voltage shift (ΔV_{FB}) of the MIS structure is found to be correlated with the charging time and charging voltage. Based on these electrical properties, the *Al/Al-rich Al₂O₃/Si* structure can be used to realize a write-once-read-many memory device.

3.2 Experiments

3.2.1 Sample fabrication

The *Al*-rich *Al₂O₃* thin film was fabricated by using RF sputtering method. In this study, an *Al*-rich *Al₂O₃* thin film with thickness of 60 nm was deposited on a p-type (100)-oriented *Si* wafer with a resistivity of 9 – 12 Ωcm , which was pre-cleaned through standard RCA clean process. The deposition was carried out by RF magnetron sputtering of an *Al* target with the purity of 99.99% at a distance of target to substrate about 40 cm from each other. RF power was set to 310 W with a deposition pressure of 0.93 Pa; and the ambient gas was a mixture of argon and oxygen with the constant flow rates of 60 sccm and 1 sccm, respectively. The detailed procedures are shown in Fig. 3-1:

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Fig. 3-1: Fabrication process of the MIS structure. The Al -rich Al_2O_3 thin film was fabricated by RF sputtering.

After the deposition of the Al oxide thin films, a rapid thermal annealing of the thin film was conducted at 550 °C for 30 s in N_2 ambient. To fabricate the MIS structure, an ohmic contact on the Si wafer backside was formed by the deposition of 200 nm Al , and the gate electrodes on the surface of the Al -rich Al_2O_3 thin film were formed by the deposition of 100 nm Al with a masking process. The diameter of each gate electrode is ~ 200 μm and the inter-pad distance is ~ 300 μm .

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3.2.2 Sample characterization

Cross-sectional Transmission Electron Microscopy (TEM) and X-ray Photoemission Spectroscopy (XPS) were used to investigate the structural and chemical properties of the Al -rich Al_2O_3 thin film as shown in Figure 3-2. The chemical states of the films were analyzed by XPS (Kratos AXIS Ultra) with monochromatic $Al\ K\alpha$ (1486.71 eV) X-ray radiation. The XPS result indicates that the as-fabricated thin film is indeed Al rich with an Al -to- Al_2O_3 atomic ratio of 1.24 and the TEM images show that Al nanocrystals (nc- Al) are formed in the Al_2O_3 matrix. The Al element is detected by SAD method. However, the accurate density of nc- Al could not be tested. The details of the TEM and XPS experiments have been reported in [119]. I - V measurement was carried out with a Keithley 4200 semiconductor characterization system, and capacitance-voltage (C - V) measurement was performed with an HP 4284A LCR meter at the frequency of 1 MHz, both at room temperature.

Fig. 3-2: XPS (a) and TEM image (b) of the Al -rich Al_2O_3 thin film. The XPS result indicates that the thin film is Al -rich. The TEM image shows the existence of aluminum nanocrystal with the diameter of about 5-10 nm.

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3.2.3 MIS device structure

The MIS device structure is shown in Figure 3-3. As discussed above, the insulator film is an Al -rich Al oxide layer with nc- Al embedded in the Al_2O_3 film. The Al -rich Al oxide layer has a thickness of 60 nm. The Al thicknesses of the top and bottom aluminum electrodes are 200 nm and 100 nm, respectively. Such structure is compatible with current CMOS technology.

Fig. 3-3: Structure of the Al/Al -rich Al oxide/ p -Si MIS diode.

3.3 Effects of charging and discharging in Al based dielectric thin film

3.3.1 Flatband voltage shift (ΔV_{BF}) in C - V measurement

To confirm the charge trapping and de-trapping effect in nc- Al embedded Al_2O_3 thin film, the C - V measurement should be executed at different charging conditions as shown in Fig. 3-4(a).

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Fig 3-4: a) ΔV_{FB} in C - V measurement before and after charging at ± 15 V for 1 ms and b) ΔV_{FB} as function of voltage charging at ± 5 V, ± 10 V, ± 15 V, ± 20 V and ± 25 V with 0.1s and 1s charging time on Al-rich Al_2O_3 based memory device.

Charging at ± 15 V at 1 ms will make the C - V curve shift to right and left side which indicate electron and hole trapping occur in the dielectric thin film respectively. The flat-band voltage shift as a function of charging voltage of ± 5 V, ± 10 V, ± 15 V, ± 20 V and

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± 25 V with different charging durations 0.1 s and 1 s was shown in Fig. 3-4(b). The application of a higher voltage leads to a larger flat-band voltage shift. For example, charging -10 V and -25 V at 1 s will cause the flat band voltage to shift 0.08 V and 0.78 V respectively. The flat-band voltage shift is also increased with the charging time. For example, charging -20 V at 0.1 s and 1s will cause flat band voltage to shift at 0.45 V and 0.65 V respectively. It is observed that the charge trapping/de-trapping depends on the polarity of the voltage applied, which indicates that both holes and electrons are found to be injected from the substrate with negative and positive charging voltages respectively. The capability of charge storage in the nc-*Al* and the effect on the flat-band voltage shift provide the possibility of the application of the nc-*Al* embedded *Al₂O₃* thin films in memory devices.

Such flat band voltage shift in *C-V* curve makes the film to be potential dielectric material applied in memory device. Meanwhile, the charge trapping/de-trapping may affect the current conduction which will be investigated in following section.

3.3.2 Effect of charge trapping/de-trapping behavior on current conduction

As indicated before, both positive and negative charge trapping in nc-*Al* are possible, depending on the gate voltage polarity applied. The capability of charge storage in the nc-*Al* and the effect on the flat-band voltage shift provide the possibility of the application of the nc-*Al/Al₂O₃* thin films in memory devices. The charge trapping in nc-*Al* embedded in *Al₂O₃* thin films here is similar to that in *Si* nanocrystals embedded in *SiO₂* thin films [121–124] or nc-*Al* embedded in *AlN* thin films [125].

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Fig. 3-5: Shift in *C-V* characteristic after the application of +15 V for 100 s showing electron trapping in the oxide layer.

As shown in Fig. 3-5, the application of +15 V to the gate for 100 s shifted the *C-V* characteristic to a positive flatband voltage shifting of 0.15 V ($\Delta V_{FB} = +0.15$ V), indicating that electron trapping occurred in the *Al*-rich *Al₂O₃* layer, with the possibility that the electrons could have been trapped in the nc-*Al*. On the other hand, as revealed by the TEM images, the interfaces between nc-*Al* and *Al₂O₃* were imperfect. Due to the imperfection of the *Al₂O₃* matrix with the embedded nc-*Al*, it is reasonable to assume that there was a large amount of defects at the interfacial regions between the embedded nc-*Al* and the *Al₂O₃* matrix. Therefore, the electrons could also be trapped in these defects. Nevertheless, the electron trapping was associated with the existence of the excess *Al* (i.e., nc-*Al*) distributed in the oxide layer. The electron trapping in either the nc-*Al* or the defects occurred when the injected electrons were transported along the tunneling paths

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formed by the nc- Al . The electron trapping, in turn, affected the carrier transport across the oxide layer as discussed below.

Fig. 3-6: I - V characteristics before and after the application of +15 V for 100 s. (a) Reverse I - V characteristics; and (b) forward I - V characteristics.

Figure 3-6 shows the I - V characteristics before and after the electron trapping. The electron trapping was achieved under the same bias conditions with the same charging duration as those in Fig. 3-5. As shown in Fig. 3-6 (a) for the reverse I - V characteristics, the electron trapping led to a significant reduction in the current. The reverse I - V characteristic after the electron trapping also followed a power law, but with smaller values of power-law parameters, I_0 and ζ , as compared to those before the electron trapping. The influence of electron trapping on the current conduction is explained as follows. Electron trapping in an nc- Al or a defect increased the resistance of the tunneling paths involving the nc- Al or the defect because of the electrostatic interaction of the transported electrons with the trapped electrons, and the tunneling paths could also be

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broken due to the coulomb blockade effect [121]. Therefore, the electron trapping suppressed the electron transport across the oxide layer.

On the other hand, the electron trapping reduced the electric field in the region of the oxide / *Si* interface, thus decreasing the electron injection from the *Si* substrate during the reverse *I-V* measurement. In contrast to the reverse *I-V* characteristic, the electron trapping did not have a large impact on the forward *I-V* characteristic, as shown in Fig. 3-6(b). This situation was due to the fact that both electron injection from the gate and the hole injection from the *Si* substrate occurred during the forward *I-V* measurement. The electron trapping suppressed the transport of the injected electrons but enhanced the transport of the injected holes. In addition, the electron injection was reduced while the hole injection was enhanced due to the electron trapping. Therefore, the forward *I-V* characteristic was not significantly affected by the electron trapping.

The other situation is applying a negative gate voltage, both the electron injection from the gate and the hole injection from the *Si* substrate occurred simultaneously, but the net charge trapping in the oxide layer could be either negative or positive, depending on the magnitude of the voltage and the charging duration. The net charge trapping tended to be positive for a larger voltage magnitude and a longer charging duration. As shown in Fig. 3-7, the application of -15 V for 1 s shifted the *C-V* characteristic to the negative with a negative flatband voltage shift of 0.15 V ($\Delta V_{FB} = -0.15$ V), indicating a net positive charge trapping in the *Al*-rich *Al₂O₃* layer (i.e., the hole trapping was dominant). The positive charge trapping had a strong impact on the reverse *I-V* characteristic as shown in Fig. 3-8(a).

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Fig. 3-7: Shift in C - V characteristic after the application of -15 V for 1 s showing net positive charge trapping in the oxide layer.

In Fig. 3-8(a), the reverse current was increased by about two orders after the positive charge trapping. The increase in the reverse current was due to the enhancements in both the electron injection from the Si substrate and the transport of the injected electrons along the $nc-Al$ tunneling paths during the reverse I - V measurement by the net positive charge trapping in the oxide layer. Being similar to the situation of the electron trapping discussed earlier, the positive charge trapping did not cause a large change in the forward I - V characteristics as shown in Fig. 3-8(b), because both the electron injection from the gate and the hole injection from the Si substrate were involved in the forward I - V measurement.

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Fig. 3-8: *I-V* characteristics before and after the application of -15 V for 1 s. (a) Reverse *I-V* characteristics; and (b) forward *I-V* characteristics.

3.3.3 Influence of charging time and charging voltage

From previous section 3.3.2, the charging effect on both reverse and forward current has been investigated. It is found that the charging time and charging voltage still have effect on current conduction. In this section, the effect of charging time and charging voltage has been studied. The current conductivity before and after charging (writing process) should be dependent on both charging time and voltage. Figure 3-9(a) shows the reverse current measured at +2 V as a function of writing voltage for the fixed writing time of 1 s. The current is ~ 1 nA before writing, and it increases to ~ 3 nA after the writing at -5 V. The current drastically increases to ~ 200 nA after the writing at -10 V, and it keeps increasing further with the magnitude of the writing voltage. Figure 3-9(b) shows the current as a function of writing time for the fixed writing voltage of -15 V. It should be pointed out that the experiments shown in Fig. 3-9 were carried out on different

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devices to avoid accumulated charging effect. There may be a variation in the currents for different devices. However, such variation does not affect the conclusion drawn from the present study.

Fig. 3-9: Reverse current measured at +2 V as a function of either writing voltage for the fixed writing time of 1 s (a) or writing time for the fixed writing voltage of -15 V (b).

As shown in Fig. 3-9(b), the current ratio of the state after writing to the state before writing is ~ 50 and ~ 200 for the writing time of $1 \mu\text{s}$ and 1 ms , respectively. This indicates that even a short writing pulse of $1 \mu\text{s}$ can produce a memory state well distinct from the state before writing. As can be observed from Fig. 3-9(b), the current has a power-law dependence on writing time (t), i.e., $I \sim t^{0.20}$. The power-law behavior is due to the power-law dependence of the charge trapping on the charge injection time. A power-law dependence of the charge trapping on the charge injection time has been observed experimentally [125,127].

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Fig. 3-10: Equivalent trapped charge per unit area at the oxide / Si interface as a function of the writing time.

Figure 3-10 shows the equivalent trapped charge per unit area (ΔQ) at the oxide / Si interface determined from the flat-band voltage shifts in the C - V measurements as a function of the writing time (i.e., the charge injection time). The trapped charge density has a power-law dependence on writing time (i.e., $\Delta Q \sim t^{0.19}$), which is similar to the power-law dependence of the reverse current on writing time. It is worth to mention that a power-law dependence of charge trapping on charge injection time is usually observed in the gate oxide of a MIS structure [126,127].

3.3.4 Retention and endurance properties

The charging effect on the reverse I - V characteristic could be used to realize two-terminal charging-controlled resistive memory MIS structure devices. The reverse resistance of the MIS memory device can be changed by the charge trapping in the Al -

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rich aluminum oxide layer (i.e., the resistance is switched to a high- or low-resistance state by the electron trapping or the hole trapping, respectively). The memory states represented by the resistance states can be changed by a large voltage, and they can be distinguished by measuring the resistance (or current) at a small reverse bias. The two-terminal charging-controlled resistive memory offers a higher memory density and a lower fabrication cost. Thus the study of its retention property is quite necessary.

Figure 3-11 shows the preliminary result of the retention performance of the memory device. The current measurement was conducted at a low bias of + 2 V while the charging operation was carried out at – 15 V for 1 s. As seen from the figure, the current ratio of the two memory states (i.e., the states before and after the charging) was large enough for distinguishing the two memory states. In addition, the currents of the two memory states had no significant changes after a waiting time of 30000 s. In addition to the retention performance, the read endurance of the WORM device has also been examined, and the result is shown in Fig. 3-12. As seen in the figure, after 10^6 readings there is no significant degradation in the state before writing and only a small decrease in the current of the state after writing, which indicates a good read endurance. The decrease of in the state after writing is due to the charge release during the waiting period of the endurance experiment and/or caused by the reading operations.

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Fig. 3-11: Measurement of the retention property at room temperature. 2 V read pulses with 1 ms pulse width are used in the measurement.

Fig. 3-12: Measurement of the reading endurance at room temperature. 2 V read pulses with 1 ms pulse width are used in the measurement.

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3.3.5 Conclusion

In summary, an *Al*-rich *Al₂O₃* thin film was deposited on a p-type silicon substrate by RF sputtering to form an *Al* / *Al*-rich *Al₂O₃* / p-*Si* MIS memory device. Under a positive bias applied to the *Al* gate (i.e., reverse bias), electrons were injected from the *Si* substrate and some of them were trapped in the *Al*-rich *Al₂O₃* layer. In contrast, both the electron injection from the *Al* gate and the hole injection from the *Si* substrate occurred under a negative bias (i.e., forward bias), leading to both electron and hole trapping in the *Al*-rich *Al₂O₃* layer, and a positive charge trapping could be achieved with a large voltage magnitude and/or a longer charge duration. The electron trapping and hole trapping caused a significant reduction and a large increase in the reverse current, respectively. However, the charge trapping (either electron or hole trapping) did not produce a large change in the forward *I-V* characteristic. The charging effect on the reverse current could be used to realize a two-terminal charging-controlled resistive memory based on the MIS structure.

3.4 Current transport in *Al*-rich *Al₂O₃* based two terminals memory device

In previous section 3.3, the charging effect and corresponding effect on current conduction have been investigated. There are two memory states are distinguished before and after voltage charging. Based on this phenomenon, the *Al* based dielectric thin film exhibited memory effect and could be potential candidates of memory device

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applications with good retention property. However, such memory effect could only be observed in positive biasing. In this section, the difference between positive/negative biasing current and the mechanism of such charge-induced memory effect in reverse current transport were explained by using power law model.

3.4.1 Modulation of current transport based on charging/dis-charging effect

The modulation of charging and discharging behavior of this two terminal memory device will be discussed first. Figure 3-13 shows the I - V characteristics of the MIS device. As seen in the figure, the memory device structure exhibited a “rectifying” behavior, namely, the current under the forward bias condition (i.e., the gate voltage was negative) was larger than that under the reverse bias condition (i.e., the gate voltage was positive).

Fig. 3-13: I - V characteristic of the MIS memory device structure. The insets in the upper-right and lower-left panes show the carrier injection under a reverse bias (i.e., a positive voltage is applied to the Al gate) and a forward bias (i.e., a negative voltage is applied to the gate), respectively.

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This behavior can be explained as follows. Both the electron injection from the Al gate and the hole (the majority carrier in the Si substrate) injection from the p-type Si substrate occurred simultaneously under a negative gate voltage; in contrast, only electron (the minority carrier in the Si substrate) injection from the Si substrate occurred under a positive gate voltage.

As shown in the figure, the reverse I - V characteristic followed a power law, i.e., $I = I_0 V^\zeta$ where the parameters ζ and I_0 were determined by both the structural properties of the oxide thin film and the charge trapping in the thin film [128]. The power-law transport could be explained by a model similar to the one of collective charge transport in arrays of normal-metal QDs [129,130]. The injected electrons can be transported along the tunneling paths formed by the nc- Al distributed in the aluminum oxide thin film [119,128]. This mechanism is used to explain the observed charging-induced changes in the reversed I - V characteristics, which will be discussed in later section. On the other hand, the forward I - V characteristic cannot be described with the above power law, because both the electrons injected from the gate electrode and the holes injected from the Si substrate were to be transported across the aluminum oxide layer.

The energy band diagrams could be helpful for understanding this. Figure 3-14 shows the energy band diagrams of the device under a positive gate bias (i.e., $V_G > 0$) (e.g., in the reverse current measurement) for the situations without charge trapping, with positive charge trapping near the oxide /p- Si interface and with negative charge trapping near the interface, respectively.

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Fig. 3-14: Energy band diagrams of the device under a positive gate bias (e.g., in the reverse current measurement) for the situations without charge trapping, with positive charge trapping near the oxide /p-Si interface and with negative charge trapping near the interface, respectively.

For both the charging experiment and current measurement, under the forward bias condition (i.e., a negative voltage is applied to the Al gate), both electron injection from the Al gate and hole injection from the p-type Si substrate occur simultaneously; and under the reverse bias condition (i.e., a positive voltage is applied to the Al gate), only electron injection from the Si substrate occurs. The injected carriers can be transported along the tunneling paths formed by the nc- Al distributed in the aluminum oxide thin film [131]. The oxide thin film should have a large amount of defects due to the imperfection of the Al_2O_3 matrix embedded with nc- Al , which can act as effective charge trap centers. Some of the transported carriers are trapped in either the nc- Al or the defects in the oxide layer [131,132] and at the same time charge trapping also occurs at the interfaces (either the gate / oxide or oxide / Si substrate interfaces) where the carriers are injected. The situation should be similar to the charge trapping in the gate oxide and at the oxide / Si interface in a MIS structure when carriers are injected at the interface from the Si

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substrate to the gate oxide [133]. The charging trapping in the interface region due to the carrier injection causes a change in the electric field at the interface, which in turn affects the carrier injection [126,135].

In a charging experiment, under the bias of a positive charging voltage, there is electron trapping in the oxide layer as electrons are injected from the *Si* substrate. However, under the bias of a negative voltage, there could be both electron trapping and hole trapping in the oxide layer as both the electron injection from the gate and the hole injection from the *Si* substrate occur simultaneously. The net charge trapping in the oxide layer detected by the *C-V* measurement which is sensitive to the charge trapping near the interface of oxide / *Si* substrate could be either negative or positive depending on the magnitude of the charging voltage and the charging duration. The net charge trapping tends to be positive for a larger magnitude of negative charging voltage as a result of strong hole injection from the p-type *Si* substrate (note that holes are the majority carriers in the substrate). In the charging experiment of the present study, a net negative or positive charge trapping was observed from the *C-V* measurement for a positive or negative charging voltage, respectively.

3.4.2 Power law model

As mentioned in section 3.3.1, the power law model could be used to explain the reversed current conduction which is shown in Fig. 3-15. Empty dots represent uncharged nc-*Al*, shadow ones are charged nc-*Al*, black sticks stand for high resistance tunneling path (high-R), and white sticks are low resistance tunneling paths (low-R). Electron tunneling can take place between adjacent uncharged nanocrystals, and many such

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nanocrystals form conduction paths connecting the Si substrate to the metal gate as shown in the Figure 3-15 (a). In this two-dimensional-transport model, vertical and transverse are two fundamental directions. Between the uncharged nc- Al , there are low-R tunneling paths formed. Low-R path is easier for electron to tunnel from one nc- Al to next nc- Al . With the existence of these tunneling paths formed by uncharged nc- Al , the current conduction of the high-k dielectric thin film is drastically enhanced.

Fig 3-15: Two-dimensional transport model used to explain nc- Al formed a) and broken tunneling path b).

The scenario of the influence of charge trapping in nc- Al on the tunneling paths is shown in Figure 3-15 (b). Electron trapping in one nc- Al will affect the tunneling of other electrons into this nc- Al . The resistance of the tunneling paths involving this nc- Al will increase due to the electrostatic interaction with the electron trapped in the nc- Al . In addition, the tunneling paths could be broken due to the coulomb blockade effect too.

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Therefore, as a result of the charging in nc- Al , the current conduction will decrease because of the decrease in the number of available tunneling paths due to the breaking of some tunneling paths.

Figure 3-16: Sweeping from 0V to 10V/-10V then back from 10V/-10V to 0V and measure current.

In some study, coulomb blockade phenomenon can be detected at the temperature of 0 K during the study of single electron transport [134]. As gate voltage increase by steps of 10-100 mV, the measured gate current shows a staircase increase instead of smooth increase. At room temperature, the charges must be following collective transport, which is different from the behavior of single electron transport. Taking this view into account, the coulomb blockade effect can be applied to explain some phenomenon occurred in our experiment. There are several ways of detecting charge-trapping phenomena. One easy and commonly used method is to use a double sweep in either DC I - V or high-frequency C - V measurements. These techniques involve ramping gate voltage back and forth while

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gate current or gate capacitance is measured. If such hysteresis can be seen on the resulting I - V or C - V curves, it can be inferred that the charge trapping occurs as shown in Fig. 3-16.

Figure 3-16 shows the I - V characteristics when V_{bias} was scanned from 0V to -10V or +10V then back from -10 V or +10 V to 0 V. Each scanning took around 20 seconds. The backward scanning from +10 V to 0 V shows a lower conductivity than the forward measurement. Such a current reduction can be explained in terms of the breaking of some tunneling paths formed by the nc- Al due to electron trapping in certain nanocrystals during the I - V measurement as mentioned in power law model. The positive I - V measurement can cause electron injection from the substrate and some of them are trapped in nc- Al . As we mentioned before, the electrostatic interaction with the trapped electrons make some tunneling paths broken and thus the current is reduced. When V_{bias} increases up to -10 V or + 10V, V_{gate} is high enough to cause charge trapping of nc- Al embedded in dielectric thin film. The paths may be broken as illustrated in Figure 3-15 (b). The increased resistance of tunneling path and coulomb blockade effect may make tunneling difficult and thus current conductivity is reduced. In collective transport, it may not be easy to figure out the number of charges trapped, but the current conductivity should be affected as the tunneling path is broken. Nc- Al can be treated as a charge storage site. For electrons, these nanocrystals are more like their transport islands. When the tunneling occurs, electrons can hop from one nc- Al to adjacent nanocrystal. In each nc- Al , there are several trap states. If these states are fully occupied by electrons, it will be impossible for nc- Al to continuously accept more electrons. In this situation, hopping of electrons is not as easy to happen. The phenomenon is the coulomb blockade effect. It

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refers to the increase of resistance at small bias voltage of an electronic device which comprises at least one low-capacitance tunnel junction. The thin dielectric film could be the simple tunnel junction. When bias voltage is applied, in electrons term, the tunnel junction behaves as a resistor with a constant resistance [135]. In $nc-Al/Al_2O_3$ structure, uncharged $nc-Al$ will form tunneling path with low resistance path build in between and help electrons to tunneling. However if an $nc-Al$ is charged, the tunneling path is blocked due to the coulomb blockade effect [135]. Based on this theory, the reverse current before and after charging could be analyzed as shown below.

Fig. 3-17: I - V characteristics before and after application of + 10 V for 100 s. The lines show the fittings based on Eq. 3.1. $I_0 = 2.4 \times 10^{-6}$ A and $\zeta = 1.22$ before application of the voltage and $I_0 = 8.24 \times 10^{-7}$ A and $\zeta = 1.12$ after application of the voltage.

Typical I - V measurement of Al -rich Al_2O_3 based memory device is shown in Figure 3-17. In this figure, a power law fitting to the I - V characteristics before and after the application of +10 V for 100 s is executed. The current follow the power-law relationship

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$$I = I_0 V^\zeta \quad (3.1)$$

where the ζ is scaling exponent and I_0 is related to initial current. The scaling exponent ζ is 1 and 5/3 for the one- and two-dimensional arrays of quantum dots (QDs), respectively. Equation 3.1 can be used to fit our experimental result of the system of nc- Al embedded in Al_2O_3 matrix. The values of the factors including ζ and I_0 of Equation 3.1 can be obtained from the fitting. However, both ζ and I_0 should depend on a prior application of voltage to the sample. Such dependence can be attributed to the charging in the nc- Al caused by the application of voltage.

Fig 3-18: a) ζ change with accumulated charging time at $V_{gate} = +15$ V and b) $V_{gate} = +10$ V; c) I_0 change with accumulated charging time at $V_{gate} = +15$ V and d) $V_{gate} = +10$ V.

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As shown in Figure 3-18, two different charging voltages +10 V and +15 V are applied with accumulated charging time from 0 s to 1000 s. It is quite obvious that such charge trapping process leads to reduction in both ζ and I_0 .

In Figure 3-18 (a), the charging voltage is kept at +15 V. With charging time increased, ζ shows a decreasing trend. After charging +15 V by 0.1 s, ζ is about 1.744, which is more close to the value of two-dimensional transport. The whole figure can be divided into four domains: in 0.1s domain, ζ decreases from around 1.744 to 1.672; in 1s domain, ζ decreases from around 1.671 to 1.585; in 10s domain, ζ decreases from around 1.573 to 1.424; beyond 100s, ζ decreases from around 1.295 to 1.220. There is a big drop of ζ when charging time approaches 100s. From this result, it is concluded that electrons transport evolves from two-dimensional to quasi-one-dimensional. This can be attributed to the occurrence of some charge trapping. Figure 3-18(c) also shows that the corresponding I_0 will decrease from 8.024×10^{-8} A to 0.478×10^{-8} A with increasing charge trapping. The similar measurement was executed with charging voltage of +10 V as shown in Figure 3-18(b) and (d). In Figure 3-18(b), the increasing of charging time will decrease ζ from around 1.837~1.985 to 1.6. Figure 3-18(d) shows the corresponding I_0 related to Figure 3-18(b) as function of charging time. It can be found that I_0 showed significant reduction with charging time increased.

It is still possible to find out the relationship between charge trapping and current transport property from the results in Figure 3-18, even the charge trapping is a random process. The effect of charge trapping on current transport property (I_0 and ζ) can be explained as below. The lower ζ indicates lower transport dimension, which means that

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there are increasing amount electrons trapped inside nc- Al embedded Al_2O_3 thin film. As the charged nc- Al increased, the current conduction should be reduced due to the coulomb block effect as explained before. In this way, the tunneling paths are broken and the I_0 will decrease with increasing tunneling resistance. It can be concluded that the current conduction of the system is still a quasi-two-dimensional transport, but it evolves with a trend towards the one-dimensional transport when the charge trapping is increased. This evolution is due to the breaking of some transverse tunneling paths as a result of charging trapping in the nc- Al . The charging voltage, polarity and charging time should have effect on current transport and current conductivity.

3.4.3 Conclusion

A two-dimensional transport model [120] can be used to explain the current transport in Al -rich Al oxide based capacitor-type memory device. As uncharged nc- Al will form tunneling path with low resistance between adjacent nc- Al , electrons are easily hopping from metal gate to substrate or in opposite tunneling direction. With the existence of many tunneling paths formed by the nc- Al , the current conduction of the thin film system is drastically enhanced. However, after charging, some nc- Al s are charged, that means their whole trap states are occupied by electrons. These nc- Al s reject to accept any more electrons. In such situation, tunneling path is broken by forming high resistant path between adjacent nc- Al . Current conductivity will be reduced accordingly as electrons are no longer easy to tunnel throughout the dielectric film as a result of the coulomb blockade effect.

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3.5 Write once read many (WORM) memory devices

3.5.1 Introduction

Write-once-read-many (WORM) memory devices have widespread uses in all kinds of permanent archival storage applications, such as wireless identification tags and smart cards, rapid archival storage of video images where the vulnerability to breakage associated with slow and power-hungry magnetic or optical disk drives are not acceptable, etc. WORM memory devices based on organic small molecules and polymers have been reported in recent years [136-141]. WORM memory devices based on all-inorganic materials such as aluminum nitride thin film containing nc-*Al* [142] and *ZrO₂* [143] have also been reported recently. In the present studies, a WORM device was realized based on the charging-controlled modulation in the current conduction of *Al/Al-rich Al₂O₃/p-Si* memory device. It has been reported in previous studies that both electrons and holes can be trapped in the *Al-rich Al₂O₃* thin films and the charge trapping greatly affects the current conduction across the thin films [131,132]. In this work, it is observed that a large increase in the reverse current of the *Al/Al-rich Al₂O₃/p-Si* memory device could be achieved by applying a negative charging voltage to the memory device. Memory states of the WORM device based on the memory device structure could be manipulated with the charging effect. The WORM memory exhibits good reading endurance and retention characteristics.

In this section, the WORM device was realized based on the charging-controlled modulation in the current conduction of *Al/Al-rich Al₂O₃/p-Si* memory device. This is first study about *Al* rich dielectric thin film based WORM device. A large increase in the

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reverse current of the memory device could be achieved with a negative charging voltage (e.g., the charging at -25 V for 1 ms results in a current increase by about four orders). Memory states of the WORM device could be altered by changing the current conduction with charge trapping in the Al -rich Al_2O_3 layer. The memory exhibited good reading endurance and retention characteristics.

3.5.2 WORM memory device based on nc- Al embedded Al_2O_3 thin film

An Al -rich Al_2O_3 thin film was synthesized with a reactive sputtering process has been reported in previous study. A 60 nm Al -rich Al_2O_3 thin film was deposited on a p-type Si substrate by the RF magnetron sputtering of an Al target in the presence of a small amount of O_2 with the flow rate of ~ 1 sccm. A rapid thermal annealing was then conducted at 550°C for various durations ranging from 30 s to 300 s in N_2 ambient. For an aluminum oxide film synthesized with the reactive sputtering process, it is Al -rich as confirmed by the X-ray Photoelectron Spectroscopy (XPS) analysis, and the excess Al forms Al nanocrystals (nc- Al) in the Al_2O_3 matrix as revealed by the cross-sectional Transmission Electron Microscopy (TEM) measurement [131].

An aluminum film of 200 nm was deposited on the surface of the Al -rich Al_2O_3 thin film to form an Al/Al -rich Al_2O_3/p - Si memory device as shown in Fig. 3-19 (a) which is quite similar with the one in section 3.2.3. The area of the memory device is $\sim 3 \times 10^{-4}$ cm². The memory device structure actually serves as a two-terminal WORM memory device in this work. As the WORM device has a memory device structure, its ON and OFF state currents (i.e., the reverse currents of the memory device after and before a charging operation as discussed later) are proportional to the memory device area, and thus the

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currents can be scaled with the device area. Electrical measurements including current-voltage (I - V) and capacitance-voltage (C - V) measurements and the charging operations were carried out with a Keithley 4200 semiconductor characterization system in air at room temperature.

Fig. 3-19: a) Schematic illustration of the WORM device based on the $Al/Al\text{-rich } Al_2O_3/p\text{-Si}$ memory device. B) Reverse I - V characteristics of the memory device before and after the charging at ± 15 V for 1 ms.

The memory device structure exhibited forward and reverse I - V characteristics under a negative and positive gate voltage respectively. It has been observed that the reverse I - V characteristic can be seriously affected by applying a charging voltage to the device. However, the charging voltage has no significant impact on the forward I - V characteristic. For example, Fig. 3-19 (b) shows the reverse I - V characteristics of the memory device before and after the charging at ± 15 V for 1 ms. As seen in the figure, the negative charging voltage leads to a large increase in the reverse current, while the positive charging voltage causes a small reduction in the reverse current. The influence of a charging voltage on the I - V characteristic is related to the influence of the charge trapping

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in the Al -rich Al_2O_3 layer caused by a charging voltage on the carrier transport in a current measurement [131], as discussed below.

The charge trapping produced by the charging experiment could affect the carrier transport during the current measurement. The charge trapping (either electron or hole trapping) does not cause a large change in the forward I - V characteristics because both the electron injection from the gate and the hole injection from the Si substrate are involved in the forward I - V measurement [131]. However, the charge trapping has a significant impact on the reverse I - V characteristics, as shown in Fig. 3-19 (b).

As shown in Fig. 3-19 (b), the application of the positive charging voltage of 15 V for 1 ms, which causes only electron trapping in the oxide, leading to a small reduction in the reverse current. The application of the positive charging voltage of 15 V for 1 ms leads to a net electron trapping in the oxide near the oxide / Si substrate interface. As shown in the energy band diagram for the situation with negative charge trapping near the interface presented in Fig. 3-14, the electron trapping reduces the electric field in the interface region under a positive gate voltage (i.e., the reverse bias condition), thus decreases the electron injection from the Si substrate during the reverse I - V measurement. In addition, the electron trapping can also suppress the electron transport across the oxide layer under the reverse bias condition because of the electrostatic interaction of the transported electrons with the trapped electrons during the reverse current measurement [131]. Therefore, the application of the positive charging voltage leads to a reduction in the reverse current.

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In contrast, the application of the negative charging voltage of -15 V for 1 ms leads to a large increase in the reverse current (e.g., the current measured at +2 V is increased by ~ 2 orders) as shown in Fig. 3-19 (b). The application of -15 V for 1 ms leads to a significant equivalent amount of hole trapping in the oxide near the oxide / substrate interface. The energy band diagram for the situation with positive charge trapping near the interface presented in Fig. 3-14, in the reverse current measurement under a positive voltage, the hole trapping causes an increase in the electric field at the oxide / substrate interface, enhancing the electron injection at the interface during the reverse current measurement. Therefore, a negative charging voltage leads to a large increase in the reverse current. The increase (ΔE) in the electric field in the oxide region near the oxide / substrate interface due to the hole trapping could be estimated from the C - V measurement (note that the C - V measurement is only sensitive to the charge trapping near the oxide / Si substrate interface) by using $\Delta E \approx \Delta V_{FB} / d$ where d is the oxide thickness. ΔE is estimated to be 3.7×10^4 V/cm and 1.1×10^5 V/cm for the charging time of 1 ms and 1 s, respectively, at the charging voltage of -15 V.

As a negative charging voltage can produce a large increase in the reverse current, a two-terminal WORM memory device can be realized based on the change in the reverse current of the *Al/Al-rich Al₂O₃/p-Si* memory device caused by a negative charging voltage. In other words, the memory states are represented by the currents measured at a small reverse bias that will not cause any significant charging in the oxide layer, and the memory states can be altered by using a large magnitude of negative charging voltage (i.e., the writing voltage in the WORM operation). For example, the reverse currents measured at +2 V before and after the charging at -15 V for 1 ms represent two well

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distinguished states (the current ratio of the state after writing to the state before writing is about 200). From previous study, it is known that the reverse current depends on the reverse bias. Therefore, the current ratio of the state after writing to the state before writing also depends on the detection voltage (i.e., the reverse bias). Thus a suitable detection voltage should be chosen to achieve a large current ratio but not to change the charging state. It is also worthy to mention that the charging voltage can be scaled down by using a thinner Al -rich Al_2O_3 layer. For example, if constant electric field scaling law is used, the voltage can be reduced from 15 V to ~ 10 V when the oxide thickness decreases from 60 nm to 40 nm. To demonstrate the feasibility of the WORM application, a study on the memory performance and reliability has been conducted, as discussed below.

Fig. 3-20: Retention characteristics of different memory states. (a) Writing at -15 V for 1 μ s or 1 ms; and (b) writing at -25 V for 1 μ s or 1 ms. The reading voltage is kept at +2 V. There is no significant degradation observed in this measurement.

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Figure 3-20 shows the retention characteristics of the WORM devices. The reading operation (i.e., the reverse current measurement) was carried out at +2 V. Within the time limit of 3×10^4 s in our experiment, the state before writing and the state after writing at different writing voltages (-15 V and -25 V) for different writing time (1 μ s and 1 ms) do not show a significant degradation with time. This indicates that there is no significant loss of the trapped charges and the reading operation at +2 V itself does not cause a significant change in the charge trapping within the time limit.

3.5.3 Retention property of nc-*Al/Al₂O₃* based WORM device on temperature dependence

In industry, the retention application is very important in real applications. The retention property of nc-*Al/Al₂O₃* based WORM device will be discussed in this section. In the previous discussion, it has been pointed out that the negative charging voltage of -15 V produces a large increase in the reverse current but the positive charging voltage of +15 V causes only a small reduction in the current. This means that a written state cannot be easily reverted by a positive charging voltage. This is confirmed by experiment. As shown in Fig. 3-21 (a), the state written at -15 V for 1 ms does not revert to the state before writing after the application of +15 V for 100 s. This also explains why the reading operation at +2 V doesn't significantly change the memory states as discussed above. However, a baking of the charged device at 200 °C for 2 minutes leads to a reversion of the written state to the state before writing, as shown in Fig. 3-21 (b). This indicates that most of the trapped charges associated with the writing process are released from the trap centers after the baking. It is noted that the memory cell can be written

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again after the baking. The release of the trapped charges at an elevated temperature will also affect the retention performance of the WORM device.

Fig. 3-21: Changes of a written state by the application of +15 V for 100 s (a) or the baking at 200 °C for 2 minutes (b). The trapped electrons could release at 200 °C, which cannot be achieved by applying electric field.

Figure 3-22 shows the retention behaviors at various baking temperatures for the memory state written at -25 V for 1 ms. As can be seen in the figure, the retention performance is excellent at room temperature. It is still good at 50 °C for practical

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application as the current ratio of the state after writing to the state before writing is still larger than 5×10^3 after the waiting time of 10^4 s. However, the retention performance degrades significantly at a higher temperature. This means that the WORM device is not suitable for those applications at high temperatures (e.g., $> 50^\circ\text{C}$), which is the limitation of the device. As the memory states are determined by the charge trapping in the oxide layer, their retention performance could be highly sensitive to the temperature depending on the trap depth. The thermal de-trapping process is enhanced when the temperature is increased, leading to a more significant loss of the trapped charges [144]. This explains the significant degradation of the retention performance at an elevated temperature. The possible method to improve this retention and endurance performance is to add the silicon oxide film between the dielectric film and substrate or between dielectric film and the gate. This oxide layer will reduce current releasing from dielectric layer.

Fig. 3-22: Retention behaviors at various temperatures. The waiting time is up to 10^4 s.

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On the other hand, the release of trapped charges at a high temperature suggests that the WORM device can be erased by a baking at a sufficiently high temperature for re-programming. This has been confirmed by experiment. The reversion of the written state to the state before writing by the baking at 200 °C for 2 minutes is shown in Fig. 3-21 (b). The result indicates that most of the trapped charges associated with the written state have been released by the thermal de-trapping process during the baking.

3.5.4 Conclusion

In summary, the reverse current of *Al/Al-rich Al₂O₃/p-Si* memory device can be modulated by the charge trapping in the oxide layer, and such effect can be used to realize the WORM memory. A written state can be achieved by applying a negative charging voltage to the gate of the memory device, and memory states can be distinguished by detecting the reverse memory device current at a small positive voltage. The memory exhibits good reading endurance and retention characteristics at room temperature. At elevated temperature, the retention property is sensitive to the temperature depending on the trap depth, which can be explained by the thermal de-trapping process. The WORM device is a new topic which has similar basic function as ROM (read-only memory). The differences between WORM and ROM is that WORM devices are more two-terminal based and ROM is more like MOSFET based structure.

3.6 Charge-controlled memristor device

3.6.1 Introduction of memristor device

Non-volatile semiconductor memory plays a very important role in our modern digital life. Conventional non-volatile semiconductor memory devices usually have four-terminals and are fabricated on silicon wafers with the complementary metal–oxide–semiconductor (CMOS) technology. Although having a huge commercial success, conventional non-volatile memory devices have their limitations. The most prominent one today is the limited potential for continued scaling of the device structure. Another limitation is the very complex fabrication process, which leads to a high fabrication cost. Due to the second limitation, the conventional non-volatile memories are not suitable for the low-cost archival storage applications. Therefore, it would be attractive to provide non-volatile memory devices that are with simpler structure and fabrication process for the low-cost archival storage applications. The above objective has been realized with the charging-controlled memristor-like memory structure which is based on the charging-controlled modulation in the current conduction of metal/ nanocrystal-dielectric nanocomposite (e.g., metal or semiconductor nanocrystals embedded in a dielectric film such as metal oxide, SiO_2 , Si_3N_4 , AlN , etc.)/p-Si memory devices.

The memristor was generalized to memristive systems in a 1976 paper by Leon Chua. In 2008, a team at HP Labs announced the development of a switching memristor based on a thin film of titanium dioxide [109]. These devices are being developed for application in nanoelectronic memories, computer logic and neuromorphic computer architectures.

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As it is a two-terminal device, the structure as well as fabrication process is much simpler than that of the conventional non-volatile memory devices, leading to a much lower cost. And importantly, the fabrication process of the two-terminal device is fully compatible with the main-stream CMOS process, which is critical because the memory device must be integrated with the controlling circuits, encoders and decoders, etc. on a silicon chip with the CMOS process. No published patents on the similar memory structure have been found. The memory exhibits good reading endurance and retention characteristics. In contrast to conventional non-volatile memory devices, the two-terminal memristor has a much smaller size and can be scaled down to a few nm, and its fabrication process is much simpler. Due to its ultra-low cost and ultra-high device density, it is particularly suitable for permanent archival storage applications, such as wireless identification tags and smart cards, rapid archival storage of video images where the vulnerability to breakage associated with slow and power-hungry magnetic or optical disk drives are not acceptable, etc.

3.6.2 Charge-controlled memristor based on MIS structure

Figure 3-23 shows the current-voltage (I - V) characteristics of the device. As seen in the figure, when the voltage is swept from 0 V to +30 V and then from +30 V to 0 V, the device exhibits a hysteresis with a large difference in the current at a lower voltage (e.g., +5 V). The situation is due to the effect of charge trapping in the active layer caused by the voltage on the reverse current of the memory device structure. The inset of Fig. 3-23 shows the reverse I - V characteristics of the device before and after the charging at ± 15 V for 1 ms. As seen in the inset, the negative charging voltage leads to a large increase in

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the reverse current, while the positive charging voltage causes a small reduction in the reverse current. The influence of a charging voltage on the I - V characteristic is related to the influence of the charge trapping in the nc- Al / Al_2O_3 nanocomposite layer caused by a charging voltage on the carrier transport of the memory device structure under a current measurement, as discussed below.

Under the reverse bias condition (i.e., a positive voltage is applied to the Al gate), only electron injection from the Si substrate occurs. The injected carriers can be transported along the tunneling paths formed by the Al nanocrystals or nanoparticles (nc- Al) distributed in the nc- Al /aluminum oxide nanocomposite thin film. Some of the transported carriers are trapped in either the nc- Al or the defects in the oxide layer [62,63], and at the same time charge trapping also occurs at the interfaces (either the gate / dielectric or dielectric / Si substrate interfaces) where the carriers are injected. The situation should be similar to the charge trapping in the gate oxide and at the oxide / Si interface in a MOS structure when carriers are injected at the interface from the Si substrate to the gate oxide. The charging trapping in the interface region due to the carrier injection will cause a change in the electric field at the interface, which will in turn affect the carrier injection. The charge trapping produced by the charging operation could affect the carrier transport during the current measurement. In particular, the charge trapping has a significant impact on the reverse current.

As shown in the inset of Fig. 3-23, the application of a positive charging voltage of 15 V for 1 ms causes only electron trapping in the oxide, leading to a small reduction in the reverse current. The electron trapping reduces the electric field in the interface region

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under a positive gate voltage (i.e., the reverse bias condition), thus decreases the electron injection from the Si substrate during the reverse I - V measurement. In addition, the electron trapping can also suppress the electron transport across the oxide layer under the reverse bias condition because of the electrostatic interaction of the transported electrons with the trapped electrons during the reverse current measurement [131]. Therefore, the application of a positive charging voltage leads to a reduction in the reverse current. It is noticed that the charging effect only could be observed in reverse biasing. It is mainly because there is only one carrier involved in reverse biasing. A detailed discussion has been done in previous section 3.4.1.

Fig. 3-23: I - V characteristics of the memory structure for the voltage sweepings from 0 V to +30 V and from +30 V to 0 V. The inset shows the reverse I - V characteristics of the device before and after the charging at ± 15 V for 1 ms.

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In contrast, the application of the negative charging voltage of -15 V for 1 ms leads to a large increase in the reverse current (e.g., the current measured at +2 V is increased by ~ 2 orders) as shown in the inset of Fig. 3-23. It has been found that the application of -15 V for 1 ms leads to a significant amount of hole trapping in the oxide. In the reverse current measurement under a positive voltage, the hole trapping causes an increase in the electric field at the oxide / substrate interface, enhancing the electron injection at the interface during the reverse current measurement. Therefore, a negative charging voltage leads to a large increase in the reverse current.

As a negative charging voltage can produce a large increase in the reverse current, various memory states can be realized based on the changes in the reverse current caused by negative charging voltages. In other words, the memory states are represented by the currents measured at a small reverse bias that will not cause any significant charging in the oxide layer, and the memory states can be created by using a large magnitude of negative charging voltage (i.e., the writing voltage in the memory operation). For example, the reverse currents measured at +2 V before and after the charging at -15 V for 1 ms represent two well-distinguished states (the current ratio of the state after writing to the state before writing is about 200). Note that as seen in the inset of Fig. 3-23, the reverse current depends on the reverse bias. Therefore, the current ratio of the state after writing to the state before writing also depends on the detection voltage (i.e., the reverse bias). Thus a suitable detection voltage should be chosen to achieve a large current ration but not to change the charging state. It is also worthy to mention that the charging voltage can be scaled down by using a thinner active layer. For example, if constant electric field scaling law is used, the voltage can be reduced from 15 V to ~ 10 V when the active layer

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thickness decreases from 60 nm to 40 nm. Figure 3-26 shows the typical resistance measurement for charge-control memristor.

Fig. 3-24: Change of the reverse resistance of the memory device measured at + 2 V corresponding to the charging voltage pattern shown in (a).

The pulse applied to memristor is shown in Figure 3-24 (a). The pulse width is fixed as 1 s. As the pulse voltage increased from -5 V to -25 V, the resistance of the nc- Al/Al_2O_3 based memory device is decreased from 10^8 Ohm to 10^6 ohm accordingly. The resistance exhibited time relationship. Figure 3-25 shows the equivalent trapped charge per unit area (ΔQ) at the active layer / Si interface determined from the flat-band voltage shifts in the capacitance-voltage ($C-V$) measurements and the resistance of the device measured at + 2 V as functions of the charging time. It can be concluded from the figure that as the charging time increases, the charge trapping in the active layer increases while the resistance of the device decreases. Therefore, a charging-controlled memristor-like

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memory device is demonstrated as its resistance is controlled by the charge trapping in the active layer.

Fig. 3-25: Equivalent trapped charge per unit area (ΔQ) at the active layer / Si interface and the resistance of the device measured at + 2 V as functions of the charging time. The charging voltage is fixed at - 15 V.

3.7 Summary of this chapter

The current modulation of a two terminal memory device based on Al / Al -rich Al_2O_3 / p -Si MIS structure has been investigated in this chapter. It was observed that electrons were injected from the Si substrate and trapped in the Al-rich Al_2O_3 layer under positive biasing. In contrast, both electron injection from the Al gate and hole injection from the Si substrate occurred under a negative biasing, leading to both electron and hole trapping in the Al-rich Al_2O_3 layer. The electron trapping and hole trapping caused a significant

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reduction and a large increase in the reverse current, respectively. Even the trapping and de-trapping were random processes, the conduction still showed charging time and charging voltage dependence at positive biasing. The charging effect on the reverse current could be used to realize a two-terminal charging-controlled resistive memory based on the MIS structure.

The charge trapping in the oxide layer could be modulated by the reverse current of *Al/Al-rich Al₂O₃/p-Si* memory device, and this effect can be used to realize the WORM memory and charge controlled memristor. A written state can be achieved by applying a negative charging voltage to the gate of the memory device, and memory states can be distinguished by detecting the reverse memory device current at a small positive voltage. The memory exhibited good reading endurance and retention characteristics. However, the resistance of this memory device had charging time dependence which is the fundamental principles for memristor. It is the first time to report a study regarding the charge-controlled memristor based on MIS structure. Such behavior could be explained as the trapped charge will affect the current conduction or the memory states.

Chapter 4 Resistive Switching Properties and Memory Behaviors of Partially Anodized *Al* Films

4.1 Introduction

Resistive Random Access Memory (ReRAM) based on metal oxides is emerging as one of the most promising candidates for the next generation of non-volatile memory due to its superior performance such as fast switching speed, low operating voltage, simple structure, and great scalability potential. The metal oxides including *NiO*, *TiO₂*, *Cu_xO*, *ZnO* and *Al₂O₃* are popularly used for ReRAM [145-150]. Although resistive switching behaviors of these metal oxides have been intensively studied, most of the studies were carried out at room temperature and there are relatively few studies done at elevated temperatures [151-156]. Moreover, for the resistive-switching memory application, a forming process, where switching from the initial state to the low-resistance state, is usually required. Such forming process is not desirable for practical applications as the forming voltage is usually much higher than the set voltage.

In this chapter, we report unipolar resistive switching in a partially anodized aluminum film with no forming process required due to the pre-existing of conductive filaments formed by the excess aluminum in the partially anodized aluminum film. Metal-Insulator-Metal (MIM) structure was fabricated by partially anodizing aluminum film followed by deposition of another aluminum film. Unipolar resistive switching

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between a high-resistance state (HRS) and a low-resistance state (LRS) with a high resistance ratio ($> \sim 10^4$) was observed with the structure. The switching occurred without the requirement of a forming process, which was attributed to the pre-existing conductive filaments in the *Al*-rich Al_xO_y layer formed by anodization. Each resistance state at low fields exhibited ohmic behavior, which could be explained by the metallic conduction and electron hopping from one isolated state to the next in the *Al*-rich Al_xO_y layer. The MIM structure was tested to show good memory characteristics. The Arrhenius behavior suggests that the resistive switching is related to thermally-activated solid-state diffusion and or electrochemical reactions. The pulse voltage experiment also shows that the electrical energy required for the conductive filament breaking / reconnection is lower at a higher temperature. At elevated temperatures in the absence of electric fields, while the high resistance state exhibited no significant change with time, the low-resistance state showed a continuous degradation and there was a sudden failure occurred.

4.2 Sample fabrication and device structure

4.2.1 Aluminum oxidation method

The *Al*-rich aluminum oxide thin film was fabricated by solution-based oxidation method which is a traditional method to produce dielectric films for large scale devices. In our study, the sample was fabricated on a p-type silicon supporting substrate. After depositing the top electrode, a metal-insulator-metal (MIM) structure was formed. Detail of the fabrication is described below. The diagram of anodization setup for our device is shown in Fig. 4-1:

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Fig. 4-1: Diagram of aluminum anodization setup. The anode is the sample with 500 nm aluminum film deposited on p-Si substrate. The cathode is $2 \times 2 \text{ cm}^2$ Pt mesh. The electrolyte is 0.15 M/L oxalic acid.

As shown in Fig. 4-1, 500 nm *Al* thin film was deposited on a supporting p-type silicon substrate, which was thermally oxidized to form a 10 nm silicon dioxide layer prior to the *Al* thin film deposition. The *Al* thin film deposition was carried out by DC sputtering of an *Al* target with a purity of 99.99%. Anodization of the *Al* thin film was carried out in a 0.15 M/L solution of oxalic acid at 25 °C with a constant voltage of 40 V using a Keithley 2400 source meter with a $2 \times 2 \text{ cm}^2$ platinum mesh as the cathode. The anodizing time takes about two hours. The thickness of the aluminum oxide layer formed is about 30-50 nm.

4.2.2 Sample characterization

The SEM image in Fig. 4-2 (a) shows the surface structure of the anodized thin film. The porous structure revealed by the SEM image indicates that the aluminum film was anodized. The TEM image in Fig. 4-2 (b) confirms that such oxidation process was not

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complete and the aluminum film was partially anodized. The unreacted aluminum acts as the bottom electrode. From the result, the thickness of the anodized aluminum oxide film, i.e., *Al*-rich Al_xO_y layer, is around 30-50 nm. The X-ray photoelectron spectroscopy (XPS) analysis in Fig. 4-2 (d) indicates that the aluminum oxide layer is an *Al*-rich Al_xO_y layer with the ratio of $Al : Al_2O_3 = 1 : 1.16$. This confirms that the oxide layer contains a lot of unreacted *Al*. It should be pointed out that the binding energies of *Al* and Al_2O_3 of the anodized aluminum oxide film obtained from the XPS measurement shown in Fig.4-2(d) are slightly different from those of the Al_2O_3 film synthesized by RF sputtering shown in Fig.3-2(a). The possible reasons are explained in the following. XPS measure the kinetic energy of all collected electrons. The electron signal includes contributions from both photoelectron and Auger electron ones. The binding energy of the electron is just the difference between the final state and initial state energies of the target atom. Such energy could be expressed as the energy for the orbital on an isolated atom, plus a shift to allow for bonding in a molecule. Therefore, the differences in the binding energies of *Al* and Al_2O_3 between the XPS result shown in Fig. 3-2 (a) and the XPS result shown in Fig. 4-2 (c) can be due to the following factors: 1. The surface charging effect induced by photoemission depends on the experimental conditions (e.g. X-ray intensity) and the sample surface structures. The sample in Fig. 3-2 (a) is a *Al*-rich Al_2O_3 thin film deposited by RF sputtering; while the sample in Fig.4-2(d) is anodic *Al* oxide layer which has a porous structure. Although we have tried to make the correction for the surface charging effect by taking the carbon signal on the sample surface as the reference, some errors may still exist as the charging effect varies with the probing depth. 2. The atomic

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environment of the two samples is not the same. On the other hand, the existence of nc-Al is demonstrated by the selected-area-diffraction (SAD) pattern shown in Fig.4-2(c).

Fig. 4-2: a) Surface SEM image of the anodized aluminum thin film. The porous structure with diameter of around 200 nm could be observed; b) cross-sectional high resolution TEM image of the anodized aluminum thin film; c) SAD image of the anodized aluminum thin film; and d) XPS result of the anodized film.

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4.2.3 Device structure

Fig. 4-3: Structure of Al-rich anodized aluminum oxide based metal-insulator-metal (MIM) memory device. The anodized film is about 30-50 nm. The top electrode pad is a 300 nm pure aluminum thin film with diameter of 200 μm .

After oxidation, 300 nm Al was deposited on the anodized aluminum film as the top electrode. As shown in Fig.4-3, a symmetric Al/anodized aluminum oxide/Al MIM structure was formed on the top of the p-type silicon substrate. The diameter of the top electrode pad is about 200 μm .

4.3 Resistive switching phenomena and mechanisms

4.3.1 A brief introduction to unipolar and bipolar resistive switching

In a resistive switching process, an electrical field switches the resistance reversibly between a high-resistance state (HRS) and a low-resistance state (LRS) [157]. Based on the dependence of the operation voltage polarity, resistive switching can be classified as bipolar resistive switching (BRS) and unipolar resistive switching (URS) [158]. BRS and

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URS mean that the set and reset process occurred at the same or different voltage polarity, respectively. Normally, the BRS could be caused by the ion diffusion which depends on the voltage polarity. On the other hand, the URS is more related to the connection/breaking of conductive filaments, which is independent of the electric field direction. The interesting thing is that the BRS and URS may exist in the same kind of metal oxides with different metal-oxide components [159]. The true mechanism behind this phenomenon is still not clear.

4.3.2 Unipolar switching without forming process of the *Al* / anodized aluminum / *Al* MIM structure

With the anodized aluminum thin film MIM structure, a unipolar switching without forming process was observed. The forming process is used to switch a device from an insulating phase to a resistive switching phase. In general opinion, the forming process was explained as introducing more oxygen vacancies or defects into a dielectric thin film. The forming process is an obstacle in real applications as the forming voltage is usually much larger than the set voltage. With the anodized aluminum thin film MIM structure, the forming process is not required, because the pre-existence of *Al* has already formed conductive filaments (CFs).

Figure 4-4 (a) shows the typical unipolar switching characteristics of the MIM structure. By sweeping the voltage applied to the top electrode from 0 V to + 1.1 V with a 1 mV step, a bistable resistive switching was observed. As the biasing voltage was increased to a certain voltage (V_{reset}) with a current compliance of 0.1 A, a sudden drop of

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current appeared (the current dropped from $\sim 10^{-2}$ A to $\sim 10^{-8}$ A), i.e., the so-called “reset” process occurred, without any prior forming process. In the reset process the resistance was switched from a low-resistance state (LRS) to a high-resistance state (HRS) and then the sample maintained at the HRS.

Fig. 4-4: a) Typical I - V curve of unipolar resistive switching under positive bias. The inset shows the I - V curve under negative bias. b) I - V curve after 10 switching cycles.

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In the second voltage sweeping starting from 0 V with a smaller current compliance of 0.01 A that was to set to avoid any hard breakdown in the anodized film, the HRS was maintained until the voltage was increased to certain value (V_{set}), at which an abrupt increase of current appeared. This process is known as the “set” process defined as the resistive transition from the HRS to the LRS. The reset and set processes were highly reproducible.

The above results are based on vertical measurement, which measured the I - V characteristics between the top and bottom electrodes. For our device, the switching phenomenon can also be observed between two neighbor top electrode pads. The results are shown in Fig. 4-5.

Fig. 4-5: Lateral I - V measurements between two neighbor top electrode pads at room temperature. The device exhibited stable unipolar switching properties. The inset shows the device structure with the arrow indicating the current flow direction.

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In Figure 4-5, the lateral measurement was executed between adjacent top electrodes at room temperature. The inset of figure shows the device structure and the arrow indicates the current flow direction. After 10 cycles, the switching did not show significant degradation. Compared to the case of the vertical measurement in Figure 4-4 (a) and (b), the set voltage in the lateral measurement is larger than that in the vertical measurement, which may be attributed to the difference in the current traveling distance.

Figure 4-6: Force-current-measure-voltage (V - I) measurement on the MIM structure. When the current increases to $\sim 10^{-6}$ A, the measured voltage suddenly drops from 1.5 V to 0.6 V, showing a switching from the HRS to LRS.

Voltage driving is a commonly used method to program the resistive switching memory. However, the current driving is also possible for device switching. Figure 4-6 shows the force-current-measure-voltage (V - I) measurement on the MIM device. From this figure, the switching behavior can be observed also. At the beginning, the measured

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voltage increased with the biasing current. However, when current increased to 10^{-6} A, the measured voltage changed from 1.5 V to 0.60 V, indicating that the device switching from HRS to LRS occurred. Normally, a resistive switching device should exhibit switching properties in both force-current and force-voltage measurement. The conductive filaments model is usually used to explain the switching phenomena of metal oxide thin films. In this model, the connection/breaking of a conductive filament inside an oxide film at certain voltages makes the oxide resistance decreased/increased. Detail of the conductive filaments model is discussed below.

4.3.3 Conductive filaments (CFs) model

Resistive random access memories (ReRAM) are candidates for future nonvolatile random access memories (RAMs). Their functioning is based on the ability to switch between high and low resistance states. However, the physical mechanism responsible for the low resistivity remains a mystery. Switching between these high and low resistance states can then be programmed by the application of appropriate voltage/current pulses, thereby forming the basis of a nonvolatile memory element. For the resistive switching device, voltage or current pulses are applied to a transition metal oxide. The formation and rupture of a conductive filament through the oxide is suggested to explain the resistive switching especially for metal oxide film. This model is so-called conductive filament model which could be used for both bipolar and unipolar switching with different driving mechanisms. However, the conduction mechanism and the characteristics of the filaments are still poorly understood. Further information concerning the structure, size and chemical composition of these filaments are needed to

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efficiently control and optimize the resistive switching behavior of ReRAM. A simple graph of CFs model is shown in Fig. 4-7.

Fig. 4-7: Ketch depicting a) connected conductive filament and b) broken conductive filament within an Al_xO_y based ReRAM.

The processes of CFs formation and rupture may relate some thermochemical or electrochemical reaction which is still not clear. Fig.4-8 is a reset model which indicated the reset operation is driven by the Joule heating during the application of an electrical pulse. The thermal origin of the reset process can be explained by thermally activated dissolution and/or oxidation of the CF. This is schematically shown in Fig. 4-7: The application of a voltage results in an increased in temperature due to Joule heating, leading to thermally activated loss of conductive species. Note that the major heating takes place close to the middle of the CF due to the approximately parabolic temperature profile in the CF during the applied electrical bias. The thermal induced decrease of the CF cross section (Fig. 4-8 (b)) eventually culminated in an electrical opening between the two ends of the conductive bridge, thus reestablishing the HRS (Fig. 4-8(c)).

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Fig. 4-8: Schematic for the thermally activated dissolution process at the origin of the reset transition. The application of a voltage results in a significant current flowing through the CF. Joule power causes heating in the filament, resulting in (a) a thermally driven diffusion/oxidation of conductive species from the CF. This results in (b) the CF size reduction, eventually culminating in (c) the CF collapse at reset (from Ref. [161]).

However, it is difficult to explain the set process by using the joule heating model as the CFs have been broken already. It is more like reduction occurred between CFs and oxide film which make CFs change from metallic phase to oxidized phase. Figure 4-9 is the electrochemical model to explain the mechanism behind the formation and rupture of the filaments. With the electrochemical effect, the formation of conductive filaments is due to redox reactions in solid state electrolytes as shown in Fig. 4-9 [162-164]. The formation of conductive filaments in this case involves the following steps: (i) When a positive voltage is applied on the oxidized anode, an electrochemical reaction occurs in the anode, which oxidizes the anode metal atoms to metal ions; (ii) the highly mobile cations drift in the ion conductive layer under the electrical field; and (iii) the metal ions are deoxidized back to metal atoms at the inert cathode. As this process continues,

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metallic filaments are established between the two electrodes and the device switches to LRS. Figure 4-9 shows a sketch of the formation and rupture of *Al* conductive filaments based on the electrochemical effect [165].

Fig. 4-9: The formation and rupture of *Al*-conductive filaments explained by the electrochemical effect. Set process and reset process are shown in a) and b) separately.

No matter it is a thermochemical or an electrochemical effect, the most prominent feature in the filament model is a linear relationship between current and voltage, similar to the ohmic characteristic. The switching behaviors of *Al* rich anodized aluminum thin film observed in previous section could be explained with the conductive filament (CF) model which is shown in Figure 4-8 and Figure 4-9. As revealed by the XPS analysis, there was a high concentration of metallic aluminum existing in the *Al*-rich Al_xO_y layer. The metallic aluminum pre-formed the CFs, yielding the initial LRS. This explains why no prior forming process was required for the reset / set processes. The pre-existing CFs,

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which were formed by the excess aluminum in the Al_xO_y layer, were alternatively connected and disconnected during the set/reset operation, and the situation, could be somewhat different from that of other metal oxides. A high current was produced at a small voltage due to a large number of the pre-existing CFs. The sudden increase of resistance at the reset transition is attributed to the dissolution of some of the CFs as a consequence of Joule heating caused by the high current or oxidation of CFs occurred. In the set process, some of the broken CFs could be reconnected and or new CFs could be formed as a result of electrochemical reactions such as reduction reactions occurring in the Al -rich Al_xO_y layer under the influence of both the electric field and the electron injection from the cathode.

4.4 Temperature dependence of switching behaviors

Most of the studies on resistive switching in transition metal oxides reported in the literature were carried out at room temperature, and there are relatively few studies at elevated temperatures. In this work, we have conducted a study of the resistive switching behaviours of the partially anodized aluminium thin film at elevated temperatures (25 °C~250 °C). Both the reset and set voltages decrease with increasing temperature and exhibit Arrhenius dependence. The pulse voltage experiment also shows that the conductive filament breaking / reconnection are easier to occur at a higher temperature. Some possible mechanisms for the phenomena are discussed.

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Fig. 4-10: I - V characteristics of resistive switching at the temperatures of 25 °C and 125 °C: (a) at initial measurements; and (b) after 10k set/reset cycles.

Figure 4-10 (a) shows the repeated I - V measurements at temperatures of 25 °C and 125 °C. The I - V measurements were carried out by voltage sweeping starting from 0 V with the step of 1 mV. The reset and set switching can be observed at both 25 °C and 125 °C during the voltage sweeping. As can be observed in Fig. 4-10 (a), the temperature has a significant effect on the reset and set voltages (V_{reset} and V_{set}) and the currents at the

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LRS and HRS as well. Both the V_{reset} and V_{set} at 125 °C are significantly lower than that at 25 °C. As the temperature increases, the currents at the LRS decreases, showing the metallic behaviour; while the current at the HRS increases, showing the semiconductor behaviour [159]. The above switching behaviour and temperature dependence are also observed after 10^4 set/reset cycles, as shown in Fig. 4-10 (b). Indeed, the set/reset cycling does not cause large device degradation, as demonstrated by Fig. 4-11 which shows the V_{reset} and V_{set} measured from the voltage sweeping experiment as a function of the number of set/reset cycles.

Figure 4-11: Set and reset voltages as a function of number of set/reset cycles at 25 °C.

Temperature dependence of both V_{reset} and V_{set} has been measured on 10 devices in the temperature range of 25 – 200 °C, and the result is shown in Fig. 4-12. It can be observed that both V_{reset} and V_{set} significantly decrease with increasing temperature. Note

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that the change in the voltage drop in the contacts and metal connection with temperature is insignificant (the voltage drop is estimated to increase by less than 2 mV under the current of 10 mA when the temperature is increased from 20 °C to 120 °C). The significant reductions in V_{reset} and V_{set} imply that the CFs are easier to be formed and ruptured at a higher temperature. The phenomenon of decrease of set/reset voltage with increasing temperature was also observed on HfO_x thin film [159]. However, we should notice the difference between the two material systems: the HfO_x thin film required a forming process and showed bipolar switching; in contrast, the partially anodized aluminum thin film of the present study doesn't require a forming process and its switching is unipolar.

According to the joule heating reset model, the decrease of the V_{reset} with temperature could be explained as follow: in the reset process, a higher ambient temperature makes more thermal energy produced by the joule heating to be dissipated in the CFs, and thus the CFs are easier to break up [150,160]. It was also suggested that as temperature increases, both the probability to create oxygen vacancies and the oxygen ion mobility increase, therefore a reduced electrical field (and thus a lower reset/set voltage) is required to break/re-connect the CFs in the reset / set process [162]. In the set process, the electrical field can cause oxygen ions to be removed from their original lattice, leading to the oxygen vacancy-related filament formation; in the reset process, oxygen ions can move to the oxygen vacancy sites, making the filament broken. Therefore, the creation of oxygen vacancies and the movement of the oxygen ions to the oxygen vacancy sites could play a dominant role in the set and reset processes, respectively. As

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both processes are enhanced by temperature, a lower reset/set voltage is required at a higher temperature. As can be observed in Fig. 4-12, the temperature dependence of V_{set} is stronger than that of V_{reset} , which could be due to the factor that the temperature effect on the oxygen vacancy creation is more significant than that on the oxygen ion mobility.

Fig. 4-12: Temperature dependence of the reset and set voltages.

On the other hand, the electrochemical reactions including oxidation and reduction involved in the reset/set process could be also enhanced at a higher temperature, leading to a lower reset/set voltage. Therefore, multiple mechanisms could be responsible for the observed temperature dependence of the reset and set voltages shown in Fig. 4-12. If a

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thermally activated process such as solid-state diffusion/migration and electrochemical reactions is involved in the set/reset process, Arrhenius behaviour could be observed.

Fig. 4-13: Arrhenius plots of the reset and set voltages a) before and b) after 10 k set/reset cycles. The activation energies for set and reset process are around 60 meV.

Fig. 4-13 shows the Arrhenius plots of the average values of the set and reset voltages measured on 10 devices. As can be observed in Fig. 4-13, although there could

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be more than one mechanisms involving in the set and reset processes, the average values of the set and reset voltages are approximately proportional to $\exp(E_a/kT)$ where k is the Boltzmann constant, T is the absolute temperature, and E_a is the activation energy. The activation energies for both the set and reset voltages are ~ 60 meV. The physics for the small activation energies is not clear yet. The temperature dependence of the average values of the set and reset voltages after 10^4 reset/set cycles are also shown in Fig.4-13(b). There are no large changes in both the temperature dependence and the values of the set and reset voltages after the 10^4 reset/set cycles, indicating that the reset/set cycling does not have a large impact on the reset/set process.

Temperature-enhanced reset / set switching is also observed in the pulse voltage experiment. Figure 4-14 shows the influence of temperature on the set / reset switching of one device under various pulse voltages / pulse widths. As can be observed in the figure, stable switching (i.e., the device can switch to the opposite resistance state definitely), unstable switching (i.e., the device has a probability to stay in its current resistance state) and no switching (i.e., the device keeps in its current resistance state without conduction transitions) can be observed depending on the pulse voltage, pulse width and temperature. Obviously, a higher pulse voltage facilitates the set / reset switching to occur in a shorter time. On the other hand, the pulse voltage / pulse width required for a stable switching is smaller at a higher temperature, showing that thermal energy can significantly enhance the set/reset switching triggered by a voltage pulse.

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Fig. 4-14: Set switching (a) and reset switching (b) at 25 °C and 100 °C under various pulse voltages / pulse widths.

In summary, the resistive switching in the *Al*/anodized aluminum oxide/*Al* thin film structure showed strong temperature dependence. LRS exhibited metallic conductor

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behavior (i.e., the resistance increased with increasing temperature); however, HRS showed semiconducting behavior (i.e., the resistance decreased with increasing temperature). Both the V_{reset} and V_{set} decrease with increasing temperature, showing Arrhenius dependence with small activation energies. No large change in the set/reset voltage and the temperature dependence is observed after 10^4 set/reset cycles. The pulse voltage experiment also suggests that the CF breaking / reconnection is easier to occur at a higher temperature.

4.5 Conduction mechanisms of LRS and HRS

Up to now, most of the reported works about resistive switching in metal oxides have mainly focused on the switching behaviors and mechanisms [153-159]; few works have investigated the conduction behaviors and mechanisms of the low resistant state (LRS) and high resistant state (HRS) [160-164], particularly at elevated temperatures. A good understanding of the current conduction in different resistance states would help to understand the physics behind the resistive switching phenomena, and it is also necessary to the RRAM applications. In this work, we have conducted a study of the conduction behavior of the LRS and HRS in the aluminum / partially anodized aluminum film structure at elevated temperatures. Various conduction mechanisms have been identified based on the temperature and field dependence of the current conduction.

As pointed out early, low-resistance state (LRS) shows ohmic conduction with a metallic behavior similar to that of pure aluminum. The situation can be explained by the

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existence of the metallic filament formed by the excess *Al* in the *Al* oxide. On the other hand, the high-resistance state (HRS) shows two distinct regimes: ohmic conduction at low fields with a semiconductor behavior; and a non-ohmic conduction at high fields. The ohmic conduction of HRS at low fields is attributed to the electron hopping between the states in the oxide with the activation energy of ~ 0.23 eV. It is shown that the conduction of HRS at high fields is due to the field-enhanced thermal excitation of the electrons trapped in the states of the metallic *Al* nano-phase into the conduction band of the *Al* oxide or the electron emission from the potential well of the metallic *Al* nano-phase to the conduction band.

Figure 4-15 shows the current-voltage (I - V) characteristics of both the LRS and HRS at room temperature (25 °C). Note that the applied biasing voltage must be lower than the reset voltage and the set voltage which are dependent on temperature and vary from device to device for the LRS and HRS measurements. As shown in Fig. 4-15 (a), the LRS exhibits perfect ohmic conduction with the resistance of $6\ \Omega$ at room temperature. However, as can be observed in Fig. 4-15 (b), the current conduction of the HRS first follows the ohmic law at low fields (the voltage is lower than ~ 0.4 V) with the resistance of $2.8 \times 10^4\ \Omega$ at room temperature and then there is a departure from the ohmic conduction at high fields (the voltage higher than ~ 0.4 V). This indicates that there are at least two conduction mechanisms involved in the current conduction of the HRS, depending on the voltage applied.

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Fig. 4-15: a) *I-V* characteristics of LRS (a) and HRS (b) at 25 °C.

Figure 4-16 shows the temperature dependence of the LRS ohmic resistance in the temperature range of 25 - 125 °C. The resistance increases with temperature, showing the

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behavior of a metallic conductor. In fact, the resistance is a liner function of temperature with the temperature coefficient of $4.1 \times 10^{-3} \text{ }^{\circ}\text{C}^{-1}$, which is close to the value ($3.9 \times 10^{-3} \text{ }^{\circ}\text{C}^{-1}$) of pure aluminum. This indicates that the ohmic conduction of the LRS is due to the existence of the metallic filament formed by the excess *Al* phase. Note that, as reported in our previous work [151], there is a high concentration of excess metallic aluminum in the anodized aluminum layer. In this case, as temperature increases, the scattering of the electrons transported in the *Al* filament by the phonons of the *Al* phase increases, leading to an increase in the resistance.

Fig. 4-16: LRS resistance versus temperature.

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Fig. 4-17: a) HRS resistance at a low field versus temperature; and b) Arrhenius plot of the HRS current at a low field. Both the resistance and current measurements were conducted at 0.2V.

In contrast to the metallic behavior of ohmic resistance of the LRS, the ohmic resistance of the HRS at low fields exhibits a semiconductor behavior, i.e., the resistance

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decreases with temperature, as shown in Fig.4-17 (a). To understand the semiconductor behavior, the Arrhenius plot of the HRS current at the voltage of 0.2 V is shown in Fig. 4-17 (b). The linear plot indicates that the ohmic characteristic is exponentially dependent on temperature, i.e., the resistance $R \sim \exp(\Delta E_a/k_B T)$ where ΔE_a is the activation energy, k_B is the Boltzmann constant and T is the absolute temperature. The activation energy yielded from the plot is 0.233 eV. Therefore, the current conduction of the HRS at low fields can be explained as follows. In the HRS, although the metallic filament is broken, a small current is carried by thermally excited electrons hopping from one state (e.g., the shallow defect states in the *Al*-rich aluminum oxide) to the next at low fields at high temperatures, yielding an ohmic conduction with the shallow trap depth of 0.233 eV. As the thermal excitation process is enhanced at higher temperature, the ohmic resistance decreases with temperature.

As pointed out early, the conduction of the HRS at high fields departs from the ohmic conduction. The conduction could be limited by a bulk effect or an interface effect. Poole-Frenkel (PF) emission is a mechanism of bulk effect that is frequently used to describe the leakage conduction in insulators [165]. It is due to field-enhanced thermal excitation of electrons trapped in the insulator (e.g., the *Al* oxide in the present study) into the conduction band of the insulator. On the other hand, Schottky emission (SE) is an interface-limited mechanism, which describes the field emission of hot electrons from a metal to the conduction band of an insulator in contact with it [166]. In the *Al* film/*Al*-rich *Al* oxide/*Al* film structure of the present study, the SE can occur at both the oxide/ *Al* film interface and the interface between the oxide and the *Al* nano-phase (e.g., *Al*

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nanoparticles) embedded in the oxide. The strong temperature dependence of the conduction of the HRS at high fields observed in the present study suggests that other conduction mechanisms including the space-charge limited current as well as direct or Fowler–Nordheim tunneling currents can be excluded as the main conduction mechanisms. In order to determine whether the P-F emission or SE is responsible for the conduction of the HRS at high fields, a detailed data analysis has been carried out, as discussed below.

The I - V relationship of the PF emission can be described by

$$I = SC \frac{V}{d} \exp \left\{ -\frac{q}{k_B T} \left[\Phi_{PF} - \sqrt{\frac{qV}{d\pi\epsilon_0\epsilon_i}} \right] \right\} \quad (4.1)$$

where S is the contact area, C is a constant, d is the film thickness, q is electronic charge, $q\Phi_{PF}$ is the depth of the trap's potential well, ϵ_i is the dynamic dielectric constant, and ϵ_0 is the vacuum permittivity.

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Fig. 4-18: Current conduction of high resistance state (HRS) at high fields: a) plots of Poole-Frenkel emission; and b) Arrhenius plots of $\ln(I/V)$ at different voltages.

According to Eq. (4.1), $\ln(I/V)$ should be a linear function of $\sqrt{V}$. Indeed, in the small voltage range of 0.55 – 0.75 V (the small voltage range is chosen to avoid any

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switching process), a weak linear dependence of $\ln(I/V)$ on $\sqrt{V}$ is observed, as shown by the PF plots in Fig. 4-18(a). As can be observed in Fig. 4-18(b), $\ln(I/V)$ also shows the Arrhenius behavior for different voltages. The activation energy, $\Delta E_{PF} = q(\Phi_{PF} - \sqrt{\frac{qV}{4\pi\epsilon_0\epsilon_i}})$ for the PF emission obtained from the Arrhenius plots is about 0.43 eV for different voltages in the small voltage range.

On the other hand, Schottky emission can be expressed as

$$I = SA^*T^2 \exp \left\{ -\frac{q}{k_B T} \left[\Phi_B - \sqrt{\frac{qV}{4\pi\epsilon_0\epsilon_i}} \right] \right\} \quad (4.2)$$

where A^* is a constant and $q\Phi_B$ is the barrier height. Obviously, $\ln(I)$ should have a linear dependence on $\sqrt{V}$. As shown in Fig. 4-19 (a), the SE plots (i.e., $\ln(I)$ versus $\sqrt{V}$) indicate that $\ln(I)$ indeed increases linearly with $\sqrt{V}$. As shown in Fig. 4-19 (b), $\ln(I)$ also exhibits the Arrhenius behavior for different voltages. The activation energies, $\Delta E_{SE} = q(\Phi_B - \sqrt{\frac{qV}{4\pi\epsilon_0\epsilon_i}})$ for Schottky emission obtained from the Arrhenius plots at various voltages are about 0.40 eV. Obviously, the field dependence of the activation energies for both PF emission and Schottky emission cannot be clearly observed in the measurements due to the narrow voltage range chosen as a result of avoiding any switching process. Nevertheless, it can be concluded that the activation energies for the PF emission and the Schottky emission are about the same.

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Fig. 4-19: Current conduction of high resistance state (HRS) at high fields: a) plots of Schottky emission; b) Arrhenius plots of $\ln(I/T^2)$ at different voltages.

The above analysis indicates that both PF emission and Schottky emission can well describe the current conduction of the HRS at high fields and have about the same activation energies. The situation can be explained as follows. The metallic *Al* nano-

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phase (e.g., *Al* nanoparticles or nanowires) embedded in the *Al*-rich Al_xO_y layer plays an important role in the conduction of the HRS at high fields. As shown in Fig. 4-20, the PF emission can occur due to the field-enhanced thermal excitation of the electrons trapped in the states of the metallic *Al* nano-phase into the conduction band of the *Al* oxide. On the other hand, the metallic *Al* nano-phase forms a potential well, and the electron emission from the potential well to the conduction band of the *Al* oxide can also be described by the Schottky emission.

Fig. 4-20: Schematic diagram for the PF emission and Schottky emission in the system of metallic *Al* nano-phase embedded in the *Al* oxide.

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In summary, the LRS shows ohmic conduction with a metallic behavior similar to that of pure aluminum, which can be explained by the existence of the metallic filament formed by the excess *Al* in the *Al* oxide. The conduction in the HRS exhibits two distinct regimes: ohmic conduction at low fields with a semiconductor behavior; and a non-ohmic conduction at high fields. The ohmic conduction of HRS at low fields is attributed to the electron hopping between the states in the oxide with the activation energy of ~ 0.23 eV. It is shown that the conduction of HRS at high fields is due to the field-enhanced thermal excitation of the electrons trapped in the states of the metallic *Al* nano-phase into the conduction band of the *Al* oxide or the electron emission from the potential well of the metallic *Al* nano-phase to the conduction band.

4.6 A reliability study of the resistive switching memory

A ReRAM can be switched between HRS and LRS frequently. Each operation can introduce permanent damages, normally referred to as degradation. Endurance, also called electric fatigue, is the number of set/reset cycles that can be endured before HRS and LRS are no longer distinguishable. To gain an advantage over Flash memory, which shows a maximum number of write cycles between 10^3 and 10^7 , depending on the type, ReRAM should provide at least the same endurance, preferably a better one. The retention time means the length of time a memory cell will stay in one state after programming or erasing, indicates the intrinsic ability of a memory cell to retain its content. Most commercially available products are guaranteed to retain information for at

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least 10 years, either with the power on or off. In this section, a study of the reliability of the resistive switching memory based on the partially anodized Al films is reported.

Fig. 4-21: Variation in resistance for both the LRS and HRS with number of reset/set cycles. The resistance was measured at 0.2 V. The inset shows the distributions of both V_{reset} and V_{set} .

Figure 4-21 shows the variation in resistance for both the LRS and HRS with the number of switching (set/reset) cycles. To minimize the influence of the electrical field during the resistance measurement, the resistance was measured at as low as 0.2 V ($< V_{reset}$). The resistance ratio of the HRS to the LRS is larger than $\sim 10^4$. The large memory window easily satisfies the requirement for distinguishing the two states in memory

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application. The inset of Fig. 4-21 shows the distributions of both V_{reset} and V_{set} . The distribution of V_{reset} was quite narrow (around 0.4 ~ 0.5 V), the distribution of V_{set} was relatively larger (around 1.0 ~ 1.4 V), but a window of ~ 0.5 V between the V_{reset} and the V_{set} was still achieved. As shown in Fig. 4-21, the resistance of the HRS was not as stable as that of the LRS, which is probably due to the formation/disconnection of some local conductive filaments in the case of HRS. This phenomenon has been commonly observed in ReRAM devices, and it is one of the disadvantages ReRAM devices.

In the meantime, both the HRS and the LRS are stable over time before switching occurring, as can be seen in Figure 4-22 which shows the retention property for both the HRS and LRS. The device also has a very good reading endurance for both the HRS and LRS, as shown in Fig. 4-23. The results shown in Figs. 4-22 and 4-23 indicate that the MIM structure in this study is promising in the ReRAM application in terms of its reliability performance.

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Fig. 4-22: Stability of the LRS and HRS resistance over time up. The reading voltage is 0.2 V.

Fig. 4-23: Reading stability of both the LRS and HRS. The current was measured at 0.1 V, and the time period corresponding to 100 readings was about 200 s.

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At elevated temperatures without continuous electric field applied, while the high-resistance state (HRS) exhibited no significant change with time, the low-resistance state (LRS) showed a continuous degradation and there is a sudden failure. The LRS failure time showed Arrhenius dependence with the activation energy of ~ 1.3 eV, suggesting that the LRS failure could be due to the migration of the excess *Al* atoms at high temperatures.

Figure 4-24 shows the retention experiment of the LRS and HRS at 25 °C and 200 °C. At 25 °C, both the HRS and LRS exhibit no significant change within the time limit (10^5 s) of the experiment; however, at 200 °C, while the HRS also exhibit no significant change, the LRS shows a continuous degradation with time and there is an abrupt increase (by $\sim$ two orders) in its resistance after $\sim 2 \times 10^4$ s. Such situation is regarded as a retention failure as it is difficult to distinguish the LRS from the HRS now. It is worth to mention that the reading voltage (0.2 V) is small and is applied only during the reading operation. In addition, the duration of the reading operation is shorter than 1 μ s, which is too short to change the device state at the voltage of 0.2 V. Therefore, the effect of the reading voltage on the retention behaviors can be ignored.

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Fig. 4-24: Retention behaviours of the LRS and HRS at 25°C and 200°C . Notice the LRS decreases abruptly after 30000 s at 200°C .

Figure 4-25 shows the Arrhenius plot of the LRS retention failure time ($t_{\text{LRS-failure}}$).

The Arrhenius behaviour can be expressed as:

$$t_{\text{LRS-failure}} \propto \exp\left(\frac{E_a}{kT}\right) \quad (4.3)$$

where E_a is the activation energy for the LRS failure. The E_a value yielded from the Arrhenius plot is ~ 1.3 eV, which is much larger than the activation energies of the set/reset process occurring during the voltage sweeping. The Arrhenius behaviour of the LRS failure time with the large activation energy suggests that the LRS failure could be due to the dissolution of some CFs caused by the migration of the excess Al atoms at high temperatures without the application of continuous electric fields. It is worth to point out

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that the reset/set process in the voltage sweeping or pulse voltage experiments is caused by an applied electric field while there is no electric field involved during the retention periods. The mechanisms for the CF breaking/reconnection in the reset/set process should be different from that for the LRS failure in the retention experiment because the former is triggered by an electric field but the latter doesn't involve an electric field. This argument is supported by the fact that the activation energies for the former are much lower than that of the latter. On the other hand, as shown in Figure 4-25 the retention time of 30 years can be achieved at 85 °C, which is long enough for a practical non-volatile memory application.

Fig. 4-25: Arrhenius plot of the LRS retention failure time. The activation energy is about 1.3 eV which may relate to Al migration rate.

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Fig. 4-26: *I-V characteristics measured at 25 °C after the LRS failure at 200 °C. From this result, the device still exhibits switching property after baking at 200 °C.*

It is also worth to mention that the LRS failure is permanent if there is no further set operation. However, the device with the LRS failure can be set and reset again, and the situation of the set/reset switching is similar to that before the LRS failure. Figure 4-26 shows the set/reset switching at 25 °C after the LRS failure at 200 °C. The current levels and the set/reset voltages are about the same as before the LRS failure.

4.7 Summary of this chapter

In summary, the Al-rich Al_xO_y layer formed by partially anodizing Al thin film showed unipolar and repeatable switching between the LRS and the HRS with a high resistance

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ratio ($> \sim 10^4$). The switching occurred without the requirement of a forming process, which is attributed to the pre-existing conductive filaments in the Al-rich Al_xO_y layer. The MIM structure consisting of the Al-rich Al_xO_y layer showed good memory characteristics. At low fields, both LRS and HRS showed ohmic conduction. LRS exhibited metallic conductor behavior (i.e., the resistance increased with increasing temperature), which is due to the metallic conduction paths formed by the excess Al in the oxide matrix; however, HRS showed semiconducting behavior (i.e., the resistance decreased with increasing temperature), which is attributed to the hopping of thermally excited electrons from one isolated state to the next. At high fields, the current conduction departed from the ohmic conduction, and the conduction was enhanced at a higher temperature. The current conduction at high fields is explained by the Schottky emission and or the Poole-Frenkel emission. Both the V_{reset} and V_{set} decrease with increasing temperature, showing Arrhenius-like dependence with small activation energies. No large change in the set/reset voltage and the temperature dependence is observed after 10^4 set/reset cycles. The pulse voltage experiment also suggests that the CF breaking / reconnection is easier to occur at a higher temperature. At elevated temperatures, while the HRS exhibits no significant change, the LRS shows a continuous degradation with time and there is an abrupt increase in its resistance. The LRS retention failure time shows Arrhenius dependence with the activation energy of ~ 1.3 eV, which suggests that, the LRS failure could be due to the dissolution of some CFs caused by the migration of the excess Al atoms at high temperatures.

Chapter 5 Electrical properties and memory behavior of AlO_xN_y thin films

5.1 Introduction

Aluminum oxynitride (AlO_xN_y) is a transparent ceramic material with the properties of high strength and hardness. It is frequently used as a protective coating against diffusion and corrosion [166,167], optical coating [168], etc. This material has the possibility of a broad combination of the physical and chemical properties of the oxynitride films with variable concentrations of aluminum, oxygen and nitrogen. The film properties can be tailored between those of pure aluminum oxide (Al_2O_3) and aluminum nitride (AlN), depending on different applications. The synthesis of AlO_xN_y films has been commonly reported using physical vapor deposition, such as ion-beam-assisted evaporation and sputtering method [166,167,169,171]. As shown in some studies [170,173], in the case of the deposition of AlO_xN_y films by sputtering, the oxygen concentration in the films increases with increasing sputtering power. In this work, the radio-frequency (rf) magnetron sputtering technique is utilized to synthesize AlO_xN_y thin films with different sputtering powers at room temperature, in order to fabricate samples with different oxygen concentrations. Although the optical, mechanical and gas barrier properties of AlO_xN_y films have been investigated in some studies [166,167], electrical

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properties of the dielectric film and their dependence on the oxygen concentration have been rarely reported.

In this chapter, the electrical properties of the AlO_xN_y films grown on Si (100) substrates by rf magnetron sputtering have been investigated. The composition of AlO_xN_y films which is varied with different sputtering powers was analyzed by X-ray photoelectron spectroscopy (XPS). To investigate the influence of oxygen content on the electrical properties of the AlO_xN_y films, both metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM) structures devices were fabricated and studied. The resistive switching behaviors and switching mechanisms are discussed in terms of oxygen vacancies inside the AlO_xN_y film. Memory behaviors and performance of both MIS and MIM structures based on AlO_xN_y films are investigated also.

5.2 Sample fabrication and characterization

5.2.1 RF sputtering

The AlO_xN_y dielectric film was grown on p-Si (100) substrates by using rf magnetron sputtering from high-purity aluminum (99.999%) target. During the sputtering, the AlO_xN_y films were deposited by using the different rf powers of 100 W, 150 W and 250 W. As the sputtering power increases, the oxygen concentration inside the film increases correspondingly, which is proved by the XPS results shown in next section. The gas flow rate of $Ar : N_2$ was fixed at 45:15. The oxygen may be from residual oxygen or plasma itself. The substrate temperature during sputtering was maintained at room

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temperature. After the deposition, the top and bottom *Al* electrode pads were deposited by using e-beam evaporation. No thermal annealing process was conducted after the film deposition. Therefore, the dielectric film itself or the interface between the two layers should have a lot of defects.

5.2.2 XPS results

The XPS technique is used to analyze the chemical characteristics of the thin film. From this result, it is shown that the oxygen concentration increases with the sputtering power.

The composition of AlO_xN_y films fabricated with different sputtering powers was analyzed by XPS as shown in Fig. 5-1. It can be concluded from the figure that the AlO_xN_y films are *Al*-rich and have different oxygen concentrations. It is found that the existence of oxygen in the AlO_xN_y thin films is due to the residual oxygen in the chamber with a base pressure of 6×10^{-6} mbar or from the reactive plasma. The characterization results clearly indicate that the oxygen concentration increases with increasing sputtering power, which is consistent with other study [173]. As estimated from the XPS results, the samples fabricated with the rf powers of 100 W, 150 W and 250 W samples have the oxygen concentrations of 11%, 18% and 25%, respectively.

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Fig. 5-1: XPS results of the samples fabricated with various powers: a) 100 W; b) 150 W and c) 250 W which produced the low, medium and high oxygen concentrations in the AlO_xN_y thin films, respectively.

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5.2.3 Device structure

The devices based on MIS and MIM structure are shown in Fig. 5-2. These two device structures are often used in electrical studies, as discussed in Chapter 3 and Chapter 4. It should be noted that the Al -rich AlO_xN_y dielectric thin films in these two structures are identical. The thickness of the films is 15 – 20 nm. Fig. 5-2 (a) is the memory device with the MIS structure which is fabricated on p-type silicon. Fig. 5-2 (b) is the device with the MIM structure in which a 200 nm pure Al thin film deposited on a p-type silicon substrate is used as the bottom electrode. The Al based dielectric film was fabricated by using sputtering method as in section 5.2.1. For both MIS and MIM structures, a 250 nm Al film is deposited by e-beam evaporation to form the top electrodes.

Fig. 5-2: a) MIS and b) MIM structures.

5.3 Electrical properties of the MIS structures based on the AlO_xN_y thin films

5.3.1 Capacitance-voltage (C-V) characteristics

C - V characteristics of the MIS structure based on AlO_xN_y films with different oxygen contents have been measured. The C - V curves of the MIS device show shifts as a result of charge trapping (electron or hole trapping) in the dielectric films caused by the application of a positive or negative voltage (e.g. ± 15 V) for a sufficiently long duration (e.g. 1 s). The mechanisms of charge trapping have been discussed in Chapter 3. The C - V curve shifts to the right- or left-hand side along the voltage axial indicate the electron trapping or hole trapping in the dielectric layer, respectively.

As examples, Fig. 5-3 and Fig. 5-4 show the C - V characteristics of the samples (i.e., Sample 2 and Sample 3) with medium and high oxygen concentrations, respectively. As can be observed from Fig. 5-3(a) and Fig. 5-4(a), after charging at -15 V or 1 s, the C - V curves shifts to the left-hand side, indicating hole trapping in the AlO_xN_y layer. The hole trapping is due to the hole injection from the p-Si substrate under the negative gate bias. On the other hand, as shown in Fig. 5-3(b) and Fig. 5-4(b), the charging at +15 V for 1 s causes a shift to the right-hand side, indicating electron trapping in the AlO_xN_y layer. The electron trapping is due to the electron injection from the p-Si substrate under the positive gate voltage (note that the p-Si surface is now under strong inversion). The C - V shifts actually represent shifts in the flat-band voltage of the MIS structures. This suggests that the MIS structures based on the AlO_xN_y layer can be used in non-volatile memory applications.

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Fig. 5-3: C - V shifts of the sample fabricated with the RF power of 150 W (with a medium oxygen concentration): (a) charging at -15V for 1 s; and (b) charging at + 15V for 1 s.

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Fig. 5-4: C-V shifts of the sample fabricated with the RF power of 250 W (with a high oxygen concentration): (a) charging at -15V for 1 s; and (b) charging at + 15V for 1 s.

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5.3.2 Current-voltage (I - V) characteristics

I - V measurements were conducted for the samples fabricated with the RF powers of 100, 150 and 250 W, which have a low, medium and high oxygen concentration, respectively. Fig. 5-5 shows the I - V characteristic of the sample with low oxygen concentration. As can be seen in the figure, the diode structure exhibited a “rectifying” behavior, namely, the current under the forward bias condition (i.e., the gate voltage was negative) was larger than that under the reverse bias condition (i.e., the gate voltage was positive). This behavior can be explained as follows. Both the electron injection from the Al gate and the hole (the majority carrier in the Si substrate) injection from the p-type Si substrate occurred simultaneously under a negative gate voltage; in contrast, only electron (the minority carrier in the Si substrate) injection from the Si substrate occurred under a positive gate voltage. A very stable current conduction in the MIS structure was observed, as shown in Fig. 5-5.

Being similar to the sample with low oxygen concentration, the samples with medium or high oxygen concentration exhibit the “rectifying” behavior also, as shown in Figs. 5-6 and 5-7. However, as can be observed from the two figures, in contrast to the sample with low oxygen concentration, the two samples with medium or high oxygen concentration exhibit instability in the I - V measurements. In other words, conduction switching (or resistance switching) occurred in the two samples during the I - V measurement. Such conductive switching could be explained as the carrier trapping and de-trapping occurred between mobile charge ions (O^-) and trap centers. These trap centers may form the conductive paths which will enhance the conductivity a lot. If the

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trap centers are charged, the conductive path will be broken which will make the conductivity decreased. However, such process is random and unpredictable.

Fig. 5-5: *I-V characteristic of the sample with low oxygen concentration.*

Fig. 5-6: *I-V characteristic of the sample with medium oxygen concentration.*

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Fig. 5-7: I - V characteristic of the sample with high oxygen concentration.

5.4 Resistive switching in the MIM structures based on the AlO_xN_y thin films

5.4.1 Resistive switching behaviors

5.4.1.1 The sample with low oxygen concentration

The I - V measurement result of the sample with low oxygen concentration is shown in Fig. 5-8. In this measurement, the biasing voltage step is 0.001 V and the compliance current is set to 0.1 A. As shown in the figure, after the first I - V measurement (which can be seen as a forming process), the current is quite high even at the beginning of the

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biasing and I - V curve shows perfect linear relationship between I and V which behave like a resistor with a resistance of around 4.5 ohm. It could be concluded that the conductive filaments have been connected through this dielectric film due to pre-exist excess Al .

Fig. 5-8: I - V measurement of the low oxygen concentration sample based on MIM structure. The linearity of the I - V curve indicates that the current follows ohmic conduction with a resistance of 4.5 ohm.

The inset of Fig. 5-11 is the model of conductive filament with resistance of 4.5 ohm which has been formed to connect the top and bottom electrodes during the first I - V measurement. The conductive filament is formed by the high concentration of excess aluminum in the AlO_xN_y film. In this situation, the conductive filament behaves like a perfect resistor connecting the top and bottom electrodes, and it is hardly to be broken by current or voltage biasing.

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5.4.1.2 The sample with medium oxygen concentration

As mentioned before, the medium oxygen concentration sample shows a resistive switching after the forming process. During the forming process as shown in Fig. 5-12, more oxygen vacancies or defects are induced into the dielectric thin film and the device will switch from the insulating state to a conductive state. The forming process could be carried out by voltage biasing (force- V -measure- I) or current biasing (force- I -measure- V) as shown in Fig. 5-9.

Fig. 5-9: Forming process for the sample with medium oxygen concentration by the I - V biasing or the V - I biasing (the inset of the figure).

In order to avoid hard breakdown in the dielectric layer, the compliance current is set to 0.1 μ A for voltage biasing and 1 μ A for current biasing. During the forming process, there was a sharp increase in current for the voltage biasing measurements or an

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obvious switch back for the current biasing measurements. From both of the I - V and V - I biasing measurements, the forming voltage for the sample with medium oxygen concentration is around 7 V.

Fig. 5-10: Switching during repeated I - V measurements: (a) force voltage and measure current, and (b) force current and measure voltage.

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After the forming process, the device should maintain at LRS and will be switched back to HRS if the biasing voltage exceeds a critical value, as shown in Fig. 5-10 (a). The critical voltage is the so-called reset voltage.

Such reset process is caused by breaking of conductive filament. After the reset process, the device should be at HRS and could be switched back to LRS by set process as shown in the Fig. 5-10 (b), which is executed by the V - I biasing. From Fig. 5-10 (b), it is obvious that the measured voltage will switch back to a low level if the forced current exceeds a certain value. This switch back voltage is so-called set voltage. Both of the set and reset processes are reversible. In conclusion, the sample with medium oxygen concentration exhibits unipolar resistive switching after a forming process.

5.4.1.3 The sample with high oxygen concentration

Fig. 5-11: Forming process for the sample with high oxygen concentration executed by I - V biasing. The forming process can also be conducted by V - I biasing as shown in the inset of the figure.

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Fig. 5-12: a) Switching from LRS to HRS (i.e., the reset process) by I-V biasing and b) switching from HRS to LRS (i.e., the set process) by V-I biasing.

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The I - V measurements of resistive switching of the sample with high oxygen concentration are shown in Fig. 5-12. After the forming process, the device is maintained at LRS. The device can be switched back to HRS by the I - V biasing, as shown in Fig. 5-12 (a), and then the device can also be switched from HRS back to LRS by V - I biasing, as shown in Fig. 5-12 (b).

5.4.2 On/off currents at LRS and HRS and set/reset voltages

The on/off current and set/reset voltage distributions of the samples with medium and high oxygen concentrations are investigated in this section. It is found that the switching characteristics are affected by the oxygen concentration.

Fig. 5-13 shows the statistical distributions of the on/off currents for the samples with medium and high oxygen concentrations. The results were obtained from the measurements at room temperature on 15 devices. It can be observed from Fig. 5-13 (a) that the on current of the LRS of the sample with high oxygen concentration is lower than that of the sample with medium oxygen concentration. The corresponding resistances of the formed CFs in the samples with high and medium oxygen concentrations are 16 ohm and 11 ohm samples, respectively. After the CFs are broken, the sample with high oxygen concentration still shows lower conductance than the sample with medium oxygen concentration, as demonstrated by the off currents of the HRS shown in Fig. 5-13 (b). Therefore, it can be concluded that a thinner CF is formed in the sample with high oxygen concentration samples.

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Fig. 5-13: Statistical distributions of the on-state current a) and off-state current b).

As shown in Fig. 5-14, the above results should have a connection with oxygen concentration. It is reasonable to suppose that the high oxygen concentration dielectric film should have high concentration of oxygen ions (O^-) but low concentration of oxygen

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vacancies (V_o^+). In other words, the sample with medium oxygen concentration should have a lower O^- concentration but higher V_o^+ concentration as compared to the sample with high oxygen concentration. The oxygen vacancies can form a conductive filament. A higher concentration of oxygen vacancies can form a wider CF with low resistance. This assumption is consistent with the results in Fig. 5-13. It is thus concluded that the oxygen concentration should have effect on the LRS and HRS conductivity.

Fig. 5-14: (a) Diagram of CFs formed in the samples with medium and (b) high oxygen concentration.

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Fig. 5-15: Statistical distributions of the reset voltage a) and set voltage b).

Fig. 5-15 shows the statistical distributions of the reset and set voltages. As can be observed in Fig. 5-15 (a), the sample with medium oxygen concentration has higher reset voltage than the sample with high oxygen concentration, i.e. the sample with medium oxygen concentration has the reset voltage in the range of 0.37 – 0.81 V while the sample with high oxygen concentration has the reset voltage in the range of 0.25 – 0.7 V. In other

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words, the conductive filament of the sample with medium oxygen concentration needs more energy to be broken as compared with the sample with high oxygen concentration as the CF in the sample with medium oxygen concentration is wider. On the other hand, as shown in Fig. 5-15 (b), the sample with high oxygen concentration has higher set voltage (in the range of 1.4 to 5.0 V) than the sample with medium oxygen concentration which has the set voltage in the range of 1.1 to 2.6 V. It means that the sample with high oxygen concentration needs more energy to form the conductive filaments than the sample with medium oxygen concentration. This is because the V_o^+ concentration in the sample with high oxygen concentration is lower.

5.4.3 Retention of LRS and HRS

As mentioned before, the resistive switching memory device can be switched between HRS and LRS with a current ratio large enough to distinguish the two memory states. For a potential application in NVM, the MIM structure based memory device should guarantee to retain the same state (HRS or LRS) for at least 10 years without power applied. The two samples that have medium and high oxygen concentrations discussed above are found to have good retention performance as shown in Fig. 5-16.

In Fig. 5-16, LRS is the on-state which corresponds to high current conduction (10^{-2} A) and HRS is the off-state which corresponds to low current conduction ($10^{-8} \sim 10^{-9}$ A). The current ratio of the two is over six orders, which is large enough to distinguish the on-off states. No significant degradations was observed in the retention measurement in the measurement time limit of 50000 s. The reading voltage was kept at 0.15 V which

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should be small enough to avoid reset process occurring. It can be concluded from the retention study that the AlO_xN_y based ReRAM device should have a good retention capability.

Fig. 5-16: Retention experiment with the reading voltage of 0.15 V.

5.4.4 Resistive switching mechanism

As oxygen vacancies widely exist in metal oxides, the oxygen vacancy model could be one of the important understandings to the origin of the resistance switching phenomena [174-177]. In the reset process, oxygen ions can move to the oxygen vacancy sites, making the filament broken. This process is mainly related to oxygen ion movement. In the set process, the electrical field can cause oxygen ions to be removed from their original lattice, leading to the oxygen vacancy-related filament formation.

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Therefore, the creation of oxygen vacancies and the movement of the oxygen ions to the oxygen vacancy sites could play a dominant role in the set and reset processes, respectively, as shown in Fig. 5-17.

Fig. 5-17: Reset and set processes involved with oxygen ions.

Here, the Vo^+ forms the conductive paths, and oxidation of Al makes the CFs broken. By using this model, the oxygen concentration effect on switching behavior could be explained as following. As we mentioned before, the sample with high oxygen concentration should have high concentrations of oxygen ions (O^-) and low concentration of oxygen vacancy concentrations. Comparing with the sample with high oxygen concentration, the sample with medium oxygen concentration should have lower O^- concentration and higher vacancy concentration. If the O^- concentration is higher, the reset process should be easier to occur, which explains why the sample with high oxygen concentration has lower reset voltage than the sample with medium oxygen concentration

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(see Fig 5-15 (a)). However in the set process, the switching is mainly determined by the accumulation of vacancies. In this situation, the sample with higher vacancy concentration should have a smaller set voltage, which is confirmed by the experiment shown Fig 5-15 (b).

5.5 Summary of this chapter

In this chapter, the current conduction and resistive switching properties of the MIS and MIM structures based on AlO_xN_y have been studied. For the sample with low (11%) oxygen concentration, there is no conduction switching or resistive switching observed in both MIS and MIM structures. However for the samples with medium (18%) and high (25%) oxygen concentrations, conduction/resistance switching is observed. It could be concluded that the oxygen in the AlO_xN_y layer plays an important role in the current conduction and resistance switching in the AlO_xN_y layer.

Chapter 6: Summary and Recommendations

6.1 Summary

Modern electronic applications aggressively demand the down scaling of nonvolatile memory devices in pursuit the advantages of larger capacity, smaller device area, lower power consumption and higher operating speed. However, the limited potential in continuous scaling of the conventional memory structure based on a floating-gate urges the search for new dielectric materials. In addition, the constantly growing demand of compact systems capable of performing new and increased numbers of operations brings on the development of CMOS-compatible memory devices to fulfill the integration of electronic circuits.

Nc-Al embedded in Al_2O_3 and AlO_xN_y have been proved as a promising candidate for the next-generation non-volatile memory devices. In this thesis, the syntheses of Al-rich Al_2O_3 and AlO_xN_y have been successfully demonstrated using the sputtering and anodization techniques which are fully compatible with modern CMOS technology. The electrical properties and memory applications of the Al-rich Al_2O_3 and AlO_xN_y thin films have been investigated in details. The results presented in this thesis have enhanced our understanding of the properties of Al-rich Al_2O_3 and AlO_xN_y thin films which open up new possibilities to fabricate next-generation non-volatile memory devices. This section summarizes the overall work presented in this thesis. A summary of two type memory device is shown in table 6-1.

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	Memory characteristic with MIS structure	Memory characteristic with MIM structure
Al-rich Al_2O_3 based memory	Charging effect; No conduction switching	Resistive switching
Al-rich AlO_xN_y based memory	Charging effect; Conduction switching	Resistive switching observed when oxygen concentration is high enough

Table 6-1: Summary of Al-rich Al_2O_3 and AlO_xN_y based memory devices.

6.1.1 Current transport and modulation behaviors of Metal-Insulator-Semiconductor (MIS) structure device

The current transport and modulation behaviors of Al-rich Al_2O_3 thin films based MIS devices have been investigated in this thesis. Two different methods were used to fabricate dielectric thin films including sputtering and anodization. The structural properties of the samples have been characterized. By introducing metal nanoclusters / nanoparticles into the dielectric matrix, the conductivity of the thin film can be greatly enhanced. Meanwhile, the presence of metal phases makes it possible to alter the current conduction by charging and discharging as a result of the application of voltage pulses. The characteristics of the gate current at various temperatures have been investigated and the different transport mechanisms dominating in the different oxide field regions have been also identified. The current transport behavior has been explained with appropriate

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models which can be modulated due to the charging and discharging in the nc-*Al* induced by the electrical field. It has been found that the current transport is dependent on the polarity of applied voltages and also the measurement temperatures.

6.1.2 Charge trapping behavior and memory applications of MIS structure devices

The charge trapping and charge retention behaviors of the *Al*-rich Al_2O_3 dielectric thin films have been investigated. The dependence of charge trapping and charge retention on the polarity and magnitude of the charging voltage has been studied. For a positive charging voltage, only electron trapping occurred and the trapped electrons showed stable retention property. However for a negative charging voltage, both the hole trapping and electron trapping occurred simultaneously and the hole trapping was dominant due to the relatively easier loss of the trapped electrons, the net charge trapping in the nc-*Al* exhibited a continuous shift towards a more negative value with charging time. Based on this theory, a two-terminal charging-controlled resistive memory based on *Al* / *Al*-rich Al_2O_3 / *p*-*Si* MIS diode structures has been demonstrated. The resistance of the *Al*-rich Al_2O_3 layer can be controlled by the charge trapping, i.e., the quantity of the trapped charges in the dielectric film determines the resistance. By optimizing the composition of the *Al*-rich Al_2O_3 through thermal annealing, a long retention of 10^5 s in the MIS devices has been achieved with a memory window greater than 2.5 decades, which could be a potential candidate for memory applications.

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6.1.3 Current transport and modulation behaviors of Metal-Insulator-Metal (MIM) structure device

The current conduction of resistance switching at both LRS and HRS are investigated which are quite useful for further understanding the switching mechanisms. At low field, both conduction of LRS and HRS follow ohmic conduction. For LRS, the metallic conductive filament will form, connecting top and bottom electrode, and the device behaves like a resistor. The conduction in the HRS exhibits two distinct regimes: ohmic conduction at low fields with a semiconductor behavior; and a non-ohmic conduction at high fields. The ohmic conduction of HRS at low fields is attributed to the electron hopping between the states in the oxide with the activation energy of ~ 0.23 eV. It is shown that the conduction of HRS at high fields is due to the field-enhanced thermal excitation of the electrons trapped in the states of the metallic Al nano-phase into the conduction band of the Al oxide or the electron emission from the potential well of the metallic Al nano-phase to the conduction band.

6.1.4 Oxygen concentration effect on the electrical properties of the MIS and MIM memory structures

The electrical property of AlO_xN_y thin film based MIS and MIM memory devices with different oxygen concentrations have been investigated in detail. With increasing oxygen concentration, the ion movement inside dielectric thin film is much more complicated than intrinsic materials and some interesting phenomenon appeared. For example, the repeatable conduction switching was observed in I - V measurement for MIS structured memory devices based on medium (18%) and high (35%) oxygen

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concentrations AlO_xN_y thin films. However, for MIM structured devices, the samples with low oxygen concentrations (16%) will behave like a resistor. The resistance switching can only be observed in samples with medium (18%) and high (35%) oxygen concentrations AlO_xN_y thin films.

6.2 Recommendations

The work presented in this thesis has enriched the understanding on the electrical properties of the metal-dielectric nanocomposite thin films including *Al*-rich Al_2O_3 and AlO_xN_y . These nanocomposite materials have good potentials in next-generation CMOS-compatible nonvolatile memory device applications. However, some future work can benefit the realization of these applications in real life.

6.2.1 Synthesis of nc-*Al* embedded in AlO_xN_y with controllable oxygen concentration by using gas-timing techniques

In some reported studies, the oxygen concentration in rf sputtering is controlled by the partial pressure of oxygen gases with fixed sputtering power. By introducing the different quantities of O_2 gas which could be controlled by the timing techniques (e.g., introducing O_2 gas with period of 1 s, 5 s and 10 s) the oxygen concentration in the deposited film can be controlled.

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6.2.2 Further study on charging effect and conduction switching mechanisms based on MIS memory structures

In chapter 3, charging effect on the current conduction of the devices based on *Al*-rich Al_2O_3 thin films has been demonstrated by examining the charging voltages. The charging mechanisms can be identified in future, regarding the energy level of the charge trapping and the trapping locations of the charges (i.e., inside the metal nanoparticles or in the interface region between metal nanoparticles and dielectric matrix or in other defects in the dielectric matrix). The influence of the charge trapping with different trapping quantities and trapping energy levels on the current conduction needs to be studied in more detail as well.

6.2.3 Further study on the resistive switching mechanisms based on the MIM memory structures

The proposed resistive switching mechanisms can be classified into two models: the filament model and the interface model. The results of this thesis shows the representative achievements supporting the filament model, where the switching is believed to be due to the formation and rupture of a metallic filament in the metal oxide thin film sandwiched between two electrodes. However, a systematic study on the switching behaviors of MIM structures with different electrode materials should be conducted in order to examine the effects of the electrodes and the interfaces between the electrodes and the oxide layers.

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6.2.4 Further study on the oxygen concentration effect on electrical properties

The properties of oxide material, such as the resistivity are drastically changed by the oxygen concentration. This is an advantage of oxide materials. It is crucial to control the partial oxygen pressure in their deposition process. According to studies in chapter 5, the oxygen concentration plays an important role in the electrical properties of the AlO_xN_y thin films. It would be useful to investigate the influence of the oxygen concentration on the current transport and resistive switching in the AlO_xN_y films.

6.2.5 Improvement of the device performance

Methods to improve the performance of non-volatile memory devices and resistive switching memory devices based on Al -rich Al_2O_3 and AlO_xN_y should be systematically investigated in the future work. For practical non-volatile memory device, a low operating voltage and a large memory window are desired. However for the present device structure, the charging voltage is larger than 15 V for a significant flatband voltage shift (ΔV_{FB}). One way to achieve a lower charging voltage and a wider memory window is to reduce the total oxide thickness. In this way, the electric field across the oxide is sufficiently high at low operating voltages. However, the charge retention time could be sacrificed due to the easier charge leakage to the Si substrate. For the ReRAM device based on Al -rich Al_2O_3 and AlO_xN_y thin films, the endurance characteristic obviously has to be improved to meet the industrial standard of 10^6 cycles. For the WORM memory devices, the device miniaturization (e.g., reducing the dielectric layer

Chapter 6: Summary and recommendations

thickness and shortening the inter-electrode distance) is needed to satisfy low-power and high-density requirements.

List of Publications

LIST OF PUBLICATIONS

- [1] **W. Zhu**, T.P. Chen, Y. Liu, M. Yang , S. Zhang, W.L. Zhang and S. Fung, "Charging-Induced Changes in Reverse Current-Voltage Characteristics of Al/Al-Rich Al₂O₃/p-Si Diodes," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, September 2009.
- [2] **W. Zhu**, T. P. Chen, Z. Liu, M. Yang, Y. Liu, and S. Fung, "Resistive switching in aluminum/anodized aluminum film structure without forming process," *J. Appl. Phys.*, vol. 106, no. 9, p. 093706, Nov. 10, 2009.
- [3] **W. Zhu**, T. P. Chen, M. Yang, Y. Liu, and S. Fung, "Two-terminal write-once-read-many-times memory device based on charging-controlled current modulation in Al/Al-rich Al₂O₃/p-Si diode," *IEEE Transactions on Electron Devices*. vol. 58, no. 4, p. 960, Apr. 2011.
- [4] **W. Zhu**, T. P. Chen, M. Yang, Y. Liu, and S. Fung, "Temperature dependence of resistive switching in aluminum/anodized aluminum film structure", *Nanoscience and Nanotechnology Letters*, vol. 3, no. 2, p.222, Apr. 2011.
- [5] **W. Zhu**, T. P. Chen, M. Yang, Y. Liu, and S. Fung, "Resistive Switching Behaviour of Partially Anodized Aluminum Thin Film at Elevated Temperatures", *IEEE Transactions on Electron Devices*, vol. 59, no. 9, p. 2363-2367, Sep. 2012.
- [6] **W. Zhu**, T. P. Chen, Y. Liu, and S. Fung, "Conduction mechanisms at low- and high-resistance states in aluminum/partially anodized aluminum oxide/aluminum thin film structure", *journal of applied physics*, vol. 112, p. 063706-5, Sep. 2012.

US Patent Applications

US Patent Applications

1. T. P. Chen, and **W. Zhu**, “A Charging-controlled memristor-like memory structure”, US patent application no. 61/472,846 (Filing date: 7 April 2011)
2. S. S. Tan, **W. Zhu** and T. P. Chen, “RRAM device with free-forming conductive filament(s), and methods of making same”, US patent application (being filed by Commissioner for Patents, Attorney Docket: 2262.001100/CSG039, Jan. 2012)

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