Transition metal oxide based resistive RAM for high density non-volatile memory

Tran, Xuan Anh

2013

Tran, X. A. (2013). Transition metal oxide based resistive RAM for high density non-volatile memory. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/54826>

<https://doi.org/10.32657/10356/54826>

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**TRANSITION METAL OXIDE BASED RESISTIVE RAM
FOR HIGH DENSITY NON-VOLATILE MEMORY**

**TRAN XUAN ANH
SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
2013**

TRANSITION METAL OXIDE BASED RESISTIVE RAM FOR HIGH DENSITY NON-VOLATILE MEMORY

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2013

Acknowledgements

First and foremost, I would like to express my deepest gratitude to my research advisors, Prof. Yu Hong-Yu and Prof. Zhu Weiguang, for their supervision, advice, and guidance from the very early stage of this research and encouraging me, not only in terms of technical knowledge, but also personally, during my graduate study at NTU. Especially I am extremely grateful to Prof. Yu's help, who offers me a chance to join his group in first place. Without the unflinching encouragement and support in various ways from both Prof. Yu and Prof. Zhu, this thesis would not have been completed or written. I consider myself privileged to work with such outstanding and highly motivated professors.

I would also like to extend my sincere appreciation to Prof. Pey Kin-Leong from STUD, Prof. Yeo Yee-Chia from NUS, Prof. Kang Jin-Feng and Mr. Gao-Bin from Peking University, Beijing, Dr. Wang Xinpeng from IME, Ms. Bich-Yen from Soitec, USA and Prof. Li Ming-Fu from Fudan University, China for their intellectual support and many useful technical discussion.

I greatly acknowledge numerous exceptionally talented graduate students and colleagues in Prof. Yu and Prof. Zhu's group, including Dr. Chen Xiaofeng, Dr. Liu Wenjun, Mr. Fang Zheng, Mr. Wang Zhongrui, Mr. Wu Ling, Mr. Chen Weigang and Mr. Lin Zhipeng. I would also like to express my appreciation to all other NOVITAS teaching staffs, fellow graduated students, and technical staffs.

Special thanks to my wife, Ms. Hien-Dzung, and my daughter, Thao-Linh, for their love, consistent support, wonderful experiences and happiness. I would like to thank my parents and parents-in-law for having been my advisers and supporters ever.

Table of Contents

Acknowledgements	i
Table of Contents	ii
SUMMARY	viii
List of Tables.. ..	x
List of Figures	xi
 Chapter 1 Introduction	 1
1.1. Background.....	1
1.2. Motivation	3
1.3. Objectives	4
1.4. Organization of Thesis	5
1.5. Contributions	6
 Chapter 2 Literature Review	 10
2.1. FLASH Memory Overview	10
2.2. Emerging Non-volatile Memory Overview	12
2.2.1. Magneto-resistive Random Access Memory (MRAM).....	12
2.2.2. Ferroelectric Random Access Memory (FeRAM)	14
2.2.3. Phase-change Random Access Memory (PCRAM)	16
2.2.4. Resistive-switching Random Access Memory (RRAM)	18
2.3. General Introduction of RRAM.....	19

2.4.	Basic Operational Switching of RRAM.....	20
2.5.	Resistive Switching Mechanism.....	24
2.5.1.	Classifications of Resistive Switching Mechanism	24
2.5.2.	Thermo-chemical Mechanism (TCM)	25
2.5.3.	Electrochemical Metallization Mechanism (ECM)	30
2.5.4.	Valence Change Mechanism (VCM).....	32
2.6.	Switching Materials and Transition Metal Oxides (TMOs).....	36
2.7.	RRAM Integration	38
2.7.1.	Introduction of RRAM Integration	38
2.7.2.	Active CMOS Array	39
2.7.3.	Passive Array.....	42
2.7.4.	Cross-talk Interference	47
2.7.5.	Selection Devices.....	48
2.7.5.1.	Diode-Type Selection Device.....	48
2.7.5.2.	Resistive-Switch-Type Selection Device	49
2.7.5.3.	Metal-Insulator transition (MIT) Switch.....	49
2.7.5.4.	Threshold Switch	50
2.7.5.5.	Mixed-ionic-electronic-conduction (MIEC) Switch.....	50
2.7.6.	Self-rectifying RRAM Device.....	51

Chapter 3	High Yield HfO_x-Based Unipolar Resistive RAM Employing Ni Electrode Compatible with Si-Diode Selector for Cross-Bar Integration.....	54
3.1.	Introduction	54
3.2.	Experimental Details	55
3.3.	Results and Discussion.....	56
3.3.1.	Physical Analysis of RRAM Cell	56
3.3.2.	Electrical Characterization of RRAM Cell	58
3.3.2.1.	DC Resistive Switching Characterization of RRAM Cell	58
3.3.2.2.	Current Conduction Mechanism of RRAM Cell in <i>LRS</i> and <i>HRS</i>	60
3.3.2.3.	Resistive Switching Performance of RRAM Cell	63
3.3.2.4.	Resistive Switching Mechanism of RRAM cell.....	66
3.4.	Conclusion.....	68
Chapter 4	Performance Enhancement for Ni Electrode Unipolar Resistive RAM with AlO_y Incorporation into HfO_x Switching Dielectrics	69
4.1.	Introduction	69
4.2.	Performance Enhancement of Resistive Switching Characteristic with Bi-layer and Doping Technology.....	69
4.3.	Experimental Details	71
4.4.	Results and Discussion.....	72
4.4.1.	Physical Analysis of RRAM Cell	72

4.4.2.	Electrical Characterization of RRAM Cell	74
1.1.1.1.	DC Resistive Switching Characteristic of RRAM Cell	74
4.4.2.1.	AC Conductance Measurement of RRAM Cell in <i>LRS</i> and <i>HRS</i>	75
4.4.2.2.	Temperature Dependence of <i>HRS</i>	76
4.4.2.3.	Cycle-to-Cycle and Device-to-Device Resistive Switching Performance	78
4.5.	Switching Mechanism of RRAM Cell	83
4.6.	Conclusion	84
Chapter 5 Self-Rectifying Unipolar HfO_x Based RRAM Built by Fab-Available Materials		86
5.1.	Introduction	86
5.2.	Experimental Details	86
5.3.	Results and Discussion	88
5.3.1.	DC Resistive Switching Characteristics of Ni/HfO _x /n ⁺ -Si RRAM Cell	88
5.3.2.	Temperature Dependence of Reverse Current of RRAM Cell in <i>LRS</i>	91
5.3.3.	NxN Cross-bar Array Based Ni/HfO _x /n ⁺ -Si RRAM Cell.	93
5.3.4.	DC Resistive Switching Characteristics of Ni/HfO _x /p ⁺ -Si RRAM Cell	96
5.3.5.	Schottky Barrier Model of Self-rectifying Effect in Ni/HfO _x /n ⁺ -Si RRAM Cell .	100
5.4.	Conclusion	101
Chapter 6 A Self-Rectifying HfO_x-Based Unipolar RRAM with NiSi Electrode		103
6.1.	Introduction	103

6.2.	Experiment Details.....	103
6.3.	Results and Discussion.....	104
6.3.1.	Physical Analysis of RRAM Cells.....	105
6.3.2.	Electrical Characterization of RRAM Cell	105
6.3.3.	Resistive Switching Performance of RRAM Cell	107
6.3.4.	NxN Cross-bar Array based Fabricated RRAM Cell	109
6.3.5.	Switching Mechanism of TiN/HfO _x /NiSi RRAM Cell.....	110
6.4.	Conclusion.....	112
Chapter 7 A Self-rectifying AlO_y Based Bipolar RRAM with Sub-50μA <i>SET/RESET</i>		
Current for Cross-bar Array Architecture.....		113
7.1.	Introduction	113
7.2.	Experiment Details.....	114
7.3.	Results and Discussion.....	115
7.3.1.	Physical Analysis of RRAM Cell.....	115
7.3.2.	Electrical Characteristics of RRAM Cell.....	116
7.3.2.1.	DC Resistive Switching Behavior of RRAM cell	116
7.3.2.2.	Temperature Dependence of RRAM Cell in LRS.....	119
7.3.3.	<i>RESET</i> Current Characteristic of RRAM Cell	121
7.3.4.	Resistive Switching Performance of RRAM Cell	123
7.3.5.	NxN Cross-bar Array based Fabricated RRAM Cell	124

7.4. Conclusion.....	126
Chapter 8 Conclusion and Recommendations	127
8.1. Conclusion Remarks	127
8.2. Recommend for future works	127
Publications.....	132
References.....	135

SUMMARY

Nonvolatile memory technology (NVM) is one of the key driving factors for information storage development. With memory technology aggressively migrating into the sub-10 nm nano-scale regime, the traditional nonvolatile FLASH memory is facing challenging issues such as lithography, coupling ratio, cross-talk between cells and short channel effect. It is essential to identify replacement emerging memory devices as potential alternatives for next generation of memory technology. Recently, Resistive Random Access Memory (RRAM) has emerged as one of promising candidates succeeding the conventional FLASH memory due to its low cost, simple structure, low power dissipation, high endurance and compatibility with CMOS technology.

Recently, transition metal oxide (TMO) materials have attracted great attention as switching materials largely because of their simple composition and outstanding performance. A unique high performance unipolar RRAM based on HfO_x and AlO_y dielectrics and Ni electrode is investigated in this work. By using highly doped Si as bottom electrode, the memory cell makes it feasible to exploit a vertical Si-diode as a selector for RRAM crossbar architecture, highly suitable for low-cost three-dimensional (3D) integration. To improve the performance of RRAM devices, bi-layer $\text{HfO}_x/\text{AlO}_y$ dielectric structures are studied. With bi-layer structures and the doping effect, the tight distribution of switching parameters could be greatly enhanced.

Self-rectifying voltage-current ($I - V$) characteristics of RRAM devices are encouraging to increase the array size without integrating selector (*e.g.* diode, transistor, *etc.*), so that higher integration density could be achieved for the cross-bar architecture. RRAM device with forming-free, unipolar switching, and self-selection for cross-point architecture is demonstrated successfully. With self-rectifying characteristic and high forward current density, the sneak

current path in the conventional cross-bar architecture is effectively eliminated. The fabricated devices show great potential application for nano-scaled memory technology. Being possible in cross-bar architecture, the memory cell can be scaled to $4F^2$ dimensions, the best possible scaling so far in memory.

Owning to superior bipolar resistive switching characteristic, the bipolar RRAM with cross-bar architecture has received widespread attentions. A CMOS friendly and low fabrication cost RRAM device with bipolar switching characteristic, ultra-low current, and self-selection is exploited for RRAM cross-point array application in this work. Vertical RRAM (VRRAM) cross-point structure with vertical Si-nanowire MOSFET is proposed to achieve ultra-high density integration and low fabrication cost. VRRAM cross-point structure could be fabricated and operated correctly based on the fabricated device. By stacking the cross-point arrays in n layers, an effective cell size of $4F^2/n$ could be achieved.

List of Tables

Table 2.1 Summary of resistances witching materials for RRAM device [5].....	36
Table 2.2 A representative list of transition metal-oxide RRAM device characteristics [9].	37
Table 2.3 Solutions and selector's drawbacks for both RRAM types for cross-bar array.	52
Table 4.1 Comparison of device performance for various unipolar RRAM devices.	85

List of Figures

Figure 2.1 (a) Schematic of a typical FLASH memory cell, (b) Drain-Source (D-S) current versus Gate voltage bias, threshold voltage (V_T) shift caused by change in electronic charge on storage element [4].	10
Figure 2.2 Illustration of a field-switched MRAM cell undergoing read and write operations [16].	14
Figure 2.3 (a) Schematic diagram of PZT crystal structure, and (b) hysteresis loop characteristic of a ferroelectric capacitor [21].	15
Figure 2.4 Illustration of operation of a typical PCRAM device.	17
Figure 2.5 (a) Schematic diagram of a typical RRAM cell, and (b) Typical resistive switching behavior of RRAM cell [9].	19
Figure 2.6 Two types of resistance switching behavior : (a) unipolar RS and (b) bipolar RS [33].	21
Figure 2.7 Classification of the resistive switching effects are considered for nonvolatile memory applications [39]. Phase change mechanism is mainly found in chalcogenides like GeSbTe or AgInSbTe [40].	24
Figure 2.8 Unipolar $I-V$ characteristic of a Pt/NiO/Pt stack with a NiO film thickness of 50nm [39].	26
Figure 2.9 Schematics of (a) the initial state as well as (b) forming, <i>SET</i> , and (c) <i>RESET</i> process [42].	27
Figure 2.10 Infrared thermal micrograph of a planar Cr-doped SrTiO ₃ single-crystal cell. The cell has a current of 5mA at an applied voltage of 30V [32].	28
Figure 2.11 Calculated temperature map for applied voltages of (a) 0.53, (b) 0.78, (c) 0.85, and (d) 0.87V across a conductive filament (CF) with length $t_{NiO} = 160$ nm and an initial diameter of 100 nm. The CF edge is also shown, indicating the thermally activated shrinking effect.(e) Measured and calculated $I-V$ and $R-V$ characteristics [43].	29
Figure 2.12 Typical $I-V$ characteristic of Ag/Ag-Ge-Se/Pt electrochemical metallization cell. The insets A to E show the different stages of the switching procedure [45].	31

Figure 2.13 Observation of conducting filament dynamics in SiO ₂ -based resistive memories, (a) TEM image of an as-fabricated SiO ₂ -based RRAM device (<i>Inset</i> : schematic of the device), (b) TEM image of the same device after the forming process. The arrows highlight several representative filaments.(c) TEM image of the same device after erasing [44].	31
Figure 2.14 Schematic of two types of VCM based on geometrical localization : (a) conductive filamentary type, and (b) homogenous interface-type [33].	32
Figure 2.15 (a) Schematic diagram of oxygen vacancy migration and the growth of a CF from the cathode in TiO ₂ . Electroforming-induced morphological change occurring in Pt/TiO ₂ /Pt cells under (b) a positive and (c) a negative voltage applied to the top electrode of a switching cell [47].	34
Figure 2.16 Barrier modulations by oxygen accumulation along the interface between (a) <i>HRS</i> corresponding to a wide barrier, and (b) <i>LRS</i> corresponding to a narrow barrier [50].	35
Figure 2.17 Schematic diagram of RRAM active array (a) 1MOSFET-1RRAM, and (b) 1BJT-1RRAM [53].	40
Figure 2.18 Circuit diagram for an active RRAM in (a) NOR array, (b) NAND array, and (c) AND array with resistive switching MIM structures for memory application [54].	41
Figure 2.19 (a) Schematic of 3D X- point array architecture based RRAM device. A selector is connected in series with RRAM cell to eliminate cross-talk interference. (b) Schematic of 3-D Vertical-RRAM (VRAM) array architecture. RRAM cells share same vertical electrode in this design.	43
Figure 2.20 Schematic diagram of two schemes to program data into the memory cells (a) $V_{dd}/2$ and (b) $V_{dd}/3$ schemes [57].	44
Figure 2.21 Optimal CMOS setup of reading operation for RRAM based crossbar architecture [58].	46
Figure 2.22 Schematic of crosstalk phenomenon in 2x2 cross-bar architecture.	47
Figure 3.1 (a) Schematic of fabricated Ni/HfO _x /p ⁺ -Si RRAM cell. (b) Brief fabrication process flow of RRAM cell.	56
Figure 3.2 (a) Cross-sectional HTEM image of the Ni/HfO _x /p ⁺ -Si memory cell. (b) Elemental analysis of EELS with direction from Si bottom electrode to Ni top electrode.	57
Figure 3.3 Ni _{2p} XPS scan of 5nm Ni film on the 3nm HfO _x layer. (The signal is calibrated with C _{1s} .)	58

Figure 3.4 Typical $I - V$ curve of positive DC sweep. The compliance current (I_{comp}) is set at 10^{-4} A.	60
Figure 3.5 Temperature dependence of the current for (a) LRS and (b) HRS of Ni/HfO _x /p ⁺ -Si device. The applied voltage is 0.2 V.	61
Figure 3.6 Frequency dependence of AC conductance on fresh state and HRS at 25°C.	62
Figure 3.7 Retention behavior of RRAM device measured at 150°C.	64
Figure 3.8 (a) Resistance distribution for 100 DC sweep cycles. (b) SET and $RESET$ voltage distribution for 100 DC sweep cycles.	65
Figure 3.9 Endurance characteristic of RRAM device under pulse switching. The 50 ns pulse is set by equipment and stable switching more than 10^5 cycles is obtained.	66
Figure 3.10 Schematic diagrams illustrating the possible formation or rupture of filament under SET and $RESET$ process for a Ni/HfO _x /p ⁺ -Si RRAM device.	68
Figure 4.1 (a) Schematic diagram and (b) Brief fabrication process flow of Ni/HfO _x /AlO _y /p ⁺ -Si RRAM.	71
Figure 4.2 Physical analysis of RRAM device. (a) Cross-sectional TEM image of the Ni/HfO _x /AlO _y /p ⁺ -Si memory cell. (b) Elemental analysis of EELS with direction from Si bottom electrode to Ni top electrode.	73
Figure 4.3 Typical $I - V$ curve of positive dc sweep of Ni/HfO _x /p ⁺ -Si and Ni/HfO _x /AlO _y /p ⁺ -Si RRAM devices.	75
Figure 4.4 Frequency dependence of ac conductance on LRS of both HfO _x and HfO _x /AlO _y based RRAM devices.	76
Figure 4.5 Temperature dependence of the current for HRS of Ni/HfO _x /p ⁺ -Si and Ni/HfO _x /AlO _y /p ⁺ -Si RRAM devices. The applied voltage is 0.2 V.	77
Figure 4.6 (a) Resistance distribution for 200 dc sweep cycles of HfO _x and HfO _x /AlO _y based single device. (b) Set voltage and reset voltage comparison for 200 dc sweep cycles of HfO _x and HfO _x /AlO _y based RRAM cells.	79
Figure 4.7 (a) Device-to-device resistance distribution in AlO _y /HfO _x based RRAM cells (ten devices each and 100 DC cycles of each device). (b) Device-to-device V_{set}/V_{reset} distribution in AlO _y /HfO _x -based RRAM cells (10 devices each and 100 DC cycles of each device).	80
Figure 4.8 Endurance characteristic of AlO _y /HfO _x based RRAM cell under pulse switching.	81

Figure 4.9 (a) Endurance characteristic of $\text{AlO}_y/\text{HfO}_x$ based RRAM cell under pulse switching.(b) Typical I - V curve of DC sweep for $\text{AlO}_y/\text{HfO}_x$ based RRAM at 200°C (repetition after 100 sweeps).	82
Figure 4.10 The dependence of set and reset current under SET current sweep of $\text{HfO}_x/\text{AlO}_y$ based RRAM.	84
Figure 5.1(a) Schematic of fabricated $\text{TiN}/\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ memory device. (b) Schematic of fabricated $\text{TiN}/\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ memory device.(c) Brief fabrication process flow of the RRAM devices.	87
Figure 5.2 Typical I - V curve of DC sweeps of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$. Rectification in LRS , the crosstalk phenomenon can be suppressed without connecting a diode.	89
Figure 5.3 $I - V$ characteristics and inserted circuit diagram of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ cell in LRS under various temperatures. Rectifying ratio @ 1V is $> 10^3$	90
Figure 5.4 Resistance distribution of device-to-device variation in (a) thin and (b) thick Ni cells in 100 cycles of 10 devices each.	91
Figure 5.5 Reverse current in LRS of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM cell. Current curve can be characterized by the Schottky emission model.	92
Figure 5.6 Temperature dependence of reverse current in LRS of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ at -0.5 V for various device sizes. Schottky barrier height is independent with device size.	93
Figure 5.7 (a) Schematic diagram of $\text{N} \times \text{M}$ cross-bar array structure. (b) Typical self-rectifying unipolar resistive switching device, inset shows simplified 2×2 array.(c) Extracted readout margin versus the WL number N in N^2 RRAM cells. The maximum number $N > 2^6$ can be realized using the self-rectifying RRAM cells.	95
Figure 5.8 Typical $I - V$ curve of DC sweep of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ under the unipolar resistive switching mode.	96
Figure 5.9 (a) Typical $I - V$ curve of D.C. sweep of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ under the bi-polar resistive switching mode. (b) $I - V$ characteristics and inserted circuit diagram of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ cell in LRS	97
Figure 5.10 Schematic diagram of the physical switching mechanism to clarify the coexisted (a) bipolar and (b) unipolar RS behaviors in $\text{p}^+\text{-Si}/\text{HfO}_x/\text{Ni}$. The electric-field induced oxygen ions drift and Joule-heating induced oxygen ions thermal-decomposition govern the bipolar and unipolar switching behaviors respectively.	99
Figure 5.11 Reverse current transport diagram in (a) $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ and (b) $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$	100

Figure 6.1(a) Brief fabrication process flow of the RRAM devices.(b) A schematic of fabricated TiN/Ni/HfO _x /p ⁺ -Si memory device.....	104
Figure 6.2 Cross-sectional TEM image of the TiN/HfO _x /NiSi memory cell.	105
Figure 6.3 Typical $I-V$ curve of dc sweep of TiN/HfO _x /NiSi.	106
Figure 6.4 (a) Resistance distribution of device-to-device variation in NiSi/HfO _x /TiN cells in 100 cycles of each of the five devices. (b) Rectification ratio distribution of device-to-device variation in TiN/HfO _x /NiSi cells in 100 cycles of each of the five devices.	108
Figure 6.5 Retention characteristics of TiN/HfO _x /NiSi RRAM at 125°C.....	109
Figure 6.6 (a) Schematic view of the crossbar memory array with N ² RRAM cells. (b) Maximum N increased with read voltage. Inset indicates the readout ratio versus WL number N for different read voltages. The maximum N can be extracted when the anti-cross-talk ratio approaches one.	110
Figure 6.7 Measured distribution of the $I_{reset} - R_{LRS}$ at 100μA compliance current in set process.....	111
Figure 6.8 Measured distribution of the $V_{reset} - R_{LRS}$ at 100μA compliance current in set process.	112
Figure 7.1 Comparison of endurance and reset current in excellent unipolar and bipolar RRAM [36, 95, 103, 104]......	113
Figure 7.2 Process flow and schematic structure of the Ni/AlO _y /n ⁺ -Si RRAM device.	115
Figure 7.3 HTEM image of Ni/AlO _y /n ⁺ -Si RRAM cell, 4.5 nm amorphous AlO _y layer is observed.....	116
Figure 7.4 (a) Unipolar resistive switching behavior of Ni/AlO _y /n ⁺ -Si RRAM device. (b) Bipolar resistive switching behavior of Ni/AlO _y /n ⁺ -Si RRAM devices.....	118
Figure 7.5 I-V curves of the LRS in linear scale of the Ni/AlO _y /n ⁺ -Si cell at different temperatures under bipolar RS mode.....	119
Figure 7.6 (a) Reverse current in LRS of Ni/AlO _y /n ⁺ -Si can be characterized by the Schottky emission model. (b) Temperature dependent current with Schottky conduction model fitting in LRS of Ni/AlO _y /n ⁺ -Si at -0.4 V.	120
Figure 7.7 Cumulative plot of I_{reset} for unipolar and bipolar RS modes.	121

Figure 7.8 Frequency dependence of A.C. conductance on LRS under unipolar and bipolar RS modes.	122
Figure 7.9 Cumulative probability plot of $I_{LRS-Forward}$, $I_{LRS-Reverse}$ and I_{LRS} under bipolar RS mode.	123
Figure 7.10 Retention time projected from the life time extracted from HRS at different temperature points.....	124
Figure 7.11 Comparison of calculated readout margins in NxN cross-bar array integrating RRAM cells with and without self-rectifying behavior. The maximum number $N > 2^5$ can be realized using the self-rectifying RRAM cells.	125

Chapter 1 Introduction

1.1. Background

Semiconductor device technology has continuously advanced through intensive active research and has experienced an inconceivable growth during the past two decades. Semiconductor products have followed well-known Moore's law, which predicts that number of transistors per integrated circuit would double every ~ 18 months [1]. In the beginning, only several components were integrated, nowadays, billions of semiconductor device components can be integrated into a chip size of thumbnail. In addition, the advanced microelectronic fabrication technology and the synthesis of nano-structure materials enable mass production of electronic devices with a critical dimension as small as sub-10 nm technology node.

There are many types of semiconductor device, including logic devices, memory devices and displays. Among these, non-volatile memory (NVM) is considered as an essential core component of nano-electronic system owing to high density, high speed and low power consumption. Recently, huge markets are available for NVM, such as in consumer electronics (TV, Stereo-audio, MP3, Digicam, *etc.*), internet communication (handphone, GPS *etc.*), computer (solid-state disk, desktop, laptop, display, printer, *etc.*), and military applications. Thus, it is no surprise that tremendous works have been done to develop low cost, low power consumption, high density and nonvolatile solid-state storage devices.

With the development of CMOS transistor technology, NVM based on FLASH memory has occupied a remarkably large share in electronic markets [2]. FLASH memory does not require refreshing, consumes less power and achieves high array density with stacked floating gate structure. Currently, Si-based FLASH memory density is the highest among other memory devices and technology for fabricating FLASH memory devices is most advanced [3]. Moreover, the scaling of FLASH memory is expected to come to an end beyond sub-20 nm node, due to serious challenges on both process development (*e.g.* lithography) and device limitation (*e.g.* coupling ratio, cross-talk between cells, short channel effect and few electrons for information storage) [4]. As a result, it is necessary to identify new emerging memory devices to overcome the problems of current non-volatile concept.

Faced with such a situation, a number of alternatives have been intensively studied for next generation of NVM [5]. The idea characteristics for a memory device consist of low power consumption, simple structure, fast programming speed ($\sim$ ns), long retention time (>10 years), good reliability, high integration density, continued scalability and compatibility with CMOS process. Recently, several potential candidates have been proposed to achieve these goals, ranging from magneto-resistive random access memory (MRAM) [6], ferroelectric RAM (FeRAM) [7], phase-change RAM (PRAM) [8], to resistive RAM (RRAM) [9].

Among these devices, RRAM has emerged as a strong potential candidate to be the front-runner due to lower programming currents and faster switching time, good and perfectible reality. More importantly, owing to its simple structure, 3D cross-bar architecture based on RRAM device is extremely promising solution for high density storage [5].

1.2. Motivation

RRAM has proven to be one of the most promising candidates for next-generation NVM or universal memories [10]. Currently, TMO-based RRAM device is the best candidate with great potential, owing to the excellent operating characteristics: 1) fast writing/erasing (W/E) speed (below than 10 ns W/E time is expected); 2) a simple device architecture (1Transistor-1RRAM (1T/1R) or 1Diode/1RRAM (1D/1R) can be employed to integrate the RRAM into IC); 3) low operating voltage (1-2V), which leads to low power consumption; 4) CMOS compatibility and thus very low cost of fabrication. In 2010 International Electron Devices Meeting (IEDM 2010), B. Govoreanu *et al.* [11] has first time demonstrated world's smallest HfO₂-based RRAM cell, featuring a novel Hf/HfO₂ resistive element stack, with very low power consumption, fast ns-range ON/OFF switching, an area of less than 10x10 nm², a switching energy per bit of 0.1 pJ or lower, an endurance of more than 5x10⁷ cycles, and excellent retention.

Moreover, although RRAM looks simple and promising, challenges are enormous to bring RRAM into mass-production. These challenges include: 1) partially understood material properties and physical mechanism on the resistive switching behaviors, 2) cell switching parameters variability from device-to-device, die-to-die and wafer-to-wafer in terms of material control and process integration control, (3) poor device reliability, especially the device retention. Based on the predication of International Technology Roadmap for Semiconductors (ITRS), in the near future, RRAM characteristics are expected to meet all major requirements for device-level non-volatile memory [12].

1.3. Objectives

Since 1960s [13], a large number of materials with reversible resistance switching have been explored as switching layers for RRAM. Among these switching materials, transition metal oxides (TMOs) are extensively investigated owing to simplicity of materials and compatibility with silicon CMOS BEOL fabrication process [9]. However, several obstacles still need to be overcome to meet the requirements of actual nonvolatile memory applications such as non-uniform switching, low W/E endurance, short retention time, high operation voltage, and required forming processes, which also causes large variation of the switching parameters. Therefore, this research project aims to design and realize a high performance RRAM devices based on TMO materials and integrate with CMOS circuit.

The objectives are described as following:

- (1) Based on the methodology, a high quality TMO material system with appropriate metal electrodes for RRAM application is designed and developed to address aforementioned concerns. Material investigation, process optimization, and device structure novelties are explored to achieve low operation voltage, high W/E speed, good endurance, and stable retention. This project intends to investigate more conventional and CMOS compatible oxides, starting from binary oxide system such as HfO_x , AlO_x , ZrO_x , TiO_x , *etc.* Important parameters such as thickness of switching layers, oxygen ion concentration, and impurity doping of the dielectric would be served as controlling parameters to modulate the device performance.
- (2) Investigate and clarify resistive switching behaviours and behind physical mechanisms on device switching, stability, uniformity, reproducibility, retention, scalability, and lifetime

prediction which are critical to bring RRAM into mass-production. By properly designing experimental work, the clear understanding of materials, optimization, and quantitative model is realized to predict RRAM device switching behavior and device performance.

- (3) The ultimate goal of this project is to provide the key materials/process/device solutions to realize a simple 3D RRAM circuit with appropriately selected device design. The basic RRAM device will be designed in-line with the requirements in the ITRS: a) ultra-low operating voltage ($<3\text{V}$) and current ($<500\text{nA}$); b) fast program/erase speed ($<10\text{ns}$); c) non-volatility properties with excellent endurance ($>10^8$ times); and d) excellent retention (>10 years @ 120°C).

1.4. Organization of Thesis

This thesis is divided into eight chapters. The organization is as follows:

- *Chapter One* provides background, motivation, objectives, organization and contributions of this project.
- *Chapter Two* is a literature review on research work that has been briefly summarized current FASH memory technology as well as several new emerging NVMs. We also briefly review the development of a new NVM concept, the RRAM, especially TMO-based RRAM. Applied integration of RRAM elements in large array, with the use of selector is also discussed in this chapter.
- *Chapter Three* presents a novel high yield HfO_x -based unipolar RRAM employing Ni electrode that is compatible with Si-diode selector for cross-bar integration.

- *Chapter Four* provides a comprehensive study of performance enhancement method for unipolar RRAM with AlO_y incorporation into HfO_x dielectric material.
- *Chapter Five* presents a novel self-rectifying HfO_x -based unipolar RRAM built by fab-available material.
- *Chapter Six* presents a self-rectifying HfO_x -based unipolar RRAM with NiSi electrode for CMOS compatibility and 3D integration.
- *Chapter Seven* discusses a self-rectifying AlO_y -based bipolar RRAM with sub-50 μA current for cross-bar array architecture.
- *Chapter Eight* provides the conclusions and the future extensions of this project.

1.5. Contributions

The main contribution of this thesis is the study of high performance TMO-based RRAM device for 3D cross-bar architecture. In Chapter 3, a unique high performance HfO_x -based unipolar RRAM with highly doped p^+ -Si substrate as bottom electrode has been demonstrated successfully. The RRAM cell exhibits good resistive switching performance, high window ratio ($>10^3$), fast switching speed ($\sim 50\text{ns}$), satisfactory retention time ($>10^5\text{s}$ @ 150°C), and excellent cycling endurance ($> 10^5$ cycles). Based on physical analysis and electrical characterization, the unipolar resistive switching (RS) behavior is observed in the memory cell is induced by rupture and formation of conductive filaments in association with the local Joule-heat-induced redox reaction inside NiO_x interfacial layer, which is in similar to the unipolar RRAM device with NiO_2 dielectric used as switching layer.

In Chapter 4, incorporation of AlO_y into HfO_x switching dielectric is employed to further enhance device performance. With doping effect, the distribution of operation parameters of bi-layer devices is much tighter compared to single layer devices. Highlights of the demonstrated RRAM include: 1) a high *ON/OFF* resistance ratio of $\sim 10^5$; 2) excellent cycle-to-cycle and device-to-device uniformity of switching parameters; 3) $\sim 100\%$ device yield on a 4-inch wafer; 4) satisfactory pulse switching endurance ($> 10^6$ cycles); 5) high temperature retention ($> 10^5$ s @ 120°C), and high temperature operating stability ($> 200^\circ\text{C}$) without threshold resistive switching; 6) a fast *SET/RESET* speed of $\sim 10/30$ ns; 7) fully CMOS compatible material and process; and with p^+ -Si bottom electrode (eliminating the use of noble metal Pt). By employing highly doped p^+ -type Si as bottom electrode in the memory cell, it is feasible to integrate with a vertical Si-diode as a potential selector for a possible high-density crossbar structure that is highly suitable for low-cost 3D integration.

In Chapter 5, CMOS friendly and low fabrication cost $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM device with unipolar RS behavior, and self-selection for cross-point array is successfully demonstrated. With rectifying characteristics and high forward current density observed in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM device, the sneak current path in conventional cross-bar architecture is effectively eliminated. The self-rectifying behaviors or nonlinearity $I - V$ characteristics are encouraged to increase the array size without a series selection part (*e.g.* diode, transistor, *etc.*), so that higher integration density could be achieved. The asymmetry and rectifying reproducible behavior in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ memory cell is resulted from the Schottky barrier of defect state level in $\text{SiO}_x/\text{HfO}_x$ junction and $\text{n}^+\text{-Si}$ substrate.

In Chapter 6, NiSi has been used as the Source/Drain (S/D) contact for the mainstream CMOS technology. As a result, HfO_x -based RRAM with NiSi bottom electrode that is suitable

for advance CMOS technology process is investigated for the integration concern. The performance of this memory cell, switching mechanism and possible passive cross bar structure are studied. Highlights of the demonstrated RRAM include: 1) CMOS technology friendly material and process; 2) well-behaved unipolar RS behavior (ON/OFF ratio $> 10^2$); 3) forming-free RS; 4) wide read-out margin for high density cross-point memory devices (number of word-line $> 2^6$ for worst case condition). The demonstrated RRAM has the obvious rectification in LRS ($> 10^3$ at 1V), so the crosstalk phenomenon can be alleviated without serially connecting a diode. Owing to the self-rectifying effect, memory cell can significantly improve misreading in matrix crossbar memory without extra rectifying selectors.

The cross-bar architecture based on bipolar RRAM gets attractive attentions because performance of bipolar RRAM (*e.g.* power, reliability *etc.*) is generally demonstrated with better performance than unipolar one partially due to their inherent different switching mechanisms [14]. In Chapter 7, it is the first time, CMOS friendly and low fabrication cost $Ni/AlO_x/n^+-Si$ RRAM with bipolar switching, low current, and self-selection for cross-point array structure is reported. 3D memory stacks employing demonstrated self-rectifying bipolar RRAM are extensively explored for the sake of ultra-high density. The vertical electrodes of proposed RRAM stack sharing the same Si-nanowire with vertical gate-all-around (VGAA) Si-MOSFETs as current limiter is realized for Vertical-RRAM (VRRAM) cross-point structure. By implementing RRAM cell on VGAA Si MOSFET, the 1T-1R structure is scaled down to $4F^2$ footprint in one plane. By stacking the cross-point arrays in n layers, an effective cell size of $4F^2/n$ is achieved. VRRAM cross-point memory expects to be an excellent candidate to replace NAND FLASH memory when CMOS technology scales to sub-10nm node.

The above works have been published in world-recognized conferences, which are *IEEE International Electron Devices Meeting (IEDM)* and *IEEE Symposium on VLSI Technology and Circuits (VLSI)*, as well as prestigious journals, such as *Electron Device Letters (EDL)* and *Transactions on Electron Devices (TED)*.

Chapter 2 Literature Review

2.1. FLASH Memory Overview

There are two main categories in memory including volatile and nonvolatile. Volatile memory (VM) is memory that loses any data after the power supply is turned off, thus it requires constant power to remain viable. In contrast, non-volatile memory (NVM) is memory that retains its data even when the system or device is turned off. Currently, the leading memory technologies are Dynamic Random Access Memory (DRAM) and FLASH memory [15]. The former is used for VM and owing to its charge-based switching mechanism, its scalability is limited. Among the existing NVMs, FLASH memory turns out to be the dominant NVM which leads memory technology to be scaling down to critical dimension continuously [4].

Figure 2.1 (a) Schematic of a typical FLASH memory cell, (b) Drain-Source (D-S) current versus Gate voltage bias, threshold voltage (V_T) shift caused by change in electronic charge on storage element [4].

A typical FLASH memory cell consists of a single floating gate transistor and retains a '1' or a '0' bit by storing a certain amount of charge on the floating gate (Fig.2.1 (a)). The amount of charge stored on the floating gate determines the threshold voltage (V_T) of device (Fig. 2.1 (b)). Advanced FLASH memory technology can retain more than 1 bit per cell, making it possible to allow much higher memory density without scaling the cell-size. Due to the charges stored in the potential well between the blocking layers and tunneling oxide layers, the data could be maintained even after the power supply turns off, resulting in NVM operation.

NOR and NAND FLASH are two main technologies of FLASH memory used today [2]. A great success with respect to the memory cell-size reduction and the corresponding product cost decrease are achieved in both classes. NOR FLASH device implements channel hot electron (CHE) injection for the programming. In addition, NOR FLASH device requires a separate metal contact for each cell and is arranged with transistors in parallel thus the cell size is about $10F^2$ feature size [4]. NAND FLASH device applies Fowler-Nordheim (FN) tunneling for the programming operation. The array architecture does not require any metal contact in the cell, so that the cell size can be scaled down to a minimal $4F^2$ feature-size [4]. As such, NAND FLASH has a denser layout than NOR FLASH and is used for most removable solid-stated memory application today.

However, the NAND FLASH device is currently facing a number of difficult and challenging issues in further scaling down to sub-20nmtechnology node. The issues include :1) scaling limitation; 2) few electron storage; 3) breakdown between neighboring word lines; and 4) high capacitive coupling of the control gate with floating gate and coupling of adjacent cells

[4].Currently, there is un-known solution to any of the aforementioned problems. As a result, NAND FLASH memory device will eventually beat its scaling limit.

To keep on the expansion of NVMs beyond sub-20nm technology node, it is necessary to quest for new alternative memories. New emerging NVMs should meet several requirements for NAND FLASH replacement such as simple structure, low fabrication cost, lower power consumption, faster W/E programming speed, better endurance, scalability down to sub 10 nm technology node, and most importantly a possible integration in cross-bar architecture for higher density storage. NVMs that do not inherently based on charge storage have demonstrated potential to substitute FLASH memory. Among these NVMs, it is expected that RRAM meets the above requirements.

2.2. Emerging Non-volatile Memory Overview

2.2.1.Magneto-resistive Random Access Memory (MRAM)

A MRAM utilizes a tunneling magneto-resistive (TMR) effect that exhibits change in the resistance once the magnetic field applied in a magnetic tunneling junction (MTJ) for data storage[16].AMRAM cell consists of a transistor in series with one MTJ to form 1T-1MJT structure as shown in Fig.2.2. When the electrons move across the fixed magnetic layer, the spin of electrons is aligned by the applied magnetic field. The spin direction of electrons will remains when passing through the tunneling layer. In case the free layer has an opposite polarity, the spin is realigned, inducing high resistance state (HRS). Otherwise, memory cell keeps low resistance state (LRS).

In early stage, MRAM is operated under an external magnetic field to toggle the free layer, giving rise to high power consumption and large cell size. To overcome this issue, a spin transfer torque (STT) type of MRAM has appeared to become a most attractive solution recently [17]. In STT-MRAM cell, a torque is self-generated by interaction among the spin-polarized current and the spin of the magnetic layer and spin-polarized current [6]. The STT switching technique brings significant advantages to magnetic random access memory (MRAM). STT-RAM enables MRAM scalability beyond 90 nm by reducing write current more than 10x in a 1-T (transistor)/1-MTJ memory cell architecture, and leads to simpler memory architecture and manufacturing than conventional MRAM [18].

In addition, one of the major drawbacks of conventional MRAM has been the increase of switching current as the technology scales down. STT-RAM solves this switching current problem by applying the spin polarized current through the MTJ element. Fast and steady advances in reduction and the obvious advantages of STT-RAM have led to more and more international and domestic industry activities in STT-RAM. SONY Corporation has demonstrated for the first time a 180 nm logic STT-RAM test chip in 2005 [19], and Hitachi and Tohoku University have demonstrated a circuit design for a 2 Mb STT-RAM chip in 2007 using a 200 nm CMOS process [20].

Figure 2.2 Illustration of a field-switched MRAM cell undergoing read and write operations [16].

MRAM was originally thought to be the next generation candidate to replace flash memories, but it showed many serious problems that affect the ability for high-density storage. The major MRAM disadvantage is the high current in writing process. To operate MRAM device, the current density is required up to 10^6 - 10^8 A/cm² range, which increase power consumption. In addition, it is worth noting that the writing current must go through the tunnel oxide in MTJ, this may degrade the reliability of the device. As a result, the most important task for MRAM development is programming current reduction before it brings to mass-production.

2.2.2. Ferroelectric Random Access Memory (FeRAM)

FeRAM exploits a ferroelectric materials such as $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$, Lead Zirconate-Titanate, also known as PZT (Fig. 2.3(a)), sandwiched between two metallic electrodes [21]. A

remanent polarization induced by switching the spontaneous polarization of the material indicates two stable states at zero applied voltage as shown in Fig.2.3.(b) [21].

Figure 2.3 (a) Schematic diagram of PZT crystal structure, and (b) hysteresis loop characteristic of a ferroelectric capacitor [21].

To identify the state of such a FeRAM, a voltage pulse is triggered to take the device to the extreme of its hysteresis loop, which comes out with a current spike whose magnitude depends on the initial state [7]. Moreover, this readout process is destructive due to the FeRAM cell ends up in the same final state that does not depend on the original data. Therefore, a subsequent write step is required after a successful read operation. A large switching endurance is required to take over the FLASH memory. Until now, FeRAM is one of the strongest early candidates to be the next NVM owning high operating speed ($<20\text{ns}$), lower power consumption and possibility of straightforward CMOS integration. However, the FeRAM devices also show serious problems such as reliability (*e.g.* the remanent polarization degrades with number of switching), poor scaling prospective, and unsatisfactory retention (*e.g.* loss of stored polarization

over time) [7]. The expansion of high density memory based FeRAM device has faced a lot of challenges over the last several years due to lack of materials breakthrough that may resolve the above issues [22].

2.2.3. Phase-change Random Access Memory (PCRAM)

PCRAM device employs the resistive switching between the amorphous and crystalline states in phase-change material. Chalcogenide glass (e.g. $\text{Ge}_2\text{Sb}_2\text{Te}_5$) normally is used as switching material in which the amorphous phase exhibits high electrical resistivity, while the crystalline phase shows a low electrical resistivity, approximately four or five orders of magnitude lower [23]. The basic mechanism of PCRAM is well understood. In case the phase-change layer at the heart of the PRAM element is amorphous, the electrical resistance across the device is high. I the phase-change material is crystalline, the resistance is low. Fig. 2.4 illustrates the operation of a typical PCRAM device. The Joule heating effect is employed to switch the states of the cell. By triggering an electrical pulse, a large portion of the switching material is heated to its crystallization temperature in set operation [23]. This operation decides the writing speed of PCRAM cell because the required duration of the electrical pulse depends strongly on the crystallization speed and thermal stability of the phase-change material. Most phase-change materials crystallize slower than 10ns.

Figure 2.4 Illustration of operation of a typical PCRAM device.

PCRAM has been demonstrated high endurance ($> 10^{12}$ cycles), inherent scaling of the phase change process beyond 22 nm node, fast speed (< 10 ns), and integration at the technology nodes down to 32 nm. Recently, 30×30 nm² PCRAM devices have been demonstrated with excellent switching performance and more scalable than NAND FLASH memory. The demonstrated density, cycling endurance and read/write speed either are on par or exceeded NOR FLASH. The most important unknown for the success of PCRAM technology is whether the memory access device such as diode or transistor in a dense memory array will be able to supply sufficient current to reset the phase-change memory cell. However, even with this difficult integration task, the success of PCRAM technology may end up depending on advances in the access device as much as on the phase change memory cell itself [24].

2.2.4. Resistive-switching Random Access Memory (RRAM)

Beside these memory technologies, RRAM is being developed by many companies and institutes [9] due to its potential of becoming next generation NVM or maybe universal memory. The high speed, low power, high integration density and CMOS compatibility of the device are the principal merits.

It is worth mentioning that RRAM is also sometimes referred to as memory resistor (memristor), a fourth element of integrated circuit [25]. Memristor was mathematically predicted by Prof. Leon Chua in his seminal research paper in *IEEE Transaction on Circuit Theory* on the symmetric background [25]. It was widely announced that the memristor was the god particle for science and engineering domains. After four decade in 2008, researchers at the Hewlett–Packard (HP) laboratories reported the development of a new basic circuit element that completes the missing link between charge and flux linkage, which was postulated by Chua [26, 27]. However, the prediction of memristor is based on symmetrical relationship between charge and magnetic flux but in early realized memristor does not having magnetism and magnetic signals which neither applied nor measured [28]. As a point of view of resistance, the direction of charge flow will be increase or decrease the memristor resistance but this dependency in charge and resistance at the nanoscale is very well known to the world before it is predicted. The hype of memristor further create problem regarding with the implementation viewpoint. The memristor promises faster, smaller and cheaper technology, but there is no scientific evidence of commercial device level memristor is realized and reported in the literature until now. The memristor does not having proven and matured technology that changes the mainstream silicon technology [29].

2.3. General Introduction of RRAM

In 1962, Hickmott illustrated for the first time the hysteresis of current-voltage ($I - V$) characteristics in metal-insulator-metal (MIM) structure of $\text{Al}/\text{Al}_2\text{O}_3/\text{Al}$ [13], representing that the resistance changes as a result of applied electric fields. Fig.2.5 (a) shows a typical RRAM with MIM structure.

Figure 2.5 (a) Schematic diagram of a typical RRAM cell, and (b) Typical resistive switching behavior of RRAM cell [9].

Because materials exhibiting resistive switching behavior are typically amorphous or polycrystalline, resistive switching (*RS*) devices are also referred as amorphous semiconductor devices. Subsequently, *RS* behavior has been reported in other binary metal oxides. Based on this characteristic of MIM, several studies and reviews started in 1990 have demonstrated its potential application on NVM [30, 31]. The basic operating principle of RRAM is demonstrated in Fig. 2.5(b), the device is able to be abruptly switched between high resistance state (*HRS*) and low resistance state (*LRS*) by applying write voltage [32].

HRS represents “*OFF*” state while *LRS* represents “*ON*” state. In addition, these resistance states keep almost unchanged even when not powered. As a result, *RS* device is a kind of NVM effect. Recently, with the advancement of CMOS fabrication techniques, RRAM has been considered as one of the candidates of the next generation NVM due to high programming speed, CMOS compatibility, and ease of fabrication.

2.4. Basic Operational Switching of RRAM

A *RS* phenomenon employs a hysteretic *I-V* characteristic referring to the switching between a *LRS* and *HRS* in MIM structure. Either current or voltage is applied between two electrodes to control the resistance states. During the switching process, the switching from *HRS* to *LRS* is called “*SET*” process, and resistance switch in other way, from *LRS* to *HRS*, is named “*RESET*” process [32]. When applied voltage reaches *SET/RESET* voltage, the operation of *RS* happens, that is, unless the applied voltage is as high as the *SET/RESET* voltage, the resistance of memory cell retains its state. This nonvolatile *RS* characteristic can be applied to NVM applications.

The operation of *RS* is distinguished by two different schemes based on the electrical polarity, as shown in Fig. 2.6. *RS* is classified into unipolar resistive switching (*URS*) (Fig. 2.6 (a)) and bipolar resistive switching (*BRS*) (Fig. 2.6 (b)). It is worth noting that both *URS* and *BRS* can be observed in the same RRAM device. *URS* is independent from the applied voltage polarity. It means that both the set and reset process happen at the same polarity of the voltage or current. As a result, the applied voltage must be accurately controlled in the unipolar switching to avoid the overlap of *SET* and *RESET* process [33]. In *SET* process, a current compliance is required to protect the memory cell from permanent breakdown [34]. The *SET* voltage is usually higher than the reset voltage, and the reset current is usually higher than the current compliance during *SET* operation.

Figure 2.6 Two types of resistance switching behavior : (a) unipolar RS and (b) bipolar RS [33].

In *BRS*, the applied voltage polarity plays an important role in the resistive switching behavior. The set and the reset-applied voltages are opposite to each other. The set switching happens at one voltage polarity, but the reset switching happens at the other polarity. Therefore,

both the amount of the applied voltage and its polarity must satisfy proper conditions for the BRS operation. In Set process, the current compliance sometimes is not necessary.

The important parameters of RRAM that are considered to evaluate memory performance include operating voltage, resistance ratio, endurance, retention time, device yield, and even multilevel storage.

1. Operating voltage/current (*SET/RESET* voltage/current)

It is well known that high operating voltage and current is a disadvantage for low power application. When the operating voltage increases, power consumption also increases and reliability decreases. In addition, reliability can be a problem with a high operating voltage. To prevail over FLASH memory, which undergoes from high power consumption, the operating voltages for RRAM devices is requested to be only a few volts.

2. *ON/OFF* ratio

The *ON/OFF* Ratio is an essential parameter to distinguish the difference between memory states. For RRAM, it is classified as the ratio of *HRS* to *LRS*. *ON/OFF* ratio directly influences the accuracy of data reading. In term of circuit aspects, a minimum *ON/OFF* ratio of 10 is required [35]. A highly stable *ON/OFF* ratio is attractive for multi-level storage and high-density cross-bar array.

3. Write/Read (*W/R*) speed

Write/Read speed is defined as the minimum time for writing or reading a RRAM cell. Recently, the fastest operating speed has been reported to date by Lee *et al.* [36] on the RS characteristics of a TiN/TiO_x/HfO_x/TiN RRAM stack. The operating speed of this device is as fast as 5 ns. The write time of FLASH memory is at the order of 10⁻⁶s to 10⁻³s. To gain an

advantage over FLASH memory, the best operating speed of RRAM devices is expected between 5 and 50 ns.

4. Endurance

Endurance is the maximum number of *SET/RESET* cycles that an RRAM device can be switched until no longer distinguishable. Good endurance is also a crucial requirement for the commercial application of RS memory devices. FLASH memory has demonstrated a maximum number of write cycles between 10^3 and 10^7 cycles. Therefore, RRAM should offer an endurance of greater than 10^7 , even a better one.

5. Retention time

Retention time is the length of time a RRAM cell can keep programmed state after writing process. Most quality nonvolatile available memories are expected to retain their value for at least 10 years at room temperature, either with the power on or off.

6. Multi-level memory

Multi-level RRAM indicates that memory cells are able to operate reproducible switching between more than two resistance states and, consequently, enhance the storage density. The multilevel switching requires a large enough *ON/OFF* ratio between each state to ensure an external circuit to distinguish between states. The compliance current (I_{comp}) or operating voltage is governed to achieve multilevel memory.

7. Device yield

Device yield indicates percentage of working cells. Using a suitable electrode material or doped metal oxide [37] or intentionally introducing metal nano-crystals [38] in the oxide seems to improve the device yield. In order to evaluate systematically the performance of RRAM

devices fabricated in this study, we use the above indicators to depict and compare performance of devices.

2.5. Resistive Switching Mechanism

2.5.1. Classifications of Resistive Switching Mechanism

Although RRAM has been intensively investigated in recent years, the underlying fundamental principles of the switching mechanism are still under heated debate. So far, several switching models have been proposed to explain different observed phenomena. Although the physical driving force of all these resistive switching is electrically induced, it is quite different from one another. Fig 2.7 represents five groups of resistance switching mechanism according to ITRS 2010 [35]. The resistance switching mechanism can also be divided into three types in terms of position. They are interface effect, bulk effect and combination of bulk and interface effect.

Figure 2.7 Classification of the resistive switching effects are considered for nonvolatile memory applications [39]. Phase change mechanism is mainly found in chalcogenides like GeSbTe or AgInSbTe [40].

Regarding to phase change mechanism, the resistance of switching materials is determined by the transition between crystalline phase and amorphous phase induced by a thermal process. This switching mechanism normally is used to the change of resistance in PCRAM. For commonly defined RRAM, it usually refers to the categories of thermo-chemical memory effects, electrochemical metallization effects, electrostatic/electronic effects and valence change memory effects. These mechanisms are to be discussed in details in the following part. To date, no single mentioned model can describe all the experimental results obtained from numerous switching materials. It seems that the thermo-chemical mechanism and phase change mechanism can address parts of the unipolar switching mode, while other switching mechanisms can explain most of the bipolar switching modes. However, the distinction between the two switching behaviors is ambiguous.

2.5.2.Thermo-chemical Mechanism (TCM)

The thermo-chemical mechanism (TCM) is generally observed in TMOs. It is also identified as fuse/anti-fuse type. Because the switching mechanism is based on thermal effects, it is inherently unipolar switching operation. NiO_x has been considered the most prominent candidate material for resistive switching based on the TCM effect, first reported in the 1960s [41]. Recently, various transition metal oxides have been studied and unipolar type has been observed. Some examples are TiO_x , HfO_x , CuO_x [9]. Fig 2.8 shows a typical log current-voltage behavior of a NiO_x based RRAM with Pt electrodes.

Figure 2.8 Unipolar I-V characteristic of a Pt/NiO/Pt stack with a NiO film thickness of 50nm [39].

Within the first sweep starting at 0V, by performing a so-called forming process, MIM structure exhibits an abrupt current increase at a voltage of approximately 4.6V. To protect RRAM cell from hard-breakdown, a current compliance (I_{comp}) is applied. The forming process turns the cell into the *ON* state. Afterward, the cell can reset by increasing the voltage up to 1V. The cell suddenly turns into the *OFF* state again. Thereafter, the entire cycle can repeat with the exception that the *SET* voltage is generally lower than the forming voltage of the first sweep at about 2V.

As schematically depicted in Fig.2.9, the RS characteristic is imitated by a voltage-induced partial dielectric breakdown, which forms a discharge filament heated by Joule effect. Within the first sweep, the current suddenly increase at a forming voltage. The sudden current increase is limited by I_{comp} to protect switching layer from breakdown. Subsequently, the RRAM

cell can be switched between two resistance states. When *SET* voltage is applied, the insulator is heated to soft breakdown. Since I_{comp} is applied, only a weak conduction filament is formed. During the *RESET* process, a voltage is triggered without a limiting compliance current. The conductive filament is once again ruptured thermally as a consequence of a very high power density of the order of 10^{12} W/cm² [32]. As plotted in Fig. 2.9, the difference between the initial state and the OFF state indicates that the filament still exists but partially disrupted.

Figure 2.9 Schematics of (a) the initial state as well as (b) forming, *SET*, and (c) *RESET* process [42].

RESET characteristics are to large extent decided by the forming and *SET* transition, which is responsible for the formation and properties of filaments. Within this type of switching mechanism, there are two fundamentally resistive switching characteristics including threshold switching and memory switching. Threshold switching is observed when the electronic *ON* state caused by the localized thermal runaway does not result in permanent resistance change. Memory switching is observed when the permanent *ON* state is established [39]. The material properties of the actively switching layers and the structural properties of the switching cell and,

more specifically, the thermal properties will govern the interchange between threshold switching and memory switching. Heat conduction of the electrodes is also expected to play a key role within this scenario as they serve as heat sink.

For instance, M. Janousch *et al.* [32] studied microscopic origin of switching mechanism of Cr-doped SrTiO₃ based RRAM device. By using infrared thermal microscopy, the majority of the power is dissipated near the anode electrode (Fig. 2.10) indicated by the “hot spot”, which gives an evidence of Joule heating mechanism.

Figure 2.10 Infrared thermal micrograph of a planar Cr-doped SrTiO₃ single-crystal cell. The cell has a current of 5mA at an applied voltage of 30V [32].

Russo *et al.* [43] simulated electrical conduction and heating properties in the localized conductive filament. Fig 2.11 shows that the reset process itself-accelerated as a result of a positive feedback between the thermal dissolution of the filament and local Joule heating effect in the filament bottleneck, which can explain the abrupt resistance change.

Figure 2.11 Calculated temperature map for applied voltages of (a) 0.53, (b) 0.78, (c) 0.85, and (d) 0.87V across a conductive filament (CF) with length $t_{NiO} = 160$ nm and an initial diameter of 100 nm. The CF edge is also shown, indicating the thermally activated shrinking effect.(e) Measured and calculated $I - V$ and $R - V$ characteristics [43].

2.5.3. Electrochemical Metallization Mechanism (ECM)

Electrochemical metallization system (ECM) is also known as programmable metallization cell (PMC) or conductive bridging (CB) cell or solid-electrolyte (SE) cell in the literature. Electrochemical metallization is related to cation-migration induced redox reaction. During the electroforming process, the oxidation of metal electrode takes place at the anode interface, and then positively charged metal cations migrate toward the cathode made of inert metal and are reduced at the interface [39]. The electric field enhanced which leads to formation of a metallic conductive path growing toward the anode. After the metal filament has grown enough to contact the cathode electrode, it turns the cell to the *ON* state. The *ON* state retains unless an adequate voltage of opposite polarity dissolves the metal atoms from the edge of metal filament and eventually annihilates the filament, after which the cell is reset to *OFF* state. It is worth noting that there is an electronic current through the metallic bridge and, in parallel, an electrochemical current (called Faradic current) dissolves the metal filament in the initial phase of reset.

Fig 2.12 schematically illustrates the basic principle of operation of an ECM memory cell with typical $I - V$ characteristic. An ECM memory cell consists of an electrochemical active metal (*e.g.* Cu or Ag), a thin solid electrolyte layer (*e.g.* M^{Z+} ion-conductor) and an electrochemically inert counter-electrode (*e.g.* Pt, Ir, W or Au)). Ag or Cu is typically used as the electrochemically active anode with $GeSe_x$ as a switching material. Recently, Y. Yang *et al.* [44] presented explicit evidence that localized, nano-scale filaments consisted of elemental metals (and, in some cases, composing of discrete nano-particles instead of a solid wire) are formed

during resistive switching. The filament growth is critically dependent on the cation mobility in the dielectric film.

Figure 2.12 Typical I - V characteristic of Ag/Ag-Ge-Se/Pt electrochemical metallization cell. The insets A to E show the different stages of the switching procedure [45].

Figure 2.13 Observation of conducting filament dynamics in SiO_2 -based resistive memories, (a) TEM image of an as-fabricated SiO_2 -based RRAM device (*Inset*: schematic of the device), (b) TEM image of the same device after the forming process. The arrows highlight several representative filaments. (c) TEM image of the same device after erasing [44].

Ag and Cu are frequently used as electrochemically active metals and phase separated amorphous (*e.g.* selenides and sulfides) as well as various oxides, acting as solid electrolytes in the studied ECM systems [32]. During last decade, the development of ECM devices has achieved advanced progress, fast switching of 100ns and high *ON/OFF* ratio of larger than five orders of magnitude were illustrated.

2.5.4. Valence Change Mechanism (VCM)

The third possible switching mechanism is valence change mechanism (VCM). This mechanism occurs in many oxides, especially binary transition metal oxides. VCM refers to anion transport induced redox type. Within this type of switching mechanism, there are two fundamental models that based on geometrical localization of switching event are conductive filamentary type [39] and homogenous interface-type switching [46] as illustrated in Fig.2.14.

Figure 2.14 Schematic of two types of VCM based on geometrical localization : (a) conductive filamentary type, and (b) homogenous interface-type [33].

The major difference between two types can be examined by the area dependence of the cell resistance. In conductive filamentary type, the *LRS* resistance does not depend on the electrode area, whilst in the latter, the *LRS* current is distributed homogeneously over the whole area, and hence, the *ON* resistance is proportional to the electrode area. These two types have also been used to elucidate the bipolar switching in most of the transition metal oxides.

For filament type switching, anions, oxygen-ions defects in many TMO, typically oxygen vacancies which are much more mobile than transition metal cations. During the electroforming process, they migrate to and accumulate at the cathode; therefore, an oxygen deficient region starts to grow up and to expand towards the anode. Oxygen vacancies affect the valence state of the transition metal cations and transition oxide into conductive phase by forming metallic conductive channel. Thus, the conduction path is composed of highly oxygen deficient, non-stoichiometric phase, which shows higher conductivity than normal phase. This may due to the fact that only a very small portion of the whole area is turned into conduction path and the remaining area contributes to a parallel resistance. Consequently, the *ON/OFF* ratio improves significantly with scaling on the basis that *HRS* is proportional to the electrode area. In this respect, filamentary VCM shows excellent scaling prospects. However, the controllability of the filament formation and rupture might be a problem. Owing to this characteristic, this switching mechanism is called VCM. K. M. Kim *et al.* [47] have detected oxygen gas evolution at the top electrode surface of their bipolar TiO_2 switching cells during the electro-forming process as shown in Fig.2.15. Janoush *et al.* [48] have examined the oxygen concentration region between top and bottom electrode using spectroscopy (XANES) spectra. Lee *et al.* [49] have studied the composition change in their unipolar NiO switching cells by secondary ion mass spectroscopy (SIMS), during set process, it indicates that the oxygen ions within the NiO_x layer migrate to the

Pt electrode after the switching, thus forming the Ni-rich filaments in NiO_x bulk. This proves that the behavior of oxygen vacancies in transition metal oxide plays an important role in resistance switching. It is known that HfO_2 , ZrO_2 , AlO_2 also belong to this category.

Figure 2.15 (a) Schematic diagram of oxygen vacancy migration and the growth of a CF from the cathode in TiO_2 . Electroforming-induced morphological change occurring in Pt/ TiO_2 /Pt cells under (b) a positive and (c) a negative voltage applied to the top electrode of a switching cell [47].

Beside conductive filamentary type, other publications in the literature reported about resistive switching characteristic, which exhibits electrode area dependent resistance in LRS. A so called homogenous interface-type switching has been reported by Sawa *et al.* [33], it is observed between different conductive oxide and metal electrode. For this type of switching cells, the device resistance scales with area and the change of resistance attributed to the field-induced change of Schottky-barrier at the interface homogeneously distributed over the entire electrode area. An electric field is applied, oxygen vacancies can migrate toward and effectively

change the width of the barrier. If the vacancies moved away from the metal electrode, the width of the barrier increases and electron transport takes place over the barrier to denote the HRS as shown in Fig. 2.16 (a). The current is lower and strongly unidirectional, so the metal/oxide interface behaves as Schottky barrier. Conversely, if the vacancies are pushed towards the electrode, the barrier becomes narrower and electron tunnel through as shown in Fig 2.16 (b) to denote *LRS*.

Figure 2.16 Barrier modulations by oxygen accumulation along the interface between (a) *HRS* corresponding to a wide barrier, and (b) *LRS* corresponding to a narrow barrier [50].

Another successful approach towards a design of resistive switching cells with tunable parameters was presented by Meyer *et al.* [51]. In this memory cell, they introduce a thin tunneling oxide (TO) between electrode and a conductive metal oxide (CMO). The working mechanism of this kind of switching cell is based on the modulation of potential barrier height of tunneling oxide by electric field induced oxygen ion transfer between the conductive oxide and the insulating tunneling oxide. The resistive switching in the memory cell can be understood in terms of a variation of the space.

2.6. Switching Materials and Transition Metal Oxides (TMOs)

The resistive switching phenomena have been observed in variety of metal-insulator-metal structures. There have been many investigations on the improvement of switching materials and electrical switching properties. A number of materials used as switching layer are listed in Table 2.1.

Table 2.1 Summary of resistance switching materials for RRAM device [5].

Binary Metal Oxide	HfO _x , ZrO _x , TaO _x , NiO _x , NbO _x , TiO _x , CuO _x , MnO _x , WO _x , VO _x , MgO _x ...
Perovskite	PCMO($\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$), LCMO($\text{La}_{1-x}\text{Ca}_x\text{MnO}_3$), BSCFO($\text{Ba}_{0.5}\text{Sr}_{0.5}\text{Co}_{0.8}\text{Fe}_{0.2}\text{O}_{3-\xi}$), YBCO($\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$), (Ba,Sr)TiO ₃ (Cr,Nb-doped), SrZrO ₃ (Cr,V-doped), (La,Sr)MnO ₃ , Sr _{1-x} La _x TiO ₃ , La _{1-x} Sr _x FeO ₃ , La _{1-x} Sr _x CoO ₃ , SrFeO _{2.7} , LaCoO ₃ , RuSr ₂ GdCu ₂ O ₃ , YBa ₂ Cu ₃ O ₇ , SrTiO ₃ , SrZrO ₃ ...
Others	Ge _x Se _{1-x} (Ag,Cu,Te-doped), Ag ₂ S, Cu ₂ S, Cds, ZnS, CeO ₂ , SiO ₂ , ...

Although the materials reported in Table 2.1 have illustrated different resistive switching, only a few promising candidates are considered, and then continue to further improve their performance and understand the switching mechanism. Among them, transition metal oxides (TMOs) have been receiving considerable attention over last few decades owning their good electrical properties that are required to reach the requirements of nonvolatile memory, the simplicity of the material and compatibility with silicon oxide-semiconductor field effect transistor (CMOS), Back-End-Of-Line (BEOL) fabrication process. In the early stage, the TMO-

based RRAM demonstrated with large device sizes, high *SET/RESET* operating voltages ($> 4V$), large switching currents ($\sim mA$), slow operating speeds ($\sim \mu s$), low switching cycles ($< 10^2$ cycles) and short retention time. Recently, advances in TMO-based RRAM demonstrated in literatures are reviewed in Table 2.2.

Table 2.2 A representative list of transition metal-oxide RRAM device characteristics [9].

	NiO IEDM 2004	Ti:NiO IEDM 2007	TaO _x IEDM 2008	Ti/HfO _x IEDM 2010	WO _x IEDM 2010	N:AlO _x VLSI 2011	TaO _x /Ta ₂ O ₅ IEDM 2011	Hf/HfO _x IEDM 2011
Switching Type	Unipolar	Unipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar
Structure	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R	1T-1R
Cell Area (μm^2)	~ 0.2	~ 0.49	~ 0.25	~ 0.0009 (30nm)	0.0036 (60nm)	~ 1	~ 9000	0.0001 (10nm)
Speed	$\sim 5\mu s$	$\sim 5ns$	$\sim 10ns$	$\sim 0.3ns$	$\sim 50ns$	N/A	$\sim 10ns$	$\sim 10ns$
Peak Voltage	$< 3V$	$< 3V$	$< 2V$	$< 2.5V$	$< 3V$	$< 2V$	$< 2.5V$	$< 1.5V$
Peak Current	$\sim 2mA$	$\sim 100\mu A$	$170\mu A$	$200\mu A$	$\sim 1mA$	$\sim 50nA$	$\sim 30\mu A$	$\sim 50\mu A$
HRS/LRS Ratio	> 10	> 90	> 10	> 100	> 10	> 100	> 100	> 10
Endurance	10^6	100	10^9	10^{10}	10^6	10^5	10^{12}	5×10^7
Retention	300h@ 150°C	30h@ 150°C	3000h@ 150°C	28h@ 150°C	200h@ 150°C	28h@ 125°C	3h@ 200°C	30h@ 250°C

RRAM device sizes now aggressively scale down to $10 \times 10\text{ nm}^2$, programming currents are now in the order of μA range; programming and read speed are on the order of ns; endurance cycles are up to 10^{12} , retention time is near 3000 hours at $150^\circ C$, the forming process can be eliminated. Chip-scale memory array with Mb size was demonstrated. Baek *et al.* [10] studied several TMO device properties that indicate: (a) the forming voltage depends linearly on film thickness. (b) under the condition of the increasing cell size, the resistance of fresh cells

decreases proportionally, while low and high resistance states slightly decrease. The threshold voltages do not change with cell size variation. (c) the asymmetric resistance transition speeds are represented, where the high resistance state transits to low resistance state at a faster rate than the low resistance state transits back. (d) the TMO-based RRAM devices have excellent thermal stability. Besides the metal oxide material itself, the materials for the top and the bottom electrodes are also critical in determining the memory device characteristics. It is found that even for the same oxide material but with different electrode materials, the switching mode can be drastically different. The reported references suggest that HfO_x , AlO_x has a great potential to be a strong candidate for the next generation of non-volatile memories. In this regard, HfO_x , AlO_x were chosen as the resistance switching material in this theoretical study. Here we choose HfO_x , AlO_x , ZrO_x , NiO_x because they have drawn most attention and have been extensively studied in the past several years. The deposition methods of these binary oxides usually include the oxidation of the corresponding metal, reactive sputtering, pulse laser deposition (PLD), and atomic layer deposition (ALD). Among these methods, ALD is recently widely used due to the ability to precisely control the thickness and uniformity of the thin film.

2.7. RRAM Integration

2.7.1. Introduction of RRAM Integration

The previous discussion has been mainly emphasizing on the nature and operations of RRAM devices itself. However, the applied integration of RRAM elements in large array, with the use of selection devices is equally or possibly even more important in order to realize high-density memory. Presently, two basic integrating solutions for RRAM device consist of active

array and passive array. According to industry R&D trend, the active array is used for embedded NVM and the passive array mainly is used for stand-alone NVM. The passive crossbar array is more promising than the active array from the point of view fabrication processing and storage density because of several reasons. One reason is the inherently high density which allows for $4F^2$ cells, where F is minimum feature size of fabrication technology. A second reason is the chance further shrink the size of passive matrix, without the need to do the same for the MOSFETs. The third reason lies in the fact that a potential 3D stacking is easier and more effective for passive crossbar than active CMOS circuits.

2.7.2. Active CMOS Array

An active CMOS array typically employs a MOSFET in series with an RRAM cell, to form the 1T-1R structure [52], as shown in Fig 2.17 (a). In this structure, each RRAM cell is selected or isolated by a transistor. In this active array, the RRAM cell size depends on that of selection transistor, and since a transistor consists of three terminal contacts for access, the minimum cell size is $6F^2$ (F is the minimum feature size). Recently, Wang *et al.* [53] has proposed new structure by using a multi-emitter bipolar junction transistor (BJT) with vertically formed underneath resistive stacked films of TiN/Ti/HfO₂/TiN to substitute MOSFET, lead to the minimum cell size decreased to $4F^2$ (Fig. 2.17 (b)). By using superior structure, RRAM cells can simply be implemented in advanced CMOS logic platforms for ultra-high density and very low voltage applications. In fabrication processing technology, the MOSFET and the BJT are implemented in the Front-End-of-Line (FEOL) processing, and RRAM cell usually integrated in BEOL processing. Though the integration method is capable of increasing the storage density, thermal budget should be taken into account to avoid material degradation.

Figure 2.17 Schematic diagram of RRAM active array(a) 1MOSFET-1RRAM, and(b) 1BJT-1RRAM [53].

The circuit diagram of an active RRAM is classified into three categories of array including NOR, NAND and AND [54].

Figure 2.18 Circuit diagram for an active RRAM in (a) NOR array, (b) NAND array, and (c) AND array with resistive switching MIM structures for memory application [54].

In the NOR architecture, 1T-1R cells are connected in parallel, which is comparable with DRAM and FeRAM (Fig. 2.18 (a)). The selected cell's MOSFET is operated by applied voltage between word-line and bit-line. The plate line is applied to V_{DD} or ground to invert voltage drop over the RRAM cells for bipolar switching purpose. In the NAND architecture, a set of 1T1R cells is connected in series, where the RRAM cell is in parallel to source/drain (S/D) of the transistor (Fig. 2.18 (b)). So far, the structure is comparable with NAND-FLASH and chain FeRAM [55]. Recently, Mustafa *et al.* [54] has proposed the AND architecture (see Fig. 2.18 (c)) which is similar with the NOR structure. However, the plate line, which is used for the voltage inversion, is in parallel with the bit line for AND architecture. Consider a row of 1T-1R cells, the leakage current passing through unselected cells must be much smaller than the current passing

through the selected cell. Normally, MOSFETs have specified *ON/OFF* ratios of 10^4 - 10^5 . This recommends that number of bit-lines should not be more than $\sim 10^4$. This conclusion also applies to BJT-based 1T-1R cells.

2.7.3. Passive Array

One of promising advantage of RRAM devices is their ability for cross-bar array architecture, transistors as selection devices may not be applicable. As a result, a passive crossbar RRAM arrays are very attractive for future memory technologies and achieve very high density with the simplicity of their manufacturing. Recently, two different designs have been pursued for ultra-high-density passive crossbar RRAM arrays (dimension: $4F^2/n$), e.g. X-point RRAM and Vertical-RRAM (VRRAM) [56]. X-point RRAM constitutes of word lines and bit lines perpendicular to each other, with resistive switching cells put in between the crossing points (Fig. 2.19 (a)). VRRAM employs vertical NAND like structure where RRAM cells are stacked between vertical electrodes (Fig. 2.19 (b)). Being possible in crossbar architecture, it can be scaled to $4F^2$ dimensions, the best possible scaling so far in memory. In addition, the memory element in RRAM can be simply integrated into the BEOL process. Therefore, the cells can be vertically stacked with metal lines, called a 3-D cross point architecture. Further scaling is possible by vertical stacking of crossbars e.g. n times scaling will make the cell area $4F^2/n$. Considering process and storage density, passive crossbar array is not only the prior choice to integrate RRAM but also the most economical solid-state memory.

(a)

(b)

Figure 2.19 (a) Schematic of 3D X- point array architecture based RRAM device. A selector is connected in series with RRAM cell to eliminate cross-talk interference. (b) Schematic of 3-D Vertical-RRAM (VRAM) array architecture. RRAM cells share same vertical electrode in this design.

However, utilizing passive crossbar array, every cross-point must have the switching characteristic in order to eliminate the crosstalk phenomenon which will result in misread[57]. The challenge of passive crossbar arrays is the accessibility of a specific junction. Parasitic bypasses include the risk of crosstalk, which means that nearby junctions are unintentionally programmed or interfere with the stored information of a specific cell during its operation. Fundamentally, a device is switched when the applied voltage exceeds the write or the erase voltage.

1. Write program

There are two schemes to program data into the memory cells which are the $V_{dd}/2$ and the $V_{dd}/3$ schemes [57]. The choice of scheme depends mainly on the properties of the resistive material.

Figure 2.20 Schematic diagram of two schemes to program data into the memory cells (a) $V_{dd}/2$ and (b) $V_{dd}/3$ schemes [57].

To program a cell using the $V_{dd}/2$ writing scheme, the selected row is biased at V_{dd} , the selected column is grounded, while all the other un-selected row and column electrodes are charged with $V_{dd}/2$ (Fig. 2.20 (a)). Apart from the selected cell, the voltage drop over all unselected cells is correspondingly between 0 and $V_{dd}/2$. A second writing scheme can be used if the deviations of the threshold voltages are larger than $V_{dd}/2$. In this scheme, the selected row is biased at V_{dd} , the selected column is grounded, while the remaining unselected row are biased at $2V_{dd}/3$ and the respective column electrodes are biased at $V_{dd}/3$ (Fig. 2.20 (b)). As a result, the maximum voltage drop along un-selected cells reduces to $V_{dd}/3$. The disadvantage is however the provision of an additional voltage level. If the threshold voltage for switching is well defined and the material is insensitive for voltages below the threshold then the scheme $V_{dd}/2$ would be preferred since it is easier to implement. Otherwise, the $V_{dd}/3$ is used to reduce the distortion voltage on non-accessed cell.

2. Read program

The reading voltage of un-selected WLs/BLs affects the sensing margin. Reading information from the crossbar is conducted by applying a certain read voltage across a junction and transforming the current flow into a voltage. This can be achieved by forming a voltage divider with a pull up resistor and the resistance in the accessed junction. The output of the voltage divider is then connected to a CMOS read circuit (Fig. 2.21). The voltage swing at the output of the crossbar read circuit between reading a high impedance state and reading *LRS* has to be large enough to be CMOS compliant. The read circuit implemented in CMOS technology can be of any amplifier [58].

Figure 2.21 Optimal CMOS setup of reading operation for RRAM based crossbar architecture [58].

In general, there are three different ways of accessing selected cell in the crossbar array structure [58]:

1. Select on word line, pull up one bit line, the other bit lines floating. This approach will save the power consumed in the crossbar, but the accessing time is slow because only one bit can be accessed at a time.
2. Select one word line and pull up all bit lines simultaneously. This approach will increase the power dissipation. One advantage is the read-out speed can be increased significantly by reading multiple outputs at the same time.

3. Select one word line, pull up some of the bit lines simultaneously and leave the other bit lines floating.

2.7.4. Cross-talk Interference

In the resistive switching memories, no matter bipolar or unipolar RS characteristic, the I - V curve in the LRS is almost symmetric in both negative and positive of applied voltage. If WL/BL resistance and access resistance from voltage sources are negligible, cross-bar arrays of any size can be simplified to a 2×2 array structure. Taking a simple 2×2 array as an example, a selected RRM cell in HRS will be misread as LRS if the sneak current path is passed through the other three neighboring cells in LRS , called the crosstalk phenomenon (Fig. 2.22). In a $M \times N$ ($N, M > 2$) crossbar array or a 3-D stacked array, the number of the sneak current paths is larger, making the misread more serious. This crosstalk phenomenon not only limit the signal swing, which annihilates the advantage of the high density of the cross-bar array by adding large sensing circuits and lowering the memory array efficiency but also reduce array size. To resolve this problem, an effective RRAM selector with rectifying behavior is absolutely required to realize a high density, low-power memory.

Figure 2.22 Schematic of crosstalk phenomenon in 2×2 cross-bar architecture.

2.7.5. Selection Devices

A memory cell in array can be viewed as being composed of two fundamental components: the ‘Storage node’, which is usually characterized by the physics of operation of different memory devices, and the ‘Selector’, which allows a given memory cell in an array to be addressed for read or write. Both components affect scaling limits of memory. It should be noted that for several advanced concepts of resistance-based memories, the storage node could in principle be scaled down below 10 nm [59], and the memory density will be limited by the select device. Thus, the select device represents a serious bottleneck for RRAM scaling to 10nm and beyond. The select device is a non-linear element, which can operate as a switch. Typical examples are transistors (*e.g.* FET or BJT) or 2-terminal devices, *e.g.* diodes. Up to now, a planar FET is commonly used as the select device in practical memory arrays, such as DRAM or flash. In a two-dimensional layout using in-plane select FETs, the cell layout area is $6-8 F^2$. In order to reach the highest possible 2-D memory density of $4F^2$, a vertical select transistor needs to be used, and this approach is currently being pursued.

2.7.5.1. Diode-Type Selection Device

The simplest realizations of two-terminal memory select devices use semiconductor diode structures, such as a pn-junction diode, Schottky diode, or heterojunction diode. Such devices are suitable for a unipolar memory cell. For bipolar memory cells, selectors with two-way switching are needed. Proposed examples include Zener diodes, reverse breakdown Schottky diode, and complementary resistive switches. In the latter approach, the memory cell is composed of two identical non-volatile RRAM switches connected back-to-back [12]. In such a configuration, one of the switches will always be at the high-resistance state so the sneak current

can be suppressed at low bias. The read operation however is destructive, and the cell state needs to be recovered by re-programming the disturbed switch back to *HRS* afterwards. It should be noted that several read modes have been suggested which could be adapted to specific applications.

2.7.5.2. Resistive-Switch-Type Selection Device

The category of “switch-based selector” refers to recent innovative device concepts that exhibit resistive switching behavior. In fact, in some of these concepts, the device structure/physics of operation is similar to the structure of the storage node. In other words, a modified memory element could act as a select device. The main difference between the two is that a ‘nonvolatile’ switch is required for the storage node, while for the select device, depending on the approaches, non-volatility may not be necessary and can sometimes be detrimental. A brief description of several proposed select devices is given below.

2.7.5.3. Metal-Insulator transition (MIT) Switch

This device is based on the Metal-Insulator Transition, such as Mott transition, and exhibits a low resistance above a critical electric field (threshold voltage). The select device will exhibit a high-resistance state if the voltage is below a hold voltage. To achieve reliable read the select device needs to be volatile to ensure rapid transition from the low-resistance state to high-resistance state at low bias. If the electronic conditions that triggered Mott transition can relax within the operation time scale, the Mott transition device is essentially a volatile resistive switch, which can be utilized as a select device. A VO_2 -based device has been demonstrated as a

select device for NiO_x RRAM element [60]. However, the switching mechanism is not clear and the feasibility of the Mott-transition switch as select devices still needs further research. It should be also noted that VO_2 undergoes a phase transition to the metal state at temperature around 68°C , and thus its operation as MIT switch is restricted to temperatures below 68°C . This limits practical applications of VO_2 in memory devices as current specifications require operational temperature of 85°C . Suitable Mott materials with higher transition temperatures need to be investigated. Recently, metal insulator transitions at $\sim 130^\circ\text{C}$ and electrically driven MIT switching were observed in thin films of SmNiO_3 [61].

2.7.5.4. Threshold Switch

This type of select device is based on the threshold-switching effect observed in thin-film based MIM structures, where the threshold switching is caused by electronic charge injection. An electronic switching process thus governs operation of the threshold switch. Significant resistance reduction can occur at a threshold voltage and this low-resistance state quickly recovers to the original high-resistance state when the applied voltage falls below a holding voltage. One example is the threshold switching which occurs before the structural change in phase change materials [62].

2.7.5.5. Mixed-ionic-electronic-conduction (MIEC) Switch

This type of select device is based on the exponential I-V characteristics observed in materials that conduct both ions and electronic charges so called mixed ionic and electronic

conduction materials (MIEC). The resistive switching mechanism of MIEC switch is similar to the ionic memories. With appropriate control, the resistive switching in MIEC devices is volatile and provides device selection functions.

2.7.6. Self-rectifying RRAM Device

The cross-talk interference during the operation of cross-point arrays can be eliminated if selection devices were integrated in each cell. However, selection devices owned serious problems to achieve high density cross-point based RRAM devices. For instance, integrating diode not only increases the complexity of fabrication, also lead to the increase of operation voltage and hence the degradation of the memory stability for unipolar resistive switching. The conduction current of many resistive switching materials have a linear relationship with area, and the current density of the diode is an important factor affecting its scaling limitation.

Table 2.3 summarizes solutions and selector's drawbacks for both RRAM types. Recently, the quest of self-rectifying resistive memory has been actively pursued for both bipolar and unipolar types. Owing to the rectification in *LRS*, the crosstalk phenomenon can be alleviated without serially connecting a selector. The memory cell can significantly reduce the complexity of fabrication, lower the reading voltage and improve misreading in matrix crossbar memory without extra selector device; the self-rectifying resistive memory has been actively pursued.

Table 2.3 Solutions and selector's drawbacks for both RRAM types for cross-bar array.

Types of RRAM device	Selector	Selector Drawbacks
Unipolar RS	p-n Diode (Sc-Si, Poly-Si)	Complex structure
	Schottky Diode (n-ZnO, Ge NW, a-Si, p-Si, Pt/TiO ₂)	Loss of voltage drop on diode
	Heterojunction Diode (n-ZnO/p-Si, CuO/InZnO)	Low current density when RRAM cells scale down to sub-nm node
Bipolar RS	Complementary Resistive Switching (CRS)(eg. Pt/GeSe/Cu/GeSe/Pt)	-Fixed read-out voltage leads to destructive readout
	MIT (eg. VO _x , NbO _x)	Thermal stability issue
	MIEC Switch	Metal ion control , not stable under high temperature
	Ovonic Threshold Switch (OTS) (Chalcogenide alloy undisclosed)	Need to use material Composition
	Reverse Breakdown (Cu/n-Si)	Loss of voltage drop on diode

Until now, several self-rectifying RRAM devices has been demonstrated such as Ag/a-Si/p-Si [63], Au/ZrO₂:Au-nanocrystal/n+-Si [64], TiW/Ge₂Sb₂Te₅/W [65], Si/a-Si core/Ag nanowire [66] . As an anti-fuse, the fresh device can be set to a low resistance state and kept in *LRS* permanently with a rectification ratio exceeding 10⁴. M. Jo *et al.* [67] manufactured a RRAM using a self-formed Schottky barrier based on Al/PCMO/TiN structure. These devices have such advantages as complete compatibility with CMOS technology, simple structure, and good stability. Furthermore, they can overcome the problems caused by the serially installed diode in the 1D-1R crossbar array, such as increased operation voltage and poor endurance. In

consequence, self-rectifying RRAM devices are highly competitive for the high density passive crossbar array application.

Chapter 3 High Yield HfO_x-Based Unipolar Resistive RAM Employing Ni Electrode Compatible with Si-Diode Selector for Cross-Bar Integration

3.1. Introduction

In this chapter, a unique high-performance and high yield unipolar RRAM based on HfO_x dielectrics and Ni electrode on highly doped p⁺-Si substrate are presented. The performance of this memory cell, the current transport mechanism and possible switching mechanism are investigated. The unipolar device shows well-behaved memory performance, such as high ON/ OFF resistance ratio ($> 10^3$), good retention characteristics ($>10^5$ s at 150°C), satisfactory pulse switching endurance ($>10^5$ cycles),and a fast programming speed of about 50 ns. More importantly, it also exhibits almost 100% device yield on a 4-in wafer. By using highly doped p⁺-type Si as bottom electrode, the memory cell makes it feasible to employ a vertical Si-diode as a selector for crossbar structure integration, highly suitable for low-cost 3D integration.

3.2. Experimental Details

Fig 3.1 illustrates the schematic diagram (Fig. 3.1 (a)) and fabrication process flow of Ni/HfO_x/p⁺-Si stack (Fig. 3.1 (b)). After standard RCA cleaning process, HfO_x films with thickness of ~3 nm were deposited using Atomic Layer Deposition (ALD) at 250°C on 4-inch p⁺-Si substrate ($N_A \sim 10^{19} \text{ cm}^{-3}$). ALD is known as an industry-preferred solution for uniform deposition of ultra-thin film over a large area. Subsequently, a 100 nm Ni top electrode was fabricated by physical vapor deposition (PVD) at room temperature and followed by lift off process into final devices with areas ranging from 50x50 to 500x500 μm^2 . Ni has been widely used in the current mainstream CMOS technology as source/drain (S/D) contact metal, and has also been widely reported to be used as the metal gate in the form of fully-silicide metal. From this viewpoint, there is no contamination issue for Ni. In addition, Ni can be patterned using dry etching such as Cl₂/Ar gases that are commonly available in the IC fabrication. Finally, all samples are received a 425°C forming gas annealing for 30 minutes.

The microstructure and elements of the stacked layers of the devices were investigated by high-resolution cross-sectional transmission electron microscopy (HR-XTEM) in combination with electron energy loss spectroscopy (EELS). Chemical composition was analyzed with X-ray photoelectron spectroscopy (XPS). The electrical measurements were performed using a Keithley 4200-SCS semiconductor parameter analyzer and an Agilent 8110a pulse generator at the ambient condition.

Figure 3.1 (a) Schematic of fabricated Ni/HfO_x/p⁺-Si RRAM cell. (b) Brief fabrication process flow of RRAM cell.

3.3. Results and Discussion

3.3.1. Physical Analysis of RRAM Cell

In Fig. 3.2 (a), HTEM image of the fabricated Ni/HfO_x/p⁺-Si capacitor reveals that the HfO_x layer is amorphous and with a thickness of ~3 nm. A SiO₂ interfacial layer between HfO_x and p⁺-Si substrate can be identified, which is a native oxide SiO_x and also can be formed during ALD deposition process. From EELS study (Fig. 3.2 (b)), the diffusion of oxygen atoms from HfO_x layer into Ni top electrode is observed, leading to the formation of NiO_x interfacial layer between HfO_x dielectrics and Ni electrode. The thin layer of NiO_x may not be observed clearly in HTEM image due to the surface roughness of the HfO_x layer.

Figure 3.2 (a) Cross-sectional HTEM image of the Ni/HfO_x/p⁺-Si memory cell. (b) Elemental analysis of EELS with direction from Si bottom electrode to Ni top electrode.

XPS study conducted on 5 nm Ni thin film on same 3 nm HfO_x layer further verifies NiO_x layer formation, as shown in Fig. 3.3. Adventitious hydrocarbon C_{1s} binding energy at 285eV was used as a reference to correct the energy shift of N_{2p} core levels due to differential charging phenomena. This NiO_x interfacial layer is believed to play a key role for the unipolar switching observed in our devices, which shall be explained in more details in later part. NiO_x switching

layers has been reported as one of candidates, which exhibit good unipolar resistive switching recently.

Figure 3.3 Ni_{2p} XPS scan of 5nm Ni film on the 3nm HfO_x layer. (The signal is calibrated with C_{1s} .)

3.3.2. Electrical Characterization of RRAM Cell

3.3.2.1. DC Resistive Switching Characterization of RRAM Cell

In Fig. 3.4, the RRAM device shows well-behaved unipolar resistive switching current-voltage (I - V) characteristics using D.C. sweep. It is noted that the I - V characteristics of RRAM cells are measured at 75° C. To activate the device, a forming process is initiated with a forming

voltage of $\sim 3\text{V}$. In the *SET* process, a positive voltage sweep ($V_{set} \sim 2.1\text{V}$) with a current compliance of $100\mu\text{A}$ triggers the conduction abruptly, and the resistance switches from *HRS* to *LRS*. Afterward, another voltage sweep ($V_{reset} \sim 1.1\text{V}$) causes the abrupt decrease of current and the resistance switches back to *HRS* (denoted as *RESET* process). The polarity independence of the *SET* and *RESET* transition indicates unipolar RS characteristics. The unipolar RS characteristic observed in demonstrated device is related to the rupture and formation of conductive filaments in association with the local Joule-heat-induced redox inside NiO_x interfacial layer.

It is especially worth mentioning that the yield of the devices is almost 100%: 100 devices with various areas were randomly measured from the 4-inch wafers. The devices measured exhibited similar unipolar switching characteristics and did not show any degradation in switching properties after 100 switching cycles. It is worth noting that the unipolar RRAM device is generally connected in series with high performance diode for the cross-bar architecture. By using Si as bottom electrode, the Si-diode is considered as viable low cost option for the proposed RRAM device. To clarify the role of SiO_x interfacial layer, control devices with various metals (*e.g.* Pt, TiN and Au) as the bottom electrode and with same HfO_x dielectric material and Ni top electrode were fabricated as a control sample. The devices have shown unipolar resistive switching without the appearance of SiO_x layer. In addition, by using Pt as top electrode (Pt/HfO_x/Si), both unipolar and bipolar RS were not observed. Due to the SiO_x formation is formed by the native oxide and during HfO_x growth process, many defects are located inside very thin SiO_x layer, which induced high conductivity of this insulator. As a result, SiO_x interfacial layer does not play key role in $I - V$ behavior of RRAM device.

Figure 3.4 Typical $I - V$ curve of positive DC sweep. The compliance current (I_{comp}) is set at 10^{-4} A.

3.3.2.2. Current Conduction Mechanism of RRAM Cell in *LRS* and *HRS*

In Fig. 3.5, temperature dependence of the electrical conductivity is used to study the current transportation mechanism during RS of the fabricated devices. It is seen that the *LRS* current is independent on temperature (300-450K) and is linear with applied voltage, implying metallic Ohmic behavior [68] (Fig. 3.5 (a)). On the other hand, the conduction of *HRS* current strongly relies on temperature (See Fig. 3.5 (b)). To find out the dominant switching factors, the value of activation energy controlling the conductivity in HRS was calculated, supposing the following relationship:

$$\sigma = \sigma_0 * \exp\left(-\frac{E_a}{kT}\right)$$

where σ , is the conductivity, E_a is the activation energy, k is Boltzman's constant and T is the absolute temperature. The activation energy of charge transport under *HRS* is estimated to be 0.18eV.

Figure 3.5 Temperature dependence of the current for (a) *LRS* and (b) *HRS* of Ni/HfO_x/p⁺-Si device. The applied voltage is 0.2 V.

To clarify current transport in *HRS*, the AC (1KHz to 1MHz) conductivity measurements were also done with AC signal amplitude of 10 mV (to minimize the influence to the device). The frequency dependent AC conductance measured from both fresh and *HRS* devices are illustrated in Fig. 3.6. Total conductivity of RRAM can be expressed as $\sigma(\omega) = \sigma_{dc} + \sigma_0 \omega^s$ where σ_0 is a pre-exponential factor, ω is the angular frequency and s is the frequency exponent. For fresh devices, AC conductance is linearly proportional to exponential frequency ω^s , with s of ~2 which indicates localized defect states [69].

Figure 3.6 Frequency dependence of AC conductance on fresh state and *HRS* at 25°C.

The frequency response of the AC conductance of fresh device is well fitted with an AC electrical conductivity of the Mott's 3-D variable hopping model (VRH) [70]. Mott's VRH theory describes the low temperature behavior of disorder semiconductor where states are localized [70]. The atoms in amorphous material are distributed at random and electrons associated with them have distribution energy. An atom might have an empty state whose energy is slightly higher than that of occupied state of a chosen give atom. Typically, the activation energy required for electrons to hop to an empty state is very small and hence the conduction take place. The hopping distance varies because of the random arrangement of the atom having suitable energy scales and hence the name is give as VRH. Therefore, AC conductance result suggests that the conduction transport in fresh and *HRS* device is electron hopping through localized oxygen vacancies in HfO_x [71]. At low oxygen vacancy concentration corresponding to *HRS* and fresh state, the oxygen vacancies act like electron-trapping centers that induce 3D variable hopping conduction under electric field. It is interesting to observe that *HRS* has a residual conductance in low-frequency region. The partially recovered filament may contribute this frequency-independent difference in conductance between *HRS* (after *RESET*) and fresh device.

3.3.2.3. Resistive Switching Performance of RRAM Cell

The data retention measurement of the memory cell at a high temperature of 150°C is shown in Fig. 3.7, without observable degradation.

Figure 3.7 Retention behavior of RRAM device measured at 150°C.

Despite of the fluctuation in *HRS* resistance values, the *ON/OFF* ratios larger than 3 orders of magnitude can be well maintained after 100 cycles (Fig. 3.8 (a)). Fig. 3.8 (b) shows the *SET* and *RESET* voltage distribution after 100 cycles. The *RESET* voltage varies from 1.10 ~ 1.62 V while the *SET* voltage ranges from 1.91 ~ 2.32 V.

Figure 3.8 (a) Resistance distribution for 100 DC sweep cycles. (b) *SET* and *RESET* voltage distribution for 100 DC sweep cycles.

The switching endurance of the RRAM device is studied with pulse width of 50 ns, and no degradation is seen after 10⁵ switching cycles (Fig. 3.9). Note that the *SET* and *RESET* voltages under pulse measurement are larger than those obtained by DC sweep mode, which is believed to be due to the parasitic *RC* delay during the measurement [72].

Figure 3.9 Endurance characteristic of RRAM device under pulse switching. The 50 ns pulse is set by equipment and stable switching more than 10⁵ cycles is obtained.

3.3.2.4. Resistive Switching Mechanism of RRAM cell

Finally, possible switching mechanism of the demonstrated devices is illustrated in Fig.- 3.10. As control samples, various metals (Cu, Ag and Pt) instead of Ni as the top metal electrode was fabricated with the same dielectrics of ALD HfO_x on p⁺-Si. With Pt top electrode (similar work function as Ni), no successful switching characteristics can be measured, i.e. the device cannot recover to *HRS* after being programmed to *LRS*. It indicates that the conducting filament paths in HfO_x may not breakdown under high voltage in *RESET* process. According to electrochemical metallization (ECM) theory [32], in resistive switching memories with active electrodes (Ag or Cu) as anode and inert electrodes (Pt) as cathode, when a positive bias voltage is applied on the anode, metal atoms will be oxidized to active metal ions at the anode and migrate to the inert cathode, and eventually reduced back to metal atoms at the cathode/electrolyte interface. With the accumulation of these metal atoms, they will grow toward

the anode, and connect the anode with the cathode, eventually turn the memory on. Therefore, Cu and Ag top electrodes are fabricated to compare the ability of Ni diffusion in HfO_x layer under electric field. By using Al, Cu and Ag as the source of mobile ions due to its faster diffusion rate and ability to create filamentary paths, the devices show unipolar switching with very low endurance (< 15 cycles), large dispersion of switching parameters and low on/off ratio (<50). It reveals that the switching behavior of device may not be due to the immigration of Ni ions into dielectric under electric field. Wang *et al.* [73] systematically investigated different HfO_x-based resistive random access memory stacks with Ni-containing electrodes. In this report, there is no clear indication of Ni diffusion through the ~10-nm HfO_x layer from the EDX analyses, consistent with TOF-SIMS results from similar stacks [74]. Therefore, NiO_x and Ni involvement at the interface, rather than Ni filaments through the switching layer [75], [73], would play the key role for the unipolar switching shown here. More specifically, the reduction/oxidation reactions inside the Ni involved interfacial layer, corresponding to SET: NiO_x→Ni and RESET: Ni→NiO_x [76], will finally determine the formation/rupture of conductive filaments in-between HfO_x and electrodes. Considering this, in combination with XTEM/EELS and XPS study shown in Fig. 3.10, the unipolar resistive switching can thus be explained by the rupture and formation of conductive filaments in association with the local Joule-heat-induced redox inside NiO_x interfacial layer, which is in analog to the unipolar RRAM device based on NiO_x dielectrics.

Various oxide dielectric materials (ZrO_x, AlO_x, SiO_x *etc.*) have been implemented to replace HfO_x in the work. The devices also illustrated unipolar resistive switching behaviors like HfO_x-based RRAM. However, only AlO_x and HfO_x as dielectric layer show good and stable device performance. The randomness in ruptured conducting filaments inside other transition

metal oxides may be induced the poor switching uniformity. Therefore, in my work, HfO_x material is implemented for dielectric materials to achieve high performance RRAM device

Figure 3.10 Schematic diagrams illustrating the possible formation or rupture of filament under *SET* and *RESET* process for a Ni/HfO_x/p⁺-Si RRAM device.

3.4. Conclusion

In summary, a unique reproducible unipolar RRAM Ni/HfO_x/p⁺-Si due to the formation/rupture of an electrically active filament in NiO_x is reported. The memory cell possesses excellent performance of high resistance ratio (*ON/OFF* ratio > 10³), long retention time (> 10 years), fast 20ns switching time, excellent cycling endurance (> 10⁵ cycles). Besides, by using highly doped p-type Silicon as bottom electrode, the hafnium oxide-base memory with Si-diode is promising for future highly-density-crossbar nonvolatile memory.

Chapter 4 Performance Enhancement for Ni Electrode Unipolar Resistive RAM with AlO_y Incorporation into HfO_x Switching Dielectrics

4.1. Introduction

In Chapter 3, HfO_x -based RRAMs with Ni electrode is presented in detail. Their switching performance still need to be further improved to meet ITRS requirement for unipolar RRAM device. In this chapter, a Si-diode selector compatible high performance unipolar RRAM with Ni-electrode/ $\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ structure is demonstrated. Compared to the single-layer HfO_x devices, the demonstrated $\text{HfO}_x/\text{AlO}_y$ -based RRAM shows a high *ON/OFF* resistance ratio of $\sim 10^5$, decent switching parameters uniformity ($V_{\text{set}}/V_{\text{reset}}$, HRS/LRS), satisfactory pulse switching endurance ($>10^6$ cycles), high temperature retention ($>10^5\text{s}$ at 120°C), high temperature operating stability (200°C) without threshold resistive switching, and a fast set/reset speed of $\sim 10/30$ ns.

4.2. Performance Enhancement of Resistive Switching Characteristic with Bi-layer and Doping Technology

The RS behavior in a transition metal oxide (TMO) based RRAM device is mainly explained by the formation and rupture of the conducting filaments inside the switching layer

[77]. The conductive percolation path is formed by defects, such as oxygen vacancies and metal ions. These defects are induced by decomposition of metal oxide materials themselves or diffusion process from the electrode under applied voltage. However, the applied voltage should be high to generate defects in pure TMO films. As a result, the quality of the switching layers degrades faster under high electrical stimulus, resulting in the poor resistive switching performance. In addition, large distributions in *SET/RESET* voltages and *HRS/LRS* resistance are generally observed in undoped-TMO-based RRAM devices. The poor uniformity not only reduces the stability of the device, but also enhances the complexity of the peripheral circuit for read/write operations.

To improve switching uniformity, various approaches were proposed such as structure optimization (*e.g.* top electrode control, multi-switching layers, localized path) and defect control (*e.g.* doping method, active film scaling, device area scaling). Among these approaches, doping technology is an effective method for modulating and improving RRAM's performance. The conductive filaments are formed/ruptured near the impurities doped location. This reduces the randomness of the CF formation/rupture process and improves the uniformity of the resistive switching properties. As a result, the RS performance and yield can be improved and high voltage no longer is necessary. Gao *et al.* [78] found that the average forming voltage of the TiN/HfO₂/Pt device decreased from 7.82V to 2.71V and RS uniformity is enhanced by doping Al in the HfO₂ films. Recently, Wang *et al.* [79] reported that the retention characteristics of both resistive states in the CuO_x-based RRAM can be significantly improved by doping Si impurities.

Although Al doping effect was applied for bipolar HfO_x-based RRAM, doping technology was not studied in detail for unipolar RS. Therefore, Al-doping effect on unipolar RS is investigated to further understand the beneficial impact of metal doping in the proposed

RRAM cell. In this work, compared to the single-layer HfO_x devices, the demonstrated bilayer HfO_x/AlO_y devices can significantly enhance unipolar switching characteristics of unipolar HfO_x- based RRAM.

4.3. Experimental Details

Schematic diagram and brief fabrication process flow of RRAM cell are shown in Fig. 4.1 (a) and Fig. 4.2 (b). Respective amorphous HfO_x and HfO_x/AlO_y films were grown using Atomic Layer Deposition (ALD) at 250° C on the 4 inch p⁺-Si substrates (N_A ~10¹⁹ cm⁻³). Subsequently, a 100-nm Ni top electrode was fabricated by physical vapor deposition and followed by a lift-off process to form final devices with areas ranging from 50x50 to 500x500 μm². Finally, all samples are received a 425°C forming gas annealing for 30 minutes.

Figure 4.1 (a) Schematic diagram and (b) Brief fabrication process flow of Ni/HfO_x/AlO_y/p⁺-Si RRAM.

The microstructure and elements of the stacked layers of the devices were investigated by high-resolution cross-sectional transmission electron microscopy (HR-XTEM) in combination with electron energy loss spectroscopy (EELS). The AC and DC current–voltage and resistive switching characteristics of the fabricated RRAM device were obtained using a Keithley 4200-SCS semiconductor parameter analyzer and an Agilent 8110a pulse generator in ambient condition.

4.4. Results and Discussion

4.4.1. Physical Analysis of RRAM Cell

In Fig. 4.2 (a), cross-sectional TEM image of the fabricated $\text{Ni}/\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ capacitor reveals that the high-k dielectric films are amorphous. The total thickness of the high-k stack is ~ 4.2 nm with no distinguishable boundary between HfO_x and AlO_y . A SiO_x interlayer is formed between $\text{HfO}_x/\text{AlO}_y$ and Si. From EELS analysis (Fig. 4.2(b)), the inter-diffusion of Al atoms into HfO_x films is revealed, consistent with XTEM results. Diffusion of oxygen atoms from HfO_x layer into the Ni top electrode was also observed, leading to the formation of NiO_x interfacial layer between HfO_x and Ni electrode. NiO_x formation was also verified by XPS characterization [80]. As reported in previous chapter, the thin NiO_x layer contributes to the formation/rupture of filament in unipolar switching behavior of devices.

Figure 4.2 Physical analysis of RRAM device. (a) Cross-sectional TEM image of the Ni/HfO_x/AlO_y/p⁺-Si memory cell. (b) Elemental analysis of EELS with direction from Si bottom electrode to Ni top electrode.

4.4.2. Electrical Characterization of RRAM Cell

1.1.1.1. DC Resistive Switching Characteristic of RRAM Cell

In Fig. 4.3, the RRAM device shows typical unipolar switching $I-V$ characteristics using DC sweep of both HfO_x/AlO_y and HfO_x based RRAMs. In the *SET* process, the current compliance (I_{comp}) is set to 10^{-4} A to protect the device from breakdown. Similar to the HfO_x based RRAMs device, forming process is initiated at 3V to induce the resistive switching in HfO_x/AlO_y based device. Compared to the HfO_x based device, the device with AlO_y incorporation has reduced *SET* voltage (from ~2.3V to ~1.2V) and *RESET* voltage (from ~1.6V to 0.4V), showing great promises for low-voltage application. No degradation in $I-V$ is seen after 10^6 AC switching cycles for HfO_x/AlO_y based memory.

ON/OFF resistance ratio of the RRAM is increased by ~ 2 orders of magnitude (up to 10^5) after incorporating AlO_y into the device (*LRS* current increases by ~10x, and *HRS* current reduces by ~10x). The HfO_x/AlO_y bi-layer devices get a higher *ON/OFF* resistance ratio and lower *SET/RESET* voltage than HfO_x single-layer devices, which are attributed by the incorporation of AlO_y into HfO_x. It has been demonstrated that the performance of HfO_x-based RRAM devices can be greatly improved by intentionally introducing AlO_y in the HfO_x films. AlO_y can also be stacked with other RRAM materials to improve the uniformity of the device characteristics. Chen *et al.*[81] used an AlO_y buffer layer underneath the HfO_x resistive layer to enhance the read disturb immunity. Yu *et al.*[82] utilized a bi-layer HfO_x/AlO_y cell structure and obtained better switching uniformity than the pure HfO_x layer cells.

Figure 4.3 Typical I - V curve of positive dc sweep of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ and $\text{Ni}/\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ RRAM devices.

4.4.2.1. AC Conductance Measurement of RRAM Cell in *LRS* and *HRS*

To understand *LRS* current increase after AlO_y incorporation, AC measurement at different temperature is carried out for *LRS*, shown in Fig. 4.4. *LRS* current of HfO_x based device is seen to obey the barrier-correlated hopping mechanism [70], while metallic conduction behavior is observed in *LRS* for $\text{HfO}_x/\text{AlO}_y$ based device. The conduction mechanism transition from hopping to metallic can be explained by the Al doping effect in HfO_x [83], which would

significantly increase the density of oxygen vacancies (leading to electron state overlap) in the dielectric.

Figure 4.4 Frequency dependence of ac conductance on LRS of both HfO_x and $\text{HfO}_x/\text{AlO}_y$ based RRAM devices.

4.4.2.2. Temperature Dependence of HRS

The reduction of the HRS current after AlO_y incorporation can be understood from the measurement of activation energy (E_A) of the charge transport for both devices, as in Fig. 4.5. E_A is estimated to be $\sim 0.78\text{eV}$ for $\text{HfO}_x/\text{AlO}_y$ based device, which is much higher than HfO_x based device ($\sim 0.34\text{eV}$). The E_A increase is attributed to the larger energy gap (thus larger barrier for electron hopping) after Al doping into HfO_x [84]. Yu et al. [85] has studied the gap energy for dielectrics (the oxides) by XPS. From the results, a linear change of energy gap value with x in

the $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ system is observed. Accordingly, The electrical properties of $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ gate dielectrics should be able to be tuned by simply changing the HfO_2 mole fraction while keeping the stoichiometry of the materials. Similarly, Zhang et al. [37] has investigated the doping effects in HfO_2 dielectric based on the first principles calculations. Based on his simulation results, the trap level is located near the mid-gap in the HfO_x . In contrast to this, the deep trap level is shifted upward to a shallow level in the Al-doped HfO_x . Since deep level states more easily trap electrons or holes than shallow level, Al-doping HfO_x and HfO_x can cause different reliability characteristics. This might be caused by the barrier modulation by the metallic Hf and Al on the thermally activated hopping process of electrons. As a result, the ON/OFF ratio was improved by the lowering of HRS current, which might relate to the inter-diffusion of Al and Hf atoms and the change of activation energy of transport.

Figure 4.5 Temperature dependence of the current for HRS of Ni/ $\text{HfO}_x/\text{p}^+\text{-Si}$ and Ni/ $\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ RRAM devices. The applied voltage is 0.2 V.

4.4.2.3. Cycle-to-Cycle and Device-to-Device Resistive Switching Performance

Single device resistive switching of 200 DC device cycles of bi-layer and single layer cell is shown Fig. 4.6 (a). Very tight *HRS/LRS* distribution is achieved in $\text{HfO}_x/\text{AlO}_y$ bi-layer device, compared to quite large variation in HfO_x single layer device. Both *SET* and *RESET* voltages are also smaller and more uniformity bilayer device than single layer device (Fig. 4.6(b)). It suggests that the diffusion of Al atoms stabilize the conductive filaments and the EELS analysis verified such inter-diffusion, thus it is expected that $\text{HfO}_x/\text{AlO}_y$ bi-layer samples may have a better uniformity and lower set/reset voltage.

Figure 4.6 (a) Resistance distribution for 200 dc sweep cycles of HfO_x and $\text{HfO}_x/\text{AlO}_y$ based single device. (b) Set voltage and reset voltage comparison for 200 dc sweep cycles of HfO_x and $\text{HfO}_x/\text{AlO}_y$ based RRAM cells.

To study the device-to-device variation of two structures, resistance and V_{set}/V_{reset} distribution of ten devices (100 DC cycles measured for each device) are shown in Fig. 4.7 (a) and Fig. 4.7 (b), respectively. Similar to the case in a single device (cycle-to-cycle variation), the HRS/LRS resistance and V_{set}/V_{reset} dispersion are greatly improved for the bi-layer structure than the single-layer one. The results further confirm the effect of Al-doping HfO_x on the uniformity of operation switching parameters in the $\text{HfO}_x/\text{AlO}_y$ bi-layer devices[83].

Figure 4.7 (a) Device-to-device resistance distribution in $\text{AlO}_y/\text{HfO}_x$ based RRAM cells (ten devices each and 100 DC cycles of each device). (b) Device-to-device $V_{\text{set}}/V_{\text{reset}}$ distribution in $\text{AlO}_y/\text{HfO}_x$ -based RRAM cells (10 devices each and 100 DC cycles of each device).

The data retention measurement of the memory cell of both HfO_x and $\text{HfO}_x/\text{AlO}_y$ based RRAM at a high temperature of 120°C is shown in Fig. 4.8, without observable degradation.

Figure 4.8 Endurance characteristic of $\text{AlO}_y/\text{HfO}_x$ based RRAM cell under pulse switching.

The switching endurance of the $\text{HfO}_x/\text{AlO}_y$ based RRAM device is examined with pulse width of 10ns for set pulse and 30ns for reset pulse in Fig. 4.9 (a). The device *HRS/LRS* resistance can be well retained after more than 10^6 switching cycles. Note that the set and reset voltages under pulse measurement are larger than those obtained by DC sweep mode, which is believed to be due to the parasitic RC-delay during the measurement [86]. Fig.4.9 (b) illustrates the high temperature operating stability of the $\text{HfO}_x/\text{AlO}_y$ based RRAM. At 200°C , the device can well maintain its unipolar switching behavior after 100 DC sweeps without undergoing threshold resistive switching.

Figure 4.9 (a) Endurance characteristic of $\text{AlO}_y/\text{HfO}_x$ based RRAM cell under pulse switching. (b) Typical I - V curve of DC sweep for $\text{AlO}_y/\text{HfO}_x$ based RRAM at 200°C (repetition after 100 sweeps).

4.5. Switching Mechanism of RRAM Cell

To understand possible switching mechanism of the demonstrated devices, several control samples using different metal as top electrode. The mobile ion source (e.g. Cu or Ag) were used as electrode rather than Ni to fabricate the $\text{HfO}_x/\text{AlO}_y$ RRAM. Those devices can show unipolar switching, but with very low endurance (< 15 cycles), and low on/off ratio (< 50). It indicates that the switching behavior of $\text{Ni}/\text{HfO}_x/\text{AlO}_y$ RRAM may not be due to the Ni ions diffusion into dielectric under electric field.

Gao *et al.* [87] has proposed a microscopic mechanism of unipolar switching based on the decomposition-depletion-recombination effects. Based on the proposed model, for unipolar *RESET* process, the rupture of filament at NiO_x interface is dominated by electric field controlled electron depletion in oxygen vacancy (producing Vo^{2+}) (P1) and Joule heating controlled thermal releasing of O^{2-} (P2). Therefore, *RESET* current is a function of *SET* current for unipolar switching. Current sweep mode is employed to analyze the relationship between *SET* and *RESET* current in Fig. 4.10. Two different regions can be observed which are dominated by the respective occurring sequence of P1 and P2 at different *LRS*. In the proposed device, the compliance current is set in “flat” region as shown in Fig. 4.10. In this region, the *RESET* current is reduced with increasing temperature, which is due to Joule heating effect dominated. As a result, the rupture of conductive filaments is associated with the local Joule-heat-induced redox of NiO_x and the interface with $\text{HfO}_x/\text{AlO}_y$ dielectric layer, which is similar with proposed switching mechanism in Chapter 3 for single layer HfO_x -based RRAM.

Figure 4.10 The dependence of set and reset current under *SET* current sweep of $\text{HfO}_x/\text{AlO}_y$ based RRAM.

4.6. Conclusion

In summary, a high-performance, high-yield unipolar RRAM based on $\text{Ni}/\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ structure is reported, which is compatible with the Si-diode as the selector for 3D cross-bar implementation. By using $\text{HfO}_x/\text{AlO}_y$ bi-layer instead of HfO_x one-layer, the demonstrated memory device possesses superior. In addition, by using highly doped p-type silicon as bottom electrode, the hafnium oxide-base memory integrated with Si-diode is promising for future highly-density-crossbar nonvolatile memory. Table 1 illustrates the $\text{Ni}/\text{HfO}_x/\text{AlO}_y/\text{p}^+\text{-Si}$ RRAM achieves superior performance as compared to the recently reported unipolar RRAM devices employing various switching materials.

Table 4.1 Comparison of device performance for various unipolar RRAM devices.

	AlO _y /HfO _x This work	HfO _x This work	TaO _x [88]	Ti:NiO _x [89]	WO _x [90]	SiO _x [91]	ZrO ₂ [92]	TiO ₂ [93]	ZnO [94]
T/B electrode	Ni/p-Si	Ni/p-Si	Cu,Al/Pt	Pt/Pt	TiN/W	Cu/W	Pt/p ⁺ -Si	Pt/Pt	Pt/Pt
On/Off	~10 ⁵	~10 ³	~10 ⁴	~10 ²	~10 ⁴	~10 ⁵	~10 ¹	~10 ²	~10 ³
Endurance	AC>10 ⁶	AC >10 ⁵	DC >10 ²	AC>10 ²	AC: 10 ⁷	-----	DC >80	-----	DC >10 ²
V_{reset}/V_{set}	0.5/1.3V	1.5/2.1V	0.7/2.3V	0.8/1.8V	1.5/4V	1.5/5V	1.1/1.6 V	0.9/2.5 V	-1/-2V
On/Off speed	10/30ns	50/50ns	20/80ns	50/50ns	50/300ns	-----	100/100 ns	-----	----- --
Retention	>10 ⁵ s @ 120° C	>10 ⁵ s @ 120° C	10 ⁴ s @ 85° C	10 ³ hours @ 100° C	10 ⁴ s @ 25° C	10 ⁴ s @ 100° C	10 ³ s @ 25° C	-----	----- -----

Chapter 5 Self-Rectifying Unipolar HfO_x Based RRAM Built by Fab-Available Materials

5.1. Introduction

In this chapter, $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM structure with self-rectifying behavior is proposed. The effect of highly-doped $\text{n}^+/\text{p}^+\text{-Si}$ as bottom electrode on unipolar RRAM with Ni -electrode/ HfO_x structure is investigated in detail. With heavily doped $\text{p}^+\text{-Si}$ as bottom electrode, RRAM devices illustrate coexistence of bipolar and unipolar resistive switching. Meanwhile, by substituting by heavily doped $\text{n}^+\text{-Si}$, the switching behavior change to self-rectifying unipolar device. The asymmetry and rectifying reproducible behavior in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ structure is resulted from the Schottky barrier of defect state level in $\text{SiO}_x/\text{HfO}_x$ junction and $\text{n}^+\text{-Si}$ substrate, but this is not seen for the $\text{p}^+\text{-Si}$ electrode case. With rectifying characteristics and high forward current density observed in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ device, the sneak current path in conventional cross-bar architecture was effectively reduced. The proposed structure is a promising candidate for future cross-bar type RRAM applications.

5.2. Experimental Details

RRAM devices using heavily doped $\text{p}^+\text{-Si}$ and $\text{n}^+\text{-Si}$ as bottom electrode are fabricated in same condition, as shown in Fig. 5.1 (a) and Fig. 5.1 (b) respectively. The brief fabrication process flow is summarized in Fig. 5.1 (c). After the RCA cleaning and the dilute HF clean ($\text{HF}+\text{H}_2\text{O}_2$) for 2 minutes, HfO_x films with a thickness of ~ 4 nm were deposited using ALD at

250°C on 4-inch highly doped n^+ -Si ($N_D \sim 10^{18} \text{ cm}^{-3}$) and p^+ -Si ($N_A \sim 10^{18} \text{ cm}^{-3}$) substrates, respectively. Hafnium tetrachloride (HfCl_4) and water (H_2O) were used as reactants for HfO_x deposition. Consequently, a 50 nm Ni/50 nm TiN top electrode was deposited by sputtering at room temperature, followed by device patterning to complete final devices with areas ranging from 50×50 to $500 \times 500 \mu\text{m}^2$. The elements of the stacked layers of the devices were investigated in our previous chapters [95]. The current-voltage ($I - V$) characteristics of the fabricated samples with different types of bottom electrodes are measured by Keithley 4200 semiconductor characterization system under air condition.

Figure 5.1 (a) Schematic of fabricated $\text{TiN}/\text{Ni}/\text{HfO}_x/n^+$ -Si memory device. (b) Schematic of fabricated $\text{TiN}/\text{Ni}/\text{HfO}_x/p^+$ -Si memory device. (c) Brief fabrication process flow of the RRAM devices.

5.3. Results and Discussion

5.3.1. DC Resistive Switching Characteristics of Ni/HfO_x/n⁺-Si RRAM Cell

Fig. 5.2 illustrates unipolar well-behaved RS characteristic of Ni/HfO_x/n⁺-Si device after 1st and 200st cycles. Based on our previous chapters [80], the unipolar RS behaviors are related to NiO_x-involvement at the interface. In addition, Wang *et al.* [96] have carried out recently chemical analysis for Ni/HfO_x-based RRAM structure using EDX after *RESET* process. They found out that there is no clear indication of Ni diffusion through the HfO_x layer. As a result, the switching behavior may not be induced by Ni diffusion in our Ni/HfO_x/Si structure. The conductive filaments' formation and rupture are determined by reduction and oxidation reactions through the interfacial layer. *SET* process is the formation of filaments and *RESET* process is the annihilation of filaments in NiO_x interfacial between Ni and HfO_x layer. The Joule-heating-induced rupture plays a key role for melting filaments in unipolar *RESET* process.

Figure 5.2 Typical I - V curve of DC sweeps of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$. Rectification in LRS , the crosstalk phenomenon can be suppressed without connecting a diode.

At 0.5V reading voltage, a large memory window of more than 10^3 is achieved, which can be easily integrated into cross-bar structure with possible higher density. It is observed that the device exhibits a pronounced rectifying effect at LRS . When the memory is set to LRS , the current in positive direction of LRS is $>10^3$ larger than the negative current value, for a given 1V reading voltage. Fig.5.3 also demonstrates the excellent self-rectifying characteristics at various working temperature (50-150°C). It is worth mentioning that the HRS current does not change when changing the polarity of applied voltage for this device.

Figure 5.3 $I - V$ characteristics and inserted circuit diagram of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ cell in LRS under various temperatures. Rectifying ratio @ 1V is $> 10^3$.

The almost consistent rectifying behaviors with high rectification ratio and forward driving current are observed in the devices with different areas. With such a forward/reverse current ratio at LRS , the cross-talk effect in the crossbar structure arrays can be restrained and misreading can thus be avoided. This kind of self-rectifying resistive memory shows a potential to be used in crossbar structure arrays. Since there is no need to add any extra rectifying diodes to proposed memory cell, the negative impact from diodes on device performance can be omitted. An endurance test has been carried out on the resistive memory sample. After 200 cycles of set and reset operation by dc sweeping, the forward/reverse current ratio keeps almost unchanged (Fig. 5.2). The uniformity of the resistive switching of our proposed device can be enhanced by using a thinner Ni top electrode, as evidenced by the comparison of R_{HRS}/R_{LRS}

distribution in Fig. 5.4 (a) and Fig. 5.4 (b). By using thin Ni layer deposition, a well-controlled interfacial layer is formed which is very helpful for the switching uniformity improvement.

Figure 5.4 Resistance distribution of device-to-device variation in (a) thin and (b) thick Ni cells in 100 cycles of 10 devices each.

5.3.2. Temperature Dependence of Reverse Current of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM Cell in *LRS*

To understand self-rectifying effect of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ in *LRS*, the reverse current transport mechanism is investigated. Fig. 5.5 shows the reverse current can be fitted well with the Schottky current transport model. The effective Schottky barrier height at the given voltage applied (0.5 V) is calculated as $\sim 0.534\text{eV}$ by plotting $\ln(\frac{I}{T^2})$ vs. $\frac{1}{kT}$, as shown in Fig. 5.6. The

extracted Schottky barrier height does not change with different device areas (Fig. 5.6), which is essential for the device scaling. It is worth noting that the forward current seen to obey the barrier-correlated hopping mechanism has been discussed in previously report [80]. Owing to the Schottky barrier in reverse current region, rectifying behavior is observed in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM cell.

Figure 5.5 Reverse current in *LRS* of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM cell. Current curve can be characterized by the Schottky emission model.

Figure 5.6 Temperature dependence of reverse current in *LRS* of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ at -0.5 V for various device sizes. Schottky barrier height is independent with device size.

5.3.3. NxN Cross-bar Array Based $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM Cell.

The cross-bar memory array with NxN RRAM cells is proposed estimate total number of $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ memory cells in cross-bar array structure, as shown in Fig. 5.7 (a). In order to estimate readout margin, we assumed the ideal interconnect, same current level of all RRAM devices, and no variations in cross-point arrays. The cross-bar arrays of NxM size can be

simplified to 2x2 arrays as shown in inset of Fig. 5.7 (b). The value of equivalent resistances of 2x2 arrays is calculated by

$$\frac{1}{R_1} = \sum_{j=2}^n \frac{1}{R(1, j) @ V_{read1}} \quad (1)$$

$$\frac{1}{R_2} = \sum_{i=2}^n \frac{1}{R(i, 1) @ V_{read1}} \quad (2)$$

$$\frac{1}{R_3} = \sum_{i=2}^n \sum_{j=2}^n \frac{1}{R(i, j) @ V_{read2}} \quad (3)$$

where i is location of the bit-line and j is location of the word-line. $R(i, 1)$, $R(1, j)$ and $R(i, 1)$ are defined as resistances in Region 1, Region 2, Region 3 of Figure 5.7(a), respectively. R_1 , R_2 and R_3 are value of equivalent resistances of 2x2 arrays as shown in inset of Fig. 5.7. (b). Owing to self-rectifying behavior of *LRS*, the *LRS* current is suppressed in negative voltage region as shown in Fig. 5.7. (b). As a result, the value of R_3 is much larger than R_1 and R_2 , leads to the leakage current of un-selected cell will be suppressed. When placed in an array, the cross-interference can be eliminated. Using device parameters which can be extracted from $I-V$ results, the max N can be extracted when the anti-crosstalk ratio approaches to 1. The maximum word-line $N > 2^6$ is demonstrated in Fig. 5.7 (c) at 0.5V reading voltage which is satisfied to high density crossbar- arrays without using selection device.

Figure 5.7 (a) Schematic diagram of $N \times M$ cross-bar array structure. (b) Typical self-rectifying unipolar resistive switching device, inset shows simplified 2×2 array. (c) Extracted readout margin versus the WL number N in $N \times N$ RRAM cells. The maximum number $N > 2^6$ can be realized using the self-rectifying RRAM cells.

5.3.4. DC Resistive Switching Characteristics of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ RRAM Cell

On the other hand, co-existence of both unipolar and bipolar RS mode is observed for $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ device, as shown in Fig. 5.8 and Fig. 5.9 (a) respectively. The symmetric current of LRS is thus observed in $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ RRAM device (Fig. 5.9 (b)) under different temperature measurements. By using $\text{p}^+\text{-Si}$ as a bottom electrode, the rectifying effect is not seen.

Figure 5.8 Typical $I-V$ curve of DC sweep of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ under the unipolar resistive switching mode.

Figure 5.9 (a) Typical $I-V$ curve of D.C. sweep of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ under the bi-polar resistive switching mode. (b) $I-V$ characteristics and inserted circuit diagram of $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ cell in LRS.

Schematic of switching mechanisms is plotted to explain the difference of 2 RS modes as shown in Fig. 5.10. The *SET* process for unipolar RS mode is similar to the bipolar RS mode. However, *RESET* processes for unipolar and bipolar RS modes observed in p⁺-Si/HfO_x/Ni devices may induced by different switching mechanisms. In the *SET* process, O²⁻ ions is created from oxygen vacancies in the HfO_x resistive switching layers and drifted to the Ni electrode under applied electric-field. The conducting filament is reconnected at resistive switching layer near Ni electrode after *SET* process. Fig 5.9 (a) shows gradual transition of reset process which normally is illustrated in reported HfO_x-based bipolar RRAM devices [95]. This gradual reset switching of the Ni/HfO_x/p⁺-Si device is associated to gradual filament annihilation caused by oxygen ion drifts [95] (Fig. 5.10 (a)). The O²⁻ stored in Ni TE can be released by the *RESET* electric-field to recombine with the charged effect oxygen vacancy (V_o^{••}) near the interfacial layer. Therefore, bipolar mode attributes the set reset switching operations to the voltage-driven attraction and repelling of oxygen-vacancy defects.

Moreover, Ni/HfO_x/p⁺-Si device under unipolar RS mode illustrates a sharp-transition reset which is different with gradual reset transition in bipolar RS (Fig. 5.8). Regarding the reset switching process, it is probably related to the local Joule heat-induced redox inside NiO_x interfacial layer, thus explain sharp drop leakage current in RRAM device [80] (Fig. 5.10 (b)). The Ni/HfO_x/p⁺-Si structure shows reproducible and stable the coexistence of both modes.

Figure 5.10 Schematic diagram of the physical switching mechanism to clarify the coexisted (a) bipolar and (b) unipolar RS behaviors in $\text{p}^+\text{-Si}/\text{HfO}_x/\text{Ni}$. The electric-field induced oxygen ions drift and Joule-heating induced oxygen ions thermal-decomposition govern the bipolar and unipolar switching behaviors respectively.

5.3.5. Schottky Barrier Model of Self-rectifying Effect in $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ RRAM Cell

Based on the aforementioned results, Fig. 5.11 proposes a model to qualitatively clarify the self-rectifying effect in *LRS* for $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$ device.

Figure 5.11 Reverse current transport diagram in (a) $\text{Ni}/\text{HfO}_x/\text{p}^+\text{-Si}$ and (b) $\text{Ni}/\text{HfO}_x/\text{n}^+\text{-Si}$.

During forming process, defects or traps (oxygen vacancy (V_o) related) can be introduced inside the HfO_x/SiO_x dielectrics whose energy level might align around the mid-gap of Si substrate (based on the Schottky barrier height data in Fig. 5.6) [97]. During reverse bias operation, injection of electrons from the defect states in HfO_x/SiO_x into Si electrode is required. For p⁺-Si substrate, electrons inject through this localized conducting filaments connecting the top electrode and the semiconductor. These electrons directly inject into the valence band (as in an Ohmic contact), therefore the rectifying behavior has not been observed (Fig. 5.11 (a)) [87]. For n⁺-Si substrate, the current transport shows diode-like behavior in *LRS*. Owing to the Schottky-like barrier in Si/HfO_x interface which attributed to the offset between Si Fermi level and energy level of oxygen vacancies in HfO_x, the current transport would be suppressed, as illustrated in Fig. 5.11 (b). The diode-like behavior is also studied by E. Yalon *et al.* [98] for the post-breakdown current in metal-oxide-semiconductor structures. Further, it is worth noting that the current transport in *HRS* is dominated by hopping transport in HfO_x bulk [95], and this Schottky barrier would not affect the *HRS* current transport.

5.4. Conclusion

In this chapter, the effect of highly-doped n⁺-/p⁺-Si as bottom electrode on unipolar RRAM with Ni-electrode /HfO_x structure is investigated. With heavily doped p⁺-Si as bottom electrode, RRAM devices illustrate coexistence of bipolar and unipolar resistive switching. Meanwhile, by substituting by heavily doped n⁺-Si, the switching behavior change to self-rectifying unipolar device. The asymmetry and rectifying reproducible behavior in Ni/HfO_x/n⁺-Si device is resulted from the Schottky barrier of defect state level in SiO_x/HfO_x junction and n⁺-Si substrate, but this is not seen for the p⁺-Si electrode case. With rectifying characteristics and high

forward current density observed in Ni/HfO_x/n⁺-Si device, the sneak current path in conventional cross-bar architecture was effectively eliminated. We believe that the proposed structure is a promising candidate for future cross-bar type RRAM applications.

Chapter 6 A Self-Rectifying HfO_x-Based Unipolar RRAM with NiSi Electrode

6.1. Introduction

In this chapter, we report the self-rectifying unipolar HfO_x based RRAM fabricated with TiN top electrode and NiSi bottom electrode (both are fab-available materials), which is compatible with NiSi source/drain in advance CMOS technology process. The performance of this memory cell, switching mechanism and possible passive cross bar structure are investigated.

6.2. Experiment Details

The brief fabrication process flow and the schematic of fabricated devices are summarized in Fig. 6.1 (a) and Fig. 6.1 (b). First, 4-inch highly doped n+ Si (ND ~ 10¹⁸ cm⁻³) dipped into diluted hydro-fluoride acid solution (1 HF: 20 H₂O) for two minutes to remove native oxide and other contaminants. A layer of 20-nm-thick Ni film were sputter-deposited using a pure Ni target at room temperature, followed by rapid thermal processing (RTP) at 500 °C for 60 seconds to achieve NiSi layer. Consequently, HfO_x film with a thickness of ~ 4 nm was deposited using atomic layer deposition (ALD) at 250°C on NiSi substrate. Finally, a 50-nm TiN

top electrode is deposited with reactive sputtering and patterned with lithography, dry etch is done to pattern RRAM devices with areas ranging from 50×50 to $500 \times 500 \mu\text{m}^2$.

Figure 6.1 (a) Brief fabrication process flow of the RRAM devices. (b) A schematic of fabricated TiN/Ni/HfO_x/p⁺-Si memory device.

The microstructure of the stacked layers of the devices was investigated by high-resolution cross-sectional transmission electron microscopy (HR-XTEM). Chemical composition of NiSi layer was analyzed with X-ray photoelectron spectroscopy (XPS). The electrical measurements were performed using a Keithley 4200-SCS semiconductor parameter analyzer.

6.3. Results and Discussion

6.3.1. Physical Analysis of RRAM Cells

High resolution transmission electron microscope (HRTEM) is used to check the morphology of the prepared samples. In Fig. 6.2, HTEM image of the fabricated NiSi/ HfO_x /TiN capacitor reveals that the HfO_x layer is amorphous and has a thickness of ~ 4.1 nm. XPS study on chemical composition of NiSi after annealing process confirms the formation of NiSi (data not shown here).

Figure 6.2 Cross-sectional TEM image of the TiN/ HfO_x /NiSi memory cell.

6.3.2. Electrical Characterization of RRAM Cell

The RRAM device shows well-behaved unipolar resistive switching $I - V$ characteristics using positive DC sweep as in Fig. 6.3. In *SET* process, a positive voltage sweep (0- 2.8V)

triggers the conduction abruptly, and the resistance switches from high resistance state (*HRS*) to low resistance state (*LRS*). A current compliance of $100\mu\text{A}$ is applied at the same time to protect RRAM devices from permanent breakdown. Afterwards, another voltage sweep ($0\text{V} - 1.6\text{V}$) causes the abrupt decrease of current and the resistance switches back to *HRS*. From Fig. 6.3, it is also observed that the devices show a pronounced rectifying effect at *LRS*. When the memory is set to *LRS*, the current in positive direction of *LRS* is $>10^3$ larger than the negative current value, for a given 0.5V reading voltage.

Figure 6.3 Typical I –V curve of dc sweep of TiN/HfO_x/NiSi.

Based on such excellent rectifying properties with high forward/reverse current ratio, the cross-talk effect in crossbar structure arrays can be eliminated and misreading errors can be avoided. It is worth mentioning that the *HRS* current does not change when changing the polarity of applied voltage for this device. The possible mechanism of self-rectifying effect is described

as following. During set process, oxygen vacancies ($V_o^{\bullet\bullet}$) can be created inside the HfO_x dielectric films. These defects may introduce energy level which aligns with the mid-gap of NiSi substrate. During reverse bias operation, injection of electrons from the defect states in HfO_x into NiSi electrode is required. Owing to the Schottky barrier at the NiSi bottom electrode and HfO_x junction, the current transport would be suppressed. The effective Schottky barrier height of NiSi/HfO_x at the given voltage (0.5V) can be calculated as ~0.51eV. However, in forward current region, LRS current of TiN/HfO_x/NiSi is of Ohmic nature due to the injection of electron from the bottom electrode into the defect states. As a consequence, self-rectifying characteristic is observed in *LRS* of TiN/HfO_x/NiSi device.

6.3.3. Resistive Switching Performance of RRAM Cell

Resistance distribution and rectify ratio distribution of 5 random devices (100 DC cycles measured for each device) is plotted in Fig. 6.4 (a) and Fig. 6.4 (b) respectively. Good *HRS/LRS* distribution is achieved and the resistance ratio is larger than 2 orders of magnitude. Device-to-device distributions of rectify ratio also can be well maintained in all devices.

Figure 6.4 (a) Resistance distribution of device-to-device variation in NiSi/HfO_x/TiN cells in 100 cycles of each of the five devices. (b) Rectification ratio distribution of device-to-device variation in TiN/HfO_x/NiSi cells in 100 cycles of each of the five devices.

The retention measurement of the memory cell at a high temperature of 125°C is shown in Fig. 6.5. No observable degradation is seen, with a lifetime of 10 years can be expected.

Figure 6.5 Retention characteristics of $\text{TiN}/\text{HfO}_x/\text{NiSi}$ RRAM at 125°C .

6.3.4. NxN Cross-bar Array based Fabricated RRAM Cell

The passive cross-bar memory NxN array using $\text{TiN}/\text{HfO}_x/\text{NiSi}$ cells is proposed to study the impact of the parasitic sneak path on maximum number of resistive switching cells (Fig. 6.6 (a)). In order to calculate readout margin, one bit-line pull-up scheme is implemented in which only one bit line is pulled up, and all other bit lines are floating when each word line is selected [99]. Using this operating technique, the power consumed in the crossbar can be reduced significantly. The worst case behavior is applied when reading the HRS cells, and resistance of sneak paths is as small as possible. Using the device parameters which are extracted from $I-V$

results, the max N can be extracted when the anti-crosstalk ratio approaches 1. The maximum word-line with different reading voltages is illustrated in Fig. 6.6 (b). A maximum $2^6 \times 2^6$ array size can be achieved at the 0.5 V reading voltage, which is the best reported one among all existing projections on the unipolar crossbar array based experimental results without using a selection device. The tradeoff between readout-ratio and maximum number of word lines is also illustrated in the inset of Fig. 6.6 (b).

Figure 6.6 (a) Schematic view of the crossbar memory array with N^2 RRAM cells. (b) Maximum N increased with read voltage. Inset indicates the readout ratio versus WL number N for different read voltages. The maximum N can be extracted when the anti-cross-talk ratio approaches one.

6.3.5. Switching Mechanism of $\text{TiN}/\text{HfO}_x/\text{NiSi}$ RRAM Cell

The switching mechanism of proposed device is believed to be related to thermal dissolution of conducting filaments stemming from Joule-heating effect [86, 100]. To elucidate the unipolar switching of device, the measured $I_{reset} - R_{LRS}$ and $V_{reset} - R_{LRS}$ curves is fitted in Fig 6.7 and Fig. 6.8 respectively. The V_{reset} exhibits $R_{LRS}^{1/4}$ relation in the R_{LRS} region as shown in Fig 6.7, while $R_{LRS}^{3/4}$ dependence on R_{LRS} is observed in Fig. 6.8. The similar results can also be found in other unipolar devices in the literatures [101, 102]. The aforementioned observations suggest the Joule heating effect dominates the reset process, which represents the thermal decomposition of O^{2-} (thermal dominated region) at compliance current (set to $100\mu\text{A}$).

Figure 6.7 Measured distribution of the $I_{reset} - R_{LRS}$ at $100\mu\text{A}$ compliance current in *SET* process.

Figure 6.8 Measured distribution of the $V_{\text{reset}} - R_{\text{LRS}}$ at $100\mu\text{A}$ compliance current in *SET* process.

6.4. Conclusion

In summary, a unipolar resistive switching RAM based on TiN/HfO_x/NiSi structure is demonstrated successfully. The reported RRAM is fabricated with CMOS technology friendly materials and process, exhibiting excellent self-rectifying behavior in LRS ($>10^3$ @1V), and well-behaved memory performance in term of on/off resistance ratio, retention, and read-out margin.

Chapter 7 A Self-rectifying AlO_y Based Bipolar RRAM with Sub-50 μA *SET/RESET* Current for Cross-bar Array Architecture

7.1. Introduction

Recently, the quest of self-rectifying resistive memory has been actively pursued for both bipolar and unipolar types. Owing to the rectification in *LRS*, the crosstalk phenomenon can be alleviated without serially connecting a selector. The memory cell can significantly reduce the complexity of fabrication, lower the reading voltage and improve misreading in matrix crossbar memory without extra selector device. So far, almost all self-rectifying RRAM devices are demonstrated with unipolar resistive switching (RS) characteristic. However, the RS performance of bipolar RRAM is generally much better than unipolar RRAM (Fig. 7.1).

Figure 7.1 Comparison of endurance and reset current in excellent unipolar and bipolar RRAM [36, 95, 103, 104].

Owning to superior RS characteristics, it is first time, self-rectifying bipolar RRAM cell is proposed to realize selector-free for 3D cross-bar integration. In this chapter, we report the self-rectifying bipolar based-Ni/AlO_y/n⁺-Si RRAM structure with 50 μ A *RESET/SET* current. The device exhibits well-behaved bipolar RS with self-rectifying characteristic in *LRS*. The performance of this memory cell, switching mechanism and possible passive cross bar structure are investigated

7.2. Experiment Details

The process flow and schematic diagram for the Ni/AlO_y based resistive memory with highly doped n⁺-Si substrate are shown in Fig. 7.2(a). After RCA cleaning, on the 4-inch highly doped n⁺-Si ($N_D \sim 10^{18} \text{cm}^{-3}$) substrate, AlO_y film with a thickness of ~ 4 nm was deposited using atomic layer deposition (ALD) at 250°C with Al(CH₃)₃ and H₂O precursors. Consequently, a 100 nm Ni top electrode was deposited by sputtering at room temperature, followed by device patterning to complete final devices with areas ranging from 50x50 to 500x500 μm^2 . The current-voltage characteristics of the fabricated samples are measured by Keithley 4200 semiconductor characterization system.

Figure 7.2 Process flow and schematic structure of the Ni/AlO_y/n⁺-Si RRAM device.

7.3. Results and Discussion

7.3.1. Physical Analysis of RRAM Cell

High resolution transmission electron microscope (HRTEM) is used to check the morphology of the prepared samples. In Fig. 7.3, HTEM image of the fabricated Ni/AlO_y/n⁺-Si capacitor reveals that the AlO_y layer is amorphous and has a thickness of ~4.5 nm. The interfacial layer SiO₂ between AlO_y and n⁺-Si is observed with ~1.5nm.

Figure 7.3 HTEM image of Ni/AlO_y/n⁺-Si RRAM cell, 4.5 nm amorphous AlO_y layer is observed.

7.3.2. Electrical Characteristics of RRAM Cell

7.3.2.1. DC Resistive Switching Behavior of RRAM cell

The coexistence of unipolar and bipolar RS characteristics is achievable for Ni/AlO_y/n⁺-Si RRAM device as shown in Fig. 7.4 (a) and Fig. 7.4 (b), respectively. For unipolar RS, a positive voltage sweep (0-3.3V) triggers the conduction abruptly, and the resistance switches from high resistance state (*HRS*) to low resistance state (*LRS*). Afterwards, another voltage

sweep (0-1.8V) causes the abrupt decrease of current and the resistance switches back to *HRS* (Fig. 7.4 (b)). The bipolar RS mode is enabled by applying negative DC voltage sweep (0-4.5V) for *SET* process as shown in Fig. 7.4 (b). The current compliance of 10 μ A is applied in *SET* process to protect RRAM devices from permanent breakdown for both 2 modes. To activate the device, a forming process is initiated with forming voltage of $\sim\pm 5$ V. The unipolar RS mode is operated under positive forming voltage and the bipolar RS mode is operated under negative forming voltage.

It is worth noting that the value of I_{reset} under bipolar RS mode is as low as 1–50 μ A, in contrast with typical reset currents under unipolar RS mode, in the range of 1–10mA. The presence of low I_{reset} and V_{reset} observed in bipolar RS mode is preferred for low power application. In addition, Fig. 7.4 (a) and Fig. 7.4 (b) also reveal that the device exhibits a pronounced rectifying effect in the *LRS*. When the RRAM cell is set to the *LRS*, the positive current value of *LRS* is >700 larger than the negative current value, for a given 0.2 V reading voltage. This phenomenon is found with excellent reproducibility and stability.

Figure 7.4 (a) Unipolar resistive switching behavior of Ni/ AlO_y /n⁺-Si RRAM device. (b) Bipolar resistive switching behavior of Ni/ AlO_y /n⁺-Si RRAM devices.

7.3.2.2. Temperature Dependence of RRAM Cell in LRS

The self-rectifying effect of $\text{Ni}/\text{AlO}_y/\text{n}^+\text{-Si}$ in LRS is observed with good stability at high temperature as well, shown in Fig. 7.5. Inset of Fig. 7.5 shows circuit diagram of fabricated RRAM device in LRS. The RRAM device exhibits diode-like structure and is stable at various temperatures.

Figure 7.5 $I-V$ curves of the LRS in linear scale of the $\text{Ni}/\text{AlO}_y/\text{n}^+\text{-Si}$ cell at different temperatures under bipolar RS mode.

In order to understand the origin of the rectifying hysteric behavior, we fabricated a control sample $\text{Ni}/\text{AlO}_y/\text{Pt}$ (details not shown here), which illustrated quasi-symmetrical $I-V$ curve, indicating the rectifying property is mainly resulted from the contact of AlO_y and $\text{n}^+\text{-Si}$.

The reverse current can be fitted well with the Schottky current transport model as shown in Fig. 7.6 (a) and Fig. 7.6 (b) respectively.

Figure 7.6 (a) Reverse current in LRS of Ni/AlO_y/n⁺-Si can be characterized by the Schottky emission model. (b) Temperature dependent current with Schottky conduction model fitting in LRS of Ni/AlO_y/n⁺-Si at -0.4 V.

The effective Schottky barrier height of n⁺-Si/AlO_x at the given voltage (0.4 V) can be extracted as ~ 0.31 eV. During the memory programming, defects or traps can be introduced inside the AlO_x dielectrics, whose energy level might form the Schottky barrier height with conduction band of n⁺-Si in LRS state. In the forward current region, the Shottky barrier is not observed owing to the injection of electrons from the bottom electrode into the defect states. It is worth noting that the extracted Schottky barrier height doesn't change with device areas, which is able to scale for high density application.

7.3.3. *RESET* Current Characteristic of RRAM Cell

In order to understand switching mechanism for both unipolar and bipolar mode, we plotted the cumulative probability plot of I_{reset} as shown in Fig.7.7. There is significant drop of the reset currents by 1–2 orders of magnitude for the bipolar RS mode compared to unipolar RS mode.

Figure 7.7 Cumulative plot of I_{reset} for unipolar and bipolar RS modes.

Two reset modes observed in n⁺-Si/AlO_x/Ni are believed to be induced by different switching mechanisms. For unipolar RS mode, the unipolar RS behaviors are related to NiO_x involvement at the interface as our previous reports [95, 105]. The conductive filaments' formation is determined by reduction and oxidation reactions through the interfacial layer for unipolar set process. The unipolar reset process possibly related to local Joule heating-induced annihilation of Ni conducting filaments at interfacial layer, which require high reset current in range of few mA. For bipolar process mode, the filament formation and annihilation is caused by electric-field-assisted migration of oxygen ions/vacancies at interfacial layer between AlO_x and Si substrate[106]. Due to reset process caused by different switching mechanism, unipolar RS mode illustrates a sharp-transition reset, which is different with gradual reset transition in bipolar RS.

Figure 7.8 Frequency dependence of A.C. conductance on *LRS* under unipolar and bipolar RS modes.

7.3.4. Resistive Switching Performance of RRAM Cell

To further study the device memory performance, resistance distribution and rectifying ratio distribution of devices (200 DC cycles measured for each device) is plotted in Fig.7.9. Good *HRS/LRS* distribution is achieved and the resistance ratios larger than three orders of magnitude. The distributions of rectify ratio also can be retained in all devices.

Figure 7.9 Cumulative probability plot of $I_{LRS-Forward}$, $I_{LRS-Reverse}$ and I_{HRS} under bipolar RS mode.

Retention time projected from the life time extracted from HRS at different temperature points is shown in Fig. 7.10 [11]. The projected retention time at room temperature is longer than 10⁷ s.

Figure 7.10 Retention time projected from the life time extracted from *HRS* at different temperature points.

7.3.5. NxN Cross-bar Array based Fabricated RRAM Cell

From the I–V characteristic of the self-rectifying bipolar device, the readout margins are investigated under the worst case condition. The cross-bar memory array with NxN RRAM cells is proposed in which Ni/AlO_x/n⁺-Si memory cell is integrated between word line and bit line without connecting a selector device. To estimate readout margins of cross-bar array, a worse case read scheme, so-called one bit-line pull-up scheme, is utilized [58]. We assumed that the

ideal interconnect, same current level of all RRAM devices, and no variations in cross-point arrays. Fig. 7.11 shows the simulated results of output signal swing as function of array size for read operation. At 10% of the readout margin, the self-rectifying RRAM cell illustrates an increase in the number of words compare with device without self-rectifying behavior. The nonlinearity I-V curve and self-rectifying characteristics significantly enhance number of cells [57, 107]. The maximum word-line $N > 2^5$ is demonstrated which is satisfied to crossbar- array blocks without using selection device. Vertical gate-all-around (GAA) Si nanowire MOSFET can be used realized multi-RRAM stacks. In this case, multiple-layers $\times 2^5$ array sizes could be built for this device, hence high density crossbar array are achieved.

Figure 7.11 Comparison of calculated readout margins in $N \times N$ cross-bar array integrating RRAM cells with and without self-rectifying behavior. The maximum number $N > 2^5$ can be realized using the self-rectifying RRAM cells.

7.4. Conclusion

In this chapter, a high reliable, self-rectifying bipolar resistive switching based on $\text{Ni}/\text{AlO}_x/\text{n}^+\text{Si}$ structure is demonstrated successfully. The demonstrated RRAM possesses excellent self-rectifying behavior in *LRS* ($>700@ 0.2 \text{ V}$), good memory performance, high potential for high density cross-point memory devices (number of word-line $>2^5$ for worst case condition) and low fabrication cost memory application. In earlier work, self-rectifying unipolar RRAM using $\text{Ni}/\text{HfO}_x/\text{n}^+\text{Si}$ cells to realize selector-free cross-bar array is reported. However, the resistive switching performances of bipolar RRAM devices are generally much better than unipolar RRAM owing to their different switching mechanisms. As a result, in this work, AlO_x based bipolar RRAM, with low power performance and well-behaved rectifying behavior is a promising candidate for future cross-bar RRAM application. It is the first time that the self-rectifying bipolar RRAM device is proposed for cross-bar, especially for AlO_x based materials

Chapter 8 Conclusion and Recommendations

8.1. Conclusion Remarks

In this thesis, the RRAM cells with Si substrate as bottom electrode were demonstrated. The proposed RRAM cells exhibits low programming currents and fast switching time, good and perfectible reality. More importantly, owing to its simple structure, 3D cross-bar architecture based on proposed RRAM device is extremely promising solution for high density storage

HfO_x-based materials have been employed as one of promising candidates for the gate insulator of CMOS MOSFETs. Interestingly, defect-rich HfO_x is also used as superior switching material due to its excellent performance switching behavior and reliable data retention. In the early stage of HfO_x memory exploration, the TiN/HfO_x/Pt MIM structure is usually employed to achieve the bipolar switching characteristics. However, the use of expensive metal electrode and noble metals increase the cost of fabrication process. In addition, only few options of diode selectors could be integrated with bipolar RRAM devices for high density cross-bar architecture. So far, although HfO_x is one of the most mature RRAM materials explored, the unipolar HfO_x-based RRAMs have not been investigated in detail. As a result, a high performance unipolar RRAM based-HfO_x dielectrics and Ni electrode on highly doped Si substrate has been reported in this study. In this structure, Ni acts as an oxygen reservoir. The unipolar RS can be explained by the rupture and formation of conductive filaments in association with the local Joule-heat-induced redox inside NiO_x interfacial layer, which is in analog to the unipolar RRAM device based on NiO_x dielectrics. By using Ni as top electrode, the proposed RRAMs have shown

Chapter 8 Conclusion and Recommendations

excellent performance of high resistance ratio, long retention time, fast switching time. More importantly, by using highly doped n-type silicon as bottom electrode the memory cell makes it feasible to employ a vertical Si- diode as a selector for crossbar structure integration, highly suitable for low-cost 3D integration. It is worth noting that the RRAM cells have illustrated one of the best RRAM devices in unipolar resistive switching field.

Poor uniformity of device characteristics is a major barrier to large-scale manufacturing of RRAM. Significant parameter fluctuations exist in terms of variations of the switching voltages as well as the resistances in HRS and LRS. The variations of the resistance switching include temporal fluctuations (cycle to cycle) and spatial fluctuations (device to device). AlO_y can be stacked with other RRAM materials to improve the uniformity of the device characteristics. Therefore, to further improve memory performance, incorporation AlO_y into HfO_x switching dielectrics is implemented. With doping effects, bi-layer $\text{HfO}_x/\text{AlO}_y$ cell structure has obtained better switching uniformity than the pure HfO_x - layer cell such as: 1) a high on/off resistance ratio of $\sim 10^5$; 2) excellent cycle-to-cycle and device-to-device uniformity of switching parameters (e.g. V_{set} , V_{reset} , and HRS/LRS currents); 3) $\sim 100\%$ device yield on a 4-inch wafer; 4) satisfactory pulse switching endurance ($> 10^6$ cycles); 5) high temperature retention ($> 10^5$ s @ 120 °C), and high temperature operating stability (> 200 °C) without threshold resistive switching; 6) a fast set/reset speed of $\sim 10/30$ ns.

RRAM based cross-point architecture has emerged as one of the promising successors to the current Flash technology. In order to avoid parasitic current paths and makes possible to addressing each single bit, a selecting component is required in series with RRAM cell which leads to the degradation of RRAM performance. Self-rectifying or nonlinearity $I - V$ characteristics are encouraged to increase the array size without a series selection part (e.g.

diode, transistor, etc.), so that higher integration density could be achieved for 3D vertical RRAM (VRRAM) stacking. A CMOS friendly and low fabrication cost Ni/HfO_x/n⁺Si RRAM device with forming-free unipolar switching, and self-selection for cross-point array structure has been explored. The asymmetry and rectifying reproducible behavior in Ni/HfO_x/n⁺Si device is resulted from the Schottky barrier of defect state level in SiO_x/HfO_x junction and n⁺Si substrate. With rectifying characteristics and high forward current density observed in Ni/HfO_x/n⁺Si device, the sneak current path in conventional cross-bar architecture was effectively eliminated. Due to NiSi has been used as the S/D contact for the mainstream CMOS technologies, therefore the HfO_x RRAM with NiSi as bottom electrode is fabricated for the integration concern.

The performance of bipolar RRAM (e.g. power, reliability etc) is generally demonstrated with better performance than unipolar one partially due to their inherent different switching mechanisms. Consequently, bipolar RRAM cross-bar gets more attractive attention because it's switching performance. It is the first time, CMOS friendly and low fabrication cost Ni/AlO_x/n⁺Si RRAM device with bipolar switching, low current, and self-selection for cross-point array structure has been demonstrated. VRRAM cross-point structure could be fabricated and operated correctly based on the proposed device.

8.2. Recommend for future works

Based on the previous results, the following future works are proposed:

Mechanism study: oxygen vacancies related conduction filament is commonly accepted for explanation of resistive switching behavior, however, the detailed mechanism is still under debate. More electrical and physical characterization is needed to understand the physics behind. By properly designing experimental work, the future work aims to understand: 1) the formation

Chapter 8 Conclusion and Recommendations

process and the characteristics of oxygen vacancies and their impact to carrier transport; 2) the impact of grain-boundaries or interface/surface of the oxide materials on the RRAM switching behaviours. This will help us to gain a deep understanding on the physical switching mechanisms of the oxide-based RRAM. To understand the switching properties of the proposed systems focusing on the physical mechanism through a set of structural and material analysis using tool such as XPS, Synchrotron-based techniques, BEEM/STM and TEM/EELS. Simulation model will be developed in parallel to verify the experimental results and predict the performance (set/reset, endurance, and retention) of combination of a few switching mechanisms.

Materials oriented solutions should be helpful to improve the device performance. Different doping atoms or multi-layers plan to be used for performance improvement with guidance from possible model prediction. In term of high-performance RRAM materials/device demonstration, utilize novel process will be utilized, such as small devices down to nanometer range and impurity doping before and after oxide deposition, to precisely manipulate the oxygen concentration in the metal oxide, and thus control the oxygen vacancies. In term of oxide switching behaviour modelling, it is new to model the combined effects from oxygen vacancies, Joule heating effect, ionic metal, and barrier height modulation by carrier injection. Small devices down to nanometer range should be prepared for electrical testing and more importantly, such small devices are useful for TEM characterization

Circuit integration with CMOS platform: integrate HfO_x -based RRAM cell with conventional CMOS circuit is also one of the goals of the future work. 3D cross-point RRAM bipolar and unipolar circuits will be designed and fabricated based on the proposed RRAM cell. This state-of-the-art circuit involves stacking MIM cells vertically. The potential advantages of this future work are the lower temperature processing and the simpler integration.

Chapter 8 Conclusion and Recommendations

Multi-level switching capability: Among all memory characteristics, the so-called multi-bit operation or multilevel cell (MLC), which exploits the layout area of a memory device to realize more than one bit of digital data per cell, is a desirable capability for high-density memory application. In the proposed device, the switching behavior only can exhibit 2 states (*HRS*, *LRS*). Therefore, multi-level storage capability of RRAM cell is expected in future work. For MLC operation, first, enough resistance windows between any two states and the uniformity of each resistance state are required. Second, the cycling endurance for each state is also an important criterion. Pulse programming schemes, materials oriented solutions is investigated to achieve multilevel characteristic of RRAM cell.

Due to the limitation of fabrication facilities in university, the future works have not been done in present work. The author will carry out future demonstration with facility support from microelectronic institute or Semiconductor companies to enhance the performance of proposed RRAM cell and understand more detail its switching mechanism.

Publications

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