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High Fidelity Closed-loop Pulse Width Modulated Class-D Amplifiers

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Abstract

High power efficiency, small size and reduced heat dissipation are highly desirable for both the low power and high power devices and the switched-mode Class-D amplifiers can readily satisfy these requirements. However, full adoption of the Class-D technology has been somewhat limited due to concerns such as signal distortion and poor power supply noise rejection. In a well-designed Class-D amplifier, the intrinsic distortions dominate the linearity performance when the input signal is large and at high frequency.

In the first part of this research, a systematic analysis on the intrinsic distortion of the closed-loop Class-D amplifier is investigated based on a large-signal time-domain modeling technique. The audible output components of closed-loop Class-D amplifiers with either AD- or BD-modulated 2nd-order designs are derived. The expressions are simple, accurate, and clearly reflect the relationship among the input signal, carrier frequency, and the distortion components.

In the second part of this research, a novel dual-feedforward carrier modulation topology is proposed for a 2nd-order Class-D amplifier. The proposed design can be considered a combination of two solutions/steps—a quadratic carrier generator plus two feed-forward signals. It is demonstrated that the THD of the Class-D amplifier using the proposed topology has improved by ten times over a wide range of input signal frequency and magnitude. The adopted low switching frequency also ensures a low switching loss and hence high power efficiency.

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Symbols and Abbreviation

PWM	Pulse Width Modulation
PDM	Pulse Density Modulation
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion plus Noise
IMD	Intermodulation Distortion
IMP	Intermodulation Product
PSRR	Power Supply Rejection Ratio
BTL	Bridge-Tied Load
ICMR	Input Common Mode Range
CMFB	Common Mode Feedback
CMRR	Common Mode Rejection Ratio
PCB	Printed Circuit Board
M	Modulation index of the input signal
f_{in}	Frequency of the input signal
f_c	Carrier switching frequency
$s(t)$	normalized input of the mathematical models
$g(t)$	normalized output of the mathematical models

Chapter 1 Introduction

1.1 Motivation

In recent years, manufactures of portable devices are faced with growing demands for integrating high-fidelity audio device into their produces, such as smart phone, notebook and multimedia player. This is driven by the consumers' expectation as well as the high-fidelity audio recording technology. On the other hand, power efficiency has become a major consideration for the state-of-the-art audio amplifier, for both low power and high power applications. For low power portable devices, the higher power efficiency of the audio amplifier is translated to longer battery life and smaller device size. For high power systems such as home stereos, the audio output specifications can commonly reach 6-channels $\times$ 50 W, with a 150-W bass channel. The deployment of traditional linear amplifier, such as the Class-AB type, is therefore not feasible, since power dissipation across the six channels implies thermal management challenge and the need for a large heat sink. The size, weight and cost of such surround sound amplifiers designed using Class-AB principles would also be prohibitive [1].

The amount of power dissipation strongly depends on the methodology engaged by the audio amplifier for biasing the power transistors. The power transistors in Class- A, B, and AB amplifiers are biased in linear mode, so that the process of generating output signal unavoidably causes non-zero I_{DS} and V_{DS} in at least one power transistor. The switching mode Class-D amplifier offers a

potential solution to this challenge, as its output stage switches between the positive and negative power supplies to produce a train of voltage pulses. This switching output waveform is benign for power dissipation because the power transistors dissipate little power when operating in the cut-off or linear region [2]. With continuous improvement on both the fabrication process and structure design, Class-D amplifier has become one of the most popular integrated amplifier topologies for battery operated portable devices as well as home audio-visual equipments. The lower power dissipation of Class-D amplifiers saves the cost and space of cooling apparatus, such as heat sinks or fans. Hence, an integrated Class-D amplifier may be able to use a smaller and cheaper package than is possible for the linear counterpart.

Although Class-D power amplifier can provide superior power efficiency performance, the major problems in the design of Class-D amplifier are the linearity and rejection of the noises injected from the power supply rails. In addition, the high frequency components of the modulated pulse signal cause electromagnetic interference to other devices and render it hard for integration on the printed circuit board (PCB). The need for LC filter also increases the cost and space occupied by the Class-D amplifier. Thus the future trend in Class-D amplifier design is to 1) minimize external components to reduce the size and cost; 2) improve the linearity to enhance sound fidelity; 3) increase the ability to suppress supply noise; and 4) reduce the electromagnetic interference. Last but not least, these goals must be achieved without significantly reducing the power efficiency of the Class-D amplifier.

1.2 Objective

The advanced fabrication technology of power MOSFETs and the enhanced linearity of the inductor and capacitor have contributed to the appreciable improvement in performance of the conventional Class-D amplifiers in the past decade. Thus, the intrinsic distortion caused by the feedback topology that applies to nonlinear modulation schemes becomes apparent. This project therefore aims to investigate the intrinsic distortion performance of closed-loop Class-D amplifiers through rigorous mathematical modeling techniques. The derived output expressions of the audible output signals shall provide an insight to the relationship between the circuit design parameters and the intrinsic distortions, and to better guide the circuit designers in their design process.

This project also targets to develop a new pulse width modulation topology that is able to suppress the intrinsic distortion. Meanwhile, the proposed topology aims for a high power supply rejection ratio (PSRR) that is comparable to its linear counterparts. The high PSRR performance shall facilitate the integration of the Class-D amplifier on printed circuit board or even on the same chip with other functional blocks. In addition, the high linearity of the proposed topology shall be achieved with a low switching frequency, which is quite important to avoid non-ideal effects in the output devices during the switching and minimize the switching loss. Recall that the low switching frequency is essential for achieving high power efficiency, especially for high-voltage applications.

1.3 Contributions

A number of contributions are made in this Ph.D. research journey, and they had been largely reported in four journal publications [3-6], as well as in a conference [7]. The main contributions of the work presented in thesis are summarized below:

- 1) An algorithm to visualize the phase and duty cycle errors (that are widely used to represent the intrinsic distortion of a closed-loop Class-D amplifier) has been developed. The time domain waveform of the error signals can help circuit designers to investigate the means to compensate the intrinsic harmonic distortion.
- 2) A systematic time-domain analysis on the intrinsic harmonic distortion performance of a closed-loop Class-D amplifier has been investigated. A series of simple and accurate expressions for the audible output signal have been derived. The time-domain analysis method has been verified to be suitable for both the AD modulation (with two-level PWM signal) and BD modulation (with three-level PWM signal). In addition, a stability criterion for preventing chaotic operation of a 2nd-order Class-D amplifier has been developed.
- 3) A dual-feedforward carrier modulation topology has been proposed for a 2nd-order Class-D amplifier. The proposed topology effectively attenuates the intrinsic harmonic distortion by around ten times and is suitable for implementation in both the AD and BD modulations.

1.4 Organization of the thesis

This thesis is organized as follows. Chapter 2 provides a brief introduction to the Class-D amplifier and a literature review on the various design and modeling techniques reported for the closed-loop Class-D amplifiers. Chapter 3 presents an insightful methodology to investigate the intrinsic harmonic distortion of the closed-loop Class-D amplifier by a simple means of comparing the output PWM signals between the closed-loop and open-loop Class-D amplifiers. Chapter 4 investigates the intrinsic distortion of the closed-loop AD-modulated Class-D amplifier based on a precise time-domain mathematical analysis. Chapter 5 extends the mathematical analysis to fully-differential BD-modulated Class-D amplifier. Chapter 6 provides an overview of the chaotic dynamic and bifurcation scenarios occurred on Class-D power amplifier when the loop filter parameters vary. A new stability criterion is introduced to replace the conservative linear system design guideline to maximize the suppression on power supply noise. Chapter 7 introduces a proposed dual-feedforward carrier modulated Class-D amplifier that can effectively suppress the intrinsic harmonic distortion. Chapter 8 reports the internship work of the candidate at the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), on designing a high-voltage driver for piezoelectric transducer. Lastly, the conclusion and future works are presented in Chapter 9.

Chapter 2 Literature Review

2.1 Basics of Class-D power amplifier

Class-D amplifier is a switch-mode power amplifier widely used in audio amplifier and in motor drivers. The primary motivation for using Class-D amplifier is its high power efficiency - typically higher than 80% - over a large modulation index range. This is because the output stage transistors operate in the triode and cut-off region thereby dissipating very little power [8]. The high efficiency allows very high output power with modest heat dissipation. Class-D amplifiers are becoming more prevalent in consumer electronic products, including micro-power hearing aids, low-power headphones, mid-power automotive audio and high-power public address sound systems, etc.

The linearity of Class-D amplifier has improved significantly in the last decade. However, when compared to the linear amplifiers, Class-D amplifiers incur a higher Total Harmonic Distortion (THD) at high frequency and high modulation index. Hence, most commercial Class-D products are characterized at 1 kHz and relatively low output power level, so that its performance is comparable to the linear amplifiers (around 0.02%).

2.1.1 Open-loop design

As the most basic circuit architecture, the block diagram of a generic open-loop Class-D amplifier was described in [9] and reproduced in Figure 2.1. The modulator converts an input audio signal, v_{in} , into a sequence of square pulses that drives the switching power stage. The switching power stage comprises

gate drivers and power MOSFETs. It boosts the modulated pulse signal to high power levels and ensures low output impedance, which are necessary to drive the heavy load. Next, the low-pass filter is used to suppress the energy at the switching frequency and to recover the low frequency input signal. The LC filter is engaged to avoid significant power dissipation in the filter element and to maintain the highest possible power efficiency for the amplifier system. Finally, a speaker is connected to the LC filter output, v_{out} .

Figure 2.1 Generic Open-loop Class-D Amplifier [9].

2.1.2 Closed-loop design

Due to component variations, power stage non-ideality, power supply noise and distorted carrier signal [10], the THD for an open-loop Class-D amplifier is typically of 0.1% or worse and the Power Supply Rejection Ratio (PSRR) is only 6 dB. Negative feedback is widely applied in Class-D amplifiers to improve their linearity. The block diagram of a conventional closed-loop Class-D amplifier is depicted in Figure 2.2. The modulator and a loop filter are embedded inside a negative feedback loop. The loop filter is essential to provide a high loop gain within the audio band, in which a high error suppression is desired [11], as well as to attenuate the high frequency carrier component of the feedback signal.

Figure 2.2 Block diagram of conventional Class-D amplifier with analog feedback.

Although the feedback signal shown in Figure 2.2 is derived from the output of the power stage, it can be extracted after the low-pass filter. The motivation for including a low-pass filter in the feedback loop is to suppress the distortion due to the speaker load variation (especially in the case of high-efficiency speakers [12]) and the LC filter's nonlinearities [13]. Recall that the frequency response of the output filter is dependent on the load, which varies with the output current. However, due to stability issue, it is not easy to take the feedback signals after the low-pass filter. To explain further, the commonly used 2nd-order LC filter introduces an additional 180° phase shift to the feedback signal and besides, the load impedance changes with the output power. Consequently, the loop filter structures used to compensate the phase shift are usually quite complicated and involve many passive components, which are hard to be integrated on chip. Alternatively, the feedback signals may be taken from the outputs of both the power stage and the low-pass filter, forming a dual-feedback loop (i.e., current internal loop plus voltage external loop) [12, 14].

2.1.3 Pulse width modulation versus pulse density modulation

The modulation methods applied by the modulator can be classified into two categories: Pulse Width Modulation (PWM) and Pulse Density Modulation

(PDM). As reflected in the name, pulse width modulation makes use of the width of the pulse signal to present the level of the input signal, whereas pulse density modulation use the number of identical pulses in a certain period to present the level of the input signal.

2.1.3.1 Pulse Width Modulation (PWM)

PWM is the most prevalent topology for open-loop Class-D amplifier design as it features the lower possible switching frequency and provides a higher power efficiency and stability at near 100% modulation [9]. Figure 2.3 illustrates the generation of a PWM waveform by simply comparing the input modulating signal, v_{in} , with a triangular wave carrier signal, v_c .

Figure 2.3 Pulse width modulator: (a) waveforms for input modulating signal, triangular carrier signal and PWM output signal; (b) typical circuit schematic for pulse width modulator.

It is well known that ideally the pulse width modulation process does not introduce harmonic distortions in audio band. This has been proven in [15] by the double Fourier analysis on the frequency components of the output signal of an open-loop Class-D amplifier, as described in the following equation:

$$\begin{aligned}
V_{PWM}(t) = & M \cos 2\pi f_{in}t + 4 \sum_{m=1}^{\infty} \frac{J_0\left(\frac{m\pi M}{2}\right)}{m\pi} \sin\left(\frac{m\pi}{2}\right) \cos(m2\pi f_c t) \\
& + 4 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \sin\left(\frac{(m+n)\pi}{2}\right) \cos 2\pi (mf_c + nf_{in})t
\end{aligned} \tag{2.1}$$

where M is the modulation index, f_{in} is the frequency of the input signal, f_c is the carrier switching frequency and $J_n(*)$ is the n^{th} -order Bessel function of the first kind.

The first term on the right hand side of Eqn. (2.1) is the desired output fundamental component. The second term presents the sum of the carrier frequency components and its odd-order harmonics. The third term presents the sum of the intermodulation products between the input signal and the carrier signal, which are located at the sidebands of the multiples of the carrier frequency. To prevent the intermodulation products folding back into the audio band (causing fold-back distortion), the switching frequency for the pulse width modulator is usually set much higher than the Nyquist criterion, i.e., the carrier frequency is more than 8 to 10 times higher than the audio bandwidth.

2.1.3.2 Pulse Density Modulation (PDM)

Pulse density modulation, also known as Sigma-Delta Modulation (SDM or $\Sigma\Delta$) in [9, 16, 17], uses noise shaping to reduce the noise floor inside the audio band. Owing to the high switching frequency, its THD performance is very good. The main drawback of sigma-delta Class-D amplifier is its relative low efficiency. This is because PDM requires a large amount of pulses to represent a large input signal, whereas PWM only needs to extend the pulse width to present a large input signal without causing extra switching in the power stage.

As a result, PDM will always incur additional switching loss as compared to PWM, and hence it is not the interest of this research work.

The conventional 1-bit $\Sigma\Delta$ modulator is in fact not commonly used in Class-D amplifiers [18]. This is because it is only stable up to 50% modulation and its power efficiency is also limited as typical output data rates are at least 1 MHz (since over 64 times oversampling is necessary to realize sufficient audio band signal-to-noise ratio). Some enhancement methods are introduced to help conventional 1-bit $\Sigma\Delta$ modulators to overcome these problems. In [9], a dynamically adjusted quantizer hysteresis is reported to reduce the output data rate to 450 kHz, helping it to achieve 88% power efficiency. The instability for large input signal is resolved by reducing the order of the modulator from 7 to 2.

2.1.4 Input signal formats — analog versus digital

The input signal formats of a Class-D amplifier can be either analog or digital. The resulting designs are referred as analog Class-D amplifier and digital Class-D amplifier, respectively, in this thesis.

The pulse width modulation process illustrated previously in Figure 2.3 is actually the simplest analog modulator design, which is also referred as natural sampling PWM process, compared to a digital input pulse width modulator. The advantage of analog Class-D amplifier is its simple circuit structure and apparent ease to apply negative feedback control.

Nowadays, most of the musical information are stored in digital format (mainly in pulse code modulated (PCM) format). Digital Class-D amplifier modulates the PCM input signal directly in digital domain, hence removes the requirement for a digital-to-analog converter (DAC) to convert the digital PCM

signal into analog signal. The motivation to eliminate the DAC is its power consumption. Although both the PWM and PDM are widely used in digital Class-D amplifier, only the digital PWM modulator will be briefly reviewed in this thesis. The block diagram of typical open-loop digital PWM Class-D amplifier is shown in Figure 2.4.

Figure 2.4 Block diagram of a typical open-loop Digital Class D amplifier [19].

Despite the advantages of digital amplification, digital Class-D amplifiers are prone to distortion especially in the digital PCM-to-PWM conversion stage. As the PWM signal is generated in digital domain, the effects of sampling and quantization have to be dealt with [20]. The conversion of a sampled PCM signal directly into a proportional PWM signal is known as uniform sampling [21, 22]. Uniform sampling introduces harmonic distortion due to its non-linearity [23]. Many algorithms [21-25] have been investigated and reported in literature to predict the natural sampling point of the analog pulse width modulator based on the successive sampled digital inputs.

Digital Class-D amplifiers require very high frequency bit-clock to produce a high resolution quantized PWM signal. For instance, a 16-bit resolution CD quality signal with 44.1 kHz sampling frequency encoded in PCM format would require a switching frequency of 2.89 GHz (i.e. $44.1\text{k} \times 2^{16}$) in order to reproduce an analog signal equivalent to that resolution [21], without being

affected by the quantization noise. This poses a very strong limitation on the digital Class-D amplifier. To solve this problem, oversampling and noise shaping technology are employed to reduce the number of discrete stages of output PWM signal and to maintain the overall resolution of the output signal. Consequently, Figure 2.5 illustrates the conventional architecture of an open-loop digital Class-D amplifier.

Figure 2.5 Conventional digital Class-D amplifier architecture [20].

Furthermore, it is difficult to apply negative feedback to the digital Class-D amplifier since it requires an analog-to-digital converter (ADC) to convert the output signal back to the digital domain. The ADC limits the cost and performance competences of the digital Class-D amplifier as compared to the analog Class-D amplifier, since the ADC is even more complex and power hungry than the DAC. Up to now, there are mainly two techniques to improve the power supply rejection of the digital Class-D amplifier. One attempt is to sense the supply voltage with a DAC, and using the feed forward correction technique to compensate the digital PWM signal [26, 27]. But it is claimed in [20] that this technique only yield a moderate improvement in the power supply rejection. The other technique is to apply local feedback around the output stage, which is also known as direct pulse amplification or Pulse Edge Delay Error Correction (PEDEC) [28-35]. Such design takes the digitally generated PWM signal as the reference input signal. An error signal is then generated by comparing the feedback output PWM signal with the input PWM signal.

Subsequently, this error signal will be used to modulate the pulse width of the next output pulse. As mentioned in [20], the input PWM signal needs to be well defined in both amplitude and timing. Thus, a high quality one-bit DAC may be required to re-sample the digital input signal to achieve lower jitter.

2.2 Key design specifications and trade-offs

2.2.1 Stability and Reliability

When negative feedback is applied to a Class-D amplifier, the most important design concern is its stability. As Class-D amplifier is a nonlinear system, the stability analysis of such system is quite complicated. For example, the delay through the modulation and pre-driver stages can detrimentally affect the stability of a closed-loop Class-D amplifier. With the various circuit topologies developed in recent years, it is essential to ensure that the system is stable and perform as expected under differential input combinations. The main design block used to shape the transfer function of the system is the loop filter block as shown in Figure 2.2.

The reliability of a Class-D amplifier is mainly determined by the robustness of the power transistors. Since the on-resistance of the p-type and n-type power transistors is very low, power dissipation and heat generation increase due to the shoot-through current that occurs when two transistors are turned on simultaneously [36]. This large shoot-through current may damage the power transistors. To prevent this shoot-through current, a non-overlapping time is usually inserted, which is also well known as dead-time. It ensures one power transistor turns off first, before the other one turns on.

2.2.2 Efficiency

Due to power losses in the output transistors, which have finite on-resistance, and rise/fall times, the power efficiency of a practical Class-D amplifier is less than 100%. Additionally, the control circuit also consumes a fixed amount of quiescent current. To summarize the results, the efficiency of the amplifier is given by the following equation:

$$Efficiency(\eta) = \frac{P_L}{P_L + P_C + P_{SW} + P_Q} \quad (2.2)$$

where P_L is the power delivered to the load, P_C is the conduction loss, P_{SW} is the switching loss and P_Q is the quiescent power loss.

The expression of the conduction loss P_C is dependent on the output stage configuration (see Section 2.3.2) and can be estimated as

$$P_C = \begin{cases} P_L \times 2(R_{DS(on)} + R_{Ind}) / R_L & \text{for BTL output} \\ P_L \times (R_{DS(on)} + R_{Ind}) / R_L & \text{for single-ended output} \end{cases} \quad (2.3)$$

where $R_{DS(on)}$ is the on-resistance of the power MOSFETs, R_{Ind} is the DC resistance of the inductor and R_L is the DC resistance of the load (i.e. the speaker). For BTL configuration, two MOSFETs and two inductors are connected to the load in the conduction loop. The drain current is defined as

$$I_{D(RMS)} = \sqrt{P_L / R_L} \quad (2.4)$$

The switching loss P_{SW} is the result of the charging/discharging the circuit parasitic capacitance and short-circuit current, which can be estimated based on the amplifier's specifications and the MOSFET's datasheet parameters.

$$P_{SW} = \frac{1}{2} I_D V_{DD} \cdot (t_r + t_f) \cdot f_{SW} + \frac{1}{2} C_{oss} V_{DD}^2 f_{SW} + \frac{1}{2} K Q_{rr} V_{DD} f_{SW} + 2 Q_g V_{driver} f_{sw} \quad (2.5)$$

where V_{DD} is amplifier's supply voltage, t_r and t_f are MOSFET rise and fall times, C_{oss} is MOSFET output capacitance, Q_{rr} is MOSFET body diode reverse recovery charge, K is the factor due to MOSFET's T_J and specific amplifier's conditions such as I_F and dI_F/dt , and V_{driver} is the voltage of the gate driver. More details can be found in [37].

When designing an amplifier for efficiency, it is vital to identify the normal operating power range since an audio signal has a much lower average power than pure sinusoidal wave. A good example is given in [38] which illustrates how the amplifier efficiency varies with output power, where it concludes that at high power levels, the conduction loss dominates and at the lower power levels, however, the switching and quiescent current losses dominate. It is also worthwhile to highlight that an audio signal operates at a much lower average power level than many engineers believe. Most music has a crest factor of 13 dB to 19 dB. Crest factor is a measurement for comparing the peak power P_{PK} to average power P_{RMS} and is expressed as

$$\text{Crest Factor} = 10 \cdot \log(P_{PK} / P_{RMS}) \quad (2.6)$$

For a given fabrication process, supply voltage and load resistance, two design methodologies were presented in [39] to determine the optimized aspect ratios of the power transistors in terms of power efficiency either at a single modulation index or in a range of modulation indexes.

2.2.3 Total Harmonic Distortion (THD)

Linearity is probably the most important specification for amplifiers. This is especially true for audio amplifier that aimed to reproduce a high-fidelity audio signal. For a non-linear device, the output waveform will deviate from the input

waveform. In the frequency domain with a single sine wave stimulus, this non-linearity will appear as energy at harmonics of the fundamental sine wave in addition to the fundamental itself [40].

Hence, the fidelity of the audio amplifiers is regularly examined in the form of Total Harmonic Distortion (THD) with a single-tone input signal, which is defined as an amplitude ratio:

$$THD(\%) = \frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{3f}^2 + \dots}}{V_f} \quad (2.7)$$

where V_f is the output signal component at frequency equal to the input signal and V_{2f} is the output signal component at frequency equal to two times input signal frequency (i.e., the second harmonic) etc.

Another widely used specification that considers both the linearity and noise performance of the DUT is Total Harmonic Distortion plus Noise (THD+N). It accumulate all the frequency components inside the 20-20k Hz audio band and then compare it with the output fundamental frequency component.

2.2.4 Intermodulation Distortion (IMD)

Recently, there have been increasing demands on the analysis of the multi-tone response of Class-D amplifiers, which is quantified by the intermodulation distortion (IMD), as IMD makes music sound harsh and unpleasant [41]. Some audio engineers have even claimed that IMD is more important than harmonic distortions and closely reflect the fidelity (linearity) of the amplifier.

Intermodulation distortion occurs when two or more signals with different frequencies are fed into a nonlinear amplifier. The sum and difference of the input frequencies are present at the output. In actual measurement, with a two-

tone stimulus signal (i.e. at frequencies equal to f_1 and f_2), the amplifier output signal will consist of the desired two sinusoidal waves plus an infinite number of intermodulation products (IMPs) at frequencies equal to

$$|mf_1 \mp nf_2| \quad (2.8)$$

where m and n are all possible integers. The “order” of any particular IMP is the sum of the absolute values of m and n . IMD is usually expressed as the ratio of RMS summation of the IMPs to the magnitude of the higher frequency component:

$$IMD_K(\%) = \frac{\sqrt{\sum_{m=1}^{K-1} \sum_{n=1}^{K-m} (V_{m \cdot f_2 - n \cdot f_1}^2 + V_{m \cdot f_2 + n \cdot f_1}^2)}}{V_{f_2}} \times 100 \quad (2.9)$$

where V_{f_2} is the frequency component of the output signal at frequency f_2 , and $V_{mf_2+nf_1}$ is the voltage at frequency equal to $m \cdot f_2 + n \cdot f_1$, etc. The subscript K indicates the maximum order of the IMPs that is considered in the IMD calculation.

2.2.5 Signal to Noise Ratio (SNR) and Dynamic Range (DR)

The noise performance determines the smallest discrete power level that an amplifier can accurately output, and hence affects its dynamic range. As explained in [42], “a wide dynamic range is what makes music sound live and 3-dimensional. The sonic implications of a broad dynamic range become more striking with the observation that while the upper amplitude regions impart what a musical instrument is, the lower regions impart where it is. Spatial location of sound is the driving force behind the entire home theatre movement, which makes these low-level signals even more important”. The dynamic range

of human hearing is roughly 140 dB [43]. The dynamic range of music normally perceived in a concert hall does not exceed 80 dB, and human speech is normally perceived over a range of about 40 dB [37].

Signal-to-Noise Ratio (SNR) is simply a computation of the results of two measurements [40]. The “signal” measurement is typically of a mid-band (usually 1 kHz) sine wave at a specified output level, usually the maximum rated or normal operating level of the device. The “noise” measurement must specify either the measurement bandwidth or a weighting filter, where the latter is an approximation to the sensitivity curve of the ear under some conditions. In addition, the input of the device under test (DUT) must be properly terminated. The ratio of the two measurements is then the SNR of the device. This is normally considered to be the effective dynamic range of the device. The most common bandwidth for noise measurements in professional audio, broadcasting, and consumer audio applications is 20 Hz–20 kHz, or the nearly-equivalent 22 Hz–22 kHz specified in ITU-R 468 [40]. Note that ITU-R stands for the Radio communications sector of the International Telecommunications Union.

2.2.6 Power Supply Rejection Ratio (PSRR)

Power Supply Rejection Ratio (PSRR) is a measure of a device’s ability to reject noise from the power supply. It is defined as the ratio of the change in power supply voltage ΔV_{in} to the corresponding change in output signal of the device ΔV_{out} , which is often expressed as

$$PSRR(dB) = 20 \log \left(\frac{\Delta V_{in}}{\Delta V_{out}} \right) \quad (2.10)$$

When integrating the Class-D amplifier on chip with other functional blocks, as presented in [44-48], a high PSRR becomes essential to guarantee a good listening experience. For example, when a global system for mobile communications (GSM) phone transmits signals, RF power amplifier can sink up to a 2.5-A pulse current from the battery for a 557- μ s period. This pulse is repeated every 4.6 ms, i.e., 217 Hz, while the transmission continues, and the supply rail fluctuates as a result [48]. In the past, 65-dB PSRR was sufficient, but higher PSRR (> 80 dB) is now required for modern Class-D amplifiers [49], especially for direct battery hook-up designs. In addition, it is often desirable to measure PSRR over a range of frequencies and to produce a spectrum plot of PSRR versus frequency [13].

Open-loop Class-D amplifier has a poor PSRR performance of only 6 dB, hence requires a high performance linear regulator. For a closed-loop Class-D amplifier, the loop filter structure and component matching dominant the PSRR performance. In addition, the differential load configuration (see Section 2.3.2) instead of the single-ended design is preferred, as ideally it has infinite rejection on power supply noise.

2.2.7 Electromagnetic Interference (EMI)

The integration of circuit blocks on the same printed circuit board or even on the same chip has prompted active research in the study of electromagnetic interference (EMI). EMI emission of one circuit can pollute the surrounding circuits and appliances. This is especially critical for switching-mode devices, such as the Class-D amplifier and DC-DC converter, as the switching operation generates high dv/dt and di/dt signals with wide disturbance bandwidths. These

voltage and current spikes induce large ac displacement currents in both the physical and parasitic circuit elements [50] and are widely believed to be the main sources of EMI emissions.

The investigation on EMI can be centered around three aspects: the EMI source, the coupling path (i.e. conducted or radiated) and the victim [51]. While it is important to block the coupling path and to improve the EMI immunity of the victims, the most effective way to achieve electromagnetic compatibility is to suppress the EMI emission of the source. Hence, various EMI reduction techniques for switching-mode circuits have been proposed in recent years, for example, filtering, random modulation, soft switching, and frequency modulations [51-53]. It is well known that the slowing down the turn-on/turn-off times of the modulated pulse signal can significantly reduce EMI emissions. However, designing a low-EMI switching power amplifier usually causes power efficiency reduction, and even corrodes the linearity.

2.3 Analog pulse width modulated closed-loop Class-D amplifier

Based on the basic overview on Class-D amplifiers presented in Section 2.1, the pulse width modulated closed-loop structure has been selected for further study. PWM provides high efficiency and the negative feedback ensures the essential immunity to supply noise. Due to time limitation, the study focused on analog input Class-D amplifier with a single feedback path (from the output of the power stage to the input of the loop filter). This section investigates the circuit structure, which includes load configurations, potential pulse signal

levels, the widely adopted linear continuous-time model, popular loop filter structures and also the alternative modulator topologies.

2.3.1 Conventional circuit structure

While there are a variety of modulator topologies for modern Class-D amplifiers, the most basic topology deploys pulse width modulation that has a triangle-wave carrier generator. Figure 2.6 shows a simplified circuit diagram of a PWM-based, single-ended Class-D amplifier. The loop filter is constructed as a first-order integrator. The resistor, R_2 , is connected between the output of the power stage v_{pwm} and the inverting input of the operational amplifier (op-amp), forming a negative feedback path. The linear triangular carrier generator can be constructed using a 1st-order op-amp integrator and a comparator [54]. The output of the loop filter is then sent to the comparator, where it is compared with a triangular carrier signal. A pre-driver is employed to drive the large gate capacitors of the power MOSFETs. The power MOSFETs are connected as totem-pole structure to act as switches. The load R_L presents the speaker with typical values of 4 Ω , 8 Ω , 16 Ω and 32 Ω . The Class-D amplifier is powered by dual supply rails, $\pm V_{DD}$.

Figure 2.6 Conventional circuit structure of PWM-based Class-D amplifier.

2.3.2 Load configurations—single-ended versus bridge-tied-load

As shown in Figure 2.6, one side of the load resistor is connected to the output of the second-order LC filter and the other side is connected to ground. This load configuration is named as single-ended or half-bridge. Alternatively, the load can be differentially connected, as depicted in Figure 2.7(b), yielding a so-called bridge-tied-load (BTL) configuration (also known as differential-ended or full-bridge design).

Figure 2.7 Load Configurations: (a) single-ended; (b) Bridge-tied-load.

Since only one power MOSFET is connected to the load at any time, a single-ended design will have a lower on-resistance, and hence less conduction loss. This is quite important for high-power appliance. However, it requires either dual supply voltages (as seen in Figure 2.6) or a big decoupling capacitor, C_c , to be connected in series to the load to remove the DC components of the pulse signal (as shown in Figure 2.7(a)).

The BTL configuration doubles in component need (e.g., four power MOSFETs and two inductors), and which increases the size and cost of the power amplifier. But, it also doubles the output swing, yielding four times output power to the load. Furthermore, BTL configuration requires only single supply voltage, without decoupling capacitor, and the balanced operation cancels out the even order distortions.

2.3.3 Pulse signal levels—AD-modulation versus BD-modulation

Figure 2.8 illustrates the PWM signal waveforms with respect to the input signal for both the AD and BD modulations when implemented with a BTL output configuration. When the carriers of the two halves are in opposite phases, as seen in Figure 2.8(a), the PWM signal across the load has only two voltage levels and is referred to as AD modulation or binary modulation. Conversely, when the carriers of the two halves are in phase, as demonstrated in Figure 2.8(b), the output PWM signal takes on three voltage values, and thus named BD modulation or ternary modulation.

Figure 2.8 Pulse signal levels: (a) AD modulation and (b) BD modulation [49].

AD modulation is dominant in single-ended output configurations, thanks to its simple circuit implementation. The main advantage of AD modulation is that the output signal has zero common-mode voltage since the bridge halves always switch simultaneously in opposite directions [49].

The BD-modulation was introduced by Martin [55] in 1970 and first realized with a single-ended output configuration. Nowadays, BD modulation is usually realized with a BTL output configuration. Furthermore, since the carrier frequency components of the two half bridges are in phase, BD modulation has much lower differential-mode high-frequency current ripple loss, as compared to AD modulation. This is essential for a “filterless” Class-D amplifier to achieve high power efficiency. A “filterless” Class-D amplifier removed the explicit external LC filter but use the speaker itself to filter the output signal. In addition, BD modulation is much less sensitive to clock jitter, than the AD modulation [56].

2.3.4 Loop filter designs—first-order versus second-order

The design of the closed-loop Class-D amplifier with pulse width modulator was originally focused on the loop filter schemes and the implementations were based on the linearized continuous-time model [48, 57]. Figure 2.9 presents the circuit schematics of the well-known 1st-order and 2nd-order loop filter designs. Some commercial products, such as TDA7490[58], are based on the 2nd-order loop filter design shown in Figure 2.9(b).

The loop filter transfer function, G_{LF} , is defined from the feedback signal, v_{pwm} , to the loop filter output signal, v_{int} . Thus, the transfer functions of the 1st and 2nd order loop filter are expressed as follows:

$$G_{LF_1st}(s) = \frac{v_{int}(s)}{v_{pwm}(s)} = -\frac{A_1}{s} \quad (2.11)$$

$$G_{LF_2st}(s) = \frac{v_{int}(s)}{v_{pwm}(s)} = -\frac{A_2(s + \omega_z)}{s^2} \quad (2.12)$$

where $A_1 = 1/(R_2 C_0)$, $A_2 = 2/(R_2 C_1)$ and $\omega_z = 1/(2R_3 C_1)$ are derived based on the passive components given in Figure 2.9 under the hypothesis of ideal op-amps. Then the transfer function from input signal v_{in} to loop filter output signal v_{int} is expressed as $(R_2 / R_1) \times G_{LF}(s)$. Alternative circuit implementations of the 2nd-order loop filter were introduced in [57, 59] with the same transfer function.

Figure 2.9 Circuit implementations of (a) 1st-order and (b) 2nd-order loop filter in a closed-loop conventional PWM Class-D amplifier.

Except the widely used 1st-order and 2nd-order designs, higher order loop filters have also been reported [11, 48]. A three-level 3rd-order input-feedforward structure proposed in [48], aimed to achieve a high PSRR and SNR. In [11], a 3rd-order minimum aliasing loop filter was employed to attenuate the intrinsic harmonic distortion (see Section 2.4.3). However, the 3rd-order (or higher order) loop filters are more liable to have stability problems and hence extensive simulations during the design phase are necessary to confirm the circuit's stability [48].

2.3.5 Linearized continuous-time model

As the pulse width modulator is ideally distortion-free inside the audio band, it is usually modeled as a constant gain block, G_{PWM} , combined with an error signal, $n(t)$, as illustrated in Figure 2.10(a). G_{PWM} is equal to V_{DD}/V_C with the

assumption that the PWM output signal switches between the supply rails $\pm V_{DD}$ and the triangular carrier signal varies between $\pm V_C$ (as specified in Figure 2.6). In a typical pulse width modulator design, the peak-to-peak amplitude of the high frequency carrier is typically in the range of 30% to 70% of the supply voltage [59]. Hence, in general, G_{PWM} is less than 5 for a larger input dynamic range and signal-to-noise ratio. The error signal, $n(t)$, presents the distortion caused by the non-linearity of the output stage and power supply noise. For power supply noise at the Class-D output, the resultant noise will be attenuated by 50% after low-pass filtering [59] and as a result, $n(t)$ is only half if the noise is originated from the supply rails. This should be reflected in the linearized model of the Class-D amplifier for PSRR simulation [8].

Figure 2.10 Linearized continuous-time model of the PWM Class-D amplifier.

Base on the linearized model, two transfer functions are identified: $STF(s)$ is the transfer function from input signal, $s(t)$, to PWM output signal, $g(t)$; and $ETF(s)$ is the transfer function from the error signal to the PWM output signal. These two transfer functions are expressed as

$$STF(s) = \frac{g(s)}{s(s)} = \frac{H(s)}{1 + H(s)} \quad (2.13)$$

$$ETF(s) = \frac{g(s)}{n(s)} = \frac{1}{1 + H(s)} \quad (2.14)$$

where $H(s) = G_{LF}(s) \cdot G_{PWM}$ is the loop gain.

Based on linear control theory, the loop gain, $H(s)$, should be maximized in the audio band so as to improve the linearity of the audio amplifier and to suppress the nonlinearities of the power stage. The loop filter, $G_{LF}(s)$, is the dominant factor that determines the transfer function of the loop gain. The conventional design procedure for the loop filter parameters based on the linearized model will be reviewed in Chapter 6.

This linear continuous-time model is simple and hence widely accepted by industry, yet it has some limitations summarized as follows:

- 1) This model becomes less accurate at higher frequencies (near the switching frequency). As presented latter in Chapter 6, the system stability criteria derived based on this linear model causes an unoptimized placement of the zero inside a 2nd-order loop filter transfer function.
- 2) This model does not reflect the intrinsic distortion phenomenon of the closed-loop Class-D amplifier. Further investigation in this will be detailed in Section 2.4.

2.3.6 Self-oscillating modulation

Besides the conventional PWM-type architecture in [11, 24, 48, 57], a variety of modulator topologies have been developed for the analog feedback pulse width modulated Class-D amplifiers in recent years. They are: self-oscillating modulation [13, 46, 60-65], carrier modulation [66] and uniform PWM by inserting a sample-and-hold block between the loop filter and the pulse generator [47, 67, 68]. As an important alternative, a brief review on self-oscillating modulation is provided here. The remaining two topologies that are

developed specially for suppressing the intrinsic harmonic distortion will be reviewed later in Section 2.4.3.

Self-oscillating modulation refers to a group of modulators designed for closed-loop pulse width modulated Class-D amplifier that does not require carrier signal. They are characterized by the open loop transfer function that is shaped to achieve the 180° phase shift at a desired switching frequency [69]. This is obtained via either phase-shaping the loop filter network or using a hysteresis comparator. The circuit structures of the self-oscillating topologies are simple, as no carrier generator is required. Furthermore, the self-oscillating topologies offers a wide frequency bandwidth and hence, the fast response.

The switching frequency of a self-oscillating amplifier reduces significantly with increasing modulation index due to the integration of a variable error. The advantage of varying the switching frequency is to spread out the energy of the switching frequency signals, to reduce the EMI. It also leads to an improved power efficiency at high output levels. On the contrary, in the case of stereo application, the switching frequency difference between the multiple channels can inject low frequency intermodulation products into the audio band [62]. Fortunately, with careful layout and substrate isolation, such effect can be greatly reduced [46]. In addition, the effect of the modulation index on Class-D switching frequency implies that the audio signal level should be limited to a proper value in order to keep the switching frequency variation within a permissible range [70]. Consequently, the idle switching frequency of the self-oscillating amplifier is usually designed much higher than that of PWM topology to achieve equivalent audio amplitude range.

The designs of the self-oscillating amplifiers are commonly classified into two broad categories: hysteresis-controlled (HC) oscillation [60, 61] and phase-shift controlled (PSC) oscillation [13, 63-65]. The PSC designs reported in [13, 63, 64] obtain the feedback signal from the output of the low-pass filter. The advantage of this design is that the 180° phase lag of the LC filter is helpful for creating a positive feedback and the nonlinearity of the LC filter is suppressed by including it in the feedback loop. A control block is used to shape the phase response of the loop gain. On the other hand, the HC designs are stable by nature, but require a hysteresis window generator, which makes its overall architecture more complex when compared to the PSC designs.

2.4 Intrinsic distortion of closed-loop Class-D amplifier

2.4.1 Mechanism of intrinsic harmonic distortion

A block diagram of a conventional pulse width modulated Class-D amplifier is presented in Figure 2.11. Here, a 2nd-order integrator is engaged as the loop filter to provide a high loop gain in the audio band, and hence suppress the non-ideality of the power stage.

Figure 2.11 Block diagram of conventional pulse width modulated Class-D amplifier.

Intrinsic harmonic distortion arises when the PWM signal is fed back to the loop filter through resistor R_2 in Figure 2.11. As the loop filter cannot completely remove the carrier frequency components inside the feedback PWM signal, there exists input dependent residual carrier signal at the output of the loop filter [47]. The residual carrier components create timing errors at the rising and falling edges of the PWM signal, thus causing the intrinsic harmonic distortions on the reconstructed output signal.

This phenomenon can also be explained based on the sampling nature of the pulse width modulator [11]. In the frequency domain, the residual carrier components inside the loop filter output signal are presented as intermodulation products between the carrier and the input signal located in the sideband at multiples of the carrier frequency. The sampling nature of the pulse width modulator causes aliasing errors, thereby shifting the sideband frequency components back into the audio range.

In a well-designed Class-D amplifier, the intrinsic distortions dominate the linearity performance when the input signal is large and at high frequency. Since intrinsic harmonic distortion is generated due to circuit structure and is unrelated to the practical implementation of the circuit, its effect can be simulated using MATLAB Simulink, where the circuit is represented by transfer functions for the linear blocks and ideal switches for the nonlinear blocks. Consequently, only the intrinsic harmonic distortions are considered, as no practical circuit distortion is included in this model. Figure 2.12 illustrates a typical frequency spectrum of a closed-loop PWM Class-D amplifier, which clearly indicates that there are significant odd order harmonics in the audio band.

Figure 2.12 Output frequency spectrum of a closed-loop PWM Class-D amplifier through MATLAB Simulation.

2.4.2 Analysis of intrinsic harmonic distortion

Various analyses on the intrinsic distortion phenomenon have been reported in recent years [11, 71-73], focusing only on AD modulation (binary PWM signal).

The analysis in [11] provides an insight into the source of the intrinsic distortions, and the derivation process closely reflects the working mechanism of the system. At modest algebraic cost, it gives an expression for the output which is valid for a general input signal before detailing on the case of a sinusoidal input that captures the third-harmonic distortion terms. This problem is analyzed based on a conceptual model by Risbo in [11]. He claimed that the forms of the intrinsic harmonic distortion are different for 1st-order and 2nd-order integration loop filters. For 1st-order integration loop filter, the intrinsic harmonic distortion is due to the phase modulated error, which is influenced by the imaginary part of the loop filter frequency response. However, for 2nd-order

integration loop filter, the intrinsic harmonic distortion is due to the DC-error, which is influenced by the real part of the loop filter frequency response. In addition, it was found that the third harmonic from the 1st-order loop filter design is predicted to be 6 dB lower than for the 2nd-order design.

In 2006, a large-signal time-domain modeling methodology was first introduced by Stephen M. Cox [73] to analyze the nonlinearity of a 1st-order Class-D amplifier. Through its rigorous derivation process, the time-domain modeling is able to accurately predict the audible frequency components in the output spectrum. Through collaboration with Professor Cox, a series of analytical works on the intrinsic distortion of a closed-loop 2nd-order Class-D amplifier was successfully implemented and will be presented in this thesis. In Chapter 4, the audible output spectrum of a 2nd-order loop filter Class-D amplifier with AD modulation under both single-tone and two-tone stimulus is investigated. The intrinsic distortions of a fully-differential BD-modulated Class-D amplifier have also been scrutinized and will be described in Chapter 5.

2.4.3 Techniques in suppressing intrinsic harmonic distortion

Some attempts at reducing the intrinsic harmonic distortion have been reported in literature [11, 47, 67, 68, 73, 74].

2.4.3.1 *Minimum aliasing error (MAE) loop filters*

The proposed solution in [11, 74] is to build a loop filter that behaves as a 1st-order integrator from a distortion perspective but has the loop gain of a 2nd-order integrator so as to attain a higher loop gain. Therefore, even when the phase delay modulation distortion is unchanged in the open-loop, the high loop gain

will be able to reduce the closed-loop THD. The transfer function of the proposed design can be expressed as

$$\begin{cases} H_{mae}(s) = \frac{K_2}{s^2} + \frac{p \cdot K_p}{s + p} \\ K_p = K_2 / p^2 \end{cases} \quad (2.15)$$

By summing the designed low-pass filter (i.e., $p \cdot K_p / (s + p)$) with the 2nd-order integrator, the real part of the loop filter frequency response above the switching frequency is asymptotic cancelled. Note that the MAE filter has a 1st-order high frequency roll-off of the amplitude characteristic, which is helpful for ensuring closed-loop stability. Another property is that all low and high frequency asymptotes in log-log plots will intersect at one point, having frequency equal to the pole frequency p and amplitude K_p . The circuit implementation of the MAE loop filter is presented in Figure 2.13.

Figure 2.13 Circuit schematic of the Class-D audio Amplifier with an MAE loop filter [11].

2.4.3.2 Inserting a sample-and-hold block and a feedforward path

It was first reported in [68, 73] that inserting a sample-and-hold (SAH) block between the loop filter and the pulse width modulator and a feedforward path from the input of the Class-D amplifier to the input of the pulse width modulator can suppress the intrinsic harmonic distortion. Figure 2.14 demonstrates the circuit topology. The output of the loop filter is connected to the input of the sample-and-hold device, where $h(t)$ is sampled at either one or two times per carrier period. The rigorous mathematical derivation in [73] proved that for a 1st-order loop filter design, by properly selecting the gain of the feedforward path, the intrinsic distortion can be completely eliminated (at least up to the order of the analysis).

Figure 2.14 Block diagram of a sample-and-hold topology.

The above idea was recently implemented in [47, 67] for a BD-modulated fully-differential Class-D amplifier (but without the feedforward path), and alternatively named as “UPWM”. The explanations on the working mechanism of the SAH block from both the time and frequency domains are quite interesting. As illustrated in Figure 2.15, by sampling the loop filter output twice per carrier period, infinite attenuations at twice the carrier switching frequency and its harmonics can be formed in the frequency response. It is

equivalent to a transmission zero (very deep notch) at the sample frequency and hence blocks the carrier frequency components from the input of the pulse width modulator. Figure 2.16 demonstrates the time domain waveforms, illustrating that the ripples at the output of the loop filter are eliminated by the sample-and-hold process. The above explanations reproduced from [67] are quite reasonable, but further investigation is required, as based on the mathematical analysis in [73], on a first-order Class-D amplifier, the effect of the SAH block without the feedforward path on suppressing the intrinsic distortion is quite limited.

Figure 2.15 Comparison of the closed-loop frequency responses between conventional PWM and SAH topology [67].

Figure 2.16 Timing waveforms for SAH topology [67].

Consequently, an impressive THD of 0.00122% at 1 kHz and 50% maximum output power, have been reported in [47, 67], even though an extremely high switching frequency (i.e., 1 MHz) was employed in the design, and is probably limited by the size of the switching capacitors inside the sample-and-hold block. In fact, when the switching frequency of the Class-D amplifier is high enough, the intrinsic distortion problem is insignificant. Hence, alternative sample-and-hold circuit topologies should be adopted (rather than a switching capacitor design to reduce the switching frequency and switching loss). In addition, the sample-and-hold block introduces delay to the control loop and compromises the stability margin of the amplifier. Therefore, preserving the stability margin was the primary design concern in [67].

2.4.3.3 *Carrier symmetry modulation*

A novel approach to suppress the intrinsic harmonic distortion was reported in [68] by modulating the symmetry of the carrier signal. The idea was based on an analysis on the source of intrinsic harmonic distortion through observing the output PWM signal with DC input, as described in Figure 2.17.

The actual switching times, t_1 and t_3 , are asymmetrical with respect to the peak of the carrier signal, and hence causes nonlinear phase advances compared with t_2 and t_4 , the switching times of open-loop Class-D amplifier with the same DC input signal. It was claimed in [68] that it is the nonlinearity of this phase advance that is largely responsible for the intrinsic distortion of the amplifier design. To compensate this nonlinear phase advances, the symmetry of the triangular carrier signal is modulated to create a phase delay. The proposed modulating signal is a feed-forward signal that is in proportion to the derivative

of the input signal. The block diagram of the design is shown in Figure 2.18. A mathematical analysis is provided in [73] to support the design. However, its application is limited as it is only reported to be effective for the 1st-order loop filter Class-D amplifier. Since 1st-order loop filter is not widely used due to its low loop gain, this topology has not received much attention.

Figure 2.17 Analysis on intrinsic harmonic distortion [68]: (a) Illustrative circuit diagram, (b) Plot of waveforms $h(t)$ and $v(t)$, showing the phase advance of the switching times.

Figure 2.18 Block diagram of the proposed carrier modulation topology [68].

2.4.3.4 Feedforward Sample-and-Hold block

The block diagram shown in Figure 2.19 is another circuit topology proposed in [73] to eliminate the intrinsic harmonic distortion of a first-order Class-D amplifier. It shows that a sample-and-hold (SAH) block is added on the feedforward path from the Class-D input signal to the positive input of the comparator. The output of the SAH block, $p(t)$, is equal to the input signal at the beginning of each carrier period. Until now, no circuit implementation on this proposed topology has been reported.

Figure 2.19 Block diagram of the feedforward sample and hold topology.

2.5 Summary

This chapter has first critically reviewed the Class-D power amplifier in the aspects of basic circuit blocks and key design specifications. Compared to pulse density modulation (PDM), the pulse width modulation (PWM) is more prevalent largely due to its low switching frequency that is essential for achieving a high power-efficiency. A comprehensive review on closed-loop analog-input PWM Class-D amplifiers thereof has been delineated, including the conventional circuit structure, load configuration, pulse signal levels, loop

filter designs and the various advanced topologies. Finally, a deeper review on intrinsic distortion of a closed-loop PWM Class-D amplifier has been provided to form the essential background knowledge for this research work.

Chapter 3 Visualization of Intrinsic Harmonic Distortion

3.1 Introduction

In this chapter, we present an insightful methodology to investigate the intrinsic harmonic distortion of the closed-loop Class-D amplifier by a simple means of comparing the output PWM signals between the closed-loop and open-loop Class-D amplifiers. The advantage of this method is that it permits direct visualization of the error signals, allowing the circuit designer to envisage the source of the intrinsic harmonic distortion. Furthermore, the relationship between the error sources and the distortions within the demodulated output signal is also investigated. A large portion of work presented in this chapter had been published in [7].

This chapter is organized as follows. In Section 3.2, the methodology for plotting the phase and duty cycle errors' time domain waveforms is demonstrated. The analysis on the phase and duty cycle errors, corresponding to a sinusoidal input signal, is illustrated in Section 3.3. The relationship between the error signals and the distortions within the demodulated output signal is then investigated in Section 3.4. Finally, a summary is given in Section 3.5.

3.2 Phase and duty cycle errors

As explained in Section 2.4, the intrinsic harmonic distortion is caused by the residual high frequency components, i.e., the ripple signal, inside the loop filter output signal of a closed-loop Class-D amplifier. As a result, both the rising-edge and the falling-edge switching times of the output PWM signal varied, creating unwanted odd-order harmonics in the demodulated output signal. Since an ideal open-loop PWM-based Class-D amplifier is distortion-free, we had deployed it as a reference to examine the errors caused by the ripple signal.

3.2.1 Definition of phase and duty cycle errors

The analysis on the intrinsic harmonic distortion begins with a comparison of the output PWM waveforms between the closed-loop and open-loop Class-D amplifiers with synchronized input signal and triangular carrier signal. Figure 3.1 shows the block diagram designed for MATLAB simulation in this research. Due to the negative feedback topology, the output signal of the closed-loop amplifier is inverted as compared to the input signal. For the output signal of the open-loop amplifier to be in-phase with the closed-loop amplifier, the input signal to the open-loop amplifier is inverted via an unity-gain inverter.

Figure 3.1 Simulink model for comparing the PWM output signals between the closed-loop and open-loop designs.

The typical PWM waveforms with the inverted input signal and loop filter output signal for the respective open-loop and closed-loop amplifiers are illustrated in Figure 3.2. As can be seen, due to the residual high frequency ripples at the output of the loop filter (see solid line in Figure 3.2(a)), the switching times of the PWM signal for the closed-loop amplifier arrives earlier than that of the open-loop amplifier. The time advancements are unequal at the rising and falling edges of the PWM signals, i.e., t_1 is ahead of t_2 , and t_3 is ahead of t_4 . Note that the input signal frequency is set to 20 kHz for easy viewing of the mismatch.

The timing errors between the closed-loop and open-loop PWM signals at the rising and falling edges are defined as

$$T_{re} = t_2 - t_1 \quad (3.1)$$

and

$$T_{fe} = t_4 - t_3 \quad (3.2)$$

Figure 3.2 Typical signal waveforms: (a) inverted input signal for the open-loop amplifier and loop filter output signal of the closed-loop amplifier and carrier signal; (b) PWM signals for open-loop and closed-loop amplifiers.

Alternatively, as reported in [71] the mismatch between the two PWM signals can be described through phase and duty cycle errors. In this work, the phase error is defined based on the average of the rising-edge and falling-edge timing errors whereas the duty cycle error is defined as the ON duration of the closed-loop output PWM signal minus the ON duration of the open-loop output PWM signal, which is in fact proportional to the difference between the rising-edge and falling-edge timing errors, and can be expressed as follows:

$$\theta_e = \pi \cdot (T_{re} + T_{fe}) / T \quad (3.3)$$

and

$$D_e = (T_{re} - T_{fe}) / T \quad (3.4)$$

3.2.2 Phase and duty cycle error waveforms

In order to analyze the effect of the phase and duty cycle errors on the output signal, we need to plot the time-domain waveforms of the two errors that correspond to a sinusoidal input signal. However, this is not a straightforward task, as the phase and duty cycle errors are scaled values that are defined in each carrier period, but without a proper time reference. Based on analyses, the location of the phase and duty cycle errors in time domain is extremely important. For example, by simply placing them at the centre of each period will lead to artificial frequency components in the waveforms created.

In order to circumvent this obstacle, the rising-edge and falling-edge timing errors are first located at the respective switching time of the ideal open-loop PWM signal, i.e., t_2 and t_4 . This will yield the two timing error signals of Figure 3.3(a) and (b), where both are discrete in time, with unequal time intervals, and unsynchronized with each other.

In order to calculate the phase and duty cycle errors, the rising-edge and falling-edge timing errors are to be aligned in the time axis. This is achieved by converting the non-uniform sampled data to uniform sampled data through interpolation. With the assumption that the two timing error signals contained only low frequency components as compared to the carrier signal, cubic spline interpolation is applied to formulate a piecewise function $S(x)$ that contains a group of third degree polynomials defined by

$$s_i(x) = a_i(x - x_i)^3 + b_i(x - x_i)^2 + c_i(x - x_i) + d_i \quad (3.5)$$

where a_i , b_i , c_i and d_i are the coefficients of the fitting curve for the interval starting from data input (x_i, y_i) and hence $y_i = s_i(x_i)$. The coefficients are calculated such that the first and second derivatives of the piecewise function, i.e., $S'(x)$ and $S''(x)$, are continuous across the entire data interval, to allow the resulting interpolated curve to smoothly pass through all data points. Further details on the calculation procedures can be found in [75].

The interpolated uniform-sampled timing error signals are depicted in Figure 3.3(c) and (d). Note that in time domain, the interpolated samples for the rising and falling edge timing errors do synchronize with each other. For the purpose of illustration, only two samples are considered at each carrier period, but in the actual application, more samples will be inserted to guarantee a smooth curve.

Figure 3.3 Procedures for generating phase and duty cycle error waveforms: (a) non-uniform sampled rising-edge timing error; (b) non-uniform sampled falling-edge timing error; (c) interpolated rising-edge timing error; (d) interpolated falling-edge timing error; (e) phase error and (f) duty cycle error.

With the uniform-sampled timing error data, the time domain waveforms of the phase and duty cycle errors can be plotted by extending the definitions of the phase and duty cycle errors to as follows:

$$\theta_e(n \cdot \tau) = \pi \cdot [T_{re}(n \cdot \tau) + T_{fe}(n \cdot \tau)] / T \quad (3.6)$$

$$D_e(n \cdot \tau) = [T_{re}(n \cdot \tau) - T_{fe}(n \cdot \tau)] / T \quad (3.7)$$

where τ is the time interval of the interpolated error data. The computed phase and duty cycle errors are plotted in Figure 3.3(e) and (f). The complete process was programmed in MATLAB.

3.3 Analysis on phase and duty cycle errors

In this section, the phase and duty cycle errors of a 2nd-order Class-D amplifier are demonstrated through waveform simulations. The amplifier's loop filter has a 2nd-order integrator transfer function described in [57]. Figure 3.4 shows the resulting phase and duty cycle error waveforms based on sinusoidal input signals that are simulated at different frequencies, i.e., 1 kHz, 2 kHz and 5 kHz. The modulation index of the input signal was set to 0.7. The horizontal axis is the period of the input signal which allows overlapping of error signals with different input signal frequencies. The characteristics of the phase and duty cycle errors can be summarized as follows:

- As shown in Figure 3.4(a), the phase error is the lowest when the input signal is at its peak or valley. On the other hand, when the input signal crosses the zero reference, the phase error is at its maximum. As a result, the phase error contains frequency components that are twice the frequency of the input signal.
- In addition, the magnitude of the phase error remained unchanged with different input signal frequencies. This although is a very interesting phenomenon, it does not imply that the resulting distortion of the output

signal is independent of the frequency of the input signal. The relationship between the phase error and the resulting output distortion is given in Eqn. (3.8) in Section 3.4.

- The duty cycle error seen in Figure 3.4(b) reaches its peak when the input signal in Figure 3.4(a) crosses the zero reference. This indicates that the mismatch between the rising-edge and falling-edge timing errors is at its maximum when the input signal crosses the zero reference. The magnitude of the duty cycle error increases with larger input signal frequency. This is consistent with the fact that the intrinsic harmonic distortion becomes more significant for high frequency input signal.

Figure 3.4 Phase and duty cycle errors with respect to different input frequencies: (a) phase error with input signal; and (b) duty cycle error.

The key frequency components of the phase and duty cycle errors corresponding to a 5-kHz input signal (as shown in Figure 3.4) are listed in Table 3.1. The table clearly reflects that the phase error comprises even order

harmonics whereas the duty cycle error involves the fundamental component and odd order harmonics.

Table 3.1 Frequency Components in Phase and Duty Cycle Errors.

Error source	Frequency components	Magnitude	Phase (Degree)
Phase error (rad)	2 nd -harmonic	0.16956	-1.83537
	4 th -harmonic	0.00106	-77.38772
Duty cycle error (s/s)	Fundamental	0.005315	-147.7
	3 rd -harmonic	7.7466E-4	-166.17815

The variations of the phase and duty cycle errors at different input magnitudes are shown in Figure 3.5. The input signal frequency was set to 5 kHz and the modulation index was varied from 0.1 to 0.9, and with a 0.2 step. From the comparison, we noted that when the input magnitude decreased, the lower peak of the phase error rose toward the higher peak and hence the magnitude of the 2nd-order harmonic inside the phase error diminished. At the same time, the duty cycle error became smaller and approached a sinusoidal wave. This implied that both the fundamental and 3rd-order harmonic frequency components would quickly vanish. These phenomena are consistent with the fact that the intrinsic harmonic distortion should become insignificant when the magnitude of the input signal decreases.

Figure 3.5 Phase and duty cycle errors with respect to different input signal magnitudes: (a) Phase error; (b) Duty cycle error.

3.4 Relationship between errors signals and output distortion

Having established the phase and duty cycle errors, the major distortion components contained in the demodulated output signal then can be calculated. The phase error behaves like a phase modulation on the ideal output PWM signal. Taking reference from [11], the distortion created by this mechanism can be approximated by the slope of the ideal output signal times the time displacement, which is a linear approximation to the phase modulation. The duty cycle error directly modulates the magnitude of the output signal and can therefore be translated to output distortion by multiplying by 2. Consequently, the generated distortion within the audible output signal can be calculated as follows:

$$E(t) = \theta_e(t) \cdot \frac{T}{2\pi} \cdot \frac{d}{dt} V_{out_ideal}(t) + 2D_e(t) \quad (3.8)$$

From Table 3.1, the most significant frequency component of the phase error is the 2nd-order harmonic of the input signal. Hence, the resulting error signal due to the phase error (i.e. 1st-term at the right hand side of Eqn. (3.8)) is a 3rd-order harmonic. In addition, since the duty cycle error comprises mainly the fundamental and 3rd-order harmonic of the input signal, the resulting error signal (i.e. 2nd-term at the right hand side of Eqn. (3.8)) introduces both the 3rd-order harmonic and the distortion on the fundamental frequency component. For instance, based on the data tabulated in Table 3.1, the 3rd-order harmonic distortion of the demodulated output signal can be calculated as follows:

$$H_{3rd} = \left| \begin{aligned} &0.1696 \cos\left(2\omega_{in}t - \frac{1.835}{180}\pi\right) \cdot \frac{T}{2\pi} \cdot \frac{d}{dt} \sin(\omega_{in}t) \\ &+ 2 \times 0.0007747 \cos\left(3\omega_{in}t - \frac{166.2}{180}\pi\right) \end{aligned} \right|_{@3\omega_n} \quad (3.9)$$

$$\approx 0.000517$$

In addition, the magnitude of the distorted fundamental component of the output signal is calculated to be equal to 0.70576. A comparison of the MATLAB simulation results, analytical results based on [3], and this work is compiled in Table 3.2. It is evident that the results derived from this work matches well with simulation and the analytical work [3] that was based on time-domain modeling technology. It is worthwhile to highlight that the 3rd-order harmonic distortion within the demodulated output signal is contributed by the phase and duty cycle errors, where both are equally important. This finding provides more insight than the previous works [11, 71] which reported that the 3rd-order harmonic distortion of a 2nd-order Class-D amp is mainly due to the duty cycle error.

Table 3.2 Comparison on Output Frequency Components.

	MATLAB Simulation	Time-domain analysis [3]	This work
Fundamental	0.7055	0.7058	0.70576
3 rd -harmonic	0.0005266	0.0005078	0.000517

3.5 Summary

The time domain waveforms of the phase and duty cycle errors were generated by comparing the closed-loop and open-loop PWM signals and with the help of the cubic spline interpolation. The waveforms created provide an insight to the mechanism of the intrinsic harmonic distortion of a closed-loop Class-D amplifier. The relationship between the error signals and the distortion inside the output signal is investigated. The results show that both the phase and duty cycle errors play collective roles in the 3rd-order harmonic, which is the most significant distortion component within the demodulated output signal of a 2nd-order Class-D amplifier.

Chapter 4 Time Domain Analysis on AD-modulated Class-D Amplifier

4.1 Introduction

In this chapter, a systematic analysis on the intrinsic distortion of the closed-loop AD-modulated Class-D amplifier is presented. The work is based on a precise time-domain mathematical analysis, where the system is defined and converted into mathematical models for simulating using MATLAB. With the mathematical model and the simulation data, a mathematical expression of the output signal is derived. This study is in collaboration with Professor Stephen M. Cox at University of Nottingham and most of the mathematical derivations are contributed by Prof. Cox. After arriving at the final expression, it is compared with MATLAB simulation results, circuit simulation results (using either HSPICE or Cadence Spectre) and the experimental results. A large portion of this chapter has been published in [3, 5].

This chapter is organized as follows. In Section 4.2, the major steps in analyzing the AD-modulation design are summarized, and an explicit amplifier output expression is derived. In Section 4.3, the closed-form expressions for intrinsic distortion, in the form of total harmonic distortion (THD) and intermodulation distortion (IMD) are derived and analyzed. In Section 4.4, the analytical results are compared with the amplifier simulation results, where an

excellent agreement had been arrived at. Finally, a summary is given in Section 4.5.

4.2 Mathematical analysis on AD-modulated closed-loop design

A typical AD-modulated closed-loop PWM-based Class-D amplifier with a single feedback path is illustrated in Figure 4.1, although the implementation of AD-modulation is not limited to the single-ended output configuration. The analysis results presented in this chapter is suitable for any Class-D amplifier that can be converted to the mathematical model depicted in Figure 4.2. The 2nd-order loop filter provides a high loop gain inside the audio band, and hence offers great attenuation of power supply noise and power stage nonlinearity.

Figure 4.1 Circuit schematic of a 2nd-order Class-D amplifier

Figure 4.2 depicts a generalized model of an AD-modulated closed-loop Class-D amplifier with either 1st-order or 2nd-order loop filter. The carrier signal $v(t)$ and the PWM output signal $g(t)$ are normalized to ± 1 in order to simplify the analysis; this normalization procedure does not affect the generality of the model. The feedforward path with a constant gain equal to $-k$ can be added to reduce the distortion of the fundamental output signal, although it is not shown

in Figure 4.1. The model parameters, c_1 and c_2 , and the input signal, $s(t)$, (indicated in Figure 4.2) are derived in Table 4.1, where the passive components and the signals are referred to the circuit schematic shown in Figure 4.1. Note that the two capacitors in Figure 4.1, C_1 and C_2 , are assumed to be of equal values, which is a common practice in commercial design [76]. For a 1st-order loop filter design, R_3 will be removed and the serial connected C_1 and C_2 can be represented by a single capacitor C_0 with value equal to $C_1/2$.

Figure 4.2 General mathematical model of a closed-loop Class-D amplifier

Table 4.1 Mathematical Model Parameters

	First order loop filter	Second order loop filter
c_1	$(\alpha / \beta) \cdot (1 / R_2 C_0)$	$(\alpha / \beta) \cdot (2 / R_2 C_1)$
c_2	0	$1 / (2 R_3 C_1)$
$s(t)$	$(R_2 / R_1) \cdot (v_{in}(t) / \alpha)$	

As a detailed time-domain modeling process will be presented in Chapter 5 when deriving the output expression of a BD-modulated Class-D amplifier, only a summary of the mathematical analysis process for AD-modulation is provided here to avoid duplication. The detailed derivation process can be found in [3]. The time-domain modeling process can be divided into three steps:

First, the switch-mode system is modeled using a set of nonlinear difference equations which relate the state of the circuit at successive switching instants. The state variables consist of the switching times of the PWM signal and the integrator outputs, $m(t)$ and $p(t)$, shown in Figure 4.2.

Next, a perturbation solution for the state variables based on a small parameter ε (i.e. $\varepsilon \equiv \omega T \ll 1$, where ω is a typical audio frequency and T is the carrier period) is derived. The accuracy of the solution is determined by the expansion order in ε , but the complexity of the solution also increases with the order of ε .

Finally, the audio-frequency contents, $g_a(t)$, is extracted from the PWM signal. The perturbation solution of the system states is then substituted into the $g_a(t)$ expression. The audible output components of closed-loop Class-D amplifiers with either 1st-order or 2nd-order loop filter are expressed in Eqns. (4.1) and (4.2), respectively. More details can be found in [3, 73].

$$\begin{aligned} g_{a_1st}(t) = & -s(t) - \frac{1}{48c_1^2} [48(1+k) - c_1^2 T^2] \frac{d^2}{dt^2} s(t) \\ & + \frac{1+k}{c_1} \cdot \frac{d}{dt} s(t) + \frac{T^2}{48} \frac{d^2}{dt^2} s^3(t) + O(\varepsilon^3) \end{aligned} \quad (4.1)$$

$$\begin{aligned} g_{a_2nd}(t) = & -s(t) + \frac{1}{24c_1c_2} [24(1-k) + c_1c_2 T^2] \frac{d^2}{dt^2} s(t) \\ & - \frac{T^2}{24} \frac{d^2}{dt^2} s^3(t) + O(\varepsilon^3) \end{aligned} \quad (4.2)$$

Equation (4.2) is interpreted as follows. The first term on the right-hand side of Eqn. (4.2) represents the desired input signal component contained in the output PWM signal, and will be referred to as the fundamental output component in the rest of the chapter. The minus sign is due to the feedback

topology design, which does not affect the linearity of the amplifier. The second term is proportional to the second derivative of the input signal. The third term is proportional to the second derivative of the cube of the input signal. The effect of the last two terms on the linearity of the amplifier will be examined in Section 4.3.

Note that the input signal in Eqns. (4.1) and (4.2) may be any arbitrary audio signal, and is not limited to a sinusoidal signal. The term $O(\varepsilon^3)$ represents the truncation error of the analytical expression. For instance, if the input signal frequency is 1 kHz and the carrier frequency is 250 kHz, then the analytical results in Eqns. (4.1) and (4.2) omit terms of the order $(2\pi/250)^3$, i.e., of the order 10^{-5} .

When comparing the expressions for the 1st-order and 2nd-order Class-D amps, it is worthwhile to highlight that the intrinsic harmonic components and the intermodulation products of the 2nd-order Class-D amplifier are exactly twice that of the 1st-order loop filter. This is confirmed in Section 4.4. In Section 4.3, only the output expressions of a 2nd-order Class-D amplifier with both single-tone and two-tone input signals will be derived.

4.3 Intrinsic distortion of a AD-modulated Class-D amplifier

4.3.1 Total harmonic distortion

In order to derive the expression of THD, the input signal $s(t)$ is substituted with a single-tone sinusoidal signal $s_0 \sin(\omega t)$, where s_0 is normalized magnitude of the input signal (from +1 to -1) and ω is the angular frequency of

the input signal. The output expression for the 2nd-order Class-D amplifier is obtained as shown in Eqn. (4.3) and can be interpreted as follows:

- The first term in Eqn. (4.3) represents the fundamental component, which is the demodulated input signal. The second term represents the distortion on the magnitude of the fundamental component.
- The third term in Eqn. (4.3) indicates that there exists third order harmonic distortion inside the output signal of 2nd-order Class-D amplifier. Since the output signal is derived based on ideal model of the 2nd-order Class D amplifier, the third order harmonic distortion is created due to the system itself and hence referred as intrinsic harmonic distortion.
- In addition, the 3rd-order harmonic distortion is independent on the loop filter parameters, c_1 and c_2 , and hence, they cannot be attenuated by increasing the loop gain. Furthermore, the 3rd-order harmonic is proportional to s_0^3 , ω^2 and T^2 , rendering it significant for high frequency and large input signal.

$$g_{a_2nd}(t) = -s_0 \sin(\omega t) + \left(\frac{k-1}{c_1 c_2} - \frac{T^2}{24} + \frac{1}{32} s_0^2 T^2 \right) s_0 \omega^2 \sin(\omega t) - \frac{3}{32} s_0^3 \omega^2 T^2 \sin(3\omega t) + O(\varepsilon^3) \quad (4.3)$$

Consequently, the THD expression of the 2nd-order Class D amplifier is derived as

$$THD_{2nd}(\%) = \frac{\frac{3}{32} s_0^2 \omega^2 T^2}{1 - \left(\frac{k-1}{c_1 c_2} - \frac{T^2}{24} + \frac{1}{32} s_0^2 T^2 \right) \omega^2} \approx \frac{3}{32} s_0^2 \omega^2 T^2 \quad (4.4)$$

It will be proven later in Section 4.4 that the distortion on the fundamental output signal can be ignored for input frequency less than 6 kHz. Its effect on THD is thus insignificant. The expression of THD in Eqn. (4.4) only accounts for the intrinsic harmonic distortion due to the switching output stage combined with negative feedback, which is proportional to the square of both magnitude and frequency of the input signal. Hence, the intrinsic harmonic distortion is the dominant THD component for large input signal and at high frequency. In addition, it is independent of the loop filter design, but could be considerably attenuated by increasing the carrier frequency.

It is instructive to examine the significance of the distortion on the magnitude of the fundamental component when the Class-D amplifier is designed for high fidelity application. The gain error from the operational amplifier with negative feedback as presented in Eqn. (4.5) is therefore introduced. It is defined as the percentage deviation of the gain from the ideal and is equivalent to the percentage deviation of the fundamental component from the ideal.

$$\text{Gain Error}(\%) = \frac{V_f - V_{f_ideal}}{V_{f_ideal}} \times 100 \quad (4.5)$$

Hence the expression of the gain error for 2nd-order Class-D amplifier is derived as

$$\text{Gain Error}_{2\text{nd}}(\%) = \left(\frac{1-k}{c_1 c_2} + \frac{T^2}{24} - \frac{T^2}{32} s_0^2 \right) \cdot \omega^2 \times 100 \quad (4.6)$$

Note that the gain error is proportional to the square of the angular frequency of the input signal and also dependent on the loop filter design as well as the carrier frequency. Without the feedforward path ($k = 0$), as we will show later in Section 5.4.1, the first term inside the parenthesis is the dominant term.

Hence, the magnitude of the fundamental output signal will be larger than expected, to result in a positive gain error and its effect should be analyzed with the load configurations. When the LC low-pass filter present, the intrinsic gain error is preferred, as its positive gain error can be used to partially compensate the gain reduction of the LC low-pass filter. For “filterless” Class-D amplifier, the intrinsic gain error may be a potential problem, as the external low-pass filter is not available, especially when the designers want to use lower switching frequency to enhance the power efficiency of their design. In summary, the design parameters that affect the gain error are listed as follows:

- Gain of the loop filter—The gain error can be reduced by increasing the gain of the loop filter. For instance, as will be discussed in Section 5.4.1, by increasing the loop filter gain by 6 dB, the gain error is almost reduced to half.
- The switching frequency—It is shown in Eqn. (4.6) that part of the gain error, i.e., $T^2(1/24 - s_0^2/32)$, is proportional to the period of the carrier signal and hence inverse proportional to the switching frequency. In addition, with higher switching frequency, the loop filter can be designed with a higher low frequency gain, to further reduce the gain error.
- Feedforward gain (i.e., k)—The gain error can be partially eliminated by setting the input signal feed-forward parameter k using Eqn. (4.7). The desired value for k should be independent of the input signal parameter, so that it eliminates only the fundamental distortion due to the 2nd-order derivation of the input signal, rather than that due to the 2nd-order derivation of the cubic of the input signal. Note that the desired value for

k is dependent on the loop filter gain and is larger than 1. This can be realized by either cascading a difference amplifier after the loop filter or adding an inverse input port at the comparator. A typical difference amplifier circuit can be found in [77]. The remaining distortion on the magnitude of the fundamental component is due to the nonlinear cubic distortion term, which is dependent on the input signal magnitude.

$$k = 1 + \frac{1}{24}c_1c_2T^2 \quad (4.7)$$

4.3.2 Intermodulation distortion

To derive the expression for IMD, the angular frequencies of the two input signals are first denoted as ω_1 and ω_2 , and the input signal is expressed as follows:

$$s(t) = s_1 \cdot \sin(\omega_1 \cdot t) + s_2 \cdot \sin(\omega_2 \cdot t) \quad (4.8)$$

where s_1 and s_2 are the magnitudes of the respective input frequency components. Consequently, the expression for $g_a(t)$ is derived in Eqn. (4.9).

Equation (4.9) is interpreted as follows. The first two terms on the right-hand side of Eqn. (4.9) represent the desired fundamental components. The third and fourth terms correspond to the 3rd-order harmonic distortion terms, which are the same as that derived based on a single tone input signal in Eqn. (4.3) and not affected by the other input signal up to the leading order of analytical expression. The fifth and sixth terms signify the distortion on the magnitude of the two fundamental components; such distortion is proportional to the square of the respective input signal frequency. Compared to the output expression in Eqn. (4.3) for a single-tone input signal, there exists an additional term in each

fundamental distortion expression, which is proportional to the squared magnitude of the other input signal. This indicates that there exists intermodulation on the magnitude of the fundamental output components. To the best of our knowledge, this is the first reported work to quantify this phenomenon. The last four terms stand for the third order intermodulation products (3rd-IMPs). An indication of the size of the truncation error involved in Eqn. (4.9) is given by $(\omega_1 \cdot T)^3$ or $(\omega_2 \cdot T)^3$.

$$\begin{aligned}
 g_{a_2nd}(t) = & -s_1 \sin(\omega_1 t) - s_2 \sin(\omega_2 t) \\
 & - \frac{3}{32} s_1^3 \omega_1^2 T^2 \sin(3\omega_1 t) - \frac{3}{32} s_2^3 \omega_2^2 T^2 \sin(3\omega_2 t) \\
 & + \left(\frac{(k-1)}{c_1 c_2} - \frac{1}{24} T^2 + \frac{1}{32} T^2 s_1^2 + \frac{1}{16} T^2 s_2^2 \right) \omega_1^2 s_1 \sin(\omega_1 t) \\
 & + \left(\frac{(k-1)}{c_1 c_2} - \frac{1}{24} T^2 + \frac{1}{32} T^2 s_2^2 + \frac{1}{16} T^2 s_1^2 \right) \omega_2^2 s_2 \sin(\omega_2 t) \\
 & + \frac{1}{32} s_1^2 s_2 T^2 (2\omega_1 - \omega_2)^2 \sin((2\omega_1 - \omega_2)t) \\
 & + \frac{1}{32} s_1 s_2^2 T^2 (2\omega_2 - \omega_1)^2 \sin((2\omega_2 - \omega_1)t) \\
 & - \frac{1}{32} s_1^2 s_2 T^2 (2\omega_1 + \omega_2)^2 \sin((2\omega_1 + \omega_2)t) \\
 & - \frac{1}{32} s_1 s_2^2 T^2 (\omega_1 + 2\omega_2)^2 \sin((\omega_1 + 2\omega_2)t)
 \end{aligned} \tag{4.9}$$

The characteristics of the 3rd-IMPs are summarized as follows:

- The 3rd-IMPs are proportional to the magnitude of the input signal with the power equal to the absolute value of the coefficient of the input frequency forming the frequency of the 3rd-IMPs. For instance, the magnitude of the 3rd-IMP at frequency $2\omega_1 - \omega_2$ is proportional to $s_1^2 s_2$, whereby its power factors (i.e., 2 for s_1 and 1 for s_2) are equal to the absolute coefficients of ω_1 and ω_2 that form the frequency of the 3rd-IMP, $2\omega_1 - \omega_2$, which is again 2 for ω_1 and 1 for ω_2 .

- The IMPs are inversely proportional to the square of the carrier frequency. Thus, increasing the carrier frequency can dramatically reduce IMD. However, the power efficiency of the amplifier will drop with the increased carrier frequency.
- Unfortunately, the IMPs are independent of the loop filter parameters and cannot be attenuated by adjusting the location of the zero and DC gain. As this result disagrees with the conclusion of [72], an analysis on its correctness is provided below in the next paragraph and further verification through hardware testing is given in Section 4.5.

Figure 4.3 illustrates the MATLAB simulation results of the significant 3rd-IMPs when the loop filter parameter c_2 of a 2nd-order Class-D amplifier reduces from a typical value to 0. It confirms that in a broad range, the IMPs are almost independent of the loop filter parameter. Of course, it should be borne in mind that when the zero of the 2nd-order loop filter is shifted to the origin (i.e., the limiting case of $c_2 = 0$ as indicated by the linearized loop gain transfer function, $c_1(s+c_2)/s^2$), the intrinsic intermodulation distortion should converge with that of the 1st-order Class-D amplifier and be reduced by half, as demonstrated in Figure 4.3. This also means that the IMD is not completely independent of the loop filter design. Unfortunately, it is not possible to predict the convergence from a 2nd-order Class-D amplifier to a 1st-order Class-D amplifier using the expressions in this paper. This is because the derivation of Eqn. (4.2) relies on fixed nonzero c_1 and c_2 values, which is clear from the presence of both these parameters in the denominator of the second term in Eqn. (4.2). Put more abstractly, Eqn. (4.9) provides an excellent approximation for “genuinely

second order amplifiers”, i.e., when $c_1T = O(1)$ and $c_2T = O(1)$, but it gives a much poorer approximation for amplifiers that are “nearly first order”.

Figure 4.3 Intermodulation products of a 2nd-order Class-D amplifier versus the loop filter parameter c_2 . The input signal is set with $f_1 = 60$ Hz, $f_2 = 7$ kHz, $M_1 = 0.7$ and $M_2 = 0.175$.

From circuit analysis, there are two contrary effects when we adjust the loop filter parameters. On one hand, when we increase c_1 or c_2 to enhance the linearized loop gain, the low-frequency audible error between the input signal and output PWM signal is further suppressed, just like any linear system. On the other hand, the increase of c_1 and c_2 creates larger phase and duty cycle errors in the PWM signal during the modulation process through altering the waveform of the high frequency ripple signal at the output of the loop filter. The second effect is the root of the difference when applying negative feedback to a switch-mode system as compared with a linear system. As demonstrated in [11] when deriving the total harmonic distortion of a closed-loop Class-D amplifier, the duty cycle error is proportional to the real part whereas the phase error is proportional to the imaginary part of the loop filter transfer function.

The counterbalance of these two effects in a typical 2nd-order Class-D amplifier causes IMD to be almost independent of the loop filter design.

Since the expression for the output signal is derived based on an ideal model of the 2nd-order Class-D amplifier, the derived intermodulation products are produced intrinsically due to the negative feedback applied to the nonlinear pulse width modulator. Finally, the IMD expression of the 2nd-order Class-D amplifier is derived in Eqn. (4.10), which reflects that IMD of the 2nd-order Class-D amplifier is independent of the design of the loop filter, and instead, it is determined by the frequency and amplitude of the input signals, and also the carrier frequency. Note that the slight distortion on the fundamental component is ignored so as to simplify the expression without notably affecting the precision.

$$IMD_3(\%) \approx \frac{1}{32} s_1 T^2 \sqrt{s_1^2 (32\omega_1^4 + 48\omega_1^2 \omega_2^2 + 2\omega_2^4) + s_2^2 (32\omega_2^4 + 48\omega_1^2 \omega_2^2 + 2\omega_1^4)} \times 100 \quad (4.10)$$

Figure 4.4 shows the output spectrum of a 2nd-order Class-D amplifier with a two-tone stimulus signal of 5 kHz and 6 kHz. The amplitudes of the two sinusoidal input signals are both equal to 0.3. The first pair of 3rd-IMPs are located to either side of the fundamental components, i.e., at frequencies equal to $2f_1 - f_2$ and $2f_2 - f_1$, and the other pair of 3rd-IMPs are located between the two 3rd-order harmonics, i.e., at frequencies equal to $2f_1 + f_2$ and $2f_2 + f_1$. Note that the latter two 3rd-IMPs are even larger than the 3rd-order harmonics of the input signals. This demonstrates that the IMD may have a greater impact on the linearity of a closed-loop PWM-based Class-D amplifier than the harmonic distortion.

Figure 4.4 Output spectrum of a 2nd-order Class-D amplifier with two 0.3 V sinusoidal input signals that are of $f_1 = 5$ kHz and $f_2 = 6$ kHz, respectively.

The accuracy of the mathematical expression is verified by comparing the analytical results and the MATLAB simulation results as shown in Figure 4.5. The results are in good agreement with each other across the modulation index range. The input signals are set with $f_1 = 60$ Hz, $f_2 = 7$ kHz and $M_2 = M_1/4$, which are a typical SMPTE testing setup that will be further explained in Section 4.4. As illustrated in Figure 4.5, the analytical results precisely predict the magnitudes of all the significant frequency components—the two fundamental components in Figure 4.5(a) and Figure 4.5(b) and the four 3rd-IMPs (see Figure 4.5(c)—(f)) with varying M_2 setting (ranging from 0.025 to 0.175).

Figure 4.5 Matching between analytical and MATLAB simulation results for all significant frequency components in a typical SMPTE test: (a)-(b) the two fundamental frequency components; (c)-(f) the four 3rd-IMPs.

4.4 Analytical, simulation and measurement results

In this section, the analytical derivations are verified by comparing the derived expressions against MATLAB simulation, HSPICE simulation, and also experimental measurements on a Class-D amplifier built on PCB using discrete components as shown in Figure 4.6. As the HSPICE models for some components are not available from the companies' website, the Spice models used in our HSPICE simulation are created based on the specifications on the datasheets and only the main parameters were considered. In addition, both 1st-order and 2nd-order loop filter designs are tested using this board by inserting or removing the resistor, R_3 , shown in Figure 4.1.

Figure 4.6 Hardware implementation for IMD testing.

Furthermore, in order to verify the effect of the loop gain parameters on the intrinsic distortions, two different 2nd-order loop filters (Design I and II) have been tested. The loop filter design parameters are tabulated in Table 4.2 and the respective linearized loop gains are plotted in Figure 4.7. Note that the feedforward gain k in Figure 4.2 is equal to 0 for all the loop filters used here. The output low-pass filter is designed as $L = 33 \mu\text{H}$, $C = 0.242 \mu\text{F}$ and $R_L = 8 \Omega$. In the absence of specification to the contrary, the carrier switching frequency

is set to 250 kHz by default. Note that the 2nd-order loop filter with Design II parameters achieved a 6 dB higher low-frequency gain as compared to that with the Design I parameters recommended in [57].

Table 4.2 Model Parameters of Different Loop Filter Designs.

Parameter	2 nd -order Design I [57]	2 nd -order Design II	1 st -order Design
c_1	4.3301e5	4.988e5	4.988e5
c_2	2.8868e5	4.9034e5	0

Figure 4.7 Plots of linearized loop gains of the closed-loop Class-D amplifiers based on different loop filter designs provided in Table 4.2.

4.4.1 Verification of total harmonic distortion

The verification on total harmonic distortion presented in this subsection is based on a 2nd-order Class-D amplifier. Design II parameters stated in Table 4.2 is used in default for the loop filter design. In the hardware measurement presented in this subsection, audio analyzer from Rohde & Schwartz is used which integrates both signal generator and analyzer functions.

Figure 4.8 plots the THD against input frequency predicted by Eqn. (4.4) and that obtained from simulations and on the basis of measurements for the 2nd-order Class-D amplifier at $M = 0.7$ and $f_c = 250$ kHz. The frequency range of the input signal is from 1 kHz to 6 kHz, as for signal of below 1 kHz, the harmonic distortion due to the negative feedback is not significant, and for signal of above 6 kHz, the 3rd harmonic is out of the audio range. The derived analytical results agree well with the simulation and measurement results, which verified the precision of the analytical output signal expression. As expected, the THD of 2nd-order Class D amplifier is proximately proportionally to the square of the input frequency.

Figure 4.8 THD vs. input frequency at $M = 0.7$ and $f_c = 250$ kHz.

Figure 4.9 plots the THD against modulation index predicted by Eqn. (4.4) and that obtained from simulations and measurements, for the 2nd-order Class-D amplifier at $f_{in} = 6$ kHz and $f_c = 250$ kHz. The simulation results agree well with the analytical results. It shows that the THD increases considerably with the modulation index of the input signal and is proportional to the square of the

modulation index. The measurement results agree well with the analytical results.

Figure 4.9 THD vs. Modulation index at $f_{in} = 6$ kHz, $f_c = 250$ kHz.

Figure 4.10 depicts the gain error against the input signal frequency of two 2nd-order Class-D amplifier with Design I and Design II parameters stated in Table 4.2. The modulation index of the input signal is set to 0.3. The simulation results are compensated with the respected attenuation of the demodulation low-pass filter. It shows that the analytical results agree well with both Matlab and HSPICE simulation results, and hence verifying the prediction on the fundamental distortion. It also proved that the gain error increases considerably with input signal frequency and is up to 13% at 20 kHz for loop filter Design I. With loop filter Design II (has 6 dB higher loop gain at low-frequency), the gain error is reduced by half. Recall that for a practical Class-D amplifier with LC low-pass filter, the gain error may be preferred as it partially compensates the gain drop of the low-pass filter at high frequency.

Figure 4.10 Gain error vs. input signal frequency at $M = 0.3$ and $f_c = 250$ kHz.

4.4.2 Verification of intermodulation distortion

The most common IMD measurement standard in the professional, broadcast, and consumer audio fields is set by the Society of Motion Picture and Television Engineers (SMPTE) and is referred to as the SMPTE method; it uses a two-tone test signal consisting of a low-frequency high-amplitude tone (60 Hz) linearly combined with a high-frequency tone (7 kHz) at 1/4 the amplitude (−12 dB) of the low-frequency tone [40]. In the hardware measurement for IMD, the National Instrument equipments combined with its provided NI Sound and Vibration Measurement Suite are used.

Figure 4.11 depicts the frequency spectrum of the output signal in a typical SMPTE IMD test in MATLAB simulation. In this case, the intermodulation products are located at the sidebands of the high-frequency tone and its harmonics, which are the 3rd-IMPs at $f_2 \pm 2f_1$ and $2f_2 \pm f_1$. Note that although the spectrum lacks 2nd-order harmonic component (i.e., at 14 kHz), IMPs around the second harmonic do exist. In addition, Figure 4.11 also demonstrates that

there are no 2nd-IMPs, and hence corroborates the prediction based on Eqn. (4.9).

Figure 4.11 Output spectrum of a 2nd-order Class-D amplifier with two sinusoidal input signals of 60 Hz and 7 kHz, with amplitudes of 0.5 V and 0.125 V, respectively.

The SMPTE IMD of the 2nd-order Class-D amplifier is plotted against the modulation index of the high-frequency input component in Figure 4.12. To ensure that the combined input magnitude is less than 1, the modulation index of the 60-Hz input signal varies from 0.1 to 0.7 and the modulation index of the 7-kHz input signal varies from 0.025 to 0.175, respectively. The loop filter deployed in the amplifier is designed using the Design I parameters stated in Table 4.2.

Figure 4.12 SMPTE IMD of the 2nd-order Class-D amplifier versus the modulation index of the 7 kHz input signal with loop filter Design I.

As evident in Figure 4.12, the analytical results agree well with the two simulation outcomes, derived from MATLAB and HSPICE. Furthermore, the IMD is proportional to the square of the modulation index of the high frequency input tone. This can be explained using Eqn. (4.10) by substituting s_1 with $4 \cdot s_2$. The measurement results have the same increasing trend as the analytical results. The mismatch between the simulation and the measurement results is probably due to the non-ideality of the power MOSFETs and the nonlinearity of the decoupling LC filter. This was investigated through an experiment in which the LC filter and the 8- Ω load are replaced by a 3rd-order RC filter with an almost identical cut-off frequency. As the RC filter draws much less current than the LC filter with a resistive load, the effect of the on-resistance can be ignored and the PWM waveform at the output of the power stage achieves sharper rising and falling edges. It is interesting to note that by replacing the LC filter with the RC filter, the non-ideality of the power stage is also minimized. As shown in Figure 4.12, the measured IMD under such conditions (i.e. the purple dash-dot line with star symbols) is much closer to the analytical result as

compared to that with the LC filter (i.e. the blue solid line with diamond symbols). Through this experiment, it is reasonable to conclude that the discrepancy between the measurement results and the analytical results is mainly due to the non-idealities of the power stage and the output filter. A comprehensive analysis on the non-ideality of the power stage was reported in [78]. Figure 4.12 also reveals that by appropriately choosing the inductor and capacitor, and also using well-designed power MOSFETs, the intermodulation distortion of a 2nd-order Class-D amplifier is dominated by the intrinsic IMD, especially when the input signal is large.

After modifying the 2nd-order loop filter based on the Design II parameters provided in Table 4.2, a 6 dB higher loop gain is achieved. The IMD versus modulation index of the high-frequency tone is re-plotted in Figure 4.13 using this modified loop filter. The simulation results match the analytical results and remain unchanged as compared to that seen in Figure 4.12. Hence, we have verified that the intrinsic IMD is independent of the loop filter design. This is a very important characteristic of both the intrinsic harmonic distortion and intermodulation distortion. Furthermore, the measured IMD in Figure 4.13 is noted to be smaller than that of Figure 4.12. This is attributed to the additional suppression of the non-ideality effect of the power stage, due to the increased linearized loop gain.

Figure 4.13 SMPTE IMD of the 2nd-order Class-D amplifier versus the modulation index of the 7 kHz input signal with loop filter Design II.

Figure 4.14 illustrates the IMD performance of a 1st-order Class-D amplifier. The 1st-order loop filter is realized by removing resistor R_3 from the 2nd-order loop filter using Design II parameters. Comparing with the results of the 2nd-order Class-D amplifier shown in Figure 4.13, the simulated IMD of the 1st-order Class-D amplifier is reduced by half and matches well with the analytical results. However, there exists significant mismatch between the measurement results and the simulation results. This is mainly due to the much lower loop gain of the 1st-order Class-D amplifier where it is unable to sufficiently attenuate the distortions introduced by the practical power stage. This is also reflected in the HSPICE simulation results when the input signal is small. As the intrinsic distortion reduces quadratically with the decreasing magnitude of the input signal, the power stage distortion becomes the dominant factor that determines the linearity of the Class-D amplifier and cannot be predicted by Eqn. (4.10). Consequently, the deviation between the analytical results and HSPICE simulation results becomes larger at small modulation index. It may be

worthwhile to highlight that the loop gain of the first-order Class-D amplifier has been maximized based on the constraint to prevent multiple switching in each carrier period. A detailed analysis on the loop filter design constraints will be provided later in Chapter 6, under Section 6.2.

Figure 4.14 SMPTE IMD of a 1st-order Class-D amplifier versus the modulation index of the 7 kHz input signal.

As a short summary, although a 1st-order Class-D amplifier can achieve a lower intrinsic IMD, its overall performance may be worse than that of a 2nd-order Class-D amplifier. Hence, to achieve a good overall performance, a 2nd-order loop filter is always preferred and the gain of the loop filter inside the audio band should be as high as possible. Furthermore, in order to improve the linearity of a closed-loop pulse-width modulated Class-D amplifier, more research on the circuit structure should be established; some relevant work has been reported in [68, 73]. In the rest of this section, all the verifications are based on the 2nd-order loop filter with Design II parameters, which manages to achieve a maximized attenuation of the non-ideality of the power stage and

supply noise, hence yielding more accurate results on the intrinsic IMD of the closed-loop Class-D amplifier.

Figure 4.15 illustrates the IMD performance of a 2nd-order Class-D amplifier versus the frequency of the low-frequency tone inside the two-tone input signal, i.e. from 60 Hz to 6 kHz, while fixing the high-frequency tone at 7 kHz. This test is used to examine the relationship between the magnitude of the IMPs and the frequencies of the input signal. As illustrated in Figure 4.15, the analytical results are noted to match well with the simulation and measurement results. It is also worthwhile to highlight that when the low-frequency input signal shifts towards the high-frequency tone, the intermodulation distortion increases significantly.

Figure 4.15 SMPTE IMD versus f_1 for 2nd-order Class-D amplifier with Design II parameters at $M_1 = 0.5$, $M_2 = 0.125$ and $f_2 = 7$ kHz.

Figure 4.16 demonstrates the relationship between the carrier switching frequency of the Class-D amplifier and the IMD. The input signal has the following settings: $f_1 = 60$ Hz, $f_2 = 7$ kHz, $M_1 = 0.7$ and $M_2 = 0.175$. Note that the IMD decreases dramatically with increasing switching frequency, similar to

the THD, and the analytical results accurately predict the trend of the rapid diminishing of the intermodulation distortion. As the loop filter Design II parameters used in the test were optimized based on a typical carrier frequency of 250 kHz, when the carrier frequency is reduced to 200 kHz, the output of the pulse width modulator may fail to switch inside a carrier period. This phenomenon has been explained in [3] as "pulse skipping", which is similar to the "fast-scale" instability issue described in [79, 80] for DC-DC converters. The criterion for preventing the occurrence of the pulse skipping has been derived in [3] and is reproduced here as $c_1 c_2 T^2 < 4$. The occurrence of pulse skipping will raise the noise floor of the output signal and cause extra distortions that cannot be predicted based on Eqn. (4.9) (shown as mismatch between the analytical result and simulation results at 200 kHz). However, since a properly designed Class-D amplifier will not have the pulse skipping issue, the small mismatch noted here is not a concern.

Figure 4.16 IMD versus switching frequency of a 2nd-order Class-D amplifier.

Another testing standard known as the "ITU-R" or "CCIF" method is also widely used by some manufacturers. This method was originally recommended

by the Consultative Committee for International Telephone (CCIF), which later became the Radio communications sector of the International Telecommunications Union (ITU). The stimulus signal for this intermodulation distortion test consists of two equal-amplitude high frequency signals that are spaced rather close together in frequency. Common signal frequencies are: 13 kHz and 14 kHz for 15 kHz band-limited systems, and 19 kHz and 20 kHz for systems with a full audio bandwidth. For the often seen case of the 19 kHz and 20 kHz test, only the 1 kHz component is measured, which is the 2nd-IMP at frequency equal to $f_2 - f_1$.

Figure 4.17 illustrates the output spectrum of a 2nd-order Class-D amplifier in the ITU-R test based on MATLAB simulation. The Class-D amplifier achieves an excellent IMD performance in the ITU-R test when only the 1 kHz IMP is counted. This is because the 2nd-order intermodulation products of a Class-D amplifier are usually negligible. However, this does not mean that Class-D amplifiers have good rejection on intermodulation distortion. As seen in Figure 4.17, the most significant IMP within the audio band is at 18 kHz (i.e. the 3rd-IMP at $2 \cdot f_1 - f_2$). Hence, we conclude that the traditional ITU-R test is not suitable for evaluating the performance of Class-D amplifiers.

Figure 4.17 ITU-R IMD MATLAB simulation result for $f_1 = 19$ kHz, $f_2 = 20$ kHz, $M_1 = M_2 = 0.45$ based on Design II parameters.

In [5], the candidate has proposed a modified testing setup that uses two input signals at the middle-band of the audio range, such as 5 kHz and 6 kHz signals, with equal modulation index. The output spectrum is as previously depicted in Figure 4.4, which showed that the main 3rd-IMPs are located alongside the fundamental components and in between the two 3rd-order harmonics. Figure 4.18 demonstrates the IMD performance of a 2nd-order Class-D amplifier with input signals set at 5 kHz and 6 kHz, each with equal modulation index that sweeps from 0.1 to 0.45. This test clearly reflects the rapid increase of the IMD with respect to the magnitudes of the input signals.

Figure 4.18 IMD versus modulation index for modified ITU-R test with $f_1 = 5$ kHz, $f_2 = 6$ kHz, $M_1 = M_2$ and Design II parameters.

4.5 Summary

In this chapter, we introduced a time-domain analysis technique that is able to precisely predict the intrinsic distortion of an AD-modulated Class-D amplifier in terms of THD and IMD. The essential mathematical tool for this calculation is a perturbation method based on the small ratio between typical audio frequencies and the amplifier switching frequency. The advantages of this technique are: 1) the output signal is obtained analytically for any band-limited input signal, in a compact form, 2) the derivation procedure is systematic and hence the analytical expression can in principle be obtained to any desired precision, and 3) the order of magnitude of the errors that arise from computing only the first few terms in the perturbation expansion can be estimated.

The derived expressions are simple, accurate and clearly reflect the relationship between the input signal, carrier frequency and the intrinsic distortion components. Compared to previous reported work [72], the derived

expressions are much simpler and more precise. Furthermore, they do not involve complicated Bessel functions, and hence allow hand calculation.

The analytical results demonstrate that although negative feedback can reduce the distortion due to the non-ideality of the power stage, it can cause significant undesired odd-order intrinsic harmonic components under a single-tone stimulus, and even larger intrinsic intermodulation products under a two-tone input signal. Furthermore, it shows that a Class-D amplifier with 1st-order loop filter has an intrinsic distortions half that of the 2nd-order loop filter. Nevertheless, for a broad range of parameters, the intrinsic distortion is independent of the parameters of a fixed loop filter structure.

Chapter 5 Time Domain Analysis on BD-modulated Class-D Amplifier

5.1 Introduction

In this chapter, the time domain analysis technique presented in Chapter 4 is extended to the fully differential BD-modulated closed-loop Class-D amplifier. Due to the ternary stage of the output signal, the analytical work is even more complex than previous treatments, involving much heavy algebra, which is relegated to a computer algebra package. The value of this analysis is that it yields a closed-form expression for the audio-frequency components of the amplifier output, which allows us to investigate the unique properties of the BD modulation. To our knowledge, this is the first analytical work on the output spectrum of BD modulation, although it was first introduced in the 1970s and has been widely used for audio amplifiers for nearly one decade.

A large part of this chapter is extracted from the candidate's collaboration work with Professor Cox [4], with whom the mathematical analysis work was developed. With the permission from Professor Cox, the candidate has included the mathematical work in this thesis to make it complete and convenient for reading.

Figure 5.1 demonstrates a popular circuit structure of a 2nd-order Class-D amplifier with BD modulation. The output stage is differential-ended and the carriers of both bridge halves are in-phase, whereas the modulating signals are

generated from a fully-differential 2nd-order loop filter and hence have opposite phase. The optional output *LC* filter is omitted, as it does not affect the analysis presented in this work. Fully-differential loop filters have been widely deployed in the recent works [48, 67, 81, 82], and it should be noted that their implementations are not limited to the structure shown in Figure 5.1. The 2nd-order loop filter may consist of two 1st-order integrators, as demonstrated in [81], and the input resistors can be replaced by a differential operational transconductance amplifier (OTA) [82].

Figure 5.1 Circuit schematic of a fully differential BD-modulated Class-D amplifier.

Note that there are some reported BD-modulated Class-D amplifiers that are built using pseudo-differential loop filters, where two single-ended loop filters are employed, one for each bridge half. Consequently, the circuit is exactly a combination of two single-ended AD modulated Class-D amplifiers. The audible frequency components of such pseudo-differential BD modulation are therefore the same as those of AD modulation, except that the output swing is

doubled. Hence, it is the interest of this chapter to evaluate the BD-modulated Class-D amplifiers with fully-differential loop filter.

This chapter is organized as follows. In Section 5.2, the major steps in analyzing the BD-modulation design are summarized, and an explicit amplifier output expression is derived. In Section 5.3, the closed-form expressions for the intrinsic distortion, in the form of total harmonic distortion (THD) and intermodulation distortion (IMD) are derived and analyzed. The analytical results are compared with the simulation results in Section 5.4, and lastly, a summary is provided in Section 5.5.

5.2 Mathematical analysis of BD modulation

Figure 5.2 shows the mathematical model that is derived for the BD-modulated Class-D amplifier illustrated in Figure 5.1. As in the previous chapter, a constant gain block (i.e., equal to $-k$) is added to the mathematical model to represent a feedforward path from the input signal to the loop filter output signal. Although this feedforward path is not shown in Figure 5.1, it can be easily realized by creating an extra input port at each comparator. In addition, this model is suitable for both the first-order (i.e., $c_2 = 0$) and second-order (i.e., $c_2 > 0$) loop filter designs. In this work, focus has been on the second-order loop filter design since it provides a higher linearized loop gain to significantly suppress the distortion caused by the power stage. For completeness, the output expression for the first-order design is also provided at the end of this section. The expressions for the model parameters c_1 and c_2 , and the input signal, $s(t)$,

(all indicated in Figure 5.2) are given in Table 5.1, where the passive components and the signals refer to the circuit schematic shown in Figure 5.1.

Figure 5.2 Fully differential BD-modulated Class-D amplifier with negative feedback and BTL output configuration.

Table 5.1 Mathematical model parameters.

Model Parameter	Expression
c_1	$(V_{DD}/V_T)(1/(R_2C_1))$
c_2	$1/(2R_3C_1)$
$s(t)$	$(R_2/R_1)(1/V_{DD})V_{in}(t)$

5.2.1 Formulation of model

The input to the device is an audio signal, $s(t)$, of relatively low frequency. Throughout this chapter, the voltages are scaled so that $s(t)$ lies in the range, $-1 < s(t) < 1$. The amplifier output is a high-frequency square-wave PWM signal, $g(t)$, taking the values -1 , 0 and 1 . As illustrated in Figure 5.2, the signals, $s(t)$ and $g(t)$, are summed and this sum is then integrated twice, in succession, yielding signals, $m(t)$ and $p(t)$, which satisfy

$$\frac{dm(t)}{dt} = -c_1(s(t) + g(t)), \quad \frac{dp(t)}{dt} = c_2 m(t), \quad (5.1)$$

where c_1 and c_2 are positive constants.

Next, $m(t)$ and $p(t)$ are summed with a multiple of the original audio signal, $-k \cdot s(t)$, and with a high-frequency triangular carrier wave $v(t)$ of period T ; this sum is fed to the non-inverting input of a comparator, whose inverting input is at zero volts. The carrier wave is given by

$$v(t) = \begin{cases} 1 - 4t/T & \text{for } 0 \leq t < \frac{1}{2}T, \\ -3 + 4t/T & \text{for } \frac{1}{2}T \leq t < T, \end{cases} \quad (5.2)$$

together with the periodicity condition $v(t+T) = v(t)$. The comparator output voltage is given by

$$u(t) = \begin{cases} +1/2 & \text{if } m(t) + p(t) - ks(t) + v(t) > 0, \\ -1/2 & \text{if } m(t) + p(t) - ks(t) + v(t) < 0. \end{cases} \quad (5.3)$$

In addition, the sum $m(t) + p(t) - k \cdot s(t)$ is inverted, added to the carrier wave and fed to a second comparator, whose output is given by

$$w(t) = \begin{cases} +1/2 & \text{if } -(m(t) + p(t) - ks(t)) + v(t) > 0, \\ -1/2 & \text{if } -(m(t) + p(t) - ks(t)) + v(t) < 0. \end{cases} \quad (5.4)$$

The output of the amplifier is given by $g(t) = u(t) - w(t)$:

$$g(t) = \begin{cases} +1 & \text{if } |v(t)| < m(t) + p(t) - ks(t), \\ 0 & \text{if } -|v(t)| < m(t) + p(t) - ks(t) < |v(t)|, \\ -1 & \text{if } m(t) + p(t) - ks(t) < -|v(t)|. \end{cases} \quad (5.5)$$

Finally, this output is fed back to the input of the amplifier, providing negative feedback.

Figure 5.3 shows the typical waveform of the output differential PWM signal, $g(t)$, corresponding to a sinusoidal input signal, $s(t)$. Note that $g(t)$ switches

between -1 and 0 when $s(t) > 0$, and between 0 and 1 when $s(t) < 0$. A zoomed-in view of the internal control signals ($\pm h(t)$ and $v(t)$) and the two comparator output signals ($u(t)$ and $w(t)$) is illustrated in Figure 5.4 for the time interval from 0.15 ms to 0.16 ms of Figure 5.3. These figures show that $u(t)$ and $w(t)$ each switch twice during one carrier-wave period, with $g(t)$ switching correspondingly four times. The times at which the comparator outputs switch between the values $\pm 1/2$ are denoted as A_n, B_n, C_n and D_n , for integers n , where $nT < A_n, B_n, C_n, D_n < (n+1)T$. More specifically,

$$u(t) = \begin{cases} +1/2 & \text{for } B_{n-1} < t < A_n, \\ -1/2 & \text{for } A_n < t < B_n \end{cases} \quad (5.6)$$

and

$$w(t) = \begin{cases} +1/2 & \text{for } D_{n-1} < t < C_n, \\ -1/2 & \text{for } C_n < t < D_n. \end{cases} \quad (5.7)$$

Figure 5.3 Waveforms base on typical operation of the amplifier. Note that the amplifier output $g(t)$ alternates between 0 and -1 when $s(t) > 0$ and between 1 and 0 when $s(t) < 0$.

Figure 5.4 Waveforms for typical operation of the amplifier.

In writing Eqns. (5.6) and (5.7), a normal operation is assumed, i.e., that each comparator switches twice during each carrier-wave period, as observed in simulations. Note that for sufficiently large signal amplitudes, occasional pulses may be skipped in some other Class-D amplifier designs, leading to a degradation in performance; however, we have not observed pulse-skipping in the present design. A discussion of the “large-signal” stability of an AD-modulated Class-D amplifier can be found in [3].

It proves useful to introduce the fractional switching times α_n , β_n , γ_n and δ_n , given by $A_n = (n + \alpha_n)T$, $B_n = (n + \beta_n)T$, $C_n = (n + \gamma_n)T$, $D_n = (n + \delta_n)T$, where

$$0 < \alpha_n < \frac{1}{2} < \beta_n < 1, \quad 0 < \gamma_n < \frac{1}{2} < \delta_n < 1. \quad (5.8)$$

Finally, in view of the need to integrate the input signal twice (See Eqn. (5.1)), we introduce $f(t)$ such that $s(t) = f''(t)$.

5.2.2 Construction of the equations

The present BD modulation design is more complicated to analyze than previously considered AD modulation designs [3]. In part this is because the output $g(t)$ switches four times per carrier-wave period. However, the more significant complication, for the mathematical model, is that the relative *order* of the switching of $u(t)$ and $w(t)$ differs, depending on the sign of $s(t)$. A detailed analysis for the case $s(t) > 0$ is presented below, for which the order of switching is

$$\cdots < A_n < C_n < D_n < B_n < A_{n+1} < \cdots. \quad (5.9)$$

For the case $s(t) < 0$, the order of switching is $\cdots < C_n < A_n < B_n < D_n < A_{n+1} < \cdots$ and consequent modifications to the account below are readily worked out.

The details of the calculation are highly algebraically involved, and it is useful to highlight the structure of the calculation, as follows. First, we integrate Eqn. (5.1) from $t = A_n$ to $t = A_{n+1}$, across each of the subintervals indicated in Eqn. (5.9), noting that $g(t)$ is constant in each subinterval; specifically,

$$g(t) = \begin{cases} -1 & \text{for } A_n < t < C_n \text{ or } D_n < t < B_n, \\ 0 & \text{otherwise.} \end{cases} \quad (5.10)$$

Thus, we obtain

$$\begin{aligned}
 m(C_n) &= m(A_n) - c_1(f'(C_n) - f'(A_n)) + c_1(C_n - A_n), \\
 p(C_n) &= p(A_n) + c_2m(A_n)(C_n - A_n) - F(A_n, C_n) \\
 &\quad + \frac{1}{2}c_1c_2(C_n - A_n)^2, \\
 m(D_n) &= m(C_n) - c_1(f'(D_n) - f'(C_n)), \\
 p(D_n) &= p(C_n) + c_2m(C_n)(D_n - C_n) - F(C_n, D_n), \\
 m(B_n) &= m(D_n) - c_1(f'(B_n) - f'(D_n)) + c_1(B_n - D_n), \\
 p(B_n) &= p(D_n) + c_2m(D_n)(B_n - D_n) - F(D_n, B_n) \\
 &\quad + \frac{1}{2}c_1c_2(B_n - D_n)^2, \\
 m(A_{n+1}) &= m(B_n) - c_1(f'(A_{n+1}) - f'(B_n)), \\
 p(A_{n+1}) &= p(B_n) + c_2m(B_n)(A_{n+1} - B_n) - F(B_n, A_{n+1}),
 \end{aligned}$$

where $F(t_1, t_2) = c_1c_2(f(t_2) - f(t_1) - f'(t_1)(t_2 - t_1))$.

It is then straightforward, if algebraically messy, to eliminate the intermediate values of m and p and hence obtain difference equations, of the form

$$m_{n+1} = M(n, m_n, p_n, \alpha_n, \beta_n, \gamma_n, \delta_n, \alpha_{n+1}), \quad (5.11)$$

$$p_{n+1} = P(n, m_n, p_n, \alpha_n, \beta_n, \gamma_n, \delta_n, \alpha_{n+1}), \quad (5.12)$$

where m_n denotes $m(A_n)$ and p_n denotes $p(A_n)$.

The switching times are determined, according to Eqns.(5.3), (5.4), (5.6) and (5.7), from

$$m(A_n) + p(A_n) - ks(A_n) + 1 - 4\alpha_n = 0, \quad (5.13)$$

$$m(B_n) + p(B_n) - ks(B_n) - 3 + 4\beta_n = 0, \quad (5.14)$$

$$-m(C_n) - p(C_n) + ks(C_n) + 1 - 4\gamma_n = 0, \quad (5.15)$$

$$-m(D_n) - p(D_n) + ks(D_n) - 3 + 4\delta_n = 0. \quad (5.16)$$

The six equations (5.11)–(5.16) constitute a set of governing difference equations for the amplifier. They can be used as the basis for accurate numerical simulations of the amplifier (cf. [79, 80]), but, more importantly,

they can be used to predict a closed-form expression for the audio output of the amplifier in response to a general audio input, as we now demonstrate.

5.2.3 Solving the model

The key to a mathematical analysis of the difference-equation model (5.11)–(5.16) is the observation that the carrier-wave frequency greatly exceeds a typical audio frequency (typically 500 kHz and 20 Hz - 20 kHz, respectively). Thus, each voltage in the amplifier may be considered to oscillate at the carrier-wave frequency, with a slow modulation. To make this idea more precise, a small parameter is introduced,

$$\varepsilon \equiv \omega T \ll 1, \quad (5.17)$$

where ω is a typical audio (angular) frequency, and the (dimensionless) slow time scale

$$\tau = \omega t = \varepsilon t / T. \quad (5.18)$$

To acknowledge the relatively slow variation of the audio signal, we also write $s(t) = S(\tau) = d^2 F(\tau) / d\tau^2$, where $F(\tau) = \varepsilon^2 f(t) / T^2$. The presence of a small parameter in the problem allows the use of the perturbation methods to solve the mathematical model.

Six functions are then introduced and are to be determined from Eqns. (5.11)–(5.16): these represent the four switching times in a given switching period, together with the values of the integrator outputs sampled at times $t = A_n$. Thus we introduce the functions $\alpha(\tau)$, $\beta(\tau)$, $\gamma(\tau)$, $\delta(\tau)$, $m(\tau)$ and $p(\tau)$, such that

$$(\alpha(\varepsilon n), \beta(\varepsilon n), \gamma(\varepsilon n), \delta(\varepsilon n), m(\varepsilon n), p(\varepsilon n)) = (\alpha_n, \beta_n, \gamma_n, \delta_n, m_n, p_n).$$

Furthermore, we expand each function in powers of ε , so that

$$\alpha(\tau) = \sum_{n=0}^{\infty} \varepsilon^n \alpha^{(n)}(\tau), \quad \beta(\tau) = \sum_{n=0}^{\infty} \varepsilon^n \beta^{(n)}(\tau), \quad \text{etc.}, \quad (5.19)$$

and solve the problems that arise from substituting these functions into Eqns. (5.11)–(5.16) at successive powers of ε .

At leading order, after much algebra, the fractional switching times are derived as

$$\begin{aligned} \alpha^{(0)}(\tau) &= \frac{1}{16}(1 - S(\tau))(4 - c_1 TS(\tau)), \\ \beta^{(0)}(\tau) &= \alpha^{(0)}(\tau) + \frac{1}{2}(1 + S(\tau)), \\ \gamma^{(0)}(\tau) &= \alpha^{(0)}(\tau) + \frac{1}{2}S(\tau), \\ \delta^{(0)}(\tau) &= \alpha^{(0)}(\tau) + \frac{1}{2}, \end{aligned}$$

while the sampled values of the integrator outputs are

$$m^{(0)}(\tau) = -\frac{1}{4}c_1 TS(\tau)(1 - S(\tau)), \quad p^{(0)}(\tau) = -(1 - k)S(\tau). \quad (5.20)$$

From Eqn. (5.10), the average of $g(t)$ over a carrier-wave period is

$$-\beta^{(0)}(\tau) + \delta^{(0)}(\tau) - \gamma^{(0)}(\tau) + \alpha^{(0)}(\tau) = -S(\tau) = -s(t). \quad (5.21)$$

Thus, to a good approximation, the audio-frequency component of the amplifier output is the inverted audio input signal.

In order to make useful predictions about the amplifier distortion, it is necessary to proceed in succession to terms of orders ε , ε^2 and ε^3 . The volume of algebra necessary to analyze these problems grows rapidly. Since it is really only the final answer that is of practical significance, none of the detailed intermediate results is recorded here.

Once the first few terms in the expansions for the functions α , β , γ and δ have been found, the final step in the calculation is to extract from the switching times the audio components that are present in $g(t)$. Extending the approach

used previously in [3], the audio-frequency components of the output, which is denoted by $g_a(t)$, are given by (cf. [83, 84])

$$g_a(t) = \sum_{n=1}^{\infty} \frac{(-\varepsilon)^{n-1}}{n!} \frac{d^{n-1}}{d\tau^{n-1}} (\alpha^n(\tau) + \delta^n(\tau) - \beta^n(\tau) - \gamma^n(\tau)). \quad (5.22)$$

Calculating terms up to order ε^3 , then rewriting the answer in terms of $s(t)$, the output expression is finally derived as

$$\begin{aligned} g_a(t) = & -s(t) + T^2 \frac{d^2}{dt^2} \left\{ \left[-\frac{1}{48} + \frac{1-k}{c_1 c_2 T^2} \right] s(t) - \frac{1}{24} s^3(t) \right\} \\ & + \frac{1}{16} T^2 \frac{d^2(s^2(t))}{dt^2} \text{sgn}(s(t)), \end{aligned} \quad (5.23)$$

where $\text{sgn}(s)$ equals 1 for $s > 0$, and -1 for $s < 0$.

Equation (5.23) is of particular importance because it accurately predicts the audible output components for BD modulation and is suitable for an arbitrary band-limited input signal. Comparing Eqn. (5.23) with the output signal expression in [3], the similarities and differences between the audible output signals for AD and BD modulation may be interpreted as follows.

Similarities—The terms in the first line of Eqn. (5.23) are exactly that of the AD-modulated second-order design analyzed in [3]. The term $(s(t))''$ contributes only to the distortion of the fundamental frequency components, causing the magnitude of the fundamental frequency components to slightly increase. Also, the feedforward path (i.e., $-k$) can be used to compensate the distortion of the fundamental output components.

Differences—The quadratic term in the second line of Eqn. (5.23), i.e., $\frac{1}{16} T^2 (s^2(t))'' \text{sgn}(s(t))$, is new and unique to BD modulation. This term reflects

the change in the relative switching order of the two bridge halves for positive and negative values of $s(t)$ and significantly affects the intrinsic distortion components that are appreciably present in the output. Note that this term is a product of an even function of the input signal, $(s^2(t))''$, and an odd function, $\text{sgn}(s(t))$. As a result, it will generate only odd-order harmonics, with magnitudes proportional to the square of the input signal magnitude.

It may also be worthwhile to highlight that the terms $(s^3(t))''$ and $(s^2(t))''\text{sgn}(s(t))$ in Eqn. (5.23) are the source of harmonics and intermodulation products in the demodulated output signal. As these two terms are independent of the loop filter parameters, i.e., c_1 and c_2 , it can be concluded that, up to the order of the analysis (i.e., ϵ^3), the THD and IMD of the BD-modulated Class-D amplifier are independent of the design of the loop filter. Recall that the same property also holds for AD modulation [3].

The audible output expression for first-order loop filter design (i.e., $c_2 = 0$) has been derived in the same way, and is

$$g_a(t) = -s(t) + \frac{1-k}{c_1} \frac{ds}{dt} - \frac{1}{32} T^2 \frac{d^2(s^2(t))}{dt^2} \text{sgn}(s(t)) + T^2 \frac{d^2}{dt^2} \left\{ \left[\frac{1}{48} - \frac{1-k}{c_1^2 T^2} \right] s(t) + \frac{1}{48} s^3(t) \right\}. \quad (5.24)$$

As the coefficients for the nonlinear terms in Eqn. (5.24) are exactly half of those in Eqn. (5.23), the intrinsic distortion components for the first-order design have the same trend as that for the second-order design, except that the magnitude is reduced by half. For the sake of brevity, the analysis in the following sections of this chapter is based only on the second-order design.

5.3 Intrinsic distortion of a BD-modulated Class-D amplifier

In this section, the intrinsic distortion of a BD-modulated closed-loop Class-D amplifier will be examined for both single-tone and two-tone input signals, in the form of THD and IMD, respectively. Due to the $\text{sgn}(s(t))$ function, this derivation procedure is rather mathematically involved. To simplify the presentation, only the final expressions are presented here.

5.3.1 Total harmonic distortion

By substituting the audio signal, $s(t) = s_0 \sin \omega t$, into Eqn. (5.23), $g_a(t)$ may be derived as

$$\begin{aligned} & -s_0 \left\{ 1 + (\omega T)^2 \left[\left(-\frac{1}{48} + \frac{1-k}{c_1 c_2 T^2} \right) - \frac{1}{32} s_0^2 \right] \right\} \sin \omega t \\ & - \frac{3}{32} (\omega T)^2 s_0^3 \sin 3\omega t + (\omega T)^2 s_0^2 \sum_{\text{odd } n} \frac{n \sin n\omega t}{2\pi(n^2 - 4)}. \end{aligned} \quad (5.25)$$

Note that, in contrast to AD modulation, there exist significant high-order odd harmonics in the output of a BD-modulated Class-D amplifier, which are represented by the summation term in Eqn. (5.25). In addition, we note that the third harmonic distortion term has coefficient $3(\omega T)^2 s_0^2 \left(\frac{1}{10\pi} - \frac{1}{32} s_0 \right)$, which has a maximum at $s_0 = \frac{32}{15\pi} \approx 0.679$. Furthermore, the third-harmonic distortion of the BD modulation is greater than that of the single-ended design (AD modulation) unless the audio signal amplitude is sufficiently large, specifically unless $s_0 > \frac{8}{5\pi} \approx 0.509$.

If we include all generated harmonics from Eqn. (5.25), we find

$$\begin{aligned} \text{THD} &\sim (\omega T)^2 s_0 \left\{ \left(\frac{3}{10\pi} - \frac{3}{32} s_0 \right)^2 + \sum_{\text{odd } n \geq 5} \frac{n^2}{4\pi^2 (n^2 - 4)^2} \right\}^{1/2} \\ &\sim (\omega T)^2 s_0 \left\{ \left(\frac{3}{10\pi} - \frac{3}{32} s_0 \right)^2 + \frac{1}{64} \left(1 - \frac{1696}{225\pi^2} \right) \right\}^{1/2}. \end{aligned} \quad (5.26)$$

Equation (5.26) shows that the THD of a BD-modulated Class-D amplifier increases with increasing signal amplitude s_0 . As with the third-harmonic distortion, this amplifier has greater THD than its AD-modulated counterpart for small signal amplitudes; the present design has lower THD only when $s_0 > 5(9\pi^2 - 16) / (162\pi) \approx 0.715$. Of course, it should be borne in mind that the higher harmonics generated by the amplifier is beyond the range of human hearing, so the infinite sum implicit in Eqn. (5.26) should be (generally severely) truncated. If such a truncation is made, it still remains the case that the THD increases with increasing s_0 (unless we keep only the third harmonic term, in which case the THD has a maximum at $s_0 = \frac{32}{15\pi}$, as above).

Figure 5.5 illustrates the output spectrum of a BD-modulated 2nd-order Class-D amplifier based on MATLAB simulation. The input signal is set at 1 kHz with modulation index equal to 0.7. The carrier frequency is set to 250 kHz, which will be the default value in the rest of the work presented in this chapter (in the absence of specification to contrary). This figure clearly shows that there exist significant high-order harmonic components in the output spectrum. It is particularly noteworthy that the 5th-harmonic is in this case larger than 3rd-harmonic. This indicates that the BD-modulated Class-D amplifier has an output spectrum that is quite different from that for AD modulation.

Figure 5.5 Frequency spectrum of the demodulated output signal of the Class-D amplifier with BD modulation. The input signal is set to have frequency $F_{in} = 1$ kHz and modulation index $M_{in} = 0.7$. Carrier frequency is set to 250 kHz.

Using Eqn. (5.25), we are able to predict the THD performance of a BD-modulated Class-D amplifier, with relatively little computational effort, and without the need for numerous time-consuming simulations. Figure 5.6 shows a three-dimensional plot of the THD with respect to both the modulation index and the frequency of the input signal. The data are calculated based on our analytical expression, including all significant harmonics within the 20 kHz audio band. The corresponding contour lines with 0.01% THD incremental step are plotted on the base of the 3D diagram.

Figure 5.6 3D plot of the THD of a BD-modulated Class-D amplifier as a function of both the modulation index and frequency of the input signal.

5.3.2 Intermodulation distortion

Intermodulation distortion (IMD) arises when the amplifier input comprises multiple signals with different frequencies. The output then contains contributions at sums and differences of the various frequencies. IMD can significantly detract from the listening experience.

We thus consider the IMD for an input signal

$$s(t) = s_1 \sin \omega_1 t + s_2 \sin \omega_2 t \quad (s_1, s_2 > 0). \quad (5.27)$$

The contribution to the IMD from the terms in the first line of Eqn. (5.23) may be expressed as

$$\sum G_{m,n} \sin(m\omega_1 + n\omega_2)t, \quad (5.28)$$

where the nonzero coefficients are

$$\begin{aligned}
 G_{1,0} &= -(1 + \mu\omega_1^2 T^2)s_1 + \frac{1}{32}s_1^3\omega_1^2 T^2 + \frac{1}{16}s_1s_2^2\omega_1^2 T^2, \\
 G_{0,1} &= -(1 + \mu\omega_2^2 T^2)s_2 + \frac{1}{32}s_2^3\omega_2^2 T^2 + \frac{1}{16}s_1^2s_2\omega_2^2 T^2, \\
 G_{3,0} &= -\frac{3}{32}s_1^3\omega_1^2 T^2, \quad G_{0,3} = -\frac{3}{32}s_2^3\omega_2^2 T^2, \\
 G_{2,\pm 1} &= -\frac{1}{32}s_1^2s_2(2\omega_1 \pm \omega_2)^2 T^2, \\
 G_{1,\pm 2} &= -\frac{1}{32}s_1s_2^2(\omega_1 \pm 2\omega_2)^2 T^2,
 \end{aligned}$$

and where $\mu = -\frac{1}{48} + (1-k)/(c_1c_2T^2)$. Recall that the intermodulation products generated by the first line of Eqn. (5.23) are consistent with those of an AD-modulated Class-D amplifier [5].

The corresponding calculation for the term $\frac{1}{16}T^2(s^2(t))''\text{sgn}(s(t))$ in the second line of Eqn. (5.23) is more complicated; for this we use the method of Bennett [85, 86]. The detailed derivation is given in the Appendix of [4], with the final expression for $g_a(t)$ being

$$\begin{aligned}
 & -\frac{1}{16}T^2\sigma(\omega_1^2s_1\sin\omega_1t + \omega_2^2s_2\sin\omega_2t) \\
 & + \frac{1}{16}T^2\sigma^2\sum_{p=1}^{\infty}\sum_{\substack{q=-\infty \\ p+q\text{ odd}}}^{\infty}(p\omega_1 + q\omega_2)^2H_{pq}\sin(p\omega_1 + q\omega_2)t \\
 & + \frac{1}{16}T^2\sigma^2\sum_{\substack{q=1 \\ q\text{ odd}}}^{\infty}q^2\omega_2^2H_{0q}\sin q\omega_2t,
 \end{aligned} \tag{5.29}$$

where

$$H_{pq} = \sum_{\substack{n=1 \\ n\text{ odd}}}^{\infty} \frac{16}{n^3\pi^3} J_p(n\pi s_1/\sigma) J_q(n\pi s_2/\sigma), \tag{5.30}$$

and $\sigma = s_1 + s_2$. Here J denotes the Bessel function of the first kind. Note that the second line of Eqn. (5.29) indicates high-order IMPs. For instance, the 5th-IMP at frequency $3\omega_1 + 2\omega_2$ has coefficient $\frac{1}{16}T^2(3\omega_1 + 2\omega_2)^2\sigma^2H_{32}$.

To provide some insights into the functions, H_{pq} , corresponding to low-order intermodulation products, Figure 5.7 illustrates the functions $H_{pq}(\lambda)$ up to fifth order, where $\lambda = s_1 / \sigma = s_1 / (s_1 + s_2)$. Note that only the case of odd $p+q$ needs to be considered and that the behavior of the remaining low-order H_{pq} which are not plotted in Figure 5.7 may be inferred from that figure using the relation $H_{pq}(\lambda) = H_{qp}(1 - \lambda)$. The variable λ represents the relative magnitude of s_1 to the total input signal. Finally, combining Eqn. (5.28) and Eqn. (5.29) allows us to analytically determine the IMD.

Figure 5.7 Plots of the functions $H_{pq}(\lambda)$ for low-order intermodulation products with odd $p+q$, where $\lambda = s_1 / (s_1 + s_2)$. Values of p, q are indicated next to each curve.

The frequency spectrum of the output signal in a typical IMD test is shown in Figure 5.8. The two-tone stimulus signals are at 60 Hz and 7 kHz, with the amplitudes equal to 0.5 and 0.125, respectively. Compared to the frequency spectrum of the AD-modulated amplifier shown in [5], there exist significant

high-order IMPs in a BD-modulated amplifier, illustrated as the sideband components surrounding the peaks at 7 kHz and 14 kHz. Furthermore, this figure justified that the 5th-order IMPs are even larger than the 3rd-order IMPs at the frequencies surrounding the 2nd-order harmonic of the high-frequency tone (i.e., at 14 kHz).

Figure 5.8 Frequency spectrum of the output signal for a BD-modulated 2nd-order Class-D amplifier.

5.4 Analytical, simulation and measurement results

In this section, the analysis for the audible output signal of a BD-modulated 2nd-order Class-D amplifier is verified by comparing the derived expressions, i.e., Eqn. (5.23), against computer simulations using both MATLAB Simulink and Cadence Spectre simulators. Since this work focuses on the intrinsic distortion of the BD-modulated Class-D amplifier with the assumption that all the effects of a practical circuit, such as component variation, non-ideality of the output stage and nonlinearity of the low-pass filter, are eliminated, no hardware test is required. The Cadence simulation is sufficient to demonstrate

the accuracy of the mathematical model derived from the circuit schematic. The second-order loop filter is designed to achieve a high low-frequency gain inside the audio range and the parameter values used are: $c_1 = 498800 \text{ s}^{-1}$, $c_2 = 490340 \text{ s}^{-1}$, $T = 4\text{e}-6 \text{ s}$ and $k = 0$. In Cadence simulations, the power stage is constructed using a pair of PMOS and NMOS transistors with large W/L ratio, and are simulated using foundry provided BISIM models for the 0.18- μm CMOS process. The fully differential amplifier is created based on a macro model (a single pole system: DC gain = 120 dB and gain-bandwidth product = 100 MHz). The comparator is built using a simple voltage-controlled voltage source. The passive components (capacitors and resistors) are taken from Cadence analog library. The supply voltage is 3.3 V. As described above, the simulation circuit built in Cadence is quite ideal except for the power MOSFETs.

5.4.1 Verification of total harmonic distortion

Figure 5.9 shows the THD performance against the modulation index of the input signal. The modulation index ranges from 0.1 to 0.9 and the input signal frequency is set to 3 kHz, so that the high-order harmonic distortions are included. The THD results are calculated based on all the harmonics within the audio range, i.e., from 20 Hz to 20 kHz. The MATLAB simulation results for a 2nd-order Class-D amplifier with binary PWM signal is also provided in the figure for comparison.

As illustrated in Figure 5.9, the matching between the analytical results and the simulation results is excellent; in particular, the MATLAB simulation results and the analytical results are almost indistinguishable. Compared with

its AD-modulated counterpart, BD modulation suffers from a much higher THD for small input signal whereas it achieves a better performance for large input signal. Recall that music has a crest factor (i.e., peak to rms ratio) range of 4–10. This means that the modulation index of the input signal in most conditions is around 0.35 or even lower, in which case the AD-modulated Class-D amplifier has a much better performance, as compared to BD modulation.

Figure 5.9 THD of a BD-modulated 2nd-order Class-D amplifier against the modulation index of the input signal.

Figure 5.10 shows the magnitude of the 3rd- and 5th-harmonic components plotted against the magnitude of the input signal with the same input setting as in Figure 5.9. The analytical results perfectly match the MATLAB simulation results even for individual frequency components and hence demonstrates the accuracy of the analytical expression. The Cadence Spectre simulation results are slightly higher than both the analytical predictions and the MATLAB simulation results. This is probably due to the practical limitations of the power MOSFET model employed in the Cadence simulation, such as the on-resistance

and the asymmetry of the rising and falling switching edges. As expected from our analysis, the 3rd-order harmonic distortion reaches its peak when the modulation index of the input signal is around 0.7 and then decreases with further increase in input signal. On the other hand, the 5th-order harmonic increases quadratically with the magnitude of the input signal and becomes the dominant distortion component for large input signal.

Figure 5.10 The 3rd and 5th harmonic components in the demodulated output signal.

The THD performance against the input signal frequency of the BD-modulated 2nd-order closed-loop Class-D amplifier is given in Figure 5.11. The modulation index of the input signal is fixed at 0.7. The input signal frequency is from 1 kHz to 6 kHz. The flattening of the curve between 4 kHz and 5 kHz is due to the fact that the 5th-harmonic distortion for input frequency higher than 4 kHz will fall outside the audio band. As a result, the advantage of lower THD at large modulation index for BD modulation becomes quite obvious for high frequency input signal.

Figure 5.11 THD against the frequency of the input signal. The modulation index of the input signal is 0.7.

As for the AD-modulated design, the THD of a BD-modulated Class-D amplifier is predicted by the model to be inversely proportional to the square of the switching frequency. This is illustrated in Figure 5.12 by the same decreasing slopes for both AD and BD modulations. Note that analytical and MATLAB simulation results are almost indistinguishable. The Cadence simulation results also closely follow the predicted analytical results; the increasing mismatch at higher carrier frequency is probably because of the relative weakening of the intrinsic distortion compared to other sources of distortion.

Figure 5.12 THD versus carrier frequency. The input signal has $f_{in} = 3$ kHz and $M_{in} = 0.7$.

Figure 5.13 illustrates the MATLAB simulation results of the significant 3rd- and 5th-harmonics when the second-order loop filter parameter c_2 reduces from a typical value to 0. The result confirms that the harmonic components are independent of the loop filter parameters over a wide range of values, corresponding to normal second-order loop filter design. When c_2 is sufficiently small, however, a dependence on this parameter emerges, and the loop filter exhibits a closer resemblance to a first-order design (i.e., the limiting case of $c_2 = 0$ as indicated by the linearized loop gain transfer function, $c_1(s + c_2)/s^2$); in this case, the THD is reduced by half (as predicted by the output expression of a first-order loop filter design given in Eqn. (5.24)).

Figure 5.13 Harmonic components of a fully differential BD-modulated Class-D amplifier versus the loop filter parameter c_2 . The input signal has $f_{in} = 3$ kHz and $M_{in} = 0.7$.

5.4.2 Verification of intermodulation distortion

The testing standard set by the Society of Motion Picture and Television Engineers (SMPTE) is applied here to examine the performance of the BD-modulated Class-D amplifier and to verify the accuracy of the analytical output signal expressions. The two-tone input signal consists of a low-frequency high-amplitude tone (60 Hz) and a linearly combined high-frequency tone (7 kHz) at 1/4 the amplitude (12 dB) of the low-frequency tone [40]; thus $f_1 = \omega_1 / 2\pi = 60$ Hz, $f_2 = \omega_2 / 2\pi = 7$ kHz, $s_1 = 4s_2$.

Figure 5.14 illustrates the SMPTE IMD of the BD-modulated 2nd-order Class-D amplifier against the modulation index of the high-frequency input component. To ensure that the combined input magnitude is less than 1, the modulation index of the 60 Hz input signal varies from 0.1 to 0.7 and the modulation index of the 7 kHz input signal changes correspondingly from 0.025 to 0.175. Recall that the maximum order of the intermodulation products included for the IMD calculation is indicated by the subscript. For example,

IMD₅ implies up to 5th-order IMPs are considered in the calculation. As seen in Figure 5.14, the analytical prediction of the IMD has a perfect match with the MATLAB simulation results. The Cadence simulation results also closely follow the analytical results. The mismatch in the low modulation index range is probably due to the insignificance of the intrinsic intermodulation distortion for small input signal as compared to the distortions introduced by other error sources, e.g., the tolerance error of the simulator and the extra distortion caused by the non-ideal power MOSFETs. For instance, due to the low-frequency input signal at 60 Hz, a longer simulation duration is required for frequency analysis, compared to that for THD. Consequently, the error tolerance setting of the Cadence Spectre simulator is relaxed as a trade-off to achieve an affordable simulation time and not to have overloaded simulation data. However, the relaxed tolerance setting limits the accuracy of the Cadence simulation results.

Figure 5.14 SMPTE IMD against the modulation index of the high-frequency input signal.

In addition, the MATLAB simulated IMD₃ and IMD₅ results for AD modulation are also provided in Figure 5.14. Similar to THD, BD modulation

managed to attain smaller IMD for large input signal, but has larger IMD for small input signal, compared to AD modulation. The crossing point for equal IMD performance is around $M_2 = 0.1$, i.e., the summed magnitude for the two-tone signals is equal to 0.5, half the full input signal swing. It may also be worthwhile to highlight that, for AD modulation, the IMD_5 almost overlaps with IMD_3 . This indicates that the 5th-order IMPs at the output of an AD-modulated Class-D amp are insignificant and can be ignored when compared to the 3rd-order IMPs.

Figure 5.15 plots the magnitude of the typical 3rd and 5th-order IMPs for BD modulation against the modulation index of the high-frequency input signal, M_2 , with the same input setting as Figure 5.14. Note that only the IMPs at frequency equal to $nf_2 + mf_1$ are shown here, as the remaining IMPs at frequency $nf_2 - mf_1$ have similar patterns to their respective counterparts. It is clear that the analytical expression accurately predicts the dependency of each individual frequency component for a range of values of M_2 . Note that the 3rd-order IMP at frequency $f_2 + 2f_1$ has a roughly parabolic response against the magnitude of the input signal, whereas the 3rd-order IMP at frequency $2f_2 + f_1$ has a fluctuating response, i.e., rising to a peak when M_2 increases to 0.1, followed by a trough at $M_2 \approx 0.15$. As a result, IMD_3 in Figure 5.14 is noted to decrease when M_2 is higher than a certain value, approximately 0.1. On the other hand, the 5th-order IMPs increase monotonically with respect to M_2 and dominate the intrinsic distortion of the amplifier for large input signal. This is reflected in Figure 5.14 as the IMD_5 is significant larger than the IMD_3 for M_2 beyond 0.1.

Figure 5.15 The IMPs along with the high frequency fundamental output component against the modulation index of the high frequency input signal.

5.5 Summary

In this chapter, we have presented a comprehensive mathematical analysis of the intrinsic distortion of a BD-modulated closed-loop Class-D amplifier. The

derived analytical expression accurately predicts the audio components of the frequency spectrum of the output signal and is applicable to any band-limited input signal. For the special case of either single-tone or two-tone input signals, the analytical expression clearly demonstrates the unique intrinsic distortion properties of a BD-modulated design, as compared to its AD-modulated counterpart. More precisely, it shows that the 3rd-order harmonic and intermodulation products for BD modulation have a roughly parabolic response as a function of the magnitude of the input signal. Furthermore, there exist significant high-order distortion components in the output spectrum for BD modulation, in the form of the 5th-order harmonic and 5th-order intermodulation products, as compared to AD modulation. This may be a potential drawback of BD modulation since human beings are quite sensitive to such high-order distortion.

Chapter 6 Stability of Closed-loop

Class-D amplifier

6.1 Introduction

Though the closed-loop PWM-type Class-D amplifiers have been widely used, the design of the loop filter is still based on the linear system theory, which restricts the phase margin of the linearized loop gain to be around 60 degree. As the field of the Class-D amplifier gains maturity and the demand for better functionality, reliability and performance of power amplifier keeps increasing, in-depth analysis of complex behavior and nonlinear phenomena of the Class-D amplifier becomes justifiable and even mandatory.

In this chapter, circuit behavior variation of an AD-modulated closed-loop PWM-type Class-D amplifier with its loop filter parameters swept beyond the conventional design region was investigated. Part of the observations that was named as pulse skipping had been reported in [3]. The phenomenon is evaluated here from an engineering point of view, looking at the fundamental behavioral change of the system and for the indicator of the chaotic operation. The examination revealed that the second order Class-D amplifier underwent a border collision after a period-doubling bifurcation.

Further to the above, and based on the criterion to preclude the occurrence of pulse skipping, an extended boundary for the second-order loop filter design is proposed. The experimentally validated theoretical results of this work enhance

understanding on the dynamics of the Class-D amplifier beyond the linear regime. This is truly beneficial allowing circuit designers to explore beyond the conservative designs.

This chapter is organized as follows. In Section 6.2, the conventional design guideline for a second-order Class-D amplifier is briefly reviewed. The route to chaos of a second-order Class-D amplifier is investigated in Section 6.3. The performance of the Class-D amplifier in chaotic operation is verified in Section 6.4. An extended and clear design boundary for the second-order loop filter is demonstrated in Section 6.5. Finally, a summary is drawn in Section 6.6.

6.2 Conventional design guidelines

For simplicity and consistency with the analytical work presented in Chapter 4, the analysis in this chapter is based on the same normalized mathematical model discussed in Figure 4.2, and reproduced in Figure 6.1 for ease of referring. Recall that the procedure to convert a practical circuit structure to the model was demonstrated in [3].

Figure 6.1 Mathematical model of a closed-loop Class-D amplifier.

In a conventional design, the linearized loop gain of a second-order Class-D amplifier can be expressed as follows:

$$H(s) = \frac{c_1(s + c_2)}{s^2} \quad (6.1)$$

where the pulse width modulator is replaced by a unity gain block. The conventional design criteria of a second-order loop filter had been reported in [57], which states that

$$\omega_{UG} = \omega_C / \pi \quad (6.2)$$

$$\omega_Z = \omega_{UG} / \sqrt{3} \quad (6.3)$$

where ω_C is the fundamental carrier frequency, ω_{UG} is the unity gain frequency of the loop gain $H(s)$ and ω_Z is the frequency of the left hand plane (LHP) zero. The unity gain frequency and the LHP zero frequency can be expressed in terms of the model parameters, c_1 and c_2 , as $\omega_{UG} \approx c_1$ and $\omega_Z = c_2$.

Equation (6.2) is established to ensure that the slopes of the triangular carrier are steeper than those of the loop filter output signal, to prevent multiple switching in each carrier period (a.k.a ripple instability). It indicates that ω_{UG} should be lower than ω_C ; the ratio of π is obtained based on the worst case condition when the normalized input signal is equal to one. Recall that this criterion is strictly derived for 1st-order loop filter system, and be applied to the 2nd-order loop filter design provided that ω_Z is sufficiently lower than ω_{UG} [57, 59].

Equation (6.3) is introduced based on linear system stability consideration such that the LHP zero frequency, ω_Z , should be lower than the unity-gain frequency, ω_{UG} , to ensure sufficient phase margin. A ratio of $\sqrt{3}$ yields a phase margin of 60 degrees. Note that Eqn. (6.3) is merely a design guideline

following classical linear control theory, and not a solid stability criterion for the switching-mode Class-D amplifier.

Compared with first-order loop filter, the only additional degree of freedom to design a second-order loop filter is the location of the zero, which is limited by the design guideline for linear system. To pursue a higher power supply reject ratio (PSRR) and better attenuation on the distortion caused by the non-ideality of the power stage, it is desirable to shift the zero to higher frequency so as to increase the low frequency loop gain, without affecting the carrier attenuation [8].

6.3 Routes to chaos

The effect of the right-shifted zero is investigated through MATLAB simulation—using a DC input signal, with the modulation index, M , set to 0.9, the magnitude of the loop filter output signal is sampled when the triangular carrier signal reached its minimum value, i.e. $v(nT) = -1$. At steady state, the sampled magnitude of the loop filter output signal, $h(t)$, is expected to remain constant and larger than -1 for normal operating condition. Figure 6.2 shows the bifurcation diagram obtained, with loop filter parameter, c_2 , being the bifurcation parameters and c_1 is set to 4.988e5. 500 sampled data have been recorded for each value of c_2 . Recall that the bifurcation diagram is a summary chart of the behavioral changes of a system as the parameter is varied. The configuration of the MATLAB simulator is set as follows: $MaxStep = 1e-9$, $AbsTol = 1e-6$, and $RelTol = 1e-3$. Note that the setting of both $absTol$ and $RelTol$ affects the magnitude of the diverged values, as they determine the

truncation error in the simulation. But the simulator setting does not affect the chaos starting point.

Figure 6.2 Bifurcation diagram of a PWM-type Class-D amplifier with DC input set to 0.9. Carrier frequency is 250 kHz.

Figure 6.2 illustrates how the system behaves when the zero of the loop filter is shifted to the right. For c_2 smaller than 5.8×10^5 , the system is stable and the sampled loop filter output signal maintains constant. The system is in typical period-1 operation, where all waveforms repeat at the same rate as the driving clock, i.e. the triangular carrier in Class-D amplifier. Thus, period-n operation refers to the case where the periods of all waveforms are exactly n times that of the driving clock. The system exhibits a period doubling at c_2 equal to 5.82×10^5 , which is in period-2 regime. When c_2 is further increased to 5.9×10^5 , the system suddenly jumps (without further period doublings) to chaos, where the diversity of the loop filter output signal continues to increase with respect to increasing c_2 . Recall that chaos is a special equilibrium solution (or simply an attractor) of a nonlinear system that is characterized by an aperiodic and apparently random trajectory [87].

For a second-order system, the entire attractor can be presented by the two integrator outputs, $m(t)$ and $p(t)$. The phase portraits of these two states shown in Figure 6.3 are very useful in uncovering subtle periodicity of the nonlinear dynamic system. The input and carrier settings are the same as that of Figure 6.2, and will be used later in Figure 6.4.

Figure 6.3 Phase portrait for: (a) period-1 operation at $c_2 = 2.5e5$, (b) period-1 operation at $c_2 = 5e5$ (higher loop filter gain), (c) period-2 operation at $c_2 = 5.82e5$, (d) Chaotic operation at $c_2 = 6.5e5$.

Figure 6.3 shows that when c_2 is designed at $2.5e5$ and $5e5$ (see Figure 6.3(a) and Figure 6.3(b)), the system is stable, and the trajectory moves along a closed path in the state space. This indicates that the attractors have a periodic orbit. When c_2 increases to around $5.82e5$, period-1 orbit loses stability and period-2 orbit takes over. This is clearly illustrated in Figure 6.3(c) as a sudden doubling of the period of a stable periodic orbit. Recall that period-doubling bifurcation is a smooth bifurcation, which means that it does not involve structural changes

of the system. A smooth bifurcation is normally associated with the loss of stability of one solution and the picking up of another. When c_2 is further increased to $6.5e5$, as seen in Figure 6.3(d), the system becomes chaotic—the trajectory is non-periodic and apparently random. This route to chaos is quite common for some power converter systems, in which a smooth bifurcation is followed by a non-smooth bifurcation [79, 80, 88].

Figure 6.4 depicts the time-domain waveforms of the loop filter output signal, i.e. the modulating signal, the triangular carrier signal and the PWM signal, when the system is in period-2 regime with c_2 set to $5.82e5$ (Figure 6.4 (a)-(b)); and in chaotic regime with c_2 equal to $6.5e5$ (Figure 6.4 (c)-(d)).

Figure 6.4 Signal waveforms in period-2 regime: (a) PWM signals, (b) triangular carrier signal and loop filter output signal, and in chaotic regime: (c) PWM signals, (d) triangular carrier signal and loop filter output signal.

Note that the modulating signal in period-2 regime (see Figure 6.4(b)) has a period equal to two times that of the carrier period (consisting of a lower-peak ripple plus a higher peak ripple). When the system is in the chaotic regime, the modulating signal sometimes fails to hit the carrier signal within one cycle (refer to Figure 6.4(d)), causing the border collisions, hence disrupting the standard period-doubling bifurcation pattern. This is the reason why this bifurcation phenomenon is named as pulse skipping phenomenon in [3]. Note that although the carrier signal and the output PWM signal is normalized to ± 1 , the loop filter output signal can have a value beyond that range. This is because the carrier signal swing in a practical circuit implementation is typically around half the supply rails.

In summary, the Class-D amplifier experiences a period-doubling bifurcation and follows a border collision to become chaotic. When the parameter, c_2 , varies across the boundary of the chaos regime, an abrupt change in system behavior occurs, and is characterized as pulse skipping phenomenon. The missing of the square pulse causes the system to behave structurally different from a modeling point of view, since the original discrete-time difference equations for determining the behavior of the system are no longer applicable. In the next section, the focus will be on the chaotic operation of the Class-D amplifier, where it involves significant alteration of the circuit operation.

6.4 Class-D amplifier performance in chaotic operation

In contrast to ripple instability that causes the carrier frequency to increase to infinity [15], pulse skipping occurred in chaotic operation results in the carrier

frequency to drop and “leak” through the LC low-pass filter, thereby distorting the output signal. Figure 6.5 depicts the demodulated output signal for a 100-Hz input signal with magnitude equal to 0.7. As shown in Figure 6.5(a), the “oscillating” components at the peak of the demodulated output signal are the “leaked” sub-harmonic carrier components. Note that the magnitude of leaked carrier component is dependent on the bandwidth of the low-pass filter. In this example, the 3-dB bandwidth of the output filter is 30 kHz. As seen in Figure 6.5(b), there exist significant sub-harmonics of the carrier frequency component (mainly at half of the carrier frequency, i.e., 125 kHz). Although these leaked high frequency components are outside the audio range, they will cause unnecessary power consumption to reduce the power efficiency.

Figure 6.5 Pulse skipped output signal of second-order Class-D amplifier for $c_1 = 4.988e5$ and $c_2 = 8.5e5$: (a) time-domain signal waveform; and (b) FFT analysis of the output signal.

Recall that the key property of the chaotic systems is the sensitively dependent upon initial condition. In brief, two nearby starting points can evolve

into two entirely uncorrelated trajectories. This is specially marked as the growing perturbation on switching times of the output PWM signal of a Class-D amplifier, and represented as an oscillated residual carrier inside the loop filter output signal in [3]. The sensitivity on initial condition is also referred as fast-scale instability in [79, 80, 88]. It is expected that the growing perturbation on switching times affects the linearity of the Class-D amplifier. This is because errors on switching times due to circuit noise or power supply variation are amplified rather than attenuated.

Figure 6.6 provides a comparison on the THD+N (%) of two loop filter designs—one with $c_2 = 5e5$ and the other with $c_2 = 8.5e5$. To calculate the THD+N (%), a 3rd-order Butterworth filter with bandwidth equal to 80 kHz is inserted at the output to prevent aliasing error during FFT process. The results concluded that in the low frequency range, the THD+N (%) with $c_2 = 8.5e5$ is larger than that the case of $c_2 = 5e5$. The notable increase in THD+N (%) signifies that Class-D amplifier operates in the chaotic regime for large low frequency input signal. But in the high frequency range, the performances of the two designs are identical. This is because for large low frequency signal, the loop filter output signal remains at its peak for a longer duration than that for a high frequency signal. This will increase the likelihood of growing oscillated residue carrier for preventing the loop filter output signal from intersecting with the carrier signal.

Figure 6.6 THD+N (%) in MATLAB simulations for second-order Class-D amplifier with different loop filter design.

6.5 Criterion for precluding chaotic operation

The criterion to preclude the chaotic operation was derived in [3] by determining the sign of the eigenvalues for the second order system. The final design criterion is reproduced as follows:

$$c_1 c_2 < (\omega_c / \pi)^2 \quad (6.4)$$

Equation (6.4) is derived based on a maximum DC-input signal with $s(t) = 1$ for $t > 0$, which is the worst-case condition for pulse skipping occurrence. Therefore, for general audio input signal, the criterion guarantees the preclusion of the chaotic operation and no further margin is required. It is worthwhile to highlight that the occurrence of pulse skipping is not only dependent on the loop filter parameters, but also the switching frequency and the magnitude of the input signal. Note that the magnitude of the input signal appears in the expression of the eigenvalues in [3] but is substituted by maximum input value in worst case analysis. It therefore does not appear in Eqn. (6.4). This property

differentiates itself from the traditional instability criterion for linear system which relates only to the loop filter design, as described in Eqn. (6.3). In addition, the system is still bounded-input-bounded-output (BIBO) stable, even when the system operates in the chaotic regime.

The criterion for precluding the chaotic operation can be used to replace the linear system stability criterion in the design of a 2nd-order Class-D amplifier. To prevent the Class-D amplifier from any unwanted switching condition, the design of the 2nd-order loop filter should satisfy Eqns. (6.2) and (6.4). Consequently, the model parameters must also fulfill the following criteria:

$$c_1 < \omega_c / \pi \quad (6.5)$$

$$c_2 < \omega_c^2 / c_1 \pi^2 \quad (6.6)$$

Note that the first criterion is used to prevent multi-switching of the output stage inside one designed carrier period. The second criterion is instead employed to prevent the missing of the switching activity inside each carrier period. Interestingly, the boundary condition is at $c_1 = c_2 = \omega_c / \pi$.

As an illustration, the carrier frequency is set as $f_c = 250$ kHz. With available discrete passive components, the loop filter parameters of both the proposed design and the conventional design are tabulated in Table 6.1, and their magnitude responses are plotted in Figure 6.7. The proposed new design managed to achieve about 6 dB higher low frequency loop gain without any extra cost.

Table 6.1 Model parameters of the 2nd-order Class-D amplifier.

Parameter	Conventional Design	Proposed Design
c_1, c_2	4.3301e5, 2.8868e5	4.988e5, 4.9034e5
f_c	250 kHz	250 kHz

Figure 6.7 Linearized loop gain of the 2nd-order Class D amplifier.

6.6 Summary

This chapter provides an overview of the chaotic dynamic and bifurcation scenarios of the Class-D power amplifier when the loop filter parameter varies. The *route to chaos* in a conventional PWM-type Class-D amplifier is identified. When the zero of the loop filter is shifted to high frequency, a period-doubling bifurcation surfaces, and is followed by a border collision where the system enters the chaos regime. The chaotic operation of the Class-D amplifier is characterized by the occurrence of the pulse skipping phenomenon. The criterion for precluding the chaotic operation has also been determined. The study demonstrates that a design based on the new criterion can achieve higher loop gain of around 6 dB, as compared to the conventional design that is based on linear system stability criterion, and without any extra cost.

Chapter 7 Dual Feed-forward

Carrier Modulation Topology

7.1 Introduction

As investigated previously, intrinsic harmonic distortion is a limiting factor for the linearity of conventional PWM-type Class-D amplifier for both AD modulation (in Chapter 4) and BD modulation (in Chapter 5). Since it is caused by the high-frequency feedback signal and unrelated to the loop filter design in a wide parameter range, the suppression of intrinsic harmonic distortion require circuit structure innovation.

In this chapter, a dual feed-forward carrier modulation topology able to significantly attenuate the intrinsic harmonic distortion of the 2nd-order loop filter Class-D amplifier will be introduced. Its modest switching frequency ensures high power efficiency, especially for high voltage applications. The switching frequency of the proposed topology varies within a much narrower range than that of the self-oscillating topologies. This helps in mitigating the audible intermodulation distortion in multi-channel applications. A portion of this chapter is extracted from the candidate's publication [6].

This chapter is organized as follows. In Section 7.2, the proposed carrier modulation technique is presented based on a single-ended AD modulation circuit architecture. The working mechanism of the proposed topology is partially investigated in Section 7.3. The simulation and measurement results

for an AD-modulated implementation are given in Section 7.4. Following that, in Section 7.5, the feasibility of the proposed design on BD modulation is demonstrated, where a transistor-level circuit is designed using Global Foundry 0.18- μm CMOS process. Finally, a summary is proposed in Section 7.6.

7.2 Circuit structure of the proposed topology

To reduce the intrinsic harmonic distortion, a quadratic carrier generator with dual feed-forward modulating signals is proposed. A demonstration of the proposed circuit is illustrated in Figure 7.1 and can be considered a combination of two solutions/steps.

First, by adding two passive components, C_4 and R_7 , on the feedback path of the op-amp, X_5 , the linear triangular carrier generator is converted to a quadratic carrier generator. As illustrated in Figure 7.2, the quadratic carrier produces a phase delay on the PWM signal, which partially compensates the phase advance caused by the ripple signal (see Figure 3.4 and Figure 3.5). With careful allocation of the zero created by C_4 and R_7 , the intrinsic harmonic distortion can be suppressed by 4 to 5 times. A suitable starting point for optimization is to set the created zero at the same location as the zero inside the 2nd-order loop filter (i.e., $R_7 = R_3 C_1 / C_3$).

Second, two feed-forward signals, input signal $V_{in}(t)$ and loop filter output signal $V_{in}(t)$, are fed to the negative input of X_5 to adjust the carrier signal, which will be referred to as the carrier modulating signal in the rest of the chapter. The introduction of the carrier modulating signal is an additive solution on the quadratic carrier to further improve the linearity by another 3 to 5 times.

R_8 and R_9 provide an extra degree of design freedom and through verifications on different loop filter designs, the proper initial settings for the two resistors are $R_8 = R_6 R_4 / R_5$ and $R_9 = 1.3 R_8$.

Figure 7.1 Schematic diagram of the proposed carrier modulation topology for 2nd-order loop filter Class-D amplifier.

Figure 7.2 Reduction of timing errors using proposed quadratic carrier.

Compared with conventional PWM, only four additional components are required—three resistors (i.e. R_7 , R_8 and R_9) and one capacitor (C_4). The proposed design therefore has modest hardware overhead as compared to [11, 47]. An output spectrum of the proposed design is given in Figure 7.3. The frequency and modulation index of the input signal are set to 5 kHz and 0.7, respectively. The plot verifies that the remaining intrinsic harmonics are very small compared to the fundamental frequency component. The simulated THD is 0.0046%.

Figure 7.3 Output spectrum of proposed design based on MATLAB simulation.

7.3 Analysis on the proposed topology

A normalized mathematical model of the proposed carrier modulation topology is presented in Figure 7.4. To simplify analysis, the op-amp and comparator are both assumed to be ideal. The model parameters are tabulated in Table 7.1; the passive components and the signals are referred to the circuit schematic of Figure 7.1, with $C_1 = C_2$ and $C_3 = C_4$.

Figure 7.4 Mathematical model of proposed carrier modulation topology.

Table 7.1 Mathematical model parameters of the proposed topology.

Model Parameter	Expression
c_1	$(\alpha / \beta) \cdot [2 / (R_2 C_1)]$
c_2	$1 / (2 R_3 C_1)$
c_3	$(R_5 / R_4) \cdot (2 / R_6 C_3)$
c_4	$1 / (2 R_7 C_3)$
K_1	$(R_6 / R_8) \cdot (R_4 / R_5)$
K_2	$(\alpha / \beta) \cdot [(R_1 R_4 R_6) / (R_2 R_5 R_9)]$
K_3	$(R_2 / R_1)(1 / \alpha)$

The full mathematical model for the complete design proves difficult to analyze to completion. The main obstacles are the varying carrier frequency and the increased complexity due to extra state variables for the quadratic carrier and the combined carrier modulating signal. Because practical applications are the prime concerns, it often turns out that a particular circuit topology or system implementation found widespread application long before it has been thoroughly analyzed. In this thesis, the analysis is limited to: (a) examining the low-frequency response of the proposed modulator; and (b) calculating the carrier frequency dependence on the magnitude of the input signal.

7.3.1 Carrier modulated pulse width modulator

To allow straightforward analysis, the carrier modulated pulse width modulator is isolated from the complete system and reproduced in Figure 7.5.

Figure 7.5 Mathematical model of the carrier modulated pulse width modulator.

The audible output of a pulse width modulator can be considered a combination of two parts: (i) low frequency response to the audio range input signal (e.g. constant gain for linear carrier design) and (ii) the high frequency response to the ripple signal (i.e., the sampling effect that causes aliasing error and is the source of the intrinsic harmonic distortion). Nevertheless, the low frequency response assists the negative feedback to partially suppress the created distortion. The low frequency response of the proposed modulator, i.e., from input $h(t)$ to its partial output $g_L(t)$, in the presence of a carrier modulating signal, $r(t)$, can be expressed as follows:

$$g_L(t) = \frac{1+r(t)}{2c_4} \sqrt{(1-r(t))^2 c_3^2 + 2c_3 c_4 (1-r(t)) h(t) + c_4^2} - \frac{1-r(t)}{2c_4} \sqrt{(1+r(t))^2 c_3^2 - 2c_3 c_4 (1+r(t)) h(t) + c_4^2} \quad (7.1)$$

where

$$h(t) = V_{int}(t) / \beta \quad (7.2)$$

$$r(t) = \frac{R_4 R_6}{\beta R_5 R_9} V_{in}(t) + \frac{R_4 R_6}{\beta R_5 R_8} V_{int}(t) \quad (7.3)$$

Equation (7.1) is strictly derived based on DC signals, but it should approximately hold for low frequency sinusoidal signals, similar to the technique reported in [11]. It is worthwhile to highlight that, unlike the conventional PWM, the transfer function, from $h(t)$ to $g_L(t)$, is no longer linear.

For this reason, the loop gain of the system cannot be plotted. Fortunately, numerical verification proves that the nonlinear response is able to provide additional gain at the harmonic frequency, which further suppresses the aliasing error generated by the high frequency response of the modulator.

The modulated carrier waveform, $v(t)$, and carrier modulating signal, $r(t)$, with respect to a sinusoidal input signal for the proposed design are illustrated in Figure 7.6. In order to examine the modulation effect of the carrier modulating signal on the high frequency carrier, the input signal frequency and modulation index are set to 20 kHz and 0.7, respectively. Note that the carrier modulating signal is 180° out of phase with the input signal. This indicates that the linearly combined carrier modulating signal is dominated by the loop filter output signal but with its fundamental input frequency components reduced by the feedforward input signal. Figure 7.6 also illustrates that the low frequency components of the carrier modulating signal modulate the instantaneous switching frequency as well as the symmetry of the rising and falling intervals, whereas the high frequency ripple signal mainly affects the slopes of the rising and falling edges of the carrier.

Figure 7.6 Waveforms of modulated carrier, carrier modulating signal and input reference signal.

7.3.2 Variation range of the carrier frequency

To predict the input-signal dependence of the modulated carrier wave frequency, a mathematical model has been developed through collaboration with Prof. Cox, similar to that reported in [68, 73]. However, the greater complication of the present design precludes the derivation of an explicit formula for the modulated carrier frequency. Instead, we are able to reduce the problem to three coupled nonlinear equations that involve: (i) this frequency, (ii) the time interval, D , between the start of a carrier wave period and the switching from +1 to -1 of the output, $g(t)$, and (iii) the voltage at the output of the second integrator in the carrier wave modulator, sampled at the start of a carrier wave period. These three equations may be written, respectively, as quadratic, cubic and quartic equations for D , with highly algebraically complicated coefficients. For specific parameter values, these equations are then solved numerically.

Figure 7.7 illustrates the carrier switching frequency variation with respect to the duty cycle. It is evident that the mathematical model has perfectly predicted the variation of the switching frequency. Furthermore, the switching frequency of the proposed carrier modulation topology drops by ~20% with respect to the idle frequency when the duty cycle is at 0.05 or 0.95. This decrease in frequency is substantially lower than the ~64% drop in the self-oscillating topology reported in [65].

Figure 7.7 Carrier switching frequency variation with respect to duty cycle.

Referring to [89], for stereo amplifiers on the same silicon die, the intermodulation between the two channels can be prevented by creating an offset between the switching frequencies of the left and right channels. For instance, the idle switching frequencies are set to 300 kHz and 350 kHz for a two-channel application. When input signals with the same magnitude are present, both the switching frequencies drop by the same amount and the offset remains unchanged, so that the intermodulation between the two channels does not fall into the audio range. However, when the difference between the magnitudes of the two input signals is large, the carrier frequency offset between the two channels will be small and the intermodulation products will probably become audible for the self-oscillating topology, due to its large carrier frequency variation range. By contrast, with a much smaller range of carrier frequency variation, the proposed design can achieve a much better prevention of audible intermodulation distortion in multi-channel applications.

7.4 Implementation on AD-modulated Class-D amplifier

The proposed design was first simulated using MATLAB to theoretically verify the proposed topology. The circuit was subsequently simulated in HSPICE using practical component models to ensure that the proposed topology was practically realizable. Finally, the proposed circuit was built on Printed Circuit Board (PCB) using discrete components, as shown in Figure 7.8; the values of the components are listed in Table 7.2.

Table 7.2 Circuit parameters of the proposed AD-modulated design.

Parameter	Value
V_{DD} , R_{Load} , L , C	3.3 V, 8 Ω , 33 μ H, 0.242 μ F,
C_1 , C_2 , R_1 , R_3 , R_2	330 pF, 330 pF, 14 k Ω , 3.09 k Ω , 24.3 k Ω
C_3 , C_4 , R_7 , R_8 , R_9	330 pF, 330 pF, 3.65 k Ω , 5.37 k Ω , 8.02 k Ω

Figure 7.8 Hardware implementation with consideration for linear and modulated carrier tests.

By disconnecting the proposed carrier modulation circuit and feeding a triangular carrier signal using an external function generator, a linear carrier 2nd-order Class-D amplifier can be realized on the same PCB, for the purpose of comparison with the proposed design. In this hardware measurement, the National Instrument (NI) equipments combined with the accompanied NI

Sound and Vibration Measurement Suite was employed. Since this measurement suite is developed by NI, its accuracy is guaranteed. To ensure that the testing equipments are set up properly, the measurement results were compared with the results collected from the SR770 FFT network analyzer from Stanford Research System. The results from these two equipments were verified to be compatible.

Figure 7.9 depicts the THD performance against the input signal frequency of the 2nd-order Class-D amplifier for both the proposed modulated carrier and linear carrier. The dashed and dotted lines are the MATLAB and HSPICE simulation results, respectively, of the two designs, whereas the solid lines indicate the prototype measurement results. The results were measured at input frequencies ranging from 100 Hz to 6 kHz, and at modulation index equal to 0.7. It is evident from Figure 7.9 that the THD of the Class-D amplifier using the proposed topology has improved by ten times over a wide range of input signal frequency, the measured THD being about 0.01% at 6 kHz. The measured THD of the proposed design at low input signal frequency is roughly 0.0007%. This is attributed to the residual harmonics contained in the input signal and also the circuit ground noise.

Figure 7.9 THD (%) against input audio signal frequency.

Figure 7.10 shows the THD versus the modulation index of the 2nd-order Class-D amplifier for both the proposed modulated carrier and linear carrier. The modulation index ranges from 0.1 to 0.9 and the input signal frequency is 5 kHz. Both the simulation and measurement results indicate that the proposed topology is able to improve the THD by almost ten times at all modulation indices, compared to its linear carrier counterpart. The discrepancy between the simulation and measurement results at low modulation index is mainly due to the nonlinearity of the power transistors and the non-ideality of the carrier generator that produced the additional harmonic components, which become significant when the intrinsic harmonic distortion is mitigated by the proposed topology. The op-amp selected for hardware testing has a DC gain of 120 dB and gain-bandwidth product (GBW) equal to 50 MHz (the same specifications were employed in the HSPICE simulation). Through further verification, it is confirmed that there is no significant degradation in the performance of the proposed design if a modest low power op-amp is deployed—DC gain = 100 dB and GBW = 10 MHz.

Figure 7.10 THD (%) versus modulation index of the input signal.

A performance comparison between the proposed design and some recently reported works is tabulated in Table 7.3.

Table 7.3 Performance comparison on proposed carrier modulation topology and recently reported work.

Parameters	[11] /2006	[90] /2010	[47] /2011	[36] /2008	[70] /2008	[91] /2009	This work
Architecture	MAE	PWM	UPW M	$\Delta\Sigma$	SMC- SO	SMC- SO	CM
Carrier Frequency (f_{sw}) [kHz]	~350	150 ~580	1000	3200	1000	450	~310
Supply Voltage [V]	-	3.6	5.5	3	3.6	2.7	3.3
Load[Ω] /configuration	8/SE	8/BTL	4/BTL	32/SE	8/BTL	8/BTL	8/SE
P_{out} (THD:1%, f_s :1 kHz) [W]	~250	0.65	3.1	-	-	0.25	0.18
THD+N(%) @ 1 kHz, 50% P_{out}	0.015	0.02	0.0012	0.022	0.0022	0.02	0.0026
PSRR @ 217 Hz [dB]	-	72	96	-	70	77	90

The measured THD+N (%) of 0.0026 is appreciably greater than the THD (%) (=0.0007) of Figure 7.9. This is mainly due to the coupled AC power noise within the test environment. The AC power noise may be injected from the high impedance points of the circuit. The result substantiates that the linearity performance of the proposed design is state-of-the-art, and with a low switching

frequency. The reported output power is low due to single-ended output configuration. A better indicator for THD performance is the modulation index and the proposed design approaches THD of 1% at almost full signal swing. Although the design is here implemented using low supply voltage, due to limitations on hardware and testing equipment, the proposed topology is applicable to high voltage designs and has the additional advantage of power efficiency due to its modest switching frequency.

7.5 Implementation on BD-modulated Class-D amplifier

As explained in Chapter 5, BD-modulation is essential for filterless Class-D amplifier and becomes popular for portable devices. In addition, the analysis in Chapter 5 indicates that the fully-differential BD-modulated design has different intrinsic distortion behavior as compared to the AD-modulated design. In this section, the proposed dual-feedforward carrier modulation topology is implemented on a fully-differential BD-modulated Class-D amplifier with analog feedback. The study confirmed that the proposed topology not only works in AD-modulated design, but also BD-modulated design, which further extends its application.

7.5.1 Mathematical model

The effectiveness of the proposed design on fully-differential BD-modulated Class-D amplifier was first verified on MATLAB Simulink using a normalized model, as shown in Figure 7.11. The 2nd-order loop filter is designed based on the criterion derived in Chapter 6 for AD-modulated Class-D amplifier, since the criterion that prevents chaotic operation for BD-modulation is still in

investigation—it seems that BD-modulation has a higher immunity from chaotic operation. As a result, the parameters, c_1 and c_2 , are set to 4.988e5 and 4.9034e5 respectively. The switching frequency of the carrier generator is set to 250 kHz (before applying the feedforward signals) and hence $c_3 = 1\text{e}6$. Through numerical tuning process, the optimized parameters for the modulated carrier generator are set to $c_4 = 441306$, $k_1 = 1.0153845$ and $k_2 = 0.603306$.

Figure 7.11 Mathematical model of proposed carrier modulation topology on BD-modulated design.

The transfer functions of the 2nd-order loop filter and the 2nd-order integrator inside the carrier generator of Figure 7.11, are derived in Eqns. (7.4) and (7.5), and the bode diagrams are plotted in Figure 7.12.

$$\frac{h(t)}{g(t)} = \frac{h(t)}{s(t)} = -c_1 \cdot \left(\frac{s + c_2}{s^2} \right) \quad (7.4)$$

$$\frac{v(t)}{r(t)} = -c_3 \cdot \left(\frac{s + c_4}{s^2} \right) \quad (7.5)$$

As shown in Figure 7.12, the transfer function of the 2nd-order integrator inside the carrier generator closely follows that of the loop filter and the

location of the zeros for these two transfer functions are quite close to each other.

Figure 7.12 Bode diagram of the loop filter and the integrator transfer function.

7.5.2 Circuit architecture

Figure 7.13 shows the circuit architecture of the proposed BD-modulated Class-D amplifier. The analog building blocks for the main signal path are identical to a conventional fully-differential design, including a fully-differential op-amp, two identical comparators and two power stages. The proposed modulated carrier generator is the same as that for single-ended design, except that circuit implementation is modified for the sake of the on-chip implementation. The load is in Bridge-Tied-Load (BTL) configuration to double the output swing.

Figure 7.13 Architecture of the proposed BD-modulated Class-D amplifier.

The expressions of the model parameters (indicated Figure 7.11) in terms of the passive components and the signals (given in Figure 7.13) are listed in Table 7.4, where $v_{in}(t) = v_{ip}(t) - v_{im}(t)$ and $V_T = (V_{TH} - V_{TL}) / 2$.

Table 7.4 Model parameters of the proposed design in Figure 7.11.

Model Parameter	Expression
c_1	$(V_{DD} / V_T) \cdot [1 / (R_2 C_1)]$
c_2	$1 / (2 R_3 C_1)$
c_3	$(2 V_{DD} / V_T) \cdot (2 / R_6 C_2)$
c_4	$1 / (2 R_7 C_2)$
K_1	$(R_6 / R_4) \cdot (2 V_T / V_{DD})$
K_2	$(R_1 R_6) / (R_2 R_5)$
$s(t)$	$(R_2 / R_1) (1 / V_{DD}) \cdot v_{in}(t)$

The transistor-level circuit design is based on the Global Foundry 0.18- μm CMOS process. All circuit blocks are powered by 3.3-V supply voltage and the load resistance is set to 8 ohm. The component values of the proposed BD-modulated Class-D amplifier are summarized in Table 7.5.

Table 7.5 Component values of the proposed design in Figure 7.13.

Parameter	Value
$V_{DD}, R_{Load}, V_{TH}, V_{TL}$	3.3 V, 8 Ω , 2.475 V, 0.825 V
C_1, R_1, R_2, R_3	10 pF, 400.962 k Ω , 801.924 k Ω , 101.97 k Ω
C_2, R_4, R_5, R_6, R_7	10 pF, 196.97 k Ω , 331.506 k Ω , 400 k Ω , 113.3 k Ω

Figure 7.14 illustrates the typical signal waveforms of the proposed circuit design in Figure 7.13. It contains the PWM signals at the output of the two bridge halves (i.e., V_{PWMp} and V_{PWMm} in the top two slots), voltages at the input of the fully-differential amplifier (i.e., V_{fbp} and V_{fbm} in the third slot), the modulating signals at the output of the fully-differential amplifier, and the carrier signal (i.e., V_{modp} , V_{modm} and V_{tri}). For the sake of observing the high-frequency switching signals, the input signal frequency is set to 20 kHz.

The fully-differential nature of the loop filter can work just fine in an AD-modulated loop where both the modulating signal and carrier of the two bridge halves have opposite phase. Hence, no common-mode voltage appears at the input of the fully-differential amplifier. However, in a BD-modulated loop, only the modulating signals have opposite phase whereas the carriers are in-phase. As the fully-differential integrator has infinite common-mode input impedance, it can only realize a virtual ground at the input for differential mode signals. This means that there is a significant common-mode voltage at the integrator

input (see the third slot in Figure 7.14), which has the same frequency as the carrier signal. For proper operation, the differential amplifier (i.e., X_1 in Figure 7.13) must have an extremely high input common mode rejection ratio (ICMRR), especially at high frequencies. This is a practical design issue when applying fully-differential loop filter to a BD-modulated design.

Figure 7.14 Typical signal waveforms of the proposed design in Figure 7.13.

7.5.3 Circuit implementation

In this section, details on transistor-level implementation of the circuit blocks, as indicated in Figure 7.13, will be presented. Except special indication, all the results presented in Section 7.5.3 are based on Cadence Spectre simulation.

7.5.3.1 Fully-differential operational amplifier(X_1)

Recall that the loop filter based on a fully-differential design has three basic advantages: a higher immunity to environmental noise (e.g. substrate noise and output switching noise), a wider dynamic range, and a good common-mode rejection ratio. The dynamic range is increased by 6 dB as a result of the outputs being equal in magnitude but opposite in phase.

Figure 7.15 depicts the circuit schematic of the fully-differential op-amp. A folded-cascode, two-stage circuit topology is adopted. The folded-cascode first stage boosts the DC gain and achieves a wide input common-mode range. The common-source transistor of the second stage ensures a wide output signal swing. The input pair is implemented using PMOS devices since these devices have lower flicker noise than NMOS devices, and provide better isolation from the substrate due to the PMOS N-well.

Figure 7.15 Schematic of fully-differential operational amplifier.

To stabilize the average or common-mode output level, the common-mode feedback (CMFB) amplifier is required to set one of the two conflicting bias

voltages in the first stage. Bear in mind that, as listed in [92], the main requirements of CMFB amplifiers are: (1) high speed; (2) matching; (3) output swing (limited by the output swing of the differential-mode amplifier and the input range of the common-mode amplifier) and (4) low power consumption. As the CMFB amplifier is always connected in unity-gain feedback, the stability of the loop is critical [92].

In this design, two 40-k Ω resistors are engaged to cancel out the differential signals and sense the common-mode output voltage. This common-mode voltage sensing technique ensures a high differential output signal swing, but compromises the gain of the second stage. In addition, a small capacitor (i.e., 0.173 pF) in parallel with each resistor, R_1 , is required to form a feedforward path to compensate the pole at the input of the CMFB amplifier. The two NMOS transistors in the CMFB amplifier are both diode-connected to remove the high impedance node at the output of the CMFB amplifier. This is essential to ensure the stability of the CMFB loop. The accuracy of the common-mode output voltage with respect to the reference voltage (i.e., V_{cm}), is determined by the matching of the bias currents between the first stage of the differential amplifier and the CMFB amplifier.

Figure 7.16 plots the frequency response of the fully-differential op-amp at typical condition based on schematic simulation. The low-frequency differential gain of the circuit is 120 dB. When driving a 5-pF capacitive load at each output port, the gain bandwidth (GBW) is equal to 78 MHz and the phase margin is 80 degree. The low-frequency gain of the first stage is 80 dB (dashed lines in Figure 7.16), whereas the second stage contributes extra 40 dB gain to the overall gain of the fully-differential op-amp. Including the bias circuit, the

quiescent current consumption of the fully-differential op-amp is found to be 2 mA.

Figure 7.16 Frequency response of the fully-differential op-amp.

Figure 7.17 illustrates the frequency response of the CMFB loop. The phase margin is 62 degree and GBW is 77.4 MHz. The high CMFB loop gain is preferred so as to achieve a high ICMRR.

Figure 7.17 Frequency response of the CMFB loop.

The Monte Carlo simulation results (100 samples) in Figure 7.18 evaluates the common-mode gain of the fully-differential amplifier with consideration for both process and mismatch variations. In the worst case, the common-mode gain is -21.4 dB and it remains flat up to 1 MHz. Consequently, the ICMRR at the carrier switching frequency of 250 kHz is around 70 dB.

Figure 7.18 Common-mode gain of the fully-differential amplifier.

Some alternative fully-differential operational amplifier circuit structures can be found in [48]. In addition, a discussion on alternative circuit topologies for the loop filter can be found in [81, 82]. In [81], a differential operational amplifier (OPA) (as the first stage) and a differential operational transconductance amplifier (OTA) (as the second stage) are used to implement a 2nd-order loop filter. This topology aimed to achieve a high ICMRR. Furthermore, as demonstrated in [82], when the input resistors are replaced by a differential OTA, the common-mode voltage at the input of the fully differential loop filter can be regulated by the output of the OTA through a common-mode feedback circuit.

7.5.3.2 Comparator for PWM generator (X_2 and X_3)

Designing a comparator usually begins with considering input common-mode range, power dissipation, propagation delay, and comparator gain. As a pulse width generator, the inputs of the comparator are the modulating signal from the output of the loop filter and the triangular carrier signal. The input common-mode range of the comparator is equal to the carrier oscillating swing, from 0.825 V (i.e. $V_{DD}/4$) to 2.475 V (i.e. $3V_{DD}/4$). A short propagation delay is essential to ensure a stable closed-loop operation. In addition, it was found through simulation, a long propagation delay will significantly degrade the linearity performance of the proposed design.

Consequently, the comparators (X_2 and X_3 , in Figure 7.13) are designed based on a high-performance comparator circuit structure presented in [93], which consists of three stages: the input preamplifier, a positive feedback or decision stage, and an output buffer. The complete circuit structure is presented in Figure 7.19. The pre-amp stage amplifies the input signal to improve the comparator sensitivity, which is to increase the minimum input signal with which the comparator can make a decision, and isolates the inputs of the comparator from the switching noise (a.k.a. kickback noise) coming from the positive feedback stage. The positive feedback stage determines which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal. The inverter at the output is specially sized to switch at the centre of the output range of the buffer amplifier. If its following gate driver stage is located far from the comparator, an additional inverter-chain buffer stage should be inserted after the comparator.

Figure 7.19 Schematic of the proposed comparator with rail-to-rail ICMR.

As seen in Figure 7.19, both the PMOS and NMOS diff-amps feed the decision circuit. The input common-mode range (ICMR) therefore encompasses both supply rails. The rail-to-rail ICMR is desired due to the wide input signal swing and ensure a good performance in case of supply voltage drop, which is essential for future application where the Class-D amplifier is directly hooked on the battery of a portable devices. The DC current consumption of the comparator is 500 μA , including the bias circuit.

The variation on the comparator gain and offset at different input common mode voltages is verified through schematic simulation, as shown in Figure 7.20. The results are simulated in typical condition. The horizontal axis presents the sweep range of positive input signal around the common-mode input voltage levels. Therefore, the deviation of the peak gain from the zero origin presents the offset. As demonstrated in Figure 7.20, the gain of the comparator is larger than 128 dB and the systematic offset is less than 82 μV .

Figure 7.20 Gain and offset variation of the comparator in Figure 7.19. The input common mode voltage sweeps from 0.825 V to 2.475 V.

Figure 7.21 presents the Monte Carlo simulation results (100 samples) for evaluating the input-referred offset voltage of the comparator with consideration for both process and mismatch variations. The results indicate that the random offset due to process and parameter mismatch dominates the overall offset of the comparator. For instance, in the worst case of the simulation, the offset is 22.47 mV. Therefore, the layout of the comparator needs to be drawn symmetrically to minimize the random offset.

Figure 7.21 Offset voltage of the comparator in Figure 7.19.

The corner simulation results are listed in Table 7.6, in which the negative input is fixed at 1.65 V. The “condition” column lists the corner condition, temperature, and supply voltage (V_{DD}). The propagation delay is simulated based on a transient analysis by driving the positive input of the comparator 50 mV over the negative input, as specified in [93]. Note that the propagation delays at the rising- and falling-edge are very close.

Table 7.6 Corner simulations of the comparator in Figure 7.19.

Condition	Gain (dB)	Systematic Offset (μ V)	Prop. Delay [Falling] (ns)	Prop. Delay [rising] (ns)
FF, -40°C, 3.465V	130.6	141	1.369	1.405
Typ., 27°C, 3.3V	130	65	1.920	1.886
SS, 85°C, 3.135V	130.4	1	2.730	2.602
SF, 27°C, 3.3V	130.4	39	2.033	2.019
FS, 27°C, 3.3V	129	100	1.815	1.812

Some alternative circuit implementations of the PWM comparator can be found in [48]. In [48], a simple comparator was employed, consisting of a two stage op-amp and an inverter chain buffer.

7.5.3.3 Power Stage (X_4 and X_5)

Shown in Figure 7.22 is the design of the power stage—make up by a gate driver and a pair of power MOSFETs. The gate drive circuit is similar to that reported in [60]. It is employed to introduce a dead-time so as to prevent simultaneous conduction in the P-type and N-type power MOSFETs, thereby ensuring non-overlapping operation. A dead-time is necessary to avoid the risk of excessive switching transients and permanent device failure, caused by large shoot-through currents [94]. A large dead-time however increases the distortion level and causes voltage spikes at the output of the Class-D amplifiers, because of the large current flowing through the back-gate diode of the power MOSFETs during the dead-time period. Extra dead-time can be added and adjusted by inserting a “Delay” block (see dashed block in Figure 7.22). In this design, only the minimum dead-time is applied to minimize the distortion introduced.

Figure 7.22 Circuit schematic of the gate drive and power MOSFETs.

The W/L ratio of the n-type power MOSFET is $23116.8 \mu\text{m}/0.35 \mu\text{m}$ and the size of the p-type power MOSFET is three times larger than that of the n-type power MOSFET.

Figure 7.23 illustrates typical signal waveforms of the output stage, which contains the input and output PWM signal, i.e., V_{in} and V_{PWM} in the top slot, and gate voltages of the power MOSFETs, i.e., V_{gp} and V_{gn} in the bottom slot. The dead-times at the rising- and falling-edge are about 1.1 ns.

Figure 7.23 Signal waveforms of the output stage at (a) rising-edge; (b) falling-edge.

7.5.3.4 Operational amplifier inside the carrier generator (X_6)

The op-amp, i.e., X_6 in Figure 7.13, is a single output op-amp employed in the 2nd-order integrator inside the carrier generator. The positive input of the op-amp is connected to analog ground, $V_{DD}/2$, and thus the negative input is also virtually fixed at half supply voltage. The open-loop frequency response should exceed the frequency response of the 2nd-order loop filter.

Figure 7.24 shows the circuit schematic of the proposed two-stage op-amp. As the input common-mode voltage of the op-amp is fixed at half supply voltage, transistors M_{C1} through M_{C4} implement the telescope cascoding on the first stage to increase the low-frequency gain. The floating bias voltages for transistors M_{C1} through M_{C4} are realized by the transistors M_{B1} through M_{B7} . The common-mode input voltage is taken from the drain of M_{B1} and M_{B2} , and applied to the input of the n-channel cascode current mirror consisting transistors M_{B3} through M_{B6} plus the resistor R . The output of the current mirror provides the bias current for the MOS diode M_{B7} , which implements the floating bias for M_{C1} and M_{C2} . At the same time, the self-biased current mirror provides a fixed biasing voltage to M_{C3} and M_{C4} .

Figure 7.24 Schematic of the single-ended operational amplifier.

The output range of the op-amp is the carrier signal swing. The total DC current consumption is 0.9 mA. The op-amp is designed to drive a 5-pF capacitive load and the miller capacitor is set to 1.56 pF. The figure of Merit, which is designed as $GBW \times C_L / I_{tot}$, is equal to 454. In typical condition, the DC gain is 132 dB, GBW is 78.6 MHz and the phase margin is 68 degree. Figure 7.25 illustrates the bode plots.

Figure 7.25 Bode diagram of the operational amplifier in Figure 7.24.

7.5.3.5 Comparators inside the carrier generator (X_7 and X_8)

The comparators used in the carrier generator are designed with minimized propagation delay time. One of the comparator input pin is fixed at reference voltages and the other input is connected to the carrier signal. The comparison proceeds around the reference voltages (i.e., at 0.825 V and 2.475 V). As a result, one of the comparators is designed with PMOS input transistors and the other uses NMOS transistors. The circuit schematics of these two comparators are given in Figure 7.26.

Figure 7.26 Comparators with: (a) PMOS differential input stage; (b) NMOS differential input stage.

The comparator gain and offset are investigated through a DC sweep surround the respective reference voltage, which are shown in Figure 7.27 and Figure 7.28. The horizontal axis is the sweep range of the positive input over the reference voltage at the negative input of the comparator. The corner simulation results are given in Table 7.7 and Table 7.8.

Figure 7.27 Gain and offset of the comparator in Figure 7.26(a). The input common-mode voltage is set to 0.825 V.

Figure 7.28 Gain and offset of the comparator in Figure 7.26(b). The input common-mode voltage is set to 2.475 V.

Table 7.7 Corner simulations of the comparator with PMOS input pair.

Condition	Gain (dB)	Systematic Offset (mV)	Prop. Delay [Falling] (ns)
FF, -40°C, 3.465V	94	+0.561	0.926
Typ., 27°C, 3.3V	94.8	+0.435	1.789
SS, 85°C, 3.135V	94.7	+0.299	1.895
SF, 27°C, 3.3V	93.5	+0.442	1.462
FS, 27°C, 3.3V	93.3	+0.479	1.034

Table 7.8 Corner simulations of the comparator with NMOS input pair.

Condition	Gain (dB)	Systematic Offset (mV)	Prop. Delay [Rising] (ns)
FF, -40°C, 3.465V	87.58	-1.289	0.719
Typ., 27°C, 3.3V	89.1	-0.97	1.350
SS, 85°C, 3.135V	90.2	-0.8	1.329
SF, 27°C, 3.3V	94.0	-0.686	1.004
FS, 27°C, 3.3V	84.98	-1.4	1.262

The slight offsets at the input of the comparators are preferred as they help to compensate the proportional delay of the comparators. The DC current consumption of the comparator with PMOS differential input pair is 645 μA when output is at logic “0”, and 84 μA when output at logic “1”. The DC current consumption of the comparator with NMOS differential input pair is 270 μA when output at logic “1”, and 108 μA when output is at logic “0”. The beauty of this carrier generator circuit (see Figure 7.13) is that the comparators, X_7 and X_8 stay at their low power consumption stage most of the time (i.e. the output of the comparator with PMOS input pair remains at logic “1”, whereas the output of the comparator with NMOS input pair stays at logic “0”), and only very narrow pulses are generated at their outputs when the carrier signal approaches the respective reference voltage.

7.5.3.6 Current Reference

Figure 7.29 presents the circuit schematic of the current reference. The transistors, MA1 to MA4, form the differential amplifier to force equal voltages at the gates of M_1 and M_2 . The design is adopted from [93]. Alternatively, the

current reference can be taken from the off-chip circuit, which is simple to design and the bias current can be easily adjusted.

Figure 7.29 Current reference using the beta-multiplier.

7.5.4 Layout of the chip

The layout of the chip is illustrated in Figure 7.30. The red rectangular line cycles the analog controller blocks, consisting the fully-differential op-amp, the comparators, current reference and the proposed modulated carrier generator. The controller blocks only occupy a small area, as compared to the power stage. The first-round fabricated chip did not work functionally. Through debugging, the malfunction of the chip is probably due to a mistake in the design of the fully-differential operational amplifier. The circuit schematic presented in Section 7.5.3 has corrected the mistake. However, due to time and financial limitation, the second-round fabrication has not been scheduled.

Figure 7.30 Layout of the proposed BD-modulated 2nd-order closed-loop Class-D amplifier.

7.5.5 Simulation results

In this section, the simulation results of the proposed BD-modulated 2nd-order closed-loop Class-D amplifier are presented. The simulation results for a conventional linear carrier design are also included for comparison. The designs are simulated in both MATLAB (using Simulink) and Cadence (using Spectre). In MATLAB simulation, the power stage is modeled as ideal switch and the linear blocks are represented by their transfer functions, whereas in Cadence schematic simulation, the circuit is implemented in transistor-level based on the designs presented in Section 7.5.3.

The THD performance against the input signal frequency is provided in Figure 7.31. The modulation index of the input signal is fixed at 0.7. The input signal frequency is from 1 kHz to 6 kHz. The MATLAB simulation indicates that the proposed design improves the THD performance by more than 10 times in a wide frequency range. The close match between the Cadence and MATLAB simulation results for linear carrier design proves that the intrinsic harmonic distortions dominate the performance of a conventional BD-modulated Class-D amplifier. The Cadence simulation results for the proposed design are significantly higher than the MATLAB simulation results. The mismatch indicates that the linearity of the proposed design is dominated by the practical circuit performance of the building blocks of the Class-D amplifier. Through verification in Cadence simulation, it was confirmed that the delay of the comparators inside the PWM generator (i.e. X_2 and X_3 in Figure 7.13) and the inserted dead-time for the power stage are the main sources of the added distortion in the circuit implementation.

Figure 7.31 THD vs. Input signal frequency at $M_{in} = 0.7$.

Figure 7.32 presents the THD performance against the modulation index of the input signal. The modulation index ranges from 0.1 to 0.9 and the input signal frequency is set to 3 kHz, so that the high-order harmonic distortions are included. The THD results are calculated based on all the harmonics within the audio range (up to 20 kHz). Again, for conventional linear carrier design, the MATLAB and Cadence simulation results match well when the modulation index of the input signal is larger than 0.3. At low modulation index, the intrinsic distortion is insignificant (proven earlier in Chapter 5), and the linearity of the Class-D amplifier is mainly determined by the circuit noise and the performance of the power stage. MATLAB simulation verified that the proposed design achieves a significant reduction in intrinsic distortion, especially in the middle range of the signal swing. The Cadence simulation results of the proposed design are higher than the MATLAB simulation results, but the improvement on linearity performance as compared to linear carrier design is still considerable.

Figure 7.32 THD vs. Modulation index of the input signal at $f_{in} = 3$ kHz.

Recall that, the noise of the fully-differential integrator dominates the noise floor of the Class-D amplifier [48] and has to be optimized to meet the SNR requirement. In addition to the thermal noise, flicker noise in MOS transistors can result in a serious noise component when referring to the op-amp input. A common technique for mitigating the effect of flicker noise is to increase the size of current sources as well as input transistors at the first stage. For future design, noise performance of the fully-differential amplifier should be considered.

7.6 Summary

In this chapter, the proposed dual-feedforward carrier modulation topology for achieving significant reduction in the intrinsic harmonic distortion of a closed-loop 2nd-order loop filter Class-D amplifier is presented. The input signal and loop filter output signal are employed to modulate the 2nd-order carrier. The effectiveness of this topology is evident from the dramatically reduced intrinsic harmonic distortion. When implemented on AD-modulated Class-D amplifier, the measured THD is less than 0.01% for input frequency of up to 6 kHz, and has an idle carrier frequency of 310 kHz. The proposed topology is also proven to be effective in fully-differential BD-modulated Class-D amplifier. The transistor-level implementation of the circuit architecture has been demonstrated.

Although the proposed design involves a 2nd-order carrier generator and hence consumes more power as compared to self-oscillating designs, the low switching frequency of the proposed design guarantees a low switching loss, which is extremely important in high power devices, to ensure higher overall

efficiency. Furthermore, the switching frequency of the proposed design only varies in a narrow range and helps to suppress the audible intermodulation distortion in multi-channel applications.

Chapter 8 High-voltage driver for acoustic telemetry transmitter

This chapter presents a high-voltage (HV) driver for piezoelectric acoustic transducer, designed to operate up to 260°C. The driver is fabricated using the 1.0- μm Silicon-on-Insulator (SOI) CMOS process, and is targeted to drive a stack of piezoelectric discs modeled as a capacitive load of 0.3 μF , with a broadband signal from 600 Hz to 1.2 kHz. To ensure stability, the driver is designed as an open-loop system, comprising a dead-time controller, level shifters, pre-drivers and power MOSFETs. The performance of the driver is investigated up to 260°C, at way beyond the specified process limits of 225°C. The experimental results also validated the functionality of the proposed high-voltage driver for voltages up to 60 V. This work is a collaboration with Mr. Muthukumaraswamy Annamalai Arasu and Dr. Minkyu Je, of the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore.

8.1 Introduction

High temperature electronics are essential in modern oil and gas industry. In the oil drilling services industry, an applications that demands high temperature electronics is the Measurement While Drilling (MWD). It demands electronics that operate at $> 225^\circ\text{C}$, in order to make exploration of deeper reservoirs

possible. While drilling, data such as temperature, pressure and properties of the earth formation near the drill bit are collected by various sensors and are transmitted to the surface to facilitate controlled drilling operation. The ambient temperature in deep-well conditions are above 200°C and increases with the depth of the well. Standard bulk silicon technology is not suitable in this application due to the large junction and sub-threshold leakages above 150°C. The SOI process is a potential candidate for high temperature application due to their much lower leakage current resulting from their isolated thin bulk region. In addition, the threshold voltage variation with temperature is smaller in SOI devices compared to their bulk-CMOS counterparts [95]. SOI also provides improved latch-up immunity which improves reliability of the circuit operation at higher temperature [95]. Although most of the commercial SOI processes are specified up to 225°C, it is reported in [96] that SOI process can be used up to 400°C, at least for a short period (e.g. 300 hours).

Acoustic telemetry using the drill string as the acoustic transmission channel has been pursued for many years in the oil drilling industry to improve the data rate over the <10 bps offered by present mud pulse telemetry systems. A drill string is composed of many segments of hollow drill pipes that are joined together by a threaded pin and box joint. The transmitter of the telemetry system is housed in a Bottom Hole Assembly (BHA) that sits above the drill collar and the drill bit. The system diagram of the downhole transmitter is illustrated in Figure 8.1. The acoustic energy is usually generated by a stack of piezoelectric discs that launch extensional (axial) stress waves that propagate through the drill string to the surface [97]. Thin piezoelectric discs are interleaved with metallic terminals and stacked up with alternate terminals in

the stack connected together to form the two electrical terminals of the acoustic transducer. For our frequencies of interest, the piezoelectric stack is electrically modeled as a capacitor. The whole transmitter is placed near the drill bit and powered by battery. The challenge of the driver design is the high ambient temperature and the high output voltage required to drive the transducer. Furthermore, a higher efficiency is always desired to extend the battery life.

Figure 8.1 Typical acoustic telemetry system for oil exploration application [98].

The candidate is tasked to design a SOI-based high-voltage (HV) driver for the piezoelectric transducer for operating up to 260°C ambient temperature. The targeted operating voltage of the transducer driver is 60 V. The design focus of the work is on the robustness of the circuit across a wide temperature range and the ability to fit the Class-D type power amplifier operation with the reactive load, which is desired, in order to achieve high data rate and power efficiency under high supply voltage.

This chapter is organized into four main sections. Following this introduction, Section 8.2 describes the proposed high data-rate acoustic telemetry system for well drilling application. Section 8.3 discusses the detailed circuit design of the HV driver. Section 8.4 presents the measurement results. A summary is then drawn in Section 8.5.

8.2 Acoustic telemetry for well drilling application

There are very limited reported works in circuit or system design in oil well drilling application, as it is a niche application. In the only reported work [97], a transformer is deployed to generate a high voltage signal across at the capacitive acoustic transducer with the secondary winding resonating with the capacitance of the transducer at the intended carrier frequency. However, as the capacitance of the piezoelectric transducer varies with temperature and externally applied pressure, a dedicated control system was required to ensure the inductance is tracking this variation and maintain the resonant operation. Moreover in a resonant mode, only one carrier is employed for telemetry which limits the data rate to about 20 bits per second.

The nearly regular periodic structure of drill string, consisting of alternating pipe segments and joints imposes an alternating passband and stopband structure on the frequency response, similar to that of a comb filter. To increase the data rate, multiple signal carriers can be employed to fully utilize the available passbands of the drill string acoustic channel. A multi-carrier signal will have a higher peak to average ratio, demanding linear amplification in order to avoid intermodulation between the carriers and harmonics. A linear driver has low power efficiency leading to heat generation and shorter battery life.

As a potential solution, the Class-D type switching power amplifier is proposed. Class-D amplifier is rarely used in wireless communication application, as it requires an even higher switching frequency than the transmitting carrier frequency. However, in this application, since the signal

carrier frequency is low (up to 2 kHz), it is feasible to pulse width modulate (PWM) the signal with a modest switching frequency (e.g. 50 kHz) for feeding into the Class-D power amplifier. Figure 8.2 illustrates the system architecture of the proposed down hole transmitter system.

Figure 8.2 System architecture of acoustic transmitter for well drilling application.

The piezoelectric transducer stack needed to generate $>5W$ of acoustic power is approximately 2 meter in height, which has a capacitance in the order of a few microfarads. As shown in Figure 8.2, a parallel architecture is proposed in which multiple drivers are distributed along the transducer and drive each section in parallel. An inductor, L , is added to the output of each driver to form a low-pass filter with the load capacitor (piezo stack section) to recover the desired low frequency modulated carrier signals and for minimizing ripples at the switching frequency. The HV driver presented serves the Class-D amplifier

function. In this topology, resonant mode operation is not required. The proposed design can therefore tolerate the capacitance change of the piezoelectric transducer due to the varying temperature. In this chapter, a Class-D HV driver circuit is described to fulfill the requirement of the high data rate acoustic telemetry system. The driver is powered by a 60-V supply and capable of working up to 260 °C without any cooling accessories.

8.3 High-voltage driver circuit

Figure 8.3 shows the circuit level block diagram of the designed HV driver with off-chip charge pump circuit. The monolithic chip contains an adjustable dead-time controller, two level shifters, gate drivers and a half-bridge output stage. The input signal of the HV transducer driver would be a PWM signal (i.e., a 5-V pulse signal with variable pulse width) to fit the multi-channel high data rate transmitter architecture. The output signal is an amplified PWM signal with large current sourcing and sinking capability. The switching mode operation ensures high power efficiency and reduces heat generation on the chip, which is important for this application.

Figure 8.3 Block diagram of the HV transducer driver.

To ensure the system operate robustly in a wide temperature range, a series of design techniques are applied. First, the dead-time controller is designed based on zero temperature coefficient biasing technique. Second, the level shifter is designed with a SR latch. This is to prevent the output of the high-side level shifter from being affected by the fast ramping of the output signal. Although the level shifter is not necessary for the lower-side, it is added to ensure a comparable delay with the upper-side pre-driver.

8.3.1 Power stage and charge pump

The half-bridge output stage is built using a pair of n-type thin-oxide lateral DMOS transistors, which can sustain a high drain-source and drain-gate voltage (i.e., 90 V) but low gate-source voltage (i.e., 5 V). The all-NMOS (M_H and M_L) structure is employed as it minimizes the size of the output stage as compared to PMOS plus NMOS counterpart. This is even more essential for HV application, as the lateral DMOS is significantly larger than standard MOS due to the extended drain region. As is shown in Figure 8.8, the power MOSFETs occupied more than two-thirds of the total chip area.

In order to turn-on the high-side N-type DMOS, a floating voltage is required which is ~ 5 V higher than the voltage level of the output signal. This is achieved through a bootstrap capacitor (i.e. C_B) based charge pump establishing a 5 V boost above the output voltage. This floating voltage is used by the upper-side level shifter and the gate driver and ensures the gate voltage of the M_H is 5 V higher than its source voltage whenever M_H is turned on.

8.3.2 Dead-time controller

To ensure reliability and reduce power consumption of the chip, it is important to maintain complementary turning ON and OFF operation of the two transistors in the output stage. The temperature independent dead-time controller circuit reported in [99] has been implemented to generate two non-overlapping copies of the control logic signals (inp_H and inp_L). Figure 8.4 shows the schematic of the dead-time controller circuit as well as the transistor level adjustable delay line circuit. The working mechanism is to inject a temperature-independent phase lag to the rising-edge of each control signal.

Figure 8.4 Adjustable dead-time controller circuit: (a) typical circuit structure; (b) current-controlled delay line.

The inverting-buffers at the output of the dead-time controller are used to shape the control signal and drive the large input capacitance of the level shifter. The adjustable delay line is comprised of a chain of current-starved inverters.

The charging/discharging current can be adjusted by the external resistor, R_{ext} . The zero-temperature coefficient biasing is applied in this design, where drain current reduction due to mobility degradation is perfectly compensated by the drop in threshold voltage. Consequently, the drain current (10 μA) of the transistors are independent of temperature variation. When the circuit is biased at zero temperature coefficient point, the designed dead time is 55 ns.

8.3.3 Level shifter

The level shifter of Figure 8.5 is used to transfer the 0-V to 5-V logic level signals to voltage levels able to drive the upper-side power MOSFET. When the input signal, V_{in} , rises from 0 V to 5 V, the N-type DMOS transistor, M_1 , turns on. The voltages at nodes n_1/n_3 are then pulled down correspondingly, which triggers the flip of the upper-side latch formed by transistors M_5 - M_6 . The cascode P-type DMOS transistors, M_3/M_4 , are used to protect the floating thin-gate transistors sitting between the V_{out} and V_{boost} rails. The transistors, M_7/M_8 , are employed as active clamping to prevent voltage at nodes n_3/n_4 to drop below the upper-side “ground”, due to the leakage current through M_3/M_4 . For proper DC operation, the transistors M_1 and M_3 should be sufficiently large to flip the latched state at node n_3/n_4 , and the W/L ratio of M_7 should be much smaller than that of M_5 . By symmetry, M_2 , M_4 , M_6 and M_8 follow identical ratios as those of M_1 , M_3 , M_5 and M_7 .

The circuit topology is adopted from [100], but the circuit behavior and design emphasize are different. The “ground” rail of the upper-side level shifter is no longer a fixed voltage reference and instead connected to the output of the driver (V_{out}) that switches between 0 V and 60 V. The “power” rail of the upper-

side level shifter is also connected to a floating voltage, V_{boost} . The circuit topology is adopted because of its immunity to the fault logic switch during the fast ramping period of the driver output signal, as detailed in next paragraph.

Figure 8.5 Circuit schematic of high-voltage level shifter.

Figure 8.6 illustrates the transient signal waveforms of the level shifter. The first slot shows the upper-side level shifter output signal, V_{Q_H} (the blue dot-dashed line), voltage at node n_4 (the green solid line) and voltage at node n_2 (the purple dotted line). The second slot shows the driver output signal, V_{out} (the red dashed line) and level shifter input signal (yellow solid line). The operation of the upper-side level shifter is comprised of two phases. First step, the output of the level shifter is changed based on the input signal; second step, the output of the level shifter flats with the output signal, from 5V to 65V at the rising edge or from 60 V to 0V at the falling edge. The period between the two steps represents the delay of the gate driver block.

Illustrated in Figure 8.7 is a zoom-in view of these transient signals at the fast rising-edge of the driver output signal. As transistors M_6 and M_4 are unable to charge up the large parasitic capacitor at n_2 , a momentary change in logic level at n_4 to logic '0' will happen. The SR latch is hence employed to isolate the level shifter output from this fault logic change at node n_4 .

Figure 8.6 Demonstrative transient operation of the high-voltage level shifter.

Figure 8.7 Zoom-in view of the transient signals of the level shifter at the rising-edge of the driver output signal.

8.4 Measurement results

The driver circuit was fabricated in a 1.0- μm SOI CMOS process with Double-Diffused MOSFET (DMOS) transistor option for high-voltage application. Including bonding pads and ESD protection circuit, the chip occupies an area of 5.76 mm². Figure 8.8 shows the micro-photograph of the chip. The pads for the power rails of the power MOSFETs and the output node, i.e., PVDD, PVSS and OUTPUT, respectively, are located on the metal rails. Figure 8.9 displays the test set-up. All off-chip passive components are soldered on a separate printed circuit board (PCB), which is placed outside the temperature chamber. The chip is bonded in 28-pin dual-in-Line package. The thermal wires connect the chip and the PCB. The input PWM signal is generated from an AFG3022 function generator with external modulating signal from the signal generation port of the R&S audio analyzer.

Figure 8.8 Micro-photograph of the high-temperature driver IC.

Figure 8.9 Test board for high temperature test.

Figure 8.10 depicts the rising-edge and the falling-edge of the 60-V_{pp} 50-kHz output of the driver at different ambient temperatures (up to 260°C). The input signal is a pulse signal with 50% duty cycle. As shown in Figure 8.10, the driver performs well at high temperature without any significant degradation in switching behavior in terms of rising and falling times.

Figure 8.10 Typical output signal waveforms at different ambient temperatures without any cooling accessories.

Figure 8.11 shows a two-tone test of the driver at 260 °C. The input signal contains two frequency components, at 600 Hz and 900 Hz. The output fundamental components have equal magnitudes at 5.61 V_{rms}, and the 2nd-order intermodulation product at 1.2 kHz is 44 dB lower than the fundamentals. The low intermodulation distortion is essential for the three-channel data transmission, centered at 600 Hz, 900 Hz and 1.2 kHz.

Figure 8.11 Two-tone test at 260°C: (a) signal waveforms for input (low-pass) and output, and (b) frequency spectrum of the output signal.

Figure 8.12 shows the measured THD+N versus the ambient temperature. The driver was tested at signal frequencies of 600 Hz, 900 Hz and 1.2 kHz with modulation index equal to 0.9. The measurement frequency band is set to 300Hz ~5 kHz. The solid lines represent the output signal of the driver and the dashed lines indicate the input PWM signal generated from the function generator AFG3022. The close match between the measured THD+N at the input and output of the high-voltage driver proves that the linearity of the driver is very good.

Figure 8.12 THD+N (dB) versus the ambient temperature.

Figure 8.1 lists the variations of key parameters of the HV driver with respect to the ambient temperature. The THD+N performance is measured at input modulation index of 0.9, whereas the intermodulation distortion (IMD) performance is measured at modulation index equal to 0.3 for each signal tone. As indicated in Table I, the linearity of the driver keeps almost unchanged with increasing ambient temperature.

Table 8.1 Key parameters variation at different ambient temperatures.

Parameter	27°C	100°C	225°C	260°C
The rising time of the output (ns)	49.8	61.2	64.8	74.2
The falling time of the output (ns)	77.4	75.4	77.2	63.2
THD+N (%) at $F_{in} = 600\text{Hz}$	1.85	1.91	1.83	1.73
IMD (%) at $F_{in} = 600 \text{ \& } 900\text{Hz}$	0.63	0.64	0.64	0.64

8.5 Summary

This work presents a high-voltage driver circuit that fits the requirement for the proposed Class-D output multi-carrier acoustic transmitter architecture that is targeted for well-drilling application. The proposed driver has been verified to function properly in high temperature (up to 260°C) and is able to drive a 0.33 μF capacitive load with 60- V_{pp} output signal swing.

For future tapeout, the following suggestion may be considered. First, the on-chip decoupling capacitor is preferred to reduce the switching noise on the supply rails. Second, Smith buffer should be added at the input of the driver.

Chapter 9 Conclusions and Future Work

9.1 Conclusion

This Ph.D thesis pertains to an investigation into the nonlinearities of the analog-input closed-loop Class-D amplifiers and the development of new modulation topology to overcome the limitation of a conventional design.

The investigation on the nonlinearity of the closed-loop Class-D amplifier focused on pulse-width modulation topologies with both two-level and three-level output signals (a.k.a. AD- and BD-modulation). The derived expressions are simple, accurate, and clearly reflect the relationship with the input signal, carrier frequency, and the distortion components.

The proposed dual-feedforward carrier modulation topology improves the linearity of the closed-loop 2nd-order Class-D amplifier by ten times and has been proven to be effective for both the AD- and BD-modulated designs. The low switching frequency of the proposed topology ensures a high power efficiency of the whole system, especially for high-voltage applications.

In Chapter 3, the time domain waveforms of the phase and duty cycle errors have been established—by comparing the closed-loop and open-loop PWM signals, with the help of the cubic spline interpolation. The waveforms created provide an insight to the mechanism of the intrinsic harmonic distortion of a closed-loop Class-D amplifier. The relationship between the error signals and

the distortion inside the output signal has also been investigated. The results show that both the phase and duty cycle errors play collective roles in the 3rd-order harmonic, which is the most significant distortion component within the demodulated output signal of a 2nd-order Class-D amplifier.

In Chapter 4 and 5, a series of time-domain analysis able to precisely predict the intrinsic distortions are presented for both AD-modulated and BD-modulated Class-D amplifiers. The advantages of this technique are: (1) the output signal is obtained analytically for any band-limited input signal, in a compact form; (2) that the derivation procedure is systematic and hence, the analytical expression can in principle be obtained to any desired precision; and (3) the order of magnitude of the errors that arise from computing only the first few terms in the perturbation expansion can be estimated. The derived expressions clearly reflect the relationship between the input signal, carrier frequency and the intrinsic distortion components. The analytical results demonstrate that although the negative feedback can reduce the distortion due to the non-ideality of the power stage, it can cause significant undesired odd-order intrinsic harmonic components under a single-tone stimulus, even larger intrinsic intermodulation products under a two-tone input signal. Furthermore, it shows that a Class-D amplifier with 1st-order loop filter has an intrinsic distortions half that of the 2nd-order loop filter. Nevertheless, for a broad range of parameters, the intrinsic distortion is independent of the parameters of a fixed loop filter structure.

In Chapter 6, an overview of the chaotic dynamic and bifurcation scenarios that occur in Class-D power amplifier when the loop filter parameter varies is presented. The route to chaos in a conventional PWM-type Class-D amplifier is

identified. When the zero of the loop filter is shifted to a high frequency, a period-doubling bifurcation first occurs, followed by a border collision where the system enters the chaos regime. The chaotic operation of the Class-D amplifier is characterized by the occurrence of pulse skipping phenomenon. The criterion for precluding chaotic operation has also been determined. It shows that a design based on the new criterion achieves around 6 dB higher loop gain, as compared to the conventional design based on linear system stability criterion, without any extra cost.

In Chapter 7, the proposed dual-feedforward carrier modulation topology to achieve a significant reduction in the intrinsic harmonic distortion of a closed-loop 2nd-order loop filter Class-D amplifier is described. The input signal and loop filter output signal are employed to modulate the second order carrier. When implemented on an AD-modulated Class-D amplifier, the measured THD is less than 0.01% for input frequency up to 6 kHz, and has an idle carrier frequency of 310 kHz. The proposed topology is also proven to be applicable to fully-differential BD-modulated Class-D amplifier. The transistor-level implementation of the circuit architecture has been demonstrated.

In Chapter 8, a high-voltage switching-mode driver circuit is reported. This circuit is designed for a multi-carrier acoustic transmitter system targeted for well-drilling application to drive a piezo-electronic transducer. The measurement results demonstrate that the driver is able to function properly in high temperature, up to 260°C, and is able to drive a 0.33-μF capacitive load with 60-V_{pp} output signal swing.

9.2 Recommendations: Future Research

On the basis of the literature review and investigation in this thesis, the following further works are recommended.

i. Model the proposed carrier modulation design

Although the proposed 2nd-order Class-D amplifier gives excellent performance, the analysis on its mechanism is rather complex, mainly due to the modulated carrier and the internal loop created by the feedforward paths. The attempt of using time-domain analysis technique to model the topology shows that it is too complex to complete. New modeling technique may be developed for analyzing the system.

ii. Investigate the distortion introduced by practical circuit

There are several practical circuit issues that limit the linearity performance of the Class-D amplifier, including clipping noise, dead-time, and transient noise. These nonlinearities introduce significant audible distortions in certain conditions, and dominate the performance of the Class-D amplifier when the intrinsic distortion is minimized with advanced circuit topology. It is recommended that a systematic analysis of these nonlinearity sources should be investigated to provide a deeper understanding of the Class-D amplifier.

iii. Evaluate the self-oscillating topology

Self-oscillating Class-D amplifier achieves a better linearity performance than the conventional PWM Class-D amplifier. As no carrier generator is required, its circuit structure can be quite simple and promises a higher efficiency. A system analysis of self-oscillating Class-D amplifier should be quite valuable.

iv. New topology for compensating the load variation

The impedance of the load varies with the output signal. This is true for both the speakers for audio and piezo-electronic transducers. Due to the phase delay of the low-pass filter at the output of the Class-D amplifier, it is quite hard to embed the load into the feedback loop. However, the load variations can affect the performance of the power amplifier significantly. Therefore, it is best to explore new feedback topologies to compensate the load variation.

v. Techniques for suppressing intrinsic harmonic distortion

For stereo audio application, it is always desirable to have a fixed switching frequency for the Class-D amplifier, as this will simplify the integration process. It is hence useful to develop new techniques or topologies with fixed switching frequency. The development of proper circuit implementations for the two developed sample-and-hold topologies as reviewed in Section 2.4.3.2 and Section 2.4.3.4 may also be further investigated.

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