Space vector pulse-width modulation theory and topology improvement for Z-source inverters

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**SPACE VECTOR PULSE-WIDTH MODULATION THEORY AND
TOPOLOGY IMPROVEMENT FOR Z-SOURCE INVERTERS**

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Summary

High-performance voltage- and current- source inverters (VSIs and CSIs) are the most important components in various direct current (DC)/alternating current (AC) conversion utilities. However, with the development of the renewable energy, the traditional VSIs and CSIs have been seriously restricted due to their narrow obtainable output voltage range property. In 2002, an impedance-source power inverter (termed Z-source inverter (ZSI)) was proposed to overcome the limitations and barriers in traditional VSIs and CSIs. It has successfully integrated the function of the traditional DC/DC boost converter into the DC/AC inverter by a unique X-shape impedance network. Owing to its inherent advantages, such as wider obtainable output voltage range, higher reliability and higher efficiency, it has drawn many researchers' attention. As a research hotspot in power electronics, the Z-source topology has been greatly explored from various aspects, including developed topologies, modulation techniques, mathematical modelings and control strategies.

However, most of the carrier-based modulation strategies are found to have the drawbacks of higher switching actions than that of the traditional VSI, which would introduce more switching loss of the system. To solve this problem, the space vector pulse width modulation (SVPWM) theory of ZSI has been explored. Based on an in-depth mathematical derivation and theoretical explanation, the SVPWM theory of three-phase ZSI has been discussed in detail. Besides, novel SVPWM-based implementation schemes of two popular modulation methods (maximum boost control method and constant boost control method) have been presented. By selecting different null state and shoot-through state, three switching patterns of SVPWM technique have been explored and compared with the carrier-based strategies.

In addition, the SVPWM concept has been successfully extended to the single-phase ZSI. With consideration on the circuit characteristics, the theory and implementation schemes of the SVPWM strategy for single-phase ZSI have been deduced and explained thoroughly. By properly selecting the shoot-through vectors and null vectors, switching patterns with less switching actions have been presented as well. These efforts will be

helpful for understanding the SVPWM concept and promoting the industrial applications of the ZSI.

As is known, the voltage boost ability is the most notable advantage of the ZSI. However, this capability of the classical ZSI is very limited, which will certainly restrict its further applications for low voltage energy sources that require strong boost inversion abilities, such as fuel cells, batteries and photovoltaic (PV) systems. Hence, an in-depth research on advanced topology with a higher voltage gain has been performed. It is noted that the voltage boost ability of the ZSI comes from its impedance network. To get further understanding of the impedance network, the small signal models of the improved ZSI have been studied by employing state-space averaging method. Through the study of the dynamic modeling, a developed impedance-type power inverter that is termed the switched-inductor (SL) ZSI is proposed based on the classical ZSI to improve the voltage adjustable ability. It employs two SL cells to replace the inductors of the impedance network. With this modification, the proposed SL ZSI increases the voltage boost inversion ability significantly compared with the classical ZSI. Only a very short shoot-through state is required to obtain high voltage conversion ratio, which is beneficial for improving the output power quality of the main circuit. In addition, the voltage buck inversion ability is also provided in the proposed inverter for those applications that need low AC voltages. Same to the classical ZSI, the proposed SL ZSI can be applied to various applications of DC/AC, AC/AC, DC/DC and AC/DC power conversion, which will be beneficial for the engineering applications using impedance-type power inverters.

With the view of detailed analyzing the dynamic system and designing closed-loop controllers of the proposed SL ZSI, an accurate small signal model of the SL ZSI has also been presented. By employing the state-space averaging method, small signal models have been established and related transfer functions have been derived. Through mathematical analyses, the right-half plane (RHP) zeros are found to present in the transfer functions, which would degrade the performance of the closed-loop system. In order to keep satisfactory performance and stability, a group of root loci plots are illustrated to observe the movements of the RHP zeros. Besides, the influences of the Z-

network parameters on the NMP effects caused by the RHP zeros have been investigated.

Furthermore, the SVPWM theory and implementation schemes for single- and three-phase SL ZSI have also been explored. As with that of the classical ZSI, the SVPWM theories of single- and three-phase SL ZSI together with different switching patterns have been discussed in detail. In addition, implementation schemes of maximum boost control method and constant boost control method of three-phase SL ZSI based on SVPWM theory have also been presented and compared with that of the classical ZSI, which shows the advantage of the SL ZSI in boost inversion ability.

All the proposed topology and control schemes have been validated by simulation and experimental investigations. These efforts will be helpful for understanding the SVWPM theory and promoting the applications of the impedance-type power inverters.

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List of Abbreviations

AC	Alternating Current
ASD	Adjustable Speed Drives
CCM	Continuous Conduction Mode
CSI	Current Source Inverter
DC	Direct Current
DCM	Discontinuous Conduction Mode
DLL	Dynamic link library
EZSI	Embedded Z-Source Inverter
FFT	Fast Fourier Transform
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MW	Megawatts
NMP	Non-Minimum Phase
PSIM	Physical Security Information Management
PWM	Pulse Width Modulation
PV	Photovoltaic
QZSI	Quasi Z-Source Inverter
RHP	Right Half Plane
RMS	Root Mean Square
SC	Switched Capacitor
SL	Switched Inductor
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
TSI	T-Source Inverter
UPS	Uninterruptable Power Supply
VL	Voltage Lift
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

List of Symbols

A_n	State matrix during switching-on or -off ($n=1, 2$)
B	Boost factor
B_n	Input matrix during switching-on or -off ($n=1, 2$)
C_f	Capacitor of output filter
C_n	Capacitor of Z-network ($n=1, 2$)
D	Shoot-through duty ratio
f_c	Corner frequency of output filter
f_o	Output fundamental frequency
f_s	Switching frequency
G	Voltage gain
i_C	Current of Z-network capacitor
i_L	Current of Z-network inductor
i_l	Load current
L_f	Inductor of output filter
L_l	Inductor of inductive load
L_n	Inductor of Z-network ($n=1, 2, 3, 4$)
M	Modulation index
R	Resistor of resistive load
R_l	Resistor of inductive load
s	Laplace operator
S_{ap}	Upper switching pattern of phase a
S_{an}	Lower switching pattern of phase a
S_{bp}	Upper switching pattern of phase b
S_{bn}	Lower switching pattern of phase b
S_{cp}	Upper switching pattern of phase c
S_{cn}	Lower switching pattern of phase c
T	Switching cycle
T_{sh}	Shoot-through state time duration
T_z	Time duration of zero state

V_{ab}	Output line-line voltage (RMS)
V_C	Voltage of Z-network capacitor
v_{dc}	Voltage stress of the dc-link across the inverter bridge
V_{dc}	Peak value of v_{dc}
v_{in}	Input dc source voltage
v_L	Voltage of Z-network inductor
V_n	Non-shoot-through switching state ($n=0, 1, 2, \dots, 7$)
$\hat{v}_{pn}$	Peak value of output phase voltage
$\vec{V}_{ref}$	Reference of output voltage vector
V_{shn}	Shoot-through switching state ($n=1, 2, \dots, 7$)
V_x	Output phase voltage ($x=a, b, c$)
Z_n	Negative zeros of transfer functions
Z_p	Positive zeros of transfer functions
θ	Phase angle

Chapter 1. Introduction

1.1 DC/AC Inverters in Renewable Energy System

High-performance voltage- and current- source inverters (VSIs and CSIs) are the most important components in various DC/AC conventional utilities, such as servo-motor drives [1-4], UPS system [5-8], distributed power systems [9-12], and hybrid electric vehicles [13-15]. After decades of development of inverters, their topologies and control methods tend to be mature.

In order to meet the increasing requirement of energy without emitting greenhouse gases that would harm the environment, the renewable energy sources, such as solar panels, wind turbines, fuel cells and so on, play an important role in today's and future's power supply systems. About 16% of global final energy consumption comes from renewables, and the number is growing rapidly. At the end of 2012, the worldwide installed capacities of wind power and PV power were 282,482 megawatts (MW) and 100,000 MW [16], respectively, which had grown rapidly.

Unfortunately, due to their narrow obtainable output voltage range, traditional VSIs and CSIs have been seriously restricted in the applications of renewable energy system. Usually, this problem is solved by utilizing a DC/DC boost-buck converter in front of the traditional VSI or CSI when the power supply is a DC source [17-19]. Alternatively, if it is an AC source, an additional AC/DC rectifier should be employed before the DC/DC converter [20-22]. However, these multi-stage topologies are known to be inefficient and the controller design becomes much more complex. Thus, a high-efficiency single-stage topology solution would be quite appropriate.

In 2002, an impedance-source power inverter with such single-stage topology (termed Z-source inverter (ZSI)) was proposed to overcome the aforementioned limitations and barriers [23]. It has successfully integrated the function of the traditional DC/DC boost converter into the traditional VSIs or CSIs by adding two capacitors and two inductors that form an "X"-shape impedance network between the input power source and the bridge-type inverter, as depicted in Fig. 1.1. With this unique impedance network, it allows the switches in the same phase-leg to conduct simultaneously, which is rigorously forbidden in traditional VSIs. By properly setting the shoot-through duty cycle, ZSIs can

have both voltage boost and buck capabilities, which cannot be achieved by traditional VSIs or CSIs. Owing to its inherent advantages, such as wider obtainable output voltage range, higher reliability and higher efficiency, the ZSI has drawn many researchers' attentions and found many applications in industrial fields, such as adjustable speed drives [24, 25], UPS systems [26, 27], fuel cells [28, 29], photovoltaic systems [30, 31], wind turbines [32, 33], and so on.

Figure 1.1 Prototype of the three-phase ZSI

1.2 Review of Z-Source Inverters

As a hotspot research topic in power electronics of renewable energy system, the Z-source topology has been greatly explored in various aspects, including developed topologies [34-38], modulation techniques [39-42], mathematical models [43-46], closed-loop control methods [47-50], and so on. In this section, some important issues associated with the research work of this thesis will be reviewed.

1.2.1 Review of Topological Characteristics of ZSI

In this section, the operating principles of the ZSI are introduced in detail. The steady state equations are deduced by combining the equations of shoot-through state and non-shoot-through state. Then, a comparison study between ZSIs and DC/DC/AC converters is given. Afterwards, the time domain analysis of the Z-network with the waveform of capacitor voltage from the initial start-up to steady state is conducted.

Operating Principles

As is known, according to different switching status of the six switches, a traditional three-phase VSI has eight permissible switching states: six active states and two null

zero states. Table 1-1 lists the switching status of the six switches S_a , S_b , S_c , S_a' , S_b' and S_c' in each switching state, where the value 1 indicates a switching on status and the value 0 indicates a switching off status, V_0 and V_7 represent the null states and the rest are the active states. During the active states, the DC voltage is impressed to the load; alternatively, during the null states; the load is short-circuited by turning on either all the upper switches or all the lower switches.

Table 1-1: Switching states of three-phase VSI

	S_a	S_a'	S_b	S_b'	S_c	S_c'	V_a	V_b	V_c
V_0	0	1	0	1	0	1	0	0	0
V_1	0	1	0	1	1	0	0	0	V_{dc}
V_2	0	1	1	0	0	1	0	V_{dc}	0
V_3	0	1	1	0	1	0	0	V_{dc}	V_{dc}
V_4	1	0	0	1	0	1	V_{dc}	0	0
V_5	1	0	0	1	1	0	V_{dc}	0	V_{dc}
V_6	1	0	1	0	0	1	V_{dc}	V_{dc}	V_{dc}
V_7	1	0	1	0	1	0	0	0	0

However, as mentioned above, the ZSI has an additional zero state when the load terminals are shorted through both the upper and lower devices of the same phase leg, which is strictly forbidden in the traditional VSI. We call this additional zero state the shoot-through state. By carefully distributing the shoot-through period over a switching cycle, one can obtain a given output voltage whether greater or smaller than the input DC source voltage. Generally, ZSI has three operation modes: shoot-through states, active states and null states. The active states and null states can be represented in the same equivalent circuit for steady state analysis and this common state is termed non-shoot-through state. In this section, equivalent circuits of ZSI in different modes are demonstrated and corresponding operating principles are introduced.

Fig. 1.2 (a) and (b) show the equivalent circuits of the ZSI viewed from the DC link when the ZSI operates in the shoot-through state and in the non-shoot-through state, respectively. For the simplicity of steady-state analysis, all the inductors and capacitors

are assumed to be ideal and symmetrical, so we have $V_{C1} = V_{C2} = V_C$ and $V_{L1} = V_{L2} = V_L$. The inverter system is represented by a current source according to its characteristic.

During the shoot-through state time interval T_{sh} , the voltage after the diode is greater than the input DC voltage, therefore, the diode D_{in} (as depicted in Fig. 1.1) is anti-biased. The capacitors will charge the inductors. According to Fig. 1.2 (a), one has

$$\begin{cases} v_{L-on} = V_C \\ v_{i-on} = V_C + v_{L-on} = 2V_C \\ v_{dc-on} = 0 \end{cases} \quad (1-1)$$

(a) shoot-through state

(b) non-shoot-through state

Figure 1.2 Equivalent circuit of the ZSI viewed from the DC-link

Alternatively, during the non-shoot-through state time interval T_n , the ZSI operates in any one of the six active states or two null states. In the active states, there is a current flow from the input DC source to the AC load, and the diode D_{in} is forward-biased. While in the null states, the load is short-circuited, hence the inverter input current is zero. The diode is still conducting and the capacitors are charging from the input voltage source. According to Fig. 1.2 (b), the following equations can be obtained:

$$\begin{cases} v_{L-off} = V_{in} - V_C \\ v_{i-off} = V_{in} \\ v_{dc-off} = V_C - v_{L-off} = 2V_C - V_{in} \end{cases} \quad (1-2)$$

The average voltage across the Z-network inductor should be zero in one switching period T according to the volt-second balance principle. Then through (1-1) and (1-2), one can thus obtain

$$\bar{v}_L = \frac{T_{sh} \cdot v_{L-on} + T_n \cdot v_{L-off}}{T} = \frac{T_{sh} \cdot V_C + T_n \cdot (V_{in} - V_C)}{T} = 0 \quad (1-3)$$

$$V_C = \frac{T_n}{T_n - T_{sh}} V_{in} \quad (1-4)$$

Similarly, the average DC-link voltage across the inverter bridge can be described as

$$\bar{v}_{dc} = \frac{T_{sh} \cdot 0 + T_n \cdot (2V_C - V_{in})}{T} = \frac{T_n}{T_n - T_{sh}} V_{in} = V_C \quad (1-5)$$

The peak value of the voltage across the DC-link can be expressed as

$$V_{dc} = v_{dc-off} = V_C - V_L = 2V_C - V_{in} = \frac{T}{T_n - T_{sh}} V_{in} = B \cdot V_{in} \quad (1-6)$$

where

$$B = \frac{T}{T_n - T_{sh}} = \frac{1}{1 - 2T_{sh}/T} = \frac{1}{1 - 2D} \quad (1-7)$$

B is termed the boost factor determined by the shoot-through state duty ratio D . The peak DC-link voltage V_{dc} can be regarded as the input voltage of an ordinary inverter.

On the other side, the peak value of the output phase voltage can be stated as

$$\hat{V}_{pn} = M \cdot \frac{V_{dc}}{2} \quad (1-8)$$

where M is the modulation index of the inverter.

Substituting (1-6) into (1-8), one has

$$\hat{V}_{pn} = \frac{1}{2} M \cdot B \cdot V_{in} = G \cdot \frac{V_{in}}{2} \quad (1-9)$$

where $G=M B$ is the voltage gain of the whole ZSI.

For a traditional three-phase VSI, the relations between peak value of the output phase voltage and the input source voltage can be expressed as $\hat{V}_{pn} = M \cdot V_{in}/2$. Regarding that the linear operating range of a three-phase inverter is from 0 to 1 [51], it is obvious that the output phase voltage cannot be greater than the input source voltage. Meanwhile, it is

also indicated in (1-9) that the voltage gain G , determined by both the modulation index M and the boost factor B , can be any value from 0 to ∞ theoretically. Therefore, ZSI is able to produce an output phase voltage greater or less than the input source voltage provided that the M and B are selected appropriately.

Comparison of ZSIs and DC/DC/AC Converters

As described in the previous section, one of the main advantages of ZSIs compared to traditional VSIs is the voltage boost ability. However, adding a DC/DC boost converter before the VSI is also an approach to obtain higher output voltage than the input source voltage. To show the differences between these two approaches, the comparison study of ZSIs and DC/DC/AC converters is introduced.

Figure 1.3 Sketch map of typical DC/DC/AC converters

Fig. 1.3 demonstrates the typical topology of a DC/DC/AC converter. Recalling the topology of ZSIs depicted in Fig. 1.1, the following table that shows the detailed comparison between ZSIs and DC/DC/AC converters can be obtained.

Table 1–2: Comparison between ZSIs and dc/dc/ac converters

	ZSI	DC/DC/AC Converter	
		DC/DC boost converter	VSI
<i>Input voltage</i>	DC	DC	DC
<i>Output voltage</i>	AC	DC	AC

<i>Voltage gain</i>	Boost/Buck	Boost	Buck
<i>Number of inductors</i>	2	1	0
<i>Number of capacitors</i>	2	1	0
<i>Number of diodes</i>	1	1	0
<i>Number of switches</i>	6	1	6

As shown in the above table, the obvious advantages of the ZSI can be listed below:

- has only one stage to achieve voltage boost and buck abilities
- has less number of high-frequency switching devices

Besides, conducting both the upper and lower switches in the same phase leg will not destroy the devices any more, which improves the safety of the system. Additionally, only one single controller is required for the ZSI, which would degrade the complexity of the controller design.

Also, it is shown in the table that more passive components are required for ZSIs, which indicates more conducting loss considering the parasitic resistors of the passive components. However, the parasitic resistors are usually very small that the effects of them can be neglected. According to [28], the whole efficiencies of ZSIs are higher than the DC/DC/AC converters for fuel-cell vehicles generally.

Inrush Current at Start-up

Figure 1.4 Current path of ZSIs at initial start-up

Fig. 1.4 shows the current flows of ZSIs at initial start-up. The initial voltage stresses across the Z-network capacitors are zero, hence, huge inrush current charges the capacitors to $0.5V_{in}$ immediately through the path shown in Fig. 1.4 when the upper and lower switches in the same phase leg are conducting simultaneously. Then, the resonance of Z-network capacitors and inductors starts, resulting in large voltage and current surge. The voltage waveform of the Z-network capacitor from the initial start-up to steady state is depicted in Fig. 1.5. Due to the topological characteristics of ZSIs, the inrush current and resonance of Z-network components can not be avoided. In another way, when the upper switch is turned on first at start-up, the voltage across the upper switch will be V_{in} , thus the rating voltages of the switches should be large enough to avoid failure.

Figure 1.5 voltage waveform of the Z-network capacitor from the initial start-up

1.2.2 Review of Developed Topologies of ZSI

As a newly proposed topology, the ZSI has several significant drawbacks. For example, the input current is discontinuous in the boost mode; the voltage stresses of the capacitors of impedance network sustain high levels; the inrush current caused by Z-source capacitors and inductors at startup cannot be suppressed, which will introduce a voltage and current surge that may destroy the devices. To improve one or more of these issues, many developed topologies based on the classical ZSI have been proposed. Several typical ones among them are introduced in this section. Essentially, most of these topologies contain both voltage fed and current fed types. Only the voltage fed topologies are selected to present here due to the length limit.

Quasi ZSI

The voltage fed quasi ZSIs (QZSIs) that feature several improvements compared with the traditional ZSI were proposed in [35]. The prototypes are depicted in Fig. 1.6 (a) and (b). It is shown that though the quasi ZSIs have the same components as the traditional one, the position and connection of inductors and capacitors of the impedance network are different. With the slight modifications, the QZSI, shown in Fig. 1.6 (a), compared with the traditional ZSI, features a lower DC voltage on capacitor C_1 as well as a continuous input current; while the QZSI shown in Fig. 1.6 (b) features a lower DC voltage both on capacitor C_1 and C_2 , whereas, the input current is discontinuous. It is noted that the QZSIs feature a common DC rail between the voltage source and the inverter bridge and both these two topologies can be made bidirectional by utilizing a bidirectionally conducting switch instead of the diode D_1 .

(a) with continuous input current

(b) with discontinuous input current

Figure 1.6 Prototypes of voltage fed quasi ZSI

Embedded ZSI

In order to prevent the high-frequency current ripple flowing into the DC source under load disturbance, which may degrade the dynamics of the power source, usually a second-order LC filter is required to be placed before the input diode. However, it might lead to a slight cost increase of the entire system. Besides, the parameters of the filters should be well designed; otherwise unnecessary dynamic and resonance would be introduced to the system. Hence, the embedded ZSI (EZSI) was proposed in [38] to solve this problem. As depicted in Fig. 1.7, it embedded the input voltage source into the impedance network, using its existing inductors and capacitors for current and voltage filtering, instead of adding an external LC filter. With this modification, another advantage is found that the capacitor sizing (voltage rating) is reduced significantly. Obviously, Fig. 1.7 shows an obvious disadvantage that two DC sources of $V_{in}/2$ are required for the EZSI. Nevertheless, it would not be regarded as serious limitation for applications of PV or fuel cell, where the ZSI is primarily promoted, because the required voltage ratings can be produced easily by rearranging the existing cell units properly.

Figure 1.7 Prototype of voltage-fed embedded ZSI

Improved ZSI

The improved ZSI was proposed in [37] to solve these two drawbacks existing in the classical ZSI: 1) the Z-capacitor voltage stresses are no less than input DC voltage, resulting in larger volume and higher cost of the system on account of the requirement of

high-voltage capacitors; 2) the inrush current and the resonance introduced by capacitors and inductors of impedance network at startup cannot be suppressed, which causes a voltage and current surge that may destroy the devices. As depicted in Fig. 1.8, the improved ZSI has the same elements as the traditional one; while it moves the impedance network to the back end of the inverter bridge and the position and connection direction of the input diode have also been changed. With this modification, the voltage stresses of the capacitors have been reduced significantly to obtain the same voltage boost conversion and the inherent inrush current has been limited since there is no current path at startup.

Figure 1.8 Prototype of improved ZSI

T-Source Inverter

The above three types of topologies focused on rearranging the positions and connections of the elements of the impedance network to obtain advanced features. However, the T-source inverter (TSI) aims to reduce the number of the elements of the impedance network [36]. Fig. 1.9 shows several equivalent four terminal networks that can replace the basic impedance network of the traditional ZSI with reduced number of passive elements. Taking the modification from Fig. 1.9 (b) for example, the topology of the TSI is depicted in Fig. 1.10. It can be seen that the number of passive elements is reduced since the low leakage inductance transformer and one capacitor are required. Obviously, the modifications of impedance network from Fig. 1.9 (b) and (c) can be applied to other power electronic systems as well. It should be noted that the TSI topologies features a common DC rail between the voltage and the inverter, like the

QZSI circuits. Moreover, additional possibilities for the output voltage manipulation can be achieved by using a transformer with different than 1:1 transformer ratio.

Figure 1.9 Examples of the alternative equivalent impedance networks

Figure 1.10 Prototype of Low-leakage-inductance-transformer-based TSI

1.2.3 Review of Modulation Techniques of ZSI

In this section, several of the popularly employed modulation methods for ZSIs are introduced. As described in previous section, the main difference of ZSI compared to the traditional VSI is the presence of the shoot-through state. Theoretically, the shoot-through state can be inserted anywhere in the switching period. However, the duration of active states should not be affected, i.e. the volt second average should not be changed.

Simple Boost Control Method

As described in the original paper on ZSI [23], the simplest modulation method is to insert the shoot-through state inside the traditional null interval. For this strategy, two straight lines equal to or greater than the peak value of the three phase references are used to control the shoot-through duty ratio in a traditional sinusoidal PWM, as shown in

Fig. 1.11. When the triangular waveform is greater than the upper line, V_p , or lower than the bottom line, V_n , the circuit turns into shoot-through state. Otherwise it operates just as traditional carrier-based PWM. This method is very straightforward; however, the resulting voltage stress across the switches is relatively high because some traditional null states are not utilized.

Figure 1.11 Sketch map of the simple boost control method

Modified PWM Method

Though the simple boost method is able to work, it has a disadvantage that the number of switching transitions is increased. Besides, conducting all the switches in the shoot-through states is necessary because the shoot-through stress can be allocated only in one particular leg each time. To avoid this, the modified PWM method is proposed in [39]. For this method, six sine waves are employed instead of three in traditional VSI. From the schematic plot shown in Fig. 1.12, it uses two sine waves to generate switching signals for each leg and shifts these two sine waves up or down to get the required shoot-through level, which results in equally spread six shoot-through intervals per half carrier cycle. The shoot-through signals are inserted without increasing the number of switching actions per half carrier cycle. Furthermore, this spread shoot-through insertion method would bring about improved spectral characteristics.

Figure 1.12 Modulation signals of modified PWM method

Maximum Boost Control Method

As is known, one of the most important features of the ZSI is that it can obtain higher output phase voltage than the input DC source voltage, and the voltage gain is defined as MB . Since the linear modulation index M has very limited operation range ($0 \leq M \leq 1$), we should maximize the boost factor B to obtain the maximum voltage gain, i.e. we have to make the shoot through duty ratio D as large as possible. Besides, reducing the voltage stress under a desired voltage gain becomes more important to control the ZSI. Accordingly, the maximum boost control method turns all traditional null states into shoot-through-states while maintaining all the six active states unchanged [40]. Thus maximum D and B are obtained without distorting the output waveforms. The sketch map of maximum boost control is shown in Fig. 1.13. However, this method would introduce a low frequency current ripple that is associated with the output frequency in the inductor current and the capacitor voltage, which will cause a higher requirement of the passive components when the output frequency becomes very low. Therefore, the maximum boost control is suitable for applications that have a fixed or fairly high output frequency.

Figure 1.13 Sketch map of the maximum boost control method

Constant Boost Control Method

In order to reduce the volume and cost, it is very important to keep the shoot-through duty ratio constant at all the time. Meanwhile, a greater voltage boost for any given modulation index is required to reduce the voltage stress across the switches. The constant boost control method is proposed to obtain the maximum voltage gain while keeping the shoot-through duty ratio as a constant always [41]. It employs five modulation curves: three-phase reference signals V_a , V_b , and V_c , and two shoot-through envelope signals V_p and V_n to compare with the carrier triangle wave. When the triangle wave is higher than the upper shoot-through envelope V_p or lower than the bottom shoot-through envelope V_n , the inverter is turned into a shoot-through state. Fig. 1.14 shows the sketch map of constant boost control method.

Figure 1.14 Switching signals of constant boost control method

Summary of the Modulation Strategies

So far, four popular modulation methods for ZSI have been introduced, and they are all proved to be able to work in various applications. Table 1-3 shows a summary of all the specified variables for different control methods and Figs. 1.15 and 1.16 show G versus M and V_{dc} versus G for all control methods, respectively. It can be seen from Fig. 1.15 that the boost conversion ability of all the methods decreases rapidly with the increase of modulation index, especially when M is greater than 0.8. Fig. 1.16 indicates that the DC-link voltage stress using the simple boost control is the highest of the four methods while achieving the same voltage gain.

Table 1–3: Summary of different PWM control methods of classical ZSI

	Simple Boost	Maximum Boost	Constant Boost	Modified PWM
D_{max}	$1-M$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$	$1-\frac{\sqrt{3}M}{2}$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$
B_{max}	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$	$\frac{1}{\sqrt{3}M-1}$	$\frac{\pi}{3\sqrt{3}M-\pi}$
G_{max}	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$	$\frac{M}{\sqrt{3}M-1}$	$\frac{\pi M}{3\sqrt{3}M-\pi}$
M_{max}	$\frac{G}{2G-1}$	$\frac{\pi G}{3\sqrt{3}G-\pi}$	$\frac{G}{\sqrt{3}G-1}$	$\frac{\pi G}{3\sqrt{3}G-\pi}$
V_{dc}	$(2G-1)V_{in}$	$\frac{3\sqrt{3}G-\pi}{\pi}V_{in}$	$(\sqrt{3}G-1)V_{in}$	$\frac{3\sqrt{3}G-\pi}{\pi}V_{in}$

Figure 1.15 Voltage gain versus modulation index for different control methods

Figure 1.16 Voltage stress versus voltage gain for different control methods

1.2.4 Review of Main Analysis Principles in Power Electronics Circuits

To perform a theoretical analysis for a given power electronics topology, the circuit is usually assumed to operate in the steady state. It means that: 1) the duty ratio of the switch is kept constant for a long time (over a large number of switching cycles); 2) the current and voltage waveforms become periodic with the switching cycle T . There are two important principles that describe the steady-state performance of a power electronics circuit: *volt-second balance* of the inductor and *charge balance* of the capacitor. These two principles will be employed throughout the thesis to analyze the steady-state performance of various topologies, which will be briefly reviewed in the following subsections. Besides, the classical *state-space averaging* method will also be introduced because it is widely used in the mathematical modeling of power electronics circuits.

Volt-Second Balance and Charge Balance Principles

The steady-state condition indicates a periodic behavior of the current flowing through the inductor. Thus

$$i_L(n \cdot T) = i_L((n+1) \cdot T) \quad (1-10)$$

Also

$$v_L = L \frac{di_L}{dt} \quad (1-11)$$

Integration over one switching period yields,

$$i_L((n+1) \cdot T) - i_L(n \cdot T) = \frac{1}{L} \int_{nT}^{(n+1)T} v_L(t) dt \quad (1-12)$$

Form (1-10), obviously, the left side of (1-12) is zero. And consequently, the right side of (1-12) should be zero, too. That is

$$0 = \frac{1}{L} \int_{nT}^{(n+1)T} v_L(t) dt \quad (1-13)$$

Equation (1-13) indicates that the integral of the voltage across the inductor along a switching period must be zero for the steady state. This feature is termed *volt-second balance* principle in the steady state.

Similarly, the following equation can be obtained through mathematical analysis

$$0 = \frac{1}{C} \int_{nT}^{(n+1)T} i_C(t) dt \quad (1-14)$$

Equation (1-14) indicates that the integral of the current flowing through the capacitor along a switching period must be zero for the steady state. This feature is termed *charge balance* principle in the steady state.

State-Space Averaging Method

State-space averaging method is an approximation technique that approximates the switching converter as a continuous linear systems [52-60], which was firstly proposed by R.D. Middlebrook and S. Cuk [52]. State-space averaging method requires the condition that the effective output filter corner frequency f_c should be much smaller than the switching frequency f_s . The mathematical model derived from the state-space averaging permits the designer to determine the steady-state performances and small-signal transfer functions of the circuits. Procedures for state-space averaging are summarized as follows:

- 1) Identify switched models over a switching period. Draw the linear switched circuit model for each sub-mode of the switching converter.
- 2) Identify state variables of the circuit. Write state equations for each switched circuit model using Kirchhoff's voltage and current laws.
- 3) Perform state-space averaging using the duty ratio as a weighting factor and combine state equations into a single averaged state equation. The state-space averaged equation is given as

$$\dot{x} = [A_1 d + A_2 (1-d)]x + [B_1 d + B_2 (1-d)]u \quad (1-15)$$

where: x is the state vector and u is the input signal;

A_1 and A_2 are the state matrixes during switching-on and -off;

B_1 and B_2 are the input matrixes during switching-on and -off.

- 4) Perturb the averaged state equation to yield steady-state (DC) and dynamic (AC) terms and eliminate the product of any AC terms.

1.3 Objectives, Research Plan and Major Contributions

1.3.1 Objectives

Reviewing the research work introduced in the previous section, we find that most of the carrier-based control strategies have the drawbacks of higher switching actions than that of traditional VSI, which would yield more switching loss. Besides, the voltage boost inversion ability is very limited, especially with a high modulation index value, which would definitely restrict the further applications of the ZSI for low voltage sources such as full cells, batteries and PV systems. Hence, the main objectives of this research project include the following aspects:

- To explore advanced modulation schemes for the single- and three-phase Z-source topologies that can reduce the switching actions.
- To investigate advanced topologies that can improve the voltage boost inversion ability of the classical ZSI.

1.3.2 Research Plan

As is known, with the fast development of microprocessors, the space vector pulse-width modulation (SVPWM) technique has been extensively employed for three-phase power electronics applications [60-69] due to its easy digital implementation, wide linear modulation range and less harmonic distortion features. Hence, it might be a possible solution for reducing the switching actions of the ZSI.

It is noted that the voltage boost inversion ability of the ZSI comes from the impedance network, which has the same function of the DC/DC boost converter. In recent years, advanced DC/DC conversion enhancement techniques such as switched-capacitor (SC), switched-inductor (SL), hybrid SC/SL, voltage multiplier cells and voltage-lift (VL) techniques, have been greatly explored, which are used to get the high step-up capacity in transformerless and cascade structures. The main objective is to reach a high efficiency, high power density and simple structures. Therefore, the combination with the ZSI and advanced DC/DC enhancement techniques could be a

good solution for improving impedance-type inverters' performance and promoting their further industrial applications.

Based on the aforementioned research objectives, the main research work in this thesis is divided into three steps as depicted in Fig. 1.17. The first step is to explore the theory and implementation schemes of SVPWM technique of three-phase ZSI and study the dynamics of the Z-source impedance network. The second step is to propose an advanced topology (SL ZSI) with higher voltage boost inversion ability based on the classical ZSI according to the dynamic modeling study of the Z-source impedance network; on the other hand, the SVPWM theory has been extended to the single-phase ZSI. The third step is to study the dynamics of the newly proposed SL ZSI and explore the SVPWM theory for single- and three-phase SL ZSI.

Figure 1.17 Sketch map of the research plan

1.3.3 Major Contributions

The major contributions of this research work are summarized as follows:

- SVPWM theories of single- and three-phase ZSI and SL ZSI have been introduced and three switching patterns with less switching actions are explored.
- The SL ZSI topology has been proposed to improve the voltage boost inversion ability of the classical ZSI.
- Dynamic models of the improved ZSI and SL ZSI have been developed.

SVPWM Theories of single- and three-phase ZSI and SL ZSI

Most of the carrier-based control strategies are found to have the drawbacks of higher switching actions, which would result in more switching loss. To solve this problem, the SVPWM techniques of ZSI and SL ZSI have been explored. Based on an in-depth mathematical derivation, the SVPWM principles and implementation schemes of three-phase ZSI have been discussed in detail. Besides, novel SVPWM-based implementation schemes of two popular modulation methods (maximum boost control method and constant boost control method) have been presented. In order to reduce the number of switching actions in each switching cycle, different switching patterns of SVPWM technique have been explored. In addition, the SVPWM concepts have been successfully extended to the single-phase ZSI. With consideration on the circuit characteristics, the principles and implementation schemes of the SVPWM strategy for single-phase ZSI have been deduced and explained thoroughly. Similar to that of the classical ZSI, the implementation schemes of SVPWM techniques together with different switching patterns for single- and three-phase SL ZSI have also been investigated. These efforts will be helpful for understanding the SVPWM concept and promoting further applications of the three-phase and single-phase ZSI and SL ZSI.

Switched-inductor ZSI

To enlarge the voltage adjustable ability of the classical ZSI, a developed impedance-type power inverter (termed SL ZSI) is proposed. With a slight modification of the impedance network, the proposed SL ZSI increases the voltage boost inversion ability significantly compared with the classical ZSI. Only a very short shoot-through state is required to obtain high voltage conversion ratio, which is beneficial for improving the output power quality of the main circuit. In addition, the voltage buck inversion ability is also provided in the proposed inverter for those applications that need low AC voltages. As with the classical ZSI, the proposed SL ZSI can be applied to various applications of DC/AC, AC/AC, DC/DC and AC/DC power conversion, which will be beneficial for the engineering applications using impedance-type power inverters.

Mathematical Models of Improved ZSI and SL ZSI

To further understand the dynamics of the Z-source impedance network, small signal models of the improved ZSI have been well established by employing the state-space averaging method and related transfer functions have been derived. Similarly, the dynamic modeling of the SL ZSI has been studied through the state-space averaging method. However, the transfer function indicates the existence of the right half plane (RHP) zeros that would degrade the dynamic response of the system. In order to keep satisfactory performance and stability, various root-locus plots have been investigated by altering a specified parameter while keeping others as constant values. Unfortunately, the RHP zeros could not clear away by modulating the parameters but the non-minimum phase (NMP) effects can be reduced by selecting proper values of the passive components in the impedance network. These efforts will be helpful for understanding the dynamics of the SL Z-source impedance network and designing proper closed-loop controller for the SL ZSI.

1.4 Organization of the Thesis

There are 8 chapters in this thesis which are structured as follows:

Chapter 2 details the SVPWM theory of three-phase ZSI and implementation schemes of maximum boost control method and constant boost control method.

Chapter 3 extends the SVPWM concepts to single-phase ZSI and explores different patterns to reduce switching actions.

Chapter 4 studies the dynamic system of the improved ZSI by employing the state-space averaging method.

Chapter 5 performs the topology analysis of the novel SL ZSI, which is proposed to enhance the boost invention ability of the classical ZSI.

Chapter 6 presents small-signal models of the SL ZSI and selection of the parameters for the SL impedance network.

Chapter 7 introduces the SVPWM theories and implementation schemes for single- and three-phase SL ZSI.

Chapter 8 concludes the thesis and recommends developments for future research.

Chapter 2. Space Vector PWM of Three-Phase ZSI

In this chapter, the theory of SVPWM technique for the three-phase ZSI has been derived and discussed in detail. Besides, implementation schemes with less switching actions of maximum boost control and constant boost control methods for three-phase ZSIs based on SVPWM theory have been presented. Moreover, the harmonic spectrums of different schemes have been discussed according to different switching actions. All the theoretical analysis has been verified by simulation and experimental results. The proposed control schemes will be helpful for enhancing the understanding of SVPWM technique and promoting the applications of three-phase ZSIs.

2.1 Introduction

In literature review, several popular control methods for ZSI have been introduced. These methods are all carrier-based and they have been applied in many cases. However, most of the carrier-based strategies are found to have the drawbacks of higher switching actions than that of the traditional VSI, which would introduce more switching loss of the system.

Toward this end, as one of the most popular modulation strategy of power inverters, the SVPWM technique has drawn many researchers' attention [70-73]. However, most of these papers gave the results modified from the principles of VSI directly, which lack in-depth explanation and analysis. Some important inherent issues haven't been explained very clearly, for example, how to select the shoot-through states without increasing the switching numbers, the influences of switching actions on harmonic spectrums. Besides, the implementation schemes of maximum boost control and constant boost control strategies have not been discussed in these literatures.

Hence, to achieve the abovementioned goals, this chapter now presents the SVPWM technique for a three-phase ZSI in detail. This chapter starts by introducing the principles of SVPWM technique for a three-phase ZSI step by step. According to different selection of null state and shoot-through state, various switching patterns of SVPWM technique are explored and compared with the traditional carrier-based strategies. Afterwards, implementation schemes of maximum boost control and constant

boost control methods based on SVPWM theory are presented. At last, all the proposed schemes have been validated by simulation and experiment results under different operating conditions.

2.2 SVPWM Theory of Three-Phase ZSI

In this section, the SVPWM technique for a three-phase ZSI is introduced in detail. At first, by employing a proper designed transformation matrix, a new two dimensional coordinate frame and corresponding basic space vectors in this frame are established. Then, the selection of the active vector, shoot-through vector and null vectors are

2.2.1 Establishment of New Coordinate Frame and Basic Space Vectors

As illustrated in Fig. 1.1, V_a , V_b and V_c are the output voltages of a three-phase ZSI. The six power switches S_a , S_b , S_c , S_a' , S_b' or S_c' are controlled by an appropriate switching sequence to shape the output. When the switching variable a , b , c , a' , b' or c' is 1, the corresponding switch is switched on; alternatively, the value 0 indicates switching off. The relationship between the switching variable vector $[a \ b \ c]^T$ and the phase voltage vector $[V_a \ V_b \ V_c]^T$ is given as follows:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2-1)$$

As listed in Table 2–1, there are fifteen possible combinations of on-off patterns for the six power switches which feed the power inverter, including six active states (V_1 – V_6), two null states (V_0 , V_7) and seven shoot-through states (V_{sh1} – V_{sh7}). Essentially, since a , b and c can be 0 or 1, each of V_{sh1} , V_{sh2} and V_{sh3} contains four substates, and each of V_{sh4} , V_{sh5} and V_{sh6} contains two substates. Assuming d and q are the horizontal and vertical axes of the new coordinate frame, the dq transformation given in (2-2) can transform a three dimensional voltage vector $\vec{V}_{abc} = [V_a \ V_b \ V_c]^T$ into a two dimensional vector in the dq coordinate frame $\vec{V}_{dq} = [V_d \ V_q]^T$, which is written in (2-3). The derived output phase voltages of the fifteen states in the dq coordinate frame are listed in Table 2–1, and the

corresponding voltage vectors termed basic space vectors are mapped into the dq plane in Fig. 2.1.

$$T_{abc-dq} = \begin{bmatrix} \frac{2}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \quad (2-2)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{abc-dq} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V_{dc} \begin{bmatrix} \frac{\sqrt{6}}{3} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2-3)$$

TABLE 2–1: Switching states and output voltages of three-phase ZSI (!X represents complement of x, where x=a,b,c)

states		S_a	S_a'	S_b	S_b'	S_c	S_c'	V_d	V_q
Null	V_0	0	1	0	1	0	1	0	0
Active	V_1	0	1	0	1	1	0	$-\frac{\sqrt{6}}{6}V_{dc}$	$-\frac{\sqrt{2}}{2}V_{dc}$
Active	V_2	0	1	1	0	0	1	$-\frac{\sqrt{6}}{6}V_{dc}$	$\frac{\sqrt{2}}{2}V_{dc}$
Active	V_3	0	1	1	0	1	0	$-\frac{\sqrt{6}}{3}V_{dc}$	0
Active	V_4	1	0	0	1	0	1	$\frac{\sqrt{6}}{3}V_{dc}$	0
Active	V_5	1	0	0	1	1	0	$\frac{\sqrt{6}}{6}V_{dc}$	$-\frac{\sqrt{2}}{2}V_{dc}$
Active	V_6	1	0	1	0	0	1	$\frac{\sqrt{6}}{6}V_{dc}$	$\frac{\sqrt{2}}{2}V_{dc}$
Null	V_7	1	0	1	0	1	0	0	0
Shoot-through	V_{sh1}	1	1	b	!b	c	!c	0	0
Shoot-through	V_{sh2}	a	!a	1	1	c	!c	0	0
Shoot-through	V_{sh3}	a	!a	b	!b	1	1	0	0
Shoot-through	V_{sh4}	1	1	1	1	c	!c	0	0
Shoot-through	V_{sh5}	1	1	b	!b	1	1	0	0
Shoot-through	V_{sh6}	a	!a	1	1	1	1	0	0
Shoot-through	V_{sh7}	1	1	1	1	1	1	0	0

Figure 2.1 Basic space vectors and sectors of three-phase ZSI

The objective of SVPWM technique is to approximate the desired output voltage by setting proper switching patterns of the power switches. As shown in Fig. 2.1, the desired output voltage vector $\vec{V}_{ref}$ can be approached by the linear combinations of the fifteen basic space vectors, which is described by the following equation:

$$\vec{V}_{ref} = \frac{T_i}{T} \vec{V}_i + \frac{T_j}{T} \vec{V}_j + \frac{T_0}{T} (\vec{V}_0, \vec{V}_7) + \frac{T_{sh}}{T} \vec{V}_{shk} \quad (2-4)$$

($i, j = 1 \sim 6, k = 1 \sim 7$)

where $\vec{V}_{ref}$ represents the desired phase voltage vectors in the dq plane; $\vec{V}_n$ and T_n represent one of the fifteen basic space vectors and the corresponding duration time.

The reference voltage vector $\vec{V}_{ref}$ of the three-phase ZSI is obtained by mapping the desired three-phase voltages to the dq plane through (2-3).

$$\vec{V}_{ref} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{abc-dq} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{\sqrt{6}}{2} \hat{V}_{pn} \begin{bmatrix} \cos \omega t \\ \sin \omega t \end{bmatrix} \quad (2-5)$$

The envelope of the hexagonal formed by the six active basic space vectors is the locus of maximum $\vec{V}_{ref}$, as illustrated in Fig. 2.1. Therefore, the magnitude of $\vec{V}_{ref}$ must

be limited to the shortest radius of this envelope that is the circle in Fig. 2.1, when $\vec{V}_{ref}$ is a rotating vector. This gives a maximum magnitude of $\vec{V}_{dc}/\sqrt{2}$ for $\vec{V}_{ref}$. It should be noted that beyond the hexagon tracking mode, where null vector is not available, the voltage boost ability is not possible. According to (1-6), (1-9) and (2-5), the modulation index M must have the maximum value of $2/\sqrt{3}$, which allows the SVPWM technique to generate an output voltage with $2/\sqrt{3}$ times the amplitude by the classical carrier-based sinusoidal PWM (SPWM) strategy. Therefore, in terms of the final output voltage amplitude, it is seen that the SVPWM technique for three-phase ZSI retains the same benefit of wide linear operation range as for traditional three-phase VSIs. Actually, with the third harmonic injection technique, the linear operation ranges of the maximum boost and constant boost control methods can also be extended to $2/\sqrt{3}$ as mentioned in [40, 41]. However, the following disadvantages have not been solved yet: 1) switching on all the six switches to produce the shoot-through state is needless; 2) increase number of switching transitions compared to that of traditional VSIs. Both these disadvantages can be solved by using SVPWM technique.

2.2.2 Determination of Time Duration for Each Vector

As demonstrated in Fig. 2.1, the selection of the active vectors depends on the phase angle $\theta = \omega t$, it can be easily implemented once the phase angle is detected. It should be noted that two adjacent active vectors should be selected in each sampling interval in order to reduce the switching loss [74], and the switching patterns should be symmetrical and centered for the sake of a low THD and easy implementation [75]. The details of the switching patterns for different sectors are described as follows.

A Condition 1

If $0 \leq \theta \leq \pi/3$ (i.e., Sector 1). One can thus obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_4 \cdot |\vec{V}_4| \cdot \begin{bmatrix} \cos 0 \\ \sin 0 \end{bmatrix} + T_6 \cdot |\vec{V}_6| \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix} \quad (2-6)$$

then through (1-6), (1-8), and (2-5)

$$|\vec{V}_{ref}| = \frac{\sqrt{6}}{2} \hat{V}_{pn} = \frac{\sqrt{6}}{4} M \cdot V_{dc} \quad (2-7)$$

also it is indicated in Table 2-1 that

$$|\vec{V}_4| = |\vec{V}_6| = \frac{\sqrt{6}}{3} \cdot V_{dc} \quad (2-8)$$

substituting (2-7) and (2-8) into (2-6)

$$\Rightarrow \begin{cases} T_4 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{\pi}{3} - \theta) \\ T_6 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin\theta \end{cases} \quad (2-9)$$

and then from (2-4)

$$T_0 + T_{sh} = T - T_4 - T_6 = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] \quad (2-10)$$

Analogously, the time duration of each vector for all the other five sectors can be obtained and discussed as follows.

B Condition 2

If $\pi/3 \leq \theta \leq 2\pi/3$ (i.e., Sector 2). One can obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_6 \cdot |\vec{V}_6| \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix} + T_2 \cdot |\vec{V}_2| \cdot \begin{bmatrix} \cos(2\pi/3) \\ \sin(2\pi/3) \end{bmatrix} \quad (2-11)$$

Referring to the derivation procedure of Condition 1, from (2-4), (2-7) and (2-11) one can get:

$$\Rightarrow \begin{cases} T_6 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{2\pi}{3} - \theta) \\ T_2 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{\pi}{3}) \\ T_0 + T_{sh} = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] \end{cases} \quad (2-12)$$

C Condition 3

If $2\pi/3 \leq \theta \leq \pi$ (i.e., Sector 3), one can thus obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_2 \cdot |\vec{V}_2| \cdot \begin{bmatrix} \cos(2\pi/3) \\ \sin(2\pi/3) \end{bmatrix} + T_3 \cdot |\vec{V}_3| \cdot \begin{bmatrix} \cos\pi \\ \sin\pi \end{bmatrix} \quad (2-13)$$

Referring to the derivation procedure of Condition 1, from (2-4), (2-7) and (2-13) one can get:

$$\Rightarrow \begin{cases} T_2 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\pi - \theta) \\ T_3 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{2\pi}{3}) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] \end{cases} \quad (2-14)$$

D Condition 4

If $\pi \leq \theta \leq 4\pi/3$ (i.e., Sector 4), one can thus obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_3 \cdot |\vec{V}_3| \cdot \begin{bmatrix} \cos\pi \\ \sin\pi \end{bmatrix} + T_1 \cdot |\vec{V}_1| \cdot \begin{bmatrix} \cos(4\pi/3) \\ \sin(4\pi/3) \end{bmatrix} \quad (2-15)$$

Referring to the derivation procedure of Condition 1, from (2-4), (2-7) and (2-15) one can get:

$$\Rightarrow \begin{cases} T_3 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{4\pi}{3} - \theta) \\ T_1 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \pi) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] \end{cases} \quad (2-16)$$

E Condition 5

If $4\pi/3 \leq \theta \leq 5\pi/3$ (i.e., Sector 5), one can obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_1 \cdot |\vec{V}_1| \cdot \begin{bmatrix} \cos(4\pi/3) \\ \sin(4\pi/3) \end{bmatrix} + T_5 \cdot |\vec{V}_5| \cdot \begin{bmatrix} \cos(5\pi/3) \\ \sin(5\pi/3) \end{bmatrix} \quad (2-17)$$

Referring to the derivation procedure of Condition 1, from (2-4), (2-7) and (2-17) one can get:

$$\Rightarrow \begin{cases} T_1 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{5\pi}{3} - \theta) \\ T_5 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{4\pi}{3}) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] \end{cases} \quad (2-18)$$

F Condition 6

If $5\pi/3 \leq \theta \leq 2\pi$ (i.e., Sector 6), one can thus obtain the following equation from Fig. 2.1.

$$T \cdot |\vec{V}_{ref}| \cdot \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} = T_5 \cdot |\vec{V}_5| \cdot \begin{bmatrix} \cos(5\pi/3) \\ \sin(5\pi/3) \end{bmatrix} + T_4 \cdot |\vec{V}_4| \cdot \begin{bmatrix} \cos 2\pi \\ \sin 2\pi \end{bmatrix} \quad (2-19)$$

Referring to the derivation procedure of Condition 1, from (2-4), (2-7) and (2-19) one can get:

$$\Rightarrow \begin{cases} T_5 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(2\pi - \theta) \\ T_4 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{5\pi}{3}) \\ T_0 + T_{sh} = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] \end{cases} \quad (2-20)$$

Then according to (1-7) and (1-9), the T_{sh} can be figured out using the following equation once the parameters T , M , V_{in} and V_{pn} are given.

$$T_{sh} = \frac{T}{2} - \frac{T \cdot M \cdot V_{in}}{4\hat{V}_{pn}} \quad (2-21)$$

And then the time duration of T_0 for each sector can be obtained by substituting (2-21) into (2-10) – (2-20).

2.2.3 Selection of the Shoot-Through Vectors

As discussed above, the selection of the active vectors can be easily determined according to the phase angle θ . However, the selection of the null vectors and shoot-through states is much more complex because all the output voltage of them are the same. Theoretically, T_0 can be any subset of the two null vectors and T_{sh} can be any subset of the seven shoot-through vectors. Besides, by altering the allocations and distributions of the null states and shoot-through states, we can get infinite different switching patterns that are able to obtain the desired output voltages. In order to simplify the analysis, all the null states and shoot-through states are evenly distributed.

Fig. 2.2 demonstrates all the possible transitions between different switching states of SVPWM for a three-phase ZSI, where each arrow indicates half a switching action only (given the definition that one switching action indicates status change of both upper and lower switches of the same leg). For an example, a transition from active state V_4 to the adjacent shoot-through states V_{sh1_1} , V_{sh2_3} or V_{sh3_3} requires half a switching action; while the transition from V_4 to either adjacent active state V_6 or V_5 requires one switching actions at least, respectively. As mentioned above, each of V_{sh1} , V_{sh2} and V_{sh3} contains four substates, thus V_{shm_n} ($m=1\sim3$, $n=1\sim4$) indicates the n^{th} substate of the shoot-through state V_{shm} . Apparently, in Sector 1, since the two active vectors V_4 and V_6 are adopted, the proper shoot-through state between them is V_{sh2_3} , other shoot-through vectors would introduce additional switching actions. Thus, it can be concluded that the selection of the shoot-through states does affect the number of switching actions in one sampling period.

Figure 2.2 Switching transitions between different states of three-phase SL ZSIs

2.2.4 Switching Patterns Analysis

As shown in (2-4), the switching period consists of active states, null states and shoot-through states. The time duration of each state has been discussed already and it's determined by output requirements and operating conditions. The selection of the active states is terminated by the phase angle and the shoot-through states are selected to connect active states and null states according to Fig. 2.2. It should be noted that $T_0 = T_{00} + T_{07}$, where T_{00} and T_{07} represent the time durations of null vectors V_0 and V_7 . It is known that T_{00} and T_{07} can be distributed with infinite different ways and each distribution way yields one switching pattern. The details of different distributions of T_{00} and T_{07} for traditional VSIs are discussed in [76]. In this section, the selection of null states for ZSIs is discussed, which results in three different switching patterns.

Pattern I

Pattern I adopts both null vectors V_0 and V_7 in one switching period, and T_0 is distributed evenly into these two states; that is, $T_{00} = T_{07} = 0.5T_0$. The appropriate shoot-through states are carefully selected according to Fig. 2.2 and evenly inserted between each active vector and null vector. The corresponding switching signals in every sector are depicted in Fig. 2.3 (a) – (f).

(a) Sector 1 ($0 \leq \theta \leq \pi/3$)

(b) Sector 2 ($\pi/3 \leq \theta \leq 2\pi/3$)

(c) Sector 3 ($2\pi/3 \leq \theta \leq \pi$)

(d) Sector 4 ($\pi \leq \theta \leq 4\pi/3$)

(e) Sector 5 ($4\pi/3 \leq \theta \leq 5\pi/3$)

(f) Sector 6 ($5\pi/3 \leq \theta \leq 2\pi$)

Figure 2.3 SVPWM control switching pattern I for a three-phase ZSI

Pattern II

Pattern II adopts only one null vector V_0 , and T_0 is entirely distributed into this state; that is, $T_{00}=T_0$, $T_{07}=0$. The appropriate shoot-through states are carefully selected according to Fig. 2.2 and evenly inserted between each active vector and null vector. The corresponding switching signals in every sector are depicted in Fig. 2.4 (a) – (f).

(a) Sector 1 ($0 \leq \theta \leq \pi/3$)

(b) Sector 2 ($\pi/3 \leq \theta \leq 2\pi/3$)

(c) Sector 3 ($2\pi/3 \leq \theta \leq \pi$)

(d) Sector 4 ($\pi \leq \theta \leq 4\pi/3$)

(e) Sector 5 ($4\pi/3 \leq \theta \leq 5\pi/3$)

(f) Sector 6 ($5\pi/3 \leq \theta \leq 2\pi$)

Figure 2.4 SVPWM control switching pattern II for a three-phase ZSI

Pattern III

Pattern III adopts only the other null vector V_7 , and T_0 is entirely distributed into this state also; i.e., $T_{07}=T_0$, $T_{00}=0$. The appropriate shoot-through states are carefully selected according to Fig. 2.2 and evenly inserted between each active vector and null vector. The corresponding switching signals in every sector are depicted in Fig. 2.5 (a) – (f).

(a) Sector 1 ($0 \leq \theta \leq \pi/3$)

(b) Sector 2 ($\pi/3 \leq \theta \leq 2\pi/3$)

(c) Sector 3 ($2\pi/3 \leq \theta \leq \pi$)

(d) Sector 4 ($\pi \leq \theta \leq 4\pi/3$)

(e) Sector 5 ($4\pi/3 \leq \theta \leq 5\pi/3$)

(f) Sector 6 ($5\pi/3 \leq \theta \leq 2\pi$)

Figure 2.5 SVPWM control switching pattern III for a three-phase ZSI

From the above analysis, we can summarize the procedure for implementing the SVPWM technique for a three-phase ZSI as follows. It is noted that the sequence of step 2 and step 3 are interchangeable.

- Step 1. Establish new coordinate frame and basic space vectors
- Step 2. select proper active, null and shoot-through vectors
- Step 3. determine time duration of each vector
- Step 4. determine the switching time of each switch

2.2.5 Comparison of Switching Actions

It is known that switching actions would introduce switching loss to the system, thus we will conduct the comparison study of the switching actions between carrier-based strategy and SVPWM-based patterns. As shown in Fig. 1.11, to produce the shoot-through state, the simple boost strategy purposely turns on all the six switches simultaneously (i.e. shoot-through state V_{sh7}) when the value of triangle wave is greater than that of the upper envelope V_p or smaller than that of the lower envelope V_n . Consequently, the number of each switching action will be increased once per switching cycle. It can be seen from Figs 2.3, 2.4 and 2.5 that, for all three patterns of SVPWM-based control method, only one switching variable of the six switches will change during each switching transition, which is very easy to implement for digital control system. All the specified numbers of switching actions in different control patterns with different phase angles are listed in Table 2-2. Though the number of each individual switch may be different in different sector, the total number of the six switches in one switching cycle will be always the same. It is shown in the table that the total number in each switching cycle is twelve for the carrier-based strategy, and that of the pattern I is reduced to six, while that of pattern II and III is as small as four. As we know, fewer switching actions yield less switching loss. Thus, all three SVPWM-based patterns lead to less switching loss compared with the traditional carrier-based strategy. In addition, the comparison of switching actions for all the four control schemes is demonstrated in Fig. 2.6. It is shown clearly that compared with the carrier-based method, a 50% switching action number reduction can be achieved by using the pattern I of SVPWM technique, and the reduction can be as high as 75% by adopting the pattern II and III of SVPWM technique.

Table 2–2: Numbers of switching actions of carrier- and SVPWM-based simple boost control of a three-phase ZSI

Sectors		1	2	3	4	5	6
Carrier-Based Strategy	S_a	2	2	2	2	2	2
	S_a'	2	2	2	2	2	2
	S_b	2	2	2	2	2	2
	S_b'	2	2	2	2	2	2
	S_c	2	2	2	2	2	2
	S_c'	2	2	2	2	2	2
Total		12	12	12	12	12	12
SVPWM-Based Pattern I	S_a	1	1	1	1	1	1
	S_a'	1	1	1	1	1	1
	S_b	1	1	1	1	1	1
	S_b'	1	1	1	1	1	1
	S_c	1	1	1	1	1	1
	S_c'	1	1	1	1	1	1
Total		6	6	6	6	6	6
SVPWM-Based Pattern II	S_a	1	1	0	0	1	1
	S_a'	1	1	0	0	1	1
	S_b	1	1	1	1	0	0
	S_b'	1	1	1	1	0	0
	S_c	0	0	1	1	1	1
	S_c'	0	0	1	1	1	1
Total		4	4	4	4	4	4
SVPWM-Based Pattern III	S_a	0	1	1	1	1	0
	S_a'	0	1	1	1	1	0
	S_b	1	0	0	1	1	1
	S_b'	1	0	0	1	1	1
	S_c	1	1	1	0	0	1
	S_c'	1	1	1	0	0	1
Total		4	4	4	4	4	4

Figure 2.6 Switching action comparison of both carrier- and SVPWM-based simple boost control of ZSIs

2.3 Simulation and Experimental Verification

2.3.1 Simulation Verification

To verify the validity of the proposed three patterns, the following study case is conducted in Matlab/Simulink software. Regarding the parameter selection of the Z network components, several references have discussed this issue to achieve different objectives. Among them, [30] has studied the parameter design to avoid the discontinuous conduction mode (DCM) under different operation conditions; in [77], the parameters of Z-network are properly chosen to limit the voltage ripple of the capacitors and inductors in steady state; while the design guideline of [44] is to obtain suitable transient performances with the help of small signal models. According to these references, the parameter selection is also affected by the voltage and power level of the simulation case. In this thesis, the typical values of [44] have been adopted. To get better understanding of this selection strategy, the same design guideline has been performed for selecting the Z-network components of SL ZSIs which will be discussed in Chapter 6. The main circuit parameters of ZSIs are selected as follows:

- 1) impedance network: $L_1=L_2=300\mu\text{H}$, $C_1=C_2=360\mu\text{F}$;
- 2) output LC filter: $L_f=2\text{mH}$, $C_f=15\mu\text{F}$;

- 3) three-phase balanced resistive load: $R=25\Omega$;
- 4) switching frequency: $f_s=10\text{kHz}$;
- 5) input source voltage $V_{in}=100\text{V}$;
- 6) output fundamental frequency: $f_o=50\text{Hz}$;
- 7) modulation index $M=0.7$;
- 8) shoot-through duty ratio $D=0.3$;

Thus, according to the steady state equations given in Chapter 1, the theoretical values of SVPWM patterns are listed in the following table.

Table 2–3: Theoretical values of SVPWM-based three-phase ZSI

<i>Conditions</i>			<i>Theoretical Values</i>				
$V_{in} \text{ (V)}$	M	D	B	G	$V_{dc} \text{ (V)}$	$V_C \text{ (V)}$	$\hat{V}_{ab} \text{ (V)}$
100	0.7	0.3	2.5	1.75	250	175	151.55

All the simulation results of three patterns are depicted in Figs. 2.7, 2.8 and 2.9, where S_{ap} , S_{an} , S_{bp} , S_{bn} , S_{cp} , S_{cn} indicate the upper and lower switch actions of phase a , phase b and phase c , and V_{dc} , V_c , V_{pn} , V_{ab} indicate the voltage stresses of the dc-link, Z-network capacitor, output phase before the filter and line voltage after the filter, respectively. To clearly demonstrate the number of switching actions of each switch, the enlarged waveforms of switching actions in one switching cycle for three patterns are depicted in Fig. 2.7(d), Fig. 2.8(d) and Fig. 2.9(d). The switching actions of all switches are in accordance with the theoretical results shown in Figs. 2.3, 2.4 and 2.5 and the number of switching actions is the same as shown in Table 2-2. The voltage stresses of all three patterns are depicted in Fig. 2.7(e), Fig. 2.8(e) and Fig. 2.9(e), which support the theoretical results shown in Table 2-3. In addition, to investigate the effects of switching numbers on the THD values, harmonic spectrums of the output voltage using all three patterns are given in Fig. 2.10. It is shown clearly that all the harmonics with dominant amplitudes start at around 10 kHz, which equals to the switching frequency, and the amplitudes of pattern II and III are larger than that of pattern I. Besides, the output voltages of pattern II and III contain more harmonics in the sidebands as compared with that of pattern I.

(a)

(b)

(c)

(d)

(e)

Figure 2.7 Simulation results of SVPWM pattern I: (a) switching actions of phase a ; (b) switching actions of phase b ; (c) switching actions of phase c ; (d) switching actions of 6 switches in one switching cycle; (e) voltage stresses in steady state.

Figure 2.8 Simulation results of SVPWM pattern II: (a) switching actions of phase a ; (b) switching actions of phase b ; (c) switching actions of phase c ; (d) switching actions of 6 switches in one switching cycle; (e) voltage stresses in steady state.

Figure 2.9 Simulation results of SVPWM pattern III: (a) switching actions of phase a ; (b) switching actions of phase b ; (c) switching actions of phase c ; (d) switching actions of 6 switches in one switching cycle; (e) voltage stresses in steady state.

(a)

(b)

(c)

Figure 2.10 Harmonic spectrums of output voltages: (a) pattern I; (b) pattern II; (c) pattern III.

2.3.2 Experimental Verification

To further verify the validity of the proposed switching patterns, the corresponding hardware testing circuits were also constructed. In the hardware testing circuits, the components are selected based on the simulation parameters, voltage rating, current rating and power rating.

Table 2–4: Components used in experimental verification

Components	Manufactures	Parameters	Ratings
Z-network inductor	MES	2mH	Max 5A
Z-network capacitor	BHC	800 μ F	Max 450V
Power diode	SEMIKRON		
Power IGBT	SEMIKRON		Max 800V
Filter inductor	MES	2mH	5A
Filter capacitor	BHC	15 μ F	Max 230V
Resistive load	RS	25 Ω	Max 300W

The control scheme is utilized by employing a DSPACE ds1006 with composed C codes and the switching frequency is set to be 10kHz. Due to the limitations of the laboratory conditions and equipment, the experiments can only be done at low voltage and power level. The input source voltage used here is 50V and the other parameters such as the modulation index and the shoot-through duty ratio are chosen the same as the simulation case, thus all the voltage stresses will reduce to half. The experimental waveforms in steady-state of all three patterns are depicted in Figs. 2.11–2.13. Switching actions of all switches for three patterns together with the enlarged waveforms of switching actions in two switching cycles are depicted in Figs. 2.11-2.13 (a)-(f), respectively. Voltage stresses of all patterns are depicted in Figs. 2.11-2.13 (g)(h), respectively. The experiment results show a good agreement with the theoretical analysis and simulation results.

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{cn} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{cn} (5V/div)

(g) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(h) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 2.11 Experiment results of SVPWM pattern I: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b in two switching cycles; (e) switching actions of phase c ; (f) enlarged waveforms of switching actions of phase c in two switching cycles; (g) V_c and V_{dc} ; (h) V_{pn} and V_{ab}

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{cn} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{cn} (5V/div)

(g) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(h) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 2.12 Experiment results of SVPWM pattern II: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b ; (e) switching actions of phase c ; (f) enlarged waveforms of switching actions of phase c ; (g) V_c and V_{dc} ; (h) V_{pn} and V_{ab}

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{cn} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{cn} (5V/div)

(g) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(h) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 2.13 Experiment results of SVPWM pattern III: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b ; (e) switching actions of phase c ; (f) enlarged waveforms of switching actions of phase c ; (g) V_c and V_{dc} ; (h) V_{pn} and V_{ab}

2.4 Implementation Scheme of Maximum Boost Control Method Based on SVPWM Theory

2.4.1 Principle of Maximum Boost Control Method

According to the principles of maximum boost control, M has a very limited operation range, and D should be as large as possible during each carrier cycle to maximize the boost factor B . As is known, the purpose of the null state is to fill in the blanks of the switching period, thus it will not affect the output reference voltage. From (2-10) – (2-20), it is known that the total time duration of null states and shoot-through states are fixed to a certain value with the given condition. Hence, the time duration of null states should be made to be zero, by which the maximum T_{shmax} can be obtained. The detailed expressions of T_{shmax} are expressed as follows:

$$T_{shmax} = \begin{cases} T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] & 0 \leq \theta \leq \frac{\pi}{3} \\ T \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] & \frac{\pi}{3} \leq \theta \leq \frac{2\pi}{3} \\ T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] & \frac{2\pi}{3} \leq \theta \leq \pi \\ T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] & \pi \leq \theta \leq \frac{4\pi}{3} \\ T \left[1 + \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] & \frac{4\pi}{3} \leq \theta \leq \frac{5\pi}{3} \\ T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] & \frac{5\pi}{3} \leq \theta \leq 2\pi \end{cases} \quad (2-22)$$

It can be seen from (2-22) that T_{shmax} varies with θ . The sketch map of T_{shmax} versus θ in one cycle is demonstrated in Fig. 2.14. Thus, one can figure out the average value of T_{shmax} , by using (2-23).

Figure 2.14 Sketch map of the maximum shoot-through state time duration

$$\begin{aligned} \bar{T}_{shmax} = \frac{T}{2\pi} & \left\{ \int_0^{\frac{\pi}{3}} \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] d\theta + \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] d\theta \right. \\ & + \int_{\frac{2\pi}{3}}^{\pi} \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\frac{\pi}{6} + \theta) \right] d\theta + \int_{\pi}^{\frac{4\pi}{3}} \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\frac{\pi}{6} - \theta) \right] d\theta \\ & \left. + \int_{\frac{4\pi}{3}}^{\frac{5\pi}{3}} \left[1 + \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] d\theta + \int_{\frac{5\pi}{3}}^{2\pi} \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\frac{\pi}{6} + \theta) \right] d\theta \right\} \quad (2-23) \\ & = \frac{T}{2\pi} (2\pi - 3\sqrt{3}M) \end{aligned}$$

Accordingly, the average value of maximum shoot-through duty ratio $\bar{D}_{max}$ can be expressed by

$$\bar{D}_{max} = \frac{\bar{T}_{shmax}}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \quad (2-24)$$

Then, the maximum boost factor B_{max} and maximum voltage boost inversion gain, G_{max} , can be written as:

$$B_{max} = \frac{1}{1 - 2\bar{D}_{max}} = \frac{\pi}{3\sqrt{3}M - \pi} \quad (2-25)$$

$$G_{max} = MB_{max} = \frac{M \cdot \pi}{3\sqrt{3}M - \pi} \quad (2-26)$$

It is indicated in (2-26) that the maximum boost inversion ability of three-phase ZSIs only depends on M . Fig. 2.7 shows how various modulation indices affect the voltage

gain for different two cases, carrier-based and SVPWM-based maximum boost control methods. It can be observed from Fig. 2.15 that within the unit modulation index range, the two control methods behave identically, while the SVPWM technique extends the operation range to $2/\sqrt{3}$ due to its inherent feature. For both control methods, the voltage gain tends to infinity when $M = \pi/3\sqrt{3}$, then it decreases smoothly with the increase of M .

Figure 2.15 G versus M of carrier- and SVPWM-based maximum boost control of ZSI

Additionally, it is indicated in Chapter 1 that the voltage stresses across the Z-network capacitors of three-phase ZSI can be calculated by the following equation:

$$V_{C1} = V_{C2} = \frac{1 - D_{max}}{1 - 2D_{max}} V_{in} \quad (2-27)$$

According to (1-7) (1-9) (2-24) and (2-27), the expression of V_{C1} and V_{C2} are given as:

$$V_{C1} = V_{C2} = \frac{3\sqrt{3} \cdot \hat{V}_{pn}}{\pi} \quad (2-28)$$

Then, from (2-28), one can find that V_{C1} and V_{C2} are determined by the desired output phase voltage only.

2.4.2 Implementation Scheme Based on SVPWM Theory

Following the steps summarized in the previous section, it's easy to find the reference voltage using the dq transformation matrix given in (2-5). The selection of active vectors is determined by θ , and the corresponding time durations can be obtained using (2-10) –

(2-20). As discussed before, no null state is adopted in maximum boost control method, thus only active states and shoot-through states are utilized for implementation. Different switching patterns are classified due to the selection of null states, hence, only one switching pattern for the SVPWM-based maximum boost control method in each sector is illustrated in Fig. 2.16 (a) – (f), respectively.

(a) Sector 1 ($0 \leq \theta \leq \pi/3$)

(b) Sector 2 ($\pi/3 \leq \theta \leq 2\pi/3$)

(c) Sector 3 ($2\pi/3 \leq \theta \leq \pi$)

(d) Sector 4 ($\pi \leq \theta \leq 4\pi/3$)

(e) Sector 5 ($4\pi/3 \leq \theta \leq 5\pi/3$)

(f) Sector 6 ($5\pi/3 \leq \theta \leq 2\pi$)

Figure 2.16 Implementation scheme of maximum boost control for a three-phase ZSI based on SVPWM theory

Using the proposed SVPWM-based control method, only one switching variable of the six switches will change during each switching transition. It means that each power switch will turn on and off once at most in each carrier cycle, which is very easy to implement in the digital control system. The on-off switching loss would be significantly reduced, and the harmonic condition would be improved, compared with the traditional carrier-based maximum boost control strategy.

2.4.3 Comparison of Switching Actions

As mentioned above, one of the most important advantages of the SVPWM scheme is the reduction of switching actions. In this part, the switching actions of all the six switches in one switching cycle using different control schemes are discussed. As shown in Fig. 1.13, to produce the maximum shoot-through state, the carrier-based strategy purposely turns on all the six switches simultaneously (i.e. shoot-through state V_{sh7}) when the value of triangle wave is greater than the largest instantaneous value of the three sinusoidal references or less than the smallest instantaneous value. Consequently, the number of switching actions for two switches would be reduced once and that for the other four switches would be increased once. Generally, the total number of switching actions would be increased for the carrier-based strategy. On the other hand, it can be seen from Fig. 2.8 that, the number of two switches would be reduced once while that of

the other switches kept the same. In general, the total number of switching actions would be reduced for the SVPWM scheme. All the specified numbers of switching actions of the two control schemes are listed in Table 2–5 according to different phase angles.

TABLE 2–5: Numbers of switching actions of maximum boost control of three-phase ZSI
(Subsector n (n=1~12) corresponds $(n-1) \pi/6 \leq \theta \leq n \pi/6$)

Subsector		1	2	3	4	5	6	7	8	9	10	11	12
Carrier-Based	S_a	2	0		0		2		2		2		2
	S_a'	2	2		2		2		0		0		2
	S_b	2	2		2		0		0		2		2
	S_b'	0	0		2		2		2		2		0
	S_c	0	2		2		2		2		0		0
	S_c'	2	2		0		0		2		2		2
Total		8	8		8		8		8		8		8
SVPWM-Based	S_a	0		1		1		1		1		0	
	S_a'	1		1		0		0		1		1	
	S_b	1		0		0		1		1		1	
	S_b'	1		1		1		1		0		0	
	S_c	1		1		1		0		0		1	
	S_c'	0		0		1		1		1		1	
Total		4		4		4		4		4		4	

Though the behavior of each individual switch may be different, the total number of the six switches in one switching period will be always the same. It is shown in the table that the total switching action number of the six switches is 8 for carrier-based strategy, while a 50% reduction is achieved by using the SVPWM scheme.

2.5 Simulation and Experimental Verification

2.5.1 Simulation Verification

To verify the validity of the proposed control schemes, different study cases are conducted in Matlab/Simulink software. The main circuit parameters of ZSIs are selected as follows:

- 1) impedance network: $L_1=L_2=300\mu\text{H}$, $C_1=C_2=360\mu\text{F}$;
- 2) output LC filter: $L_f=2\text{mH}$, $C_f=15\mu\text{F}$;
- 3) three-phase balanced resistive load: $R=25\Omega$;
- 4) switching frequency: $f_s=10\text{kHz}$
- 5) desired output phase voltage: 110V (root means square (RMS) value)

For all the four cases, the configurations of the modulation indices are different; thus, from the foregoing theoretical analysis, it is known that the values of B and G will vary with different conditions. To maintain a stable output phase voltage, different input DC source voltage should be configured appropriately for each case according to (1-9) and (2-26). To compare the voltage stresses of simple boost and maximum boost control strategies, the theoretical configuration values of all cases are listed in Table 2–6. It is shown that with the increase of M , the voltage stresses across the DC-link V_{dc} decrease due to a smaller boost factor B . However, a higher DC source voltage V_{in} is required under the large M condition, because the corresponding voltage gain G gets smaller..

Table 2–6: Theoretical values of maximum boost control of ZSI under different operating conditions

<i>Case No.</i>	<i>Condition</i>				<i>Expected Values</i>		
	V_{in} (V)	M	B	G	V_{dc} (V)	V_{C1} (V)	V_{ab} (V)
1	125.71	0.8	3.09	2.48	388.96	257.30	190.53 (RMS)
2	168.93	0.9	2.05	1.84	345.71		
3	203.52	1.0	1.53	1.53	311.18		
4	231.74	1.1	1.22	1.34	282.93		

The simulated waveforms of the proposed SVPWM-based maximum boost control method with different M ($M=0.8, 0.9, 1.0$, and 1.1) are shown in Fig. 2.17 (a), (b), (c) and (d), respectively, where V_{dc} indicates the voltage stress across the DC-link, V_{C1} indicates the Z-capacitor voltage, V_{pn} indicates the output phase voltage before the filter, and V_{ab} indicates the output line-to-line voltage after the filter. All the measured values of V_{dc} , V_{C1} and V_{ab} in different cases together with the errors are stated in Table 2–7. It can be seen that, the maximum errors of the parameters are 3.21%, 2.91% and 3.39%, respectively, which proves the validity of the proposed control scheme.

Table 2–7: Measured values and corresponding errors of SVPWM-based maximum boost control of ZSI

Case No.	V_{dc} (V)	Error (%)	V_{C1} (V)	Error (%)	V_{ab} (V)	Error (%)
1	377.14	3.07	249.83	2.91	185.91	2.42
2	334.66	3.21	250.49	2.65	184.06	3.39
3	303.72	2.40	252.65	1.81	185.40	2.69
4	279.17	1.34	254.36	1.14	186.25	2.24

(a) Case 1: $M=0.8$ and $V_{in}=125.71V$

(b) Case 2: $M=0.9$ and $V_{in}=168.93V$

(c) Case 3: $M=1.0$ and $V_{in}=203.52V$

(d) Case 4: $M=1.1$ and $V_{in}=231.74V$

Figure 2.17. Simulation results of SVPWM-based maximum boost control of ZSI

2.5.2 Experimental Verification

To further verify the validity of the proposed control scheme, the corresponding hardware testing circuits were also constructed to compare with the simulation results. The main circuit components are selected as listed in Table 2-2. Also, the desired output phase voltage is reduced to 55V (RMS value) due to the laboratory limitation. Thus, the input source voltage and all the voltage stresses will reduce to half. The control scheme is utilized by employing a DSPACE ds1006 with composed C codes and the switching frequency is set to be 10kHz. The experimental waveforms of the switching actions of phases a , b , and c together with the enlarged waveforms in two switching cycles are depicted in Fig. 2.18, and all the voltage stresses in steady-state of the cases $M=0.8$, 0.9 and 1.0 are depicted in Figs. 2.19–2.21, respectively, which show a good agreement with the theoretical analysis and simulation results.

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{cn} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{cn} (5V/div)

Figure 2.18. Switching actions of SVPWM-based maximum boost control: (a) phase a ; (b) enlarged waveforms in two switching cycles; (c) phase b ; (d) enlarged waveforms in two switching cycles; (e) switching actions of phase c ; (f) enlarged waveforms in two switching cycles

(g) CH1: V_C (50V/div); CH2: V_{dc} (50V/div)

(h) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.19. Experiment results of SVPWM-based maximum boost control with $M=0.8$ and $V_{in}=62.8V$

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.20. Experiment results of SVPWM-based maximum boost control with $M=0.9$ and $V_{in}=84.5V$

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.21. Experiment results of SVPWM-based maximum boost control with $M=1.0$ and $V_{in}=101.8V$

2.6 Implementation Scheme of Constant Boost Control Method Based on SVPWM Theory

2.6.1 Principle of Constant Boost Control Method

As introduced in [41], the key point of the constant boost control is to achieve maximum boost ability while keeping the duty ratio constant. That is, D should reach the maximum possible constant regardless of the phase angle, which corresponds to a maximum value of T_{sh} . The detailed expressions of T_{shmax} for each sector are given in (2-22) and the sketch map of T_{shmax} versus θ is depicted in Fig. 2.14. As shown in Fig. 2.14, the T_{shmax} reaches its minimum value when $\theta=(2n+1)\pi/6$ ($n=0\sim5$). Obviously, this minimum value would satisfy the requirements of the constant boost control method

Thus, the corresponding values of T_{sh} , D , B and G can be expressed by the following equations:

$$T_{sh} = T(1 - \frac{\sqrt{3}}{2}M) \quad (2-29)$$

$$D = \frac{T_{sh}}{T} = 1 - \frac{\sqrt{3}}{2}M \quad (2-30)$$

$$B = \frac{1}{1 - 2D} = \frac{1}{\sqrt{3}M - 1} \quad (2-31)$$

$$G = MB = \frac{M}{\sqrt{3}M - 1} \quad (2-32)$$

It is shown in (2-32) that, the boost inversion ability of constant boost control method, as with that of the maximum boost control, depends on modulation index only. Fig. 2.22 shows how various modulation indices affect the voltage gain for both carrier-based and SVPWM-based constant boost control methods of a three-phase SL ZSI. It can be observed from Fig. 2.22 that, similar to the maximum boost control method, within the unit modulation index range, the two control methods behave identically, while the SVPWM technique extends the operation range to $2/\sqrt{3}$. For both control method, the voltage gain tends to infinity when $M = \sqrt{3}/3$, then it decreases smoothly with the increase of M .

Figure 2.22 G versus M of carrier- and SVPWM-based constant boost control of ZSI

Additionally, according to (1-7) (1-9) (2-27) and (2-30), the voltage stresses across the Z-network capacitors, V_{C1} and V_{C2} can be expressed as:

$$V_{C1} = V_{C2} = \sqrt{3}\hat{V}_{pn} \quad (2-33)$$

As with that of the maximum boost control method, the V_C of constant boost control method is determined by the required output voltage only.

2.6.2 Implementation Scheme and Switching Action Comparison

According to the aforementioned principles, it's easy to figure out the time durations of each state and following the steps summarized in the previous section. All the three patterns for simple boost control can be applied to constant boost control and the switching signals can be referred to Figs. 2.3-2.5.

The comparison of switching actions between carrier- and SVPWM-based constant boost control methods is also studied. As shown in Fig. 1.14, to produce the shoot-through state, the carrier-based constant boost control method purposely turns on all the six switches simultaneously (i.e. shoot-through state V_{sh7}) when the value of triangle wave is greater than that of the upper envelope V_p or smaller than that of the lower envelope V_n . Consequently, the number of each switching action will be increased once per switching cycle. Fortunately, the waveform of V_p or V_n overlaps with part of one of the three-phase sinusoidal waveforms. As a result, one switch of the corresponding phase leg would keep conducting state, and the number of switching action would be zero. Generally, for the carrier-based strategy, the number of switching action would be one for the given switch and that of all the other five switches would be two. It can be seen from Figs. 2.3-2.5 that, for the SVPWM-based control schemes, only one switching variable of the six switches will change during each switching transition, which is easy to implement for digital control system. All the specified numbers of switching actions using different control schemes are listed in Table 2-8. It is shown in the table that the total number in each switching cycle is 10 for the carrier-based strategy, and that of the pattern I is reduced to 6, while that of pattern II and III is as small as 4.

TABLE 2–8: Numbers of switching actions of constant boost control of three-phase ZSI
(Subsector n (n=1~12) corresponds $(n-1)\pi/6 \leq \theta \leq n\pi/6$)

Subsector		1	2	3	4	5	6	7	8	9	10	11	12
Carrier-Based	S_a	2	2		2		0		2		2		2
	S_a'	0	2		2		2		2		2		0
	S_b	2	2		2		2		2		0		2
	S_b'	2	2		0		2		2		2		2
	S_c	2	0		2		2		2		2		2
	S_c'	2	2		2		2		0		2		2
Total		10	10		10		10		10		10		10
SVPWM-Based Pattern I	S_a	1		1		1		1		1		1	
	S_a'	1		1		1		1		1		1	
	S_b	1		1		1		1		1		1	
	S_b'	1		1		1		1		1		1	
	S_c	1		1		1		1		1		1	
	S_c'	1		1		1		1		1		1	
Total		6		6		6		6		6		6	
SVPWM-Based Pattern II	S_a	1		1		0		0		1		1	
	S_a'	1		1		0		0		1		1	
	S_b	1		1		1		1		0		0	
	S_b'	1		1		1		1		0		0	
	S_c	0		0		1		1		1		1	
	S_c'	0		0		1		1		1		1	
Total		4		4		4		4		4		4	
SVPWM-Based Pattern III	S_a	0		1		1		1		1		0	
	S_a'	0		1		1		1		1		0	
	S_b	1		0		0		1		1		1	
	S_b'	1		0		0		1		1		1	
	S_c	1		1		1		0		0		1	
	S_c'	1		1		1		0		0		1	
Total		4		4		4		4		4		4	

2.7 Simulation and Experimental Verification

2.7.1 Simulation Verification

To verify the validity of the proposed SVPWM-based switching patterns of constant boost control schemes, different study cases are conducted in Matlab/Simulink software.

The main circuit parameters are selected as follows:

- 1) impedance network: $L_1=L_2=L_3=L_4=300\mu\text{H}$, $C_1=C_2=360\mu\text{F}$;
- 2) output LC filter: $L_f=2\text{mH}$, $C_f=15\mu\text{F}$;
- 3) resistive load of each phase: $R=25\Omega$;
- 4) switching frequency: $f_s=10\text{kHz}$
- 5) desired output phase voltage: 110V (RMS)

As with the cases of the maximum boost control, the modulation index is different for each case; and consequently, the values of B and G will vary with different operating conditions. To maintain the stable output phase voltage, different input DC source voltages should be configured appropriately for all cases according to (1-9) and (2-32). Theoretical configurations and expected values of all cases are listed in Table 2–9. It indicates that, like the maximum boost control, with the increase of M , the voltage stress of DC-link V_{dc} decreases and the required input DC source voltage V_{in} increases. In addition, the required value of V_{in} with the same M is larger than that of the maximum boost control method because the voltage gain is smaller. Besides, the Z-capacitor voltage V_{C1} is higher than that of the maximum boost control method.

Table 2–9: Theoretical values of constant boost control of ZSI under different operating conditions

Case No.	Condition				Expected Values		
	V_{in} (V)	M	B	G	V_{dc} (V)	V_{C1} (V)	V_{ab} (V)
1	150.0	0.8	2.59	2.07	388.96	269.44	190.53 (RMS)
2	193.2	0.9	1.79	1.61	345.71		
3	227.8	1.0	1.37	1.37	311.18		
4	256.1	1.1	1.10	1.22	282.93		

To avoid repetition, the simulated waveforms of pattern I under different operating conditions are selected to depict in Fig. 2.23, where V_{dc} indicates the voltage stress across the DC-link, V_{C1} indicates the Z-capacitor voltage, V_{ph} indicates the output phase voltage before the filter, and V_{ab} indicates the output line-to-line voltage after the filter. All the measured values of V_{dc} , V_{C1} and V_{ab} of the three patterns in different cases together with the errors are stated in Tables 2–10. It can be seen that, the simulation results have good agreement with the theoretical analysis. Besides, the THD values within double the switching frequency ($\leq 21000\text{Hz}$) are listed in the tables as well. It is seen that with the increase of the modulation index, the THD decreases rapidly. Thus, to achieve better performance of the output waveform with less distortion, the ZSI is better to operate with a high modulation index. However, the aforementioned problem of the classical ZSI is more obvious, the voltage boost ability is very limited with higher modulation index. Thus, to develop an advanced topology with enhanced boost ability is very necessary for the further application of the classical ZSI.

(a) Case 1: $M=0.8$ and $V_{in}=150.0\text{V}$

(b) Case 2: $M=0.9$ and $V_{in}=193.2\text{V}$

(c) Case 3: $M=1.0$ and $V_{in}=227.8V$

(d) Case 4: $M=1.1$ and $V_{in}=256.1V$

Figure 2.23. Simulation results of SVPWM-based constant boost control of ZSI

Table 2–10: Measured values of SVPWM-based constant boost of ZSI

Case No.	V_{dc} (V)	Error (%)	V_{Cl} (V)	Error (%)	V_{ab} (V) (RMS)	Error (%)	THD (%)	
							before filter	after filter
1	384.65	1.09	267.14	0.85	187.89	1.39	91.59	2.57
2	342.23	1.01	267.31	0.79	189.90	0.36	79.08	2.33
3	308.96	0.71	267.85	0.61	190.34	0.11	68.05	2.02
4	280.68	0.78	268.22	0.45	189.47	0.94	58.14	1.57

2.7.2 Experimental Verification

The SVPWM-based constant boost control scheme has also been tested on the laboratory setup for further validating. The main circuit components are selected as listed in Table 2-2. Also, the desired output phase voltage is reduced to 55V (RMS value) due to the laboratory limitation. Thus, the input source voltage and all the voltage stresses will reduce to half. The control scheme is utilized by employing a DSPACE ds1006 with composed C codes and the switching frequency is set to be 10kHz. The experimental waveforms in steady-state of the cases $M=0.8$, 0.9 and 1.0 are depicted in Figs. 2.24–2.26, which show a good agreement with the theoretical analysis and simulation results.

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.24. Experiment results of SVPWM-based maximum boost control with $M=0.8$ and $V_{in}=75V$

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.25. Experiment results of SVPWM-based maximum boost control with $M=0.9$ and $V_{in}=96.6V$

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 2.26. Experiment results of SVPWM-based maximum boost control with $M=1.0$ and $V_{in}=113.9V$

2.8 Conclusion

In this chapter, the theory of SVPWM technique for the three-phase ZSI has been derived and discussed in detail. By selecting different null states and shoot-through states, three switching patterns have been introduced and compared with the carrier-based strategy. Besides, novel implementation schemes of maximum boost control and constant boost control methods for three-phase ZSIs based on SVPWM theory have been presented. Compared with the carrier-based strategies, the proposed SVPWM solution has reduced the number of switching transition greatly. All the theoretical analysis has been verified by simulation and experimental results. The proposed control schemes will be helpful for enhancing the understanding of SVPWM technique and promoting the applications of three-phase ZSIs.

Chapter 3. Space Vector PWM of Single-Phase ZSI

This chapter has successfully extended SVPWM concepts to the single-phase ZSI. With the considerations on the circuit characteristics, the principles and implementation schemes of the SVPWM strategy of single-phase ZSI have been explained in detail. The effectiveness of the proposed control schemes has been verified by the simulation and experimental results. As with that of three-phase ZSI, the number of switching actions has been significantly reduced by using the SVPWM-based control schemes. The proposed SVPWM implementation schemes will be helpful for enhancing our understanding of the SVPWM technique and promoting the industrial applications of the single-phase ZSI.

3.1 Introduction

The single-phase full-bridge ZSI is also a promising topology that found many applications in industrial fields [78-83]. So far, two popular modulation methods for single-phase ZSI have been proposed, namely simple boost control [23] and modified PWM [39]. Both these two methods are carrier-based strategies, which are illustrated in Figs. 3.1 and 3.2. As shown in Fig. 3.1, the disadvantage of the simple boost control method is that, it has increased the number of switching transitions remarkably since it turns on the switches in the same phase leg to produce the shoot-through state purposely. Besides, conducting all the switches in the shoot-through state is unnecessary because the shoot-through stress can be allocated only in one particular leg each time. To avoid this, the modified PWM method employs two sinusoidal waveforms as modulation signals to generate switching signals for each leg, as shown in Fig. 3.2, which inserts the shoot-through signals without increasing the number of switching actions. It is noted that fewer switching actions yield less switching loss; therefore, it would be beneficial for the further industrial applications of the single phase ZSI if a proper modulation scheme with less switching actions were established.

This chapter aims to give an in-depth mathematical derivation of SVPWM for the single-phase full-bridge ZSI and explore optimal SVPWM implementation schemes with less switching actions. It starts by reviewing the circuit principles of single-phase ZSI. Then through in-depth mathematical derivation, the principles of SVPWM implementation schemes for the single-phase full-bridge ZSI are established. According to the selection of null vectors, three different switching patterns are introduced. In addition, the number of switching actions has been compared between these three SVPWM patterns and the two carrier-based modulation schemes. At last, all the three SVPWM patterns have been verified by both the simulation in MATLAB/SIMULINK software and experimental investigations.

3.2 Operating Principle of Single-Phase Full-Bridge ZSI

The typical topology of a single-phase full-bridge ZSI is illustrated in Fig. 3.3. As with the three-phase topology, it is able to be operated in either voltage buck or boost mode. The operating states can be classified into three groups, which can be represented by two equivalent circuits, as shown in Fig. 3.4 (a) and (b).

Figure 3.3 Prototype of the single-phase full-bridge ZSI

For the simplicity of steady-state analysis, all the inductors and capacitors are assumed to be ideal and symmetrical, so we have

$$\begin{cases} V_{C1} = V_{C2} = V_C \\ V_{L1} = V_{L2} = V_L \end{cases} \quad (3-1)$$

Figure 3.4 Equivalent circuits of the single-phase ZSI in different operating modes

During the shoot-through state time interval T_{sh} , the voltage after the diode is greater than the input DC voltage, therefore, the diode D is reverse-biased. The capacitors will charge the inductors. In another point of view, inductors are limiting the short-circuit current introduced by the shoot-through state. From Fig. 3.4 (a), one has

$$\begin{cases} v_L = V_C \\ v_d = V_C + v_L = 2V_C \\ V_{dc} = 0 \end{cases} \quad (3-2)$$

During the non-shoot-through state time interval T_n , the ZSI operates in any one of the two active states or two null states. In the active states, there is a current flow from the DC source to the AC load, and D is conducting. While in the null states, the load is short-circuited, hence the inverter input current is zero. The diode is still conducting and the capacitors are charging from the DC source. From the equivalent circuit Fig. 3.4 (b), the following equations can be obtained:

$$\begin{cases} v_L = V_{in} - V_C \\ v_d = V_{in} \\ v_{dc} = V_C - v_L = 2V_C - V_{in} \end{cases} \quad (3-3)$$

The average voltage of the inductors over one switching period ($T = T_{sh} + T_n$) should be zero in steady state, then

$$V_L = \bar{v}_L = \frac{T_{sh} \cdot V_C + T_n (V_{in} \cdot V_C)}{T} = 0 \quad (3-4)$$

Thus

$$V_C = \frac{T_n}{T_n - T_{sh}} V_{dc} \quad (3-5)$$

The peak voltage V_{dc} across the DC-link can be obtained from (3-3) and (3-5)

$$V_{dc} = \frac{T}{T_n - T_{sh}} V_{in} = B \cdot V_{in} \quad (3-6)$$

where

$$B = \frac{T}{T_n - T_{sh}} = \frac{1}{1 - 2T_{sh}/T} = \frac{1}{1 - 2D} \quad (3-7)$$

The output line-to-line peak voltage $\hat{V}_{ab}$ can be written as:

$$\hat{V}_{ab} = M \cdot V_{dc} = M \cdot B \cdot V_{in} \quad (3-8)$$

3.3 SVPWM Theory of Single-Phase ZSI

3.3.1 Establishment of New Coordinate Frame and Basic Space Vectors

From the analysis of SVPWM technique for three-phase ZSI, it is known that the key point of the SVPWM technique is to simplify the voltage vectors with an appropriate transformation matrix and find the basic space vectors in the new frame. In order to produce a set of voltage vectors, the output line voltages of the single-phase full-bridge ZSI can be expressed by the following equation:

$$\begin{bmatrix} V_{ab} \\ V_{ba} \end{bmatrix} = \sqrt{2} V_\varphi \begin{bmatrix} \sin \omega t \\ \sin(\omega t + \pi) \end{bmatrix} \quad (3-9)$$

where V_φ represents the RMS value of the output voltage.

Figure 3.5 Trajectory of line-to-line voltages of single-phase ZSI and configuration of single-phase space-vector frame

Each value of t would produce a defined set of single-phase output line-to-line voltage vectors $\vec{V}_S = [V_{ab} \ V_{ba}]^T$, which are demonstrated in Fig. 3.5. We can see that all the vectors lie on the α line where $x+y=0$. Therefore, we can select the α line and its normal line (β) as the axes of a new coordinate system. Then we can transform the two dimensional vectors $\vec{V}_S$ into one-dimensional ones because the projection of the vectors on the β axis will always be zero. In this case, the corresponding transformation matrix $T_{ab-\alpha\beta}$ can be given as follows:

$$T_{ab-\alpha\beta} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \quad (3-10)$$

Thus, the voltage vectors in the new system can be expressed by:

$$\vec{V}_S' = T_{ab-\alpha\beta} \cdot \vec{V}_S = \begin{bmatrix} V_\alpha \\ 0 \end{bmatrix} = 2V_\phi \begin{bmatrix} \sin\omega t \\ 0 \end{bmatrix} \quad (3-11)$$

The possible switching states of the single-phase full bridge ZSI are listed in Table 3–1. It is shown that there are nine basic space vectors, including two active vectors (V_1 and V_2), two null vectors (V_0 and V_3) and five shoot-through vectors (V_{sh1} , V_{sh2} , V_{sh3} , V_{sh4} and V_{sh5}). Hence, the voltage vectors can be written as:

$$\vec{V}_S = V_{dc} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} = B \cdot V_{in} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} \quad (3-12)$$

Table 3–1: Switching states and output voltages of single-phase full-bridge ZSI

states		S_a	$S_{a'}$	S_b	$S_{b'}$	V_{ab}	V_{ba}	V_a
Null	V_0	0	1	0	1	0	0	0
Active	V_1	0	1	1	0	$-BV_{in}$	BV_{in}	$-\sqrt{2}BV_{in}$
Active	V_2	1	0	0	1	BV_{in}	$-BV_{in}$	$\sqrt{2}BV_{in}$
Null	V_3	1	0	1	0	0	0	0
Shoot-through	V_{sh1}	1	1	0	1	0	0	0
Shoot-through	V_{sh2}	1	1	1	0	0	0	0
Shoot-through	V_{sh3}	1	0	1	1	0	0	0
Shoot-through	V_{sh4}	0	1	1	1	0	0	0
Shoot-through	V_{sh5}	1	1	1	1	0	0	0

And consequently, the basic space vectors in the new frame can be obtained using the following equation and mapped in Fig. 3.6.

$$\vec{V}_S' = T_{ab-\alpha\beta}^{-1} \cdot \vec{V}_S = \sqrt{2}B \cdot V_{in} \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} \quad (3-13)$$

Figure 3.6 Basic space vectors and sectors of single-phase ZSI

Based on the space vector concepts, the desired output voltage of a single-phase full bridge ZSI can be obtained by using the linear combinations of one active space vector and several null vectors and shoot-through vectors according to the following equation:

$$\vec{V}_{ref} = \frac{T_i}{T} (\vec{V}_1, \vec{V}_2) + \frac{T_0}{T} (\vec{V}_0, \vec{V}_3) + \frac{T_{sh}}{T} (\vec{V}_{sh1} \sim \vec{V}_{sh5}) \quad (3-14)$$

where T_i , T_z and T_{sh} represent the time durations of active state, null state and shoot-through state, respectively.

3.3.2 Selection of Shoot-through and Null Vectors

As demonstrated in Fig. 3.6, the selection of the active vectors depends on the phase angle θ ($\theta = \omega t$). When $0 \leq \theta \leq \pi$, V_2 is employed; otherwise V_1 is adopted.

All the possible transitions between different switching states of single-phase ZSI are demonstrated in Fig. 3.7, where each arrow indicates half switching action only. It can be seen that, a transition from active state V_2 to the adjacent shoot-through states V_{sh1} or V_{sh3} requires half switching action, while the transition from V_2 to either null state V_0 or V_3 requires one switching actions at least, respectively. The special shoot-through state, V_{sh5} can only get to any non-shoot-through state directly, so it would introduce additional switching actions if it is utilized in the control scheme. To minimize the switching actions, the shoot-through state between corresponding active state and null state should be selected.

Figure 3.7 Switching transition between different states of single-phase ZSI

Similar to the three-phase SVPWM technique, according to the selection of the null vector, three different switching patterns are introduced.

Pattern I adopts both null vectors V_0 and V_3 in one switching period, and T_z is distributed evenly into these two states; that is, $T_{00}=T_{03}=0.5T_z$. Pattern II adopts only one null vector V_0 , and T_z is entirely distributed into this state; that is, $T_{00}=T_z$, $T_{03}=0$. Pattern

III adopts only the other null vector V_3 , and T_z is entirely distributed into this state; that is, $T_{00}=T_z$, $T_{03}=0$. Taking sector I for example, the three patterns are depicted in Fig. 3.8 (a), (b) and (c), respectively.

Figure 3.8 Three switching patterns of single-phase ZSI

3.3.3 Determination of Time duration for Each Vector

A. Condition 1

If $0 \leq \theta \leq \pi$, one can obtain the following equation from Fig. 3.6.

$$T \cdot |\vec{V}_{ref}| = T_2 \cdot |\vec{V}_2| + T_z \cdot |\vec{V}_0, \vec{V}_3| + T_{sh} \cdot |\vec{V}_{sh1}, \vec{V}_{sh2}, \vec{V}_{sh3}, \vec{V}_{sh4}, \vec{V}_{sh5}| \quad (3-15)$$

then through (3-8), (3-9), and (3-11), one can get

$$|\vec{V}_{ref}| = 2V_\phi \cdot \sin\theta = \sqrt{2}B \cdot V_{in} \cdot M \quad (3-16)$$

also it is indicated in Table 3–1 that

$$\begin{cases} |V_2| = \sqrt{2}\hat{V}_{dc} = \sqrt{2}B \cdot V_{in} \\ |V_0| = |V_3| = |V_{sh1}| = |V_{sh2}| = |V_{sh3}| = |V_{sh4}| = |V_{sh5}| = 0 \end{cases} \quad (3-17)$$

substituting (3-16) and (3-17) into (3-15)

$$\Rightarrow \begin{cases} T_2 = T \cdot M \sin\theta \\ T_z + T_{sh} = T - T_2 \end{cases} \quad (3-18)$$

B. Condition 2

If $\pi \leq \theta \leq 2\pi$, the following equation is obtained from Fig. 3.6.

$$T \cdot |\vec{V}_{ref}| = T_1 \cdot |\vec{V}_1| + T_z \cdot |\vec{V}_0, \vec{V}_3| + T_{sh} \cdot |\vec{V}_{sh1}, \vec{V}_{sh2}, \vec{V}_{sh3}, \vec{V}_{sh4}, \vec{V}_{sh5}| \quad (3-19)$$

Referring to the derivation procedure of Condition 1, from (3-16) and (3-19), one has

$$\Rightarrow \begin{cases} T_1 = T \cdot M \sin(\theta - \pi) \\ T_z + T_{sh} = T - T_1 \end{cases} \quad (3-20)$$

According to (3-7) and (3-8), the shoot-through time duration can be figured out using the following equation once the operating conditions of input DC voltage V_{in} , modulation index M and output voltage V_{ab} are given.

$$T_{sh} = \frac{1}{2} - \frac{M \cdot V_{in}}{2\hat{V}_{ab}} \quad (3-21)$$

Then the time duration of null state can be obtained through (3-18), (3-20) and (3-21)

$$T_z = T - T_i - T_{sh} \quad (3-22)$$

3.3.4 Switching Signals of the SVPWM Patterns

Through the above analysis, we can obtain the implementation schemes and the on-off switching signals of SVPWM for single-phase ZSI as depicted in Figs.3.9 – 3.11.

(a) Sector 1 ($0 \leq \theta \leq \pi$)

(b) Sector 2 ($\pi \leq \theta \leq 2\pi$)

Figure 3.9 SVPWM control switching pattern I for single-phase ZSI

(a) Sector 1 ($0 \leq \theta \leq \pi$)

(b) Sector 2 ($\pi \leq \theta \leq 2\pi$)

Figure 3.10 SVPWM control switching pattern II for single-phase ZSI

(a) Sector 1 ($0 \leq \theta \leq \pi$)

(b) Sector 2 ($\pi \leq \theta \leq 2\pi$)

Figure 3.11 SVPWM control switching pattern III for single-phase ZSI

3.3.5 Comparison of Switching Actions

It is noted that fewer switching actions lead to less switching loss; thus we'll study on the switching actions of all the switches in one sampling period with different modulation methods. As shown in Fig. 3.1, to produce the shoot-through state, the simple boost strategy purposely turns on all the four switches simultaneously (i.e. shoot-through state V_{sh5}) to produce the shoot-through states. Consequently, the number of each switching action will be increased one per sampling interval. Fortunately, for the modified PWM strategy, the number of switching action would not be increased since the shoot-through states are appropriately produced. It is clearly depicted in Fig. 3.9 that, for SVPWM control pattern I, each switch would turn on and off once in each switching period. And Figs. 3.10 and 3.11 indicate that the switching actions are reduced because two switches will keep the switching status unchanged during one switching period. All

the specified numbers of switching actions for different control schemes are listed in Table 3–2 and the comparison of the numbers is depicted in Fig. 3.12.

Table 3–2: Numbers of switching actions with different modulation methods

<i>Condition</i>	<i>Simple boost</i>					<i>Modified PWM</i>				
	S_a	S_a'	S_b	S_b'	Total	S_a	S_a'	S_b	S_b'	Total
$0 \leq \theta \leq \pi$	2	2	2	2	8	1	1	1	1	4
$\pi \leq \theta \leq 2\pi$	2	2	2	2	8	1	1	1	1	4

<i>Condition</i>	<i>SVPWM</i>														
	<i>Pattern I</i>					<i>Pattern II</i>					<i>Pattern III</i>				
	S_a	S_a'	S_b	S_b'	total	S_a	S_a'	S_b	S_b'	total	S_a	S_a'	S_b	S_b'	total
$0 \leq \theta \leq \pi$	1	1	1	1	4	1	1	0	0	2	0	0	1	1	2
$\pi \leq \theta \leq 2\pi$	1	1	1	1	4	0	0	1	1	2	1	1	0	0	2

Figure 3.12. Comparison of switching actions of different control schemes for single-phase ZSI

Generally, the figure indicates that compared with the simple boost strategy, a 50% switching action reduction can be achieved by using modified PWM method or SVPWM pattern I, while the reduction can reach 75% if the SVPWM pattern II or III is employed.

3.4 Simulation and Experimental Verification

3.4.1 Simulation Verification

To verify the aforementioned theoretical analysis, all the three switching patterns of SVPWM technique for the single-phase ZSI have been verified in Matlab/Simulink software. The main circuit parameters for simulation are selected as follows:

Table 3–3: Parameters used for simulation of single-phase ZSI

<i>Parameters</i>	<i>Values</i>
V_{in}	60V
L	300 μ H
C	360 μ F
L_f	2mH
C_f	15 μ F
R	25 Ω
f_s	10kHz
M	0.8
D	0.2

By using (3-4) – (3-7), the theoretical values are figured out and list in Table 3–4.

Table 3–4: Theoretical values of SVPWM-based single-phase ZSI

<i>Conditions</i>			<i>Theoretical Values</i>				
V_{in} (V)	M	D	B	G	V_{dc} (V)	V_C (V)	$\hat{V}_{ab}$ (V)
60	0.8	0.2	1.67	1.33	100	80	80

All the simulation results of three patterns are depicted in Figs. 3.13, 3.14 and 3.15, where S_{ap} , S_{an} , S_{bp} , S_{bn} , indicate the upper and lower switch actions of phase a and phase b , and V_{dc} , V_c , V_{pn} , V_{ab} indicate the voltage stresses of the dc-link, Z-network capacitor, output phase before the filter and line voltage after the filter, respectively. To clearly demonstrate the number of switching actions of each switch, the enlarged waveforms of switching actions in one switching cycle for three patterns are depicted in Fig. 3.13(c),

Fig. 3.14(c) and Fig. 3.15(c). The switching actions of all switches are in accordance with the theoretical results shown in Figs. 3.9–3.11 and the number of switching actions is the same as shown in Table 3-2. The voltage stresses of all three patterns are depicted in Fig. 3.13(d), Fig. 3.14(d) and Fig. 3.15(d), which support the theoretical results shown in Table 3-4. In addition, to investigate the effects of switching numbers on the THD values, harmonic spectrums of the output voltage using all three patterns are given in Fig. 3.16. It is shown in Fig. 3.16 that the distinct harmonic distortion of the output voltage of pattern I starts around 20KHz, which is twice as much as the switching frequency; while that of the pattern II and pattern III start around 10KHz, which is as much as the switching frequency. Hence the pattern II and pattern III contain more THD compared with pattern I.

Figure 3.13 Simulation results of SVPWM pattern I: (a) switching actions of phase a; (b) switching actions of phase b; (c) switching actions of 4 switches in one switching cycle; (d) voltage stresses in steady state.

Figure 3.14 Simulation results of SVPWM pattern II: (a) switching actions of phase a; (b) switching actions of phase b; (c) switching actions of 4 switches in one switching cycle; (d) voltage stresses in steady state.

Figure 3.15 Simulation results of SVPWM pattern III: (a) switching actions of phase a; (b) switching actions of phase b; (c) switching actions of 4 switches in one switching cycle; (d) voltage stresses in steady state.

(a) pattern I

(b) pattern II

(c) pattern III

Figure 3.16 Harmonic spectrums of output voltages of three patterns

3.4.2 Experimental Verification

The proposed schemes have also been tested on the laboratory setup for further validating. The main circuit components are selected as listed in Table 2-5. The control scheme is utilized by employing a DSPACE ds1006 with composed C codes and the switching frequency is set to be 10kHz. The experimental waveforms of switching actions of all switches for three patterns together with the enlarged waveforms in two switching cycles and voltage stresses in steady state are depicted in Figs. 3.17-3.19,

respectively. The experiment results show a good agreement with the theoretical analysis and simulation results.

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(f) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 3.17 Experiment results of SVPWM pattern I: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b in two switching cycles; (e) V_c and V_{dc} ; (f) V_{pn} and V_{ab}

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(f) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 3.18 Experiment results of SVPWM pattern II: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b in two switching cycles; (e) V_c and V_{dc} ; (f) V_{pn} and V_{ab}

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(f) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 3.19 Experiment results of SVPWM pattern III: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b in two switching cycles; (e) V_c and V_{dc} ; (f) V_{pn} and V_{ab}

3.5 Conclusion

This chapter has successfully extended SVPWM concepts to the single-phase full-bridge ZSI. With the considerations on the circuit characteristics, the principles and implementation schemes of the SVPWM strategy of single-phase ZSI have been explained in detail. By selecting different null state and shoot-through state, three switching patterns have been discussed and compared with carrier-based strategies. The effectiveness of the proposed switching patterns has been verified by simulation and experimental results. The proposed SVPWM implementation schemes will be helpful for enhancing our understanding on the SVPWM technique and promoting the applications of the single-phase full-bridge ZSI.

Chapter 4. Dynamic Modeling and Analysis of Improved ZSI

Developed from the classical ZSI, the improved ZSI has successfully reduced the Z-capacitor voltage stresses and suppressed the inrush current of classical ZSI. To enhance the understanding of the dynamic system and detailed analysis of the improved ZSI, the dynamic mathematical models of improved ZSI have been studied in this chapter. By employing the state space averaging method, small-signal models have been well established and related transfer functions have been derived through mathematical analyses. To predict the RHP zeros of the transfer functions, a group of root loci Plots are illustrated. The study of this chapter is helpful for enhancing the understanding of the dynamics of the Z-source topology and developing new topologies based on classical ZSI.

4.1 Introduction

As mentioned in the literature review, the improved ZSI has successfully reduced the Z-capacitor voltage stresses and suppressed the inrush current and the resonance at startup which causes a voltage and current surge that may destroy the devices [37]. The typical prototype of the improved ZSI has been depicted in Fig. 4.1 [37]. It shows that the improved ZSI has exactly the same components as the classical ZSI, whereas the impedance network is moved to the end of the inverter bridges. With this slight modification, the developed topology has achieved the aforementioned improvements.

Figure 4.1 Prototype of the improved ZSI

To analyze the dynamics of this developed topology in detail, the AC small signal modeling of the improved ZSI has been studied in this chapter. By employing the state-space averaging method, small signal models of the improved ZSI have been well

established and relative transfer functions have been obtained after mathematical analysis. Computer simulations are offered to verify the validity of the proposed modeling. To predict the existence of the RHP zeros, which would limit the dynamic response of the system, the movements of the poles and zeros with various values for a specified component has been analyzed in detail. At last, simulation results are presented for verifying the dynamic response.

4.2 State Space Averaging of Improved ZSI

In this section, the voltage type improved ZSI is analyzed. For ease of illustration and analysis, the studied topology is simplified as in Fig. 4.2, where the diode and the inverter bridge are represented by two ideal switches S_1 and S_2 . A resistor and inductor connected in series is considered here as the load. To simplify the analysis, the following assumptions are made:

- 1) The improved ZSI operates in continuous conduction mode (CCM).
- 2) All passive elements in X-shape network are lossless and symmetric, i.e. $C_1 = C_2 = C$ and $L_1 = L_2 = L$.
- 3) All switches and diode are ideal (i.e. R_{on} and V_d are negligible).

Figure 4.2 Simplified equivalent circuit of the improved ZSI

As with the classical ZSI, the improved ZSI has three operation modes: shoot-through state, active state and null state. The equivalent circuits of the three operating states are depicted in Fig. 4.3 (a) and (b), respectively, where the active state and null state are represented by the same equivalent circuit as in Fig. 4.3 (b).

Define the voltages of Z-capacitors and currents of Z-inductors and load inductor as state variables.

$$x(t) = [i_{L1}(t) \ i_{L2}(t) \ v_{C1}(t) \ v_{C2}(t) \ i_l(t)]^T \quad (4-1)$$

Figure 4.3 Equivalent circuits of the improved ZSI in different operation states

During the shoot-through state, the switch S_1 is turned on, which yields a reverse-biasing of the diode and a short circuiting of the inductive load. According to the equivalent circuit depicted in Fig. 4.3 (a), the state-space form of the differential equations in shoot-through state can be expressed as:

$$\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R_l \end{bmatrix} \cdot \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot v_{in} \quad (4-2)$$

which is always recorded as $K \cdot \dot{x} = A_1 \cdot x + B_1 \cdot u$

where

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_l \end{bmatrix} \quad A_1 = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R_l \end{bmatrix} \quad B_1 = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Alternatively, during the non-shoot-through state, the switch S_1 is turned off, allowing the phase-legs to perform in active states or null state, and the diode is forward-biased, which means the switch S_2 is closed. According to the equivalent circuit shown in Fig. 4.3 (b), the state space form of the differential equations in non-shoot-through state thus can be written as:

$$\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 1 & -R_l \end{bmatrix} \cdot \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} \cdot v_{in} \quad (4-3)$$

that is $K \cdot \dot{x} = A_2 \cdot x + B_2 \cdot u$,

where

$$A_2 = \begin{bmatrix} 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 1 & 1 & -R_l \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}$$

The duty ratio of S_1 is defined as d and that of S_2 is d' . Then an average model for the improved ZSI can then be deduced by performing state-space averaging equations (4-2) and (4-3) as follows:

$$K \cdot \dot{x} = (A_1 d + A_2 d') \cdot x + (B_1 d + B_2 d') \cdot u \quad (4-4)$$

that is

$$\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -d' & 0 & 0 \\ 0 & 0 & d & -d' & 0 \\ -d & d' & 0 & 0 & -d' \\ d' & -d & 0 & 0 & -d' \\ 0 & 0 & d' & d' & -R_l \end{bmatrix} \cdot \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} d \\ d \\ 0 \\ 0 \\ d' \end{bmatrix} \cdot v_{in} \quad (4-5)$$

The steady state equations at the operation point can be shown as:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -D' & 0 & 0 \\ 0 & 0 & D & -D' & 0 \\ -D & D' & 0 & 0 & -D' \\ D' & -D & 0 & 0 & -D' \\ 0 & 0 & D' & D' & -R_l \end{bmatrix} \cdot \begin{bmatrix} I_{L_1} \\ I_{L_2} \\ V_{C1} \\ V_{C2} \\ I_l \end{bmatrix} + \begin{bmatrix} D \\ D \\ 0 \\ 0 \\ D' \end{bmatrix} \cdot V_{in} \quad (4-6)$$

Thus, the steady state Z-capacitor voltages, load inductor current and Z-inductor currents can be obtained from equation (4-6) as follows:

$$V_c = \frac{D}{1-2D} \cdot V_{in} \quad (4-7)$$

$$I_l = \frac{1-D}{1-2D} \cdot \frac{V_{in}}{R_l} \quad (4-8)$$

$$I_L = \frac{1-D}{1-2D} \cdot I_l = \frac{(1-D)^2}{(1-2D)^2} \cdot \frac{V_{in}}{R_l} \quad (4-9)$$

These steady-state values perfectly match the results of the theoretical analysis as expressed in [37] where the improved ZSI has been firstly proposed.

Recalling that the Z-capacitor voltage of the classical ZSI is expressed as

$$V_c = \frac{1-D}{1-2D} \cdot V_{in} \quad (4-10)$$

It is noted that the shoot-through duty ratio D should be less than 0.5, thus

$$\frac{1-D}{1-2D} \cdot V_{in} > \frac{D}{1-2D} \cdot V_{in} \quad (4-11)$$

Equation (4-11) proves that the Z-capacitor voltage of improved ZSI is smaller than that of the classical ZSI.

4.3 Derivation of Small-Signal Model and Transfer Functions

To derive the small-signal models, small time-varying perturbations are applied to the input voltage and the shoot-through duty cycle of S_1 described by $v_{in}(t) = V_{in} + \hat{v}_{in}(t)$ and $d(t) = D + \hat{d}(t)$. The perturbations lead to small signal variations in the state variables,

$x(t) = X(t) + \hat{x}(t)$. Substituting these perturbations into (4-4), we get the perturbed state equations as follows,

$$\begin{aligned}\dot{x} + \hat{x} &= \left[A_1(D + \hat{d}) + A_2(1 - D - \hat{d}) \right] \cdot (X + \hat{x}) + \left[B_1(D + \hat{d}) + B_2(1 - D - \hat{d}) \right] \cdot (V_{in} + \hat{v}_{in}) \\ &= [A_1D + A_2(1 - D)] \cdot X + [B_1D + B_2(1 - D)] \cdot V_{in} + [A_1D + A_2(1 - D)] \cdot \hat{x} + \\ &\quad [B_1D + B_2(1 - D)] \cdot \hat{v}_{in} + (A_1X - A_2X + B_1V_{in} - B_2V_{in}) \cdot \hat{d}\end{aligned}\quad (4-12)$$

then

$$\hat{\dot{x}} = [A_1D + A_2(1 - D)] \cdot \hat{x} + [B_1D + B_2(1 - D)] \cdot \hat{v}_{in} + (A_1X - A_2X + B_1V_{in} - B_2V_{in}) \cdot \hat{d} \quad (4-13)$$

Using Laplace transformation, (4-13) becomes

$$\begin{bmatrix} sL_1\hat{i}_{L1}(s) \\ sL_2\hat{i}_{L2}(s) \\ sC_1\hat{v}_{C1}(s) \\ sC_2\hat{v}_{C2}(s) \\ sL_l\hat{i}_l(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -D' & D & 0 \\ 0 & 0 & D & -D' & 0 \\ -D & D' & 0 & 0 & -D' \\ D' & -D & 0 & 0 & -D' \\ 0 & 0 & D' & D' & -R_l \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C1}(s) \\ \hat{v}_{C2}(s) \\ \hat{i}_l(s) \end{bmatrix} + \begin{bmatrix} D \\ D \\ 0 \\ 0 \\ D' \end{bmatrix} \hat{v}_{in}(s) + \begin{bmatrix} V_{C1} + V_{C2} + V_{in} \\ V_{C1} + V_{C2} + V_{in} \\ -I_{L1} - I_{L2} + I_l \\ -I_{L1} - I_{L2} + I_l \\ -V_{C1} - V_{C2} - V_{in} \end{bmatrix} \hat{d}(s) \quad (4-14)$$

Recalling the assumptions (1) and (2)

$$\begin{cases} D + D' = 1 \\ L_1 = L_2 = L \\ C_1 = C_2 = C \end{cases} \quad (4-15)$$

Hence, from (4-14) and (4-15), one can obtain

$$sC(\hat{v}_{C1}(s) - \hat{v}_{C2}(s)) = -(\hat{i}_{L1}(s) - \hat{i}_{L2}(s)) \quad (4-16)$$

$$sL(\hat{i}_{L1}(s) - \hat{i}_{L2}(s)) = \hat{v}_{C1}(s) - \hat{v}_{C2}(s) \quad (4-17)$$

Combining (4-16) and (4-17)

$$(LCs^2 + 1) \cdot (\hat{i}_{L1}(s) - \hat{i}_{L2}(s)) = 0 \quad (4-18)$$

When $LCs^2 + 1 \neq 0$, i.e., $\omega \neq \sqrt{1/LC}$, then

$$\hat{i}_{L1}(s) = \hat{i}_{L2}(s) = \hat{i}_L(s) \quad (4-19)$$

Substituting (4-19) into (4-18), the following equation is obtained

$$\hat{v}_{C1}(s) = \hat{v}_{C2}(s) = \hat{v}_C(s) \quad (4-20)$$

Then substituting (4-19) and (4-20) into (4-14), the equations can be reduced as follows

$$\begin{cases} sL \cdot \hat{i}_L(s) = (2D-1) \cdot \hat{v}_C(s) + D \cdot \hat{v}_{in}(s) + (2V_C + V_{in}) \cdot \hat{d}(s) \\ sC \cdot \hat{v}_C(s) = (1-2D) \cdot \hat{i}_L(s) - (1-D) \cdot \hat{i}_l(s) - (2I_L + I_l) \cdot \hat{d}(s) \\ sL_l \cdot \hat{i}_l(s) = 2(1-D) \cdot \hat{v}_C(s) - R_l \cdot \hat{i}_l(s) + (1-D) \cdot \hat{v}_{in}(s) - (2V_C + V_{in}) \cdot \hat{d}(s) \end{cases} \quad (4-21)$$

According to the equations of (4-21), the equivalent circuits of the AC small-signal models of improved ZSI are depicted in Fig. 4.4. The circuit variables of Fig. 4.4 (a) (b) and (c) are the small signals of Z-inductor current, load inductor current and Z-capacitor, respectively. Thus, these figures represent the small signal model equation described in (4-21). In these figures, all the terms that contain any of the small signal variables $\hat{i}_L$, $\hat{i}_l$ or $\hat{v}_C$ are considered as dependent sources because they are determined by other voltages or currents. On the other side, the terms that contain the small signal variable $\hat{d}$ are regarded as independent sources since they are determined by the variation of the shoot-through duty ratio only.

(a)

(b)

(c)

Figure 4.4 Equivalent circuits of the small-signal models of improved ZSI

It is indicated in [84] that the response of one state variable to several small signal perturbations can be regarded as the linear combination of the variable response to every individual perturbation. Hence, according to the equivalent circuits shown in Fig. 4.4, the small signal relationship for the Z-capacitor voltage and Z-inductor current can be written as follows

$$\begin{cases} \hat{v}_c(s) = G_{vc-vin}(s) \cdot \hat{v}_{in}(s) + G_{vc-d}(s) \cdot \hat{d}(s) \\ \hat{i}_L(s) = G_{iL-vin}(s) \cdot \hat{v}_{in}(s) + G_{iL-d}(s) \cdot \hat{d}(s) \end{cases} \quad (4-22)$$

where $G_{vc-vin}(s)$ denotes the transfer function of Z-capacitor voltage to input voltage, $G_{vc-d}(s)$ denotes the transfer function of Z-capacitor voltage to shoot-through duty ratio, $G_{iL-vin}(s)$ denotes the transfer function of Z-inductor current to input voltage, and

$G_{iL-d}(s)$ denotes the transfer function of Z-inductor current to shoot-through duty ratio. All these transfer functions can be derived from (4-21) and the results are shown in the following equations

$$G_{vc-in}(s) = \left. \frac{\hat{v}_C(s)}{\hat{v}_{in}(s)} \right|_{\hat{d}(s)=0} = \frac{[D(1-2D)L_l - (1-D)^2 L]s + D(1-2D)R_l}{LCL_l s^3 + LCR_l s^2 + [(1-2D)^2 L_l + 2(1-D)^2 L]s + (1-2D)^2 R_l} \quad (4-23)$$

$$G_{vc-d}(s) = \left. \frac{\hat{v}_C(s)}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{\begin{Bmatrix} -LL_l(2I_L - I_l)s^2 + [(1-2D)L_l(2V_C + V_{in}) + (1-D)L(2V_C + V_{in})] \\ -LR_l(2I_L - I_l)s + (1-2D)R_l(2V_C + V_{in}) \end{Bmatrix}}{LCL_l s^3 + LCR_l s^2 + [(1-2D)^2 L_l + 2(1-D)^2 L]s + (1-2D)^2 R_l} \quad (4-24)$$

$$G_{iL-in}(s) = \left. \frac{\hat{i}_L(s)}{\hat{v}_{in}(s)} \right|_{\hat{d}(s)=0} = \frac{DCL_l s^2 + (1-D)CR_l s + (1-D)^2}{LCL_l s^3 + LCR_l s^2 + [(1-2D)^2 L_l + 2(1-D)^2 L]s + (1-2D)^2 R_l} \quad (4-25)$$

$$G_{iL-d}(s) = \left. \frac{\hat{i}_L(s)}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{\begin{Bmatrix} CL_l(2V_C + V_{in})s^2 + [CR_l(2V_C + V_{in}) - (2D-1)L_l(2I_L - I_l)]s \\ + (1-D)(2V_C + V_{in}) - (2D-1)R_l(2I_L - I_l) \end{Bmatrix}}{LCL_l s^3 + LCR_l s^2 + [(1-2D)^2 L_l + 2(1-D)^2 L]s + (1-2D)^2 R_l} \quad (4-26)$$

4.4 Simulation Verification and Root Locus Analysis

In order to validate the effectiveness of the derived small-signal model, both the simplified average model and the detailed model are tested by using PSIM software. System parameters used for simulations are given in Table 4–1.

Table 4–1: Parameters used for simulation of improved ZSI

<i>Parameters</i>	<i>Values</i>
V_{in}	100V
L	2mH
C	800 μ F
L_l	2mH
R_l	10 Ω
D	0.3

The simulation results of the Z-capacitor voltage of improved ZSI using both models are illustrated in Fig. 4.5. A step change of shoot-through duty ratio from 0 to 0.3 is introduced to both the detailed circuit model (Fig. 4.5 top) and simplified equivalent model (Fig. 4.5 middle). To compare these two methods, an enlarged waveform is depicted at the bottom of Fig. 4.5. As shown in these figures, the steady state Z-capacitor voltages of both models are 75V, which perfectly matches the expected value using equation (4-10).

Figure 4.5. Simulation results of Z-capacitor voltage of improved ZSI

It is noted that one of the notable advantages of small-signal models is to predict RHP zeros of the transfer functions. Hence, further study on the transfer functions should be conducted. Taking the transfer function (4-24) for example, the numerator is a quadratic equation. As we know, for a quadratic equation $ax^2 + bx + c = 0$, there will be two different poles x_1 and x_2 if the condition $b^2 - 4ac > 0$ is fulfilled. In addition, we can obtain that $x_1 x_2 = c/a$ according to Lagrange resolvents. With respect to this case, substituting (4-7) – (4-9) into (4-24), the coefficients a and c can be expressed as:

$$\begin{cases} a = -LL_l(2I_L - I_l) = -\frac{(1-D)LL_l}{(1-2D)^2} \cdot \frac{V_{in}}{R_l} \\ c = (1-2D)(2V_C + V_{in})R_l = V_{in} \cdot R_l \end{cases} \quad (4-27)$$

Apparently, we can have the conclusion that $a < 0$, $c > 0$ and $c/a < 0$; therefore, we obtain that this transfer function has two zeros: one is negative and the other is a positive one, which is called RHP zero. It is noted that the tradeoff exists between performance of the closed-loop system and zero placement of the open-loop architecture. Besides, the tradeoff would become rigorous when the RHP zeros are near the original point. Recalling that the ZSI used commonly for renewable energies like solar panels and fuel-cells that have low voltage sources and require wider operation ranges, it is very important to investigate the movements of zeros and poles for the system to keep stable and achieve good performances.

Figure 4.6. Pole-zero locus of transfer function of improved ZSI with the increase of C

Table 4–2: Zero movements with the increase of C

C	200 μF	400 μF	600 μF	800 μF	1000 μF
Z_p	25.4492	25.4492	25.4492	25.4492	25.4492
Z_n	-25.6614	-25.6614	-25.6614	-25.6614	-25.6614

Towards this end, a series of root-locus plots are depicted in Fig. 4.6, 4.7 and 4.8 by changing a specified parameter while keeping others as constant. Since the movements of the zeros are not noticeable, the values of zeros in different conditions are listed in the following tables, where Z_p and Z_n represent the positive and negative zeros, respectively.

In detail, it is indicated in Fig. 4.6 and Table 4–2 that the variations of C (from 200 μF to 1000 μF) have little influences on the RHP zeros. Additionally, with the increase of C , the conjugated complex poles move towards the original point gradually, which would yield a smaller damping factor and a slightly lower natural frequency.

Figure 4.7. Pole-zero locus of transfer function of improved ZSI with the increase of L

Table 4–3: Zero movements with the increase of L

L	1mH	2mH	3mH	4mH	5mH
Z_p	36.0995	25.4492	20.7381	17.9319	16.0178
Z_n	-36.1812	-25.6614	-20.9939	-28.2095	-16.3084

It is observed from Fig. 4.7 that the increase in L (from 1mH to 5mH) will generally push the RHP zeros to the original point, which would aggravate the NMP effect. As mentioned above, the trade-off between performance of the closed-loop system and zero placement of the open-loop architecture would become rigorous when the RHP zeros are near the original point [85], which means that the RHP zeros should be made far from the original point to achieve good closed-loop performance. Hence, it is very important to select appropriate capacitance and inductance values to obtain a satisfying compromise between NMP effect and oscillatory response.

Figure 4.8. Pole-zero locus of transfer function of improved ZSI with the increase of D

Table 4–4: Zero movements with the increase of D

D	0.1	0.2	0.3	0.4
Z_p	56.4459	41.0979	25.4492	10.4194
Z_n	-55.9916	-41.0604	-25.6614	-10.6639

Fig. 4.8 shows how the shoot-through duty ratio variations (from 0.1 to 0.4) would influence the Z-capacitor voltage of the improved ZSI. The root-locus plot indicates that with the increase of D , the RHP zeros would move towards the original point; thus, the attainable closed-loop performances are degraded. Additionally, with the increase of D ,

the dominant conjugate poles are found to move close to the real axis, which would aggravate the damping effects.

4.5 Experimental Verification

To illustrate the presence of a right hand plane zero as predicted theoretically in (4-24, Fig. 4.9 shows the transient response of voltage stress of Z-capacitor during a step change in shoot-through duty ratio from 0.25 to 0.3 at $t=100\text{ms}$. The parameters of the main circuit are chosen as listed in Table 4-1. This figure indicates that the capacitor voltage decreases initially before rising to its new steady-state value, according with the non-minimum-phase characteristic for right hand plane zero.

Figure 4.9. Variations of V_C during a step change in D from 0.25 to 0.3 at $t=100\text{ms}$

4.6 Conclusion

This chapter has studied the dynamics of the improved ZSI based on small-signal modeling. By employing the state space averaging method, small-signal models have been well established and related transfer functions have been derived through mathematical analyses. Simulations are offered to verify the validity of the proposed modeling. To predict the RHP zeros of the transfer functions, a group of root loci Plots are illustrated. These figures indicate the presence of RHP zeros, which would result in NMP effect that would diminish the robustness of the system. The study of this chapter is helpful for enhancing the understanding of the dynamics of the ZSI and developing new topologies based on classical ZSI.

Chapter 5. Switched-Inductor ZSI

In this chapter, based on the study of dynamics of the Z-source impedance network, a new switched-inductor (SL) ZSI has been presented. The proposed inverter employs a SL Z-source impedance network to couple the low DC voltage energy source to the main circuit of the inverter. By an in-depth topology analysis, it is known that the proposed inverter can provide a strong boost inversion ability to overcome the limitations of the classical ZSI. Both the simulation and experimental results demonstrate its advantages in the topology and boost inversion ability. The concepts of SL Z-source impedance network will be beneficial for the applications of the impedance-type power converters.

5.1 Introduction

As discussed in the Chapter 1, many developed topologies have been presented to solve some drawbacks of the classical ZSI. However, the related research work on its boost inversion ability has seldom been reported in the open literatures. It is known that the ZSI was primarily promoted for renewable energy sources due to its wide operating range feature. Among these sources, fuel cells, batteries and PV systems usually require strong boost inversion abilities for industrial uses because their DC voltages are very low. In order to provide a very high boost factor for these low voltage sources, usually a large value of D needs to be taken, i.e., the classical ZSI would have to be operated under the extreme condition of a long interval of the shoot-through state. And consequently, the modulation index of the inverter side, M will be decreased to a very low level.

According to the harmonic spectral of traditional VSIs, the condition of low M will result in poor boost inversion ability with high THD value, and consequently, the final AC output performance will be degraded significantly. For an optimum system design, the practical values of D have an upper limit, so the practical boost factor of Z-source impedance network is restricted seriously according to (1-7). This disadvantage should be solved to avoid limiting its further applications.

It is learned from the previous chapter that the boost conversion ability of the ZSI comes from its impedance network and all the developed topologies have achieved

improvements by modifying the positions and connections of the elements of impedance network. And consequently, the mission to improve the boost ability is focused on the modification of impedance network as well.

In recent years, advanced DC/DC conversion enhancement techniques such as switched-capacitor (SC), switched-inductor (SL), hybrid SC/SL, voltage multiplier cells and voltage-lift (VL) techniques, have been greatly explored [86-94], which are used to get the high step-up capacity in transformerless and cascade structures. The main objective is to reach a high efficiency, high power density and simple structures. Therefore, the combination with the ZSI and advanced DC/DC enhancement techniques could be a good solution for improving impedance-type inverters' performance and promoting their further industrial applications. Fig. 5.1 depicts three basic step-up switching structures, though through analysis, the SL cell shown in Fig. 5.1 (c) is the only suitable structure for utilizing here to fulfill the above requirement.

Figure 5.1 Basic step-up switching structures

In this chapter, the concept of the SL techniques has been integrated into the classical Z-source impedance network, and consequently a new SL Z-source impedance network is proposed. With the modification, the proposed inverter can provide a strong boost inversion ability to overcome the limitations of the classical ZSI. The main characteristics are summarized as follows:

- The basic X-shape structure is retained.
- As for the high power quality and high boost inversion ability, their conflict caused by M and D has got an initial solution.
- Only six diodes and two inductors are added compared with the classical ZSI.
- The boost factor has been increased from $1/(1-2D)$ to $(1+D)/(1-3D)$.

- The new structure is extensible for the further development using the coupled-inductor techniques.

In the following sections, a detailed topology and operating analysis will be performed and the voltage boost abilities between SL ZSI and classical ZSI under different modulation methods have been compared and discussed. At last, the theoretical analysis has been verified by simulation and experimental investigations.

For the convenience of a general description, each component is ideal and the output power is equal to the input power (i.e. $V_o * I_o = V_{in} * I_{in}$). All reference directions of currents and voltages can be referred to in the corresponding figures. For any component X , its instantaneous current and voltage are expressed as i_X and v_X . Its average current and voltage during a switching cycle in the steady state are expressed as I_X and V_X . The corresponding peak value is represented by the small letter with a tilde symbol.

5.2 Topology Analysis of SL ZSI

The newly-proposed topology is termed the SL ZSI and shown in Fig. 5.2. This topology is totally different from any other existing ZSIs from the viewpoint of circuit structures and operating principles. As illustrated in Fig. 5.2, the proposed SL ZSI consists of four inductors (L_1, L_2, L_3 and L_4), two capacitors (C_1 and C_2), and six diodes (D_1, D_2, D_3, D_4, D_5 and D_6). The combination of L_1 - L_3 - D_1 - D_2 - D_3 and the combination of L_2 - L_4 - D_4 - D_5 - D_6 perform the function of the top SL cell and the bottom SL cell, respectively. Both of these two SL cells are used to store and transfer energies from the capacitors to the DC bus under the switching action of the main circuit.

Figure 5.2 Topology of the proposed SL ZSI

5.2.1 Operating Principle

From the viewpoint of the switching states of the main circuit connected with SL impedance network, the operating principles of the proposed impedance network are similar to those of the classical ZSI. For the convenience of analysis, the equivalent circuit of the proposed impedance network viewed from the DC bus is shown in Fig. 5.3, in which a virtual active switch S and a passive switch D_0 are introduced to simulate the practical shoot-through actions of the top and bottom arms. Therefore, the sub-states of the proposed impedance network are classified into the shoot-through state and the non-shoot-through state, respectively. The main circuit is simplified into a current source according to its characteristics. For the convenience of mathematical derivation, all inductors and capacitors are assumed to have the same inductance (L) and capacitance (C), respectively, so both the equivalent circuits in Fig. 5.4 show the symmetry characteristics. In addition, since C_1 and C_2 are sufficiently large, thus, in the steady state, we have $V_{C1}=V_{C2}=V_C$ and $V_{L1}=V_{L2}=V_{L3}=V_{L4}=V_L$.

Figure 5.3 Simplified circuit of the SL ZSI viewed from the DC link bus

During the shoot-through state, S is on, while both D_{in} and D_o are off. For the top SL cell, D_1 and D_2 are on, and D_3 is off. L_1 and L_3 are charged by C_1 in parallel. For the bottom SL cell, D_4 and D_5 are on, and D_6 is off. L_2 and L_4 are charged by C_2 in parallel. This state corresponds to the additional zero state produced by the shoot-through actions of the top and bottom arms, and its equivalent circuit is shown in Fig. 5.4 (a). It is seen that both the top and bottom SL cells perform the same function to absorb the energy stored in the capacitors.

Figure 5.4 Equivalent circuits of the SL ZSI in different operating states

Alternatively, during this sub-state, as shown in Fig. 5.4 (b), S is off, while both D_{in} and D_o are on. For the top SL cell, D_1 and D_3 are off, and D_5 is on. L_1 and L_2 are connected in series, and the stored energy is transferred to the main circuit. For the bottom SL cell, D_4 and D_5 are off, and D_6 is on. L_3 and L_4 are connected in series, and the stored energy is transferred to the main circuit. At the same moment, to supplement the consumed energy of C_1 and C_2 during the shoot-through state, C_1 is charged by V_{in} via the bottom SL cell, and C_2 is charged by V_{in} via the top SL cell.

5.2.2 Boost Ability Analysis of SL Z-Source Impedance Network

As described above, the inductor current i_{L1} increases during switching ON and decreases during switching OFF. During switching ON, the corresponding voltage across L_1 , V_{L1-ON} is equal to V_C . Applying the volt-second balance principle to L_1 , we can get the corresponding voltage across L_1 during switching OFF, V_{L1-OFF} , which is expressed by

$$V_{L1-OFF} = -\frac{D}{1-D}V_C = V_{L3-OFF} \quad (5-1)$$

Similarly, the inductor increases during switching ON and decreases during switching OFF. The corresponding voltage across L_3 , V_{L3-ON} and V_{L3-OFF} are equal to V_C and $(V_{C2} - V_{in} + V_{L1-OFF})$. Applying the voltage-second balance principle to L_3 , we have

$$\begin{cases} DTV_C = (1-D)T(V_C - V_{in} + V_{L1-OFF}) \\ DTV_{in} = (1-D)T(V_C - V_{in} - \frac{D}{1-D}V_C) \end{cases} \quad (5-2)$$

Hence, we can get the Z-capacitor voltage as

$$V_C = \frac{1-D}{1-3D}V_{in} \quad (5-3)$$

During switching OFF, C_1 , L_1 , L_3 , and the DC-link voltage V_{dc} form a closed loop; therefore, the following equation is obtained

$$V_C = V_{dc} + V_{L1-OFF} + V_{L3-OFF} \quad (5-4)$$

Thus, the peak voltage across the DC-link can be expressed as

$$V_{dc} = \frac{1+D}{1-3D}V_{in} = BV_{in} \quad (5-5)$$

The boost factor of the SL Z-source impedance, B is thus expressed by

$$B = \frac{1+D}{1-3D} = \frac{1+T_{sh}/T}{1-3T_{sh}/T} \quad (5-6)$$

For the comparison of the individual boost ability, the curves of the boost factor B versus the duty ratio D for classical Z-source impedance network and the proposed SL Z-source impedance network, respectively, are depicted in Fig. 5.5. As shown in Fig. 5.5, the boost ability of the proposed SL impedance network is significantly increased compared with that of the classical Z-source impedance network.

Figure 5.5 Boost ability comparison of the classical Z-source impedance network and the proposed SL Z-source impedance network

5.2.3 Boost Inversion Ability Analysis of the Whole Inverter

The boost ability of a whole Z-source is determined by the interactions of Z-source impedance and the PWM control method applied to the main circuit. As described in [40], two PWM control methods, termed as *the simple boost control method* and *the maximum boost control method* have been explored, which result in the different relationships of the voltage boost ability versus the given modulation index M . Since the above two methods can be regarded as the theoretical basis of various advanced PWM control strategies such as the harmonic injection method and space vector PWM method, in the following parts boost ability of the proposed whole inverter under the condition of these two methods will be explored, respectively.

As discussed in chapter 1, the obtainable shoot-through duty ratio of the simple boost control method can be regarded as a constant value, and its maximum value is limited to $(1-M)$. The voltage conversion ratio of the whole inverter G can be expressed by

$$G = \frac{\tilde{v}_{pn}}{V_{in}/2} = MB \quad (5-7)$$

where $\tilde{v}_{pn}$ is the peak value of the output phase voltage.

Therefore, according to (5-6) and (5-7), the maximum voltage conversion ratio G_{max} versus any desired modulation index M , can be expressed by

$$G_{max} = M B|_{D=1-M} = \frac{M(2-M)}{3M-2} \geq G_{0-s} \quad (5-8)$$

Where G_{0-s} is defined as the maximum voltage conversion ratio of the classical ZSI and its expression depend on M is given in Table 1-2 as

$$G_{0-s} = \frac{M}{2M-1} \quad (5-9)$$

For the maximum boost control method as shown in Fig. 1.10, the key point is that all null states need to be turned into the shoot-through state so as to maximize the duty ratio as large as possible. Therefore, the shoot-through duty cycle varies in each cycle. As described in Table 1-2, the average duty ratio of the shoot-through state, $\bar{D}$ is expressed by

$$\bar{D} = \frac{\bar{T}_{sh}}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \quad (5-10)$$

Substituting (5-10) to (5-6), we can get the equivalent boost factor $\bar{B}$ under the condition of variable duty ratios.

$$\bar{B} = \frac{1 + \bar{D}}{1 - 3\bar{D}} = \frac{4\pi - 3\sqrt{3}M}{9\sqrt{3}M - 4\pi} \quad (5-11)$$

Therefore, the maximum voltage conversion ratio G_{max} versus any desired modulation index M , approximates to

$$G_{max} = \frac{\hat{v}_{pn}}{V_{in}/2} = M\bar{B} = \frac{M(4\pi - 3\sqrt{3}M)}{9\sqrt{3}M - 4\pi} > G_{0_m} \quad (5-12)$$

Where G_{0_m} is defined as the maximum voltage conversion ratio of the classical ZSI and its expression depend on M is given as

$$G_{0_m} = \frac{\pi M}{3\sqrt{3}M - \pi} \quad (5-13)$$

Fig. 5.6 (a) shows the maximum obtainable voltage conversion ratios versus the given modulation index under the simple boost control condition, where Curve 1 and Curve 2 correspond to the proposed SL ZSI and the classical ZSI, respectively. It is shown that no voltage boost ability can be obtained at $M=1$. However, at $M<1$, with the decrease of M , the voltage boost ability of the proposed inverter becomes much stronger than that of the classical ZSI, which means that for a given voltage conversion ratio, a higher modulation index can be used in the proposed inverter to improve the inverter performance.

Fig. 5.6 (b) shows the maximum obtainable voltage conversion ratios versus the given modulation index under the maximum boost control condition, where Curve 1 and Curve 2 correspond to the proposed SL ZSI and the classical ZSI, respectively. It is shown that the voltage boost abilities of both these two inverters have been developed to a wider range by the maximum boost control method. As with the observation of Fig. 5.6 (a), the

proposed inverter shows its advantage of higher voltage boost ability at the lower modulation index.

Figure 5.6 Comparison of the maximum voltage conversion ratio of the proposed SL ZSI and classical ZSI under different modulation condition

5.2.4 Summary of Stresses

The current stresses of the impedance-type power converters are different under different control and load conditions, and the exact current analysis results on the classical ZSI are still a topic to be explored [37, 44, 95, 96]. For the purpose of comparison, both the proposed inverter and the classical ZSI are represented by the simplified equivalent circuit as shown in Fig. 5.7 [44]. Different from Fig. 5.3, an inductive load impedance ($Z_l = R_l + sL_l$) is paralleled with S directly as shown in Fig. 5.7. As for the proposed inverter, the inductor currents $I_{L1} - I_{L4}$ are the same and can be expressed by I_L for the convenience of analysis. The tedious computation is thus avoided.

Figure 5.7 Simplified and unified equivalent circuit of impedance-type power inverters (i.e., the proposed SL ZSI and classical ZSI)

Applying the steady-state analysis method in [44] to Fig. 5.7, we can obtain the voltage and current stresses of the main components (passive power switch D_{in} , L , C and DC link) and tabulated them in Table 5-1. The results in Table 5-1 are based on the assumption that both of these two inverters are working in the case of the same D and V_{in} . Consequently, it can be known that the proposed inverter has the higher voltage and current stresses due to its stronger voltage boost ability.

When the proposed inverter is used to replace the classical ZSI in a particular case, V_{dc} and V_{in} are usually fixed. If we assume that the detailed value of D in the classical ZSI is k , the corresponding D in the proposed inverter should be $k/(2-k)$ so as to obtain the same V_{dc} . Correspondingly, the voltage and current stresses are tabulated in Table 5-2. It is seen from Table 5-2 that the voltage stresses of the proposed inverter are the same to those of the classical ZSI. The current stresses of the proposed inverter have a rise for the same load impedance, thus higher power is transferred from the source to the load under this condition compared to the classical ZSI, which indicates that the proposed inverter has a stronger power processing capability. If the condition of the same load currents is considered, the current stresses of these two topologies will be the same.

Table 5–1: Stress comparison in the case of the same D and V_{in}

	SL ZSI	Classical ZSI
V_{dc}	$\frac{1+D}{1-3D}V_{in}$	$\frac{1}{1-2D}V_{in}$
V_C	$\frac{1-D}{1+D}V_{dc}$	$(1-D)V_{dc}$
V_{Din}	V_{dc}	V_{dc}
I_{Din}	$2I_L-I_l$	$2I_L-I_l$
I_l	$(1-D)\frac{V_{dc}}{R_l}$	$(1-D)\frac{V_{dc}}{R_l}$
I_L	$\frac{(1-D)^2}{1-3D}\frac{V_{dc}}{R_l}$	$\frac{(1-D)^2}{1-2D}\frac{V_{dc}}{R_l}$

Table 5–2: Stress Comparison in the case of the same V_{dc} , V_{in} and R_l

	SL ZSI	Classical ZSI
V_{dc}	$\frac{1}{1-2k}V_{in}$	
V_C	$(1-k)V_{dc}$	
V_{Din}	V_{dc}	
I_{Din}	$2I_L-I_l$	
I_l	$\frac{2}{2-k}I_{lo}$	I_{lo}
I_L	$\frac{2}{2-k}I_{Lo}$	I_{Lo}

5.2.5 Discussion

On the basis of the foregoing theoretical analysis, an overview from two designated topics is given, which tries to demonstrate the main characteristics and technical issues for the future study and application.

Compact Structure Scheme

From the viewpoint of the circuit structure, it is seen that two more inductors are added so that the practical circuit construction with discrete inductors might make the inverter more complex in the size and cost. Reexamining the current and voltage dynamics of each inductor, we see that the corresponding waveforms in each cycle as shown in Fig. 5.8 (a) are the same due to the symmetrical characteristics of switching actions. Therefore, as shown in Fig. 5.8 (b), the original SL cells can be improved by introducing the coupled inductor technique [97-99], by which the compact structure can be successfully obtained. All analysis results in previous parts are applied to the case with the coupled inductor structure, and only the transient characteristics will be affected.

Figure 5.8 Compact circuit scheme using the coupled inductors a) enlarged waveforms of each inductor; b) Coupled inductors applied to the proposed inverter

Figure 5.9 Typical applications of SL ZSI in distributed renewable energy power system

System-level Applications

As discussed in [100], due to the limited boost ability of the classical ZSI, the wide voltage range and limited voltage level of the renewable energy sources usually have to require a DC/DC boosted power converter to realize the high voltage conversion ratios. Therefore, from the viewpoint of the voltage boost ability, it is seen that the proposed inverter will be very competitive in the areas that need the high voltage conversion ratios (usually $G > 2$). Furthermore, from (5-8), it is known that the proposed inverter has a voltage buck inversion ability in the case that a small modulation index is taken to

generate the PWM signal. This step-down function can be utilized for those applications that need a slightly decreasing of the output voltage amplitude. In the case that the high reliability of the main circuit is required, the proposed inverter will show the distinct advantage over all traditional topologies. As shown in Fig. 5.9, the proposed inverter can be utilized in the future distributed renewable energy power systems.

5.3 Simulation and Experimental Verification

5.3.1 Simulation Verification

To verify the above theoretical results, a simulation example for the voltage inversion from dc 36V to ac 110V (RMS) is given in the physical security information management (PSIM) software. It is seen that the required voltage conversion ratio will be as high as 8.64, which will be difficult for the classical ZSI. Here, both the simple boost control method and the maximum boost control method are to be applied to the circuit. The main circuit parameters are chosen as follows

- 1) SL Z-source impedance network: $L_1=L_2=L_3=L_4=2\text{mH}$, $C_1=C_2=800\mu\text{F}$
- 2) Three-phase output filter: $L_f=1\text{mH}$, $C_f=22\mu\text{F}$;
- 3) The switching frequency $f_s=1/T=10\text{kHz}$;
- 4) Three-phase balanced resistive load, $R=25\Omega$
- 5) All components are assumed ideal.

Simple Boost Control

Under the condition of the simple boost control, according to (5-8), we make $D=0.3$ and $M=0.7$. Then, from (5-5) – (5-8), we obtain that $B=13$, $G=9.1$, $V_{dc}=468\text{V}$, $V_{C1}=V_{C2}=252\text{V}$ and $\hat{v}_{pn}=163.8\text{V}$ (i.e., $V_{pn-rms}=115\text{V}$). Since the duty cycle of the shoot-through state is constant, it is easy to implement the control circuit by an analog PWM circuit in the simulation. Fig. 5.10 (a) shows the simulation results from the zero initial condition to the steady state, where the phase voltage of Phase A (V_{an}), DC-link voltage (V_{dc}) and the Z-capacitor voltages (V_{C1} and V_{C2}) are recorded, respectively. It is seen that the steady-state performance in the simulation is identically matching to the theoretical analysis. The enlarged waveforms in the steady state are shown in Fig. 5.10 (b), where $I_{short-through}$

(i.e., the current flowing from the top bus to the bottom DC bus during T_{sh}) is recorded so as to compare with I_L . It is verified that the sum of all four inductor currents (i.e., $4I_L$) is about equal to $I_{short-through}$ during each T_{sh} , besides, the voltage variation ratios of the Z-capacitors are very small ($<0.5\%$).

If the same values of D and M as the simulation are applied to the classical ZSI, the boost inversion ability will be decreased sharply. The corresponding parameters are: $B=2.5$, $G=1.75$, which are much lower than those achieved by the proposed SL ZSI. Correspondingly, $\hat{v}_{pn}$ is equal to 63V in theory, i.e., only 44.6V (RMS) phase voltage can be achieved at the AC side, so it is far away from the original design specification.

Figure 5.10 Simulation results under the simple boost control condition

Maximum Boost Control

Under the condition of the maximum boost control, according to (5-10) – (5-12), we let $M=0.8577$. Therefore, we obtain that $\bar{D}=0.2907$, $\bar{B}=10.1$, $\bar{B}=10.1$, $G_{max}=8.66$, $V_{dc}=363.6V$, $V_{C1}=V_{C2}=200V$ and (i.e. $V_{pn-rms}=110V$). Obviously, compared with the stresses in the previous case, the stresses in this case are significantly decreased. To produce the varying duty ratios in PSIM, C programming is performed in a dynamic link library (DLL) block, which can calculate and send the real-time PWM signals like a digital unit. Fig. 5.11 shows the simulation results from the zero initial condition to the steady state. Because the duty ratio varies periodically, a small oscillation has been

introduced into the steady-state values of V_{dc} , V_{C1} and V_{C2} . From the small harmonic associated with the output phase voltage and the small voltage oscillation of the capacitor voltages, it is seen that the power quality under the maximum boost control condition is not as good as that under the simple boost control condition. On the whole, the steady-state performance is very close to the theoretical analysis.

For the case of the classical ZSI, if M is taken as 0.8577, the boost inversion ability is still very weak. The corresponding parameters are: $\bar{B} = 2.389$ and $G_{max} = 2.05$. Only 52.2V (RMS) phase voltage can be obtained at the ac side.

Figure 5.11 Simulation results under the maximum boost control condition

5.3.2 Experimental Verification

The same parameters as the simulation are chosen to construct a testing hardware circuit. The input source voltage is reduced to 18V and output phase voltage is reduced to 55V (RMS value) due to the laboratory limitation. Thus, all the voltage stresses will reduce to half. The control scheme is utilized by employing a DSPACE ds1006 with composed C codes and the SVPWM strategy is adopted. The output phase voltages are shown in Figs. 5.12 and 5.13, which correspond to the experiment results under the simple boost control condition and the maximum boost control condition, respectively. The experimental results have a good agreement with the simulation and theoretical analysis results.

(a) CH1: S_{ap} (10V/div); CH2: S_{an} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{an} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{bn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{bn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{cn} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{cn} (5V/div)

(g) CH1: V_c (50V/div); CH2: V_{dc} (100V/div)

(h) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 5.12 Experiment waveforms under the simple boost control condition: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a in two switching cycles; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b ; (e) switching actions of phase c ; (f) enlarged waveforms of switching actions of phase c ; (g) V_c and V_{dc} ; (h) V_{pn} and V_{ab}

(a) CH1: S_{ap} (10V/div); CH2: S_{bn} (10V/div)

(b) CH1: S_{ap} (5V/div); CH2: S_{bn} (5V/div)

(c) CH1: S_{bp} (10V/div); CH2: S_{cn} (10V/div)

(d) CH1: S_{bp} (5V/div); CH2: S_{cn} (5V/div)

(e) CH1: S_{cp} (10V/div); CH2: S_{an} (10V/div)

(f) CH1: S_{cp} (5V/div); CH2: S_{an} (5V/div)

(g) CH1: V_c (50V/div); CH2: V_{dc} (50V/div)

(h) CH1: V_{pn} (50V/div); CH2: V_{ab} (100V/div)

Figure 5.13 Experiment waveforms under the maximum boost control condition: (a) switching actions of phase a ; (b) enlarged waveforms of switching actions of phase a ; (c) switching actions of phase b ; (d) enlarged waveforms of switching actions of phase b in two switching cycles; (e) switching actions of phase c ; (f) enlarged waveforms of switching actions of phase c ; (g) V_c and V_{dc} ; (h) V_{pn} and V_{ab}

5.4 Conclusion

In this chapter, a new SL Z-source inverter by improving the existing classical Z-source impedance network has been presented. The proposed inverter employs a unique SL Z-source impedance network to couple the low DC voltage energy source to the main circuit of the inverter. By an in-depth topology analysis, it is known that the proposed inverter can provide a strong boost inversion ability to overcome the limitations of the classical ZSI. To illustrate the theoretical analysis, an example for DC 36V input and ac 110V output is given under two typical PWM control conditions. Both the simulation and experimental results demonstrate the advantages of the proposed inverter in the topology and boost inversion ability. Therefore, the proposed inverter could be widely used in the distributed renewable energy power systems. Furthermore, the concepts of SL Z-source impedance network can be applied to all fields of DC/AC, AC/DC, AC/AC, and DC/DC power conversion, which will be beneficial for the engineering applications of the impedance-type power converters.

Chapter 6. Dynamic Modeling and Design-Oriented Analysis of SL ZSI

With the view of detailed analyzing the dynamic system of the proposed SL ZSI, an accurate small signal model of the SL ZSI has been presented. By employing the state-space averaging method, small signal models have been established and related transfer functions have been derived. Through mathematical analyses, the RHP zeros are found to present in the transfer functions. In order to keep satisfactory performance and stability, a group of root loci Plots are illustrated to observe the movements of the RHP zeros. To minimize the NMP effects caused by the RHP zeros, the parameters of the impedance network are carefully selected through simulation results.

6.1 Introduction

In previous chapter, the SL ZSI with enhanced voltage inversion ability has been proposed for the further applications for distributed renewable energy power system. As is known, most of these industrial applications require good quality of output voltage. Thus, an appropriate closed-loop control method is very important to maintain the output voltage waveform with different input voltage conditions and load disturbances, which asks for more research efforts on understanding the dynamic characteristics of SL impedance network.

In this chapter, an AC small signal model of the SL ZSI has been studied. By employing the state-space averaging method, small signal models have been well established and related transfer functions have been derived. Computer simulations are offered to verify the validity of the proposed modeling. The developed transfer functions indicate the existence of a RHP zero, which would limit the dynamic response of the system; hence, the shift of the poles and zeros with various values for a particular component has been analyzed in detail. Afterwards, simulation results are presented for verifying the dynamic response and selecting the values of the passive components in the impedance network.

6.2 State Space Averaging of SL ZSI

In this work, the voltage type SL ZSI has been analyzed. For ease of illustration and analysis, the studied topology is simplified as in Fig. 6.1, where the input diode and the inverter bridge are represented by two ideal switches S_1 and S_2 . A resistor and inductor connected in series are considered here as the load. To simplify the analysis, the following assumptions are tenable:

- 1) SL ZSI operates in continuous conduction mode;
- 2) All passive elements in X-shape network are lossless and symmetric, i.e. $C_1 = C_2 = C$ and $L_1 = L_2 = L_3 = L_4 = L$;
- 3) All switches and diode are ideal.

Figure 6.1. Simplified equivalent circuit of the SL ZSI

As introduced in the previous chapter, the SL ZSI has two operation modes in principle; namely shoot-through state and non-shoot-through state. The equivalent circuits of these two states are depicted in Fig. 6.2 (a) and (b), respectively.

Figure 6.2. Equivalent circuits of the SL ZSI in both operation modes

During the shoot-through state, the switch S_1 is turned off and the switch S_2 is turned on; thus the load is short-circuited. The inductors are charged by the capacitors in parallel through each SL cell.

Define the capacitor voltages and inductor currents as state variables. Since the dynamics of the L_1 and L_3 , L_2 and L_4 are always the same, i_{L1} and i_{L2} are selected only to simplify the analysis.

$$x(t) = [i_{L1}(t) \ i_{L2}(t) \ v_{C1}(t) \ v_{C2}(t) \ i_l(t)]^T \quad (6-1)$$

According to the equivalent circuit shown in Fig. 6.2 (a), the shoot-through state differential equations then can be written in the state space form as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L} & 0 \\ -\frac{2}{C} & 0 & 0 & 0 & 0 \\ 0 & -\frac{2}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-R_l}{L_l} \end{bmatrix} \cdot \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot v_{in} \quad (6-2)$$

which is always recorded as $\dot{x} = A_1 \cdot x + B_1 \cdot u$

where

$$A_1 = \begin{bmatrix} 0 & 0 & \frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L} & 0 \\ -\frac{2}{C} & 0 & 0 & 0 & 0 \\ 0 & -\frac{2}{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-R_l}{L_l} \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Alternatively, during the non-shoot-through state, the switch S_1 is turned on and the switch S_2 , is turned off. The inductors in either SL cell are connected in series and the energy stored in both SL cells is transferred to the inductive load. At the same time, to supplement the consumed energy during the shoot-through state, the capacitors are charged by voltage source via either SL cell.

According to the equivalent circuit shown in Fig. 6.2 (b), the non-shoot-through state differential equations then can be written in the state space form as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{2L} & 0 \\ 0 & 0 & \frac{-1}{2L} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & \frac{-1}{C} \\ \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{C} \\ 0 & 0 & \frac{1}{L_l} & \frac{1}{L_l} & \frac{-R_l}{L_l} \end{bmatrix} \cdot \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ \frac{1}{2L} \\ 0 \\ 0 \\ \frac{-1}{L_l} \end{bmatrix} \cdot v_{in} \quad (6-3)$$

that is $\dot{x} = A_2 \cdot x + B_2 \cdot u$,

where

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{2L} & 0 \\ 0 & 0 & \frac{-1}{2L} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & \frac{-1}{C} \\ \frac{1}{C} & 0 & 0 & 0 & \frac{-1}{C} \\ 0 & 0 & \frac{1}{L_l} & \frac{1}{L_l} & \frac{-R_l}{L_l} \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{2L} \\ \frac{1}{2L} \\ 0 \\ 0 \\ \frac{-1}{L_l} \end{bmatrix}$$

The duty ratio of S_2 is defined as d and that of S_1 is thus $1-d$ according to the assumption (1). Then an average model for the SL ZSI can then be deduced by performing state-space averaging equations (6-2) and (6-3) as follows:

$$\dot{x} = [A_1 d + A_2(1-d)] \cdot x + [B_1 d + B_2(1-d)] \cdot u \quad (6-4)$$

that is

$$\frac{d}{dt} \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d}{L} & \frac{d-1}{2L} & 0 \\ 0 & 0 & \frac{d-1}{2L} & \frac{d}{L} & 0 \\ \frac{-2d}{C} & \frac{1-d}{C} & 0 & 0 & \frac{d-1}{C} \\ \frac{1-d}{C} & \frac{-2d}{C} & 0 & 0 & \frac{d-1}{C} \\ 0 & 0 & \frac{1-d}{L_l} & \frac{1-d}{L_l} & \frac{-R_l}{L_l} \end{bmatrix} \cdot \begin{bmatrix} i_{L_1}(t) \\ i_{L_2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_l(t) \end{bmatrix} + \begin{bmatrix} \frac{1-d}{2L} \\ \frac{1-d}{2L} \\ 0 \\ 0 \\ \frac{d-1}{L_l} \end{bmatrix} \cdot v_{in} \quad (6-5)$$

The steady state equations at the operation point can be shown as:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D}{L} & \frac{D-1}{2L} & 0 \\ 0 & 0 & \frac{D-1}{2L} & \frac{D}{L} & 0 \\ \frac{-2D}{C} & \frac{1-D}{C} & 0 & 0 & \frac{D-1}{C} \\ \frac{1-D}{C} & \frac{-2D}{C} & 0 & 0 & \frac{D-1}{C} \\ 0 & 0 & \frac{1-D}{L_l} & \frac{1-D}{L_l} & \frac{-R_l}{L_l} \end{bmatrix} \cdot \begin{bmatrix} I_{L_1} \\ I_{L_2} \\ V_{C1} \\ V_{C2} \\ I_l \end{bmatrix} + \begin{bmatrix} \frac{1-D}{2L} \\ \frac{1-D}{2L} \\ 0 \\ 0 \\ \frac{D-1}{L_l} \end{bmatrix} \cdot V_{in} \quad (6-6)$$

According to the assumptions, the steady state Z-capacitor voltages and the Z-inductor currents can be obtained from equation (6 - 6) as follows:

$$V_C = \frac{1-D}{1-3D} \cdot V_{in} \quad (6-7)$$

$$I_l = \frac{(1+D)(1-D)}{1-3D} \cdot \frac{V_{in}}{R_l} \quad (6-8)$$

$$I_L = \frac{1-D}{1-3D} \cdot I_l = \frac{(1+D)(1-D)^2}{(1-3D)^2} \cdot \frac{V_{in}}{R_l} \quad (6-9)$$

These values are exactly the same as the results of the theoretical analysis in the previous chapter.

6.3 Derivation of Small signal Models and Transfer Functions

To derive the small-signal models, small time-varying perturbations are applied to the input voltage and the shoot-through duty cycle of S_2 described by $v_{in}(t) = V_{in} + \hat{v}_{in}(t)$ and $d(t) = D + \hat{d}(t)$. The perturbations lead to small signal variations in the state variables, $x(t) = X(t) + \hat{x}(t)$. Substituting these perturbations into (6-4), we get the perturbed state equations as follows,

$$\begin{aligned} \dot{\hat{x}} + \hat{x} &= \left[A_1(D + \hat{d}) + A_2(1 - D - \hat{d}) \right] \cdot (X + \hat{x}) + \left[B_1(D + \hat{d}) + B_2(1 - D - \hat{d}) \right] \cdot (V_{in} + \hat{v}_{in}) \\ &= [A_1D + A_2(1 - D)] \cdot X + [B_1D + B_2(1 - D)] \cdot V_{in} + [A_1D + A_2(1 - D)] \cdot \hat{x} + \\ &\quad [B_1D + B_2(1 - D)] \cdot \hat{v}_{in} + (A_1X - A_2X + B_1V_{in} - B_2V_{in}) \cdot \hat{d} \end{aligned} \quad (6-10)$$

then

$$\hat{\dot{x}} = [A_1D + A_2(1 - D)] \cdot \hat{x} + [B_1D + B_2(1 - D)] \cdot \hat{v}_{in} + (A_1X - A_2X + B_1V_{in} - B_2V_{in}) \cdot \hat{d} \quad (6-11)$$

Using Laplace transformation, (6-11) becomes

$$\begin{bmatrix} s \cdot \hat{i}_{L1}(s) \\ s \cdot \hat{i}_{L2}(s) \\ s \cdot \hat{v}_{C1}(s) \\ s \cdot \hat{v}_{C2}(s) \\ s \cdot \hat{i}_l(s) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D}{L} & \frac{D-1}{2L} & 0 \\ 0 & 0 & \frac{D-1}{2L} & \frac{D}{L} & 0 \\ \frac{-2D}{C} & \frac{1-D}{C} & 0 & 0 & \frac{D-1}{C} \\ \frac{1-D}{C} & \frac{-2D}{C} & 0 & 0 & \frac{D-1}{C} \\ 0 & 0 & \frac{1-D}{L_l} & \frac{1-D}{L_l} & \frac{-R_l}{L_l} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_{C1}(s) \\ \hat{v}_{C2}(s) \\ \hat{i}_l(s) \end{bmatrix} + \begin{bmatrix} \frac{1-D}{2L} \\ \frac{1-D}{2L} \\ 0 \\ 0 \\ \frac{D-1}{L_l} \end{bmatrix} \hat{v}_{in}(s) + \begin{bmatrix} \frac{2V_{C1} + V_{C2} - V_{in}}{2L} \\ \frac{V_{C1} + 2V_{C2} - V_{in}}{2L} \\ \frac{-2I_{L1} - I_{L2} + I_l}{C} \\ \frac{-I_{L1} - 2I_{L2} + I_l}{C} \\ \frac{-V_{C1} - V_{C2} + V_{in}}{L_l} \end{bmatrix} \hat{d}(s) \quad (6-12)$$

Recalling the assumptions (2), the steady state values of the capacitors should be the same, and so are the values of the inductors, i.e., $V_{C1} = V_{C2} = V_C$ and $I_{L1} = I_{L2} = I_L$. Hence, (6-12) can be reduced as follows

$$\begin{cases} \hat{i}_L(s) = \frac{(3D-1) \cdot \hat{v}_C(s) + (1-D) \cdot \hat{v}_{in}(s) + (3V_C - V_{in}) \cdot \hat{d}(s)}{2sL} \\ \hat{v}_C(s) = \frac{(1-3D) \cdot \hat{i}_L(s) - (1-D) \cdot \hat{i}_l(s) - (3I_L - I_l) \cdot \hat{d}(s)}{sC} \\ \hat{i}_l(s) = \frac{2(1-D) \cdot \hat{v}_C - R_l \cdot \hat{i}_l(s) - (1-D) \cdot \hat{v}_{in}(s) - (2V_C - V_{in}) \cdot \hat{d}(s)}{sL_l} \end{cases} \quad (6-13)$$

According to the (6-13), the equivalent circuits of the AC small-signal models of the SL ZSI are depicted in Fig. 6.4. The circuit variables of Fig. 6.3 (a) (b) and (c) are the small signals of Z-inductor current, Z-capacitor capacitors, and load inductor current respectively. Thus, these figures represent the small signal model equation described in (6-13). In these figures, all the terms that contain the small signal variables $\hat{i}_L$, $\hat{v}_C$ or $\hat{i}_l$ are considered as dependent sources and the terms that contain the small signal variable $\hat{d}$ are regarded as independent sources.

(a)

(b)

(c)

Figure 6.3 Equivalent circuits of the small-signal models of the SL ZSI

And the small-signal relationship for the Z-capacitor voltage and Z-inductor current can be written as follows

$$\begin{cases} \hat{v}_C(s) = G_{vc-vin}(s) \cdot \hat{v}_{in}(s) + G_{vc-d}(s) \cdot \hat{d}(s) \\ \hat{i}_L(s) = G_{iL-vin}(s) \cdot \hat{v}_{in}(s) + G_{iL-d}(s) \cdot \hat{d}(s) \end{cases} \quad (6-14)$$

where $G_{vc-vin}(s)$, $G_{vc-d}(s)$, $G_{iL-vin}(s)$ and $G_{iL-d}(s)$ denote the transfer function of Z-capacitor voltage to input voltage, Z-capacitor voltage to shoot-through duty ratio, Z-inductor current to input voltage, and Z-inductor current to shoot-through duty ratio, respectively. All these transfer functions can be derived from (6-13), which are shown in following equations

$$\begin{aligned} G_{vc-vin}(s) &= \left. \frac{\hat{v}_C(s)}{\hat{v}_{in}(s)} \right|_{\hat{d}(s)=0} \\ &= \frac{[(1-D)(1-3D) + 2(1-D)^2 L]s + (1-D)(1-3D)R_l}{2LCL_l s^3 + 2LCR_l s^2 + [4(1-D)^2 L + (1-3D)^2 L_l]s + (1-3D)^2 R_l} \end{aligned} \quad (6-15)$$

$$\begin{aligned} G_{vc-d}(s) &= \left. \frac{\hat{v}_C(s)}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0} \\ &= \frac{\begin{cases} -2LL_l(3I_L - I_l)s^2 + [(1-3D)L_l(3V_C - V_{in}) + 2(1-D)L(2V_C - V_{in})] \\ -2LR_l(3I_L - I_l)s + (1-3D)(3V_C - V_{in})R_l \end{cases}}{2LCL_l s^3 + 2LCR_l s^2 + [4(1-D)^2 L + (1-3D)^2 L_l]s + (1-3D)^2 R_l} \end{aligned} \quad (6-16)$$

$$G_{iL-in}(s) = \left. \frac{\hat{i}_L(s)}{\hat{v}_{in}(s)} \right|_{\hat{d}(s)=0} \quad (6-17)$$

$$= \frac{(1-D)CL_t s^2 + (1-D)CR_t s + (1+D)(1-D)^2}{2LCL_t s^3 + 2LCR_t s^2 + [4(1-D)^2 L + (1-3D)^2 L_t]s + (1-3D)^2 R_t}$$

$$G_{iL-d}(s) = \left. \frac{\hat{i}_L(s)}{\hat{d}(s)} \right|_{\hat{v}_{in}(s)=0}$$

$$= \frac{\left\{ CL_t(3V_C - V_{in})s^2 + [CR_t(3V_C - V_{in}) - (3D-1)L_t(3I_L - I_l)]s + 2(1-D)^2 \cdot \right.}{\left. (3V_C - V_{in}) + (1-D)(3D-1)(2V_C - V_{in}) - (3D-1)R_t(3I_L - I_l) \right\}} \frac{1}{2LCL_t s^3 + 2LCR_t s^2 + [4(1-D)^2 L + (1-3D)^2 L_t]s + (1-3D)^2 R_t}$$

(6-18)

6.4 Simulation Verification and Root Locus Analysis

In order to validate the effectiveness of the derived small-signal model, both the simplified average model and the detailed model are tested by using MATLAB/Simulink software. System parameters used for simulations are given in Table 6–1.

Table 6–1: Parameters used for simulation of SL ZSI

<i>Parameters</i>	<i>Values</i>
V_{in}	50V
L	2mH
C	800 μF
L_l	2mH
R_l	10Ω
D	0.2
f_s	10kHz

The simulation results are illustrated in Fig. 6.4. A step change of shoot-through duty ratio from 0 to 0.2 is introduced to both models: the detailed circuit model (Fig. 6.4 (a)) and the simple-equivalent model (Fig. 6.4 (b)). Then to compare these two methods, an enlarged waveform is given in Fig. 6.4 (c). As shown in these figures, the steady state Z-

capacitor voltages of both models are 100V, which perfectly matches the expected value using equation (6-7).

(a) detailed model

(b) simplified equivalent model

(c) comparison in detail

Figure 6.4. Simulation results of Z-capacitor voltage of SL ZSI

It is noted that one of the notable advantages of small-signal models is to predict RHP zeros of the transfer functions. Hence, further study on the transfer functions should be conducted. Taking the transfer function (6-16) for example, the numerator is a quadratic equation. As we know, for a quadratic equation $ax^2 + bx + c = 0$, there will be two different poles x_1 and x_2 if the condition $b^2 - 4ac > 0$ is fulfilled. In addition, we can obtain that $x_1 x_2 = c/a$ according to Lagrange resolvents. With respect to this case, substituting (6-7) – (6-9) into (6-15), the coefficients a and c can be expressed as:

$$\begin{cases} a = -2LL_t(3I_L - I_l) = -\frac{4(1+D)(1-D)LL_t}{(1-3D)^2} \cdot \frac{V_{in}}{R_l} \\ c = (1-3D)(3V_C - V_{in})R_l = 2V_{in} \cdot R_l \end{cases} \quad (6-19)$$

Apparently, we can have the conclusion that $a < 0$, $c > 0$ and $c/a < 0$; therefore, we obtain that this transfer function has two zeros: one is negative and the other is a positive one, which is called RHP zero. It is noted that the tradeoff exists between performance

of the closed-loop system and zero placement of the open-loop architecture. Besides, the tradeoff would become rigorous when the RHP zeros are near the original point. Recalling that the SL ZSI used commonly for renewable energies like solar panels and fuel-cells that have low voltage sources and require wider operation ranges, it is very important to investigate the movements of zeros and poles for the system to keep stability and achieve good performances. Towards this end, a series of root-locus plots are depicted in Figs. 6.5, 6.6 and 6.7 by changing a specified parameter while keeping others constant. Since the movements of the zeros are not noticeable, the values of zeros in different conditions are listed in the following tables, where Z_p and Z_n represent the positive and negative zeros, respectively.

Figure 6.5. Pole-zero locus of the transfer function of SL ZSI with the increase of C

Table 6–2: Zero movements with the increase of C

C	400 μF	800 μF	1200 μF	1600 μF	2000 μF
Z_p	533.70	533.70	533.70	533.70	533.70
Z_n	-6505.92	-6505.92	-6505.92	-6505.92	-6505.92

In detail, it is indicated in Fig. 6.5 and Table 6–2 that the variations of C (from 400 μF to 2000 μF) have little influences on the either the positive or negative zeros. Additionally, with the increase of C , the conjugated complex poles move towards the original point gradually, which would yield a smaller damping factor and a slightly lower natural frequency.

Figure 6.6. Pole-zero locus of the transfer function of SL ZSI with the increase of L

Table 6–3: Zero movements with the increase of L

L	1mH	2mH	3mH	4mH	5mH
Z_p	1090.51	533.70	353.04	263.72	210.46
Z_n	-6368.32	-6505.91	-6556.74	-6583.27	-6599.38

It is observed from Fig. 6.6 and Table 6–3 that the increase in L (from 1mH to 5mH) will generally push the RHP zeros to the original point, which would aggravate the NMP effect. As mentioned above, the trade-off between performance of the closed-loop system and zero placement of the open-loop architecture would become rigorous when the RHP zeros are near the original point [85], which means that the RHP zeros should be made far from the original point to achieve good closed-loop performance. Hence, it is very important to select appropriate capacitance and inductance values to obtain a satisfying compromise between NMP effect and oscillatory response.

Figure 6.7. Pole-zero locus of the transfer function of SL ZSI with the increase of D

Table 6–4: Zero movements with the increase of D

D_{sh}	0.05	0.1	0.15	0.2	0.25
Z_p	3261.12	1990.95	1108.74	533.70	192.52
Z_n	-5288.23	-5650.21	-6067.65	-6505.97	-6925.83

Fig. 6.7 shows how the shoot-through duty ratio variations (from 0.05 to 0.25) would influence the Z-capacitor voltage of the SL ZSI. The root-locus plot indicates that with the increase of D , the RHP zeros would move towards the original point along the real axis; thus, the attainable closed-loop performances are degraded. Additionally, with the increase of D , the dominant conjugate poles are found to move close to the real axis, which would aggravate the damping effects.

6.5 Selection of Z-network Parameters

As discussed in previous section, changing the values of the Z-network inductance and capacitance would affect the movements of the RHP zeros. To achieve satisfying transient performance, appropriate capacitance and inductance values should be selected according to the following three case studies.

For the first case, the value of the capacitance is kept constant at 800 μ F, while the inductance value varies from 1mH to 4mH with a step change of the shoot-through duty ratio from 0.1 to 0.2 at $t=100$ ms. The results are shown in Fig. 6.8 (a). According to the NMP characteristic, the Z-capacitor voltage decreases initially before arising to the new value of steady state. It is indicated in Fig. 6.8 (a) that the large inductor value we choose, the heavier undershoot response we will obtain. Alternatively, for the second case, the value of inductance is kept at 2mH and the capacitance value varies from 400 μ F to 1200 μ F with the step change of duty ratio as well. The results are shown in Fig. 6.8 (b). During the step change, the NMP effect is also observed and it becomes severe with a higher capacitance value. From the first case, it is learned that to minimize the NMP effect, the Z-inductance value should be as small as possible; and the second case tells that a larger Z-capacitance can reduce the NMP effect. To investigate the coordination of the two parameters, the third case is studied. In this case, the values of both the capacitance and inductance are different for the three groups. The result is

shown in Fig. 6.8 (c). The NMP effect is also observed during the step change of the duty ratio. Besides, among the three groups, the second group with $L=2\text{mH}$ and $C=800\mu\text{F}$ has the smallest undershoot before getting back to the new steady-state. Thus, it is a better choice to construct the impedance network with the values of the second group.

(a) Case 1: $C=800\mu\text{F}$ and L varies

(b) Case 2: $L=2\text{mH}$ and C varies

(c) Case 3: both L and C vary

Figure 6.8. Variations of V_C with a step change of D from 0.1 to 0.2 at $t=100\text{ms}$

6.6 Conclusion

In this chapter, an simple equivalent small signal model of the SL ZSI has been presented. By employing the state-space averaging method, small signal model has been established and related transfer functions have been derived. Computer simulations are offered to verify the validity of the proposed model. Through mathematical analyses, the RHP zeros are found to present in the transfer functions, which would degrade the dynamic characteristics of the system. Hence a group of root loci plots are illustrated. These figures indicate the presence of RHP zeros, which would diminish the robustness of the system. In order to keep satisfactory performance and stability, various root-locus plots have been investigated by altering a specified parameter while keeping others as constant values. Unfortunately, the RHP zeros could not clear away by modulating the parameters but the NMP effects can be reduced by selecting proper values of the passive components in the impedance network. Therefore, the advanced closed loop control methods that can compensate the NMP effects should be explored based on the small signal modeling and analysis of this chapter.

Chapter 7. Space Vector PWM of SL ZSI

Based on the principles of the SVPWM technique for classical ZSIs discussed in Chapter 2 and Chapter 3, the theory and implementation schemes of SVPWM technique for single- and three-phase SL ZSI have been derived and discussed in this chapter. In addition, implementation schemes of maximum boost control and constant boost control methods for three-phase SL ZSIs based on SVPWM theory have been presented and compared with that of classical ZSIs, which shows the advantage of the enhanced voltage boost inversion ability of the SL ZSI. All the theoretical analysis has been verified by simulation and experimental results. The proposed control schemes will be helpful for enhancing the understanding of SVPWM technique and promoting the applications of SL ZSIs.

7.1 Introduction

Developed from classical ZSI, any modulation methods that used in ZSI are applicable for controlling the SL ZSI. Hence, as one of the advanced control strategies, the SVPWM technique for single- and three-phase SL ZSI will be discussed in this chapter.

Based on the discuss of Chapter 2 and Chapter 3, this chapter starts by reviewing the circuit principles of single-phase SL ZSI, followed by the principles and implementation schemes of SVPWM technique for the single-phase full-bridge SL ZSI. According to the selection of null vectors, three different switching patterns are introduced. Afterwards, the principles of SVPWM technique for three-phase SL ZSI are introduced briefly. In addition, implementation schemes of maximum boost control and constant boost control methods of three-phase SL ZSIs based on SVPWM theory are presented and compared with that of the classical ZSIs, which shows the advantage of the enhanced voltage boost inversion ability of the SL ZSI. All the proposed schemes have been validated by simulation and experiment results.

7.2 Operating Principle of Single-Phase Full-Bridge SL ZSI

The typical topology of the single-phase full-bridge SL ZSI is depicted in Fig. 7.1. As with the three-phase SL ZSI, the operating states of the single-phase impedance network

are classified into two groups: the shoot-through state and the non-shoot-through state. The corresponding equivalent circuits of single-phase ZSI in each state are depicted in Fig. 7.2 (a) and (b), respectively.

Figure 7.1. Typical topology of single-phase full-bridge SL ZSI

Figure 7.2 Equivalent circuits of the single-phase SL ZSI

During the shoot-through state, L_1 and L_3 are charged by C_1 in parallel for the top SL cell, and L_2 and L_4 are charged by C_2 in parallel for the bottom SL cell. The corresponding equivalent circuit is shown in Fig. 7.2 (a). It is seen that both the top and bottom SL cells perform the same function to absorb the energy stored in the capacitors. According to Fig. 7.2 (a), one can obtain the following equation:

$$\begin{cases} v_{L-on} = V_C \\ v_{i-on} = V_C + v_{L-on} = 2V_C \\ v_{dc-on} = 0 \end{cases} \quad (7-1)$$

Alternatively, during the non-shoot-through state, as shown in Fig. 7.2 (b), L_1 and L_2 are connected in series for the top SL cell, L_3 and L_4 are connected in series for the bottom SL cell. The energy stored in the inductors is transferred to the main circuit. At the same moment, to supplement the consumed energy of C_1 and C_2 during the shoot-through state, C_1 and C_2 are charged by V_{in} via each SL cell. According to Fig. 7.2 (b), one can obtain the following equation:

$$\begin{cases} 2v_{L-off} = V_{in} - V_C \\ v_{i-off} = V_{in} \\ v_{dc-off} = V_C - 2v_{L-off} = 2V_C - V_{in} \end{cases} \quad (7-2)$$

The average voltage across the Z-network inductor should be zero in one switching period T according to the volt-second balance principle. Then through (7-1) and (7-2), one can thus obtain

$$\bar{v}_L = \frac{T_{sh} \cdot v_{L-on} + T_n \cdot v_{L-off}}{T} = \frac{T_{sh} \cdot V_C + T_n \cdot \frac{(V_{in} - V_C)}{2}}{T} = 0 \quad (7-3)$$

$$V_C = \frac{T_n}{T_n - 2T_{sh}} V_{in} = \frac{T - T_{sh}}{T - 3T_{sh}} V_{in} = \frac{1 - D}{1 - 3D} V_{in} \quad (7-4)$$

The peak value of the DC-link voltage can be expressed as

$$V_{dc} = v_{dc-off} = V_C - 2v_{L-off} = 2V_C - V_{in} = \frac{1 + D}{1 - 3D} V_{in} \quad (7-5)$$

Then the boost factor of the impedance network is given by

$$B = \frac{T - T_{sh}}{T - 3T_{sh}} = \frac{1 + D}{1 - 3D} \quad (7-6)$$

Accordingly, the peak value of the output voltage can be stated as

$$\hat{V}_{pn} = M \cdot V_{dc} = M \cdot B \cdot V_{in} \quad (7-7)$$

7.3 SVPWM Theory of Single-Phase SL ZSI

As illustrated in Fig. 7.1, V_{ab} , and V_{ba} are the output voltages of a single-phase full-bridge SL ZSI. The relationship between the switching variable vector $[a \ b]^T$ and the phase voltage vector $[V_{ab} \ V_{ba}]^T$ is given as follows:

$$\vec{V}_S = \begin{bmatrix} V_{ab} \\ V_{ba} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} = B \cdot V_{in} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} \quad (7-8)$$

The possible switching states of the single-phase full bridge ZSI are listed in Table 7–1. It is shown that there are nine basic space vectors, including two active vectors (V_1 and V_2), two null vectors (V_0 and V_3) and five shoot-through vectors (V_{sh1} , V_{sh2} , V_{sh3} , V_{sh4} and V_{sh5}). Using the $\alpha\beta$ transformation matrix given in (7-9), the two dimensional voltage vector $\vec{V}_S = [V_{ab} \ V_{ba}]^T$ can be simplified into a single dimensional vector in the dq coordinate frame $\vec{V}_S' = V_\alpha$, which is written in (7-10). The derived output phase voltages of the nine states in the $\alpha\beta$ coordinate frame are listed in Table 7–1, and the corresponding basic space vectors are mapped into the $\alpha\beta$ plane in Fig. 7.3.

$$T_{ab-\alpha\beta} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \quad (7-9)$$

Thus, the voltage vectors in the new system can be expressed by:

$$\vec{V}_S' = T_{ab-\alpha\beta} \cdot \vec{V}_S = \begin{bmatrix} V_\alpha \\ 0 \end{bmatrix} = 2V_\phi \begin{bmatrix} \sin\omega t \\ 0 \end{bmatrix} \quad (7-10)$$

Where V_ϕ represents the peak value of the output phase voltage.

Table 7–1: Switching states and output voltages of a single-phase SL ZSI

	S_a	S_a'	S_b	S_b'	V_{ab}	V_{ba}	V_a
V_0	0	1	0	1	0	0	0
V_1	0	1	1	0	$-BV_{in}$	BV_{in}	$-\sqrt{2}BV_{in}$
V_2	1	0	0	1	BV_{in}	$-BV_{in}$	$\sqrt{2}BV_{in}$
V_3	1	0	1	0	0	0	0
V_{sh1}	1	1	0	1	0	0	0
V_{sh2}	1	1	1	0	0	0	0
V_{sh3}	1	0	1	1	0	0	0
V_{sh4}	0	1	1	1	0	0	0
V_{sh5}	1	1	1	1	0	0	0

And consequently, the basic space vectors in the new frame can be obtained using the following equation and mapped in Fig. 7.3.

$$\vec{V}_S' = T_{ab-\alpha\beta}^{-1} \cdot \vec{V}_S = \sqrt{2}B \cdot V_{in} \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} a \\ b \end{bmatrix} \quad (7-11)$$

Figure 7.3 Basic space vectors and sectors of single-phase SL ZSI

The desired output voltage of a single-phase full bridge SL ZSI can be obtained by using the linear combinations of the active vector, null vectors and shoot-through vectors according to the following equation:

$$\vec{V}_{ref} = \frac{T_i}{T} (\vec{V}_1, \vec{V}_2) + \frac{T_0}{T} (\vec{V}_0, \vec{V}_3) + \frac{T_{sh}}{T} (\vec{V}_{sh1} \sim \vec{V}_{sh5}) \quad (7-12)$$

where T_i , T_z and T_{sh} represent the time durations of active state, null state and shoot-through state, respectively.

As demonstrated in Fig. 7.3, the selection of the active vectors depends on the phase angle θ ($\theta=\omega t$). When $0 \leq \theta \leq \pi$, the V_2 is employed; otherwise the V_1 is adopted. To minimize the number of switching actions, the shoot-through state should be properly selected according to the principle of Fig. 7.4.

Figure 7.4 Switching transition between different states of single-phase SL ZSI

Similar to the SVPWM technique for classical single-phase ZSI, according to the selection of the null vector, three different switching patterns of SL ZSI are introduced. Pattern I adopts both null vectors V_0 and V_3 in one switching period, and T_z is distributed evenly into these two states; that is, $T_{00}=T_{03}=0.5T_z$. Pattern II adopts only one null vector V_0 , and T_z is entirely distributed into this state; that is, $T_{00}=T_z$, $T_{03}=0$. Pattern III adopts only the other null vector V_3 , and T_z is entirely distributed into this state; that is, $T_{00}=0$, $T_{03}=T_z$.

In addition, the time duration of each vector in the two sections can be expressed as follows through simple mathematical analysis:

$$\Rightarrow \begin{cases} T_2 = T \cdot M \sin \theta \\ T_z + T_{sh} = T - T_2 \end{cases} \quad (0 \leq \theta \leq \pi) \quad (7-13)$$

$$\Rightarrow \begin{cases} T_1 = T \cdot M \sin(\theta - \pi) \\ T_z + T_{sh} = T - T_1 \end{cases} \quad (\pi \leq \theta \leq 2\pi) \quad (7-14)$$

According to (7-6) and (7-7), the shoot-through time duration can be figured out using the following equation once the operating conditions of input DC voltage V_{in} , modulation index M and output voltage V_{ab} are given.

$$T_{sh} = \frac{1}{2} - \frac{M \cdot V_{in}}{2\hat{V}_{ab}} \quad (7-15)$$

Then the time duration of null state can be obtained through (7-13) – (7-15)

$$T_z = T - T_i - T_{sh} \quad (7-16)$$

The implementation schemes and the on-off switching signals of SVPWM for single-phase SL ZSI can be referred to Figs. 3.9–3.11.

7.4 Simulation and Experimental Verification

All three switching patterns of SVPWM technique for the single-phase SL ZSI have been verified in Matlab/Simulink software. The main circuit parameters for simulation are selected as follows:

- 1) input voltage source: $V_{in}=50\text{V}$;
- 2) impedance network: $L_1=L_2=L_3=L_4=2\text{mH}$, $C_1=C_2=800\mu\text{F}$;
- 3) output LC filter: $L_f=2\text{mH}$, $C_f=15\mu\text{F}$;
- 4) resistive load: $R=25\Omega$;
- 5) switching frequency: $f_s=10\text{kHz}$
- 6) modulation index: $M=0.8$;
- 7) shoot-through duty ratio: $D=0.2$;

Table 7–2: Theoretical values of single-phase SL ZSI

	<i>Conditions</i>			<i>Theoretical Values</i>				
	$V_{in} \text{ (V)}$	M	D	B	G	$V_{dc} \text{ (V)}$	$V_C \text{ (V)}$	$\hat{V}_{ab} \text{ (V)}$
Classical ZSI	50	0.8	0.2	1.67	1.33	83.5	66.7	66.7
SL ZSI				3	2.4	150	100	120

By using (3-4) – (3-7) and (7-4) – (7-7), the theoretical values of both classical ZSI and SL ZSI under this conditions are figured out and list in Table 7–2. Obviously, the voltage boost inversion ability has been improved though all the devices sustain high voltage stresses. The same parameters as the simulation are chosen to construct a testing hardware circuit. The control strategy is implemented using the DSPACE with C code. The simulation and experiment results are presented in Figs. 7.5–7.8, where V_C , V_{dc} , V_{pn} and V_{ab} represent the Z-capacitor voltage, DC-link voltage, output voltage before and after the filter, respectively. Due to length limit, the gating signals are not demonstrated here and they can be referred to Figs. 3.17-3.19 for single-phase ZSIs. All the waveforms show good agreement with the theoretical results.

Figure 7.5. Simulation results of SVPWM technique of single-phase SL ZSI

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100/div) and CH2: V_{ab} (100/div)

Figure 7.6. Experiment results of SVPWM pattern I of single-phase SL ZSI

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100/div) and CH2: V_{ab} (100/div)

Figure 7.7. Experiment results of SVPWM pattern II of single-phase SL ZSI

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100/div) and CH2: V_{ab} (100/div)

Figure 7.8. Experiment results of SVPWM pattern III of single-phase SL ZSI

7.5 SVPWM Theory of Three-Phase SL ZSI

The possible switching states of the three-phase SL ZSI are listed in Table 7–3. With the dq transformation matrix given in (2-2), the three dimensional voltage vectors can be

transferred into two dimensional vectors. The derived output phase voltages of the fifteen states in dq coordinate frame are listed in Table 7–3, and the corresponding voltage vectors termed basic space vectors are mapped into the dq plane in Fig. 7.9.

Table 7–3: Switching states and output voltages of a three-phase SL ZSI (!X represents complement of x, where $x=a,b,c$)

<i>states</i>		S_a	S_a'	S_b	S_b'	S_c	S_c'	V_d	V_q
<i>Null</i>	V_0	0	1	0	1	0	1	0	0
<i>Active</i>	V_1	0	1	0	1	1	0	$-\frac{\sqrt{6}}{6}V_{dc}$	$-\frac{\sqrt{2}}{2}V_{dc}$
<i>Active</i>	V_2	0	1	1	0	0	1	$-\frac{\sqrt{6}}{6}V_{dc}$	$\frac{\sqrt{2}}{2}V_{dc}$
<i>Active</i>	V_3	0	1	1	0	1	0	$-\frac{\sqrt{6}}{3}V_{dc}$	0
<i>Active</i>	V_4	1	0	0	1	0	1	$\frac{\sqrt{6}}{3}V_{dc}$	0
<i>Active</i>	V_5	1	0	0	1	1	0	$\frac{\sqrt{6}}{6}V_{dc}$	$-\frac{\sqrt{2}}{2}V_{dc}$
<i>Active</i>	V_6	1	0	1	0	0	1	$\frac{\sqrt{6}}{6}V_{dc}$	$\frac{\sqrt{2}}{2}V_{dc}$
<i>Null</i>	V_7	1	0	1	0	1	0	0	0
<i>Shoot-through</i>	V_{sh1}	1	1	b	$!b$	c	$!c$	0	0
<i>Shoot-through</i>	V_{sh2}	a	$!a$	1	1	c	$!c$	0	0
<i>Shoot-through</i>	V_{sh3}	a	$!a$	b	$!b$	1	1	0	0
<i>Shoot-through</i>	V_{sh4}	1	1	1	1	c	$!c$	0	0
<i>Shoot-through</i>	V_{sh5}	1	1	b	$!b$	1	1	0	0
<i>Shoot-through</i>	V_{sh6}	a	$!a$	1	1	1	1	0	0
<i>Shoot-through</i>	V_{sh7}	1	1	1	1	1	1	0	0

The objective of SVPWM technique is to approximate the desired output voltage by setting proper switching patterns of the power switches. As shown in Fig. 7.9, the

desired output voltage vector $\vec{V}_{ref}$ can be approached by the linear combinations of the basic space vectors, which is described by the following equation:

$$\vec{V}_{ref} = \frac{T_i}{T} \vec{V}_i + \frac{T_j}{T} \vec{V}_j + \frac{T_0}{T} (\vec{V}_0, \vec{V}_7) + \frac{T_{sh}}{T} \vec{V}_{shk} \quad (7-17)$$

($i, j = 1 \sim 6, k = 1 \sim 7$)

Figure 7.9 Basic space vectors and sectors of three-phase ZSI

The reference voltage vector $\vec{V}_{ref}$ of the three-phase ZSI is obtained by mapping the desired three-phase voltages to the dq plane through (7-18).

$$\vec{V}_{ref} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{abc-dq} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{\sqrt{6}}{2} \hat{V}_{pn} \begin{bmatrix} \cos \omega t \\ \sin \omega t \end{bmatrix} \quad (7-18)$$

As demonstrated in Fig. 7.9, the selection of the active vectors depends on the phase angle $\theta = \omega t$, it can be easily implemented once the phase angle is detected. The selection of shoot-through vectors should follow the principles of the following figure.

Figure 7.10 Switching transitions between different states of three-phase SL ZSIs

Similar to the SVPWM technique for three-phase ZSI, according to the selection of the null state and shoot-through state, three different switching patterns of SL ZSI can be obtained as discussed in Chapter 2. In addition, the time duration of each vector in the six sections can be expressed as follows through simple mathematical analysis:

$$\Rightarrow \begin{cases} T_4 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{\pi}{3} - \theta) \\ T_6 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin \theta \\ T_0 + T_{sh} = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] \end{cases} \quad (0 \leq \theta \leq \pi/3) \quad (7-19)$$

$$\Rightarrow \begin{cases} T_6 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{2\pi}{3} - \theta) \\ T_2 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{\pi}{3}) \\ T_0 + T_{sh} = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \sin \theta \right] \end{cases} \quad (\pi/3 \leq \theta \leq 2\pi/3) \quad (7-20)$$

$$\Rightarrow \begin{cases} T_2 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\pi - \theta) \\ T_3 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{2\pi}{3}) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] \end{cases} \quad (2\pi/3 \leq \theta \leq \pi) \quad (7-21)$$

$$\Rightarrow \begin{cases} T_3 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{4\pi}{3} - \theta) \\ T_1 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \pi) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \cos(\theta - \frac{\pi}{6}) \right] \end{cases} \quad (\pi \leq \theta \leq 4\pi/3) \quad (7-22)$$

$$\Rightarrow \begin{cases} T_1 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\frac{5\pi}{3} - \theta) \\ T_5 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{4\pi}{3}) \\ T_0 + T_{sh} = T \left[1 + \frac{\sqrt{3}}{2} M \cdot \sin\theta \right] \end{cases} \quad (4\pi/3 \leq \theta \leq 5\pi/3) \quad (7-23)$$

$$\Rightarrow \begin{cases} T_5 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(2\pi - \theta) \\ T_4 = \frac{\sqrt{3}}{2} T \cdot M \cdot \sin(\theta - \frac{5\pi}{3}) \\ T_0 + T_{sh} = T \left[1 - \frac{\sqrt{3}}{2} M \cdot \cos(\theta + \frac{\pi}{6}) \right] \end{cases} \quad (5\pi/3 \leq \theta \leq 2\pi) \quad (7-24)$$

Then according to (7-6) and (7-7), T_{sh} can be figured out using the following equation once the parameters T , M , V_{in} and V_{pn} are given.

$$T_{sh} = \frac{T}{2} - \frac{T \cdot M \cdot V_{in}}{4\hat{V}_{pn}} \quad (7-25)$$

And then the time duration of T_0 for each sector can be obtained by substituting (7-25) into (7-19) – (7-24). The implementation schemes and the on-off switching signals of SVPWM for three-phase SL ZSI can be referred to Figs. 2.3–2.5.

7.6 Implementation Scheme of Maximum Boost Control of SL ZSI Based on SVPWM Theory

According to the analysis of maximum boost control of classical ZSI, it is known that to achieve the maximum boost inversion ability, the average value of shoot-through duty ratio of the SL ZSI is expressed as:

$$\bar{D}_{max} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \quad (7-26)$$

Then, the maximum boost factor and maximum voltage boost inversion gain of the SL ZSI can be written as:

$$B_{max} = \frac{1 + \bar{D}_{max}}{1 - 3\bar{D}_{max}} = \frac{4\pi - 3\sqrt{3}M}{9\sqrt{3}M - 4\pi} \quad (7-27)$$

$$G_{max} = MB_{max} = \frac{M(4\pi - 3\sqrt{3}M)}{9\sqrt{3}M - 4\pi} \quad (7-28)$$

Equation (7-28) indicates that the maximum voltage gain of SL ZSI is determined by the modulation index only, as with the classical ZSI. The comparison of maximum voltage gain of classical ZSI and SL ZSI using the SVPWM-based control is illustrated in Fig. 7.11, where curve 1 and 2 represent that of the SL ZSI and classical ZSI, respectively. It is clearly shown that the achievable voltage gain of the SL ZSI is greater than that of the classical ZSI, even beyond the unit range.

Figure 7.11 Comparison of voltage gain of SVPWM-based maximum boost control

Additionally, it is derived in the previous chapter that the voltage stresses across the Z-capacitors of a SL ZSI can be calculated by the following equation:

$$V_{C1} = V_{C2} = \frac{1-D_{max}}{1-3D_{max}} V_{in} \quad (7-29)$$

According to (5-7) (7-26) (7-27) and (7-29), the expression of V_{C1} and V_{C2} is given as:

$$V_{C1} = V_{C2} = \frac{6\sqrt{3} \cdot \hat{V}_{pn}}{4\pi - 3\sqrt{3}M} \quad (7-30)$$

Equation (7-30) indicates that V_{C1} and V_{C2} of SL ZSIs are determined by both the desired output phase voltage and the modulation index, while it is indicated in (2-28) that V_{C1} and V_{C2} of classical ZSIs are determined by the desired output phase voltage only.

7.7 Implementation Scheme of Constant Boost Control of SL ZSI Based on SVPWM Theory

Similarly, according to the analysis of constant boost control of classical ZSIs, it is learned that to achieve maximum boost inversion ability while keeping the duty ratio constant, the shoot-through duty ratio of the SL ZSI is expressed as:

$$D = \frac{T_{sh}}{T} = 1 - \frac{\sqrt{3}}{2} M \quad (7-31)$$

Thus, the corresponding B and G can be expressed by the following equations:

$$B = \frac{1+D}{1-3D} = \frac{4-\sqrt{3}M}{3\sqrt{3}M-4} \quad (7-32)$$

$$G = MB = \frac{M(4-\sqrt{3}M)}{3\sqrt{3}M-4} \quad (7-33)$$

Equation (7-33) indicates that the maximum voltage gain of SL ZSI using the constant boost control method is determined by the modulation index only. The comparison of maximum voltage gain of classical ZSIs and SL ZSIs using the SVPWM-based constant boost control is illustrated in Fig. 7.12, where curves 1 and 2 represent that of the SL ZSI and classical ZSI, respectively. It is clearly shown that the achievable voltage gain of the SL ZSI is greater than that of the classical ZSI.

Figure 7.12 Comparison of voltage gain using SVPWM-based constant boost control

Additionally, according to (5-7) (7-29) (7-31) and (7-33), the voltage stresses across the Z-network capacitors, V_{C1} and V_{C2} can be expressed as:

$$V_{C1} = V_{C2} = \frac{2\sqrt{3}\hat{V}_{pn}}{4-\sqrt{3}M} \quad (7-34)$$

Equation (7-37) indicates that V_{C1} and V_{C2} are determined by both the desired output phase voltage and the modulation index, while (2-33) indicates that V_{C1} and V_{C2} of classical ZSIs are determined by the desired output phase voltage only. Due to the length limit, the details of the switching patterns of all switches in each sector can be referred to Figs. 2.3-2.5.

7.8 Simulation and Experimental Verification

7.8.1 Simulation Verification

To verify the validity of the proposed control schemes, different study cases are conducted in Matlab/Simulink software. The main circuit parameters are selected as follows:

- 1) impedance network: $L_1=L_2=L_3=L_4=2\text{mH}$, $C_1=C_2=800\mu\text{F}$;
- 2) output LC filter: $L_f=2\text{mH}$, $C_f=15\mu\text{F}$;
- 3) resistive load of each phase: $R=25\Omega$;
- 4) switching frequency: $f_s=10\text{kHz}$
- 5) desired output phase voltage: 110V (RMS)

Maximum Boost Control

For the three cases, modulation indices are different from each other; thus, from the foregoing theoretical analysis, it is known that the values of G_{max} will vary with the different configurations. To maintain a stable output phase voltage, different input DC source voltages should be appropriately configured for all cases.

To compare with the classical ZSI, the theoretical values of maximum boost control of both classical ZSIs and SL ZSIs under all operating conditions are listed in Table 7-4. Generally, with the increase of M , the voltage stresses across the DC-link V_{dc} decrease due to a smaller boost factor B . However, a higher DC source voltage is required under the large M condition, because the corresponding voltage gain G gets smaller. Also, it is observed that with the same M , the required input DC voltage of the classical ZSI is much higher than that of the SL ZSI due to a smaller voltage gain. The DC-link voltage stresses are the same for the classical ZSI and SL ZSI in each case. The Z-capacitor voltages of SL ZSI are different from case to case, which is in accordance with the theoretical results in (7-30); alternatively, the Z-capacitor voltages of classical ZSI keep the same for all the three cases, which is in accordance with the theoretical results in (2-28). Besides, the Z-capacitor voltage stresses of the SL ZSI are smaller than that of the classical ZSI. All these results show the advantages of SL ZSIs.

Table 7–4: Theoretical values of maximum boost control of both classical ZSIs and SL ZSIs under different operating conditions

Case No.		Condition		Expected Values			
		V_{in} (V)	M	B	G	V_{dc} (V)	V_C (V)
1	Classical ZSI	148.86	0.85	2.46	2.09	366.06	257.30
	SL ZSI	30.71		11.92	10.13	366.06	198.37
2	Classical ZSI	187.09	0.95	1.75	1.66	327.28	257.30
	SL ZSI	96.26		3.40	3.23	327.28	211.88
3	Classical ZSI	218.88	1.05	1.05	1.36	296.25	257.30
	SL ZSI	158.42		1.87	1.96	296.25	227.37

The simulated waveforms of the proposed SVPWM-based maximum boost control of SL ZSI with different M ($M=0.85$, 0.95 , and 1.05) are shown in Fig. 7.13 (a), (b) and (c), respectively, where V_{dc} indicates the voltage stress across the DC-link, V_C indicates the voltage stress of the Z-network capacitor, V_{pn} indicates the output phase voltage, and V_{ab} indicates the output line-to-line voltage. It can be seen that, all of results shown in the figures have a good agreement with the theoretical analysis and the expected values listed in Table 7–4.

(a) Case 1: $M=0.85$ and $V_{in}=30.71V$

(b) Case 2: $M=0.95$ and $V_{in}=96.26V$

(c) Case 3: $M=1.05$ and $V_{in}=158.42\text{V}$

Figure 7.13. Simulation results of SVPWM-based maximum boost control of SL ZSI

SVPWM-Based Constant Boost Control

As with the cases of the maximum boost control, the modulation index is different for each case; and consequently, the values of B and G will vary with different operating conditions. To maintain the stable output phase voltage, different input DC source voltages should be configured appropriately.

To compare with the classical ZSI, the theoretical values of constant boost control of both classical ZSIs and SL ZSIs under all operating conditions are listed in Table 7-5. Generally, with the increase of M , the voltage stresses across the DC-link V_{dc} decrease due to a smaller boost factor B . However, a higher DC source voltage is required under the large M condition, because the corresponding voltage gain G gets smaller. Also, it is observed that with the same M , the required input DC voltage of the classical ZSI is much higher than that of the SL ZSI due to a smaller voltage gain. The DC-link voltage stresses are the same for the classical ZSI and SL ZSI in each case. The Z-capacitor voltages of SL ZSI are different from case to case, which is in accordance with the theoretical results in (7-34); alternatively, the Z-capacitor voltages of classical ZSI keep constant for all the three cases, which is in accordance with the theoretical results in (2-33). In addition, the Z-capacitor voltage stresses of the SL ZSI are smaller than that of the classical ZSI. All these results show the advantages of the SL ZSI.

Table 7–5: Theoretical values of constant boost control of both classical ZSIs and SL ZSIs under different operating conditions

Case No.		Condition		Expected Values			
		V_{in} (V)	M	B	G	V_{dc} (V)	V_C (V)
1	Classical ZSI	172.86	0.85	2.12	1.79	366.05	269.44
	SL ZSI	60.34		6.07	5.16	366.05	213.19
2	Classical ZSI	211.38	0.95	1.55	1.47	327.42	269.44
	SL ZSI	130.24		2.51	2.39	327.42	228.87
3	Classical ZSI	242.58	1.05	1.22	1.28	296.31	269.44
	SL ZSI	197.78		1.49	1.57	296.31	247.04

The simulated waveforms of constant boost control using the SVPWM pattern I with different M ($M=0.85$, 0.95 , and 1.05) are depicted in Figs. 7.14(a), (b) and (c), respectively. All the values shown in these figures are in accordance with the theoretical analysis results of Table 7-5.

(a) Case 1: $M=0.85$ and $V_{in}=60.34V$

(b) Case 2: $M=0.95$ and $V_{in}=130.24V$

(c) Case 3: $M=1.05$ and $V_{in}=197.78V$

Figure 7.14. Simulation results of SVPWM-based constant boost control of SL ZSI

7.8.2 Experimental Verification

To further verify the proposed control schemes, the same parameters as the simulation are chosen to construct a testing hardware circuit. Also, the desired output phase voltage is reduced to 55V (RMS value) due to the low power limitation. Thus, the input source voltage and all the voltage stresses will reduce to half. The gate signal was generated digitally using the DSPACE ds1006 with composed C codes and the switching frequency was 10 kHz. The case of $M=0.85$ was tested and the experiment results are depicted in Figs. 7.15 – 7.16, which correspond to the results of the SVPWM-based maximum boost control and constant boost control, respectively. It is shown that all the waveforms and values indicate a good agreement with the simulation results and theoretical analysis.

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 7.15. Experiment results of SVPWM-based maximum boost control of SL ZSI

(a) CH1: V_C (50V/div); CH2: V_{dc} (50V/div) (b) CH1: V_{pn} (100V/div); CH2: V_{ab} (100V/div)

Figure 7.16. Experiment results of SVPWM-based constant boost control of SL ZSI

7.9 Conclusion

In this chapter, the theory of SVPWM technique for single- and three-phase SL ZSI has been introduced and discussed. Besides, novel implementation schemes of maximum boost control and constant boost control methods for three-phase SL ZSIs based on SVPWM theory have been presented. The comparison study between SL ZSIs and classical ZSIs shows the advantage of higher boost inversion ability of SL ZSIs. All the theoretical analysis has been verified by simulation and experimental investigations. The proposed control schemes will be helpful for enhancing the understanding of SVPWM technique and promoting the applications of SL ZSI.

Chapter 8. Conclusions and Recommendations

8.1 Conclusions

This thesis concerns SVPWM theory and advanced topology of Z-source inverters. In Chapter 1, the background of the research work is introduced at first, and some basic issues of the classical ZSI are reviewed then. The detailed research work is given in Chapter 2-7, respectively.

In Chapter 2, the theory of SVPWM technique for the three-phase ZSI has been derived and discussed in detail. Besides, novel implementation schemes of maximum boost control and constant boost control methods for three-phase ZSIs based on SVPWM theory have been presented. Compared with the carrier-based strategies, the proposed SVPWM solution has wider linear operation range, and the number of switching actions is reduced significantly.

In Chapter 3, the SVPWM concept has been successfully extended to the single-phase ZSI. With the considerations on the circuit characteristics, the principles and implementation schemes of the SVPWM strategy for single-phase ZSI have been explained in detail. Three switching patterns according to different selections of null state and shoot-through state are discussed and compared with carrier-based strategies.

In Chapter 4, to enhance the understanding of the dynamic system of the impedance network, the mathematical models of improved ZSI have been studied in detail. By employing the state space averaging method, small-signal models have been well established and related transfer functions have been derived through mathematical analyses. To predict the RHP zeros of the transfer functions, a group of root loci Plots are illustrated and transient response of voltage stress of Z-capacitor during a step change in shoot-through duty ratio has been illustrated to show the existence of right hand plane zeros.

In Chapter 5, based on the study of dynamics of the Z-source impedance network, a new switched-inductor (SL) Z-source topology has been presented. The proposed inverter employs a SL Z-source impedance network to couple the low DC voltage energy source to the main circuit of the inverter. By an in-depth topology analysis, it is known that the proposed inverter can provide a strong boost inversion ability to

overcome the limitations of the classical ZSI. Both the simulation and experimental results demonstrate its advantages in the topology and boost inversion ability. The concepts of SL Z-source impedance network will be beneficial for the applications of the impedance-type power converters.

In Chapter 6, with the view of detailed analyzing the dynamic system of the proposed SL ZSI, an equivalent small signal model of the SL ZSI has been presented. By employing the state-space averaging method, small signal models have been established and related transfer functions have been derived. Through mathematical analyses, the RHP zeros are found to present in the transfer functions. In order to keep satisfactory performance and stability, a group of root loci Plots are illustrated to observe the movements of the RHP zeros. To minimize the NMP effects caused by the RHP zeros, the parameters of the impedance network are carefully selected through simulation results.

In Chapter 7, the theory and implementation schemes of SVPWM technique for single- and three-phase SL ZSI have been discussed. In addition, implementation schemes of maximum boost control and constant boost control methods for three-phase SL ZSI based on SVPWM theory have been presented and compared with that of classical ZSI, which shows the advantage of the enhanced voltage boost inversion ability of the SL ZSI.

Following the theoretical analysis, all the proposed topology and control schemes have been tested by simulation and experimental investigations and the results show satisfying agreement with the theoretical analysis. All the research work will be helpful for understanding the SVPWM technique for ZSI and the applications of impedance-type power inverters in renewable energy systems.

8.2 Recommendations

Based on the work accomplished in the thesis, the following aspects should be focused on in future research.

All the topologies of single and three-phase ZSI and SL ZSI in the thesis utilize ideal DC voltages as the input power source. However, the practical renewable energy sources, such as solar panels, fuel cells, and wind turbines, have quite complex dynamic

characteristics that may affect the performances of the inverters seriously. Thus, the future researches on ZSI and SL ZSI are supposed to replace the DC voltages by more accurate models with consideration of the dynamic characteristics of the power sources.

It is noted that the challenge of designing an inverter is to maintain its clean and stable sinusoidal output voltage under any conditions and the key point to achieve this end is an appropriate design of its closed-loop controller. Besides, through the dynamic modeling of the SL ZSI, the RHP zeros are found to exist in the transfer functions, which would degrade the performances of the closed-loop system. Thus, the possible future work could include proper closed-loop controller design with advanced RHP compensation methods based on the AC small signal modeling and analysis derived in this thesis.

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1. **K. Yu**, F. L. Luo, M. Zhu, and X. Cai, "Space Vector Pulse-Width Modulation Theory and Solution for Z-Source Inverters With Maximum Constant Boost Control", *International Journal of Circuit Theory and Applications*, 2012. (early publication, DOI: 10.1002/cta.1842)
2. M. Zhu, **K. Yu**, and F. L. Luo, "Switched-Inductor Z-Source Inverter", *Power Electronics, IEEE Transactions on*, vol. 25, pp. 2150-2158, 2010.
3. **K. Yu**, F. L. Luo, M. Zhu, J. Y. Zhao and K. J. Tseng, "Space Vector Pulse-Width Modulation for Single- Phase Full-Bridge Z-Source Inverter", *International Journal of Circuit Theory and Applications*, 2012. (Accepted)

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4. **K. Yu**, F. L. Luo, and M. Zhu, "Study of an Improved Z-Source Inverter: Small Signal Analysis", *Industrial Electronics and Applications, 2009. ICIEA 2009. 5th IEEE Conference*, 2010. pp. 2169-2174.
5. M. Zhu, **K. Yu**, and F. L. Luo, "Topology Analysis of a Switched-Inductor Z-Source Inverter", *Industrial Electronics and Applications, 2009. ICIEA 2009. 5th IEEE Conference*, 2010. pp. 364-369.
6. **K. Yu**, F. L. Luo, and M. Zhu, "Implementation of Maximum Constant Boost Control of Z-Source Inverters Based on Space Vector Modulation Technique", *Industrial Electronics and Applications, 2012. ICIEA 2012. 7th IEEE Conference*, 2012. pp. 1497-1502.
7. **K. Yu**, F. L. Luo, and M. Zhu, "Space Vector Pulse-Width Modulation Based Maximum Boost Control of Z-source inverters", in *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*, 2012, pp. 521-526.