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Abstract

Residue Number System (RNS) offers significant advantages over conventional number system in terms of parallel signal processing and power consumption. This makes it ideally suitable for communication, computer security, digital signal processing, in which long word addition and multiplication are involved critically. However, traditional Analog-Digital (binary)-Residue conversion scheme requires large silicon area and high power consumption. Therefore, direct Analog-to-Residue conversion starts to attract attention from circuit designers and researchers.

In this thesis, a novel direct A/R conversion scheme based on clock overlapping is proposed. The intermediate binary stage was eliminated completely. 2 comparators, 1 OpAmp, 1 resistor, 1 Capacitor, $3(\sum_{i=0}^n [\log_2 m_i] + 1)$ D Flip-Flops and several combinational circuit blocks, where n is the number of modulus channels and m is the modulus number. The logarithmically increase in hardware complexity and the low power dissipation make it ideally suitable for low-power high resolution application. A 3 channels (modulus 3,4,5) converter consumes $159.104\mu\text{W}$, with analog blocks and digital blocks consume $127.152\mu\text{W}$ and $31.952\mu\text{W}$ respectively. With more research to improve sampling speed, this technique will be more viable for future high speed application.

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1 Introduction

1.1 What is Residue Number System (RNS)?

Residue number system (RNS) was first written in book by the third-century Chinese scholar Sun Tzu -- a different Sun Tzu from the author of the famous *Art of War*. In Problem 26 of his *Suan Ching* (Calculation Classic), Sun Tzu posed a mathematical riddle:

We have things of which we do not know the number

If we count them by threes, we have two left over

If we count them by fives, we have three left over

If we count them by sevens, we have two left over

How many things are there?

In other words, "What number yields the remainders 2, 3, and 2 when divided by 3, 5, and 7, respectively?" In modern terminology, 2, 3, and 2 are residues, and 3, 5, and 7 are modulo . Sun Tzu gave a rule, the *Tai-Yen* (Great Generalization) for the solution of his puzzle. In 1247, another Chinese mathematician, Qin Jiushao, generalized the Great Generalization into what we now call the Chinese Remainder Theorem, a mathematical jewel.

1.2 Where to apply RNS and Why ?

In the 1950s, RNS was rediscovered by computer scientists, who sought to put it to use in the implementation of high-speed arithmetic and fault-tolerant computation. Three of the RNS properties make it very suitable. Firstly, the absence of carry-propagation in addition and multiplication, carry-propagation were the most significant speed-limiting factor in these operations. Secondly, the residue representations carry no weight-information, an error in any digit position in a given representation does not affect other digit positions. Lastly, there is no significance ordering of the digits in an RNS representation.

The new interest in RNS did not last long because of three main reasons:

- (1) A complete arithmetic unit should be capable of at least addition, multiplication, division, square-root, and comparisons, but implementing the last three in RNS is not easy;
- (2) Computer technology became more reliable;
- (3) Converting from RNS notation to conventional notation, for "human consumption", is difficult.

Nevertheless, in recent years there has been renewed interest in RNS. The reason for that includes the followings.

A great deal of computing now takes place in embedded processors, such as those found in mobile or implantable devices, for which the high speed, low-power or both specifications are critical.

The absence of carry-propagation facilitates the realization of high-speed, low-power arithmetic. Also, computer chips are now getting to be more and more dense, to have them to be fully tested will no longer be possible; so fault-tolerance and the general area of computational integrity have again become important.[1]

The great advantages of RNS architectures, especially in terms of speed and power have been mentioned, which make it quite suitable to implement RNS in different applications. However, in spite of their great advantages, RNS processors have not been found widely used but remained as an interesting research topic [2-4]. There are two main reasons behind the limited use of RNS in applications:

(1) Although the RNS representation simplifies and expedites addition and multiplication compared to the conventional binary system, other operations such as division, square-root, sign detection, and comparison are still difficult and are costly to apply in the residue domain. Thus, building an RNS based ALU that is capable of performing the basic arithmetic is not an easy job yet.

(2) Residue-to-Binary or Binary-to-Residue Conversion circuitry can be complex and the latency introduced by such circuits may offset the speed advantage gained by the RNS computation. Hence, the design of efficient conversion circuits is considered to be the bottleneck of a successful RNS system.

However, RNS architectures are still to be treated as an interesting theoretical topic for researchers. Some applications that are computationally intensive and require mainly recursive addition and multiplication operations, such as FFT, FIR filters, and public-key cryptography are appealing to be implemented using RNS. Therefore, investigating new conversion schemes can lead to overcoming some obstacles in the

RNS implementation of different applications by reducing the overhead of the conversion stages.

1.3 Why Direct Analog-to-Residue ?

Fig. 1.1 Conventional RNS Based System

Fig. 1.1 demonstrates a conventional RNS based system. Due to the hardware complexity, power consumption as well as the latency introduced by the forward and reverse converter as indicated in Fig 1.1, direct analog-to-residue and residue-to-analog conversion(ARC & RAC) techniques have been discussed more frequently among the circuit designers and researchers in recent years, and so the new architecture is shown as in Fig. 1.2.

Fig. 1.2 ARC-RNS Based System

1.4 Forward Conversion

Apparently from the above discussion, the main purpose and motivation of direct analog-to-residue conversion is to eliminate the forward conversion block. Therefore, the review on the modern forward converters is necessary here.

The forward converters are generally categorized into 2 kinds based on the moduli set used, which will be the arbitrary moduli set and the special moduli set respectively.

1.4.1 Arbitrary Moduli-Set Forward Converters

As the name itself implies, in this converter category, both of the numbers of the moduli channel and moduli number (integer value) are arbitrary. And this is useful for the application which needs very large dynamic range, in other words, very high resolution.

In order to represent this large dynamic range, researchers are focusing on 2 main approaches, first approach is to develop more efficient algorithms or schemes for the arbitrary moduli set conversion, whereas, the second approach is to find the new special moduli set numbers keeping the moduli number in each channel be as small as possible, so that, the efficiency will not decrease significantly.

There are 3 approaches in hardware implementation for the arbitrary moduli set forward conversion, look-up table-based, pure combinational circuitry-based and the combination of the two. Look-up table-based implementation will cost significant silicon area for a large dynamic range and makes the overall conversion inefficient. Whereas combinational circuitry needs pre-programming every time when the

different moduli numbers are chosen, and it does involved certain big-sized processing units like multi-bit modular adders, multiplexers, etc [5].

The hardware comparison tables of selected arbitrary converter are listed below [5].

TABLE 1.1 SERIAL METHOD: COMPARISON AMONG [5], [6] AND [7]

	No. of bits in exponent	No. of 2 to 1 MUX	No. of Gates used in MUX	Total No. of Gates	No. of FAs
Ref [5]	5 bits (4 to 1 MUX)	13	117	117+132+5+5FF	5
Ref [6]	5 bits (4 to 1 MUX)	13	117	117+132+5+5FF	5
Ref [7]	-	10	90	ROM+5INV+5FF	5

TABLE 1.2 PARALLEL METHOD: COMPARISON AMONG [5], [6] AND [7]

	No. of bits in exponent	No. of 2 to 1 MUX	No. of Gates used in MUX	Total No. of Gates	No. of FAs
Ref [5]	5 bits (4 to 1 MUX)	450	4050	4050+132+85+85FF	85
Ref [6]	5 bits (4 to 1 MUX)	790	7110	7110+132+155+155FF	155
Ref [7]	-	170	1530	ROM+1530+85INV+85FF	85

MUX : Multiplexer FF: Flip-Flop FA: Full Adder

The aim of quoting the above comparisons is to illustrate the general idea of the hardware requirement on implementing the arbitrary forward converter. More advanced and detail explanation on the algorithms and architectures are available in [1] and [5].

1.4.2 Special Moduli-Set Forward Converters

Early researches using mutually prime integers as the moduli numbers are in the chosen RNS (Arbitrary Moduli-Set Forward Conversion). However, it was later realized that by using 2^n related moduli sets, the basic building blocks like RNS adders, RNS multipliers, forward converters (binary-to-RNS), and reverse converters

(RNS-to-binary) can be implemented by using logic gates much more easier. Although moduli set like $\{2^n-1, 2^n, 2^{n-1}-1\}$ [8-10] was proposed and discussed, 4-channel sets $\{2^n-1, 2^n, 2^{n+1}, 2^{n+1}-1\}$ [11], $\{2^n-1, 2^n, 2^{n+1}, 2^{n+1}+1\}$ [12] and $\{2^n-3, 2^n-1, 2^n+1, 2^{n+1}+3\}$ [13] were even reported for large dynamic range. The most popular moduli set still goes to $\{2^n-1, 2^n, 2^{n+1}\}$ [14-16], as its close to the traditional binary representation in digital circuits and systems.

If the binary value X is represented as

$$X = B_1 * 2^{2n} + B_2 * 2^n + B_3 \quad (1.1)$$

the typical $\{2^n-1, 2^n, 2^{n+1}\}$ based forward converter can be shown in Fig. 1.3. The moduli adder is used to perform the moduli addition, for instance,

$$(2+8) \bmod 4 = 2 \quad (1.2)$$

$$(2+1) \bmod 4 = 3 \quad (1.3)$$

Fig. 1.3 Typical $\{2^n-1, 2^n, 2^{n+1}\}$ Based Forward Converter

And due to the complexity of the moduli adder especially the 2^{n+1} moduli adder, researchers *Pourbigaraz, F* [17] and *Ming-Hwa Sheu* [18] proposed their moduli

adder-free architecture of forward converter. The working principle is able to be found in their publications.

Fig. 1.4 Moduli adder-free structure of $\{2^n-1, 2^n, 2^n+1\}$ Based Forward Converter from *Ming-Hwa Sheu*

The table below from [18] helps us roughly understand the hardware cost in the proposed moduli adder-free forward converters.

**TABLE 1.3 MODULI-FREE FORWARD CONVERTER: COMPARISON
BETWEEN [17] AND [18]**

	CSHA		CSA		CPA		MUX		Correction function	
	n-bit	(n+1)-bit	n-bit	(n+1)- bit	n-bit	(n+1)- bit	n-bit	(n+1)- bit	n-bit	(n+1)- bit
[17]	--	2	2	4	1	1	--	--	--	n+2
[18]	3	--	1	1	--	--	2n+2	3n+1	n+3	2n+3

CSHA: Carry-Save Half Adder CSA: Carry-Save Adder

CPA: Carry-Propagation Adder MUX : Multiplexer

*Cost (CSHA) = Cost (CSA) / 2

1.5 Organization of the Thesis

This rest of the thesis is organized as follows: Chapter 2 focuses on the literal reviews on the pre-published ARCs. Chapter 3 analyses the similarity of RNS property and clock signal, therefore, proposes the algorithm of a new direct analog-to-residue conversion with clock overlapping. Chapter 4 describes the hardware realization of the proposed algorithm and also the simulation results. Chapter 5 concludes briefly and discusses about the possible future work.

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2 Literature Review

2.1 Introduction of Data Conversion between Analog and Digital Signal

Fig. 2.1 demonstrates how the Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) would change the characteristic of the signal.

Fig. 2.1 Signal Characteristics Changed by ADC & DAC

The original analog signal is first filtered by the Low-Pass Filter (LPF) to remove the unwanted high frequency signal that may introduce the aliasing. The output of the LPF is then sampled and held (S/H) for quantization process to convert the output to digital discrete format. After the digital signal processing, the digital signal is fed to a DAC to convert back to analog format.

2.1.1 Sample-and-Hold

A S/H circuit is critical in data converting process, it works like a camera to 'capture a moment' of the analog signal and hold the 'moment' for ADC to process. Theoretically, the value of the analog signal should be captured instantly like what is shown in Fig. 2.2.

Fig. 2.2 Ideal Sample-and-Hold

However, a certain finite period of time interval is required for the sampling to occur. During the sampling time, the analog signal may vary continuously, therefore, the real S/H waveform (Track-and-Hold) behaves like what is shown in Fig. 2.3.

Fig. 2.3 Track-and-Hold

A simple S/H circuit uses an operational amplifier (OpAmp) as a buffer, the structure is shown in Fig. 2.4.

Fig. 2.4 Simple S/H Circuit

The control signal issues the command for sampling. When S1 turns on, the hold capacitor C_H starts to accumulate the charges on the non-grounded plate until the voltage level V_+ tracks the input value V_{IN} . And when S1 turns off, V_+ holds its own value for this holding period as the charge stored on the capacitor plate has no way to discharge, so through negative feedback, V_{OUT} will be forced to be equal to the value of V_+ . Practical issues that arise in the implementation of the S/H circuits such as delay, glitches, and charge injection will not be covered in this thesis.

2.1.2 Quantization

A quantizer, is a device that performs quantization, is assumed to be memory-less and completely defined by its static input/output characteristics curve. Quantization is a non-linear process that converts a continuous input samples into a finite set of digital codes. It is uniform usually, so that a fixed level spacing (difference) exists between any 2 adjacent quantized value. An illustration of the transfer curve is shown below in Fig. 2.5.

Fig. 2.5 Transfer Curve of an Ideal 3-bit ADC

2.2 Architectures of the Analog-to-Digital Converter

ADCs may be classified into 3 major categories based on their conversion algorithms which are Serial ADCs, Flash (Parallel) ADCs and Subranging ADCs.

A high resolution ADC is generally based on serial architecture, generally, serial ADCs convert analog input into digital format one bit at a time. And the speed of serial method ranges from low to moderate.

Flash (Parallel) ADCs implements the parallel architectures where all the output digital bits are determined simultaneously in one shot.

Subranging ADCs combine both serial and parallel techniques to compromise between the two. Therefore, they are faster than serial ADCs and have higher resolution than parallel ADCs. Table 2.1 lists out the common architectures of the 3 different categories.

TABLE 2.1 DIFFERENT TYPES OF ADCs

Classifications	Architectures	Resolution (bits)	Conversion Speed (sample/second)
Serial	Single-Slope	8-14	60-60k
	Dual-Slope	12-24	10-30
	Successive Approximation	8-16	10k-1M
	Oversampled (Delta-Sigma)	12-22	10k-100k
Subranging	Two-Step	8-16	150k-10M
	Multi-step	8-16	
	Pipelined	8-16	
Parallel	Folding	6-16	1M-GHz
	Flash		

2.2.1 Flash ADC

Flash ADCs have the highest speed of any type of data converters [1-3]. As shown in Fig. 2.6, the comparator is used for every quantization level, for n -bit conversion, $2^n - 1$ comparators and 2^n resistors are required. The input is compared with each reference value generated by the resistor ladder and results in a thermometer code at the comparators' output. If the input voltage level is less than the reference value, a '0' will appear at the respective output of the comparator, otherwise, '1' will appear. The obvious advantage of this converter is the speed, however, the hardware cost

doubles with every single bit resolution increased. For instance, a 3-bit Flash converter requires 7 comparators and 8 resistors, whereas, 8-bit resolution converter consumes 255 comparators, 256 resistors in the ladder and also similar increase in power consumption, doubling with every bit increase.

Fig. 2.6 Block Diagram of a Flash ADC

Not only the area and power consumption limit the Flash ADC's resolution goes high, as the resolution goes high, the large input capacitance, switching of the comparator and the digital logic also limit the speed of the conversion.

2.2.2 Two-Step Flash ADC

Due to the limitation of Flash ADC mentioned earlier, researchers developed another type of flash converter, Two-Step Flash ADC. The block diagram of the two-step Flash ADC is shown in Fig. 2.7.

Fig. 2.7 Block Diagram of a Two-Step Flash ADC

The converter is formed by 2 separated Flash ADCs, MSB ADC and LSB ADC, as seen in Fig. 2.7. The first converter performs the coarse conversion and generates the first few Most Significant Bits (MSBs) value of the final binary code, the second converter converts the analog residue value into digital format and therefore generates the rest of the LSBs of the final binary code.

The intuitional way of seeing conversion process may be observed from Fig. 2.8.

Fig. 2.8 Conversion Process of Two-Step Flash ADC

After the input is sampled, the MSBs are generated from first converter, the result is then converted back to analog format by the DAC and subtracted from the original signal. The difference of the subtraction is amplified by the Residue Amp to $2^{n/2}$ times and then fed to the input of the second converter. This amplification increased the quantization interval and also made the 2 converters identical; the second converter generated the rest of the LSBs.

2.2.3 Successive Approximation ADC

In Two-Step Flash ADC, 2 converters can be made identical. Thus, will it be possible to use 1 single converter instead of 2 identical blocks?

If the residue analog voltage value is fed-back to the first converter instead of fed-forward to the second converter, then yes. Also, in extreme circumstances where only 1 bit determines each clock cycle, the converter may be further simplified to a comparator as seen in Fig. 2.9.

Fig. 2.9 Block Diagram of a SAR ADC

The SAR ADC basically performs the binary search algorithm, as illustrated in Fig. 2.10.

Fig. 2.10 SAR Operation Process (4- Bit ADC Example)

The MSB of the SAR is initially set to 1, while the rest bits are set to 0. This will result in the output of DAC to be 1/2 the reference or a full-scale voltage during the first cycle of conversion. The '1' in the SAR is then shifted to next position. Depending on the result of the first comparison, the MSB is set to '0' or maintained as '1'. This results in the comparison voltage (output of DAC) to become 1/4 or 3/4 of full-scale voltage. Eventually, the output of DAC will approach the input voltage level. In other words, the input of DAC (output of converter) turns out to be the binary representation of the analog input.

Due to the mechanism in the SAR conversion, the disadvantage in speed is obvious, as the number of the clock cycles needed to perform the conversion is proportional to

the number of bits needed to be converted. However, with this mechanism, the SAR conversion is still the best among current structures of conversion in terms of power saving [4-6]. By applying the charge-redistribution technique, the SAR ADC can even achieve the Figure of Merit (FOM) of 4.4fJ/Conversion-Step with 1.9 uW power consumption, 10 bits resolution and 1MS/s sampling speed[7].

2.2.4 Pipeline ADC

From Two-Step Flash ADC, instead of feeding back, the residue signal forms a SAR ADC, thus feeding forward the residue signal to more identical blocks to form a pipeline structure. Theoretically, the pipeline ADC is N-Step converter, converting 1 bit per stage. The block diagram as in Fig. 2.11 illustrates this.

Fig. 2.11 Block Diagram of a Pipeline ADC

The converter contains a 1-bit quantizer (comparator), a S/H, an analog summer and a gain of x2 amplifier for each stage.

After the input been sampled, it compares with $1/2$ of the full-scale voltage similar to that of the SAR converter. If comparator output is 1, $1/2 V_{ref}$ is subtracted from the original value, and the residue is then amplified by 2 and is passed to the next stage; if $V_{in} < 1/2 V_{ref}$, the original held value is amplified instead. Therefore, the output of comparator represents the respective bit.

The main advantage of pipeline converter is its high throughput. One conversion will be completed after N clock cycles latency. And also, this latency disadvantage's severity depends on the application.

2.2.5 Integrating ADC

The integrating ADCs perform the conversion by comparing the input signal with the reference integrated voltage level (constant ramp), and quantizing the output by a digital counter.

2.2.5.1 Single-Slope ADC

The block diagram of single-slope ADC is shown in Fig. 2.12. A counter counts the number of reference clock cycles needed when the ramped voltage at the output of the integrator reaches the input held value. The timing diagram in Fig. 2.13 further illustrates the working principle.

Fig. 2.12 Block Diagram of a Single-Slope ADC

As the DC reference voltage is applied to the integrator's input, a linear increase should be occurred at the integrator's output, at the time when it reached the V_{in} level and so for the triggering comparator to change state. The control logic will latch the value of the counter due to the states switched.

Due to the mechanism of the converter, the time signal is used as the intermediate between analog signal and digital codes. Therefore, the linear relationship between analog signal and time signal need to be governed first, in other words, the larger the input value is, the longer the time is needed to convert signal. Although, the slope of the ramp signal in the integrator may be adjusted by varying the value of the passive component like resistors, capacitors, the speed is still restricted by the highest speed that the digital circuitry can run and, of course, the resolution need to be achieved.

Fig. 2.13 Timing Diagram of Single-Slope ADC

2.2.5.2 Dual-Slope ADC

In Single-Slope ADC structures, accuracy is highly dependent on the integrator. The process variation will directly affect the slope of the ramp which leads to the inaccuracy of the conversion. The Dual-Slope structure was proposed to eliminate this problem.

Fig. 2.14 Block Diagram of a Dual-Slope ADC

Two integrations are performed in Dual-Slope ADC (Fig. 2.14) - one on the input and the other on the reference.

The working principle is explained by a 3-bit ADC example, and the timing diagram is shown below in Fig. 2.15.

The counter determines the fixed length of the first integration, 2^3 clock cycles in this example, and due to the inverting configuration of the OpAmp, the output of the integrator, V_C , will then ramp up by integrating the negative S/H input signal. After 2^3 clock cycles, the counter overflows and changes the state of the switch so as to connect V_{REF} to the integrator. A constant negative slope is therefore observed at the output of integrator.

Depending on the value of the input, V_C will be charged to various values in the fixed integration period. By quantizing the discharge time, the final digital codes are obtained.

Integrating the unknown input V_{in} for fixed time T_1 , the output of the integrator becomes :

Fig. 2.15 Timing Diagram of a 3-bit Dual-Slope ADC

$$V_{C(1)} = \int_0^{T_1} \frac{V_{in}}{RC} dt = \frac{V_{in} T_1}{RC} \quad (2.1)$$

Obviously, if only one integration is utilized, the result is highly dependent on the accuracy of resistor and capacitor.

By disconnecting the analog input and connecting the fixed V_{REF} to discharge the capacitor,

$$V_C = V_{C(1)} + V_{C(2)} = \frac{V_{in}T_1}{RC} - \frac{V_{REF}t_A}{RC} = 0 \quad (2.2)$$

And by Combining equations (2.1) and (2.2), it can be seen that

$$V_{in} = \frac{V_{REF}t_A}{T_1} \quad (2.3)$$

Therefore, the output is independent on the passive component's accuracy. Intuitively speaking, if the input signal and the reference signal are integrated (disintegrated) by the same integrator, any effect of the inaccuracy by the component is cancelled. From the timing diagram, it is apparent that the conversion time of Dual-Slope ADC is larger than that of the Single-Slope structure.

2.2.6 Oversampling ADC

ADCs can be categorized into two kinds based on sampling rate. All previously mentioned structures belong to the first category, Nyquist-rate ADC, which have sampling rate of $f_n = 2F$, where F is the bandwidth of the signal.

Traditionally, SAR ADCs or Slope ADCs are used for high resolution applications. However, trimming technique is often required to achieve high accuracy. Additionally, high speed and high accuracy integrators are needed in dual-slope structure, High performance S/H circuitry is another restriction that limits the realization of high resolution using these structures.

Therefore, the oversampling ADC is used for high resolution applications. This is because when complex and high precision-needed analog blocks are replaced by digital circuitry, the accuracy of the converter no longer highly depends on the

device matching, precise S/H or trimming. High accuracy is achieved in the system level through the appropriate feedback structure. The mathematics and principle of this will be explained later in this chapter.

2.2.6.1 Delta (Δ) Modulator

One of the main types of oversampling modulators is the Delta (Δ) Modulator.

Fig. 2.16: (a) A Delta Modulator and (b) Its z-Domain Model

A basic delta modulator which contains a low resolution quantizer and DAC, as well as an integrator is shown in Fig. 2.16a. Due to the quantization effect of the quantizer

and the memory in the integrator, it is a dynamic nonlinear system. Therefore, it is very difficult to analyse the modulator directly through mathematics.

However, by introducing a random signal E to represent the quantization noise, assuming the perfect DAC as well, the whole system is able to be modelled as shown in Fig. 2.16b.

It should be noted that, although the DAC is assumed to be perfect, there is still a delay associated with it, in z domain, modelled as z^{-1} . The integrator model is shown in Fig. 2.17.

Fig. 2.17 z-Domain Model of Integrator

From the model in Fig. 2.17

$$u + z^{-1} * v = v \quad (2.4)$$

results in transfer function of the integrator,

$$\frac{v}{u} = \frac{1}{1 - z^{-1}} = \frac{z}{z - 1} \quad (2.5)$$

therefore, the transfer function of the feedback path is $\frac{z}{z-1} * z^{-1} = \frac{1}{z-1}$ as shown in Fig. 2.16b.

By rearranging the equation,

$$U - V * \frac{z}{z-1} + E = V \quad (2.6)$$

from the Fig. 2.16b, it leads to the transfer function being

$$V = U (1 - z^{-1}) + E (1 - z^{-1}) \quad (2.7)$$

and

$$v(n) = u(n) - u(n-1) + e(n) - e(n-1) \quad (2.8)$$

in time domain.

The name delta is derived from the fact that the output is determined by the sampled input and a predicted value of that sample. The transfer function of the delta modulator can be applied to SAR structures as well, the difference lying on the sequence of the integrator(shift register in SAR) and DAC.

As the integrator is in the feedback path, any non-idealities caused by it will not be cancelled out through the feedback. Also, due to its high gain in the signal band, it will amplify the error caused by the imperfect DAC.

2.2.6.2 Delta-Sigma (Δ - Σ) Modulator

Another oversampling structure which avoids the shortcoming of the Delta Modulator is the Delta-Sigma Modulator, shown in Fig. 2.17.

Fig. 2.18: (a) A Delta-Sigma Modulator and (b) Its z-Domain Model

The same analysis applies and yields,

$$V = U + E (1 - z^{-1}) \quad (2.9)$$

$$v(n) = u(n) + e(n) - e(n-1) \quad (2.10)$$

Compared with the Delta Modulator, the output is no longer a function of the difference between a sample and its previous value, but a function of a replica of the analog input and a differentiated quantization error.

Firstly, it does not need an integrator in the demodulation circuit, as the signal is not changed in the modulation process. In addition, any nonlinearity associated with the quantizer is simply combined with the quantization error E , and is thus attenuated and noise shaped. However, nonlinear distortion introduced by DAC causes the output to not be 'shaped' and therefore limits the performance of the converter. Like single-bit quantization, techniques of digital correction or dynamic matching may be considered to overcome this problem.

2.3 Review on Residue Number System (RNS)

Before introducing some existing structures of Analog-to-Residue conversion, it is important to review the definition and some important properties of RNS first.

An integer N can be represented by the set of residues $\{r_1, r_2, r_3, \dots, r_n\}$ with respect to its 'modulus' set $\{m_1, m_2, m_3, \dots, m_n\}$, where the greatest common divisor (GCD) of $\{m_1, m_2, m_3, \dots, m_n\}$ is one. The representation is unique within the range of 0 to $(M-1)$, where the dynamic range M is defined as,

$$M = \prod_{i=1}^n m_i \quad (2.11)$$

TABLE 2.2 INTEGER NUMBERS AND RESPECTIVE RESIDUE REPRESENTATION WITH MODULUS SET {3, 4, 5}

Integer N	0	1	2	3	4	5	6	...	59	60
$m_1=3$	0	1	2	0	1	2	0	...	2	0
$m_2=4$	0	1	2	3	0	1	2	...	3	0
$m_3=5$	0	1	2	3	4	0	1	...	4	0

Table 2.2 illustrates several integer representations with modulus set $\{3, 4, 5\}$. With this modulus set, for instance, integer 59 and 6 can be represented as $\{2, 3, 4\}$ and $\{0, 2, 1\}$ respectively. This kind of remainder or residue combination also remains unique within the dynamic range, in other words, $59 \equiv \{2, 3, 4\}$ and $\{2, 3, 4\} \equiv 59$.

The most obvious advantage (at this moment) of RNS is that, a relatively large number can be represented in a set of small numbers, and the importance of this property will be illustrated in the following equations.

$$3 = \{0, 3, 3\} \quad (2.12)$$

$$7 = \{1, 3, 2\} \quad (2.13)$$

and the residue set of the above 2 numbers added up in residue number system yields,

$$\{0, 3, 3\} + \{1, 3, 2\} = \{1, 6, 5\} = \{1, 2, 0\} \quad (2.14)$$

illustrating addition,

$$3 + 7 = 10 = \{1, 2, 0\} \quad (2.15)$$

And similarly, subtraction,

$$7 - 3 = 4 = \{1, 0, 4\} \quad (2.16)$$

$$\{1, 3, 2\} + \{0, 3, 3\} = \{1, 0, -1\} = \{1, 0, 4\} \quad (2.17)$$

and multiplication,

$$3 * 7 = 21 = \{0, 1, 1\} \quad (2.18)$$

$$\{0, 3, 3\} * \{1, 3, 2\} = \{0, 9, 6\} = \{0, 1, 1\} \quad (2.19)$$

in general, addition (or subtraction) can be accomplished by simply adding (or subtracting) the small integer values, modulo their specific modulo. That is,

$$C = A \pm B \text{ mod } M \quad (2.20)$$

can be calculated in RNS as

$$c_i = a_i \pm b_i \text{ mod } m_i \quad (2.21)$$

Multiplication can be accomplished in a manner similar to addition and subtraction.

To calculate

$$C = A * B \bmod M \quad (2.22)$$

we calculate:

$$c_i = a_i * b_i \bmod m_i \quad (2.23)$$

Based on the properties discussed above, by decomposing a large integer into a set of smaller integers, a relative large calculation can be performed as a series of smaller calculations that can be performed in parallel and independently.

Also, RNS can represent negative numbers. Let us take the integer number (-198) and moduli set {7,8,9} as example. The number is converted to the moduli sets legitimate range [0, 504).

$$-198 = 504 - 198 \quad (2.24)$$

$$= 306 \quad (2.25)$$

$$= \{5, 2, 0\}_{7,8,9} \quad (2.26)$$

Hence, the RNS calculation involving negative numbers can be performed by addition.

$$-198 + 223 = \{5, 2, 0\}_{7,8,9} + \{6, 7, 7\}_{7,8,9} \quad (2.27)$$

$$= \{11, 9, 7\}_{7,8,9} \quad (2.28)$$

$$= \{4, 1, 7\}_{7,8,9} \quad (2.29)$$

The result can be verified by direct subtracting:

$$223 - 198 = \{6, 7, 7\}_{7,8,9} - \{2, 6, 0\}_{7,8,9} \quad (2.27)$$

$$= \{4, 1, 7\}_{7,8,9} \quad (2.28)$$

$$= 25 \quad (2.29)$$

The results' consistency as illustrated above shows that RNS can be used for the computation of negative numbers through addition. This is quite convenient and suitable for applications like digital filters that involve negative coefficient(s) but does not involve any subtraction units. However, it would not be easy to directly tell the sign of the number(s) they represent from the residue digits.

As mentioned earlier, it is not easy to perform the division operation in the residue domain, but this is not impossible. In order to find the quotient of division, the definition of the multiplication inverse needs to be introduced first.

The multiplication inverse r_i^{-1} of the residue r_i is defined as:

$$(r_i^{-1} \times r_i) \bmod m_i = 1, \text{ when } \text{GCD}(r_i, m_i) = 1 \quad (2.30)$$

if the modulus number $m = 7$, the multiplication inverse r^{-1} of $r = 5$ is found as:

$$(r_i^{-1} \times 5) \bmod 7 = 1 \quad (2.31)$$

$$r_i^{-1} = 3 \quad (2.31)$$

The multiplicative inverse is usually obtained by brute-force method. Only when the modulus number m is prime, Fermat's Theorem can then be utilized in determining the multiplicative inverse. This topic is out of the scope of this thesis. [1.1] provides more details about the theorem and its application in RNS.

Division is one of the main obstacles that discourage the use of RNS. It is not a simple operation in RNS. The analogy does not hold between division in conventional representation and RNS representation.

In the conventional representation, division can be represented as:

$$\frac{a}{b} = q \quad (2.32)$$

or,

$$b \times q = a \quad (2.33)$$

where q is the quotient.

In RNS,

$$b \times q = a \bmod m \quad (2.34)$$

Multiplying the multiplication inverse of b at both sides of (2.34) gives

$$q = (b^{-1} \times a) \bmod m \quad (2.35)$$

In the above equation, q is equivalent to the quotient obtained from Equation (2.32) only when q is an integer number. Otherwise, multiplying the multiplicative inverse in RNS will not be equivalent to division in conventional representation.

Take modulus number 5 as an example, if $6 \div 2$ is needed to be calculated,

$$\frac{6}{2} = q$$

$$2q = 6 \bmod 5$$

$$q = (2^{-1} \times 6) \bmod 5$$

$$q = (3 \times 6) \bmod 5$$

$$q = 18 \bmod 5 = 3$$

The key advantage of representing numbers in RNS format is that, (1) the dynamic range of each residue digit is confined to its respective modulus and its value is normally very small. (2) parallel computation can be performed among the modulus channels independently. This implies that the RNS-based operation can be implemented with relatively simple circuitry or any kind of standard cell, therefore, the speed can be increased compared to the conventional number system operation.

Another advantageous feature of RNS representation is the possibility to utilize the redundant moduli channel to realize error detection and correction in RNS based system [8], [9]. This unique RNS feature is due to the independency of the residue digits, such that the exclusion of one (or more) moduli channel (e.g. due to the detection of a faulty digit) will not destroy the integrity of the other remaining digits if the smaller overall dynamic range and lower resolution is acceptable. For example, by starting with a $\{5,7,8,9\}$ moduli set with a dynamic range of $[0, 2520)$, it is possible to remove the moduli 5 channel from the original set to form a new $\{7,8,9\}$ moduli set with reduced dynamic range of $[0, 504)$.

2.4 Architectures of Analog-to-Residue Conversion

Due to the renewed interests of using RNS in modern DSP system as mentioned in Chapter 1, researchers have worked on the direct A/R conversion and proposed

some conversion schemes [10-14] to combine the traditional ADC and Forward Converter.

2.4.1 Flash ARC

The Flash ARC structure described in [10] uses the same number of comparators and resistors for references ladder. Similarly to the ADC structure, the proposed n-bit converter needs 2^n-1 comparators and 2^n resistors. The only modification is that the thermometer code is transferred into residual digital format instead of binary digital format. Therefore, it suffers whatever a traditional Flash ADC suffers, such as the matching issue of passive components, the huge area required and also the large power dissipation. The structure proposed in [10] used only one channel to encode/decode the thermometer code by utilizing the property of RNS in which unique combinations of residues exist within the dynamic range.

Basically, the FLASH ADC combines a traditional Flash ADC with a traditional forward converter.

2.4.2 2-Stage Flash ARC

The 2-stage Flash structure [13] demonstrated below in Fig. 2.19. achieves a significant reduction in hardware complexity and power dissipation compared to the flash approach mentioned in the earlier section.

Fig. 2.19 2-Stage-Flash ARC

By defining that the analog input is within the dynamic range $[0: M-1]$, the input is compared with the base values of modulus m_i which are generated from the first resistor ladder, and this requires $\frac{M}{m_i} - 1$ comparators instead of M in the traditional structure. The digital output is then converted back to analog value through the DAC, and subtracted from the original analog input value, resulting in the output value of the Difference Amplifier (DA) to be the residue value of this mathematical division operation. If the gain of DA can be maintained at a level of $\frac{M}{m_i}$, the same V_{ref} may be applied to the second resistor ladder used in the second stage. The second stage converts the residue analog value into digital format with another m_i-1 comparators.

Therefore, the total number of comparators in this structure is $\frac{M}{m_i} - 1 + m_i - 1$.

Consider the moduli-set {15,16,17}: the traditional Flash needs 4079 comparators, whereas the 2-Stage ARC only requires 255 comparators in one channel.

However, the DAC and fixed gain amplifiers are still required in the system. The common constriction of conventional Flash structure applies to both approaches mentioned earlier, where mismatch of passive components like resistors, offset of op-amp or analog comparators limit the bit-resolution of the system. Though it is fast, the disadvantages outweigh the advantages in long word arithmetic for the RNS.

2.4.3 2-Stage SAR ARC

An architecture based on the successive approximation algorithm has been introduced in [15] and [16] for direct conversion from analog to RNS representation. The proposed architecture is shown in Fig. 2.20.

Fig. 2.20 2-Stage-SAR ARC in [15] and [16]

The proposed architecture requires two stages. Similar to the 2-Stage Flash structure, where the first stage is used to generate the base value and the second stage converts the residue into digital format.

The comparator in the traditional SAR is replaced by the DA, and the DAC is modified to have a fixed gain m_i , which is the modulus. After $B+1$ cycles, the base value is stored in the register, where B is defined as

$$B = \left\lceil \log_2 \frac{2^n - 1}{m_i} \right\rceil \quad (2.24)$$

and the analog residue at the output of DA is converted to digital form through another SAR or Flash ADC.

2.4.4 SAR ARC

Another approach based on successful approximation is proposed in [13] as shown in Fig. 2.21.

Fig. 2.21 SAR ARC

It consists of one normal DAC, one gain modified DAC, one analog summer, one comparator and one SA register.

To illustrate the operation, consider the moduli channel $\{17\}$, assume the normalized analog input is 95: then the final value stored in the register would be 00000101-1010. The first 8 MSBs 00000101 represents the base value, $(2^2 + 2^0) * 17 = 85$, whereas, the LSBs 1010 represents the residue value $(2^3 + 2^1) * 1 = 10$.

The proposed structure reduces the number of converters needed to calculate one residue number in a traditional Successive Approximation residue approach. However, variable gain Digital-to-Analog converter (DAC) and analog summer potentially introduce offset errors so as to limit the resolution of the converter.

2.4.5 Folding Approach

A conversion method based on folding circuit has been discussed in [17] as shown in Fig. 2.22.

Fig. 2.22 Structure of Folding ARC

The working principle is straightforward. Every folded point shown in Fig. 2.22 can be considered as a point where residue equals to 0, and each reference point

indicated in the Y-axis corresponds to their respective residue value threshold. In other words, this approach chops the whole input range into several sub ranges (divides the range by a certain integer number), and quantizes the value in the sub range (calculates the residue value of the division).

The major drawback of the converter is the non-linearity of the analog folding circuit itself and the large numbers of comparators involved in each modulus base channel, especially when the bit-resolution starts to go high.

Fig. 2.23 Characteristics of Folding ARC

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3 Proposed Direct A/R Conversion

3.1 Introduction

In this chapter, the proposed direct A/R Conversion scheme will be presented to the system and detailed circuit block levels.

3.2 Similarity with the Clock

The self repeating property of RNS can be easily observed from Table 2.2, where the residue number repeats itself after every fixed period. With modulus-4, for instance, the corresponding residue number sets (0, 1, 2, 3) repeat every 4 steps (integers) in modulus-4 axis. Whereas, a clock signal in an electronic gadget repeats its rising edge (or falling edge) every fixed period. Fig. 3.1 below further illustrates this similarity.

Fig. 3.1 Residue Number Compared with the Clock Signal

As the *modulus-4 clock* repeats its rising edge every cycle, if another clock, the *Basic Frequency Clock* with 4 times the frequency was introduced, the timing signal

between 2 continuous rising edges in the modulus-4 clock can therefore be quantized, as shown above in Fig. 3.1.

If the period of the basic clock is defined and correlated with one step in the modulus-4 axis as in Fig. 3.1, it can be described as 1 Least Significant Bit (LSB) in the dynamic range of the specific modulus set. The corresponding residue number of unknown X with modulus-4 is easily calculated by counting up the number of rising edges of the basic frequency clock that occurs in between the representation point of the unknown value X and its previous rising edge of the modulus-4 clock. Therefore, the residue number of X in Fig. 3.1 is 2.

The other possible residue values in modulus-4 axis are shown as:

Fig. 3.2 Corresponding Residue Values in Modulus-4 Axis

Another property of RNS is that, such as the quotient is of any interest. Previously discussed architecture, especially 2-Stage Flash and SAR approaches, computed the quotient with respect to certain modulo numbers in their respective algorithm to help

calculate the residue. However, the quotient is redundant with RNS, and it is a waste of power and silicon area, hence, the RNS is a "pseudo-direct A/R conversion".

In clock domain (axis), residue is found by clock overlapping quantization, without the need of quotients.

Fig. 3.3 Residue Value Quantized through Clock Overlapping

3.3 System Level

The system level architecture of the proposed A/R converter is presented in Fig. 3.4

Figure. 3.4 System Level of Proposed A/R Converter

It can be categorized into three major circuit blocks:

- Voltage Controlled Pulse Generator (VCPG)
- Residue Range Detector (RRD)
- Residue Quantization and Calibration Block

3.4 Voltage Controlled Pulse Generator (VCPG)

The VCPG converts the analog voltage level into a pulse signal to indicate where the 'Input X' (in Fig. 7) is located in the time domain. The well-known formulas:

$$Q = I * t = C * V \quad (3.1)$$

$$t = \frac{C * V}{I} \quad (3.2)$$

provide the linear relationship between voltage potential and time if C (capacitance) and I (current) are kept constant.

Fig. 3.5 Voltage Controlled Pulse Generator

As shown in Fig. 11, the resistor R , PMOS and op-amp resemble a relatively constant current source. The amplifier boosts the output resistance of the PMOS, allowing the current to be independent of the V_{ramp} variation through negative feedback. With a constant current charging the capacitor, the output voltage V_{ramp} increases linearly. Once V_{ramp} reaches V_{in} , the top comparator generates a pulse voltage $V_{\text{in_pulse}}$, which translates the analog V_{in} into the time domain. The other comparator emulates the top comparator to create the pulse voltage $V_{\text{FS_pulse}}$ when V_{ramp} reaches V_{FS} . Here V_{FS} is the upper limit to the input voltage range and is equivalent to the dynamic range in RNS. Although the circuit will still function if the input range is exceeded, it will cause an overflow in RNS, as the residue number combination is unique if and only if the number to be converted (input) is within the dynamic range.

The signal V_{FS_pulse} assists the final residue value calibration and will be explained later in this chapter. For every sample and hold cycle, the switch S1 will reset the charge on the capacitor.

3.4.1 Operational Amplifier (OpAmp)

The operational amplifier (OpAmp) is a fundamental block in analog circuitry, it regulates the current in the proposed VCPG circuits. Some important specifications of an OpAmp are Unit Gain Bandwidth (UGB), Open-loop Gain (A_{OL}), Common-Mode Input Range (CMR), Common-Mode Rejection Ration (CMRR), Power Supply Rejection Ration (PSRR), Output Range, Power Consumption and so on.

As the semiconductor technology scales down, it is becoming more difficult to meet all the required specifications through OpAmp design. This is also the reason why engineers and researchers begin to research and develop digital-assisted analog building blocks.

Although the proposed VCPG is highly analog at first glance, the OpAmp in this design does not deal with the input signal, which relaxes the required specification.

Fig. 3.6 OpAmp Used in VCPG

A simple 2-stage OpAmp structure is used as shown in Fig. 3.6.

3.4.2 Comparator

The latch type comparator is chosen in this structure.

Fig. 3.7 Comparator Used in VCPG

As shown in Fig. 3.7, the PMOS current source (A1 and A2) is used to reduce the flicker noise, B1 - B4 form the latch structure which provides the internal positive feedback to do the decision making, and C1 - C4 transfer the differential signal into single-ended signal.

3.5 Residue Range Detector (RRD)

The Residue Range Detector is the core portion of this proposal, as it realizes the algorithm mentioned earlier in section 3.2.

3.5.1 Frequency Divider

The frequency dividers generate different frequency clocks with respect to each modulus number. The frequency of Clock m_1 to m_n are defined as:

$$f_{clock_m_i} = \frac{f_{Reference_clock}}{i}, \text{ where } i \in \{1, n\} \quad (3.3)$$

Since only rising edges of these clock signals will be of interest, the hardware complexity of this block may be reduced as compared to the commonly used 50% duty cycle frequency divider as shown below in Fig. 3.8.

Fig. 3.8 Frequency Divider (divided by 3)

As discussed in section 3.2, the system is supposed to count the number of rising edges from the basic frequency clock that occurs between the representation point of X and its previous rising edge of the modulus n clock. However, the input X in Fig. 3.1 is unpredictable, and there is no way to determine the rising edge of the modulus n clock before knowing the pulse signal generated in VCPG.

3.5.2 The Range Detector

The solution to the problem is to count up the reference clock cycle from the rising edge of the modulus n clock until right before the pulse signal, then to count down from the pulse signal until the following rising edge of the modulus n clock. The time interval between the two signals needs to be determined first. The 'Out' signal

generated in the RRD block, as in Fig. 3.9, will be fed to the Residue Quantization block together with the external reference clock.

Fig. 3.9 Frequency Divider and RRD

It needs to be mentioned that the XOR gate used in Fig. 3.9 is used for general explanation, In real implementations, it can be replaced by an AND gate and modified to connect one input terminal of AND gate to the Q bar of the D-FlipFlop. The other terminal remains as connected to the V_pulse signal.

3.5.3 Residue Quantization and Calibration Block

Residue quantization is easily realized by a count - down binary counter and an AND gate, as in Fig. 3.10.

Out* is the output of Residue Range Detector

Fig. 3.10 Residue Quantization Block

The modulus number in the specific channel, m_i , is set as the initial value in the count-down binary counter. Hence, $\lceil \log_2 m_i \rceil$ is the number of DFFs required to construct the counter. The binary output $\{B1, B2, \dots, Bn\}$ represents the residue number in the m_i channel, and the external reset signal can be synchronized with the input sample and hold clock.

The output of the count-down counter is only valid when the initial timing of V_{ramp} matches with the rising edge of the reference clock. Otherwise, a phase mismatch (shift) of a value ϕ will appear at every clock rising edge and will be included in the quantized residue. In this case, the binary counter output is no longer the true residue value but instead, $(R_{in_pulse} + \phi)$. This problem can be avoided by the synchronization of the sample and hold clock with the reference clock. However, doing this reduces the flexibility of the system. A calibration scheme is therefore introduced to relax this requirement.

Recall V_{FS_pulse} generated by the lower comparator in Fig. 10, the V_{FS} is equivalent to the maximum number in the dynamic range of the RNS. Therefore, V_{FS_pulse} must coincide with the respective rising edge in each and every modulus time (clock) axes, in other words:

$$R_{FS_pulse} = 0 \quad (3.4)$$

This equation serves to relate voltage with time. With (3.4) being ensured, the following equations will be valid:

$$V_{in_pulse} + \varphi \equiv R_{in_pulse} + \varphi \mod (m_i) \quad (3.5)$$

$$V_{FS_pulse} + \varphi \equiv R_{FS_pulse} + \varphi \equiv \varphi \mod (m_i) \quad (3.6)$$

Therefore, (3.5)- (3.6) yields the desired $R_{in_pulse} = (R_{in_pulse} \mod m_i)$. The digital code of $(R_{in_pulse} + \varphi) \mod m_i$ and $(R_{FS_pulse} + \varphi) \mod m_i$ are generated through V_{in} and V_{FS} channel respectively.

Table 3.1 below illustrates the relationship between the desired residue value and 2 outputs from the respective counters in the modulus 3 channel. The calibration circuit can be easily realized digitally.

The above equations (3.4) - (3.6) and TABLE 3.1 can help to answer the question raised in section 3.4. As a matter of fact, the VCPG can be considered as a Voltage-to-Time Converter (VTC), as the process, threshold voltage and temperature variations in this analog block will be translated into time domain signal, in other words, φ is not only represented as a phase mismatch between 2 clock signals, but is also involved in the device mismatch error in the analog circuitry. As V_{FS} and V_{in}

channels share the same resistor, capacitor, OpAmp and PMOS, if the 2 comparators in Fig. 3.5 can be matched carefully in layout (similar amount offset), it is reasonable to conclude that, the 2 channels will inherent have the same amount of φ , and the error will be calibrated eventually.

Fig. 3.11 is the circuit realization of Table 3.1, where A_{in} and B_{in} represent the MSB and LSB of $R_{in,3} + \varphi$, and A_{fs} and B_{fs} represent the MSB and LSB of $R_{FS,3} + \varphi$ respectively. Outputs A_OUT and B_OUT are the MSB and LSB of final calibrated results.

TABLE 3.1 KARNAUGH MAP of RESIDUE VALUE in MODULUS 3 CHANNEL

$R_{in,3} + \varphi$ \ $R_{FS,3} + \varphi$	00	01	11	10
00	00	01	X	10
01	10	00	X	01
11	X	X	X	X
10	01	10	X	00

Fig. 3.11 Calibration Circuits of Mod 3 Channel

3.5.4 D-FlipFlop

The D-FlipFlop (DFF) is the core block in most digital circuitries, and is the most important factor in determining the speed of the proposed structure.

Fig. 3.12 D-FlipFlop [1]

The 9-transistor DFF with True Single Phase Clock (TSPC) technique [1] is commonly used in high speed applications. It is constructed by a P-C²MOS stage (MP1, MP2, MN1), an N-precharge stage (MP3, MN2, MN3) and an N-C²MOS (MP4, MN4, MN5) stage, in which the input data is latched by the positive transition of the clock signal.

The detailed working principle is as follow:

When CLK = 0:

If D = 1, the node y1 is pushed down to 0 as MN1 is on, and the low voltage level at node y1 will turn off MN2 resulting in y2 being pulled up to 1. As MN4 and MP4 are both turned off due to CLK = 0 and y2 = 1 respectively, QB will remain its value as both MP4 and MN4 both are off.

When CLK goes high, MP2 is turned off, y1 remains as 0 and MN2 remains off, and as MP3 is turned off as well, y2 remains as 1. Also, when MN4 is turned on, $QB = \text{NOT}(y2) = 0$.

If $D = 0$, y1 is pulled up to 1 and y2 is pulled up to 1 as well due to the turned on of MP3 and turned off of MN3 which leads to QB remaining the same value.

When CLK goes high, y1 remains 1 as MN1 is off. MN2 is turned on causing y2 to be pushed down to 0 through MN3 which results in $QB = \text{NOT}(y2) = 1$.

When $CLK = 1$:

If D changes from 0 to 1, y1 is pushed down to 0 and MN2 is therefore off which leaves y2 remaining the same value and the same for QB.

If D changes from 1 to 0, y1 will remain at the value of 1, causing no state change at the output QB.

Collectively, QB will remain its value when CLK is in the steady state 0 and will only possibly change its state when the rising edge of CLK arrives.

3.6 Time-to-Residue Converter (TRC)

Other than counter-based timing quantizer which has been explained earlier, the Time-to-Digital Converter (TDC) based timing quantizer further increases the conversion speed. The TRC exploited in this work is orientated from DLL (Delay-line Locked Loop)-based Flash TDC. The accuracy of the conventional TDC is sensitive to the time delay. And the delay of each delay cell is PVT (Process, Voltage,

Temperature) dependent, when the time delay of one LSB is scaled into Pico-second (which is the case in high speed TDC application), the TDC accuracy will be affected dramatically.

With the proposed TRC, the requirement of delay accuracy is much more relaxed. The system works with a sampling frequency of 250MHz. The three 4ns-delay cells in the moduli-3 channel contribute to a total of 12ns delay in the Delay Lock Loop (DLL) , and each phase represents a corresponding residue output.

Fig. 3.13 Three-channel TDC

Fig. 3.13 describes the three-channel TDC used in this proposal. For the first moduli-3 channel, the DLL produces three-phase clocks. These clock signals trigger the successive DFFs. Therefore the corresponding residue outputs of DFFs are generated

through this Flash-like TDC. The same comparison applies in moduli-4 and moduli-5 channels accordingly.

More detailed circuit structures of DLL are depicted in Fig. 3.14 The DLLs are all based on conventional structures, which includes a Phase Detector, Charge Pump, Loop Filter, and inverter-based Delay Line.

Fig. 3.14 Three-channel DLL

References

- [1] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62-70, Feb. 1989

4 Simulation Results and Discussion

4.1 Simulation Results

4.1.1 Counter-Based Simulation Result

Fig. 4.1 Schematic of VCPG and RRD for V_{in}

With the reference clock frequency and the full scale voltage set at 1MHz and 600mV (100mV - 700mV) respectively, using Cadence Virtuoso with Global Foundry 65nm CMOS process. Fig. 4.1 illustrates the schematic of the voltage controlled pulse generator and residue range detector of modulus 3, 4, 5 channels for input voltage. *reset* signal is used to discharge the capacitor, V_{ref} is selected to be 1V, V_{DD} is kept at 1.2V and all the digital blocks are supplied by 1V. The clock signal of Freq_div_3, Freq_div_4 and Freq_div_5 are the respective output signals from frequency dividers.

V_{in}
 V_{ramp} -----

Fig. 4.2 Simulation Results of Fig. 4.1

With the outputs of RRD, $RRD_OUTPUT_ [3-5]$, fed to the Residue Quantization block shown in Fig. 4.3 as below. The respective digital code was generated accordingly.

Fig. 4.3 Schematic of Residue Quantization Block

The Fig. 4.4 - Fig. 4.6 demonstrate the residue quantization results from modulus 3 to modulus 5 channels respectively.

Fig. 4.4 Input and Output of Residue Quantization in Modulus 3 Channel

Fig. 4.5 Input and Output of Residue Quantization in Modulus 4 Channel

Fig. 4.6 Input and Output of Residue Quantization in Modulus 5 Channel

The counting down method is used to quantize the residue value in each channel. as for illustration in modulus 3 channel, 2 pulses are quantized as '1'. (digital outputs are changing from '10' to '01' as shown in Fig. 4.4)

Fig. 4.7 below demonstrates the calibration block's simulation result. With input channel's value being '10' and full scale channel's value being '00', the final output after calibration is '10'. It matches the **TABLE 3.1**.

Fig. 4.7 Simulation Results of calibration block in Modulus 3 Channel

To summarize, Fig. 4.8 - Fig. 4.10 conclude the simulation results

Fig. 4.8 Residue vs Vin in Modulus 3 Channel

Fig. 4.9 Residue vs Vin in Modulus 4 Channel

Fig. 4.10 Residue vs Vin in Modulus 5 Channel

4.1.2 TRC-Based Simulation Result

Fig. 4.11 shows the simulation waveforms of three-channel DLL output. The time difference between the adjacent rising edge is 4ns.

Fig. 4.11 Output of the Three-Channel DLL

Fig. 4.12 depicts the simulation result of the residue output of moduli-5 channel.

The residues are in one-hot mode. From bottom to top, the square waves represent residue 0 to residue 4. These residues are equally spaced one LSB apart.

Fig. 4.12 Residue Output of Moduli-5 with One-hot Code

4.2 Discussion

Based on the initial assumption, the whole dynamic range of RNS is evenly divided into blocks with 1 clock period of reference clock signals in the time domain, in other words, 1 LSB in the voltage domain. In order to make the output (residue or binary digital) codes change from '0' to '1', 1 LSB change in the input must exist, which potentially introduces at least 0.5 LSB DC offset. However, this is not true for this structure.

The whole system can be considered as VTC-TDC, where the TDC is realized by the means of counters. Fig. 4.9 clearly shows the 2 different inputs in the time domain within 1 clock period, which is equivalent to 1 LSB in the input analog voltage domain. It is also obvious that the final residue outputs of the 2 inputs are different

due to different numbers of pulse fed to the count-down counter. This difference is defined by the position of the input pulse, whether it is in between the falling edge and rising edge of the reference clock or the rising edge and falling edge, which is just a 0.5 LSB difference in the voltage domain.

Fig. 4.13 Different Counter Input Pulse within 1 LSB

From Table 4.1 below, it is evident that the proposed direct A/R converter utilizes the least hardware components. The complexity of the analog circuitry is reduced remarkably, as both full scale and input channels share the same analog portion. Therefore, any possible mismatch introduced may be potentially cancelled in the digital calibration block mentioned earlier. Furthermore, the hardware requirement grows only logarithmically with every bit increased in resolution as $\lceil \log_2 m_i \rceil$, in terms of the number of DFFs required for frequency dividers, binary counters and calibration blocks. The drawback of the proposed system is the sampling speed, limited by:

$$f_{sample} = \frac{f_{D-FLIPFLOP}}{M} \quad (4.1)$$

where $f_{D-FLIPFLOP}$ is the maximum frequency of a single DFF in a certain process, and M is the dynamic range in the RNS. It is believed that, f_{sample} may be improved with the scaling of the process when $f_{D-FLIPFLOP}$ increases.

TABLE 4.1 COMPARISON with PREVIOUS RESEARCH PUBLICATIONS

		[1] CP	[2] AERO	[3] ICESE	[3] ICESE	[4] IETCDS	This Work
Year		1999	2004	2010	2010	2010	2011
Analog Circuitry	Approach	2 Stage Flash	2 Stage Flash	2 Stage Flash	SAR	Folding Number System	Clock Overlapping
	Comparator	$2 \sum_{i=1}^n (2^{m_i} - 1)$	$\sum_{i=1}^n m_i$	$\sum_{i=1}^n (M/m_i + m_i - 2)$	n	$\sum_{i=1}^n (m_i - 1)$	2
	OpAmp*	2n	2	n	n	0	1
	Passive Component +	$\sum_{i=1}^n (2^{m_i+1} - 1)$	>25	$\sum_{i=1}^n (M/m_i + m_i)$	0	$> \sum_{i=1}^n (m_i + 1)$	2
	DAC	n	0	n	2n	0	0
	Analogue MUX	n	n	0	0	0	0
	Folding Block	0	0	0	0	$\sum_{i=1}^n (m_i - 1)$	0
Analog Blocks Power Consumption		Unknown	Unknown	Unknown	Unknown	Unknown	127.152uW
Digital Circuitry		PLAs, Control Timing Logic, Registers, Digital Correction Logic	Encoding Blocks	Encoding Blocks	SA Register	Encoding Blocks	$3(\sum_{i=1}^n [\log_2 m_i] + 1)$ DFFs, Combinational Blocks
Digital Blocks Power Consumption		Unknown	Unknown	Unknown	Unknown	Unknown	31.952uW
Total Power Consumption		Unknown	Unknown	Unknown	Unknown	Unknown	159.104uW

* refers to Difference Amplifier, Analogue Summer	M : Dynamic Range of RNS		mi : Modulus number
+ refers to Resistor and Capacitor	n : Numbers of Modulus Channel		

References

- [1] A. P. Preethy and D. Radhakrishnan, "A VLSI architecture for analog-to-residue conversion," in *Advanced A/D and D/A Conversion Techniques and Their Applications, 1999. Third International Conference on (Conf. Publ. No. 466)*, 1999, pp. 83-85.
- [2] R. Lojacono, "An analogue to RNS converter based on RNS properties," in *Aerospace Conference, 2004. Proceedings. 2004 IEEE*, 2004, pp. 705 Vol.1.
- [3] O. Abdelfattah, A. Swidan, and Z. Zilic, "Efficient direct analog-to-residue conversion schemes," in *Signals and Electronic Systems (ICSES), 2010 International Conference on*, 2010, pp. 85-88.
- [4] D. M. Pham, A. B. Premkumar, and A. S. Madhukumar, "Reduced complexity analogue-to-residue conversion employing folding number system," *Circuits, Devices & Systems, IET*, vol. 4, pp. 30-41, 2010.

5 Another Approach (Folding ARC)

As discussed in chapter 3 and recalled the Fig. 3.2 and Fig. 3.3, the final desired residue digital representation is determined by quantizing the amount of difference between the rising edge which represents the input value and the rising edge of the nearest modulus clock, this algorithm or mechanism can be applied in voltage domain as well.

5.1 Zero-Crossing

The folding converters are based on a zero-crossing detection circuit. In order to explain folding, it is necessary to understand zero-crossing first. The main feature of folding ADC is with its internal folding sub-blocks which detects the zero-crossing of the input analog signal.

5.1.1 Single Folding Block

Fig. 5.1 A Single Folding Block

Fig. 5.2 DC Transfer Curve of Fig. 5.1

The symmetrical structure and the ideal current source, as shown in Fig. 5.1, together with equal gate voltages level causes the currents to split into equal parts and any difference in gate voltages will cause a part of the current to flow from one branch into the other. A voltage difference V_{in} causes relatively small current deviations i_1 and i_2 . As V_{in} keeps on increasing, i_1 will increase until saturated to the amount of the tail current source, whereas i_2 will reduce to 0.

i_1 and i_2 will equal only be when the differential input equals 0, and their values will change accordingly with the polarity and magnitude of V_{in} .

5.1.2 Folding Circuitry with More Folding Blocks

More folding blocks can be connected together and loaded with the loading elements, for example with resistors, as shown in Fig. 5.3.

This results in the initial value of the output as shown in Fig. 5.4.

When input voltage increases near V_1 , M1 and M2 starts to drain the according current as explained in the previous section, but without affecting the other transistors as input voltage is still far below V_2 and V_3 .

When V_1 increases to the mid-point of V_1 and V_2 , the currents flowing through R_1 and R_2 are 2 times of biased current and 1 time of biased current respectively, as the transistors M1, M4 and M6 drain all the current within their respective sub blocks, thus causing V_{on} and V_{op} to exchange their polarities as shown.

Continually increasing the input voltage beyond the operational range of M5 and M6, results in M1, M3 and M5 draining all possible current, in other words, $I_1 = 2 \times I_2$.

This causes V_{on} and V_{op} to remain at the same value.

5.2 Folding ADC

The structure of Folding ADC is shown in Fig. 5.5

Fig. 5.5 Structure of Folding ADC

There are two ADCs operating in parallel which are Coarse ADC and Folder + Fine ADC. The Folding structure requires fewer comparators compared to that in Flash structure like 2-Step converter does, and due to the parallel structure, theoretically, the sampling speed is as fast as a Flash converter can achieve.

5.3 Folding ARC

The Folding Circuit in Fig. 5.5 is used to generate the desired residue digital outputs.

The transfer curves of folding circuit is shown in Fig. 5.6

Fig. 5.6 Transfer Curve of Folding Circuit

In Fig. 5.6 the output waveform is formed by folding the input waveform 4 times, by sending the folded waveform to the Fine ADC, the LSB is determined as illustrated in Fig. 5.5.

By feeding the folded waveform to a comparator instead of the Fine ADC, the waveform becomes similar to what is shown in Fig. 5.7

Fig. 5.7 Folded Waveform and Corresponding Output from Comparator

The waveform pattern is exactly like a clock signal in the voltage domain, and the method of quantizing the residue is proposed in [1].

Fig. 5.8 Interpolated Outputs from Comparators Bank

The method of quantizing is to interpolate the folded waveform and feed the signal into a bank of comparators.

For example, in modulus-3 channel, if 3 LSB is selected as the step size of reference voltage, then the output from the comparators is shown in Fig. 5.8. For normalized input value between 0 and 1, the output digits will be '0', '0' and '1', Table 5.5 summarizes all the possible outputs.

From Table 5.1, the pattern of the comparator outputs is easily observed, the combination repeats every 6 LSB. It is not matching with the residue combination at first glance as in modulus-3 channel as the combination is supposed to repeat every 3 LSB. However, the number of same output digits from the outputs do repeat every 3 LSB. To illustrate this, for input value '1', there are two '0's and one '1'; for input value '4', there are two '1's and one '0', and it is similar for the rest of the input values.

Table 5.1 Normalized Input Value and Respective Comparators Output

Normalized Input	1	2	3	4	5	6	7	...
C1	0	0	0	1	1	1	0	...
C2	0	0	1	1	1	0	0	...
C3	0	1	1	1	0	0	0	...

By introducing two XOR gates as shown in Fig. 5.9. Two XOR gates are introduced in Fig. 5.9 resulting with D1 and D2.

Fig. 5.9 F&I-Based ARC

The outputs $D1$ and $D2$ are shown in Fig. 5.10, and their patterns repeat every 3 LSB.

These outputs will be fed to decoder or RNS-based DSP, depending on application, for further processing.

Normalized Input	1	2	3	4	5	6	7	...
D1	0	0	1	0	0	1	0	...
D2	0	1	1	0	1	1	0	...

Fig. 5.10 Outputs of XOR Gates in F&I-Based ARC

References

- [1] C. H. Vun and A. B. Premkumar, "RNS Encoding Based Folding ADC," in *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on, 2012.*, pp. 814-817.

6 Conclusion and Future Work

In this thesis, a novel direct A/R conversion scheme is proposed based on clock overlapping. The intermediate binary stage was eliminated completely. The logarithmically increase in hardware complexity and low power dissipation make it ideally suitable for low-power high resolution applications. With more research to improve sampling speed, this technique will be more viable for future high speed application.

6.1 Possible VTC & TDC Approaches

Fig. 6.1 Pulse Width Modulator with Time Quantizer

The very first approach of translating voltage domain signal against time domain signals is the use of the delta sigma modulator. Delta sigma modulators based on time domain quantizers have been demonstrated in [1]. The general idea is to quantize the output signal of the loop filter not in the voltage but in the time domain. Therefore, the voltage provided by the loop filter is converted into time intervals that are measured and quantized in TDC. A very basic VTC is a voltage controlled

oscillator (VCO) or a Voltage-to-Frequency Converter. The drawback of VCO is the linearity which limits the input voltage range of the overall system. The future possible approach discussed here circumvents the linearity issue by using a linear pulse width modulator (PWM) as a voltage-to-time converter. Fig. 6.1 shows a block diagram of the modulator. The quantizer is replaced by a pulse width modulator and a time domain quantizer.

In order to increase the speed of the whole system (as a normal delta sigma modulator is naturally low in speed), a modification needs to be made. Instead of using normal low pass modulator, a narrow band band-pass modulator may be implemented. Fig. 6.2 illustrates the difference between the two.

Fig. 6.2 Output Spectra for Low-Pass and Band-Pass Modulator

The techniques for finding the Noise Transfer Function (NTF), and Signal Transfer Function (STF) of Band-Pass Modulators along with circuit design techniques are worth further study.

The variety of TDC architectures, also, show that there is not a single TDC architecture that is suited and optimized for all applications. In fact the TDC

architecture must be optimized for specific application requirements. This is illustrated in Fig. 6.3 which was provided in [2].

Fig. 6.3 Area and power consumption of different TDC architectures

6.2 Possible Residue-to-Analog Conversion

As explained earlier in chapter 1, the residue-to-digital conversion (reverse conversion) normally causes much more area than forward conversion. Thus, if the

final RNS-based digital computation result needs to be converted into analog format for transmission or any other purpose, it will be quite suitable to apply the Residue-to-Analog converter instead of the conventional Reverse Converter-DAC based block.

A simple 3-bit Digital-to-Analog Converter (DAC) can be realized as shown in Fig. 6.4.

Fig. 6.4 A Simple 3-bit DAC

The characteristic equation of this 3-bit DAC is given by:

$$V_{out} = V_{REF} \times (D_0 2^{-1} + D_1 2^{-2} + D_2 2^{-3}) \quad (6.1)$$

In this approach, V_{REF} has been divided into 8 levels through the resistors ladder, and depending on the digital code (D_0, D_1, D_2), only one low impedance path will be formed. The corresponding analog value is therefore passed to the buffer.

Small modification can be done to form a similar Residue-to-Analog Converter (RAC), shown below in Fig. 6.5.

Fig. 6.5 A Decoder-Based RAC

Fig. 6.5 above illustrates a modulus set $\{3, 4, 5\}$ based RAC, for example, if the residue input equals $\{1, 1, 1\}$, the switches that will be turned on are controlled by $m_3(1)$, $m_4(1)$ and $m_5(1)$. According to the unique representation property of RNS, only one low impedance path is created, the second bottom path in Fig. 6.5, would pass the respective value to the buffer.

Similarly, the Analog-to-Residue conversion can be done both in the voltage and time domain, and the time domain RAC can be realized as shown below:

Fig. 6.6 A Counter-Based RAC

The counter m_i in Fig. 6.6 resets its own value every i cycles of the CLK input, and counts the modulus number in its respective channel. The output of counter in each channel then compares with the digital representation of the input residue value. Only when all channels issue a '1' (when counter output matches the input residue value), the AND gate will assert 'hold' control signal to the Ramp circuits and therefore V_{out} is obtained.

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