Experimental and theoretical study of nanotwinned copper fabricated by pulse-reverse electrodeposition for interconnect and through-silicon via (TSV) technologies

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NANYANG
TECHNOLOGICAL
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**Experimental and Theoretical Study of Nanotwinned
Copper Fabricated by Pulse-Reverse Electrodeposition
for Interconnect and Through-Silicon Via (TSV)
Technologies**

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School of Mechanical and Aerospace Engineering

2014

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Abstract

Through-silicon via (TSV) copper interconnects of varying sizes and aspect ratios are fabricated using pulse and pulse-reversed electrodeposition techniques in deep reactive ion etched silicon vias. Mechanical properties of fabricated TSV are characterized by nanoindentation. The measurements show the strong influence of electrode geometry on the properties and microstructure of copper. The impurity incorporation at current densities below and above the limiting current density is measured by the secondary ion mass spectroscopy. Strong relationship between mechanical properties and impurity incorporation in TSV is observed. The impurity influence on microstructure of copper TSV with various diameters is also studied and reported. Electron backscatter diffraction (EBSD) experiments on TSV show no preferred orientation.

In order to understand the effects of texture on formation of nanotwinned copper, experiments were conducted to evaluate the texture of electroplated copper films of varying thickness using pulse-reverse electrodeposition. It is observed that pulse reverse electroplating produced a deposit with a high volume fraction of (111) textured copper. The initial nucleation studies of copper on (111) textured sputtered gold seed layer show that initial copper grains have strong (111) orientation. Micro-Raman measurements of stress evolution in the thin copper films show the stress evolution over time.

The role of stress on (111) textured copper crystals is evaluated by first-principle calculations within the framework Generalized Stacking Fault Energy (GSFE) and twinnability. Theoretical calculations show that the biaxial stress has strong effects

on the stacking fault energies, unstable and stable stacking and twinning fault energies. It leads to the variation of twinnability in copper with level of biaxial stress. Compressive biaxial stress increases twinnability while tensile stress decreases twinnability. The electromigration reliabilities of nanotwinned copper and aluminum doped copper are also calculated. It is concluded that pure copper has better performance than Al-doped alloys.

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Chapter 1

Introduction

This chapter presents an overview of interconnect technologies used in microelectronics and microsystems packaging. Ultra large scale integration (ULSI) and three-dimensional integration technologies[1] require advanced interconnect technologies. Increasingly complex and compact fabrication technologies require a detailed understanding of the underlying physical properties of materials used in those technologies. The limitations of existing interconnection technologies and materials are discussed, along with recently discovered material which may be suitable for future interconnection technologies. Finally, the organization of the dissertation is presented.

1.1 Overview of interconnect technologies

The metals used in microelectronics and Microelectromechanical Systems (MEMS) as interconnect material are summarized in the following table. Aluminum was used as a material for interconnect metallization previously. However, it was replaced by copper interconnect technology because of its reliability issue with increasing current density. Silver is not a viable option due to its high cost. Copper is the most suitable for mass consumption as an electronic material due to its low cost and high performance. Although silver has highest electrical conductivity, its status as precious metal prohibits the applications in microelectronics which requires mass manufacturing. The use of silver in microelectronic fabrication is not a viable and sustainable solution. Therefore, copper continues to be the only sustainable solution for the micro and nanoelectronics. Due to the complicated fabrication process, the electrical resistivity of nanofabricated copper is higher than that of bulk resistivity.

Therefore, the copper fabrication process can be improved by using the novel fabrication process to produce copper with lower electricity performance.

Table 1-1: Metals used as interconnect materials in integrated circuit and MEMS due to their low cost and high performance. (Source- CRC Handbook of chemistry and Physics)

Metal	Electrical resistivity $\rho(\mu\Omega.cm)$	Applications
Al	2.7	Electrical interconnects
Cu	1.7	Low resistance electrical interconnects
Au	2.4	Electrical interconnects and electrodes in MEMS
Pt	10.5	Thermal sensors
W	5.6	First level interconnect in ICs

1.2 Copper electrodeposition for interconnect applications and nanotwinned copper

Copper is an important structural material for microelectronics and MEMS due to its excellent mechanical properties, low electrical resistivity (lowest in the table, except for silver), low cost of fabrication, etc. As the performance requirements of nanoscale systems increased, the existing interconnect technology based on conventional electroplated copper has been exploited. New materials and process technologies need to be implemented for handling increasingly complex and demanding performance of nanoscale microelectronics and MEMS components. Nanotwinned copper has recently been shown to have superior electrical and mechanical performance. It provides an opportunity to improve the performance of copper in practical applications without the need of implementing a set of whole new

technologies. However, the mechanism of its formation and reliability is not yet fully understood. This thesis deals with the nanotwinned copper interconnect technology for three-dimensional integration for emerging copper through-silicon via TSV.

1.3 Organization and scope

The present research study is focused on the analysis and characterization of copper microstructure fabricated by pulse-reverse electroplating technique for through-silicon via and other applications in micro-nano systems. Mechanical and microstructural properties of electrodeposited high aspect-ratio copper through-silicon via are evaluated by various techniques such as nanoindentation, scanning electron and ion microscopy, Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) impurity analysis and electron back scatter diffraction (EBSD).

Theoretical calculations to evaluate the twinnability of copper under stress or strain developed during electrodeposition are performed using the density functional theory (DFT). Density functional calculations provide the electronic origin of variation of twinnability under stress/strain conditions. These calculations provide insight into the electronic nature of copper's mechanical properties. They also reveal the atomic origin of reliability of copper interconnects by theoretically evaluating the electromigration/ion migration energy barriers.

1.4 Thesis organization

The thesis is organized in the following chapters as such:

In chapter 2, the literature relating to the nanostructured twinned copper including fabrication technologies, characterization technologies and associated applications in microelectronics and MEMS/NEMS technologies are reviewed. Previous theoretical studies of nanotwinned copper using molecular dynamics and ab-initio quantum mechanical calculations are also presented.

In chapter 3, the microstructural, mechanical and chemical composition studies of electro-deposited copper with constant current pulse-reverse modulation are reported. The details of experimental setup and electrochemical parameters are also provided.

In chapter 4, microstructural, surface morphology and texture studies of pulse-reverse electroplated copper foils are presented. The effects of microstructural and thermodynamics of copper are investigated by focused ion beam (FIB), atomic force microscopy (AFM) and differential scanning calorimetry (DSC).

In chapter 5, initial nucleation of copper in pulse-reverse electroplating on (111) textured sputter gold films is examined. X-ray diffraction (XRD) and energy dispersive spectrometry are used to characterize the composition and preferred orientation of copper initial nuclei on the sputter gold surface.

In chapter 6, ab-initio theory of metals from quantum mechanics together with density-functional theory is briefly described. Theoretical calculation details and results of the copper twinnability under strain are presented. Theoretical values of twinnability of copper (111) textured film under compressive/tensile strain is calculated. The experimental observation of twinning and the proposed theoretical model are also discussed.

Chapter 7 summarizes the contribution and conclusion of the work conducted in the duration of PhD research. Challenges in the TSV fabrication related issues are discussed. Future research work, which will be useful in understanding and deployment of copper TSV technology, is also presented.

Chapter 2

Literature Review

This chapter presents a comprehensive review of interconnect technologies used in the microelectronic and micro-electromechanical systems (MEMS) [2]. The emphasis is on the fabrication, applications and theoretical studies of twinned copper in the nanoscale. Copper with nanoscale twins is suitable for practical applications due to its high strength and conductivity. The atomistic origin of twinning in copper is also presented. The present state of understanding in copper twinning as deformation twinning and experimental evidence is highlighted.

2.1 Introduction

Interconnect metallization is one of the most important technologies in modern electronics and micro/nano-scale systems. The performance of interconnect plays a leading role in the successful operation of such systems in terms of electrical performance such as low resistance, low RC delay and mechanical performance such as good adhesion with surrounding environment, resistance against electromigration and stress-induced migration. Aluminum was previously used as the main material of choice for metallization. However, relatively high electrical resistance and low resistance to electromigration make the copper the next natural choice for metallization. Although silver has the lowest resistivity of all metals, it is not likely to be a choice of functional material for ubiquitous electronics micro devices due to its high cost.

Presently, copper is the main material in those applications due to its low cost and ease of fabrication and etching. Electrochemical deposition provides an efficient and economical method to produce a complex metallization system. Electrochemical phase transformation is a first-order phase transition [3] in non-equilibrium conditions.

Its phase transformation is complex and the knowledge on it is experimental. It is difficult to predict the properties of electrodeposition.

Figure 2-1: Schematic of TSV stacking technology (a) against on-chip metallization as shown in (b).

TSV technology shortens the electrical interconnection path as shown in Figure 2-1(a). Therefore, the RC delay is greatly reduced in TSV built electronic circuits. A shorter conductor gives lower electrical resistivity. The electrical conductivity of the copper in the TSV needs to be low in order for the system to achieve a high overall electrical performance. Therefore, a whole new technology for well-controlled TSV fabrication is needed for the growing integration of electronic components according to Moore's law.

Figure 2-2: (a) 3D stacked package by copper interconnects, (b) 120 μm deep TSV and (c) 80 μm deep electroplated copper filled via[4].

Figure 2-2 shows the fabricated silicon devices stacked with TSV technology from Intel Corporation. Blind-via of diameter 12 μm was etched to a depth of 70 μm by deep

reactive ion etching process, followed by copper filling in pulse-reverse plating. Copper bumps were fabricated by through-photoresist plating as shown in Figure 2-2 (b). The wafers were thinned down from the back side to expose the copper interconnects. Figure 2-2 (a) shows the stacked wafers.

2.2 Review of twinned copper

The relevant literature on the twinned/nano-twinned copper is presented. Although twinning of copper can be observed in various experimental situations, electrodeposition is the main method in the field of micro/nano-fabrication due to its reliable process. Therefore, the review of the copper with nanoscale twins will emphasize on electrochemical deposition. The ability to fabricate nanotwinned copper by electrochemical method simplifies future integration due to its compatibility with existing equipment.

2.2.1 Fabrication of twinned copper for micro/nano systems

Figure 2-3 shows the nanoscale copper twins fabricated using the pulse electroplating [5, 6]. The thickness of nanotwin lamella varies from a few nanometers to 1 μm . The nanotwinned copper shows excellent electrical properties without compromising its mechanical properties. It has advantages over nanocrystalline copper because nanocrystalline copper has higher electrical resistivity than bulk copper. Therefore, excellent mechanical and electrical properties cannot be obtained at the same time. The stability of twinned structure under mechanical loading was also proven to be high [7]. Pulse electroplating and pulse-reverse electroplating are used to produce such nanostructures in copper grains. Nanotwinned copper shows improved mechanical properties such as hardness while it retains the low electrical resistivity. Nanocrystalline copper impedes electrons at its grain boundaries inducing higher electrical resistivity.

Figure 2-3: Nanotwinned copper fabricated by pulse electrodeposition (a) TEM micrograph, (b) grain size distribution, (c) thickness of copper twins, (d-e) high resolution TEM micrograph of nanotwins [5].

Figure 2-3 shows the microstructure of copper fabricated by pulse electroplating. More recently, Zhang et al. [8] studied the microstructure and crystal texture of pulse electroplated copper. Copper was electrodeposited on the Ti/Ni seed layer in copper sulphate electrolyte solution with no additives. With focused ion beam techniques, the microstructures of the copper deposit were examined. It was reported that the microstructure of the copper was dependent on the thickness of the film. At thicknesses near the interface, finer grains were observed as shown in Figure 2-4. It was concluded that the microstructure evolution occurred during the early stage of deposition. The surface morphologies of the electroplated copper films are shown in Figure 2-5. It can be observed that microscopic twinning was observed on the plan view of the surface copper films. However, it is noted that morphologies similar to the grain structure do not necessarily represent crystallographic grain structure as measured by analytical methods such as Transmission Electron Microscopy (TEM) or Focused Ion Beam (FIB). High-resolution TEM is the most accurate method for such measurements. For measurements of grain structure, FIB is a good enough analytical method since it can reveal the grain structure of larger area.

Figure 2-4: FIB images of microstructure of pulse electroplated copper [8].

The cross-sectional pictures show the columnar structure of copper deposit. Micro and nano twinings were observed due to the low stacking fault energies of copper. The texture of the copper was shown to be (110). Strong (110) texture was correlated to the pulse electrodeposition.

Figure 2-5: (a-c) SEM and (d) TEM micrographs of copper microstructure of pulse electroplated copper[8].

Figure 2-5 shows the surface of pulse electroplated copper. Surface twins are clearly observed. However, the existence of such structure and improvement in

properties are not well established. Recrystallization and texture development may well affect the surface structure of the deposit.

2.2.2 Mechanical and electrical properties of twinned copper

Twinned and nanotwinned copper exhibit excellent mechanical and electrical properties simultaneously without sacrificing either property. Nano-crystalline (n-c) copper has excellent mechanical properties, such as modulus of elasticity and hardness. However, electrical properties of copper, such as electrical conductivity and electromigration resistance, are degraded in the case of n-c copper. The resistivity of the twin boundaries in silver was previously shown to be smaller than that of grain boundaries [9, 10]. Recent experimental measurements on copper [5] show the similar results. Therefore, the nanotwinned copper could be applied to nanoelectronics and NEMS.

2.2.3 Applications of twinned copper in micro-nano systems

Because of the excellent electrical and mechanical properties of nanotwinned copper, it is an excellent candidate for fabrication at micro and nano-scale. In many micro/nano and MEMS system applications, both excellent mechanical and electrical properties are required. For example, the MEMS micromachined inductor with metallic structure requires low electrical resistivity to reduce the resistive loss of the radio frequency (RF) power while better mechanical properties of metal are required for reliability issues such as external load and impact reliability during the service lifetime. High-aspect ratio through-silicon via copper interconnect is one of the most important technologies for large-scale integration [11] using pulse reverse electrodeposition[12], which gives advantages of reliability and strength in practical applications. Metallic micro-structures in MEMS also can use nanotwinned copper as a functional material (for example in LIGA technology). However, challenges remain in such applications,

due to the complex cathode geometry evolution during electroforming which will result in non-uniformity of mechanical properties of electroplated copper. Hence, the design and analysis of such structures are difficult.

Figure 2-6: SEM images of high aspect ratio through-wafer copper interconnects after the dissolution of silicon by KOH etching [13].

The strength of the nanotwinned copper provides a rare chance for controlling the properties of copper deposits in very small features such as TSV or on-chip interconnect. It provides many advantages in future MEMS and NEMS designs which require excellent thermal and mechanical properties of copper.

Figure 2-6 shows high-aspect ratio copper through-wafer interconnect fabricated by pulse-reverse electroplating. Void free reliable interconnect with aspect ratio of up to 10 has been achieved using the technology developed. TSV technology can be used in many aspects of micro and nanosystems such as electrical

interconnection, heat pipe in thermal applications, three-dimensional functional structures such as RF devices.

Figure 2-7: Nanoscale twins at different positions of TSV [13] (a) bottom, (b) middle, (c) top position of TSV and (d) detailed view of nano twins.

Further examinations of such microstructure using transmission electron microscopy show the high density of nanoscale twins in electroplated copper, which make them suitable in high performance interconnect technology for nanoelectronics, MEMS and NEMS. Figure 2-7 (a) shows the high density of nanoscale twinning in copper at the bottom of the through-silicon via where the low current density is used to ensure the void free filling. With the increasing current densities, the density of twinning has reduced. Higher current densities are favorable due to their shorter plating times. However, the exact nature of such phenomena requires an intensive investigation in terms of electrochemical, crystallization and recrystallization aspects.

2.3 Theoretical studies of twinned copper

Different methods have been used to study the properties of nanotwinned copper, depending on the objective of investigation. At the continuum level, numerical methods such as the finite element and finite difference methods can be used to study the response of the material to an external load. Computational plasticity can use the continuum model to predict the material response or deformation. At the microscopic scale, classical molecular dynamics and molecular statics are used to study the various properties of matter such as dislocation movement, grain boundary properties, twinning

deformation, etc. The response of the material to forces can be calculated using the millions of atoms in the computational unit cell. Although the molecular dynamics methods can be successfully used to study many properties at atomic scales, at the most fundamental level, the behavior of materials is governed by their electronic structure. Quantum mechanical methods have been extensively used to study the properties of matter such as elastic constants, optical properties and magnetic properties.

2.3.1 Quantum mechanical calculations of twinning

The properties of materials are governed by the underlying quantum-mechanical nature of atoms which are the basic building blocks of materials. Different metals and alloys have different levels of tendency to form twinings in their crystals. The developments in fundamental physics—such as Density Functional Theory (DFT) and various other methods to solve Schrodinger Equation to calculate the total energy of given material in ground state—improve the understanding of twinning of various materials including metals, alloys and semiconductors. Recently, the numerical calculations with DFT [14] show that the original copper FCC crystals have more favorable energy with twinned structured crystals than strained FCC. Figure 2-8 shows the total energy of copper of the predefined supercell with twins. It can be observed that total energy of twinned crystal is less than that of the strained FCC structure. Favorable energy is one of the methods that can be used to explain the high density twinning of copper under pulse electro-deposition.

Figure 2-8: Total energy of nanotwinned copper under strained conditions calculated by first-principle calculation method [14].

2.3.2 GSFE of metals under strained conditions

The Generalized Stacking Fault Energy (GSFE) model of metal under strained conditions is applied to calculate the behavior of metallic materials where the deformation process is by sliding of low index atomic planes [5]. Figure 2-9 shows the typical energy surface of FCC metals on (111) plane. Since (111) plane is a primary plane for sliding, its behavior is well studied and experimentally verified using various techniques such as Transmission Electron Microscopy. The magnitude of the stacking fault energies depends on the type of material and is strongly influenced by other factors such as existence of foreign species or dopant, composition of alloy, localized state of stress, etc. Its origin lies in the electronic structure of solid.

This thesis shows that the energy barrier varies with applied biaxial strain which explains the varying twinnability of same pure metal such as copper. It is important to correlate the twinnability with strain attained in the crystal since no experimental lattice is completely free of stress. This is especially true for copper electrodeposits since electrochemical phase transformation is a highly non-equilibrium process with many sources of defects in lattice such as grain boundaries, vacancies and dislocations.

Figure 2-9: A typical γ energy surface of FCC metals by translation of upper unit cell on (111) plane [15, 16].

Figure 2-10: Tight binding calculations of GSFE of various FCC metals [17].

Figure 2-10 shows the GSFE of FCC metals calculated using tight binding approximation. It shows the varying level of energy barriers and profiles for different FCC metals. The calculated energy profile has been successfully used to predict the tendency of forming twins in the FCC matrix. The prediction is in line with the results of the experiments. However, this theoretical calculation reflects the ideal bulk material conditions. In reality, localized conditions such as high stress/strain or dopant or grain boundaries affect the GSFE and therefore twinnability. As such, detailed calculations for each situation are required.

Figure 2-11: Supercell used to calculate GSFE under strained conditions[16].

Figure 2-11 shows the computation unit cell used in previous studies to calculate the GSFE of FCC copper under isotropic volume strain and simple shear strain conditions. The previous investigation was conducted to study the effect of shear strain in $[-1-12]$ on (111) plane on bonding angles of the atoms. It should be noted that the choice of supercell and type of strain applied to it provide different numerical values corresponding to different situations. Surface relaxation at the first few atomic layers affects the calculated theoretical values such as twinnability and GSFE. The details of such information are not yet available in the current computational/theoretical literature. Such details of theoretical parameters are needed for understanding the physical phenomena observed in the electroplated copper. The calculations of these parameters are especially important in the case of copper since it is important for the practical application of microelectronic and nanoelectronics devices. Copper has second-most highest electrical conductivity after silver, which is an expensive precious metal.

Figure 2-12: GSFE curves of Al, Cu and Ni as a function of isotropic change in unit cell volume (changes are given as percentage), NM=nonmagnetic, FM=ferromagnetic in case of Ni[15].

Figure 2-12 shows the GSFE as a function of isotropic volume change for Al, Cu, Ni with the volumetric strain ranging from -2.9 to 3.8 percent. It is clear that the height of energy barriers is a strong function of strain.

Figure 2-13: GSFE curves of Al, Cu and Ni as a function of superimposed volume conserving shear strain, NM=nonmagnetic, FM=ferromagnetic in case of Ni[15].

Figure 2-15 shows the GSFE curves of volume conserving shear strains in $[-1 \ -1 \ 2]$ direction on the (111) plane. For Al and magnetic Ni, the stacking fault energies increases as the shear strain increases, and the unstable stacking faults energy decreases as the shear strain increases.

Figure 2-14 Unstable stacking fault energies, stable stacking fault energies(a) and their ratios(b) as the function of isotropic volume changes given in percentage, NM=nonmagnetic, FM=ferromagnetic in case of Ni[15].

Figure 2-15 Unstable stacking fault energies, stable stacking fault energies(a) and their ratios(b) as the function of volume conserving shear strain, NM=nonmagnetic, FM=ferromagnetic in case of Ni[15].

Figure 2-16 Local density of states of the atom on the slip plane for (a) Al and (b) Cu(FCC=equilibrium face center cubic, USF=Unstable stacking fault configuration, SF=Stable stacking fault[15].

Figure 2-16 shows the density of states (DOS) of the FCC configuration, unstable stacking fault configuration and stable stacking fault configuration of both aluminum and copper. Although the DOS curve has spikes which is due to broken periodicity in the supercell, the DOS shows the square root form of free electron gas with only Van Hove singularities near Fermi energy in the case of aluminum. For copper, d-band dominance can be observed. It is clear that the atom-projected DOS

shows minimal modification to the DOS structure of the bulk for both copper and aluminum.

2.3.3 Molecular dynamics studies of twinning deformation

Molecular dynamics uses the classical equation of motion of individual atoms to compute the forces and motion of the material systems. The electronic nature of material is approximated with the suitable potential function to describe the interaction between the atoms. With state-of-the-art computational facilities, material systems with millions of atoms can be studied numerically. This makes the technique of molecular dynamics suitable for the study of phenomena such as dynamics of dislocations, grain structure, grain boundary-twin boundary interaction and phase changes. However, it does not explain material behavior in terms of electronic origin/structure.

2.4 Impurity incorporation during electrodeposition

Impurities play an important role in electrodeposition. In fact, electrodeposition is the science of application of defects to fabricate and manufacture the deposit with required physical properties. However, the study of impurities and their role on copper microstructure is not well studied due to its experimental cost. Mass spectroscopic techniques such as secondary ion mass spectroscopy (SIMS) found their application in industrial materials such as copper to study the details of impurity incorporation.

shows the level of species measured by SIMS from the sample fabricated with standard sulfuric acid based electrolyte [18]. Compared to vacuum technique such as sputtering or electron beam evaporation, electrodeposition produces copper with higher density of twins largely due to impurity incorporation. In vacuum technique, the chamber is relatively clean with only the sputtering medium inert gas such as nitrogen. However, in electrodeposition, additives used to control the deposition act as impurity species. These impurities species are large organic molecules to initiate a new

nucleation sites during deposition leading to more complex structure evolution in copper.

Table 2-1: Impurity contents of copper electrodeposits by standard electrolyte [18].

Impurity species	Experimentally measured content
Carbon	$2 \times 10^{19} \text{ cm}^{-3}$
Chlorine	$2 \times 10^{19} \text{ cm}^{-3}$
Oxygen	$8 \times 10^{18} \text{ cm}^{-3}$
Sulfur	$8 \times 10^{18} \text{ cm}^{-3}$
Nitrogen	$1 \times 10^{18} \text{ cm}^{-3}$

2.5 Characterization techniques

Various characterization methods to measure the microstructure and composition of deposits in the context of material analysis for copper TSV are briefly reviewed in this section. Advantages and disadvantages of each characterization technique are discussed in the context of microstructure examinations specific to TSV technology. Different methods are used to characterize the microstructural properties of TSV in this thesis.

2.5.1 Scanning Electron Microscopy (SEM)

SEM is used to observe the microscale structure and microstructure of fabricated copper through-silicon vias (TSV). It can be used to observe the morphology and possibly grain size of the samples, although measurement of grain sizes using SEM does not always provide accurate solutions. Secondary electron images in SEM may provide better grain contrast if the surface of the sample is clean and free of defects.

2.5.2 Atomic Force Microscopy (AFM)

AFM is used to study the morphology of the electroplated copper. It can be used to measure the grain size if the proper etching of the grain boundary has been achieved

on the samples. However, in ultrafine-grain copper crystals, such usage may be limited. It is a useful characterization method to measure the initial nucleation of copper and surface morphology.

2.5.3 Focused Ion Beam (FIB)

FIB uses the ionized gallium (Ga) beam to irradiate the material. Since different orientations of the metals have different contrasts to ion beam, FIB can be used to characterize the detailed microstructure of the copper. Microstructural features such as grain boundaries and twins can be easily observed in FIB [19] with features as small as 60 nm. Because it is a destructive characterization method, FIB can be used to etch the material with high precision to cut the sample out of bulk material for TEM examinations. The FIB technique provides the imaging of the microstructure of copper at the precise position in TSV. It easily allows detailed examination of microstructure at different locations of TSV.

2.5.4 Electron Backscatter Diffraction (EBSD)

EBSD is a technique to measure microstructure and orientation with great precision. The incident electron wave is diffracted by the lattice which acts as grating. The diffracted patterns can be captured on the phosphor screen as Kikuchi bands with each band associated with a particular Miller index plane of the crystal. The Kikuchi pattern from every point in the scanning area is recorded to reconstruct the grain and orientation mapping on a post processing system. It can be used to measure the orientation of individual grain and texture in case of large area scanning. If it is carefully applied with in situ etching, it provides the three-dimensional microstructure of crystalline materials. The ability to measure the texture at selected regions in TSV makes EBSD a valuable tool to study the localized texture at different regions. By analyzing the diffraction pattern, the localized stress within and around the grain can be measured.

2.5.5 X-ray diffraction (XRD)

X-ray diffraction is used to study the orientation, lattice size, phase identification, texture and stress determination. In electrodeposition, XRD is an important tool to analyze the vast majority of properties such as recrystallization, texture and volume fraction of its components, residual stress and grain size. However, the use of XRD is limited to large sample sizes such as blanket electroplated copper thin films. For the smaller samples with localized properties, EBSD gives more detailed information on individual grains.

2.5.6 Secondary Ion Mass Spectroscopy (ToF-SIMS)

In ToF-SIMS, the sample surface is bombarded with energetic ion beams to remove chemical species from the surface. The mass of the detected species is analyzed in the mass spectrometer. The advantage of using SIMS is that the ultra-low level of impurity species at PPM level can be detected, while techniques such as XPS and AES are limited to a few percentage of the content. In the present work, ToF-SIMS is used to analyze the impurity incorporation and segregation in electroplated TSV. It provides a powerful analysis to control the impurity levels for process optimization in electrochemical deposition of copper in high-aspect ratio TSV. With proper calibration, the quantitative measurements of contents of every species can be identified. However, even without such detailed calibration, the analysis can still be used to measure the relative concentrations of species at different locations across the TSV specimen.

2.6 Conclusions

A brief survey of the relevant literature on copper interconnect technology is presented in this chapter. It can be concluded that nano-structured microcrystalline copper with nanoscale twin boundaries is a possible candidate as the next generation of interconnection material in micro/nano-scale devices. However, a detailed understanding of such materials has not been achieved in terms of fabrication and

material properties. Since pulse and pulse-reverse electrodeposition provide the copper deposit with excellent mechanical and electrical properties, the emphasis of the present thesis will be the microstructural aspect of pulse-reverse electrodeposited copper. Primitive investigation suggests that the deformation twinning-like mechanism involves copper. However, the role of impurity incorporation is still not well understood, especially the high aspect ratio through-silicon via fabrication where complicated phenomena are involved.

Review of the theoretical considerations in twinning of copper shows that the electronic structure aspect is missing from theoretical calculations under stress/strain conditions. The effect of strain and stress on the twinning of copper will provide thorough insight into the twinning deformation process. This is especially important in future, when twinned metals such as nano-twinned copper come into technological applications as reviewed in the present chapter. This calls for detailed theoretical analysis of the twinning process at atomic/electronic scales using principles of quantum mechanics which is currently a state-of-the-art approach in understanding the properties of materials via their electronic origin.

Chapter 3**Microstructural and Mechanical Characterization of Pulse-reverse Electrodeposited TSV**

This chapter presents the electrochemical and microstructural studies of pulse-reversed electrodeposited copper in deep reactive ion etching (DRIE) etched through-silicon vias. Current distributions in the electrodeposition are discussed because of their practical importance to speedy electrodeposition with desirable microstructure and properties. The pulse-reverse or pulse electrodeposition technique can enhance the limiting current density under which the void free electrodeposition can be achieved. The experimental fabrications with different current densities are studied and discussed. The void formation and microstructural aspects of TSV are investigated. Impurity species play a key role in the electrochemical deposition achieving fine grain and void free deposit. The incorporation of these impurity species has strong effects on the properties of copper. The localized impurity levels in TSV are measured using the time-of-flight: secondary ion mass spectroscopy. After three years of storage at room temperature, localized grain growth is observed in the electroplated copper TSV. The important species such as carbon, chlorine and sulfur are measured. The local dependent concentration of such species, localized contamination and impurity segregation are observed in the TSV. The orientation and grain size are measured by the electron backscatter diffraction.

3.1 Current distribution model for a rotating-disk electrode

Current distribution is important in every electrochemical system, since it is related to the reliability and quality of a product. For this experiment, a rotating disk electrode model is the most appropriate model due to the geometry of electroplating setup used to

fabricate the TSV in wafer level. Distribution of current and other electrochemical phenomena such as forced convection and buoyancy induced convection have strong effects on the electrochemical growth of the deposit crystals [20], especially electrochemical growth in the small feature sizes such as sub-millimeter scale, which is still under active theoretical and experimental investigation. The charge distribution for plating systems as shown in Figure 3-1 is governed by the following equation [12] :

$$\frac{\partial C}{\partial t} + v_r \frac{\partial C}{\partial r} + v_z \frac{\partial C}{\partial z} = D \frac{\partial^2 C}{\partial z^2} \quad (3-1)$$

With the boundary conditions:

$$C = C_b, r \geq 0, z \geq 0 \text{ at } t = 0 \quad (3-2)$$

$$C = C_b, r^2 + z^2 \rightarrow \infty \text{ at } t > 0 \quad (3-3)$$

$$-D \frac{\partial C}{\partial z} = \frac{j}{nf}, z = 0 \text{ for } 0 < r < r_0 \text{ at } t > 0 \quad (3-4)$$

$$\frac{\partial C}{\partial r} = 0, r = 0 \text{ for all } z \text{ at } t > 0 \quad (3-5)$$

where C is concentration of copper ion, j is current density, D is the diffusion constant,

Figure 3-1: Schematics of rotating disc electrode with wafer holder mounted on cathode electrode of electrodeposition system.

F is Faraday's Constant, n is the number of electrons, t is time and r is the radial coordinate.

3.2 Electric double layer and overpotential

When a metal is in contact with an aqueous solution containing its salt, there will be an exchange of ions between the metal's surface and the solution's surface. A potential difference is formed due to the transfer of electrons from the electrode and the simultaneous transfer of ions from the electrolyte solution.

3.2.1 Surface activation overpotential and concentration overpotential

The driving force required for the electrode reactions is the surface potential, and it is the only overpotential that contributes to the charge transfer reaction at the surface. The current density depends on the surface overpotential and the composition of solution at the electrode surface. For first-order metal ion reactions of the type[12]:

The Faradaic current density i_f at the electrode is related to the electrode surface overpotential η_s by Butler-Volmer equation as:

$$i_f = i_0 \left(\frac{c_s}{c_\infty} \right)^\gamma \left\{ \exp \left(\frac{\alpha n F}{RT} \eta_s \right) - \exp \left(\frac{\beta n F}{RT} \eta_s \right) \right\} \quad (3-7)$$

In this equation, i_0 is the exchange current density of reaction, C_∞ is bulk concentration of M^{n+} ions, c_s is concentration of M^{n+} ions at the electrode surface, α and β are anodic and cathodic transfer coefficients, n is number of electrons transferred, F is Faraday constant and γ is kinetic parameter.

The difference in concentrations at the electrode surface from that of bulk solution leads to a potential difference called concentration overpotential (η_{conc}). For a metal/metal ion system, it can be expressed by the Nernst relation as[12]:

$$\eta_{conc} = \frac{RT}{nF} \ln \left(\frac{c_s}{c_\infty} \right) \quad (3-8)$$

In this equation, c_s is the concentration of ions at the electrode surface and c_∞ is the concentration of ions in the bulk solution. As will be seen in the following studies, concentration has a strong effect on the fabrication of TSV over limiting current density. And it subsequently affects the reliable fabrication of TSVs.

3.2.2 Current uniformity

In electrodeposition, the amount of mass deposited on the electrode depends on the current density which is a function of space and time at the electrode surface. Variations in current density will result in the non-uniformity of deposit which leads to poor performance in the copper electrodeposits [21].

3.2.3 Primary current density

The primary current density is the current density in the electrochemical system without any polarization such as polarization across the electrodes. Therefore, the primary current distribution is solely the function of geometry of the electrochemical systems under consideration [12].

3.2.4 Secondary current density

The current distribution in the electrochemical cell is affected by the polarization of the electrode surface. Adsorption of organic additives on the metal electrode surface will limit the area for electrochemical reactions to take place. Other causes of polarizations are: reduced concentration of ions from the bulk electrolyte in the thin diffusion layer under very high current concentrations and the evolution of hydrogen bubbles. Secondary current distribution normally polarizes the electrode in opposite directions with respect to primary current distribution. The use of additives can enhance the adsorption of these species onto the area with higher current density,

thereby blocking a portion of area to reduce the local current density. Therefore, the local current density across the electrode will be uniform. Various organic additives had been used as the leveling agent in electrodeposition during the investigation.

3.2.5 Tertiary current density

When the current distribution is in the tertiary current distribution region, the mass transfer controls the current, i.e. the mass transfer is limited by the concentration in the region of electrolyte near to electrode [12].

$$I_{lim} = \frac{nFD(c_b - c_s)}{\delta} \quad (3-9)$$

In this equation, c_b and c_s are concentrations of ion in the bulk electrolyte and at the surface of electrode and δ is the thickness of diffusion layer. Therefore, the thickness of the diffusion layer is important in electrodeposition. The mass transfer in very high current density region can be enhanced by agitating the electrolyte solution near the electrode to reduce the concentration gradient, which leads to a larger diffusion layer thickness.

3.3 Pulse-reverse electrodeposition

The applied external current to the electrochemical system during electrodeposition affects the finished electro-deposit. One of the benefits of the pulse-reverse current modulation is the replenishment of the depleted region of electrolyte with ion dissolved from the cathode during the cathodic cycle of the deposition. Previous experiments and calculations showed significant improvement in limiting current density with the use of pulse-reverse electroplating. In through-silicon via applications, it was previously found that the pulse-reverse modulation provided the void free filling of high aspect ratio trenches [22] with excellent electrical and mechanical properties [13]. Although there were theoretical modeling analyses of

pulse-reverse mass transport in electrodeposition [23] in the past, research into the electrochemical crystallization phenomenon is still at the experimental stage.

Figure 3-2: Wave form of applied current in pulse reverse electrodeposition.

Figure 3-2 depicts the pulse-reverse waveform applied from the power supply during the experiments carried out in the duration of this thesis.

3.4 Limiting current in pulse-reverse electrodeposition

Limiting current is an important factor in the electrodeposition. When the limiting current density is exceeded, electroplating ceases to occur and generates hydrogen instead, due to the depletion of copper ions for electrochemical crystallization. It depends on many factors such as geometry of plating cell and electrodes, and there are theoretical models available in the literature. Experiments can be conducted to measure the limiting current as well for a given playing system. Therefore, it is important to understand the limiting current and to speed up the fabrication while avoiding the situation where hydrogen bubbles are generated and trapped in the deposit, which leads to copper deposits with pores. The ability to minimize the production time for TSV requires higher plating rate without risking the quality of copper deposit.

3.4.1 Theoretical model

The theoretical model [24] proposed previously for the limiting rate in pulse-reverse plating can be described as:

$$\frac{i_{pr-l}}{i_{dc-l}} = \frac{1}{1 - \frac{8}{\pi^2} \left(\frac{r-1}{1} \right) \sum_{j=1}^{\infty} \frac{1}{(2j-1)^2} \frac{e^{[(2j-1)^2 a \theta_2]}}{e^{[(2j-1)^2 a] \theta - 1}}} \quad (3-10)$$

In this equation, r is the ratio of forward and reverse current densities, a is a diffusion parameter and θ and θ_2 are total and reverse cycle durations.

The diffusion parameter a is given by the equation, $a = \frac{\pi D}{4\delta^2}$. The limiting overall plating rate in direct current is given by $i_{DC} = -nFD \frac{c_0}{\delta}$, where c_0 for the present case is 0.16021 mol/liter, $D = 10^{-5} \text{ cm}^2/\text{sec}$ and $\delta = 0.01 \text{ cm}$ and $n = 2$ for copper and F is the Faraday constant. The limiting current density in direct current (DC) is about 30 mA^{-2} . The diffusion thickness is larger in the present case of the stirred solution due to its deep trenches (Aspect ratio up to 7). Therefore, the current densities of 20 mA^{-2} and 40 mA^{-2} are chosen for our experimental investigation.

Since the ratio of the limiting rate of deposition in pulse reverse (PR) mode to that of DC is always less than one, the limiting current density for PR is less than that of DC. Since the reverse cycle is small compared to forward (cathodic) current, the ratio is approximately one. The experiments are designed to observe the maximum plating speed with reliable copper filling. This is a requirement for the practical applications of TSV where plating time is directly related to the cost effectiveness of the technology. Optimal choice of electrochemical parameters and conditions is required for successful realization of TSV design integration process. Since the direct measurement of flow velocity is almost impossible in small TSV, finite element analysis is used to calculate the electrolyte velocity near the vicinity of trench.

Figure 3-3: Finite element simulation of velocity profile in narrow TSV blind holes.

Figure 3-3 shows the close view of finite element simulation results of electrolyte fluid flow velocity in the narrow blind hole of TSV of $60\ \mu\text{m}$ diameter. It shows that the applied agitation of wafer holder does not provide the effect of stirring in conventional surface plating. Therefore, the diffusion layer of the TSV plating is expected to be thicker than the well agitated surface plating. Only two dimensional simulations are done to reduce the complexity of the calculations. The inlet (from left of diagram) and outlet (right of diagram) are 1 mm away from the blind hole to ensure fully developed flow. The characteristic dimension of finite elements is chosen to be $2\ \mu\text{m}$ to ensure that no significant error is embedded into the solution due to the rough computational mesh for finite elements.

3.5 Experimental setup

All the fabrications of TSV were carried out in a custom-built electroplating set-up. The following section describes the schematics diagram of the plating setup. The electrolyte is pumped from the bottom of the electrolyte tank towards the rotating wafer holder. The wafer holder and copper anode electrode are placed parallel to each other to ensure the uniformity of the current. The solvable copper anode is made from commercially pure copper plate with the thickness of five millimeters.

3.5.1 Electroplating setup and details of electrolyte

For the fabrication of through-silicon vias, the copper electrolyte supplied by the ATOTECH Ltd. (Germany) was used. The electrolyte bath is specially designed for the filling of microstructure such as deep trenches and small features. It consists of three components: solution containing copper sulphate, sulfuric acid, hydrochloric acid and propriety additives (brightener and leveler) as shown in Table 3-1.

Table 3-1: Chemical composition of the electrolyte.

Component	Optimum value	Working range
Copper	35 g/L	32-38 g/L
Sulphuric acid	170 g/L	140-190 g/L
Chloride	50 mg/L	40-60 mg/L
Leveler	15 ml/L	4-17 ml/L
Brightner	10 ml/L	4-13 ml/L

The composition of the electrolyte solution is checked regularly, before each experiment, to ensure that accurate levels of each component in the solution are maintained across different processes.

Figure 3-4 shows the schematics of the electroplating setup designed and used in the present work. The fountain type plating tank is constantly pumped with the electrolyte from the inlet channel near the copper anode electrode. The flow is streamed towards the rotating wafer. Figure 3-5 and Figure 3-6 show the assembly of wafer holder. The wafer is connected to a current source via a ring electrode to ensure a uniform electric field across the wafer. Ring contact is used to ensure that potential

field distortion which usually is due to complex point or pin contact, does not exist in the experiments.

Figure 3-4: Schematics of electroplating setup for wafer level deposition.

A detailed description of the electrode configurations for the electroplating systems is needed because experimental results of the deposition process are strongly affected by differences in the designs of the plating system. The electrical contact around the perimeter of the wafer ensures proper electrical potential distribution across the wafer as shown in Figure 3-5 and Figure 3-6. The use of point contact in convention electrode (wafer holder) design is prone to process errors due to the reliability of point contact points. Improper electrical contact creates potential distribution across the electrode surface, making the process very difficult to control and monitor and gives rise to highly non-uniform copper deposits on cathode. In the present work, a thick layer of sputtered gold is used to ensure that ohmic potential drop across the gold thin

film area is minimal. This helps to ensure the uniform electroplating across the wafer eliminating the effects due to potential drop in sheet resistance of seed layer. A rubber sealing ring is used to enclose the wafer properly, so that electrolyte does not contact with contact rings and back of the wafer.

Figure 3-5: Schematics of wafer holder with detailed assemblies showing the electrical contact to seed layer of wafer.

Figure 3-6: Schematics of wafer holder for electroplating.

Figure 3-7 (a) and (b) shows the photos of electroplating setup and automated agitation methods. Rotational and lateral agitations are used during the plating process

to ensure the uniformity of copper across the wafer. The machines are designed and built in house specifically for TSV fabrication research projects. The applications of the fabrication include TSV, through-photoresist electroplating for on-chip interconnects and RF devices such as inductors, filters and transmission lines.

Figure 3-7: (a) Electroplating setup used for TSV fabrication showing, (b) the rotational and lateral agitation mechanisms.

Schematics of the fabrication process for through-silicon via (TSV) interconnection are shown in Figure 3-8. Two separate wafers, a device wafer and support wafer, were used for TSV fabrication. The device wafer, a $\langle 100 \rangle$ p-type silicon wafer with a resistivity of $0.10 - 10 \Omega\text{cm}$ was used for fabrication. The thickness and diameter of the wafer were $450 \mu\text{m}$ and 100 mm respectively. Photolithography was carried out on the device wafer using the pattern for TSV with the diameters ranging from 60 to $150 \mu\text{m}$. The positive photoresist (AZ9260) layer with

a thickness of $10\ \mu\text{m}$ was spun-coated on the polished side of the wafer at a spinning speed of 1500 rpm. The exposure was performed in MA6 mask aligner for 55 seconds at the energy intensity of $10\ \text{mJ}/\text{cm}^2$. A thin layer of aluminum with a thickness of 20 nm was deposited on the back side of the wafer to obtain a smooth profile. The through-wafer trenches were fabricated by deep reactive ion etching (DRIE) [25] after bonding the device wafer to a carrier wafer with the photoresist.

A support wafer with a thickness of $450\ \mu\text{m}$ was used. A photoresist layer of $5\ \mu\text{m}$ thickness was used in order to remove the device wafer after TSV fabrication. A thin layer of photoresist is desirable due to its stability while developing the bonding photoresist layer in the later stage. After coating the photoresist, the support wafer is coated with a 20 nm chromium layer (adhesion layer) and 200 nm gold layer (seed layer for electroplating) in the sputtering process without breaking the vacuum.

After the sputtering process on the support wafer, the oxidized device wafer with through-holes is bonded on the support wafer with a $5\ \mu\text{m}$ thick photoresist (AZ9260). During the pre-baking, the temperature is set to $80\ ^\circ\text{C}$ to avoid the cracking of the gold seed layer underneath with the longer baking time of 10 minutes. The photoresist was exposed in MA6 mask aligner with a blank glass mask with no pattern for 60 seconds. After exposure, the photoresist was developed in AZ400 developer in ultrasonic condition for 60 seconds to ensure the clean development of photoresist layer which is essential for bottom up plating. Longer exposure to ultrasonic condition affects the stability of photoresist layer on the support wafer. After developing in ultrasonic condition, the wafer was soaked in the deionized water for five minutes to disperse the photoresist particles in the solution since a single monolayer of polymer remaining on the gold seed layer will block the plating process. Blocking of a portion of plating area will increase the current density of the remaining area, causing void

formation at the core of TSV if the current density goes beyond the limiting current density. Therefore, the complete removal of photoresist is important as it ensures that the cathode surface area is exposed to the electrolyte solution.

Figure 3-8: Fabrication process of through-silicon via by bottom up plating.

After electroplating, the bonded wafers are separated by dissolving the intermediate photoresist layer between two wafers. Ultrasound agitation can be used to speed up the separation process.

3.6 Experimental results and discussion

This section presents the experimental results of copper electroplating. The electrochemical parameters used in the fabrication process are as shown in Table 3-2.

Table 3-2: Electrochemical deposition parameters for copper TSV electrodeposition.

Cathode	Silicon wafer
Anode	Copper plate
Cathodic current density	20 – 40 mA/cm ²
Anodic current density	60 – 80 mA/cm ²
Pulse time	2 sec (Cathodic) 0.1 sec (Anodic)

Figure 3-9: Cross-section SEM picture of TSV with diameters ranging from (a) 60, (b) 80, (c), 130 and (d) 150 μm .

After electroplating is finished, the samples are cut into small pieces and molded in the epoxy resin for further investigation of their properties. Figure 3-9 shows the cross-section of TSV fabricated at a low current density of 20 mA/cm^2 . The void free deposition of copper throughout the length of the TSV with a diameter ranging from 60 to 150 μm has been achieved. It should be noted that TSV with various diameters are simultaneously on the same wafer. This shows that pulse-reverse electroplating can be used to fabricate copper structures of various dimensions at the same time with very good uniformity. It is a great advantage to have the ability to fabricate various dimensions of high aspect ratio structures because in MEMS most of the structures have varying physical dimensions. The amount of over-plated copper is acceptable in modern polishing processes for further processing of the wafer.

Figure 3-10: SEM picture of (a) plan view, (b) magnified view of 80 μm diameter TSV.

SEM picture in Figure 3-10 shows the surface morphology of TSV fabricated with pulse-reverse electrodeposition. It is shown that fabricated TSV does not go through the excessive grain agglomeration as reported previously [26] using simple direct current modulation electroplating. Further improvements and optimizations in wafer holder design will provide larger control over the uniformity of copper deposition.

3.7 Microstructure of TSV in constant current pulse-reverse electrodeposition

The FIB technique is used to characterize the microstructure of the electroplated through-silicon via. The electrolyte chemistry and geometry of the interconnection have effects on grain sizes and reliability of the electroplated copper [27]. The electroplated copper with a diameter of 60 μm was analyzed two weeks after the fabrication process was finished to measure the stable grain structure after self-annealing. Figure 3-11 shows the positions of the cross-section for analysis. Figure 3-13(a) and (b) show the FIB image of copper at the bottom of the pillars. The diameter of the grain size is less than 1 μm . No void or pore was observed in the analysis. It can be seen from the figure that the grain structures of copper are randomly oriented and no apparent structure, such as columnar shapes, has been observed. Figure 3-13(c) shows the magnified SEM

image of the FIB etched surface. Copper twinning with widths of hundreds of nanometers can be observed.

Figure 3-11: SEM picture of cross-sectional view of TSV with 60 μm diameter showing the location of microstructural examinations.

Figure 3-12 shows the equivalent circuit diagram of the copper electroplating cell for TSV with various diameters. The power supply provides a constant periodic current. The resistance of the electrolyte is given by

$$R = \frac{\rho l}{A} \quad (3-11)$$

where ρ is the resistivity of the electrolyte, l is the length of the electrolyte tank and A is the cross sectional area of the electrolyte container. The resistance consists of two components, which are due to the bulk of the electrolyte being far away from the cathode and individual pillars. Since the resistances of the individual pillars are far larger than those of the bulk electrolyte, the potential drop across the individual pillars plays the dominant role. The various diameters of through-holes have different resistances during the electroplating process. Therefore, the pillars with larger

diameters have lower resistances, thereby inducing a higher local current, which explains the variation of measured hardness and Young's modulus values across the wafer with different diameters of through-silicon vias.

Figure 3-12: Equivalent circuit of electroplating system with cathode with various via for plating.

Such variations in electrochemical circuits have direct implication on the electrocrystalliation of copper such as grain size, texture, impurity adsorption and desorption during electroplating. Since grain size and structure are fundamental to the mechanical and electrical properties of electroplated copper, thorough analysis is carried out. The texture of the copper is affected by the room temperature annealing during storage of copper. Annealing behavior of copper is strongly dependent on the impurity actions of foreign species.

Figure 3-13: (a-b) FIB image and (c) SEM images of microstructure of copper at the bottom portion of the TSV with 60 μm diameter.

Figure 3-14 (a) and (b) show the FIB image of copper microstructure at the middle of the pillar. The grain size is apparently larger than that at the bottom of the pillars. The average diameter of the grain size is about 2-4 μm. Smaller sized copper grains have twinning structure. Figure 3-14(b) shows the microstructure of copper at the top of the through-silicon via. The grain sizes are similar to those at the middle of the pillars. While the variation of ion transport is insignificant in the through-hole plating process due to its low current density in both forward and reverse periods, the incorporation of leveler species may be significant at the bottom of pillar where smaller

grain sizes are observed. Previous theoretical modeling shows the influence of lithographic mask patterns on the deposit profile in electroplating [28].

Figure 3-14: FIB image of microstructure of copper at the (a-b) top and (c-d) middle portion of the TSV with 60 μm diameter.

Although significant variations of copper grain sizes are observed in the aspect-ratio dependent current density plating modulation, such variations are also observed in the present work. This is due to the lower concentration gradient during electroplating near the opening of the TSV. It shows that even with the constant pulse-reverse current modulation, homogeneity in grain sizes is not achieved. As such, even with the annealing of the TSV, homogeneity in grain sizes will not be obtained. Therefore, in

critical applications where the microstructure of deposits is very important, the current modulation needs to be controlled to obtain uniform grain size distribution.

Figure 3-15: Transmission electron microscopy of copper nanotwins formed at the bottom of electroplated TSV.

Figure 3-15 shows the TEM picture of the twinned structure inside the grain. At the bottom, the TSV shows twin lamella spacing of about 5 nm. The existence of such nanoscale twins can be attributed to the observed high hardness of the TSV at the bottom of the TSV. It shows a nanotwin having a thickness of approximately 7 nm. Observation of nanotwins in electroplated copper experimentally allows the use of its properties such as high mechanical strength. However, formation of nanoscale twins is an atomic scale process during or immediately after the electrocrystallization process. Twinning is easier when the grain sizes are smaller, as observed in pulse/pulse-reverse electroplating. A theoretical analysis of such phenomena is proposed in chapter 6.

Modification of stacking fault energies in copper due to applied stress could lead to various possibilities of twinning in copper lattices.

3.8 Mechanical properties of TSV

3.8.1 Nanoindentation

The instrumented nanoindentation method was introduced in 1992 [29, 30] for measuring the hardness and elastic modulus of materials at micro scale. Using sophisticated instrumentation, the technique can be used to investigate the materials at micro and nano scale. The advantage of this technique is its ability to determine the mechanical properties from the load-displacement curve without the need to take the image of impression on the test specimen. In this method, the Berkovich indenter is commonly used to obtain the load-displacement curve although, traditionally, other indenters such as Bridgnell, Meyer and Vickers hardness tests are used for characterization of structural material in mechanical metallurgy [31].

Figure 3-17 illustrates the typical load-displacement curve of the instrumented indentation measurement. During the loading, both elastic and plastic deformations occur. Therefore, the hardness impression conforms to the shape of the indenter. During the unloading process, the elastic portion of the deformation is recovered. Hence, the contact process of the unloading process can be modeled using the elastic solution. The most important parameters that can be obtained from such measurements are the maximum load P_{max} , the maximum displacement h_{max} , the elastic unloading stiffness, which is the slope of the unloading curve at the beginning of the unloading process, and the final depth h_f . The final depth h_f represents the depth of penetration of the indenter after the load has been totally removed. The method of analysis to determine the hardness H and elastic modulus E was proposed by Doerner and Nix [32]. The unloading curve can be approximated by the power law relation [33]:

$$P = \alpha(h - h_f)^m \quad (3-12)$$

where α and m are the power law fitting constants. For aluminum, α and m are 0.265 and 1.38 respectively while values for nanotwinned copper are not available.

Figure 3-16: Schematic illustration of loading-unloading process in nanoindentation.

Figure 3-17: A typical load-displacement curve in nanoindentation.

The elastic model shows that the amount of sink-in h_f is given by [33]:

$$h_s = \epsilon \frac{P_{max}}{S} \quad (3-13)$$

where ϵ is a constant which depends on the geometry of the indenter. The value of ϵ for conical punch indenter is 0.72. The commonly used Berkovich indenter can be approximated as the conical indenter with half-angle = 70.3° . As illustrated in Figure

3-16, the depth at which the contact between the specimen and indenter contact is h . The area function $h = F(h_c)$ is usually calibrated with independent measurements to include all non-ideal indenter geometrical effects. The hardness of the material can be calculated from the (3-4): [33]

$$H = \frac{P_{max}}{A} \quad (3-14)$$

The elastic modulus can be obtained from the contact area and the measured unloading stiffness S from the following relations:

$$S = \beta \frac{2}{\sqrt{\pi}} E_{eff} \sqrt{A} \quad (3-15)$$

Where E_{eff} is the effective elastic modulus defined by [33]

$$\frac{1}{E_{eff}} = \frac{1 - \nu^2}{E} + \frac{1 - \nu_i^2}{E_i} \quad (3-16)$$

E and S in the above equations are Young's modulus and Poisson ratio of the specimen, and E_i and ν_i are Young modulus and Poisson ratio of the indenter. The value of β is taken as unity although more recent research shows that the value can deviate from unity significantly. The model takes the elastic properties of both specimen and indenter.

Figure 3-19 (a) and (b) show the hardness and modulus of elasticity measured by the nanoindentation method in the instrumented indentation system by MTS. The Poisson ratio of the bulk copper was used in the measurements. The Poisson ratio of

bulk copper, 0.33, is used for calculations. The applied force during the experiments is 20 mN. Figure 3-20 shows the place where indentations are performed on a 60 μm copper TSV. The previous Figure 3-18 shows a typical load displacement curve of the instrumented indentation testing. The indentation depth of 700 nm is enough to calculate the properties because the measurement with Continuous Stiffness Method (CSM) shows the converged measured value around 600 to 700 nm. The applied load of 20 mN is used in the measurements. CSM was also used to ensure that the measurements are within reasonable accuracy.

Figure 3-18: A typical load displacement curve for nanoindentation of copper TSV.

Measurements are repeated over three sets of TSV of different diameters. A more complete set of measurements and results is given in the appendix B. Figure 3-20 shows the optical photograph of nanoindentation marked on the TSV of diameter 60 μm . A very smooth surface is needed for the accurate measurement of modulus of elasticity and hardness in nanoindentation. The smooth surface is achieved by polishing

the surface with diamond based polishing solution with a particle size of 50 nm.

Figure 3-19: (a) Hardness and (b) modulus of elasticity of TSV of various diameters ranging from 60 to 150 μm. (Arrows show the direction of electroplating beginning from bottom [noted as point 8] until the vias are fully filled at point 1.)

Figure 3-20: Indentation marks along the axial direction on a cross section of 60 μm TSV.

3.9 EBSD studies of TSV

Grain size and the structure of grains in copper and the orientation of grains in copper have strong effects on the mechanical and electrical properties of electrodeposited copper. Especially in electroplated copper, grain structure evolution processes such as stress induced texture development, grain agglomeration, twinning and detwinning, room temperature annealing and recrystallization [34], and high temperature annealing are important phenomena [35]. EBSD has been used to study the microstructure of small structure and their mechanical properties in oxide materials [36] and damascene copper plated TSV [37]. The grain size of copper and its associated behavior are well studied in chip scale electroplated damascene interconnection. However, similar phenomena are not well explored due to its recent development in integration of TSV into functional devices. In the present work, EBSD grain mapping and orientation are studied for 60 μm TSV well after the usual stabilized room temperate annealing of electroplated copper. Previous studies show that the grain agglomeration and de-twinning take place under a high temperature annealing process. However, information about the room temperature behavior of pulse-reverse electroplated copper after self-annealing period is lacking. A TSV of diameter 60 μm is cut to study its cross-sectional views. Fine polishing with low current ion beam in the

FIB system produces the smooth and clean surface required to provide electron diffraction patterns in EBSD.

Figure 3-21 (a) shows the cross sectional FIB ion image after the fine polishing. It can be seen from the figure that fine grains are observed at the bottom of the TSV (top of the FIB image), followed by the larger grain size area. Figure 3-21 (b) shows the band contrast during EBSD measurement, which clearly depicts the grain boundaries and grain sizes. The band contrast figure matches with the orientation mapping of the copper. Interestingly, the area with large sized grains lies between two regions with finer grain sizes. This could be attributed to localized grain growth after years of room temperature storage. There is no variation in grain sizes along the radial direction of TSV which shows that electroplated copper grows uniformly from the bottom with no preferential deposition and dissolution near the side wall of the trench. Note that TSV fabricated with a higher current density has varying grain sizes in the radial direction as discussed previously in this chapter. Figure 3-21(b) evidently shows the migration of grain boundaries in copper during the recrystallization process.

Figure 3-21: (a) FIB ion imaging of the bottom cross-section of 60 μm diameter TSV, (b) band contrast.

Figure 3-22: Schematic representation of nucleation by migration of boundaries induced by deformation[38].

Figure 3-22 shows the grain growth model by migration of boundaries. In both the ion image and band contrast as shown in Figure 3-21(b), it can be observed that the larger grain area penetrates through the area with small grains. The proposed mechanism [38] of grain growth is used to explain the recrystallization or grain growth of highly strained specimens. Previous observations of such mechanism were made with the metals deformed at a strain of 0.4 or less. The condition for such grain growth is given by [31]:

$$L < \frac{2\gamma}{\Delta E} \quad (3-17)$$

where γ is the grain boundary energy per unit area and ΔE is the energy released by the decreased defects level. The twin boundary energy may have played a strong role in the process and further studies are needed for such twin boundary effects on recrystallization. Previous studies in the literature use in-situ observations of the detwinning process, which may have significant effects on the observation due to the electron transparent sample. The observed grain growth is not due to geometrical constraints [39] as the grain sizes are smaller than the characteristic dimensions of the

Figure 3-23 shows the Kikuchi patterns of electron diffraction in copper at two random spots with and without indexing the Kikuchi band from various lattice planes in copper crystal. The indexing matches the standard copper diffraction pattern with excellent accuracy.

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Figure 3-24: EBSD grain orientation mapping of bottom area of 60 μm TSV in (a) axial, (b) radial, and (c) surface normal direction.

Figure 3-24 shows the grain orientation mapping of the area in the cross-sectional picture in Figure 3-21 (a) with its associated legend for orientation. As shown in the figure, the deposit has no apparent preferred orientation in both axial and radial directions. It also agrees with previous investigations of texture in TSV [41] although details of the fabrications and electrochemical parameters are different. This shows that

pulse-reverse modulation or chemical composition has no significant effect on the texture of copper after recrystallization in case of high aspect ratio TSV.

Figure 3-25: Inverse pole figures of the sample in all three directions [(a) axial, (b) radial, (c) cross-sectional normal direction].

Figure 3-25 shows the inverse pole figure of the scanned area. The observed strong texture in the grains of smaller sizes may have been due to the sub grain rotation [42] during recrystallization in the region near to the silicon dioxide interface. It is important to obtain the detailed orientation in such situations, because the large stress

introduced to make microstructural changes in copper can affect the reliability of the brittle silicon dioxide interface.

3.9.1 Microstructure of TSV fabricated with high current densities

The microstructure of the TSV fabricated with high current density of 40 mA/cm² is investigated with a FIB of 40 mA/cm² because it is beyond the theoretical limiting current density as discussed earlier. The experimental procedure is the same as mentioned previously.

Figure 3-26: (a-b) Microstructure of copper in the void formed at the core of TSV, (c-d) magnified view of copper surface morphology at the core of TSV.

Figure 3-26 (a) and (b) show the cross sectional SEM pictures of voided TSV at the core. Figure 3-26 (c) shows the SEM picture of the surface morphology and microstructure of copper in the void. The detailed view of the SEM picture in Figure 3-26 (d) shows the voided porous microstructure of copper. It can be seen clearly that a visible small void core has formed in the copper deposit. Such deposits can largely

affect the reliability and performance of TSV. Although such voids were encountered during microfabrication [43] in the past, detailed information of such phenomena was not available. Electrochemical studies as can be found in Figure B-13 of Appendix B show that limiting current density is responsible for such voiding.

3.10 Micro-Raman spectroscopic measurement of stress in silicon due to TSV

Levels of stresses in the silicon and silicon dioxide layer are to be controlled and kept to a minimum to ensure the reliability of the TSV interconnected devices under various operating environments. The stress introduced to the silicon and silicon dioxide during the electroplating process may play an important role in the reliability of the silicon/silicon dioxide interface [22]. Various spectroscopic methods can be used to observe the stress in silicon such as micro-Raman or x-ray diffraction [44]. Previous investigations showed that pulse reverse electroplating may induce residual stress in copper in addition to the dynamic evolution of complex stresses during deposition, which relates to the formation of nanotwins due to their crystal structure being energetically favored compared to highly stressed FCC crystals. On the other hand, residual stress in crystalline copper with a nanotwin structure is not thoroughly studied yet. Since TSVs are fabricated in through-hole silicon, highly sensitive micro-Raman spectroscopy can be used to measure the residual stresses in silicon, which are due to the electrodeposition of copper. In order to study the stress in silicon caused by a single pillar and avoid coupling with the stress caused by other pillars, the pillar at the edge of the array was scanned with micro-Raman spectroscopy. The TSVs with a diameter of 60 μm were studied at three different locations along the pillars. Assuming biaxial strain in the silicon (001) plane, the stress component can be described as:

$$\sigma(MPa) = -435 \times \Delta\omega^{-1}$$

Equation 3-18

where the stress (σ) is in the unit of MPa and $\Delta\omega$ is Raman shift in the unit of cm^{-1} . Figure 3-27 below shows the cross-sectional SEM picture of TSV with 60 μm diameter and the details of measurements of Raman response. The Raman shift in the region near the silicon/silicon dioxide surface is plotted on the picture to visualize the Raman response along the scanning line. The scanning lines are not near to the top and bottom surface of the wafer to ensure that the stress measured with Raman spectroscopy is purely due to the stress in TSV.

Figure 3-27: Cross-section picture of TSV and Raman shift in silicon near TSV of 80 μm .

The beam spot size of the laser used to measure the Raman scattering is less than 0.5 μm to ensure that the measurement is accurate. The scanning was carried out from 100 μm at the side of the copper to the interface of the silicon and silicon dioxide in a step size of 1 μm . The measured Raman-scattered signal is fitted with Lorentz function to define the peak position of the measurement. Only at the nearest point from

the Si/SiO₂ interface was a Raman shift of 0.5 cm⁻¹ observed, which is equivalent to a stress of 215 MPa (compressive). The scanning was carried out on copper samples with diameters of 60 and 80 μm at different locations. The maximum measured value is 0.5 cm⁻¹ with some points lower than this value. The dependence of the stress on the location of measurement along the length of TSV is statistically insignificant. The present level of stress is commonly encountered in the thermal oxidation of thick silicon dioxide. The corresponding strain is less than 0.0002, which is a very small strain. The stress due to electrodeposition in through-holes is very low compared to the thermal stresses. Although micro-Raman spectroscopy was used to measure the local stress state in the silicon adjacent to the Si/SiO₂ interface, the surface morphology of the DRIE-etched sidewall and oxidation stress due to surface unevenness of the DRIE-etched sidewall may play an important role. Further investigation is needed regarding this important aspect of the interaction between the DRIE sidewall roughness, stresses due to oxidation/passivation and the electrodeposition of copper.

3.11 Void formation in TSV plated over limiting current densities and resulting copper grain structure

Figure 3-28 shows the open-ended void formation resulting from the high current density in the electroplating of TSV's. Such edge build-up effects were previously reported for through-polymeric mask plating [45] using numerical simulations which consider tertiary current-distribution. Complicated electrochemical transport phenomena such as concentration polarization, activation polarization and stagnant diffusion-layer treatment of convective mass transport intoned to be included in the model to obtain an understanding of the effects. Trench spacing and diffusion film thickness can affect such edge build-up effects. It is obvious that the electroplating parameters can have a strong influence too. However, due to their complicated electrochemical phenomena, numerical simulations have been limited to simple cases

and no experimental observations, especially regarding the deposit properties, is available. Although there are other void formation mechanisms such as stress relaxation over time through diffusion of vacancies [46], the present case is purely of electrochemical nature.

Figure 3-28: Open type void formation at the core of TSV with 120 μm diameter.

Figure 3-28 shows a cross-sectional SEM picture of the grain structure investigation of TSV plated with current density over the limiting current density. The current density is 40 mA/cm^2 . Since the uniformity of plating along the radial direction of TSV is affected, the area largely affected by this non-uniform deposition is at the perimeter of TSV. Three areas at the perimeter of TSV were etched in the ion beam for microstructural examination. The objective of the measurements is to study the microstructure of copper at the regions where electroplated copper builds up rapidly. Figure 3-29 shows the formation of closed type voids at the core of TSV. It is observed that both open and closed type voids can result in plating with current densities over the limiting current density. As discussed in this chapter, the void formation is due to current density higher than limiting current density. However, whether the void will be

open or closed void is purely random nature due to the strong variations of electrochemical parameters locally at each site of wafer.

Figure 3-29: Cross-sectional SEM picture of void formation of the TSV with 100 μm diameter.

Figure 3-30: Cross-sectional view of TSV of 120 μm diameter showing the location of FIB microstructure examination.

The void is filled with the epoxy compound during the molding process of TSV for analysis such as measurements of modulus elasticity, hardness, impurity incorporation and microstructural imaging.

Figure 3-31: FIB cross-sectional analysis of microstructure of copper TSV near the region close to the sidewall (a) at the location marked as *A*, (b) at the location marked as *C* and (c) at the location marked as *D* in the figure.

Figure 3-31 shows the FIB ion image of the region marked in the cross-sectional SEM picture in Figure 3-30. Figure 3-31(a) shows the grain structure of TSV at the bottom region. It can be seen that there is no significant variation of grain size in the region close to the side wall. However smaller grain sizes are observed in Figure 3-31b and c. As the void is formed at the core of the plating trench, the variation in current distribution has been affected, resulting in preferential deposition and dissolution at the edges of the trenches, inducing the smaller grain sizes near to the side wall. Such inhomogeneity in grain sizes can affect the performance and reliability of the TSV, as smaller grain sizes usually involve higher stresses, which may lead to failures or cracks in the insulation layer between the copper TSV and silicon substrate. Higher levels of impurity incorporated at such fine grain regions are discussed later in this chapter.

This mechanism of faster growth of copper near the side walls due to oversupply of metal ions from above the silicon wafer is explained numerically and reported previously [14,15] for electroplating through thick photoresist patterns at current densities near the limiting current density. The larger TSV has voids in the middle because the availability of extra copper ions from the area above the silicon makes copper grow faster at the perimeter and center of TSV, depriving copper ion from following the faster growth rate around the perimeter. It induces a slower growth rate at the core of TSV. The smaller TSV has no void due to its smaller size. There is no ion-deprived gap or space at the core of TSV due to its small diameter. The thickness of the rapidly growing copper layer at the perimeter is around 25 to 30 μm . Therefore for TSV with a smaller diameter, there is no space at the core. The entire volume of TSV is filled by rapidly growing copper from each side of the trench. This shows that the observed phenomena can be applied by carefully using the current densities near to limiting current density for fabrication of smaller TSV to increase the plating speed.

3.12 ToF-SIMS analysis of impurity incorporation in TSV fabrication process

Plating current density and annealing have strong effects on impurity inclusion in copper electrodeposition for on-chip interconnection [47]. The main species of impurities in copper electroplating are carbon, sulfur, oxygen and chlorine. The carbon comes from the inclusion of organic molecules from additives used in the plating. The source of the chlorine is the chloride ions that come from hydrochloric acid content in the electrolyte. Recent improvements in the application of ToF-SIMS in electronics materials are given in [48].

TOF-SIMS [49] uses the primary pulse ion beam to remove and release the ionic and molecular species from the surface of the sample. Due to the energy transfer from the primary ion beam, the secondary ions from the surface are released and accelerate

towards the spectrometer. The mass of the species is measured by the time taken to arrive at the detector from the surface of the sample.

There are three steps in the TOF-SIMS chemical analysis of the sample. Firstly, the mass spectra are recorded for every point across the surface of the sample. The scanning range of the spectrum depends on the ionic and molecular mass of the species detected on the surface of the sample. In the present case, since the ionic impurity species are generally associated with impurity in the copper deposit, the lower range of mass spectra is enough. However, it has been shown in the literature that the organic additive species such as macromolecular structures can be embedded into the copper deposit depending on the electrodeposition methods and parameters. Secondly, the intensity of the ion mass for a particular mass spectrum is plotted to produce the chemical image of the surface. Thirdly, the depth profiling of the surface can be performed by etching the surface with ion beams at the determined rate. During the spectroscopy analysis, only the outermost one or two atomic layers are removed by the energetic primary ion beam via the collision-cascade mechanism.

Although impurity levels in the on-chip interconnection fabrication have been extensively studied, the impurity investigation of TSV, especially high aspect ratio TSV, has not been well studied. Due to the differences in on-chip interconnection and TSV such as size and aspect ratio, the mechanisms of impurity inclusion may be different and it is important to study such inclusions due to their relation to electrical, mechanical and thermo-mechanical reliability issues. The issue in the case of TSV is complicated by the use of pulse-reverse electrochemistry. Recent studies in pulse-reverse electroplating for TSV show the requirement of using detailed impurity analysis during fabrication and its relation to the reliable fabrication of TSV [50].

Continuous sputtering and analysis of ion masses of the sample for a period of time will give the comparative chemical content of the bulk material in the etching direction. But this strategy has some limitations such as slow etching/sputtering rate in the SIMS-TOF analysis, long durations of etching, difficulties in focusing the ion-beam over large etching distances, etc. Therefore, the surface scanning over the cross-sectional area of TSVs with various dimensions is conducted.

Impurity incorporation is an important phenomenon in electroplating in general and fabrication of TSV in particular. Incorporation of impurity induces the deposition of copper with finer grain sizes, while at the same time increasing the level of stress. Previous investigation on the fabrication of high-aspect ratio TSV shows that void free copper filling of TSV should not be the sole criteria for the evaluation of TSV fabrication and integration processes. The other important criteria are low resistivity for better electrical performance and low residual stress for higher performance in reliability aspect of the system or component.

ToF-SIMS and/or SIMS is becoming an important tool in the analysis of microelectronic and MEMS material due to its capability to perform quantitative/qualitative surface chemical analysis and elemental analysis. Previous applications of ToF-SIMS to materials in microelectronic and MEMS materials can be found in the reference [51].

Although the depth-profiling analysis of copper may be the best method of analysis to examine the impurity profile of copper, the high-aspect ratio nature of copper TSV in the order of hundreds of micrometers does not allow the use of in-situ depth-profiling. Therefore, surface scanning on the cross-section of TSV is performed to obtain the impurity profile in TSV.

The three samples of TSV fabricated with constant current periodic pulse-reverse modulation are examined using the ToF-SIMS analysis. The TSV with 60 and 100 μm diameters fabricated with low-current density and a sample of 150 μm TSV with void are examined using ToF-SIMS. The analysis is done with the 25 KeV Bi⁺ analysis gun at a current of 1.1 pA over a 500 μm wide square. A 2KeV Cs⁺ primary source is used with a current of 100 nA over larger scanning areas of 600 and 800 μm . The samples were sputter-cleaned in the SIMS equipment to ensure that contamination from atmosphere is removed prior to analysis. For each of the ion images, the log scale legend is shown. For the impurity concentration, the ion intensity for the selected area of approximately 40 μm $\times$ 40 μm for each element is given. The values are normalized with the total ion intensity with arbitrary units.

The smallest possible size of the ion beam is about 1 μm in the experimental setup. The copper samples are polished with alumina oxide power down to sub-micrometer particles. Due to the existence of thin oxide layer on the copper surface after polishing and other absorbents such as mono or bi-layer carbon on the surface, the sputtering of 30 nm depth of copper surface is performed before the actual chemical analysis is conducted. The following Table 3-3 shows the assignment of mass spectrum peaks to each of the elements monitored in experiments, although complete information is collected from spectrometer. In this research work, only the elemental counts are used to analyze the impurity incorporation because these elements act as finger print of the larger molecular structure which embeds in the copper during electroplating. Scanning is performed up to 300 amu which is enough to detect the typical atomic species which came out of impurity compounds.

Table 3-3: ToF SIMS ion mass assignment for various ion species under investigation.

Center mass (U)	Assignment
12.00	C ⁻
15.99	O ⁻
31.97	S ⁻
34.97	Cl ⁻
62.93	Cu ⁻

Figure 3-32 shows the SIMS ion image of the 60 μm TSV. Figure 3-32(a) shows the total ion image while the remaining subfigures b from h show the image formed by various ion channels of SIMS analysis. It can be seen in Figure 3-32(b) that the concentration of carbon peaks at some localized spots. Figure 3-32(d) shows the ion image for silicon and a clear contrast between the silicon region and copper can be observed. Figure 3-32(e) shows the uniform distribution of sulfur throughout the copper while the significant contrast/gradient in chlorine content along the length of TSV can be observed in Figure 3-32(f). Figure 3-32(g) and (h) show the profile copper ions. The ultra-high contrast of the image of copper ions shows the amount of diffusion of copper into silicon substrate via the silicon oxide layer is very low or almost negligible. Impurity incorporation in copper has a strong relationship with electrochemistry, waveform and current density [52]. It should be noted that although ToF-SIMS can be used to analytically measure the absolute content of individual components, in the present case, it is used to study the differential intensity across the scanning area to figure out the process-impurity level-mechanical properties relations of electroplated TSV. Therefore, the ion count units as shown in the chemical images in

this chapter are arbitrary because different species have different ion-yields during measurement.

Figure 3-32: ToF-SIMS chemical image of 60 μm TSV, (a) overall ion intensity, (b) carbon, (c) oxygen, (d) silicon, (e) sulfur, (f) chlorine, (g)-(h) copper.

Figure 3-33 shows the negative ion image of TSV with 100 μm diameter. Figure 3-33(a) shows the ion image of all channels while the remaining subfigures show the ion channel assigned to specific atomic species. Figure 3-33(b) shows the profile of carbon impurities and it can be clearly observed in the localized high-concentration spots or narrow line of areas adjacent to the side wall. It shows that the organic additives used in the plating tend to deposit near to the side wall during deposition. Since the carbon contents come mainly from the large organic additive

molecules, it is less likely to be atomic carbon, although the dynamics of individual elemental species from large organic molecules embedded into copper are not well-studied and understood.

Figure 3-33: ToF-SIMS chemical image of 100 μm TSV (a) overall ion intensity (b) carbon, (c) oxygen, (d) silicon, (e) sulfur, (f) chlorine, (g)-(h) copper.

Figure 3-33(c), (d) and (e) show the clear contrast of oxygen, silicon and sulfur respectively. It is observed that the oxygen concentration in TSV is larger than that of the silicon substrate since the oxygen comes from various sources during electrochemical deposition. Figure 3-33(g) and (h) show the copper ion channel image with excellent contrast, with very low diffusion of copper into silicon substrate.

Figure 3-34 shows the negative ion images of SIMS fabricated with high current density. Therefore, voids are formed at the core of the TSV. Figure 3-34(a) shows the ion image of all ion channels and Figure 3-34(b) shows the carbon impurity profile. Very uniform carbon impurity profiles can be observed. Figure 3-34(c) shows the image for oxygen and a clear concentration gradient can be observed. The bottom portion of the TSV has lower oxygen content. The oxygen may have been diffused from the free surface of the void into the copper. Figure 3-34(d) and (e) show the uniform concentration profile of silicon and sulfur. Figure 3-34(f) shows the ion image of chlorine with heavily localized high concentration spots in the region near the sidewall. Therefore, chlorine species diffuse to the regions near to the silicon dioxide layers. Deposition of chlorine at the silicon / silicon dioxide layer interface can reduce the reliability of copper adhesion to the insulation layer. This shows that it is important to control the chlorine species in future TSV specific electrolyte solution designs. Figure 3-34(g) and (h) show the clear contrast of copper which means that the diffusion of copper into silicon substrate has not been observed.

The chlorine and oxygen ions may have decomposed during the room temperature annealing of copper TSV since the experiments were conducted on the sample well after the recrystallization period to observe the natural room temperature annealed state. Previous studies [53] with similar copper sulphate plating chemistry show that the carbon impurity concentration is not changed during the high temperature annealing process. This implies that the observed variation in carbon impurity along the length of TSV with 60 μm diameter as shown in the Figure 3-37 is not due to the room temperature annealing phenomenon. It is associated with the electrochemical condition during the fabrication by pulse-reverse electroplating. Absolute intensities or numerical values of ion counts in the chemical maps are not important.

Figure 3-34: ToF-SIMS chemical image of 150 μm TSV (a) overall ion density (b) carbon, (c) oxygen, (d) silicon, (e) sulfur, (f) chlorine, (g)-(h) copper.

The core void region of the chemical image shown in Figure 3-34 is filled with the epoxy compound during the molding and cross-sectioning sample preparation process. Therefore, the reading from the void region is that of a molding compound. The diffusion of species from the molding compound into the copper and silicon is assumed to be negligible due to its large molecular structure. Impurity incorporation in TSV fabrication with plating current density over the limiting current density is thoroughly analyzed in this thesis.

Figure 3-35: The area of reading from SIMS spectra from 60 μm TSV (a) position 1, (b) position 2, (c) position 3, (d) position 4, (e) position 5.

Figure 3-35 shows the ion image with the area selected for impurity level analysis. Since the plating is uniform and no preferential growth of copper deposit at the perimeter of TSV is observed, the impurity level along the radial direction of the TSV is nearly constant. The area averaged ion intensities are calculated for the analysis. The positions 1 to 5 as shown in Figure 3-35 will be used in analysis of impurity incorporation along the length of TSV. The objective of the measurements is to measure and correlate the impurity incorporation level, microstructure and mechanical properties of the copper TSV in axial direction. Relatively large areas in each portion of the TSV are chosen to ensure that some localized concentrations of species do not affect the final analysis. Since there is no preferential growth of copper in TSV with 60 μm diameter, it is a reasonable assumption that the impurity concentrations do not change in the radial direction of TSV. However, for TSV with larger diameters, there can be variation in radiation direction as evident by the variation of grain sizes along the radial direction in this chapter.

Figure 3-36: The areas of reading from SIMS spectra from 60 μm TSV (a) position 1, (b) position 2, (c) position 3, (d) position 4, (e) position 5.

Figure 3-37 shows the impurity level of species along the axial direction of 60 μm TSV. The readings are taken from a square area ($20 \times 20 \mu\text{m}$) from the TSV as shown in Figure 3-35. A large area is selected in plotting of the impurity level to minimize the localized concentration spots. It can be seen from the figure that carbon and chlorine impurity levels are significantly higher at the bottom of the TSV than at the upper portion of the TSV. The primary source of the copper and chlorine species is the additives used in the plating solution. Since the experiments are done well after the self-annealing duration, it is clear that the impurity species are still trapped in the copper matrix rather than diffusing away during room temperature annealing process. The source of the sulfur is most likely the decomposition of sulphate compounds during the deposition, although such incorporation of sulphate is controversial. A possible source for sulfur is the fragments of additive molecules such as sodium polyanethol sulfonate (SPS), which are the brightener and leveler compounds in the electrolyte solution. However, the probability of molecules from organics additives breaking is

low. A more likely source is the additive molecules embedded into the copper matrix during electroplating.

Figure 3-37: Impurity level of TSV with 60 μm diameter (a) copper,(b) chlorine,(c) sulfur and (d) oxygen (Position 1 to 5 are shown in Figure 3-35).

Figure 3-36 shows the ion image with the area selected for impurity level analysis for TSV with a diameter of 100 μm . Since the plating is uniform and no preferential growth of copper deposit at the perimeter of TSV is observed, the impurity level along the radial direction of the TSV is nearly constant. The area averaged ion intensities are calculated for the analysis. The ion intensities collected from position 1 to 5 will be used in the analysis of impurity profile in the following paragraph. It shows the significant variations in carbon and chlorine along the length of TSV while the concentration of sulfur and oxygen remain similar along the TSV. Carbon is the principal component in many organic additives.

Figure 3-38: Impurity level of TSV with 100 μm diameter (a) copper, (b) chlorine, (c) sulfur and (d) oxygen (Position 1 to 5 are shown in Figure 3-36).

Figure 3-38 shows the impurity profile of the TSV of 100 μm diameter as shown in Figure 3-36. It can be seen easily that although the carbon impurity varies along the length of the TSV, it is less significant than the impurity level of the TSV's with 60 μm diameter. However, the chlorine impurity level is much higher at the bottom of the plating. Variation in the impurity level of sulfur is also more significant than that of 60 μm TSV. In both 60 and 100 μm diameter TSV, the variation in level of oxygen is less significant. The observed impurity level, especially carbon impurity, has been found to be in direct correlation with the observed grain size variation and mechanical properties of the TSV of different diameters. A higher concentration in carbon impurity is a sign of a higher level of organic additive trapping in the copper matrix, which leads to the smaller grain sizes in the lower portion of the TSV with a

smaller diameter. Variations in the mechanical properties of larger diameter TSV are not as significant as reported previously. Therefore, impurity effects and electrochemical effects of pulse reverse electro-deposition significantly affect deposit properties at various locations along TSV.

The main impurities incorporated into the deposit are sulfur, carbon and chlorine [54, 55]. The self-annealing behavior of blanket copper films has been studied [56]. The segregation of impurity species to the grain boundaries was also reported in blanket electroplated copper films [57]. By studying the impurity concentration using SIMS, the correlation between impurity and mechanical properties can be obtained. As discussed in earlier in this thesis, the observed greater hardness and smaller grain size and higher density of nanotwins have a direct relationship with the higher impurity concentrations of carbon and chlorine, which are the principal components of an organic additive. Therefore, organic additives play a significant role in the microstructure crystallization and room temperature annealing of the copper TSV. It also shows that even after the long room temperature annealing, the inhomogeneity in impurity species still persist. This implies that the impurity particles from atomic and molecular species of additives form a stable structure within the copper lattice matrix. Thermal energy associated with the room temperature is not enough to completely recrystallize the copper. This observation is important because a longer annealing time or higher annealing temperature can be used to remove such inhomogeneity if it is needed.

Although it is clear from the ToF-SIMS measurement results so far that there is inhomogeneity in impurity incorporation during TSV plating process, the measurements of impurity incorporation at the center of the TSV along axial direction will reveal the aspect-ratio dependent impurity levels so that measurements can be used to compare

again the mechanical properties measured along the TSV. As shown previously in this chapter, grain sizes are smaller at the bottom of TSV. Since the TSV used for impurity measurements are fabricated with low current density, the effect of limiting current density is limited. Therefore, the variation in grain sizes and mechanical properties are directly associated with the impurity incorporation.

Figure 3-39: Impurity profile of (a) carbon, (b) chlorine and (c) sulfur, along the 60 μm TSV.

Figure 3-39 shows the impurity levels of carbon, chlorine and sulfur along the length of TSV of 60 μm diameter. It can be clearly seen that carbon has a higher intensity at the bottom of the TSV. The level for chlorine follows the same trends. A peak at the position from 100 μm shows the region with a high intensity of impurity which may be due to excessive accumulation of additive or segregation of impurity

after fabrication. However, the intensity for sulfur shows no significant change along the length of TSV. Sulfur is a common ingredient in an electroplating solution. However, not many experiments have been done to investigate its source and role in electroplating. It is observed that higher impurity in TSV correlates with higher mechanical strength as discussed previously in this chapter.

The presence of chloride ions in $H_2SO_4 + CuSO_4$ solution makes the formation of the $CuCl$ phase [58] intermediate. The possible reaction routes for copper deposition are:

Out of many possible reaction routes, previous measurements using Electrochemical Quartz-Microbalance (EQCM) show the possible dominant route in (3-19a). When the chloride ion concentration exceeds 1 mM, the $CuCl$ phase appears as described in reaction (3-19a). Copper chloride crystals deposited on the copper surface due to the chloride intermediation have been reported previously [59].

Therefore, the observation of higher concentration of chloride species indicates that the chloride ions act as nucleation sites resulting in smaller grain sizes. Therefore, the observed chlorine species is likely to be located in intergranular rather than intragranular incorporation into the copper grains. In this present work, the ToF-SIMS analysis is performed long (three years) after the deposition of copper. Therefore, it also means that the diffusion of incorporated chloride ions is very limited. At higher concentrations of chloride ions, the formation of $CuCl_2^-$, $CuCl_3^{2-}$ and $CuCl_4^{3-}$ leads to

complicated electrochemical reaction routes [60, 61]. The CuCl compounds reduce the electrical conductivity of copper deposits. Therefore, it is expected that a smaller TSV with higher level of chlorine incorporation will have higher resistivity.

Oxygen impurities from additives and copper oxide CuO_2 reduce the reliability of copper by hydrogen embrittlement. The high temperature (approximately 400°C) annealing of electroplated copper with hydrogen impurities shows that oxygen and diffused molecular hydrogen form water bubbles at the impurity sites causing the intergranular and intra-granular cracking of copper grains [62]. Other possible sources of oxygen impurities include the organic additives such as PEG with the molecular formula of $\text{HO}[\text{CH}_2\text{-CH}_2\text{O}]_n\text{-H}$ which acts as a suppressor agent in the plating solution. Therefore it is essential to monitor the oxygen impurity of the copper deposit. The most common brightener additive, Bis-(sodium sulfopropyl) disulfide (SPS) with the molecular formula of $\text{C}_6\text{H}_{12}\text{O}_6\text{S}_4(\text{Na})_2$ is also a possible source of carbon, oxygen, sulfur and sodium. Regardless of the sources of the species, their role in microstructure of copper is not properly understood. The branch of electrochemical research dealing with incorporation of impurities in deposit matrix is still at its infancy. The complexity of the problem is compounded by the fact that different electroplating parameters with different electrode configurations are used to achieve the desired electrochemical deposit with required properties. Therefore, the present experimental study will shed light on the role and relative quantity of impurity incorporation in high aspect ratio TSV and metallic MEMS fabrication. It is important to note that the impurity incorporation, microstructure and its mechanical properties are correlated. Thorough analysis of such incorporation is vital to the reliable fabrication of TSV and small structures for nano-electronic and MEMS devices.

Figure 3-40 shows the line scan of impurity level measurements along the center line of TSV in the axial direction. It is observed that the concentration of carbon has small variations along the length of the TSV. However, it still has significant variation as shown previously in Figure 3-38. Therefore, it is observed that the TSV with larger diameter has little variation in impurity along the length. This also partially explained the observed variation of mechanical and micro-structural properties of TSV as more significant in TSV with smaller diameters than that with larger diameters. In larger diameter trenches, the effect of stagnant electrolyte solution is less than those with smaller diameters.

Figure 3-40: Impurity profile of (a) carbon, (b) chlorine and (c) sulfur along the 100 μm TSV.

The detailed analysis of impurity incorporation in properly filled TSV will be followed by the measurements of impurities species in open voided TSV.

Figure 3-41: Areas of reading from SIMS spectra from 120 μm TSV.

Figure 3-41 shows the locations of the areas where the ion-intensity is collected from six different regions on the cross-section of the open-voided TSV with a dimension of 150 μm . The relative concentrations of the species of interest are given in the appendix. It shows the variation of ion intensities at different locations of the TSV. As will be explained in the following chapter 4 and 6, the impurity species contribute to the internal stress in copper grains.

Figure 3-42: (a) Intensity map and (b) Impurity concentration along the side wall of TSV of 120 μm diameter.

Figure 3-43: (a) Intensity map and (b) Impurity concentration along the middle of TSV of 120 μm diameter.

Therefore, it affects the copper's tendency to form twinning or acts as pinning point during room temperature annealing/recrystallization. This is an important issue in electrochemical fabrication as the effect of these phenomenons can contribute to the failure of nanoscale microfabricated devices.

Figure 3-42 and Figure 3-43 show the impurity profile of TSV with a void at the core. As shown in Figure 3-42, the oxygen and sulfur impurity levels remain constant along the line. However, the impurity in chlorine has significant variation especially from the area where the void begins to grow. The high impurity level from zero to 50 μm is due to the impurity from the molding compound during the measurement. Similarly, the high impurity level at the bottom of TSV is due to impurity incorporation at the beginning of TSV where smaller grain sizes are naturally observed. From Figure 3-43, it can be observed that the impurity level in the portion of TSV without void (from 300 to 400 μm in figure) is almost constant with no significant variation. Therefore, the lateral variation in impurity incorporation in large TSV is observed. Due to the tertiary current distribution over a certain limiting current density for a specific electrochemical system, there are inhomogeneous deposits with variations in grain structure.

Figure 3-44: Impurity concentration (a) intensity map and (b) intensity along the side wall of TSV of 120 μm diameter.

Such an effect on the geometrical evolution of electrode has been numerically studied for acidic plating solution in the literature. The present work reports the experimental observation of such voiding mechanisms and its effects on impurity incorporation and grain structure.

Figure B-11 and Figure B-12 in the appendix B show the typical mass spectra of SIMS ranging from 1 to 300 *amu*. Due to the ultra-sensitivity of the ToF-SIMS technique, the peak other than the interest of this present study appears. These spectra are associated with the other elemental or molecular species. Some fraction of molecular structure from organic additives which were embedded into the copper matrix during deposition may appear in the mass spectra.

Variation of the impurity levels along the length of TSV is observed by using the TOF-SIMS technique. While the level of carbon impurity is essentially constant along the length of the TSV, significant variation is detected in chlorine for 100 μm TSV. In agreement with previous reports, incorporated carbon species which are diffused throughout the electroplated copper after electroplating make no significant variation in carbon impurity level while significant variation along the chlorine ion is detected well after the normal room temperature recrystallization. This clarifies the

association with a higher density of nano-twinned copper at the bottom portion of the TSV, even by the use of constant current pulse reverse current modulation as reported previously.

It can be concluded that the incorporation of impurities plays a significant role in the formation of nano-twinned copper, in addition to previously proposed stress/strain induced total energy minimization of copper crystal by twinning. TSVs with larger diameters tend to have concentrated areas of chlorine segregation. In the case of higher current density, the observation of smaller grain sizes shows the preferential dissolution of copper at the edge of the TSVs. Such areas are also associated with a higher level of impurity incorporation which may be due to trapping or segregation of impurity during deposition and room temperature annealing. TSV fabricated with larger current density tend to have voids at the core. They are also associated with higher levels of inhomogeneity in grain size, impurity incorporation and higher tendencies of having concentrated areas with higher impurity levels which is unfavorable for good performance in terms of electrical resistivity, corrosion resistance and electro-migration. In summary, the physical dimensions of the TSV and electroplating parameters such as current density and current modulation techniques have strong effects on the void-free filling of TSV, grain size, impurity incorporation, mechanical properties such as modulus of elasticity and hardness. TSV with desired physical properties can be fabricated by evaluating the effects of such parameters for future three-dimensional interconnect and high aspect-ratio metallic structure for MEMS applications. In all the cases, the intensity of copper in the silicon is constant, which shows that the diffusion of copper from TSV into silicon did not happen due to the silicon dioxide barrier layer, although the copper can diffuse in the silicon easily due to its relatively small atomic radius and its weak interaction with silicon lattice [63, 64].

3.13 Summary

The details for fabrication of TSV with diameters ranging from 60 to 150 μm by pulse-reverse electroplating were presented together with the relevant electrochemical and experimental parameters. Micro-structural and mechanical properties of plated copper TSV are investigated. Focused-ion beam (FIB) measurement of grain size shows the variation of grain sizes along the TSV. Mechanical properties as investigated by nanoindentation show that properties of copper such as modulus of elasticity and hardness vary not only along the electroplated TSV but also with different sizes. The edge buildup effect over limiting current using pulse-reverse electroplating is also investigated together with microstructural studies. It shows that beyond the limiting current density, tertiary current distribution will affect the uniformity of the deposit, especially with the TSV of larger diameters. The impurity levels in the TSV are investigated by the SIMS-TOF technique. Analysis shows that higher impurity incorporation levels are associated with finer grain sizes. The edge buildup effect in TSV fabricated with high current density usually presents with higher level of impurity species and finer grain sizes. The possible routes of impurity species such as chlorine and carbon are discussed.

Chapter 4**Microstructural and Electrochemical Characterization of
Pulse-reverse Electrodeposition****4.1 Introduction**

The microstructure and morphology [65] of the electrodeposits are largely affected by the deposition parameters [66] as shown in Figure 4-1. The kinetics of structural evolution after deposition is also important in practical applications. For twinned and nano-twinned copper structure, it is important to understand their recrystallization and kinetics because twinned structures are not minimum energy structures as compared to the perfect FCC structure. In this chapter, the texture, volume fraction of each texture component, microstructure and texture evolution after ultra-long period of room temperature recrystallization is evaluated. While Figure 4-1 shows the parameter property relationship, it does not provide information such as texture evolution. For example, the thickness and current density dependent on mechanical properties of electroplated copper films have been reported [67]. The texture of deposits varies according to the geometrical constriction as in the case of copper electroplating in damascene trenches [27, 68].

It is important to investigate electrodeposits experimentally due to their complex nature. The initial development of (111) copper texture and its subsequent reduction in its intensity to randomly orientated texture is related to the multiple twinning deformation and stress relaxation in electroplated copper films [69].

Figure 4-1: Effects of plating parameters on microstructure of electrodeposits[70].

As described in Figure 4-1, higher levels of agitation produce finer grain structures in the deposit. The effects of temperature, current density and polarization also have strong effects. However, important quantities such as preferred orientation, time dependent change in preferred orientation and its correlation with electroplating parameters such as current density and type of current modulation are not available. In this thesis, an acid-based electrolyte solution is used to study the texture and stress evolution in electroplated copper thin film using direct and pulse-reverse current modulation.

4.2 Experimental details

The properties of electrodeposition strongly depend on the nature of seed layer or underlying substrate properties such as type, orientation, textured thin film or bulk with certain orientation, etc. In the present study, the copper electrodeposition from the commercial electrolyte on the sputtered gold seed layer is investigated. Since the nature of seed layer is important, it is characterized intensively in next chapter. The (100) silicon wafer of 100 *mm* diameter is used as substrate. The seed layer is 20 *nm* of

titanium and 200 nm of gold deposited by sputtering. The experimental setup used for deposition is as described in the previous chapter.

Figure 4-2 Growth twin theory in silver DC plating [71].

Previous studies show that the secondary grain growth in electroplated copper is incomplete after resistance and stress in the copper arrive at the stable condition [72]. Observation of Cl species at Cu grain boundaries has been previously reported [73]. The presence of additive species also affects the microstructural and thermo-mechanical properties of electrodeposited copper [53] and copper deposited in the damascene process [74]. As shown in Figure 4-2 twinning formation may also originate in the impurity incorporation. This chapter intends to investigate the type of twin formation in electroplated copper.

4.2.1 Chemical compositions of electrolyte

The properties of electrodeposits are very sensitive to the chemical composition of the electrolyte especially in the presence of additives. In the present work, the commercial electrolyte is used to study the properties of deposit which is important for industrial applications. The chemical composition of the electrolyte used for the copper film deposition is shown in the Table 4-1.

Table 4-1: Chemical composition of the electrolyte used in experiments.

Component	Optimum value	Working range
Copper	35 g/L	32-38 g/L
Sulfuric acid	170 g/L	140-190 g/L
Chloride	50 mg/L	40-60 mg/L
Leveler	15 ml/L	4-17 ml/L
Brightener	10 ml/L	4-13 ml/L

The composition is same as the electrolyte used for TSV fabrication. It allows the comparison of measurements such as grain structures and texture.

4.3 X-ray diffraction (XRD) studies of copper films deposited by various current modulations

The properties of electroplated copper films such as surface morphology, texture, grain size, electrical resistivity and hardness vary with the process conditions. In the applications of electroplated copper films for micro/nano systems, the properties of the electroplated copper are required to be well characterized because of their significant involvement in the device fabrication and performance of fabricated devices. For example, the mechanical properties of the electroplated copper are critical in three-dimensional micro structures, while electrical resistivity of the electroplated copper is of paramount importance to the fabrication of electrical and radio frequency devices, due to the large contribution to resistive losses of electroplated copper. Surface morphology is important in microfabrication since rough surfaces can initiate inter-granular cracks and corrosion in the material, hence affecting the mechanical properties and reliability of the micro devices. In this section, the properties of electroplated

copper films on the wafer level are studied with different process conditions. X-ray diffraction is used to study the crystal texture of the electroplated copper films.

The texture coefficient proposed by Charles S. Barrett and T. B. Massalski based on Harris's work [75, 76] is given by the following equation:

$$\text{Texture coefficient} = T(hkl) = \frac{\frac{I(hkl)}{I_o(hkl)}}{\frac{1}{n} \sum \frac{I(hkl)}{I_o(hkl)}} \quad (4-1)$$

$$M(hkl) = T(hkl) \times \left(\sum_{hkl} F(hkl) \right)^{-1} \quad (4-2)$$

where $I(hkl)$ is measured relative intensity, $I_o(hkl)$ is the relative intensity of the corresponding plane in JCPDS database and n is the number of reflections. The values of the standard power diffraction data used in the calculations are given in Table 4-2. When the texture coefficient of all reflection planes are unity, the orientation of the crystal is random. When the coefficient of any of the planes is larger than unity, the preferred orientation exists where the grains are oriented with their planes parallel to the surface. Superior mechanical and electrical properties are associated with a certain texture in electroplated copper [77]. The value of $M(hkl)$ in equation (4-2) indicates the approximate of volume fraction of texture component hkl .

Table 4-2: Standard power diffraction data used in texture computation.

Crystal plane (hkl)	X-ray angle (deg)	Standard intensity (I_o)
Cu (111)	42.98	100
Cu (200)	50.2	46
Cu (220)	73.88	20

Scanning electron microscope is used to study the surface morphologies of the electroplated copper. For copper, (111) fiber texture is developed due to surface energy

driven growth and (100) fiber texture for strain energy driven growth in the elastic regime. The (110) fiber texture is developed for strain energy driven growth in plastic regime.

Figure 4-3: X-Ray diffraction of copper film plated at (a) 2 mA(DC), (b) 10 mA(DC).

At the low current of 2 mA/cm^2 , the peak of Cu (111) is strongest at the beginning and the peak shifts to the (110) at the thickness of $10 \text{ }\mu\text{m}$ as shown in Figure 4-3(a). As the thickness of the copper film increases, the texture of the crystal evolves and the growth is driven by strain energy at plastic region. With the pulse reverse electroplating at the current density of 2 mA/cm^2 , the (111) texture is developed at the thicknesses of 1 or $10 \text{ }\mu\text{m}$, as shown in Figure 4-5(a), meaning that the mechanism of grain growth is surface energy driven throughout the process. The initial development of (111) texture and its gradual decrement has been observed experimentally and the

role of multiple twinning mechanism has been proven by the detailed texture analysis of blanket electroplated copper films [78].

At the higher current density of 10 mA/cm^2 , (100) texture is dominant at thicknesses of $1 \text{ }\mu\text{m}$ and $10 \text{ }\mu\text{m}$ as shown in the XRD pattern of Figure 4-3(b). The grain growth mechanism can be interpreted as strain energy driven growth in the elastic regime. This shows the complete dominance of copper (111) texture. The texture analysis for all the samples is discussed later in this section of the thesis.

Figure 4-4: X-Ray diffraction of copper film plated at 20 mA(DC) at (*top*) $1 \text{ }\mu\text{m}$ and (*bottom*) $10 \text{ }\mu\text{m}$ thickness.

With pulse reverse electroplating at the current density of 10 mA/cm^2 , the strong (111) texture is developed at $1 \text{ }\mu\text{m}$ and $10 \text{ }\mu\text{m}$, as can be seen in the XRD pattern in Figure 4-5. Surface energy driven grain growth is the dominant mode in pulse reverse electroplating, although its exact mechanism is not clearly understood.

At the higher current density of 20 mA/cm^2 with DC electroplating, the (111) texture is dominant at the beginning. After reaching the film thickness of $10 \text{ }\mu\text{m}$, the texture is (110) at current density of 20 mA/cm^2 as shown in XRD pattern in Figure

4-4. The development of (110) texture after (111) texture is due to the deposition of grains with (110) texture at the grain boundaries [79]. The lack of reverse current will not dissolve these grains. Therefore, the texture is finally dominated by the (111) grains of copper deposits.

Figure 4-5: X-Ray diffraction of copper film plated at (a) 2 and (b) 10 mA PR at 1 μm (top) and 10 μm (bottom) thicknesses.

At the high current density of 20 mA/cm², very strong Cu (111) texture is developed at the thicknesses of both 1 μm and 10 μm . In all the cases above, the pulse reverse electroplating is always associated with (111) texture. Based on the present XRD analysis on the copper films, the grain growth mechanism in the pulse reverse electroplating is driven by the surface energy.

Figure 4-5(b) shows the XRD pattern of 1 μm and 10 μm thick copper films at a forward current density of 10 mA/cm². A strong peak associated with copper (111) can be observed. The peaks, associated with gold layer recorded due to the sample cutting

from the edge of the wafer which acts as contact area, are described in the previous chapter.

Figure 4-6: X-Ray diffraction of copper film plated at 20 mA(PR)(a) 1 μm , (b) 10 μm thickness.

Figure 4-6 shows the XRD patterns of 1 μm and 10 μm thick copper films at a forward current density of 20 mA/cm². It can be clearly observed that for both thicknesses, the (111) orientation is dominant pulse-reverse electroplating. The peaks associated with the gold layer are recorded due to the sample cutting from the edge of the wafer acting as contact area as described in the previous chapter. Cu(111) planes are the principal planes on which the sliding of layers happen to produce twinning. Growth twins can also be formed on Cu(111) as explained in Figure 4-2, in which case the stress tends to be low.

Table 4-3: Texture coefficient of electroplated copper films with different current densities.

Modulation	Current Density (mA/cm ²)	Film thickness (μm)	111	200	220
DC	2	1	1.993	0.963	0.044
DC	2	10	0.002	0.007	2.00
DC	10	1	3	0	0
DC	10	10	3	0	0
DC	20	1	0.765	0.229	2.007
DC	20	10	0.175	0.114	2.711
PR	2	1	2.597	0.403	0
PR	2	10	2.645	0.024	0.331
PR	10	1	3	0	0
PR	10	10	1.386	0.479	1.134
PR	20	1	1.555	0.738	0.707
PR	20	10	1.760	0.665	0.574

As listed in Table 4-3 calculated using the approximation equation in (4-1), the texture for all pulse reverse electroplated copper is (111) dominant at both thin and thick copper films plated on (111) sputtered gold layer. The orientation of sputtered gold seed layer is measured in the next chapter.

Table 4-4: Estimated volume fractions of different texture components of copper films.

Modulation	Current Density (mA/cm ²)	Film thickness (μm)	111	200	220
DC	2	1	0.664	0.321	0.015
DC	2	10	0.001	0.002	0.997
DC	10	1	1	0	0
DC	10	10	1	0	0
DC	20	1	0.255	0.076	0.669
DC	20	10	0.058	0.038	0.904
PR	2	1	0.866	0.134	0
PR	2	10	0.882	0.008	0
PR	10	1	1	0	0
PR	10	10	0.462	0.160	0.378
PR	20	1	0.518	0.246	0.236
PR	20	10	0.587	0.222	0.191

The above Table 4-4 shows the volume fraction of individual texture components using (4-2). This concludes that the number of grains with (111) texture is

dominant for pulse-reverse electroplating with both thin and thick copper films. The development of (111) texture coincides with the fact that (111) planes are the principal twinning planes in FCC metals. The sliding of atomic layers on (111) planes induces the formation of stacking faults and twinning.

4.4 Microstructural and surface morphology studies by FIB and SEM

Chloride and sulfuric acid content and additives in electrolyte affect morphology, grain size and shape [80]. SEM and AFM are the best characterization tools to characterize such quantities. The following Figure 4-7 and Figure 4-8 show the cross-sectional ion images and surface SEM images of the copper films fabricated with pulse reverse current density of 20 mA/cm². There are granular grain structures which are different from the common long fiber grain structures usually obtained with the direct current method. In order to examine the grain structure of copper films, films are vertically etched by the ions in focused ion beams to a depth of approximately 8 μm after which the side wall is scanned with ion beam for microstructural observations. Although granular grain structure is observed, the lengths of fibrous grain are less than the thickness of the copper film. This shows that pulse-reverse electroplating produces finer grains than conventional DC plating.

Pulse-reverse plating mode reduces the grain sizes by disturbing the excessive grain growth. However it associates with the creation of new nucleation sites at defect such as impurity incorporation points, at kink sites and at dislocation sites. Impurity incorporation is one of the factors even if all other parameters are assumed same. Therefore, higher impurity levels associate with smaller grain sizes and higher density of grains with nano-scale twinning. Nanoscale twinning is also one of the intragranular defects which are formed due to various reasons. One of them is the stress induced twinning as will be discussed in chapter 6.

Figure 4-7: Cross-sectional ion image of copper film fabricated with a pulse reverse current density of 20 mA/cm^2 .

Figure 4-8: SEM image of copper film fabricated with a pulse reverse current density of 20 mA/cm^2 .

As shown in Figure 4-8, the surface of the sample does not exactly resemble the grain structure. Surface reconstruction may have taken place due to the storage of the sample a few weeks before the examinations.

Figure 4-9: (a) Cross-sectional ion image (b) magnified view of copper film fabricated with a pulse reverse current density of 2 mA/cm^2 .

Figure 4-9 shows the cross-sectional ion image of the structure of copper plated with a low current density of 2 mA/cm^2 . Figure 4-9b shows the detailed features of the structure of copper. It can be observed that the small pores at the bottom of the copper films are mainly at the inter-granular sites. Ultra-low current densities may have created ultra-fine grains with excess vacancies. During room temperature

recrystallization, the diffusion of vacancies to grain boundaries sites induces the small pores at the grain boundaries.

Figure 4-10: SEM picture of copper surface plated with DC modulation.

Figure 4-10 shows the surface morphology of copper plated with direct current. The surface appears to be more granular due to direct current modulation. Continuous growth of copper without interruption produces a surface with a more granular morphology.

4.5 Texture evolution of copper films after ultra-long duration of room temperature recrystallization

The samples described previously are stored at room temperature in a clean environment for an ultra-long duration of 4.5 years. After such a long recrystallization period, the samples are examined with three dimensional XRD to evaluate the texture evolution. Two samples with a thickness of 10 μm fabricated by a direct and pulse-reverse current density of 20 mA/cm² are evaluated. The current density of 20 mA is chosen due to the practical interest for TSV fabrication as shown in Chapter 0.

Figure 4-11: XRD pattern of copper film with PR plating.

Firstly, the two theta scans are performed to measure the peak positions and the measured XRD patterns are given in Figure 4-11 for sampling with pulse-reverse electroplating. With this method, more accurate information such as information on texture, pole figures, inverse pole figures and the orientation distribution function (ODF) can be obtained for detailed analysis. The spot size of the x-ray beam on the sample is approximately 3 mm so that the analysis is statistically significant especially when analyzing the thin films with microstructure of a few to tens of micrometers. Figure 4-12 shows the x-ray optics [81] for the measurement of the texture of copper film. The experimental parameters of the XRD setup are a tube voltage 40 kV and current of 30 mA. X-ray diffraction intensities were measured as a function of tilt angle α with respect to the surface normal and the angle of rotation β in the plane perpendicular to the normal direction. The range of tilt angle tested is from 0 to 75 degrees at the interval of 5 degrees, and 0 to 355 degrees for angle of rotation.

Figure 4-12: X-ray diffraction configuration for measurement of texture.

Table 4-5: Texture evolution after an ultra-long period of room temperature storage.

	111	200	220
DC 20 mA (10μm) before recrystallization	0.175	0.114	2.711
DC 20 mA (10μm) after recrystallization	0.162	0.317	2.521
PR 20 mA (10μm) before recrystallization	1.760	0.666	0.574
PR 20 mA (10μm) after recrystallization	1.363	1.07	0.568

Table 4-6: Volume fraction of different texture components after an ultra-long period of room temperature storage.

	111	200	220
DC 20 mA (10μm) before recrystallization	0.058	0.038	0.904
DC 20 mA (10μm) after recrystallization	0.054	0.106	0.840
PR 20 mA (10μm) before recrystallization	0.547	0.222	0.191
PR 20 mA (10μm) after recrystallization	0.454	0.456	0.189

It can be deduced from Table 4-5 and

Table 4-6 that the volume fraction and texture are still (111) dominant after a long period of room temperature recrystallization, where the DC plated copper remains non (111) dominant as previously measured. As will be shown in the following section, pulse-reverse electroplated copper still possesses some stored energy to be released. The volume fraction of (111) slightly decreased with the slight increase of (200) volume fraction, showing that recrystallization takes a longer time in pulse-reverse plating. It is a favorable kinetic condition since it will take longer for copper to recrystallize and de-twin. (111) textured copper foils were previously observed to have strong electrical and mechanical properties [82].

Figure 4-13 shows the pole figure of copper film plated with 20 mA/cm² with a weak texture of (110). In Figure 4-4, the XRD pattern performed after two weeks of deposition also shows a strong (110) texture. Therefore it can be concluded that the texture of copper films plated with direct current is stabilized after a short period of room temperature recrystallization. A (220) texture is also reported in previous studies with a high current density of 160 mA/cm² [81]. This shows that strain energy minimization is a primary factor, and once the minimization is finished after a short period of recrystallization (about two weeks), the structure is stabilized with no further evolution in texture.

Figure 4-13: Pole figure of copper film with direct current plating

Figure 4-14: Pole figure of copper film with pulse-reverse plating

It can be observed in Figure 4-14 that the relative intensity of the (220) peak has increased when compared to the XRD pattern in Figure 4-6, which was measured after two weeks of deposition. Note that the pole figure measurements were performed after

an extra-long period of recrystallization (4.5 years). Previous studies on the preferred orientations in electrodeposited metals show a similar trend with Cu (111) orientation for depositions with low overpotential [83].

4.6 Effect of aged plating solution on microstructure of films

The ageing of an electrolyte has a strong influence on the properties of the deposit. In the present study, the microstructures of the copper films plated with aged electrolyte solution are studied. It is shown that the aged solution produces large grains with less twinning structure.

Figure 4-15: Surface SEM image of cross-section of copper film plated in aged electrolyte solution.

Figure 4-15 shows the SEM picture of the copper foil electroplated in the aged electrolyte solution. The composition of the electrolyte is the same as listed. The picture was taken three days after the deposition, just after the previously reported room temperature recrystallization. The surface twins are seen clearly in the SEM picture, just like in previous literature [84]. However, the following cross-sectional ion image of the film in Figure 4-16 shows large grain sizes with less twinning. Hence, the aged electroplating solution has a significant effect on copper deposition and its microstructure.

Figure 4-16: FIB image of cross-section of copper film plated in aged electrolyte solution.

4.7 Electrical property of the pulse-reverse electroplated copper

Electrical resistivity is an important parameter since it directly correlates with the microstructure of copper. Immediately after the electrodeposition, ultra-fine grain boundaries are obtained. This phenomenon is especially obvious with pulse-reverse or pulse electrodeposition. At the initial phase of recrystallization, the electrical resistivity of copper is higher due to the scattering of electrical current. The sources of scattering are grain boundary scattering and impurity scattering. As the grains begin to grow by accumulating smaller grains and impurity sites diffuse to grain boundaries or surface, the level of scattering is decreased. Therefore, continuous or ex-situ measurement of electrical resistivity gives relevant information about the microstructure of copper. In order to measure the electrical resistivity, a small structure as shown in the insert of the following figure is fabricated using lithography. The four-probe electrical measurement method is used to measure the current and potential across the two ends of the structure. The curve in Figure 4-17 shows the voltage-current (IV) characteristics of the

electroplated copper after more than one week of fabrication. It is shown that the electroplated copper has almost as much resistivity as the bulk copper.

Figure 4-17: Measurement of IV characteristics of copper.

4.8 Differential Scanning Calorimetry (DSC) studies of PR copper foils

Electrodeposited copper is known to have a strong tendency to recrystallize during and immediately after the electrodeposition process. The recrystallization and grain growth and their relation to the formation of twinning and their role in the impurity and stress level in FCC functional material such as copper are still under active investigation. Differential scanning calorimetry has been applied to such investigations in metals, although this technique is best applied to soft materials such as polymers.

At the beginning of every cycle of electrodeposition, impurity species such as sulfur, chlorine and carbon are adsorbed and incorporated into the electroplated bulk copper. Pulse-reverse electrodeposition is a more complex electroplating technique.

Due to its complicity, a simple analytical model of adsorption and growth is not available. It also is known to have the ability to produce fine grain sizes with a high density of nano-scale twinned copper as shown previously. Previous DSC studies using direct current on 8 mA/cm^2 plated copper show that the activation energy for grain growth is 0.85 eV/atom . However, similar detailed studies in the case of pulse-reverse plating are lacking. The recrystallization behavior of PR-plated copper needs to be investigated. Copper is known to recrystallize at about 300°C [85]. However, room temperature crystallization happens at much a lower temperature of around 100°C . Therefore DSC measurements are carried out at the maximum temperature of 300°C .

The DSC measurements were performed in an inert gas atmosphere using Perkin Elmer DSC system. The weight of the copper thin film during measurements is approximately 10 mg. Aluminum containers are used for both the copper sample and reference specimen. The sample temperature was increased to 300°C at 10 degrees per minute. Two complete thermal cycles were performed in DSC analysis. The endothermic responses are plotted above the baseline in the figure. DSC measurement results show the latent energy in the pulse-reverse electroplated copper. This may be due to the increased incorporation of impurities and finer grain structures that usually comes with pulse-reverse electroplating.

Figure 4-18: DSC measurement curve of DC plated copper film.

The free energy of deformed/strained crystal is greater than that of annealed crystal. The difference is approximately equal to the energy stored in the form of strain. Plastic deformation of ultrafine grains during electrodeposition may increase the entropy of the copper. However, this is much smaller than the strain energy stored in the crystal.

Therefore, the free energy equation

$$\Delta G = \Delta H - T\Delta S \quad (4-3)$$

can be approximated as

$$\Delta G \approx \Delta H \quad (4-4)$$

where ΔG is the free energy associated with deformation or strain, ΔH is enthalpy or stored strain energy, ΔS is the entropy increase due to cold work and T is absolute temperature. The energy term due to entropy increase $T\Delta S$ is negligible. Therefore the release in energy (exothermic) in the copper film is due to the release of strained energy stored in the copper during deposition to rearrange the atoms into crystals with lower free energy. The stored energy might have originated in the impurity incorporation or was induced by stress during electrodeposition. Therefore, it can be concluded that pulse-reverse electroplated copper stores more energy than direct current electroplated copper.

Figure 4-19: DSC measurement curve of PR plated copper film

As can be seen in the above Figure 4-19, a broad exothermic peak at the temperature 100°C is observed while it disappears in the second cycle. The observed variation in the heat flow with respect to the DSC curve of DC electroplated copper is due to the recrystallization of pulse-reverse electroplating.

Therefore, in the case of pulse-reverse electroplating, higher levels of impurity incorporation may act as the Zener pinning effect in the bulk of the copper. The recrystallization of copper has been kinetically slow due the pinning effects as shown in the DSC of the pulse-reverse electroplated copper film. The incorporation of impurity species such as sulphur, chlorine and copper has previously been studied using TEM, AES and SIMS in the literature and is shown in a previous chapter in the case of TSV fabrication in pulse-reverse electrodeposition.

4.9 Summary

Extensive studies of crystal orientation, texture, recrystallization of copper during ultra-long duration of room temperature storage have been conducted. Images of grain structure of copper films deposited with pulse-reverse electroplating are investigated. The effects of various current densities are also examined. It can be concluded that the use of pulse-reverse application provides the preferred orientation of (111) in the direction perpendicular to the electroplating surface in large area plating. As the (111) plane is the principal twinning plane in FCC crystals, the twinning mechanism of copper in pulse reverse electroplated copper is related to the preferential recrystallization texture. Additionally, pulse-reverse plating was proven to produce void-free high-aspect ratio TSV for practical applications, and it also provides copper deposits with a highly twinned structure. Therefore, it is shown to have the potential to be developed into commercial technology applications.

Initial Nucleation and Stress Measurement of Pulse-reverse Copper Deposition

5.1 Introduction

Electrochemical nucleation of deposit metals is an important phenomenon from both the scientific and technological points of view, due to the anisotropic properties of deposited material on the same substrate. The rate of nucleation determines the vacancy and stress level, texture and grain size of the deposit material. Under different electrochemical environments such as substrate material and its orientation or texture [81], the chemical composition of the electrolyte, electrodeposition parameters such as overpotential and the use of additives all have a strong influence on the properties and structure of deposits, which have strong impact on the practical applications such as interconnects in microelectronics, MEMS. The material of the seed layer and its texture are also important, since they affect the rate of nucleation due to differences in surface diffusion parameters of the seed layer and its surface orientation [86].

5.2 Experimental details

Silicon wafers (100) of four-inch diameters are cleaned in the sulfuric acid and oxygen peroxide solution at 120°C for 20 minutes. The resistivity of the wafer is 0.01 to 20 Ω -cm. The wafers are cleaned in acetone under ultrasonic agitation to remove organic contaminants. The cleaned wafers are brought into the sputtering vacuum chamber equipped with both DC and magnetron sputtering heads. The sputtering gas in the chamber is argon. The chromium layer is used as the adhesion layer for the present study. After sputtering a chromium layer of thickness 20 nm, a gold layer of 200 nm is sputtered without breaking the vacuum. A relative low pressure of 0.01 mbar is used to ensure that impurities are trapped into the sputtered films.

After sputtering the seed layer in the sputtering process, the wafers are cut into pieces for the electrochemical experiments. The potentiostat from CHI instrument is used in the following electrochemical study. The compositions of the electrolyte used in the experiments are listed in the following table. Since the objective of the study is to determine the nucleation of copper with pulse-reverse current modulation, pulse current with cathodic and anodic currents are used to deposit the copper on the sputtered gold layer on the silicon substrate. A commercially pure copper piece is used as the anode. The overpotentials are measured with respect to the Ag/AgCl electrode.

Figure 5-1: Experimental measurement of pulse reverse current.

Figure 5-1 shows the potential response of electrolyte to the applied current in the CHI electrochemical workstation. The initial few cycles in the waveform require a higher potential due to the interface with the sputtered gold surface. The effects of other species in electrolyte solution may also mean a higher potential to drive the electrochemical reaction is required.

5.3 Fabrication of micro diaphragms on SOI wafer for stress measurement

SOI wafers with handle layers of thickness 350 μm are used. The device layer and oxide layer thickness are 2 μm . The wafers are cleaned before the 200 nm thick seed layer of gold is sputtered on the device layer of the wafer. An adhesion layer of 20 nm thickness is deposited before gold sputtering without breaking the chamber. The sputtering process produces (111) textured gold thin films as described. After sputtering the seed layer, deep reactive ion etching is done on the reverse side of the wafer (handle layer). Holes of 3 mm diameters are etched after photo-lithographically defining positive AZ 9260 photoresist. After the buried oxide layer is exposed, the oxide layer is removed in a buffered oxide etching solution to obtain the final diaphragm of silicon with a thickness of 2 μm .

5.4 Micro-Raman spectroscopic measurement of stress in electroplated copper

Micro-Raman can be used to investigate the stress in the material [87]. The study of intrinsic stress in physical vapor deposition [88] shows that tensile stress builds up in metals with high melting points while compressive stress builds up in metals with lower melting points. It is more involved in the case of electrochemical deposition due to its complex non-equilibrium nature during electrochemical phase transformation. There are many sources of tensile and compressive stress in metal deposition. And the exact nature and origin of such stresses are not well understood [89], although some possible mechanisms have been proposed in the past. The difficulty arises from the fact that the stress in the electro-deposit is a microscopic phenomenon and it is difficult to observe even with the most advanced analytical

methods such as combined EBSD and TEM analysis. Therefore, macroscopic measurements still provide valuable information.

Figure 5-2: Schematics of silicon diaphragm for stress measurements.

Figure 5-2 shows the schematics of SOI silicon diaphragm for measurement of stress in micro-Raman spectroscopy. Since only silicon will give the Raman response in this spectroscopic method, the stress as indicated by the Raman shift is due to the stress in the silicon. Therefore, the finite element method is used to calculate the stress in the electroplated copper, taking the stress measured as input into the finite element model.

Figure 5-3: Raman scattering from the stress free Si (100) surface at 520 cm^{-1} .

Figure 5-3 shows the typical signal of Raman spectroscopy from silicon (100) surface. The stress free silicon surface $\langle 100 \rangle$ direction has a Raman scattering at the wavelength of 520 cm^{-1} . The peak position shifts depending on the amount of strain or stress in lattice in the silicon diaphragm.

Figure 5-4: Stress evolution in copper with (a) leveler alone and (b) brightener and leveler.

Figure 5-4(a) shows the evolution of stress in copper after electroplating the copper using pulse-reverse deposition on (111) textured sputtered gold. Figure 5-4(b) shows the stress evolution in copper plated from the electrolyte with both brightener

and leveler. Three or four measurements as shown in the figure are carried out to ensure the accuracy of the measurements. The stress evolution is measured in the first two hours after deposition.

Equation 3-18 in a previous chapter shows the simple relationship between Raman shift and stress in the silicon (100) surface. A bimorph structure with silicon and copper layers is used to calculate the stress in the copper. The clamped bimorph structure is heated to produce the level of stress in silicon measured in the Raman experiment by increasing the temperature of the whole model. When the calculated stress in silicon diaphragm is equal to the measured stress, the stress in the copper layer is taken from the finite element result.

Figure 5-5: FEM calculation of stress in silicon and copper layers.

Figure 5-5 shows the finite element calculations of stress in the copper and silicon diaphragm. The graphs show the stress evolution over time within one hour since deposition. The calculations are performed for the case of the brightener and leveler components of organic additives in the electrolyte. The varying levels of stress in copper show the varying levels of GSFE in copper crystal and hence twinnability, which will be shown in the next chapter.

5.4.1 Texture of sputtered gold seed layer

Figure 5-6 shows the XRD pattern of the sputtered gold layer on the silicon substrate. A peak of very high intensity which can be observed around 38 degrees is the peak associated with Cu(111). No other peak in the entire spectrum can be observed. Therefore, it is assured that the sputtered gold thin film are (111) textured. The underlying seed layers have a strong influence on the initial nucleation and subsequent crystallization of copper in electrodeposition. The XRD examination in the present work ensures that the initial nucleation of copper in pulse-reverse electroplating on copper (111) textured seed layer is studied.

Figure 5-6: XRD for gold seed layer.

5.5 XRD examination of copper initial nucleus

The seed layer morphology and structure have strong influence on the electro crystallization of copper. Therefore, XRD measurement on the copper seed layers is performed to understand the nature of sputtered gold thin film on silicon. XRD measurements are performed on the specimens of silicon substrate with sputtered gold layer. Measurements are done one week after the sputtering process. This length of time between the sputtering process and XRD measurements ensures that the room

temperature recrystallization is complete. One week is enough because the gold thin film is only less than 100 nm thick.

Figure 5-6 shows the XRD pattern of sputtered gold on silicon (100) wafer. It is clear that except the peak associated with Au(111) around 37 degrees, no other peak was observed. It can be observed that almost all the grains are (111) oriented along the direction normal to the surface of the wafer.

Figure 5-7: (a) XRD for gold seed layer with electroplated copper and (b) magnified at Cu(111) peak

Figure 5-7 shows the XRD pattern after depositing the copper on the seed layer with pulse-reverse plating. Only a few minutes of plating is done to ensure that a very thin layer of copper is deposited on the gold layer. The use of precision potentiostat enables accurate control of current. From the XRD pattern, only the peak associated with Cu (111) is observed. This shows that almost all of the grains are (111) oriented in the direction perpendicular to the surface. Therefore, sputtering gold thin film on silicon substrate is a reliable method to produce (111) textured thin film.

5.5.1 Sputtered gold thin films

The sputtered gold thin films on the silicon wafers are characterized by atomic force microscopy (AFM) and X-ray diffraction (XRD) to evaluate texture, surface morphology and roughness.

5.6 Morphology studies by AFM

The surface morphology of 200 nm thick copper layer was studied by the SEM and AFM in tapping mode. The following Figure 5-8 shows the surface profile of the gold seed layer.

Figure 5-8: AFM of surface morphology of sputtered gold seed layer.

The figure shows the nucleus sizes of sputtered gold film to be approximately 100 nm. The scanning is done on a 2 μm by 2 μm area to ensure that the localized defects are not significantly scanned in the image. This allows the comparison of nucleus size after plating copper on the sputtered gold seed layer.

Figure 5-9 shows the AFM measurement of the sample after deposition of copper. It shows the similar surface topology as that of gold seed layer in figure Figure 5-8, but with increased grain sizes. Atomic force microscopy has been used to study the nucleation and deposition of copper in industrial application. Measurements such as roughness of deposits on surface [90] and in trenches [91] reveal the mechanisms of copper deposition with particular plating techniques.

Figure 5-9: AFM of copper electroplated on gold seed layer.

Previous studies with sputtering of copper on different substrates show the strong effects of texture and surface wettability on the twin boundary formation [92].

Figure 5-10: AFM of sputtered gold seed layer.

Figure 5-10 shows the surface morphology of the sputtered gold seed layer. Very small grain sizes of less than 100 nm can be observed.

Img. Z range	11.429 nm
Img. Mean	-0.000000 nm
Img. Raw mean	39.663 nm
Img. Rms (Rq)	1.091 nm
Img. Ra	0.865 nm
Img. Rmax	11.429 nm
Img. Srf. area	4.021 μm^2
Img. Prj. Srf. area	4.000 μm^2
Img. Srf. area diff	0.523 %

Figure 5-11: Roughness measurements of the sputtered gold seed layer.

Figure 5-11 shows the results of roughness measurements on the gold seed layer. The variation in z-direction is only 11.42 nm. Figure 5-12 shows the atomic force microscopy image of initial copper nucleation after 10 seconds of copper deposition in pulse-reverse current modulation. The image shows that the grains are not much larger in size than that of gold seed layer.

Figure 5-12: AFM characterization of electrodeposited copper on gold seed layer.

Figure 5-13: Magnified view of copper initial nucleus on gold seed layer.

Img. Z range	76.130 nm
Img. Mean	-0.000004 nm
Img. Raw mean	395.80 nm
Img. Rms (Rq)	10.256 nm
Img. Ra	8.296 nm
Img. Rmax	76.130 nm
Img. Srf. area	1.096 μm^2
Img. Prj. Srf. area	999999 nm^2
Img. Srf. area diff	9.571 %

Figure 5-14: Roughness measurements of electroplated copper on gold seed layer.

Figure 5-13 shows the detailed surface measurement on a smaller scanning area of $1 \mu\text{m} \times 1 \mu\text{m}$. Figure 5-14 shows the results of roughness analysis after depositing copper. It is observed that the difference in surface area has increased to 9.57 percent from 0.52 percent as shown in Figure 5-11. The range in the vertical Z direction also increased from 11.429 nm in Figure 5-11 to 76.130 nm after copper deposition. The initial nuclei of copper with diameter less than 60 nm has been deposited onto the (111) textured gold seed layer.

Figure 5-15: EDX spectrum of sample with electrodeposited copper on random point.

Figure 5-15 shows the EDS spectrum at a random point of the electroplated gold seed layer while Figure 5-16 shows the spectrum of the entire scanning area. Both of them show a similar composition.

Figure 5-16: EDX spectrum of sample with electrodeposited copper on scanning surface.

Figure 5-17 shows the area from which the EDX data is taken. In both cases, the atomic composition of copper is about 27 percent while the rest of the matrix is the gold seed layer.

Figure 5-17: SEM picture showing the scanning area for EDX measurements.

As can be seen in the SEM picture, the collection of data from a surface area of approximately $120\ \mu\text{m} \times 100\ \mu\text{m}$ has been performed. As such, this rules out the possibility of localized inconsistencies in atomic concentration at point measurements.

5.7 Discussion and Summary

The initial nucleation of copper on (111) textured sputtered gold seed layer in pulse-reverse electrodeposition is studied. It is found that (111) textured initial nucleation of copper is deposited under pulse-reverse electroplating conditions as investigated by the ex-situ XRD and AFM studies. Surface topology measurements show that the size of initial nucleation is similar to that of the seed layer. The measurements by micro-Raman spectroscopy show the stress induced in the deposited copper thin film. The varying levels of stress in the copper significantly affect the GSFE of the copper on its principal twinning plane, as will be shown in the following chapter 6.

Chapter 6

Ab initio theory of modified GSFE and twinability under biaxial strain and electromigration reliability

6.1 Introduction

In this chapter, first principle quantum mechanical methods are employed to investigate the mechanical and electrical properties of nano-twinned copper within the framework of Density-Functional Theory (DFT). The development of the DFT in both theoretical methods and numerical algorithms, together with advancement in computing has allowed a new branch of investigation in which the properties of real materials can be accurately predicted with minimal experimental parameters [93]. Calculations based on DFT calculations are used to evaluate the effects of stress/strain on the generalized stacking faults of the copper. Twinability of copper under strained conditions is also calculated. The theory of generation of deformation twins in nanocrystalline materials within the framework of classical linear elasticity is given in the article by Gutkin et al [94].

6.2 Density-functional theory

Hohenberg-Kohn proposed the theory of inhomogeneous electron gas theory [95]. Kohn-Sham's Density Functional Theory is the central pillar of the so-called modern day standard model of material science. Within the framework of Density-Functional Theory, it can be proved that experimental observables can be calculated in terms of ground state electronic distribution in the crystal lattice. The development of Density Function Theory allows the calculation of complex material properties from first principles based on quantum mechanics.

Figure 6-1: Self-consistent cycle for ground state energy calculations in DFT[96].

6.2.1 Hamiltonian of the solid

The complete hamiltonian of the solid is given by the following equation [96]:

$$\begin{aligned}
 \hat{H} = & -\frac{\hbar^2}{2m_e} \sum_i \nabla_i^2 - \sum_{i,l} \frac{Z_l e^2}{|r_i - R_l|} \\
 & + \frac{1}{2} \sum_{i \neq j} \frac{e^2}{|r_i - r_j|} - \sum_l \frac{\hbar^2}{2M_l} \nabla_l^2 + \frac{1}{2} \sum_{l \neq j} \frac{Z_l Z_j e^2}{|R_l - R_j|}
 \end{aligned} \tag{6-1}$$

where lower case subscripts denote electrons and nuclei are denoted by upper case with charge Z_l , electronic charge e , electronic mass m_e , electronic displacement vector r , nuclear displacement vector R , Plank's constant $\hbar$ and mass M_l . (6-1 is too complicated to be solved within reasonable time because of the inclusion of all the

ionic and electronic degrees of freedom. It can be reduced to a simpler form as explained in the following section.

6.2.2 Born-Oppenheimer approximation

Born-Oppenheimer approximation is based on the assumption that the election motion of the electrons in the lattice and nuclear motions of the atoms in the solids can be separated, since the electrons are much lighter than the ions by many orders of magnitude. Except for hydrogen, the lightest element, wherein its nucleus is treated as a quantum-mechanical particle, this approximation is applicable to all other elements. After ignoring the kinetic energy terms, the hamiltonian of the solid becomes [96]:

$$\begin{aligned} \hat{H} = & -\frac{\hbar^2}{2m_e} \sum_i \nabla_i^2 - \sum_{i,l} \frac{Z_l e^2}{|r_i - R_l|} \\ & + \frac{1}{2} \sum_{i \neq j} \frac{e^2}{|r_i - r_j|} - \frac{1}{2} \sum_{l \neq j} \frac{Z_l Z_j e^2}{|R_l - R_j|} \end{aligned} \quad (6-2)$$

The last term is the Madelung energy which is just a constant. After the above simplifications, the hamiltonian of the solid can be described as [96]:

$$\hat{H} = -\frac{\hbar^2}{2m_e} \sum_i \nabla_i^2 + \sum_i V_{ion}(r_i) + \sum_{i \neq j} \frac{e^2}{|r_i - r_j|} \quad (6-3)$$

Even with the above simplifications, the hamiltonian of the solid is difficult to solve due to the nature of electrons. Density Functional Theory uses electron density as the primary quantity rather than the many-body wavefunction to further simplify the complexity of the many-body problem in solids. Since the copper is a conducting metal with distributed electronic structure rather than localized bonding as in carbon, methods which involve the overlapping of atomic wave functions are not suitable in this case. Ab-initio methods such as planewave pseudopotential method can be used to reliably

predict the properties of metallic systems. In planewave calculation, the difference of 6 meV is calculated in HCP and FCC site of copper (111) interface.

6.2.3 Hohenberg-Kohn theorems and Kohn-Sham equations

Instead of dealing with the complex many-body wave function, the Hohenberg-Kohn-Sham theory based on the Thomas-Fermi-Dirac approximation proved that the ground state density $n(r)$ is a unique solution to any many-body system with a given external potential. This theory allows the great simplification of solving for only scalar function $n(r)$.

The resulting Kohn-Sham hamiltonian is[96]:

$$\widehat{H}_{KS} = \widehat{T}_0 + \widehat{V}_H + \widehat{V}_{xc} + \widehat{V}_{ext} \quad (6-4)$$

$$\widehat{H}_{KS} = -\frac{\hbar^2}{2m_e} \nabla_i^2 + \frac{e^2}{r\pi\epsilon_0} \int \frac{\rho(r)}{|r-r'|} dr' + V_{xc} + V_{ext} \quad (6-5)$$

where exchange and correlation potential is given by:

$$\widehat{V}_{xc} = \frac{\delta V_{xc}[\rho]}{\delta \rho} \quad (6-6)$$

The ground-state density $\rho(r)$ is

$$\rho(r) = \sum_{i=1}^N \phi_i(r)^* \phi_i(r) \quad (6-7)$$

where $\phi_i(r)$ are the single-particle wavefunction of the Kohn-Sham equation

$$\widehat{H}_{KH} \phi_i = \varepsilon_i \phi_i \quad (6-8)$$

where ε_i denotes the eigen-energy of the electronic system. However, it is noted that the calculated energy eigenvalues do not represent the spectroscopic energies as they

are eigenvalues of the Kohn-sham operator rather than the many-body hamiltonian operator. However, the total energy can be used to calculate parameters such as GSFE and twinability.

6.2.4 Planewave pseudopotential method

Planewaves are the fundamental solutions of the Schrodinger wave equation. Without the effects of nuclear charges, planewaves are the exact solution of the Schrodinger equations. The orthogonality of planewaves also make them a convenient choice for solving Schrodinger equations. Since the inner electron of the atoms does not participate in the bonding of atoms in condensed matters, it can be replaced by a pseudopotential which has the same scattering properties as full atomic potential. A review of the pseudopotential method and its applications in different aspects of condensed matter systems can be found in Pickett [97].

6.2.5 Pseudopotentials

The existence of core states in the atoms makes the use of planewaves as a basis set for the solution of solid state Hamiltonian difficult due to the very complex wavefunction near the nucleus. However, the involvement of electrons in the chemical bonding process is mainly due to the outer electrons. The core/inner electronic configuration is almost inert to the chemical environment of the atom. Therefore, in the theory of pseudopotential, the core state of the atoms is approximated into the effective potential. As such, only the charge density of the valence electrons is calculated, reducing the computational cost of calculations.

6.2.6 Planewave cut-off energy and k-point convergence

In practical calculations, only a limited number of planewaves is used, i.e. only the finite basis set is used, since the higher energy Fourier components of the solution

are relatively less important. The cut-off energies for planewaves in DFT calculations are given by the equation:

$$\frac{\hbar^2 |k + K|^2}{2m} = E_{cut} \quad (6-9)$$

where k is vector in reciprocal space and K is the reciprocal lattice vector in the same space. A large energy cut-off is usually needed to achieve a converged solution which gives the correct ground state energy and associated charge density.

6.2.7 Pulay stress in DFT calculations

Pulay stresses occur in the computation of stress tensor using the density functional theory due to the incomplete basis set employed during the calculations. This stress miscalculation is especially important in the computation of strain energy due to its dependence on the computation volume. There are generally two acceptable ways to minimize the Pulay stress. The first is the use of much larger cut-off energy. When the cut-off energy is higher, the calculated energy is more accurate and a converged solution is obtained. The second is to use constant cut-off energy rather than a fixed number of planewaves in the case of the planewave pseudopotential method.

6.3 Structure of (111) twin in copper

Recent experimental work reports two different kinds of twins in copper, which are incoherent and coherent twins. The deformation mode of twinning happens on the slip planes. Therefore, it is important to note the slip systems of the FCC crystal structure. The three slip systems in FCC are [98]:

- $\{111\}\langle 110 \rangle$, which is the principal slip system for FCC crystal structure and also the plane on which stacking faults are formed
- $\{100\}\langle 110 \rangle$ slip, which were reported at high temperature

- $\{110\}\langle 110 \rangle$ slip, which has been observed in high temperature ranges after impact loading
- $\{212\}$ slip system, which form incoherent twin boundaries

Coherent twin boundaries are the twins across $\{111\}$ planes while the incoherent twin boundaries are the observed twins across $\{212\}$ planes. It is also known that the incoherent twin boundaries are thermally instable compared to their $\{111\}$ counterparts, due to the higher amount of energy stored in their boundaries. However, the two types of twins are related in that a set of coherent twin boundaries end in the FCC matrix forming incoherent twin boundaries.

Figure 6-2: Schematic illustration of pinning of grain boundaries

As shown in the previous chapters and in related literature, the (111) texture of copper is developed in pulse and pulse-reverse electroplating. Therefore, one of the possible mechanisms for deformation is the impurity or atom pinning at the grain boundaries acting as a source of high stress in the localized regions of the grain. That can explain why a level of low stress is observed where twinning occurs. The schematic of the grain boundary pinning is given in Figure 6-2. When the localized pinning of grains happens, localized stress is larger than average stress measured by conventional methods.

6.4 Twinning mode of deformation and twinability

The tendency of metals to deform to form twins is defined by a parameter called twinability which is a function of various stacking fault energies. The theory of twinning as a mode of deformation is proposed by Tadmor et al. [99] followed by the ab-initio calculations [17,100]. The twinability (τ_a) of FCC metals is given by

$$\tau_a = (1.136 - 0.151 \frac{\gamma_{ist}}{\gamma_{ut}}) \sqrt{\frac{\gamma_{us}}{\gamma_{ut}}} \quad (6-10)$$

The proposed theory of deformation twinning was originally designed to explain the twinning at the crack tip region in fracture mechanics. However, twinning deformation due to applied stress has been reported for many FCC metals such as aluminum and copper. In the context of copper twinning in electroplated copper, it was proposed that a large amount of stress is induced in deposit under certain conditions.

6.4.1 Generalized stacking fault energies

Generalized stacking fault energies are introduced by Vitek [101] and have been calculated for many FCC metals [102]. The single layer stacking fault energy is calculated by translating the upper half of the crystal along $\langle 112 \rangle$ direction. The energies as a function of the displacement along the deformation movement are termed generalized stacking fault energies. Stacking fault energies are directly influenced by the electronic structure of solids. Figure 6-3 shows the shifting of layers together with corresponding stacking fault energies and their atomic configurations.

Figure 6-3(a) shows the original FCC copper lattice with (111) planes depicted as individual layers. Sliding of upper half of the lattice produces the stacking faults as depicted in red color at the interface. Formation of another stacking fault within the

upper half of the lattice produces the nucleation of twin which is depicted as **BCB** in Figure 6-3(c). Continuation of this process form the repeated sliding of (111) planes which produce wider twins as notated as **ABCBA** and **BACAB**. In these two cases, the **C** planes depicted in red will acts as the mirrors across which twinning happens. The process may repeat under various conditions such as stress, phonon action.

Figure 6-3: The shifting of (111) FCC planes along (-1-12) direction, (a) stacking fault configuration, (b to c) shows the formation of a micro twin and, (d to e) shows the twin migration[16].

6.4.2 Atomic structure and ionic relaxation calculations

All the calculations were carried out using the PWscf suite of software [103]. Large cut-off energy for the planewave basis set is used to achieve a well-converged charge density and ground state energy. In the ionic relaxation calculations of the twinning process, stringent criteria for atomic force calculations are used to ensure the convergence of geometrical structure of lattice. Relatively thick slab geometry (16 layers) was chosen to avoid the possible quantum size effects in periodic slab calculations in DFT [104].

6.5 Computational supercell and details

The sampling points integration is done by using the method proposed by Methfessel [105] with Generalized Gradient Approximation (GGA) density functional approximation [106]. Similar calculations to investigate the ideal tensile strength under transverse biaxial stresses have been reported [107]. Previous calculations show that the valence electron structure affects the mechanical properties of metals [108] and also aluminum was shown to possess higher ideal shear strength than copper, and its strength is strongly dependent on stress in the bulk.

All the calculations are performed with the density functional package PWscf using the ultrasoft pseudopotential with Perdew-Burke-Ernzerhof (PBE) functional [106]. A planewave basis set up of 30 *Ry* and charge density cutoff of 300 *Ry* are used. The first Brillouine Zone (BZ) is sampled with Γ -centered 20 X 20 X 1 grid. The total energies of the perfect FCC crystal with 14 atoms supercells are calculated with increasing finer k-grid until the energy converged to 0.1 *meV/atom*. The smearing method of Methfessel-Paxton [109] is used to perform BZ integration with the smearing parameter of 0.02 *Ry*. The supercells having 15 and 16 layers in the $\langle 111 \rangle$ direction with each layer containing one copper atom are used for the evaluation of Intrinsic Stacking Fault (ISF) energy and Extrinsic Stacking Fault (ESF) energy respectively. Figure 6-4(a) shows the schematic of the computation unit cell used in the calculations, with A, B and C showing the stacking sequence as described in the following. Figure 6-4(b) is the crystallographic illustration of the computational supercell. The vacuum layer with the thickness of eight atomic layers at the top of the cell is employed to isolate the cells from interaction with its periodic image. The theoretical lattice constant of 6.944 *bohr* is used for calculation to avoid the introduction of artificial stress occurred due to the density functional approximation. The

overestimation of lattice constant in gradient corrected pseudopotentials has been reported previously. However, they tend to give accurate predictions with their theoretical lattice values [110]. The vacuum layer approach is used in calculations to avoid the variable cell optimization along the $\langle 111 \rangle$ direction. Therefore, the variation in the $\langle 111 \rangle$ direction is completely determined by atomic position optimization using the forces calculated from Hellmann-Feynman theorem. The stacking sequences along the $\langle 111 \rangle$ direction for the calculation of unstable stacking (γ_{us}) and unstable twinning (γ_{ut}) are ABC|ABCABACBA|CBA and ABC|BCABCACBACB|CBA respectively as shown in Figure 6-5. The vertical lines in the sequences mark the beginning and end of the layers whose atomic positions are moved along the $[112]$ direction for GSF calculations. The lowest two layers of the supercell are fixed during relaxation. It is important to note that the variation of fully relaxed and un-relaxed calculation of GSF results in about ten percent discrepancy with tight-binding calculations [111]. In the present calculation, the full relaxation in stacking direction is allowed. The relaxation in the (111) planes is allowed for the layer adjacent to the gliding layers in order for realistic capturing of the deformation process. The relaxation pattern during the shearing process has been reported to be an important factor which is directly related to the nature of bonding found to be different in metallic systems [108, 111, 112]. The positions of atoms in the top two layers in the Cu (111) plane are fixed. Similar surface relaxation of the Cu (111) surface was observed in the calculations.

In order to study the effects of strain on the formation of twins in the copper, isotropic strain was applied to the supercell in the crystallographic axis along a and b . Four different strains in both tension and compression are calculated. The four strain values are 0.003, 0.005, 0.01 and 0.02 for both tension and compression cases. For each atomic configuration, relaxation with the constraint mentioned above is performed to force convergence to 0.001 $Ry/bohr$ using the BFGS algorithm. The intrinsic properties

of the material which affect the formation of twinned structure are studied in the deformation twinning at the crack tip [99]. After the transmission of the leading partial dislocation, two modes of deformation, namely trailing partial transmission and leading partial transmission in adjacent planes are possible. The emission of the leading partial in the adjacent plane leads to the formation of twins. The model has been adapted to predict the twinnability of different FCC metals [113].

Figure 6-4: Unit cell used in computing the twinnability (a) graphical presentation, (b) crystallographic description.

Figure 6-5: Stacking sequence of the simulation cell

6.6 GSFE of copper under different modes of Cu(111) translation

Theoretical calculations of the equilibrium lattice constant help to obtain the lattice constant of copper in the stress-free state. More complex geometries for

calculations of GSFE and diffusion barrier are produced using the computed equilibrium lattice constant. The equilibrium lattice constant was determined to be $3.677\text{\AA}$ while the experimental lattice constant for copper is $3.615\text{\AA}$. The calculated constant is in agreement with values reported in the literature using the GGA correction functional [114]. A surface relaxation effect is found from the calculations. Similar surface relaxation of copper surface as previously reported [109] is also calculated.

Although the GSFE curves are defined as energies barriers in moving the atomic planes on the sliding crystal planes, the various computation methodologies used by different authors are not always the same [115]. In our model, the crystal slab with vacuum layer is used. Previous studies utilizing DFT use the crystal supercell to calculate the GSFE. With the vacuum layer, the surface process can be calculated. Therefore, the GSFE for twinning specific to the surface of the strained slabs are calculated in the present work.

The (111) texture development and high density twinning have been observed in sputtered copper thin films [116] and electroplated copper through-silicon via interconnects. In electrodeposition, this texture development means the surface energy minimizes the mode of crystal growth during electroplating. Therefore, grains with (111) texture are strained during and after deposition. Our present theoretical calculations consider this situation by taking into account the electronic nature of the mechanical deformation of such textured copper, although the computational methodology can also be applied to any other crystal. Highly localized compressive strains in copper during crystal growth or annealing may be the reason for the high probability of high-density nano-twinned copper in micro/nano crystalline copper. This is in accordance with experimental findings that the level of twinning in copper is dependent on processing history, rather than being a function of intrinsic properties of copper. The development of postcoalescence compressive stress in copper and silver

thin films [116] may also act as a source of stress that lead to the modified twinability of copper.

Figure 6-11 shows the X-ray diffraction with a cross-sectional view of pulse-reverse electrodeposited copper on silicon wafer with strong (111) texture. The electrochemistry used in the deposition has been described previously. The current density in the present work is 2 mA/cm^2 and plating was performed to a thickness of $10 \text{ }\mu\text{m}$. XRD shows the strong (111) texture of the copper films. The Focused Ion Beam (FIB) analysis was done well after a period of several months of self-annealing or recrystallization. As can be observed in the cross-sectional FIB, the nanoscale twins are nucleated on the planes that are parallel to the copper growth direction. Strong (111) texture of copper and coherent twin boundary on the plane in the direction of growth, closely resemble our theoretical models for DFT calculations.

Pulse-reverse electrodeposition with forward current density was previously reported to be able to fabricate high density nano-twinning copper with strong (111) texture [77]. The stresses generated during annealing or/and recrystallization during the electrodeposition process control the tendency for twinning mode deformation, depending on the tensile or compressive nature of the stress [117]. Electroplated copper films tend to possess strong (111) texture due to energy minimization and low energy of this surface. This crystal orientation is also desirable in practical applications in micro and nano-systems due to its reliability [118]. The strain in lattice in our theoretical model may have its origin in a variety of sources such as adatom trapping [119] and pinning pressure as modeled by Zener's model [120]. Because such mechanisms are random atomic processes, the strain/stress on the grain can be both isotropic and anisotropic, which results from the slightly unbalanced stress/strain leading to shear stress in the grain and subsequent dislocation or twinning process, depending on the electronic nature of atoms in the crystals.

Figure 6-6: Generalized stacking fault energy of copper with rigid translation.

Figure 6-7: Generalized stacking fault energy of copper with relaxation in $\langle 111 \rangle$ crystallographic direction.

Figure 6-6 and Figure 6-7 show the GSFE of copper with and without relaxation in a vertical direction. It is shown that the stacking fault energies are affected by the relaxation along $\langle 111 \rangle$ direction. The two GSFEs reflect the situations in different experimental conditions. GSFE of the copper without relaxation reflects the situation where the twinning happens in the bulk of copper where relaxation is not likely. The lower levels of stacking faults with relaxation show that the twinning process on the few atomic layers can easily take place. This explains the reason why the twinning is

more frequent in pulse-reverse electroplating where each cycle of pulse/pulse-reverse induces large stress/strain.

6.6.1 Supercell constraint and its effects of GSFE

The constraints set upon the supercell affect the GSFE of the material significantly. Therefore, in theoretical calculations, it is important to mention the geometrical details of supercells to ensure correct evaluation of the calculated properties. Surface effects on twinability of metals have also been reported [121].

6.6.2 Twinability of copper under strained condition

The tendency of metals to form twins depends on the intrinsic electronic nature of the materials. The most important parameter affecting twinability are the unstable and stable stacking fault energies and unstable and stable twinning fault energies.

From (6-10), it is clear that twinability is a function of unstable stacking and twinning energies and intrinsic stacking fault energy. As shown in Figure 6-10, the twinability of copper is not affected at low strain in both compressive and tensile isotropic strains in the (111) plane. But at a strain of 0.01, the twinability drops significantly due to the lowering of γ_{us} in the case of compressive strain and increasing of γ_{ut} in the tensile case.

It is noted that the twinability of copper at equilibrium in present calculations is 1.0337 while that in the previous tight binding method was 1.001. This discrepancy is due to the wide variation of calculations of ISF and different unstable stacking fault energies. The experimentally measurable ISF values vary from 61 ± 17 from experiments to 54 ± 16 from first principles calculations with tight binding models giving 64 mJ/m^2 [17] as discussed previously. Since the twinability of copper itself is characterized by the GSF energy curve which considers the competition of dislocation emission and leading partial emission in adjacent slip planes, the theoretical meaning of

our calculations follows the same fundamental fact with the exception of the existence of strain in the crystals. Asymmetry of dislocation nucleation in tensile and compressive strains has been reported previously in reference [122].

Figure 6-8: (a) Unstable stacking fault energy, (b) unstable twinning fault energy and (c) intrinsic stacking fault energy of copper under tension deformation.

Figure 6-8 shows the unstable stacking fault energies, unstable twinning fault energies and intrinsic stacking fault energies of copper supercell under biaxial tension. It shows an increase in unstable twinning fault energies with increasing tension while intrinsic stacking fault energies decrease. This implies that applied biaxial strain has noticeable effects on fault energies of the original FCC lattice and therefore its twinnability. Although the application of twinnability in such situations is yet to be firmly established, there is evidence that the basic lattice properties (fault energies) are modified by the applied strain in the lattice. Detailed analysis of electron densities and bonding charge analysis would likely explain the variations in stacking faulting

energies. However, the calculations presented in this chapter are enough to provide the evidence that stress/strain affects the deformation properties of copper.

Figure 6-9: Unstable stacking fault energy, unstable twinning fault energy and intrinsic stacking fault energy of copper under compression deformation.

Figure 6-9 shows the unstable stacking fault energies, unstable twinning fault energies and intrinsic stacking fault energies of copper (111) surface. ISF of copper increases with increasing strain. It shows the relative stability of unstable stacking energy of copper with tension strains. The variation of these parameters have strong attribute to the anisotropy nature of copper. Finally, after passing all the stacking faults parameters into the twinnability equation, the variation in twinnability of copper under various tensile and compressive biaxial strains of $\langle 111 \rangle$ textured copper crystals are obtained and graphically depicted in Figure 6-10. It shows the nonlinear nature of twinnability of copper with large increasement of twinnability over large strain for compressive strains. For tensile strain, the twinnability decreases as strain increase

although the relationship is non-linear relationship. It clearly shows the strain dependent variations of twinability and further theoretically analysis is required.

Figure 6-10: Twinnability of copper under tensile and compressive strains.

Due to the highly intricate relationship between electronic structure of lattice and twinnability of copper, non-linearity of twinnability against the biaxial lattice strain is observed. Currently in literature, non-linear theory of elasticity is not fully understood and therefore further investigation and theoretical proofs within the solid mechanics remain needed.

6.6.3 Discussion and comparison with experimental results

The ab-initio results from first principles of quantum mechanics show that the stacking fault energy and energy barriers during deformation twinning vary significantly when biaxial strain is applied to the supercell. This implies that the twinning behavior of FCC matrix in copper grain is modified when it faces strain from the surrounding grains. The following Figure 6.11 shows the XRD and cross-sectional

focused ion beam of the copper film electroplated with pulse-reversed plating. As shown in previous chapters, pulse-reverse electroplating produces (111) oriented copper grains. In Figure 6.11, the parallel twin in the plane parallel to growth direction across the grain is observed.

Figure 6-11: XRD and FIB sectional analysis of copper foil.

Previous studies by molecular dynamics simulations show the effect of biaxial strain or stress on the stacking fault, proving that transformation to a twinning mode of deformation is energetically favorable [123]. It is important to note that DFT calculations describe the ideal situation where the whole of copper lattice is strained by a large amount. However, in practical situations, the strain can be localized so the macroscopically observed stress/strain is much lower than the 1 to 3 percent strain used in theoretical calculations.

6.7 Diffusion barriers in twinned copper

Addition or alloying of aluminum in copper interconnect seed layers improves reliability [124]. The examination of vacancies in aluminum and copper alloys is an important research field due to their importance in applications and significance in scientific research [125]. It is known that during recrystallization of electroplated copper, the vacancy-type defects are introduced into the copper according to measurements using position annihilation spectroscopy [126, 127]. Previous studies by positron annihilation spectroscopy show that the grain boundary annihilation is significant only for the thicknesses of 1-2 μm . Positron annihilation level becomes similar to that of plastically deformed copper after a certain thickness. Therefore, it was concluded that the majority of defects are in the form of vacancy-clusters. As shown in previous chapters, different relative concentrations of impurities are detected in ToF-SIMS measurements in microfabricated copper TSV. The grain size and density of nanoscale twins are correlated with impurities species such as carbon and chlorine. The interaction between impurity species and twinning in copper is not thoroughly understood and may relate largely to the practical characteristics in real application. The observation of higher concentrations of impurities in high density twinning areas shows the effects of impurities on copper crystallization or grain growth. Previous investigations also show that positron trappings in their experiments were due to vacancy-type defects even for films annealed at temperatures up to 700°C. The defects other than grain boundaries contribute largely to the microstructural evolution in copper because a driving force of at least 100 J/cm³ is required to account for the room temperature grain evolution [128]. This amount of energy cannot be supported by the grain boundaries alone. Other impurities such as dislocations and vacancy defects play an important role. The determination of diffusion energy barriers relates to the experimental studies of electromigration in copper interconnects [129]. The measured

mechanical properties of the electrodeposited copper may have been affected by the superabundant vacancy formation rather than texture or grain size [130, 131].

In this section of the thesis, the first principles calculations are carried out using density functional theory to study the migration of various impurity species. Since the impurities measured may also have their origin in large molecules rather than atomic impurity species, our studies in the present work will be limited to the atomic impurity. The activities of large molecules in the copper matrix are much more complicated and require large computation resources for calculations within the first principles framework.

6.7.1 Computational details

All the computations in studies of defects and ion migration are carried out in the planewave pseudopotential density functional theory framework as reviewed in the previous chapters. Previous studies using less expensive computation such as molecular dynamics show the decreased migration barrier of copper across or near the twin boundaries [132]. The following Figure 6-12 shows the computational supercell used for vacancy and twin boundary interaction in nanotwinned copper.

Previous studies of vacancies in metals using DFT show that 32 or 64 atom supercells are sufficient to isolate the defect from its periodic images [133]. First principles calculations of positron annihilation characteristics at metal vacancies for copper have been done before [134] to accurately predict the annihilation time for different metals. Results of calculations of positron annihilation have been shown to converge to less than ten percent for a supercell with 32 lattice sites. Present model also resembles the copper nanotwins of few atomic layers. It gives the ability to analyse the electronic structure of the nanotwinned copper and its effect on reliability.

Figure 6-12: Unit cell used in computing the diffusion parameters.

Figure 6-12 shows the computation cell of FCC lattice with **ABCBA** close-packed structure in $\langle 111 \rangle$ direction. The colored atom represents the copper of aluminum migrating atom near the twin boundary. The migration process is a completely solid state process with two important parameters. They are the diffusion barrier height and the attempt frequency of the migrating species in Transition State Theory (TST). The experimental model of the copper interconnect reliability also involves the energy barrier height of the migrating atom as in the following Black's equation to calculate Mean-Time-To-Failure (*MTTF*).

$$MTTF = A\omega J^{-n} e^{\frac{Q}{kT}} \quad (6-11)$$

where A is an experimentally fitted constant, J is the current density, n is a modal parameter, Q is the activation energy, k is the Boltzmann's constant and T is the absolute temperature in Kelvin (K). As shown in the equation, the reliability of the interconnection system as measured by *MTTF* is a function of the height of the diffusion energy barrier Q . Such an energy barrier can also be used to evaluate copper self-diffusion especially in electrodeposited copper due to their high density of vacancies immediately after deposition.

Figure 6-13: Charge density of migration for (a) aluminum and (b) copper atoms across the (111) plane.

Figure 6-13(a) and (b) shows the charge density plot of the copper and aluminum atom migration across the (111) plane respectively. The density shows the charge density at the position at the peak of the energy barrier. It shows a similar charge distribution. However, migrating copper atoms have higher charge density at their lattice sites, making the migration more difficult than in aluminum. The barrier for copper and aluminum atoms is 0.72766 and 0.6235 eV respectively. The energy of copper and aluminum atoms at the twinning plane are 24 and 9 meV higher than at FCC site.

Figure 6-14: Charge density of migration for (a) aluminum and (b) copper atoms within the (111) plane.

Figure 6-14(a) and (b) show the charge density plot of copper and aluminum atom migrations within the (111) plane adjacent to the twinning plane. The charge density profile is observed to be similar to the previous case with migrating copper atoms having higher charge density around them. The energy barriers for migration of copper and aluminum atoms are 0.69 and 0.59 eV respectively. The lower valence charge densities around migrating aluminum atoms explain the lower energy barrier. Since the initial and final positions of the migration atoms lie within the same plane, the energies of both positions are the same within computational limits.

6.7.2 Results and discussion

Previous studies show that the diffusion barrier of copper FCC lattice along (111) direction is 0.6 eV [135], which agrees well with the computational results presented. Previous studies show the [136] vacancy carbon interaction. Computational studies show that nanotwinned copper provides better performance in electromigration barriers compared to copper with aluminum alloy [137]. Present theoretical results show that although aluminum has larger ideal shear strength due to its strong covalent-like directional electronic bonds [108], pure copper twinned crystal provides a better reliable material system for practical applications.

6.8 Conclusion

In this chapter, the ab-initio first principles quantum mechanical calculations were performed to evaluate the effect of biaxial strain on the twinnability of copper. It is shown that twinnability increases with compression and decreases with tensile stress. The diffusion barriers across the twins are also calculated for copper and aluminum atoms. The results show that copper possesses a higher barrier for diffusion compared to aluminum. Therefore, it can be concluded that twinned copper is better studied for

future interconnection applications than alloyed twinned copper [137] which also has the disadvantage of higher manufacturing cost.

Chapter 7

Conclusions and Recommendations for Future Work

7.1 Conclusions

It is concluded that for the high aspect ratio TSV fabrication, the current density should be within the limiting current density to ensure reliable void-free fabrication of through-silicon vias. The geometry (i.e. diameter) and depth of the trench have strong effect on the mechanical and microstructural properties of copper TSV. Therefore, in the design of practical applications such as MEMS and TSV, geometry related effects on mechanical properties should be addressed, especially when the deposit is used as a structural component such as in MEMS.

7.2 Contributions

This thesis contains a detailed study of TSV fabrication and characterization of electroplated TSV in terms of microstructure and mechanical aspects. The relationship between microstructure, electrodeposition parameters and impurity incorporation are examined in detail. The measurements of stress and its role in the twinning process are calculated using density functional theory. The major contributions of this thesis research are summarized as follows:

- Microstructure of pulse-reverse electroplated copper through-silicon via was investigated and the correlation between electrochemical deposition parameters, microstructure and mechanical properties has been ascertained. It is found that even the use of constant pulse-reverse modulation along the length of TSV produces TSV with mechanical properties along the length of TSV.

- Impurity inclusions in the TSV are studied by secondary ion mass spectroscopy-time of flight (ToF-SIMS). It shows the relationship between impurity concentration and mechanical properties at various locations of TSV.
- The effect of tertiary current distribution or high current density over limiting current densities on the microstructural and impurity incorporation has been observed. It induces the void formation at the core of TSV due to preferential deposition around the perimeter of TSV.
- The texture and its evolution for pulse-reverse electroplating are extensively studied by x-ray diffraction. It is established that the pulse-reverse plating produced (111) textured copper which is known to possess excellent mechanical and electrical properties for applications such as zero level or TSV level integration technologies.
- Density functional theoretical studies of twinning in electroplated copper were carried out. The effect of biaxial stress/strain on the twinnability of copper was calculated with the framework of DFT. It has been proven that the GSFE of copper FCC lattice is altered by the applied external strain.
- The interaction between the vacancies and impurity atomic species is studied and the resulting energy landscapes of migration of these species are calculated with the use of DFT. The Al/Cu alloy and pure Cu material systems are compared. It is revealed that pure copper in the twinned crystal structure has a higher potential barrier to prevent the migration.

7.3 Recommendations for future work

Although a considerable amount of research has been done in this thesis, the science and applications of nanotwinned copper provide a huge arena for further

research. Recommendations for future research work in the area of nanotwinned copper and its applications are as follows:

- More research can be conducted on the full fabrication of nanotwinned copper based devices such as the suspended high-performance RF inductor discussed in appendix A. The high performance vacuum core floating MEMS RF inductor based on TSV technology will most likely benefit from the properties of nanotwinned copper.
- The role of impurity species, both atomic and molecular, in the recrystallization and grain growth and their relation to the twinning / detwinning process is not clearly understood. More detailed molecular dynamics models and in-situ studies using TEM will help to understand their dynamics.
- More detailed studies of orientation mapping, texture and grain evolution and their effects on copper interconnect performance and mechanical reliability can pave the way for practical applications of nanotwinned copper interconnect technology for future high power density electronic devices.
- Figure 7-1 shows the possible detwinning mechanism during recrystallization via ITB [138]. Details of electronic and atomic structure of nanotwinned copper are not yet known, but will be useful for evaluating the range of temperatures where stable nanotwinned structures can be used in practical applications.

Figure 7-1: Two possible exchange mechanisms for the detwinning process.

- First principles dynamical calculations can be used to predict the reliability of AlCu alloys with ab-initio calculation of attempt frequencies of migration. Such calculation gives the complete ab-initio theory of migration in nanotwinned copper.
- The role of impurity atomic species such as chlorine, carbon or carbon fragments of larger additive chemicals in the twinning process can be studied by the molecular static/dynamic or first principles methods.
- The effect of GSFE on copper lattice with atomic impurity species such as chlorine can be studied using first principles methods to determine the effects of the electronic structure of such species on the copper.

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Appendix A

A TSV based three-dimensional RF inductor

The fabrication of through-silicon based micromachined radio-frequency MEMS is demonstrated as a proof-of-concept for TSV based devices. Full-wave electromagnetic simulations of the fabricated devices are calculated in high-frequency structure simulator (HFSS) software package. The resulting RF performance shows the acceptable inductance and quality factor.

Fabrication of TSV based RF inductor

Firstly, the wafer was cleaned in piranha solution. A 150 nm thick aluminum thin film was sputtered on the back side of the layer as an anti-notching layer. The wafer is temporally bonded to a carrier wafer of thickness 450 μm using a 5 μm thick photoresist layer as a bonding material. The photoresist layer was baked at the temperature of 90 $^{\circ}\text{C}$ for 45 minutes to ensure that the photoresist layer is totally dried and solidified. After bonding the wafer to the carrier wafer, a layer of photoresist AZ 9260 of 10 μm was spun on the silicon wafer. The through silicon via pattern was formed by photolithography as shown in figure (a). Deep reactive ion etching was performed with STS DRIE tool for three hours to ensure that through-holes were obtained. After DRIE process, the device wafer was separated from the carrier wafer by soaking in acetone solution for 5 hours. After separating from the carrier wafer, the device wafer was cleaned in piranha solution to remove the organic residues from the previous processes. The wet oxidation process is used to obtain a 2 μm thick silicon dioxide layer. The silicon dioxide layer acts as electrical insulation and it also improves the wetting in the electroplating process to ensure that all the through-holes are filled with copper. After the oxidation process, the device wafer was bonded to a carrier with

Appendix A

3 μm thick positive photoresist (AZ 9260) layer as a temporary bonding layer. The thickness of the carrier wafer was 450 μm , with a 3 μm thick positive photoresist (AZ 9260) layer and a 300 μm thick titanium/gold thin film which acted as a seed layer for the through-silicon via electrodeposition.

After bonding the device wafer to the carrier wafer, the bonded pair of wafers was baked for 45 minutes at a temperature of 65 °C. Low temperature was used to ensure that the existing photoresist layer underneath the gold seed layer is intact. Then, ultraviolet exposure was carried out to remove the intermediate photoresist layer between the device wafer and the seed layer. The exposure time was 12 seconds. The photoresist was developed in the AZ400 developer solution under ultrasonic agitation to ensure that the photoresist was fully developed and removed from the bottom of the trenches. Since a single atomic layer of organic residue can prevent electrodeposition from occurring, it is important to remove the photoresist properly before electrodeposition.

After development, the wafer was soaked in deionized water for 15 minutes to diffuse the residual photoresist into the water. The electroplating process was performed in a home-made electroplating setup for 10 hours. The pulse reverse electroplating technique as discussed in the previous chapter was used to fill the through-holes with copper to form through-silicon vias. The forward and reverse current densities are 10 mA/cm^2 and -40 mA/cm^2 respectively. The pulse duration was 1.9 seconds for forward current and 0.1 second for reverse current. After electroplating process, the device wafer was removed from the carrier wafer by soaking in acetone solution for 5 hours under the ultrasonic agitation. The device wafer was attached to a glass plate using the wax. Polishing was performed to remove the overplated copper on top of the surface. After polishing, the gold seed layer (titanium/gold) of thickness 300 nm was deposited in the sputtering process to be used

Appendix A

as the seed layer for metallization. The photolithography process with a 10 μm of photoresist (AZ9260) was performed to pattern the bottom metallization lines. After developing, the electroplating was performed using the pulse reverse electrodeposition technique. The thickness of the metallization was about 8 μm . After the electroplating of bottom metallization lines, the photoresist mould was removed in acetone solution and the underlying gold seed layer was removed by reactive ion etching using chlorine as the process gas. Etching time was 15 minutes. After finishing the bottom metallization, the titanium/gold seed layer on the other side of the wafer was deposited using sputtering. The device wafer was then bonded to a carrier wafer using photoresist as a bonding layer. The photolithography process was repeated for the front side metallization. After the photolithography process, the electroplating of top side metallization was performed. The thickness of the top side metallization was 8 μm . The photoresist mould was removed by soaking the wafer in acetone solution. The titanium/gold seed layer was removed in reactive ion etching process by using chlorine gas for 15 minutes. It should be noted the corrosive nature of chlorine plasma in reactive ion etching process. Therefore, protection of copper from corrosive environment is needed to achieve the reliable copper plated structure. The detailed process flow of the fabrication is shown in Figure A-1.

After removing the seed layer in chlorine based reactive ion etching process, inductor fabricated with TSV technology is achieved. Further removal of silicon at the core of inductor by isotropic etching will improve the microwave performance of the device since silicon is a lossy material and loss of RF signal is significant even though high resistance silicon substrate is used. Furthermore, the silicon substrate compatible with microelectronic fabrication is not lowly doped silicon. Therefore, three dimensional TSV with hang structure is necessary for future development of practical applications in TSV based inductors.

Appendix A

Figure A-1: Fabrication process for TSV based RF inductor.

Appendix A

Figure A-2 shows the optical image of the copper electroplated through-silicon via. Almost all the copper pillars are plated uniformly although some of them are overplated due to the statistical nature of electrochemical deposition.

Figure A-2: Optical picture of copper TSV.

Figure A-3 shows the through-silicon via after the partial removal of silicon substrate in potassium hydroxide (KOH) solution. The oxide layer was removed in the reactive ion etching (RIE) process to expose the copper pillars. It shows the clear surface of copper pillars. Therefore, it indicates the reliable filling of deep trenches with electroplated copper.

Figure A-3: TSV embedded in silicon after partial removal of silicon by KOH etching (a) magnified view and, (b) array of inductors.

Figure A-4 shows the front side of the three-dimensional inductor after finishing all the fabrication process.

Figure A-4: Three-turn inductor based on TSV technology.

Figure A-5 shows the backside of a six turn inductor with ground guards. The purpose of using ground guard is to prevent the electromagnetic wave from penetrating into the silicon substrate and further increase losses. Finally Figure A-6 shows the front and back side of the eight turn inductor fabricated using TSV technology.

Figure A-5: Six-turn inductor based on TSV technology.

Figure A-6: Eight-turn inductor (a) front side and (b) backside based on TSV technology.

It has been demonstrated that a three-dimensional RF inductor can be realized using the through-silicon via TSV fabrication technology reported in this thesis. Although the performance of the fabricated inductor is not comparable to that of discrete RF modules due to the existence of lossy silicon at the core where there is high magnetic field, the simulations show that adequate performance can be achieved by removal of silicon at the core using micro-machining technique such as controlled anisotropic deep reactive ion etching. A TSV based RF inductor is successfully fabricated. An additional etching process using isotropic etching of silicon to remove

Appendix A

the silicon at the core of the inductor would improve the performance of inductor. The fabrication of such device makes the integration of TSV in microwave engineering.

Appendix B

Detailed experimental measurement results

Modulus of elasticity and hardness of TSV with various diameters

Figure B-1: Measured hardness of TSV of different diameters.

Figure B-2: Modulus of elasticity of TSV of different diameters.

Appendix B

Fig B-1 shows the significant variation in mechanical properties of different diameters of TSV. Generally, the TSV with smaller diameters will have larger hardness.

X-ray diffraction of copper films

XRD analysis of pulse-reverse and direct current electroplated copper film

Figure B-3: ODE of copper film with pulse reverse electroplating.

Figure B-4: ODE of copper films with pulse-reverse electroplating (value of isosurface is 5).

Figure B-5: ODE of copper films with direct current electroplating (value of isosurface is 5).

Figure B-6: Inverse pole figure of copper film electroplated with pulse reverse current.

Figure B-7: Pole figure of copper film electroplated with pulse reverse current (a) 100, (b) 110, (c) 111, (d) 311 direction.

Appendix B

Figure B-8: ODE of copper film with direct electroplating.

Figure B-9: Inverse pole figure of copper film electroplated with direct current.

Figure B-10: Pole figure of copper film electroplated with direct current (a) 100, (b) 110, (c) 111 and (d) 311 direction.

Appendix B

Figure B-11: TOF-SIMS mass spectra of TSV from 1 to 200 amu.

Figure B-12: TOF-SIMS mass spectra of TSV from 200 to 320 **amu**.

Figure B-11 and Figure B-12 show an example of a complete mass spectrum reading of ToF-SIMS. This spectrum is taken from the center portion of the TSV with 100 μm diameter.

In order to study the underlying electrochemical nature of plating, electrochemical current potential-curves are measured in the copper sulfate solution with increasing concentrations of brightener and leveler (Two organic additives were used to achieve void free filling of TSV). The measurements were done with a three-electrode system using Ag/AgCl electrode as reference. Commercially pure copper plate is used as the anode. The measurements were done under the well agitated small scale electrochemical cell. Magnetic agitation was used to ensure the well stirred plating condition during the experiments. The scanning was done at the rate of 0.2 V/sec.

Figure B-13: Current-potential curves for various concentrations of brightener and leveler.

Figure B-13 shows the current-potential curves of the copper sulfate solution with increasing concentrations of brightener and leveler. Curve **A** represents the solution without any additives. Curves **B** and **C** show the current-potential curves with the brightener solution at the concentration of 5 and 10 ml/l respectively. Curve **D** and **E** show the characteristics of solutions with 7.5 and 15 ml/l of leveler concentration respectively. Abrupt increase in the current density in case **B** and **C** can be seen in Fig 3. However, such increase in the current density is suppressed in the solution with the concentration used in TSV electroplating. As can be seen in the figure, the current saturates around 40 to 60 mA/cm².

Figure B-14: location dependent impurity concentration in open voided TSV (a) SIMS map and (b) SIMS ion intensity at various locations.

Figure B-15: Load displacement curves for nanoindentation of 60 μm TSV.

Figure B-15(a-d) shows the load displacement curves of nanoindentation performed on TSV with 60 μm diameter. These curves show the consistency of load-displacement curves across the points with similar mechanical properties.

Appendix C List of Publications

Journal

-**Nay Lin** and Jianmin Miao, “Modified twinnability of copper under biaxial strain: an ab-initio study”, to be submitted.

-**Nay Lin**, Jianmin Miao and Robert Preisser, “Microstructural investigation of through-silicon via fabricated by pulse-reverse electroplating for high density nanoelectronics”, Accepted for publication in International Journal of Nanotechnology (2013).

-**Nay Lin**, Jianmin Miao and Pradeep Dixit, “Void formation over limiting current density and impurity analysis of TSV fabricated by constant-current pulse-reverse modulation”, Microelectronic Reliability, Vol 53, Issue 12 (2013).

-Haobing Liu, **Nay Lin**, Shanshan Pan, Jianmin Miao and Les Norford, “High sensitivity, miniature, full 2-D anemometer based on MEMS hot-film sensors”, IEEE Sensors Journal, Vol 13, Issue 5 (2013).

-**Nay Lin**, Jianmin Miao and Pradeep Dixit, "Mechanical and microstructural characterization of through-silicon via fabricated with constant current pulse-reverse modulation", Journal of the Electrochemical Society 157 (6) D323-D327 (2010).

-**Nay Lin**, Huili Wang, Pradeep Dixit, Ting Xu, Sam Zhang and Jianmin Miao, "Investigation of carbon nanotube growth on multimetal layers for advanced interconnect applications in microelectronic devices", Journal of the Electrochemical Society, 156 (3) K23-K27 (2009).

-Ting Xu, Jianmin Miao, Mohammed Ashraf, **Nay Lin** and Franck Chollet, "Synthesis of regular nano-pitched carbon nanotube array by using nanosphere lithography for interconnect applications", Materials Letters 63 (2009) 867-869.

-Pradeep Dixit, **Nay Lin**, Jianmin Miao, Wai Kwan Wong and Teo Kiat Choon, "Silicon nanopillars based 3-D stacked microchannel heat sinks concept for enhanced heat dissipation applications in MEMS packaging", Sensors and Actuators A: Physical 141 (2008) 685-694.

- Pradeep Dixit, Tan Chee Wee, Luhua Xu, **Nay Lin**, Jianmin Miao, John H. L. Pang and Robert Preisser, "Fabrication and characterization of fine pitch on-chip copper

Appendix C

interconnects for advanced wafer level packaging by high aspect ratio through AZ9260 resist electroplating", Journal of Micromechanics and Microengineering 17(5) 1078 (2007).

Conferences

-Shuwei Liu, Shanshan Pang, Fei Xue, **Nay Lin**, Haobing Liu, Jianmin Miao, Les K. Norford and H. B. Lim, "Out-of-plane micro triple-hot-wire anemometer based on Pyrex bubble for air flow sensing", Proceeding of 27th International Conference on Micro Electromechanical System, Jan 2014, San Francisco, USA.

-**Nay Lin** and Jianmin Miao, "Through-silicon via fabrication with pulse-reverse electroplating for high density nanoelectronics", Proceedings of IEEE 5th International Nanoelectronics Conference (INEC) 2013, Singapore.

-**Nay Lin**, Pradeep Dixit and Jianmin Miao, "(111) texture development in pulse-reverse electro-deposited copper film", Asia pacific conference on transducer APCOT 2010, July 2010, Perth, Australia (Oral presentation).

-**Nay Lin**, Pradeep Dixit, Jianbo Sun, Kaixue Ma, Jianmin Miao and Jianguo Ma, "A through-silicon via (TSV) shunt-grounded conductor backed ring resonator", Proceedings of International conference on communications, circuits and systems ICCAS, 2009, USA.

-**Nay Lin**, Pradeep Dixit, Xu Ting and Jianmin Miao, "Study of multi-walled carbon nanotubes growth on multi-metal layers for advanced interconnect applications in microelectronic devices", 4th International conference on materials for advanced technologies ICMAT, Singapore (Oral presentation).

-Pradeep Dixit, **Nay Lin**, Jianmin Miao, Wai Kwan Wong and Kiat Choon Teo, "Concept and analytical analysis of silicon micro/nanopillars based 3D stacked microchannel heat sink for advanced heat dissipation applications", Proceedings of 57th Electronic components and technology conference ECTC, May 2007, Reno USA.