Impedance source inverters with enhanced voltage boost capability

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**IMPEDANCE SOURCE INVERTERS WITH ENHANCED
VOLTAGE BOOST CAPABILITY**

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**SCHOOL OF ELECTRIC AND ELECTRONIC
ENGINEERING**

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IMPEDANCE SOURCE INVERTERS WITH ENHANCED VOLTAGE BOOST CAPABILITY

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Summary

Semiconductor-based power inverters have widely been used in the industry because of their compact size, high power density and efficiency. However, traditional power inverters can only either step down or up their outputs, but not both. They are hence not suitable for interfacing renewable energy sources to the main power grid. The reason is linked to the inconsistent and high weather dependent nature of the renewable sources, which would then require buck-boost energy conversion for maximum flexibility. To achieve buck-boost capabilities, a front-end dc-dc converter is usually added to a rear-end dc-ac inverter. Alternatively, single-stage buck-boost inverters can also be used, which comparatively, are more integrated. A few single-stage buck-boost topologies have so far been reported. They include the Ćuk and SEPIC-derived inverters, which in effect, are nice integrations of the Ćuk and SEPIC dc-dc converters to the rear-end dc-ac inverters. Other possibilities are the Z-source inverters, which over the years, have attracted more attention than the others because of their many unique advantages.

For example, the added X-shaped impedance network of the Z-source inverters allows two switches from the same phase-leg to turn on without causing damages. The shoot-through state is instead intentionally added for voltage boosting, while retaining the usual voltage-buck capability of the six-switch inverter bridge. Besides two-level Z-source inverters, three-level Z-source NPC inverters have also been studied, whose main intention is to lower the switch voltage stress, while improving the inverter output waveform quality. Even with their proven advantages, existing Z-source inverters still have some shortcomings to resolve. One of them is their chopped input current, which requires bulky input passive filter for smoothing their input current. This can be resolved by the embedded Z-source, quasi-Z-source and LCCT inverters, whose common objective is to make the input current continuous by using an existing Z-source inductor.

Another shortcoming is related to the low modulation ratio permitted, while

performing high voltage boosting with high shoot-through duty ratio. The low modulation ratio then causes the inverter waveform quality to drop and the switch voltage stress to rise. These effects are no doubt undesirable, leading to a few topologies being proposed to resolve them. One solution is to use coupled inductors or transformer, leading to the development of trans-Z-source inverter, T-source inverter and trans-quasi-Z-source inverter. These inverters offer a high voltage gain at a high modulation ratio, which needless to say, have resolved the complications mentioned earlier regarding waveform quality and switch voltage stress. They however still draw a chopping input current, which at times, might not be tolerated by the source.

Therefore, the intention set for this thesis is to formulate a few topologies with enhanced voltage boost, while drawing continuous input current. The proposed inverters use one coupled transformer, one inductor and two capacitors, which are more than components used by the trans-Z-source inverters. The components used are however the same if a low-pass filter is included with the latter for input current filtering. The component selection process, voltage/current stress and efficiency comparison between the proposed inverters and traditional impedance-source inverters will all be covered in the thesis. Simulation and experimental results will also be given for verifying the theoretical analyses presented.

To further reduce the device switching stress and improve the output waveform quality, a series of impedance-source NPC inverters based on transformer-capacitor impedance network inserted to the front-end of the NPC inverter bridge are proposed. These inverters integrate all advantages of the transformer-based impedance-source two-level inverters and classical NPC three-level switching. The proposed trans-Z-source NPC inverter has enhanced voltage boost capability over the traditional Z-source NPC inverters. The proposed gamma-source NPC inverter, on the other hand, uses a transformer with a smaller turns ratio to gain the same voltage boost capability as that of the trans-Z-source NPC inverter.

The third type of transformer-capacitor impedance-source NPC inverter further extends the concepts of asymmetrical embedded Z-source inverter to the NPC configuration. The result is again an enhanced voltage boost similar to those of the

first two types of transformer-capacitor impedance-source inverters. The third type of NPC inverter however draws a continuous input current, which is different from the chopping discontinuous input current drawn by the earlier two types of transformer-capacitor impedance-source NPC inverters. All topologies and concepts discussed so far have appropriately been verified in experiments, whose results are explained in relevant chapters.

Last but not least, a model predictive control method has been adapted for controlling the traditional Z-source inverters and also the proposed inverters for use in renewable energy systems that require buck-boost energy conversion. The discussed method has been tried in simulation with promising results observed.

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Abbreviations

Z-source	Impedance-Source
Trans-Z-source	Transformer-Based Impedance-Source
EZ-source	Embedded Z-Source
LC	Inductor Capacitor
NPC	Neutral Point Clamped
CCM	Continuos Conduction Mode
DCM	Discontinuons Conduction Mode
MPC	Model Predictive Control
PWM	Pulse Width Modulation
PFC	Power Factor Correlation
PDPWM	Phase Disposition Pulse Width Modulation
APODPWM	Alternative Phase Opposition Disposition Pulse Width Modulation
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PI	Proportional Integral
PR	Proportional Resonant
RHP	Right Half Plane
RCM	Reduced Common Mode
VS	Voltage Source

Chapter 1 Introduction

This chapter introduces the background and motivation of the thesis. The main contributions and organizational structure of the thesis are also clarified in the chapter.

1.1. Background and Motivation

The increasing emission of carbon dioxide, sulphur dioxide as well as other types of greenhouse gases leads to global temperature and sea level rising, which can potentially affect the agricultural and industrial activities. The outcomes might be a food crisis or permanent damages to the environment. Concerning the greenhouse gas emission, traditional ways of electricity generation like coal, gas or oil are slowly being substituted by greener energy sources like solar, wind or tidal energy. As a result, the clean energy industry has developed very fast in recent years. At the end of year 2011, renewable energy accounts for more than 25% of the total power generating capacity (5360 GW estimated), and supplies 20.3% of the global electricity. This is almost 50% of the newly added power capacity (208 GW estimated) in the year of 2011. Two major contributors for renewable energy so far are wind and photovoltaic sources with the former reaching a total capacity of 238 GW mainly in Northern Europe, Italy, Portugal and Spain. Photovoltaic source, on the other hand, rises to a total capacity of 67 GW with most activities concentrating in Germany, United States and Asia at the end of year 2011[1].

The development of green energy harnessing has however created many challenges for electrical engineer in terms of converting its inconsistent power to regulated power for injection to the utility grid. For example, most wind power farms would require AC-DC-AC power conversion, while solar farms would need DC-AC power conversion before supplying the regulated energy to the grid or for own usage in an islanded area. Semiconductor-based power converters are now the preferred choices for these types of power conversion, and have been widely adopted by the industry for manufacturing products that have compact size, low power loss, high efficiency and

high power density [2-10]. This leads to rapid research and developmental efforts in power converter topological design and their suitable control algorithm formulation [11-26]. As a result, the conversion of unregulated green power to regulated grid power by using power converters is now well understood [27-31].

Despite their popularity, traditional voltage-source inverters used for AC-DC-AC and DC-AC applications usually only have voltage buck capability. That means their dc-link voltages are always higher than the grid ac voltages. They are therefore not suitable for some renewable systems like photovoltaic panels, where many panels need to be series cascaded to obtain the higher dc-link voltage regardless of weather conditions. Otherwise, DC-DC boost converters need to be added to the front-end of the conventional DC-AC inverters, or alternatively, single-stage buck-boost inverters can be used to adapt to the varying voltage level of the renewable energy sources. The former, being quite straightforward, is not discussed further. The latter, being more integrated, has a few possible topologies for consideration like the Ćuk and SEPIC-derived inverters discussed in [32]. Other possibilities are those Z-source inverters proposed in [33], which over the years, have attracted more attention than the others.

Topologically, the uniqueness of a Z-source inverter is the presence of an X-shaped LC impedance network between the dc source and inverter bridge. The network prevents the inverter from accidental short-circuit damages [33, 34]. Instead, the short-circuit or shoot-through state has been intentionally used by the Z-source inverter for temporary storing energy in its impedance network. This temporary energy is subsequently released to the load for voltage boosting when the inverter returns to its usual switching states.

Despite its promising features, Z-source inverter has some shortcomings. One of them is its discontinuous chopping input current. The other is its limited modulation ratio during high boost gain operation. The former might affect the input dc source, and is usually resolved by adding a low pass filter after the source. This will raise the system cost and lower its efficiency. The latter, on the other hand, can affect the output waveform quality, increase the voltage stresses of the switching devices, and more critically, might cause the Z-source inverter to enter its unintended discontinuous

conduction mode. To overcome the aforementioned drawbacks, this thesis presents topologies with transformer-based impedance networks that can produce an enhanced voltage buck-boost capability and a continuous input current. For even better switching performance and lower voltage stresses, three-level NPC topologies with cascaded transformer-capacitor impedance network are also presented.

1.2. Contributions to the Thesis

Motivated by an interest to generate new thoughts, a number of contributions are made in the thesis. They are summarized below as:

- ✓ Proposed 6 types of asymmetrical transformer-based embedded Z-source inverters, which have continuous input current and enhanced voltage boost capability over traditional Z-source inverters.
- ✓ Proposed transformer-based Z-source (trans-Z-source) NPC inverters which use cascaded connected trans-Z-source impedance networks to achieve high voltage boost gain.
- ✓ Proposed Γ -source NPC inverter which utilizes cascaded connected Γ -source impedance network to gain high voltage boost gain with low requirement on transformers.
- ✓ Proposed 7 types of transformer-based impedance source NPC inverters, which have overcome the discontinuous input current drawback and enhanced voltage boost capability over traditional Z-source NPC inverters.
- ✓ Implemented two-level and three-level Z-source inverter in the application of grid-tied photovoltaic system through model predictive control algorithm.

1.3. Organization of the Thesis

This thesis has eight chapters organized in a streamlined manner, whose aim is to concisely express the theoretical findings contributed by the research work. An

overview of each chapter is now presented before progressing to the detailed analyses found in each individual chapter.

The background and motivation, followed by the main contributions of the research work, are spelled in Chapter 1. Overall organization of the thesis is also described in the chapter to give an overview of each subsequent chapter.

Existing voltage buck-boost concepts realized with two-level inverters are reviewed in Chapter 2. Theories of the conventional two-stage buck-boost inverter, single-stage Ćuk and SEPIC-derived buck-boost inverters, Z-source inverters, embedded Z-source inverters and transformer-based impedance-source inverters are presented.

The review of three-level Z-source NPC inverters with either two cascaded impedance-source networks or a single impedance-source network are presented in Chapter 3. Pulse width modulation schemes for the Z-source NPC inverters are also briefly described.

Six types of asymmetrical transformer-based embedded Z-source inverters with enhanced voltage boost capability and continuous input current are proposed in Chapter 4. These features are presently not simultaneously achieved by the traditional Z-source inverters unless an additional input LC filter is added.

The discussion of the transformer-based impedance-source NPC inverters with enhanced voltage buck-boost capability is continued in Chapter 5. More specifically, trans-Z-source NPC inverter with two cascaded impedance networks, trans-Z-source NPC inverter with single impedance-source network, and Γ -source NPC inverter are discussed in the chapter.

The NPC inverters discussed in Chapter 5 however still draw a discontinuous input current. To resolve that, Chapter 6 presents a few improved NPC configurations with enhanced voltage boost capability and continuous input current. They are respectively named as the LCCT NPC inverter, and types EA, EB and EC asymmetrical transformer-based embedded Z-source inverters.

The inverters proposed thus far have been tested with an open-loop modulation scheme. For realizing a renewable system, closed-loop control scheme will usually be needed. For that, Chapter 7 introduces a MPC scheme for use with existing Z-source inverters. The same scheme can also be used for the proposed enhanced boost impedance-source inverters. This work is however at its preliminary stage with only simulation results obtained. Further effort needs to be spent in it, which will be suggested as a scope for future investigation.

The thesis, with some future research topics suggested for consideration, is eventually concluded in Chapter 8.

Chapter 2 Voltage Buck-Boost Concepts

Generally, either two-stage or single-stage DC-AC inverter can be used for voltage buck-boost power conversion. The two-stage approach simply involves adding a DC-DC converter to the front-end of a DC-AC inverter, while the single-stage approach integrates the functionalities of DC-DC and DC-AC power conversions to save some semiconductor switches or passive LC components [35-51]. The earlier proposed Ćuk and SEPIC derived buck-boost inverters are grouped under the single-stage approach, which have been analyzed for various applications such as solar power [52] and PFC applications [53-55]. More popular than these two choices would be the single-stage Z-source inverter, which structurally has a unique impedance network that can protect again short-circuit or shoot-through. Improvements to the Z-source circuit have since been proposed through the development of the embedded and quasi-Z-source inverters, whose input current drawn is smoother or capacitor voltage stress is lower. This chapter reviews these developments before presenting new contributions in subsequent chapters.

2.1. Conventional Two-Stage Buck-Boost Inverter

The circuit diagrams of classic buck inverter and two-stage buck-boost inverter with a front-end DC-DC boost converter added are shown in Fig. 2.1 and Fig. 2.2, respectively. The classic buck inverter connects directly to the dc source with a source voltage of V_{dc} . The amount of AC output voltage obtained can then be controlled by

Fig. 2.1. Circuit diagram of classic two-level buck inverter.

Fig. 2.2. Circuit diagram of two-stage buck-boost inverter.

adjusting the modulation ratio M , which even at its maximum value of 1 (or 1.15 with triplen offsets added), cannot be higher than the input voltage if no AC transformer is used. In contrast, the two-stage buck-boost inverter can produce voltage step-up and down by adding a DC-DC boost converter in front of the DC-AC buck inverter. Instead of modulation ratio M only, the amount of voltage step-up or down can now also be adjusted by the duty ratio d , which is the turn-on time for switch SW during one switching period [56]. Switch SW will no doubt increase the switching losses, and hence lower the system efficiency. This is certainly a trade-off introduced by gaining both voltage buck and boost capabilities for the two-stage buck-boost inverter.

2.2. Traditional Z-Source Inverter

A circuit diagram showing the traditional Z-source inverter can be found in Fig. 2.3,

Fig. 2.3. Traditional Z-source inverter.

where an X-shaped impedance network can clearly be seen. The added impedance network allows two switches from the same phase-leg to be turned on without causing damages. Instead, the shorted shoot-through state is intentionally added for voltage boosting, while retaining the conventional voltage-buck capability of the six-switch inverter bridge. Each Z-source inverter therefore has nine switching states, including those traditional eight non-shoot-through active and null states. With such simple addition and introduced flexibility, Z-source inverters have already been implemented in many applications such as motor drives [57-60], photovoltaic systems [61-65], fuel cells [66, 67], distribution generation systems [68] and uninterruptable power supplies [69].

When in its voltage-buck mode with no shoot-through state inserted, a Z-source inverter operates just like a traditional voltage-source inverter with inductors L_1 and L_2 behaving like two short-circuits in the steady state. Capacitors C_1 and C_2 then appear in parallel across the DC source with the dc-link voltage v_i now given as V_{dc} , as written in (2.1). The peak ac output voltage in terms of modulation ratio M and source voltage V_{dc} can also be written as $\hat{v}_{ac}$ in (2.1).

$$\begin{aligned} v_i &= V_{dc} \\ \hat{v}_{ac} &= \frac{M}{2} V_{dc} \end{aligned} \quad (2.1)$$

When voltage-boost operation is now demanded, at least one shoot-through state must be inserted to the traditional null states, during which no energy is transferred to the ac load, and hence will not affect the inverter terminal volt-sec average. The Z-source inverter is therefore able to provide boosted ac output voltage without degrading the output sinusoidal performance. Assuming now that the switching period is T and the shoot-through time is T_0 , the non-shoot-through time is then $T_1 = T - T_0$. Assuming also a balanced network where $L_1 = L_2 = L$ and $C_1 = C_2 = C$, relevant network voltages can then be expressed as $v_{L1} = v_{L2} = v_L$ and $V_{C1} = V_{C2} = V_C$ (if C is large). With these, the shoot-through equivalent circuit of the Z-source inverter in Fig. 2.4(a) can next be analysed, where it is seen that shorting the inverter bridge causes diode D to turn off, and the capacitors to charge the inductors. Energy stored in the inductors therefore increases. Assuming further that the average input current is I_{dc} , the following relations can be derived:

Fig. 2.4. Equivalent circuits of Z-source inverter during (a) shoot-through state and (b) non-shoot-through state.

$$\begin{aligned}
 v_L &= V_C \\
 i_{ST} &= 2I_L = 2I_{dc}
 \end{aligned} \tag{2.2}$$

On the other hand, when in a non-shoot-through state represented by any traditional inverter active and null states, the energy stored in the inductors is released to the external ac load. With diode D conducting, energy will also flow from the dc source to the capacitors and external ac loads, as shown in Fig. 2.4(b). The following expressions can thus be derived as:

$$\begin{aligned}
 v_L &= V_{dc} - V_C \\
 v_i &= V_C - v_L
 \end{aligned} \tag{2.3}$$

Integrating the inductor voltage over one switching period and equating it to zero ($\int_0^T v_L = 0$) then lead to the capacitor voltage shown in (2.4), where $d = T_0/T$ is the shoot-through duty ratio.

$$V_C = \frac{1-d}{1-2d} V_{dc} \tag{2.4}$$

Substituting (2.4) into (2.3), the boosted peak dc-link voltage v_i and peak ac output voltage can then be expressed as:

$$\begin{aligned}
 \hat{v}_i &= \frac{1}{1-2d} V_{dc} \\
 \hat{v}_{ac} &= \frac{M}{2} \hat{v}_i = \frac{M}{2} \frac{1}{1-2d} V_{dc}
 \end{aligned} \tag{2.5}$$

From (2.5), the dc-link voltage can be from V_{dc} to infinity by adjusting the shoot-through duty ratio d from 0 to 0.5. Since the shoot-through states are inserted only to

the traditional null intervals, the shoot-through duty ratio has to be in the range of $d \leq (1 - \frac{2M}{\sqrt{3}})$ when triplen offset is added to the three-phase sinusoidal references. Certainly, the Z-source inverter performances discussed so far are favourable, but not really its chopped input current, which can be damaging to the dc source. A low-pass filter is thus commonly placed between the source and inverter bridge, which will no doubt increase the system losses and overall cost. In order to resolve this drawback, the embedded Z-source inverters have been proposed, and introduced in the next section.

2.3. Embedded Z-Source Inverters

Embedded Z-source inverters were proposed in [70, 71], using two isolated dc sources. They are, in principles, designed to overcome the drawback of the Z-source inverter, where one of them is the requirement for an additional low-pass filter at the input side

Fig. 2.5. Z-source inverter with additional LC filter in practical applications.

Fig. 2.6. Embedded Z-source inverter.

for current smoothing (see top left corner of Fig. 2.5). To avoid incurring costs associated with the filter, the embedded Z-source inverter shown in Fig. 2.6 is proposed, where the original dc source is split into two and embedded in series with the network inductors. The existing network LC components are thus used for power conversion as well as filtering of switching current ripples. The passive component requirements are thus lowered with significant reduction in size and power losses of the network expected. Other publications related to embedded Z-source inverters can also be found in [72-75], but they are named differently as quasi-Z-source inverters. Other topologies with similar functions are also introduced in [76, 77]. With their inherent filtering advantage and lower required capacitor voltage, embedded Z-source inverters have again been investigated for a number of applications including induction motor drives [78], distributed generation systems [79], and photovoltaic systems [79, 80].

The operational principles of the embedded Z-source inverters are similar to those of the Z-source inverter. Their buck operation is again assumed with no shoot-through state added and diode D always conducting. The inductors therefore appear as shorted, while the capacitors appear connected in parallel to the two dc sources. In this case, the dc-link voltage v_i equals to the sum of the two dc source voltages V_{dc} , and the peak ac output voltage can be expressed as (2.6) in terms of modulation ratio M and source voltage V_{dc} .

$$v_i = V_{dc}$$

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (2.6)$$

Fig. 2.7. Equivalent circuits of embedded Z-source inverter during (a) shoot-through state and (b) non-shoot-through state.

On the other hand, when boost operation is demanded, shoot-through states have to be added to the conventional switching sequence. Similar to the traditional Z-source inverter, during a shoot-through state, the inverter bridge is shorted and diode D is opened. The resulting equivalent circuit representing the balanced embedded impedance network is then shown in Fig. 2.7(a), from which the following voltage and current relationships can be derived:

$$\begin{aligned} v_L &= V_C + \frac{V_{dc}}{2} \\ i_{ST} &= 2I_L = 2I_{dc} \end{aligned} \quad (2.7)$$

Upon changing to a non-shoot-through state, diode D starts to conduct with energy earlier stored in the inductors now releases to inverter ac output as shown in Fig. 2.7(b). The following expressions can then be derived:

$$\begin{aligned} v_L &= \frac{V_{dc}}{2} - V_C \\ v_i &= \frac{V_{dc}}{2} - v_L \end{aligned} \quad (2.8)$$

Integrating the voltage across the inductor over one switching period and equating it to zero ($\int_0^T v_L = 0$) then gives (2.9), where the shoot-through duty ratio is written as $d = T_0/T$.

$$V_C = \frac{1}{1-2d} \frac{V_{dc}}{2} \quad (2.9)$$

Substituting (2.9) into (2.8), the boosted maximum dc-link voltage v_i and peak ac output voltage can be expressed as:

$$\begin{aligned} \hat{v}_i &= \frac{1}{1-2d} V_{dc} \\ \hat{v}_{ac} &= \frac{M}{2} \hat{v}_i = \frac{M}{2} \frac{1}{1-2d} V_{dc} \end{aligned} \quad (2.10)$$

As shown in (2.9) and (2.10), the maximum dc-link voltage is double of the capacitor voltage. Comparing the voltage expressions of the Z-source and embedded Z-source inverters, their peak dc-link voltage and ac output voltage are obviously the same. The only difference would be the capacitor voltage stress, as seen from (2.4) and (2.9), which clearly show the embedded Z-source inverter having a lower capacitor voltage stress when shoot-through duty ratio $d < 0.5$, as demonstrated in Section 2.2.

The split voltage sources might however be costly for the embedded Z-source inverter unless it is used with applications, where multiple sources are readily available like photovoltaic and fuel cell systems. If only a single dc source is available, one of the two dc sources from the embedded Z-source inverter can be removed without affecting its voltage buck-boost capability [71]. It can in fact be shown that only the voltage stress for one capacitor will rise to the same level as the traditional Z-source inverter. The second capacitor voltage will still remain low as per derived in (2.9).

2.4. Trans-Z-Source Inverters

Another interesting attempt is to couple the two inductors on the same core, which to a great extent, resembles a two-winding transformer. The thought of changing the winding turns ratio is then introduced to raise the inverter voltage gain and modulation ratio. Doing so allows one capacitor to be removed too with the resulting circuits named as T-source [81] or trans-Z-source [82] inverters (collectively referred to as trans-Z-source inverters from here onwards). Similar theory can be applied to the embedded or quasi-Z-source inverters, but the topologies formed will no longer have a continuous input current. The present concerns faced by the trans-Z-source inverters can therefore be summarized as discontinuous input current and high turns ratio or many winding turns at high gain. The latter is probably obvious, as understood from the classical transformer theory. The trans-Z-source inverter configurations are shown in Fig. 2.8, where by placing the dc source in series with either the diode or inverter bridge, will result in the two shown types of trans-Z-source inverters.

The operational principles of the trans-Z-source inverters are similar to those of the traditional Z-source inverter. Equivalent circuits of the trans-Z-source inverter corresponding to its shoot-through and non-shoot-through states are shown in Fig. 2.9(a) and (b), respectively. For the trans-Z-source inverter in Fig. 2.8(a), during its shoot-through state, the inverter bridge is shorted, while diode D blocks to open-circuit winding W1. Capacitor C now charges winding W2 with its magnetizing inductance L_m being considered large enough to keep the magnetizing current I_m constant during the shoot-through period. Setting the transformer turns ratio to $W1:W2 = n:1$, the following expressions can then be derived:

(a)

(b)

Fig. 2.8. Trans-Z-source inverters with source in series with (a) diode or (b) inverter bridge (also called trans-quasi-Z-source inverter).

$$v_{W2} = V_C$$

$$i_{ST} = i_{W2} = -i_C$$

$$i_{W1} = I_m - \frac{i_{W2}}{n} = 0 \quad (2.11)$$

Fig. 2.9. Equivalent circuits of trans-Z-source inverter during (a) shoot-through state and (b) non-shoot-through state.

During a non-shoot-through state, diode D starts to conduct with energy stored in winding W2 now released to the ac output. Based on the equivalent circuit shown in Fig. 2.9(b), the following expressions can thus be derived:

$$\begin{aligned}
 V_{dc} &= v_{W1} + V_C \\
 v_i &= V_C - v_{W2} \\
 i_{W1} - i_{W2} &= i_C \\
 i_{W1} &= I_m - \frac{i_{W2}}{n} = i_{dc}
 \end{aligned} \tag{2.12}$$

Again, by integrating the transformer winding voltages and capacitor current over one

Fig. 2.10. Shoot-through duty ratio versus input-to-output voltage gain.

Fig. 2.11. Normalized capacitor voltage of conventional Z-source inverter and trans-Z-source inverter obtained by varying n , d and $M=1.15*(1-d)$.

switching cycle and equalizing them to zero ($\int_0^T v_{W1} = 0$; $\int_0^T v_{W2} = 0$; $\int_0^T i_C = 0$), the capacitor voltage V_C , magnetizing current I_m , shoot-through current stress during shoot-through states $\hat{i}_{ST}$, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ of the trans-Z-source inverter shown in Fig. 2.8 (a) can be expressed as:

$$\begin{aligned} V_C &= \frac{1-d}{1-(n+1)d} V_{dc} \\ I_m &= \frac{n+1}{n} I_{dc} \\ \hat{i}_{ST} &= (1+n) I_{dc} \\ \hat{v}_i &= \frac{1}{1-(n+1)d} V_{dc} \\ \hat{v}_{ac} &= \frac{M}{1-(n+1)d} \frac{V_{dc}}{2} \end{aligned} \quad (2.13)$$

Performing the same analysis with the trans-quasi-Z-source inverter, the same magnetizing current, boosted dc-link voltage and ac output voltage can be obtained. The only difference noticed is the capacitor voltage, which is $V_C = \frac{nd}{1-(1+n)d} V_{dc}$ for the trans-quasi-Z-source inverter (2.13) undeniably states that the inverter voltage gain can be raised by increasing $n \geq 1$, d or both. It also states the narrowed range for d as $0 \leq d < 1/(1+n)$, obtained by setting the denominator ($1-(n+1)d$) to be greater than zero. The corresponding modulation range for M can then be stated as $0 \leq M \leq 1.15(1-d)$, which no doubt resembles that of the traditional Z-source inverter shown in Fig. 2.3. Its upper limit is however higher because of the smaller maximum d for $n > 1$. To further illustrate the smaller d and hence higher M , Fig. 2.10 shows that under the same input-to-output voltage gain $\hat{v}_{ac}/V_{dc}$, a trans-Z-source inverter needs a smaller shoot-through duty ratio, which can be further reduced by increasing its turns ratio. In other words, when the same duty ratio is assumed, the input-to-output voltage gain can be increased by increasing the transformer turns ratio. For illustration, the obtained voltage gain is plotted up to 20 in Fig. 2.10. Theoretically, voltage gain can be boosted up to infinity by approaching d to $1/(1+n)$.

Fig. 2.12. Γ -source inverter.

A point to note though when enforcing the same voltage gain is the same capacitor voltage stress experienced by the trans-Z-source and conventional Z-source inverters. This can be seen in Fig. 2.11, where it is also noticed that the trans-quasi-Z-source inverter shown in Fig. 2.8(b) has lowest capacitor voltage stress among the three. Therefore, the trans-Z-source inverters overcome the drawbacks of the traditional Z-source inverter linked to its low modulation ratio at high gain, which usually results in high voltage stress and poor waveform quality. In other words, the presented trans-Z-source inverters are capable of operating at high gain and modulation ratio simultaneously. They are however burdened by higher instantaneous current during the shorter shoot-through duration, as conveyed from (2.13). Besides high current stress, the trans-Z-source inverters are burdened by two other constraints. The first is their chopping input current caused by their input diode or six-switch inverter bridge. The second is their accompanied high turns ratio, and hence many winding turns at high gain.

2.5. Γ -Source Inverters

Although the boost enhancement and component reducing feature of the trans-Z-source inverters presented in Section 2.4 are attractive, their buck-boost performance is highly reliant on the characteristics of the coupled transformer used. In general, a higher turns ratio is always required for generating a higher boost gain. To provide alternatives with a different characteristic, a series of Γ -source inverters has been

proposed to achieve the same high voltage gain, but with a lower turns ratio. Other than this single difference, components used with the Γ -source inverters are the same as the trans-Z-source inverters [83]. The configuration of a type of Γ -source inverter is shown in Fig. 2.12, where both dotted ends of the transformer are tied to the cathode of diode D. The resulting transformer orientation has a Γ shape, and the network is thus referred to as the Γ -source network.

The operational principles of the Γ -source inverter are similar to those of the trans-Z-source inverter. During buck operation with no shoot-through state inserted, diode D will always conduct, hence causing the transformer windings to behave like two short-circuits. The network capacitor is then connected to the source in parallel, thus causing the dc-link voltage to be the same as the dc source voltage. The amount of buck gain obtained is then controlled by adjusting the modulation ratio M of the reference signal. Setting the dc-source voltage to V_{dc} , the peak AC output voltage $\hat{v}_{ac}$ is thus, as per usual, expressed as:

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (2.14)$$

A slight modification is however needed during boost operation, where an additional shoot-through state must be introduced to the usual inverter active and null states. During the shoot-through state, diode D is reverse biased, while the inverter bridge becomes shorted. Supposing the transformer turns ratio is n and based on the

Fig. 2.13. Equivalent circuits of Γ -source network during (a) shoot-through state and (b) non-shoot-through state.

equivalent circuit shown in Fig. 2.13(a), the following equations can be derived:

$$\begin{aligned} v_{W2} + V_C &= v_{W1}; \quad v_{W1} = n v_{W2} \\ \hat{i}_{ST} &= i_{W1} = -i_C \end{aligned} \quad (2.15)$$

During any of the non-shoot-through states, diode D becomes forward biased as shown in Fig. 2.13(b), and the following expressions can be derived:

$$\begin{aligned} v_{W2} &= V_{dc} - V_C \\ i_{dc} &= i_{W1} + i_C \end{aligned} \quad (2.16)$$

Based on setting the integral of the inductor voltage and capacitor current over a switching period to zero, the following voltage expressions related to the network shoot-through current $\hat{i}_{ST}$, capacitor voltage V_C , peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can then be derived in terms of the source voltage V_{dc} .

$$\begin{aligned} \hat{i}_{ST} &= \frac{1}{n-1} I_{dc} \\ V_C &= \frac{1-d}{1-\left(1+\frac{1}{n-1}\right)d} V_{dc} \\ \hat{v}_i &= \frac{1}{1-\left(1+\frac{1}{n-1}\right)d} V_{dc} \\ \hat{v}_{ac} &= \frac{M}{2} \hat{v}_i = \frac{M}{2} \frac{1}{1-\left(1+\frac{1}{n-1}\right)d} V_{dc} \end{aligned} \quad (2.17)$$

The boost gain is similar to that obtained by the trans-Z-source inverters. The only difference is the turns ratio of the transformer of the trans-Z-source inverters must be increased to produce a higher gain, while the turns ratio of the transformer found in the Γ -source inverters needs to be reduced to raise their gain. Therefore, a smaller transformer might be needed by the Γ -source inverters. To be precise, a higher boost gain than the traditional Z-source inverters can be obtained by adjusting the turns ratio of the trans-Z-source inverters to be $n>1$, while for the Γ -source inverters, the same can be done by setting $1<n<2$. The smaller transformer turns ratio can at times be an advantage especially at high gain. Take note that when turns ratio n decreases, shoot-through current increases and which increases the system loss. It is unavoidably a trade-off of high boost gain with small turns ratio.

2.6. LCCT Inverter

Fig. 2.14. LCCT inverter with continuous input current.

The Inductor-Capacitor-Capacitor-Transformer (LCCT) Z-source inverter was developed by integrating transformer-based topologies of the embedded Z-Source inverter [77]. The configuration of the LCCT Z-source inverter is shown in Fig. 2.14. Comparing with the asymmetrical embedded Z-source inverter, LCCT Z-source inverter replaces one of its inductors with a coupled inductor having two windings (windings 1 and 2) connected in series. The coupled inductor has two terminals connected to capacitors C1 and C2 shown in the figure. It has continuous input current, which helps to reduce the source stress, and its appropriately placed capacitors can help to block dc currents from saturating the transformer windings.

The operational principles of the LCCT Z-source inverter are similar to those of the trans-Z-source inverter. When no shoot-through state is added, the LCCT Z-source inverter operates like a conventional two-level inverter with diode D always forward biased, capacitor C2 and winding W1 always shorted. At all times, inductor L acts as an input filter for smoothing the input current. In this case, the dc-link voltage equals to the source voltage, and the peak output AC voltage $\hat{v}_{ac}$ can be expressed as:

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (2.18)$$

When shoot-through states are added, the LCCT Z-source inverter obtains its voltage boost capability. During the shoot-through states, the inverter bridge is shorted, while diode D becomes reverse biased by the high voltage capacitor. The equivalent circuit of the impedance network during shoot-through is then as shown in Fig. 2.15(a). Assuming that the transformer turns ratio $W1:W2 = n$, the related characteristic equations are then derived as:

$$\begin{aligned} v_{w2} &= -V_{C1}; \quad v_{w1} = n v_{w2}; \quad V_{dc} + v_L + V_{C2} = v_{w1} \\ \hat{i}_{ST} + i_{C1} &= -i_{C2} = -I_{dc} \end{aligned} \quad (2.19)$$

During the non-shoot-through states as shown in Fig. 2.15(b), the inverter bridge assumes one of the conventional active and null states, causing diode D to become forward biased, and the following characteristic equations to be derived.

$$\begin{aligned} v_{w1} &= V_{C2} \\ V_{dc} + v_L &= v_{w2} + V_{C1} \end{aligned} \quad (2.20)$$

The integrals of the inductor voltage and capacitor current over a switching period can next be set to zero, resulting in the following voltage expressions for computing the network shoot-through current $\hat{i}_{ST}$, capacitor voltage V_C , peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ in terms of the source voltage V_{dc} .

$$\begin{aligned} \hat{i}_{ST} &= (n + 1)I_{dc} \\ V_{C1} &= \frac{1-d}{1-(n+1)d} V_{dc}; \quad V_{C2} = \frac{nd}{1-(n+1)d} V_{dc} \end{aligned}$$

Fig. 2.15. Equivalent circuits of LCCT impedance network during (a) shoot-through state and (b) non-shoot-through state.

$$\hat{v}_i = \frac{1}{1-(n+1)d} V_{dc}$$

$$\hat{v}_{ac} = \frac{M}{2} \hat{v}_i = \frac{M}{2} \frac{1}{1-(n+1)d} V_{dc} \quad (2.21)$$

Comparing (2.21) with (2.5) for the conventional Z-source inverter with same shoot-through duty ratio, the boost gain of the LCCT Z-source inverter is definitely higher than the traditional Z-source inverter, so long as the coupled transformer turns ratio n is greater than 1. The passive component count will not increase so long as the coupled transformer is wound on a high permeability magnetic core. Moreover, with the series connection of dc source and inductor L , the input current is made smooth without demanding for an additional input filter. The input filter is to date always required by the traditional Z-source inverter if its input current is to be conditioned. In addition, the series connection of capacitors with the transformer windings results in dc current being blocked and hence no saturation of the transformer [77]. Therefore, the proposed topology has nearly the same efficiency, but produces a higher boost gain and a smoother input current, as compared to the traditional Z-source inverter.

Fig. 2.16. Pulse width modulation of Z-source inverters.

2.7. Pulse Width Modulation of Z-source Inverters

Various pulse width modulation schemes have so far been implemented for modulating Z-source inverters [33, 84-86]. The improved boost control modulation as described in [86] is preferred here as it retains six commutations per switching cycle, which is the same as the conventional three-phase inverter carrier-based modulation scheme. Switching losses and harmonic performances of the inverters will hence not be degraded severely. To perform the modulation with shoot-through states inserted equally among the three phase-legs, the original three sinusoidal references must be vertically shifted to produce six modified references, whose equations are written as follows.

$$\begin{aligned}
 V_{\max}(SX) &= V_{\max} + \frac{d}{2} \\
 V_{\max}(SX') &= V_{\max} + \frac{d}{6} \\
 V_{\text{mid}}(SX) &= V_{\text{mid}} + \frac{d}{6} \\
 V_{\text{mid}}(SX') &= V_{\text{mid}} - \frac{d}{6} \\
 V_{\min}(SX) &= V_{\min} - \frac{d}{6} \\
 V_{\min}(SX') &= V_{\min} - \frac{d}{2}
 \end{aligned} \tag{2.14}$$

where $X = A, B \text{ or } C$, $V_{\max}$ is the reference with the maximum value among the three sinusoidal references, V_{mid} is the reference in the middle, and $V_{\min}$ is the reference with the smallest value. Viewing Fig. 2.16 as an example, where six transitions occur (000-100-110-111-110-100-000), $V_{\max}$ is reference V_a , V_{mid} is reference V_b and $V_{\min}$ is reference V_c . By shifting the switches SX and SX' according to (2.14), a shoot-through duration of $\frac{d}{6}$ is inserted by phase X , as represented by any one of the shaded areas in Fig. 2.16. In total, six shoot-through states are inserted to the six transitions per switching cycle. The modulation index is still represented by M , whose value is confined to be below $1.15 \cdot (1-d)$ when triplen offset is added. Simulation results of the traditional Z-source inverter controlled by the improved PWM scheme are shown in Fig. 2.17. Its associated input and load variations are displayed for showing the robustness of the improved modulation scheme.

Fig. 2.17. Traditional Z-source inverters simulation results of input voltage V_{dc} , DC-link voltage v_i , line voltage v_{AB} and line current i_a , i_b , i_c of (a) variation of input voltage and (b) variation of load.

2.8. Summary

This chapter reviews the basic theories behind two-level voltage buck-boost inverters. The reviewed inverters are conventional two-stage buck-boost inverter, single-stage Z-source inverter, continuous input current embedded Z-source inverter and enhanced voltage boost transformer-based Z-source inverter. In particular, for the Z-source inverter and its various variants, they have the advantages of not increasing active components and omission of dead-time from the phase-legs. Embedded Z-source inverter also has a continuous input current, which is better for the dc source, as compared to the traditional Z-source inverter. However, the embedded Z-source inverter still requires a high shoot-through duty ratio, and hence a low modulation ratio, to obtain the high voltage gain.

To resolve the low modulation concern, trans-Z-source inverters are proposed to enhance the voltage boost capability by utilizing magnetically coupled circuits. That also effectively reduces the passive component count, and improves the voltage boost gain, while maintaining a high modulation ratio for reduced system voltage stress and improved waveform quality. The trans-Z-source inverters however draw the same discontinuous chopping input current as the traditional Z-source inverters. Their transformer turns ratio can also be at times high if a higher voltage boost is required. These shortcomings lead to interest in developing new sophisticated circuits, which is also the intention of this thesis.

Chapter 3 Three-Level Z-Source NPC Inverters

Comparing with the traditional two-level inverters, NPC inverter has a lower device voltage stress and better harmonic performance [87-92]. It is thus commonly chosen for medium voltage, high power applications like ac motor drives [90, 93-96]. It has also been investigated for low power applications, as mentioned in [97]. However, the NPC inverter has some drawbacks, where one of them is its voltage-buck mode when no additional DC-DC boost converter is added to its front end. This constraint might not be preferred by renewable energy systems, where at times, boost function might be needed for interfacing low voltage sources such as fuel cells or batteries to the higher voltage utility grid.

To add boost functionality to the otherwise buck NPC inverter, the thought of integrating Z-source and NPC topologies was studied in [98], where two impedance-source networks can clearly be seen. Reference [99] subsequently presents another Z-source NPC inverter with only one impedance-source network. Regardless of the number of networks, the proposed Z-source NPC inverters will always operate with the minimum number of device commutations per half carrier cycle, as long as the right modulation scheme is used. With the right modulation scheme, the Z-source NPC inverter can also operate with either a minimal harmonic distortion or a completely eliminated common-mode voltage. The Z-source NPC inverter is thus an appropriate combination of concepts for introducing boost functionality without affecting the existing three-level switching. Because of its effectiveness, Z-source NPC inverter has already been tried with distributed generation systems [100] and photovoltaic systems [101, 102]. Its review is therefore presented in this chapter before introducing improvements to it in later chapters.

3.1. Z-Source NPC Inverter with Two Impedance Networks

As stated in [98], cascading two Z-source networks and connecting to a classic NPC inverter, Z-source NPC inverter is created with two isolated dc sources. The configuration is shown in Fig. 3.1, where the two impedance networks are observed to

Fig. 3.1. Topology of traditional Z-source NPC inverter with two cascaded LC impedance networks.

have the same structure as the traditional Z-source inverter. Therefore, the same circuit operational principles are expected, where during voltage-buck operation, no shoot-through state is inserted, hence causing the inductors of the Z-source networks to behave like short circuits. The capacitors are also in parallel with the dc sources. With these observations, expressions for computing the peak dc-link voltages $\hat{v}_{iup}$ and $\hat{v}_{idn}$, and peak ac output voltage $\hat{v}_{ac}$ can be derived as those in (3.1) when no shoot-through state is added:

$$\begin{aligned}\hat{v}_{iup} &= \hat{v}_{idn} = \hat{v}_i = \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{M}{2} V_{dc}\end{aligned}\quad (3.1)$$

On the other hand, when shoot-through states are inserted for voltage boosting, expressions for computing the capacitor voltage V_C , dc-link voltages $\hat{v}_{iup}$ and $\hat{v}_{idn}$, and peak ac output voltage $\hat{v}_{ac}$ can be derived as (3.2) if the shoot-through duty ratio is denoted as d .

$$\begin{aligned}V_{C1up} &= V_{C2up} = V_{C1dn} = V_{C2dn} = V_C = \frac{1-d}{1-2d} \frac{V_{dc}}{2} \\ \hat{v}_{iup} &= \hat{v}_{idn} = \hat{v}_i = \frac{1}{1-2d} \frac{V_{dc}}{2}\end{aligned}$$

$$\hat{v}_{ac} = \frac{M}{2} \frac{1}{1-2d} V_{dc} \quad (3.2)$$

Comparing (2.5) and (3.2), under the same boosted ac output voltage, the capacitor voltage stress and dc-link voltage stress of the two impedance networks of the Z-source NPC inverter are only half those of the traditional Z-source inverter. This is clearly an advantage of the Z-source NPC inverter, but of course only with more passive and active components added.

3.2. Z-Source NPC Inverter with Single Impedance Network

The circuit configuration showing a Z-source NPC inverter with only a single LC network is given in Fig. 3.2, as first proposed in [99]. The X-shaped LC impedance network is added to the front-end of a classic NPC inverter, as shown by the shaded area. Unlike the impedance network of a two-level Z-source inverter, the LC network shown in Fig. 3.2 uses one additional dc source and one additional diode to form a balanced NPC circuit. The neutral point is then tapped from the mid-point of the two series-connected dc sources. The resulting operating modes are similar to those of the traditional two-level Z-source inverter. For its buck operating mode, the inductors L1

Fig. 3.2. Topology of Z-source NPC inverter with single LC network.

and L2 are shorted, hence causing capacitors C1 and C2 to become parallel-connected with the dc source during steady state. Diode D1 and D2 will also always be forward biased. The dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can then be derived as follows when no shoot-through state is added:

$$\begin{aligned}\hat{v}_i &= \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{M}{2} V_{dc}\end{aligned}\quad (3.3)$$

When changed to its boost operating mode, shoot-through states must be inserted to the state sequence, together with the conventional active and null states. During shoot-through, the inverter bridge can then be represented by a short-circuit, while diodes D1 and D2 become reverse biased by the network capacitors. The two network inductors are also charged up by the two network capacitors. In contrast, during any of the non-shoot-through states, the diodes are forward biased with energy stored in the inductors now released to power the external ac load. The capacitor voltage V_C , peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can then be calculated as:

$$\begin{aligned}V_{C1} = V_{C2} = V_C &= \frac{1-d}{1-2d} V_{dc} \\ \hat{v}_i &= \frac{1}{1-2d} V_{dc} \\ \hat{v}_{ac} &= \frac{M}{2} \frac{1}{1-2d} V_{dc}\end{aligned}\quad (3.4)$$

Therefore, under the same boosted ac gain $\hat{v}_{ac}/V_{dc}$, the capacitor voltage stress of the Z-source NPC inverter with a single LC network is the same as the two-level Z-source inverter. Thus, the advantage of the Z-source NPC inverter with a single LC network is only its halved switching device voltage stress and better output waveform quality.

3.3. Pulse Width Modulation of Z-Source NPC Inverters

Z-source NPC inverter with cascaded impedance networks can be controlled by either the modified PDPWM or APODPWM scheme. For the modified PDPWM scheme, the upper and lower triangle carriers are in phase [98]. They are used to compare with two modified voltage references placed above and below the original reference by a height proportional to half the shoot-through duty ratio. In this way, it allows the

Fig. 3.3. Modified PDPWM for Z-source NPC inverters.

independent generation of upper Z-source network shoot-through state indicated as U and lower network shoot-through state indicated as G, respectively. An example transition (0-1-1,1-1-1,10-1) is shown in Fig. 3.3, where references $V_a(SA)$, $V_b(SB)$ and $V_c(SC)$ are the three original NPC inverter modulating references, and $V_a(SA')$ and $V_c(SC')$ are the two additional modified references used for switch SA1 and SC2'. The two modified references can be represented by:

$$\begin{aligned} V_{\max}(SX1) &= V_{\max} + d \\ V_{\min}(SX2) &= V_{\min} - d \end{aligned} \quad (3.5)$$

By doing so, the intermediate shoot-through state U is inserted at the $0 \rightarrow 1$ transition of phase-leg A by gating $(SA1, SA2, SA1', SA2') = (0,1,1,0) \rightarrow (1,1,1,0) \rightarrow (1,1,0,0)$. During the U state (1,1,1,0), diode DA1 is forward-biased, and thus the upper network

is short-circuited. Insertion of lower shoot-through state G is similar to that of the U state except it involves another phase-leg. The advantage of shifting the references is the insertion of shoot-through states by shifting the ON/OFF times of the switches without introducing additional commutation. The number of device commutations per switching cycle therefore remains the same as the traditional NPC inverter. It is also reported that the maximum modulation index can be extended to 1.15 by adding a third harmonic offset with one sixth of the fundamental amplitude to the three phase sinusoidal references [98].

For modified APODPWM, the upper and lower triangular carriers have a 180° phase shift [99]. These carriers are compared with two additional references added to the usual three sinusoidal references used with the classical NPC inverter. One of the additional references is derived by adding a height proportional to the duty ratio to the

Fig. 3.4. Modified APODPWM for Z-source NPC inverters.

maximum reference $V_{\max(SX)}$ ($\max(V_a, V_b, V_c)$). This added reference is for controlling switch SX1. The second additional reference is obtained by subtracting a height proportional to its duty ratio away from the minimum reference $V_{\min(SX)}$ ($\min(V_a, V_b, V_c)$). This modified reference is for controlling switch SY2', as shown in Fig. 3.4. The rest of the switches are switched "normally" as per the conventional NPC inverter.

The described method has the advantage of adjusting the time advance/delay of switches SX1 and SY2' without affecting the overall device commutations. In addition, the upper three switches of phase-leg X and lower three switches of phase-leg Y will be ON at the same time, hence creating a short-circuit at the NPC inverter bridge. At the same time, diodes DX2 and DY1 will become forward biased. One example state sequence is shown in Fig. 3.4, where the reference of phase-leg A has the maximum value V_a and reference of phase-leg C has the minimum value V_c during the state transition from $[000 \rightarrow 10-1 \rightarrow 1-1-1 \rightarrow 10-1 \rightarrow 000]$. Accordingly, the additional maximum reference and minimum reference are hence expressed as:

$$\begin{aligned} V_{\max(SX1)} &= V_{\max} + d \\ V_{\min(SX2)} &= V_{\min} - d \end{aligned} \quad (3.6)$$

The two added references are for controlling switch SA1 and switch SC2', respectively. They cause the ON/OFF times of switch SA1 and SC2' to be advanced/delayed so that SA1, SA1', SA2 and SC1', SC2, SC2' are turned ON simultaneously. With diodes DA2 and DC1 forward biased, the shoot-through state S is added between transition $[000 \rightarrow 10-1]$ and $[10-1 \rightarrow 000]$. In effect, the modified APODPWM scheme allows the two impedance networks of the Z-source NPC inverter with two cascaded impedance networks to be shorted simultaneously, so that it can be used for either Z-source NPC inverters with single LC network or two cascaded impedance networks.

3.4. Summary

This chapter reviews Z-source NPC inverters with either two cascaded or a single impedance network. Both types of inverters have lower voltage stress and better

output performance than the two-level Z-source inverters. Both of the NPC inverters can be controlled by either the modified PDPWM scheme or the modified APODPWM scheme, while retaining the device commutations per switching cycle the same as traditional NPC inverter.

Chapter 4 Asymmetrical Transformer-Based Embedded Z-Source Inverters

Despite their advantages mentioned in Chapter 2, Z-source inverters are burdened by their chopping input current and low modulation ratio at high gain. The former may shorten the lifespan of certain sources, while the latter can cause unnecessarily high voltage stress and poor spectral characteristic. To smooth the source current, an external input filter has to be added or the source can be shifted to a position in series with one of the existing Z-source inductors. The Z-source inductor can then help to filter the source current without having to add an external filter. In [70] and [103], this concept led to the creation of the embedded and quasi Z-source inverters, whose second advantage is their ability to lower the Z-source capacitor voltages. Input-to-output gain versus modulation ratio produced by these inverters are however still the same as the traditional Z-source inverters.

Modifications were subsequently introduced to raise the inverter gain, while maintaining a high modulation ratio. Most techniques however require a high component count [104, 105], which may not be attractive. To avoid such deterrent, the trans-Z-source inverters as described in Section 2.4 use coupled transformers in place of the inductors found in the original Z-source network. The inverter voltage gain can then be raised by increasing the transformer turns ratio, but at the expense of chopping input current even if the quasi or embedded variants are used. To rectify this latter concern, a number of asymmetrical transformer-based embedded Z-source (EZ-source in short) inverters are presented in the thesis, whose gain is higher and input current is smoother. Operational principles, similarities and differences among the proposed inverters are discussed before verifying their performances in experiments.

4.1. Type EA Inverters

From (2.5), the input-to-output gain of the conventional Z-source and embedded Z-source inverters can be written as $\hat{v}_{ac}/V_{dc} = 0.5M/(1 - 2d)$. By setting its denominator to zero, the corresponding range of variation for the duty ratio can be written as $0 \leq d < 0.5$, where the extreme of 0.5 leads to infinite gain. The remaining fractional time $(1 - d)$ is occupied by active or null state, whose associated modulation range is then defined as $0 \leq M \leq 1.15(1 - d)$, where 1.15 is a multiplier introduced by triplen offset. Modulation ratio at high gain is therefore low, whose accompanied impacts are poor spectral performance and unnecessarily high dc-link voltage. To mitigate these concerns while drawing a continuous source current, a number of asymmetrical transformer-based EZ-source inverters are proposed from this section onwards, beginning with the *EA* inverter shown in Fig. 4.1.

Fig. 4.1. Asymmetrical transformer-based EZ-source inverters. Types (a) *EA1* (b) *EA2*

Fig. 4.2. Network equivalent circuit of inverter EA1 during (a) shoot-through states and (b) non-shoot-through states.

Fig. 4.3. Network equivalent circuit of inverter EA2 during (a) shoot-through states and (b) non-shoot-through states.

As seen from Fig. 4.1, the EA inverter is realized with a coupled transformer replacing an inductor found in an asymmetrical EZ-source inverter. The replacement does not change the inverter operation, meaning it can still enter the shoot-through or non-shoot-through (active or null) state depending on the amount of boosting required. When in the shoot-through state, the VS bridge is again replaced by a short circuit, while diode D is replaced by an open circuit. The impedance source network equivalent circuit for inverter EA1 during shoot-through state is shown in Fig. 4.2(a). The corresponding voltage and current expressions can then be written as:

$$v_{w2} = V_{C1}; V_{C2} + V_{dc} = v_L; v_{w1} = n_{EA}v_{w2}$$

$$i_{W2} = i_{C1}; i_{C2} = -I_{dc} \quad (4.1)$$

where I_{dc} is the average dc current drawn from the source, and n_{EA} is the transformer turns ratio associated with the EA inverters.

On the other hand, when in a non-shoot-through state, the VS bridge can be replaced by a current source whose value is non-zero when in an active state or zero when in a null state. Simultaneously, diode D starts to conduct as shown in Fig. 4.2(b), leading to the following voltage and current expressions:

$$\begin{aligned} V_{C1} + v_L + v_{W1} &= V_{dc}; V_{C2} + v_{W2} + v_{W1} = 0 \\ V_{C1} &= v_{W2} + \hat{v}_i; V_{C2} + V_{dc} = v_L + \hat{v}_i \\ i_{W1} &= i_{C2} + I_{dc} \\ i_{C1} &= i_{W1} - i_{W2} \end{aligned} \quad (4.2)$$

Performing state-space averaging on the inductive elements then leads to compute the capacitor voltages, dc-link voltage, and peak ac output voltage as:

$$\begin{aligned} V_{C1} &= \frac{1-d}{1-(2+n_{EA})d} V_{dc}; V_{C2} = \frac{d(1+n_{EA})}{1-(2+n_{EA})d} V_{dc} \\ \hat{v}_i &= \frac{1}{1-(2+n_{EA})d} V_{dc} \\ \hat{v}_{ac} &= \frac{1}{1-(2+n_{EA})d} \left(\frac{MV_{dc}}{2} \right) \end{aligned} \quad (4.3)$$

Similar state-space averaging performed on the capacitors leads to (4.4) for computing the peak currents $\hat{i}_{W2}$ and $\hat{i}_{ST}$ flowing through winding W2 and the dc-link, respectively, during the shoot-through state. Note that current through W1 is not mentioned in (4.4) because it is usually much smaller, and hence not a major concern. Its value is in fact zero ($\hat{i}_{W1} = 0$) during the shoot-through state because of the blocking of diode D.

$$\begin{aligned} \hat{i}_{W2} &= (1 + n_{EA})I_{dc} \\ \hat{i}_{ST} &= (2 + n_{EA})I_{dc} \end{aligned} \quad (4.4)$$

Collectively, (4.3) and (4.4) show that the inverter voltage gain can be raised by increasing the transformer turns ratio, but with the trade-off of higher network

currents during the shorter shoot-through interval. As per earlier, proof for the shorter shoot-through interval can be derived by setting the denominator of (4.3) to zero. The resulting range is given by $0 \leq d < 1/(2 + n_{EA})$, whose upper limit is undeniably smaller than 0.5 for $n_{EA} > 0$. Modulation ratio, limited by $0 \leq M \leq 1.15(1 - d)$, can then be higher to improve the overall spectral quality and dc-link utilization. These advantages are further accompanied by the continuous input current drawn from the source, which no doubt is a characteristic inherited from the EZ-source placement concept. A second topology (*EA2*) sharing the same gain is shown in Fig. 4.1(b), whose corresponding network equivalent circuit is illustrated in Fig. 4.3 and relevant voltage expressions are again given by (4.3). Its peak winding *W2* and dc-link currents during shoot-through also remain the same as in (4.4), but not its winding *W1* current, whose expression is given by $\hat{i}_{W1} = I_{dc}$ instead of zero. Current through *W1* is however usually not a concern since its value is comparably much smaller than that flowing through *W2*.

4.2. Type EB Inverters

The next two asymmetrical transformer-based EZ-source inverters proposed are shown in Fig. 4.4(a) and (b) (*EB1* and *EB2*). The network equivalent circuits are shown in Fig. 4.5 and Fig. 4.6 respectively. They are classified separately because their governing voltage expressions derived from state-space averaging are found to be different from those in (4.3). For easier reference, the *EB* expressions are written in (4.5), which can be made equal to (4.3) if their turns ratio n_{EB} is set according to (4.6).

$$V_{C1} = \frac{1-d}{1-(2+1/(n_{EB}-1))d} V_{dc}; V_{C2} = \frac{n_{EB}d/(n_{EB}-1)}{1-(2+1/(n_{EB}-1))d} V_{dc}$$

$$\hat{v}_l = \frac{1}{1-(2+1/(n_{EB}-1))d} V_{dc}$$

$$\hat{v}_{ac} = \frac{1}{1-(2+1/(n_{EB}-1))d} \left(\frac{MV_{dc}}{2} \right) \quad (4.5)$$

$$n_{EA} = \frac{1}{n_{EB}-1} \text{ or } n_{EB} = \frac{1}{n_{EA}} + 1 \quad (4.6)$$

Since n_{EA} and n_{EB} are inversely related, gain of the *EB* inverters is raised by lowering the transformer turns ratio n_{EB} towards unity, rather than increasing it like in the *EA* cases. Peak current expressions of the *EB* inverters can also be written in (4.7), which

when compared with (4.4), demonstrate a significant difference even after setting their turns ratio to be in agreement with (4.6). To be more specific, winding current $\hat{i}_{W1}$ has been mentioned in (4.7) since its value is now comparable to those flowing through winding W2 and the dc-link during the shoot-through state. This is especially so for low turns ratio close to one, and is definitely in agreement with classical transformer theory, where the same number of turns will carry the same current when magnetically coupled.

$$\hat{i}_{W1} = \left(1 + \frac{1}{n_{EB} - 1}\right) I_{dc}$$

(a)

(b)

 Fig. 4.4. Asymmetrical transformer-based EZ-source inverters. Types (a) *EB1* (b) *EB2*

Fig. 4.5. Network equivalent circuit of inverter *EB1* during (a) shoot-through states and (b) non-shoot-through states.

Fig. 4.6. Network equivalent circuit of inverter *EB2* during (a) shoot-through states and (b) non-shoot-through states.

$$\hat{i}_{W2} = \begin{cases} (2 + 1/(n_{EB} - 1))I_{dc}, & \text{Type EB1} \\ (1 + 1/(n_{EB} - 1))I_{dc}, & \text{Type EB2} \end{cases}$$

$$\hat{i}_{ST} = \left(2 + \frac{1}{n_{EB} - 1}\right)I_{dc} \quad (4.7)$$

4.3. Type EC Inverters

Type *EC* inverters are shown in Fig. 4.7(a) and (b). They are respectively named as the *EC1* and *EC2* inverters, according to the network equivalent circuits as shown in Fig. 4.8 and Fig. 4.9, whose common voltage expressions are derived as:

$$V_{C1} = \frac{1-d}{1-(1+n_{EC})d} V_{dc}, V_{C2} = \frac{n_{EC}d}{1-(1+n_{EC})d} V_{dc}$$

$$\hat{v}_i = \frac{1}{1-(1+n_{EC})d} V_{dc}$$

$$\hat{v}_{ac} = \frac{1}{1-(1+n_{EC})d} \left(\frac{MV_{dc}}{2} \right) \quad (4.8)$$

Input-to-output gain deduced from (4.8) can therefore be written as $0.5M/(1 - (1 + n_{EC})d)$, which is the same as the trans-Z-source inverters proposed in [82] that draw discontinuous input current. Equations (4.3), (4.5) and (4.8) can further be made equal if their respective turns ratios are set according to (4.9)

Fig. 4.7. Asymmetrical transformer-based EZ-source inverters. Types (a) *EC1* and (b) *EC2*.

Fig. 4.8. Network equivalent circuit of inverter *EC1* during (a) shoot-through states and (b) non-shoot-through states.

Fig. 4.9. Network equivalent circuit of inverter *EC2* during (a) shoot-through states and (b) non-shoot-through states.

$$n_{EA} = \frac{1}{n_{EB}-1} = n_{EC} - 1 \text{ or } n_{EC} = n_{EA} + 1 = \frac{n_{EB}}{n_{EB}-1} \quad (4.9).$$

Types *EA* and *EC* inverters are therefore proportionally related in the sense that their turns ratios must be increased to raise their respective inverter gains. Turns ratio of the *EC* inverters is however higher, which somehow causes them to be not as competitive as the *EA* and *EB* inverters. Peak currents of the *EC* inverters can also be derived as (4.10), where $\hat{i}_{W1}$ is again not included because of its comparably lower shoot-through values ($\hat{i}_{W1} = I_{dc}$ for *EC1* and $\hat{i}_{W1} = 0$ for *EC2*).

$$\hat{i}_{W2} = \begin{cases} (1 + n_{EC})I_{dc}, & \text{Type EC1} \\ n_{EC}I_{dc}, & \text{Type EC2} \end{cases}$$

$$\hat{i}_{ST} = (1 + n_{EC})I_{dc} \quad (4.10)$$

4.4. Topology Comparison

Fig. 4.10. Turns ratio versus input-to-output gain ($d = 0.135$ and $M = 0.92$).

Fig. 4.11. Normalized capacitor voltages versus gain obtained by varying turns ratio, d and $M = 1.15(1 - d)$.

Fig. 4.12. Shoot-through duty ratio versus gain obtained by fixed turns ratio $n_{EA} = 1/(n_{EB}-1) = n_{EC} - 1 = 2$.

For most applications, the input and output conditions are determined by the environment or user-defined, and hence cannot be modified. The inverter designed must therefore adapt to these given conditions, which for comparison here, mean a constant input-to-output gain $\hat{v}_{ac}/V_{dc}$. It is also reasonable here to demand that the shoot-through duty ratios and modulation ratios of the inverters are set equal so that they produce the same waveform quality and device stress. Turns ratios for the different inverter types must therefore satisfy (4.9), which when plotted against the common voltage gain, gives those variation curves shown in Fig. 4.10. The distinctive feature observed from the figure is the decreasing turns ratio of the *EB* inverters, which eventually levels off at one. This trend is obviously different from those of the *EA* and *EC* inverters, whose turns ratios must increase, and might become too excessive at high gain.

Table. 4.1. Summarized features of asymmetrical transformer-based EZ-source inverters.

Feature	EA1	EA2	EB1	EB2	EC1	EC2
Turns Ratio Relationship for Gain Equalization	$n_{EA} = \frac{1}{n_{EB} - 1} = n_{EC} - 1$					
Turns Ratio Trend for Gain Increasing	Increasing	Increasing	Decreasing	Decreasing	Increasing	Increasing
Input-To-Output Gain	$\frac{v_{ac}}{V_{dc}} = \frac{0.5M}{1-(2+n_{EA})d}$ (Same for all)					
Range of Shoot-Through Duty Ratio	$0 \leq d < 1/(2 + n_{EA}) < 0.5$ (Same for all)					
Range of Modulation Ratio	$0 \leq M \leq 1.15(1 - d)$ (Same for all)					
Capacitor Voltages	$\frac{V_{C1}}{V_{dc}} = \frac{1-d}{1-(2+n_{EA})d}$ and $\frac{V_{C2}}{V_{dc}} = \frac{d(1+n_{EA})}{1-(2+n_{EA})d}$ (Same for all)					
Peak DC-Link Current	$\frac{i_{ST}}{I_{dc}} = (2 + n_{EA})$ (Same for all)					
Peak Winding Currents	$\frac{i_{W1}}{I_{dc}} = 0$ $\frac{i_{W2}}{I_{dc}} = (1 + n_{EA})$	$\frac{i_{W1}}{I_{dc}} = 1$ $\frac{i_{W2}}{I_{dc}} = (1 + n_{EA})$	$\frac{i_{W1}}{I_{dc}} = (1 + n_{EA})$ $\frac{i_{W2}}{I_{dc}} = (2 + n_{EA})$	$\frac{i_{W1}}{I_{dc}} = (1 + n_{EA})$ $\frac{i_{W2}}{I_{dc}} = (1 + n_{EA})$	$\frac{i_{W1}}{I_{dc}} = 1$ $\frac{i_{W2}}{I_{dc}} = (2 + n_{EA})$	$\frac{i_{W1}}{I_{dc}} = 0$ $\frac{i_{W2}}{I_{dc}} = (1 + n_{EA})$
Advantages	<ul style="list-style-type: none"> - High modulation ratio at high gain. - Better waveform quality. - Better dc-link utilization and hence lower switch stress. 					
Disadvantages	<ul style="list-style-type: none"> - High instantaneous winding and dc-link currents. - Require transformer with tight magnetic coupling and hence lower leakage impedance. 					
Other Comments	<ul style="list-style-type: none"> - Many winding turns at high gain. - One unstressed winding. 		<ul style="list-style-type: none"> - Lesser winding turns. - Windings stressed equally because of near unity turns ratio. 		<ul style="list-style-type: none"> - Highest number of winding turns. - One unstressed winding. 	

Despite their different turns ratio variations, capacitor voltages of the six inverters are found to share two common values when the relationship in (4.9) is enforced. Variations of these two capacitor voltage values can be found in Fig. 4.11, which in concept, were obtained by varying the turns ratio, shoot-through duty ratio and modulation ratio to arrive at the different gain values listed on the horizontal axis. These curves are interesting since they inform that a certain desired gain can be obtained by changing the turns ratio (increasing for types *EA* and *EC*, and decreasing for type *EB*) without increasing the capacitor voltages even though it can lead to a lower dc-link voltage associated with a smaller duty ratio.

The same plotting can be performed for shoot-through duty ratio and voltage gain, as shown in Fig. 4.12. It clearly shows that the duty ratio needed by the proposed asymmetrical transformer based EZ-source inverters is smaller than that of the conventional Z-source inverter. Therefore, larger modulation ratio $M = 1.15(1-d)$ can be utilized with long proven improved output performance as well as lower switch stresses. Similar plotting can be carried out to show the shoot-through dc-link current, whose variation is shown in Fig. 4.13. Only one curve is shown in the figure since it is a common curve produced by all six inverters when (4.9) is satisfied. Winding currents of the six inverters are however different, and are better summarized in Table 4.1. Their variations are either the same or proportional to the shoot-through dc-link

Fig. 4.13. Normalized shoot-through dc-link current versus gain obtained by varying turns ratio ($d = 0.135$ and $M = 0.92$).

current shown in Fig. 4.13, and are hence not explicitly plotted in the paper.

Table. 4.2 Experimental Components List

Component	Value	Part Number
Capacitors $C1$ and $C2$	500V, 470 μ F	PEH200ZH3470MU2
Input inductor L and coupled inductor core	125 μ , 178 nH/T ²	C055906A2
Input inductor L and coupled inductor winding wire	20 parallel strings	AWG32
Diode D	600V, 16A	D16S60C
Switching devices ($SA - SC'$)	1200V, 50A	F4-50R12KS4

Table. 4.3. Simulated efficiencies and component losses for traditional and proposed inverters

Inverter Type ($n_{EA} = 2$ in (4.9))								
Gain	Z-Source	EZ-Source	$EA1$	$EA2$	$EB1$	$EB2$	$EC1$	$EC2$
0.92	93.12%	94.13%	93.81%	94.22%	93.89%	94.09%	94.21%	93.78%
1.35	93.08%	94.11%	93.56%	93.98%	93.52%	93.72%	93.96%	93.46%
2	93.03%	94.08%	93.31%	93.72%	93.14%	93.34%	93.69%	93.11%

Break-up component losses when gain = 1.35								
Gain = 1.35	Z-Source	EZ-Source	$EA1$	$EA2$	$EB1$	$EB2$	$EC1$	$EC2$
Capacitors	0.34%	0.19%	0.44%	0.42%	0.43%	0.44%	0.42%	0.43%
Transformer	2.76%	1.81%	2.19%	1.77%	2.23%	2.03%	1.79%	2.30%
Switching	3.82%	3.89%	3.81%	3.83%	3.82%	3.81%	3.83%	3.81%

Another feature for comparison among the inverters is efficiency, whose value for each inverter was obtained from simulation. The simulated model was constructed with resistances measured from the experimental setup and semiconductor losses read from datasheets. The components used are summarized in Table. 4.2, while the obtained results are tabulated in Table. 4.3, where values for the traditional Z-source and EZ-source inverters are also included (obtained with the same number of turns and core C055906A2 used for winding their inductors). The numbers show that efficiencies of the proposed inverters are closely comparable to those of the traditional Z-source and EZ-source inverters. The closeness in efficiency may not appear justifiable initially since the proposed inverters carry much higher shoot-through

instantaneous currents. These are however for a short time interval only, and can more than shadowed by higher losses generated by the traditional inverters due to their higher dc-link voltage and poorer spectrum at the same input-to-output gain.

4.5. Experimental Results

The proposed transformer-based inverters were assembled and tested in the laboratory. Parameters used for the experiments were tabulated in Table. 4.4, where it should be noted that the same transformer turns ratio of 1.5 had been used for all inverters rather than in accordance to (4.9). Their boosted gains would hence be different. Results obtained from the experiments are discussed as follows, but before proceeding, it is important to mention that while designing the transformer, it is necessary to tightly interleave the two windings by following the bifilar winding technique [82]. This will help to keep the mutual coupling coefficient between the two windings close to unity and their leakage inductances close to zero. Any compromise will lead to overvoltage spikes at instants of switching between non-shoot-through and shoot-through states. An alternative to remove the spikes is to add snubbers like those found in [106] and [107] for the tapped-inductor dc-dc converter and sparse matrix converter,

Table. 4.4. Experimental parameters

System Parameter	Value
DC Source, V_{dc}	100 V
Fundamental AC Frequency, f	60 Hz
Switching Frequency, f_s	10 kHz
Capacitors $C1$ and $C2$	470 μ F
Inductor L	3.2 mH
Transformer Turns Ratio	1.5
Y-Connected RL Load	38 Ω , 10 mH
Modulation Index, M	0.92
Shoot-Through Duty Ratio, d (Voltage-Boost Mode)	0.135
Shoot-Through Duty Ratio, d (Voltage-Buck Mode)	0

respectively. This will however raise the system cost, which unquestionably is undesirable. It is hence better to wind the transformer properly by using an appropriate core and the bifilar winding technique, whose subsequently obtained results have demonstrated their effectiveness even without snubbers. Due to their tight coupling nature, the inductance of each winding will also be enhanced by the mutual coupling of the other winding. The coupled winding turns and magnetic permeability requirements are therefore lower than those of two individual inductors. The size of the coupled magnetic core will thus not be increased. And the energy loss increase would only be caused by the additional winding of the coupled inductor, which is expected to be low when high conductivity material is used.

4.5.1. Type EA Inverters

For illustrating the type *EA* performances, results obtained for the inverter shown in Fig. 4.1(a) are presented in Fig. 4.14. Under buck mode when no shoot-through state is used, the peak ac voltage should theoretically be $\hat{v}_{ac} = 0.92 \times \frac{100}{2} = 46$ V, and the peak ac current should approximately be $\hat{i}_{ac} = 46 / \sqrt{38^2 + 3.77^2} = 1.20$ A based on the parameters given in Table III. This value indeed matches that read from Fig. 4.14(a). Under voltage-boost mode, the relevant voltage values can also be computed as $V_{C1} = 164$ V, $V_{C2} = 64$ V, $\hat{v}_i = 189$ V and $\hat{v}_{ac} = 87$ V, which when applied to the same load, gives a peak ac current of $\hat{i}_{ac} = 2.27$ A. These values are again the same as in Fig. 4.14(b). More waveforms are shown in Fig. 4.15 for the *EAI* inverter, which confirm that the input current drawn is smooth, capacitor voltages are unequal and instantaneous currents flowing through winding *W2* and the dc-link during shoot-through state are high (happened at zero dc-link voltage in Fig. 4.15(a)).

The weighted total harmonic distortion (WTHD) of the switched line voltage and total harmonic distortion (THD) of the output line current were also computed with data points saved with Fig. 4.14(b). Their respective values were WTHD = 1.52% and

Fig. 4.14. Waveforms obtained with EAI inverter when in (a) voltage-buck and (b) voltage-boost modes (c) spectrum of boosted line current i_a .

Fig. 4.15. Waveforms measured within impedance network of *EAI* inverter when in voltage-boost mode.

THD = 3.4% with the former more appropriate for measuring switched waveforms and the latter more suitable for filtered waveforms [108]. Being the current flowing directly into the load, waveform quality of the output current must be assessed with more details. Its spectrum up to the first integer multiple of its switching frequency was therefore plotted and shown in Fig. 4.14(c). Indeed, the intensity of each low-order harmonic observed was reasonably low.

Fig. 4.16. Waveforms measured within impedance network of *EBI* inverter when in voltage-boost mode.

4.5.2. Type EB Inverters

Switched waveforms of the *EB* inverters are not explicitly shown here since they are the same as those of the *EAI* inverter shown in Fig. 4.14. Their magnitudes are however higher when the same turns ratio and control parameters listed in Table. 4.3 are used. Their values are summarized here as $V_{C1} = 188 \text{ V}$, $V_{C2} = 88 \text{ V}$, $\hat{v}_i = 217 \text{ V}$, $\hat{v}_{ac} = 99.8 \text{ V}$ and $\hat{i}_{ac} = 2.61 \text{ A}$. Differences can however be observed from those waveforms measured within their impedance network. They are therefore shown in Fig. 4.16 for the *EBI* inverter, where the same smooth input current can be seen. Winding current through *W1* is also noted to be high, which undeniably is in agreement with the earlier presented analysis.

Fig. 4.17. Waveforms measured within impedance network of *EC1* inverter when in voltage-boost mode.

4.5.3. Type EC Inverters

The setup was finally rearranged to give the *EC1* inverter shown in Fig. 4.7(a). Its switched waveforms are not shown here since they are similar to those of the *EA1*

Fig. 4.18. Experiment prototype.

inverter shown in Fig. 4.4. Its boosted amplitudes are however different, whose values are given as follows: $V_{C1} = 130$ V, $V_{C2} = 31$ V, $\hat{v}_i = 151$ V, $\hat{v}_{ac} = 69$ V and $\hat{i}_{ac} = 1.82$ A. To demonstrate its other differences, Fig. 4.17 shows waveforms measured at its impedance network, which again show a smooth input current and smaller instantaneous current through the transformer *WI* winding. The experimental prototype is shown in Fig. 4.18.

4.6. Summary

This chapter presents six asymmetrical transformer-based EZ-source inverters organized into three different types. They differ mainly with their turns ratio requirements depending on where their transformers are placed. For that, the *EB* inverters demonstrate a unique trend whereby their turns ratio has to be lowered to raise their inverter gain. Placing the windings differently also leads to different instantaneous peak currents flowing through them with the *EB* inverters enduring high stress in both their windings as compared to only one for the *EA* and *EC* inverters. Other than these, they produce the same high voltage boost with the same improved waveform quality and lower switch stress achieved. They also draw a continuous input current from the source without demanding for an external filter. Each inverter therefore has a few common advantages, as well as a few distinct features of its own that might suit certain applications. Experimental testing has already been performed with results discussed in the chapter.

Chapter 5 Transformer-Based Impedance-Source NPC Inverters with Enhanced Voltage Boost Capability

Motivated by the significant advantages that NPC inverter and trans-Z-source inverter can offer, this chapter proposes a series of transformer-based impedance-source NPC inverters, which use two cascaded transformer-based impedance-source networks for voltage boosting. Comparing with traditional Z-source NPC inverter, the proposed NPC inverters have an enhanced voltage boost, and less number of passive components. They are hence better choices than the former. The proposed inverters are therefore expected to be of interest to medium voltage high power motor drives, fuel cell power conversion systems, and renewable energy applications such as PV and wind turbines equipped with the appropriate rectification.

Among the proposed impedance-source NPC inverters, trans-Z-source NPC inverter with two transformer-based impedance-source (trans-Z) networks has the advantages of trans-Z-source inverter and NPC inverter. By using two cascaded impedance-source networks with magnetically coupled circuits embedded, it enhances the voltage boost capability and reduces the number of passive components over the traditional Z-source inverter. Trans-Z-source NPC inverter with single trans-impedance network further reduces the passive component count, while maintaining the voltage-boost capability to be the same as the traditional Z-source NPC inverters presented in Chapter 3.

Γ -source NPC inverters are also proposed, which produce the same voltage boost as the trans-Z-source NPC inverter with two cascaded trans-Z source networks. The Γ -source NPC inverter however uses a smaller transformer turns ratio at high gain, which better helps with ensuring good coupling. The series of asymmetrical transformer-based embedded Z-source NPC inverters integrate the advantage of asymmetrical transformer-based embedded Z-source inverters and the classical NPC configuration to obtain enhanced voltage boost capability by differently configuring the magnetically coupled circuits dot orientations. The unique feature of serially

connecting the dc source with the impedance-source network inductor helps to eliminate the input filters which are essential for other trans-impedance source NPC inverters. Furthermore, it also prevents the inverters from being harmed by the chopping input current, and hence it is more reliable than the other topologies.

Fig. 5.1. Trans-Z-source NPC inverters with source in series with (a) diode or (b) inverter bridge (also called trans-quasi-Z-source NPC inverter).

5.1. Trans-Z-Source NPC Inverter with Two Cascaded Impedance-Source Network

Motivated by the promising advantages that trans-Z-source inverters and NPC inverters can offer as presented in Chapter 2 and Chapter 3, this section illustrates two trans-Z-source NPC inverters, which use cascaded trans-Z-source networks to achieve voltage boost function. Comparing with traditional Z-source NPC inverter, the two proposed inverters have enhanced the voltage boost capability and reduced passive component counts. With properly designed PWM scheme, the proposed inverters can produce the correct volt-sec average and inductive voltage boosting without adding extra switching commutations. The theories and simulation/experimental verification are stated in the following subsections.

5.1.1. Configurations

Similarly as configuring traditional Z-source NPC inverter with two cascaded impedance-source networks with two floating ground isolated dc sources, the circuit configurations of trans-Z-source NPC inverters can be formed by cascading two trans-Z-source/trans-quasi-Z-source networks together, and connecting it to a classic NPC inverter, as shown in Fig. 5.1. The two cascaded transformer-based Z-source networks are named upper network and lower network as depicted in the shaded area. Respectively, $W1_{up}/W1_{dn}$ and $W2_{up}/W2_{dn}$ are the primary and secondary winding of the transformer located at upper/lower network. In order to obtain a balanced voltage provided by upper and lower side impedance network, winding $W1_{up}$ and $W1_{dn}$ are connected to the two terminals of the dc-rail. And for the same reason, the turns ratios of the two network transformers are set to be the same with $W1_{up} : W2_{up} = W1_{dn} : W2_{dn} = 1 : n_{IZ}$. Furthermore, identical dc voltage sources and same shoot-through duty ratio are used for both of the upper and lower networks.

5.1.2. Operational Principle

Same as two-level trans-Z-source inverters, the proposed three-level trans-Z-source

NPC inverters can also operate in both buck and boost operation modes. Modulation strategy of trans-Z-source inverters is the same as that of traditional Z-source NPC inverters as described in Section 3.3, which could be either modified PDPWM scheme or modified APODPWM scheme. Therefore, during buck operation when no shoot-through states added, the amount of buck gain will be adjusted by the modulation index M of the sinusoidal reference signals. Setting dc source voltages V_{dc} and modulation index M , the peak output AC output voltage $\hat{v}_{ac}$ can be calculated as:

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (5.1)$$

While under the boost operation mode, there is a need to insert additional shoot-through switching states for the two cascaded trans-Z-source networks. According to (2.13), inserting same shoot-through duty ratio d to upper and lower networks, the capacitor voltage V_{Cup}/V_{Cdn} , peak dc-link voltage $\hat{v}_{iup}/\hat{v}_{idn}$ and peak ac output voltage $\hat{v}_{ac}$ during boost operation can be expressed in terms of V_{dc} .

$$V_{Cup} = V_{Cdn} = V_C = \begin{cases} \frac{1-d}{1-(n_{tZ}+1)d} \frac{V_{dc}}{2}, & \text{configure Fig. 5.1(a)} \\ \frac{n_{tZ}d}{1-(n_{tZ}+1)d} V_{dc}, & \text{configure Fig. 5.1 (b)} \end{cases}$$

$$\hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i = \frac{1}{1-(n_{tZ}+1)d} \frac{V_{dc}}{2}$$

$$\hat{v}_{ac} = \frac{M}{1-(n_{tZ}+1)d} \frac{V_{dc}}{2} \quad (5.2)$$

Table. 5.1. Testing parameters of simulation and experiment.

Parameters	Value
Upper and lower DC source voltage $V_{dc}/2$	50 V
Fundamental ac frequency f	50 Hz
Switching frequency f_s	10 kHz
Capacitor capacitance $C1=C2$	470 μ F
RL load R	40 Ω
RL load filter L	10 mH
Modulation index M	0.8*1.15=0.92
Shoot-through ratio (for boost operation only) d	0.175
Transformer winding turns ratio n_{tZ}	2

5.1.3. Simulation and Experimental Results

Fig. 5.2. Simulation results of trans-Z-source NPC inverter dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{ab} , phase voltage v_{aN} and load currents (i_a, i_b, i_c) with (a) buck operation $M=0.92, d=0$ and (b) boost operation $M=0.92, d=0.175$ (10 ms/div).

Fig. 5.3. Simulation results of trans-Z-source NPC inverter (a) dc-link voltage v_{iup}/v_{idn} , transformer winding voltage v_{W1up}/v_{W1dn} and v_{W2up}/v_{W2dn} , diode voltage v_{D1}/v_{D2} , capacitor voltage V_{Cup}/V_{Cdn} and (b) capacitor current i_{Cup}/i_{Cdn} , transformer winding current i_{W1up}/i_{W1dn} , i_{W2up}/i_{W2dn} during boost operation (100 μs/div).

The proposed inverters have been verified by both Matlab/PSIM toolbox simulation and laboratory experiment. The experimental prototype gating signals were generated by a field programmable gate array (FPGA) from *Xilinx*. The simulation and experimental operation condition and system parameters are listed in Table. 5.1. The system components such as the capacitor and coupled inductors can be designed according to [82], which selects the components according to shoot-through duty ratio, voltage and current ratings, to make sure that the designed circuits will be able to operate under continuous conduction mode [34]. The capacitors used in this experiment are PEH200ZH3470MU2 with 500V voltage rating, which is selected based on the design of [82] and laboratory availability.

The simulation results under buck and boost operation modes are depicted in Fig. 5.2. During buck operation as shown in Fig. 5.2(a), Z-source NPC inverter acts same as classical NPC inverter, where the dc-rail voltage equals to the sum of split dc source voltages. Substituting the system parameters into (5.2), the resulting capacitor voltage and peak dc-link voltage can be evaluated to be $V_{Cup}=V_{Cdn}= 86.8$ V and $\hat{v}_{iup} = \hat{v}_{idn} = 105.2$ V for boost operation mode when shoot-through duty ratio $d=0.175$. These computed values have been verified by measured simulated results as shown in Fig. 5.2(b), where the dc-rail voltage ($v_{iup}+v_{idn}$) is chopping between 105.2 V to 210.4 V. The corresponding line voltage v_{ab} , phase voltage v_{aN} and load currents (i_a, i_b, i_c) of the trans-Z-source inverter are all shown in Fig. 5.2. The simulation results clearly show that the dc-link voltage, phase voltages as well as line voltages and line currents are all boosted with gain factor $105/50=2.1$, which is the same as calculation of trans-Z-source voltage boost gain when substituting the turns ratio 2 and shoot-through duty ratio 0.175 into (5.2).

Based on the trans-Z-source NPC modulation scheme and operational principle, the upper and lower network components have the same voltage/current pulses, only different in phase. The zoom in view simulation results of upper/lower network dc-link voltage v_{iup}/v_{idn} , transformer winding voltages v_{W1up}/v_{W1dn} , v_{W2up}/v_{W2dn} as well as capacitor voltages V_{Cup}/V_{Cdn} and diode voltage v_{D1}/v_{D2} , capacitor current i_{Cup}/i_{Cdn} , transformer winding current i_{W1up}/i_{W1dn} and i_{W2up}/i_{W2dn} are shown in Fig. 5.3(a) and (b) correspondingly.

The simulation results of trans-quasi-Z-source NPC inverters are shown in Fig. 5.4 and Fig. 5.5 respectively. Most of the voltage and current amplitudes of the network components are the same as those of trans-Z-source NPC inverter except the capacitor voltage V_{Cup}/V_{Cdn} , as expected from (5.2). Another difference is the source current i_{dc} , which equals to i_{W2up}/i_{W2dn} for trans-Z-source NPC inverter and i_{W1up}/i_{W1dn} for trans-quasi-Z-source NPC inverter.

The experimental results of buck operation mode with no shoot-through states added and boost operation mode with shoot-through states added are shown in Fig. 5.6-Fig. 5.7.

The experimental results of buck operation are shown in Fig. 5.6(a), where the upper/lower band dc-link voltage v_{iup}/v_{idn} equals to source voltage 50V. And the resulted dc-rail voltage now would be 100V, which is the sum of the two dc source voltages. It drives +50V, 0 and -50V three-level phase voltage and $\pm 100V$, $\pm 50V$ and 0 five-level line voltage as shown in Fig. 5.6(a). The amplitude of load current measured is 2.2A peak-peak. The experiment results of boosted mode operation with shoot-through duty ratio $d=0.175$ is shown in Fig. 5.6(b). The upper/lower network dc-link voltages v_{iup}/v_{idn} now has been boosted to 99.2V, which is slightly less than the simulation value due to the power loss of the passive components and switching devices. The load current of boost operation measured is 4.45A peak-peak. The boosted voltage gain factor then can be evaluated to be $99.2/50=1.98$, which is slightly less than theoretical value 2.1 as computed before. The zoom-in view of trans-Z-source upper network dc-link voltage v_{iup} , winding voltage v_{W1up} , v_{W2up} , diode voltage v_{D1} , capacitor voltage V_{Cup} , capacitor current i_{Cup} , winding currents i_{W1up} and i_{W2up} during voltage-boost mode are shown in Fig. 5.7. The lower network voltages and currents are similar, only have phase difference. The shoot-through states are clearly shown by dc-link voltage when it becomes to nearly zero, not exactly zero because of the forward voltages of IGBTs and diode forward voltage. The capacitor voltages are boosted to 85V, which are also very close to the theoretical simulation value.

Fig. 5.4. Simulation results of trans-quasi-Z-source dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{ab} , phase voltage v_{aN} and load currents (i_a, i_b, i_c) with (a) buck operation $M=0.92, d=0$ and (b) boost operation $M=0.92, d=0.175$ (10 ms/div).

Fig. 5.5. Simulation results of trans-quasi-Z-source NPC inverter (a) dc-link voltage v_{iup}/v_{idn} , transformer winding voltage v_{W1up}/v_{W1dn} and v_{W2up}/v_{W2dn} , diode voltage v_{D1}/v_{D2} , capacitor voltage V_{Cup}/V_{Cdn} and (b) capacitor current i_{Cup}/i_{Cdn} , transformer winding current i_{W1up}/i_{W1dn} and i_{W2up}/i_{W2dn} during boost operation (100 μs/div).

Fig. 5.6. Experimental waveforms of trans-Z-source NPC inverter dc-rail voltage $v_{iup}+v_{idn}$, output line voltage v_{ab} , output phase voltage v_{aN} and output current i_a , with (a) buck operation $M=0.92$, $d=0$ and (b) boost operation $M=0.92$, $d=0.175$.

(a)

(b)

Fig. 5.7. Experimental waveforms of trans-Z-source NPC inverter upper network (a) dc-link voltage v_{iup} , winding voltage v_{W1up} , v_{W2up} , diode voltage v_{D1} , capacitor voltage V_{Cup} and (b) capacitor current i_{Cup} , winding currents i_{W1up} and i_{W2up} during voltage-boost mode with $M=0.92$, $d=0.175$.

5.2. Trans-Z-Source NPC Inverter with Single Impedance-Source Network

This section presents a transformer based Z-source NPC inverter with single impedance-source network. Comparing with Z-source NPC inverter with single LC network as described in Section 3.2, the proposed inverter effectively reduces passive components count while retaining the boost gain. By utilizing modified APODPWM scheme, the proposed topology has been verified by both simulation and experiment.

5.2.1. Configuration

The configuration of proposed magnetically coupled-inductor based Z-source NPC inverter is shown in Fig. 5.8, where neutral point 'N' is connected to the middle point of the split dc sources. Two diodes D1 and D2 are used to block reverse currents from inverter side. The impedance-source network contains one couple inductor and one capacitor as shown in the shaded area. The two windings of the coupled-inductor are wired on the same magnetic core. Thus the coupled-inductor size is almost the same as single winding inductor. Furthermore, the proposed Z-source NPC inverter reduces

Fig. 5.8. Trans-Z-source NPC inverters with single impedance-source network.

one capacitor from the traditional Z-source NPC inverter with single LC network as shown in Fig. 3.2, which further reduced the inverter size and system components.

5.2.2. Operational Principle

Buck operation mode, boost operation mode as well as modulation scheme have been discussed in this section.

A. Buck Operation Mode

Under its buck operation mode, there is no shoot-through required. The proposed inverter operates the same as classical NPC inverter does. The diode D1 and D2 are always forward biased, and the coupled transformer is short-circuited in steady state. The voltage buck gain can be controlled directly by modulation index M . The ac output voltage $\hat{v}_{ac}$ during buck operation mode can be computed in (5.3).

$$\hat{v}_{ac} = M \frac{V_{dc}}{2} \quad (5.3)$$

B. Boost Operation Mode

Under its boost operation mode, shoot-through states have to be inserted into state sequences. The shoot-through states can be inserted among the 27 conventional active

Fig. 5.9. Equivalent circuit of proposed inverter impedance network during (a) shoot-through state and (b) non-shoot-through states.

and null states of three-level NPC inverter by simultaneously turning on all four switches of the same phase leg, which undoubtedly will add extra switching commutations hence increase the switching loss. To retain the conventional switching pattern, the modified PDPWM and APODPWM scheme are applied as described in Section 3.3. During shoot-through states, the diodes will be reverse blocked and dc sources will be disconnected from coupled-inductor windings. The capacitor C will charge up coupled-inductor winding W2 as shown in Fig. 5.9(a). During non-shoot-through states, the coupled-inductor will release stored energy to output ac load. The equivalent impedance-source network circuit of non-shoot-through state is shown in Fig. 5.9(b). Based on the above analysis, with turns ratio $n = W1:W2 = 1:1$, the following expressions can be derived as:

During shoot-through states:

$$\begin{aligned} V_C &= v_{W2}; v_{W1} = v_{W2} \\ -i_C &= i_{W2} = i_{ST} \end{aligned} \quad (5.4)$$

During non-shoot-through states:

$$\begin{aligned} V_C &= v_{W2} + v_i; V_{dc} = 2v_{W2} + v_i \\ i_{dc} &= i_C + i_{W2} \end{aligned} \quad (5.5)$$

By integrating the transformer winding voltages and capacitor current over one switching cycle and equalizing them to zero ($\int_0^T v_{W1} = 0$; $\int_0^T v_{W2} = 0$; $\int_0^T i_C = 0$), the average source input current $I_{dc1} = I_{dc2} = I_{dc}$, the capacitor voltage V_C , shoot-through current i_{ST} , peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated in terms of dc source voltage V_{dc} and average source input current I_{dc} .

$$\begin{aligned} V_C &= V_{dc} \frac{1-d}{1-2d}; i_{ST} = 2I_{dc} \\ \hat{v}_i &= V_{dc} \frac{1}{1-2d} \\ \hat{v}_{ac} &= \frac{V_{dc}}{2} \frac{M}{1-2d} \end{aligned} \quad (5.6)$$

Comparing with (3.4), the capacitor voltage, boosted dc-link voltage and boosted ac output voltage are the same as those of Z-source NPC inverter with single LC network.

However, the proposed magnetically coupled inductor based Z-source NPC inverter uses only one capacitor instead of two, which greatly reduces the passive power loss. While comparing with trans-Z-source NPC inverter with two impedance networks characteristics as shown in (2.13) and (5.2), the proposed single network trans-Z-source NPC inverter has the same current ratings for all the components, only the capacitor voltage rating becomes double under same input-to-output gain condition. The increased voltage rating for capacitor nevertheless will increase the size of the capacitor, which can be compensated by reducing half of the passive component count, as shown in Fig. 5.1 and Fig. 5.8.

C. Modulation Scheme

To retain the conventional switching commutations, the proposed NPC inverter can be modulated by modified APODPWM scheme. As depicted in Section 3.3, the modified APODPWM Scheme for Z-source NPC inverter is operated by the three conventional sinusoidal references and two additional references specially designed for shoot-through states. One of the additional references is used as reference of switch SX1. It located at the top and has the value $V_{(max)}+d$, where d is the shoot-through duty ratio and $V_{(max)}$ is the conventional modulation reference with maximum value. Another additional reference located at the bottom and has the value minimum reference $V_{(min)}-d$, where $V_{(min)}$ is the conventional modulation reference with minimum value. It is

Fig. 5.10. Sample shoot-through state of trans-Z-source NPC inverter with single impedance source network.

used as switching reference for switch SY2' as shown in Fig. 3.4. The rest switches keep the same switching actions as the conventional NPC inverters do. By doing so, time advance/delay will be added to switch SX1 and SY2'. During the time advance/delay overlapping, the upper three switches of phase leg X and lower three switches of phase leg Y will be ON at the same time. The diode DX2 and DY1 will be forward biased hence the inverter dc-link will be shorted. This modulation retains the switching commutations of conventional APODPWM scheme thus no additional switching states needed to insert as shoot-through states. One example is shown in Fig. 3.4, where the reference of phase leg A has maximum value V_A and reference of phase leg C has minimum value V_C during state transition $[000 \rightarrow 10-1 \rightarrow 1-1-1 \rightarrow 10-1 \rightarrow 000]$. Accordingly, $(V_A + T_0/T)$ is used as reference for switch SA1 and $(V_C - T_0/T)$ is used as reference for switch SC2'. The ON/OFF time of switch SA1 and SC2' are shifted/delayed so that SA1, SA1', SA2 and SC1', SC2, SC2' are turned ON simultaneously at the overlapping period. With diode DA2 and DC1 forward biased, the shoot-through state S is added between transition $[000 \rightarrow 10-1]$ and $[10-1 \rightarrow 000]$, as indicated in red arrows in Fig. 5.10.

5.2.3. Simulation and Experimental Results

The proposed inverter topology has been verified by both simulation and experiment. The testing parameters are shown in Table. 5.2.

Table. 5.2. Testing parameters of trans-Z-source NPC with single impedance source network.

Input voltage $V_{dc}/2$	50 V
Switching frequency	10 kHz
AC frequency	50 Hz
Couple inductor self-inductance	0.6 mH
Capacitor C	2200 μ F
RL load R	40 Ω
RL load L	5 mH
Modulation index M	0.8625
Shoot-through duty ratio d (for boost operation)	0.25

Fig. 5.11. Simulation results of 1: dc-rail voltage ($v_{iup}+v_{idn}$), 2: line voltage (v_{AB}), 3: phase voltage v_{AN} , 4: load current i_a, i_b, i_c under (a) buck operation with $M=0.8625$ and $T_0/T=0$ and (b) boost operation with $M=0.8625$ and $T_0/T=0.25$ (time: 10ms/div).

With these testing parameters, the ac output voltage for buck operation is 43.125 V according to (5.3) when $d = 0$. Under boot operation mode, substituting value of dc source voltage $V_{dc}/2=50V$, shoot-through duty ratio $d=0.25$ into (5.6), the resulting

(a)

(b)

Fig. 5.12. Simulation results of (a) zoom in view dc-rail voltage ($v_{iup}+v_{idn}$), voltages across transformer winding 1 and 2 v_{w1} , v_{w2} as well as capacitor voltage V_C and (b) dc source current i_{dc} , winding W1 current i_{w1} and i_{w2} during boost operation. (time: 0.01ms/div).

capacitor voltage V_C the peak dc-link voltage $\hat{V}_i$ and peak ac output voltage $\hat{v}_{ac}$ are estimated to be 150 V, 200 V and 86.25V respectively. Therefore, by setting shoot-through duty ratio $d=0.25$, the input-to-output voltage gain ($\hat{V}_{ac}/V_{dc}$) can be evaluated to be 1.725. The simulation results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage V_{AB} ,

phase to neutral voltage V_{AN} and line current i_a, i_b, i_c during buck and boost operation are shown in Fig. 5.11. The zoom-in view of dc-rail voltage ($v_{iup}+v_{idn}$), voltages across transformer winding 1 and 2 v_{w1}, v_{w2} and capacitor voltage V_C , as well as dc source current i_{dc1} , transformer winding current i_{w1} and i_{w2} during boost operation are shown in Fig. 5.12, which are all expected from theoretical calculations. The corresponding experimental results are shown in Fig. 5.13 and Fig. 5.14.

Fig. 5.13. Experimental results of 1: dc rail voltage ($v_{iup}+v_{idn}$), 2: line voltage ($v_{AN}-v_{BN}$), 3: phase voltage v_{AN} , 4: load current i_a under (a) buck operation with $M=0.8625$ and $d=0$ and (b) boost operation with $M=0.8625$ and $d=0.25$ (time: 5ms/div).

(a)

(b)

Fig. 5.14. Experimental results of (a) zoom in view dc-rail voltage ($v_{iup}+v_{idn}$), as well as voltages across transformer winding 1 and 2 v_{w1} , v_{w2} and capacitor voltage V_C , (b) dc source current i_{dc1} , winding W1, W2 current i_{w1} and i_{w2} during boost operation. (time: 50 μ s/div).

5.3. Γ -Source NPC Inverter

Motivated by the significant advantages of NPC inverter and Γ -source inverter, this section introduces a Γ -source NPC inverter which utilizes two cascaded Γ -source networks for buck-boost operation. Comparing with conventional impedance-source network, the Γ -source network effectively increases the voltage boost capability and reduces one capacitor at the front-end of DC-AC inverter, while maintaining voltage/current stress at the remaining system devices/components. The Γ -source network also replaces four inductors with two coupled-transformers, helps to reduce circuit inductive components count. Furthermore, under same input-to-output voltage gain operation, the coupled-transformers of Γ -source NPC inverter require less turns ratio comparing with those needed for the trans-Z-source inverters, which shows the significant advantages of Γ -source network based inverters.

5.3.1. Configuration

The circuit configuration of proposed Γ -source NPC inverter is shown in Fig. 5.15. It has two cascaded transformer-based Γ -source networks, namely the upper side network and lower side network (as illustrated in the shaded area). Respectively, $W1up/W1dn$ and $W2up/W2dn$ are the primary and secondary winding of the

Fig. 5.15. Configuration of Γ -source NPC inverter.

transformer located at upper/lower side network.

In order to obtain a balanced boosted voltage provided by upper and lower side impedance network, the turns ratios of the two transformers are set to be $W_{1up}: W_{2up} = W_{1dn}: W_{2dn} = n_\Gamma$. And also for the same reason, the identical dc sources and shoot-through duty ratio $T_\theta/T=d$ for both Z-source networks are used. Note that theoretically the transformer can also be replaced by a proper designed switched-inductor or tapped-inductor to achieve enhanced boost ability [109].

5.3.2. Operational Principle

Under buck operation, the modulation of Γ -source NPC inverter is the same as that of traditional NPC inverter, which could be conventional PDPWM scheme with two in phase triangle carriers. Therefore, the amount of buck gain can be controlled by adjusting the modulation index M of the sinusoidal reference signal. Setting upper/lower dc-link voltage to be $V_{dc}/2$, the peak AC output voltage $\hat{v}_{ac}$ can be evaluated as equation (5.7).

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (5.7)$$

Under boost operation mode, the shoot-through duty ratio d will determine the voltage boost gain. Assuming the transformer turns ratio of Γ -source impedance network n_Γ , the capacitor voltage V_C , peak dc-link voltage $\hat{v}_{iup}, \hat{v}_{idn}$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated in terms of V_{dc} and d .

$$\begin{aligned} V_{Cup} = V_{Cdn} = V_C &= \frac{1-d}{1-\left(1+\frac{1}{n_\Gamma-1}\right)d} \frac{V_{dc}}{2} \\ \hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i &= \frac{1}{1-\left(1+\frac{1}{n_\Gamma-1}\right)d} \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{M}{2} \frac{V_{dc}}{1-\left(1+\frac{1}{n_\Gamma-1}\right)d} \end{aligned} \quad (5.8)$$

5.3.3. Simulation and Experimental Results

The proposed Γ -source NPC inverter has been verified by Matlab/PSIM toolbox simulation. The operation condition and system parameters are shown in Table. 5.3.

Substituting the system parameter values (5.8), the resulting capacitor voltage V_C and dc-link voltage $\hat{v}_i$ is estimated to be 86.8 V and 105.2 V respectively. Fig. 5.16 shows the simulation results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and load currents i_a, i_b, i_c of the designed configuration.

Comparing the buck operation with the boost operation, the simulation results clearly shows that both the line voltage and phase voltage are boosted with gain factor $102/50=2.04$, which is the same as calculated (5.8). And hence the load currents are also booted to the same gain ratio, only a little loss due to the transformer resistance and capacitor series resistance.

The simulation results of dc-link voltages v_{iup} , capacitor voltages V_{C1} as well as transformer winding voltages v_{W1}, v_{W2} are shown in Fig. 5.17.

The lower network components voltages are with same amplitude as those of the upper network components, only with phase differences.

Table. 5.3. Testing parameters of Γ -source NPC inverter.

Parameters	Value
Upper and lower DC source voltage $V_{dc}/2$	50 V
Capacitor capacitance $C1=C2$	1000 μ F
Load resistance R (Simulation)	25 Ω
Load resistance R (Experiment)	48 Ω
Modulation index M	$0.8*1.15=0.92$
Shoot-through ratio (for boost operation only) d	0.175
Transformer winding turns ratio n	1.5
Switching frequency f_s	10 kHz

Fig. 5.16. Simulation results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and load currents i_a, i_b, i_c during (a) buck operation $M=0.92$, $T_0/T=0$ and (b) boost operation $M=0.92$, $T_0/T=0.175$ (time: 20 ms/div).

As depicted in Fig. 5.17, the voltage between the upper/lower dc-link to neutral point V_{iup}/V_{idn} has been boosted to 103.6V under boost operation mode when 0.175 shoot-through duty ratio is inserted. The voltage of the two capacitors is boosted to 85.4V, which is a little smaller than theoretical value due to the internal resistances of transformers and capacitors for practical situation consideration. The passive components from upper and lower Γ -source networks have identical voltages only with phase differences. Therefore, the upper/lower transformer winding 1 voltage

Fig. 5.17. Simulation results of DC-link voltage, capacitor voltage as well as voltages across transformer winding 1 and 2 during boost operation.

v_{W1up}/v_{W1dn} is represented by v_{W1} from here onwards. Similar simplified representation would refer to winding 2 voltage and capacitor voltage.

As analyzed in Section 2.5, during shoot-through states, the voltage v_{W1} is the sum of voltage v_{W2} and capacitor voltage V_C . It gives v_{W1} 253.1V and v_{W2} 168.7V according to voltage ratio v_{W1}/v_{W2} equals to transformer turns ratio 1.5. During non-shoot-through states, the winding 2 voltage v_{W2} equals to the voltage of dc source subtracts the capacitor voltage V_C , which gives v_{W2} -34.4. And the winding 1 voltage v_{W1} would equal to 1.5 times of v_{W2} which is -51.6V. The dc-link voltage v_{iup}/v_{idn} would be dc source voltage $V_{dc}/2$ minus v_{W1} , which gives 103.6V. And it is the same value as measured previously. Hence it verifies the validation of the theories of the proposed inverter.

The gating signals of experimental prototype were generated by a field programmable gate array (FPGA) from *Xilinx*. Modulation index and shoot-through duty ratio during buck and boost operation mode were the same as those of simulation settings.

Fig. 5.18. Experimental results of 1: dc-rail voltage ($v_{iup}+v_{idn}$) and 2: line voltage ($v_{AN}-v_{BN}$), 3: phase voltage v_{AN} , 4: load current i_a when (a) buck operation with $M=0.92$ and $T_0/T=0$ and (b) boost operation with $M=0.92$ and $T_0/T=0.175$ (time: 10ms/div).

Switching frequency was set to be 10 kHz and load resistor coupled transformers were wound on Magnetics C055906A2 MPP high frequency core with permeability 125. To make transformer turns ratio $n_T=1.5$, the primary winding has 87 turns and secondary winding has 58 turns. The experimental results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase voltage v_{AN} and load current i_a during buck and boost operation modes are shown in Fig. 5.18, where the peak dc-rail voltage, line voltage and phase voltage have been boosted 2.04 times with shoot-through duty ratio $d=0.175$. Zoom in view of dc source voltage, dc-link voltage, transformer primary winding voltage, secondary voltage and capacitor voltage during boost operation are shown in Fig. 5.19.

Fig. 5.19. Zoom in view of upper Γ -source network experimental results 1: dc source voltage $V_{dc}/2$, 2: dc-link voltage v_{iup} , 3: voltages across transformer winding 1 v_{w1up} , 4: voltages across transformer winding 2 v_{w2up} , 5: capacitor voltage V_{Cup} . (time: 100 μ s/div)

5.4. Summary

This chapter presents three types of transformer-based impedance-source NPC inverters. The first two types use trans-Z-source networks to boost up the dc voltage and the third one uses Γ -source network. The three types of NPC inverter have enhanced voltage boost capability and less components comparing with traditional Z-source NPC inverter. Same as two-level version, the trans-Z-source NPC inverter with two cascaded impedance-source networks will have enhanced voltage boost capability when the transformers turns ratio $n > 1$, and $1 < n < 2$ for Γ -source NPC inverter. Despite the enhanced voltage capability, the proposed NPC inverters are also suffering from chopping input current, which leads to the development of continuous input current impedance-source NPC inverters, as described in next chapter.

Chapter 6 Transformer-Based Impedance-Source NPC Inverters with Continuous Input Current

As analysed in Chapter 5, all the trans-Z-source NPC inverters and Γ -source NPC inverter have enhanced voltage boost capability over traditional Z-source NPC inverters, thanks to the magnetically coupled circuits. They effectively suppress the system voltage stress by utilizing low shoot-through duty ratio and high modulation depth. However, despite the enhanced voltage boost capability, all the three transformer-based impedance-source inverters suffer from discontinuous chopping input current, which is harmful to input dc source. Therefore low pass filters like simple LC filters are usually needed for practical applications as described in Section 2.4. Aiming to solve this problem, this section presents one LCCT NPC inverter and six asymmetrical transformer-based embedded Z-source inverters with continuous input current and enhanced voltage boost capability. Simulation and experimental results are also illustrated to verify the theoretical validation.

6.1. LCCT NPC Inverter with Continuous Input Current

The configuration, operational principle, simulation and experimental results obtained

Fig. 6.1. Configuration of LCCT NPC inverter.

are described in this section.

6.1.1. Configuration

The configuration of LCCT Z-source network based buck-boost DC-AC NPC inverter is shown in Fig. 6.1. It contains the cascaded LCCT Z-source networks with two floating ground isolated dc sources as in the shaded area and the basic NPC inverter as on the right side. Each LCCT Z-source network from upper/lower side has one input inductor $L1/L2$, one diode $D1/D2$, two capacitors $C1up/C1dn$, $C2up/C2dn$ and one coupled inductor. The components of upper and lower side network are the same and configured in a flipped manner to make the boosted dc-link voltages v_{iup} and v_{idn} are balanced. The turns ratios of the transformers are set to be $W1up : W2up = W1dn : W2dn = n_L : 1$. Note that theoretically the transformer can also be replaced with a proper designed switched-inductor or tapped-inductor in order to achieve more enhanced voltage boost ability as analysed in Section 2.6.

6.1.2. Operational Principle

Same as the conventional Z-source NPC inverter, the proposed LCCT Z-source NPC inverter can operate in both buck and boost operation modes.

As presented in Section 3.3, in case of buck operation, the inverter modulation is the same as that of the conventional three-level NPC inverter. It can be either Phase Disposition Pulse Width Modulation (PDPWM) or Alternative Phase Opposition Disposition Pulse Width Modulation (APODPWM) with upper and lower triangle carriers in phase or 180° phase shifted respectively. Generally, the PDPWM is preferred for three-level inverters as it always ensures that the nearest three vectors are used and therefore has better output performance [110]. The amount of AC output voltage can be controlled by the modulation index M . Setting dc source voltages for upper/ lower networks to be $V_{dc}/2$, the AC output peak voltage $\hat{v}_{ac}$ can be calculated as:

$$\hat{v}_{ac} = \frac{M}{2} V_{dc} \quad (6.1)$$

Under boost operation mode, the shoot-through states are inserted among conventional active and null switching sequence for storing energy into the coupled inductors. By analyzing the LCCT impedance-source networks as shown in Fig. 6.1, assuming the transformer turns ratio is n_L , the capacitor voltage V_C , peak dc-link voltage $\hat{v}_{iup}$, $\hat{v}_{idn}$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated as in (6.2).

$$\begin{aligned} V_{C1up} = V_{C1dn} = V_{C1} &= \frac{1-d}{1-(n_L+1)d} \frac{V_{dc}}{2}; V_{C2up} = V_{C2dn} = V_{C2} = \frac{n_L d}{1-(n_L+1)d} \frac{V_{dc}}{2} \\ \hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i &= \frac{1}{1-(n_L+1)d} \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{M}{2} \frac{V_{dc}}{1-(n_L+1)d} \end{aligned} \quad (6.2)$$

6.1.3. Simulation and Experimental Results

The proposed inverter has been tested by both Matlab simulation and laboratory prototype. The dc source voltage $V_{dc}/2$ and the modulation index M are set to be 50 V and 0.92 respectively. The switching frequency $f_s=10$ kHz, capacitor $C1up=C2up=C1dn=C2dn=470$ μ F, transformer turns ratio $n_L=2$, three-phase Y connected RL load has $R=39$ Ω and $L=5$ mH.

During boost operation, the shoot-through duty ratio d is set to be 0.175 for each of the LCCT impedance-source network banks. Fig. 6.2 shows the simulation results of the dc-rail voltage ($v_{iup}+v_{idn}$), line voltage V_{AB} , phase voltage V_{AN} and load currents i_a , i_b , i_c of the designed inverter configuration. It clearly shows that both the line voltage and phase voltage are boosted with gain factor $105/50=2.1$, which is close to the theoretical value $\frac{\hat{v}_{ac}}{v_{dc}}$ when substituting the turns ratio $n_L=2$ and shoot-through duty ratio $d=0.175$ into (6.2). The load currents hence also have been boosted with the same gain, only a little smaller due to the parasitic resistance of the transformers and capacitors. The simulation and theoretical calculation difference is expected to be larger if the power loss of the switching devices is also considered. The capacitor voltage V_{C1} , V_{C2} and peak dc-link voltage $\hat{v}_i$ are calculated to be =86.8 V, =36.8 V and 105.3 V respectively according to (6.2). Simulation results of transformer and diode voltage are shown in Fig. 6.3. Both of them are coordinated well with the theoretical analysis. The corresponding experimental results are shown in Fig. 6.4 and Fig. 6.5. In

the figures, it should be noted that the inverter input current still has ripples caused by switching nature between shoot-through and non-shoot-through states. These ripples are however continuous and hence less damaging than the chopping input current expected with a conventional Z-source inverter.

Fig. 6.2. Simulation results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and load currents i_a, i_b, i_c during (a) buck operation $M=0.92$, $d=0$ and (b) boost operation $M=0.92$, $d=0.175$ (time: 10 ms/div).

Fig. 6.3. Simulation results of zoom in view of (a) dc-link voltage, transformer winding 1 and 2 voltage, and diode voltage as well as (b) input current, capacitor voltages and inductor voltages during boost operation $M=0.92$, $d=0.175$ (time: 100 $\mu\text{s}/\text{div}$).

(a)

(b)

Fig. 6.4. Experimental results of 1: dc-rail voltage ($v_{iup}+v_{idn}$), 2: line voltage ($v_{AN}-v_{BN}$); 3: phase voltage v_{AN} , 4: load current i_a when (a) buck operation with $M=0.92$ and $d=0$ and (b) boost operation with $M=0.92$ and $d=0.175$ (time: 5ms/div).

Fig. 6.5. Experimental results of zoom in view of (a) dc-link voltage v_{iup} , transformer winding 1 and 2 voltage v_{W1up} , v_{W2up} , and diode voltage v_{DI} as well as (b) input current i_{L1} , capacitor voltages V_{C1up} , V_{C2up} and inductor voltages v_{L1} during boost operation $M=0.92$, $d=0.175$ (time: $50 \mu\text{s}/\text{div}$).

6.2. Asymmetrical Transformer-Based Embedded Z-source Type EA NPC Inverter

The first category of asymmetrical transformer-based embedded Z-source NPC inverters are the type *EA1* and *EA2* NPC inverters as shown in Fig. 6.6.

6.2.1. Configurations

The two EA NPC inverters make use of two cascaded type EA asymmetrical transformer-based embedded Z-source networks as shown in Fig. 4.1, which contains one magnetically coupled inductor with two windings $W1$ and $W2$, one input inductor L , one diode D and two capacitors $C1$ and $C2$. To make boost stage even, the lower network has flipped configuration as that of upper/two-level version network. Therefore, the lower network input inductor $L2$ together with the series connected dc source are placed near to the neutral point while coupled transformer is put at the bottom. The transformer dot orientation of the lower network is configured in the way

(a)

(b)

Fig. 6.6. Asymmetrical transformer-based embedded Z-source NPC inverters. Types (a) EA1 (b) EA2.

that retains the two level EA inverter operation principles for both shoot-through and non-shoot-through states. Following the analysis of Section 4.1, according to equation (4.3), both the upper and lower networks capacitors voltage can be boosted to the same level to make $V_{C1up}=V_{C1dn}=V_{C1}$, $V_{C2up}=V_{C2dn}=V_{C2}$. Consequentially, both the dc-link voltages of the upper and lower network will also be boosted to the same level $\hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i$.

6.2.2. Operational Principle

To make the input/output voltage level same to that of two-level version, the dc source voltage of each impedance-source network is set to be $V_{dc}/2$. Being modulated by modified PDPWM or modified APODPWM scheme as described in Section 3.3, the upper and lower impedance network of type EA NPC inverters will operate identically to the two-level asymmetrical transformer-based embedded Z-source type EA inverters. Under buck operation mode, with modulation ratio M , the EA NPC inverters operate same as classical NPC inverter. And the peak ac output voltage $\hat{v}_{ac}$ can be evaluated as:

$$\hat{v}_{ac} = M \frac{V_{dc}}{2} \quad (6.3)$$

Under boost operation mode, shoot-through states are added. Assuming the average source input current I_{dc} , shoot-through duty ratio d and transformer turns ratio n_{EA} , the capacitor voltage V_C , shoot-through current $\hat{i}_{ST}$, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated as:

$$\begin{aligned} V_{C1} &= \frac{1-d}{1-(2+n_{EA})d} \frac{V_{dc}}{2}; V_{C2} = \frac{d(1+n_{EA})}{1-(2+n_{EA})d} \frac{V_{dc}}{2} \\ \hat{i}_{ST} &= (2 + n_{EA})I_{dc} \\ \hat{v}_i &= \frac{1}{1-(2+n_{EA})d} \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{V_{dc}}{2} \frac{M}{1-(2+n_{EA})d} \end{aligned} \quad (6.4)$$

Comparing (6.4) and (5.2), with the same shoot-through duty ratio and transformer turns ratio, the voltage boost gain of type EA inverter will always be higher than the traditional trans-Z-source inverter as analyzed in Section 4.1. Continuous input

current is achieved by serially connecting inductor and dc source. The only trade-off would be the shoot-through current, which also determines the current stress of the transformer winding and switching devices.

6.3. Asymmetrical Transformer-Based Embedded Z-source Type EB NPC Inverters

(a)

(b)

Fig. 6.7. Asymmetrical transformer-based embedded Z-source NPC inverters. Types (a) EB1 (b) EB2.

Type EB NPC inverters are configured based on the cascaded asymmetrical transformer-based embedded Z-source type EB inverters described in Section 4.2.

6.3.1. Configurations

The configurations of type EB NPC inverters are shown in Fig. 6.7. The upper impedance-source network is the same as the two-level version. Its coupled inductor winding W2up is connected to the inverter bridge as shown in Fig. 4.4. The lower impedance-source network flips the configuration of upper one in order to keep the symmetry of the NPC inverter boost stage to maintain the shoot-through/non-shoot-through operation principle. Therefore, the capacitors voltages of the upper and lower impedance-source network can obtain same boosted voltage level, such that $V_{C1up}=V_{C1dn}=V_{C1}$, $V_{C2up}=V_{C2dn}=V_{C2}$. Consequentially, the dc-link voltages of the upper and lower network will also be boosted to the same level with $\hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i$.

6.3.2. Operational Principle

The operational principle of type EB inverters is similar as that of type EA inverters.

Under buck operation mode, no shoot-through is added. Diode D1 and D2 always keep forward-biased. The input inductor L1, L2, transformer winding W1up, W1dn and W2up, W2dn become short circuited and the capacitors C1up, C1dn become parallel connected to dc source. With split dc source voltage $V_{dc}/2$, the dc-link voltage will be the same as the dc source voltage. Therefore, the peak ac output voltage $\hat{v}_{ac}$ during buck operation can be expressed as:

$$\hat{v}_{ac} = M \frac{V_{dc}}{2} \quad (6.5)$$

When boosted dc-link voltage is required, shoot-through states are inserted among conventional active and null states, and purely occupy in null states to retain the inverter correct volt-sec average. During shoot-through states, upper/lower inverter bridge to neutral point N is shorted. The diode D1 and D2 are triggered to be reverse biased by high voltage capacitors. The four coupled inductor windings are charged up

by capacitors. During non-shoot-through states, diode D1 and D2 become forward biased. The energy stored in transformer windings now is released to ac load. As the operational principle is same as that of two-level version as shown in Section 4.2, assuming the transformer turns ratio n_{EB} , the capacitor voltage V_{C1}/V_{C2} , shoot-through current $\hat{i}_{ST}$, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated as:

$$\begin{aligned} V_{C1} &= \frac{1-d}{1-(2+1/(n_{EB}-1))d} \frac{V_{dc}}{2}; V_{C2} = \frac{n_{EB}d/(n_{EB}-1)}{1-(2+1/(n_{EB}-1))d} \frac{V_{dc}}{2} \\ \hat{i}_{ST} &= \left(2 + \frac{1}{n_{EB}-1}\right) I_{dc} \\ \hat{v}_i &= \frac{1}{1-(2+1/(n_{EB}-1))d} \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{V_{dc}}{2} \frac{M}{1-(2+1/(n_{EB}-1))d} \end{aligned} \quad (6.6)$$

Comparing equation (5.6) and equation (6.6), after equalizing the transformer turns ratio $n_I=n_{EB}=n$, the boosted dc-link voltage of Γ -source NPC inverter becomes $\frac{1}{1-(1+1/(n-1))d} \frac{V_{dc}}{2}$ while boosted dc-link voltage of type EB NPC inverters become $\frac{1}{1-(2+1/(n-1))d} \frac{V_{dc}}{2}$. The denominator of type EB boosted dc-link voltage is less than d , which indicates that the proposed type EB NPC inverters have enhanced voltage boost capability over Γ -source NPC inverter with same transformer turns ratio. And furthermore, the presented inductor L1 and L2 which are serially connected to dc-sources, help to smooth the source input currents, prevent the source from harming by discontinuous chopping input current.

6.4. Asymmetrical Transformer-Based Embedded Z-source Type EC NPC Inverters

Similar to the type EB NPC inverters, type EC NPC inverters are constructed based on the cascaded impedance-source networks of type EC asymmetrical transformer-based embedded Z-source inverters introduced in Section 4.3.

6.4.1. Configurations

The circuit configurations of type EC NPC inverters are shown in Fig. 6.8, where the upper network is the same the two-level version. The lower impedance-source network has flipped the upper network configuration to keep the boosted NPC circuits symmetrical, and retain the same capacitors and dc-link voltage boosted voltage level such that $V_{C1up}=V_{C1dn}=V_{C1}$, $V_{C2up}=V_{C2dn}=V_{C2}$, $\hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i$.

(a)

(b)

Fig. 6.8. Asymmetrical transformer-based embedded Z-source NPC inverters. Types (a) EC1 (b) EC2.

6.4.2. Operational Principle

The operational principle is similar as that of type EB NPC inverters. Under buck operation mode, the type EC NPC inverters can be modulated by conventional PDPWM or APODPWM scheme without inserting any additional shoot-through states. After the system running into steady state, the transformer windings become short circuited. The diode D1 and D2 always keep forward biased. The capacitor C1up and C1dn are connected dc source in parallel. In this case, the dc source, capacitor C1up/C1dn and inverter dc-link have the same voltage value V_{dc} , the peak ac output voltage $\hat{v}_{ac}$ during buck operation can be expressed as:

$$\hat{v}_{ac} = M \frac{V_{dc}}{2} \quad (6.7)$$

Under boost operation mode, shoot-through states are inserted among conventional three-level inverter active and null states by modified PDPWM or APODPWM scheme, as described in Section 3.3. During shoot-through states, the inverter bridge is shorted. The transformer windings are charged up by capacitors. The diode D1 and D2 are forced to be reverse biased. During non-shoot-through states, the diode D1 and D2 become forward biased. The energy stored in transformer windings now is released to ac load. By performing state-space average on the transformer winding voltages and capacitor currents, setting transformer turns ratio n_{EC} , the capacitor voltage V_{C1} and V_{C2} , shoot-through current $\hat{i}_{ST}$, peak dc-link voltage $\hat{v}_i$ and peak ac output voltage $\hat{v}_{ac}$ can be calculated as:

$$\begin{aligned} V_{C1} &= \frac{1-d}{1-(1+n_{EC})d} V_{dc}, V_{C2} = \frac{n_{EC}d}{1-(1+n_{EC})d} V_{dc} \\ \hat{i}_{ST} &= (1 + n_{EC})I_{dc} \\ \hat{v}_i &= \frac{1}{1-(1+n_{EC})d} \frac{V_{dc}}{2} \\ \hat{v}_{ac} &= \frac{V_{dc}}{2} \frac{M}{1-(1+n_{EC})d} \end{aligned} \quad (6.8)$$

The boosted dc-link voltage of type EC NPC inverters is the same as that of trans-Z-source NPC inverters as calculated in equation (5.2). However, connecting the embedded inductors serially to dc sources solves the discontinuous chopping input current problem of previous trans-Z-source NPC inverters.

6.5. Asymmetrical Transformer-Based Embedded-Z-Source NPC Inverters Simulation and Experimental Results

The proposed inverters have been verified by Matlab/PSIM toolbox simulation. The operation condition and system parameters are shown in Table. 6.1.

Type EA NPC inverters use shoot-through duty ratio 0.13 while type EB and type EC NPC inverters use shoot-through duty ratio 0.17 to make the boosted dc-link voltage roughly 2 times of the dc source voltage, as calculated from (6.4), (6.6) and (6.8).

6.5.1. Type EA Inverters

As above analyses, the operational characteristics of upper network components and lower network components are the same, the capacitor voltage $V_{C1up}=V_{C1dn}=V_{C1}$, $V_{C2up}=V_{C2dn}=V_{C2}$, peak dc-link voltage $\hat{v}_{iup} = \hat{v}_{idn} = \hat{v}_i$. Hence the transformer winding voltage, diode voltage and input inductor voltage for upper network and lower network have same values during shoot-through states and non-shoot-through states, only different in phase. Simulation results of dc-rail voltage $v_{iup}+v_{idn}$, NPC

Table. 6.1. Testing parameters of asymmetrical transformer based embedded Z-source NPC inverter.

Parameters	EA	EB	EC
Upper and lower DC source voltage $V_{dc}/2$	50 V		
Fundamental frequency f	60 Hz		
Switching frequency f_s	10 kHz		
Capacitor capacitance $C1_{up}=C2_{up}=C1_{dn}=C2_{dn}$	470 μ F		
Input inductor L	2 mH		
Load resistance R	40 Ω		
Load filter L_f	5 mH		
Modulation index M	0.8*1.15=0.92		
Shoot-through ratio (for boost operation only) d	0.13	0.17	
Transformer turns ratio n	2		

inverter line voltage v_{AB} , phase voltage v_{AN} , load line current i_a, i_b, i_c are shown in Fig. 6.9. The Zoom in view simulation results of dc-link voltage v_{iup}/v_{idn} , transformer winding voltage v_{W1up}/v_{W1dn} and v_{W2up}/v_{W2dn} , transformer winding current i_{W1up}/i_{W1dn} and i_{W2up}/i_{W2dn} , inductor voltage v_{L1}/v_{L2} , input current i_{L1}/i_{L2} , capacitor voltage V_{C1up}/V_{C1dn} and V_{C2up}/V_{C2dn} , diode voltage v_{D1}/v_{D2} are shown in Fig. 6.10. As analysed in Section 6.2, under buck operation mode, dc-link voltage becomes dc source voltage 50 V. The dc-rail voltage $v_{iup}+v_{idn}$ then becomes 100 V. Hence the inverter output line voltage v_{AB} has five distinctive voltage levels (-100, -50, 0, 50, 100 V), and output phase voltage v_{AN} has three voltage levels (-50, 0, 50 V). Since load $R = 4\Omega$ $L = 5$ mH and modulation ratio $M = 0.92$, the peak line current has amplitude $\frac{0.92*100}{2\sqrt{40^2+(2\pi 60*0.005)^2}} = 1.15$ A. It is very close to simulation results as shown in Fig. 6.9(a). Under boost operation mode, the dc-link voltage is boosted from $V_{dc}/2 = 50$ V to $\frac{1}{1-(2+2)*0.13} * 50 = 104$ V. Therefore, the dc-rail voltage has value chopping between 104 V and $104*2=208$ V. The output line voltage now has five voltage levels from -208 V to 208 V, and the phase voltage has three voltage levels switch from -104 V to 104 V. The ac output line current amplitude now has been boosted to two times the buck operation, 2.31 A, as shown in Fig. 6.9(b). Fig. 6.10 shows the zoom-in view results of type EA NPC inverter. Based on (6.4), under boost operation mode, the capacitor voltage $V_{C1} = \frac{1-0.13}{1-(2+2)*0.13} 50 = 90.5$ V and $V_{C2} = \frac{0.13(1+2)}{1-(2+2)*0.13} 50 = 40.6$ V. During shoot-through states, diode D1/D2 is reverse biased, inverter bridge is shorted and the dc-link voltage becomes zero. The winding W2 has voltage of V_{C1} 90.5 V and winding W1 has voltage $n_{EA}*v_{W2} = 2*90.5 = 181$ V. During non-shoot-through states, diode D1/D2 is forward biased, and thus the diode voltage becomes zero. The dc-link voltage is boosted to 104 V. The winding W1, W2 and capacitor C2 now forms close circuit so that $v_{W1}+v_{W2}=-V_{C2}$. With $v_{W1}=n_{EA}*v_{W2}$, v_{W1} can be derived to be -27.1 V. The average input current can be calculated to be $I_{in} = \frac{3I_a^2*R}{2V_{dc}} = 3.92$ A. These are all expected as shown in the simulation results. The corresponding experimental results are shown in Fig. 6.11-Fig. 6.13.

Fig. 6.9. Simulation results type EA NPC inverter dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and load currents i_a , i_b , i_c during (a) buck operation $M=0.92$, $d=0$ and (b) boost operation $M=0.92$, $d=0.13$ (time: 10 ms/div).

Fig. 6.10. Simulation results of type EA2 NPC inverter (a) zoom in view dc-link voltage v_{iup}/v_{idn} , voltages and currents of transformer winding 1 and 2 v_{W1up}/v_{W1dn} , v_{W2up}/v_{W2dn} and i_{W1up}/i_{W1dn} , i_{W2up}/i_{W2dn} (b) input inductor voltage v_{L1}/v_{L2} , capacitor voltage V_{C1up}/V_{C1dn} , V_{C2up}/V_{C2dn} and diode voltage v_{D1}/v_{D2} during boost operation when $M=0.92$, $d=0.13$. (time: 0.01ms/div).

(a)

(b)

Fig. 6.11. Experimental results type EA NPC inverter dc rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and load current i_a during (a) buck operation $M=0.92$, $d=0$ and (b) boost operation $M=0.92$, $d=0.13$ (time: 5 ms/div).

Fig. 6.12. Experimental results of type EA2 NPC inverter (a) zoom in view dc-link voltage v_{iup} , voltages of transformer winding 1 and 2 v_{W1up} , v_{W2up} and diode voltage v_{D1} (b) input source voltage $V_{dc}/2$, inductor voltage v_{L1} capacitor voltage V_{C1up} , V_{C2up} during boost operation when $M=0.92$, $d=0.13$. (time: 0.05ms/div).

Fig. 6.13. Experimental results of type EA2 NPC inverter zoom in view input current i_{dc} , currents of transformer winding 1 and 2 i_{W1up} , i_{W2up} during boost operation when $M=0.92$, $d=0.13$. (time: 0.05ms/div).

6.5.2. Type EB Inverters

Under boost operation mode, with shoot-through duty ratio $d=0.17$ and transformer turns ratio $n_{EB}=2$, the peak dc-link voltage will be boosted to $\hat{v}_i = \frac{1}{1-\left(2+\frac{1}{2-1}\right)0.17} * 50 = 102 \text{ V}$ according to (6.6), close to the 104 V boosted dc-link voltage of type EA inverters. Therefore the resulted dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} and output load currents are similar as type EA inverters. The capacitor voltages can be calculated as $V_{C1} = \frac{1-0.17}{1-\left(2+\frac{1}{2-1}\right)0.17} * 50 = 84.7 \text{ V}$ and $V_{C2} = \frac{2*0.17}{1-\left(2+\frac{1}{2-1}\right)0.17} * 50 = 34.7 \text{ V}$. During shoot-through states, upper and lower inverter bridge are shorted. The diode D1 and D2 are reversed biased. The capacitor C1 and the transformer two windings now form a closed loop. The dc source, input inductor, capacitor C2 and winding W2 form another closed loop. With $v_{W1}=n_{EB}v_{W2}$, the winding voltage v_{W1} , v_{W2} can be calculated to be 169.4 V and 84.7 V respectively. During non-shoot-through states, diode D1 and D2 are forward biased, capacitor C2 and winding W1 form closed loop. Therefore, the transformer winding voltage $v_{W1}=-V_{C2}=-34.7 \text{ V}$ and $v_{W2}=v_{W1}/2=-17.35 \text{ V}$. The zoom in view simulation results of dc-link voltage v_{iup}/v_{idn} , transformer winding voltage v_{W1up}/v_{W1dn} and v_{W2up}/v_{W2dn} , transformer winding current i_{W1up}/i_{W1dn} and i_{W2up}/i_{W2dn} , inductor voltage v_{L1}/v_{L2} , input current i_{L1}/i_{L2} , capacitor voltage V_{C1up}/V_{C1dn} and V_{C2up}/V_{C2dn} , diode voltage v_{D1}/v_{D2} are shown in Fig. 6.14. And the corresponding experimental results are shown in Fig. 6.15 and Fig. 6.16.

(a)

(b)

Fig. 6.14. Simulation results of type *EBI* NPC inverter (a) zoom in view dc-link voltage v_{iup}/v_{idn} , voltages and currents of transformer winding 1 and 2 v_{W1up}/v_{W1dn} , v_{W2up}/v_{W2dn} and i_{W1up}/i_{W1dn} , i_{W2up}/i_{W2dn} (b) input inductor voltage v_{L1}/v_{L2} , capacitor voltage V_{C1up}/V_{C1dn} , V_{C2up}/V_{C2dn} and diode voltage v_{D1}/v_{D2} during boost operation when $M=0.92$, $d=0.17$. (time: 0.01ms/div).

Fig. 6.15. Experimental results of type *EBI* NPC inverter (a) zoom in view dc-link voltage v_{iup} , voltages of transformer winding 1 and 2 v_{W1up} , v_{W2up} and diode voltage v_{DI} (b) input source voltage $V_{dc}/2$, inductor voltage v_{L1} , capacitor voltage V_{C1up} , V_{C2up} during boost operation when $M=0.92$, $d=0.17$. (time: 0.05ms/div).

Fig. 6.16. Experimental results of type *EBI* NPC inverter zoom in view input and transformer winding currents during boost operation when $M=0.92$, $d=0.17$ (time: 0.05ms/div).

6.5.3. Type EC Inverters

Fig. 6.17. Simulation results of type EC NPC inverter (a) zoom in view dc-link voltage v_{iup}/v_{idn} , voltages and currents of transformer winding 1 and 2 v_{W1up}/v_{W1dn} , v_{W2up}/v_{W2dn} , i_{W1up}/i_{W1dn} , i_{W2up}/i_{W2dn} (b) input inductor voltage v_{L1}/v_{L2} , capacitor voltage V_{C1up}/V_{C1dn} , V_{C2up}/V_{C2dn} and diode voltage v_{D1}/v_{D2} during boost operation when $M=0.92$, $d=0.17$. (time: 0.01ms/div).

With shoot-through duty ratio $d=0.17$ and transformer turns ratio $n_{EC}=2$, the peak dc-link voltage can be boosted to $\hat{v}_i = \frac{1}{1-(2+1)0.17} * 50 = 102 \text{ V}$ according to (6.8). Therefore the results of dc-rail voltage ($v_{iup}+v_{idn}$), line voltage v_{AB} , phase to neutral voltage v_{AN} , output load currents are also similar as type EA inverters. Under boost operation mode, the capacitor voltages can be calculated as $V_{C1} = \frac{1-0.17}{1-(2+1)0.17} * 50 = 84.7 \text{ V}$ and $V_{C2} = \frac{2*0.17}{1-(2+1)0.17} * 50 = 34.7 \text{ V}$.

During shoot-through states, the upper and lower inverter bridges are shorted. The diode D1 and D2 are reversed biased. The capacitor C1 and the transformer winding

Fig. 6.18. Experimental results of type *EC1* NPC inverter (a) zoom in view dc-link voltage v_{iup} , voltages of transformer winding 1 and 2 v_{W1up} , v_{W2up} , and diode voltage v_{D1} (b) input source voltage $V_{dc}/2$, inductor voltage v_{LI} , capacitor voltage V_{C1up} , V_{C2up} during boost operation when $M=0.92$, $d=0.13$. (time: 0.05ms/div).

W2 now form a closed loop while dc source, inductor, capacitor C2 and winding W1 form another closed loop. With $v_{W1}=n_{EB}v_{W2}$, the winding voltage v_{W1} , v_{W2} can be calculated to be 169.4 V and 84.7 V respectively. During non-shoot-through states, diode D1 and D2 are forward biased. The capacitor C2 and winding W1 form closed loop. Therefore, the transformer winding voltage $v_{W1}=-V_{C2}=-34.7$ V and $v_{W2}=v_{W1}/2=-17.35$ V. The Zoom in view simulation results of dc-link voltage v_{iup}/v_{idn} , transformer winding voltage v_{W1up}/v_{W1dn} and v_{W2up}/v_{W2dn} , transformer winding current i_{W1up}/i_{W1dn} and i_{W2up}/i_{W2dn} , inductor voltage v_{L1}/v_{L2} , input current i_{L1}/i_{L2} , capacitor voltage V_{C1up}/V_{C1dn} and V_{C2up}/V_{C2dn} , diode voltage v_{D1}/v_{D2} are shown in Fig. 6.17. And the corresponding experimental results are shown in Fig. 6.18 and Fig. 6.19.

Fig. 6.19. Experimental results of type *ECI* NPC inverter zoom in view input and transformer winding currents during boost operation when $M=0.92$, $d=0.17$ (time: 0.05ms/div).

6.6. Summary

This chapter introduces seven types of transformer-based impedance-source NPC inverters with enhance voltage buck-boost capability and continuous input current. They are constructed based on the cascaded LCCT network and the six asymmetrical transformer-based embedded impedance-source networks. They embed the dc sources into the impedance-source networks, which make use of the impedance-source network inductors as input filters. Hence they eliminate the input filter. Therefore, the system size decreases and overall system efficiency increase subsequently.

Chapter 7 Z-Source Inverters in the Application of Grid-Tied Photovoltaic System

Most of the renewable energy available on earth is accounted by solar irradiation or its secondary solar power sources like wind, tidal, hydro electrical power and biomass energy. Capturing solar energy becomes a hot research area due to its plenty of resources. However, there are a lot of challenges ahead during photovoltaic power harvesting. One of them is the efficiency of conversion from solar to electricity. Maximum power produced by the photovoltaic system can be extracted by implementing a DC-DC buck-boost conversion stage to adjust the solar panel output voltage level. Z-source inverter can also be chosen to implement the grid-tied photovoltaic application, thanks to its buck-boost capability and reliable configuration. In the application of Z-source based grid-tied photovoltaic system, integrated MPPT algorithm is designed to produce the appropriate input reference for the controller. This controller controls the converter output voltage and makes it follow the MPP which is located at the knee of the photovoltaic I-V characteristics.

7.1. PV Characteristics

Fig. 7.1. Equivalent circuit diagram of a typical PV module.

7.1.1. PV Module

The simplest model for a PV panel consists of a current source in parallel with a diode, as shown in Fig. 7.1. The output of the current source is directly proportional to the solar irradiance, and the parallel diode determines the I-V characteristics of the solar cell. To make the model more sophisticated, a shunt resistance may be included in parallel with the diode [111]. For this research work, moderate complexity is preferred. Hence, the chosen model includes a temperature dependent photo-current I_L , diode saturation current I_0 , series resistance R_S and parallel diode D. Setting the current-temperature constant K_0 and ideality factor n , the equations for describing the I-V characteristics of the solar cell are given as [113]:

$$\begin{aligned}
 I &= I_L - I_0 \left(e^{\frac{q(V+IR_S)}{nkT}} - 1 \right) \\
 I_L &= I_{L(T_1)} (1 + K_0(T - T_1)) \\
 K_0 &= (I_{SC(T_2)} - I_{SC(T_1)}) / (T_2 - T_1) \\
 I_0 &= I_{0(T_1)} * (T/T_1)^{3/n} * e^{\frac{-qV_g}{nk(1/T-1/T_1)}} \\
 I_{0(T_1)} &= I_{SC(T_1)} / \left(e^{\frac{qV_{OC(T_1)}}{nkT_1}} - 1 \right) \\
 R_S &= -dV/dI_{V_{oc}} - 1/X_V \\
 X_V &= I_{0(T_1)} * q/nkT_1 * e^{\frac{qV_{OC(T_1)}}{nkT_1}} \quad (7.1)
 \end{aligned}$$

The constants in the above equations, such as open-circuit voltages $V_{OC(T_1)}/V_{OC(T_2)}$ and short-circuit currents $I_{SC(T_1)}/I_{SC(T_2)}$ at temperatures T_1/T_2 , can be extracted from the manufacturer's datasheets. The parameters used in the thesis are taken from the commercially available datasheet of solar panel Solarex MSX60 60W as an example. The relationship between the solar cell voltage V and current I can be expressed by the famously known Shockley Diode equation as given in (7.2).

$$I = I_0 \left(e^{\frac{q(V+IR_S)}{nkT}} - 1 \right) \quad (7.2)$$

Fig. 7.2. MSX60 I-V characteristics under various illumination levels at 25 °C.

Fig. 7.3. MSX60 P-V characteristics under various illumination levels at 25 °C.

Equation (7.2) is for a period when the cell is not illuminated. When the PV cell is opened, the photocurrent flows entirely through the diode. The I-V curve is then displaced from the origin by the amount of photocurrent I_L . There is a linear relationship between the photo-current and temperature, as shown by the second expression of (7.1). The fourth expression also illustrates this linear relationship, indicates that the change of photo-current with change of temperature. Based on the datasheet of MSX60 [112], as the temperature changes from 25°C to 75°C, the short circuit current I_L changes from 3.8A to 3.92A, which is directly proportional to the

Fig. 7.4. MSX60 I-V characteristics under various temperature levels at 1 sun.

Fig. 7.5. MSX60 P-V characteristics under various temperature levels at 1 sun.

irradiance G (Wm^{-2}). When the PV module is short circuited, the diode current is negligible. Therefore the proportionality constant current $I_{SC(T1,nom)}$ can set as rated short circuited current I_{SC} under rated irradiance (usually 1 Sun= 1000 Wm^{-2}) as derived in third expression. For MSX60, I_{SC} is 3.8A at 1 Sun under temperature 25°C. Fifth expression shows the relationship between saturation current I_0 and temperature T . The I_0 at temperature T_l is calculated from the open circuit voltage and short circuit current. According to [113], the ideality factor n can be suggested to be 1.2 under normal operation, and the series resistance R_s of the solar panel can be approximate 8 m Ω for seventh expression.

The I-V and P-V characteristics of the MSX60 model are illustrated at Fig. 7.2 to Fig. 7.5 under different operating conditions. As shown from these curves, the PV characteristics are highly dependent on the solar irradiance and temperature. These four figures give information about the open-circuit voltage, short-circuit current and the operating point where the module produces maximum power and corresponding operation voltage V_{max} and current I_{max} .

7.1.2. MPPT

Fig. 7.6 shows that the MPP and its corresponding operation voltage V_{max} and current I_{max} are located at the knee of the I-V curve. At MPP point (V_{max} , I_{max}), the slope of the P-V curve equals to zero.

$$\left. \frac{dP}{dV} \right|_{(V=V_{max})} = 0 \quad (7.3)$$

As $P=VI$, equation (7.3) can be rewritten as:

$$\begin{aligned} \frac{dP}{dV} &= I \frac{dV}{dV} + V \frac{dI}{dV} \\ \frac{dP}{dV} &= I + V \frac{dI}{dV} \end{aligned} \quad (7.4)$$

Hence:

$$\left(I + V \frac{dI}{dV} \right) \bigg|_{(V=V_{max})} = 0 \quad (7.5)$$

Fig. 7.6. MSX60 characteristics at 25°C, 1 sun irradiation.

Fig. 7.7. Flow chart of proposed MPPT method (Y=Yes, N=No).

holds at the maximum power operation point (MPP). And at the left side of the MPP, the differentiation of dP/dV is positive so that:

$$I + V \frac{dI}{dV} > 0 \quad (7.6)$$

while at the right side of MPP, the slope of P-V curve is negative and:

$$I + V \frac{dI}{dV} < 0 \quad (7.7)$$

For practical implementations, equation (7.5) is rarely met and small error e is permitted [114]. The size of the e is determined by the specific sensitivity requirement of the system. Normally e can be set to be a small positive digit and the MPPT tracking program may be set to idle when:

$$-1 * e < I + V \frac{dI}{dV} < e \quad (7.8)$$

The flow chart of MPPT algorithm is shown in Fig. 7.7. The algorithm is carried out each settled sampling time which depends on the atmosphere changing. This determines the output current reference of grid tide inverter.

7.2. Model Predictive Control of Z-Source Inverters

Control strategy for power converters has been developed since the middle of the twentieth century. It has since become a very active research topic in the field of power electronics. Among all control strategies investigated, the modulation scheme based linear control and hysteresis based nonlinear control are widely analyzed and improved over the past 60 years [115]. Cooperated with discrete time digital scenario, these control methods are wildly applied to industrial power electronic applications. In parallel, more complex control strategies have also been developed together with the evolution of digital signal processing techniques. Model Predictive Control (MPC) is one of them, and is now applied to the Z-source inverter.

7.2.1. MPC Strategy

The main process of MPC is to precalculate the behavior of a specific model and therewith to choose an optimal value for a control variable. MPC control allows multivariable system subjecting to constraints by formulating a control model of the object, needless any additional control loops which is essential for other control

Fig. 7.8. Schematic of MPC control strategy.

strategies such as PI or PR controller. Therefore, MPC has been established as a widespread and systematic control approach, which has been applied for current control of converters [116, 117], active filter [118], rectifiers [119], and uninterruptible power supplies [120]. The implementation steps of MPC can be illustrated as follows. Firstly the reference (load voltage or current of power converters for example) is set by designer. Secondly the predicted variables are estimated by a modulation stage. Next the predicted variables are used to be compared with reference variable. Lastly the one closest to the reference will be chosen as control variable. The control strategy is shown in Fig. 7.8, where x^* is the reference signal, x is system variable to be controlled, P_i are control actions, and $x_{pi(k+j)}$ ($i, j = 1, 2, 3 \dots n$) are the predicted variables derived based on previous system variables and control actions. Based on current system variable x_k , prediction starts from time t_k , predicts the next sample time variables. With different control actions, a set of predicted system variables $x_{pi(k+j)}$ can be derived. Among which, the one nearest to reference value, $x_{p3(k+1)}$ will be chosen and its corresponding control action P_3 will be used as system control action for time scope t_k to t_{k+1} . Then set $k=k+1$, pick the reference variable and do the predicting action again for the next sample time.

7.2.2. Model Predictive Control of Two-Level Z-source Inverter

Traditional Z-source inverter modulation strategies such as pulse width modulation with specified modulation index and shoot-through ratio provides good output voltage

Fig. 7.9. MPC control diagram for Z-source inverter.

Fig. 7.10. Configuration of grid-tied Z-source inverter.

waveform. However, there exists few feedback control methodologies for Z-source inverter [121]. The MPC control action is used to generate switching signals to control the 6 switches of a two-level three-phase Z-source inverter. The control diagram is shown in Fig. 7.9. Firstly the system variable of Z-source inverter x_k (load current or voltage) is measured. Secondly the predictive value is calculated by the predictive model. Next by comparing the reference value with predictive values, the one closest to the reference value is chosen, and the corresponding control action will be used as switch signal to drive Z-source inverter. Then set $k=k+1$ and repeat the steps.

A. Two-level Z-Source Inverter Predictive Model

The switching states of Z-source inverter can be determined gating signals S_a , S_b and S_c as shown below:

$$\begin{aligned}
 S_a &= \begin{cases} 1, & \text{if } SA \text{ on and } SA' \text{ off} \\ 0, & \text{if } SA \text{ off and } SA' \text{ on} \end{cases} \\
 S_b &= \begin{cases} 1, & \text{if } SB \text{ on and } SB' \text{ off} \\ 0, & \text{if } SB \text{ off and } SB' \text{ on} \end{cases} \\
 S_c &= \begin{cases} 1, & \text{if } SC \text{ on and } SC' \text{ off} \\ 0, & \text{if } SC \text{ off and } SC' \text{ on} \end{cases} \quad (7.9)
 \end{aligned}$$

And the corresponding vectorial form can be expressed as:

$$S = \frac{2}{3}(S_a + \gamma S_b + \gamma^2 S_c) \quad (7.10)$$

where $\gamma = e^{j2\pi/3}$. The output voltage space vectors generated by the inverter can be defined as:

$$V = \frac{2}{3}(v_{an} + \gamma v_{bn} + \gamma^2 v_{cn}) \quad (7.11)$$

where v_{an} , v_{bn} and v_{cn} are phase to neutral voltages of Z-source inverter as shown in Fig. 7.10. For a balanced three-phase load, the output line current of Z-source inverter can be expressed as:

$$i = \frac{2}{3}(i_a + \gamma i_b + \gamma^2 i_c) \quad (7.12)$$

The relationship of load voltage vector v and switching states S is: $V = S\hat{v}_i$ as derived from equation (7.10) and (7.11), where $\hat{v}_i$ is the peak dc-link voltage. Z-source inverter can be modeled as linear system with modulation techniques like pulse width modulation. While in this thesis, Z-source inverter is considered as discrete time system with 15 switching states, including 6 active states, 2 null states and 7 shoot-through states. There are 7 output voltage vectors, as shown in Table. 7.1. These states can also be illustrates as 7 different output voltage vectors when transformed into $\alpha\beta$ plane, as shown in Fig. 7.11, where ST stands for shoot-through states. The relationship of switching states and output voltage vectors can be shown in Table. 7.2.

Fig. 7.11. Output voltage vectors and switching sectors.

Table. 7.1. Switching states of two level three-phase Z-source inverter (!SX represents the complements of SX, where X = A, B, C).

State(output Voltage)	SA	SA'	SB	SB'	SC	SC'
Active [100] (finite)	1	0	0	1	0	1
Active [110] (finite)	1	0	1	0	0	1
Active [010] (finite)	0	1	1	0	0	1
Active [011] (finite)	0	1	1	0	1	0
Active [001] (finite)	0	1	0	1	1	0
Active [101] (finite)	1	0	0	1	1	0
Null [000] (0V)	0	1	0	1	0	1
Null [111] (0V)	1	0	1	0	1	0
Shoot-Through E1(0V)	1	1	SB	!SB	SC	!SC
Shoot-Through E2(0V)	SA	!SA	1	1	SC	!SC
Shoot-Through E3(0V)	SA	!SA	SB	!SB	1	1
Shoot-Through E4(0V)	1	1	1	1	SC	!SC
Shoot-Through E5(0V)	1	1	SB	!SB	1	1
Shoot-Through E6(0V)	SA	!SA	1	1	1	1
Shoot-Through E7(0V)	1	1	1	1	1	1

In $\alpha\beta$ plane, the load EMF can be expressed as:

$$e = \frac{2}{3}(e_a + \gamma e_b + \gamma^2 e_c) \quad (7.13)$$

Assuming that the Y-connected load is balanced, the load L filter $L_a=L_b=L_c=L_f$ and its series resistance $R_{La}=R_{Lb}=R_{Lc}=R_{Lf}$. The three balanced grid phases have same amplitude and 120° phase difference with each other. So that the load dynamics can be described by the following vector equation:

$$v = L_f \frac{di}{dt} + R_{Lf} i + e \quad (7.14)$$

A discrete form of load equation (7.14) with sampling time T_s can be used to predict the future value of the load current and voltage by making use of the measured current and voltage at k th sampling instance. Approximate the derivative di/dt by:

$$\frac{di}{dt} \approx \frac{i(k) - i(k-1)}{T_s} \quad (7.15)$$

Substituting it into (7.14), following equation can be derived for load current:

$$i(k) = \frac{(v(k) - e(k))T_s + L_f i(k-1)}{R_{Lf}T_s + L_f} \quad (7.16)$$

Table. 7.2. Relationship of switching states and output voltage space vector.

SA	SB	SC	V
1	0	0	$V1 = \frac{2}{3} \hat{v}_i$
1	1	0	$V2 = \frac{1}{3} \hat{v}_i + j \frac{\sqrt{3}}{3} \hat{v}_i$
0	1	0	$V3 = -\frac{1}{3} \hat{v}_i + j \frac{\sqrt{3}}{3} \hat{v}_i$
0	1	1	$V4 = -\frac{2}{3} \hat{v}_i$
0	0	1	$V5 = -\frac{1}{3} \hat{v}_i - j \frac{\sqrt{3}}{3} \hat{v}_i$
1	0	1	$V6 = \frac{1}{3} \hat{v}_i - j \frac{\sqrt{3}}{3} \hat{v}_i$
Null and Shoot-through states			$V7 = 0$

The future load current can be determined by shifting the discrete-time equation (7.16) one step ahead:

$$i(k+1) = \frac{(v(k+1) - e(k+1))T_s + L_f i(k)}{R_{Lf}T_s + L_f} \quad (7.17)$$

where $e(k+1)$ is grid voltage at next sampling time, which changes considerably small for a sufficiently small sampling time so that we can assume $e(k+1) \approx e(k)$. From (7.17), predicted load voltage at next sampling time can be computed as:

$$V_{(k+1)} = e(k+1) + R_{Lf}i(k+1) - L \frac{i(k+1) - i(k)}{T_s} \quad (7.18)$$

The prediction program chooses the switching state which produces the minimum difference between reference value and predictive value calculated from (7.17). One possible way to do this comparison is to formulate a cost function. By minimizing the cost function, proper current or voltage vector can be obtained and corresponding switching state can be chosen. For instance, the cost function of load current is formulated as:

$$C = |i_{\alpha}^* - i_{\alpha(k+1)}| + |i_{\beta}^* - i_{\beta(k+1)}| \quad (7.19)$$

where i_{α}^* and i_{β}^* is the real and imaginary part of reference current respectively, while $i_{\alpha(k+1)}$ and $i_{\beta(k+1)}$ are the predicted current at next sampling time.

B. Two-level Z-source Inverter Considerations and Implementations

Apparently, load current is the main concern for regulation of grid-tied application. Other factors may also be specially considered for Z-source inverter, such as the Z-source inverter network inductor current and capacitor voltage stabilization, varied switching frequency regulation, transient reservation and null state penalization. The regulations of these factors can be achieved by making use of the MPC multivariable system constraint capability.

1). Z-Source Network Inductor Current Stabilization

Regulating the Z-source network inductor current and capacitor voltage can help to stable the inverter system. This current regulation can be achieved by adding an extra description equation to the cost function, supposing $x=1, 2$:

$$g_L = |i_{Lx}^* - i_{Lx(k+1)}| \quad (7.20)$$

where i_{Lx}^* is reference value of network inductor current, which can be estimated as $i_{Lx}^* = \frac{P_{out}}{V_{dc}}$. And $i_{Lx(k+1)}$ is the predicted value of inductor current which can be expressed as two parts according to the shoot-through and non-shoot-through states:

During Non-shoot-through states:

$$i_{Lx(k+1)} = i_{Lx(k)} + \frac{T_s}{L_x} (v_{dc} - v_{cap(k+1)}) \quad (7.21)$$

During Shoot-through states:

$$i_{Lx(k+1)} = i_{Lx(k)} + \frac{T_s}{L_x} v_{cap(k+1)} \quad (7.22)$$

where $v_{cap(k+1)}$ is the one step advance capacitor voltage, as the change of capacitor voltage is considerably small within one sampling time so that we can assume that $v_{cap(k+1)} \approx v_{cap(k)}$ and it can be measured from the Z-source network.

2). Z-Source Network Capacitor Voltage Stabilization

Similar as inductor current stabilization, capacitor voltage stabilization can also be obtained by adding an extra description equation

$$g_c = |v_{capx}^* - v_{capx(k+1)}| \quad (7.23)$$

to the cost function. Where v_{capx}^* is the next step capacitor voltage reference value which can be estimated as:

$$v_{capx}^* = 2 * \hat{v}_i \quad (7.24)$$

and $v_{capx(k+1)}$ is the predictive capacitor voltage value, it can be estimated according to non-shoot-through and shoot-through states respectively:

During Non-shoot-through state:

$$v_{capx(k+1)} = v_{capx(k)} + \frac{T_s}{C_{capx}} (i_{indx(k+1)} - i_{inv(k+1)}) \quad (7.25)$$

During Shoot-through state:

$$v_{capx(k+1)} = v_{capx(k)} - \frac{T_s}{C_{capx}} i_{indx(k+1)} \quad (7.26)$$

where C_{capx} is the capacitor capacitance, and $i_{indx(k+1)}$ is the next step inductor current which can be approximated to be $i_{indx(k)}$ for a sufficient small sampling time T_s . $i_{inv(k+1)}$ is the inverter load current which can be calculated from the load specification.

3). Switching Frequency Regulation

Due to the nature of MPC algorithm, the switching frequency of Z-source inverter under MPC process is variable. The inconsistent switching frequency may affect the output performance. In order to increase the performance, variable switching frequency of MPC is better to be regulated in a certain level. In this thesis, the fixed switching frequency regulation term is:

$$g_f = |f_{sw}^* * T_s - com(i)| \quad (7.27)$$

where f_{sw}^* is desired switching frequency and $com(i)$ is number of commutation states per sampling time at chosen switching state.

4). Transient Reservation and Null State Penalization

According to [122], due to the existence of RHP zero indicating non-minimum-phase response of the dc voltage v_{dc} , undershoot current dip occurs during transient process. In order to minimize this non-minimum-phase effect, certain amount of null state is needed in order to reduce the load current dip for pulse width modulation of Z-source inverter. The non-minimum-phase effect also exists when using MPC. Thus, the null states are inserted in-between active and shoot-through state during transient process. It can be achieved by adding a positive Transient Reservation term TR in the cost

function. The TR term can be a smaller value for null states and bigger value for active or shoot-through states. On the other hand, [33] indicates that the null states will decrease the boost range of Z-source inverter, the biggest boost gain occurs when there's no null state. Thus a Null State Penalization factor NSP can be added during non-transient state. In contradiction to transient reservation term, NSP can be set bigger for null states and smaller for active or shoot-through states.

5). Optimal Switching Control

Switching frequency is directly related to the switching power loss of inverter system, especially under high power high switching frequency operation. To increase the system efficiency, optimal switching control has to be considered to reduce the switching commutation states. After load and Z-source network voltage/current regulations and transient reservation, the optimal switching control will choose the optimal switching state to minimize the switching state changing. This technique calculates commutation states $com(i)$ and chooses the one with minimum commutations.

Summing up all the constraints and regulations together, the final cost function can be expressed as:

$$CF = \lambda_1 i + \lambda_2 g_L + \lambda_3 g_c + \lambda_4 g_f + TP + NSP \quad (4.28)$$

where $\lambda_1, \lambda_2, \lambda_3, \lambda_4, \lambda_5$ are weighting factors which are designed under different operation conditions.

C. Simulation Results

The simulation is carried out on *Matlab/Simulink* platform with PLECS toolbox. The sample time is set to be $T_s = 20 \mu s$, input voltage is set to be $V_{dc} = 150 V$, reference ac output peak value $V_{out}^* = 110 V_{RMS}$, desired switching frequency $f_s^* = 20 kHz$, Z-source network inductor inductance $L_1 = L_2 = 2 mH$, capacitance $C_1 = C_2 = 470 \mu F$, grid peak voltage $e_a = e_b = e_c = 110 * \sqrt{2} V$, load inductor $L = 5 mH$ with inductor resistance $R_L = 0.5 \Omega$.

Fig. 7.12. Simulation results of (from top to bottom) (a) phase to neutral voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c , and (b) discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c during transient response of MPC Z-source grid-tied inverter.

Simulation results of MPC Z-source grid-tied inverter phase voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c are shown in Fig. 7.12(a). And the discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c are shown in Fig. 7.12(b). The load current is boosted as required when setting the peak load current reference of predictive mode changing from 2 A to 3 A during transient process. The input inductor current changes from 3.12 A to 4.72 A, and the capacitor voltage is boosted to approximately 336 V. The phase to neutral voltage and grid voltage amplitudes remain unchanged during transient process. It indicates that the system voltage regulation is stable.

7.2.3. Model Predictive Control of Z-source NPC Inverter

As described in Chapter 2, both of Z-source NPC inverters with two impedances or single LC network have voltage buck-boost capability without any switches in the dc-dc stage. Besides traditional pulse width modulation of Z-source NPC inverters, MPC can be easily implemented to control Z-source NPC inverters by considering their possible switching states. Also, with MPC's capability of constraining multi-system variables, the quality of output waveform, stability of impedance-network, level constraint of variable switching frequency as well as robustness of transient response all can be regulated with an accurately formulated Z-source network model. Common-mode voltage of three-level Z-source NPC inverters also can be eliminated by making use of MPC control strategy and hence improve the EMI level [123].

A. Z-Source NPC Inverter Predictive Model

Three sets of phase to neutral point voltages V_{xN} ($x = a, b, c$) can be obtained by controlling switching signals S_x :

$$V_{xN} = \hat{v}_{iup}/\hat{v}_{idn}(\text{two-network}) \text{ or } \frac{\hat{v}_i}{2}(\text{single network}); \begin{cases} S_{x1} \text{ and } S_{x2} \text{ on} \\ S_{x'1} \text{ and } S_{x'2} \text{ off} \end{cases}$$

Fig. 7.13. Configuration of grid-tied Z-source NPC inverter with two impedance-source networks.

$$V_{xN} = 0; \begin{cases} S_{x1} \text{ off and } S_{x2} \text{ on} \\ S_{x'1} \text{ on and } S_{x'2} \text{ off} \end{cases}$$

$$V_{xN} = -\hat{v}_{iup}/-\hat{v}_{idn}(\text{two-network}) \text{ or } -\frac{\hat{v}_i}{2}(\text{single network}; \begin{cases} S_{x1} \text{ and } S_{x2} \text{ off} \\ S_{x'1} \text{ and } S_{x'2} \text{ on} \end{cases})$$

(7.29)

The shoot-through state can be achieved by turning on S_{x1} , S_{x2} , $S_{x'1}$ and $S_{x'2}$ ($X = A, B, C$) at same phase leg simultaneously. Also assuming that the Y-connected load is balanced and the load L filter $L_a=L_b=L_c=L_f$ series resistance $R_{La}=R_{Lb}=R_{Lc}=R_{Lf}$. The voltage difference between phases to load neutral point n can be expressed as:

$$v_{xn} = v_{xN} - v_{nN}$$

$$v_{xn} = L_f \frac{di_x}{dt} + i_x R_{Lf} + e_{xn} \quad (7.30)$$

For a three-phase system under balanced operation condition:

$$i_a + i_b + i_c = 0$$

$$e_a + e_b + e_c = 0 \quad (7.31)$$

From equation (7.30) and (7.31) the following expression can be derived:

$$\begin{aligned}
 v_{an} &= \frac{2}{3}v_{aN} - \frac{1}{3}(v_{bN} + v_{cN}) \\
 v_{bn} &= \frac{2}{3}v_{bN} - \frac{1}{3}(v_{aN} + v_{cN}) \\
 v_{cn} &= \frac{2}{3}v_{cN} - \frac{1}{3}(v_{aN} + v_{bN})
 \end{aligned} \quad (7.32)$$

The space vectors of output voltage, output phase current and grid voltage generated by the inverter are defined as:

$$\begin{aligned}
 v &= \frac{2}{3}(v_{an} + \gamma v_{bn} + \gamma^2 v_{cn}) \\
 i &= \frac{2}{3}(i_a + \gamma i_b + \gamma^2 i_c) \\
 e &= \frac{2}{3}(e_a + \gamma e_b + \gamma^2 e_c)
 \end{aligned} \quad (7.33)$$

Fig. 7.14. Configuration of grid-tied Z-source NPC inverter with single LC network.

Fig. 7.15. Three-level to two-level state mapping for a Z-source NPC inverters modulation (a) RCM three-level vector diagram (b) two-level vector diagram.

NPC inverter is restricted to seven inverter states which have zero common mode voltage as described in [123, 124]. Therefore this three-level NPC system can be mapped to two-level system. This three-level (RCM) to two-level (V) state mapping can be illustrated by Reduced Common Model (RCM) technique as shown in Fig. 7.15. The load equation and cost function derived for Z-source NPC inverters are the same as two-level Z-source inverter since the grid-tied loads are set the same, as expressed in equation (7.15) to (7.19). With same constraints and regulations as those of two-level version, the cost function then can be computed same as (4.28).

B. Simulation Results

The simulation is carried out on *Matlab/Simulink* platform with PSIM toolbox. The sample time is set to be $T_s = 20 \mu s$, input voltage is set to be $V_{dc} = 150 V$, switching frequency reference $f_s^* = 5 kHz$, Z-source network inductor inductance $L_{1up} = L_{2up} = L_{1dn} = L_{2dn} = L_1 = L_2 = 2 mH$ with series resistance 0.5Ω , capacitance $C_{1up} = C_{2up} = C_{1dn} = C_{2dn} = C_1 = C_2 = 470 \mu F$, load inductor $L = 5 mH$ with series resistance $R_L = 0.5 \Omega$.

Fig. 7.16. Simulation results of (from top to bottom) (a) phase to neutral voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c , and (b) discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c during transient response of MPC Z-source grid-tied NPC inverter with two impedance-source networks.

Fig. 7.17. Simulation results of (from top to bottom) (a) phase to neutral voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c , and (b) discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c during transient response of MPC Z-source grid-tied NPC inverter with single LC network.

Simulation results of MPC Z-source grid-tied NPC inverter with two impedance-source network phase to neutral voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c , and discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c are shown in Fig. 7.16. The v_{an} , V_C , and three-phase grid voltage have been regulated steadily. The grid currents have been forced to track reference current with peak amplitude changes from 2 A to 3 A. Both the source current and network inductor current step up correspondingly. The step change process shows clearly the robustness and effectiveness of MPC algorithm.

The simulation results of MPC Z-source grid-tied NPC inverter with single LC network phase to neutral voltage v_{an} , capacitor voltage V_C , grid voltage e_a, e_b, e_c are shown in Fig. 7.17(a), and discontinuous input current i_{in} , network inductor current i_L , and grid currents i_a, i_b, i_c are shown in Fig. 7.17(b).

The results of Z-source NPC inverter with two-impedance networks and with single LC network are similar. The only difference is the capacitor voltage which is 167V for two-network NPC inverter and 326V for single network NPC inverter. The higher voltage is the trade-off of eliminating additional passive components.

7.3. Implement Z-Source Grid-Tied Inverter into Photovoltaic System

The implementation of Z-source grid-tied inverter to photovoltaic system the can be

Fig. 7.18. Control diagram of implementation Z-source inverter into photovoltaic system through MPC algorithm.

easily achieved by MPC algorithm. The first step of this control program is extracting the input voltage and current of the PV panel. Then the MPPT algorithm calculates the MPP operation voltage V_{max} , current I_{max} as well as the corresponding maximum power at MPP and feeds the results into MPC as input references. After getting the MPP operating voltage V_{max} , current I_{max} , grid load voltage and current, the MPC calculates the switching signals of the inverter. Finally the inverter switches based on the signals produced by MPC and injects power into the grid. The control diagram flow chart is shown in Fig. 7.18. The implementation is just a simple combination of MPPT method with MPC of Z-source grid-tied inverter concepts, which is rather straight forward. More sophisticated control models such as using MPC to calculate panel MPP directly and then predictively control the inverter switches can be develop, which will refer to future research topics.

7.4. Summary

This chapter focuses on the MPC of Z-source inverters in the application of grid-tied photovoltaic systems. Basic theories of photovoltaic MPPT and Z-source inverters MPC algorithm have been presented. Simulation results of MPC two-level Z-source inverter, Z-source NPC inverter with two impedance networks and single LC network have been depicted to demonstrate the robustness and effectiveness of MPC program. The cost functions of MPC Z-source inverters can be further optimized, and then comparison between MPC and classical feedback controllers like PI, PR can be implemented, which all could be put into future research concern.

Chapter 8 Conclusion and Recommendations

After reviewing existing knowledge and presenting contributions in earlier chapters, the thesis is concluded in this chapter, together with some future recommendations for research.

8.1. Conclusion

Environmental dependent renewable energy applications require sophisticated power conversion systems for conditioning inconsistent green power into reliable power for grid-tied or islanded usage. Conventional DC-AC or AC-DC-AC converters may not be suitable for all situations since they can normally operate in the voltage-buck mode only. One solution is to add a DC-DC boost converter to the DC-AC inverter. Although straightforward, its lack of functionality merging may lead to the presence of some unnecessary components. Because of that, various single-stage DC-AC buck-boost inverters have been proposed with functionality merging. One good example is the Z-source inverter constructed by adding a unique X-shaped impedance network to the front end of a traditional DC-AC inverter.

The unique impedance network, to a great extent, makes the Z-source inverter a safe configuration, which does not require dead-time for short-circuit or shoot-through protection. Instead, it makes use of the shoot-through state for boosting its output ac voltage without increasing commutation count and with better harmonic performance since dead-time is omitted. Like its traditional DC-AC companion, the Z-source concept can also be extended to three-level Z-source inverters, which when modulated properly, will result in lower switching voltage stress and further improvement of the inverter performance.

Despite the extension to three-level inverters, the gain expression of existing Z-source inverters remains unchanged. This means further improvements can be introduced to increase the inverter voltage gain, lower its component voltage stress or filtering its

chopping input current that an existing Z-source inverter will face. Towards that scope, six asymmetrical transformer-based embedded Z-source inverters are studied in the thesis. The proposed inverters utilize magnetically coupled circuits to replace one of the two inductors found in the traditional Z-source inverter. With different transformer dot orientations, these inverters achieve different voltage boost capabilities over the traditional Z-source inverter. In common though, with the proper transformer turns ratio set, all six inverters can arrive at the same voltage boost gain with a much smaller shoot-through duty ratio, as compared with the traditional Z-source inverter. Smaller shoot-through ratio then allows a higher modulation ratio to be utilized, whose favourable impacts are lower device voltage stress and better terminal waveform quality. Moreover, with the dc source embedded in series with the network inductor, the proposed inverters draw a smoother input current even with no additional input filter used.

Several types of three-level transformer-based Z-source NPC inverters are next introduced. The first type of transformer-based Z-source NPC inverters are effectively created by cascading two trans-Z-source impedance-source networks to gain higher voltage boost than the traditional Z-source NPC inverter with two impedance-source networks. Based on the same concepts, Γ -source NPC inverter uses two cascaded Γ -shaped impedance-source networks to arrive at the same high gain, but a reduced, rather than increased, transformer turns ratio. The asymmetrical transformer-based embedded Z-source inverters are also configured, whose aim is to achieve enhanced voltage boost, while at the same time, draw a continuous input current even with three-level voltage switching. To a useful extent, the proposed NPC inverters have therefore successfully integrated the advantages of the transformer-based impedance-source network and the classical three-level NPC switching. The characteristics and main features of each proposed topology are summarized in Table. 8.1.

Last but not least, the thesis presents a model predictive control scheme for controlling the two-level and three-level Z-source inverters as a grid-tied photovoltaic system. The same scheme can also be used with the earlier proposed Z-source inverters. The presented MPC scheme effectively develops a predictive model for determining the control times and sequences of the inverter switches after collecting

reference and system information. The robustness and effectiveness of the scheme has been verified in simulations.

Table. 8.1. Summarized features of asymmetrical transformer-based EZ-source inverters.

Topology	Input voltage	AC output voltage	Turns ratio for boosting	Advantages compare to conventional Z-source (or Z-source NPC) inverters
Asymmetrical <i>EA</i>	V_{dc}	$\hat{v}_{ac} = \frac{1}{1 - (2 + n)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 0$	-High modulation ratio at high gain
Asymmetrical <i>EB</i>	V_{dc}	$\hat{v}_{ac} = \frac{1}{1 - (2 + 1/(n-1))d} \left(\frac{MV_{dc}}{2} \right)$	$1 < n < 2$	-Better waveform quality
Asymmetrical <i>EC</i>	V_{dc}	$\hat{v}_{ac} = \frac{1}{1 - (1 + n)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 1$	-Lower switch stress
Trans-Z NPC with two cascaded impedance networks	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - (n+1)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 1$	-Continuous input current
Trans-Z NPC with single impedance network	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - 2d} \left(\frac{MV_{dc}}{2} \right)$	$n=1$	-Source filter not required
Γ -source NPC inverter	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - \left(1 + \frac{1}{n-1}\right)d} \left(\frac{MV_{dc}}{2} \right)$	$1 < n < 2$	-Improved output waveform quality
LCCT NPC inverter	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - (n+1)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 1$	-Lower switch stress
Asymmetrical <i>EA</i> NPC inverter	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - (2 + n)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 0$	-Less component counts
Asymmetrical <i>EB</i> NPC inverter	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - (2 + 1/(n-1))d} \left(\frac{MV_{dc}}{2} \right)$	$1 < n < 2$	-Smaller size
Asymmetrical <i>EC</i> NPC inverter	$V_{dc}/2$	$\hat{v}_{ac} = \frac{1}{1 - (1 + n)d} \left(\frac{MV_{dc}}{2} \right)$	$n > 1$	-Lower cost

For the proposed two-level asymmetrical transformer-based type *EA*, *EB* and *EC* inverters, it can be implemented in many applications such as motor drives, photovoltaic systems, fuel cells, distribution generation systems and uninterruptable power supplies. While the proposed three-level transformer-based NPC inverters are recommended to be used for medium voltage, high power applications like ac motor drives, can also been investigated for low power applications such as low voltage drives, traction and utility applications.

8.2. Recommendations for Further Research

The proposed control strategy and inverter topologies are for making the impedance-source inverters more attractive as options for renewable energy generation. There are however still some constraints and limitations yet to be resolved. These are mentioned below as possible ideas for future investigation.

1. The cost function parameters of the model predictive control algorithm have not been optimized. A more sophisticated model can be developed by considering the cost, size, system efficiency and other possible concerns besides the controlled ac output current. Therefore, optimization of the predictive model is considered a topic that can be further investigated.
2. The impedance-source inverters proposed have advantages over the traditional Z-source inverter, which hence make them good substitutes for the traditional Z-source inverter in DC-AC power conversion. Finding and exploring practical applications for the inverters are therefore of value, and can be planned for future research.
3. The impedance-source inverters proposed in the thesis are only of the voltage-source type. For some applications, the current-source type might be preferred. Thus, the current-source type impedance-source inverters can be considered as a possible future research area.

Author's Publications

Premium Journal Publications

- [1] Mo Wei, Loh Poh Chiang, Frede Blaabjerg, "Asymmetrical Γ -Source Inverters," *IEEE Transactions on Industrial Electronics*, 2013 , Volume: 61, issue: 2, p. 637-647.
- [2] Mo Wei, Loh Poh Chiang, Frede Blaabjerg, "Asymmetrical transformer-based embedded Z-source inverters," *IET Power Electronics* Volume 6, issue 2, 2013 , p. 261 - 269.
- [3] Mo Wei, Loh Poh Chiang, Frede Blaabjerg, Wang Peng "Trans-Z-Source and Γ -Z-Source Neutral-Point-Clamped Inverters," *IET Power Electronics*, Accepted with minor revision.

Premium Conference Publications

- [1] Mo Wei, Loh Poh Chiang, Frede Blaabjerg, "Single stage buck-boost dc-ac neutral point clamped inverter," *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp.318, 323, 15-20 Sept. 2012.
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