Gate-all-around silicon nanowire FET modeling

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**GATE-ALL-AROUND SILICON NANOWIRE FET
MODELING**

CHEN XIANGCHEN

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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Abstract

As a further extension of the multi-gate MOSFET, the gate-all-around (GAA) silicon nanowire FET is the most promising nanostructure design for next generation semiconductor device. Recent research work demonstrates the excellent device performance of GAA silicon nanowire FET, especially the gate controllability and short channel effect immunity. In this work, the device modeling of GAA silicon nanowire FET is presented. The modeling work is performed in TCAD environment, and several essential modeling topics are discussed.

The process modeling and device characterization modeling are first investigated since these are the fundamental part of this project. The carrier transport selection, device self-heating effect and process induced stress effect are discussed based on the modeling results. The performance advantages of GAA silicon nanowire FET is then evaluated by conducting a comparison study between the GAA FET and FinFET.

The electrostatic discharge (ESD) modeling on GAA silicon nanowire FET is then discussed. From a contrast study to verify the simulation model with reported experiment work, the accuracy of proposed modeling is confirmed. Based on the ESD modeling, further device degradation characterization is performed and the degradation mechanism is explained. Under the ESD stress, the GAA silicon nanowire FET is found to degrade due to the hot carrier induced interface state generation. In the condition of severe stress, the device

melts catastrophically and results in hard breakdown. Both degradation phenomenons are supported by modeling result and experiment conclusion.

The random dopant fluctuation (RDF) effect is also discussed on the GAA silicon nanowire FET in this work. The RDF is a major process variation issue due to discrete dopant atom placement. The statistical simulation methodology is integrated with device simulation to characterize the RDF effect. From the extracted characterization result, the GAA silicon nanowire FET shows good RDF robustness which benefits from the intrinsic nanowire doping. A semi-analytical model is also introduced to study the RDF variation of GAA silicon nanowire FET.

Last but not least, the junctionless GAA silicon nanowire FET is also introduced. As an alternative design of GAA silicon nanowire FET, the junctionless device shows excellent electrical performance as its inversion mode counterpart. However, from the device characterization result and semi-analytical analysis, the junctionless device also shows more severe performance variation problem due to RDF which could limit its further practical usage.

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Chapter 1 Introduction

1.1 Motivation

Over the past several decades, the MOSFET scales down continually without changing the basic structure. Smaller MOSFET is more desirable for many reasons. One reason is that, more transistors can be packed into a given area with smaller feature size. This results the improvement of the functionality of chip and the reduction of manufacturing cost. Another reason is the faster switching of smaller transistor. Down scaling of the MOSFET reduces all the device dimensions proportionally. The gate capacitance gets reduced and the RC delay of transistor also gets scaled, which enhances the device switching speed.

The simple down scaling has become more challenging due to several reasons. As MOSFET structure shrinks, the gate voltage is designed to be smaller for device reliability. The device threshold voltage also needs to be reduced in order to maintain performance. This limits the device to turn off completely, which makes the subthreshold conduction become non-negligible. The down scaled MOSFET has even thinner gate oxide layer, the gate leakage then increases which results more power consumption and degraded reliability. The scaled gate length results in short channel length, which becomes comparable to the source/drain junction depletion width. The induced short channel effect leads device threshold voltage roll-off and increased junction leakage. For advanced technology, high-k dielectric material is used to maintain the dielectric physical thickness when scaling down the effective thickness, which

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can suppress the gate static leakage current due to quantum mechanical tunneling [1]. Also the channel doping engineering is applied to suppress the short channel effect. However there is already little space for further down scaling on planar MOSFET structure even with these new device design techniques.

The effort to maintain the device scaling down trend needs some new approaches on device structure design. Multi-gate MOSFET structure is a promising approach. Several proposed designs, such as dual-gate FET, FinFET and Omega-gate FET, are being massively researched during the last decade [1-4]. Multi-gate device is expected to have larger on-state current and better gate control. The improved gain and lower output resistance is desirable for the circuit design. And the device miniaturization continues by shrinking the footprint on chip area, but extends the effective channel width into the third dimension. The FinFET, as the most promising multi-gate MOSFET structure, is already in production by Intel from 2012 [5]. The gate-all-around (GAA) FET has the similar idea as the FinFET, but the gate material extends to surround the channel on all sides. The GAA FET has been successfully developed based on the silicon nanowire technology. The GAA FET is expected to be the next generation nano-structure device [6-11]. Its enhanced gate controllability and short channel effect immunity is attractive for the circuit design with further down scaled, short channel device.

However, the GAA nanowire device, as a deep scaled device, behaves differently from the classical large scale device in many aspects, such as the ballistic carrier transport and quantization mechanism [12, 13]. The small device feature size makes the device performance become sensitive to many

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factors, such as operating temperature, device self-heating and residual mechanical stress in the structure. A physics-based device modeling of GAA silicon nanowire FET is needed to study the device behavior and performance. The device modeling should not only cover the carrier transport, electrical performance modeling, but also to evaluate the related thermal and mechanical effects in order to create a practical, production worthy model. The device reliability is another important issue of GAA silicon nanowire FET. The operating condition can be scaled for the device, but the requirement for reliability cannot. The modern scaled device becomes more vulnerable to electrostatic discharge (ESD) [14, 15]. A comprehensive understanding of ESD induced failure or degradation is needed in order to evaluate the robustness or capability of GAA silicon nanowire FET against ESD, which is useful for future nanowire device based circuit design solution. The device modeling of ESD event on GAA silicon nanowire FET requires the coverage on device degradation modeling beyond electrical behavior modeling.

The GAA nanowire device also has the random dopant fluctuation (RDF) problem like the other deep scaled devices [16], as its tiny nanowire body contains only very few number of dopant atoms, the device performance is sensitive to the discrete dopant distribution in device channel. The RDF effect may limit the potential future usage of nanowire device, as in the device performance could spread seriously on the chip area, which affects the design overall performance in an unpredictable manner. Essential assessment on RDF induced device performance variation dependence on device dimension and related process condition is important to understand the possible device

performance window and also the possible device design method to control the RDF induced variation.

Modern circuit design relies on the simulation based on semiconductor device model. The GAA silicon nanowire FET modeling is performed using technology computer aided design (TCAD) tools in this work. With the above mentioned modeling considerations, the studies on different carrier transport models, thermal and self-heating effects and stress-strain effect are very necessary. Furthermore, the ESD modeling is examined in this work to evaluate the degradation behavior and device reliability of GAA silicon nanowire FET under ESD stress. Also the device statistical simulation methodology is applied to study the RDF robustness and optimization of GAA silicon nanowire FET.

1.2 Objective

This project can be divided into the following four phases.

The first phase is focused on electrical behavior modeling of GAA silicon nanowire FET based on TCAD simulation, which is the starting point and the foundation of the whole GAA silicon nanowire FET modeling work. The effects of applying different carrier transport models are studied. Then the effects of device self-heating and process induced stress are modeled and evaluated. To evaluate the advantages of GAA silicon nanowire FET, a comparison study between GAA FET and FinFET is also conducted.

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Based on the defined GAA silicon nanowire FET simulation model, two related device modeling topics, ESD event modeling and RDF effect modeling, are studied in the next phases of work.

The second phase explores device reliability topic, the ESD modeling of GAA silicon nanowire FET. The device thermal breakdown modeling through the transmission line pulse (TLP) simulation is first studied. The device ESD degradation is then evaluated by applying the hot-carrier-induced interface state kinetics modeling and the device post-degradation characterization. The device parameter shifting and interface state formation are tracked. The device degradation mechanism is also essentially analyzed.

The third phase discusses the RDF effect of GAA silicon nanowire FET, which captures the device performance variation of GAA silicon nanowire FET due to RDF. The simulation methodology related to RDF is introduced firstly. Then the RDF performance of GAA silicon nanowire FET is evaluated by both simulation result and semi-analytical modeling. Furthermore, the RDF performance of GAA silicon nanowire FETs with different geometry dimensions and process conditions are characterized in order to find a possible optimization design for better device RDF performance.

The last phase focuses on the junctionless GAA silicon nanowire FET. Since it is an alternative GAA nanowire device design which is different from the device discussed in the previous project phases, the junctionless GAA silicon nanowire FET is firstly characterized and compared with the normal inversion mode GAA silicon nanowire FET. The same RDF characterization is also conducted. Finally, the advantages and drawbacks of junctionless GAA silicon

nanowire FET is summarized and analyzed based on the characterization result.

1.3 Contribution of the Thesis

The major contributions of the thesis cover three aspects.

First is the simulation model of GAA silicon nanowire FET. The necessity of using drift-diffusion and density gradient carrier transport models is evaluated. The self-heating effect and process induced stress effect are also discussed. Moreover, both inversion mode and junctionless GAA silicon nanowire FETs are studied and compared.

Second is the ESD simulation model of GAA silicon nanowire FET. The ESD modeling simulation includes device thermal distribution tracking, interface degradation tracking and device degradation characterization. Based on the ESD modeling work, the GAA silicon nanowire FET device degradation under ESD stress is demonstrated. The device degradation mechanism is also essentially analyzed from the characterization result.

Third is the RDF modeling of GAA silicon nanowire FET. The RDF modeling describes the dopant fluctuation effect through random dopant placement methodology, and captures the RDF induced device characterization variation through impedance field method (IFM). Also, the RDF analysis on both inversion mode and junctionless GAA silicon nanowire FETs is performed in this project.

1.4 Organization of the Thesis

This thesis discusses the GAA silicon nanowire FET modeling project.

After Chapter 1 (project overall introduction) and Chapter 2 (literature review on project background), Chapter 3 discusses the electrical behavior modeling of GAA silicon nanowire FET as the starting point of the whole project. With a reliable and accuracy verified simulation model, Chapter 4 explores the ESD reliability and Chapter 5 discusses the intrinsic performance variation due to RDF of GAA silicon nanowire FET. The ESD reliability discussion of GAA silicon nanowire FET in Chapter 4 analyzes the failure and degradation of GAA silicon nanowire FET under ESD, which provides useful information to understand the ESD robustness of next generation nanowire device. The RDF related discussion in Chapter 5 analyzes the GAA nanowire device RDF impact with different device dimension and different process conditions, which provide possible device design methodology to suppress the RDF induced variation of GAA silicon nanowire FET. Moreover, two state-of-art GAA nanowire FET structures, the inversion mode and junctionless GAA nanowire FET, are introduced and compared in Chapter 6. Finally, Chapter 7 summarizes the whole project work and also discusses the recommendation of future work.

Chapter 2 Literature Review

This literature review chapter first covers the knowledge of nanowire device. The ESD model, ESD testing methodology and the semiconductor device degradation fundamentals are subsequently introduced as the background information for the ESD modeling of GAA silicon nanowire FET. The RDF related methodology is then introduced. A short discussion about TCAD application in semiconductor device analysis is presented last in this chapter.

2.1 Nanowire Technology

Nanowire device is recognized as one of the most promising candidate of the next generation nano-electronic device to extend the Moore's law with even scaled device feature size and higher density integration [11]. The gate-all-around (GAA) configuration, as a further extension of the multi-gate configuration design, can be successfully adopted on the nanowire device. Considering the process compatibility of silicon CMOS, the silicon nanowire is more preferable than III-V semiconductor or Germanium (Ge) nanowire. The silicon nanowire device shows huge potential in the electronic, optical and biochemical applications [17-20]. This section reviews the development work on nanowire device fabrication and characterization.

2.1.1 Nanowire Fabrication Process

Both bottom-up and top-down fabrication approaches are proposed and massively studied for the nanowire preparation [6, 8-10, 21-23]. The bottom-up nanowire fabrication uses the chemical- or laser-assisted catalytic growth to pattern the silicon nanowire and can form the nanowire with small feature size down to sub 10nm [23]. One maturely established fabrication method is nano-cluster assisted vapor-liquid-solid nanowire growth. The size of nano-cluster catalysts determines the nanowire thickness. With precise chemical control method to adjust the silicon growth orientation, the nanowire with high single crystallinity can be obtained. Another major bottom-up fabrication method is the laser-assisted catalytic growth. The laser beam with sub ultraviolet wavelength and high energy can cut the silicon film into extreme scaled size, and the nanowires grow with further silicon-metallic reaction under high temperature [24, 25]. The bottom-up nanowire formation method can create extreme small size nanowires as shown in Figure 2.1. However, the process control of nanowire orientation growth is very challenging [21, 23, 24].

Figure 2.1 Silicon nanowire prepared by laser-assisted growth method [25]

The top-down nanowire fabrication approach is totally different from the above mentioned bottom-up approach. The top-down approach patterns the nanowire or silicon finger using standard masks [26, 27]. The size limitation of lithography makes the nanowire formation require further trimming or oxidation techniques. One common method is the stress-limited thermal oxidation. The pre-etched silicon film in small dimension under precise temperature and time controlled oxidation process can be further trimmed down to sub 10nm thickness as shown in Figure 2.2 [26]. The formed oxide layer surrounds the trimmed silicon nanowire serve as an outer gate dielectric layer when the nanowire structure is further developed into MOSFET device.

Figure 2.2 Multiple silicon nanowires prepared by oxidation trimming [26]

The nanowire in only several nanometers thickness has limited current conduction throughput in the single nanowire configuration. To fabricate the device contains multiple nanowires is more practical for device development. However, multiple nanowire patterning is even challenging. A method of defining multiple nanowires in horizontal pitched manner is proposed in [26, 28]. The lithography mask and extra self-aligned polymer film divide the silicon film into further refined line structure in parallel. A vertical nanowire stack methodology is also proposed in order to provide multiple nanowire structure without increasing the integration density [29, 30]. The multiple nanowires scheme in vertical stack usually uses multiple material layer system plus stress-limited oxidation. The vertical stack process is harder to control than horizontal stack as it needs extra effort on interface control of multiple material layers. In most of the reported work on GAA silicon nanowire FET fabrication, the nanowire structure in horizontal stack manner is adopted. And now the total number of nanowires in one device can reach as many as one thousand [6, 7].

Most research effort attempts on GAA silicon nanowire FET fabrication development adopts the top-down nanowire patterning approach [6-10]. Figure 2.3 shows a GAA silicon nanowire FET with sub 10nm diameter silicon nanowire [6]. In general, the device fabrication process starts with an intrinsic p-doped silicon-on-insulator wafer. The active area is etched out down to the buried oxide layer and the silicon finger is patterned between source and drain regions. The silicon finger is then further trimmed down to nanowire size by thermal oxidation and then release. Gate stack material is defined by wrap the nanowire and dielectric layer, followed by spacer formation, source/drain dose implantation and dopant activation process, also the contact formation and other backend processes.

Figure 2.3 A GAA silicon nanowire FET after gate patterning [6]

Figure 2.4 shows the DC characterization result of the GAA silicon nanowire FET reported in [6]. Compare to other device gate configurations, the GAA nanowire FET shows relatively limited current conduction capability [6, 9]. However, it claims the advantages on its enhanced gate controllability and

short channel effect immunity [6-10]. The subthreshold swing (SS) level shows nearly ideal performance and the drain induced barrier lowering (DIBL) level is also extremely low. Furthermore, it shows much higher on- and off-state current throughput ratio than the planar FET and multi-gate FET [6, 7, 9], which benefits from its low off-state drain leakage current. This also proves the good gate controllability of the GAA configuration.

Figure 2.4 GAA silicon nanowire FET DC characterization [6]

2.1.2 Recent Development on GAA Silicon Nanowire FET

Recent research effort on GAA silicon nanowire FET fabrication focuses more on the optimization of device performance. The major optimization areas are the gate design, nanowire contact design and nanowire junction design [6, 10, 31, 32].

The gate design engineering of GAA silicon nanowire FET aims on the device threshold voltage adjustment. In the intrinsic lightly doped nanowire channel, the depleted charge density does not affect the device threshold effectively. Hence the device threshold level is tuned by the gate workfunction alone. Traditional doped polysilicon gate sets the device threshold voltage wrongly

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due to its limited workfunction range [9, 10]. The metal gate or silicide metal gate is developed to provide proper threshold voltage adjustment or even threshold voltage tuneability [7, 9, 10]. Common metal gate materials have been reported are Titanium and Nickel, their nitride and silicide compounds are also massively studied.

The silicon nanowire has very small contact area attach to the bulk source/drain region. Hence the nanowire contact resistance becomes extremely high which impacts the device current throughput. The developments on extra doping generation of source/drain nanowire extension region and metallic/silicide nanowire extension contact [6] successfully demonstrate the reduction of nanowire contact series resistance. And the device current driving capability of certain modified device improves significantly.

Another design optimization aspect is the nanowire junction configuration. Extreme high doping density gradient exists between the highly doped source/drain region and the intrinsic doped nanowire. It imposes fabrication work challenges when the device junction forms over a sub 10nm nanowire body [31, 33]. Far beyond an optimization design, an idea of junctionless nanowire FET suggests to use the same dopant type and uniform doping concentration over the source/drain region and nanowire channel. It eliminates the junction formation issue, while it actually changes the device work in depletion mode rather than conventional enhancement or inversion mode [31].

2.1.3 Junctionless GAA Silicon Nanowire FET

The junctionless nanowire device is designed to eliminate junction formation challenge of normal enhancement mode nanowire FET. Some research work recently even claims that the junctionless FET has extremely simple fabrication process [34, 35]. The nanowire structure is patterned after the implantation and annealing process of top silicon layer, differs from the enhancement mode FET, which generates the source/drain doping after gate stack and spacer formation.

The junctionless device works in depletion mode, which so called normal-on operation. Rather than conducting with gate induced inversion charge channel, the device takes the advantage of forming gate induced depletion region to block off the conducting channel. Figure 2.5 depicts the carrier concentration contour plots in an n-doped junctionless FET under progressive gate biasing voltage [31]. When the gate is biased at threshold voltage, the conducting channel is just pinched off. In order to obtain an effective fully depletion operation, the nanowire body should be thin and narrow, also the nanowire is better to be lightly doped [34-36].

Figure 2.5 Electron concentration in a n-type junctionless FET under progressive gate biasing voltage [31]. a. below threshold, b. around threshold, c. over threshold, d. saturation

Besides the benefits on fabrication process, the device operation of junctionless FET is also effective as it is free of carrier interface scattering ideally [31, 32, 34]. In enhancement mode FET, inversion charge layer is confined close to the Si/SiO₂ interface. The carrier scattering occurs rapidly along the channel, makes the device transconductance reduce. However, in the junctionless GAA silicon nanowire FET, the current conduction channel starts to form along the center line of the nanowire body and expand to the whole nanowire with increasing gate voltage. The carrier can flow through the nanowire with nearly bulk mobility [31, 32, 34], which suffers less from the surface scattering. Less carrier surface scattering also makes the junctionless FET has extremely limited low frequency noise (LFN) level and the LFN shows no dependence on gate biasing [32].

2.2 ESD Technology

ESD is a high current, short duration event. The instant discharge current can reach several amperes but the discharging time is usually only hundreds of nano-seconds. The ESD issue is unavoidable for semiconductor device. Statistically, more than one-third of overall IC failure is attributed to ESD or electrical overstress (EOS) [37]. Advanced technology has smaller device feature size and thinner gate oxide layer, which makes the ESD induced issues, such as latch up, soft damage, local melt and hard breakdown, become even serious. The study and understanding of GAA silicon nanowire FET is urgently needed for future nanowire device based design, since the reliability and robustness of GAA silicon nanowire FET against ESD are as critical as the device performance breakthrough.

2.2.1 ESD Failure Mode

The major problems due to ESD are gate oxide breakdown and structure local melting.

Advanced CMOS technology scales down the device gate length, also reduces the gate oxide layer thickness to maintain the gate capacitance. Thinner oxide layer faces challenges of device reliability as the oxide field can easily reach high magnitude. Assuming the oxide layer strength is 2V/nm, and then even a 6V stress voltage is enough to damage a 3nm gate oxide layer. Hence, ESD stress occurs at I/O pins can induce oxide integrity failure, especially beyond

100nm node scaling [15]. The large ESD current flow through device can induce a large amount of Joule heating, local thermal runaway would occur and results device failure. The junction region in the device has high series resistance, makes the induced heat accumulate at these regions.

Figure 2.6 shows the principle ESD I-V curve. The device ESD operation region is beyond the normal operation region. The device ESD performance is determined by the constraints of oxide breakdown and thermal failure. Both mentioned problems are catastrophic damage, which is non-recoverable and the device would lost its functionality once it get damaged. Soft damage, which the damage level does not reach the catastrophic level yet, also occurs under ESD stress. The soft damaged device does not loss its functionality fully, but the performance degrades and device leakage increases [15, 38]. It is worthy to mention that such soft damage actually occurs when device operates in the safe ESD window. Hence, the ESD stress always damages or degrades the device, and completely device damage happens when stress reaches certain severe level.

Figure 2.6 The principle ESD protection design window [39]

Figure 2.7 shows an n-MOSFET configuration under ESD event and its ideal I-V curve. The ESD stress is applied on its drain contact with its source and gate both grounded, which forms a common ESD protection configuration. During the ESD event, the drain-substrate junction keeps reverse biased until avalanche breakdown happens when drain voltage reaches V_{av} . The substrate current increases and hole charge accumulates in the device substrate. Till at the drain voltage of V_{t1} , the source-substrate junction gets forward biased. The substrate parasitic n-p-n bipolar junction transistor formed by source-substrate-drain turns on, which provides an extra current dissipation path. The drain current keep increasing with drain voltage drops dramatically. The ESD current keeps dissipate until the current level reaches I_{t2} , the maximum current conduction level that the device can sustain. High ESD current flow induces high local heating generation, melts down silicon structure and damages the

junction, which causes the non-reversible, second breakdown of device. Figure 2.8 briefly describes above ESD breakdown mechanism with a cross section schematic of n-MOSFET.

Figure 2.7 ESD I-V characteristic of an n-MOSFET [40]

Figure 2.8 ESD breakdown mechanism of a gate-grounded n-MOSFET [41]

2.2.2 ESD Characterization Model

ESD characterization is relied on the ESD model development to simulate ESD events on device or in software environment. The ESD model is represented by an equivalent circuit which can generate the required ESD pulse. As the circuit representation differs with different discharging event, many ESD models were proposed and used in industry testing development now.

The human body model (HBM) is the most fundamental ESD model. This test standard was firstly documented in 1980, the latest updated version is the US military standard MIL-STD 883.C/3015.7. It represents the ESD pulse generated when a charged human being touches a component. The equivalent model circuit is shown in Figure 2.9. A pre-charged capacitor discharges its stored charge to the component through a resistor, with the capacitor $C_{HBM} = 100\text{pF}$ and the resistor $R_{HBM} = 1500\Omega$ [39]. According to the setup specification in MIL-STD standard, the resulting HBM discharging waveform should have a rising time less than 10ns and a decay time of 150ns ($\pm 20\text{ns}$). Typically, the HBM failure voltage threshold level is 5kV [39].

Figure 2.9 HBM model circuit representation

The machine model (MM) represents the ESD pulse generated when a conductive source, like machine or metallic handling tool, touches a component. The equivalent model circuit is shown in Figure 2.10. The capacitor $C_{MM} = 200\text{pF}$ and the resistor R_{MM} is treated as a very small value which usually is negligible. Due to the nature of low discharging resistance, the resulting discharging waveform is oscillatory and the rising time is only a few nanoseconds. The MM ESD is faster than HBM ESD, but the ESD protection level obtained from MM model is lower than HBM model [39]. Currently there is no official established testing standard for MM.

Figure 2.10 MM model circuit representation

HBM and MM tests are simple to conduct. Their test setup and equipment are widely accepted by industry. However, with the improvement on ESD controlled production, the ESD issue induced by human body contact or machine handling is not dominant any more [39, 42].

The charged device model (CDM) draws more concern of modern ESD characterization. Different from HBM and MM, the CDM represents the ESD pulse generated between a chip or component and the external environment through a pin discharge path. For example, electrostatic charge may build up during process due to less effective grounding, the accumulated charge will discharge through a random pin when the component touches a handler or socket. The CDM pulse rising time characterization is designed to be comparable to the protection structure response time [43], which is at only several nanoseconds.

High voltage level may easily build up across the gate oxide layer during CDM event [39, 42, 43]. Hence, gate oxide failure is the major failure

phenomena of CDM, while the major failure signature of HBM or MM is thermal runaway [39]. Due to the failure nature of CDM, it has become more widespread used in recent ESD design as its suitability in ESD characterization of advanced CMOS technology [39]. The typical CDM equivalent circuit is shown in Figure 2.11. The capacitor $C_{CDM} = 6.8\text{pF}$, the resistor $R_{CDM} = 15\Omega$ and the inductor $L_{CDM} < 1\mu\text{H}$. The CDM generates the fastest ESD pulse. The CDM also has no official established test standard. And further development on CDM is needed as the ESD robustness and sensitivity keeps changing with the shrinking device feature size and oxide layer thickness.

Figure 2.11 CDM model circuit representation

The IEC 1000-4-2 standard is a system level ESD test standard. It includes the ESD events related to equipment and system within more environmental conditions [44]. The standard defines two test procedures, contact test and air gap test. And the standard defines the test requirements for both power-off and power-on conditions. The standard test circuit is depicted in Figure 2.12. The

capacitor $C_{IEC} = 150\text{pF}$, the resistor $R_{IEC} = 330\Omega$ and the inductor $L_{IEC} \approx 0\mu\text{H}$.

Table 2.1 shows the defined severity levels of IEC 1000-4-2 standard.

Figure 2.12 Simplified IEC 1000-4-2 ESD test circuit [44]

Table 2.1 IEC 1000-4-2 severity level [44]

Level	Contact test voltage (kV)	Air gap test voltage (kV)
1	2	2
2	4	4
3	6	8
4	8	15

Figure 2.13 shows a comparison of discharging current waveforms resulting from different ESD models. The CDM has fastest pulse rising, followed by the MM and IEC standard, the HBM has the slowest pulse rising. Another point is that both MM and IEC standard have ESD stress magnitude on both polarities, and MM shows almost the same peak levels on both positive and negative stress pulse.

Figure 2.13 Simulated waveforms from different ESD models [39]

2.2.3 ESD Testing Method

Industrial ESD testing is usually conducted at the package level. In a common ESD robustness test, all I/O pins on package are stressed with respect to both power supply and ground pins. The ESD stress generates with both positive and negative polarities. The ESD test is judged based on failure current definition. If the device leakage current under certain ESD stress is lower than certain chosen failure current level, the device is considered to be robust against ESD stress at that test level.

The generation of ESD pulse is designed to use a charged coaxial transmission line as the discharging current source. The pre-charged transmission line pulse (TLP) system generates a trapezoidal current waveform for ESD testing as shown in Figure 2.14. The TLP pulse is determined by transmission line length and propagation velocity [39]. Due to the similarities between TLP test

setup and HBM, the standard TLP testing waveform usually designs in a manner of HBM waveform equivalent [39, 45, 46]. The TLP pulse width is determined based on the HBM ESD model, which in hundreds nanoseconds level, and the TLP current level is designed with corresponding estimated HBM stress level.

Figure 2.14 TLP voltage and current waveforms [45]

2.3 Semiconductor Device Failure Fundamentals

The same as any other product, the semiconductor device has its lifetime constraint and reliability issue. The IC product is aimed towards even tiny device feature size and higher integration level nowadays. It becomes almost impossible to perform re-design or re-manufacture work on a product. Hence, reliability design has been an important part in the industry IC design.

Reliability design related to semiconductor device requires essential understanding on the physical principles behind failure mechanism. Furthermore, to describe the failure mechanism in numerical representation is also important. It helps evaluate the device failure quantitatively and provides the possibility to simulate the failure process in TCAD tool.

2.3.1 Common Failure Mechanisms in Semiconductor Device

The failure in semiconductor device majorly divides into three categories, oxide related failure, junction failure and interconnect failure [47]. Oxide related failure includes gate oxide wear-out and hot carrier degradation, such as hot carrier injection and interface state trapping. Junction failure concerns the breakdown of PN junction in device. Interconnect failure is usually contributed by stress induced voiding and electro-migration (EM).

Oxide wear-out or breakdown is related to the continuous defect generation under electric stress in oxide layer [48, 49]. Massive research work focuses on exploring how the defects trigger oxide breakdown and the relation between oxide defect generation and stress condition. For the first consideration, it is widely accepted that the defect would form a conduction path across oxide layer as the defect keep accumulating [48]. This idea is briefly depicted in Figure 2.15. The defect spot randomly generates in the oxide layer. When the defect spots line up across the oxide layer, local oxide current starts to flow. This current flow generates local hot site in the oxide layer and further accelerates the defect generation, speeds up the oxide breakdown.

Figure 2.15 Defect accumulation in a MOSFET gate oxide layer [50]

Research on stress dependence evaluation relies on the experimental work. Up to now, many dependence factors are investigated experimentally, such as voltage, power, temperature, polarity and oxide thickness [48, 51-54]. It is claimed that the oxide breakdown has direct relation with the stress condition. However, the oxide breakdown is not a deterministic phenomenon [54]. It does not only mean the experimental characterization is not easily reproducible, but also suggests the difficulties of analytical breakdown modeling. Due to the intrinsically random nature of breakdown mechanism, many attempts on building statistics based framework of breakdown physics are proposed [55-58]. One commonly used statistical model is the Weibull distribution as it models the weakest point scenario which is similar to the oxide breakdown path formation [57-59]. Multi-dimensional analytical model is also proposed based on this Weibull distribution methodology and finite element method as shown in Figure 2.16 [57]. The experimental dependence factors are treated as statistical fitting parameters in these models.

Figure 2.16 Schematic of analytical oxide defect generation model [57]

Hot carrier degradation refers hot carrier induced oxide degradation and interface state generation, also includes negative bias temperature instabilities (NBTI) effect for pMOS device. Hot carrier, both electron and hole, refers to the carrier gains large kinetic energy under high electric field region [60-62]. When the carrier energy is significantly larger than lattice thermal equilibrium energy, the carrier considers as hot carrier. Hot carrier can inject into gate oxide layer and cause interface damage [61, 62]. Hot carrier can result performance instabilities and device parameter roll-off, which makes it as a major reliability design concern of high operating electric field device. Generally, the gate oxide region, substrate region and Si/SiO₂ interface of channel region are the common regions suffer from the hot carrier degradation. More physical theory background on hot carrier injection and interface state generation is introduced in the coming sub-sections.

Junction failure is mainly induced by device overstress, like latch-up, ESD and EOS. The failure mechanism of ESD is introduced in previous section. Device latch-up and EOS failure share some similarities with ESD failure. Latch-up

refers the parasitic substrate BJTs formation in common CMOS structure [63]. As shown in Figure 2.17, the *pnp* and *nnp* parasitic BJTs both turn on and the base of *pnp* BJT connects to the collector of *nnp* BJT. A positive feedback loop is then formed as this configuration usually has a gain larger than one. In this manner, the latch-up starts and the current flow tends to overshoot in the end. EOS is also an over-voltage and over-current event as ESD, the only difference is the EOS occurs over longer time scale, usually over 1ms duration [64].

Figure 2.17 Schematic of latch-up mechanism in CMOS [63]

Interconnect failure is discussed more on backend failure characterization. The dominant failure mechanisms are EM and stress voiding [50]. EM happens under high current density condition. The conducting ion performs momentum transfer with carrier, which results the conducting atom movement [65, 66]. Furthermore, EM is closely related with the lattice inhomogeneity and grain size variation of conducting material. Atom accumulation occurs when in-flux is higher than out-flux at grain junction point while atom depletion occurs in

the reverse manner [66]. EM results voids or spiking in the metallization routing and interconnect via structure. Stress induced voiding is another metallization failure mechanism. After high temperature processing, high tension stress exists in metal interconnect due to the thermal expansion coefficient mismatch between metallization and surrounding material [50, 66]. The residual stress relaxes by diffuses the tiny void spots in structure. And this diffusion results the accumulation of voids, which leads metallization breakdown.

2.3.2 Hot Carrier Injection Fundamentals

The most discussed hot carrier is the channel hot carrier [50]. Channel hot carrier can generate in both conducting channel and non-conducting channel. It is widely accepted that channel hot carrier damage experience three stage process: gaining high kinetic energy, carrier injection or impact and oxide damage or interface trapping [50, 61].

Carrier gains energy when accelerates in high channel field or experience energy transfer under redistribution process [67-69]. Under the high drain bias condition, carrier can gain energy after passing the pinch-off point due to the large voltage drop across the pinch-off region. In deep scaled channel length, hot carrier may generate not only in the pinch-off region. With the effect of high lateral electric field, carrier in pinch-off region can be in energy non-equilibrium state [50, 69]. Non-equilibrium energy distribution usually makes carrier obtain energy larger than lattice thermal equilibrium energy, or even silicon bandgap energy. This leads the energy redistribution process between

carrier, such as carrier-carrier scattering and carrier-phonon scattering. Carrier-carrier scattering is the carrier energy exchange process due to Coulomb interaction [70]. The direct Coulomb interaction, which is a more common Coulomb interaction, occurs between single carrier particles. For two single carriers involve in direct Coulomb interaction, one carrier is able to transfer all its kinetic energy to the other one, which creates carrier with even higher energy in the system. The carrier-phonon scattering process is another high possibility energy redistribution process. The carrier can lose energy by emitting out a phonon; also can gain extra energy by absorbing a phonon [71].

Another phenomenon related to hot carrier energy is impact ionization. It can be treated as a special carrier-carrier scattering event. High energetic carrier is able to break silicon valence bond and produces high energy electron-hole pairs [50, 72]. Through continuous Coulomb interaction process, energetic carriers keep generates and also the impact ionization generation does.

Most hot carrier is collected by drain. But some carriers can impact or inject towards interface with sufficient energy. One major injection mechanism is due to the vertical field along the channel, especially in the pinch-off region [50]. Actually, the hot carrier injection mechanisms are closely related to the hot carrier generation mechanisms. Besides the high field injection scheme, another major injection mechanism is the avalanche hot carrier injection, which is contributed by the hot electron-hole pairs from impact ionization. And this mechanism more likely occurs in the drain region [50]. Multi-step hot carrier injection mechanism is also identified as a major injection mechanism. It describes the hot carrier injection due to hot carrier generation from multi-step carrier-carrier scattering [50, 73].

Hot carrier damage mechanisms are charge injection and interface state generation. It is confirmed that the device degradation or failure is related to the hot carrier induced damage. However, the damage localization makes this relation become indirect and complicated [60, 62]. Hot carrier damage mechanism highly depends on hot carrier generation and bias condition. Hot carrier with kinetic energy higher than Si/SiO₂ barrier is able to inject into oxide layer [50]. These injected carrier forms oxide defect spot and oxide charge. The other damage mechanism, interface state generation, is expressed in the next sub-section separately.

2.3.3 Interface State Generation Kinetics

Interface state generation is the dominant damage mechanism in advance technology [50, 74]. Interface state is a trivalent silicon atom at silicon interface with an unpaired valence electron. The reaction of interface state generation starts with the Si-H bond breaking, then the diffusion of hydrogen ion away from Si/SiO₂ interface. H species can re-combine with the unpaired silicon bond. Hence, the interface state generation is a dynamic balance process between Si-H bond breaking and unpaired silicon bond repassivation with H [50]. Interface state is electrically active damage. In n-MOSFET, the major interface state type is negatively charged, acceptor type interface state. Oppositely, the major type in p-MOSFET is donor type interface state with positive charge.

As stated above, the interface state generation is carried out by the hot carrier injection and hot carrier avalanche stressing. However there is still no

unanimous agreement on this degradation mechanism in spite of the massive research effort on this topic over the past several decades. The interface state induced degradation is also difficult to evaluate as it lacks of experimental support on the interface damage induced by carrier injection [60, 74]. Even with the advanced charge pumping technique, which provides more information on the interface state generation properties [75], the evaluation of interface state degradation is still only based on the device characterization result.

The physical model proposed in [61] summarizes the degradation mechanism for the first time. For an n-MOSFET, the degradation is dominated by acceptor type interface state generation at a narrow band near drain. The charged interface state impacts the channel carrier distribution and mobility, results device performance degradation. And it suggests that the hot carrier which can induce interface state would have the kinetic energy at least of 3.7eV. It also mentions about the Si-H bond break scenario as shown in Figure 2.18. If the hydrogen atom diffuses away from interface after the bond break up, a new interface state is formed as a dangling bond.

Figure 2.18 Interface state generation and Si-H bond break

This degradation threshold energy mechanism faces challenges when applying it on the explanation of low operating voltage, submicron device degradation [60]. Also the research on giant isotope effect extends the Si-H bond degradation modeling to Si-D (Deuterium) bond [76]. An updated physical model describes the degradation mechanism as desorption process of Hydrogen or Deuterium, while the depassivation process is treated as directly triggered by hot carrier. Further research using scanning tunneling microscopy (STM) technique suggests even advanced desorption mechanisms [60]. The first mechanism is consistent with the traditional bonding-antibonding theory, but latest theoretical and experimental research suggests a lower threshold energy level for degradation. The other degradation mechanism argues the bond breaking can occur in a vibrational mode which induced by multiple hot carrier impacts [50, 60, 74]. The second mechanism suggests an even lower threshold energy level (from 67meV to 290 meV) for single hot carrier [50]. It is believed that the mechanism of bond vibrational mode is more dominant in the low operating voltage degradation.

2.4 Random Dopant Fluctuation Fundamentals

The rapid development of semiconductor industry relies on the ability to shrink device feature size. As the device getting even tiny, the variability issue associate with device fabrication becomes a challenge. The random variation problem is firstly discussed in the sensitivity problem of PN junction breakdown voltage [77]. The statistical fluctuation of acceptor and donor atoms in junction results the variation of junction breakdown voltage. More

recent research work focuses on the sensitivity of device threshold voltage [78, 79].

The most discussed variability source factors are line edge roughness (LER), oxide thickness fluctuation (OTF) and random dopant fluctuation (RDF). LER is the gate edge shape distortion as shown in Figure 2.19. As the LER variation does not scale down with the device feature size. The LER induced variability problem draws much attention, especially in the memory cell design [80]. Both silicon experiment data and analytical modeling suggest the LER significantly increase the device leakage and threshold mismatch. OTF focuses more on the roughness of Si/SiO₂ interface, which is the fluctuation of gate oxide thickness. Similar to LER, OTF also introduces more challenge as the device feature size scaling down. Both silicon and oxide interface have an intrinsic fluctuation magnitude of 3Å [81]. This variation is independent to local oxide thickness, hence brings severe impact when device gate oxide thickness scales down to sub 2nm level. Some latest research also discusses the OTF of high-k gate dielectric material. The interface property of high-k/SiO_x even complicates the OTF problem.

Figure 2.19 Definition of LER effect

RDF is identified as the most significant variation source of semiconductor device [79-81]. RDF is caused by the random placement of discrete dopant atoms. As the device keep scaling down, the total number of dopant atoms decreases as shown in the trend plot in Figure 2.20. There are less than 100 dopant atoms in channel region for a 45nm technology device. The reduction of dopant atoms in device structure results in dramatic increase of threshold voltage variation as the device parameter becomes sensitive to the dopant atoms placement. For common MOSFET, the RDF is further classified into body RDF and source/drain RDF as the dopant types for these regions are different. Body RDF is treated as the dominant RDF source since it determines the variation in device channel. Source/drain RDF majorly contributes the variation of effective device channel length and overlap gate capacitance.

Figure 2.20 Threshold voltage variation trend upon device down scaling trend [82]

The discrete dopant atom placement follows Poisson distribution associate with lattice grid [16, 78, 82-84]. This theory background provides the possibility to numerically model the RDF. Three-dimensional atomistic simulation based on kinetic Monte Carlo [16] or analytical dopant placement method [85] is proposed to study the statistical property of RDF. High accuracy device RDF simulation still needs further research effort on the analytical model fitting with actual silicon data, as the purely analytical RDF modeling cannot satisfy the needs of device compact modeling.

2.5 Technology Computer Aided Design in Semiconductor Device Analysis

The complexity of semiconductor process and device physics increases dramatically in the advance technology. It is difficult to perform essential first principle analysis on semiconductor device, however, further compact device modeling needs physics driven modeling result. The technology computer aided design (TCAD) becomes an effective solution as it takes the advantages of powerful numerical computing resource on solving the complex device physics equations, also its physical approach provides excellent accuracy from its modeling simulation. In the industry, TCAD is widely used as fast turnover and low cost solution for semiconductor technology research and development. TCAD includes two major branches, process simulation and device simulation [86].

Chapter 2 Literature Review

In TCAD process simulation, the fabrication steps, such as deposition, etching, implantation and annealing, are simulated based on process physics equations. Multi-dimensional device structure can be built by defining complete process step commands. Physical parameters from the device fabrication process can be extracted for further optimization usage. Also external calibration data can be imported to make process simulation to be more comparative to the real process.

Device simulation characterizes the device virtually in TCAD environment. Device used in simulation has to be a meshed, finite element based structure. Based on the given device structure, plus proper boundary condition definition, device physics model definition and numerical simulation parameter plugin, a TCAD device simulation is modeled. The basic result extracted from device simulation is the electric representations, such as current, voltage, charge and field. Furthermore, the result related to device physics can also be extracted, such as trap concentration, impact ionization generation and band structure. Multiple simulation modes, such as static, transient and AC, are supported in commercial TCAD environment. Also various device physics models are provided in TCAD for essential study.

As a physical driven, numerical based analysis method, TCAD is sensitive to the finite element structure used in simulation and the mathematics engine used in numerical analysis. The accuracy, efficiency and robustness of TCAD modeling analysis are difficult to achieve, especially for the 3D device modeling.

Chapter 2 Literature Review

Details on the TCAD simulation setup and physics theories related to simulation modeling in this project are going to be introduced in separate sections of the following chapters.

2.6 Summary

The development background on nanowire device is reviewed in this chapter. The ESD knowledge, which related to the major topic in this project, ESD modeling, and the hot carrier induced device degradation mechanisms are then introduced. The physics background of RDF is also reviewed briefly in this chapter.

Chapter 3 Electric Modeling of GAA Silicon Nanowire FET

This whole project is aimed to model GAA silicon nanowire FET using TCAD, but different chapters will focus on different aspects or topics related to GAA silicon nanowire FET. As stated in the TCAD introduction section, the electrical characterization modeling is the most fundamental part of TCAD device modeling. The author builds the GAA silicon nanowire FET simulation model from the scratch in TCAD. The device fabrication of GAA silicon nanowire FET is essentially discussed recently. However, there are very few discussions on the GAA silicon nanowire FET modeling in commercial TCAD environment. Moreover, the thermal factor and stress-strain factor are taken account into the device modeling while most of the device electrical behavior modeling work doesn't include the consideration of these factors. An accurate, robust GAA silicon nanowire FET model is important to the whole project, since it is the starting point of the ESD event modeling and RDF effect modeling in the next project phases.

This chapter introduces the basis of whole project, the front-end process modeling and numerical device characterization of GAA silicon nanowire FET. And this chapter is organized as follows: the theoretical background about device modeling of GAA silicon nanowire FET is introduced firstly. Then process simulation flow and device simulation result are present. Lastly, a comparison study between GAA silicon nanowire FET and FinFET is present to evaluate the advantages of GAA nanowire device.

3.1 Theoretical Background

The theoretical background introduction of GAA silicon nanowire FET device modeling covers the carrier transport physics, self-heating effect and process induced stress effect.

3.1.1 Carrier Transport Fundamentals

The electric current flow in semiconductor device is actually the charge carrier, electron and hole, transport in the active region of semiconductor device. Based on the charge conservation rule, the carrier transport is governed by the continuity equation [87],

$$\begin{cases} \nabla \cdot J_n = qR_{net} + q \frac{\partial n}{\partial t} \\ -\nabla \cdot J_p = qR_{net} + q \frac{\partial p}{\partial t} \end{cases} \quad (3.1)$$

where J_n and J_p stand for electron and hole current density, n and p stand for electron and hole carrier density, R_{net} is the net carrier recombination rate.

Basically, the electric characterization of semiconductor device is obtained by solving the carrier current density. Different carrier transport models have different approach to calculate the carrier current density.

The most fundamental carrier transport model is the drift-diffusion model. It is simple to solve but it is limited to isothermal and low field condition [87]. Under low electric field, carrier velocity is proportional to field,

$$v = \mu \mathcal{E} \quad (3.2)$$

where μ is the carrier mobility.

Carrier flow introduces excess carrier locally. When carrier concentration gradient exists, carrier diffuses from high concentration region to low concentration region in order to achieve uniform carrier distribution in system [87]. This carrier flux follows Fick's law,

$$\frac{d\Delta n}{dt} = -D_n \frac{d\Delta n}{dx} \quad (3.3)$$

where D_n is the carrier diffusivity.

Drift-diffusion model combines field drift transport and diffusion transport,

$$\begin{cases} J_n = q\mu_n n\mathcal{E} + qD_n \frac{dn}{dx} \\ J_p = q\mu_p p\mathcal{E} - qD_p \frac{dp}{dx} \end{cases} \quad (3.4)$$

where $D_{n,p} = \frac{kT}{q} \mu_{n,p}$ is the Einstein relation in non-degenerate semiconductor [87].

In classical drift-diffusion model, the carrier mobility μ is constant. This assumption becomes less valid when device geometry is small as the carrier energy affects carrier mobility [86]. Hydrodynamic transport model is an improved drift-diffusion model with coupling energy transport.

Beyond the charge conservation, the local energy conservation is added into consideration. Based on energy flux balance [86, 88], and taking electron energy as example here, we have

$$\frac{dE_{nx}}{dx} = \frac{J_{nx}\mathcal{E}}{q} - \frac{nk}{q} \cdot \frac{\Delta T_n}{\tau_E} \quad (3.5)$$

where ΔT_n is the excess electron temperature, τ_E is the carrier energy relaxation time. The left-hand-side (LHS) is the energy flow rate. The first term of right-hand-side (RHS) is inflow energy rate and the last term of RHS is the carrier energy dissipation rate. By plugin the local energy flow data, the carrier current density induced by carrier temperature can be solved. In some analytical analysis, the energy term is treated as a determine factor of carrier mobility [89]. In TCAD simulation environment, the energy term is treated as an extra term to form the carrier current density.

The hydrodynamic model provides better approach for device feature size smaller than 100nm [86]. However, it brings extra numerical complexity in simulation solving. Also, the model assumptions about carrier energy relaxation, scattering and closure require further calibration work to validate.

3.1.2 Self-heating Effect in Semiconductor Device

In semiconductor device, thermal energy could be generated and dissipated during operation. The self-heating during normal operation and rapid thermal runaway can degrade device performance severely and also bring reliability issue.

A simple thermal energy generation model for semiconductor device can be expressed as,

$$H = J \cdot \varepsilon + R \cdot E_g \quad (3.6)$$

where J is the device current density, ε is the electric field, R is the net recombination rate and E_g is the semiconductor bandgap. The first term of

RHS is the Joule heating resulted from the device resistance. The second term of RHS is the heat dissipation by the carrier recombination process [90].

In semiconductor, the bulk mobility of carrier μ_b can be expressed as,

$$\frac{1}{\mu_b} = \frac{1}{\mu_{Lat}} + \frac{1}{\mu_{DAeh}} \quad (3.7)$$

where μ_{Lat} represents the carrier lattice scattering and μ_{DAeh} represents the scattering induced by other bulk scattering mechanisms. In most case, the first term of RHS contributes more to the bulk mobility.

For μ_{Lat} , it takes the form,

$$\mu_{Lat} = \mu_{max} \left(\frac{T}{300K} \right)^{-\theta} \quad (3.8)$$

where T is the lattice temperature. μ_{max} is the saturation carrier mobility, $\mu_{max,e}$ is 1417 cm²/Vs and $\mu_{max,h}$ is 470 cm²/Vs. θ is a model parameter, θ_e is 2.285 and θ_h is 2.247 [86].

Under higher temperature condition, the carrier mobility is lower. Experimentally, the device on-state resistance raises and the current driving capability reduces. Moreover, as the heat generation and dissipation in device structure are not uniform. Extremely high local temperature rising may occur during high level transient thermal energy generation. The accumulated transient thermal energy can melt the device structure, results catastrophic damage in the device.

3.1.3 Stress Effect in Semiconductor Device

Mechanical stress in semiconductor can affect band structure, carrier mobility and dielectric leakage [91]. In conventional CMOS fabrication, stress can be raised from many sources, such as different process temperature, different process mechanisms and mismatch of material thermal expansion coefficient. Usually, the process induced stress residual in device structure is not uniform.

Basically, the stress tensor $\vec{\sigma}$ is represented by a 3×3 symmetric matrix,

$$\vec{\sigma} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{xy} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{xz} & \sigma_{yz} & \sigma_{zz} \end{bmatrix} \rightarrow \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} = \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} \quad (3.9)$$

where it has six independent matrix components. Hence it always simplifies the stress tensor matrix into a six component vector notation.

To compute the strain tensor $\vec{\epsilon}$ in semiconductor based on the stress tensor, from Hooke's law [92],

$$\epsilon = \sum_{i=1}^3 \sum_{j=1}^3 S_{ij} \sigma_{ij} = \sum_{k=1}^6 S_k \sigma_k \quad (3.10)$$

where S_{ij} is the corresponding component of elastic compliance tensor. The elastic tensor can also be simplified as stress tensor, hence the strain calculation can perform further index contraction.

Also, following contraction rules are used for ϵ ,

$$\epsilon_p = \begin{cases} \epsilon_{ij} & (p < 4) \\ 2\epsilon_{ij} & (p > 3) \end{cases} \quad (3.11)$$

The ε_4 , ε_5 and ε_6 are engineering shear-strain components and related to the double subscripted shear components [92].

In crystals with cubic symmetry, by performing coordinate system rotation, the crystal system can be set in parallel to the symmetric axis of crystal. The number of independent components of material property tensors can be further reduced to three. For example, the elastic compliance tensor can be simplified as,

$$\vec{S} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \quad (3.12)$$

where the coefficients S_{11} , S_{12} and S_{44} are the parallel, perpendicular and shear components respectively.

In TCAD process simulation, the process induced stress computation is performed in four steps [86]. Firstly, the mechanics computation equations are defined. Secondly, the computation boundary condition is defined. Thirdly, the material properties are defined. Lastly, the driving mechanics of stress computation are identified. The major mechanics are intrinsic stress, thermal mismatch, lattice mismatch and material growth. In simulation content, all these mechanics are forced to stick in linear elastic regime.

3.2 Front-end Process Simulation of GAA Silicon Nanowire FET

GAA silicon nanowire FET uses a floating silicon body in scaled wire shape as the conducting channel, the oxide layer and gate material wrap around the nanowire to form the device. In this project, the GAA silicon nanowire FET device geometry is generated by using Sentaurus Process with MGoals3D library [86]. The process simulation steps are given in Table 3.1 and the steps are similar to the actual fabrication process discussed in [6-10]. The device pseudo-3D geometry structures of some key steps are shown in Figure 3.1. In actual device fabrication, the nanowire is generated through lithography patterning and high temperature hydrogen trimming [6-8]. However, the dry gas trimming process is not yet supported in Sentaurus Process. The nanowire body in simulation is formed by using external geometry insertion powered by Sentaurus Device Editor [86].

Table 3.1 Process simulation steps for GAA silicon nanowire FET generation

a	Wafer preparation
b	Nanowire patterning, trimming
c	Gate oxide formation
d	Gate material deposition
e	LDD implantation
f	Nitride spacer deposition
g	Source/drain deep implantation
h	Thermal annealing
i	Contact formation

Figure 3.1 Device geometry in different process steps. a. nanowire patterning, b. gate oxide deposition, c. gate definition, d. spacer formation, e. doping generation, f. final geometry

The radius of the intrinsic doped nanowire channel is 5nm and the nanowire doping level is $1 \times 10^{15} \text{ cm}^{-3}$ p-type. The source/drain doping is achieved by lightly doped drain (LDD) implantation and deep implantation after the gate stack formation. The tunable metal gate is achieved by defining the gate contact workfunction in the novel geometry. The meshed device geometry for simulation is shown in Figure 3.2 with boundary conforming geometry mesh applied in order to model the device behavior properly and also to enhance the numerical robustness and effectiveness of the simulation. The simulation geometry dimensions and parameters are summarized in Table 3.2.

Figure 3.2 Boundary conforming meshed GAA silicon nanowire FET (half slice)

Table 3.2 Device dimensions and key parameters used in simulation

Nanowire radius	5nm
Gate length	25nm
Gate oxide thickness	3nm
Channel doping concentration	$1 \times 10^{15} \text{cm}^{-3}$ Boron
LDD implantation dose	$2 \times 10^{14} \text{cm}^{-2}$ Arsenic (nMOS)
	$1 \times 10^{14} \text{cm}^{-2}$ Boron (pMOS)
Source/drain deep implantation dose	$6 \times 10^{15} \text{cm}^{-2}$ Phosphorus (nMOS)
	$3 \times 10^{15} \text{cm}^{-2}$ BF2 (pMOS)
Annealing temperature	950°C
Gate contact workfunction	4.4eV (nMOS)
	4.9eV (pMOS)

3.3 Numerical Device Simulation of GAA Silicon Nanowire FET

The 3D device simulation is performed using Sentaurus Device. In order to characterize the device electrical performance accurately, it is important to define the carrier transport with proper models.

The most fundamental model is the drift-diffusion carrier transport model. For submicron device simulation, the hydrodynamic transport model is commonly used to account for the carrier energy in the carrier transport [86]. The suitability of using hydrodynamic model for sub-50nm device is still in debate since the carrier transport in such small devices is in near ballistic behavior [13, 93]. There is an argue that hydrodynamic model produces the carrier velocity overshoot only with the drift energy even entering the ballistic regime, which may overestimate the drain current level [13, 93].

On the other hand, the quantum mechanical effect in the deep scaled device may not be negligible. This is because the silicon nanowire device works in full depletion mode, and the induced inversion charge layer thickness in the conducting silicon nanowire channel is comparable to the nanowire dimension. Therefore, the quantization effect model needs to be included in the device simulation. Density gradient model is a quantization correction model for 3D device simulation which is supported in the Sentaurus Device. Compare to other available quantization models, such as van Dort model, 1D Schrödinger solver and modified local density approximation (MLDA), the density gradient model shows better physical accuracy and numerical robustness as it is the only approach has self-consistent capability with the carrier transport solver [12, 86, 94].

Figure 3.3 shows the comparison of the drain current versus drain voltage characteristics of an n-type nanowire FET at 1V gate bias voltage simulated using drift-diffusion (DD), hydrodynamic (HD) and density gradient (DG) models respectively. A Monte Carlo (MC) carrier transport simulation with full specular scattering is conducted as ballistic transport benchmark simulation. Monte Carlo simulation solves the carrier transport based on the possibilities of carrier collision events rather than modeling the carrier distribution. This fundamental physical approach can model the ballistic transport closely and requires less calibration. The surface roughness is set to 100% specular scattering and 0% diffusive scattering which switches off all the scattering mechanisms along the channel and produces the device performance characteristics at ballistic limit [86, 95, 96]. This fully ballistic Monte Carlo simulation provides the upper limit of the device performance [96]. The Monte Carlo simulation in Sentaurus Device is a post-processing simulation methodology, and it consumes a lot of computing resource.

Figure 3.3 GAA silicon nanowire FET I_d - V_g characteristics using different carrier transport models

One can see that hydrodynamic model not only produces much higher drain current than the classical drift-diffusion model, but also yields higher current over the Monte Carlo simulation result. In other words, the hydrodynamic model overestimates the drain current level severely since the ballistic limit simulation provides an upper limit drain current estimation. The density gradient model help suppress down the drain current in both drift-diffusion and hydrodynamic cases.

Figure 3.4 and Figure 3.5 present the majority carrier distribution in cross section at the center of the nanowire. We can see that both the drift-diffusion and hydrodynamic models wrongly estimate the carrier density distribution near the semiconductor-oxide interface because the peak of carrier concentration cannot be at the interface due to the quantum well effect [12].

On the other hand, drift-diffusion transport with density gradient correction shows a reasonable carrier concentration, showing the necessity to include the quantum effect in the modeling.

Figure 3.4 Carrier density distribution at the center cross section of nanowire (upper left: DD, upper right: HD, lower left: DD+DG, lower right: HD+DG. Bias condition: $V_g=1.0V$, $V_d=1.0V$)

Figure 3.5 Carrier density profiles along the z-axis cut of center cross section

Figure 3.6 and Figure 3.7 present the majority carrier velocity profiles along the center line of the nanowire channel. The study in [93] benchmarks the conventional drift-diffusion and hydrodynamic models against the ballistic result in the sub-micron device scale. It argues the overestimation of on-state current produced by hydrodynamic model as compared to the ballistic limit, which has exactly agreement with the drain current characterization result as shown in Figure 3.3. The hydrodynamic model overestimates the carrier velocity since it models carrier velocity overshoot only with carrier temperature without setting the ballistic limit [13, 89, 93].

Figure 3.6 Carrier velocity distribution of the middle cut section of nanowire (upper left: DD, upper right: HD, lower left: DD+DG, lower right: HD+DG. Bias condition: $V_g=1.0V$, $V_d=1.0V$)

Figure 3.7 Carrier velocity profile along the center line of nanowire

Hence, in this project, the drift-diffusion model with density gradient quantization correction model is selected, as this set estimates the carrier transport in nanowire channel in the most reasonable manner.

As stated in previous section, the carrier mobility is highly related to the lattice scattering and carrier-carrier scattering. They both are affected by the lattice temperature, and this renders the electrical performance of semiconductor device to vary with temperature. The scaled GAA configuration and the poor thermal conductivity of the gate stack material tend to confine the heat dissipation along the nanowire channel, which results in an increasing channel temperature. Therefore, thermal energy transfer and self-heating effect should be included in the device modeling. Figure 3.8 shows the drain current versus gate voltage plot comparison between the carrier transport with and without thermal effect coupling. One can see that the thermal factor does impact the device electrical performance, and the off current level has a three times increase with thermal factor coupled as shown in the enlarged plot in Figure 3.8.

Figure 3.8 I_d - V_g comparison between the models with and without self-heating effect coupling

The lattice residual stress-strain affects the band structure and carrier mobility. The thermo-mechanical stress in the structure is induced from the fabrication process steps, and the process simulation can calculate and record the stress profile induced by the deposition, etching, implantation and thermal annealing steps. Figure 3.9 shows the component of stress distribution along the nanowire after the fabrication steps. The effect of mechanical stress-strain is described by deformation potential model and mobility enhancement model in the device simulation [86]. Figure 3.10 shows the comparison of the drain current versus gate voltage plot with and without applying stress-strain profile in the structure. Residual mechanical stress-strain in the nanowire enhances the device electrical performance such as drain current and transconductance, although the improvement is not so significant in the simulation.

Figure 3.9 Process induced stress distribution along the nanowire

Figure 3.10 I_d - V_g comparison between the models with and without stress effect coupling

From the above calculations, we can see that the thermo-mechanical stress enhances the electrical performance while the increasing temperature degrades the current level, and that the thermal effect impact on the electrical performance is more than that due to the mechanical stress factor. Under normal operation, the device temperature increases by only several degrees according to the simulation and thus its effect can even be neglected. However the device temperature can reach hundreds of degree if high level current injection occurs under the condition of ESD for example, and this can result in severe carrier mobility degradation which seriously impacts the device transconductance and on-state current.

3.4 Comparison Study Between GAA Silicon Nanowire FET and FinFET

The multi-gate configuration of FinFET also provides enhanced channel width and effective gate control, and it is a promising candidate for deep scaled device. With the modeling of GAA silicon nanowire FET established above, we would now to make comparison of the GAA silicon nanowire FET with a FinFET structure with the same device structure dimensions and doping level. This comparison is aimed to examine whether GAA silicon nanowire FET is significantly better than FinFET. Both n-type and p-type FET are built for both device configurations and the parameters used in FinFET process simulation are set according to [97]. Figure 3.11 shows both GAA silicon nanowire FET and FinFET geometries.

Figure 3.11 Geometry comparison between FinFET and GAA nanowire FET

Figure 3.12 and Figure 3.13 show the drain current versus gate voltage plots at both linear operating condition (at drain voltage of 0.05V) and saturation operating condition (at drain voltage of 1V). Figure 3.14 and Figure 3.15 show the drain current versus drain voltage plots at several different gate bias voltage levels. Table 3.3 summarizes some key device parameters for both FETs.

Figure 3.12 I_d - V_g characteristics comparison between n-type GAA nanowire (NW) FET and FinFET

Figure 3.13 I_d - V_g characteristics comparison between p-type GAA nanowire (NW) FET and FinFET

Figure 3.14 I_d - V_d characteristics comparison between n-type GAA nanowire (NW) FET and FinFET

Figure 3.15 I_d - V_d characteristics comparison between p-type GAA nanowire (NW) FET and FinFET

Table 3.3 Device parameters comparison between GAA nanowire FET and FinFET

	I_{on} (mA/ μ m)	I_{off} (nA/ μ m)	gm (S/ μ m)	SS (mV/dec)	DIBL (mV/V)	R_{on} (k Ω)	I_{on}/I_{off}
FinFET - nMOS	2.13	32.8	42.9	73.161	69.2	12.02	6.477E+04
GAA NW FET - nMOS	1.64	8.95	24.5	61.911	9.7	11.14	1.823E+05
FinFET - pMOS	1.95	70.1	37.1	-79.505	95.3	13.71	2.778E+04
GAA NW FET - pMOS	0.817	3.87	12.4	-62.430	10.6	21.14	2.109E+05

From the above simulation results, we can see that GAA silicon nanowire FET shows much smaller subthreshold swing level (almost ideal value of 60mV/dec) and DIBL as compared to the FinFET, and it also has much lower off-state current level as compare to FinFET. This shows that GAA silicon nanowire FET provides better gate controllability and short channel effect immunity. The lower off-state current of GAA nanowire FET is a result of the intrinsic doping of the nanowire channel which is much lower than the doping level of FinFET substrate, as the FinFET still has the well implantation step as the normal planar device. On the other hand, the GAA silicon nanowire FET yields limited on-state current level than the FinFET, and this is because of the scaled floating nanowire channel and low channel doping that limit its current driving capability. As a result, its transconductance (gm) is also smaller as compared to FinFET. However the on-/off-state current ratio of GAA silicon nanowire FET is much higher than that of the FinFET. This, together with the much lower off current level and near ideal sub-threshold swing are desirable for future low power circuit applications.

3.5 Summary

In this chapter, the modeling of GAA silicon nanowire FET is discussed. We show the inappropriateness of the hydrodynamics model in describing the carrier transport in GAA silicon nanowire FET, and the necessity of including the density gradient correction method in the drift-diffusion model as the quantization effect of the carrier transport in GAA silicon nanowire FET is significant. We also show the necessity of coupling the thermal effect in the device simulation, especially in the off-state current calculation. With the device simulation model established for GAA silicon nanowire FET, we show its good gate controllability, good short channel effect immunity, very low off-state current and high on-/off-state current ratio as compared to a commercial FinFET model, and these advance features are highly desirable for future low power circuit applications. The GAA silicon nanowire FET model with both process simulation modeling and device modeling is used in the study of ESD modeling and RDF effect modeling.

Chapter 4 ESD Modeling of GAA Silicon Nanowire FET

From the discussion of chapter 3, GAA silicon nanowire FET is indeed a promising candidate for future scaled silicon based devices, as it possesses enhanced electrical performances and good immunity against short channel effect. However the gate-all-around structure plus the poor thermal conductivity of gate stack material tends to confine the heat dissipated from the device itself, renders high device local temperature and impact its performances and reliability.

The scaled feature size makes the device to operate in high field condition and the gate wrap configuration increases the ratio of Si/SiO₂ interface area to nanowire body volume. This renders the device especially susceptible to Si/SiO₂ interface related failure mechanism, and in particular vulnerable to ESD stress condition. Recent experimental works demonstrated that the ESD damaged GAA silicon nanowire FET degrades significantly and some of the nanowires even burnout and melt due to the dramatic increased local hotspot temperature [98, 99].

In this project, TCAD Sentaurus is used to reproduce the ESD experimental test through simulation modeling. On one hand, we seek theoretical explanation for the reported experimental observation; and on the other hand, to deepen our understand of the degradation physics of GAA silicon nanowire FET due to ESD stress, so as to shed light on the improvement in the requirement of ESD protection circuits for GAA silicon nanowire FET circuit in the future, with respect to ESD stress which is inevitable.

This chapter is organized as follows: the TCAD methodologies related to ESD simulation and interface degradation are introduced in the first place, which followed by the simulation setup in detail and also the simulation result. Finally, the failure mechanism and degradation analysis are presented.

4.1 Simulation Methodology

This TCAD simulation methodology section covers several key points related to ESD simulation approaches in TCAD environment and the background of numerical simulation method of interface state generation.

4.1.1 ESD TCAD Simulation

Compare to normal device characterization simulation, ESD simulation is stressing the device out of the normal operation region. High current density and high device temperature are expected in the ESD simulation. Hence, extra physics models need to be added into simulation, and the numerical setup also needs different adjustment.

As introduced in chapter 3, the drift-diffusion transport model, density gradient model, temperature computation and stress-strain computation are all the basic models for GAA silicon nanowire FET. Besides all these, below models also must be included to calibrate the ESD simulation: a) Fermi statistics. The default Boltzmann statistics is not suitable when local carrier density exceeds $1 \times 10^{19} \text{cm}^{-3}$ [86] which may occur during high ESD current injection. b) Updated carrier mobility model. The basic mobility model used in

simulation is the Philips unified mobility model [100, 101]. It already includes the mobility temperature dependence, carrier-carrier scattering, ionized impurities screening and impurities clustering. In ESD simulation, the high electric field mobility saturation model is added. Also the surface mobility degradation model due to high electric field, as known as the Lombardi model [102], is included. c) The temperature depended and doping concentration depended carrier recombination model. d) Avalanche generation models. The University of Bologna impact ionization model (UniBo model) [103, 104] is used as this model calibrate the avalanche generation over a large range of temperature condition. e) Thermodynamic model with absolute thermo-electric power computation. Only include temperature calculation is not enough in ESD simulation, the thermodynamic model is needed to catch the possible hotspot movement.

In simulation practice, the ESD simulation shows the difficulty to obtain convergence. Large current injection makes the RHS value of model PDEs (partial differential equation) to be a large value. It results simulation termination or fail to converge in defined iterations. To solve this issue, the RHS factor of simulation is set to a very large number, 10^{50} in our model which allows the RHS value oscillates in large range. The maximum solve iterations is also set to larger value, 200 in our model compare to 20 in normal characterization simulation, which gives the simulator more chance to solve the model in every step.

Also special simulation setup is used in ESD simulation. During ESD pulse stressing, a small voltage step change can result a large current step change at the contact node of ESD stress applied. A series resistor is connected to that

contact as shown in Figure 4.1 during the ESD simulation. This requires mixed signal mode enabled in TCAD setting. Thus the current flow through that external contact is regulated down to a much smaller value. Better convergence can be achieved as the voltage and current now have comparative step change. Usually the value of series resistor connected is set to be larger than $10^7 \Omega$. During the result signal extraction, the contact voltage has internal value (before series resistor) and external value (after series resistor). And the internal contact voltage is the right one to use for further characterization.

Figure 4.1 ESD simulation schematic in TCAD mixed signal mode

4.1.2 Interface State Generation Fundamentals

The physics of the kinetics of interface state generation is introduced in chapter 2. In TCAD, the interface state generation is numerically modeled in transient domain. The main mechanism used is the Si-H bond breaking [86]. Moreover, the Si-H bond activation energy takes account the dependence of

field, current and power. The dynamic balance process of dangling bond generation is controlled by the hydrogen ion diffusion process.

Generally, the interface state concentration, N_{it} , is expressed as,

$$N_{it} = N - n \quad (4.1)$$

where N is the maximum dangling bond concentration of silicon interface, n is the Si-H bond concentration of silicon interface. The key point in interface modeling is to calculate the value of n .

n follows the power law,

$$n = n_0(1 + (kt)^\alpha)^{-1} \quad (4.2)$$

where n_0 is the initial Si-H bond concentration and α is the power factor [74, 86].

The bond activation energy, ε_A , can be expressed as,

$$\varepsilon_A = \varepsilon_{A0} + \beta kT \cdot \ln \left(\frac{N-n}{N-n_0} \right) \quad (4.3)$$

where ε_{A0} is the intrinsic energy to break the Si-H bond, β is the model factor related to interface barrier.

All those field, current and power dependence mechanisms have their β' factor respectively. Then the overall β is like a combination of all the sub factors. The detail on β expression and experimental extraction is presented in [86, 105].

The hydrogen ion diffusion model considers the free hydrogen ion diffuse from Si/SiO₂ interface into oxide. This mechanism follows the diffusion law,

$$\frac{dN_{Hox}}{dt} = D \cdot \frac{d^2 N_{Hox}}{dx^2} \quad (4.4)$$

where N_{Hox} is the concentration of hydrogen ion in oxide, D is the diffusion coefficient.

In simulation setup, the initial interface state concentration, maximum interface state concentration and some other model factors are needed. Generally, N is set to 10^{12} and n_0 is set to 10^8 [105, 106]. In this work, the parameter set, α and β , uses the default calibration value set provided in the software. The diffusion coefficient, D , is set to 10^{-15} if the hydrogen diffusion model turns on [105].

The interface state information stores in the device state file separately. Device characterization simulation is able to pre-load the device state from user defined source. It provides the possibility to characterize a “stressed” device by loading an ESD simulation result data file when performing the device characterization.

4.2 ESD and Degradation Simulation Procedure

The GAA silicon nanowire FET discussed in this chapter follows the one produced in chapter 3. The only difference is that the device gate length is 50nm here. The device geometry is still boundary conforming meshed based on the active doping concentration for better numerical robustness. The mesh quality at the device junction area needs to be even tiny for the device in ESD simulation, which helps carefully monitoring the temperature distribution and impact ionization generation at these regions.

The device simulation follows the ESD TCAD simulation setup discussed in last section. Besides the physics models required for ESD simulation, the interface state generation model is also needed to simulate the interface degradation. The degradation model at the Si/SiO₂ interface is based on the Si-H defect kinetics discussed in last section. The hot carrier also needs extra modeling as it is the source of interface state generation. The hot carrier model used in simulation is the Fiegna hot carrier injection model [107]. And the hot carrier coupling factors are set to electric field and carrier temperature.

The device simulation thermal boundary condition is 300K as the ambient temperature. The device thermal dissipation is defined as $5.0 \times 10^{-5} \text{ cm}^2 \text{KW}^{-1}$ surface thermal resistance at the drain contact.

While the GAA silicon nanowire FET would be unlikely to be used as ESD protection device, in order to explain the experimental results which used TLP on GAA silicon nanowire FET, the ESD simulation is done by applying a TLP input to stress the device in this work. The input pulse is set as HBM equivalent with 10ns rising/falling time and 100ns pulse width as shown in Figure 4.2, and the gate contact is left floating during the TLP test, corresponding to the experiment conditions reported [98].

Figure 4.2 TLP current waveform and corresponding drain voltage waveform

A TLP pulse with high stress current level is first applied on the device in order to obtain the critical stress level that can cause the device hard breakdown. Figure 4.2 shows the corresponding drain voltage during the TLP stress. Figure 4.3 shows the TLP I-V curve and the device hotspot temperature in the z-axis during the TLP, and we can see that the hotspot temperature can reach as high as 1700K during the TLP stress period, which causes device hard breakdown as the temperature exceeds the melting point of silicon. This stress current level, denoted as I_{t2} , is found to be 15mA/ μm from Figure 4.3. The experimental stress level causes silicon nanowire melting is around 10-30 mA/ μm [98, 99], and we can see the close agreement of our simulation results with the experiment.

Figure 4.3 TLP I-V curve with hotspot temperature tracking

Recall the ESD performance constraint discussed in the review of chapter 2, the interface degradation and oxide defect are the two dominant device degradation mechanisms. The maximum oxide electric field under the I_{t2} stress level is shown in Figure 4.4, and thus gate oxide breakdown is less likely to happen as the oxide electric field does not exceed the critical level of 1V/nm [14]. Hence, it is reasonable to consider the interface degradation as the dominant degradation mechanism in our analysis of GAA silicon nanowire FET degradation during ESD TLP.

Figure 4.4 Maximum oxide electric field tracking under TLP stress of I_{t2}

No physical damage but severe performance degradation is observed experimentally when the current stress is set to be two-thirds of I_{t2} [98]. Our simulation with the same setup shows that the maximum silicon temperature is only 600°C which is still far from the silicon melting. Furthermore, the same device performance degradation is observed as shown in Figure 4.5 where 32% on-state current degradation in the drain current is characterized from the simulation, while the degradation level reported in [98] is 39%. Again, a good agreement between our model and the experimental results is demonstrated. As the simulation model focuses only on the interface degradation mechanism, the slight underestimation of the device degradation as compared to the actual experimental result is expected.

Figure 4.5 I_d - V_d degradation comparison between simulation model and experiment in [98]

The basic simulation analysis stated above serves to show the accuracy and suitability of the designed ESD simulation and degradation modeling. As the simulation result shows good agreement with the reported experiment result, further degradation characterization and failure analysis based on this modeling are considered convincing enough.

4.3 Simulation Result

Furthermore, different stress levels ranging from one-sixth to two-thirds of I_{I2} are also applied in the device degradation simulation. The post-degradation device characterization is evaluated and compared to its characterization before the stresses. The comparison of I_d - V_g and I_d - V_d of pre- and post-ESD

devices are depicted in Figure 4.6 and Figure 4.7. The degradation characteristics of the extracted device electrical parameters are shown in Figure 4.8. And the time progression of interface state generation during the TLP stress is shown as interface state concentration (N_{it}) versus pulse time plot as shown in Figure 4.9 to Figure 4.11. The maximum interface state concentration over the entire Si/SiO₂ interfaces is shown in Figure 4.9, and the average interface state concentration level at the source and drain regions are shown in Figure 4.10 and Figure 4.11 respectively.

Figure 4.6 I_d - V_g characteristics comparison between fresh and post-ESD devices

Figure 4.7 I_d - V_d characteristics comparison between fresh and post-ESD devices

Figure 4.8 Device electrical parameters degradation characteristics under ESD stresses

Figure 4.9 Maximum interface state concentration over entire Si/SiO₂ interface

Figure 4.10 Average interface state concentration at the Si/SiO₂ interface of source region

Figure 4.11 Average interface state concentration at the Si/SiO₂ interface of drain region

From Figure 4.8, we can see that the on-state resistance (R_{on}) and off-state drain leakage current (refer to right y-axis in log scale) increase with the TLP stress level, while the transconductance (gm), threshold voltage (V_{th}) and saturation drain current decrease with the TLP stress level. Under the pulse stress at two-thirds of I_{t2} , the degraded on-state resistance nearly doubled. The saturation drain current degrades the least among all the extracted device parameters, but the degraded off-state drain leakage current can be thousands of times of that in the degradation-free device. The physical mechanisms of the shifting in these device parameters are explained in the next section.

From the discussion of chapter 3, it is known that the GAA silicon nanowire FET has good gate controllability due to the gate-all-around configuration, and its off-state drain leakage current is much lower than other device structures.

However, as we can see here, this advantage is lost significantly when it is subjected to ESD stress, and hence effective ESD protection to the device is very important to leverage on the strength of the GAA silicon nanowire FET.

The upper bound of interface state concentration is set as the silicon dangling bond concentration at the Si/SiO₂ interface, which is 10^{12}cm^{-2} as discussed in last section. From Figure 4.9 to Figure 4.11, we can see that the maximum interface state concentration increases rapidly at the rising edge of the stress pulse while the average interface state concentration of region interfaces increases relatively slower. This means that huge amount of interface state generate only over a very small interface area during the rising edge of the stress pulse. Figure 4.11 shows that the increase in the average interface state concentration at the drain region is similar to the maximum interface state concentration increase as shown in Figure 4.9, indicating that more interface state is generated at the drain region than that at the source region at the rising stage of the stress pulse.

After the pulse rising time, the interface state concentration increases steadily, and the interface state concentration at the drain region interface is also much higher than that at the source region interface. The explanation for these observations is given in the next section.

4.4 Device Failure and Degradation Analysis

The device performance is severely degraded due to the reduction of carrier mobility as more scattering occur upon the interface state formation at the

Si/SiO₂ interface. The degradation is expected to be more severe for the GAA nanowire device as the surface to volume ratio of nanowire body is high.

ESD degradation and breakdown mechanism for GAA silicon nanowire FET is expected to be different from the mechanism of normal planar MOSFET. Previous ESD failure analysis study on MOS device shows that the major failure mechanism is the second breakdown of PN junction of the transistor [39]. For a gate grounded MOS transistor during ESD event, the drain-base PN junction is reverse biased until avalanche breakdown occurs in depletion region. The generated carriers then forward bias the source-base junction, and turns on the parasitic bipolar junction transistor to dissipate the ESD charge. The device enters into second breakdown if it fails to sustain the discharging current due to overheating.

However, in the case of GAA silicon nanowire FET, its substrate is floating and the nanowire channel is fully depleted during operation. This renders the absence of the parasitic bipolar junction transistor dissipation path in the device, and thus no snapback behavior is expected during the nanowire device breakdown as the TLP I-V curve observed experimentally in [98]. The TLP simulation indicates that the hotspot position is in the drain extension region as shown in Figure 4.12, thus the junction breakdown in GAA silicon nanowire FET is expected to occur at the drain junction.

Figure 4.12 Time evolution of hotspot position during TLP stress (the left block is the drain region. The transient stress time is labeled in each frame header.)

Under the ESD TLP stress condition, the impact ionization generates high energetic electron-hole pairs when the channel current injection is high. Hot carriers inject and get trapped at Si/SiO₂ interface, and this increases the carrier scattering which in turn reduces the carrier mobility and channel current, causing a rise in R_{on} and a reduction in gm as observed in Figure 4.8. The hot carrier induced interface state in the channel region is also responsible for the threshold voltage shifting [60, 108, 109]. The degraded threshold voltage means less effective gate control, which in turn increase the off-state drain current dramatically.

With the increase in the electron-state interface state concentration at the interface, the channel current path now moves slightly further away from the

interface. This, together with the reduction in the channel current, suppresses the impact ionization and further reduces the generation rate of interface state. Therefore, the interface state concentration or degradation level reaches certain equilibrium state after some time as observed in Figure 4.9 to Figure 4.11 where the average interface state concentration maintains at a level after first 50ns stress. For low level stress, the saturation interface states level is far from the pre-set upper limit of interface states, which indicates that there is no more new interface traps created. If the stress pulse is strong enough, as in the case of $10\text{mA}/\mu\text{m}$ stress, the maximum interface state concentration can reach the saturation limit as shown in Figure 4.9.

The impact ionization generation is nearly absent when the TLP stress level is lower than $7.5\text{mA}/\mu\text{m}$, which is half of the I_{t2} . Above $7.5\text{mA}/\mu\text{m}$ stress level, impact ionization generates electron-hole pairs massively at the drain side as shown in Figure 4.13. The normal and parallel electric field shows a peak region at the drain extension, and it also becomes more significant when stress level is above $7.5\text{mA}/\mu\text{m}$ as depicted in Figure 4.14 and Figure 4.15. High electron current density and high parallel electric field exist at the drain extension, which suggests that more hot electrons injection occur at this region. Therefore, the electron density at the drain side increases rapidly during the pulse rising edge due to the TLP current injection. However the electron current density at the source side does not vary as much as that at the drain side. This explains a sudden rising of interface state generation at the drain side, while no such effect is observed at the source side.

Figure 4.13 Impact ionization generation distribution along the nanowire Si/SiO₂ interface

Figure 4.14 Normal electric field distribution along the nanowire Si/SiO₂ interface

Figure 4.15 Parallel electric field distribution along the nanowire Si/SiO₂ interface

From Figure 4.13 and Figure 4.15, the impact ionization generation and parallel field at drain region both have a significant increment when the stress level reaches 10mA/ μ m from 7.5mA/ μ m. This implies that the source of interface degradation, the energetic electron-hole pairs and hot carrier, is generated more rapidly under higher stress level. The energetic carrier generation does not follow the linear increasing trend as the applied stress, a rapid increment of generation occurs when the stress shifts above certain threshold value. Hence, the device degradation becomes more severe under higher stress level.

A large negative magnitude of normal electric field also exists at the edge of both drain extension and source extension as shown in Figure 4.14. This strong negative electric field suggests a favor for hole injection at these two

positions. Trap of holes could induce negative mirror charge near the interface, increase the effective electron concentration. This mechanism results in drain current increase and R_{on} decrease. However such reverse shifting behavior of device electrical parameter is not observed in our simulation since the electron trap or negative interface state is dominating. As the intrinsic p-type doping level of nanowire is much lower than the source/drain doping, there are relatively fewer active holes as compare to electrons, thus the dominant carrier trap and degradation mechanism is hot electron injection related and the hot hole injection is only a minor competing mechanism in this case. The time progression of electron and hole trap concentration is depicted in Figure 4.16. With higher stress current level, the electron trap becomes even more effective due to larger positive normal electric field and there are more accumulated trapped electrons, and the impact of the hot hole injection is becoming less as can be seen in Figure 4.16.

Therefore, with the increasing stress level, more energetic carrier contributes to the device interface degradation, and the major degradation mechanism becomes more dominant than the competing mechanism. Hence, the device degradation accelerates under higher stress level. The R_{on} shifting curve in Figure 4.8 shows an increasing slope with the increasing ESD stress level, which suggests a higher device degradation rate under higher stress.

Figure 4.16 Electron and hole trap concentration under TLP stresses

The ESD stress seriously degrades the device performance by generating the charge-active interface state, and high level charge traps could reduce the oxide breakdown voltage. In some cases, the breakdown voltage is so low that local oxide melts due to the local conduction path formed by accumulated oxide traps.

From the above analysis, we can see that ESD TLP stress on GAA silicon nanowire FET will first trigger the hot carrier injection at the Si/SiO₂ interface which degrades the device performance. If the stress level is high or the stress persists, oxide breakdown will occur; and in some severe cases, device melt will be observed as seen in [98].

4.5 Summary

GAA silicon nanowire FET is a promising nanostructure for next generation semiconductor device, but the deep scaled device features and its gate-all-around configuration make the device have limited ESD immunity. The work in this chapter aims to study the device hard breakdown and performance degradation under HBM equivalent ESD stress. For the first time up to author's knowledge, the ESD event on GAA silicon nanowire FET is modeled in TCAD and benchmarked with reported experimental work. Good agreement between model simulation results and the experimental results demonstrates the modeling accuracy and the value of GAA silicon nanowire FET ESD modeling. Based on the analysis on modeling results, severe level ESD stress could catastrophically melt the device structure due to large amount of local heat generation. And lower level stress induces significant device performance degradation due to the generation of interface state along the nanowire via hot carrier injection. Moreover, this work provides further understanding on the nanowire device degradation mechanism during ESD event. The modeling result and degradation analysis from this work contributes to the knowledge of ESD reliability of GAA silicon nanowire FET, while the understanding of device reliability is extremely important to the next generation nanowire device based circuit design.

Chapter 5 RDF Analysis of GAA Silicon Nanowire FET

After the device reliability related discussion, this chapter intends to present the challenge of RDF on GAA silicon nanowire FET, which is due to the device intrinsic property. RDF impacts the performance of deep scaled semiconductor device due to the random placement of discrete dopant atoms [80, 84]. The reason of why dopant atoms placement affect so much is that the number of dopant atoms becomes very small in the device channel; hence the device operation is sensitive to the dopant atoms distribution. As the RDF is identified as the most important fluctuation source of process variation, it has attracted massive research effort. However, almost all those research work focuses on the RDF modeling work, few experimental result is reported since RDF is a statistical description which needs a lot of sample characterization work. The RDF analytical modeling work is based on the atomistic doping profile generation [16, 83] and the methodology of transformation from discrete doping profile to continue doping profile [85].

Up to the author's knowledge, there is still limited research result on the RDF analysis of multi-gate and GAA device. Due to the channel intrinsic doping property, there is an expectation that these multi-gate and GAA device have better robustness to RDF [110]. However, some work also argues that the RDF induced by source/drain doping may impact the device RDF performance [84]. The source/drain dopant atoms can randomly diffuse into channel and form the under-gate overlap region, which results variation of effective gate length and gate overlap capacitance.

This chapter is organized as follows: the RDF TCAD simulation methods are introduced in the first place. Secondly, the RDF characterization result of GAA silicon nanowire FET is presented. Lastly, the RDF robustness dependence on GAA device geometry dimension and process condition is analyzed and discussed.

5.1 RDF Simulation Methodology

There are three methods available to perform RDF analysis simulation in TCAD Sentaurus: the kinetic Monte Carlo process simulation, Sano random dopant placement method and impendence field method (IFM). These three methods rely on different theory background and simulation implementation. More important, their simulation time and computation resource requirement have quite large differences.

Normal process simulation approach models the dose implantation and annealing diffusion process by solving the atom transport PDE system. This pre-calibrated system directly produces the continuum contour doping profile as shown in Figure 5.1. This kind of doping generation does not include any randomize factor. On the other hand, the small number of dopant atoms forms a discretized distribution rather than a continuum distribution [111].

Figure 5.1 A continuum contour doping profile of GAA nanowire FET (half slice)

Kinetic Monte Carlo process approach provides an alternative approach. Unlike the continuum approach takes complex conservation processing on dose concentration, thermal energy and atom momentum, kinetic Monte Carlo method only takes the consideration on impurities and defects [111]. All the reaction process is the movement or collision of impurities, and the process condition is described as the reaction probabilities. More important to RDF analysis, kinetic Monte Carlo method provides the capability to model the statistical variation for process flow.

In practical simulation, the kinetic Monte Carlo simulation takes large computation resource and faces severe difficulty to converge, since the simulation conducts on the grid size of volume of amorphized silicon which forms an extreme tiny finite element system [111]. On the other hand, the

kinetic Monte Carlo simulator takes all possible impurity types by default. This brings convergence issue if certain impurity is actually not used in process flow, which is the extreme low impurity density error. Practically, extra impurity bypass setting is needed. For example, if only boron and arsenic are used in the model, then other supported impurities, such as phosphorus, indium and fluorine, need to manually turn off in simulation. A result discrete doping profile is shown in Figure 5.2. All the small dots represent the simulated dopant position.

Figure 5.2 A discrete doping profile of GAA nanowire FET (half slice and only line plot for geometry body)

The randomized profile function is activated by setting the simulation random seed index. Also the simulator provides the function to generate random seed based on system clock [111].

The discrete doping profile cannot be used in device simulation directly. The result discrete doping profile needs to convert to the continuum profile as shown in Figure 5.1. The transformation idea is to change the point charge of ionized dopant into charge density distribution. In TCAD Sentaurus, the commonly used transformation algorithm is Sano method [85, 86]. Generally, the charge density result from a discrete dopant can be expressed as,

$$\rho(r) = N_f \cdot \frac{k_c^3}{2\pi^2} \cdot \frac{\sin(k_c r) - (k_c r) \cos(k_c r)}{(k_c r)^3} \quad (5.1)$$

where N_f is a normalization factor, k_c is inverse of Debye screening length and r is the distance from discrete dopant. Couple with the meshed geometry, the charge density of every device mesh point can be calculated and the continuum doping profile is then generated.

The first RDF simulation method is simply run multiple times of kinetic Monte Carlo simulation with different random seed, and convert different discrete doping profile into continuum profiles for characterization simulation.

The second approach still needs discrete doping profile as a basic point. However, it uses a random dopant placement algorithm instead of performing multiple run of kinetic Monte Carlo simulation. The dopant atoms can be randomly placed on the mesh point within the screening length. By rearranging the dopant in the whole geometry to its surrounding nodes, nearly infinite numbers of different doping profile can be generated which serves as the same purpose as Monte Carlo simulation.

The dopant random placement algorithm is an extra function of Sano method. It can be found in Sentaurus Mesh package [86].

The third approach, IFM analysis, directly performs RDF analysis through a pseudo-noise analysis [86, 112], as the continuum doping profile can be converted into a probability distribution profile of dopant atom. The discrete dopant follows Poisson function. The noise induced by discrete dopant is assumed to be depend on the local doping concentration,

$$K(\vec{r}_1, \vec{r}_2, \omega) = N(\vec{r}_1) \delta(\vec{r}_1 - \vec{r}_2) \quad (5.2)$$

where $\vec{r}$ is the position vector. As the induced noise is static, ω is zero. However, for numerical needs, the TCAD simulation spreads the frequency over a 1Hz interval. The simulator computes the noise response among the whole device structure, and the noise response is reflected as the voltage or current variation on the device contact. As the IFM models the noise induced by discrete dopant over the screening length, it has the background linkage with the Sano dopant placement method. The detail mathematics theory of IFM is introduced in [112].

The result noise is actually the noise or fluctuation of electric signal on device contact. In practical simulation, the fluctuation magnitude of device current and voltage can be read directly on every bias point. Multiple device characterization can be taken as multiple samples on the contact noise distribution.

The three approaches produce quite close RDF result, it is difficult to comment which one is the most accurate method. However, their computation resource cost differs a lot. For a 30 device batch RDF simulation, the kinetic Monte Carlo approach takes about 6 days. The Sano method takes about 1 day. And the IFM analysis takes about 5 hours only. IFM analysis also takes extra

data post-processing time as it produces the noise data instead of device characterization data.

In this project, the IFM approach is used to characterize the RDF effect.

5.2 RDF Characterization

The GAA silicon nanowire FET used in RDF characterization follows the similar process steps introduced in chapter 3, only the LDD implantation step is removed. And only an n-type GAA silicon nanowire FET is characterized here. The device gate length is 50nm, the nanowire diameter is 10nm, the gate oxide thickness is 3nm, the source/drain doping dose is 10^{14}cm^{-2} arsenic ion and the gate contact workfunction is set to 4.2eV.

The device simulation also follows the same setting as the characterization simulation of GAA silicon nanowire FET. The drift-diffusion model with density gradient correction is used to model the carrier transport. The RDF characterization is based on the I_d - V_g characterization under both linear and saturation operation condition. As the device may have negative threshold voltage, the gate voltage sweep is from -1V to 1V.

The RDF simulation needs to set the doping noise flag in the device physics portion. The TCAD treats the RDF IFM simulation as a noise analysis, which is a small signal AC analysis [86]. Hence, the AC analysis setting is also needed. Since the RDF noise is a static noise, there is no frequency sweep at every bias point. Furthermore, the simulator spreads the noise spectral over a

1Hz interval which is -0.5Hz to 0.5Hz, the AC analysis frequency needs to be set within this range.

The IFM method introduces in noise spectral on both voltage and current at every $\langle I_d, V_g \rangle$ pair. In this case, both drain contact and gate contact need to be added into noise observation node manually. And as the noise analysis output, a $\langle \delta I_d, \delta V_g \rangle$ pair is produced as one noise result for a $\langle I_d, V_g \rangle$ point. In our analysis, 50 samples are simulated in every RDF case, which means there are 50 noise result for every $\langle I_d, V_g \rangle$ point! The simulator saves these massive δI_d and δV_g data separately in output files. Extra data processing effort is needed to restore back the noise data onto the device I-V curves for further device characterization, and the basic processing steps are introduced in the next subsection.

5.2.1 IFM Data Analysis

As both the δI_d and δV_g data is available when IFM simulation is done, hence, there are two approaches to obtain the actual $\langle I_d, V_g \rangle$ result with adding the noise data,

$$I_{d,noise} = I_{d,V_g} - \delta I_d \quad (5.3)$$

which fixes the gate voltage and apply drain current noise spectral on reference drain current; or,

$$I_{d,noise} = I_{d,(V_g+\delta V_g)} \quad (5.4)$$

which obtains the gate voltage with voltage noise spectral first, then get the corresponding drain current from the curve.

For a linear system, define the admittance y_a ,

$$y_a = -\frac{\delta I_d}{\delta V_g} = \frac{\partial I_d}{\partial V_g} \quad (5.5)$$

By expanding Eqn (5.4) into Taylor series, since the Taylor series of a linear function has zero terms for all the terms of 2th derivative and beyond,

$$I_{d,noise} = I_{d,V_g} + \delta V_g \cdot \frac{\partial I_d}{\partial V_g} = I_{d,V_g} - \delta I_d \quad (5.6)$$

which equals to Eqn (5.3). Hence, for a linear system, both approaches result the same drain current. However, they are not equal when the I-V system is not linear. For a normal I_d - V_g characterization, there are two regions which the curve has poor linearity. One is the sub-threshold region. The drain current noise and admittance increase exponentially. The gate voltage noise can maintain constant approximately. This makes Eqn (5.4) become more practical since Eqn (5.3) may give negative drain current if the noise spectral is relatively large.

The other non-linear region is the saturation region. The saturation region occurs at high gate bias and low drain voltage. The drain current noise becomes less changing while the gate voltage noise may become diverge. Some unrealistic gate voltage result (such as over the value of V_{dd}) may occur if applying Eqn (5.4). In this case, Eqn (5.3) is a better approach.

The data processing, or re-constructing the noise data onto normal I_d - V_g curves, requires a bi-approaches method. A transition between sub-threshold

region and linear region, also linear region and saturation region is needed. In practical analysis, the data before threshold voltage point uses Eqn (5.4) and the data after threshold voltage point uses Eqn (5.3). The finite gate biasing point, 40 in our analysis, may result an unsmooth transition between the two approaches. More gate biasing points can be added around the threshold voltage; or simply compute the results from both approaches at the transition point, then take the average as the final result.

5.2.2 RDF Simulation Result

The result I_d - V_g curves under both linear and saturation conditions are shown in Figure 5.3 and Figure 5.4. The GAA silicon nanowire FET has a 7mV mean threshold voltage. From the plots, it shows good RDF robustness in sub-threshold region and linear region for both low drain biasing and high drain biasing. When the gate voltage shifts above the threshold voltage, the device under high drain biasing shows higher RDF variation than the one under low drain biasing.

Figure 5.3 RDF I_d - V_g characteristics under linear operating condition

Figure 5.4 RDF I_d - V_g characteristics under saturation operating condition

Figure 5.5 shows the histogram plot of the extracted threshold voltage, and Figure 5.6 shows the probability plot of the same threshold voltage data set. By applying a normal distribution fitting, the standard deviation σ of the threshold voltage data is 7mV.

Figure 5.5 Histogram plot of extracted threshold voltage data with normal distribution fitting

Figure 5.6 Probability plot of extracted threshold voltage data with reference line

To explore more on the RDF impact of GAA silicon nanowire FET, a set of GAA silicon nanowire FETs with different geometry dimensions and process parameters are built and then the RDF impact is characterized. By extracting the threshold voltage variation in the same manner, the RDF dependence on device dimension and process parameter is studied. As the device parameters variation is an important manufacturing concern which needs to be controlled in the process design, this RDF dependence study is aimed to explore a possible device or process design which can result better RDF robustness for the GAA silicon nanowire FET.

5.3 RDF Geometrical Dimension Dependence Analysis

Four different geometry dimension variables namely, gate length, nanowire diameter, source/drain implantation dose concentration and gate oxide thickness, are selected in the RDF geometrical dimension dependence analysis for GAA silicon nanowire FET. The gate lengths are 25nm, 50nm and 100nm. The nanowire diameters are 10nm, 15nm and 20nm. The source/drain implantation dose concentrations are 10^{14}cm^{-2} , $5 \times 10^{14}\text{cm}^{-2}$ and 10^{15}cm^{-2} . The gate oxide thicknesses are 1.5nm, 3nm and 5nm.

All these devices are characterized for the RDF induced threshold voltage variation with the same setup as stated in last section. The standard deviation σ of threshold voltage is also extracted for all the batches. The result is presented in Table 5.1.

Table 5.1 Standard deviation σ of extracted threshold voltage

L_{gate} (nm)	σV_{th} (mV)
25	5.66
50	7.03
100	6.13
D_{nw} (nm)	
10	7.03
15	4.21
20	2.84
C_{dose} (cm^{-2})	
1.0×10^{14}	7.03
5.0×10^{14}	2.46
1.0×10^{15}	1.69
T_{ox} (nm)	
1.5	7.11
3	7.13
5	7.24

From Table 5.1, we see that the threshold voltage variation values of the devices with different gate length do not show a clear trend. However, both nanowire diameter and source/drain implantation dose present a dependence trend in that; larger nanowire diameter and higher source/drain doping can suppress down the RDF induced parameter variation. Thinner gate oxide also helps to suppress down the variation slightly, but not as significant as the factors of nanowire diameter and implantation dose concentration.

The threshold voltage V_{th} of an enhancement mode MOSFET can be expressed in this classical equation [87],

$$V_{th} = V_{fb} + 2\phi_f + \frac{Q_{dep}}{C_{ox}} \quad (5.7)$$

where V_{fb} is the flat-band voltage, ϕ_f is the Fermi potential, Q_{dep} is the channel depletion charge and C_{ox} is the total gate capacitance.

As the flat-band voltage and Fermi level are the intrinsic parameters for a MOS device, they are less related to the RDF induced parameter variation. Hence,

$$\sigma V_{th} = \frac{\sigma Q_{dep}}{C_{ox}} \quad (5.8)$$

And from [84],

$$Q_{dep} \propto \sqrt{N_a} \quad (5.9)$$

where N_a is the channel doping concentration. So,

$$\frac{\partial Q_{dep}}{\partial N_a} = \frac{Q_{dep}}{2N_a} \quad (5.10)$$

Furthermore,

$$\partial V_{th} = \frac{\partial Q_{dep}}{C_{ox}} = \frac{Q_{dep}}{2N_a C_{ox}} \cdot \partial N_a \quad (5.11)$$

The doping concentration corresponds to the number of dopant atoms. Assume the dopant atoms in channel follow the normal distribution, we have [84]

$$\sigma N_a \propto \sqrt{N_a} \quad (5.12)$$

Hence,

$$\sigma V_{th} \propto \frac{Q_{dep} \sqrt{N_a}}{2N_a C_{ox}} = \frac{Q_{dep}}{2\sqrt{N_a} W L C'_{ox}} \quad (5.13)$$

where W is the effective channel width, L is the channel length and C'_{ox} is the unity capacitance per area.

From this semi-analytical model, the geometry dependence can be examined. The channel depletion charge amount is proportional to the channel length. Hence, the threshold voltage variation does not vary with the gate length.

The depletion charge is less likely to vary with the nanowire diameter, which can be treated as the channel width. Also larger nanowire diameter results higher gate capacitance, since

$$C'_{ox} = \frac{2\pi\epsilon_r\epsilon_0}{\ln\left(\frac{r_{nw}+t_{ox}}{r_{nw}}\right)} \quad (5.14)$$

where ϵ_r is the dielectric constant, r_{nw} is the nanowire radius and t_{ox} is the dielectric thickness. Based on these, larger nanowire diameter leads to lower threshold voltage variation. Smaller gate oxide thickness also leads lower threshold voltage variation, but since the oxide layer thickness is several

nanometers only, also the depletion charge amount increases with the oxide thickness, the resulted variation suppression due to gate oxide thickness changing is not so significant.

Different source/drain doping concentration has no direct relation with the threshold voltage variation analytically. However, the dopant atoms can diffuse into nanowire channel during the thermal annealing process which is the reason of gate overlap region formation. In this case, the source/drain doping is n-type. Higher source/drain doping means more n-type dopant atoms in the gate overlap portion. This could result a lower depletion charge amount, which can also suppress down the threshold voltage variation.

The threshold voltage variation of GAA silicon nanowire FET shows higher dependence on the nanowire diameter and the source/drain doping level compare to the gate length and the gate oxide thickness. Also the variation levels induced by RDF are only several mV among all the cases we explore, which shows the excellent RDF robustness of the GAA silicon nanowire FET.

5.4 RDF Process Condition Dependence Analysis

Besides the geometrical dimension dependence of RDF robustness, the process condition dependence is also valuable to investigate. Actually, the process condition dependence may become more practically useful than the dimension dependence since it is easier to adjust the process recipe than changing the device dimension in real fabrication.

Chapter 5 RDF Analysis of GAA Silicon Nanowire FET

In this analysis, three process parameters are selected to evaluate the process dependence of RDF robustness of GAA silicon nanowire FET. The three parameters are source/drain implantation energy (E_{imp}), thermal annealing time (t_{anneal}) and annealing temperature (T_{anneal}).

The GAA silicon nanowire FETs under all these different process conditions are simulated using the same process flow and the same RDF characterization as stated previously is performed. The RDF sample size is also 50. The device threshold voltage is still the selected parameter to study the RDF robustness.

The mean value μ and standard deviation σ of the result threshold voltage data sets are extracted and shown in Table 5.2.

Table 5.2 Mean value μ and standard deviation σ of extracted threshold voltage

E_{imp} (keV) ($t_{\text{anneal}}=5\text{min}$, $T_{\text{anneal}}=1000^\circ\text{C}$)	μV_{th} (V)	σV_{th} (mV)
9	0.404	3.86
12	0.406	5.03
15	0.407	5.25
18	0.406	4.30
21	0.410	4.34
t_{anneal} (min) ($E_{\text{imp}}=15\text{keV}$, $T_{\text{anneal}}=1000^\circ\text{C}$)		
3	0.408	3.95
4	0.407	4.32
5	0.407	5.25
6	0.408	3.81
7	0.408	4.27
T_{anneal} ($^\circ\text{C}$) ($E_{\text{imp}}=15\text{keV}$, $t_{\text{anneal}}=5\text{min}$)		
600	0.418	5.23
800	0.397	5.92
1000	0.407	5.25
1200	0.394	7.60
1400	0.409	12.80

From the extracted result, both mean value and standard deviation of the threshold voltage data do not show a monotonic changing trend for every process parameter. It is difficult to comment directly whether they can be controlled or optimized by adjusting the process parameter setting.

The mean value of threshold voltage maintains around 0.4V for all the cases, which suggests that the threshold voltage of GAA silicon nanowire FET is less depend on the process conditions.

The RDF induced threshold voltage variation shows higher dependence on the process conditions. The root cause of RDF induced variation is the random placement of discrete dopant atoms. Hence, if the process condition can affect the discrete dopant atoms distribution in the device, the RDF induced variation would also be affected.

The implantation energy affects the dopant atom depth. Different implantation energy can result different depths of the peaking dopant atom density. The nanowire is patterned at the middle depth of the silicon layer. Middle range of implantation energy, 12 and 15keV in this case, can generate the dopant density peaking at the close depth as the nanowire body, which means more dopant atoms may diffuse into the channel region and behaves higher RDF induced variation. However, low implantation energy generates a shallow doping while high implantation energy results the doping with large depth, which both have less dopant atoms could diffuse into the nanowire.

The annealing time and temperature affect the dopant atom diffusion. Theoretically, long annealing time and high annealing temperature can result more “complete” dopant diffusion which means longer diffusion distance. And

this may result larger RDF induced variation. From Table 5.2, the threshold voltage variation increases when annealing temperature shifts above 1000°C, which implies that more dopant atoms diffuse into nanowire under higher temperature and contributes to the channel charge variation. However, the result appears less valid for the annealing time case. The long time, constant temperature thermal annealing in this study may always generate “complete” diffusion profile as compared to the rapid thermal process annealing. And the “complete” diffusion profiles make the RDF induced variation become uncorrelated with the annealing time and render the resulting threshold voltage variation unpredictable.

To the author’s knowledge, there is no analytical analysis on the relation between the device RDF performance and fabrication process condition. Hence, it is not possible to analytically study the threshold voltage variation like the case of geometrical dimension dependence in last section. Combine with the simulation result, the RDF induced variation is possible to be controlled by limiting the dopant atoms diffuse into nanowire channel through adjusting implantation energy and annealing temperature, and this is expected as less dopant atoms means lower RDF.

5.5 Summary

RDF is identified as the most severe process variation source of the deep submicron semiconductor device. Due to the small dimension of the nanowire body in GAA silicon nanowire FET, the discrete dopant placement in body channel and gate overlap region impacts the device RDF performance

significantly. By performing the IFM statistical simulation in TCAD Sentaurus, the RDF effect in GAA silicon nanowire FET is studied. The RDF robustness of nanowire device is good due to its intrinsic nanowire doping. Further studies on device geometrical dependence and process condition dependence on RDF robustness are also conducted by applying the same simulation approach. By optimizing the device geometry dimension, the RDF induced variation can be further suppressed with larger nanowire diameter and higher S/D doping concentration. However, the adjustment on process treatment does not provide convincing result to improve the RDF robustness of GAA silicon nanowire FET. From the result, avoid using middle level implantation energy and control the annealing temperature may help to suppress down the RDF induced variation.

Chapter 6 Junctionless GAA Silicon Nanowire FET

GAA silicon nanowire FET has excellent gate controllability and short channel effect immunity as demonstrated in Chapter 3. However, for the conventional inversion mode FET, the difficulty of source/drain junction formation rises as the doping concentration abruptly changes from heavily doped source/drain region to lightly doped nanowire body over several nanometers only. The idea of junctionless GAA silicon nanowire FET is proposed recently to overcome this fabrication difficulty [31, 34, 35]. In junctionless FET, the dopant type is the same from source/drain to nanowire and the doping concentration is also uniform for all the active regions. The nanowire structure of junctionless FET is patterned after the implantation and annealing process, instead of the complex junction formation steps after gate stack definition in the inversion mode FET. The junctionless design can be successfully adopted in the GAA nanowire structure as the wrap gate and thin silicon body can provide effective gate depletion to turn off the device.

As there are only few researches to compare the performances of the conventional inversion mode GAA nanowire FET and junctionless mode GAA nanowire FET, and with the FET model developed in Chapter 3, the author extends the application of the device model for the comparison study so that the advantages and drawbacks of both type of GAA silicon nanowire FET can be analyzed and addressed.

This chapter is to discuss the characterization results of junctionless GAA silicon nanowire FET. A comparison study between junctionless FET and

inversion mode FET is also conducted, and the performance difference includes RDF robustness between the two different device configurations is analyzed. The junctionless GAA silicon nanowire FET model is produced by sharing the same model developing procedures of inversion mode GAA silicon nanowire FET as introduced in Chapter 3. The RDF characterization of junctionless GAA silicon nanowire FET follows the simulation methodology developed in Chapter 5.

6.1 Device Description

The junctionless GAA silicon nanowire FET structure is also generated from the process simulation using Sentaurus Process. It follows the similar process steps as the inversion mode FET, except the active region doping generation is at the very first step instead of the step after gate stack and spacer formation as stated previously.

The starting material is still a SOI wafer with $1.0 \times 10^{15} \text{cm}^{-3}$ p-doped top silicon layer. The active region doping process is performed before any other steps. The implantation dose is an arsenic ion dose at $1.0 \times 10^{14} \text{cm}^{-2}$ concentration. The doped silicon layer is then under constant temperature annealing process at 1000°C for 5 minutes. The nanowire is then patterned, followed by the gate stack definition and spacer formation. The nanowire is 10nm of diameter and the gate length is 50nm. The wrap gate oxide layer thickness is 3nm and the gate contact workfunction is set to 4.2eV.

The inversion mode GAA silicon nanowire FET used for comparison study has the same device size, only the source/drain implantation is applied after the gate stack and spacer formation. Figure 6.1 shows a comparison of the junctionless FET and the inversion mode FET. One can see that the junctionless GAA silicon nanowire FET has a uniform doping profile from the source/drain to the nanowire body, while the inversion mode FET has an intrinsic p-doped nanowire and the source/drain-nanowire junction.

Figure 6.1 Geometry comparison between junctionless and inversion mode GAA nanowire FET

6.2 Device Characterization

Only the n-type device is studied for both device configurations here. The device characterization of junctionless GAA silicon nanowire FET is a comparison study which uses the characteristics of the inversion mode counterpart as reference. Furthermore, the GAA silicon nanowire FETs with different gate length, nanowire diameter and implantation dose concentration (source/drain implantation for inversion mode device, active region implantation for junctionless device) are generated to evaluate the device characteristics with regard to different device specifications.

Simulated I_d - V_g plots of both junctionless and inversion mode GAA silicon nanowire FETs are shown in Figure 6.2. The key device parameters extracted from the plots are summarized in Table 6.1.

Figure 6.2 I_d - V_g characteristics comparison between junctionless and inversion mode GAA nanowire FET

Table 6.1 Device parameters of junctionless and inversion mode GAA silicon nanowire FETs

	V_{th} (V)	g_m (μA/V)	SS (mV/dec)	DIBL (mV/V)
junctionless	-0.175	1.056	60.9	43.2
inversion mode	0.007	1.044	67.4	34.6

From Table 6.1, the junctionless device has a lower threshold voltage than the inversion mode device due to its n-doped nanowire body. The transconductance (g_m) of both devices are close. The junctionless FET has the subthreshold swing (SS) of 61 mV/decade compare to 67mV/decade of the inversion mode FET, which suggests better gate controllability of junctionless FET. The drain induced barrier lowering (DIBL) level of junctionless FET is 43mV/V, while the inversion mode FET has lower DIBL at 35mV/V. This implies that the turn-off threshold level of junctionless device shifts more under high drain biasing voltage. This is because higher drain voltage renders the channel depletion region to move to drain side with larger depletion depth, and make the junctionless device turn off at lower gate biasing.

Figure 6.3 shows the I_d - V_g characteristics of both device configurations with different gate length, nanowire diameter, implantation dose concentration and gate oxide thickness. The key device parameters are extracted in Table 6.2.

Figure 6.3 I_d - V_g characteristics comparison of GAA nanowire FET with different gate length (a: junctionless, b: inversion mode), nanowire diameter (c: junctionless, d: inversion mode), implantation dose concentration (e: junctionless, f: inversion mode) and gate oxide thickness (g: junctionless, h: inversion mode)

Table 6.2 Device parameters of junctionless and inversion mode GAA silicon nanowire FETs with different device dimensions

	junctionless				inversion mode			
L_{gate} (nm)	V_{th} (V)	gm ($\mu A/V$)	SS (mV/dec)	DIBL (mV/V)	V_{th} (V)	gm ($\mu A/V$)	SS (mV/dec)	DIBL (mV/V)
25	-	1.824	62.20	97.3	0.007	1.979	69.36	68.2
50	-	1.056	60.90	43.2	0.007	1.044	67.40	34.6
100	-	0.538	59.88	31.4	0.009	0.656	64.35	19.1
D_{nw} (nm)								
10	-	1.056	60.90	43.2	0.007	1.044	67.40	34.6
15	-	1.498	61.27	39.6	0.016	1.923	67.98	17.4
20	-	1.823	62.04	37.0	0.030	2.696	67.96	14.2
C_{dose} (cm ⁻²)								
1×10^{14}	-	1.056	60.90	43.2	0.007	1.044	67.40	34.6
5×10^{14}	-	0.943	60.92	79.3	0.017	3.146	67.22	17.4
1×10^{15}	-	0.828	63.93	124.2	0.021	3.857	66.97	5.8
T_{ox} (nm)								
1.5	-	1.355	60.22	29.3	0.012	0.999	67.29	34.9
3	-	1.056	60.40	43.2	0.007	1.044	67.80	34.6
5	-	0.825	60.68	60.0	0.007	1.011	68.14	36.5

From the above results, one can see that the junctionless FET is more sensitive to the device dimensions. Especially for the nanowire diameter and implantation dose concentration, the I-V characteristic curve shifts a lot when these device dimensions change as we can see from Figure 6.3 (c) and (e). However, the inversion mode device does not suffer from this issue. Its operating mechanism, conducting through an inversion charge layer, is less dependent on the device dimensions.

6.3 Device Characterization Analysis

The junctionless GAA silicon nanowire FET works in a depletion mode. The gate induced depletion layer expands in the nanowire channel with lower gate bias, and the device turns off when the channel is fully depleted [31]. Analytically, the threshold voltage of junctionless GAA silicon nanowire FET equals to the gate bias voltage which induces the depletion layer with thickness equal to the nanowire radius.

From the analysis in [36], when the depletion layer thickness equals to the nanowire radius, the pinch-off gate voltage is,

$$V_g = - \left(\frac{qN_D}{4\epsilon_{Si}} + \frac{qN_D}{2\epsilon_{ox}} \cdot \ln \left(\frac{r_{nw} + t_{ox}}{r_{nw}} \right) \right) \cdot r_{nw}^2 \quad (6.1)$$

where N_D is the nanowire doping concentration, r_{nw} is the nanowire radius and t_{ox} is the gate oxide thickness.

Simply, this pinch-off gate voltage can be treated as the threshold voltage of the junctionless GAA silicon nanowire FET. This semi-analytical equation shows good agreement with simulation result. Larger nanowire radius, thicker gate oxide layer and higher nanowire doping concentration can shift the threshold voltage to be more negative, while the gate length does not affect the threshold level significantly. On the other hand, the threshold voltage of the inversion mode FET relies more on the induced depletion charge amount, which related to the nanowire body doping but not the source/drain doping. Hence, the changes on device dimensions have very limited effect on the threshold voltage of inversion mode FET.

By enlarging the nanowire size or scaling down the device gate length, both device configurations can achieve higher gm . Higher source/drain doping concentration and thinner gate oxide layer can also improve the gm of inversion mode FET. However, the same treatment is less effective for the junctionless device.

The SS performance of both device configurations is good. The junctionless device shows even excellent SS level which is close to the ideal value of 60mV/decade. This excellent subthreshold performance may be contributed by the uniform doping profile across the active region, since there would be less diffusion current induced by the carrier gradient.

The junctionless device shows poorer DIBL performance than the inversion mode counterpart. For the inversion mode FET, the drain bias induces the drain side depletion charge. The charge sharing between drain depletion region and gate depletion region lowering the conduction band, hence results lower device threshold voltage. Hence, if the device dimension changes can suppress the drain depletion region entering channel region, the DIBL performance is improved. Longer gate length, larger nanowire thickness and high source/drain doping result smaller drain depletion depth, and better DIBL performance is expected as shown in Table 6.2. The gate oxide thickness variation does not affect the DIBL effectively.

However, for the junctionless device, drain bias induced effect is to shift the gate depletion region. Higher drain bias can make the gate depletion shift to the drain side and have larger depletion depth. This kind of shifting actually makes the junctionless device turn off at even lower gate biasing, which

results poorer DIBL performance. Shorter gate length, smaller nanowire radius, thicker gate oxide layer and larger nanowire doping make the gate depletion region become more sensitive to the drain biasing; hence they lead to poorer DIBL performance as shown in Table 6.2.

6.4 RDF Robustness Characterization

The same RDF characterization as introduced in chapter 5 is also performed on the junctionless GAA silicon nanowire FETs. Figure 6.4 and Figure 6.5 show the simulated I_d - V_g plots result from the RDF characterization. Compare to the RDF characterization results obtained in Figure 5.3 and Figure 5.4 in chapter 5, it is clear that the variation level of junctionless device characteristics is larger than the inversion mode FET. By applying the same threshold voltage variation extraction, the standard deviation σ of device threshold voltage is 22.6mV, which is three times of the 7mV variation for the inversion mode device. The result on the RDF effect seems to contradict to the result from N. D. Akhavan et al [114] where they found from their simulation that junctionless GAA silicon nanowire FET has less performance variation in the subthreshold regime due to the absence of channel doping gradient [114]. On the other hand, their RDF variation characterization result in the above-threshold regime is matched with the result in this work, as shown in Figure 5.3 and Figure 6.4.

Figure 6.4 RDF I_d - V_g characteristics of junctionless GAA nanowire FET under linear operating condition

Figure 6.5 RDF I_d - V_g characteristics of junctionless GAA nanowire FET under saturation operating condition

Moreover, the same RDF characterization is also performed on the junctionless GAA silicon nanowire FETs with different gate length, nanowire diameter, implantation dose concentration and gate oxide thickness. The extracted threshold voltage variation is shown in Figure 6.6. The data of inversion mode FET is also presented in the same figure. The junctionless device shows poorer RDF robustness than its inversion mode counterpart among all the cases.

Figure 6.6 Threshold voltage variation characteristics of junctionless and inversion mode GAA nanowire FET

The semi-analytical modeling in [83, 113] analyses the threshold voltage variation of junctionless GAA silicon nanowire FET. The variation of channel discrete dopant atoms is considered as the major variation source. Such variation can be treated as equal to the variation of channel doping

concentration numerically. By assuming a Poisson distribution for the dopant atoms, the variation of channel doping concentration is,

$$\overline{\delta N_D(\vec{r1})\delta N_D(\vec{r2})} = \frac{N_D}{2\pi|\vec{r1}|L} \delta(\vec{r1} - \vec{r2}) \quad (6.2)$$

Furthermore, the variation of threshold voltage for junctionless GAA silicon nanowire FET can be written as [83, 113],

$$\sigma_{V_{th}}^2 \propto \frac{q^2 N_D r_{nw}^2}{L} \cdot \left(\frac{1}{8\pi\epsilon_{Si}^2} + \frac{\pi}{C_{ox}^2} + \frac{1}{2C_{ox}\epsilon_{Si}} \right) \quad (6.3)$$

where L is the gate length, r_{nw} is the nanowire radius and N_D is the nanowire doping concentration.

The simulation result shown in Figure 6.6 matches exactly the semi-analytical model. Larger nanowire radius, smaller device gate length, thicker gate oxide and higher nanowire doping concentration result in higher variation level of the device threshold voltage. In the case of high doping concentration, the threshold voltage variation can reach as high as 120mV; while for the inversion mode counterpart, the variation can be suppressed below 10mV for all the cases.

Recall the semi-analytical model of threshold voltage variation for the inversion mode GAA silicon nanowire FET,

$$\sigma_{V_{th}} \propto \frac{Q_{dep}\sqrt{N_a}}{2N_a C_{ox}} = \frac{Q_{dep}}{2\sqrt{N_a} W L C'_{ox}} \quad (6.4)$$

The fluctuation source is the channel depletion charge while that for junctionless device is the channel carrier charge. The intrinsic doped body of inversion mode nanowire FET has only $1.0 \times 10^{15} \text{cm}^{-3}$ p-doping. In the

junctionless device, the nanowire doping cannot be set to such low level due to the transconductance requirement. The doping level of junctionless nanowire body ranges from 10^{18}cm^{-3} to 10^{19}cm^{-3} in our analysis. The quantity of the carrier charge in junctionless nanowire body is much higher than the depletion charge amount in the inversion mode device. This concentration difference of fluctuation source contributes the higher performance variation in junctionless device.

Recall the different conclusion between Akhavan's work [114] and this work, the discrepancy may be due to the different assumptions on the channel doping concentration of inversion mode GAA nanowire FET. In [114], the junctionless GAA nanowire FET channel doping concentration is $1\text{e}20\text{cm}^{-3}$ and the inversion mode GAA nanowire FET channel doping concentration is about $6.67\text{e}19\text{cm}^{-3}$, the differences of channel doping concentration between junctionless and inversion mode GAA nanowire FET is very limited. However in this work, the channel doping concentration of junctionless GAA nanowire FET and inversion mode GAA nanowire FET is about $1\text{e}19\text{cm}^{-3}$ versus $1\text{e}15\text{cm}^{-3}$, which has significant difference. As concluded from above discussion and also the discussion in Chapter 5, higher nanowire channel doping concentration results in higher RDF induced variation. The junctionless and inversion mode GAA nanowire FET in [114] should show similar RDF induced variation since they have almost the same nanowire channel doping level. And there is only a 20% RDF induced variation is reported in [114]. However, the junctionless GAA nanowire FET in this work shows more significant, three times larger RDF induced variation than the inversion mode GAA nanowire FET due to the difference in nanowire channel

doping concentration. The inversion mode GAA nanowire FET studied in this work should show very limited RDF induced variation since its channel is almost un-doped as shown in Figure 6.1.

6.5 Summary

As an alternative approach of the GAA silicon nanowire FET, the junctionless device is proposed to solve the problem of abrupt source/drain junction in the nanometer scaled device. From the device characterization simulation, the junctionless GAA silicon nanowire FET shows reasonable electrical performance and excellent gate controllability. However, it shows several performance drawbacks when comparing to its inversion mode counterpart device. The device parameter of junctionless FET varies significantly with the device geometry dimension change, especially the threshold voltage. This threshold voltage roll-off brings challenge for the device design usage. Also, the junctionless nanowire FET shows much higher RDF variation than the inversion mode device. The poor RDF robustness of junctionless GAA silicon nanowire FET further limits its potential usage in future circuit design. For the junctionless GAA silicon nanowire FET, lower device doping concentration and smaller nanowire thickness can help provide practical device threshold voltage and better DIBL performance; and it can also suppress the RDF induced device performance variation.

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7.1 Conclusions

GAA silicon nanowire FET is a promising candidate for next generation nanostructure semiconductor device. Besides providing further scaling down capability, the GAA silicon nanowire FET also has improved gate controllability and short channel effect immunity as demonstrated from recent research. This master project thesis focuses on the TCAD modeling work of the GAA silicon nanowire FET. Different modeling topics are discussed in this work, from the fundamental process modeling and device characterization simulation, to the special modeling topic discussion on ESD degradation and RDF robustness.

Chapters 1 and 2 present the background of this GAA silicon nanowire FET project. Furthermore, the recent nanowire technology, ESD related knowledge and RDF background knowledge are reviewed in the chapter 2.

Chapter 3 discusses the device modeling of GAA silicon nanowire FET. Full device fabrication flow simulation based on Sentaurus Process is introduced. The device electrical characterization starts from the discussion of carrier transport model selection, followed by the evaluation of self-heating effect and process induced stress effect. The inappropriateness of hydrodynamic model is identified by Monte Carlo benchmark simulation and the study on carrier velocity profile. The necessity of using density gradient model is shown by evaluating the channel carrier distribution. Also the necessity of the thermal

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effect and stress effect coupling is studied. The advantages of GAA silicon nanowire FET is further evaluated from a comparison study between GAA silicon nanowire FET and FinFET.

Chapter 4 focuses on the ESD related modeling. Under ESD stress, the GAA silicon nanowire FET can be degraded or even thermally damaged. The modeling work is aimed to perform a comparison study with the experimental work. And from the simulation result, the physics phenomenon observed in the reported experiments can be reproduced in modeling with good agreement. Beyond the comparison study, more device degradation characterization work is performed. Combine with the knowledge of hot carrier injection and interface state generation, the device degradation mechanism is analyzed essentially. The Si/SiO₂ interface degradation induced by hot carrier impacting and channel avalanche stress contributes mostly to the GAA silicon nanowire FET ESD degradation.

Chapter 5 focuses on the RDF characterization. The RDF problem has become an important topic since it is highly related to the unavoidable process variation. Statistical based simulation methodology is introduced in the RDF modeling work. From the simulation result and also the semi-analytical study, the GAA silicon nanowire FET shows good RDF robustness. Motivated by finding an adjustment or optimization approach to control the RDF variation, the RDF geometrical dimension dependence and process parameter dependence are studied. Thicker nanowire and higher source/drain doping can help to suppress the RDF variation, which is supported from the extracted RDF characteristics. However, there is no strong evidence that the RDF variation can be controlled by adjusting the process treatment. From the

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extracted result, use low temperature annealing and avoid middle level implantation energy could result lower RDF induced variation.

Chapter 6 discusses the junctionless GAA silicon nanowire FET. As an alternative approach of GAA silicon nanowire FET, the junctionless device solves the fabrication problem on abrupt source/drain junction formation. From the characterization on junctionless GAA silicon nanowire FET and the comparison study with the inversion mode counterpart device, the junctionless device also shows good gate controllability and short channel effect immunity. However, it also shows significant device parameter roll-off upon device dimension change. Also, the junctionless device has poor RDF robustness as compared to the inversion mode FET. From the result, it is concluded that thin nanowire body and light active region doping is preferred in the junctionless GAA silicon nanowire FET design.

7.2 Future Work

This work is all about device modeling of GAA silicon nanowire FET in TCAD Sentaurus environment. There is no calibration effort involved and the lack of calibration work limits the modeling accuracy margin when compare to device experimental result.

The future work should focus more on the device characterization work. By tuning the parameter of device modeling based on the I-V characteristics from measurement, the calibrated modeling provides more valuable insight information for further device design. The calibrated, physics driven device

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model also helps the development of compact modeling and process design kit (PDK). The ESD related work also needs to be further supported from experiment work. In chapter 4, the ESD experiment results used for comparison are still limited but these are all can be obtained from recent publications. More ESD degradation experiment can help further verify and optimize the proposed ESD modeling. Furthermore, other ESD test techniques, such as average current slope test and charge pumping test, are still not been discussed on GAA silicon nanowire FET. The experiment result from these tests can provide more understanding on the device degradation physics.

The RDF study can also benefit from the experiment study, however, it may require huge experiment resource since RDF is a statistics based topic. The research effort on RDF should focus on the device optimization to suppress the RDF induced variation, especially for the variation among billions of transistors on one chip area. There is still no publication work on certain optimization methodology.

The junctionless GAA silicon nanowire FET could be a more promising nanowire device configuration due to its advantage on device fabrication. Further design effort on junctionless device is also aimed to suppress down its process variation into certain margin, as the junctionless device shows even significant performance variation as demonstrated in this work.

Publication List

- [1] Xiangchen Chen and Cher Ming Tan, “Modeling and Analysis of Gate-All-Around Silicon Nanowire FET,” in *Microelectronics Reliability*, 2014.
- [2] Cher Ming Tan and Xiangchen Chen, "Electrostatic Discharge Degradation Modeling of Gate-All-Around Silicon Nanowire Device," accepted in *Nano Convergence*, 2014.
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