Growth and characterization of III-V quantum dots on SI-based substrate

Leong, Yu Yan

2013

Leong, Y. Y. (2013). Growth and characterization of III-V quantum dots on SI-based substrate. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/61068>

<https://doi.org/10.32657/10356/61068>

**GROWTH AND CHARACTERIZATION OF III-V QUANTUM DOTS
ON SI-BASED SUBSTRATE**

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**A THESIS SUBMITTED
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY
IN ADVANCED MATERIALS FOR MICRO- AND NANO- SYSTEMS
(AMM&NS)**

SINGAPORE-MIT ALLIANCE

NANYANG TECHNOLOGICAL UNIVERSITY

2013

Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Liang Yu Yan

30 May 2013

Acknowledgements

Foremost, I would like to express my sincere gratitude to my thesis advisor Prof. Yoon Soon Fatt for his continuous support throughout my doctoral study. He is a motivated researcher and leader who knows when and how to give students a little push when we are stuck. I am very grateful for the opportunity he gave me to work with his group. This is a great team where the members help each other selflessly.

Secondly, I would like to thank my co-advisor Prof. Eugene Fitzgerald. His technopreneurial insights have never failed to impress me. He is a humor person who can turn the tough and stressful research brain-storming session into an enjoyable discussion.

I must offer my profoundest gratitude to my senior and mentor Dr. Chen Kah Pin. He joined the research group a few years ahead of me. He gave me a warm-hearted welcome to the group and advised me on many tedious administrative issues. He taught me the basic operation of the MBE system, which is one of the most important techniques in my research.

I am fortunate enough to have met Dr. Loke Wan Khai. He is the man who knows everything and the one who was always there to lend me a helping hand when the MBE machine or the PL machine broke down. He is a patient and helpful guy who generously offered help when I was in need.

Dr. Ng Chun Yong Andrew is my guru for writing a good research paper. I recalled when I handed him the draft of my first publication; he patiently went through the piece and helped me to reorganize my results and discussions. Throughout my study, we co-authored several publications. I was impressed by how he made use of his genius sense to turn the pieces of my research data into a well-organized paper.

I would like to express my special thank to Dr. Xu Zhe and Dr. Lee Shuh Ying, for their professional help in the device fabrication and the light-current measurement. They guided me from the very beginning till the end, from the design of mask until the measurement set up.

The completion of my PhD study required the help from many individuals. I would like to thank Dr. Tan Kian Hua, for sharing his MBE growth experience; Dr. Xu Dawei, for recommending a cheap and good thesis editing service; Dr. Satrio Wicaksono, for his comments and discussion in the past few years; Dr. Ng Tien Khee, for his guidance in the early stage of my PhD study; Dr. Hendrix Tanoto, for establishing a good GaAs/Ge growth recipe which was heavily used in my thesis work; Dr. Lim Kim Peng and Dr. Pham Huynh Tram, for their accompaniment during the days we worked hard in the MBE room; Dr. Zhao Hanxue, for the friendship and the memorable days when we either went for a big feast or went online shopping to relieve stress; Mr. Yeo Chiew Yong, for his encouragement and accompaniment especially during the desk-bound thesis writing days; Prof. Zhang Qing and his group members -- Dr. Li Hong, Dr. Liu Chao, Mr. Zhang Kang, for their guidance and advice in AFM; Dr. Guo Junyan from A*STAR, for sharing his insights on KMC simulation; the technicians at NTU -- Mr. Mohamad Shamsul bin Mohamad, Mr. Muhammad Fauzi bin Abdullah, Ms. Seet Lye Ping, for their kind support and assistance in the laboratory.

I am also grateful to the Singapore-MIT Alliance, for the 5-year-long financial support and the sponsorship to attend the 38th International Symposium on Compound Semiconductor 2011 at Berlin.

I would like to thank my parents, Liang Hin Cheow and Tee Poh Chan, for being supportive throughout my academic career. Last but not least, I would like to thank my husband, Hong Jing, for his love and support.

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Abstract

Growth and Characterization of III –V Quantum Dots on Si-based Substrate

Liang Yu Yan

This thesis presents a systematic study of InAs quantum dot (QD) growth on Si-based substrates. Two Si-based platforms were studied, namely the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate which has a high threading dislocation density ($\sim 10^6 \text{cm}^{-2}$), and the germanium-on-insulator (GeOI) platform which has a lower threading dislocation density ($< 10^5 \text{cm}^{-2}$). Using the solid-source molecular beam epitaxy, a defect-free GaAs heteroepitaxy on Ge surface can be obtained by employing the low temperature migration enhanced epitaxy technique. QDs with high dot density were obtained by optimizing the growth parameters, such as the V/III ratio and the growth temperature. The photoluminescence of InAs QDs grown on GeOI showed a single-peak emission at $1.33\mu\text{m}$ with a line width of 36.3meV at room temperature. The promising optical performance enables the demonstration of the world first InAs QD LED on the GeOI substrate. The edge-emitting ridge waveguide LED structure with a 5-layer-QD active core emits at $1.312\mu\text{m}$ at 25°C . This is a memorable milestone for the monolithic growth of III-V QDs on a Si-platform.

Thesis Advisors:

1. Prof. Yoon Soon Fatt, SMA Fellow, NTU
2. Prof. Eugene Fitzgerald, SMA Fellow, MIT

Summary

The monolithic integration of a III-V compound semiconductor on a silicon (Si)-based platform has attracted considerable research effort recent years. This has been motivated predominantly by the large economies of scales of Si wafers, which would potentially lead to a reduction in the production cost. Furthermore, the monolithic integration of III-V on Si enables the realization of the futuristic integrated circuits (IC) using optical interconnects.

The direct growth of gallium arsenide (GaAs) on Si platform is defective due to the large lattice mismatch between GaAs and Si. On the other hand, the growth of GaAs on Si can be done through a germanium (Ge) intermediate layer since the defect-free heteroepitaxial growth of GaAs on Ge has been consistently demonstrated using the double atomic step annealing and the low temperature migration enhanced epitaxy (MEE) technique. Employing the mentioned GaAs/Ge heteroepitaxial growth technique, a systematic study of the indium arsenide (InAs) quantum dots (QDs) growth on Si platform was carried out in this thesis work.

The growth of self-assembled InAs/GaAs QDs is a popular research topic due to the unique three-dimensional confinement of QDs and the superior performance such as low threshold current density, good temperature stability, and high optical gain when it is fabricated into a laser. Nonetheless, most of the research studies were carried out on the conventional GaAs substrates.

Using the solid-source molecular beam epitaxy (SS-MBE), the InAs/GaAs QDs were grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, which is a Si-based platform with an undulated surface due to cross-hatches. The effects of surface undulations were studied

and it was experimentally and theoretically shown that the surface roughness does not affect the QD size uniformity across the undulations. The effects of the monolayer coverage and the V/III ratio were investigated and highly dense QDs ($1.1 \times 10^{11} \text{ cm}^{-2}$) were obtained on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The achievement is promising but in order to obtain high performance QD laser on Si, the threading dislocation density (TDD) of $\sim 10^6 \text{ cm}^{-2}$ is rather high.

The use of a germanium-on-insulator-on-silicon (GeOI) substrate is proposed as the TDD is more than one order lower compared to the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The GaAs buffer grown on the GeOI substrate and has a low surface roughness of $\sim 1 \text{ nm}$ and no anti-phase domains (APDs) are found in the cross-sectional transmission electron microscopy (XTEM) image. The structural properties and optical properties of the QDs grown on GeOI were investigated. An emission peak at $1.33 \text{ } \mu\text{m}$ with a linewidth of 36 meV at room temperature was achieved. This is the first reported single peak emission from the InAs/GaAs QDs grown on the GeOI substrate.

As discussed in literature, QDs grown on an off-cut substrate are more susceptible to a bimodal size distribution. This was also observed in the case of the InAs/GaAs QDs grown on an off-cut GeOI substrate. To explain the phenomenon, the Kinetic Monte Carlo (KMC) methodology was used to simulate the QD growth on a stepped substrate. A simple double-zone model was developed, which divides the off-cut substrate into two alternating regions: the step region and the terrace region. Additional activation energy is introduced in the step region. Preferential nucleation in the step region was observed and this leads to a bimodal dot size distribution. However, as shown in the simulation results,

with a proper control of the growth temperature, the group V overpressure and the substrate surface morphology, one can achieve a more uniform size distribution.

The thesis ends with the realization of the world first InAs/GaAs QD LED on the GeOI substrate. The edge-emitting ridge waveguide LED structure with a 5-layer-QD active core emits at 1.312 μm at 25°C with an external quantum efficiency of <0.01%. Although the results imply a lot of room for improvement, this is a memorable milestone for the monolithic growth of III-V QDs on a Si-platform.

Author's Publications

Publications in refereed journals

Y. Y. Liang, S. F. Yoon, C. Y. Ngo, H. Tanoto, K. P. Chen, W. K. Loke, E. A. Fitzgerald, “Effects of growth parameters on the surface morphology of InAs quantum dots grown on GaAs/Ge/Si_{1-x}Ge_x/Si substrate”, *Journal of Crystal Growth* **323**, 426-430 (2010).

Y. Y. Liang, S. F. Yoon, C. Y. Ngo, W. K. Loke, E. A. Fitzgerald, “InAs/GaAs quantum dots on germanium-on-insulator-on-silicon substrates (GeOI) using molecular beam epitaxy”, *Physica Status Solidi (c)* **9**, 214-217 (2011).

Y. Y. Liang, S. F. Yoon, C. Y. Ngo, W. K. Loke, E. A. Fitzgerald, “Characteristics of InAs/InGaAs/GaAs QDs on GeOI substrates with single-peak 1.3μm room-temperature emission”, *Journal of Physics D: Applied Physics* **45**, 145103 (2012).

Y. Y. Liang, S. F. Yoon, E. A. Fitzgerald, “Kinetic Monte Carlo Simulation for Quantum Dot Growth on Stepped Substrates” (2013). (*Under Review*)

Y. Y. Liang, S.F. Yoon, Z. Xu, S.Y. Lee, C.Y. Ngo, E.A. Fitzgerald, “InAs Quantum Dot LED on GeOI Substrate” (2013). (*In preparation*)

Conference presentations

Y. Y. Liang, S. F. Yoon, C. Y. Ngo, H. Tanoto, K. P. Chen, W. K. Loke, E. A. Fitzgerald, “Effects of growth parameters on the surface morphology of InAs quantum dots grown on GaAs/Ge/Si_{1-x}Ge_x/Si substrate”, *16th International Conference on Molecular Beam Epitaxy (ICMBE 2010)*, Berlin, Germany, 22 – 27 August 2010.

Y. Y. Liang, S. F. Yoon, K. P. Chen, C. Y. Ngo, H. Tanoto, E. A. Fitzgerald, “Surface morphology of self-assembled InAs quantum dots on graded Si_{1-x}Ge_x/Si substrate”, *11th Singapore-MIT Alliance Annual Symposium*, Singapore, 19 January 2010.

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Y. Y. Liang, S. F. Yoon, E. A. Fitzgerald, “InAs/GaAs quantum dots on germanium-on-insulator-on-silicon substrates (GeOI) using molecular beam epitaxy”, *38th International Symposium on Compound Semiconductors (ISCS 2011)*, Berlin, Germany, 22-26 May 2011.

Y. Y. Liang, S. F. Yoon, E. A. Fitzgerald, “Kinetic Monte Carlo Simulation for Quantum Dot Growth on Stepped Substrates”, *13th Singapore-MIT Alliance Annual Symposium*, Singapore, 14-16 January 2013.

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Chapter 1 Introduction

1.1 Background

1.1.1 Motivations

Since it was invented in the 1960s, the semiconductor industry has consistently achieved technology improvements. We have seen silicon (Si) wafers grow in size from the 6-inch to the 12-inch. In addition, Taiwan Semiconductor Manufacturing Company (TSMC) recently announced that the company will embark on the construction of an 18-inch wafer foundry in 2015 [1].

As the wafer size increases, the cost per integrated circuit (IC) chip decreases tremendously due to economies of scale. Over the years, transistors have become smaller, the minimum feature size has shrunk from 65 nm to 32 nm, and now the state-of-art is 22nm-node. This is in line with the prediction of Moore's Law, as shown in Figure 1.1, where the number of transistors in a chip doubles every 18 to 24 months [2]. The cost per function is reduced significantly as the number of transistors per IC chip increases. All of these technological advancements increase the profit of semiconductor companies and enhance our quality of life through various improvements in computer performance, communication, and consumer electronics.

Figure 1.1 The number of transistors in a microprocessor doubled approximately every 18-24 months from 1970-2010.

However, as pointed out in the International Technology Roadmap for Semiconductors (ITRS), further scaling of semiconductor devices has become more difficult [1]. When the feature size approaches the limit of conventional optical lithography, more expensive methods are introduced (e.g. extreme ultra violet (EUV) lithography techniques). Thus, the cost effectiveness of scaling is greatly reduced. Furthermore, the gate oxide has already been thinned down to a few atomic layers and may not function well beyond this limit. In addition, the metallic interconnects may suffer from delay and noise as we further reduce the device dimensions and increase the integration density. Previously, the speed of an integrated circuit was limited by the gate delay where interconnect delay is almost negligible. As the device shrinks, the gate delay is improved, but the interconnect delay increases significantly due to the substantial increase in interconnect length and the reduction in the interconnect line width. Although

the use of copper to replace aluminium interconnects and the introduction of low-k dielectric as interlayer material have mitigated this problem, the metallic interconnect system is approaching its limits as scaling continues. These limitations prompt a more revolutionary alternative. Hence, researchers are starting to pay attention to optical interconnects.

In simple words, the optical interconnect is a system where conventional copper lines are replaced by optical waveguides, and photons instead of electrons are used to transmit signals. As compared to the conventional metallic interconnects, optical interconnects offer a higher bandwidth and faster speed. Additionally, crosstalk noise between metal lines is not an issue for optical interconnects. The building blocks of an optical interconnect system are shown in Figure 1.2 and they consist of a light source, a modulator, a waveguide, and a photo detector. In order to realize the optical interconnect system, these optoelectronic building blocks have to be compatible with the Si-based complementary metal–oxide–semiconductor (CMOS). However, silicon is an indirect band gap material. Thus, it is not the best candidate for optoelectronic applications. Most high performance optoelectronic devices are made of direct band gap materials such as gallium arsenide (GaAs), indium phosphide (InP), and gallium nitride (GaN). Motivated by the need to produce Si-CMOS compatible optoelectronic devices, intensive research has been carried out to integrate direct band gap III-V compound semiconductor materials on a Si-based platform.

Figure 1.2 Schematic diagram of an on-chip optical interconnect.

1.1.2 The Heterogeneous Integration of III-V Compound Semiconductor Materials on Si

Two main approaches exist for the heterogeneous integration of III-V compound semiconductor materials on Si. The first approach is hybrid integration where III-V devices and Si devices are fabricated separately, and, subsequently, the III-V die is placed on the Si IC chip via bonding. The second approach is monolithic integration where III-V devices and Si devices are fabricated on the same platform through hetero-epitaxial growth.

The hybrid method has achieved some degree of success [3-5] as it allows III-V devices and Si devices to be fabricated under optimum conditions. However, the precise placement of the III-V die onto a Si chip can be very costly, especially when the process is not scalable. This increase in cost defeats the purpose of heterogeneous integration. The monolithic integration method is a wafer-scale process. It is a more practical approach compared to hybrid integration as it offers a higher through-put and better yield and reliability. However, the hetero-epitaxial growth of III-V on Si is challenging due to lattice mismatch, thermal mismatch, and polar-on-non-polar epitaxial growth.

Numerous studies have focused on the direct epitaxial growth of GaAs on Si, but, due to the 4% lattice mismatch, the quality of epitaxy was not satisfying. The threading dislocation density (TDD) is in the range of $5 \times 10^7 \text{ cm}^{-2}$ [6]. The direct epitaxial growth of GaAs on Si is problematic, but the direct growth of GaAs on germanium (Ge) is much more manageable due to the small lattice mismatch of less than 0.1%. Table 1.1 shows the lattice constants of various semiconductor materials. Having identified that Ge is a good intermediate layer for the integration of GaAs on Si, research work has been carried out to explore the potentials of Si-based Ge virtual platforms such as a compositionally graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate and germanium-on-insulator-on-silicon. The thermal mismatch issues of these substrates were studied. The results show that substrate cracking can be avoided by careful control of the epitaxy thickness and the processing temperatures [7].

Table 1.1 Lattice constants and thermal expansion coefficients of semiconductor materials (data extracted from www.matweb.com).

Material	Si	Ge	GaAs
Lattice constant ($\text{\AA}$) at 300K	5.431	5.658	5.653
Lattice mismatch with respect to GaAs (%)	3.9	0.1	n/a
Thermal expansion coefficient (K^{-1})	2.5×10^{-6}	6.1×10^{-6}	5.4×10^{-6}
Thermal mismatch with respect to GaAs (%)	54	13	n/a

Although lattice mismatch and thermal mismatch are no issues for the hetero-epitaxial growth of GaAs on Ge, one has to consider problems due to polar-on-non-polar epitaxy. As illustrated in Figure 1.3, anti-phase domains (APDs) are common for growing polar epitaxy (GaAs) on a non-polar substrate (Ge and Si). Recently, the hetero-epitaxial growth of GaAs on Ge without APDs was demonstrated [8]. There are three essential steps for achieving APD-free GaAs on Ge. First, off-cut substrates have to be used. Second, the substrates have to undergo pre-growth high temperature annealing at 640°C in order to achieve a double-atomic-step configuration on the off-cut substrate (as shown in Figure 1.3). Last but not least, the low temperature migration enhanced epitaxy (MEE) technique is employed for the nucleation of GaAs on a Ge surface.

Figure 1.3 The schematic diagram showing (a) how single-atomic-step substrate surface configuration leads to APD formation and (b) how double-atomic-step substrate surface configuration suppresses the formation of APD.

1.1.3 The Growth of InAs Quantum Dots

In this doctoral research work, the growth of indium arsenide (InAs) quantum dots (QDs) on Si-based Ge virtual substrates was studied. Self-assembled QDs have drawn considerable interest owing to their unique three-dimensional quantum confinement effects (see diagram in Figure 1.4). InAs QDs on GaAs have been researched extensively since lasing at room temperature was first demonstrated [9].

In general, there are three growth modes for hetero-epitaxy: a) Frank-van der Merwe (FM) growth, b) Stranski-Krastonov (SK) growth, and c) Volmer-Weber (VW) growth. A schematic diagram of the three growth modes is shown in Figure 1.5. In FM growth, the subsequent layer is grown on top of a completed film layer. Consequently, it is also known as layer-by-layer growth or 2D growth. In VW growth (also known as island growth), the bonding among the adatoms is strong and they prefer to cluster together. Stranski-Krastonov (SK) growth is in between FM growth and VW growth. In SK growth, a complete film is formed within the critical thickness. Beyond this thickness, adatoms start clustering into islands. The growth of InAs on GaAs falls into this category.

Figure 1.4 The density of states (D) for systems of various dimensions. The carrier confinement increases from zero-dimensional to three-dimensional as the system moves from bulk to quantum dot [10].

Figure 1.5 Schematic of the three hetero-epitaxy growth modes: (a) Frank-van der Merwe (FM) growth, (b) Stranski-Krastonov (SK) growth, (c) Volmer-Weber (VW) growth.

Although many articles discuss how to achieve good InAs QD optoelectronic devices, most of these works were carried out on an III–V platform. The investigation of InAs QD on a Si platform starts with InAs QD on a directly-grown GaAs buffer on a Si

substrate. Despite the poor crystallinity, an InGaAs QD laser was fabricated on this GaAs/Si platform. GaAs buffer layers as thick as 2 μm were grown directly on a Si substrate and a 10-layer QD dislocation filter was introduced. The detrimental effects of TDD were mitigated. Nonetheless, the performance of such QD lasers is poor (hindered by the inherently high TDD) [11]. We believe that the use of a the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate and germanium-on-insulator (GeOI) substrate could improve the QD device performance as the substrates have low TDDs of $\sim 1 \times 10^6 \text{ cm}^{-2}$ [12] and $< 1 \times 10^5 \text{ cm}^{-2}$, respectively [13]. A detailed study of InAs QD growth on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate and GeOI substrate is discussed in this dissertation with the ultimate goal of achieving the integration of III-V optoelectronic devices on a Si platform.

1.2 Objectives

- To study the optical properties and structural properties of InAs quantum dots grown on Si-based platforms (specifically, the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ graded buffer substrates and the GeOI substrates).
- To examine the effects of substrate undulation, V/III ratios, and InAs coverage for QDs grown on $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ graded buffer substrates.
- To examine the effects of QD growth temperatures on QDs grown on a GeOI substrate.
- To simulate the QD growth kinetics on off-cut substrates via Kinetic Monte Carlo (KMC) simulation to address the bimodal QD size distribution issues.
- To demonstrate a QD light-emitting device on a Si-based platform (GeOI).

1.3 Major Contributions

The direct growth of InAs/GaAs QDs on Si substrates has been proven problematic. The growth of InAs/GaAs QDs on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate and on a GeOI substrate has provided alternatives to the direct growth of InAs/GaAs QDs on Si substrates. A step-by-step demonstration of how a well-established monolithic growth of GaAs on Ge leading to successful InAs QD growth on Si platforms is discussed in this doctoral research work. The major contributions of this research work are summarized below:

- The study of QD growth on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ has shown that substrate undulation is not the key issue for growing QD with good optical quality. Instead, the inherent TDD of the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates is the key issue.
- GeOI, which has a lower TDD, has been shown to be a better candidate for the heterogeneous integration of III-V on Si platform. Photoluminescence with a z-factor close to unity shows that the emission efficiency is not affected by TDD and APD-related defects at GaAs/Ge interfaces.
- In 2011, an InAs QD on GeOI with a 1.3 μm emission wavelength was achieved. For the first time, the single peak emission of an InAs QD on GeOI at 1.3 μm was reported.
- The first InAs QD LED on GeOI was demonstrated in 2013. Although the device suffers from low external quantum efficiency, the realization of a QD device on GeOI is considered a breakthrough for the world of III-V heterogeneous integration on Si.

1.4 Organization of the Thesis

The thesis is organized into seven chapters. In this chapter, Chapter 1, the background, motivations, objectives, and a summary of major contributions of this work were given. Chapter 2 describes the various experimental techniques used in this research work including solid source molecular beam epitaxy and characterization tools such as atomic force microscopy, transmission electron microscopy, and photoluminescence spectroscopy.

In Chapter 3, the growth of InAs quantum dots on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is described in detail and the effects of growth parameters such as growth temperature and V/III ratio are discussed. The study confirms that surface undulation due to cross hatches on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate has little effect on the QD morphology and density.

The growth of InAs QDs on GeOI is discussed in Chapter 4, 5, and 6. The optical and structural properties of InAs QDs on GeOI are studied in Chapter 4. In Chapter 5, a kinetic Monte Carlo simulation is designed to study the dot size distribution of QDs grown on an off-cut substrate. In Chapter 6, the characterization of the world first QD LED on GeOI is described and various problems associated with QD LED on GeOI substrates are discussed.

Chapter 7 contains the conclusions of the thesis and some recommendations for future research.

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Chapter 2 Experimental Techniques

2.1 Epitaxial Growth Processes

2.1.1 Solid Source Molecular Beam Epitaxy (SS-MBE)

Molecular beam epitaxy (MBE) is an epitaxial growth technique involving the reaction of molecular beams with a crystalline surface of a substrate under ultra-high vacuum conditions. J. R. Arthur and Alfred Y. Cho invented this technique at Bell Telephone Laboratories in the late 1960s. The technique was widely explored in the 1980s owing to the advancement of vacuum technology at times when the “home-designed” ultra-high vacuum chambers were developed into a commercially available MBE system.

The characteristic feature of MBE growth techniques is the beam nature mass transport of substances in the reactor. This can be achieved under ultra-high vacuum conditions. The mean free path of molecules travelling in the vacuum reactor, L , which is defined as the average distance traversed by the molecules between successive collisions, can be given by the following relation [1-3]:

$$L = \frac{k_B T}{\sqrt{2} \pi \cdot d^2 p} \quad (2.1)$$

where k_B is the Boltzmann constant, T is the temperature, d is the molecular diameter, and p is the pressure. As the pressure decreases, the mean free path increases. Molecules travel from the sources to the substrate with the least collisions. This beam-like mass transport is one of the unique features of MBE compared to other epitaxial growth techniques.

The ultra-high vacuum environment has enabled the use of reflection high-energy electron diffraction (RHEED) for *in situ* monitoring, which allows us to characterize the growth front of the crystalline surface. Reflection high-energy electron diffraction provides information on growth modes, growth rates, and surface reconstructions. This monitoring system distinguishes MBE from other epitaxy deposition techniques, where real-time characterization is possible.

A schematic view of a typical MBE system is depicted in Figure 2.1. It includes the following components:

- a) Beam sources or cells: These cells are made from non-reactive refractory materials, pyrolytic Boron Nitride (PBN), which can withstand high temperatures. There are two types of cells: (1) conventional effusion cells and (2) cracker effusion cells. The former is for group III sources whereas the latter is usually for group V sources such as As₄ and P₄.
- b) Mechanical shutters: Mechanical shutters are placed in front of the beam sources to interrupt the beam fluxes.
- c) Cryopanel: The liquid-nitrogen-cooled cryogenic screening around the chamber acts as a sink for impurities in the vacuum.
- d) Substrate holder: The holder is connected to a motor so that it rotates at a constant angular velocity during growth to improve the thickness uniformity and the composition uniformity of the grown epitaxy.
- e) Reflection high-energy electron diffraction (RHEED): Reflection high-energy electron diffraction consists of two parts: (1) an electron gun and (2) a phosphor screen. The electron gun generates an electron beam, which strikes

the sample surface at a glancing angle. The diffracted electrons interfere constructively and form the diffraction patterns on the phosphor screen.

- f) Quadrupole mass spectrometer (QMA): The QMA is a useful tool for checking the level of the background impurities inside the growth chamber.

In this project, a Riber MBE 32P system was used to grow hetero-epitaxial GaAs on a Ge surface and the InAs/GaAs quantum dots. The growth techniques will be described in detail in Sections 2.1.2 and 2.1.3.

Figure 2.1 Schematic diagram of molecular beam epitaxy (MBE).

2.1.2 The Growth of GaAs on Ge Virtual Substrates

As discussed in Section 1.1.2, growing GaAs hetero-epitaxially on Ge virtual substrates is challenging since GaAs is a polar material with a zinc blende structure whereas Ge is a non-polar material with a face-centered cubic (FCC) diamond structure. The crystalline structure of GaAs and Ge is depicted in Figure 2.2. The growth of polar epitaxy on a non-polar substrate would lead to anti-phase domains (APDs). Anti-phase domains are notorious for acting as non-radiative recombination centres. Hence, deep level traps are introduced in the forbidden gap. However, deep level traps are undesirable from the perspective of device performance as they lead to a high leakage current [4, 5].

To avoid the formation of APDs, the formation of a double atomic step configuration on a Ge surface is essential. As illustrated in Figure 1.3(a), a single atomic step configuration will result in domain rotation at the surface step edges. A typical Ge substrate consists of both type-A terraces and type-B terraces. The height difference between the terraces is one atomic step (see Figure 2.3). The type-A terrace has dangling bonds pointing perpendicularly to the surface whereas the type-B terrace has dangling bonds making a 60° angle with the surface. Considering the dangling bonds per unit area, type-A terraces are thermodynamically more favourable than type-B terraces. At a sufficiently high annealing temperature, the atoms edges of type-B terraces would diffuse towards the edges of type-A terraces. Eventually, the entire surface would become type-A given sufficient time for diffusion [6-8]. The height difference between two adjacent type-A terraces is two atomic steps and such double-atomic step configuration can suppress the formation of APDs at the GaAs/Ge hetero-interface.

Figure 2.2 (a) GaAs zinc blende structure. (b) Ge FCC diamond structure.

Figure 2.3 Type-A and type-B terraces on the Ge surface.

In order to reduce the diffusion time required for double-atomic step formation, off-cut Ge substrates are introduced. The spacing between steps (w) is a function of the off-cut angle (θ) and the step height (d) given by the expression below:

$$w = \frac{d}{\tan \theta} \quad (2.2)$$

As the off-cut angle increases, the spacing is reduced. Atoms at the edges of type-B terraces travel a shorter distance to reach the edges of type-A terraces. The time for diffusion is shortened, and, thus, surface reconstruction takes place more readily. Such surface reconstruction, which has been experimentally proven, can be achieved by annealing the Ge (100) substrate with a few degrees off-cut towards the $[110]$ direction at $\sim 640^\circ\text{C}$ under an ultra-high vacuum condition without arsenic overpressure [9]. The annealing temperature of $\sim 640^\circ\text{C}$ is crucial. Below this temperature, characteristic surface defects will be formed as shown in Figure 2.4 [10].

Figure 2.4 Characteristic surface defects of GaAs on Ge at a low annealing temperature. (Left) The AFM image of the GaAs surface (featuring the characteristic V-shaped defects). (Right) A cross-sectional transmission electron microscopy (XTEM) of a GaAs/Ge hetero-interface focusing on the defects [10].

The double atomic step formation on the Ge surface alone will not produce good quality GaAs epitaxy on a Ge virtual substrate. As pointed out in many studies, the double atomic step formation has to be coupled with the pre-growth exposure of Ga or As atoms onto the Ge surface before the nucleation of GaAs to ensure a complete pre-layer coverage on the double atomic step surface [11, 12]. On the other hand, Ge out-diffusion is observed at the conventional MBE GaAs growth temperature of $\sim 580^{\circ}\text{C}$. Consequently, the Ge-doped GaAs becomes n-type and leads to the formation of a buried p-n junction. To inhibit the Ge out-diffusion, the GaAs nucleation temperature is lowered to the range of 250°C – 350°C [9, 13]. However, Ga adatoms tend to form clusters on a Ge surface at a low temperature as the adatom mobility exponentially decreases with respect to the substrate temperature. To address this problem, the migration enhanced epitaxy (MEE) technique is adopted.

The MEE technique is a new growth method that was introduced in the late 1980s [14, 15]. The surface migration is enhanced by supplying alternating Ga and As beams and keeping the As pressures low throughout the process. As a result, the incoming Ga adatoms migrate rapidly under low As pressure or an As-free atmosphere. Thus, they do not form stable bonds with the Ge substrate. Researchers have studied the RHEED intensity variation during MEE growth extensively [16, 17]. The typical RHEED intensity oscillations during MEE growth is depicted in Figure 2.5(a), whereas the typical RHEED intensity profile for the conventional GaAs growth at high temperature is shown in Figure 2.5(b). The former is known as “layer-by-layer growth” in which Ga adatoms are deposited on the step terraces. This type of growth creates atomically rough surfaces

and gives rise to the RHEED intensity oscillations. The latter is known as “step-flow growth” in which the adatoms migrate to the edges. This type of growth results in atomically smooth step terraces and no RHEED intensity oscillations.

Figure 2.5 Schematic drawing of (a) the layer-by-layer or 2-D growth mode and (b) the step-flow growth mode. Note that the RHEED intensity oscillation ceases in (b).

Therefore, in conclusion, the hetero-epitaxial growth of GaAs on Ge is achievable by employing the MEE growth technique with the use of Ge off-cut substrates and coupled with high temperature annealing to form double atomic steps.

2.1.3 The Growth of Self-Assembled InAs/GaAs Quantum Dots

As mentioned previously in Section 1.1.3, three hetero-epitaxial growth modes exist: a) Frank-van der Merve growth, b) Stranski-Krastanov growth, and c) Volmer-Weber growth. For two similar materials with little lattice mismatch, pseudomorphic growth or Frank-van der Merve growth usually takes place. For two dissimilar materials with a large lattice mismatch, island growth or the Volmer and Weber growth usually occurs. For two similar materials with a high lattice mismatch, we expect to see a transition from 2D growth to 3D growth (that is, the Stranski-Krastanov growth mode). The InAs/GaAs material system, with a 7% lattice mismatch, belongs to the latter. Thus, the InAs/GaAs quantum dots are also known as “self-assembled quantum dots” in which quantum dots are obtained without the use of lithography and patterning. Moreover, the self-assembled islands formed are coherent or without dislocations. This unique quantum confinement can lead to many interesting optical and electrical properties.

Many thermodynamic and kinetic models have been developed to describe and predict the evolution of self-assembled QDs [18, 19], some of these models can be quite complicated. However, the basic driving force behind QD self-assembly remains simple: the epitaxy deposited on a hetero-substrate builds up its strain energy as the thickness increases. Beyond a certain critical thickness, the strain energy is so high that the system

prefers to relax the strain at the expense of generating surface energy through island formation. In this way, the total energy of the material system is minimized.

In this project, InAs/GaAs QDs are grown using MBE. The growth process is monitored through the real-time RHEED. The 2D to 3D transition can be observed through RHEED as shown in Figure 2.6. This transition is important as it carries information regarding growth rates and the degree of intermixing at high growth temperatures.

Figure 2.6 Reflection high-energy electron diffraction (RHEED) patterns captured during InAs/GaAs QD growth. (a) Streaky 2x RHEED pattern before the 2D-3D transition. (b) Spotty RHEED pattern after the 2D-3D transition [20].

2.2 Characterization Tools

2.2.1 Atomic Force Microscopy

Atomic force microscopy (AFM) is a scanning probe microscopy (SPM) technique that makes use of the variation of force between the sample and the scanning probe to characterize the sample surface with a resolution of less than a nanometre (nm). The scanning probe microscopy technique (SPM) was invented in the early 1980s by G. Binnig and H. Rohrer at IBM Research, Zurich [21]. In 1986, they were awarded the Nobel Prize in Physics for inventing SPM.

The first atomic force microscope became commercially available in 1989. The set up consists of a 3-dimensional piezoelectric scanner and a cantilever with a sharp tip attached to its end. The schematic drawing of a typical AFM apparatus is shown in Figure 2.7. As the piezo-scanner moves in the x-y plane, it also controls its z-direction to bring the tip closer to or further from the sample surface and the actuation in the z-direction will cause the cantilever to bend. A reflected laser beam is used to monitor the deflection of the cantilever. Feedback on the deflection is sent to the piezo-scanner to maintain a constant tip-to-sample separation, and the surface morphology can thus be obtained.

Figure 2.7 Schematic diagram of atomic force microscopy [22].

The three basic operating modes for AFM are determined by the tip-sample separation as shown in Figure 2.8. The three modes are: a) the contact mode, b) the non-contact mode, and c) the tapping mode. During the contact mode, the tip-sample separation is usually less than 0.5 nm and the force between the tip and sample is repulsive. Contact mode operation allows a fast scanning rate but the tip or sample is damaged easily. During the non-contact mode, the tip-sample separation is more than 1 nm. Working with the weak attraction force between the tip and the sample, the tip lifetime is extended significantly but the resolution is low and the force is very sensitive to contaminants on the sample surface. The third operating mode, the tapping mode, lies between the contact mode and the non-contact mode. It produces high resolution images at a moderate scan rate and preserves the tip lifetime.

Figure 2.8 Plot of force as a function of tip-sample separation in atomic force microscopy.

In this project, AFM is used to examine the surface roughness of GaAs grown on a Ge virtual substrate and the morphology of quantum dots. Tapping mode imaging is used extensively. The surface roughness root-mean-squared (rms) R_q can be expressed as followed:

$$R_q = \sqrt{\frac{1}{n} \sum_{i=1}^n y_i^2} \quad (2.3)$$

This important parameter indicates the quality of GaAs hetero-epitaxially grown on a Si-based substrate and it determines the quality of QDs, which would subsequently be grown on the GaAs/Si platform. However, although AFM is a widely used technique to characterize QD density and dimension, we must not neglect the notorious AFM tip

convolution effects. Atomic force microscopy tip convolution arises from the fact that the tip is large compared to the nano-sized surface features. Hence, it does not always reflect the true topology of a surface. Figure 2.9 illustrates how the traced surface topology differs from the real surface topology. The height of the feature is preserved whereas the lateral dimension is enlarged, especially for tips with a low aspect ratio. Convolution is even more significant for high density QD samples where QDs are closely packed. When two surface features are in close proximity, the lateral size and the height will suffer from convolution. To minimize the tip convolution effects, a high aspect ratio Si tip with a radius of curvature ~ 2 nm was used for the QD sample characterization in this project.

Figure 2.9 As shown in this diagram, AFM tip convolution is more severe for a low aspect ratio tip than it is for a high aspect ratio tip.

2.2.2 Transmission Electron Microscopy (TEM)

In 1925, Louis de Broglie first came out with a theory: the electron had wave-like characteristics and its wavelength is smaller than the visible light. In 1927, C. J. Davisson and L.H. Germer in the United States [23] and G. P. Thomson and A. Reid in Scotland [24] independently carried out the electron diffraction experiments and the wave-like characteristics of electrons were proven.

The revelation of the wave nature of electrons was an important milestone in modern physics. It opened up an era of electron diffraction study, and, most importantly, led to the invention of a useful and versatile tool: the transmission electron microscope (TEM). This microscope was developed by Max Knoll and Ernst Ruska in 1931 and has a better resolution than a conventional optical microscope. A typical TEM consists of several components:

- a) Electron gun: The electron gun generates beams of electrons from an electron source using high voltage ($\sim 100\text{kV}$). The electron source can be a tungsten filament or a LaB_6 crystal.
- b) Column: The column is comprised of a series of electromagnetic lenses and apertures to manipulate the electron beam. The condenser lenses direct the generated electrons from the electron source to the sample stage. By adjusting the electromagnetic strength of condenser lenses, scientists can choose to operate in a convergent beam mode or a parallel beam mode. After the beam-specimen interactions, the transmitted electrons arrive at objective lenses where images or diffraction patterns are formed. The images and diffraction patterns are then magnified by the projector lenses.

- c) Image recording system: The transmitted electrons impact on a phosphor screen and cause the screen to glow so that the images and diffraction patterns can be seen. The results can be recorded either by a film or by a charge-coupled device (CCD).
- d) Pump and vacuum system: The microscope works under an ultra-high vacuum environment of 10^{-9} Torr. A rotary pump, an oil diffusion pump, and an ion pump are used to maintain a good quality vacuum environment.

In this project, the crystallinity and defects at the hetero-interface were examined using the cross-sectional transmission electron microscopy (XTEM) technique using JOEL JEM-2100. A XTEM image can reveal the presence of anti-phase domains, threading dislocations, and the origins of these threading dislocations. This is important for understanding the quality of GaAs grown on a Ge substrate. The TEM sample preparation is done manually or by using a focused-ion-beam (FIB). The specimen has to be thin enough (~ 100 nm) for electrons to transmit through it. Using the FIB technique is preferred as a scientist can precisely obtain a cross section of the sample at the area of interest.

2.2.3 Photoluminescence Spectroscopy

Photoluminescence is a process in which the photons directed to the sample are absorbed and the absorbed photon energies trigger the emission of photons. Photoluminescence (PL) spectroscopy is a useful contactless and non-destructive optical characterization tool. The PL signals pass through a 1200mm grating and they are

detected using a liquid nitrogen cooled germanium detector, which has a detection range of 800 nm to 1400 nm. Photoluminescence measurements can be collected at an ambient temperature or at a temperature as low as 5K with the use of cryostat. In this project, an Ar⁺ laser with an emission wavelength of 514 nm was used.

2.2.4 The Light-Current Measurement Set Up

The light-current characteristics were measured using the ILX Lightwave LPA-9070 Laser Diode Parameter Analyzer. A schematic drawing of the experimental set up is shown in Figure 2.10. The current is provided to the device under test (DUT) and the output light power is collected by an integrating sphere. A thermo-electric cooler (TEC) is attached to the sample stage to control the temperature of the device.

Figure 2.10 The schematic diagram of the light-current measurement set up.

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Chapter 3 Growth of InAs QDs on the Graded Si_{1-x}Ge_x/Si Substrate

3.1 Introduction

The three-dimensional quantum confinement is a unique characteristic of self-assembled quantum dots (QDs) which has drawn much research interest in the past decade. Due to this uniqueness, a QD laser exhibits low threshold current density, high optical gain, and good temperature stability [1]. Indium arsenide QDs on GaAs is one of the most widely studied QD systems since room temperature lasing was first obtained [2]. Researchers spent lots of effort to extend the InAs QDs emission wavelengths to 1.3 μm and 1.55 μm [3, 4]. Although many articles discuss how to achieve good InAs QD optoelectronic devices [5, 6], most of these works were carried out on an III–V platform.

On the other hand, the heterogeneous integration of III-V compound semiconductor on Si substrate has recently attracted considerable attention. This attention has been motivated predominantly by the potential reduction of production cost due to the large economies of scales of Si wafers. Nevertheless, as discussed in Chapter 1, it is extremely difficult to grow a GaAs epitaxy directly on a Si substrate as this would lead to the high threading dislocation density (TDD) in the range of $\sim 5 \times 10^7 \text{ cm}^{-2}$ [7]. Recently, an InGaAs QD laser integrated on a Si platform has been demonstrated [8]. GaAs buffer layers as thick as 2 μm were grown directly on a Si substrate and a 10-layer QD dislocation filter was introduced to mitigate the problem due to TDD. Nonetheless, the effective TDD with the thick buffer and dislocation filters is still high. The resulting threshold current density is extremely high ($\sim 900 \text{ A cm}^{-2}$), as compared to the threshold

current density of 32.5 Acm^{-2} for a 3-layer InAs QD laser on a GaAs substrate [9]. The results are shown in Figure 3.1.

To address the problem of the high TDD, a compositionally graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate was introduced [10, 11]. The XTEM of the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is shown in Fig. 3.2. Starting with a (100) Si substrate with a 6° off-cut towards the [110] direction, the graded SiGe buffer layer was grown using ultra-high-vacuum chemical vapour deposition (UHV-CVD) [12, 13].

Figure 3.1 An InGaAs QD laser directly grown on a Si substrate by Z. Mi et al. [8]. The layer structure of the QD device is shown in (a), highlighting the thick GaAs buffer of $2 \mu\text{m}$ and the 10-layer QD dislocation filter. The L-I curve is shown in (b). The extremely high threshold current density J_{th} is a direct outcome of the high TDD.

Figure 3.2 The cross-sectional transmission electron microscopy (XTEM) of a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. Dislocations are mainly confined in the graded buffer region and very few propagate to the Ge capping layer.

The growth temperature is controlled carefully within $0.7T_m$ and $0.8T_m$ where T_m is the melting temperature of the $\text{Si}_{1-x}\text{Ge}_x$ composite. [14] If the growth temperature is too high, undesirable gas phase nucleation would occur. If the growth temperature is too low,

the strain relaxation could hardly take place and the TDD would be high. The grading rate at which the Ge composition is increased in each subsequent grading layer is another important parameter to achieving a low TDD graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The grading rate has to be sufficiently low for the strain to relax via existing dislocations without forming new dislocations. During the growth, the residual elastic strain will relax to form undulations on the surface, and misfit dislocations pile up orthogonally, resulting in the characteristic “cross-hatch pattern” of the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate as shown in Figure 3.3. Therefore, when the buffer layer is graded up to 50% Ge, a thick $\text{Si}_{0.5}\text{Ge}_{0.5}$ cap layer is grown and chemical-mechanical polishing (CMP) is performed to flatten the undulated surface. Subsequently, graded buffer growth is resumed. The re-growth starts with growing a few micrometers of a $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer, and then it is graded up to a 100% Ge layer.

Figure 3.3 The typical “cross-hatch pattern” on the surface of a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. This image was taken using an optical microscope.

The graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate can be regarded as a virtual Ge substrate with a low TDD of $1 \times 10^6 \text{ cm}^{-2}$. As discussed previously in Chapter 2, the direct growth of GaAs on Ge is feasible because they have a small lattice mismatch and the thermal expansion coefficient is nearly the same. The GaAs on Ge without anti-phase domains (APDs) can be consistently obtained by applying low temperature migration-enhanced epitaxy (MEE) technique [15]. The comparatively low TDD was believed to potentially lead to a breakthrough in device performance for Si-based QDs. Many III-V devices have been demonstrated on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate, for examples the GaAs/AlGaAs quantum well laser, the AlGaAs/GaAs heterojunction bipolar transistor, and the InGaP/GaAs solar cell [16-18]. However, there are very few studies of QDs on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ platform [19, 20]. In this chapter, the surface morphology of QDs is discussed. The effects of V/III ratio, monolayer coverage, and substrate undulation due to crosshatches are studied.

3.2 Experimental Details

In this experiment, (100)-oriented graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates with a 6° off-cut toward (111) planes grown by UHVCVD were used. The growth was carried out using the SS-MBE. Prior to the MBE growth, cleaning of the sample using acetone, isopropyl alcohol (IPA), and de-ionized water was required. Immediately before loading into MBE chamber, the sample was exposed to an ultraviolet ozone environment at 100°C for 20 minutes to reduce the surface carbon contamination [15]. When the sample was loaded into the MBE chamber, it was annealed at 640°C for about 20 min in order to obtain the double-atomic step surface configuration which is important for the growth of GaAs on

Ge. While the substrate temperature was ramped up to 640°C, the native oxide of Ge started desorbing. A completion desorption was observed at the temperature of 350°C as shown in the RHEED pattern. The first 10 monolayer (ML) of GaAs on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate was deposited using migration-enhanced epitaxy (MEE) technique at a low temperature of 250°C at a slow growth rate of 0.1 $\mu\text{m/hr}$ and a V/III ratio of 40. Subsequently, a 500nm-thick GaAs buffer layer was grown at 580°C at a growth rate of 1 $\mu\text{m/hr}$ and a V/III ratio of 20. After the buffer growth, the active layer – InAs was deposited at 450°C at a growth rate of ~0.1 monolayer per second (ML/s). A 5s growth interruption was introduced through the closure of indium cell shutter after every 1s InAs deposition. The schematic of the structure grown was shown in Figure 3.4. With the aid of RHEED, a clear Stranski-Krastanov (SK) 2D-3D transition was observed and the critical thickness was identified as 1.7ML.

Figure 3.4 The schematic of the InAs QD structure grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate.

In this chapter, the QD morphology were studied by varying the V/III ratio and an InAs coverage. Five samples (Samples A to E) were grown with the growth conditions listed in Table 3.1.

Table 3.1 The growth parameters of Samples A to E.

Sample	V/III Ratio	InAs Coverage
A	10	2.0
B	10	2.6
C	10	3.0
D	12	2.6
E	15	2.6

The density, width, and height of the InAs QDs were characterized using AFM. A tip with a radius of curvature $\sim 5\text{nm}$ was used. For measuring small feature size, discrepancies exist between the measured dimensions and the actual dimensions. This phenomenon is known as the AFM tip convolution effects. A simple geometrical model was developed in Ref. [21] to quantify the discrepancies between the actual dimension and the measured dimension. This model is shown in Figure 3.5.

Figure 3.5 Interaction between an AFM tip with a radius of curvature r_t and a lens-shaped dot with height h [21].

From Figure 3.5, Equation (3.1) and Equation (3.2) are obtained:

$$h = r_d - \sqrt{r_d^2 - x_d^2} \quad (3.1)$$

$$(r_t + r_d)^2 = x_i^2 + (r_t + \sqrt{r_d^2 - x_d^2})^2 \quad (3.2)$$

Let the actual dot width $w_d = 2x_d$ and the measured dot width $w_i = 2x_i$. Then, Equation (3.1) and Equation (3.2) are rewritten as Equation (3.3) and Equation (3.4):

$$r_d = \frac{h}{2} + \frac{w_d^2}{8h} \quad (3.3)$$

$$8r_t r_d = w_i^2 - w_d^2 + 4r_t \sqrt{4r_d^2 - w_d^2} \quad (3.4)$$

Rearrange Equation (3.3) and Equation (3.4) as Equation (3.5) to express the actual dot width (w_d) as a function of the measured dot width (w_i), tip radius (r_t), and dot height (h):

$$w_d = \sqrt{w_i^2 - 8r_t h} \quad (3.5)$$

Figure 3.6 is plotted based on Equation (3.5). It shows the discrepancies between the actual dot width (w_d) and the measured dot width (w_i) for various dot heights (h) at a fixed tip radius (r_t) of 5 nm. As shown, the discrepancies are negligible when the dot height is below 5 nm and the dot width is in the range of 25–35 nm. However, for a dot height greater than 5 nm and a dot width smaller than 25 nm, a tip with a smaller radius of curvature is more appropriate.

Figure 3.6 The actual dot width plotted versus the AFM measured dot width [21].

3.3 Effects of Undulation on QD Growth

The surface of a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate is undulated, as shown in Figure 3.7. The impacts of the cross-hatches on the QD growth are not well understood. There are peaks and grooves along the $[110]$ and $[1\bar{1}0]$ directions of the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The surface roughness root-mean-square (rms) for a 500 nm GaAs buffer on the substrate is in the range of 4 nm to 8 nm. The surface mass transport of adatoms on an undulated surface might be very different from that on a flat surface as the chemical potential of surface diffusion is a function of surface curvature. Therefore, variations of QD dimensions and QD density across the undulations may arise. Furthermore, the geometrical shadowing effect and the readsorption of desorbed species due to the height difference between the peak and groove on the undulated surface might affect the uniformity of the QDs [22].

Figure 3.7 The AFM image of the substrate prior to QD growth (a scan area of $30 \times 30 \mu\text{m}^2$). A 500 nm GaAs buffer was grown on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The surface roughness rms is 5.5 nm.

To verify the effects of undulation on the QD uniformity, two distinct regions were sampled as shown in Figure 3.8. Quantum dots in the groove (Region I) and QDs on the peak (Region II) were compared in terms of density, height, and width. As tabulated in Table 3.2, Regions I and II have similar dot densities, dot widths, and dot heights. The differences between the QDs in the groove and the QDs on the peak were not distinguishable. This implies that, despite the undulating surface, the surface mass transport of the adatoms in the groove and on the peak does not change much.

Figure 3.8 The AFM image of Sample E. Region I and Region II are two sampling areas (area size = $20 \times 20 \text{ nm}^2$) representing QDs in the groove of the undulated substrate and QDs on the peak.

Table 3.2 The QD density and dimensions of Sample E for Regions I and II.

	<u>Region I</u> In the groove	<u>Region II</u> On the peak
Density ($/\text{cm}^2$)	1.15×10^{11}	1.08×10^{11}
Width (nm)	28.0 ± 5.5	30.0 ± 5.8
Height (nm)	2.4 ± 0.8	2.5 ± 0.7

To understand why substrate undulation has little effect on surface mass transport, the surface curvature of the graded $\text{Si}_{1-x}\text{Ge}_x$ substrate has to be quantified. The difference in growth rates across a curved surface was studied in Ref. [22]. The curved surface is represented by a sinusoidal surface with a characteristic width of x_o and an amplitude of h_o (see Figure 3.9). The equation can be written as Equation (3.6):

$$h(x) = \frac{1}{2}h_o - \frac{1}{2}h_o \cos\left(\frac{2\pi x}{x_o}\right) \quad (3.6)$$

Figure 3.9 The sinusoidal surface profile with a characteristic width of x_o and an amplitude of h_o . Position #1 and Position #2 are highlighted and the growth rates at these positions are compared.

The activation energy of adsorption and diffusion is a function of surface curvature. The local surface curvature κ and the radius of curvature ρ are expressed in Equation (3.7):

$$\kappa = \frac{1}{\rho} = \frac{d^2h}{dx^2} \left[1 + \left(\frac{dh}{dx} \right)^2 \right]^{-3/2} \quad (3.7)$$

Consider two scenarios. The first scenario has a characteristic width and amplitude both equal to 1 μm (maximum radius of curvature $\rho_{\text{max}} = 50 \text{ nm}$ as shown in Figure 3.10(a)). The second scenario has a characteristic width and amplitude both equal to 0.1 μm (maximum radius of curvature $\rho_{\text{max}} = 5 \text{ nm}$ as shown in Figure 3.10(b)). The growth rates across the surface along the x direction are plotted in Figure 3.10. The results suggest that the influence of surface curvature is less prominent when the maximum radius of the curvature is 50 nm or more. The undulated surface of the graded $\text{Si}_{1-x}\text{Ge}_x$ substrate can be profiled as a sinusoidal surface with a characteristic width of $\sim 10 \mu\text{m}$ and an amplitude of $\sim 0.1 \mu\text{m}$ (see Figure 3.7). In such case, the maximum radius of the curvature is calculated to be $\sim 50 \mu\text{m}$. Since the radius of curvature of the graded $\text{Si}_{1-x}\text{Ge}_x$ substrate is 1000 times larger, this explains why the effect of surface undulation on the QD densities and dimensions is negligible.

Figure 3.10 Concentration profiles across the sinusoidal surfaces. The groove where $x=0$ (Position #1) has higher growth rates than the peak where $x=0.5$ (Position #2). See Figure 3.9 for Position #1 and #2. The difference in growth rates for Position #1 and #2 is more significant when the radius of the curvature is small (as in (b)). [22]

3.4 The Effects of Monolayer Coverage

Samples A, B, and C have different InAs coverage of 2.0ML, 2.6ML, and 3.0ML, respectively. As shown in Figure 3.11, coalesced dot was found in Sample C (InAs coverage= 3.0ML). Knowing that large coalesced dots are usually contain defects which act as the centres of non-radiative recombination, thus, only QDs with a dot width smaller than 50 nm were considered. The estimated density for large coalesced dots with dot widths larger than 50 nm is about $5.6 \times 10^9 \text{ cm}^{-2}$. These dots were not included in the subsequent calculations of QD widths, heights, and densities.

Figure 3.11 The AFM image of Sample C with a 3.0ML InAs coverage (the scan area = $1 \times 1 \mu\text{m}^2$).

As depicted in Figure 3.12, the QD density remained in the same level for Sample A (InAs coverage = 2.0ML) and Sample B (InAs coverage = 2.6ML). However, the QD density reduced from $5.5 \times 10^{10} \text{ cm}^{-2}$ to $3.0 \times 10^{10} \text{ cm}^{-2}$ due to dot coalescence when the InAs coverage was increased to 3.0ML. The average heights for the three samples remained within the range of 3.5 nm to 5.0 nm. The lateral size of QDs grew linearly from 26.1 nm to 36.9 nm as the InAs coverage was increased from 2.0ML to 3.0ML. The QD width and QD height depicted in Figure 3.12 did not take into account of the large coalesced dots which were found in Sample C (InAs coverage = 3.0ML).

Figure 3.12 The effects of InAs coverage on InAs QD density, width, and height. Large coalesced islands with a lateral dimension greater than 50 nm were excluded (InAs coverage = 3.0 ML).

The effects of InAs coverage has been previously studied for QDs grown on the conventional GaAs substrate [23, 24]. It can be summarized into the following four different regimes:

- (a) At a low InAs coverage (below critical value 1.7ML), no QDs are formed but a thin layer of InAs.
- (b) At critical value 1.7ML, QD formation starts and the QD density increases abruptly.
- (c) At a high InAs coverage (above critical value 1.7ML), the QD density and QD dimensions increase gradually as the coverage increases until the saturation point is reached.
- (d) At a extremely high InAs coverage, dot coalescence occurs, causing the QD density to decrease and the QD width to increase.

In this section, the range of InAs coverage chosen (2.0ML to 3.0ML) for InAs QDs grown on a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate fall into the regime (c) and (d). The QD density saturated at $5.5 \times 10^{10} \text{ cm}^{-2}$ and reduced as coalescence occurred.

3.5 Effects of V/III Ratios

Samples B, D, and E were grown at the V/III ratio of 10, 12, and 15, respectively. An InAs coverage of 2.6ML was deposited knowing that the QDs obtained at 2.6ML InAs coverage have more uniform QD widths and QD heights as discussed in Section 3.4. Figure 3.13 shows how the QD width, the QD height and the QD density change under different V/III ratios. The QD density was found to drop by two times from $1.1 \times 10^{11} \text{ cm}^{-2}$ to $5.5 \times 10^{10} \text{ cm}^{-2}$ when the V/III ratio was decreased from 15 to 10. The increasing

diffusion length of the adatoms at a lower arsenic flux causes the reduction in the density. The likelihood for an indium adatom and an active arsenic species to meet each other drops as the amount of the active arsenic species on the substrate is reduced. Instead of nucleating an island, the adatom diffuses further to the next nearest islands. Thus, the QD density is lowered. The above trend resembles what has been commonly observed for InAs QDs grown on a GaAs substrate [25, 26]. We notice that the QD width is insensitive to the change in V/III ratio as the dot width ~ 30 nm for all Samples A, B, and C. The QD height was small (less than 2 nm) for QDs grown at high V/III ratios of 12 and 15. However, the QD height increased by two approximately 2 times from 1.8 nm to 3.5 nm at low V/III of 10, due to the enhanced diffusion as discussed earlier.

Figure 3.13 The effects of V/III ratio on InAs QD density, width, and height.

3.6 Summary

The discussions in Sections 3.2 and 3.3 show that the QD density and the QD size can be tuned by varying the growth parameters. High density QDs ($1.1 \times 10^{11} \text{ cm}^{-2}$), which would potentially lead to a high gain and high optical power QD laser, [27] are essential for realizing high power light-emitting devices, was obtained by increasing the V/III ratio. The QD density obtained is four times higher than the reported for QDs grown on the other Si platform [28]. This work is beneficial to researchers working on Si-based III-V QD lasers. However, the TDD $\sim 10^6 \text{ cm}^{-2}$ remains one of the major impedances for achieving high performance InAs QD lasers on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. Thus, it is very important to explore other low TDD Si platforms such as the germanium-on-insulator-on-silicon (GeOI) substrate.

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Chapter 4 Growth of InAs QDs on GeOI

4.1 Introduction

The direct epitaxial growth of GaAs on a Si was proven to be problematic due to large lattice mismatch between GaAs and Si, not to mention growing the InAs QD device directly on a Si substrate. The presence of threading dislocations at a density of $\sim 5 \times 10^7 \text{ cm}^{-2}$ [1] has led to a high threshold current density for the InAs QD laser directly grown on the Si [2]. Growing GaAs on a Ge virtual substrate (for examples, the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates and the Ge-on-insulator-on-Si (GeOI) substrates), is more feasible than growing GaAs directly on a Si substrate since the growth can be optimized to produce APD-free epitaxy [3]. In Chapter 3, we concluded that the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrates with a lower TDD $\sim 1 \times 10^6 \text{ cm}^{-2}$ [4] is an attractive substrate for the monolithic integration of GaAs on Si only if the TDD can be further reduced. Hence, the GeOI substrate is believed to be one of the most ideal platform for the monolithic integration of III-V on Si since its TDD ($< 1 \times 10^5 \text{ cm}^{-2}$) [5] is so much lower.

Bordel *et al.* [6] has recently reported a 1.3 μm -emission InAs QDs on GeOI at room temperature with the introduction of a 1 μm -thick GaAs buffer and a QD dislocation filter layer. However, the InAs QDs obtained are bimodal in size, and the PL spectrum shows 2 emission peaks at 1.3 μm and 1.19 μm as shown in Figure 4.1. Based on our previous experience of growing heteroepitaxial GaAs/Ge, the QD dislocation filter layer and the thick GaAs buffer is unnecessary if the growth of GaAs on Ge is optimized. The bimodal dot size distribution is probably a consequence of the non-optimized growth of InAs QDs.

Figure 4.1 The InAs QDs grown on a GeOI substrate by Bordel et al. (a) The PL spectrum at room temperature, comparing InAs QDs grown on a GeOI substrate to those grown on a GaAs substrate. (b) The 1x1 μm^2 AFM image of QDs grown on a GeOI substrate [6].

In this chapter, the effects of QD growth temperatures were studied. We demonstrated that good optical quality InAs QD on GeOI can be achieved with an optimized growth of GaAs buffer without introducing a thick GaAs buffer and QD dislocation filter layer. We demonstrated a 1.33 μm PL emission at room temperature from high density ($5 \times 10^{10} \text{ cm}^{-2}$) InAs QDs grown on GeOI. The obtained full-width-half-maximum (FWHM) is 36 meV, which is comparable to the FWHM of QDs grown on GaAs substrates.

4.2 Experimental Details

The GeOI substrate with 10° off-cut towards the $[110]$ direction was used. The substrate has a 100 nm SiO_2 layer and a 70 nm Ge cap layer on top of the Si holder wafer. Figure 4.2 shows the XTEM of the GeOI substrate. Prior to the growth, the Ge surface

was first dipped in the diluted HF solution to remove the uneven native oxide and then dipped in the diluted H_2O_2 solution to reform a thin and even protective oxide layer [7]. The sample was loaded into a vacuum chamber right after the surface treatment to avoid the oxidation of Ge surface and any other potential contamination.

The growth of InAs QDs on the GeOI substrate was carried out using the molecular beam epitaxy (MBE). As described in Section 2.1.2, the GeOI substrate was annealed under ultra high vacuum environment at 640°C to obtain a double-atomic step type-A (see Figure 2.3) surface, at the same time, to desorb the germanium oxide on the surface. The growth procedure for the GaAs on Ge is similar to the one described in Section 3.2 and it would not be repeated here.

Figure 4.2 The XTEM image of a GeOI substrate [5].

Five samples were grown on the APD-free GaAs buffer layer (see Figure 4.3 for the layer structure) and their growth conditions are tabulated in Table 4.1. Indium arsenide was deposited at 0.1ML/s growth rate with a 5s growth interruption after every 1s growth. A one-minute pause was introduced after the InAs deposition to enhance the adatom diffusion. Subsequently, the QDs were capped by a GaAs or $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ strain relieving layer (SRL). After capping deposition, the temperature was raised to 580°C to grow a 25 nm GaAs spacer layer. Lastly, an uncapped InAs QD layer was grown under the same growth parameters for the AFM characterization purposes.

Figure 4.3 The schematic diagram of InAs QDs grown on a GeOI substrate.

Table 4.1 Growth parameters of Samples A to E.

Sample	Growth Temperature (°C)	InAs Coverage (ML)	Capping
A	420	2.2	GaAs
B	450	2.2	GaAs
C	480	2.2	GaAs
D	450	2.5	GaAs
E	450	2.5	In _{0.15} Ga _{0.85} As

Samples A, B, and C were grown under a V/III ratio of 12 but at three different temperatures (420°C, 450°C, and 480°C, respectively) to study the effects of growth temperatures. At 450°C, Samples D and E were grown with 2.5ML InAs but different capping layers. The former was capped with a GaAs whereas the latter was capped with a In_{0.15}Ga_{0.85}As strain reducing layer (SRL).

The QD morphology of the uncapped QDs was examined using a high aspect-ratio AFM tip with radius of curvature ~2 nm. A high aspect-ratio AFM tip can minimize the dot size discrepancies due to tip convolution effects, as discussed in Section 3.2. The optical properties of the QD samples were studied using photoluminescence (PL). Using the 514 nm green laser, measurements were collected at room temperature at various excitation powers. A temperature-dependent PL study was carried out at the temperature range of 5K to 300K to understand the quenching mechanism of PL intensities.

4.3 The Structural Properties of InAs QDs Grown on a GeOI Substrate

The AFM image of the 500 nm GaAs buffer grown on the GeOI substrate was depicted in Figure 4.4. The surface steps due to the 10° off-cut were clearly seen in the AFM image, but the undulation is relatively small and the surface roughness rms is about 1 nm. No surface defects were found. The surface quality of the GaAs on GeOI is as

good as the best reported GaAs/Ge in the literature [8]. Comparing it to the work of Bordel et al. [6], their GaAs on GeOI has surface roughness rms of 3.8 nm due to the characteristic defects on the surface as explained in Chen et al.'s study [9].

The XTEM image of GaAs grown on a GeOI substrate is shown in Figure 4.5. The GaAs buffer layer was APD-free despite the small amount of APDs that self-annihilated at the GaAs/Ge heterogeneous interface. The GaAs buffer quality is still considered good as these self-annihilated APDs were not more than 20 nm away from the GaAs/Ge interface. The XTEM image in Figure 4.6 shows the defect-free InAs QDs of Sample D.

Figure 4.4 The AFM image of the GaAs buffer grown on a GeOI substrate (scan area = 20 x 20 μm^2). The surface roughness is ~ 1 nm.

Figure 4.5 The XTEM image of the GaAs buffer grown on a GeOI substrate. The inset diagram shows the magnified image of the GaAs/Ge hetero-interface.

Figure 4.6 The XTEM image of the InAs QDs grown on a GeOI substrate. The inset diagram shows the magnified image of the InAs QDs.

The AFM images of uncapped InAs QDs on Samples A, B, and C are depicted in Figure 4.7, from which the QD density and QD sizes are extracted. Unlike the reported QDs on a vicinal GaAs substrate, the QDs on the GeOI substrate did not align along the off-cut direction and there is no obvious preferential nucleation [10, 11]. Incomplete QD formation was found in Sample A was found due to the low surface diffusivity of adatoms at a low temperature of 420°C. This agrees well with what was observed the *in situ* RHEED pattern. The typical streaky-to-spotty RHEED pattern transition was not clear. On the other hand, the RHEED pattern showed a clear 2D-to-3D transition at the critical thickness of 1.7 ML for Samples B and C. For Sample B, the temperature was increased to 450°C. We obtained QDs with a high density of $4.8 \times 10^{10} \text{ cm}^{-2}$, a width of $38.1 \pm 14.3 \text{ nm}$, and a height of $4.7 \pm 2.6 \text{ nm}$. A further increase of temperature to 480°C led to improvements in the dot size uniformity as shown in QDs in Sample C, which have an average width of $46.8 \pm 6.2 \text{ nm}$ and an average height of $7.3 \pm 1.3 \text{ nm}$. However, the QD density decreased to $2.7 \times 10^{10} \text{ cm}^{-2}$, as a result of the increased diffusion lengths at high temperatures.

Figure 4.7 The AFM images of uncapped InAs QDs on Samples A, B, and C.

Samples D and E are InAs QDs grown at 450 °C and a V/III ratio of 12, similar to Sample B, but with the InAs coverage increased from 2.2 ML to 2.5 ML. The average QD dimensions obtained from the AFM image (refer to Figure 4.8) of Sample E are 30 nm wide and 5 nm high with a high QD density of $4.95 \times 10^{10} \text{ cm}^{-2}$. These measurements exclude the large coalesced islands beyond the critical size, which are about 1% of the QD population.

Figure 4.8 The AFM image of Sample E.

Figure 4.9 shows the histograms of (a) the QD widths and (b) the QD heights in Sample E. The solid lines indicate the critical QD size. The InAs islands which are larger than the critical size are usually defective and non-radiative. We notice that the two histograms are not perfectly Gaussian but skewed. The QD width histogram has two peaks whereas the QD height histogram shows a single peak distribution. The PL emission wavelength depends on the QD height and the QD width, and the relationship is given by the following expression [12]:

$$E_{GS} = E_{InAs} + E_{el} + E_{hh} \quad (4.1)$$

where

$$E_{el} = \frac{\hbar^2 \pi^2}{2m_{el}} \left[\frac{1}{L_x^2} + \frac{1}{L_y^2} + \frac{1}{L_z^2} \right] \quad (4.2)$$

and

$$E_{hh} = \frac{\hbar^2 \pi^2}{2m_{hh}} \left[\frac{1}{L_x^2} + \frac{1}{L_y^2} + \frac{1}{L_z^2} \right] \quad (4.3)$$

given that $E_{InAs}(300K) = 0.55$ eV; $m_{el}(InAs) = 0.04m_o$; $m_{hh}(InAs) = 0.59m_o$; $L_x = L_y$.

From the above equations, we note that QD height has a more dominant influence on the PL emission wavelength due to the low aspect ratio of QDs. As a result, a bimodal QD width distribution is less influential and thus, we still obtain a single peak PL emission from the InAs QDs on the GeOI substrate. The detailed optical properties will be further discussed in Section 4.4.

Figure 4.9 Histograms of the QD width and QD height in Sample E.

4.4 The Optical Properties of InAs QDs Grown on a GeOI Substrate

Figure 4.10 shows the results of the room temperature PL measurement of Samples A, B, and C. The PL intensity of Sample A was extremely low and its PL peak centered at $1.11 \mu\text{m}$. As discussed earlier, the islands formed were either incomplete or defective due to insufficient surface diffusion at a low growth temperature of 420°C . Thus, the light signal probably originated from the wetting layer. Samples B and C which were grown at a higher temperature of 450°C and 480°C respectively emitted strongly at $1.26 \mu\text{m}$ and $1.22 \mu\text{m}$. The peak emission of Sample C was stronger and the peak linewidth was narrower, as compared to Sample B, as a result of the improved QD size uniformity at higher temperatures. The explanation is in consensus with the AFM results in Section 4.3. However, a 40nm blue-shift was observed in Sample C. We believe this is due to the high temperature In-Ga intermixing.

Figure 4.10 Room temperature photoluminescence (PL) of Samples A, B, and C.

The room-temperature power-dependent PL of Samples B and C was studied. The integrated intensities (I) and excitation power (P) can be related by a simple relation: $I \propto P^z$, where the exponent z carries the information of the sample's optical quality. The z value of a good quality sample equals to unity ($z=1$). If non-radiative recombination centres are present, the z value is somewhere between 1 and 2 ($1 < z \leq 2$) [13]. For Samples B and C, the z value equals to 1.2, which implies the presence of non-radiative recombination centres. We believe the origins of non-radiative recombination centres in Samples B and C could be due to the following: (a) intrinsic defects in the GeOI substrate, (b) defects at the GaAs/Ge hetero-interface, and (c) InAs QD-related defects.

Subsequently, the temperature-dependent PL of Samples B and C was studied to understand more about the PL quenching mechanism. PL spectra were collected over a temperature range of 5K to 300K. The Arrhenius plots of the normalized integrated PL

intensity are shown in Figure 4.11. The Arrhenius plots were fitted using two activation energies: E_1 and E_2 . Sample B has activation energies $E_1 = 10$ meV and $E_2 = 192$ meV while Sample C has activation energies $E_1 = 27$ meV and $E_2 = 123$ meV. The smaller activation energy E_1 is the energy required for defects to undergo non-radiative recombination whereas the larger activation energy E_2 is the activation energy required for the carriers to escape from the confinement. The activation energies E_1 for Samples B and C have similar magnitudes but the activation energy E_2 in Sample B is much higher than that in Sample C. It is because Sample B has a longer emission wavelength, thus, it has better carrier confinement. The barrier height is larger, and therefore, a higher thermal energy is required for carriers to escape from the confinement.

Figure 4.11 Arrhenius plots of (a) Sample B and (b) Sample C. Integrated PL intensity is normalized.

The room temperature PL results of Samples D and E are shown in Figure 4.12. Sample D, which was capped with GaAs, emits at 1.28 μm with a line width of 32.2 meV. In fact, the emission wavelength can be deduced according to Equation (4.1), Equation (4.2), and Equation (4.3). Based on the AFM-obtained QD width and height (30 nm and 5 nm), the room temperature emission wavelength of Sample D was calculated to be 1.27 μm . We believe that this value differs from the experimental result of 1.28 μm because the dimensions used in the calculation were measured from uncapped QDs. For better accuracy, dimensions should be obtained from capped QDs. Sample E, which was capped with $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ SRL, emits at 1.33 μm with a line width of 36.3 meV as shown in Figure 4.12. The emission peak was red-shifted by 50 nm with the insertion of $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ SRL. The red shift is caused by the reduced lattice mismatch stress between QDs and capping layer, and also the reduced indium out-diffusion from the InAs QDs [14]. It is noteworthy that the FWHM of 36.3 meV for Sample E is comparable to the state-of-the-art of InAs QDs grown on GaAs substrates [15].

Figure 4.12 The room temperature PL of Samples D and E.

Figure 4.13 The integrated PL intensity (I) versus laser power (P) for (a) Sample D, where $I \propto P^{1.2}$, and (b) Sample E, where $I \propto P$.

The PL peak intensity of Sample D is ~50% smaller than the PL peak intensity of Sample E. This could be a result of the reduced strain-induced QD defects with the introduction of SRL. To investigate further, a power-dependent PL study was performed to determine the exponent z in the expression $I \propto P^z$. Figure 4.13 shows the power dependent PL plots for Samples D and E. The z values extracted are 1.2 and 1.0 respectively. The value of $z=1.2$ for Sample D is similar to what is obtained from Samples B and C, since in all the three samples, the QDs were capped by GaAs. There are three potential origins for the non-radiative recombination as discussed in the earlier part of Section 4.4. The power-dependent PL results infer that non-radiative recombinations are less likely to originate from the intrinsic defects of GeOI and the defects at the GaAs/Ge interface. The non-radiative recombination observed in Samples B, C, and D is mostly due to strain-induced defects in QDs. Nevertheless, the z values for Samples B, C, D, and E are considerably close to one. This implies that, regardless of the capping layer, the optical qualities of the InAs QDs grown on GeOI substrates are generally good.

Previously, the study of the PL quenching mechanism for GaAs-capped InAs QDs on GeOI (Samples B and C) based on the Arrhenius plots and found that there are two thermal activation energies, E_1 and E_2 . The former is related to defects in the samples and its value is <30 meV whereas the latter is related to the thermal escape of carriers from quantum confinement and its value is >100 meV. A similar study was carried out for the InGaAs-capped Sample E. Figure 4.14 shows the Arrhenius plot for Sample E. The Arrhenius plot is fitted and the activation energy is extracted using Equation (4.4) [13]:

$$\frac{I_o}{I} = 1 + A \exp\left(-\frac{E_a}{kT}\right) \quad (4.4)$$

where I is the integrated PL intensity and E_a is the thermal activation energy. The thermal activation energy E_a is 55 meV according to the red fitted curve, which coincides with the energy difference between ground state (GS) and the excited state (ES) as shown in the inset of Figure 4.13. Therefore, we suspect the quenching is mainly caused by carriers overcoming the barrier via the excited state.

Figure 4.14 The Arrhenius plot of the normalized integrated PL intensity (IPL) for Sample E. The red fitted curve has activation energy of $E_a = 55$ meV. The inset shows the PL spectrum at 5K, with both GS and ES peaks are identified.

4.5 Summary

To summarize, the growth of an APD-free GaAs on a GeOI substrate was demonstrated. Rooting on the APD-free GaAs buffer, the InAs QDs with a high dot density and improved size uniformity were obtained. The room temperature PL shows a narrow FWHM of 36.3 meV at 1.33 μm . To date, this is the only single-peak-emission on the GeOI substrate reported in the literature. The results have assured that utilizing GeOI for the heterogeneous integration of III-V QDs on a Si platform is feasible and promising.

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Chapter 5 Kinetic Monte Carlo Simulation for QD Growth

5.1 Introduction

The Kinetic Monte Carlo (KMC) method is useful to simulate the time evolution of a process with known growth rates or diffusion rates at the atomistic level. It has been widely used to simulate the growth of thin epitaxy, surface diffusion, vacancy diffusion in alloys, etc. Computer simulation work showing the evolution of QD growth has been demonstrated using the KMC method [1, 2]. The simulation allows scientists to correlate various experimental observations to the fundamental parameters of surface diffusion.

In the attempts to grow InAs/GaAs QDs on various Si platforms, we have observed some unique results which are not found on the conventional GaAs substrates. We notice that, in many cases, the QDs align themselves in a certain direction [3]. In addition, the QDs obtained are occasionally bimodal in size [3, 4]. Several research studies have attributed these observations to the use of a vicinal substrate [5]. However, in-depth understandings regarding these observations are still lacking at this time.

As discussed in Chapter 4, the QDs grown on a GeOI substrate were random and bimodal in size. Bimodal size distribution would lead to broadened emission wavelength, and this would reduce the efficiency of the light emitting devices. In order to develop a better understanding of the underlying mechanism, a simple simulation based on the Kinetic Monte Carlo (KMC) method is developed to study the influence of various process parameters for QD growth on a vicinal substrate.

5.2 The Formulation and Algorithm of the KMC Method

The heteroepitaxial growth of quantum dots involves various thermally activated diffusion processes, which are governed by Arrhenius' Law. The rate equations can be expressed as followed:

$$R = \nu_o \exp\left(-\frac{E_D}{kT}\right) \quad (5.1)$$

where ν_o is the attempt frequency, typically in the order of $\sim 10^{12}$ to 10^{13} ; k is the Boltzmann constant ($k = 1.38 \times 10^{-23} \text{ JK}^{-1}$); T is the absolute temperature; and E_D is the diffusion energy barrier. In order to diffuse from one location to another, the adatom deposited on the surface has to overcome the following energy barriers:

$$E_D = E_S + E_n + E_{strain} \quad (5.2)$$

where E_S is the binding energy to the surface (the value is usually fixed at 1.0 eV -1.3 eV in our simulation); E_n is the binding energy to neighbouring atoms; and E_{strain} is the effects of elastic energy in surface diffusion.

Assuming that the bond strength of the single nearest atom is assumed to be $E_b = 0.3 \text{ eV}$, the bond strength of the next-nearest atom is reduced by a factor of $\alpha = 1/\sqrt{2}$. Given that n is the number of nearest atoms ($n \leq 4$) and m is the number of next-nearest atoms ($m \leq 4$), the binding energy of atom at location (1) can be expressed as [2]:

$$E_{n(1)} = nE_b + m\alpha E_b \quad (5.3)$$

Similarly, when the atom moves from location (1) to location (2), the binding energy at the new location, $E_{n(2)}$, with the number of nearest atoms $n' \leq 4$ and the number of next-nearest atoms $m' \leq 4$ can be written as:

$$E_{n(2)} = g(n'E_b + m'\alpha E_b) \quad (5.4)$$

where g is the coupling coefficient. Thus, the overall binding energy, E_n , can be written as:

$$E_n = E_{n(1)} - E_{n(2)} \quad (5.5)$$

$$E_n = (n - gn')E_b + (m - gm')\alpha E_b \quad (5.6)$$

The effects of strain are particularly important in the growth of quantum dots. Consider a single atom attached to location (1). The repulsive strain energy acting on it originates from all of the surrounding atoms, and can be expressed as [6]:

$$E_{strain(1)} = \sum_{ij} \frac{kT}{r_{ij}^3} \quad (5.7)$$

where k is the Boltzmann constant ($k = 1.38 \times 10^{-23} \text{ JK}^{-1}$); T is the absolute temperature; and r is the distance between two atoms. The energy barrier E_{strain} for an atom moving from location (1) to location (2) can be expressed as:

$$E_{strain} = \frac{E_{strain(2)} - E_{strain(1)}}{2} \quad (5.8)$$

The substrate was modelled as a square lattice with 100 x 100 lattice sites. Equation 5.2 is used for QD growth on a conventional flat substrate. For QD growth on a vicinal substrate, the substrate is divided into two regions [5]: the terrace region and the step region (see Figure 5.1). An additional term, E_{step} , is added to Equation 5.2 for atoms diffusing in the step region. Equation 5.2 is then modified into:

$$E_D = E_S + E_n + E_{strain} + E_{step} \quad (5.9)$$

Figure 5.1 100 x 100 lattice sites for KMC simulation. The shaded area denotes the step region whereas the non-shaded area is the terrace region.

In this study, the movements of every atom on the substrate are simulated. Each atom would choose to diffuse to one of the four nearest positions. Out of all these events, one event was chosen randomly based on the weighted probability:

$$P_i = \frac{R_i}{\sum_j R_j} \quad (5.10)$$

where R_i is the rate of occurrence as calculated from Equation 5.1, and $\sum_j R_j$ is the total occurrence rate of all events. To advance the clock, a random time, Δt , was extracted from the exponential distribution and the time interval was independent of the event chosen. The time interval, Δt , was as shown:

$$\Delta t = -\ln(u) / \sum_j R_j \quad (5.11)$$

where $u \in [0, 1]$ is a uniformly distributed random number.

A simple flowchart depicting the algorithm of KMC simulation is shown in Figure 5.2. The simulation took place in a square lattice with 100×100 lattice sites. After each KMC step, once the time is updated, the list of events and their corresponding rates of occurrence were revised. The loop repeated until the time exceeded the preset total time.

Figure 5.2 The flowchart of the KMC simulation.

5.3 Design of Experiments

The simulations in this study were carried out on a square lattice of size 100 x 100 with periodic boundary conditions. The step region width was fixed at 7 lattice units and the terrace region width was 13 lattice units. The region widths were related to the degree of the off-cut of the substrates and also the surface morphology of the substrate and the grown epitaxy. 0.2ML of adatoms was deposited at the growth rate of 0.05 ML/s with a 5 second post-growth diffusion time. For each set of simulation conditions, the results were averaged over 10-15 runs.

Using the double-zone model described in Section 5.2, the growth temperature T and the additional barrier in step region E_{step} were examined. The QD growth temperature was varied from 600K to 750K, knowing that the actual QD growth temperature is in the range of 400°C to 500°C (673K to 773K). Two values were chosen for E_{step} : 0.15 eV and 0.5 eV. The value for E_{step} depends on the characteristics of the stepped substrate and also on the group V overpressure. These two parameters are strongly related to the topmost sensitive process variables in the actual growth of QD using MBE: the growth temperature and the group V overpressure.

The simulation assumed that a thin wetting layer had already been formed prior to the onset of simulation, and that the surface diffusion characteristics of the group III adatoms and the group V adatoms in the QDs were indistinguishable. Due to the constraint of computing power, the simulation was carried out over a small area of 100 x 100 lattice sites. We assume the results do not differ much from the actual QD growth, which is over a much larger area.

5.4 Results and Discussions

The dot density and size as a function of the growth temperature T and the additional barrier E_{step} are depicted in Figure 5.3 and Figure 5.4. The dot size increases and the dot density decreases as the temperature increases. This is identical to what we observe in the case of normal flat substrates. At a higher E_{step} , the average dot density is higher and the average dot size is smaller as the overall diffusion energy barrier E_D is higher.

Figure 5.3 The average dot density for $E_{step} = \{0.15 \text{ eV}, 0.5 \text{ eV}\}$ at the growth temperature $T = 600\text{K}$ to $T = 750\text{K}$.

Figure 5.4 The average dot size for $E_{step} = \{0.15 \text{ eV}, 0.5 \text{ eV}\}$ at the growth temperature $T = 600\text{K}$ to $T = 750\text{K}$.

However, when the dot size and dot density of the step region and the terrace region were examined respectively, we found that the average dot size in the terrace region is generally larger than the average dot size in the step region due to the comparatively lower diffusion barrier (as shown in Figure 5.5).

Figure 5.5 The average dot sizes of dots in the step region and dots in the terrace region for $E_{step} = 0.15$ eV and $E_{step} = 0.5$ eV across temperature $T = 600$ K to $T = 750$ K are shown in (a) and (b).

Figure 5.6 shows the dot density in the two different regions as a function of temperature. The density in the step region is much higher for a larger E_{step} but the dot density in the terrace region is not very sensitive to E_{step} since the rate of diffusion for adatoms in the terrace region is unchanged.

Figure 5.6 The dot density in the step region and in the terrace region for $E_{step} = \{0.15 \text{ eV}, 0.5 \text{ eV}\}$. The density is normalized to the number of dots over the 100 x 100 square lattices.

Figure 5.7 shows the monolayer coverage for dots grown on a stepped substrate. Preferential nucleation in the step region is found at all temperatures. Such phenomenon is more significant for a higher value of E_{step} . The differences in morphology for dots in the step region and dots in the terrace region lead to the non-uniform dot size distribution for dots grown on a stepped substrate.

Figure 5.7 The monolayer coverage in the steps and terraces at temperatures $T=600\text{K}$ to $T=750\text{K}$ and $E_{step} = \{0.15 \text{ eV}, 0.5 \text{ eV}\}$.

For the QDs grown on flat substrate, that is $E_{step} = 0$, the dot size distribution is uni-modal as shown in the simulated results in Figure 5.8 (a). Such uniformity is rare in the case of QDs grown on a stepped substrate as explained in the KMC simulation results above. Uniform dot size distribution is important for obtaining high power laser at a discrete wavelength. Figure 5.8 (b) shows the simulated result of 600K and $E_{step} = 0.5$ eV and its dot size distribution histogram. Two populations of dots are evident: the small and dense dots in the step region and the big and sparse dots in the terrace region. These populations denote a highly right-skewed size distribution. The skewness is slightly reduced when the temperature is raised to 660K, as shown in Figure 5.8 (c). At 660K and $E_{step} = 0.15$ eV, the dot populations of the terrace region and the step region merge well and approximate to a more uniform and symmetrical size distribution, as in Figure 5.8 (d).

The above conclusions from the KMC simulation correlate well to the experimental results as discussed in Chapter 4. We fine-tuned the growth temperatures and the group V overpressures for the growth of InAs QDs on a GeOI off-cut substrate so that the two different dot size populations were brought to close proximity. Hence, a high power single-peak emission was obtained. The dot size distribution histogram and the photoluminescence spectrum are shown in Figure 5.9.

Figure 5.8 The dot morphology graphs and the dot size histograms at various simulation conditions. (a) shows the dots grown on a flat substrate whereas (b), (c), and (d) show the dots grown on a stepped substrate with a terrace and step ratio of 13:7.

Figure 5.9 (a) The dot width histogram of InAs quantum dots grown on a vicinal germanium-on-insulator (GeOI) substrate at a growth temperature of 450°C. The room temperature photoluminescence shows a sharp peak at 1330 nm with a line width of 36.3 meV, as shown in (b), where the inset is the atomic force micrograph of scan area 500 nm x 500 nm.

5.5 Summary

This simplified KMC formulation of the QD growth on a stepped substrate does not intend to mimic the actual QD growth. Instead, it is an essential study that enables us to gain an understanding of the modality of the dot size distribution on a stepped substrate. Although QD growth on a stepped substrate is prone to result in a bimodal size distribution, a proper control of the growth temperature, the group V overpressure, and the substrate surface morphology can help to achieve a more uniform size distribution. This is particularly important for the growth of III-V QDs on Si-based substrates, wherein off-cut substrates are commonly used. The in-depth understanding of QD characteristics on stepped substrates is helpful to achieve high power III-V QD lasers on Si-based substrates.

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Chapter 6 InAs QDs Light-Emitting Device on a GeOI substrate

6.1 Introduction

Employing the growth conditions established in Chapter 4, we fabricated an InAs/InGaAs/GaAs QD light emitting device (LED) on a GeOI substrate. It is worth highlighting that this LED is the first reported on the GeOI substrate, and its characteristics are discussed in this chapter. A summary of the historical timeline for the InAs QD devices on various Si platforms [1-6] is shown in Figure 6.1.

The first InAs QD laser on a Si substrate was demonstrated using the direct growth of GaAs-on-Si technique [7, 8]. A high threading dislocation density (TDD) of approximately $5 \times 10^7 \text{ cm}^{-2}$ [9] arised from the large lattice mismatch between the GaAs and Si. To minimize the adverse effects of the high TDD, a thick GaAs buffer of 2–4 μm is required [1]. Another method is by inserting multiple layers of InAs QDs [2, 10] or InGaAs/GaAs superlattices (SPL) [11] as the dislocation filter into the GaAs buffer prior to the growth of the active layer in order to reduce propagation of the threading dislocations. However, the threshold current density (J_{th}) was found to be high (the lowest $J_{\text{th}} \sim 90 \text{ Acm}^{-2}$ per active layer) whereas the threshold current density of a InAs QD laser grown on the conventional GaAs substrate is only 11 Acm^{-2} per active layer [12]. These results suggest that we should look for an alternative with a lower TDD.

Figure 6.1 The historical timeline indicating milestones for the InAs QD devices on Si platforms. [1-6]

Thus, a graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate with a lower TDD of mid 10^5 cm^{-2} was proposed [13]. The characteristics of this Ge virtual substrate on Si platform were discussed in Section 3.1. The first light-emitting device (LED) on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate was demonstrated. The external efficiency (η_{ext}) is low with a maximum optical output per unit area of $\sim 7.6 \text{ mWcm}^{-2}$ due to non-radiative recombination processes [3]. Another successful attempt is the growth of InAs QD laser on Ge/Si substrate, where Ge was deposited on Si substrate via chemical vapor deposition. The Ge virtual substrate has a TDD of $5 \times 10^6 \text{ cm}^{-2}$. The threshold current density per active layer is 33 Acm^{-2} , which is so far the lowest threshold current reported for InAs QD laser on Si-based substrate [6].

Recently, the InAs QD laser on Si platform was successfully fabricated through wafer-bonding and the layer transfer technique [4, 14]. The InAs QD laser structure was first grown on a GaAs substrate, and subsequently bonded to a Si wafer using an AuGeNi alloy layer, as depicted in Figure 6.2.

Figure 6.2 The InAs QD laser structure wafer bonded to a Si substrate. [4].

A threshold current density of 205 Acm^{-2} or 41 Acm^{-2} per active layer was obtained. So far, this is the lowest threshold current density reported for the InAs QD laser on a Si substrate [15]. Although the laser performance is improved, the scalability of the wafer bonded QD laser on Si platform is a big problem as it is constrained by the wafer size of the GaAs substrate. The original intention of growing III-V lasers on Si platform is to transfer high performance III-V lasers onto the 12" or 18" silicon wafer with large economies of scale. The wafer bonding method also loses its flexibility in terms of growth and fabrication due to the introduction of a metal alloy, which limits the processing temperatures in turn. Therefore, it is important to look for a platform with a low TDD that could be scaled up to a 12" wafer size without the use of metal.

In this chapter, we propose growing the InAs QD LED structure on a GeOI substrate, which is metal-free and has a TDD much less than 10^5 cm^{-2} . Most importantly, the GeOI wafer is theoretically scalable to 12". The monolithic integration of InAs QDs on GeOI is compared side by side with the other InAs QDs on Si integration methods. The pros and cons are summarized in Table 6.1.

Table 6.1 A comparison of InAs QD devices grown on the Si platforms using different methods.

Year [Ref]	Method	Pro(s)	Con(s)
2006 [1]	Direct growth on Si	(1) Can be scaled up to 12" wafer	(1) Thick GaAs buffer > 2 μm (2) Very high TDD $\sim 10^7 \text{cm}^{-2}$
2007 [2]	Direct growth on Si with QD dislocation filters	(1) Can be scaled up to 12" wafer	(1) Thick GaAs buffer > 2 μm (2) Very high TDD $\sim 10^7 \text{cm}^{-2}$
2009 [3]	Via the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate	(1) Can be scaled up to 12" wafer	(1) Thick graded buffer $\sim 10 \mu\text{m}$ (2) High TDD $\sim 10^6 \text{cm}^{-2}$ (3) Off-cut substrate (4) Undulated surface
2010 [4]	Via AuGeNi wafer bonding	(1) Low TDD < 10^5cm^{-2} (2) Thin buffer < 1 μm	(1) Cannot be scaled up to 12" wafer (2) Low processing temperature
2011 [5]	Direct growth on Si with SPL dislocation filters	(1) Can be scaled up to 12" wafer	(1) Very high TDD $\sim 10^7 \text{cm}^{-2}$ (2) Off-cut substrate
2013 [6]	Via CVD Ge/Si	(1) Can be scaled up to 12" wafer	(1) High TDD $\sim 10^6 \text{cm}^{-2}$ (2) Off-cut substrate
2013	Via the GeOI substrate	(1) Can be scaled up to 12" wafer (2) Low TDD < 10^5cm^{-2} (3) Thin buffer < 1 μm	(1) Off-cut substrate

6.2 Device Growth and Fabrication

The layer structure of the InAs QD LED is shown in Figure 6.3. The active core region consists of 5 periods of InAs QDs capped by a 5nm InGaAs strain-reducing layer (SRL) and separated by a 33 nm GaAs spacer layer. The pre-growth sample preparations and growth conditions were presented in detail in Section 4.2.

Figure 6.3 The schematic LED device structure on the GeOI substrate.

The as-grown sample was processed into an edge-emitting ridge waveguide structure with a ridge width of 20 μm and a ridge height of 1.3 μm . The fabrication steps are illustrated in Figure 6.4. Prior to fabrication, the as-grown sample was cleaned with acetone, isopropyl alcohol (IPA), and de-ionized (DI) water. Subsequently, a photoresist

was spun on the wafer surface. The ridge waveguides and mesas were defined through ultraviolet (UV) exposure and photoresist developing. Wet chemical etching was used to define the etch depth or the ridge height. This was followed by a plasma-enhanced chemical vapor deposition (PECVD) of silicon dioxide (SiO_2) in order to planarize the sample. After planarization, the photoresist was spun on the sample to define the contact windows. The Ti/Au metal contact was deposited using the e-beam deposition technique and the photoresist was lifted off to form the metal contacts. The processed LED sample was thinned down to $\sim 150 \mu\text{m}$ via mechanical lapping using alumina powder (diameter $\sim 40 \mu\text{m}$). Subsequently, it was manually cleaved to form the light emitting facets.

Figure 6.4 Fabrication flow of the top-top contact ridge waveguide structure.

Prior to the growth and fabrication of the QD LED structure, the mode profiles of the light output were simulated using the Finite Difference Beam Propagation Method (FDBPM). The zero-order fundamental mode profiles simulated for devices with a ridge width $w = 4, 10, 20 \mu m$ are shown in Figure 6.5. Two transverse modes were simulated: (1) the transverse magnetic (TM) mode and (2) the transverse electric (TE) mode. As shown in the top part of Figure 6.5, the TM mode has no magnetic field in its direction and the TE mode has no electric field in its direction. The simulation results confirm that a waveguide dimension of ridge width $w = 4, 10, 20 \mu m$, and etch depth $h = 1.3 \mu m$ can effectively confine at least one fundamental mode. Although the first order mode is obtained for $w = 20 \mu m$, only the fundamental mode is considered in this project as higher order modes usually experience strong attenuation as they propagate along the waveguide.

Figure 6.5 Field plots of the calculated fundamental modes for waveguide structures of various dimensions.

6.3 Device Characterization

Figure 6.6 shows the current-voltage (I-V) plot of a 5-layer QD ridge waveguide LED device on a GeOI substrate which has a dimension of $20 \times 1500 \mu\text{m}^2$. The current-voltage characteristics of a typical diode are given by the Shockley diode equation:

$$J = J_{sat} \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (6.1)$$

where J is the current density, V is the voltage, J_{sat} is the reverse saturation current density, and n is the ideality factor. The reverse saturation current density at -2V is $3 \times 10^{-5} \text{ Acm}^{-2}$ with a rectification of 4×10^5 at $\pm 2\text{V}$. Comparing the results to the best diode reported on the GeOI substrate, the leakage current density is one order greater and the rectification is ~ 100 times poorer [16]. The diode exhibits a soft reverse breakdown from -5V. The ideality factor calculated from the forward current portion is approximately 2.8. For an ideal diode, the ideality factor is usually between 1 and 2. For an ideality factor greater than 2, it implies the presence of defect-related recombination centres at the diode junction.

Figure 6.6 The current density versus voltage for the InAs/InGaAs/GaAs QD LED on a GeOI substrate in log scale (a) and in linear scale (b).

To understand the origin of recombination centres, a cross-sectional TEM (XTEM) analysis was performed. As pointed out by the red arrows on the images in Figure 6.7, defects were identified within the active layers. The QD growth conditions used here deviated slightly from the optimized condition which was established and discussed in Chapter 4. The slight deviation from the optimized condition has led to the deterioration of the QD quality.

The light-current-voltage (L-I-V) characteristics of the LED, is shown in Figure 6.8. Using the experimental set-up as described in Section 2.2.4, the measurement was obtained under a continuous wave (CW) mode at a temperature of 25 °C with the use of an integrating sphere. The turn-on voltage is ~1.3 V, and the maximum power is 13.6 μW at 140 Acm^{-2} . For a current density exceeding 140 Acm^{-2} , the power drops as the current increases, due to thermal roll-over. Figure 6.9 shows the electroluminescence spectrum of an LED on a GeOI substrate at room temperature (25°C) under a CW current density of $J \sim 170 \text{ Acm}^{-2}$. An emission peak was found at 1312 nm with a linewidth of 56 nm.

Figure 6.7 The cross-sectional TEM images of the QD LED grown on the GeOI substrate. The left image shows the 5-layer InAs/InGaAs/GaAs QD active region while the inset shows a magnified QD. The right image, which was taken from the same sample, contains defects (indicated by the red arrows).

Figure 6.8 Light-current-voltage (L-I-V) characteristics of the InAs/InGaAs/GaAs QD LED on a GeOI substrate under CW mode at 25°C.

Figure 6.9 The spectrum for InAs/InGaAs/GaAs QD LED on a GeOI substrate at 25°C under a CW current density of $J \sim 170 \text{ Acm}^{-2}$.

From Figure 6.8, we notice that the light power emitted from the QD LED is very low. The maximum external quantum efficiency (η_{ext}), which is defined as the rate of photons emitted to free space over the rate of supply electrons, was calculated to be 0.01%. This value is considered very low for direct band gap materials since the η_{ext} for

direct band gap materials is usually greater than 1% [17, 18] and a high efficiency GaN-based LED with a $\eta_{ext} \sim 26\%$ has been demonstrated recently [19]. We believe the low η_{ext} is due to two reasons: firstly, the presence of defects; secondly, the rough cleaved facets. The defects in the active layer, as shown in Figure 6.7, are primarily responsible for the low efficiency as they promote non-radiative recombination. Furthermore, the unevenly cleaved facets pose a challenge for the future realization of QD laser on GeOI substrate. Figure 6.10 shows the cross-sectional scanning electron image of a cleaved device facet. The facet shows striations due to the crystallographic misorientation between the Ge layer and the Si substrate. This batch of samples was grown on the GeOI substrate for which the Ge layer was rotated 45 degrees from the Si holder substrate. Therefore, when the device was cleaved, it tended to follow the glide planes of a Si substrate.

Figure 6.10 A cross-sectional scanning electron image of a fabricated QD LED structure on a GeOI substrate.

Rough facets were proven to improve the light extraction efficiency of an LED [20]. However, this is not the case for a laser, where facet roughness can severely affect the facet reflectivity and cause a significant reduction in efficiency. Rough cleaved facets were obtained for InGaN/GaN laser and this led to poor reflectivity of the laser [21]. A model is proposed to theoretically describe the drop in reflectivity:

$$\frac{R}{R_o} = \exp \left[-16\pi^2 \left(\frac{n\Delta d}{\lambda_o} \right)^2 \right] \quad (6.2)$$

where R is the reflectivity of the rough facet, R_o is the reflectivity of a perfectly smooth facet, n is the refractive index, λ_o is the emission wavelength in vacuum, and Δd is the facet r.m.s. roughness. Based on the average facet roughness rms obtained from the AFM images (see Figure 6.11) $\Delta d = 18.4$ nm, the ratio of reflectivity is calculated to be $R/R_o = 0.7$. The uneven facet has led to a 30% drop in the reflectivity. To avoid this problem in future attempts in the fabrication of QD laser on GeOI substrates, the Ge layer should be aligned in exact orientation with the Si holder substrate during the production of GeOI substrates.

Figure 6.11 The AFM image for the cleaved facet of the QD LED on the GeOI substrate. (Scan area = $5 \times 5 \mu\text{m}^2$) The average roughness rms is 18.4 nm.

6.5 Summary

The first InAs/InGaAs/GaAs QD LED on GeOI was reported and discussed. The LED emits at 1312 nm with a linewidth of 56 nm. The maximum output power is only 13.6 μW . The maximum quantum efficiency equals to 0.01%. The value is low due to defects in the InAs QD active region. The GeOI substrate was found to be the one of the best choices for monolithic integration of III-V QD on the Si due to the low TDD and scalability. However, to obtain high performance QD laser, improvements are required to achieve defect-free QD active layers and smooth, mirror-like cleaved facets.

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Chapter 7 Conclusions and Recommendations

7.1 Conclusions

This thesis presents the progressive study of InAs QDs growth on Si-based substrate. This project started with the growth of InAs QDs on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. The QDs were grown on an undulated surface with a surface roughness rms of ~ 5.5 nm. The effects of undulations were discussed with the underlying concern that it may affect the dot morphology uniformity across the undulations. However, the experimental results showed that the QD morphology was insensitive to the surface undulation and the argument was supported by a simple mass transport model. The effects of the monolayer coverage and the V/III ratio were studied. It was found that at high InAs coverage of 3.0ML, the undesirable dot coalescence occurred. The QD density increases as the V/III ratio increases. At a V/III ratio of 15, a high QD density of $1.1 \times 10^{11} \text{ cm}^{-2}$ was obtained with a dot width of 29 nm and a dot height of 2.5 nm. This is the highest QD density achieved in literature for the InAs QDs on the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate. Although high density QDs can be obtained by tuning the QD growth parameters, the inherently high TDD of the graded $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ substrate ($\sim 10^6 \text{ cm}^{-2}$) has driven researchers to seek for alternative substrates.

In year 2009, the GeOI substrate became commercially available. The low TDD of less than 10^5 cm^{-2} makes it an attractive candidate for the monolithic integration for III-V on Si. In this thesis work, an APD-free GaAs buffer on a GeOI substrate can be consistently achieved. The effects of the QD growth temperatures were investigated. The dot density decreases and the dot size increases as the temperature increases. At high temperature of 480°C , a significant blue shift of 40 nm was observed. Through

introduction of a 5 nm thick $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ SRL, the emission wavelength was extended from 1.28 μm to 1.33 μm and the room temperature PL shows a narrow peak line width of 36.3 meV, which is so far the best reported photoluminescence result for InAs QDs grown on the GeOI substrate. The temperature-dependent PL analysis shows that strain-related defects are presence in the QD active layer but they can be suppressed by the introduction of the $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}$ SRL. The findings are similar to what we observe for the QD growth on the conventional GaAs substrate except that the QDs grown on the off-cut GeOI substrate are usually bimodal in size. This problem was discussed using the Kinetic Monte Carlo methodology. The simulation results explained that the occurrence of bimodal QD size distribution on a stepped substrate is due to difference in diffusion barriers across the substrate and the dot size uniformity can be improved by tuning the growth temperature and group V overpressure, which is in consensus with the experimental findings.

In the last chapter of the thesis, the InAs QD LED on GeOI was successfully demonstrated. This is the first reported LED on GeOI substrate. The 5-layer QD LED was fabricated into the edge-emitting ridge waveguide structure, with a ridge width of 20 μm and the ridge length of 1500 μm . The device emits at 1312 nm with a linewidth of 56 nm at 25°C. It has a turn-on voltage of 1.3V and a maximum power of 14 μW at 50 mA under CW mode. The external quantum efficiency is only 0.007%. The low efficiency is possibly caused by the defects in active layers and the roughness of the cleaved facets. Although the device performance still needs to be improved, the preliminary results are encouraging as it demonstrates the feasibility to obtain III-V QD LED on Si platform via the GeOI substrate.

7.2 Recommendations

More efforts are needed to improve the performance of the InAs QD LED or laser on the GeOI substrate. Firstly, obtaining a defect-free active layer is extremely crucial that may improve the external quantum efficiency by a few orders. As shown in Chapter 4, defect free QDs can be obtained by tuning the growth parameters. However, a slight deviation from the optimized condition can result in defects and lead to poor device performance, as what we experience in Chapter 6.

Secondly, the facet roughness is critical since the reduction in reflectivity is exponentially related to the facet roughness rms, as described in Equation 6.2. A high performance laser should have mirror-like facets. The device fabricated in Chapter 6 has rough cleaved facets because of the crystallographic mis-orientation between the Si substrate and the Ge epitaxy. Therefore, in the subsequent attempts, the mis-orientated GeOI substrate should be replaced by a GeOI substrate for which the Si substrate and the Ge layer are crystallographically aligned. Since the QD growth is carried out on an off-cut GeOI substrate, it is also important to understand the relationship between the degree of off-cut and the facet roughness, and how it affects the facet reflectivity and the device efficiency. Instead of manual cleaving, it is recommended to consider using reflective coating or employing other etching methods such as wet etching or dry etching, or a combination of both, in order to obtain highly reflective facets.

Lastly, the design of a QD laser structure needs to be further optimized. The QD laser on a GeOI substrate is more susceptible to the thermal rollover as the thermal insulating oxide layer is embedded in the substrate. A lower junction temperature can be

achieved by optimizing the ridge waveguide geometry in order to improve the heat extraction efficiency. The AlGaAs cladding can be fine tuned by varying the Al content and the cladding thickness to enhance the carrier confinement.

Other than the GeOI substrate, we should also consider new alternatives for the monolithic integration of III-V on Si. The GaAs-on-Si substrate through the epitaxy lift off process or other layer transfer techniques is still under development. This GaAs-on-Si platform has a great potential as it eliminates the need of growing GaAs on Ge, and thus, no off-cut is required. Such platform is more versatile and more readily accepted by the semiconductor industry.