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MONOLITHIC INTEGRATION OF GAAS-TO-SI
BY
DIRECT WAFER BONDING

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(B.Eng. (Hons), NTU)

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FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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SYSTEMS (AMM&NS)**

SINGAPORE-MIT ALLIANCE

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2013

DECLARATION

I hereby declare that this thesis is my original work
and it has been written by me in its entirety.

I have duly acknowledged all the sources of
information which have been used in the thesis.

This thesis has also not been submitted for any
degree in any university previously

Yeo Chiew Yong

22nd July 2013

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Abstract

While Silicon remains the dominant material today in matured very-large-scale-integration technology, most of the III-V compound semiconductors are direct bandgap materials with high electron mobilities that are highly sought in advanced space, automobile, and telecommunication applications. Hence, it would be ideal to integrate the best of Silicon and III-V compound semiconductors. In this research work, 2-inch Silicon and Gallium Arsenide wafers were integrated monolithically using the direct wafer bonding technology. A high specific bond energy of 1220 mJ/m^2 was achieved by developing the surface activation and the heat treatment stages. Cross-sectional high-resolution transmission electron microscopy revealed an abrupt, tight Silicon-to-Gallium Arsenide bonded interface. The present efforts coupled with the layer transfer technology realize a monolithic integrated versatile substrate of dual-generic platforms on which optoelectronics and microelectronics structures and devices can emerge.

Summary

Silicon (Si) has always been the dominant material in very-large-scale integration (VLSI) technology. However, further developments of VLSI technology are impeded by the indirect bandgap and low carrier mobility limitations inherent in the Si material. In contrast, III-V compound semiconductors are direct bandgap materials with high carrier mobilities that fit perfectly into space, automobile, and telecommunication applications. As it is highly impossible to outcast the matured and economics supremacy of the Si-based integrated circuit (IC), the III-V binary compounds can only serve to compliment the Si material in the VLSI technology by means of III-V-to-Si substrate engineering.

In this thesis, thick 2-inch GaAs and Si wafers were combined using direct wafer bonding technology. The main objective of this work was to achieve a high GaAs-to-Si bond energy to start with, so that the bonding pair could undergo subsequent process(es) to make either or both of the GaAs and the Si sides sufficiently thin for high temperature structural and device growth(s). The development of the GaAs-to-Si direct wafer bonding process was carried out by developing the surface activation and the heat treatment stages.

In the development of the GaAs-to-Si surface activation stage, Argon (Ar) plasma was used to hydrophilize the GaAs and Si bonding surfaces. The Ar plasma-activated direct wafer bonding (PADWB) of GaAs-to-Si experiments was based on a 2^3 full factorial design, and the specific bond energy results were interpreted through analysis-of-variance (ANOVA). It was found that an Ar plasma parameter set of 30 s of exposure time, 120 mTorr of pressure, and 200 W of radio frequency (RF) power was able to induce a strong hydrophilization effect on the bonding GaAs and Si surfaces, while maintaining a low surface roughness for good bondability.

The heat treatment stage of the GaAs-to-Si bonding process was developed through a simplistic novel annealing technique, in which an Ar PADWB of GaAs-to-Si pair was annealed from 20°C (room temperature) to 140°C through six identical incremental sequential steps under a high vacuum (10^{-6} Torr) condition. Each sequential step involved the ramping up of the temperature by 20°C at a rate of 1°C/min followed by dwelling the GaAs-to-Si bonding pair at the reached temperature for a duration of 24 h.

A high GaAs-to-Si specific bond energy of 1220 mJ/m² was achieved in this work. The GaAs-to-Si bonded interface was examined by high-resolution cross sectional transmission electron microscopy (HR-TEM) that revealed an abrupt, tightly bonded interface. Furthermore, energy-dispersive X-ray spectroscopy analysis confirmed the strong fusion between the GaAs and the Si. A GaAs-to-Si bonded pair that was prepared using the developed Ar plasma activation and sequential-step annealing recipes was demonstrated able to withstand a prolonged high-stress mechanical thinning process.

Ultimately, the present developed GaAs-to-Si bonding process serves to compliment the layer transfer technology to realize a monolithic GaAs-to-Si bonded substrate of thin GaAs and/or Si, through which the low-cost matured Si IC could be made to integrate with the high performing optoelectronics GaAs.

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Author's Publications

Publications in Refereed Journals:

C. Y. Yeo, D. W. Xu, S. F. Yoon, and E. A. Fitzgerald, "Low temperature direct wafer bonding of GaAs to Si via plasma activation," *Applied Physics Letters*, vol. 102, p. 054107 (4 pp.), 2013.

C. Y. Yeo, D. W. Xu, S. F. Yoon, and E. A. Fitzgerald, "Multiple-step annealing of plasma-activated direct wafer bonding of GaAs to Si under a high vacuum condition," *Applied Physics Letters*, (submitted)

Conference Presentations

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Chapter 1 Introduction

1.1 Motivation

Silicon (Si) is the dictating material for today's Integrated Circuit (IC) technology. Apart from being well known for its abundance and low cost, decades of enormous efforts focused on the Si IC technology realized the matured high performance of Si microelectronic devices. Furthermore, the present laboratories and manufacturing industry processes and equipment were largely designed and built based on the Si technology. These factors have rendered Si the leading material to date.

Despite the drastic growth in Si technology in terms of increasing transistor density, which leads to a higher performance as derived from Moore's Law, the cost associated with high performance microelectronics devices has decreased tremendously as well [1, 2]. However, one may ponder if Moore's Law will be violated at some point in time in the future, especially when the present transistors are approaching unrealistically small sizes. In addition, Si is a poor material for optoelectronics (OE) applications because it is an indirect bandgap material that absorbs and emits light inefficiently. Lastly, Si has a characteristic bandgap value of 1.12 eV at 300 K. Hence, different wavelengths of light derived from the Si pose a great challenge with perhaps limited success from strain engineering [3].

With the limitations that the Si material is experiencing, attention is being turned to other materials such as Germanium (Ge) and binary III-V compound semiconductors such as Gallium-Arsenide (GaAs), Indium-Phosphide (InP), and Gallium Antimonide (GaSb). Unlike Si, most of these materials are direct bandgap materials. This makes them attractive for optoelectronics applications. Since they are able to absorb and emit light efficiently, they are found in solar cells, light emitting diodes (LEDs), and light amplification by the stimulated

Chapter 1: Introduction

Table 1-1: Selected properties of Si, Ge, and commonly used III-V compounds at 300K.

	Si	Ge	GaAs	AlAs	GaSb	InAs	InSb
Crystal Structure	Diamond	Diamond	Zinc Blende	Zinc Blende	Zinc Blende	Zinc Blende	Zinc Blende
Nature of Bandgap	Indirect	Indirect	Direct	Indirect	Direct	Direct	Direct
E_g^a (eV)	1.12	0.67	1.43	2.15	0.72	0.36	0.17
a^b (nm)	0.5431	0.5658	0.5653	0.5661	0.6096	0.6058	0.6479
m_e^Γ/m_e^c (unitless)	0.188	0.038	0.067	0.124	0.039	0.024	0.013
μ_e^d (cm ² /Vs)	1750	4330	9340	294	12040	33000	77000
α_{th}^e (10 ⁻⁶ K ⁻¹)	2.616	5.75	6.03	4.28	6.35	5.50	5.04
K^f (W/cm.K)	1.56	0.60	0.45	0.91	0.36	0.30	0.175

^a Bandgap.^b Lattice constant.^c Electron effective mass at the Γ valley, m_e^Γ , being expressed as a ratio against the electron mass, m_e .^d Electron mobility.^e Linear thermal expansion coefficient.^f Thermal conductivity.

emission of radiation (LASER) devices. Above all, Ge and most of the III-V compounds have a lower electron effective mass, which can realize high electron mobility transistors (HEMTs). Table 1-1 shows some of the relevant properties of the Si, Ge, and commonly used III-V compounds at 300K [4].

Considering the pros and cons associated with the Si, Ge, and III-V compounds as listed in Table 1-1, it would be ideal to integrate them together heterogenously. This concept

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is also known as the three-dimensional (3D) integrated system. Combining 1) the low-cost and matured Si IC technology with 2) the high speed and OE applications associated with the Ge and III-V compounds may enable novel integrated devices of higher performance that will shift microelectronics into a whole new paradigm [5].

1.2 Background

Figure 1-1 illustrates the various techniques in heterogenous integration, which can be classified broadly under the hybrid type and the monolithic type. According to the Oxford Dictionary, a hybrid is “anything derived from heterogenous sources, or composed of different or incongruous elements [6].” This implies that individual platforms of Si IC and III-V OE serving different purposes are being electrically connected externally. On the other hand, “monolithic” is derived from the word “monolith” which means a “formed of a single (large) block of stone [6].” In the present context, monolithic refers to a single block of a generic substrate on which different platforms of different purposes are integrated together and electrical connections are made internally.

Figure 1-1: State of the art techniques in heterogenous integration.

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1.2.1 Wire Bonding Technology

The simplest form of heterogenous integration is to connect two individual platforms of dissimilar materials together electrically via conducting wires [7-9]. This form of hybrid integration is also known as 3D packaging, system-in-package (SiP), or multi-chip module (MCM). Despite its associated low-cost and simplicity advantages, hybrid integration via external wire interconnects is losing ground in the present heterogenous integration technology node. The present miniaturizing microelectronics devices are pushing for a much higher wire interconnects density. However, the density is saturating and may not be increased any further. The direct consequences of having an extremely high wire interconnects density are significant resistive-capacitive (RC) delay, strong parasitic capacitance, crosstalk issue, and immense heat generation. These consequences are hostile towards the electrical interconnect reliability and jeopardize device performance in terms of speed and clocking frequency.

1.2.2 Solder Bumping Technology

In view of the limitations that the wire bonding technology is facing, attention has been shifted towards the solder bumping technology [10-14] instead. This flip-chip technology was developed in the hope that devices can continue to shrink down in size while keeping the RC delay and parasitic capacitance to a low degree, which is essential in maintaining the speed and clocking frequency at a reasonable level. Moreover, the solder bumping technology has a winning edge over the wire bonding technology in terms of heat dissipation. The main limitation that lies in the flip-chip technology is the reliability issue that is associated with solder bumps. Solder bumps will often fracture due to a difference in the thermal expansion between the chip and the substrate or due to fatigue created by the heat cycles. Furthermore, from a scaling and manufacturing point of view, flip-chip technology

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yields a low throughput as it requires a stringent alignment and planarity of the chip and substrate. Since it is a parallel interconnection process, the selective replacement of failed bumps seems to be a challenging task.

1.2.3 Heterogenous Epitaxial Growth

Heterogenous epitaxial growth is a form of monolithic integration that involves the deposition of a film on a substrate of different material through techniques such as Molecular Beam Epitaxy (MBE) or Metalorganic Vapor Phase Epitaxy (MOCVD) wherein the film and substrate are lattice mismatched to each other. The difference in the lattice constant between the film and the substrate signifies that a misfit-induced elastic strain must evolve and be borne by the film to a large extent since the film is much thinner than the substrate bulk. From a device performance standpoint, such a coherency strain will bring about an enhancement in the carrier mobility which will improve the metal-oxide-semiconductor field-effect transistor (MOSFET) performance [15]. Moreover, elastic strain will induce deep pseudo-Fermi levels in the conduction and valence bands, which is critical in an efficient lasing operation [16]. Unfortunately, such a layer cannot be grown indefinitely as a high density of threading dislocations will be evolved that are detrimental towards the performances of devices [17-21]. Perhaps the only successful breakthrough of monolithic integration via heterogenous epitaxial growth was through the concept of the quasi-linear composition grading of $\text{Si}_x\text{Ge}_{1-x}$ [22, 23]. Since the Ge is lattice-matched to a number of III-V compound semiconductors, optoelectronics devices such as LED, LASER, and the solar cell on Si platforms have emerged [24-30].

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1.2.4 Wafer Bonding Technology

One could view the wafer bonding technology as a process through which two or more platforms of different materials serving different purposes could be phenomenally combined into a single monolithic compelling substrate. Wafer bonding allows the integration of dissimilar materials of different crystal types, orientations, and lattices as opposed to heterogenous epitaxial growth. Owing to this supremacy, the wafer bonding technology has opened up vast opportunities to integrate almost any kinds of materials. As an extreme example, the bonding of single crystalline Si to amorphous glass [31-33] has realized advanced micro-electro-mechanical systems (MEMS) such as the radio frequency (RF) MEMS switch for space satellite application [34] and the microscopic microfluidic system for biological study [35]. Moreover, since the wafer bonding technology is able to combine two platforms of severe lattice-mismatched materials, GaAs OE layers on a Si bipolar complementary metal oxide semiconductor (BiCMOS) substrate have been demonstrated [36] and a novel triple junction solar cell device has emerged [37]. Moreover, the typical wafer bonding process is fairly simple and compatible with the present Si technology. Neither sophisticated nor special equipment are required to carry out the entire bonding process, except for in situations where superior bond quality is required. Hence, wafer bonding can be seen as a versatile heterogenous integration technique. Lastly, wafer bonding is a low-cost process, which does not affect a device performance significantly. This is due to the nature that the bonding can be carried out at a wafer-scale. Moreover, with the advanced accompanying technology of layer transfer such as Smart-CutTM [38], the cost of wafer bonding can be reduced as the substrates can be recycled for subsequent process cycles. Hence, significant economical leverage can be made upon the wafer bonding technology.

1.3 Research Gaps and Objectives

The coefficient of thermal expansion (CTE) mismatches among dissimilar materials has remained the main obstacle in the development of the wafer bonding technology. Most of the bonding research efforts appear to be restricted to homogenous bonded systems such as Si-to-Si [39]. This has defeated the essence of the monolithic integration since the different properties that are associated with the various semiconductor materials cannot be leveraged through a single block of heterogenous generic substrate. For example, GaAs is a direct bandgap III-V compound semiconductor material that exhibits high electron mobility, whereas Si remains the dominant material in the present, matured IC technology. Hence, it would be ideal if the two materials could be bonded together to offer a single block of a substrate with dual-generic platforms on which the OE and IC devices can be coupled.

Unfortunately, GaAs and Si have a serious thermal expansion incompatibility. The CTE value of GaAs is greater than that of Si by a factor of about 2.4 (see Table 1-1). Hence, a GaAs-to-Si bonded pair cannot be subjected to a high temperature condition. On the other hand, high GaAs-to-Si bond energies and structural and device growth processes generally involve high temperature conditions. One way to accommodate the two opposing thermal requirements is to bond GaAs with Si at a die-scale ranging from millimeters to centimeters in size [40-42]. However, such die-scale bonding will jeopardize the economics of scale and the associated cost will not be reduced significantly.

Alternatively, a pair of GaAs-to-Si bonded wafers can withstand high temperature conditions if either the GaAs wafer or the Si wafer (or both the wafers) is sufficiently thin [42-44]. However, most of the thin layer transfer techniques (refer to Section 2.4) require the bond energies of the starting, thick GaAs-to-Si bonded wafers pairs to be sufficiently high before the bonded pairs can withstand subsequent harsh mechanical or/and chemical thinning processes. As an example of realizing a GaAs-to-Si-on-insulator substrate through a lateral

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etching epitaxial lift-off process (refer to Figure 2-10) [45, 46], the process requires the bond energy to be very high so that the bonded interface can endure the prolonged hydrofluoric (HF) acidic treatment.

In light of the foregoing, the present research aims to integrate a pair of thick, thermally-mismatched GaAs and Si wafers together monolithically by using the wafer bonding technology. This could yield a sufficiently high bond energy that enables the bonded pair to withstand subsequent thinning process(es).

1.4 Major Contributions of this Thesis

A typical direct wafer bonding process generally consists of three stages in sequential order: 1) surface preparation, 2) surface activation, and 3) thermal treatment. The present research focuses on developing the surface activation and the thermal treatment stages to achieve a high GaAs-to-Si specific bond energy. As such, the major contributions of this thesis are:

In the development of the surface activation stage,

- 1) A set of Ar plasma activation experiments based on a 2^3 full factorial statistical design was performed. The GaAs-to-Si specific bond energy data were interpreted through the analysis of variance (ANOVA).
- 2) It was found that the interactions among the considered Ar plasma parameters of exposure time, pressure, and radio frequency (RF) power will affect the surface roughness and the hydrophilicity of the bonding GaAs and Si surfaces. In return, these factors interactions will affect the GaAs-to-Si specific bond energy.
- 3) The Ar plasma conditions set of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power was found to yield the highest GaAs-to-Si specific bond energy.

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In the development of the thermal treatment stage,

- 1) A simplistic novel heat treatment technique was developed to assuage the negative effect of the thermal-mismatch peeling stress by having an Ar plasma-activated GaAs-to-Si bonding pair annealed in a series of increasing sequential steps.
- 2) A heating system was built manually to carry out the sequential-step annealing under a high vacuum condition.
- 3) It was demonstrated that, after 140°C of annealing, the use of the sequential-step annealing technique improved the GaAs-to-Si specific bond energy dramatically compared to the use of the conventional one-step annealing technique (in which the temperature is ramped up within a single step to a certain value at which a GaAs-to-Si bonding pair is dwelled for a period).
- 4) The enhancement in the bond energy by annealing a GaAs-to-Si bonding pair under a vacuum condition was found to be possible only when sequential-step annealing was performed.
- 5) The total number of identical incremental steps in a sequential-step annealing process (from 20°C to 140°C) was identified to be able to affect the GaAs-to-Si specific bond energy.
- 6) The holding duration during the dwelling stage in each of the identical steps of a sequential-step annealing process (from 20°C to 140°C) was identified to be able to affect the GaAs-to-Si specific bond energy.
- 7) Qualitative mechanisms of the one-step and the sequential-step annealings were proposed to account for the experimental observations.

In the assessment of the GaAs-to-Si pair that was bonded through the developed Ar plasma activation and sequential-step annealing processes,

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- 1) A high specific bond energy of 1220 mJ/m^2 in the direct wafer bonding of GaAs-to-Si was successfully achieved.
- 2) A cross-sectional high-resolution transmission electron microscopy (HR-TEM) image of the bonded interface of the GaAs-to-Si was obtained. The image revealed an abrupt bonded interface that justified the high bond quality.
- 3) The integrity of the GaAs-to-Si bonding was further justified when GaAs fractured remains were found to stay strongly fused to the Si when the bonded pair was completely cleaved apart. This was confirmed by the EDX analysis.
- 4) Both the GaAs and the Si of a sequential step annealed Ar plasma-activated GaAs-to-Si bonded pair were mechanically thinned down. The GaAs was polished down from a thickness of $453 \pm 1 \text{ }\mu\text{m}$ to a final thickness of $64 \pm 3 \text{ }\mu\text{m}$ via chemical mechanical polishing. The Si was lapped down from a thickness of $289 \pm 1 \text{ }\mu\text{m}$ to a final thickness of $62 \pm 6 \text{ }\mu\text{m}$. A low representative roughness and a low roughness variation of the root mean square (RMS) values of 1.72 nm and 0.09 nm, respectively, were achieved on the polished GaAs backside.

1.5 Organization of this Thesis

This thesis is organized into seven chapters.

Chapter 1 contained the motivation behind this research and the background that spurs the interest in heterogenous integration and justifies why direct wafer bonding is the key form of technology for this kind of integration. Subsequently, research gaps were identified to establish the present research objectives. Lastly, the major contributions of the current work were highlighted.

In Chapter 2, the necessary background on which the present direct wafer bonding development can be built on is described. The sequential stages in a typical direct wafer

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bonding process and the various low temperature bonding solutions are discussed in detail. The chapter concludes with a review on the state-of-the-art of layer transfer technology.

Chapter 3 contains the methodologies used in the current work. These include 1) the details of a GaAs-to-Si bonding process, 2) the self-improvised vacuum annealing system, and 3) the characterization techniques such as atomic force microscopy (AFM), contact angle measurement (CAM), and infrared (IR) optical transmission imaging.

In Chapter 4, a statistical study on the Ar plasma activation process in the bonding of GaAs-to-Si is presented.

Chapter 5 contains a description of the studies on the various GaAs-to-Si heat treatments, which include the conventional one-step and the novel sequential-step annealing under a normal atmospheric and high vacuum condition.

In Chapter 6, the quality of the GaAs-to-Si bond that was derived from the developed Ar plasma activation and sequential-step annealing processes is justified. Furthermore, a demonstration showing that the developed GaAs-to-Si bonded pair was able to withstand a prolonged mechanical thinning process is also included in this chapter.

Chapter 7 contains the main findings from the present research work and the directions for future research concerning how the developed GaAs-to-Si bonding processes can be exploited.

Figure 1-2: The outline of the present research.

References

- [1] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, iss. 1, pp. 82-5, 1998.
- [2] K. Flamm, "Moore's law and the economics of semiconductor price trends," *International Journal of Technology, Policy and Management*, vol. 3, iss. 2, pp. 127-41, 2003.
- [3] C. W. Wong, X. Yang, P. T. Rakich, S. G. Johnson, M. Qi, Y. Jeon, G. Barbastathis, and S.-G. Kim, "Strain-tunable photonic band gap microcavity waveguides in silicon at 1.55 μm ," in *Tuning the Optical Response of Photonic Bandgap Structures*, vol. 5511, pp. 156-64, Aug. 4, 2004 - Aug. 5, 2004, Denver, CO, United States.
- [4] S. Adachi, P. Capper, S. Kasap, and A. Willoughby, *Properties of Semiconductor Alloys [electronic resource] : Group-IV, III-V and II-VI Semiconductors*: Hoboken : John Wiley & Sons, Ltd., 2009.
- [5] M. Alexe and U. Gösele, *Wafer bonding : applications and technology / M. Alexe, U. Gösele (eds.)*: Berlin ; New York : Springer-Verlag, 2004.
- [6] *Oxford English Dictionary [electronic resource]*: [Oxford, England] : Oxford University Press, 2000.
- [7] O. L. Anderson, H. Christensen, and P. Andreatch, "Technique for connecting electrical leads to semiconductors," *Journal of Applied Physics*, vol. 28, iss. 8, p. 923, 1957.
- [8] A. Coucoulas, "Ultrasonic welding of aluminum leads to tantalum thin films," *Metallurgical Society of American Institute of Mining, Metallurgical and Petroleum Engineers -- Transactions*, vol. 236, iss. 4, pp. 587-89, 1966.
- [9] B. Krenik, D. Buss, and P. Rickert. (May 21, 2005). *Choose the best IC integration method when designing a 3G handset* Available: <http://eetimes.com/design/power-management-design/4009380/Choose-the-best-IC-integration-method-when-designing-a-3G-handset>
- [10] M. Abtew and G. Selvaduray, "Lead-free solders in microelectronics," *Materials Science & Amp; Engineering R: Reports*, vol. R27, iss. 5-6, pp. 95-141, 2000.
- [11] J. S. Hwang, "Overview of lead-free solders for electronics and microelectronics," in *Proceedings of Surface Mount International*, pp. 405-21, Aug. 28 - Sep. 1, 1994, Edina, MN, USA.
- [12] Z. W. Zhong, T. Y. Tee, and J. E. Luan, "Recent advances in wire bonding, flip chip and lead-free solder for advanced microelectronics packaging," *Microelectronics International*, vol. 24, iss. 3, pp. 18-26, 2007.
- [13] M. K. Md Arshad, U. Hashim, and M. Isa, "Under bump metallurgy (UBM) - A technology review for flip chip packaging," *International Journal of Mechanical and Materials Engineering*, vol. 2, iss. 1, pp. 48-54, 2007.
- [14] L. Chengkuo, H. Wei-Feng, and S. Jin-Shown, "Wafer bonding by low-temperature soldering," in *EUROSENSORS*, vol. A85, pp. 330-4, Sep. 12 - Sep. 15, 1999, Switzerland.
- [15] M. L. Lee and E. A. Fitzgerald, "Hole mobility enhancements in nanometer-scale strained-silicon heterostructures grown on Ge-rich relaxed Si_{1-x}Ge_x," *Journal of Applied Physics*, vol. 94, iss. 4, pp. 2590-6, 2003.
- [16] J. P. Loehr, *Physics of strained quantum well lasers / John P. Loehr*: Boston : Kluwer Academic, 1998.
- [17] C. L. Andre, A. Khan, M. Gonzalez, M. K. Hudait, E. A. Fitzgerald, J. A. Carlin, M. T. Currie, C. W. Leitz, T. A. Langdo, E. B. Clark, D. M. Wilt, and S. A. Ringel,

Chapter 1: Introduction

- "Impact of threading dislocations on both n/p and p/n single junction GaAs cells grown on Ge/SiGe/Si substrates," in *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference 2002*, pp. 1043-6, May 19 - May 24, 2002, Piscataway, NJ, USA.
- [18] H. Ito, O. Nakajima, T. Furuta, and J. S. Harris, Jr., "Influence of dislocations on the DC characteristics of AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Electron Device Letters*, vol. 13, iss. 5, pp. 232-4, 1992.
- [19] T. Wosinski, "Electrical activity of misfit dislocations in GaAs-based heterostructures," *Semiconductor Physics Quantum Electronics & Optoelectronics*, vol. 6, iss 1, pp. 58-61, 2003.
- [20] S. Sakai and N. Wada, "Monolithic III-V light-emitting devices on Si substrates," *Fiber and Integrated Optics*, vol. 13, iss 1, pp. 31-44, 1994.
- [21] Y. B. Bolkhovityanov and O. P. Pchelyakov, "GaAs epitaxy on Si substrates: modern status of research and engineering," *Physics-Uspekhi*, vol. 51, iss. 5, pp. 437-56, 2008.
- [22] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Applied Physics Letters*, vol. 72, iss. 14, pp. 1718-20, 1998.
- [23] E. A. Fitzgerald, Y. H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. J. Mii, and B. E. Weir, "Totally relaxed $\text{Ge}_{x-1}\text{Si}_x$ layers with low threading dislocation densities grown on Si substrates," *Applied Physics Letters*, vol. 59, iss. 7, pp. 811-3, 1991.
- [24] J. A. Carlin, S. A. Ringel, E. A. Fitzgerald, M. Bulsara, and B. M. Keyes, "Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates," *Applied Physics Letters*, vol. 76, iss. 14, pp. 1884-6, 2000.
- [25] K. Chilukuri, M. J. Mori, C. L. Dohrman, and E. A. Fitzgerald, "Monolithic CMOS-compatible AlGaInP visible LED arrays on silicon on lattice-engineered substrates (SOLES)," *Semiconductor Science and Technology*, vol. 22, iss. 2, pp. 29-34, 2007.
- [26] M. E. Groenert, C. W. Leitz, A. J. Pitera, V. Yang, H. Lee, R. J. Ram, and E. A. Fitzgerald, "Monolithic integration of room-temperature cw GaAs/AlGaAs lasers on Si substrates via relaxed graded GeSi buffer layers," *Journal of Applied Physics*, vol. 93, iss. 1, pp. 362-7, 2003.
- [27] O. Kwon, J. Boeckl, M. L. Lee, A. J. Pitera, E. A. Fitzgerald, and S. A. Ringel, "Growth and properties of AlGaInP resonant cavity light emitting diodes on Ge/SiGe/Si substrates," *Journal of Applied Physics*, vol. 97, iss. 3, pp. 34504-1, 2005.
- [28] K. L. Lew, S. F. Yoon, W. K. Loke, H. Tanoto, C. L. Dohrman, D. M. Isaacson, and E. A. Fitzgerald, "High gain AlGaAs/GaAs heterojunction bipolar transistor fabricated on SiGe/Si substrate," *Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures)*, vol. 25, iss. 3, pp. 902-5, 2007.
- [29] S. A. Ringel, J. A. Carlin, C. L. Andre, M. K. Hudait, M. Gonzalez, D. M. Wilt, E. B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E. A. Fitzgerald, and C. W. Leitz, "Single junction InGaP/GaAs solar cells grown on Si substrates with site buffer layers," *Progress in Photovoltaics: Research and Applications*, vol. 10, iss. 6, pp. 417-26, 2002.
- [30] V. K. Yang, M. E. Groenert, G. Taraschi, C. W. Leitz, A. J. Pitera, M. T. Currie, Z. Cheng, and E. A. Fitzgerald, "Monolithic integration of III-V optical interconnects on Si using SiGe virtual substrates," *Journal of Materials Science: Materials in Electronics*, vol. 13, iss. 7, pp. 377-80, 2002.
- [31] J. Byeong-Kwon, K. Chang-Gi, L. Yun-Hi, K. In-Byeong, P. White, N. Samaan, M. Haskard, and O. Myung-Hwan, "A study on low temperature bonding of glass-silicon

Chapter 1: Introduction

- using modified direct bonding method," *Transactions of the Korean Institute of Electrical Engineers*, vol. 46, pp. iss. 3, 450-5, 1997.
- [32] T. K. Chuang, A. Usenko, and J. S. Cites, "The study of the bonding energy on silicon-to-glass wafer bonding," in *Semiconductor Wafer Bonding 11: Science, Technology, and Applications - In Honor of Ulrich Gosele - 218th ECS Meeting*, vol. 33, pp. 501-7, Oct. 10 - Oct. 15, 2010, Las Vegas, NV, United States.
- [33] Q. Y. Tong, U. Gosele, T. Martini, and T. Reiche, "Formation of ultrathin single crystalline Si on glass by low temperature wafer direct bonding," in *Proceedings of 1994 IEEE International SOI Conference*, pp. 53-4, Oct. 3 - Oct. 6, 1994, New York, NY, USA.
- [34] M. S. Giridhar, A. Jambhalikar, J. John, R. Islam, C. L. Nagendra, and T. K. Alex, "An X band RF MEMS switch based on silicon-on-glass architecture," *Sadhana - Academy Proceedings in Engineering Sciences*, vol. 34, iss. 4, pp. 625-31, 2009.
- [35] N. F. Raley, J. C. Davidson, and J. W. Balch, "Examination of glass-silicon and glass-glass bonding techniques for microfluidic systems," in *Micromachining and Microfabrication Process Technology*, vol. 2639, pp. 40-5, Oct. 23 - Oct. 24, 1995, USA.
- [36] A. Georgakilas, G. Deligeorgis, E. Aperathitis, D. Cengher, Z. Hatzopoulos, M. Alexe, V. Dragoi, U. Gosele, E. D. Kyriakis-Bitaros, K. Minoglu, and G. Halkias, "Wafer-scale integration of GaAs optoelectronic devices with standard Si integrated circuits using a low-temperature bonding procedure," *Applied Physics Letters*, vol. 81, iss. 27, pp. 5099-101, 2002.
- [37] J. M. Zahler, H. A. Atwater JR., and A. F. i. Morral, "GaInP/GaAs/Si Triple Junction Solar Cell Enabled by Wafer Bonding and Layer Transfer," US 2006/0021565 A1, 2006.
- [38] Q.-Y. Tong and U. M. Gosele, "Wafer bonding and layer splitting for microsystems," *Advanced Materials*, vol. 11, iss. 17, pp. 1409-25, 1999.
- [39] M. Reiche, "Semiconductor wafer bonding," *Physica Status Solidi A*, vol. 203, iss. 4, pp. 747-59, 2006.
- [40] K. Tanabe, K. Watanabe, and Y. Arakawa, "III-V/Si hybrid photonic devices by direct fusion bonding," *Scientific Reports*, vol. 2, iss. 349, DOI:10.1038/srep00349, 2012.
- [41] Q. Y. Tong, "Wafer bonding for integrated materials," *Materials Science and Engineering B: Solid-State Materials for Advanced Technology*, vol. 87, iss. 3, pp. 323-8, 2001.
- [42] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [43] M. Alexe, V. Dragoi, M. Reiche, and U. Gosele, "Low temperature GaAs/Si direct wafer bonding," *Electronics Letters*, vol. 36, iss. 7, pp. 677-8, 2000.
- [44] V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gosele, "Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 12, pp. 2141-3, 1989.
- [45] E. Yablonovitch, T. Gmitter, J. P. Harbison, and R. Bhat, "Extreme selectivity in the lift-off of epitaxial GaAs films," *Applied Physics Letters*, vol. 51, pp. 2222-4, 1987.
- [46] M. M. A. J. Voncken, J. J. Schermer, G. J. Bauhuis, A. T. J. van Niftrik, and P. K. Larsen, "Strain-accelerated HF etching of AlAs for epitaxial lift-off," *Journal of Physics: Condensed Matter*, vol. 16, pp. 3585-96, 2004.

Chapter 2 Literature Review

2.1 The Basics of Wafer Bonding

To understand and appreciate the phenomenon behind wafer bonding, it may be worthwhile to ponder why broken pieces from a bulk cannot be joined and pieced back together spontaneously. It is well known that the friction of a surface is in positive correlation with the surface roughness. However, in 1734, Desaguliers discovered that, as the frictions of two surfaces decrease with decreasing surface roughness, the frictions reach a critical point whereby the surfaces are so smooth that the pair will adhere to each other spontaneously as a result of a spike increment in the friction [1]. It was not until 1936 that Lord Rayleigh clearly demonstrated the phenomenon of bonding through two atomically smooth glass samples [2]. However, the reported bond strength of 100 mJ/m^2 was too low to be of any practical use. It was not until the mid-1980s that the strong desire for miniaturized high performance devices pushed for a development in wafer bonding technology that can realize monolithic integration. Thus, several pioneer works emerged [3, 4].

A typical wafer bonding process consists of three main stages:

Stage 1: *Surface preparation*

The bonding surfaces are cleaned through chemical means, mainly to reduce the degree of organic contamination.

Stage 2: *Surface activation and room temperature contact*

This stage terminates bonding surfaces with reactive species. When the wafers pair are brought together, strong physical forces will hold the bonding pair together.

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Stage 3: *Heat treatment*

Interfacial chemical reactions take place during this stage and the wafer pair is bonded together by strong inter-covalent bonds.

2.1.1 *The Physical Requirements of Bonding Wafers*

In a wafer bonding process, the starting point of establishing the bonding wafers planarity at a microscopic and a macroscopic level is of great importance. Macro planarity refers to the extent of wafer flatness while micro planarity refers to the degree of surface smoothness. Both will impair the bond quality in terms of reducing the bond energy and the bond efficiency, although the respective scales of dimension are different.

Wafer flatness is a global bulk property of a wafer that is characterized through the total thickness variation (TTV), the bow, and the warp of the wafer, which the definitions of these terms can be found in [5]. Generally, micron scales of dimension of the flatness parameters are required from each wafer of a bonding pair to achieve a good bonding. The macro non-planarity of the wafers of a bonding pair will generally result in large areas of unbonded regions that range readily from millimeter to centimeter scale. However, when the bonding surfaces are not flat to a small extent, a strong physical Van der Waals force could still pull the bonding pair together. Upon elastic deformations of the bonding wafers, the unbonded regions will be closed up [6]. The closing up of an unbonded region was mathematically treated in [7] and was found to be dependent on 1) the strength of the physical bonding force, 2) the degree of the wafers' non-planarity, 3) the wafers' Young's moduli, and 4) the wafers' thicknesses. In general, a pair of bonding wafers that have a TTV of less than 3 μm and a bow and a warp of less than 25 μm are able to attain a reasonably good degree of bond efficiency [8].

Figure 2-1: A schematic diagram showing (a) the bonding of two perfectly flat wafers and (b) the microscopic view of the bonding interface in which the bonding surfaces are rough.

Micro wafer planarity is characterized through the surface roughness, which is a microscopic parameter that quantifies the extent of a localized surface non-planarity. Surface roughness is commonly abbreviated as R_q , which is a root mean square (RMS) value of the heights being measured across a defined region. In a bonding process, the oppositely surface reactive species of a bonding pair have to be close enough before they can react during the annealing stage (see Figure 2-1). The few pairs of red-highlighted oppositely -OH groups in Figure 2-1(b) can be polymerized as they are in close-proximity. However, the numerous pairs of green-highlighted oppositely -OH groups in Figure 2-1(b) cannot be polymerized as they are too far apart from each other. Hence, the roughness of the bonding surfaces should have a dimension down to a molecular or even an atomic level for the reactions among the oppositely surface reactive species to proceed. In general, R_q values of less than 5 Å RMS are low enough for surface reactive species to be in close proximity to react [9]. More accurate modeling of the effects of the surface roughness on the bond quality can be found in [10, 11].

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2.1.2 The Influence of Particles

In bonding, the cleanliness of the wafers of a bonding pair is also a stringent requirement. The surfaces of the bonding wafers must be free from particle residues before the wafers are contacted together. In a situation where there is a particle residing at a bonding interface, the bonding wafers will try to deform elastically to conform to the shape of the particle as far as possible because the wafers are being pulled together by a physical bonding force. However, due to the stiffness and the thicknesses of the bonding wafers, the unbonded region will generally develop an area of a dimension much larger than the size of the interfacial residual particle (see Figure 2-2). Hence, the bond efficiency will be greatly reduced. A mathematical model in [7] indicates that the unbonded region size tolerance towards an interfacial residual particle of a certain size will be larger if the bond energy is higher and the stiffnesses and thicknesses of the bonding wafers are lower.

Figure 2-2: (a) An infrared image of a GaAs-to-Si bonded pair that has an unbonded region of diameter R as a result of a particle of size r as illustrated in (b), where $R \gg r$.

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Particles residing on bonding surfaces can be avoided easily if the bonding process is carried out in a cleanroom of class 10 or below (although class 100 is barely tolerable). At Duke University, a novel micro-cleanroom setup has been devised through which a bonding process can be performed outside a cleanroom condition. The details are contained in [12].

2.1.3 The Surface Preparation Stage

Figure 2-3 displays an infrared (IR) image of a 2-inch GaAs-to-Si bonded pair that was annealed at 140°C for a long period. A large amount of interfacial voids evolved after the annealing. Such interfacial voids are also observed in the direct wafer bonding of Si-to-Si pairs [13]. The origin of interfacial voids was initially thought to be the water by-products from the polymerization reactions during annealings [4, 14]. Presently, it is widely accepted that the evolved interfacial voids originate from organic contaminants instead. Organic contaminants are hydrocarbons of various chain lengths that may exist 1) on wafer surfaces, 2) within deposited or native oxides, and/or 3) are trapped at the oxide-bulk interfaces [15-17]. During an annealing process, a series of cracking events of a long-chain hydrocarbon will take place, which will result eventually in short-chain hydrocarbons of extremely low boiling points. The short-chain hydrocarbons can act as nucleation sites at which diffusing hydrogen and other hydrocarbons are entrapped, which leads to voids growth.

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Figure 2-3: The IR image of a GaAs-to-Si bonded pair with a high amount of interfacial bubbles.

A Standard Cleaning (SC), more commonly known as a Radio Corporation of America (RCA) cleaning, is often performed to reduce the amount of organic contaminants [18]. The recipe of a conventional RCA cleaning is shown in Table 2-1. It involves the use of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), hydrofluoric acid (HF), and hydrochloric acid (HCl) chemicals.

Table 2-1: The recipe and the details of a conventional RCA cleaning.

Stage	Chemical	Parts by Volume	Process Temperature ($^{\circ}\text{C}$)	Process Duration (min)	Purpose
RCA-1	$\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$	1:1:5	75	10	Remove particle and organic contaminants
HF dip	$\text{HF}:\text{H}_2\text{O}$	1:50	25	0.25	Oxide strip
RCA-2	$\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$	1:1:6	75	10	Remove metallic contaminants

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As opposed to conventional RCA cleaning, it has been discovered that, when the HF dip stage is performed prior to the RCA-1 treatment stage, the organic contamination can be reduced to a larger extent [19]. Moreover, the NH_4OH will inevitably etch bonding surfaces to a certain extent. The etching is in positive correlation with the surface roughness that will affect the bonding [20]. It was reported that the use of a NH_4OH (28%): H_2O_2 (30%): H_2O solution in a ratio of 0.25:1:5 by volume will yield the best compromise between a high extent of organic contamination reduction and low extent of surface roughening. Alternative chemical cleanings include the use of a sulfuric acid (H_2SO_4) in place of the NH_4OH , and the use of a nitric acid based solution [20, 21]. Dry cleaning techniques include the pre-bonding annealing of the wafers of a bonding pair at an elevated temperature under a dry oxygen, argon, or normal ambient condition [16], and plasma bombardment [22, 23] or ultraviolet (UV)/ozone exposure [24, 25] on the bonding surfaces.

2.1.4 The Surface Activation Stage

Surface activation is a process through which reactive species are induced on bonding surfaces. First, surface activation processes be generally classified into two types: 1) wet activation and 2) dry activation. Wet activation involves attacking a bonding surface through chemical means, while dry activation inflicts physical damage onto a bonding surface. Both approaches will induce reactive species on bonding surfaces. Second, surface reactive species can also be generally classified into two types: 1) hydroxyl (-OH) and 2) hydrogen fluoride (-HF). A bonding surface that is covered with -OH reactive groups will become hydrophilic, whereas a bonding surface that is covered with -HF reactive groups will become hydrophobic.

The amount and the type of the reactive species that are incorporated on a bonding surface can be determined through the contact angle of a water droplet that is dispensed on

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the bonding surface. In the case of a hydrophilic bonding surface that is covered with the -OH type of reactive groups, a small contact angle, α , of less than 45° will be measured. In an extreme case of a super-hydrophilic surface where the contact angle is too small to be measured, a modified technique known as the inverted bubble can be considered. This technique is described in [26]. On the other hand, a hydrophobic bonding surface that is covered with the -HF type of reactive groups will yield a contact angle of more than 45° .

The wet chemical cleanings discussed in Section 2.1.3 will also activate bonding surfaces in-situ. The effects brought by the various chemical treatments on the degree of hydrophilicity can be found in [26], of which some common ones are shown in Table 2-2.

It has been demonstrated that hydrophilic wafer bonding yields a higher bond energy than hydrophobic wafer bonding does [27, 28]. Hence, the discussion from here onwards will only involve hydrophilic wafer bonding.

Table 2-2: Contact angle values for some common chemically-treated Si surfaces [26].

Chemical Treatment	Contact Angle
RCA-1 ^a	5
RCA-1 and RCA-2 ^b	25
Untreated reference	44
HF-dip	70

^a At boiling state.

^b At 95°C .

Figure 2-4: A schematic diagram that illustrates the two hydrophilization mechanisms on the native oxide surface of an arbitrary material, M.

The mechanism of inducing a hydrophilic state to a bonding surface as a result of -OH incorporation onto the surface was first reported by R.J. Charles in 1958 [29]. Charles' study was based on the fatigue of glass. Subsequently, a number of models were proposed in the attempt to account for the induced hydrophilicity [14, 30]. A model was eventually perfected by Q.Y. Tong et al. in 1996 and this model is widely accepted to date [31]. It was that the presence of hydrogen (H^+) and hydroxide (OH^-) ions in a chemical solution were responsible for the development of a silanol ($\equiv Si-OH$) terminated surface. The attack by the

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H^+ and OH^+ ions on a bonding surface was highly efficient due to the strained state of the native oxide ($[Si-O-Si]_{\text{native oxide}}$) [32]. The mean angle of the $(Si-O-Si)_{\text{native oxide}}$ of a Si surface that was treated in a base solution was found to be 130° [33]. This angle is different from the $(Si-O-Si)_{\text{native oxide}}$ mean angle of an equilibrium bulk oxide, which was 144° . The two hydrophilization processes by the H_2O and H^+ and OH^- ions that decompose the native oxide surface ($[M-O-M]_{\text{native oxide}}$) of an arbitrary material, M, into a surface that contains the -OH groups are illustrated in Figure 2-4.

2.1.5 Contacting a Pair of Hydrophilic bonding wafers

Consider a pair of hydrophilic bonding wafers where the surfaces are covered with -OH reactive groups. A large difference exists in the electronegativity between an oxygen atom and a hydrogen atom. Hence, a -OH group and a H_2O molecule will develop a dipole moment. Consequently, a few monolayers of water will be adsorbed on the hydrophilic bonding surfaces. When the pair of wafers are contacted together, hydrogen bonding between the -OH groups and the H_2O molecules will develop, which was evidenced from a high-resolution electron loss spectroscopy study [34]. Hence, hydrogen bonding is the main physical force that bonds a pair of wafers together after the wafers are contacted. It was reported in [27] that the specific bond energy that is derived from the hydrogen bonding mechanism will not exceed 200 mJ/m^2 normally.

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2.1.6 The Heat Treatment Stage

The bond energy of a bonded pair of wafers is highly sensitive to the annealing temperature. In the case of the bonding of a thermally-matched homogenous Si-to-Si pair, its bond energy can reach to about 2000 mJ/m² after a 900°C anneal [27]. The temperature ranges to be considered in the annealing of a Si-to-Si bonding pair are 1) room temperature (20°C) to 110°C, 2) 110°C to 150°C, 3) 150°C to 800°C, and 4) beyond 800°C [7, 31].

Room temperature (20°C) to 110°C: The bond energy will increase slightly with increasing temperature. Within this temperature range, two main events take place. First, a slow decomposition of the (Si-O-Si)_{native oxide} network continues. Consequently, the number of Si-OH species increases. Second, mobile water molecules restructure from a less stable network of weak physical hydrogen bonding to a more stable network of strong physical hydrogen bonding [35].

110°C to 150°C: The bond energy incremental rate is increased with increasing temperature. It was reported that water molecules on a hydrophilic surface can desorb readily only at temperatures in excess of 120°C [32, 36]. Hence, in the temperature range of 110°C to 150°C, the thermal effect is sufficiently high to enable the interfacial water molecules to break free from the hydrogen bonding and diffuse out from the bonded interface. Consequently, the oppositely -OH groups on the bonding surfaces can then come close enough to polymerize and result in strong chemical siloxane ([Si-O-Si]_{bonded interface}) bonds of oxygen bridges across the bonding interface [36, 37]. The polymerization process is as follows:

150°C to 800°C: All of the (Si-O-Si)_{bonded interface} that could possibly form would have been realized by 150°C. Hence, the annealing temperature has a negligible effect on the bond energy within this temperature range. The saturated bond energy value is limited by 1) the number of Si-OH groups on the bonding surfaces that can potentially be polymerized and 2) the surface roughness that determines how many of the oppositely Si-OH groups can be polymerized.

Beyond 800°C: The bond energy incremental rate is increased dramatically with increasing temperature. During the annealing at a temperature of more than 800°C, the less viscous native oxides of the bonding wafers will be mass transported to fill up the micro voids that arise from the surface roughness [38, 39]. The specific bond energy of a wet-activated hydrophilic bonded Si-to-Si after a 900°C anneal was found to be 2082 mJ/m² [7].

Although it was demonstrated that a full bond maturity was realized only with a very high temperature annealing at 900°C, the bonded interface after a 150°C anneal can also be made to be nearly matured by ensuring the bonding surfaces are 1) as smooth as possible and 2) hydrated to a large extent.

2.2 Low Temperature Plasma-Activated Wafer Bonding

High temperature annealings are often required to realize high bond energies as discussed in the Section 2.1.6. However, a high temperature annealing is unacceptable in the bonding of a pair of dissimilar materials that have different coefficients of thermal expansion (CTE). The evolved thermal-mismatch stresses will result in debonding or bulk fracture failure [40]. In the current efforts of bonding a GaAs wafer and a Si wafer, the CTE mismatch between the two materials is 2.4. Hence, the annealing of a GaAs-to-Si bonding pair in excess of 140°C will often lead to either debonding or a fracture result [7, 41, 42]. Other negative effects that are associated with high temperature annealings include, but are

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not limited to, the modification in a doping profile (which may broaden junction depth) and the diffusion of metal species (which may develop themselves as deep-level traps and/or cause distortion in the metallization patterns of pre-processed wafers). Hence, low temperature bonding solutions such as the ultraviolet (UV) activated wafer bonding [25, 43], the plasma-activated wafer bonding [21, 44], and bonding under a vacuum condition [45, 46] are required to recede from the aforementioned ill consequences.

Plasma-activated direct wafer bonding (PADWB) is a viable form of low temperature bonding [47-49]. The PADWB technique is able to attain a strong bond even after the room temperature contact stage without any further annealings because of the high degree of surface hydrophilicity that PADWB is able to induce to bonding surfaces. Moreover, good sustainability of the hydrophilicity state over time, a short annealing time to achieve an equivalent bond energy to that derived from a conventional wet activation bonding, and a fast bonding wave speed have also been observed associated with PADWB [50, 51]. Table 2-3 shows several studies in which the plasma parameters of the gas type, the radio frequency (RF) power, the exposure time, the pressure, the flow rate, and the voltage were investigated [21, 44, 52-55].

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Table 2-3: Investigated plasma parameters in plasma-activated direct wafer bonding (PADWB).

Reference	Plasma Conditions						Investigated Parameter
	Gas Type	Exposure Time (s)	Pressure (mTorr)	Flow Rate (sccm)	Power (W)	Voltage (V)	
[52]	Ar ^a	30-900	0.75	-	-	1200	Time
[53]	O ₂	5-10	15	6	100	-	- ^b
[21]	O ₂	1-20	90	100	100	300	Time
[54]	O ₂	15-240	200	100	300	-	Time
[55]	Ar	30	-	30	200	-	- ^b
[44]	Ar	10-600	50-150	30	50-150	125-280	Gas type and voltage

^a Neutralized high energy Ar atom beam.^b Plasma activation and RCA cleaning process sequence.

The bond enhancements brought by the PADWB technique can be attributed to the energetics of the plasma species, which will correspondingly lead to four positive outcomes [56]:

1. *The high degree of induced hydrophilicity*

The bond energy of a bonding interface is dependent on the initial amount of induced -OH groups on the bonding surfaces. The -OH groups can further be polymerized to evolve into interfacial oxygen bonds. The high degree of hydrophilicity of a bonding surface derived from a plasma treatment process was

found to cause by an increase in the surface area. This increase in surface area resulted from the surface roughening effect caused by the energetic plasma species. Hence, the amount of the surface -OH groups was increased such that a high bond energy could result even after the contact stage.

2. *The physical cleaning effect*

The energetics of the plasma species can remove the surface organic contaminants by cracking the hydrocarbons into short volatile chains that will desorb from a bonding surface. Hence, when the plasma treated wafers of a bonding pair are contacted together (and upon subsequent annealings), the oppositely -OH groups will be in close proximity, which is a requirement for polymerization (see Equation [2-1]) to proceed.

3. *The enhancement in the out-diffusion of water and gaseous species*

A plasma treatment process will inflict damages to a pair of bonding oxides by increasing their roughness and porosity. This damage will lead to a more open bonding interface structure that will provide low energy barrier paths for the out-diffusion of water and gaseous species away from the bonded interface. Consequently, the polymerization reaction of Equation (2-1) will be promoted by virtue of the *Le Chatelier's* principle, which implies that a higher amount of interfacial oxygen bridges will be evolved to result in a high bond energy.

4. *The ease of oxide viscous flow*

In conventional wet-activated wafer bonding, high annealing temperatures in excess of 800°C necessitate the viscous flow of bonding oxides to close up the micro-voids and realize a fully matured bonded interface. However, in the case of PADWB, the porosities of the bonding oxides will increase. As water molecules could reside in the porosities, the bonding oxides viscosity will be decreased

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accordingly. Hence, PADWB requires a much lower annealing temperature to initiate the viscous flow of the bonding oxides.

Most, if not all, reported PADWB studies were based on the homogenous Si-to-Si bonded system. The attractive low temperature bonding solution of the PADWB technique has yet to be exploited readily in heterogenous thermally-mismatched bonding systems such as GaAs-to-Si. Although extensive efforts have been devoted to understanding the effects brought by the individual plasma parameters on the bond quality, the effects from the plasma parameters interactions have not been considered. Moreover, most of the focus has been placed on investigating the effects brought by the exposure time and the gas type. Few researchers have considered the effects from the plasma pressure and the power. Nevertheless, the available literatures to date have established two important aspects worthy of consideration in a PADWB process: 1) the degree of the plasma-induced hydrophilicity and the 2) induced surface roughness.

2.3 The Effects of Vacuum in Direct Wafer Bonding

The presence of a vacuum condition during the room temperature contact and/or the annealing stage during a wafer bonding process sought to provide an attractive alternative solution for low temperature wafer bonding [57-59]. Through an extreme example, a covalently bonded interface can be achieved after the room temperature contact stage without a need for subsequent annealing [60]. This was possible when a pair of wafers were contacted under an ultra-high vacuum (3×10^{-6} mTorr) condition. The bond energy was estimated to be more than 2J/m^2 or $3.5 \times 10^7 \text{ N/m}^2$, which was higher by a factor of 10 than the bond energy that resulted from a conventional air contact. Furthermore, the bonding wave speed was estimated to be more than 1 m/s, which was 100 times faster than the wave speed in a conventional air contact. However, the requirement of having an UHV condition to achieve

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such an excellent bonding is largely impractical from a manufacturing point of view. The lengthy duration required to reach such a low vacuum level, the equipment complexity, and the associated high costs are examples of the UHV bonding downsides. Thus, a good balance would be to utilize a vacuum condition of a level between low to high, which ranges from 1 Torr to 10^{-8} Torr.

An extensive study was conducted to investigate the effects of the use of a low vacuum condition (2 Torr) in the bonding of Si-to-Si [45]. It was observed that the presence of a low vacuum during the room temperature contact stage and/or during the annealing stage will yield a higher bond energy compared to the presence of a normal ambient condition. A specific bond energy of 2700 mJ/m^2 was achieved when both the Si-to-Si bonding stages of the room temperature contact and the annealing (at 150°C for 60 h) were carried out under a low vacuum condition. The 2700 mJ/m^2 specific bond energy value was higher than the bond energy by a factor of more than 3 when both of the bonding stages were carried out under a normal ambient condition instead. It was proposed in the study that the enhancement in the bond energy by having a bonding pair of Si wafers room temperature contacted together under a low vacuum condition was because less air pockets remain trapped at the bonding interface. This condition is critical as the presence of any air pockets will impede the oppositely -OH groups from coming close enough to be polymerized. Moreover, the presence of a vacuum condition during subsequent annealings will act like a strong suction to lug any trapped air pockets and water and gaseous by-products out from the bonding interface. Thus, the presence of a vacuum condition will promote the polymerization process.

Intuitively, if the presence of a vacuum condition works to enhance the bond energy by minimizing the amount of interfacial trapped air pockets during the contact stage and by sucking out any trapped air pockets and by-products away from the bonding interface during

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Figure 2-5: A schematic illustration of (a) a well-hydrated activated surface of an arbitrary material, M, and (b) a dehydrated deactivated surface that is of an intra-oxygen bonded structure ($[M-O-M]_{\text{intra}}$).

annealing, then the bond energy should increase with an increasing vacuum level. However, this was not observed when a medium vacuum condition was used. [46] reported that, when the medium vacuum level was increased from 10^{-2} Torr to 10^{-4} Torr during the room temperature contact stage, the bond efficiency became poorer after the annealing stage. It was proposed that a favorable reverse polymerization reaction of Equation (2-1) occurs as the medium vacuum acts to dehydrate the hydrophilic -OH covered bonding surfaces. Consequently, the bonding surfaces evolves into an intra-siloxane surface structure of $(Si-O-Si)_{\text{intra}}$ instead, and the surfaces are deemed de-activated (see Figure 2-5).

Piecing together the main information from the reviewed literatures, optimum vacuum wafer bonding procedures can then be expected by having the initial room temperature contact stage carried out under a normal atmosphere condition followed by

performing the annealing stage under a high vacuum condition. The normal ambient room temperature contact ensures that the hydrophilicity of the bonding surfaces is well preserved with a large number of -OH groups to start with. Consequently, extensive polymerization can occur during subsequent annealings. Trapped air pockets can alternatively be reduced greatly by initializing the contact wave at the center of a bonding pair by means of a central point load [61]. The presence of a high vacuum during any subsequent annealings serves to drag out many of the trapped air pockets and by-products away from the bonding interface.

2.4 The State-of-the-Art of Layer(s) Transfer Technology

Wafer bonding technology is often coupled with layer transfer technology to realize on-insulator monolithic substrates. On-insulator devices do not experience issues that are associated with the parasitic capacitance and the low drain breakdown that is due to leakages derived from the latch-up and the avalanche effects. Moreover, on-insulator devices are well-received in the space and nuclear applications as they are of high radiation hardness

The application of the wafer bonding technology in the monolithic integration of dissimilar materials to couple III-V optoelectronics with a Si integrated circuit is emerging rapidly [62]. However, the obstinate obstacle of the CTE mismatches that are inherent in heterogenous bonded systems often impedes the development. To overcome the roadblock, it is necessary to make either or both sides of a bonded pair of dissimilar wafers sufficiently thin to surpass the debonding or the fracture failure during high temperature processes. As in the example of the GaAs-to-Si bonded system, the highest temperature that a GaAs-to-Si bonding pair can withstand was found to be 160°C when the thicknesses of the GaAs and the Si were 638 μm and 635 μm , respectively [7]. However, when the GaAs and the Si of a GaAs-to-Si bonding pair were thinned down to thicknesses of 89 μm and 145 μm , respectively, the bonding pair was found to withstand temperatures of more than 350°C.

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A comprehensive review of the coupling of the wafer bonding and the layer transfer technology is contained in [7]. The state-of-the-art of layer transfer technology in achieving thin device films in on-insulator bonded structures is summarized in Figure 2-6. A layer transfer process can generally be classified as a physical or a chemical type. Although most of the literature focused on achieving a very thin Si device layer in a silicon-on-insulator (SOI) bonded structure, the underlying concepts may also be extended in the fabrication of an on-insulator dissimilar bonded structure that consists of a thin arbitrary material A and a thick arbitrary material B (A-to-B-OI) (see Figure 2-6). The arbitrary A-to-B-OI structure of the thin A-layer will be used as a reference in the subsequent discussion of the present section.

In achieving a thin layer through a layer transfer process, some of the aspects worthy of consideration include: 1) the lowest thickness achievable, 2) the thickness uniformity, the process 3) repeatability, 4) robustness, 5) complexity, and 6) process-induced imperfections such as surface defects, contaminations, and roughness.

Figure 2-6: A classification of the layer transfer techniques in achieving a thin layer in an on-insulator dissimilar bonded structure.

2.4.1 The Mechanical Abrasion Thinning Technique

The most direct approach to achieving an A-to-B-OI structure of thin A-layer is through the physical mechanical abrasive action of lapping or grinding followed by polishing the bonded A-wafer backside as illustrated in Figure 2-7. This form of global mechanical thinning could also be performed on the backside of the bonded B-wafer to reduce the thicknesses of both sides (not shown in Figure 2-7).

With the advancement in the mechanical thinning technology such as chemical mechanical polishing (CMP), a thin layer of more than $1\ \mu\text{m}$ in thickness with $\pm 0.5\ \mu\text{m}$ of thickness variation is achievable. The absolute thickness and the thickness variation can be improved further to $0.1 \pm 0.01\ \mu\text{m}$ when a localized thinning by polishing or plasma bombardment is performed [40]. Although the physical mechanical thinning technique is fairly simple, it is not as well-received as the Smart-CutTM technology because a large volume of material is inherently wasted in the mechanical thinning process.

Figure 2-7: An A-to-B-OI structure of thin A-layer is obtained by mechanically thinning a bonded A-to-B-OI structure from the bonded A-wafer backside.

2.4.2 The Smart-CutTM Technology

Smart-CutTM is another well-known form of layer transfer technology. It is a physical technique. The process flow is shown in Figure 2-8, of which the hydrogen (H) ion-implantation is the salient processing step. Prior to the bonding of the A-wafer and the B-wafer, hydrogen ions (H^+) are implanted into the A-wafer bulk to a well-controlled depth. Separately, an oxide is thermally grown or deposited on a B-substrate. After a wafer bonding process, the bonded structure is annealed to induce H^+ coalescence into micro-voids that will split the A-wafer bulk, leaving behind the A-to-B-OI structure of a thin A-layer. Hence, the thickness of the A-layer of the separated A-to-B-OI structure can be made very thin and well-defined. The remaining A-wafer bulk can be recycled for the next process cycle after polishing the A-surface.

Smart-CutTM is the dominant technology in SOI fabrication because the processing technique enables the handler substrate to be recycled. Hence, the process cost is reduced drastically. Such an elegant form of technology has been extended to realize thin GaAs and InP layers on Si substrates as well [63, 64].

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Figure 2-8: The Smart-Cut™ process flow to obtain an A-to-B-OI structure of thin A-layer.

2.4.3 The Bond and Etch-Back Technique

The bond and etch-back (BEB) technique offers an alternative approach to realizing an A-to-B-OI structure of thin A-layer. SOI structures that are realized through such a technique are commonly known as bonding and etch-back silicon-on-insulator (BESOI) structures. The BEB chemical approach involves an intermediate etch-stop layer in the A-wafer bulk to pre-define the thickness of the transferring thin A-layer as shown in Figure 2-9. First, an etch-stop layer is implanted into an A-wafer bulk. Separately, an oxide is thermally grown or deposited on a B-substrate. After a wafer bonding process, the A-wafer bulk of the bonded structure is etched until the etch-stop layer. Hence, the selectivity of the etchant solution in removing the A-wafer bulk as compared to the etch-stop layer needs to be as high as possible. Finally, the etch-stop layer is selectively etched away, leaving behind the A-to-B-OI structure of a thin A-layer.

Similar to the physical mechanical thinning technique, BEB is not an attractive approach as it involves the chemical dissolution of the wafer bulk. Hence, a large amount of material is wasted and a high process cost is incurred. Nevertheless, the processing time is short and there is good control over the thickness and uniformity of the thin layer.

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Figure 2-9: The BEB process flow to obtain an A-to-B-OI structure of thin A-layer.

2.4.4 The Lateral Etching Epitaxial Lift-off Technology

By far, layer transfer by the lateral etching of an intermediate sacrificial release layer [65, 66] serves as the main potential competitor for the Smart-CutTM technology. Figure 2-10 illustrates the use of the lateral etching epitaxial lift-off (LE-ELO) process to obtain a GaAs-to-Si-on-insulator structure of thin GaAs device layer. First, a GaAs/AlAs/GaAs structure is grown by epitaxy on a lattice-matched GaAs substrate. Separately, an oxide is thermally grown or deposited on a Si substrate. After a wafer bonding process, the bonded structure is subjected to a prolonged HF solution immersion, during which the intermediate sacrificial release layer of AlAs is being etched laterally. At the end of the LE-ELO process, the GaAs-to-Si-on-insulator structure of the thin GaAs device layer is lifted off and the separated GaAs substrate can be recycled for the next process cycle.

Hence, the LE-ELO process can also enable the recycling of the substrate for subsequent process cycles. Therefore, the cost is drastically reduced. Moreover, during the Smart-CutTM process, the H^+ is driven through the device layer and may induce crystal

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damage to a certain extent. In contrast, the exfoliation-free process of LE-ELO will not induce significant damage to the transferred device film. However, the downside of the LE-ELO technology is that the process requires a very long duration of HF bath immersion, especially if the lift-off process is performed at a wafer-scale. Hence, a very high interfacial bond energy is required before the bonded structure can withstand the prolonged HF bath immersion. The LE-ELO technology will be discussed in detail in Section 7.2.2.

Figure 2-10: The LE-ELO process flow to obtain a GaAs-to-Si-on-insulator structure of thin GaAs device layer.

References

- [1] D. Dowson, *History of tribology / D. Dowson*: London ; New York : Longman, 1978.
- [2] L. Rayleigh, "A Study of Glass Surfaces in Optical Contact," *Proceedings of the Royal Society of London. Series A - Mathematical and Physical Sciences*, vol. 156, iss. 888, pp. 326-49, 1936.
- [3] J. B. Lasky, "Wafer bonding for silicon-on-insulator technologies," *Applied Physics Letters*, vol. 48, iss. 1, pp. 78-80, 1986.
- [4] M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, "Silicon-to-silicon direct bonding method," *Journal of Applied Physics*, vol. 60, iss. 8, pp. 2987-9, 1986.
- [5] S. Franssila, *Introduction to Microfabrication [electronic resource]*: Hoboken : John Wiley & Sons, Ltd., 2010.
- [6] W. P. Maszara, B. L. Jiang, A. Yamada, G. A. Rozgonyi, H. Baumgart, and A. J. R. de Kock, "Role of surface morphology in wafer bonding," *Journal of Applied Physics*, vol. 69, iss. 1, pp. 257-60, 1991.
- [7] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [8] U. Gosele, Q. Y. Tong, A. Schumacher, G. Krauter, M. Reiche, A. Plossl, P. Kopperschmidt, T. H. Lee, and W. J. Kim, "Wafer bonding for microsystems technologies," *Sensors and Actuators a-Physical*, vol. 74, iss. 1-3, pp. 161-8, 1999.
- [9] T. Abe and J. H. Matlock, "Wafer bonding technique for silicon-on-insulator technology," *Solid State Technology*, vol. 33, iss. 11, pp. 39-40, 1990.
- [10] G. Liao, X. Lin, L. Nie, and T. Shi, "Surface roughness modeling for silicon direct bonding," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, iss. 8, pp. 1171-7, 2011.
- [11] C. Gui, M. Elwenspoek, N. Tas, and J. G. E. Gardeniers, "The effect of surface roughness on direct wafer bonding," *Journal of Applied Physics*, vol. 85, iss. 10, pp. 7448-54, 1999.
- [12] R. Stengl, K. Y. Ahn, and U. Gosele, "Bubble-free silicon wafer bonding in a non-cleanroom environment," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 27, iss. 12, pp. 2364-6, 1988.
- [13] U. Gosele and Q. Y. Tong, "Semiconductor wafer bonding," *Annual Review of Materials Science*, vol. 28, pp. 215-41, 1998.
- [14] R. Stengl, T. Tan, and U. Gosele, "A model for the silicon wafer bonding process," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 10, pp. 1735-41, 1989.
- [15] K. Mitani, V. Lehmann, and U. Gosele, "Bubble formation during silicon wafer bonding: causes and remedies," in *Technical Digest. IEEE Solid-State Sensor and Actuator Workshop (Cat. No.90CH2783-9)*, pp. 74-7, Jun. 4 - Jun. 7, 1990, New York, NY, USA.
- [16] K. Mitani, V. Lehmann, R. Stengl, D. Feijoo, U. M. Gosele, and H. Z. Massoud, "Causes and prevention of temperature-dependent bubbles in silicon-wafer bonding," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers*, vol. 30, iss. 4, pp. 615-22, 1991.
- [17] J. E. Olsen and F. Shimura, "Infrared analysis of film growth on the silicon surface in room air," *Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films)*, vol. 7, iss. 6, pp. 3275-8, 1989.
- [18] W. Kern and D. A. Puotinen, "Cleaning solutions based on hydrogen for use in silicon semiconductor technology," *R.C.A. Review*, vol. 31, iss. 2, pp. 187-206, 1970.

Chapter 2: Literature Review

-
- [19] K. Mitani, *Wafer bonding : studies of interface bubbles and electrical characterization / by Kiyoshi Mitani*: Ann Arbor, Mich. : UMI, 1991.
 - [20] M. Miyashita, T. Tusga, K. Makihara, and T. Ohmi, "Dependence of surface microroughness of CZ, FZ, and EPI wafers on wet chemical processing," *Journal of the Electrochemical Society*, vol. 139, iss. 8, pp. 2133-42, 1992.
 - [21] Z. Xuan Xiong and J. P. Raskin, "Low-temperature wafer bonding: a study of void formation and influence on bonding strength," *Journal of Microelectromechanical Systems*, vol. 14, iss. 2, pp. 368-82, 2005.
 - [22] S. V. Hattangady, R. A. Rudder, M. J. Mantini, G. G. Fountain, J. B. Posthill, and R. J. Markunas, "In situ cleaning of GaAs surfaces using hydrogen dissociated with a remote noble-gas discharge," *Journal of Applied Physics*, vol. 68, iss. 3, pp. 1233-6, 1990.
 - [23] J. Ramm, E. Beck, A. Zuger, A. Dommann, and R. E. Pixley, "Low-temperature in situ cleaning of silicon wafers with an ultra high vacuum compatible plasma source," in *SiGe Based Technologies: Symposium A of E-MRS Spring Meeting*, vol. 222, pp. 126-31, Jun. 2 - Jun. 4, 1992, Switzerland.
 - [24] J. Ruzyllo, G. T. Duranko, and A. M. Hoff, "Preoxidation UV treatment of silicon wafers," *Journal of the Electrochemical Society*, vol. 134, iss. 8A, pp. 2052-5, 1987.
 - [25] L. Xiaohui, L. Guanglan, T. Zirong, and S. Tieli, "UV surface exposure for low temperature hydrophilic silicon direct bonding," *Microsystem Technologies*, vol. 15, iss. 2, pp. 317-21, 2009.
 - [26] Y. Backlund, K. Hermansson, and L. Smith, "Bond-strength measurements related to silicon surface hydrophilicity," *Journal of the Electrochemical Society*, vol. 139, iss. 8, pp. 2299-301, 1992.
 - [27] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
 - [28] P. Gueguen, C. Ventosa, L. D. Cioccio, H. Moriceau, F. Grossi, M. Rivoire, P. Leduc, and L. Clavelier, "Physics of direct bonding: Applications to 3D heterogeneous or monolithic integration," *Microelectronic Engineering*, vol. 87, iss. 3, pp. 477-84, 2010.
 - [29] R. J. Charles, "Static fatigue of glass.1," *Journal of Applied Physics*, vol. 29, iss. 11, pp. 1549-53, 1958.
 - [30] Y. Backlund, K. Ljungberg, and A. Soderbarg, "A suggested mechanism for silicon direct bonding from studying hydrophilic and hydrophobic surfaces," *Journal of Micromechanics and Microengineering*, vol. 2, iss. 3, pp. 158-60, 1992.
 - [31] Q. Y. Tong and U. Gosele, "A model of low-temperature wafer bonding and its applications," *Journal of the Electrochemical Society*, vol. 143, iss. 5, pp. 1773-9, 1996.
 - [32] T. A. Michalske and B. C. Bunker, "Slow fracture model based on strained silicate structures," *Journal of Applied Physics*, vol. 56, iss. 10, pp. 2686-93, 1984.
 - [33] M. Grundner, "High-resolution electron energy-loss spectroscopy measurements of hydrophilic silicon (100) wafers: temperature and aging effects," in *10th International Vacuum Congress (IVC-10), 6th International Conference on Solid Surfaces (ICSS-6) and 33rd National Symposium of the American Vacuum Society*, vol. 5, pp. 2011-5, Oct. 27 - Oct. 31, 1986, USA.
 - [34] D. Feijoo, Y. J. Chabal, and S. B. Christman, "Silicon wafer bonding studied by infrared absorption spectroscopy," *Applied Physics Letters*, vol. 65, iss. 20, pp. 2548-50, 1994.

Chapter 2: Literature Review

-
- [35] J. del Bene and J. A. Pople, "Theory of molecular interactions. I. Molecular orbital studies of water polymers using a minimal Slater-type basis," *Journal of Chemical Physics*, vol. 52, iss. 9, pp. 4858-66, 1970.
 - [36] T. A. Michalske and E. R. Fuller Jr, "Closure and repropagation of healed cracks in silicate glass," *Journal of the American Ceramic Society*, vol. 68, iss. 11, pp. 586-90, 1985.
 - [37] D. A. Litton and S. H. Garofalini, "Modeling of hydrophilic wafer bonding by molecular dynamics simulations," *Journal of Applied Physics*, vol. 89, iss. 11, pp. 6013-23, 2001.
 - [38] M. Horiuchi and S. Aoki, "Characteristics of silicon water-bond strengthening by annealing," *Journal of the Electrochemical Society*, vol. 139, iss. 9, pp. 2589-94, 1992.
 - [39] E. A. Irene, E. Tierney, and J. Angilello, "A viscous flow model to explain the appearance of high density thermal SiO₂ at low oxidation temperatures," *Journal of the Electrochemical Society*, vol. 129, iss. 11, pp. 2594-7, 1982.
 - [40] Q. Y. Tong and U. Gösele, "Semiconductor wafer bonding: recent developments," *Materials Chemistry and Physics*, vol. 37, iss. 2, pp. 101-27, 1994.
 - [41] M. Alexe, V. Dragoi, M. Reiche, and U. Gosele, "Low temperature GaAs/Si direct wafer bonding," *Electronics Letters*, vol. 36, iss. 7, pp. 677-8, 2000.
 - [42] V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gosele, "Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 12, pp. 2141-3, 1989.
 - [43] R. Malik, T. Shi, Z. Tang, and S. Liu, "Effect of ultra violet process and annealing on reliability in low temperature silicon wafer direct bonding," *Advanced Science Letters*, vol. 4, iss. 3, pp. 774-80, 2011.
 - [44] T. Suni, K. Henttinen, I. Suni, and J. Makinen, "Effects of plasma activation on hydrophilic bonding of Si and SiO₂," *Journal of the Electrochemical Society*, vol. 149, iss. 6, pp. 348-51, 2002.
 - [45] Q. Y. Tong, W. J. Kim, T. H. Lee, and U. Gosele, "Low vacuum wafer bonding," *Electrochemical and Solid-State Letters*, vol. 1, iss. 1, pp. 52-3, 1998.
 - [46] Y. Wei Bo, T. Cher Ming, W. Jun, D. Shu Sheng, and H. Guang Yu, "Effect of medium vacuum on low temperature wafer bonding," *Journal of Micromechanics and Microengineering*, vol. 15, iss. 5, pp. 1001-6, 2005.
 - [47] P. Amirfeiz, S. Bengtsson, M. Bergh, E. Zanghellini, and L. Borjesson, "Formation of silicon structures by plasma-activated wafer bonding," *Journal of the Electrochemical Society*, vol. 147, iss. 7, pp. 2693-8, 2000.
 - [48] T. Plach, V. Dragoi, F. Murauer, and K. Hingerl, "Plasma activation for low temperature Wafer bonding," in *Semiconductor Wafer Bonding 10: Science, Technology, and Applications - 214th ECS Meeting*, vol. 16, pp. 549-59, Oct. 14 - Oct. 16, 2008, Honolulu, HI, United States.
 - [49] G. L. Sun, J. Zhan, Q. Y. Tong, S. J. Xie, Y. M. Cai, and S. J. Lu, "Cool Plasma Activated Surface in Silicon Wafer Direct Bonding Technology," in *Solid State Device Research Conference, 18th European*, pp. c4-79-c4-82, Sep. 13 - Sep. 16, 1988.
 - [50] G. Kissinger and W. Kissinger, "Void-free silicon-wafer-bond strengthening in the 200-400C range," *Sensors and Actuators, A: Physical*, vol. 36, iss. 2, pp. 149-56, 1993.
 - [51] H. Takagi, R. Maeda, T. R. Chung, and T. Suga, "Low-temperature direct bonding of silicon and silicon dioxide by the surface activation method," *Sensors and Actuators a-Physical*, vol. 70, iss. 1-2, pp. 164-70, 1998.

Chapter 2: Literature Review

-
- [52] H. Takagi, R. Maeda, C. Teak Ryong, N. Hosoda, and T. Suga, "Effect of surface roughness on room-temperature wafer bonding by Ar beam surface activation," *Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers)*, vol. 37, iss. 7, pp. 4197-203, 1998.
 - [53] S. N. Farrens, J. R. Dekker, J. K. Smith, and B. E. Roberds, "Chemical free room temperature wafer to wafer direct bonding," *Journal of the Electrochemical Society*, vol. 142, iss. 11, pp. 3949-55, 1995.
 - [54] O. Zucker, W. Langheinrich, M. Kulozik, and H. Goebel, "Application of oxygen plasma processing to silicon direct bonding," *Sensors and Actuators A (Physical)*, vol. A36, iss. 3, pp. 227-31, 1993.
 - [55] Y. Wei Bo, T. Cher Ming, W. Jun, D. Shu Sheng, and N. Mui Ling, "Influence of plasma treatment and cleaning on vacuum wafer bonding," in *Proceedings of the 5th Electronics Packaging Technology Conference (EPTC 2003)*, pp. 294-7, Dec. 10 - Dec. 12, 2003, Piscataway, NJ, USA.
 - [56] C. M. Tan, W. Yu, and J. Wei, "Comparison of medium-vacuum and plasma-activated low-temperature wafer bonding," *Applied Physics Letters*, vol. 88, iss. 11, pp. 114102-4, 2006.
 - [57] T. Suga, Y. Takahashi, H. Takagi, B. Gibbesch, and G. Elssner, "Structure of Al-Al and Al-Si₃N₄ interfaces bonded at room temperature by means of the surface activation method," *Acta metallurgica et materialia*, vol. 40, iss. SUPPL, pp. S133-7, 1992.
 - [58] D. Haneman, W. D. Roots, and J. T. P. Grant, "Atomic mating of germanium surfaces," *Journal of Applied Physics*, vol. 38, iss. 5, pp. 2203-12, 1967.
 - [59] H. I. Smith and M. S. Gussenhoven, "Adhesion of polished quartz crystals under ultrahigh vacuum," *Journal of Applied Physics*, vol. 36, iss. 7, pp. 2326-7, 1965.
 - [60] U. Gosele, H. Stenzel, T. Martini, J. Steinkirchner, D. Conrad, and K. Scheerschmidt, "Self-propagating room-temperature silicon wafer bonding in ultrahigh vacuum," *Applied Physics Letters*, vol. 67, iss. 24, pp. 3614-3616, 1995.
 - [61] A. Ploel and G. Krauter, "Wafer direct bonding: Tailoring adhesion between brittle materials," *Materials Science and Engineering R: Reports*, vol. 25, iss. 1, pp. 1-88, 1999.
 - [62] Y. B. Bolkhovityanov and O. P. Pchelyakov, "III-V Compounds-on-Si: Heterostructure Fabrication, Application and Prospects," *The Open Nanoscience Journal*, vol. 3, iss. 1, pp. 20-33, 2009.
 - [63] U. Gosele, Y. Bluhm, G. Kastner, P. Kopperschmidt, G. Krauter, R. Scholz, A. Schumacher, S. Senz, Q. Y. Tong, L. J. Huang, Y. L. Chao, and T. H. Lee, "Fundamental issues in wafer bonding," *Journal of Vacuum Science & Technology A*, vol. 17, iss. 4, pp. 1145-52, 1999.
 - [64] Q.-Y. Tong and U. M. Gosele, "Wafer bonding and layer splitting for microsystems," *Advanced Materials*, vol. 11, iss. 17, pp. 1409-25, 1999.
 - [65] E. Yablonovitch, T. Gmitter, J. P. Harbison, and R. Bhat, "Extreme selectivity in the lift-off of epitaxial GaAs films," *Applied Physics Letters*, vol. 51, pp. 2222-4, 1987.
 - [66] M. M. A. J. Voncken, J. J. Schermer, G. J. Bauhuis, A. T. J. van Niftrik, and P. K. Larsen, "Strain-accelerated HF etching of AlAs for epitaxial lift-off," *Journal of Physics: Condensed Matter*, vol. 16, pp. 3585-96, 2004.

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3.1 The Plasma-Activated Direct Wafer Bonding Process

	Illustration	Remarks
Si Wafer Clean		<i>Surface Clean</i>
		<ol style="list-style-type: none"> 1. Warm TCE 2. Ultrasonic warm acetone 3. Ultrasonic warm IPA 4. Thorough DI water rinse
		<i>Native Oxide Strip</i>
		<ol style="list-style-type: none"> 1. Dilute HF dip 2. Thorough DI water rinse
	<i>Clean Native Oxide Regrowth</i>
		<ol style="list-style-type: none"> 1. RCA solution immersion 2. Thorough DI water rinse
Ar Plasma Activation and Room Temperature Contact		<i>Surface Activation</i>
		<ol style="list-style-type: none"> 1. Ar plasma exposure on bonding surfaces
	<i>Room Temperature Contact</i> <ol style="list-style-type: none"> 1. Central point pressure
Thermal Treatment		<i>Anneal</i>

Figure 3-1: Sequential stages in the bonding process of a pair of GaAs and Si wafers.

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In the present work, 2-inch (100) p-type Boron-doped Si wafers of resistivity between 1 to 10 ohm.cm were plasma-activated direct wafer bonded (PADWB) to 2-inch (100) n-type Si-doped GaAs wafers of resistivity about 10^{-3} ohm.cm. The Si and GaAs wafers were commercially available from Bonda Technology Pte. Ltd. and AXT, Inc. respectively. Both batches of 275 ± 25 μm Si wafers and 450 ± 25 μm GaAs wafers were specified to have a TTV of less than 3 μm , a bow and warp of less than 25 μm , and a surface roughness of less than 5 Å RMS to ensure good bondability (refer to Section 2.1.1). All of the wafers were single-side polished. As shown in Figure 3-1, the direct wafer bonding process of a pair of GaAs and Si wafers consisted of three general stages: 1) chemical cleaning, 2) surface activation and room temperature contact, and 3) thermal treatment.

To prevent the inevitable etching of the GaAs wafers by a cleaning solution and to preserve the GaAs surface roughness from deterioration, the GaAs wafers were not chemically cleaned. Moreover, the GaAs wafers were pre-cleaned, sealed, and packaged individually by the manufacturer. The Si wafers were first soaked in warm trichloroethylene (TCE) followed by an ultrasonic bath of warm acetone. Each step lasted for 5 min. After a subsequent step of warm IPA ultrasonic bath for 5 min to get rid of the acetone residues, the Si wafers were rinsed with running deionized (DI) water for another 5 min. Most of the surface organic contaminants would have been cleaned off by this step. However, organic contaminants may also be trapped in the Si native oxide and at the Si bulk-native oxide interface [1-3]. Hence, the Si wafers were subsequently dipped in a dilute 1% HF solution for 15 s to strip off the native oxides while preserving the low Si surface roughness [4]. As bare Si wafers are known to be very reactive, they were rinsed under running DI water for 5 min immediately after the dilute HF dip to prevent any re-contamination. The last step of the cleaning stage involved soaking the wafers immediately in a NH_4OH (27%): H_2O_2 (30%): H_2O base solution in a ratio of 0.25:1:5 by volume for 10 min [5]. The NH_4OH solution was first

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prepared and heated to $70^{\circ}\text{C} \pm 5^{\circ}\text{C}$ prior to adding the H_2O_2 into the solution. After vigorous bubbling was observed, the Si wafer was then immersed into the hot NH_4OH and H_2O_2 solution. During the base cleaning step, clean native oxides were growing on the Si surfaces. After the base cleaning step, the Si wafers were rinsed thoroughly under running DI water and dried under a flow of Nitrogen (N_2) gas.

Immediately after the cleaning stage, the GaAs and Si wafers were loaded in an AST Descum-Clen100 system individually for an Argon (Ar) plasma surface treatment. In each Ar plasma process, the plasma chamber was first purged down to a base pressure of less than 25 mTorr followed by an Ar gas stabilization for 1 min. Subsequently, the bonding surfaces were treated with different Ar plasma conditions of 5 s and 30 s of exposure time, 120 mTorr and 200 mTorr of pressure, and 100 W and 200 W of radio frequency (RF) power. After the Ar plasma surface treatments, the bonding pairs were then ex-situ contacted together under a normal atmospheric condition at room temperature (20°C). The room temperature contacts were performed with a point load at the center of each bonding pair of GaAs and Si wafers to prevent the occurrence of any trapped air pockets at the bonding interface [6].

The last stage of the bonding process involved annealing the contacted pairs with different thermal conditions. The maximum annealing temperature was 140°C . Moreover, the GaAs-to-Si bonding pairs were annealed with different annealing profiles. The annealings were carried out either under a normal atmospheric (750 Torr) condition or a high vacuum (10^{-6} Torr) condition. Normal atmospheric annealings were performed using a BINDER FD series convection oven. High vacuum annealings were performed through a self-constructed high vacuum annealing system, which will be described in Section 3.3.

3.2 Characterization

3.2.1 The Infrared Optical Transmission Imaging

Optical transmission is often used to evaluate the quality of a bonded interface owing to its simplicity, low cost, and instant image acquisition compared to other imaging techniques such as scanning acoustic microscopy (SAM) [7, 8], X-ray topography scanning [9], and the magic mirror [10]. However, the optical transmission imaging technique has a poorer resolution. Coupled with an imaging software, the bond efficiency and the bond energy of a GaAs-to-Si bonded pair can be evaluated.

The infrared (IR) optical transmission imaging system that was used in this research is shown in Figure 3-2. The system included a bottom light source (halogen lamps) and a camera at the top of a GaAs-to-Si bonded pair of interest. The captured image was then output to a computer for further image processing.

Figure 3-2: A photograph showing the IR optical transmission imaging system.

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Optical transmission imaging works on the principle that radiant photons of light will propagate into the bottom of a bonded pair through the bonded interface and out from the top of the bonded pair. These radiant photons of light are captured by an IR camera. Hence, any air gaps present at the bonded interface will reduce the transmission efficiency significantly and the localized void regions will appear dark in the image.

Two important aspects have to be considered when using the optical transmission imaging technique. First, the photon wavelength (λ_{light}) has to be selected accordingly to permit light to pass through the bulks of the bonded pair. If a photon energy (E_{photon}) is greater than the bandgap (E_g) of a material, it will be absorbed by the material bulk to generate an electron-hole pair. Consequently, the light will not be permitted to transmit through the bulk. In the case of examining a bonded pair of dissimilar materials, the E_g that needs to be considered is the lower E_g out of the two bonded materials. Hence, in the present work of bonding GaAs and Si, the E_g that needs to be considered will be the E_g of the Si ($E_{g,Si}$). The E_g values of GaAs and Si are 1.43 eV and 1.12 eV, respectively (see Table 1-1). Therefore it is necessary that the condition of

$$E_{photon} < E_{g,Si} \quad (3-1)$$

has to be met. In the present optical transmission imaging work, an IR camera was used to capture the IR component of the transmitted light. The longest wavelength in the IR range is 1 mm, which corresponds to an E_{photon} of 1.24 meV that is lower than the $E_{g,Si}$ of 1.12 eV. Hence, the condition of Equation (3-1) is met. Consequently, the IR light was able to transmit through the GaAs-to-Si bonded pairs so that the IR camera will capture the IR transmitted light to image the bonded interfaces accordingly.

The second aspect that has to be considered when using the optical transmission imaging technique is that the free-carrier concentration of a bonded pair cannot be too high

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even if the condition of Equation (3-1) is met. The intensity of a transmitted light, $I(z)$, that is in a direction perpendicular to the plane of a bonded interface is

$$I(z) = I_0 e^{-\alpha z}, \quad (3-2)$$

where I_0 denotes the initial intensity of light prior to propagating into a bonded pair and α is the absorption coefficient, which is a function of both the carrier concentration and the wavelength of the transmitted light. If the carrier concentration is high, the α -value will be high and the intensity of the transmitted ray will be nearly zero. In the present study, the carrier concentration of the bonding GaAs wafers was about 10^{18} cm^{-3} and the carrier concentration of the bonding Si wafers was about 10^{16} cm^{-3} . The GaAs and the Si carrier concentrations were sufficiently low to induce weak carrier absorption, such that the IR light was able to transmit through the GaAs-to-Si bonded pairs.

3.2.2 The Evaluation of the Bond Efficiency and the Bond Energy

The use of the IR optical transmission imaging in this work was coupled with the imaging software of *ImageTool Version 3.0* developed by the University of Texas Health Science Center at San Antonio (UTHSCSA), to quantify a bond quality. A high bond quality indicates that a bonded interface has a high bond efficiency and a high bond energy.

Bond efficiency reflects the extent of the bonding coverage of a bonded pair. In this work, bond efficiency (β) was expressed as a percentage of the bonded area over the total area. First, the threshold function of the program was used to convert the entire IR image of a GaAs-to-Si bonded pair (see Figure 3-3[a]) into a full black image (see Figure 3-3[b]). Subsequently, a black pixel count (P_{total}) was performed to determine the number of pixels in the black image (see Figure 3-3[e]). Second, unbonded regions (which showed up as localized dark spots) were then selectively cropped out and converted into near-full black

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Figure 3-3: A snapshot image of the *ImageTool* software interface when determining the bond efficiency of a GaAs-to-Si bonded pair.

images via the threshold function. Figure 3-3(c) shows an example of an unbonded region that was cropped out and converted into the near-full black image (see Figure 3-3[d]). Subsequently, the area of each unbonded region was quantified by determining the number of pixels in each respective cropped out black image, $P_{i,unbonded}$ (see Figure 3-3[e]). Finally, the bond efficiency was calculated as follows:

$$\beta = \frac{P_{total} - \sum_{i=1}^{all} P_{i,unbonded}}{P_{total}} \times 100\% \quad (3-3)$$

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In this work, the bond energies of the GaAs-to-Si bonded pairs were quantified using the crack-opening technique as developed by Masazara [11]. This technique was based on an energy-balance approach of an interfacial cleavage of a bonded cantilever beam of dissimilar materials, in which the derivation can be found in [4]. In the present work of bonding GaAs and Si wafers, the bond energy, γ , can be calculated as follows:

$$\gamma = \frac{3t_{blade}^2 E_{Si} t_{Si}^3 E_{GaAs} t_{GaAs}^3}{16l^4 (E_{Si} t_{Si}^3 + E_{GaAs} t_{GaAs}^3)} \quad (3-4)$$

where t_{blade} denotes the thickness of the razor blade used in the cleaving process and l denotes the corresponding crack length. E_{Si} and E_{GaAs} are the material properties, which represent the Young's moduli of Si and GaAs respectively. t_{Si} and t_{GaAs} are geometrical properties, which denote the thicknesses of the Si and GaAs wafers, respectively.

Compared to other forms of quantification such as the tensile pull test, the crack-opening technique is widely used in quantifying the energy of a bond because of its simplicity and low cost. However, the crack-opening technique has a number of drawbacks [12]. First, the technique involves the insertion of a blade to induce a crack of a certain length at a bonded interface edge. Hence, the derived γ -value will only reflect the bond energy at the edge. Unless the bond energy is uniform across the bonded interface, the γ -value will not be a true indication of the bond energy. In the bonding of a pair of GaAs and Si wafers, the thermal-mismatch peeling stress grows significantly towards the peripheral of the GaAs-to-Si bonding wafers during an annealing. As a result, the bond energy is expected to be lower at the peripheral of the bonded interface. Hence, the determined γ -value will be underestimated.

Second, the specific bond energy (γ) in Equation (3-4) was derived based on an energy equilibrium concept. Hence, the insertion of the blade has to be performed in an adiabatic fashion, which is difficult to achieve especially when the bond energy is very high and the strength during the manual blade insertion has to be well-controlled and precise.

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Finally, it can be observed from Equation (3-4) that the γ -value is a strong function of the induced crack length (l) by a power of 4. The induced crack length is sensitive to the pressure of the environment in which the blade insertion is performed and the duration of time between the blade insertion and the image acquisition. In general, a higher pressure and/or a longer duration will result in a longer crack length. Hence, the evaluated γ -value will be underestimated.

To address the drawbacks of the crack-opening technique:

1. Each blade insertion process was performed as slow as possible. If the blade went in too fast, another edge within the same bonded pair was chosen to repeat the blade insertion process.
2. The blade was carefully inserted into a bonded interface as parallel as possible because any oblique angle blade insertion will amplify the crack length due to the stiffness of the bonding wafers.
3. The IR image was captured almost immediately after the blade was inserted into a bonded interface. This minimized the effect of further crack propagation due to the normal atmospheric pressure. Hence, the determined crack length will be more accurate.
4. To obtain the length of a crack more precisely, the *ImageTool Version 3.0* image processing software was used. First, the IR image of a bonded pair of GaAs-to-Si with a blade-induced crack was rescaled proportionally via a created standard proportional template as shown in red in Figure 3-4. Next, a line was drawn along the diameter (50.8 mm) of the GaAs-to-Si bonded pair in the rescaled IR image. The image processing program determined the number of pixels along the drawn line. Hence, the length-to-pixel proportionality was determined and recorded by the program. Subsequently, a perpendicular line was drawn from the edge of the

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blade to the crack tip, along which the program will determine the corresponding number of pixels. With the known length-to-pixel proportionality, the program algorithm can determine and output the length of the crack in millimeters.

5. Finally, the errors in the specific bond energy data *provided in this work* were taken to be $\pm 15\%$ of the bond energies [13, 14].

Figure 3-4: The IR image of a GaAs-to-Si bonded pair with a blade-induced crack that was being rescaled by fitting the image to a created standard proportional template (shown in red) and the crack length was determined to be 8.15 mm.

3.2.3 The Atomic Force Microscopy

Atomic force microscopy (AFM) is a powerful tool in surface morphology diagnostic with a resolution near the atomic level. It is capable of achieving this high resolution mainly because of its highly sensitive piezoelectric transducer and its very sharp tip at the end of a cantilever beam, which probes the region of interest. Among the various types of operation modes that the AFM can offer, the tapping-mode (also known as AC-mode) was used in this work. When the AFM was operated under the tapping-mode, the probe was in intermittent contact with the sample surfaces. Hence, the friction-induced surface damages will be kept to a negligible extent. Moreover, the sharpness of the probe tips can be preserved for a much longer period of time when the tapping-mode is used.

During a contact-mode AFM scan, the cantilever beam is driven near its resonance frequency with a characteristic amplitude that is detected by a laser sensor by means of a laser beam deflecting off the cantilever beam end. As the probe tip is scanning over a region of interest in a rastering fashion, the tip-surface interaction will change according to the surface topography. As a result, the resonating beam amplitude will be deviated away from the characteristic amplitude, which will be feed back into the system. Subsequently, the piezoelectric-crystal stage (on which the sample is laying on) will be finely positioned to restore the amplitude of the resonating beam back to the characteristic amplitude. In this manner, a 3D image of the surface topography will be obtained.

Apart from being able to provide a qualitative pictorial view of a surface morphology, the AFM is also capable of quantifying the surface roughness down to an atomic level. A low surface roughness is essential in achieving a high bond energy as the roughness will determine the extent of the intimacy between the bonding surface reactive species. In this work, the root mean square (RMS) of the measured heights was taken as the surface roughness quantification parameter (R_q). The standard deviation value indicates the

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dispersion of the measured heights relative to an average value, which reflects the degree of the surface roughness.

In this work, an ultra-high resolution Cypher™ (Asylum Research, Santa Barbara, CA) AFM system was used to analyze the bonding GaAs and Si wafers. The height resolution of the AFM system is less than 10 pm under near-ideal conditions and as high as 20 pm in noisy environments. The step height and the surface roughness of an atomic layer deposition (ALD) of Hafnium oxide (HfO₂) [15], a monolayer transfer of Molybdenum disulfide (MoS₂) [16, 17], and a monolayer transfer of polyolefin films [18] in the nanometer to angstrom range have been demonstrated using the Cypher™ AFM system. Presently, all of the AFM runs were carried out during off-hours to minimize the noise level. Nanosensors™ SuperSharpSilicon™ SSS-NCH-20 cantilevers of thicknesses between 3.60 to 3.80 μm, widths between 27 to 28 μm, and lengths of 125 μm were used with the spring constants between 28 to 35 N/m and the resonance frequencies between 296 to 319 kHz. The probe tip heights were between 10 to 15 μm and the tip radii of curvature were about 2 nm.

Each AFM scan was performed with 512 data points and lines acquisition to obtain a good quality 3D image and a more accurate surface roughness result. All of the scan sizes were set at 20 by 20 μm². Further optimization included having the trace and the retrace line placed as near to each other as possible during the scanning by tuning the set point and the integral gain values. The scan was repeated twice to obtain a finer image.

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3.2.4 The Video Contact Analyzer and the Contact Angle Measurement

In this work, the sessile drop technique was used to characterize a bonding surface hydrophilicity, which was performed through the video contact analyzer pictured in Figure 3-5. First, a sample of interest was placed on the sample stage. With the light source on, the camera was focused on the side of the sample. Subsequently, a 0.5 μL distilled water droplet was dispensed onto the surface of the sample. The disposal of the water droplet was automated by the motorized syringe assembly that was controlled by the computer unit. Next, the silhouette of the wetting water droplet on the sample was captured by the camera and was output to the computer unit.

Figure 3-5: Photograph of the video contact analyzer.

Figure 3-6: The processing of the wetting water droplet silhouette image to determine the contact angle between the tangent line to the wetting water droplet and the sample.

The next step was to process the image to determine the contact angle of the wetting water droplet (see Figure 3-6). First, a line that was coincided with the surface was drawn. Next, five near-evenly spaced out points were selected along the surface of the wetting water droplet. The algorithm of the image processing software then detected the best-fit curve through the five selected points. Subsequently, the algorithm determined a tangent line to the best-fit curve at the wetting water droplet-surface contact point, at which the contact angle will be calculated.

3.3 The High Vacuum Annealing System Design and Construction

Figure 3-7: The high vacuum annealing system that consists of the chamber, the high vacuum system, and the temperature control system.

A high vacuum annealing system was built manually to anneal the GaAs-to-Si bonding pairs under a high vacuum condition. Displayed in Figure 3-7, the high vacuum annealing system consists of three main components: 1) the chamber, 2) the temperature control system, and 3) the high vacuum system. The system can only accommodate a 2-inch wafer size and is capable of achieving a high vacuum level of 10^{-6} Torr.

3.3.1 The Chamber Design and Construction

The chamber pictured in Figure 3-7 is a thick walled hollow stainless steel pipe. The chamber top is covered with a thick transparent Pyrex plate (see Figure 3-8), which allows in-situ observations during annealings. The sealing between the chamber top and the Pyrex plate

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Figure 3-8: Photographs showing (a) the chamber, (b) a close-up view of the top of the chamber, and (c) a close-up view of the bottom of the chamber.

was achieved with an O-ring (see Figure 3-8[b]). The bottom of the chamber was sealed by securing the chamber bottom to a thick concentric stainless steel base (see Figure 3-8[c]) by means of a metal gasket, screws, and nuts (not shown in Figure 3-8[c]).

Separately, a three-legged metal tripod stand with a hexagonal metal plate at the top was constructed as shown in Figure 3-9. A hole was machined out in the middle of the hexagonal metal plate (not shown in Figure 3-9). A heater plate that contained a heating filament was then secured into the machined hole. After an electrical connection between the heating filament and the temperature control system was established, the entire setup was carefully placed into the chamber.

Figure 3-9: The three-legged metal tripod stand with a top hexagonal metal plate that contains the heater plate with the heating filament. The thermocouple is located at the bottom of the heater plate.

Prior to the annealing of a 2-inch GaAs-to-Si bonding pair, the bonding pair was fitted into a 2-inch central concentric hole of a molybdenum block as shown in Figure 3-10. The block was then secured onto the top of the heater plate by locking the protruding legs of the block into the trenches of the heater plate (see Figure 3-9). During the annealing, radiation rays from the bottom heating filament were passed through the central concentric hole of the molybdenum block to heat the bonding pair accordingly.

Figure 3-10: The inside view of the chamber from the top. The heating filament is beneath the GaAs-to-Si bonding sample that is not shown in the figure.

3.3.2 The High Vacuum System Design and Construction

The chamber was integrated with the high vacuum system that was being located below the chamber (see Figure 3-7). The high vacuum system is displayed in Figure 3-11 and its schematic layout design is illustrated in Figure 3-12. The high vacuum system consisted of a roughing pump, a high vacuum pump, and two hand-operated gate valves (A and B) that are indicated in Figure 3-11 and Figure 3-12. All of the flanges in the vacuum system were secured with wing nut clamps and sealed with O-rings and centering rings.

During the pumping down of the chamber, Valve A was first closed to disconnect the whole system from the atmosphere. Subsequently, Valve B was opened to connect the high vacuum system to the chamber. Next, the roughing pump was activated. When the vacuum level of the chamber was about 0.1 Torr (indicated by a vacuum gauge), the high vacuum

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pump was activated. The total time it took for the chamber pressure to reach down to a high vacuum level of 10^{-6} Torr was about 15 min.

When an annealed GaAs-to-Si bonded pair was ready to be unloaded, Valve B was closed to disconnect the high vacuum system from the chamber. Subsequently, the high vacuum pump and then the roughing pump were deactivated. Finally, Valve A was opened slowly to vent the chamber and the sample was unloaded.

Figure 3-11: The photograph showing the high vacuum system that consists of the roughing pump, the high vacuum pump, and hand-operated valves (A and B).

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Figure 3-12: The schematic layout of the high vacuum system design.

3.3.3 The Temperature Control System Design and Construction

The right side of the chamber was integrated with the temperature control system as shown in Figure 3-13 (or see Figure 3-7). The design layout of the temperature control system is illustrated in Figure 3-14 schematically. The system consisted of a power source, a temperature control unit, and a thermocouple that were integrated together. Electrical signals were mutually exchanged between the thermocouple and the heating filament inside the chamber with the power source and the temperature control unit outside the chamber through an electrical feedthrough (see Figure 3-13 or Figure 3-14). The temperature control unit served as user interface to control the temperature of the heating filament inside the chamber (and thus the GaAs-to-Si bonding pair). In this work, the ramping up and down of the temperatures was set at a rate of $1^{\circ}\text{C}/\text{min}$.

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First, the temperature control unit determined the temperature of the heating filament from the thermocouple inside the chamber. Subsequently, the temperature control unit signaled the power source to deliver the necessary current and voltage to the heating filament. Through this repeated closed loop signal feedback cycle, the temperature of the heating filament (and the bonding sample) was controlled.

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Figure 3-13: The photograph showing the chamber and the temperature control system. The temperature control system consisted of the power source, the temperature control unit, and the thermocouple (for the thermocouple inside the chamber, refer to Figure 3-9), which were integrated together.

Figure 3-14: The schematic layout of the temperature control system design.

References

- [1] K. Mitani, V. Lehmann, and U. Gosele, "Bubble formation during silicon wafer bonding: causes and remedies," in *Technical Digest. IEEE Solid-State Sensor and Actuator Workshop (Cat. No.90CH2783-9)*, pp. 74-7, Jun. 4 - Jun. 7, 1990, New York, NY, USA.
- [2] K. Mitani, V. Lehmann, R. Stengl, D. Feijoo, U. M. Gosele, and H. Z. Massoud, "Causes and prevention of temperature-dependent bubbles in silicon wafer bonding," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers*, vol. 30, iss. 4, pp. 615-22, 1991.
- [3] J. E. Olsen and F. Shimura, "Infrared analysis of film growth on the silicon surface in room air," *Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films)*, vol. 7, iss. 6, pp. 3275-8, 1989.
- [4] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [5] M. Miyashita, T. Tusga, K. Makihara, and T. Ohmi, "Dependence of surface microroughness of CZ, FZ, and EPI wafers on wet chemical processing," *Journal of the Electrochemical Society*, vol. 139, iss. 8, pp. 2133-42, 1992.
- [6] A. Plocl and G. Krauter, "Wafer direct bonding: Tailoring adhesion between brittle materials," *Materials Science and Engineering R: Reports*, vol. 25, iss. 1, pp. 1-88, 1999.
- [7] V. Jipson and C. F. Quate, "Acoustic microscopy at optical wavelengths," *Applied Physics Letters*, vol. 32, iss. 12, pp. 789-91, 1978.
- [8] R. A. Lemons and C. F. Quate, "Acoustic microscope-scanning version," *Applied Physics Letters*, vol. 24, iss. 4, pp. 163-5, 1974.
- [9] A. R. Lang, "Direct observation of individual dislocations by X-ray diffraction," *Journal of Applied Physics*, vol. 29, iss. 3, pp. 597-8, 1958.
- [10] O. Okabayashi, H. Shirotori, H. Sakurazawa, E. Kanda, T. Kokoyama, and M. Kawashima, "Evaluation of directly bonded silicon wafer interface by the magic mirror method," in *3rd International Symposium on Defect Recognition and Image Processing in III-V Compounds (DRIP-III)*, vol. 103, pp. 456-60, Sep. 22 - Sep. 25, 1989, Netherlands.
- [11] W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, "Bonding of silicon wafers for silicon-on-insulator," *Journal of Applied Physics*, vol. 64, iss. 10, pp. 4943-50, 1988.
- [12] O. Vallin, K. Jonsson, and U. Lindberg, "Adhesion quantification methods for wafer bonding," *Materials Science & Engineering R-Reports*, vol. 50, iss. 4-5, pp. 109-65, 2005.
- [13] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
- [14] Q. Y. Tong, W. J. Kim, T. H. Lee, and U. Gosele, "Low vacuum wafer bonding," *Electrochemical and Solid-State Letters*, vol. 1, iss. 1, pp. 52-3, 1998.
- [15] B. R. Dorvel, B. Reddy, J. Go, C. D. Guevara, E. Salm, M. A. Alam, and R. Bashir, "Silicon Nanowires with High-k Hafnium Oxide Dielectrics for Sensitive Detection of Small Nucleic Acid Oligomers," *Acs Nano*, vol. 6, iss. 7, pp. 6150-64, 2012.
- [16] J. Brivio, D. T. L. Alexander, and A. Kis, "Ripples and layers in ultrathin MoS2 membranes," *Nano Letters*, vol. 11, iss. 12, pp. 5148-53, 2011.
- [17] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," *Nature Nanotechnology*, vol. 6, iss. 3, pp. 147-50, 2011.

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- [18] M. Kobayashi, T. Matsugi, J. Saito, J.-i. Imuta, N. Kashiwa, and A. Takahara, "Direct modification of polyolefin films by surface-initiated polymerization of a phosphobetaine monomer," *Polymer Chemistry*, vol. 4, iss. 3, pp. 731-9, 2013.

Chapter 4 Development of the Surface Activation Process in the Direct Wafer Bonding of GaAs-to-Si

4.1 Introduction

Plasma-activated direct wafer bonding (PADWB) has been proven a viable low temperature solution. Farrens *et al.* demonstrated that the bond energy of PADWB is much greater than the bond energy derived from conventional wet-activated direct wafer bonding (WADWB) using suitable chemical solutions when both are subjected to the same set of annealing conditions and the annealing duration required to reach an equivalent equilibrium bond energy is much shorter with PADWB [1]. This makes PADWB feasible in mass production. Moreover, PADWB is compatible with present Si integrated circuit (IC) processes. For example, equipment such as plasma-enhanced chemical vapour deposition (PECVD) or plasma etching could be used to plasma activate bonding surfaces [2]. Other advantages of PADWB include low-cost and the flexibility to alter the degree of bond energy by changing plasma gas type, exposure time, pressure, and/or power depending on the area of the application of wafer bonding.

In the monolithic integration of dissimilar materials via wafer bonding, the thermal budget of a bonded pair is low due to an invertible coefficient of thermal expansion (CTE) mismatch. Hence, the bonding of dissimilar materials requires low temperature solutions such as PADWB. Unfortunately, most reported works of PADWB were performed with a Si-to-Si homogenous system and the usefulness of it has been undermined. Instead, PADWB could be exploited to bond thermally-mismatched dissimilar materials to realize a single entity platform of multi-functionalities. Moreover, most investigations on the PADWB of Si-to-Si treated the effects by several plasma parameters independently as the experiments were of a

one-factor-at-a-time type. Consequently, interactions among the plasma parameters that may affect bond energy were not captured, identified, and discussed.

In the present study, 2-inch GaAs and Si wafers measuring several hundreds of micrometers in thickness were bonded via Argon (Ar) PADWB and subjected to a low temperature annealing of 140°C under a normal atmospheric condition for 24 h. Argon was chosen as the plasma medium from among other gases such as oxygen and nitrogen as Suni *et al.* [3] showed it can yield a comparable high bond energy. The effects of the Ar plasma on the bond energy of PADWB of GaAs-to-Si were investigated through statistical means. The degrees of the influences brought by the various plasma parameters and the interactions among them were identified and discussed complimented by surface roughness morphology and hydrophilicity state characterization. The ultimate objective of this study is to identify a set of Ar plasma conditions so as to yield the highest bond energy possible in the PADWB of GaAs-to-Si with 140°C of low temperature annealing under a normal atmospheric condition.

4.2 Experimental Details

The Ar PADWB of GaAs-to-Si involved 3 general stages: 1) chemical cleaning of the wafers, 2) plasma activation and room temperature contact, and 3) thermal treatment. The details of each processing stage were discussed in Section 3.1. During the last stage of thermal treatment, all of the bonding pairs were subjected to a single-ramp up from room temperature to 140°C at a rate of 1°C/min. In addition, they were annealed at a low temperature for 24 h under a normal atmospheric condition.

A statistical design of a 2^3 (3 factors with 2 levels of low (-) and high (+) each) full factorial with two replicates was implemented to investigate the effects brought by three Ar plasma parameters. These effects were 1) exposure time, 2) pressure, and 3) radio frequency

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Table 4-1: Investigated plasma parameters and the associated two levels of values in the 2^3 factorial design of PADWB of GaAs-to-Si.

Level	Factor Code		
	A	B	C
	Exposure Time (s)	Pressure (mTorr)	RF Power (W)
Low (-)	5	120	100
High (+)	30	200	200

(RF) power, which were abbreviated as Factors A, B, and C, respectively. Values of 5 s, 120 mTorr, and 100 W were considered as a low level (-) of exposure time, pressure, and RF power, respectively. In contrast, values of 30 s, 200 mTorr, and 200 W, were taken as a high level (+) of exposure time, pressure, and RF power. These values are presented in Table 4-1.

Table 4-2 presents the 2^3 factorial design matrix of the Ar PADWB of GaAs-to-Si. There were eight experimental runs in total that involved different combinations of low and high levels of exposure time, pressure, and RF power. For each experimental run, two replicates were performed to realize a full factorial design. For example, in Run 6 of Table 4-2, two GaAs wafers and two Si wafers were subjected to the same plasma conditions of low level (-) pressure of 120 mTorr and high level (+) exposure time and RF power of 30 s and 200 W, respectively, to yield two GaAs-to-Si bonding pairs: Replicates 1 and 2. Post-annealing specific bond energy (see Equation [3-4]) was taken as the response from each bonded replicate of each experimental run.

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Table 4-2: The 2^3 factorial design matrix of PADWB of GaAs-to-Si.

Run	Factor Code		
	A	B	C
1	-	-	-
2	+	-	-
3	-	+	-
4	+	+	-
5	-	-	+
6	+	-	+
7	-	+	+
8	+	+	+

1 cm x 1 cm GaAs and Si cleaved out dies were used to investigate the effects of Ar plasma on the surface roughness morphology and hydrophilicity state of the wafers. The dies were divided into two groups with eight GaAs and Si dies in each group. The dies of each group were subjected to the eight different 2^3 factorial design Ar plasma conditions sets as shown in Table 4-2. Subsequently, atomic force microscopy (AFM) was performed on the plasma treated surfaces of the dies of one group while contact angle measurement (CAM) was conducted on the die surfaces of the other group.

4.3 Results and Discussion

4.3.1 Effects of Ar Plasma on the Bond Efficiency of PADWB of GaAs-to-Si

Run	Replicate 1	Replicate 2
1
2
3
4

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Run	Replicate 1	Replicate 2
5
6
7
8

Figure 4-1: Infrared images of the 2^3 factorial design of Ar PADWB of 2-inch GaAs-to-Si interfaces after room temperature contact.

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Run	Replicate 1	Replicate 2
1		<i>Debonded</i>
2	<i>Debonded</i>	<i>Debonded</i>
3	<i>Debonded</i>	<i>Debonded</i>
4	<i>Debonded</i>	<i>Debonded</i>

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Run	Replicate 1	Replicate 2
5
6
7	<i>Debonded</i>	<i>Debonded</i>
8

Figure 4-2: Infrared images of the 2^3 factorial design of Ar PADWB of 2-inch GaAs-to-Si interfaces after 140°C of low temperature annealing for 24 h under a normal atmospheric condition. The bonding pairs that were debonded after the anneals are indicated by the word ‘*Debonded*’.

Figure 4-1 and Figure 4-2 display the IR images of the 2^3 factorial design of Ar PADWB of GaAs-to-Si interfaces after room temperature contact and after 140°C of low temperature annealing for 24 h under a normal atmospheric condition, respectively. The darker regions of the IR images in Figure 4-1 indicate unbonded regions caused by trapped air pockets during room temperature contact. The IR images of some GaAs-to-Si bonding pairs could not be obtained after the annealing process because they were debonded (see ‘Debonded’ entries in Figure 4-1).

The work outlined in Section 3.2.2 was performed to quantify the bond efficiency (see Equation [3-3]) of the 2^3 factorial design of Ar PADWB of GaAs-to-Si bonded pairs after the room temperature contact and after the anneal, in terms of the percentage of the total area of a bonded pair that was bonded and unbonded. The results are shown in Table 4-3. A low percentage of unbonded areas that corresponds to a high percentage of bonded areas reflects excellent bond efficiency. A debonded pair after the 140°C anneal was deemed to have 0% of the total area bonded as indicated in the table.

As observed from Table 4-3, $\geq 95\%$ of the total areas of all the GaAs-to-Si bonding pairs were bonded after room temperature contact. This result indicates high bond efficiencies. The low percentages of the total area that were unbonded were due to the occurrence of entrapped particles and air pockets during the normal ambient room temperature contacts of the GaAs and Si bonding pairs, which were performed in a Class 100 cleanroom environment. For the bonded pairs that stayed intact after the 140°C annealing, the percentage of unbonded region after the room temperature contact and after the anneal did not change except for in Replicate 1 of the Run 1 bonded pair. In this replicate, the amount of unbonded area increased from 3% to 7% (indicating a slight deterioration in bond efficiency).

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The results indicate that a low temperature anneal of 140°C for 24 h under a normal ambient condition of Ar PADWB of GaAs-to-Si does not evolve additional voids which will otherwise lead to bond efficiency deterioration [4].

Table 4-3: Bond efficiency results of the 2³ factorial design of PADWB of GaAs-to-Si.

Run	Replicate	Bond Efficiency (%)			
		After Room Temperature Contact		After 140°C Annealing	
		Bonded	Unbonded	Bonded	Unbonded
1	1	97	3	93	7
	2	>99	0	0	100
2	1	97	3	0	100
	2	98	2	0	100
3	1	>99	0	0	100
	2	96	4	0	100
4	1	96	4	0	100
	2	>99	0	0	100
5	1	98	2	98	2
	2	99	1	99	1

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6	1	99	1	99	1
	2	99	1	99	1
7	1	>99	0	0	100
	2	99	1	0	100
8	1	99	1	99	1
	2	95	5	95	5

4.3.2 Effects of Ar Plasma on the Bond Energy of PADWB of GaAs-to-Si

Infrared images of the razor blade insertions and the corresponding crack lengths at the 2³ factorial design of Ar PADWB of GaAs-to-Si interfaces are presented in Figure 4-3. The bonding surfaces of these interfaces were subjected to the experimental conditions of Table 4-2 and annealed at 140°C for 24 h under a normal atmospheric condition. The corresponding post-annealing specific bond energies of the bonded wafers were calculated based on the crack opening method as outlined in Section 3.2.2 and using the crack length data in Figure 4-3 with Equation (3-4). The results are presented in Table 4-4. The term ‘Run Average’ in the table denotes the average of the bond energy results of Replicates 1 and 2 of each experimental run. The results show that most of the high bond energy values were associated with the plasma RF power of 200 W. Almost all of the GaAs-to-Si bonded pairs of Runs 1 to 4, which corresponded to a plasma exposure of 100 W, debonded after annealing at 140°C for 24 h under a normal atmospheric condition.

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Run	Replicate 1	Replicate 2
1		<i>Debonded</i>
2	<i>Debonded</i>	<i>Debonded</i>
3	<i>Debonded</i>	<i>Debonded</i>
4	<i>Debonded</i>	<i>Debonded</i>

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Run	Replicate 1	Replicate 2
5
6
7	<i>Debanded</i>	<i>Debanded</i>
8

Figure 4-3: Infrared images of the razor blade insertions into the 2^3 factorial design of Ar PADWB of 2-inch GaAs-to-Si interfaces after 140°C of low temperature annealing for 24 h under a normal atmospheric condition. The corresponding crack lengths are shown as inserts.

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Table 4-4: Post-annealing specific bond energy results of the 2^3 factorial design of Ar PADWB of GaAs-to-Si.

Run	Factor Code			Post-Annealing Specific Bond Energy (mJ/m ²)		
	A	B	C	Replicate 1	Replicate 2	Run Average
1	-	-	-	66	0 (<i>Debonded</i>)	33
2	+	-	-	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)
3	-	+	-	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)
4	+	+	-	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)
5	-	-	+	371	337	354
6	+	-	+	369	478	424
7	-	+	+	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)	0 (<i>Debonded</i>)
8	+	+	+	422	387	405

The analysis of variance (ANOVA) on the 2^3 factorial design of Ar PADWB of GaAs-to-Si post-annealing specific bond energy results was manually computed [5] and the results are shown in Table 4-5. The F-test statistic (indicated by 'F_o' in the table) is the ratio of the variance of bond energy due to a changing factor (or factors interaction) level to the variance due to experimental noise. The P-value denotes the probability that a change in bond energy is solely due to experimental noise. Hence, F_o and P-value have an inverse relationship and a high F_o and low P-value of an influencing factor (or factors interaction) would imply that it has significant effect. As a statistical standard, a 95% confidence level is

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Table 4-5: The analysis of variance (ANOVA) results of 2^3 factorial design of Ar PADWB of GaAs-to-Si.

Source of Variation	F_o^a	P-value ^b	Significance
Exposure time (A)	41.71	0.0002	High
Pressure (B)	35.19	0.0003	High
RF Power (C)	282.41	<0.0001	High
Exposure time-pressure (AB) factors interaction	28.94	0.0007	High
Exposure time-RF power (AC) factors interaction	55.09	<0.0001	High
Pressure-RF power (BC) factors interaction	24.68	0.0011	High
Exposure time-pressure-RF power (ABC) factors interaction	19.49	0.0022	Average

^a F_o is the F-test statistic.

^b P-value is the probability that a result changes is solely due to experimental noise.

used. Hence, a P-value of an influencing factor (or factors interaction) of less than 0.05 is deemed to be significant. The statistical results in Table 4-5 indicate that all plasma factors and factors interactions affected the bond energy significantly as all the P-values were less than 0.05. The factor of plasma RF power had the largest degree of effect while the three factors of interaction of exposure time, pressure, and RF power had the least influence.

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Figure 4-4: The grand average post-annealing specific bond energy associated with each plasma factor at each level of Ar PADWB of GaAs-to-Si.

To illustrate the extent of influence by each plasma factor, a grand average post-annealing specific bond energy was calculated for each level of each plasma factor. For the example with the plasma RF power factor, Runs 1 to 4 involved a low level (100 W) of plasma RF power exposure on the GaAs and Si bonding surfaces while Runs 5 to 8 involved a high level (200 W) of plasma RF power exposure. Two grand averages associated with the RF power factor were thus determined from the post-annealing specific bond energy results in Table 4-4 of Replicates 1 and 2 of Runs 1 to 4 (low power level) and of Replicates 1 and 2 of Runs 5 to 8 (high power level). The corresponding low and high level grand averages of the plasma RF power factor were 8 mJ/m² and 296 mJ/m², respectively. The same was repeated for exposure time and pressure factor and the results are shown in Figure 4-4.

Effects of Ar plasma RF power on the PADWB GaAs-to-Si bond energy

As observed in Figure 4-4, the change in the grand average post-annealing specific bond energy of the 2^3 factorial design of Ar PADWB of GaAs-to-Si was the greatest when the Ar RF plasma power was changed from a low 100 W to a high 200 W level. This result indicates that the RF plasma power has the most significant effect. The ANOVA results in Table 4-5 also justify this finding with the RF power factor having the highest F_0 value of 282.41 while its corresponding P-value is much lesser than 0.0001.

Figure 4-5 and Figure 4-6 show the water silhouettes on the GaAs and Si surfaces, respectively, which were subjected to the 2^3 factorial design Ar plasma conditions sets (see Table 4-1 and Table 4-2). The corresponding contact angles are shown in the figures as inserts. Images (b) to (e) in Figure 4-5 and Figure 4-6 correspond to a low level of 100 W while images (f) to (i) correspond to a high level of 200 W plasma RF power exposure on GaAs and Si surfaces, respectively. The results indicate that the hydrophilicity of the GaAs and Si surfaces was low when they were treated with the 100 W of low plasma RF power level. Hence, the corresponding contact angles were larger. However, for surfaces that were exposed with 200 W of high plasma RF power level, the water droplets spread too far apart that the silhouettes could not be observed. Hence, the surfaces were deemed to be in superhydrophilic states and the contact angles were less than 5° as indicated in the inserts in images (f) to (i) of Figure 4-5 and Figure 4-6. The results clearly indicate that the Ar plasma RF power has a large influence over the surface hydrophilicity. Consequently, this degree of activation will affect the amount of bond energy.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Figure 4-5: Water droplet silhouette images of (a) untreated bare GaAs reference surface and GaAs surfaces exposed with (b) Run 1, (c) Run 2, (d) Run 3, (e) Run 4, (f) Run 5, (g) Run 6, (h) Run 7, and (i) Run 8 of the 2^3 factorial design Ar plasma conditions (see Table 4-1 and Table 4-2). The corresponding contact angles are indicated as inserts.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Figure 4-6: Water droplet silhouette images of (a) untreated bare Si reference surface and Si surfaces exposed with (b) Run 1, (c) Run 2, (d) Run 3, (e) Run 4, (f) Run 5, (g) Run 6, (h) Run 7, and (i) Run 8 of the 2^3 factorial design Ar plasma conditions (see Table 4-1 and Table 4-2). The corresponding contact angles are indicated as inserts.

In hydrophilic direct wafer bonding of a GaAs-to-Si, two governing bonding mechanisms are occurring at the bonding interface during annealing [6-8]. The first mechanism is associated with the hydrogen bonding among adsorbed monolayers of water molecules (H_2O) and hydroxyl groups ($-OH$) of Gallium Arsenide hydroxyl ($GaAs-OH$) and silanol ($Si-OH$) species on the hydrophilic bonding surfaces. The second mechanism is derived from the polymerization process (similar to Equation [2.1]) among the oppositely pairs of $GaAs-OH$ and $Si-OH$ as

to evolve strong interfacial covalent oxygen bridges between the GaAs and Si ($GaAs-O-Si$) [9], which are accompanied by the out-diffusion of water molecules away from the bonding interface. As the polymerization process involves the reaction between $-OH$ groups of the $GaAs-OH$ and $Si-OH$ species, these reacting species have to be in sufficiently close proximity

at a molecular level before they can start to polymerize. Michalske and Fuller, Jr., mentioned that the separation distance between a pair of oppositely -OH groups has to be lesser than 4 Å before they can start polymerizing to evolve an oxygen bridge [10]. Such a condition is met only at the central region of the bonding interface of GaAs-to-Si during annealing because of the dire existence of a severe thermal mismatch between GaAs and Si [11]. The effect of the thermal-mismatch stress will be discussed in details in Chapter 5.

In parallel to the findings of Michalske and Bunker [12] and Tan *et al.* [13], it is highly possible that the high energetics of the bombarding Ar species at a high RF power level such as 200 W is capable of inducing significant damages to the native oxides of Si and GaAs. The oxides will be highly strained and reactive to result in a high number of GaAs-OH and Si-OH that will adsorb a large amount of H₂O molecules. Consequently, the bonding surfaces will be superhydrophilic with extremely low contact angles, as seen in images (f) to (i) of Figure 4-5 and Figure 4-6, and the degree of activation is deemed to be high. With the high numbers of GaAs-OH and Si-OH surface species and adsorbed H₂O molecules that are derived from the high plasma RF power level, the extent of hydrogen bonding and GaAs-O-Si evolved through the polymerization process will be high at the bonding interface during annealing. Furthermore, the density of the native oxides of GaAs and Si could also be reduced through the high energetics Ar species bombardment events at the high RF power level, evolving into a more porous open network structure. This will enhance the out-diffusion of water molecules away from the bonding interface during annealing, promoting the polymerization reaction of Equation 4.1 further to evolve a higher amount of GaAs-O-Si bridges at the central region of the bonding interface.

In the severe thermally-mismatched bonding system of GaAs-to-Si, the CTE mismatch is by a factor of more than 2. During annealing at an elevated temperature of 140°C, the thermal-mismatch stress can be strong enough to cause debonding failure. A high

bond energy through strong surface activation, such as plasma treatment at a high RF power level of 200 W, is necessary to restrain the failure. This accounts for why nearly all the 200 W Ar plasma-activated bonded pair (replicates of Runs 5 to 8 in Table 4-4) remained intact with high post-annealing specific bond energies after annealing at 140°C for 24 h under a normal atmospheric condition.

The opposite is to be implied when the bonding surfaces of a GaAs and Si pair are subjected to an Ar plasma exposure of low RF power level such as 100 W. The energies of the Ar species may be too low to induce sufficient damages to the native oxides. Consequently, the surfaces of GaAs and Si will be weakly activated with little amount of -OH groups and few H₂O molecules adsorbed. Furthermore, the out-diffusion of the water molecules away from the bonding interface though the native oxides will be inefficient. Hence, the extent of hydrogen bonding and GaAs-O-Si evolved through the polymerization process will be low. These explain why nearly all the replicates of Runs 1 to 4 in Table 4-4 debonded after annealing at 140°C for 24 h under a normal atmospheric condition. The bond energies associated with the 100 W of low Ar plasma RF power level were too low to prevent the debonding failures caused by the substantial thermal-mismatch stress during annealing.

To justify further the presence of the low energetics Ar species associated with the low plasma RF power level of 100 W, the post-annealing specific bond energy results in Table 4-4 is referred to once more. As observed from the table, almost all the bonded pairs of Runs 1 to 4 have the same energies of 0 mJ/m² (debonded) although the pressure and exposure time factor levels are changed. This implies that both of these plasma factors had no effects on the bond energy when the RF power factor was at its low level of 100 W. The Ar species at this low level of RF plasma power possessed energies too low to damage the bonding surfaces of GaAs and Si sufficiently. Hence, any changes to the amount of Ar species though the plasma pressure and/or exposure time will not induce further effects on the

surfaces. The degree of activation (and, thus, the resultant bond energy) will remain unchanged. Contrary, the fluctuations in post-annealing specific bond energy results are found to be among the replicates of Runs 5 to 8 in Table 4-4. The GaAs and Si surfaces of these replicates were subjected to different pressure and exposure time levels at a high RF plasma power level of 200 W. This observation suggests that, when the RF power factor is high and the associated high energetics of the bombarding Ar species is capable of inducing significant damage to the bonding surfaces, changes to the amount of Ar species though the plasma pressure and/or exposure time can then alter the surface morphology and chemistry further to change the bond energy. These conjectures agree with the ANOVA results in Table 4-5, which indicate that both the exposure time-power and pressure-power factors interactions effects were significant (with P-values much lesser than 0.05).

Effects of Ar plasma exposure time and pressure on the PADWB GaAs-to-Si bond energy

The effects of plasma exposure time and pressure on the bond energy of Ar PADWB of GaAs-to-Si can be observed from the post-annealing specific bond energy results of Runs 5 to 8 in Table 4-4. These runs corresponded to a fixed high level of RF plasma power of 200 W where the Ar species acquired ample energy to activate surfaces to a large extent and the effects of exposure time and pressure can then influenced the bond energy further. The highest Run Average was associated with Run 6, which had a value of 424 mJ/m². On the other extreme, the lowest Run Average was 0 mJ/m² for Run 7. Both Replicates 1 and 2 of Run 7 debonded after annealing at 140°C for 24 h under a normal atmospheric condition. Run 6 involved plasma exposure at a high exposure time factor level of 30 s and a low pressure factor level of 120 mTorr while Run 7 involved plasma exposure at a low exposure time factor level of 5 s and a high pressure factor level at 200 mTorr. These observations show that both plasma exposure time and pressure have an influence over bond energy. This was

reflected in the ANOVA results of Table 4-5, which also indicate that their interaction can affect the bond energy of Ar PADWB of GaAs-to-Si. The P-values associated with exposure time and pressure factors and the exposure time-pressure factors interaction were well below the standard P-value of 0.05, indicating that all were significant.

The observations made from the average results of Run 6 and Run 7 in Table 4-4 suggest that a high bond energy is derived from a long exposure time and low pressure plasma conditions. Figure 4-4 depicts these findings. The grand average post-annealing specific bond energies changed to a certain extent when the exposure time and pressure factor levels were changed and high bond energies corresponded to high and low levels of exposure time and pressure, respectively. To understand how plasma exposure time and pressure can influence the bond energy of Ar PADWB of GaAs-to-Si, the plasma treated GaAs and Si surfaces were being investigated.

From a surface chemical state perspective, the different factor levels of exposure time and pressure did not induce any observable changes to the GaAs and Si surface hydrophilicity when the exposures were carried out at a high RF power level of 200 W. Images (f) to (i) of Figure 4-5 and Figure 4-6 that correspond to GaAs and Si surfaces, respectively, were exposed with different combinations of levels of low and high of exposure time and pressure at 200 W. The images show that superhydrophilic states are associated with all the GaAs and Si surfaces and the contact angles are less than 5° . This observation proves that, at 200 W plasma RF power, changes to exposure time and/or pressure factor levels will not affect GaAs and Si surface hydrophilicity and the surfaces will be in superhydrophilic states since they are saturated with high amounts of -OH surface groups and adsorbed H₂O molecules. Upon subsequent room temperature contact and anneal, the extent of the hydrogen bonding and the localized GaAs-O-Si evolved at the central region through the polymerization process of Equation 4-1 should be high at the bonding interfaces of all the replicates in Runs 5 to 8.

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However, both bonding replicates of Run 7 debonded after the thermal treatment as seen in Table 4-4.

To understand how the different plasma parameters can affect GaAs and Si surface morphology, AFM work was performed and the surface roughness was investigated. The 3-D surfaces of the GaAs and Si that were subjected to the various 2^3 factorial design Ar plasma conditions sets (see Table 4-1 and Table 4-2) are shown in Figure A-1 and Figure A-2, respectively, in the Appendix Section. The corresponding surface roughness data are shown in Figure 4-7 and Figure 4-8 for the GaAs and Si surfaces, respectively.

Figure 4-7: Surface roughness data of the GaAs surfaces subjected to the different 2^3 factorial design Ar plasma conditions sets (see Table 4-1 and Table 4-2).

Figure 4-8: Surface roughness data of the Si surfaces subjected to the different 2^3 factorial design Ar plasma conditions sets (see Table 4-1 and Table 4-2).

Figure 4-7 and Figure 4-8 reveal that the surface roughness values of the GaAs and Si corresponding to Runs 1 to 4, were similar to the untreated bare reference surfaces. These surfaces were subjected to different pressure and exposure time factor levels at a low plasma RF power level of 100 W. However, the surface roughness values of GaAs and Si surfaces of Runs 5 to 8 in Figure 4-7 and Figure 4-8 were generally higher and they changed accordingly at different factor levels of exposure time and pressure at a high plasma RF power level of 200 W. These observations further demonstrate that the Ar species will have ample energy to bombard bonding surfaces to great extents only when the plasma RF power level has attained the sufficiently high level of 200 W. Thereafter, the exposure time and pressure can induce further effects.

The effect by plasma pressure on the surface roughness of GaAs and Si can be observed by comparing the results of Runs 5 and 6 against the results of Runs 7 and 8 in Figure 4-7 and Figure 4-8, respectively. Runs 5 and 6 correspond to a low pressure factor

level of 120 mTorr while Runs 7 and 8 correspond to a high pressure factor level of 200 mTorr (see Table 4-1 and Table 4-2). Figure 4-7 and Figure 4-8 illustrate that the surface roughness values of GaAs and Si were generally higher when the surfaces were subjected to the high plasma pressure factor level of 200 mTorr in Runs 7 and 8. However, when the surfaces were exposed with 120 mTorr of low pressure factor level in Runs 5 and 6, the surfaces were not as rough.

The findings indicate that a high plasma pressure level will lead to surface roughening. Similar to the effect induced by thermal-mismatch stress discussed in 0, a high amount of -OH groups of oppositely GaAs-OH and Si-OH surface species at the central region of the bonding interface will not be close enough to get polymerized (see Equation [4.1]) during annealing if the surface roughness is increased by subjecting the bonding surfaces to the high level of plasma pressure exposure of 200 mTorr. Consequently, the amount of the localized GaAs-O-Si evolved will be lowered and the resulting bond energy will be too weak to prevent the debonding failure cause by the pronounced thermal-mismatch stress during annealing at an elevated temperature. This explains why both pairs of the bonding replicates in Run 7 in Table 4-4 were debonded after annealing at 140°C for 24 h under a normal atmospheric condition.

Interestingly, Table 4-4 shows that, when the plasma exposure time was changed from the low level of 5 s (Run 7) to the high level of 30 s (Run 8) at high pressure and RF power factor levels of 200 mTorr and 200 W, respectively, the post-annealing specific bond energy of the Ar PADWB of GaAs-to-Si changed drastically after the thermal treatment. Under the former plasma conditions, the bonding pairs were debonded as discussed in the previous paragraph. However, the bonding surfaces that were subjected to the latter plasma conditions remained bonded with rather high bond energies of 422 mJ/m² and 387 mJ/m².

These findings suggest that a prolonged plasma exposure duration of 30 s could prevent the bond energy from deterioration caused by a high plasma pressure of 200 W.

As can be observed from Figure 4-7 and Figure 4-8, the surface roughness of GaAs and Si, respectively, were decreased when the plasma exposure time was longer in Run 8 as compared to Run 7. This indicates that an extended plasma exposure time could indemnify the negative effect of surface roughening caused by higher plasma pressure exposure. When the exposure time is too short, the plasma is deemed to be in a transient state and the bombarding effects by the energetic Ar species at high pressure and RF power level would not be uniform across an exposing surface. As a result, the surface roughness will be high. However, when the exposure duration is sufficiently long enough, the plasma will be in a stable state and the bombarding effects by the energetic Ar species at high pressure and RF power level will be averaged out and become uniform across the exposing surface. Hence, with a smoother surface, more of the reacting -OH groups of the oppositely GaAs-OH and Si-OH surface species at the central region of the bonding interface can then be polymerized during annealing to yield a higher amount of localized interfacial GaAs-O-Si. Alongside the hydrogen bonding among the unreacted -OH groups and the interfacial adsorbed H₂O molecules, the bond energy will be adequately high enough to arrest the failure of debonding induced by thermal-mismatch stress during annealing. This accounts for the ANOVA results in Table 4-5 that indicate that the plasma exposure time factor and the exposure time-pressure factors interaction have a significant effect on the post-annealing specific bond energy of Ar PADWB of GaAs-to-Si. Consequently, extended plasma duration could maintain a smoother surface by compensating for the surface roughening effect induced by a high plasma pressure exposure.

4.4 Conclusions

The present investigation on the Ar PADWB of GaAs-to-Si through statistical means revealed that the three plasma parameters of exposure time, pressure, and RF power and the interactions among them affected the bond energy significantly. The effects brought by each influencing factor and the interactions between the factors can be explained by considering their hydrophilization and roughening effects on the GaAs and Si bonding surfaces. These effects have direct consequences on the degree of bond energy. While a high RF plasma power is necessary for the onset of a strong surface activation with a high number of reacting GaAs-OH and Si-OH surface species to start with, a low Ar pressure and a long exposure time are essential in ensuring the bonding surfaces to be smooth for more reacting groups at the central region of a bonding interface to come in close proximity and get polymerized during annealing. The developed set of plasma conditions was found to be 5 s, 120 mTorr, and 200 W of exposure time, pressure, and RF power, respectively, and the derived bond energy was 424 mJ/m^2 on the average.

The current highest bond energy value of 424 mJ/m^2 achieved through plasma activation was twice the amount reported in [14], where the GaAs-to-Si bonding was performed with wet activation. This accredits PADWB as a viable form of low temperature bonding solution which is essential in bonding thermally-mismatched dissimilar materials. However, the present highest bond energy of Ar PADWB of GaAs-to-Si after annealing at 140°C under a normal atmospheric condition for 24 h is still much lower than the reported energy values of the homogenous thermally matched bonded system of Si-to-Si [3].

Nevertheless, the efforts until this point of research have developed the plasma conditions in Ar PADWB of GaAs-to-Si by ensuring that the bonding surfaces are of low surface roughness and are highly saturated with reactive -OH groups that can potentially be polymerized during annealing. In Chapter 5, an insight into the thermal-mismatch stress and

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how it will affect the bond energy of GaAs-to-Si will be provided, followed by the presentation of a novel annealing technique that will result in a much higher bond energy from this high amount of -OH surface reacting groups.

References

- [1] S. N. Farrens, J. R. Dekker, J. K. Smith, and B. E. Roberds, "Chemical free room temperature wafer to wafer direct bonding," *Journal of the Electrochemical Society*, vol. 142, iss. 11, pp. 3949-55, 1995.
- [2] O. Zucker, W. Langheinrich, M. Kulozik, and H. Goebel, "Application of oxygen plasma processing to silicon direct bonding," *Sensors and Actuators A (Physical)*, vol. A36, iss. 3, pp. 227-31, 1993.
- [3] T. Suni, K. Henttinen, I. Suni, and J. Makinen, "Effects of plasma activation on hydrophilic bonding of Si and SiO₂," *Journal of the Electrochemical Society*, vol. 149, iss. 6, pp. 348-51, 2002.
- [4] K. Mitani, *Wafer bonding : studies of interface bubbles and electrical characterization / by Kiyoshi Mitani*: Ann Arbor, Mich. : UMI, 1991.
- [5] D. C. Montgomery, *Design and analysis of experiments [electronic resource] / Douglas C. Montgomery*: Hoboken, NJ : Wiley, 7th ed., 2009.
- [6] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
- [7] Q. Y. Tong and U. Gosele, "A model of low-temperature wafer bonding and its applications," *Journal of the Electrochemical Society*, vol. 143, iss. 5, pp. 1773-9, 1996.
- [8] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [9] Q. Y. Tong, "Wafer bonding for integrated materials," *Materials Science and Engineering B: Solid-State Materials for Advanced Technology*, vol. 87, iss. 3, pp. 323-8, 2001.
- [10] T. A. Michalske and E. R. Fuller Jr, "closure and repropagation of healed cracks in silicate glass," *Journal of the American Ceramic Society*, vol. 68, pp. 586-90, 1985.
- [11] E. Suhir, "Stresses in bi-metal thermostats," *Transactions of the ASME. Journal of Applied Mechanics*, vol. 53, pp. 657-60, 1986.
- [12] T. A. Michalske and B. C. Bunker, "Slow fracture model based on strained silicate structures," *Journal of Applied Physics*, vol. 56, iss. 10, pp. 2686-93, 1984.
- [13] C. M. Tan, W. Yu, and J. Wei, "Comparison of medium-vacuum and plasma-activated low-temperature wafer bonding," *Applied Physics Letters*, vol. 88, iss. 11, pp. 114102-1-3, 2006.
- [14] V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gosele, "Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 12, pp. 2141-3, 1989.

Chapter 5 Development of the Heat Treatment Process in the Direct Wafer Bonding of GaAs-to-Si

5.1 Introduction

A room temperature contacted wafer pair (after surface activation) would usually undergo one final stage of thermal treatment to strengthen the bonding interface. A high bond energy is essential in permitting the bonded pair to withstand the harsh condition of a mechanical thinning process, such as lapping, polishing, or chemical mechanical polishing (CMP), or a long period of an aggressive chemical treatment, such as hydrofluoric (HF) acid immersion in an epitaxial lift-off process [1]. These processes were discussed in Section 2.4.

It has been demonstrated that, in general, the bond energy of a bonding pair will increase with increasing annealing temperature in general [2, 3]. However, in the bonding of thermally-mismatched dissimilar materials, the temperature cannot be increased indefinitely to yield a strongly bonded interface since doing so will result in debonding or fracture failure [4, 5]. Other downsides of high temperature anneals include unintended species diffusion, distortion of metal patterns in pre-processed wafers, and material degradation [6].

Hence, several low temperature solutions have been developed to fulfill the low thermal constraint [7, 8]. By far, the technique of performing the entire bonding process under a ultra-high vacuum (UHV) condition has proven to be the most viable low temperature solution since it achieves a bonded interfacial strength that exceeds the fracture strengths of bonded bulk materials [9-17]. However, the requirement of a labyrinthine and the costly setup required to conduct the entire bonding process in an UHV environment has deemed this technique ill-suited to mass production.

Through the present research efforts, a novel low temperature sequential-step annealing technique has been developed. This technique has been shown able to yield a high bonded interfacial energy, which is comparable to that derived from UHV bonding. Low-cost, simplicity, and compatibility with the present microfabrication facilities are also important considerations in manufacturing and are the main drivers towards the innovation of this technique.

Prior to the presentation of the novel low temperature bonding solution, the basic bonding principles in a homogenous bonding system will be presented. In addition, the reason why the bond energy derived from it is generally higher than that of heterogenous bonding system on a wafer-scale will be provided.

5.1.1 Basic Bonding Principles of a Homogenous Thermally-Matched Si-to-Si Hydrophilic Bonding System during Annealing

Tong et al. [18] showed experimentally that full polymerization would have been realized at an annealing temperature of 150°C in a hydrophilic bonding system of homogenous thermally-matched Si-to-Si. Figure 5-1 shows the post-annealing specific bond energy as a function of the annealing temperature, which a best-fit curve was drawn through the series of bond energy data. The data in this figure was adapted from Tong et al. [18] and re-plotted herein. The Si bonding surfaces were conventionally wet-activated and deemed hydrophilic with chemical solutions of ammonium hydroxide (NH₄OH), hydrogen peroxide (H₂O₂) and hydrochloric acid (HCl). The figure reveals that the specific bond energy of the wet-activated direct wafer bonding (WADWB) of Si-to-Si starts to saturate at an annealing temperature of 150°C and dramatically increases again from a temperature of 800°C (a temperature that is much too high to be applicable in the current efforts of bonding severe thermally-mismatched GaAs-to-Si).

Figure 5-1: The post-annealing specific bond energy of hydrophilic WADWB of homogenous thermally matched Si-to-Si as a function of the annealing temperature. The data are adapted from [18].

Fortunately, a strong bond energy in excess of 1000 mJ/m^2 can be achieved at a low annealing temperature of 150°C (as evidenced in Figure 5-1), which is permissible in a GaAs-to-Si bonding system. In principle, this temperature could also achieve the same high bond energy. Hence, the bonding mechanisms within the annealing temperature range of 20°C (room temperature) to 150°C are of particular interest.

Tong et al. [19] proposed and modeled two thermally activated bonding mechanisms associated with the two temperature ranges of 20°C - 110°C and 110°C - 150°C . In the former temperature range, the bond energy is mainly derived from the hydrogen bonding among interfacial water (H_2O) molecules and hydroxyl ($-\text{OH}$) groups. As the annealing temperature

is increased within this range, it is energetically favorable for the H₂O molecules to evolve into more stable cyclic structures of closer mutual interactions. For example, four interfacial H₂O molecules between a pair of hydrophilic Si bonding surfaces will hydrogen bond to form a simple straight chain structure after room temperature contact. Upon annealing, they can also evolve into a cyclic structure (cyclic tetramer). The binding energy of the latter is greater than the bonding energy of the former by a factor of 1.5 [20].

Within the elevated temperature range of 110°C to 150°C, the interfacial H₂O molecules start to diffuse away from the bonding interface and a chemical process of polymerization among the oppositely pairs of close proximity -OH groups of silanol (Si-OH) surface species proceeds as

This polymerization results in strong covalent oxygen bonds between the pair of Si (Si-O-Si), with the further out-diffusion of H₂O by-products. The polymerization process of the WADWB of Si-to-Si was found to be completed at an annealing temperature of 150°C with a specific bond energy of about 1200 mJ/m² (see Figure 5-1) [18].

Michalske and Fuller, Jr. [21] documented that the thermal energy even at room temperature is already sufficient for the polymerization reaction of Equation (2-1) to proceed provided that the -OH groups are adjacent to each other. Tong et al. study found that the initiation of the polymerization occurs only at an elevated temperature of 110°C because, at this temperature, the associated thermal effect initiates the breakage of the H₂O molecules away from the hydrogen bonding with the bonding surface -OH groups. Subsequently, the H₂O molecules will diffuse away from the bonding interface. This was further justified by Michalske and Bunker [22] who reported that the complete desorption of H₂O molecules on a silica surface can only be realized at temperatures in excess of 120°C. Hence, upon the

removal of excess H₂O, the oppositely pairs of -OH groups can then come into sufficient proximity to be polymerized.

Most of the low temperature wafer bonding solutions achieve relatively high bond energy at low temperatures by getting rid of the excess interfacial H₂O molecules without the use of the thermal effect. This permits the polymerization process to proceed at low temperatures. In the example given in Chapter 4, the use of the Argon (Ar) plasma activation to induce porosity in the native oxides of GaAs and Si provided an additional route for the H₂O molecules to out-diffuse away from the bonding interface [23]. The low temperature technique of bonding in a vacuum environment is also associated with this enhancement principle because the vacuum acts to extract the excess H₂O molecules out from the bonding interface forcefully [24, 25].

5.1.2 Thermal Mismatch-Induced Peeling Stress of a Bonding Pair of GaAs-to-Si during Annealing

Despite having developed the Ar plasma process in the plasma-activated direct wafer bonding (PADWB) of GaAs-to-Si (refer to Chapter 4), the associated post-annealing specific bond energy of 424 mJ/m² (see Table 4-4) after 140°C of annealing under a normal atmospheric condition was still far below the 1200 mJ/m² energy of the conventional WADWB of Si-to-Si with 150°C of annealing (see Figure 5-1) [18]. The specific bond energy of the present PADWB of GaAs-to-Si was lower than that of the WADWB of Si-to-Si by a factor of nearly 3. Lehman et al. [26], who had bonded 3 inch GaAs to 4 inch Si, also found that the bond energy was much lower than that of Si-to-Si under the same set of bonding conditions.

A direct reason why the much lower bond energy resulted in the present Ar PADWB of GaAs-to-Si is the extent of polymerization of

between oppositely -OH reacting groups of Gallium Arsenide hydroxyl (GaAs-OH) and Si-OH bonding surface species is very low. Since the plasma treatment is known to damage and induce porosity in the GaAs and Si native oxides, which will further enhance the out-diffusion of water (H₂O) molecules away from the bonding interface during annealing [23], the oppositely pairs of reacting -OH groups should be able to come close enough to react. Hence, it can be concluded that it is the intrinsic property of material mismatch in the bonding of GaAs-to-Si that prevents the -OH groups from getting close enough to polymerize during annealing.

Equivalent to the great hindrance of the lattice and crystal mismatch in a heteroepitaxy growth, the thermal mismatch intrinsic to the bonding of dissimilar materials poses a major obstacle in wafer bonding. A detailed analysis and modeling work on the thermal stresses that exist in a dissimilar materials bimetallic strip during heating was performed by Suhir [27], which is applicable in the present GaAs-to-Si bonding system [5].

During the annealing of GaAs-to-Si, four main thermal mismatch-induced stresses exist as shown in Figure 5-2: 1) normal out-of-plane stress, σ_z , 2) normal in-plane stress, σ_{xy} , 3) peeling out-of-plane stress, σ_p , and 4) shear in-plane stress, τ_{xy} , with respect to the common bonding interface xy-plane. At an elevated temperature, the overall bonding structure will assume the curved geometry as shown in the figure since the coefficient of thermal expansion of GaAs is higher than that of Si. The bow geometry is evolved to allow the GaAs and Si to relax as much as possible as the GaAs will expand more than the Si. Nevertheless, both are dimensionally constrained by the common bonding interface. Among

Figure 5-2: A schematic illustration showing the various thermal mismatch-induced stresses that exist in a GaAs-to-Si bonding pair at an elevated temperature.

the various thermal mismatch-induced stresses, the peeling stress is the most vexatious as it causes debonding, which is a commonly observed failure in wafer-scale bonding systems of dissimilar materials that are several hundreds of micrometers thick. Hence, peeling stress will be the focus of attention in the following discussion and its ill-effect on the bonding of GaAs-to-Si will be elaborated.

Peeling stress has the effect of pulling a bonding pair of dissimilar materials apart at temperatures other than the temperature at which they were contacted together initially. It can be observed from Figure 5-2 that the peeling stress is located at the edges of the bonding GaAs and Si at a direction perpendicular to the bonding interface plane. From a macroscopic point of view, the peeling stress can be seen to be opening the bonding interface by prying the bonding pair apart.

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In the case of bonding circular-size wafers, the peeling stress, σ_p , is a function of the radial distance, r , from the center of the bonding structure. It is expressed as

$$\sigma_p = \sigma_{p,max} e^{-C(R-r)}, \quad (5-1)$$

where $\sigma_{p,max}$ is the maximum peeling stress, located at the edges of the bonding wafers (the radial distance from the center to the edges of the bonding wafers is equivalent to the radius, R), and is expressed as

$$\sigma_{p,max} = \tau \delta \Delta \alpha \Delta T, \quad (5-2)$$

where $\Delta \alpha$ is the difference in the coefficient of thermal expansion (CTE), α , between the GaAs and Si, which is defined as

$$\Delta \alpha = \alpha_{GaAs} - \alpha_{Si}, \quad (5-3)$$

and ΔT is the difference between the temperature at which the wafers are contacted together (which is at room temperature, T_{rm} , in the present case) and the temperature, T_A , up to which the bonding pair is being annealed. Hence, ΔT can be expressed as

$$\Delta T = T_A - T_{rm}. \quad (5-4)$$

τ , C and δ are constants involving the bonding GaAs and Si material and dimensional constants. They are expressed as

$$\tau = \frac{1}{2} \frac{E_{GaAs} t_{GaAs}^3 t_{Si} (1 - v_{Si}^2) - E_{Si} t_{Si}^3 t_{GaAs} (1 - v_{GaAs}^2)}{E_{GaAs} t_{GaAs}^3 (1 - v_{Si}^2) - E_{Si} t_{Si}^3 (1 - v_{GaAs}^2)}, \quad (5-5)$$

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$$C = \sqrt{\frac{\beta}{\frac{2t_{GaAs}(1+v_{GaAs})}{3E_{GaAs}} + \frac{2t_{Si}(1+v_{Si})}{3E_{Si}}}} \quad (5-6)$$

where

$$\beta = \frac{1-v_{GaAs}^2}{E_{GaAs}t_{GaAs}} + \frac{1-v_{Si}^2}{E_{Si}t_{Si}} + \frac{3(t_{GaAs}+t_{Si})^2(1-v_{GaAs}^2)(1-v_{Si}^2)}{E_{GaAs}t_{GaAs}^3(1-v_{GaAs}^2) + E_{Si}t_{Si}^3(1-v_{Si}^2)}, \quad (5-7)$$

and

$$\delta = \frac{C^2}{\beta}, \quad (5-8)$$

respectively. t , v , and E are the thickness, Poisson's ratio, and Young's modulus, respectively, of the bonding GaAs and Si.

Table 5-1: Material and dimensional properties of the present bonding efforts between 2-inch GaAs and Si.

Material	Property			
	Young's Modulus, E	Poisson's Ratio, v	Thickness, t	Radius, R
	(GPa)	(unitless)	(μm)	(mm)
GaAs	119	0.29	450	25.5
Si	130	0.29	275	25.5

Figure 5-3: The peeling stress, σ_p , as a function of the radial distance, r , from the center of a 2-inch circular (approximately 25.5 mm in radius) GaAs-to-Si bonding pair at different annealing temperatures.

The list of parameters required in Equation (5-1) to Equation (5-8) to determine the peeling stress in the present efforts of bonding 2-inch circular (approximately 25.5 mm in radius) of GaAs and Si wafers that are several hundreds of micrometers thick is tabulated in Table 5-1. Figure 5-3 shows the results of theoretical peeling stress, σ_p , on the bonding wafers, as a function of the radial distance from the center, r , at various annealing temperatures, T_A , up to 160°C, which is the maximum annealing temperature at which the debonding failure of a thick wafer-scale size GaAs-to-Si bonding pair would most commonly be observed [26, 28].

Foremost, it can be observed from Figure 5-3 that the increment in the peeling stress, σ_p , starts only at a radial distance, r , of 24.9 mm from the center (hence, values of σ_p for r lesser than 24.9 mm were not considered because they were negligible) and that it grows exponentially with increasing r . Hence, the peeling stress is present from the edge towards the center within a region that is only 2% of the radius. The maximum peeling stress, $\sigma_{p,max}$,

is located at the edges of the 2-inch GaAs and Si bonding wafers. The edges are located at a radial distance, R , of 25.5 mm (approximately the radius of a 2-inch circular wafer) from the center. Thus, σ_p can be approximated to $\sigma_{p,max}$ that is located at the edges of the bonding 2-inch GaAs and Si wafers. The magnitude of $\sigma_{p,max}$ at a particular temperature is the same for GaAs and Si but is in the opposite direction and is normal to the bonding interface plane as shown in Figure 5-2.

As the prying effect of the maximum peeling stress, $\sigma_{p,max}$, acts to counteract the bonding interfacial strength, σ_{int} , debonding failure will result if the condition of

$$\sigma_{int} < \sigma_{p,max} \quad (5-9)$$

is met. To justify further, the bonding work of PADWB of bare Si to thermally oxidized Si by Tan *et al.* [23] is referred to. In their homogenous thermally-matched bonding system, the effect of the peeling stress was not present and the reported interfacial bond strength was about 12 MPa after 200°C of annealing. If this value of bond strength is assumed to be reached in the current bonding of GaAs-to-Si, where the peeling stress is present, the debonding failure would have resulted at a lower annealing temperature of 160°C as the calculated theoretical $\sigma_{p,max}$ value was about 13 MPa at 160°C (refer Figure 5-3). This accounts for why several researchers [26, 28] had claimed that the bonding pairs would not survive 160°C of annealing in the bonding of severe thermally-mismatched GaAs-to-Si. Thus, all the annealings in the present work are limited to a temperature lesser than 140°C.

Figure 5-4: A schematic illustration of the prying effect induced by the peeling stress on a thermally-mismatched GaAs-to-Si bonding pair at an elevated temperature with (a) and (b) showing close-up views at the central and peripheral regions of the bonding interface, respectively.

Microscopic insights into the bonding interface, in association to the peeling stress during annealing, could account for why the bonding system of GaAs-to-Si would generally yield much lower interfacial energy than Si-to-Si. As the peeling stress acts to pry apart a bonding pair of GaAs-to-Si at the wafer edges during annealing, a microscopic bonding interfacial gap opening may already be occurring even at temperatures below the debonding temperature. This is illustrated in Figure 5-4. Consequently, even if the adsorbed H_2O molecules have out-diffused, the oppositely reacting -OH groups of the GaAs-OH and Si-OH species cannot come close enough to be polymerized, which is depicted in Figure 5-4(b). This is true especially at the region that is near the edge of the bonding interface. Although the peeling stress was previously found to be constrained within the small region that is near the peripherals of the bonding GaAs and Si, the region at which the peeling stress-induced

remoteness of the oppositely reacting species is taking place may be extended much more beyond that because of the stiffness of the bonding wafers. This is reflected in Figure 5-4, in which the de-polymerizing zone is spanned across a wider region as compared to the region within which the peeling stress is present. Hence, the polymerization events will only be restricted at the narrow central region of the bonding interface, which is much further away from the edge. This is indicated in Figure 5-4(a), which shows the close proximity of the oppositely reacting hydroxyl groups and a pair is being polymerized to yield a covalent oxygen bridge between the GaAs and Si, accompanied by the out-diffusion of a water molecule.

Most of the annealing processes were carried out by ramping up the temperature within a single step, to an elevated value at which a bonding pair was subsequently held for a certain period. When such a one-step annealing process is performed on a dissimilar thermally-mismatched bonding pair, the peeling stress will escalate at a rate according to the temperature ramp rate, which will be much faster than the polymerization rate. Consequently, the de-polymerizing zone near the edge of the bonding interface (due to the remoteness of the oppositely reacting species) will span across a large area and a low bond energy will result.

A novel technique to suppress the antagonistic peeling stress-induced remoteness of the oppositely polymerizing species effect is to anneal a thermally-mismatched bonding pair in incremental sequential steps. By doing so, the increment in temperature (and hence, the peeling stress) would not be increased too largely at each sequential step. Eventually, the central polymerization zone of the bonding interface will be permitted to span across a larger area and result in a high bond energy. To the author's knowledge, an annealing technique like this has been rarely discussed and performed on severe thermally-mismatched bonding systems such as GaAs-to-Si. The only literature available on the use of the sequential-step annealing process in wafer bonding was authored by Tong and Gösele [19]. In their work,

Tong and Gösele heat-treated a sapphire-to-Si bonding pair by annealing it in incremental sequential steps to a highest temperature step of 150°C. A resultant specific high bond energy of 2500 mJ/m² was reported. However, no working mechanism was provided to account for the bond energy enhancement through the sequential-step annealing process.

Through the current research efforts, a high bond energy comparable to the high bond energy derived from UHV wafer bonding was achieved in the bonding of 2-inch GaAs and Si wafers that were several hundreds of micrometers thick by utilizing the sequential-step annealing technique. A comparison of this technique with the conventional one-step annealing was made and the working mechanism was provided qualitatively. Moreover, the effects on the bond energy brought by the number of steps and the dwelling duration of each step in the sequential-step annealing process were investigated.

5.2 Experimental Details

Four sets of GaAs-to-Si bonding pairs were used to investigate the influences brought by one-step and sequential-step annealing processes. The annealings were performed under either a normal atmospheric condition or a high vacuum condition. The bonding pairs were prepared using the standard bonding procedures as outlined in Section 3.1. The GaAs and Si bonding surfaces were activated using the previously established Ar plasma parameters of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power (refer to Chapter 4). In addition, they were room temperature contacted in a normal ambient condition. Subsequently, they were annealed differently as shown in Table 5-2. First, the bonding pairs of GaAs-to-Si of Set I and II were one-step annealed while those of Set III and IV were sequential-step annealed. Second, the bonding pairs of Set I and III were annealed under a normal atmospheric condition of 760 Torr while those of Set II and IV were annealed under a high vacuum condition of 10⁻⁶ Torr. Lastly, the bonding pairs of each set were annealed to the

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various highest annealing temperatures of 60°C, 100°C, and 140°C. They were abbreviated as A, B, and C, respectively, as indicated in Table 5-2. Annealing temperatures beyond 140°C were not considered since the thermal budget of the GaAs-to-Si bonding pairs was too low to endure the associated substantial thermal stresses.

Table 5-2: The different annealing conditions of the Argon plasma-activated direct wafer bonding of 2-inch GaAs-to-Si.

GaAs-to-Si Bonding Pair				
Highest Annealing Temperature (°C)	One-Step Anneal		Sequential-Step Anneal	
	Set I	Set II	Set III	Set IV
	Normal Atmospheric Condition	High Vacuum Condition	Normal Atmospheric Condition	High Vacuum Condition
60	A-I	A-II	A-III	A-IV
100	B-I	B-II	B-III	B-IV
140	C-I	C-II	C-III	C-IV

Figure 5-5: The one-step annealing profiles for Samples A-I, A-II, B-I, B-II, C-I, and C-II.

In the one-step annealing processes, the GaAs-to-Si bonding pairs were annealed by having the temperature ramped up in a single step at a rate of 1°C/min to one of the considered highest annealing temperatures. At this point, the bonding pairs were subsequently dwelled for a duration of 24 h. This is illustrated in Figure 5-5, which also highlights the bonding pairs of A-I and A-II, B-I and B-II, and C-I and C-II that were annealed at the highest annealing temperatures of 60°C, 100°C, and 140°C, respectively (see Table 5-2).

In the sequential-step annealing processes, the GaAs-to-Si bonding pairs were subjected to a series of identical thermal incremental sequential steps until the last highest annealing temperature steps were reached. Figure 5-6 illustrates the temperature profiles of the sequential-step annealing processes, which also includes the respective groups of the bonding pairs of A-III and A-IV, B-III and B-IV, and C-III and C-IV that were being annealed to the different last highest annealing temperature steps of 60°C, 100°C, and 140°C, respectively (see Table 5-2). At the beginning of the processes, the bonding pairs were dwelled at room temperature in either a normal atmospheric environment or a high vacuum environment for 24 h before the sequential-step annealings commenced. Thereafter, the

bonding pairs were annealed to one of the last highest annealing temperature steps through a series of identical thermal incremental sequential steps. Each sequential step involved a ramping up stage whereby the temperature was increased by 20°C at a rate of 1°C/min. The ramping up stage was followed by a dwelling stage whereby a bonding pair was held for a duration of 24 h.

In both the one-step and sequential-step thermal treatments, the annealings were completed by having the temperature ramped down from the highest annealing temperatures to room temperature at a rate of 1°C/min (see Figure 5-5 and Figure 5-6).

Figure 5-6: The sequential-step annealing profiles for Samples A-III, A-IV, B-III, B-IV, C-III, and C-IV.

5.3 Results and Discussion

The infrared (IR) images of the Ar plasma-activated GaAs-to-Si bonding pairs after the normal ambient room temperature contact and after the different annealing treatments of Table 5-2 are displayed in Figure 5-7 and Figure 5-8, respectively. Infrared images of Sample C-I are not included as its associated thermal treatment of one-step normal ambient annealing at 140°C for 24 h had already been performed previously in the 2³ factorial design study of Ar PADWB of GaAs-to-Si in Chapter 4. Hence, the IR images of Sample C-I after the normal ambient room temperature contact and after the anneal can be referred from the IR images of the replicates of Run 6 in Figure 4-1 and Figure 4-2, respectively. Comparisons between the IR images of the respective bonding pairs in Figure 5-7 and Figure 5-8 reveal that the various thermal treatments of Table 5-2 did not generate much additional interfacial voids after the anneals. The unbonded regions that were being shown up as darker intensity spots in the IR images of Figure 5-7 and Figure 5-8 were due to the occurrence of entrapped particles and air pockets during the normal ambient room temperature contacts of the GaAs and Si bonding pairs, which were performed in a Class 100 cleanroom environment.

(a)

(b)

(c)

(d)

(e)

Figure 5-7: Infrared images of the GaAs-to-Si bonding pairs of Samples (a) A-I, (b) A-II, (c) A-III, (d) A-IV, (e) B-I, (f) B-II, (g) B-III, (h) B-IV, (i) C-II, (j) C-III, and (k) C-IV after room temperature contact under a normal atmospheric condition.

(a)

(b)

(c)

(d)

(e)

Figure 5-8: Infrared images of the post-annealing GaAs-to-Si bonding pairs of Samples (a) A-I, (b) A-II, (c) A-III, (d) A-IV, (e) B-I, (f) B-II, (g) B-III, (h) B-IV, (i) C-II, (j) C-III, and (k) C-IV (see Table 5-2 for the respective heat treatments of the samples).

Infrared images of the razor blade insertions into the respective post-annealing bonded interfaces of Table 5-2 (for Sample C-I, refer to the IR images of the replicates of Run 6 in Figure 4-3) and the corresponding crack lengths are presented in Figure 5-9. The corresponding crack lengths were also included in Table 5-3. Alongside the respective pairs of the bonding GaAs and Si thicknesses, the corresponding post-annealing specific bond energies were determined based on the crack opening method as outlined in Section 3.2.2 using Equation (3-4) and are presented in Table 5-3. The thickness of the razor blade used in the present crack opening work was 109 μm and values of 119 GPa and 130 GPa were taken to be the Young's moduli of GaAs and Si, respectively. The post-annealing specific bond energy value of 424 mJ/m^2 of Sample C-I in Table 5-3 was taken from the Run Average result of Run 6 in Table 4-4.

(a)

(b)

(c)

(d)

(e)

Figure 5-9: Infrared images of the blade insertions into the post-annealing GaAs-to-Si bonded interfaces of Samples (a) A-I, (b) A-II, (c) A-III, (d) A-IV, (e) B-I, (f) B-II, (g) B-III, (h) B-IV, (i) C-II, (j) C-III, and (k) C-IV (see Table 5-2 for the respective heat treatments of the samples). The corresponding crack lengths are shown as inserts.

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Table 5-3: The post-annealing specific bond energies of the differently annealed GaAs-to-Si bonded samples (see Table 5-2).

Sample	Crack Length, l (mm)	GaAs Thickness, t_{GaAs} (μm)	Si Thickness, t_{Si} (μm)	Post-Annealing Specific Bond Energy, γ (mJ/m^2)
A-I	11.38	469	280	308
A-II	11.44	467	284	311
A-III	10.72	465	278	382
A-IV	10.79	467	285	396
B-I	9.56	467	282	627
B-II	9.72	468	285	602
B-III	9.38	468	283	683
B-IV	9.17	467	283	747
C-I ^a	-	-	-	424
C-II	10.11	468	274	468
C-III	8.56	469	283	986
C-IV	8.15	469	285	1220

^a The associated heat treatment of Sample C-I had already been performed previously in the 2^3 factorial design study of Ar PADWB of GaAs-to-Si in Chapter 4. Therefore, the associated post-annealing specific bond energy value was taken from the Run Average result of Run 6 in Table 4-4.

Figure 5-10: The IR image of the blade insertion into the GaAs-to-Si reference pair.

The specific bond energy of a GaAs-to-Si bonding pair that was Ar plasma-activated with the same Ar plasma parameters of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power (refer to Chapter 4) and contacted together at room temperature under a normal atmospheric condition without any further heat treatment was taken as the reference. The GaAs and Si thicknesses were 469 μm and 279 μm , respectively. Figure 5-10 displays the IR image of the blade insertion into the reference GaAs-to-Si bonding pair. The corresponding crack length was 12.20 mm. The reference specific bond energy was then determined to be 231 mJ/m^2 .

The post-annealing specific bond energy results of Table 5-3 of Ar plasma-activated GaAs-to-Si bonding pairs that were heat treated differently according to Table 5-2 are shown graphically in Figure 5-11 alongside the reference specific bond energy. A best-fit curve was drawn through each series of the bond energy data. The bonded pair that was sequential-step annealed to a highest temperature step of 140°C in a high vacuum yielded the highest specific bond energy of 1220 mJ/m^2 .

Figure 5-11: The post-annealing specific bond energies of the Ar plasma-activated GaAs-to-Si bonded pairs that were subjected to the Table 5-2 annealing conditions.

Figure 5-11 reveals three major observations as follows:

- 1) The bond energy profiles associated with the sequential-step annealing process were higher than those derived from the one-step annealing process.
- 2) All of the bond energy profiles escalated with increasing highest annealing temperature up to 100°C. Thereafter, only the two bond energy profiles of the sequential-step annealing continued to increase exponentially whereas the profiles pertaining to the one-step annealing saw a slight decrement at 140°C.
- 3) The post-annealing specific bond energies of the GaAs-to-Si bonded pair were higher when the sequential-step annealing was carried out in a high vacuum as

compared to when it was carried out in a normal ambient condition. However, the bond energy profiles of the one-step annealing carried out under a normal atmospheric and high vacuum condition did not differ significantly.

These three observations indicate that the sequential-step annealing technique will generally lead to an enhancement in the Ar PADWB of GaAs-to-Si bond energy.

5.3.1 Effect of the one-step annealing on the bonding of severe thermally-mismatched GaAs-to-Si

Figure 5-11 shows that the bond energies associated with the one-step annealing of the Ar PADWB of GaAs-to-Si did not increase continually with increasing maximum annealing temperature up to 140°C. Instead, the highest specific bond energies of the one-step annealing carried out under the normal atmospheric and high vacuum conditions were derived from a highest annealing temperature of 100°C. Such an observation has been rarely reported. Most wafer bonding literature (especially those involving homogenous Si-to-Si bonding systems) reported that the bond energy will generally increase with increasing temperature [2, 3]. To account for the one-step annealing of GaAs-to-Si bond energy behavior, the bonding mechanisms of hydrogen bonding and polymerization in relation to the annealing temperature are being analyzed critically.

From a physical bonding perspective, the main bonding force of a pair of plasma-activated GaAs and Si wafers after a normal ambient room temperature contact is derived from the hydrogen bonding among the large amount of prior plasma activation-induced surface saturated -OH groups and adsorbed H₂O molecules. As the contacted pair is subsequently subjected to an annealing, the H₂O molecules will gain the energy required to rearrange themselves and evolve into a more intimate structure of closer interactions up to 100°C [19]. Hence, the bond energy will increase correspondingly with increasing

temperature from 20°C (room temperature) to 100°C. This is schematically shown in Figure 5-12(a) and Figure 5-12(b), respectively. In Figure 5-12, the intermediate blue regions indicate the hydrogen bonding among the H₂O molecules and the -OH groups. Moreover, the intensity of the blue regions reflects the extent of the hydrogen bonding effect as the annealing temperature is increased. As an example, the intensity of the blue region at an annealing temperature of 100°C in Figure 5-12(b) is much darker than that at 20°C in Figure 5-12(a) because the bonding interfacial H₂O structure is more stable at 100°C, consisting mainly of cyclic structures of H₂O molecules of high hydrogen bonding energy [19, 20]. However, when the annealing temperature is increased beyond 100°C, the hydrogen bonding effect will begin to decrease as the H₂O molecules will start to diffuse out from the bonding interface and the interactions will weaken. This is reflected through the lighter intensity of the blue region in Figure 5-12(c) at a temperature of 140°C. As a result, the bond energy that is derived from the hydrogen mechanism will see a downturn at annealing temperatures in excess of 100°C.

Figure 5-12: A schematic illustration on the extents of hydrogen bonding and polymerization effects of thermally-mismatched GaAs-to-Si pairs contacted at (a) room temperature (20°C) and one-step annealed at (b) 100°C and (c) 140°C.

From a chemical bonding perspective, the extent of polymerization reaction (see Equation [4-1]) between the oppositely -OH reacting groups of GaAs-OH and Si-OH species will be low especially at the very low temperature of 20°C (room temperature) because of the presence of the interfacial H₂O molecules in-between the oppositely -OH polymerizing groups. Consequently, the -OH groups cannot come close enough to be polymerized. This is reflected through the large number of the discontinued interfacial yellow and purple lines across the whole bonding interface in Figure 5-12(a), which represent the unreacted -OH groups of the bonding surface GaAs-OH and Si-OH species, respectively.

On the other extreme, even when the annealing temperature is increased to 140°C at which the out-diffusion of H₂O molecules is significant, the extent of polymerization at the bonding interface may not necessary be high. In the case of the one-step annealing, the temperature is ramped up within a single step to a value at which it is subsequently dwelled for a certain period. If the one-step annealing temperature increment is high, such as from 20°C to 140°C, the peeling stress of the severe thermally-mismatched GaAs-to-Si bonding pair will escalate to a large value associated with the large temperature increment by 120°C at a rate corresponding to the temperature ramping up rate.

First, even if the ramping up of the temperature was carried out at a very low rate of 1°C/min, the peeling stress growth rate would still be much higher than the polymerization rate. As a result, insignificant polymerization events will occur during the one-step temperature ramping up stage to restrain the growing peeling stress.

Second, it was theoretically determined in Figure 5-3 that the maximum peeling stress associated with an annealing temperature of 140°C (from a room temperature of 20°C) of a severe thermally-mismatched GaAs-to-Si bonding system was about 10 MPa. Such a high peeling stress at the dwelling stage of 140°C will attempt to pry the bonding GaAs and Si pair apart at the wafer edges, inducing a microscopic gap opening at the peripheral region of the

bonding interface. Consequently, even as a large amount of excess interfacial H_2O molecules have out-diffused at 140°C , the oppositely $-\text{OH}$ groups are still unable to polymerize as they are too far apart. This is pictorially illustrated in Figure 5-12(c), in which the large number of the discontinued interfacial purple and yellow lines at the peripheral regions of the GaAs-to-Si bonding interface reflects the peeling stress-induced separation of the oppositely polymerizing species effect. In addition, the intensity of the blue region is lighter to indicate the weakening of the hydrogen bonding effect as the interfacial H_2O molecules start to diffuse away from the bonding interface at 140°C . Any polymerization events in the one-step annealing at 140°C will be confined within the narrow central region of the bonding interface where the peeling stress-induced microscopic interfacial gap opening effect is insignificant. This is reflected in Figure 5-12(c) where the red lines at the narrow central region of the bonding interface indicate the successful polymerization reactions. From these, products of the oxygen bridge between the GaAs and Si (GaAs-O-Si) are evolved.

At an intermediate annealing temperature of 100°C , the peeling stress is not as forceful as the one at 140°C . Consequently, the induced microscopic interfacial gap opening effect that separates the oppositely $-\text{OH}$ polymerizing groups is not as significant. This will permit the central polymerization region of the bonding interface to span across a wider area. At 140°C , the density of the evolved GaAs-O-Si at the central region of the bonding interface would be higher as compared to the density at 100°C due to a higher thermal effect. However, when comparing on an absolute basis, the total number of the GaAs-O-Si evolved at 100°C could be higher than that at 140°C due to a larger central polymerization spanned region associated with the former. This is illustrated in Figure 5-12(b) and Figure 5-12(c). Although the density of the evolved GaAs-O-Si (as indicated by the red lines) within the central region of the bonding interface is much higher at 140°C in Figure 5-12(c), as compared to the one at

100°C in Figure 5-12(b), the absolute amount of the GaAs-O-Si will be lesser in the former situation due to a much narrower constricted central polymerization zone.

The conjectures account for why the peak bond energies in Figure 5-11 of the one-step annealing of the Ar PADWB of the severe thermally-mismatch GaAs-to-Si bonding pairs under the normal atmospheric and high vacuum conditions were associated with the 100°C of highest annealing temperature. The post-annealing specific bond energies of the GaAs-to-Si bonding pairs was not able to sustain their increments beyond the 100°C of annealing temperature because of the abominable pronounced peeling stress effect and the weakening of the hydrogen bonding effect as the H₂O molecules were diffusing out from the bonding interface.

Even when the one-step annealing was performed under a high vacuum condition, the bond energy was not enhanced as evidenced in Figure 5-11. When an annealing is performed under a high vacuum condition, the high vacuum acts as a powerful drag force to extract the interfacial excess H₂O molecules out from the bonding interface so that oppositely -OH groups can be close enough to be polymerized [24, 25]. However, in the present situation of bonding severe thermally-mismatched of GaAs-to-Si, the existence of the abhorrent significant peeling stress physically separates the oppositely -OH polymerizing groups during annealing in the first place. Hence, even when the occurrence of the out-diffusion of H₂O molecules is extensive in a high vacuum environment, the oppositely reacting groups will still be too far away to be polymerized. This explains why the bond energy profile in Figure 5-11 of the one-step annealing process carried out under a high vacuum condition was similar to and not higher than the bond energy profile of the same process performed in a normal ambient environment.

5.3.2 Effect of the sequential-step annealing on the bonding of severe thermally-mismatched GaAs-to-Si

Figure 5-11 reveals that the post-annealing specific bond energies of the Ar PADWB of the GaAs-to-Si pairs that were subjected to the sequential-step annealing process were higher than those that were one-step annealed. Moreover, the bond energy profiles that were derived from the sequential-step annealing had shown to be able to sustain their exponential increments up to 140°C. In contrast, the bond energy profiles that were associated with the one-step annealing saw a slight dip in the bond energies at 140°C. These findings imply that a higher bond energy, deriving from a larger number of evolved interfacial GaAs-O-Si covalent bonds as a result of a more extensive polymerization, can only be realized when the annealing is carried out in incremental sequential steps.

As opposed to the conventional one-step annealing, a GaAs-to-Si bonding pair is annealed in several thermal incremental sequential steps in a sequential-step annealing process. Figure 5-6 demonstrates examples of the present sequential-step annealing temperature profiles in which all the thermal incremental sequential steps are identical. Moreover, the temperature increment by 20°C during the ramping up stage of each identical sequential step is small. Correspondingly, the strength of the peeling stress per step will also be insubstantial. As a result, the oppositely -OH groups that are within regions that are neighboring to the central region (from which GaAs-O-Si bonds evolved previously during preceding annealings at lower temperature sequential steps) will still be in close adjacency to be polymerized. Towards the end of the annealing during the dwelling stage of a sequential step, the central polymerized zone will be inched out further and the bond energy will increase correspondingly. Alongside the wafers stiffness, the growing peeling stress that corresponds to the temperature increment of the next sequential step will be opposed and the induced microscopic gap opening at the peripheral region will be reduced.

Figure 5-13: A bonding pair of GaAs-to-Si that is sequentially annealed in identical increasing steps from a room temperature of 20°C to a last annealing step of 140°C.

Figure 5-13 provides a schematic illustration of the bonding mechanism of a bonding pair of GaAs-to-Si that is sequentially annealed in increasing identical steps from a room temperature of 20°C to a last annealing step of 140°C. It is assumed that at each sequential step, the temperature increment of 20°C is sufficiently small with a low ramp rate of 1°C/min and the dwelling duration of 24 h is sufficiently long. Hence, the bonding mechanism associated with the sequential-step annealing can be envisaged to be that of a lateral outwards sequential proliferation of the evolved GaAs-O-Si covalent bridges from the central region of the bonding interface. The small peeling stress growth during the ramping up stage and the

sufficiently long duration during the dwelling stage of each identical thermal incremental step develop the bond energy and mitigate the dire effect of the peeling stress-induced separation of the oppositely polymerizing species. A comparison of Figure 5-12(c) with Figure 5-13 shows that the extent of the microscopic gap opening that leads to the -OH polymerizing species remoteness at the peripheral regions of the bonding interface is greatly reduced throughout the process of the sequential-step annealing, up to a highest annealing temperature of 140°C. Moreover, the polymerized GaAs-O-Si bonds are able to span across the bonding interface to a larger extent towards the end of the sequential-step annealing process in Figure 5-13.

The explanation reveals why both of the sequential-step annealing bond energy profiles in Figure 5-11 that were associated with the normal atmospheric and high vacuum conditions were able to sustain the bond energy increments up to 140°C. Moreover, unlike the conventional one-step annealing, the energy profile of the sequential-step annealing carried out under a high vacuum condition was distinctively higher than that carried out in a normal ambient condition. Since the peeling stress-induced microscopic interfacial gap opening effect was mitigated significantly by the sequential-step annealing, the oppositely -OH reacting groups were not separated to a great extent. Hence, the presence of the high vacuum then took the enhancement effect in promoting the polymerization reactions among the close adjacency -OH groups further by extracting more interfacial H₂O molecules from the bonding interface.

The post-annealing specific bond energy, γ , data in Table 5-3 of the Ar PADWB of the GaAs-to-Si bonded pairs that were sequentially step annealed to various highest annealing temperatures, T , under a normal atmospheric and high vacuum condition were re-plotted separately in Figure 5-14 and Figure 5-15, respectively. The colored solid lines in the figures are best-fit curves drawn through the series of bond energy data and the errors in the bond energy data are shown in red. The figures also show the corresponding best-fit exponential curves, which are indicated by the black dotted lines.

Figure 5-14: The exponential fitting of the post-annealing specific bond energy profile of the sequential-step annealing of Ar PADWB of GaAs-to-Si under a normal atmospheric (760 Torr) condition as a function of the highest annealing temperature. The bond energy data is adapted from Table 5-3.

Figure 5-15: The exponential fitting of the post-annealing specific bond energy profile of the sequential-step annealing of Ar PADWB of GaAs-to-Si under a high vacuum (10^{-6} Torr) condition as a function of the highest annealing temperature. The bond energy data is adapted from Table 5-3.

The expression of the exponential fitting curve that corresponds to the sequential-step annealing under a normal atmospheric condition in Figure 5-14 was

$$\gamma = -365 + 508e^{0.007T}. \quad (5-8)$$

The expression of the exponential fitting curve that corresponds to the sequential-step annealing under a normal atmospheric condition in Figure 5-15 was

$$\gamma = -118 + 267e^{0.01T}. \quad (5-9)$$

The expressions are valid only for a pair of GaAs and Si wafers that are being bonded through the following processes in sequence:

- 1) Ar plasma activation of the GaAs and Si wafers using a developed set of conditions of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power.
- 2) Room temperature (20°C) contact of the GaAs and Si wafers together under a normal atmospheric condition (760 Torr).
- 3) Sequential-step annealing of the GaAs-to-Si bonding pair from 20°C to a highest annealing temperature, T , through a number of identical incremental sequential steps. Each sequential step involves:
 - a. A ramping up stage during which the temperature is increased by 20°C at a rate of 1°C/min.
 - b. A dwelling stage during which the bonding pair is dwelled for a duration of 24 h.
- 4) Ramping down the temperature from the highest annealing temperature, T , to a room temperature of 20°C at a rate of 1°C/min.

Hence, the empirical expressions of Equation (5-8) and Equation (5-9) are only valid for T more than 20°C, which is the temperature at which a pair of GaAs and Si bonding wafers is contacted together and annealed from. The exponential dependency of the specific bond energy, γ , on the highest annealing temperature, T , in the empirical expressions of Equation (5-8) and Equation (5-9) is in agreement with Gösele and Tong's [19] homogenous Si-to-Si bonding model, which reflects the thermally activated nature of the polymerization process. This implies that if an extensive polymerization (that will lead to a high bond energy) is to be achieved in a severe thermally-mismatched bonding pair, such as GaAs-to-Si, the annealing

has to be performed in sufficiently small incremental sequential steps instead of in the conventional one-step annealing process.

5.3.3 Insights into the sequential-step annealing process

It has been justified that the loathsome peeling stress effect of preventing extensive polymerization (that will otherwise lead to a high bond energy) in a severe thermally-mismatched bonding pair of GaAs-to-Si can be mollified through the sequential-step annealing technique. In Figure 5-11, the highest post-annealing specific bond energy of 1220 mJ/m² of GaAs-to-Si was achieved by annealing the bonding pair under a high vacuum condition from a room temperature of 20°C to a highest annealing temperature of 140°C in 6 incremental sequential steps (see the annealing profile of Sample C-IV in Figure 5-6). All of the sequential steps were identical and each step involved a ramping up stage and a dwelling stage. During the ramping up stage, the temperature was increased by 20°C at a rate of 1°C/min while, during the dwelling stage, the bonding pair was held at the reached temperature for a duration of 24. In this section, insights into the sequential-step annealing were gained by considering the effects of the number of identical thermal incremental sequential steps in such a process and the duration of the dwelling stage in each step.

All of the 2-inch bonding pairs of GaAs and Si were first Ar plasma-activated using the developed conditions set of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power. Subsequently, they were room temperature (20°C) contacted together under a normal atmospheric condition. Lastly, all of the pairs were sequential-step annealed under a high vacuum condition from a room temperature of 20°C to a common highest annealing temperature step of 140°C. In each sequential-step annealing, the profiles of the steps were identical throughout the process. However, the step profiles were different among the number of sequential-step annealings performed. Towards the end of all the sequential-step

annealings, the temperatures were ramped down from the common highest annealing temperature step of 140°C to a room temperature of 20°C. All temperature incremental and decremental rates were fixed at 1°C/min.

To conduct the first investigation systematically, the total number of steps in a sequential-step annealing process was considered (instead of the temperature increment during the ramping up stage of each step) so that the temperature can be increased from 20°C to 140°C through a series of identical incremental sequential steps. Since the lower and upper temperature limits of all the sequential-step annealings of GaAs-to-Si bonding pairs were established at 20°C and 140°C, respectively, the absolute temperature increment throughout each annealing process will be 120°C. Hence, the temperature increment during the ramping up stage in each identical sequential step will be inversely proportional to the number of such steps in an annealing process. Identical thermal incremental sequential steps numbering from 1-6 were considered corresponding to the temperature increments of 120°C, 60°C, 40°C, 30°C, 24°C, and 20°C, respectively, during the ramping up stage in each step (see shown in Table 5-4). In this set of experiments, the holding durations during the dwelling stages in all of the sequential steps were set at 24 h.

In a separate set of experiments, the effects brought by the holding duration during the dwelling stage in each identical sequential step were investigated. Four different dwelling durations of 6 h, 12 h, 18 h, and 24 h were considered. In this set of experiments, the temperature increments during the ramping up stages in all the sequential steps were set at 20°C.

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Table 5-4: The numbers of identical incremental sequential steps and the corresponding temperature increment per step.

Number of Identical Incremental Sequential Steps	Temperature Increment Per Step ^a (°C)
1	120
2	60
3	40
4	30
5	24
6	20

^a The values were determined by taking the absolute temperature increment of 120°C, which is common in all the sequential-step annealing experimental runs, divided by the number of identical incremental sequential steps.

The effects of the number of identical thermal incremental steps in a sequential-step annealing process

Figure 5-16: The post-annealing specific bond energies of the Ar PADWB of GaAs-to-Si bonding pairs that were sequential-step annealed from 20°C to 140°C under a high vacuum condition using different numbers of identical thermal incremental sequential steps.

The post-annealing specific bond energies of the Ar PADWB of GaAs-to-Si bonding pairs that were sequential-step annealed with different numbers of identical incremental thermal sequential steps from 20°C to 140°C under a high vacuum condition are plotted in Figure 5-16. The colored solid line in the figure is a best-fit curve drawn through the series of bond energy data and the errors in the bond energy data are shown in red. The durations of the dwelling stages in all of the steps were standardized to be 24 h. The corresponding

temperature increments during the ramping up stages in the sequential steps are shown along the non-linear top x-axis. The specific bond energy data of 1220 mJ/m^2 for the 6 identical thermal incremental sequential steps was determined previously (see the post-annealing specific bond energy result of Sample C-IV in Table 5-3). It can be observed from the figure that the bond energy decreases initially when the number of steps increases from 1 to 3. Subsequently, there appears to be a recovery mechanism whereby the bond energy increases as the number of steps increases from 3 to 6.

Consider the sequential-step annealing process of a GaAs-to-Si bonding pair from 20°C to 140°C . When the number of identical thermal incremental sequential steps is low, it will correspond to a high temperature increment in each step. As mentioned in the discussion in Section 5.3.1, when the temperature increment per step is high, the peeling stress-induced microscopic interfacial gap opening effect occurring at the peripheral region of the thermally-mismatched GaAs-to-Si bonding interface will be pronounced. In addition, the oppositely -OH groups of the GaAs-OH and Si-OH species will not come close enough to each other to be polymerized during the annealing (similar to the illustration of Figure 5-12[c]). Consequently, the extent of the polymerization will be suppressed and a low bond energy will result. Given such a situation, the hydrogen bonding among the interfacial H_2O molecules and -OH groups is largely responsible for holding the GaAs and Si pair together. Unfortunately, because the peripheral region of the bonding interface is more opened (due to the peeling stress) and as the annealing duration is prolonged, the H_2O molecules will diffuse away from the bonding interface and the hydrogen bonding effect will weaken.

In this study, the bonding pairs of GaAs-to-Si were sequential-step annealed from 20°C to 140°C using 1, 2, and 3 identical thermal incremental sequential steps. The total annealing durations corresponded to 24 h (1 day), 48 h (2 days), and 72 h (3 days), respectively (neglecting the durations during which the temperatures were ramped up in the

sequential steps). Considering the 3 identical incremental sequential steps, the remaining amount of H_2O interfacial molecules will be very low after 72 h (the total annealing duration). Consequently, the resultant bond energy that was mainly derived from the weak hydrogen bonding will be very low. Contrary, in the case of the single incremental step that corresponded to only 24 h of annealing duration, the high hydrogen bonding associated with the high amount of remaining H_2O interfacial molecules will result in a high bond energy. These explain why the post-annealing specific bond energy of GaAs-to-Si was found to be decreased in Figure 5-16 when the number of identical incremental sequential steps was increased from 1 to 3.

The very opposite can be implied when the sequential-step annealing of a bonding pair of thermally-mismatched GaAs-to-Si is performed using a higher number of identical thermal incremental sequential steps from 20°C to 140°C . Correspondingly, the temperature increment in each step will be low and the resultant peeling stress will be less significant. With reference to the discussion in Section 5.3.2, the oppositely -OH groups can then come close enough to be polymerized in a sequential fashion as illustrated in Figure 5-13, which will lead to a high bond energy. In this situation, the out-diffusion of the excess H_2O molecules away from the bonding interface is desired as it necessitates the close proximity of the -OH molecules, which will lead to an extensive polymerization.

This accounts for the post-annealing specific bond energy incremental behavior in Figure 5-16 as the number of identical thermal incremental sequential steps was increased from 3 to 6. When the number was increased from 3 to 6, the developed peeling stress in each identical sequential step will be lowered. Moreover, the total annealing duration will also be longer, leading to a larger extent of excess interfacial H_2O molecules out-diffusion. Consequently, the extent of polymerization will be greater that will lead to an increment in bond energy.

Figure 5-17: The exponential fitting of the post-annealing specific bond energy profile of the sequential-step annealing of Ar PADWB of GaAs-to-Si from 20°C to 140°C under a high vacuum condition using 3 to 6 identical thermal incremental sequential steps.

Figure 5-17 shows the post-annealing specific bond energy profile for 3 to 6 identical thermal incremental sequential steps. The data were adapted from Figure 5-16. The corresponding temperature increments during the ramping stages in the sequential steps are indicated along the non-linear top x-axis. The colored solid line in Figure 5-17 is a best-fit curve drawn through the series of bond energy data and the errors in the bond energy data are shown in red. The expression of the best-fit exponential curve that is indicated by the black dotted line in Figure 5-17 was found to be

$$\gamma = 1548 - 4123e^{-0.42n}, \quad (5-10)$$

where γ denotes the post-annealing specific bonding energy (in mJ/m^2) and n denotes the number of identical thermal incremental sequential steps. The expression is valid only for a pair of GaAs and Si wafers that are being bonded through the following processes in sequence:

- 1) Ar plasma activation of the GaAs and Si wafers using a developed set of conditions of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power.
- 2) Room temperature (20°C) contact of the GaAs and Si wafers together under a normal atmospheric condition (760 Torr).
- 3) Sequential-step annealing of the GaAs-to-Si bonding pair from 20°C to 140°C under a high vacuum (10^{-6} Torr) condition using n number of identical incremental sequential step. Each sequential step involves:
 - a. A ramping up stage during which the temperature is increased by $\frac{120^\circ}{n}$ at a rate of 1°C/min .
 - b. A dwelling stage during which the bonding pair is dwelled for a duration of 24 h.
- 4) Ramping down the temperature from 140°C to room temperature (20°C) at a rate of 1°C/min .

The n -value has to be more than or equal to 3, which corresponds to the minimum number of identical thermal incremental sequential steps between 20°C to 140°C before the polymerization bonding mechanism can take place.

The effect of the holding duration during the dwelling stage of each identical sequential step of a sequential-step annealing process

Figure 5-18: The exponential fitting of the post-annealing specific bond energy profile of the sequential-step annealing of Ar PADWB of GaAs-to-Si from 20°C to 140°C, under a high vacuum condition, for dwelling durations between 6 h to 24 h per identical sequential step.

The post-annealing specific bond energies of the Ar PADWB of GaAs-to-Si bonding pairs that were sequential-step annealed with different dwelling durations per identical sequential step are plotted in Figure 5-18 alongside the best-fit exponential curve that is indicated by the black dotted line. The colored solid line in the figure is a best-fit curve drawn through the series of bond energy data and the errors in the bond energy data are shown in red. All of the bonding pairs were sequential-step annealed under a vacuum condition from 20°C to 140°C using 6 identical thermal incremental sequential steps. Each step involved a

temperature increment of 20°C. The specific bond energy data of 1220 mJ/m² for the 24 h of dwelling duration per identical sequential step was determined previously (see the specific bond energy result of Sample C-IV in Table 5-3). The post-annealing specific bond energy profile in Figure 5-18 is similar to the profile in Figure 5-17, which shows that the specific bond energy incremental rate is decreasing with increasing dwelling duration per identical sequential step. This suggests that the dwelling duration per identical sequential step affects the bond energy by affecting the polymerization kinetically.

Figure 5-19: A schematic illustration of the increment in the amount of interfacial GaAs-O-Si covalent bonds enabled by increasing the duration of the dwelling stage of a certain identical sequential step.

Consider a GaAs-to-Si bonding pair that is being sequential-step annealed with 6 identical incremental steps from 20°C to 140°C. The corresponding temperature increment at each step and the resulting peeling stress will be small. Hence, the polymerization process will be able to proceed across the bonding interface in a sequential manner. During the annealing at the dwelling stage of a sequential step at a certain temperature, the polymerization progresses within a localized region that is adjacent to the central region that had already been polymerized during the annealings at sequential steps of lower temperatures. This scenario was discussed in Section 5.3.2 and indicated in Figure 5-19. As the dwelling duration at the step increases, the extent of the localized polymerization will also increase accordingly as more interfacial H₂O molecules will diffuse away from the bonding interface and result in more oppositely -OH reacting groups to be in close adjacency. Hence, the amount of the localized GaAs-O-Si evolved will be increased at the end of the annealing step. This is illustrated in Figure 5-19. Eventually, a larger amount of GaAs-O-Si will evolve across the whole bonded interface at the end of the sequential-step annealing, which will result in an increment of the specific bond energy. This accounts for the bond energy behavior in Figure 5-18, which increases with increasing dwelling duration per identical sequential step.

The expression of the exponential fitting curve in Figure 5-18 was found to be

$$\gamma = 1492 - 1096e^{-0.06t}, \quad (5-11)$$

where γ denotes the post-annealing specific bonding energy (in mJ/m²) and t denotes the dwelling duration per identical sequential step (in h).

The expression is valid only for a pair of GaAs and Si wafers that are being bonded through the following processes in sequence:

- 1) Ar plasma activation of the GaAs and Si wafers using a developed set of conditions of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power.
- 2) Room temperature (20°C) contact of the GaAs and Si wafers together under a normal atmospheric condition (760 Torr).
- 3) Sequential-step annealing of the GaAs-to-Si bonding pair from 20°C to 140°C under a high vacuum (10^{-6} Torr) condition using 6 identical incremental sequential step. Each step involves:
 - a. A ramping up stage during which the temperature is increased by 20°C at a rate of 1°C/min.
 - b. A dwelling stage during which the bonding pair is dwelled for a duration of $t > 0$ h.
- 4) Ramping down the temperature from 140°C to room temperature (20°C) at a rate of 1°C/min.

Considering the empirical expressions of Equation (5-10) and Equation (5-11), the negative exponential functions in the equations suggest that the number of identical thermal incremental sequential steps, n , and the dwelling duration per step, t , affect the specific bond energy by affecting the polymerization reaction kinetically.

The coefficient of the n -term in the exponential function of Equation (5-10) is 0.42, which is much larger than the coefficient of the t -term in the exponential function of Equation (5-11) by a factor of 7. This comparison indicates that the number of identical thermal incremental sequential steps has a larger kinetic influence over the polymerization reaction that will directly affect the specific bond energy. This finding is justifiable since the number

of identical thermal incremental sequential steps will affect the temperature increment per sequential step, which will determine the strength of the peeling stress. The ease of the localized polymerization at each sequential step must be preceded first by having peeling stress that is weak enough to allow the localized oppositely -OH groups to come close enough to be potentially polymerized. Subsequently, the extent of the polymerization process to evolve GaAs-O-Si interfacial covalent bridges will then be determined by the dwelling duration, which will determine the extent of the excess interfacial H₂O molecules out-diffusion process away from the bonding interface. In other words, if the peeling stress at each step is very small, the localized polymerization will be made easy so that the dwelling duration does not need to be long.

The negative exponential functions in Equation (5-10) and Equation (5-11) also indicate that the specific bond energy, γ , of a bonding pair of GaAs-to-Si will not increase indefinitely with increasing n or t . Instead, the γ -incremental rate will decrease with an increasing n or t and it will reach a saturated value eventually. This is a characteristic of a kinetic-driven process. The saturated specific bond energy is limited by two factors [19]:

- 1) The starting amount of the oppositely -OH polymerizing groups that are being determined by the plasma activation process.
- 2) The roughness of the bonding GaAs and Si surfaces.

In Chapter 4, the Ar plasma activation process was developed through the 2³ factorial design statistical approach so as to strike a balance between having a large amount of -OH polymerizing groups on GaAs and Si bonding surfaces and achieving low GaAs and Si surface roughness. Assuming that all the oppositely -OH groups can be polymerized through the sequential-step annealing of a GaAs-to-Si bonded pair with an infinite n -number of identical thermal incremental sequential steps, or an infinite t h of dwelling duration per identical sequential step, Equation (5-10) and Equation (5-11) suggest that the resultant

specific bond energies would be 1548 mJ/m^2 and 1492 mJ/m^2 , respectively. The values are quite close, which should be the case as the values indicate the saturated specific bond energy that is derived from a fully polymerized bonded interface. Furthermore, if the actual saturated specific bond energy is taken to be the average of 1548 mJ/m^2 and 1492 mJ/m^2 , which turns out to be 1520 mJ/m^2 , it is not far from the current highest achieved 1220 mJ/m^2 of specific bond energy.

5.4 Conclusions

Conventional heat treatment that involves having an Ar PADWB of GaAs-to-Si pair annealed by ramping up the temperature within a single step to a large value at which the bonding pair is dwelled for a duration of time has been found to be a barren effort in achieving high bond energy. Presently, a very low specific bond energy of 468 mJ/m^2 was derived from an Ar PADWB of GaAs-to-Si pair that was one-step annealed from 20°C to 140°C under a high vacuum (10^{-6} Torr) condition. The peeling stress, which is a thermal-mismatch stress inherent in the GaAs-to-Si bonding system, prevented extensive polymerization (that will lead to a high bond energy) when the conventional one-step annealing was performed.

Presently, a simplistic novel heat treatment technique was implemented to assuage the negative effect of the peeling stress by having an Ar PADWB of GaAs-to-Si pair annealed in a series of increasing sequential steps. The highest specific bond energy of 1220 mJ/m^2 was achieved in an Ar PADWB of GaAs-to-Si pair when it was sequential-step annealed from 20°C to 140°C under a high vacuum (10^{-6} Torr) condition using 6 identical thermal incremental sequential steps. Each step involved a ramping up stage whereby the temperature was increased by 20°C at a rate of 1°C/min . This initial stage was followed by a dwelling stage during which the bonding pair was held for a duration of 24 h. The high specific bond energy of 1220 mJ/m^2 was found to be approaching the empirically determined saturated specific bond energy of 1520 mJ/m^2 .

In Chapter 6, the integrity of the bond derived from the sequential-step annealing process will be justified through a number of characterizations. Furthermore, the sequential-step annealed Ar PADWB of GaAs-to-Si pair will be subjected to chemical and mechanical processes that will prove its viability in device fabrication.

References

- [1] O. Moutanabbir and U. Gosele, "Heterogeneous Integration of Compound Semiconductors," *Annual Review of Materials Research*, vol. 40, pp. 469-500, 2010.
- [2] C. Harendt, H.-G. Graf, B. Hofflinger, and E. Penteker, "Silicon fusion bonding and its characterization," *Journal of Micromechanics and Microengineering*, vol. 2, iss. 3, pp. 113-6, 1992.
- [3] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation," *Proceedings of the IEEE*, vol. 86, iss. 8, pp. 1575-85, 1998.
- [4] Q. Y. Tong and U. Gösele, "Semiconductor wafer bonding: recent developments," *Materials Chemistry and Physics*, vol. 37, iss. 2, pp. 101-27, 1994.
- [5] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [6] H. Moriceau, F. Rieutord, F. Fournel, L. Di Cioccio, C. Moulet, L. Libralesso, P. Gueguen, R. Taibi, and C. Deguet, "Low temperature direct bonding: An attractive technique for heterostructures build-up," *Microelectronics Reliability*, vol. 52, iss. 2, pp. 331-41, 2012.
- [7] U. Gosele, M. Alexe, P. Kopperschmidt, and Q. Y. Tong, "Semiconductor wafer bonding. A flexible approach to materials combinations in microelectronics; micromechanics and optoelectronics," *1997 International Semiconductor Conference 20th Edition. CAS '97 Proceedings*, vol. 1, pp. 23-32, Oct. 7 - Oct. 11, 1997, New York, USA.
- [8] P. Ramm, J. J.-Q. Lu, and M. M. V. Taklo, *Handbook of wafer bonding / edited by Peter Ramm, James Jian-Qiang Lu, and Maaikie M. V. Taklo*: Weinheim : Wiley-VCH, 2012.
- [9] T. Akatsu, A. Plos, H. Stenzel, and U. Gosele, "GaAs wafer bonding by atomic hydrogen surface cleaning," *Journal of Applied Physics*, vol. 86, iss. 12, pp. 7146-50, 1999.
- [10] T. Akatsu, A. Plossl, R. Scholz, H. Stenzel, and U. Gosele, "Wafer bonding of different III-V compound semiconductors by atomic hydrogen surface cleaning," *Journal of Applied Physics*, vol. 90, iss. 8, pp. 3856-62, 2001.
- [11] T. R. Chung, L. Yang, N. Hosoda, and T. Suga, "Room temperature GaAs Si and InP/Si wafer direct bonding by the surface activated bonding method," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 121, iss. 1-4, pp. 203-6, 1997.
- [12] U. Gosele, H. Stenzel, T. Martini, J. Steinkirchner, D. Conrad, and K. Scheerschmidt, "Self-propagating room-temperature silicon wafer bonding in ultrahigh vacuum," *Applied Physics Letters*, vol. 67, iss. 24, pp. 3614-6, 1995.
- [13] G. Kastner, T. Akatsu, S. Senz, A. Plochl, and U. Gosele, "Large-area wafer bonding of GaAs using hydrogen and ultrahigh vacuum atmospheres," *Applied Physics A: Materials Science and Processing*, vol. 70, iss. 1, pp. 13-9, 2000.
- [14] J. Ramm, E. Beck, A. Zuger, A. Dommann, and R. E. Pixley, "Low-temperature in situ cleaning of silicon wafers with an ultra high vacuum compatible plasma source," in *SiGe Based Technologies: Symposium A of E-MRS Spring Meeting*, vol. 222, pp. 126-31, Jun. 2 - Jun. 4, 1992, Switzerland.
- [15] N. Razek, A. Schindler, and B. Rauschenbach, "Ultra-high vacuum direct bonding of a p-n junction GaAs wafer using low-energy hydrogen ion beam surface cleaning," *Vacuum*, vol. 81, iss. 8, pp. 974-8, 2007.

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- [16] A. Reznicek, R. Scholz, S. Senz, and U. Gosele, "Comparative TEM study of bonded silicon/silicon interfaces fabricated by hydrophilic, hydrophobic and UHV wafer bonding," *EMC 2002. 11th International Conference on Electron Microscopy of Solids*, 2003, vol. 81, iss. 2-3, pp. 277-80, May 19 - May 23, 2002, Krynica, Poland.
 - [17] C. Taek Ryong, Y. Liu, N. Hosoda, B. Takagi, and T. Suga, "Wafer direct bonding of compound semiconductors and silicon at room temperature by the surface activated bonding method," in *2nd International Symposium on Control of Semiconductor Interfaces*, vol. 117-8, pp. 808-12, Oct. 28 - Nov. 1, 1996, Netherlands.
 - [18] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
 - [19] Q. Y. Tong and U. Gosele, "A model of low-temperature wafer bonding and its applications," *Journal of the Electrochemical Society*, vol. 143, iss. 5, pp. 1773-9, 1996.
 - [20] J. del Bene and J. A. Pople, "Theory of molecular interactions. I. Molecular orbital studies of water polymers using a minimal Slater-type basis," *Journal of Chemical Physics*, vol. 52, iss. 9, pp. 4858-66, 1970.
 - [21] T. A. Michalske and E. R. Fuller Jr, "Closure and repropagation of healed cracks in silicate glass," *Journal of the American Ceramic Society*, vol. 68, iss. 11, pp. 586-90, 1985.
 - [22] T. A. Michalske and B. C. Bunker, "Slow fracture model based on strained silicate structures," *Journal of Applied Physics*, vol. 56, iss. 10, pp. 2686-93, 1984.
 - [23] C. M. Tan, W. Yu, and J. Wei, "Comparison of medium-vacuum and plasma-activated low-temperature wafer bonding," *Applied Physics Letters*, vol. 88, iss. 11, pp. 114102-1-3, 2006.
 - [24] Q. Y. Tong, W. J. Kim, T. H. Lee, and U. Gosele, "Low vacuum wafer bonding," *Electrochemical and Solid-State Letters*, vol. 1, iss. 1, pp. 52-3, 1998.
 - [25] Y. Wei Bo, T. Cher Ming, W. Jun, D. Shu Sheng, and H. Guang Yu, "Effect of medium vacuum on low temperature wafer bonding," *Journal of Micromechanics and Microengineering*, vol. 15, iss. 5, pp. 1001-6, 2005.
 - [26] V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gosele, "Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 12, pp. 2141-3, 1989.
 - [27] E. Suhir, "Stresses in bi-metal thermostats," *Transactions of the ASME. Journal of Applied Mechanics*, vol. 53, iss. 3, pp. 657-60, 1986.
 - [28] M. Alexe, V. Dragoi, M. Reiche, and U. Gosele, "Low temperature GaAs/Si direct wafer bonding," *Electronics Letters*, vol. 36, iss. 7, pp. 677-8, 2000.

Chapter 6 The Assessment of the Sequential-Step Annealed Ar PADWB of GaAs-to-Si

6.1 Introduction

The highest specific bond energy of 1220 mJ/m² was achieved in a heterogenous severe thermally-mismatched 2-inch GaAs-to-Si direct bonded pair by developing the surface activation and heat treatment processes, which are the main stages in a wafer bonding process.

In the surface activation stage, the GaAs and Si bonding surfaces were Argon (Ar) plasma-activated using a developed conditions set of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power (refer to Chapter 4). The parameters ensured that the bonding surfaces were of low surface roughness and saturated with -OH polymerizing groups. Subsequently, they were point-contacted together at their centers at room temperature under a normal atmospheric (760 Torr) condition.

In the last stage of the heat treatment process, the contacted pair was sequential-step annealed under a high vacuum (10⁻⁶ Torr) condition (refer to Chapter 5). Through the novel annealing technique, the thermal-mismatch peeling stress was mitigated and the polymerization among the oppositely -OH groups proceeded to yield strong GaAs-O-Si interfacial bonds. First, the bonding pair was dwelled at 20°C for 24 h. Next, the temperature was raised from 20°C to 140°C through six identical thermal incremental sequential steps. Each step consisted of a ramping up stage, followed by a dwelling stage. In the ramping up stage, the temperature was increased by 20°C at a rate of 1°C/min. In the dwelling stage, the bonding pair was held for a duration of 24 h. After the annealing at the last 140°C sequential step, the temperature was ramped down to a room temperature of 20°C at a rate of 1°C/min.

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In this chapter, the GaAs-to-Si bonded pair with the highest specific bond energy of 1220 mJ/m^2 will be assessed. First, the value will be compared with other specific bond energy values that were derived from various bonded systems and bonding techniques. Second, the bonding interface will be characterized and analyzed. Third, the integrity of the bonding will be justified by subjecting the bonded pair to a harsh mechanical process.

6.2 The Comparison with Other Specific Bond Energies

Table 6-1 presents the specific bond energies of some bonded systems and bonding techniques with which the current 1220 mJ/m^2 of GaAs-to-Si specific bond energy (achieved from the bonding processes as described in 6.1) can be compared. Most of the bonding techniques listed in the table are the current state-of-the-art low temperature solutions (except for [1, 2]), which are able to achieve very high bond energies after low temperature thermal treatments of less than 150°C . All of the bonded wafers listed in the table are of wafer-scale size (several hundred micrometers thick). The subsequent discussion in the current section will be based heavily on the data in Table 6-1.

It can be observed from the table that the ultra-high vacuum (UHV) (10^{-9} Torr to 10^{-11} Torr) bonding technique is able to achieve a very high bond energy. Comparing the various bonding techniques in the Si-to-Si bonded system, the highest specific bond energy of 2000 mJ/m^2 was derived from the UHV bonding technique [3]. The bonding procedures and mechanism that are associated with the UHV bonding technique can be found in [3-5].

The specific bond energy of the GaAs-to-GaAs bonded system seems to be much lower than the specific bond energies of the various bonding techniques considered in the Si-to-Si bonded system [2, 3, 6, 7]. Even when a pair of GaAs wafers was UHV bonded and annealed under a UHV condition at 150°C , the maximum resultant specific bond energy was only 1000 mJ/m^2 [4]. Hence, the specific bond energy of a bonded pair of GaAs-to-Si is expected to be between 1000 mJ/m^2 and 2000 mJ/m^2 or near 1000 mJ/m^2 since the bonding GaAs appeared to limit the bond energy.

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Table 6-1: The post-annealing specific bond energies of several selected bonded systems and bonding techniques.

Reference	Bonding System	Bonding Technique	Annealing		Specific Bond Energy (mJ/m ²)
			Ambient	Annealing Temperature (°C)	
[2]	Si-to-Si	wet activation	760 Torr normal atmospheric	150	1200
[6]	Si-to-Si	plasma activation	760 Torr normal atmospheric	140	1750
[7]	Si-to-Si	wet activation	5 Torr low vacuum	150	1800
[3]	Si-to-Si	UHV	-	-	2000 ^a
[5]	GaAs-to-GaAs	UHV	-	-	830 ^a
[5]	GaAs-to-GaAs	UHV	10 ⁻¹¹ Torr UHV	140	990
[4]	GaAs-to-GaAs	UHV	10 ⁻¹¹ Torr UHV	150	700 to 1000
[1]	GaAs-to-Si	(not available)	760 Torr normal atmospheric	140	220
This work	GaAs-to-Si	plasma activation	10 ⁻⁶ Torr high vacuum	140 ^b	1220

^a The bond energy value is obtained after a room temperature (20°C) contact under a 10⁻¹¹ Torr UHV condition.^b Sequential-step annealing (see Figure 5-6).

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Currently, the achieved 1220 mJ/m^2 of specific bond energy in the sequential-step annealed Ar PADWB of GaAs-to-Si is slightly higher than the specific bond energy derived from the UHV bonding of GaAs-to-GaAs [4]. Moreover, it is comparable to the specific bond energy derived from the conventional WADWB of Si-to-Si [2]. However, despite the fact that the bonding techniques were similar, the current 1220 mJ/m^2 of GaAs-to-Si specific bond energy is still much lower than the specific bond energies reported in [6, 7] regarding the Si-to-Si bonded system. This finding suggests that not all the oppositely -OH groups of the GaAs-OH and Si-OH surface species in the present GaAs-to-Si bonded pair were being polymerized as the peeling stress-induced microscopic interfacial gap opening effect was not completely eliminated with the present sequential-step annealing process. However, the use of the Ar plasma activation and the annealing under a high vacuum (10^{-6} Torr) condition will compensate for the low bond energy that was associated with the peeling stress effect. Therefore, a high specific bond energy of 1220 mJ/m^2 can be achieved. It is also highly plausible that the bonding GaAs material limits the GaAs-to-Si bond energy (see the comparison of the specific bond energies of the GaAs-to-GaAs bonded system with the Si-to-Si bonded system in Table 6-1).

Although the specific bond energy of the UHV bonding of Si-to-Si was 2000 mJ/m^2 [3], which is much higher than the currently achieved 1220 mJ/m^2 of specific bond energy in the sequential-step annealed Ar PADWB of GaAs-to-Si, the high cost that is associated with the sophisticated system used in UHV bonding may render the UHV bonding process unattractive. Both the UHV and sequential-step annealing bonding techniques require extremely long process times, which are the downsides.

The literature on the wafer-scale bonding of severe thermally-mismatched GaAs-to-Si measuring several hundreds of micrometers thick seems to be very limited and rarely discussed. To the author's knowledge, the only literature on the bonding of thick GaAs and Si

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at a wafer-scale is available in [1]. These researchers bonded 3-inch GaAs and Si wafers together and the specific bond energy was only 220 mJ/m^2 after annealing at 140°C . The form of surface activation used in their bonding work was not mentioned. The 220 mJ/m^2 of specific bond energy achieved in [1] was lower by a factor of 6 than the currently achieved specific bond energy of 1220 mJ/m^2 in the bonding of severe thermally-mismatched GaAs-to-Si.

In short, the present bonding technique of having the GaAs and Si bonding surfaces Ar plasma-activated and then followed by the sequential-step annealing process under a high vacuum condition has proven itself a viable low temperature bonding solution, especially in the bonding of severe thermally-mismatched GaAs-to-Si. The derived 1220 mJ/m^2 of specific bond energy was comparable to those in the Si-to-Si and GaAs-to-GaAs bonding systems of various low temperature bonding techniques.

6.3 The Characterization of the Sequential-Step Annealed Ar PADWB of the GaAs-to-Si Bonded Interface

The bonded interface of the GaAs-to-Si pair with the 1220 mJ/m^2 of specific bond energy was being examined by transmission electron microscopy (TEM). The cross-sectional sample was prepared using the focused ion beam (FIB) technique. Figure 6-1(a) displays the high-resolution transmission electron microscopy (HR-TEM) image of the GaAs-to-Si bonded interface. The various regions and the thicknesses of the native GaAs and Si oxides are indicated in the image. Figure 6-1(b) and Figure 6-1(d) show the orderly diffraction spots (that correspond to the crystal planes) of the bonded crystalline GaAs and Si. Figure 6-1(c) displays the diffusive diffraction pattern that is characteristic of an amorphous structure, which corresponds to the intermediate native oxide layers of the bonded GaAs and Si. Figure 6-1(e) displays the diffraction pattern of the overall bonded structure.

The HR-TEM image of Figure 6-1(a) reveals an abrupt change in the intensity of the GaAs and Si native oxides, which reflects that the interface was tightly bonded. Furthermore, no threading dislocation defects were observed, which justifies the competitive edge that wafer bonding has over epitaxial growth in the technology of monolithic integration. The GaAs and Si native oxide thicknesses were found to be roughly 7 nm and 2 nm, respectively. The large difference in the thicknesses may be attributed to the different chemical treatments that the GaAs and Si wafers were being subjected to during the initial cleaning stage. The GaAs and Si wafers were initially treated with acetone and isopropanol solutions. In addition, the Si wafer was treated with a base solution containing hydrogen peroxide (H_2O_2), which is a strong oxidizer. This explains why the Si native oxide was much thicker than the GaAs native oxide.

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Figure 6-1: (a) shows the cross-sectional HR-TEM image of the bonded interface of the sequential-step annealed Ar PADWB of GaAs-to-Si pair with the 1220 mJ/m^2 of specific bond energy. (b), (c), (d), and (e) show the diffraction patterns of the crystalline bonded GaAs, the amorphous GaAs and Si native oxides, the crystalline bonded Si, and the overall bonded structure, respectively.

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Subsequently, to determine its bond strength qualitatively, an attempt was made to cleave the GaAs-to-Si bonded pair apart completely by means of a razor blade. During the cleaving process, the interfacial bond was so strong that the insertion of the razor blade through the bonded interface required a considerable amount of force and the weaker GaAs was cracked into pieces (see Figure 6-2[a]). This suggested that the bond strength might exceed the fracture strength of the bulk GaAs.

Figure 6-2: (a) shows the photograph of the surface irregularities on the completely cleaved apart bonded GaAs surface. (b) shows the SEM image of one of the GaAs surface irregularities. (c) and (d) show the EDX analysis.

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Furthermore, upon inspections of the cleaved apart GaAs and Si bonding surfaces, a large number of surface irregularities were observed. The surface irregularities on the 2-inch cracked-GaAs and Si surfaces are shown in Figure 6-2(a) and Figure 6-3(a), respectively. The photographs were taken on a black background and a printed-out square grid pattern was reflected on the surfaces for clearer observation purposes. The scanning electron microscopy (SEM) images of one of the irregularities on each of the GaAs and Si surfaces are shown in Figure 6-2(b) and Figure 6-3(b), respectively. Energy-dispersive X-ray spectroscopy (EDX) was performed to determine the elements of the irregularities.

Figure 6-3: (a) shows the photograph of the surface irregularities on the completely cleaved apart bonded Si surface. (b) shows the SEM image of one of the Si surface irregularities. (c) and (d) show the EDX analysis.

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Both of the EDXs performed on a GaAs surface irregularity and on the completely cleaved apart bare GaAs bonded surface revealed only Gallium (Ga) and Arsenide (As) elemental peaks (see Figure 6-2(c) and Figure 6-2(d), respectively). The EDX on the completely cleaved apart bare Si bonded surface revealed a Si elemental peak (see Figure 6-3[d]). However, interestingly, Gallium (Ga) and Arsenide (As) elemental peaks were detected from the Si surface irregularity (see Figure 6-3[c]).

The EDX observations reveal that the GaAs was bonded so strongly to the Si that, during the cleaving process, the GaAs remained fused to the Si and the failure occurred in the weaker bulk GaAs instead. Figure 6-4 accounts for the EDX observations schematically. This further justifies the successful fusion between the GaAs and Si wafers using the bonding techniques as highlighted in Section 6.1.

Figure 6-4: A schematic diagram of the GaAs and Si surface irregularities that were observed after complete cleavage through the strongly GaAs-to-Si bonded interface.

6.4 The Mechanical Thinning of a Sequential-Step Annealed Ar PADWB of GaAs-to-Si Pair

The effect of the peeling stress-induced low bond energy of a thermally-mismatched GaAs-to-Si bonding pair can be mitigated by annealing the pair in incremental sequential steps, which will result in an extensive polymerization between the oppositely surface saturated -OH groups. This was discussed in Section 6.1. However, the thermal-mismatch normal stresses of σ_z and σ_{xy} , as indicated in Figure 5-2, will act to cause fracture failure when the GaAs-to-Si bonding pair is subjected to a much higher temperature during a growth process. For example, the growth temperature of a conventional molecular beam epitaxy (MBE) process ranges between 400°C to 600°C [8]. If such a high temperature MBE growth process is performed on the GaAs of a GaAs-to-Si bonded substrate, the substrate will crack even before the growth can proceed.

Table 6-2: The failure temperature at which a GaAs-to-Si bonded pair will debond or fracture as a function of the GaAs and Si thicknesses and the GaAs to Si thickness ratio.

The data are adapted from [9].

GaAs to Si Thickness Ratio	GaAs Thickness (μm)	Si Thickness (μm)	Failure Temperature (°C)
~ 1	638	635	160
0.09	48	540	200
0.65	212	325	250
0.61	89	145	> 350

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Table 6-2 shows the failure temperature of a GaAs-to-Si bonding pair in relation to the GaAs and Si thicknesses and the GaAs to Si thickness ratio [9]. The data show that, to enable a heterogenous thermally-mismatched GaAs-to-Si bonded pair to withstand high temperatures without fracture failure, it is essential for either or both sides of the bonding pair to be sufficiently thin.

In Section 2.4, the current state-of-the-art techniques in obtaining a thin layer or thin layers were reviewed. Among the discussed techniques, the physical abrasion of a wafer backside to thin it down is the most direct and facile approach. Presently, the bond energy of a GaAs-to-Si pair that was bonded through the processes described in Section 6.1 was put to a test by subjecting the bonded pair to a harsh mechanical treatment. Moreover, the eventual thinned-down bonded pair may act as a substrate for elevated temperature structural or device growth.

Unlike conventional approaches whereby only one side of a bonded pair is being thinned down [10], the present sequential-step annealed GaAs-to-Si bonded pair was thinned down from the backsides of both the GaAs and Si. This was done to provide more tolerance towards the thickness variation during the thinning process. For example, if only the GaAs of a GaAs-to-Si bonded pair is thinned down to enable the pair to withstand temperatures higher than 450°C, the final GaAs thickness needs to be lesser than 5 μm [11]. This would require very tight thickness control and leave little allowance for any thickness variation.

The mechanical thinning processes of the GaAs-to-Si bonded pair were performed using a Logitech (Ltd. UK) bench-top PM5 lapping and polishing system. The bonded pair was first thinned down by lapping the Si from its backside. The lapping of the Si was performed on a concentric grooves cast iron plate using a 9 μm alumina (Al_2O_3) particle-size slurry solution. During the lapping process, the rotational speed of the plate was set at 35 revolutions per minute (RPM) and the slurry dispense rate was set to about 1 $\mu\text{L/s}$.

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Next, the GaAs was chemical mechanical polished from its backside. The CMP of the GaAs was performed on a polishing cloth adhered onto a stainless steel plate using a proprietary polishing solution that contains sodium hypochlorite and Al_2O_3 . The pH-value of the solution was 11.4. During the CMP process, the rotational speed of the plate (with the polishing cloth) was set at 60 revolutions per minute (RPM). The slurry dispense rate was set to about 0.25 $\mu\text{L/s}$.

During the long periods of the mechanical thinning processes, the GaAs-to-Si bonded pair was subjected constantly to a high torsional stress state as static pressures were being applied to the bonded pair while it was rotating with respect to the rotating plates. However, the GaAs-to-Si bonded pair did not debond. Hence, the bond energy of the sequential-step annealed Ar PADWB of GaAs-to-Si was sufficiently high to withstand the long hours of the harsh mechanical treatment. The Si was lapped down from a thickness of $289 \pm 1 \mu\text{m}$ to a final thickness of $62 \pm 6 \mu\text{m}$. The GaAs was chemical mechanical polished down from a thickness of $453 \pm 1 \mu\text{m}$, to a final thickness of $64 \pm 3 \mu\text{m}$.

Figure 6-5(a) displays the photograph of the polished GaAs backside surface of the thinned-down GaAs-to-Si bonded pair. A printed-out square grid pattern was reflected on the surface for clearer observation purposes. The thinned-down GaAs-to-Si bonded pair was adhered onto a glass substrate by means of double-sided tape and the photograph of the whole structure was taken on a black background. Figure 6-5(b) displays the photograph of the reference bare 2-inch polished surface of a prime-grade GaAs wafer (also taken on a black background with a printed-out square grid pattern reflected on the surface). The photograph of the CMP GaAs backside surface in Figure 6-5(a) can be compared with this photograph. The regular array of the reflected grids reflects the high quality of the finished GaAs backside surface.

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Figure 6-5: (a) and (b) show the photographs of the polished GaAs backside surface and the reference bare 2-inch GaAs wafer surface, respectively.

Furthermore, the polished GaAs surface was evaluated by determining its surface roughness and the surface roughness variation. The surface roughness characterization was performed using a Bruker[®] Dimension Edge[™] AFM system, which can accommodate a 2-inch size sample. All of the AFM works were conducted under a tapping mode.

Figure 6-6 presents the representative 20 by 20 μm^2 AFM 3D scan image that was derived from a central region of the 2-inch polished GaAs backside surface of the thinned-down GaAs-to-Si bonded pair. The AFM scan was performed with 512 data points and lines acquisition. The corresponding representative surface roughness of the polished GaAs backside surface was found to be of a low root-mean-square (RMS) value of 1.72 nm.

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Figure 6-6: The representative 3D AFM scan image of the polished GaAs backside surface.

Figure 6-7: A schematic diagram showing the right, top, left, bottom, and center regions with respect to the reference primary flat of the polished GaAs backside surface.

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To determine the surface roughness homogeneity, five regions across the 2-inch polished GaAs backside surface of the thinned-down GaAs-to-Si bonded pair were selected to perform the AFM scans. The regions were the right, top, left, bottom, and center, with respect to the primary flat of the CMP GaAs backside surface (see Figure 6-7). Each scan size was 10 by 10 μm^2 and the AFM was performed with 256 data points and lines acquisition. The surface roughness data are shown in Table 6-3. The average surface roughness value of the 10 by 10 μm^2 AFM scans was 1.64 nm RMS. More importantly, the surface roughness standard deviation was determined to be only 0.09 nm RMS, which indicates a low surface roughness variation across the 2-inch CMP GaAs backside surface.

Table 6-3: The surface roughness data of the AFM scans on the polished GaAs backside surface.

Region ^a	Surface Roughness ^b (nm RMS)
Right	1.50
Top	1.71
Left	1.60
Bottom	1.68
Center	1.70

^a With respect to the reference primary flat of the polished GaAs backside surface of the thinned-down GaAs-to-Si bonded pair.

^b Each AFM scan size is 10 by 10 μm^2

6.5 Conclusion

The present chapter serves to justify the integrity of a GaAs and Si pair that was bonded via the Ar plasma activation and sequential-step annealed up to 140°C.

First, the justification was being made by comparing the associated GaAs-to-Si high specific bond energy of 1220 mJ/m² with the specific bond energy values that were derived from a couple of bonded systems of various bonding techniques. The comparison study showed that the presently achieved 1220 mJ/m² of specific bond energy of the GaAs-to-Si bonded pair was higher than all of the GaAs-to-GaAs specific bond energies. Although the 1220 mJ/m² specific bond energy value was much lower than that derived from the UHV bonding of Si-to-Si, it was still comparable to the energy value of the WADWB of Si-to-Si that was annealed at 150°C.

Second, the 1220 mJ/m² of specific bond energy bonded interface was examined by HR-TEM. The microscopy image revealed an abrupt bonded interface. This reflected the tight bonding between the GaAs and Si native oxides. Moreover, no threading dislocation defects were observed. The integrity of the GaAs-to-Si bonding was further justified by the findings that fractured GaAs remains stayed strongly fused to the Si when the bonded pair was completely cleaved apart. This was confirmed by the EDX analysis.

Lastly, a sequential-step annealed Ar PADWB of GaAs-to-Si pair was put through a prolonged torsional stress state by mechanically thinning the GaAs and the Si from their backsides. Although the bonded pair was rotated at relatively high speeds with respect to the rotating plates under high static pressures during the prolonged mechanical thinning process, the bonded pair remained strongly intact. The representative GaAs surface roughness that was derived from a 20 by 20 μm² AFM scan at the central region of the CMP GaAs backside was 1.72 nm RMS. Moreover, the surface roughness variation across the 2-inch CMP GaAs backside was low with a standard deviation of only 0.09 nm RMS.

References

- [1] V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gosele, "Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom," *Japanese Journal of Applied Physics, Part 2 (Letters)*, vol. 28, iss. 12, pp. 2141-3, 1989.
- [2] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
- [3] U. Gosele, H. Stenzel, T. Martini, J. Steinkirchner, D. Conrad, and K. Scheerschmidt, "Self-propagating room-temperature silicon wafer bonding in ultrahigh vacuum," *Applied Physics Letters*, vol. 67, iss. 24, pp. 3614-6, 1995.
- [4] G. Kastner, T. Akatsu, S. Senz, A. Plocl, and U. Gosele, "Large-area wafer bonding of GaAs using hydrogen and ultrahigh vacuum atmospheres," *Applied Physics A: Materials Science and Processing*, vol. 70, iss. 1, pp. 13-9, 2000.
- [5] N. Razek, A. Schindler, and B. Rauschenbach, "Ultra-high vacuum direct bonding of a p-n junction GaAs wafer using low-energy hydrogen ion beam surface cleaning," *Vacuum*, vol. 81, iss. 8, pp. 974-8, 2007.
- [6] T. Suni, K. Henttinen, I. Suni, and J. Makinen, "Effects of plasma activation on hydrophilic bonding of Si and SiO₂," *Journal of the Electrochemical Society*, vol. 149, iss. 6, pp. 348-51, 2002.
- [7] Q. Y. Tong, W. J. Kim, T. H. Lee, and U. Gosele, "Low vacuum wafer bonding," *Electrochemical and Solid-State Letters*, vol. 1, iss. 1, pp. 52-3, 1998.
- [8] R. F. C. Farrow, *Molecular beam epitaxy [electronic resource] : applications to key materials / edited by Robin F.C. Farrow*: Park Ridge, N.J. : Noyes Publications, 1995.
- [9] Q. Y. Tong and U. Gösele, *Semiconductor wafer bonding : science and technology / Q.-Y. Tong, U. Gösele*: New York : John Wiley, 1999.
- [10] A. Georgakilas, G. Deligeorgis, E. Aperathitis, D. Cengher, Z. Hatzopoulos, M. Alexe, V. Dragoi, U. Gosele, E. D. Kyriakis-Bitaros, K. Minoglu, and G. Halkias, "Wafer-scale integration of GaAs optoelectronic devices with standard Si integrated circuits using a low-temperature bonding procedure," *Applied Physics Letters*, vol. 81, iss. 27, pp. 5099-101, 2002.
- [11] M. Alexe, V. Dragoi, M. Reiche, and U. Gosele, "Low temperature GaAs/Si direct wafer bonding," *Electronics Letters*, vol. 36, iss. 7, pp. 677-8, 2000.

Chapter 7 Conclusions, Future Work, and Technological Impacts

7.1 Conclusions

The monolithic integration among dissimilar materials via the wafer bonding technology offers an elegant approach through which the material issue of lattice and crystal mismatches-induced detrimental massive threading dislocations will not be encountered. Moreover, the bonding of dissimilar materials at a wafer-scale can realize economics of scale that are crucial in today's electronics industry. However, the thermal-mismatch stresses that are inherent in the bonding system of thick wafer-scale dissimilar materials at elevated temperatures impede the development of the wafer bonding technology.

In the present research, the high bond energy of a severe thermally-mismatched thick GaAs-to-Si bonded pair at a wafer-scale is sought so that the pair could undergo subsequent processes that will eventually realize a single block of platforms on which Si Integrated Circuits (IC) and GaAs optoelectronics devices are integrated together. The research was conducted systematically by developing the surface activation stage first followed by the last thermal treatment stage.

The objective in the development of the surface activation stage is to achieve high amounts of the GaAs-OH and Si-OH species at the GaAs and Si bonding surfaces, respectively, while ensuring the bonding surfaces have low surface roughness. The high amount of the oppositely -OH groups can then come close enough to polymerize during the annealing to yield a large amount of strong covalent GaAs-O-Si interfacial bonds, which will lead to a high bond energy. Presently, the GaAs and Si bonding surfaces were plasma-activated with Argon (Ar) gas. The development of the Ar exposure time, pressure, and RF

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power plasma parameters was conducted through a 2^3 full factorial design study. Through the analysis-of-the-variance (ANOVA), the Ar plasma conditions set of 30 s of exposure time, 120 mTorr of pressure, and 200 W of RF power was found to yield the highest specific bond energy after one-step annealing at 140°C for 24 h under a normal atmosphere condition. The presence of the large amount of the induced -OH polymerizing surface groups and the low roughness of the GaAs and Si bonding surfaces were verified through contact angle measurement and atomic force microscopy (AFM), respectively.

The next research step was to have as much of the high amount of the induced oppositely -OH groups on the GaAs and Si bonding surfaces as possible to polymerize by annealing. This is often hindered by the abhorrent thermal-mismatch peeling stress that acts to pry a bonding pair apart at the wafer edges. In the present efforts, the peeling stress-induced remoteness of the oppositely polymerizing species effect was curbed by a developed simplistic annealing technique. The novel heat treatment process involved annealing an Ar PADWB of GaAs-to-Si pair in sequential steps of increasing temperature. The highest specific bond energy of 1220 mJ/m² was achieved after an Ar PADWB of GaAs-to-Si pair was annealed in 6 identical incremental sequential steps from a room temperature of 20°C to 140°C under a high vacuum (10^{-6} Torr) condition. Each sequential step involved ramping up the temperature by 20°C at a rate of 1°C/min followed by a dwelling stage of 24 h.

The bonded interface of the sequential-step annealed Ar PADWB of GaAs-to-Si pair with the 1220 mJ/m² of specific bond energy was examined using transmission electron microscopy. This examination revealed a high quality, tightly bonded interface. The strong fusion of the GaAs to the Si was further justified through the energy-dispersive X-ray spectroscopy (EDX) analysis on the cleaved apart bonded GaAs and Si surfaces.

For process demonstration, a GaAs-to-Si bonded pair that was prepared using the developed Ar plasma activation and sequential-step annealing processes was mechanically

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thinned down from both the GaAs and Si backsides. Although subjected to prolonged high torsional stress during the mechanical thinning processes, the GaAs-to-Si bonded pair remained bonded. The Si was lapped down from a thickness of $289 \pm 1 \mu\text{m}$ to a final thickness of $62 \pm 6 \mu\text{m}$, whereas the GaAs was chemical mechanical polished (CMP) down from a thickness of $453 \pm 1 \mu\text{m}$ to a final thickness of $64 \pm 3 \mu\text{m}$. The surface roughness and the roughness variation across the 2-inch final polished GaAs backside surface of the thinned-down GaAs-to-Si bonded pair were 1.72 nm RMS and 0.09 nm RMS, respectively, which were sufficiently low to be considered for structural or device growths.

7.2 Future Work and Applications

As commented by Samuel Johnson (1709-1784) [1]: “If a man has a science to learn he must regularly and resolutely advance.” Presently, the novel sequential-step annealing approach has presented itself as an efficient low temperature bonding alternative that does not require a costly, sophisticated system, and high temperature annealings to achieve a high bond energy in the severe thermally-mismatched bonded system of GaAs-to-Si. However, the analysis and the work performed in the current research efforts are still immature and by no means exhaustive. Deeper science understandings and stronger justifications are required. Since the development of the plasma parameters through the factorial design approach and the sequential-step annealing process was proven able to achieve a high bond energy in the bonding of GaAs and Si, the same strategies can also be extended to other thermally-mismatched bonding systems such as InP-to-Si. Furthermore, the high specific bond energies of sequential-step annealed Ar PADWB of GaAs-to-Si pairs should also be exploited in the development of monolithic substrate engineering and heterogenous devices integration.

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7.2.1 Critiques and Suggested Improvements on the Current Work

Inspection of the Interfacial Voids

Presently, the voids at the bonded interfaces of the GaAs-to-Si pairs were examined through the infrared (IR) imaging technique. However, such an imaging technique could not resolute voids of diameters less than 1 mm [2]. Hence, it is proposed that the voids inspection should be performed with the scanning acoustic microscopy (SAM) technique, which has a resolution of about 0.01 mm [3].

Bond Energy Evaluation

The specific bond energies of the current GaAs-to-Si bonding pairs were determined using the crack-opening method. In this approach, a small crack is induced at the peripheral region of a bonded interface by manually inserting a razor blade. However, the bond energy data that is derived from such a characterization technique is highly dependent on human factors. Presently, the angle and the rate at which the razor blade was inserted into the bonded interfaces were not consistent to a small extent. Hence, it is suggested that the razor blade insertion should be automated such that the insertion is parallel to a bonded interface of interest and can be controlled at a constant, low, and fixed rate [4].

The Sequential-Step Annealing Process

The demonstration of the use of sequential-step annealing in the thermally-mismatched GaAs-to-Si bonding system to achieve a high bond energy is a new technique that is rarely discussed and has just been explored. The present investigations were performed systematically by making all of the thermal incremental steps identical throughout each sequential-step annealing. Other possible forms of sequential-step annealing temperature

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profiles were not considered. Thus, a considerable number of investigations have to be conducted to gain a deeper understanding of the sequential-step annealing process.

Currently, the total annealing duration of the sequential-step annealing process that yields the highest specific bond energy of 1220 mJ/m^2 of a Ar PADWB of GaAs-to-Si pair was about 144 h (6 days), neglecting the time taken during the ramping up and down of the temperature. From a manufacturing perspective, the total annealing duration of 144 h per GaAs-to-Si bonding pair may seem to be too long to be practical.

A way to shorten the overall sequential-step annealing duration is to omit the annealings at lower temperature steps since the thermal effect may be too weak to induce significant interfacial water (H_2O) out-diffusion, which is necessary to enable the oppositely - OH groups to come in close proximity before they can polymerize. Moreover, when a sequential-step annealing is performed at an elevated temperature other than 20°C , the annealing may involve dissimilar incremental sequential steps that can shorten the overall annealing duration further. For example, the temperature increment of the steps may be decreased successively since the peeling stress grows with increasing temperature. Hence, very small temperature increments of the sequential steps are only required at higher temperature annealings to suppress the microscopic interfacial gap opening effect induced by the substantial peeling stress. In addition, the dwelling duration of the dissimilar incremental sequential steps may also decrease successively alongside the successive decrement in the temperature increment. The temperature profile of such a sequential-step annealing example that involves the dissimilar thermal steps is shown in Figure 7-1 where the annealing starts only at a temperature of 80°C . The heat treatment process can be visualized as a quasi-logarithmic annealing as indicated by the dotted line in Figure 7-1. Such a sequential-step annealing process will take a lesser total duration of 108 h (4.5 days).

Figure 7-1: The temperature profile of a quasi-logarithmic sequential-step annealing.

Alternatively, the long duration of the sequential-step annealing process of a GaAs-to-Si bonding pair can be resolved directly through batch annealing. For example, in the present sequential-step annealing process that uses 6 identical incremental thermal steps, if a batch of six Ar PADWB of GaAs-to-Si bonding pairs were annealed all at once under a high vacuum condition, the effective annealing duration per bonding pair will only be 24 h (1 day). The leverage will increase with the increasing number of bonding pairs being annealed. Furthermore, the idea of the sequential-step annealing in batches is feasible as the annealing process does not require a complex system unlike the UHV bonding technique. Hence, it is very suitable for mass manufacturing.

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Currently, only one specific bond energy data per set of bonding conditions was collected because the self-improvised high vacuum heating system (refer to Section 3.3) can only accommodate one GaAs-to-Si bonding pair per annealing process. The error bars in some of the specific bond energy plots are due to the inaccuracy that is associated with the crack-opening bond energy characterization technique, which is set at $\pm 15\%$ of the specific bond energy values [5, 6]. If a batch sequential-step annealing is performed, more specific bond energy data for every set of bonding conditions can be collected to reflect a truer variation in the bond energy result.

7.2.2 Recommended Future Work and Technological Impacts

Structural Growths on GaAs-to-Si Bonded Substrates

A GaAs-to-Si bonded pair offers a monolithic integrated substrate of dual-generic platforms on which optoelectronics and microelectronics structures and devices of any kinds of materials can be grown as long as the grown materials are lattice matched to either the GaAs or Si platform. Hence, the structures and the devices that possibly could be realized on the generic GaAs-to-Si integrated substrate are too numerous to be listed here.

However, it is vital to ensure that a GaAs-to-Si bonded substrate has to be sufficiently thin before it can withstand elevated temperature growths without fracturing. In Section 6.4, the bond energy of a sequential-step annealed Ar PADWB of GaAs-to-Si pair was demonstrated as sufficiently high enough to withstand the prolonged high torsional stress of the mechanical thinning process. Moreover, the GaAs-to-Si bonded pair was thinned down from both of the GaAs and Si backsides so that the respective final thickness was not too thin to accommodate the thinning down thickness variation that is inherent to the lapping and polishing processes. Hence, this may open up a new area of study to determine the

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withstanding temperature of a GaAs-to-Si bonded pair as a function of the GaAs and Si thickness.

Furthermore, the GaAs-to-Si bonded structure can be developed further into a GaAs-to-Si-on-insulator (GaAs-to-Si-OI) bonded structure. The advantages of on-insulator devices were highlighted in Section 2.4. A GaAs-to-Si-OI bonded structure can be easily realized by depositing an oxide on either the bonding GaAs or Si surface (or both) prior to the developed Ar plasma activation and sequential-step annealing treatments. The bonding deposited oxide surface(s) may have to undergo the additional step of a polishing process to attain a sufficiently low roughness that is required for good bonding. Figure 7-2 presents an example of the process flow in achieving a GaAs-to-Si-OI bonded structure, in which the oxide is deposited on the bonding GaAs surface.

Figure 7-2: A schematic diagram that illustrates the process flow in achieving a GaAs-to-Si-OI bonded structure.

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Low-Cost GaAs-to-Si-on-Insulator Substrate Engineering

In Section 2.4.4, the lateral etching epitaxial lift-off (LE-ELO) layer transfer technology [7, 8] was reviewed and the advantages were highlighted. However, the application of the elegant process in realizing a dissimilar materials integrated substrate at a wafer-scale was rarely reported, which may be due to the requirement that the interfacial bond energy needs to be very high to withstand the prolonged hydrofluoric (HF) bath immersion. Presently, the high bond energy that is derived from the developed Ar plasma activation and sequential-step annealing recipes could enable the coupling of the wafer bonding technology with the LE-ELO technology in achieving a GaAs-to-Si-on-insulator (GaAs-to-Si-OI) bonded substrate at a wafer-scale.

Presently, the largest commercially available Si and GaAs wafer sizes are 12-inch and 6-inch, respectively. Although the 6-inch GaAs wafers are commercially available, the cost is much higher than that of the 12-inch Si wafers. Coupled with the graded buffer technology, the evolution of a 12-inch GaAs-to-Si-OI substrate is likely possible at a low cost.

Figure 7-3 presents a schematic process flow of the coupling of the wafer bonding, the LE-ELO, and the graded buffer technologies to obtain a large wafer-scale GaAs-to-Si-OI structure. The sequential process steps are as follows:

- Step 1:
- 1) A GaAs(device)/AlAs(release)/GaAs(buffer) structure is MBE grown on a $\text{Si}_x\text{Ge}_{1-x}$ (graded buffer)/Si(wafer) lattice-matched substrate that may be 12-inch in size.
 - 2) An oxide is deposited on a Si wafer. Oxide deposition on the GaAs(device) surface of the GaAs(device)/AlAs(release)/GaAs(buffer)/ $\text{Si}_x\text{Ge}_{1-x}$ (graded buffer)/Si(wafer) substrate is possible, too.
 - 3) The deposited oxide/s may need to be polished to yield a low surface roughness that is required for good bonding.

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4) The two structures are then contacted together after Ar plasma activation of the bonding surfaces.

Step 2: The bonding structure is subjected to a sequential-step annealing heat treatment to yield a high bond energy.

Step 3: The intermediate AlAs sacrificial release layer is etched laterally by immersing the bonded structure in a HF bath of a suitable HF concentration.

Step 4: A GaAs-to-Si-OI structure will be obtained after the lift-off process. The GaAs(buffer)/Si_xGe_{1-x}(graded buffer)/Si(wafer) substrate can be recycled for subsequent LE-ELO process cycles. Hence, the material cost is reduced greatly.

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Figure 7-3: A schematic diagram that illustrates the LE-ELO process that is coupled with the graded buffer technology to obtain a low-cost GaAs-to-Si-OI substrate.

References

- [1] J. Boswell, *The life of Samuel Johnson, LL.D [electronic resource] : comprehending an account of his studies and numerous works, in Chronological order; a series of his Epistolary Correspondence and Conversations with many eminent persons; and various original pieces of his composition, never before published: the whole exhibiting a view of literature and literary men in Great-Britain, for near half a century, during which he flourished. In three volumes. The second edition, revised and augmented. By James Boswell, Esq.* London : printed by Henry Baldwin, for Charles Dilly, in the Poultry, MDCCXCIII. 1793.
- [2] W. P. Maszara, "Silicon-on-insulator by wafer bonding. A review," *Journal of the Electrochemical Society*, vol. 138, iss. 1, pp. 341-7, 1991.
- [3] R. A. Lemons and C. F. Quate, "Acoustic microscope-scanning version," *Applied Physics Letters*, vol. 24, iss. 4, pp. 163-5, 1974.
- [4] Z. Xuan Xiong and J. P. Raskin, "Low-temperature wafer bonding: a study of void formation and influence on bonding strength," *Journal of Microelectromechanical Systems*, vol. 14, iss. 2, pp. 368-82, 2005.
- [5] T. Qin-Yi, G. Cha, R. Gafiteanu, and U. Gosele, "Low temperature wafer direct bonding," *Journal of Microelectromechanical Systems*, vol. 3, iss. 1, pp. 29-35, 1994.
- [6] Q. Y. Tong, W. J. Kim, T. H. Lee, and U. Gosele, "Low vacuum wafer bonding," *Electrochemical and Solid-State Letters*, vol. 1, iss. 1, pp. 52-3, 1998.
- [7] E. Yablonovitch, T. Gmitter, J. P. Harbison, and R. Bhat, "Extreme selectivity in the lift-off of epitaxial GaAs films," *Applied Physics Letters*, vol. 51, pp. 2222-4, 1987.
- [8] M. M. A. J. Voncken, J. J. Schermer, G. J. Bauhuis, A. T. J. van Niftrik, and P. K. Larsen, "Strain-accelerated HF etching of AlAs for epitaxial lift-off," *Journal of Physics: Condensed Matter*, vol. 16, pp. 3585-96, 2004.

Appendix

Appendix

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Appendix

Figure A-1: The AFM 3D surfaces of (a) untreated bare GaAs reference surface and GaAs surfaces exposed to (b) Run 1, (c) Run 2, (d) Run 3, (e) Run 4, (f) Run 5, (g) Run 6, (h) Run 7, and (i) Run 8 of the 2^3 factorial design Ar plasma conditions (see Table 4-1 and Table 4-2).

Appendix

(a)

(b)

(c)

(d)

(e)

(f)

(g)

Appendix

Figure A-2: The AFM 3D surfaces of (a) untreated bare Si reference surface and Si surfaces exposed with (b) Run 1, (c) Run 2, (d) Run 3, (e) Run 4, (f) Run 5, (g) Run 6, (h) Run 7, and (i) Run 8 of the 2^3 factorial design Ar plasma conditions (see Table 4-1 and Table 4-2).