Transport studies in quasi one-dimensional III-V wires, tubes, and fin structures

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2014

Xing, D. (2014). Transport studies in quasi one-dimensional III-V wires, tubes, and fin structures. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/61721>

<https://doi.org/10.32657/10356/61721>

**TRANSPORT STUDIES IN QUASI ONE-DIMENSIONAL
III-V WIRES, TUBES AND FIN STRUCTURES**

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SCHOOL OF PHYSICAL AND MATHEMATICAL SCIENCES

2014

Transport Studies in Quasi One-Dimensional III-V Wires, Tubes, and Fin Structures

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirements for the degree of Doctor of Philosophy

2014

Acknowledgements

In the first place, I would like to express my great thanks of gratitude to my supervisor Asst. Prof. Cesare Soci and my mentor Asst. Prof. Shadi A. Dayeh, for their abundant support, continuous encouragement and invaluable guidance over the past three and a half years. With the great help and support of Prof. Soci, I had a chance to start my Ph.D. in Nanyang Technological University doing research on III-V nanoscale materials in his group, which for me was the first time to tackle real research problems and conduct experiments independently. Thanks to Prof. Soci's patient, insightful guidance, I learnt the serious, rigorous, and optimistic attitude of doing research, which also influenced my view of life. I also had a chance to do part of my research work in the U.S.A. under supervision of Prof. Shadi Dayeh. I feel lucky to have had the opportunity to work with Prof. Dayeh at the Center for Integrated Nanotechnologies (CINT) in the Los Alamos National Lab, during which I learned a lot about electronic devices. It was an awesome experience working with Prof. Shadi and I will always remember discussing our experimental plans when driving up to Los Alamos. All in all, I really appreciate their patience, guidance, friendship and discussions in both my research work and daily life.

Special thanks also to Dr. Alexandre Larrue and Dr. Vaithianathan Veeramuthu, who accompanied me in this journey and trained me in the use of various experimental equipment during my years in Singapore. They introduced me to the use of advanced equipment and aroused my interests in crystal growth and device fabrication. Again, thanks for their patient help and encouragements. I thank Assoc. Prof. Haibin Su for his guidance and discussion in theoretical modeling. I appreciate Asst. Prof. Yizhong Huang for his help with TEM studies. I thank all my colleagues in the Optical Spectroscopy of Nanomaterials (OSON) group, Dr.

Nan Meng, Dr. Sen Zhang, Dr. Christophe Couteau, Dr. Aurelien Olivier, Zilong Wang, Majid Panahandeh Fard, Christophe Wilhelm, Jun Yin, Manoj Kumar, Xinyu Chin, Paola Lova and Charles Altuzarra. I feel so honored to have been able to work with them. I would also like to thank students of my batch in PAP, especially Cao Guan, for his optimistic mindset and moments sharing.

I am also extremely grateful for Dr. Binh-Minh Nguyen, Dr. Yoontae Hwang and Dr. Wei Tang, Dr. John Nogan, Dr. Yongqiang Wang from CINT. They have been a treasure for me throughout my stay in New Mexico and helped me a lot with equipment training, process detail discussion besides the enjoyable time out of the experiments. I also appreciate those useful discussions and insightful comments from Prof. S.S. Lau at UC San Diego.

Finally, I would like to show deep appreciation to my mother for her encouragement and full support. She is the one who loves, cares, sacrifices, encourages and trusts me no matter what decision I take. At the same time, I am thankful to Yuxin Hu and Yi Zheng for their continuous friendship, from the time we graduated from Sichuan University to when we came to Singapore. Thanks for your encouragement and supports in the fulfillment of my Ph.D. degree.

This list cannot include everyone who helped me during these years and to whom I would like to show appreciation for. Thank you all even if you are not mentioned above.

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Symbols and Abbreviations

ALD	Atomic layer deposition
BOE	Buffer oxide etchant
CBE	Chemical beam epitaxy
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
DIBL	Drain induced barrier lowering
DOS	Density of states
EBL	Electron beam lithography
ELO	Epitaxial lift-off
EOT	Equivalent oxide thickness
FET	Field effect transistor
FFT	Fast fourier transform
HRTEM	High resolution transmission electron microscopy
HEMT	High electron mobility transistor
ICP-RIE	Inductively coupled plasma reactive ion etching
ITRS	International technology roadmap for semiconductors
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapor deposition
MOSFET	Metal oxide semiconductor field effect transistor
MSM	Metal-semiconductor-metal
NWFET	Nanowire field effect transistor
PECVD	Plasma-enhanced chemical vapor deposition

PLA	Pulse laser ablation
SAG	Selective-area growth
SCE	Short channel effect
SEM	Scanning electron microscopy
SIMS	Secondary Ion Mass Spectrometry
SN-SF	Surface nucleated stacking faults
SRIM	Stopping and range of ions in matter
SS^{-1}	Inverse subthreshold swing
TB	Twin boundary
TBP	Tertiary-butyl-phosphine
TDMAH	Tetrakis(dimethylamino)hafnium
TmIn	Trimethyl-indium
TSMC	Taiwan semiconductor manufacturing company
VLS	Vapor-liquid-solid
VS	Vapor-solid
WZ	Wurtzite
ZB	Zinc-blende
μ PL	Micro-photoluminescence
2DEG	Two-dimensional electron gas
2DET	Two-dimensional electron tube

Abstract

The semiconductor industry is one of the fastest-growing market segments in the world. To overcome the bottleneck encountered in downscaling Si-based technology, introduction of alternative materials and low-dimensional systems are highly demanded. III-V compound semiconductors promise a great potential for (opto)electronics, owing to intrinsic properties such as high electron mobility and direct bandgap, as well as the ability to build complex functional heterostructures for bandgap engineering. Both bottom-up synthesis and top-down fabrication allow the development of one-dimensional systems such as single nanowires, nanowire junctions, nanowire heterostructures and Fin structures, which offer new degrees of freedom for the design of transport properties. We discuss fundamental issues related to material synthesis, surface state control, carrier transport, and heterogeneous integration of quasi one-dimensional III-V compounds in unconventional geometries, toward their application in highly integrated electronic and light detecting devices.

Chapter 1 Introduction

1.1 Background and motivations

The demonstration of transistor amplification by John Bardeen, William Shockley and Walter Brattain, Nobel laureates in Physics in 1956 for this discovery, is considered as one of the major breakthroughs of the 20th century and constitute the starting point of the golden age of modern electronics.¹ The Metal Oxide Semiconductor Field Effect Transistor (MOSFET), one heir of the original transistor, was first experimentally demonstrated at the Bells labs and quickly became the one and almost only building block for digital integrated electronic circuits.² For decades, silicon MOSFETs have been the spearhead of the semiconductor industry. Its unrivaled characteristics and ability to be integrated at a large scale to form different logic functions were the founding features of the well-known Complementary Metal Oxide Semiconductor (CMOS) technology.³ This has been further developed in consumer electronics including flat panel displays, optical scanners and CMOS image sensors,⁴ to name just a few. The commercial and industrial success of the CMOS technology has been fueled by the continuous scaling and concurrent improvements of the MOSFET device performance according to Moore's law which predicts that chip size reduces by half every one and half years and their frequency doubles.⁵ However, this historical rapid and exciting advancement has recently slowed down and now faces significant hurdles due to saturation of device performance where smaller is no longer better and due to challenges and costs of lithography tools at sub 20 nm dimensions.^{6, 7} Novel approaches in the device design as well as new channel materials that can outperform Si are in urgent need to overcome this barrier. The emergence of advanced functional materials different from the Si-based channel material combined with the introduction of new low-

dimensional systems (such as nanowires) is now inevitable to sustain the More-than-Moore trend, that is the integration of new functionality into the fundamental CMOS chips, so that transistors can be further scaled, faster, and power efficient.^{8,9}

III-V compound semiconductors on the other hand have a huge market and demand in widely spread optoelectronic devices such as lasers, light-emitting diodes and photodetectors, as well as very high speed electronics for radar, satellite and military applications approaching switching frequencies in the THz regime.¹⁰ The III-V compound semiconductors however have not been utilized as the sole channel material for digital electronics, and with their demonstrated history of robust superior performance than any other channel material available today have recently regained substantial interest as replacement channel material. Significant efforts as well are directed toward heterointegrated photonics components within the CMOS platform, which are now clear trends in the microelectronic technology roadmap.^{11, 12} These developments are also accompanied by emergent potential of low-dimensional structures to play a critical role in future technology nodes.¹³

The introduction of new materials, architectures and concepts are not without risks. The implementation of III-V low-dimensional systems involves major developments and efforts in terms of material synthesis, control of their surface and interfacial properties, preserving their superior carrier transport characteristics, and the ease of their integration to the silicon fabrication mainstream. The work presented in this thesis aims at addressing some of these important challenges in microelectronics, by focusing on fundamental crystallographic and transport properties of unusual low-dimensional III-V systems. These include (i) one-dimensional nanowire crystal growth and their self-assembly, (ii) carrier transport in quasi-one-dimensional wires, (iii) photodetection aided by charge separation and

transport in a two-dimensional electron gas tube, and (iv) three-dimensional gate control in a III-V Fin structure on Si. Despite differences in fabrication methods and geometries, such structures present common issues and advantages: interestingly, they offer new degrees of freedom for the design of transport properties by tailoring density-of-states and bandgap engineering through size and composition, and when integrated on Si bring in the advantages of high carrier mobility, direct bandgap for light emission and absorption and the benefits of heterostructure design for devices; more advantages will be added by scaling down to low-dimensional architectures like for instance an enhanced carrier mobility relative to bulk systems; however, an improved understanding during the complex synthesis of such nanomaterial and a better control of their intrinsic optoelectronic properties are required.¹⁴

Compared to 0D systems in which carriers are completely confined and transport is inhibited without implementation of extremely complicated contacts schemes, or 2D systems where carriers are free to move in a plane but without a geometrically imposed directionality, 1D systems (e.g. nanowires and nanotubes) combine both advantages of directional carrier transport and effectiveness in contact fabrication, allowing exploration of intrinsic characteristics of low-dimensional materials and their integration with mainstream circuitry platform. This has been recognized by the International Technology Roadmap for Semiconductors (ITRS) since 2003 when nanowires and nanotubes were first introduced as “emerging research devices”.¹⁴ Despite their clear advantages, several issues are presented for realizing CMOS in 1D systems, including high density of surface states that impairs performance and radial confinement of both carriers, that affect carrier recombination for minority carrier based devices. On one hand, nanowire device performance is extensively influenced by the presence of surface states (which are charged centers in the bandgap that

can screen gate potential and trap carriers in the context of CMOS devices) due to inherent large surface-to-volume ratio. These obstacles demand the introduction of proper passivation schemes such as chemical treatment or radial heterostructure growth to alleviate their detrimental impact. On the other hand, spatial confinement in the lateral nanowire direction generally increases carrier recombination rates due to the overlap between electron and hole wavefunctions in quantum-confined systems, which degrades the performance of minority carrier based devices including bipolar junction transistors, photodetectors, etc. As a result, the design of semiconductive channels which provide efficient charge carrier transport and slow recombination rates requires either electrostatic control of accumulation layers by means of effective gating mechanisms (e.g. nanowire field-effect transistors with gate-all-around configuration), or heterostructure engineering to create spatial separation of electrons and holes and increase carrier lifetime (e.g. in nanowire photodetector applications).

In view of the large-scale heterogeneous integration of III-V 1D systems to the mainstream Si CMOS platform, one can adopt either bottom-up or top-down approaches, with corresponding advantages and disadvantages: bottom-up nanowire growth allows direct integration of III-V single crystal compounds on Si, but has still limitations in terms of material quality and nanowire achievable density, and it requires fabrication of 3D device structures (e.g. vertical wrap-around gate nanowire FETs) which are not easily implemented within conventional planar fabrication. Conversely, top-down heterointegration of III-V nanostructures on Si requires first complex pseudomorphic growth of thin-films or low-yield wafer bonding approaches and then advanced multi-step processing and high-resolution lithography.

1.2 Aims and implementation

In this thesis, several types of 1D systems are investigated, including single nanowires, nanowire junctions, core-shell nanowires and Fin structures. Comparative studies of advantages/disadvantages of bottom-up and top-down approaches are performed for the design and enhancement of carrier transport in 1D functional devices such as FETs, photodetectors, etc.

We first present our studies on the optimization of bottom-up synthesis of III-V binary compound nanowires (GaAs, InAs and InP) by Metal Organic Chemical Vapor Deposition (MOCVD). The impact of relevant growth parameters (such as growth temperature, V/III ratio, catalyst diameter, growth time, etc.) on nanowire morphology, crystal structure, crystallographic defects, impurity incorporation, and geometry were investigated. These studies were aimed at improving the understanding of the physical mechanisms behind self-assembly of defect-free single crystal nanowires by the vapor-liquid-solid (VLS) growth mechanism, and served as a basis for studies of transport characteristics in ideal quasi-one-dimensional systems. Besides transport in conventional 1D single channels, there's been significant interest in studying self-assembly of complex nanowire architectures toward controlled 3D integration and possibly the implementation of quantum transport in multi-channel devices which enable control of electronic modes similar to optical waveguides.¹⁵ Conventional approaches to achieve nanowire junctions rely on multistep seed reloading growth,¹⁶ while we have identified here a new strategy which allows the self-assembly of single-crystal GaAs monolithic nanowire junction with low defect density. Transmission electron microscopy was employed to understand the formation mechanisms and the crystallographic properties of these monolithic junctions. A model was proposed to

explain the junction formation based on the energy balance between the electrostatic energy from the interaction of polar surfaces and the mechanical energy required to bend the nanowires to the point of contact. We argued that implementation of free-standing nanowire junctions with nearly single crystal structure provides a unique system for the study of mesoscopic physics. Preliminary transport measurements demonstrate electrical conductivity across the three branches of the monolithic junction and electrostatic control of the conductance of individual transport channels in a branch by external biasing of the others, which may lead to the implementation of electron waveguide Y-junction switches,^{15, 17} nonlinear ballistic junctions,^{18, 19} and phase difference detection of input electrical signal.²⁰

Understanding and control of the VLS growth mechanism of III-V binary nanowire compounds was then exploited for the design and growth of complex core-shell nanowire heterostructures. As a proof of principle, we demonstrated controlled growth of heterostructures in the GaAs/AlGaAs alloys and their application in nanowire photodetector devices with high responsivity at room temperature. We fabricated a metal-semiconductor-metal contact on a core-shell nanowire where a wide bandgap AlGaAs shell grown on a narrower bandgap GaAs nanowire core forms a type-I heterostructure that effectively decreases surface state density and enables selective confinement of electrons into a two-dimensional tube at the heterointerface. Built-in electric fields at the semiconductor heterointerface and metal/semiconductor Schottky contact interface promote photogenerated charge separation and thus enhance the photodetectivity. The photocurrent spectrum suggests that the nanowire supports resonant optical modes in the near-infrared region, which leads to a strong photoconductive response, in agreement with the photocurrent amplitude predicted by transport modeling.

Finally, we explored the top-down approach to integrate 1D III-V transport channels on Si and demonstrated the first InGaAs FinFETs on Si substrates. Large-scale, high-quality III-V layers are transferred to Si substrates in a fab-compatible process through wafer bonding based on formation of a robust nickel-silicide (NiSi) bonding interface, which overcomes drawbacks of bottom-up growth of nanowire channels such as low fabrication yield, inefficient heterogeneous integration, and incompatibility with planar technology. Using these high quality transferred layers to Si, we fabricated a tri-gate FinFET devices, where these 1D III-V channels are gated from three-sides to achieve full electrostatic control and significant efforts were paid for passivation of surface damage induced by the etching. Such structures yield excellent transistor characteristics, in line with Si FinFET device architectures currently in production. In our work we demonstrated a novel bonding scheme for heterogeneous integration of III-V films on Si and investigated the transport characteristics of III-V FinFETs on the Si platform. To the best of our knowledge this is the first time that such devices have been realized on Si. Optimization of FinFETs on Si was performed by systematic investigation of a broad range of channel lengths and Fin perimeters.

Overall, this thesis work brings about a discussion on next-generation low-dimensional III-V systems of nanowires, nanowire junctions, core-shell nanowires and Fin structures obtained by different synthesis/fabrication techniques, and the challenges related to their implementation in large-scale integrated systems. Comparative studies highlight common issues of carrier transport in such structures, namely potential effects of crystallographic defects on charge transport, high density of surface states which are commonly responsible for channel depletion, and increased charge recombination rates due to confinement effects which degrade performance of optoelectronic devices. Strategies to

effectively overcome these issues and optimize device characteristics have also been identified, including the optimal growth parameters to improve uniformity and reduce defect density in MOCVD growth of various III-V nanowire compounds, surface passivation by radial overgrowth or chemical treatments, and formation of radial heterostructures or selective contacts to engineer carrier distribution and transport along the 1D channel and control recombination rates. To validate these strategies on device performance, we fabricated various types of nanowire devices such as Y-junction rheostats, core-multishell photodetectors and tri-gate transistors, which in few respects show superior performance and characteristics than their conventional planar counterparts. Furthermore, the new scheme we proposed to fabricate heterogeneous 1D III-V channels on Si proves compatibility of such devices (with unconventional 1D channel geometries) with conventional large-scale technologies, and feasibility of their industrial manufacturing.

1.3 Thesis structure and organization

This thesis is organized as follows: Chapter 2 briefly introduces the emerging properties of low-dimensional system and their application in (opto)electronic devices; Chapter 3 investigates common issues (high-density of surface states, increased carrier recombination rate led by confinement) existed in transport study of III-V nanowires that can be solved through growth parameter tuning in bottom-up synthesis; Chapter 4 describes the self-assembly of nanowire monolithic junctions (based on energy balance between the electrostatic energy from the interaction of polar surfaces and the mechanical energy required to bend the nanowires to the point of contact) providing a platform for research on

fundamental mesoscopic physics; Chapter 5 demonstrates an efficient core-shell GaAs/AlGaAs nanowire photodetector (spatial carrier separation together with MSM contact configuration) operating at room temperature; Chapter 6 reports the first InGaAs FinFETs on insulator on Si fabricated in a fab-compatible process showing excellent transfer characteristics; Chapter 7 concludes the thesis and lists perspective research directions motivated by my Ph.D. research.

Chapter 2 Transport in quasi-1D structures

2.1 Low-dimensional systems

The semiconductor industry is one of the fastest-growing market segments in the world. It was predicted by the international data corporation that the worldwide semiconductor revenue will improve to \$336 billion in 2014 and reach \$384 billion in 2018,²¹ which develops in the creed of smaller, faster and cheaper. Semiconductor devices including diodes, transistors, solar cells, photodetectors, rectifiers, sensors, etc., form now an exhaustive toolbox and constitute the foundation of modern (opto)electronics in most daily life objects such as computers, cell phones, fiber optic communications, broadband wireless, satellite communications, space, and radar.¹⁰ FETs play a crucial role in digital and analog integrated circuits. The scaling of FETs follows Moore's Law, which predicts that the number of transistors in integrated circuits doubles approximately every 18 months. Companies, including Intel, Taiwan Semiconductor Manufacturing Company (TSMC), and Samsung, among others have now sub-22 nm technology node and 3D transistors production. The 14 nm node is expected to be in production in 2014 and the 5 nm node in 2019.^{22, 23} With the continuous transistor size shrinking, it is imperative to achieve a complete physical understanding and control of the carrier distribution and their transport in the low-dimensional systems. On the other hand, photonics has been proposed in data communication to overcome the interconnect bottleneck originated from the fast growing demands in electronics for data processing. Thanks to their direct bandgap and the broad spectral range available by bandgap engineering, III-V materials are the best candidates for the design and fabrication of photonic active devices, such as photodetectors, light sources, etc. To combine the advantages of III-V materials for photonic applications with the strength of CMOS

technology, one needs to develop a wafer-scale technology that allows the implementation of photonic circuits based on the integration of III-V on Si. Intensive efforts have been devoted by chipmakers and microelectronics foundries to develop reliable technological building blocks mixing both the tremendous promises of III-V materials with the robustness of the silicon technology, and to assemble them together to make possible optical data transmission in data center for instance with a high bandwidth and large power efficiency at low cost. Recently, the microelectronics industry leader Intel has demonstrated the first 100 Gbps transmitter based on silicon photonics.²⁴ Combining the low cost fabrication of silicon photonic chip including hybrid laser sources, modulators and photodetectors, with low cost packaging and assembly with other platforms, Intel has demonstrated the possibility to develop integrated photonic solution for a variety of applications and markets. IBM is also pursuing upstream research towards this goal by being ambitious: the localized growth of defect free 1D dimensional III-V systems on Silicon compatible with the current 3D integration trend for CMOS scaling.²⁵ On top of their perfect crystalline qualities, such 1D low dimensional systems present novel physical phenomena compared to conventional 2D counterparts that are widely used in microelectronic of photonic devices.

New physics emerges at nanoscale dimensions. The key parameter used to characterize the carrier density in a semiconductor is the density of states (DOS), which describes the number of electronic states per unit volume per energy interval that is available for the carriers in the momentum k -space. In a semiconductor material, the density of states can be evaluated for the electrons in the conduction band and the holes in the valence band, which are highly dependent of the dimensionality of the semiconductor structure. Indeed, the DOS in a 3D bulk semiconductor continuously increases with energy since carriers are free

to move in all directions; in 3D systems the DOS has a square root dependence on energy, as illustrated in Figure 2.1e. By reducing the dimensionality to 2D, such as in a quantum well, the energy in the direction perpendicular to the heterostructure becomes quantized. The states perpendicular to the well are organized as discrete subbands and the DOS has a step-like dependence on energy, where each subband represents the set of electronic states within the same quantized state (Figure 2.1f). Further confinement is added in 1D and 0D systems, leading to the appearance of strong discontinuities (van Hove singularities) in the DOS (Figure 2.1g-h). Since the DOS determines electron and hole concentrations at a given energy, such discontinuities strongly affect the transport properties (carrier density and distribution) in low-dimensional electronic devices, such as nanowire FETs. Moreover, in optoelectronic devices such as nanowire photodetectors, the joint DOS between conduction and valence bands determines interband dipole transitions. Combined with the high surface-to-volume ratio, the absorption properties are expected to be enhanced in low-dimensional materials.

Dimensionality has also dramatic effects on the actual motion of charge carriers and their transport in mesoscopic devices. In homogeneous 3D bulk systems, carriers drift and diffuse in all directions without being constrained (Figure 2.1a), which is usually described by the Boltzmann transport equation when the structure dimension is larger than the carrier mean free path. As the dimension of the device decreases, motion of carriers is restricted by the confining potential barriers that can impose new boundary conditions for carrier transport. Tunneling becomes a relevant transport mechanism across these barriers, as in a quantum mechanical description carriers have finite probability to overcome thin potential walls and propagate into the adjacent regions. In 2D systems such as quantum wells, graphene, or two-dimensional electron gases (2DEGs), where carriers are forced to move in a thin two

dimensional slab, scattering is generally reduced and techniques such as remote doping (ionized donors in the barrier layers provide free electrons in the 2D active layer) can also be employed to reduce scattering centers and significantly enhance carrier mobility (Figure 2.1b). Although tremendous achievements were obtained in 2D systems, such as HEMT devices, lots of works have been devoted to the investigation of transport models of 2D systems; for instance, 2DEG are used in HEMT devices, where carriers are able to travel at high mobility in two directions. To go one step further, lower dimensional system seems crucial to better control the optoelectronic properties of the nanomaterial towards the fabrication of reliable integrated device presenting a small footprint. Oddly, history shows that 0D systems have been considered before their 1D counterparts. Research has been conducted to exploit 0D system (quantum dots) with high Van Hove singularity and discontinuity of DOS to improve the absorption, or to tune the emission wavelength only by changing the morphology of the quantum dots. The complete quantization of the electronic state distribution in quantum dot also leads to the occurrence of Coulomb blockade and conductance oscillations.²⁶ Such phenomena, however, are extremely difficult to observe experimentally, and generally this is achieved by split-gate contacts defined on 2DEG, seldom in free-standing quantum dots due to the technical hurdle to make electrical contacts to such small regions.²⁷ Moreover, the non-homogeneity between every single quantum dots and difficulties in precisely controlling their position degrade the prevalence of this system. 1D structures such as semiconductor nanowires, carbon nanotubes and quantum wires are now emerging as a robust platform to study and exploit transport in low-dimensional channels. Nanowires are unique systems where carrier transport can only occur in one dimension (Figure 2.1c). The electronic states density and population can be efficiently

solved by self-consistent Schrödinger-Poisson equations. Thanks to the shrinkage of device dimensions to a range that is smaller than the carrier mean free path, carriers can even move across the active region without scattering (ballistic transport), resulting in a high and constant conductance independent of the channel length.

Figure 2.1 (a) 3D bulk material with continuous energy spectrum. (b) 2D structures such as quantum wells, where electrons are confined in the z-direction but free to move in the x-y plane, present discrete electronic state spectra in the z-direction. (c) Quasi 1D structures (semiconductor nanowires, carbon nanotubes, etc.) confine carriers in the y- and z- directions, but let them free to travel in the x-direction. (d) 0D systems (quantum dots) show carrier confinement and discrete energy levels in all directions. (e)-(h) Density of states of 3D, 2D, 1D and 0D systems.

Nanowires are recently treated as unique quantum systems to study mesoscopic physics, for instance the occurrence of Majorana fermions,^{28, 29} ballistic transport,³⁰⁻³² Coulomb blockade in quantum dots in wires,^{33, 34} etc. where the 1D channel configuration facilitates electrical contacts and integration. We argue that the 1D system will play a major role in optoelectronic devices of the next generation and will be soon be adopted by the semiconductor industry. Therefore we focus on engineering and designing transport properties in 1D structure, through fundamental studies of band structure, optical

confinement, electrical contacts, surface states, spatial separation of carriers as well as electrical study required by the semiconductor industry. In addition, the characteristics of 1D system (nanowires), i.e. large surface-to-volume ratio and small diameter, promote the strain relaxation and reduce the lattice matching requirement that exist in conventional thin films growth, lowering the barriers in direct heterointegration in addition to more established flip chip and hybrid bonding technologies.

Aforementioned 1D structure can be assembled through either top-down technology or bottom-up synthesis. Top-down technique is the advanced traditional approach used in industrial production line, where lithographical process is added to define the structures, followed by either wet or dry etching. Although the pitch of top-down process is limited by resolution of lithography, researchers are working on pushing the limitation of this approach well below 30 nm. While fewer varieties of complex heterostructure can be conveyed by top-down technique compared to bottom-up synthesis, high throughput ensures that top-down process has been and will be the dominant process in semiconductor manufacturing. On the other hand, instead of removing materials to make structures, bottom-up synthesis is resembled by the atomic layer by atomic layer growth to create structures. This highly controllable method enables the self-assembly of low-dimensional structures with a single crystallographic phase, allowing the fundamental study on atomic scale and development in future scalable technologies. For example, nanowires are currently the most interesting and controlled bottom-up assembled systems that allow the precise control in terms of morphology, crystal structure, doping, and bandgap engineering. In general, both top-down and bottom-up methods are essential components in the semiconductor research, accompanied with a trade-off between manufacturing cost and size, as well as the quality of

the structure. Although top-down methods are more established, it is foreseen that to fulfill the More-than-Moore requirements, functional low-dimensional devices based on complex self-assembled architectures will eventually be introduced in some semiconductor applications for surface passivation, carrier spatial separation, etc. Both schemes have their advantages and disadvantages which at the R&D stage can be used as one deems they fit to synthesize low-dimensional systems with great quality at high yield.

In this thesis we focus on the study of engineering and designing carrier transport in 1D systems such as single nanowires, nanowire junctions, core-shell nanowires and Fin structures toward the application in transistors, photodetectors, and quantum transport devices. In the following we review the state-of-the-art and the principle of operations of nanowire FETs, FinFETs, photodetectors and quantum junctions with specific emphasis on the relationship between channel geometry and carrier transport, and effects of surface states, heterostructures, and contact/gating configurations on light absorption, charge separation, transport and extraction.

2.2 Application of one-dimensional structures

2.2.1 Transistors (Nanowire FET, FinFET devices)

Silicon transistors have reduced in size by over a million times since their invention in the late 40's. Their operation speed increased by over a billion times thanks to the progress in the fabrication processes and the recent advancements in strain engineering,³⁵ innovative metal gate stack and high-k dielectrics,³⁶ and transistor architecture.³⁷ The development of Si multi-gate 3D device topology is commonly adopted in the current mainstream CMOS technology and is predicted to remain in Si down to the 10 nm technology node, where

alternative channel materials with higher mobility will be required. Figure 2.2 shows the most recent equivalent scaling process of CMOS devices presented in the ITRS. Gate materials, channel materials, and device structures constitute the three main categories in this chart. In each category, progressive technological solutions are proposed to improve the FET characteristics. The equivalent oxide thickness (EOT) is required to be scaled below 0.7 nm when the 10 nm node is reached, which imposes an introduction of a newer higher-k dielectric together with appropriate metal gates. Since the solution involving the stress engineering in conventional Si technology cannot satisfy the higher-speed requirement, alternative materials have been proposed, such as InGaAs and Ge. Compared to Si, III-V materials possess a higher electron mobility, a lower effective mass and a smaller bandgap while Ge owns higher hole mobility. These interesting intrinsic features make them suitable for high-speed logic devices. Since device dimension keeps scaling down, a first-class electrostatic gate control over the channel has become mandatory. As a result, planar FET devices gain one dimension and are evolving to 3D devices with multi-gate configurations, which offers better electrostatic control in terms of on/off current ratio, transconductance, inverse subthreshold slope (SS^{-1}) and short channel effect (SCE). Nanowire field effect transistors (NWFETs) and FinFETs have been identified to be among the best candidates for the future technological node since their intrinsic characteristics arising from their geometry fulfill the CMOS platform requirements.

Figure 2.2 2012 ITRS equivalent scaling process technologies. Adapted from Ref. 38.

Semiconductor nanowires, synthesized from bottom-up technique, offer a degree of freedom towards the 3D integration framework since a full electrostatic control of the conducting channel can be achieved through Ω -shaped gate or wrap-around gate configurations. Fabrication and performance of III-V NWFETs of horizontally dispersed nanowires, as-grown planar nanowires, and vertical nanowire array with surrounding gates will be reviewed and constitute the starting point of this work. Intensive investigations have been carried out on InAs,³⁹⁻⁴³ GaAs,⁴⁴ InP,⁴⁵ InSb,⁴⁶ InAs/InP,⁴⁷ InAs/InAsP⁴⁸ dispersed nanowire FETs. Among the numerous choice of III-V materials, InAs is particularly attractive due to its quite high mobility at room temperature and inherent surface Fermi-level pinning in the conduction band, which allows the formation of n-type ohmic contacts on the surface electron accumulation layer. Dayeh *et al.* performed a systematic study on InAs NWFET regarding impact of surface states,^{49, 50} carrier mobility,³⁹ field dependent

transport,⁵¹ diameter dependence,⁵² and crystal structure, on transistor performance.⁵³ In addition, vertical III-V NWFETs on III-V substrate^{54, 55} and Si substrate⁵⁶⁻⁵⁹ with wrap around gate topology further improve the gate controllability, efficiently suppress the SCE and enables the heterogeneous integration. The first InAs vertical NWFET on an InAs substrate formed by a complicated three dimensional device fabrication process was reported in 2005,⁶⁰ which opens new schemes for future heteroepitaxial integration of SA-grown InAs⁵⁴⁻⁵⁷ and InGaAs^{58, 59} NWFET on the Si platform. This type of structure provides a route to increasing transconductance and motivates future advanced work.

FinFET, obtained within the top-down process framework, is the other candidate for high performance electronic devices. FinFET takes its name from the shape of the active channel resembling a vertical, three-dimensional Fin, which is wrapped with a conformal controlling gate around the three sides. It has been first proposed in 1989⁶¹ and developed successfully on Si CMOS platform.^{37, 62-64} FinFET is a mainstream technology implemented in industry nowadays. In 2012, Intel reported its first 22 nm FinFET on bulk silicon, with the intention of implementing the Xeon processors for servers. Intel claimed that the 22 nm process could either increase 37% more speed at the same voltage as their 32 nm planar transistor counterpart or maintain the same performance while using less than 50 % of the existing power. IBM, on the other hand, is working on SOI FinFET but has not yet implemented the FinFET technology to their 22 nm node. Recently, TSMC announced the validation of reference flows for 16 nm FinFET processes and use the ARM Cortex-A15 multicore processor as a validation vehicle as a final certification.⁶⁵ III-V materials have recently been introduced in the FinFET design configuration to achieve higher mobility devices. Specific attentions have been paid on the III-V material ($\text{In}_x\text{Ga}_{1-x}\text{As}$) composition,⁶⁶

high-k dielectric category, thickness and interface quality,⁶⁷ S/D doping through implantation,⁶⁸ and channel structure design.⁶⁹ Table 2.1 presents the dimensions and the performance of representative non-planar III-V transistors fabricated through top-down process. Excellent device performances (lowest $SS^{-1}=63$ mV/dec and lowest $DIBL=7$ mV/V) were achieved and demonstrate the superiority of III-V materials compared to their mainstream Si counterparts and the feasibility of implementing in the next generation low-power high-speed logic devices. However, most of the FinFETs and gate-all-around (GAA) structures have been demonstrated on their original III-V substrates to date, which is not fully compatible with the well-established Si CMOS technology. Therefore, the large-scale heterogeneous integration of III-V on Si substrates is highly desired, where one can combine the advantages of III-V devices (FETs, photovoltaics, LEDs, etc) with the conventional Si platform.

Table 2.1 Performance benchmark of typical top-down non-planar InGaAs FETs.

$\text{In}_x\text{Ga}_{1-x}\text{As}$ (x)	Structure	L_g (nm)	$W_{\text{Fin/NW}}$ (nm)	Dielectric	SS^{-1} ($V_{\text{DS}}=0.05\text{V}$) (mV/dec)	DIBL (mV/V)	Ref.
0.53	FinFET	100	40	5 nm Al_2O_3	145	180	2009 Purdue ⁷⁰
0.53	Tri-gate FET	60	40	High-k stack EOT=1.2 nm	66	65	2011 Intel ⁷¹
0.7	FinFET	130	220	19 nm HfAlO	135	230	2011 NUS ⁷²
0.65	GAA	20	20	$\text{Al}_2\text{O}_3/\text{LaAlO}_3$ EOT=1.2 nm	63	7	2012 Purdue ⁶⁷
0.53	GWA	140	40	7 nm Al_2O_3	80	20	2012 Austin ⁷³
0.53	FinFET	50	80	$\text{HfO}_2/\text{Al}_2\text{O}_3$ EOT= ~ 1 nm	150	-	2013 NUS ⁷⁴

2.2.2 Photodetectors

The inherent large surface-to-volume ratio of nanowires promises an enhanced sensitivity to light compared to the conventional planar thin films. This interesting feature arising from the quasi-1D geometry of nanowires opens new opportunities in the design of photodetectors and photovoltaics, optical switches and even novel approach for optical interconnects.⁷⁵⁻⁸⁰ The photoconductivity which characterizes the variation of electrical conductivity under light illumination is composed of three distinct successive physical mechanisms: the absorption of light, the photogeneration of carriers, and the carrier transport. The combinations of the device geometries and architectures (radial or axial heterojunction, Schottky or ohmic contact, vertical array or dispersed nanowire, etc.), the bandgap of the nanowire material (optical absorption wavelength), and the carriers mobility and lifetime (affected by the carrier density, traps, and surface states) determine the photoconductive gain and the response time, which are two key parameters evaluating the photodetector performance. The increased influence of surface states in this quasi 1D nanostructure affects the device performance by acting as nonradiative carrier traps and inducing a surface Fermi energy pinning that can impair the performance of other important functional components of the photodetector such as the carrier-extracting contacts. GaAs nanowires,⁸¹ as well as some other semiconductor nanowires (InP,⁸¹ GaN,⁸² etc.), exhibit a surface Fermi-level pinning within the forbidden energy gap, creating thus a space charge depletion layer near the surface of the nanowire, which provides a natural physical separation of the photoexcited electrons and holes. Hence, nanowires with small diameter (i.e., minimal band bending) can be fully depleted and minimize the dark current, while those with a large diameter (i.e., substantial band bending) provide a large photocurrent by preventing the photogenerated carrier to

prematurely recombine.⁸³ Nevertheless, surface-trapped charges lead to the fluctuation of the electrical potential and increased the surface recombination, deteriorating the device performance. The intensive study on the nanowire heterostructure growth mechanism and the controllability of crystallographic phases of the nanowire during the growth have enabled significant progresses in the growth of high crystalline quality core-shell nanowires with a larger bandgap material covering the surface of the nanowire core, such as type-I GaAs/AlGaAs,⁸⁴⁻⁸⁶ and type-II ZnO/ZnSe,⁸⁷ which possess the spatial confinement of the photogenerated carriers and high interface quality. The shell passivates the core nanowire surface by reducing the surface traps existing on the nanowire core and separates the electrons from holes on the coaxial interface thanks to the favorable bandedge discontinuity for such separation.

III-V nanowire direct-bandgap photodetectors can absorb the light over a wide spectral range through bandgap engineering. In 2001, Prof. Lieber's group was the first to report the measurement of photocurrent in a single InP nanowire.⁸⁸ This result inspired more advanced research works: an InP photoconductor was demonstrated with InP nanoneedles grown on non-single crystalline Si platform,⁸⁹ a photocurrent spectroscopy technique was developed to study the crystalline structure of a single InP nanowire at room temperature,⁹⁰ and a more advanced single photon detector relying on the avalanche amplification of single exciton has been achieved in InP nanowires recently.⁹¹ The photoconductive response of various nanowire architectures in the GaAs system has been also widely investigated including a single GaAs nanowire,⁹²⁻⁹⁴ GaAs p-i-n radial structure,⁹⁵ GaAs/AlGaAs core-shell,^{84, 96-100} and GaAs/InGaP/GaAs core-multishell nanowire.¹⁰¹ Growing a shell on top of the nanowire core is of the highest importance since it could passivate the core surface, thus

decreasing nonradiative carrier traps, and this was experimentally validated by the faster photoresponse of GaAs/AlGaAs core-shell nanostructure with shell-to-shell electrodes compared to a bare GaAs nanowire.⁸⁴ Apart from those aforementioned near infrared light detection (photon energy of 0.9-1.7 eV), narrow bandgap materials (such as InAs) allowed to extend the detection range to mid-infrared spectral region (photon energy of 0.15-0.4 eV). Although progresses of optoelectronics and photonics in the InAs material network have been limited by its strong Auger recombination and nonradiative surfaces, introducing an InAsP shell could effectively confine the carriers and reduce the surface recombination.^{102, 103} Furthermore, large bandgap materials based on nitrides (III-N) enable to extend the functionalities in the ultraviolet and visible spectral region. The photocurrent time responses of both vertical GaN array p-i-n axial structure on n-Si¹⁰⁴ and transferred single n-i-n GaN nanowire¹⁰⁵ were measured in the millisecond range while the one of networked GaN nanowires stays persistent and decays for more than one day.¹⁰⁶ In addition, it has been found that the photocurrent of GaN nanowires are highly dependent of their diameter, which is attributed to the different recombination barriers at the surface.⁸²

The outstanding sensitivity of nanowires to light has made them particularly interesting in the solar harvesting applications. Indeed, nanowire solar cells have attracted much interest in the past decade, especially those using III-V nanowires. An InP nanowires solar cell with an efficiency of 13.8% was recently demonstrated by designing a light trapping photonic nanowire arrays.¹⁰⁷ A single p-i-n GaAsP core-shell nanowire solar cell laying on SiO₂/Si substrate presents an overall efficiency as high as 10.2%.¹⁰⁸ In comparison, solar cell based on a p-i-n GaAs core-shell nanowire on p-Si substrate claims to boost the solar conversion efficiency to 40%, exceeded GaAs Shockley-Queisser limit.¹⁰⁹ These

remarkable efficiencies demonstrate tuning of optoelectronic properties through band gap engineering is very promising for future generation of photovoltaics.

The light sensitivity of semiconductor nanowires was also exploited to fabricate all-nanowire image sensors. Fan et al. designed an integrated nanowire image sensor with nanowire based pixel (a nanowire-based circuitry) taking advantages of both photosensitivity of CdSe nanowires and electronic properties of Si/Ge nanowires.¹¹⁰ Recently, researchers from Harvard University demonstrated a filter-free color image sensor employing vertical arrays of p-i-n Si nanowires, whose diameter determines their spectral sensitivities.¹¹¹ This method also allows wideband multispectral imaging by using other types of semiconductor nanowires such as III-V compounds.

Overall, these experimental achievements have proven the great potential of nanowires for optoelectronic devices. In particular, III-V nanowires are highly promising for high speed, light-to-current conversion efficiency, and power tolerance photodetectors in optical communication systems. However, the lack of demonstration of III-V photodetectors working at room temperature highlights the research progress that needs to be pursued to get a better understanding of what limits their performances in terms of inherent physical properties, growth of nanowires, and design of structures.

2.2.3 Nanowire junction devices

There is a growing interest in the fundamental study of complex nanoscale structures in terms of their electrical transport properties. Nanowire T- and X-junctions are among the most interesting systems that allow the research on non-linear ballistic transport in three-terminal junction devices and development of the proposed Majorana fermion braiding

devices. Thanks to their capability of ballistic transport and self-gating, nanowire junction device are theoretically expected to achieve rich functionalities.

The non-linear ballistic transport is mainly studied in nanoscale junctions fabricated through top-down approach on III-V heterostructures. It is well known that in the linear-response regime of ballistic transport electron travels in a discrete number of modes, where the conductance of the 1D constriction is quantized in the unity of $2e^2/h$ at low temperature. However, an interesting phenomenon of non-linear ballistic transport was observed in AlGaAs/InGaAs T-junction fabricated by RIE. When voltage is applied in a pull-push fashion at room temperature, V and $-V$ for the left and right branches of the junction, respectively, the output voltage from the central branch (V_c) will always be smaller than zero, see Figure 2.3a.^{19, 112} Theoretical calculation about this intriguing effect was carried out by Xu, which agrees well with the experimental behavior.¹¹³ Moreover, in the junction device works in the long diffusive region when the dimension is relatively large, similar results were found under higher bias. In this case, electron intervalley transfer increases the effective mass and induces an accumulation domain, which causes additional potential drop.¹⁸ This new phenomenon opens opportunities in device design. For instance, second-harmonic generation for microwave application could be realized on junction device because the unique property of $V_c = -\alpha V^2/2$ when pull-push input voltages are applied. Moreover, if the dc voltage applied to the left and right branches of a symmetric junction are both positive, the output central branch voltage will be positive. Thus, the devices could operate as a logic AND gate. All the studies mentioned above are based on III-V junctions fabricated through top-down technique, which limits the size of the junction and could transfer undesired surface roughness to the

final device. Instead, bottom-up synthesis is an alternative way for creating small-dimensional system with perfect crystalline structure.

Significant progress has been achieved (or realized) in the bottom-up synthesis of nanowires so that their geometrical and crystalline characteristics can be perfectly tuned during the growth. The more advanced intersected or branched nanowires have gained paramount interests thanks to their capability of realizing direct interconnection between two nanowires during the growth. Previous studies on the synthesis of nanowire junctions can be classified into two categories: multistep synthesis with the introducing of new catalysts and single-step growth through the engineering of all related conditions. The first method relies on the multistep VLS growth using the strategy of reseeded new metal catalysts (usually Au nanoparticle) on the nanowire backbone surface, which determine the diameter and the density of the branches. It can be realized in both heteroepitaxial growth of different backbone and branch materials, as demonstrated in GaN on Si,¹¹⁴ Ge, GaAs, GaP, CdSe on Si,¹¹⁵ and homogeneous growth as achieved in InAs²⁰ and GaP¹⁶ system. The possibility to form heterostructures with different doping conditions (between the branches and the bare trunk for instance) offer one more leverage in the tenability of the electronic or photonic properties of nanowire-based junctions. While the first strategy requires multi-step growth and specific techniques of catalyst attachment, the second method can avoid the introduction of an extrinsic catalyst enabling thus a more straightforward growth. Three-dimensional monolithic nanowire junctions can be synthesized using the VLS mechanism through the engineering of the orientation of the nanowire growth, the interdistance between two catalysts and the tuning of the nanowire diameter in a selective-area growth, including InAs,^{116, 117} InSb.¹¹⁸ The good crystalline quality of these junctions paves the way toward the

creation of a promising platform for low-dimensional fundamental condensed matter physics research,^{119, 120} photovoltaic application¹²¹ and biological sensors.^{115, 122}

For quantum transport study, Plissard et al. discussed the ability of horizontal InSb nanowires grown from InP/InAs stems to meet and merge into T or X junctions under specific conditions. These original junctions exhibit a high carrier mobility and an indication of supercurrent through the nanocross at low temperature (Figure 2.3b).¹¹⁸ The similar superconductive phenomenon is observed in an InSb nanowire Josephson junction, demonstrating that crossed nanowires play a vital role in topological superconducting systems such as the proposed Majorana fermion braiding devices.¹¹⁹ Low-temperature conductance measurements have also been conducted in self-assembled InAs nanowire junctions, showing similar conductance between all nanowire arms¹¹⁷ and rich nonlinear properties.²⁰ The advantages of nanowire networks go far beyond the field of mesoscopic physics. For instance, Jiang et al. applied the concept of branched heterojunctions to p-n diode, LED, FET, logic device and biosensors.¹¹⁵ Before that, Lieber's group demonstrated that an acute-angle nanoprobe made of Si nanowires can detect and record intercellular information of living cells without penetrating or damaging the cell membrane.¹²³ However, most applications of nanowire networks are limited for the large scale integration because nanowires are removed from the original substrate and randomly placed on another host substrate. As a result, a vertical array of nanowire interconnections in a deterministic manner with proper electrodes design is highly desired, as demonstrated in Dalacu et al. work,¹¹⁶ which open up new opportunities for large scale functional device integration.

Figure 2.3 (a) V_c as a function of V when biasing in push-pull fashion with different lengths: one ballistic ($L=200\text{nm}$) and one diffusive ($L=2000\text{nm}$). Image adapted from Ref. 19. (b) I - V characteristics of InSb nanocross with superconducting contacts (NbTiN/Al) at 20 mK. Contact spacings are 440 nm (A-B), 620 nm (A-C and B-C), 1300 nm (A-D and B-D) and 1480 nm (C-D). Global backgate voltages between A-C and B-C are 14.8 V (blue) and 14.4 V (black), respectively. Due to environmental shunting or self-heating, asymmetry is observed, while the kinks in the dissipative branches may be Fiske steps. Both of them are the features observed in underdamped Josephson junctions. These facts validate the possibility of implementing crossed nanowires in Majorana fermion braiding devices. Figure adapted from Ref. 118.

Chapter 3 MOCVD growth of quasi-one dimensional III-V nanowires: control of morphology, defects, surface states and heterogeneous integration

3.1 Introduction

Semiconductor nanowires are among the best candidates for large scale integration of (opto)electronic functional systems where large sensitivity,¹²⁴⁻¹²⁶ dense integration,^{127, 128} and complex polymorphic heterostructures^{127, 129-132} are desired. With the continuous demand of device performance enhancement together with the shrinkage of their footprint, III-V nanowires open up a new range of possibilities towards the engineering of innovative nanowire-based electronic and photonic applications with high carrier mobility and versatility in bandgap engineering. III-V nanowires can be obtained from both top-down and bottom-up techniques, where the latter one offers more freedom in fundamental study of nanowires with extremely small diameters, excellent surface morphology, complex structures, perfect crystallographic structure without defects, and direct integration on Silicon. Nanowire could be synthesized through bottom-up method via various techniques. Highly controllable methods include MOCVD,^{133, 134} Selective-Area (SA) growth,^{127, 135} Molecular Beam Epitaxy (MBE),¹³⁶ and Chemical Beam Epitaxy (CBE)¹³⁷; less controllable techniques contains Chemical Vapor Deposition (CVD),¹³⁸ wafer annealing,¹³⁹ pulse laser ablation (PLD),¹⁴⁰⁻¹⁴² and low temperature solution methods.^{143, 144}

Working principles of these growth techniques are different. In MOCVD, the crystalline epitaxial growth of compound semiconductors is achieved by surface reaction and deposition of pure metal organic precursors containing the desired elements. The SA growth

enables the precise positioning of the nanowire during the growth, which could be initiated by a group III catalyst (or even in absence of catalyst) on either III-V or Si substrate covered by a thin SiO₂ layer with small openings obtained through electron beam lithography patterning and wet etching. MBE growth takes place in ultra-high vacuum chamber by heating solid-source elements to gaseous elements, which condense and react with each other until they reach the sample surface. CBE is a combination of MOCVD (source phase) and MBE (with a similar transport mechanism), and the growth rate is determined by a mass-transport process (the arrival rate of the group III alkyls) at a higher substrate temperature, and is limited by the surface reaction process (surface pyrolysis rate) at lower temperatures. The differences between these three mainstream techniques are illustrated in Figure 3.1.

Figure 3.1 Growth kinetics involved in (a) conventional MBE, (b) MOCVD, and (c) CBE. Image adapted from Ref. 145.

In the presence of metal catalysts, the growth normally relies on the VLS mechanism,¹⁴⁶ originally developed in the 60s for the growth of silicon “whiskers” by Wagner and Ellis. The mechanism is based on the formation of a supersaturated alloy inside a liquid seed nanoparticle (typically Au) from gaseous precursors SiCl_4 , upon continuation of the supersaturation, the liquid droplet is displaced from the Si substrate surface and rides atop a solid Si whisker. III-V nanowire growth adds more complexity in the VLS mechanism due to the incorporation of both group-III and group-V reactants. Normally, group-III precursor decomposes and incorporates into the liquid alloy formed by the Au catalyst and the original substrate material, and then reacts with decomposed group-V precursor at the liquid-solid interface. Thus nanowire crystallizes and elongates along the low-energy $\langle 111 \rangle$ direction with the nanoparticle floating on top. To achieve growth of III-V nanowires perpendicular to the substrate surface, (111)B (group-V terminated) substrates are more favorable than (111)A (group-III terminated) substrates thanks to the fact that (111)A semiconductor surfaces can be easily oxidized, prohibiting the epitaxial growth.¹⁴⁷ Nanowire usually grows at a temperature range 100-200 °C lower than that of thin film growth. When the temperature is too low, both the formation of a nanoparticle alloy and the native oxide desorption will be hindered. If the temperature is too high, the solubility inside the catalyst alloy increased, resulting in the reduction of supersaturation, and consequently the nanowire nucleation and growth rates. The fulfillment of every optimal growth conditions leads to the achievement of a precise growth control of the nanowire morphology. In addition, in the absence of metal particles, nanowire growth can still occur, by taking advantage of different growth mechanism such as group-III catalyzed VLS growth,¹⁴⁸⁻¹⁵¹ oxide-assisted growth,¹⁵² reactive Si-assisted growth,¹⁵³ and dislocation-driven growth.¹⁵⁴

The “bottom-up” synthesis of single-crystal nanowires allows dense three-dimensional device integration, the control of doping during the synthesis, and the addition of multiple functionalities via direct axial or radial heterostructure formation. Moreover, when the physical dimensions of nanowires are reduced ($d < 10$ nm), both quantum confinement and ballistic transport effects are expected for such typical one-dimensional nanostructures. However, the reduction of the dimension involves more constraints on the fabrication process of the nanowire based devices. To this respect, a better understanding of the nanowire growth mechanism is essential for the development of a new generation of nanowire based devices offering improved performances compared to their traditional counterparts. The growth mechanisms directly determine the morphology, the crystal structure (polytypism, defects), surface states and the band diagram of the nanowire, which are correlated to its intrinsic electronic transport properties. In addition, by designing the growth condition, III-V nanowires can also be directly grown on Si. Aiming at optimization of transport properties of nanowire system, my research focused on the understanding of the growth mechanisms of various III-V nanowires grown by MOCVD, including binary compounds (GaAs, InAs and InP), core-shell nanowires, and GaAs nanowire grown on Si. Additionally, simulation and characterization of nanowire devices were also investigated. Results and discussions are presented in the following sections.

3.2 Morphology control of binary compound semiconductors

III-V binary compound semiconductor nanowires have attracted great interest towards nanodevice in photonics and high-speed electronics, where different semiconductor compounds find different application thanks to their unique intrinsic properties, e.g. band gap

and charge carrier mobility. For example, InAs nanowires are very promising for high speed nanoelectronics thanks to their high electron mobility and their ability to form low resistance ohmic contacts.⁵⁰ For photonics applications, the low bandgap energy of InAs limit the wavelength range achievable to the near infrared, while GaAs and InP nanowires are promising for application in as photovoltaics or light emitting diodes thanks to their direct bandgap in the visible and near infrared spectral range.

The distinctive applications of different III-V binary semiconductor compounds demand the development of suitable MOCVD growth recipes to enable the bottom-up synthesis of nanowires with the desired crystallographic structure and morphology, and ultimately the growth of complex heterostructures allowing the embedment of multiple functionalities on one device. Relevant growth parameters, including growth temperature, V/III ratio, diameter, and growth time, tailor the diameter, height, morphology, crystal structure, crystallographic defects and impurity incorporation of the bare nanowire. Given the strong interplay between these parameters in the nanowire self-assembly, growth conditions need to be optimized for each material compound. The following section presents the preliminary optimization studies for prototypical III-V nanowire materials, namely GaAs, InP and InAs.

GaAs nanowires can be grown in a wide range of temperature and V/III ratio combinations and their growth rate is typically linear with growth time. On the contrary, indium compound nanowires are easily influenced by small fluctuations of the growth parameters due to the long diffusion length of In adatom and efficient crystallization of In by abundant group V elements. To illustrate these points, Figure 3.2 and Figure 3.3 show the effect of changing growth temperature and V-III ratio on the growth of InP and InAs

nanowires, respectively. After studying the growth mechanisms and optimizing the growth conditions of InAs and InP nanowires, uniform and vertical nanowires were successfully achieved on InAs (111)B and InP (111)B substrates, respectively (Figure 3.2b and Figure 3.3b).

In general, precursor adatoms contribute to the growth mainly through three different absorption paths including: direct adsorption in the liquid particle, absorption from the sidewalls, or absorption from the substrate surface within the collection area. The temperature affects the rate of the precursor decomposition and the surface reaction, the adatoms diffusion length and the sticking coefficient on the nanowire sidewalls, resulting in the differences of nanowire nucleation, axial and radial growth rate. Figure 3.2 shows InP nanowire grown on InP (111)B substrate with the same V/III ratio of 61.5 at three different temperatures. At the lower growth temperature of 420 °C, nanowires show irregular shape and nucleation problems occur. When the temperature increases to 440 °C, vertical nanowires without tapering (i.e. the enlargement of the nanowire diameter toward its base due to radial deposition during the growth) are successfully obtained. However, when the temperature reaches 450 °C, nanowires begin kinking in non-vertical orientations and show pronounced tapering. This phenomenon is mainly due to the decomposition of the group V organometallic precursor (tertiary-butyl-phosphine, TBP), which starts decomposing at approximately 400 °C and undergoes a complete pyrolysis at 550°C¹⁵⁵ (for the group III precursor, trimethyl-indium, TMIIn, complete decomposition occurs at lower temperature, between 300 and 400 °C). Since approximately 10% of TBP decomposes at 420 °C, the concentration of P adatoms is insufficient to promote the growth of vertical nanowire at such low V/III ratio. When the temperature increases, the decomposition of TBP increases

significantly and straight vertical nanowires are observed at 440 °C. However, at higher temperatures, the P adatom concentration considerably increases and impacts the nanowire morphology which starts presenting kinking and tapering morphology (Figure 3.2). The Tapering effect comes from the excessive P atoms that crystallize with In atoms and prevent their diffusion from the nanowire sidewall facets or the substrate surface to the Au-In alloy. Eventually, at higher P atoms concentration, In atoms are all consumed and the excess of P atoms causes the solidification of the nanoparticle. Consequently, a kinking phenomenon may occur.

Figure 3.2 InP nanowires grown with the same V/III ratio of 61.5 at different temperatures: (a) 420 °C, (b) 440 °C, (c) 450 °C.

Another key parameter affecting the nanowire growth is the V/III ratio, which has a pronounced impact on the nanowire morphology. To investigate the dependence of the nanowire morphology regarding the V/III ratio, a set of growths of InAs nanowire were performed at 490 °C and the V/III ratio was varied while keeping a constant molar fraction of group V precursor of 2.58×10^{-4} mol/min (tertiary-butyl-arsine, TBA). For a high V/III ratio of 50 (Figure 3.3a), stable As trimers form on {111}B surfaces and crystallize the available In atoms on the substrate surface instead of those on the sidewall or in the liquid catalyst. The

depletion of In from the nanowire growth site leads to a low nucleation rate and the formation of islands under the Au nanoparticles preventing the growth of the wire.¹⁵⁶ As the V/III ratio decreased to 40, more In atoms are available, promoting the vertical, uniform nanowire growth (Figure 3.3b). However, below certain V/III ratios, the In concentration gradient between the substrate surface and the nanowire increases as In flow rate increases. At this stage, the excess of In at the base of InAs nanowire results in a radial growth and a tapering effect at the base. Furthermore, if In concentration is sufficiently high, In droplets may form near the nanowire base, acting as nucleation centers for undesirable nanowire growth in close proximity of the Au-catalyzed InAs nanowires (as shown in Figure 3.3c).¹⁵⁷ These studies not only enable the understanding of the III-V nanowire growth, but also allow the control of both their morphology and composition toward the formation of complex heterostructures.

Figure 3.3 InAs nanowires grown at the same growth temperature of 490 °C and different V/III ratios: (a) 50, (b) 40, (c) 30. The V/III ratio was varied by changing the TMI molar flow rate while keeping the TBA constant.

The tuning window of the different parameter for the growth of GaAs nanowires is wider than for In-containing nanowires. Indeed the V/III ratio does not affect the growth significantly, but higher growth temperatures result in a larger tapering. Figure 3.4a

represents typical GaAs nanowires epitaxially grown on GaAs (111)B from randomly dispersed Au nanoparticles with a 40 nm diameter, at a growth temperature of 430 °C and a V/III ratio of 14.25. In Figure 3.4b, a high-resolution transmission electron microscope (HRTEM) image of a GaAs nanowire grown with the same conditions as Figure 3.4a is presented, showing perfect zinc-blende (ZB) crystal structure.

Figure 3.4 (a) Epitaxial growth of GaAs nanowires from 40 nm diameter Au catalyst at a growth temperature of 430 °C and V/III ratio of 14.25. (b) Typical HRTEM image and FFT pattern of the GaAs nanowires in (a) shows nearly perfect ZB cubic structure.

Given the complexity of the growth mechanism and the interplay of multiple growth parameters affecting morphology, crystallographic properties (defect formation) and composition, optimization of binary III-V nanowire growth is a necessary step to synthesize material combinations for nanowire based devices such as transistors and photodetectors, and constitute a solid starting point for the growth of ternary nanowires with better performance for high-power and high-frequency electronics, long wavelength optical transmission, and integrated photonics.¹⁵⁸

3.3 Crystallographic defects in III-V nanowires

The progresses in the bottom-up III-V nanowire synthesis discussed in previous section have allowed tuning the structural quality, occurrences of random structural defects and polytypism. While vacancy, anti-site, and interstitial defects are widely investigated in III-N nanoscale system,¹⁵⁹ twin boundaries (TBs) and stacking faults (SFs) are usually considered in III-V nanostructures as main source of defects which can degrade the device performances. For example, these defects can induce a variation of charge carrier concentration and an increment of phonon scattering.¹⁶⁰ Thus, a full understanding and precise control of crystal structure by tuning growth parameters are highly demanded.

Defects are existed in both bulk and nanowire systems. Their multiplications in the bulk structures are widely explained by the mechanisms of Frank-Reed, cross-glide, climb or grain boundary-emission, while the propagation in nanowires are not fully understood. Nanowire growth is initiated by a liquid eutectic particle in a layer-to-layer fashion with the crystallographic structure determined by the interface properties which affect the driving forces for nucleation of a certain crystal phase¹⁶¹ or formation of defects.¹⁶² Thus nucleation, propagation, and interaction of defects in nanowires can be different from their bulk counterpart and remain unresolved.

3.3.1 Crystal structure from random to single phase

III-V nanowires commonly exhibit a mixture of ZB cubic structure and wurtzite (WZ) hexagonal structure in the $\langle 111 \rangle$ direction (Figure 3.5d),^{131, 163-168} while their bulk counterparts usually crystallize in ZB. The ZB structure includes the stacking of monoatomic

layers in the sequence of ...cAaBbCcA... in the $\langle 111 \rangle$ direction, whereas the WZ crystalline phase displays a stacking sequence of ...bAaBbA... in the $\langle 0001 \rangle$ direction (Figure 3.5a-b). Due to the small difference in the cohesive energy of these two structures ($\Delta_{ZB-WZ} \leq 25 \text{ meV}$),^{162, 169} polytypism is observed by the appearance of small segments of ZB in WZ when a SF misplaces an “Aa” plane with a “Cc” plane, or small WZ segments appearing in ZB after the introduction of two sequential twin planes, or a twin plane between which the ZB segment rotates 60° around the $\langle 111 \rangle$ axis from the original ZB structure.^{166, 170, 171} Other than these, a 20 to 40 nm long 4H polytype (...bAaBbCcBbA...) was observed right above the inserting ZB GaAsSb segment in the WZ GaAs nanowire¹⁷² and a 6 monolayer superlattice consisted of twinned and ZB structure was also reported as a new stacking sequence (...cAaBbCcBbAaCcA...).¹⁷³

In general, the defecting segments within the primary structure are nucleating at the triple phase contact line on the small side facets or defects, acting as a form of stored surface and interface energy release.^{174, 175} Notably, both the interface energies at the triple phase boundary and the supersaturation of the liquid seed significantly affect the nucleation process and consequently determine the definitive crystallographic phase.^{162, 176} Therefore, the preferential growth of a particular phase can be controlled by tuning relevant VLS growth parameters such as the V/III ratio, the temperature, and the nanowire radius. It is generally accepted that high supersaturation, i.e. where high growth temperature, low V/III ratio and small radii, promotes the appearance of a WZ crystalline phase.^{162, 177-179} Although III-V nanowires commonly display ZB and WZ polymorphism, pure crystallographic phases can be achieved by carefully tuning the growth conditions. Based on this, the remarkable advances in the control of the crystallographic properties of III-V nanowires by the VLS

mechanism have enabled the realization of axial periodic structures, such as polytypic superlattices made of alternating segments with different phases¹⁶⁶ or twinning superlattices formed by the repetition of segments with constant length between twin planes.

Figure 3.5 Polymorphism in III-V nanowires. Ball-and-stick model of (a) the ZB structure in the $\langle 111 \rangle$ growth direction, showing the sequence of monoatomic stacking planes ...cAaBbCc... and (b) the WZ structure in the $\langle 0001 \rangle$ growth direction with stacking plane sequence ...bAaBb... (c-e) High resolution TEM images of: (c) GaAs nanowire grown on GaAs (111)B surface. The electron diffraction pattern in the inset shows a pure ZB phase. (d) GaAs nanowire grown on Si (111) exhibiting a mixture of ZB and WZ phases. Reprinted from Ref. 163. (e) Stacking fault free GaAs nanowire displaying pure WZ phase. Reprinted with permission from Ref. 180. Reproduced from Ref. 176.

III-V nanowires with different crystal phases behave dissimilarly in their electronic transport behavior. It is reported that WZ InAs nanowires with numerous stacking faults exhibited improvement of the on/off ratio compared to pure ZB nanowires, but lower current

level,¹⁶³ which is also observed by Thelander *et al.*, where nanowires with mixture of two phases presented a higher resistivity by two orders of magnitude compared to single-phase nanowires.⁴⁰ The nonzero spontaneous polarization charges presented at the WZ/ZB interfaces suppress carrier accumulation at the nanowire surface, resulting in a full depletion of the channel. These studies pave the way for incorporating III-V nanowires into future electronic devices.

3.3.2 Defect propagation: understanding of fundamental crystallization mechanism

Semiconductor nanowire is grown in a layer-by-layer fashion seeded by a eutectic nanoparticle with its perfection determined by the interface quality. Except those well-known defect multiplication mechanisms in bulk systems, such as Frank-Reed, cross-glide, climb or grain boundary-emission, we here discovered a new phenomenon of defect propagation in nanowire growth. We observe that steps at the liquid-solid interface, resulting from surface nucleated defects (Figure 3.6a-c), causing a gradual multiplication of stacking faults in the regions bounded by two faults (Figure 3.6e-g). One can envision that as a growing layer nucleated by SF1, for example, approaches SF2 a new fault is formed within a couple atomic distances of SF2 (Figure 3.6c, f). This rocking chair multiplication mechanism is a unique feature of nanowire layer-by-layer growth.

Figure 3.6d shows a HRTEM image of a GaAs nanowire showing three surface nucleated stacking faults (SN-SFs) and a surface nucleated twin boundary (TB) illustrating this mechanism. Multiple SFs are generated in regions bounded by SFs or a SF/TB. In the first ~ 70 (111) bi-layers to the left of TB (red dashed line), there are no additional generated SFs. When SF3 emerges (green dashed line), successive nucleation of multiple SFs is

observed (green & red arrows numbered in sequence of formation). All regions bounded by SFs show a consistent behavior: SFs emerge near SF and TB and their density increases periodically toward the center of the bounded region between them.

In the postulated SF generation mechanism (Figure 3.6c and e-g) the nucleation energy for the next layer is lowest at the triple-phase intersection of the SF and nanowire surface (blue arrows in Figure 3.6b-c and stars in Figure 3.6e-g) and this leads to one additional bi-layer, above blue star in Figure 3.6e, that stacks to preserve the underlying structure. Following a nucleation event at SF1 (Figure 3.6f), fast ledge propagation on the (111) surface encounters a surface step (Figure 3.6c), resulting in formation of a new SF near SF2 (dashed red line in (c) and arrow in (f)). Random switching of nucleation between the two SFs leads to alternating generation of SFs.

This defect generation mechanism can explain the presence of dense stacking faults and lamellar twins previously observed during the growth of groups IV and III-V semiconductor nanowires. Superlattice structures along nanowire axes that are formed with such mechanism contrast those perpendicular to nanowire axes frequently found in III-V nanowires.¹³¹ In both structures, surface passivation and reduced supersaturation¹⁸¹ will allow improved growth of pure nanowire crystal phases.

Most of this section was published in Applied Physics Letters, 2012, S. A. Dayeh, X. H. Liu, X. Dai, J. Y. Huang, S. T. Picraux, C. Soci. The dissertation author is the third author of this paper.

Figure 3.6 Perspective view of nucleation and ledge flow in nanowires at their faceted surface and triple-phase boundary (a) in the absence of defects (b) at the intersection of triple-phase with stacking fault, marked by blue arrow, (c) and at triple-phase intersection with one of two stacking faults (SF2) leading to a new stacking fault (dashed red line) near SF1. (d) HRTEM image of a GaAs nanowire with three surface-nucleated stacking faults (SN-SF) and a twin boundary (TB) marked by dashed lines. In any region bounded by two SN-SFs or a SN-SF and SN-TB, a successive increase in the density of SFs (numbered ≥ 2) outgoing from these SN defects is observed. (e) Layer nucleation (blue star) at SF2 and subsequent layer growth in a nanowire with two defects. (f) Switching nucleation to SF2 and subsequent ledge propagation toward SF1 encounters a step at SF2 resulting in the generation of an additional SF (marked 2) near SN-SF2. (g) Repetition of the process in (f) leads to generation of successive SFs in between the two SN-SFs. Image adapted from Ref. 182.

3.4 Impact of surface states on carrier transport

The transport properties of nanowires are mainly determined by the nanowire growth conditions as described in the previous section, which affect their intrinsic properties, namely size, carrier concentration and surface states. A further understanding of the nanowire electronic properties will in return allow the optimization of the key growth parameters involved in the enhancement of the device performances. The increasing surface area of nanowires leads to the issue of high density of surface states, which may act as nonradiative carrier traps and induce surface Fermi energy pinning. GaAs nanowires,¹⁸³ as well as some other semiconductor nanowires (InP,¹⁸³ GaN,⁸² etc.), suffer from surface Fermi-level pinning within the forbidden band, thus a space charge depletion layer existed inside the nanowire. Consequently, nanowires with small diameter (i.e., minimal band bending) can be fully depleted and decrease the current, while those with large diameter (i.e., substantial band bending) provide large photocurrent by preventing photogenerated carrier recombination in the depletion region.¹⁸⁴ Nevertheless, surface-trapped charges lead to the potential fluctuation, deteriorating the controllable device performance.

To further investigate the impacts of surface states on nanowire transistors, Silvaco-Atlas simulation is conducted on a GaAs nanowire with 5 μm in length and 80 nm in diameter. The GaAs slab lies on a 300 nm thick SiO_2 layer with metal on the bottom acting as global backgate (inset of Figure 3.7a). In these simulations, a typical n-type doping concentration of $N_D = 5 \times 10^{16} \text{ cm}^{-3}$, ohmic source/drain contacts, and a variation of four interface charge densities $Q_f = 0, -1 \times 10^{10}, -1 \times 10^{11}, \text{ and } -1 \times 10^{12} \text{ cm}^{-2}$ to simulate surface states are assumed. Figure 3.7a displays the simulated transfer curves at $V_{DS}=0.1 \text{ V}$

for four different conditions. The transfer characteristics are similar for nanowire without interface states and with $Q_f = -1 \times 10^{10} \text{ cm}^{-2}$, while it's extremely difficult to turn on the nanowire transistor with $Q_f = -1 \times 10^{12} \text{ cm}^{-2}$. Mechanism that lies behind this phenomenon can be explained by the contour plots of electron contribution inside the GaAs slabs in Figure 3.7b ($V_{DS}=0 \text{ V}$, $V_{GS}=0 \text{ V}$). In the case of $Q_f = 0 \text{ cm}^{-2}$, electron concentration is around $5 \times 10^{16} \text{ cm}^{-3}$, while the gradient in radial direction is affected by work function of metal gate. As the density of surface states increases, conduction channel becomes narrower and fully depleted with $Q_f = -1 \times 10^{12} \text{ cm}^{-2}$, thus limits the magnitude of the current and on-characteristics of the device. These simulations further support our understanding of the strong correlation between the surface condition and the transport property of GaAs nanowire, which facilitate the design and engineering of nanowire electronic and optoelectronic devices.

Figure 3.7 (a) Simulated I_{DS} - V_{GS} curve of a GaAs slab on SiO_2 with global backgate at $V_{DS}=0.1 \text{ V}$ on the dependence of density of surface states $Q_f = 0, -1 \times 10^{10}, -1 \times 10^{11}$, and $-1 \times 10^{12} \text{ cm}^{-2}$. (b) Electron concentration in GaAs slabs. As surface states increases, electron concentration decreases, hence leading to the degradation of transfer curve.

To alleviate the deterioration induced by large density of density of states, surface passivating methods has been proposed. Ammonium sulfide $(\text{NH}_4)_2\text{S}$ is widely used to passivate the surface of III-V materials by removing surface oxide layer thoroughly and saturating surface III/V bonds by sulfur atoms. However, sulfur-passivation is stable and effective for short time. Thus, capping GaAs nanowire with a larger bandgap material ($\text{Al}_x\text{Ga}_{1-x}\text{As}$) becomes the inevitable solution to provide long-term surface stability. The shell passivates core nanowire surface and separates electrons and holes on the coaxial interface due to bandedge discontinuity, reducing the influence of surface states. Experimentally, growth of core-shell GaAs/AlGaAs (40/300 nm in radius) nanowires was conducted in in a horizontal MOCVD reactor on GaAs (111)B substrates. Firstly, core GaAs nanowires were seeded by 40 nm diameter gold nanoparticles. Metal organic precursors, TMGa and TBAs, were carried by hydrogen gas with the flow rate of 0.91, 12.91 $\mu\text{mol/s}$, respectively, corresponding to a V/III ratio of 14.25. The reactor pressure was fixed at 50 mbar with temperature of 430 $^\circ\text{C}$ during the growth. After 5 min growth of GaAs core structure, a ~300 nm AlGaAs shell was grown at 630 $^\circ\text{C}$ for 10 min (thick shell to increase accuracy of composition analysis), with TMGa, TBAs, and Trimethyl-aluminum (TMAI) flow rates of 0.45, 6.46 and 0.17 $\mu\text{mol/s}$, respectively. The AlGaAs shell was n-doped using SiH_4 gas at a flow rate of 3.13×10^{-4} $\mu\text{mol/s}$, which resulted in doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$, as determined by Secondary Ion Mass Spectrometry (SIMS), in an equivalent thin film growth. Final core-shell structure had an overall diameter of 680 nm, as shown in the inset of Figure 3.8. Compositional measurements were conducted point-by-point along the nanowire axis in a Jeol JSM-6700F SEM equipped with Energy dispersive X-ray (EDX) detector. Figure 3.8

shows Al content in the nanowire shell of ~14-18 %. The composition is rather uniform along the nanowire axis, showing some variation near the nanowire tip, most likely due to reactant diffusion on the sidewalls near the Au catalyst.

Figure 3.8 Atomic composition of a thick AlGaAs shell in a GaAs/AlGaAs nanowire as a function of position along the nanowire axis obtained by EDX spectroscopy. Inset: SEM image of the GaAs/AlGaAs nanowire with core diameter of ~40 nm and overall diameter of 680 nm. Scale bar is 1 μm .

Comparative optical measurements were also conducted on a single GaAs nanowire with radius of 40 nm, and a GaAs/high-T GaAs/AlGaAs (40/170/30 nm) nanowire where the high-T GaAs layer was grown at 630 °C for 5 min, with respective TMGa and TBAs flow rates of 0.45 and 6.46 $\mu\text{mol/s}$. These nanowires were removed from their initial substrate by sonication in an ethanol solution and sequentially dispersed onto a SiO_2/Si substrate. With the help of a Nikon microscope coupled with a Jobin-Yvon spectrometer of 30 cm focal length and a nitrogen-cooled CCD camera, micro-photoluminescence (μPL) emission was measured through a 100 $\times$ /0.7 numerical aperture microscope objective at room temperature.

Nanowires were excited by 514 nm cw ArKr laser. Figure 3.9a compares the μ PL results of a single GaAs nanowire and a single core-multishell nanowire. No obvious peak is observed in case of single GaAs nanowire, while the core-multishell nanowire exhibits a strong photoluminescence peak at 878 nm (~ 1.412 eV). It is slightly red shifted from bulk ZB GaAs PL peak at room temperature of 870 nm,¹⁸⁵ indicating the indirect recombination of electrons confined in the GaAs/AlGaAs interface and the holes in the GaAs flat valence band region (band diagram is illustrated in the inset of Figure 3.9a).¹⁸⁶ In addition, Silvaco-Atlas simulation was conducted to map the electron distribution in the cross-section of three different nanowires by solving self-consistent Schrödinger-Poisson equations. Figure 3.9b shows the contour plots in linear scale of GaAs nanowire ($r=40$ nm), GaAs/high-T GaAs nanowire (40 nm/170 nm), and core-multishell GaAs/high-T GaAs/AlGaAs nanowire (40 nm/170 nm/30 nm). Electrons are almost depleted in the first two cases of GaAs nanowires without surface passivation, while electron confinement at the GaAs/AlGaAs heterointerface can be clearly observed in the last image of Figure 3.9b. All these evidences manifest the importance of surface passivation in electronic applications of III-V nanowires.

Figure 3.9 (a) Comparison between micro-photoluminescence emission from a single GaAs nanowire ($r=40$ nm) and a core-multishell GaAs/high-T GaAs/AlGaAs nanowire at room temperature. Inset is schematic band diagram of GaAs/AlGaAs heterostructure, showing the band discontinuity at the heterointerface. (b) Simulated electron contour plot of the cross-sectional plane of a core GaAs nanowire ($r=40$ nm), a GaAs/high-T GaAs nanowire (40 nm/170 nm), and a core-multishell GaAs/high-T GaAs/AlGaAs nanowire (40 nm/170 nm/30 nm). The scale bar is in linear scale. Image adapted from Ref. 187.

3.5 Heterogeneous integration of III-V on Si

3.5.1 Heteroepitaxial growth

The growing demand for the implementation of high-performance III-V structures into the well-established and functional silicon platform is facing technological challenges due to lattice mismatch, thermal expansion coefficient difference, and polar/nonpolar surface nature. However, the quasi 1D geometry characteristics of the nanowire, i.e. the large surface-to-volume ratio and small diameter, promote the strain relaxation coming from lattice mismatch, thus reducing the lattice matching requirement existed in conventional thin films

growth, and enabling direct high quality heteroepitaxy without introducing buffer layer. A non-exhaustive list of lattice mismatch of III-V on non III-V is reported, e.g. GaAs (4.1%),^{149, 150, 188-197} InAs (11.6%),¹⁹⁸⁻²⁰⁶ InP (8.1%),^{135, 196, 198, 200, 207} GaP (0.37%),^{191, 196, 198, 208} and ternary-alloy^{197, 209-216} on Si, InP on Ge (3.7%),²¹⁷ and even GaAs, InAs on graphite.^{218, 219} III-V nanowire based devices integrated on Si, such as photodetectors,¹⁹⁰ photovoltaics,^{190, 210} LEDs,^{197, 212} tunneling diodes,²²⁰ and surrounding gate FETs,^{56, 57} have been demonstrated relying on the successful III-V/Si heteroepitaxial growth.

III-V nanowires normally grow on (111)B substrate in the $\langle 111 \rangle$ direction. However, due to the unpolarized surface of the Si (111) substrate, they tend to grow in the four equivalent $\langle 111 \rangle$ directions with one perpendicular to the Si substrate and three other orientations having a 19.5° angle with respect to the surface and 120° between in-plane projections of each other. Vertical nanowires grown on Si have been reported through proper substrate preparation (Buffer oxide etchant for native oxide removal), surface reconstruction, and annealing.^{190, 201, 203} Figure 3.10a shows our growth of GaAs nanowire on Si in four equivalent directions, which is undesired for large-scale applications. Zoom-in SEM image in Figure 3.10b illustrate one of the vertically grown nanowire on Si. More efforts are needed in this exploration, including optimization of growth condition, reducing the time surface preparation and loading, etc. Nevertheless, the capability of III-V nanowire growth on Si or on insulator on Si enables the heterogeneous integration of III-V based building block to CMOS technology for hybrid information process.²²¹

Figure 3.10 (a) GaAs nanowires grown on Si substrate in four equivalent $\langle 111 \rangle$ directions. (b) Zoom-in SEM image of GaAs nanowire grown vertically on Si substrate.

3.5.2 Epitaxial growth on transferred III-V layer on Si

Heteroepitaxial growth of III-V at predetermined locations on Si has been demonstrated by some groups.^{190, 198, 201, 206} However, the prevalence of such architecture is limited by the electrical isolation prohibited by underlying Si substrate and the ability to study individual single nanowires. Alternatively, postgrowth assembly of individual nanowires and nanowire arrays onto external substrates resolves the electrical conduction issue and allows the distribution of nanowire in a parallel and scalable manner, which includes electric-field manipulation,²²² fluidic alignment,²²³ Langmuir-Blodgett alignment,²²⁴ and sequential printing.²²⁵ While these techniques are suitable for low temperature processing, they may not fully compatible with current planar devices that requires dense and high performance integration. Here, we applied an unconventional strategy²²⁶ (a combination of bottom-up synthesis and top-down technique) that allows vertical heterointegration, electrical isolation and individual control of III-V nanowires grown on Si.

Here we applied Smart-cut technique to integrate III-V layers to Si platform, which has been widely used in fabrication of silicon-on-insulator wafers. Similar implantation and exfoliation process have been conducted except we based on an eutectic bonding scheme. Firstly, H⁺ ions were implanted in InAs surface followed by deposition insulating layers and Ti/Ni layers. A rapid thermal annealing was then conducted at 400 °C in a forming gas environment to achieve III-V/Si bonding through nickel silicidation formation, during which a pristine InAs film can also be exfoliated from the donor substrate and transferred to the Si side. More details of this bonding technique will be discussed in Section 6.2. Cross-sectional HRTEM image in Figure 3.11a shows single crystalline InAs bonded on SiN_x layer, which enables integration of III-V to Si and also electrical isolation between diverse III-V devices. Figure 3.11b illustrates the top-view SEM image of the transferred InAs top-surface with an average roughness of 2.4 nm measured by atomic force microscopy. However, InAs layers are partially bonded to Si substrate as exhibited in the inset optical microscopy image (2.5 mm×3 mm area size) caused by undesired micro-bubble formation and surface blistering. Thus a better control in the conditions of implantation and exfoliation are desired. Nevertheless, this approach allows in growth of InAs nanowire arrays from pre-patterned Au nanodots by MOCVD as demonstrated by Dayeh *et al.* shown in Figure 3.11c.²²⁶ For the purpose of device integration, electrical isolation between individual nanowires could be realized by introduction of one more electron beam lithography (EBL) step using electron beam resist to align and protect the InAs nanowires, followed by wet etching of exposed InAs layer in a mixture of HCl:H₂O₂:H₂O solution, leading to arrays of isolated InAs nanowire on nanodiscs as illustrated in the inset of Figure 3.11c. Such architecture enables the realization of individually addressable vertical nanowire devices, such as gate-all-around

vertical FETs. Overall, the partial exfoliation of InAs layer in the Smart-cut and NiSi bonding process has a potential in fundamental study of epitaxial growth on transferred layers, but remains as an issue for large scale integration which couldn't be optimized during my Ph.D. time, thus we explored an alternative scheme for III-V layer transfer, which will be discussed in Chapter 6.

Figure 3.11 (a) Cross-sectional HRTEM shows the single crystalline InAs transferred to a SiN_x layer, relying on a combination of Smart-cut process and nickel silicidation. (b) Top-view SEM image of the transferred InAs layer on insulator on Si. Inset microscopic image shows partially transferred InAs layer (orange color) to Si caused by undesired surface blistering and micro-bubble formation. (c) 85° tilted SEM image of InAs nanowire arrays grown on InAs/SiN_x/NiSi/Si substrate, with the inset illustrating a 45° angle-view SEM image of etched islands with electrically isolated InAs nanowires on top, adapted from Dayeh's work in Ref. 226. All the scale bars are 1 μm.

Chapter 4 Self-assembly of monolithic Y-junctions: a bottom-up approach toward quantum transport devices

4.1 Introduction

Advances in both top-down and bottom-up techniques have allowed the full development of nanometer size devices in the investigation of mesoscopic science. Mesoscopic physics becomes more and more important with the miniaturization of electronic and photonic devices when atoms at the surface determine the properties of the system. It enables the study from classical physics to quantum mechanics. Researchers focused on the study of quantum dots since last decade, while the electronic study of quantum dots remains a big issue. Traditional solution is based on split-gate electrostatic confinement, which creates a quantum dot on 2DEG and realizes the electrical connection for research of charge transport in mesoscopic systems. However, lots of active areas are sacrificed for the split gate contacts in this method. Though quantum dots can also be synthesized through Stranski-Krastanov growth (coherent islands formation during the thin film growth) or chemical reactions in colloidal solutions, the random distribution limits their application in electronic devices. Instead, it's worthy noticing the presence of quantum dots as small axial hetero-segments inside nanowires. Moreover, the nanowire networks, complex 3D junctions of 1D components, have the potential in the study of unexpected mesoscopic science. For instance, self-assembled InAs nanowire junction exhibits quantized conductance between all arms and nonlinear ballistic transport.^{20, 117} InSb X-junction (Figure 4.1b) shows high carrier mobility and an indication of supercurrent through the nanocross at low temperature.¹¹⁸

Figure 4.1 (a) 30° tilted SEM images of GaP nanotrees grown in MOCVD at temperature of 460°C with two-step VLS process. Top-view SEM image on the left showing three branch directions in nanotrees with fewer than seven branches, image on the right exhibiting six branch orientation for trees with more than ten branches per tree. Figure adapted from Ref. 16. (b) InSb nanocrosses forming through the merging process between two InSb NWs grown on InP/InAs stems. Adapted from Ref. 118. (c) 45° tilted SEM image of InAs nanowire pairs grown on an array of InP ridges with 4 μm interdistance, the close-up images are shown on the right (scale bar is 100 nm). Figure adapted from Ref. 116.

Samuelson's group explores the two-step growth of GaP nanotrees with branches growing in the $\langle 111 \rangle_B$ direction on the [001] trunk (Figure 4.1a).¹⁶ Followed by that, branched nanowire junctions have intensively been reported in oxide and group VI compounds. Controllable self-assembly of III-V networks becomes inevitable recently, which determined by the growth orientation, the interdistance between two catalysts and the diameter of the nanowire. However, most of these growths are limited for the large scale integration because nanowires are removed from the original substrate and randomly placed on another host substrate.^{20, 117, 118} Consequently, a vertical array of nanowire

interconnections in a deterministic manner with proper electrodes design is highly desired, as demonstrated in Dalacu et al. work in Figure 4.1c,¹¹⁶ which opens up new opportunities for large scale functional device integration.

4.2 Selective area growth of compound nanowires

For applications that require a dense 3D integration of vertical nanowire circuits and systems, it will be necessary to precisely control the nanowire morphology, crystal structure, and position with a high yield and a great reproducibility at the wafer scale. Within the bottom-up paradigm, the so-called selective-area nanowire growth can be achieved by two methods, which include the VLS nanowire growth from predetermined positions of patterned metal catalysts or the self-catalyzed growth from predetermined openings in a sacrificial oxide mask.^{127, 227, 228} In our study, the selective-area growth of arrays of GaAs nanowires has been investigated and optimized by pre-defining Au nanodiscs by standard electron beam lithography (EBL) and metal lift-off techniques, as shown in Figure 4.2. Nanowire arrays with a periodic interdistance and a desired diameter were then successfully achieved by MOCVD growth using the patterned substrates under the optimized growth conditions discussed in Section 3.2.

The demonstration of bottom up growth of engineered, ordered and uniform arrays of III-V nanowires offers both a high accuracy and repeatability in ordering nanowire as periodic arrays, promoting mandatory requirement for most of applications in small feature size electronics, photonics and life sciences. For instance, the integration of 3D vertical surround-gate nanowires FETs has been demonstrated to improve the performance of circuits together with reducing the footprint of a single logic element.^{54, 58} Furthermore, the high

aspect ratio of III-V nanowires combined with their high index contrast with air make them particularly attractive for the development of innovative integrated photonic light sources. Indeed, bottom-up nanowire arrays can be designed to form a two-dimensional photonic crystal offering one more degree of freedom to tailor their optical properties compared to the traditional Bragg mirror fabricated by top down techniques. It opens new opportunities in the fabrication of high efficiency LEDs as well as bottom-up photonic crystal cavity and laser.²²⁹⁻²³¹ To be more specific, it paves the way for the designing highly-ordered nanowire networks for both electronic and photonic applications.

Figure 4.2 Selective-area growth of GaAs nanowires: (a) pre-pattern Au nanodiscs used as initiators of the VLS growth; (b) GaAs nanowire array grown from (a).

4.3 Self-assembly of monolithic nanowire junctions

Intersected or branched nanowires with continuous crystalline (monolithic) structures offer a promising platform for low-dimensional fundamental condensed matter physics research.^{119, 120} Thanks to the advances in the control and understanding of nanowire growth

mechanisms, self-assembly of monolithic junctions^{116-118, 232} and two-steps catalytically branched nanowires growth become achievable by standard synthesis methods.^{16, 20, 115}

In our experiment, spontaneous GaAs nanowire merging (kissing) and the successively self-assembly of monolithic junctions was observed for the first time during the growth from randomly dispersed Au nanoparticles (Ted Pella, Inc.) with diameters of 10-40 nm by MOCVD with V/III ratio of 14.25 at 430 °C on GaAs (111)B substrates Figure 4.3a. To explain and further investigate the dynamics of the nanowire kissing phenomenon, several nanowire growths were conducted in an identical chamber condition, by only increasing the growth time. Figure 4.3b-d present the typical results for nanowires growing for 1, 2, and 3 min from ~40 nm nanoparticles with an average distance of 0.3 μm . Similar kissing and merging phenomena were found in nanowires grown from smaller nanoparticles (~20 or 10 nm in diameter), but with decreased distance between the point of contact to the substrate and increased maximum interdistance between the branches, thanks to the greater mechanical flexibility of such thinner nanowires.

Before occurrence of kissing, both adjacent nanowires present a ZB crystal structure with a few stacking faults as indicated in the Fast Fourier transform (FFT) patterns of HRTEM images in Figure 4.4b. {111} lattice fringes were marked with yellow dashed line, $(\bar{1}\bar{1}1)$ direction was illustrated in oranges line. White arrow in Figure 4.4b points at a stacking fault which leads to a 60° rotation around the nanowire axis of (111) plane, changing the crystalline structure of the lower nanowire from Figure 4.4a to c. The side facets of the nanowire in Figure 4.4d are oriented in $\langle 112 \rangle$ direction with a stepped structure of polar {111} and {113} planes¹²⁹ that correspond to the lowest calculated surface energies.²³³

Reconstructions of faceted nanowires are displayed from top (Figure 4.4e) and side $\langle 110 \rangle$ views (Figure 4.4f), together with the modeling of two adjacent nanowires for kissing (Figure 4.4g). It is proposed that nanowire kissing will happen when the electrostatic force between polar facets ((111)A and (111)B) on the adjacent nanowire surface is larger than the mechanical stiffness at microscopic length scales.

Figure 4.3 Nanowire kissing. (a) 45° tilted SEM image showing coexistence of individual GaAs nanowires and merged nanowire bundles in the same substrate region. (b-d) The evolution of GaAs nanowire kissing observed from three individual growth runs with increasingly longer growth times (nanowire lengths): (b) the two vertical nanowires grow parallel to each other (tg=1 min); (c) the nanowires bend and kiss (tg=2 min); (d) the nanowires merge in a bundle (tg=3 min). Image adapted from Ref. 232.

Figure 4.4 Crystalline structural analysis of kissing nanowires. (a-c) $\langle 110 \rangle$ viewing orientated HRTEM images showing registered (111) planes across the two kissing nanowires: white arrow in (b) marked the locations (a) before and (c) after the stacking fault. FFT patterns in insets of (b) stands for the two adjacent nanowires. Scale bar is 10 nm. (d) HRTEM image of one of the NWs in (b) taken from $[101]$ viewing orientation displaying $(1\bar{1}1)$ and $(\bar{1}3\bar{1})$ facets. (e-g) Atomic model of a GaAs NWs grown in the $[111]$ orientation. (e) Top view, and (f) side view from a $\langle 110 \rangle$ orientation showing facet edges in agreement with those in (d). (g) Adjacent NWs with polar $\{111\}$ A and B facets electrostatically attract each other. Image adapted from Ref. 232.

To prompting nanowire kissing, the increment of electrostatic energy must exceed the mechanical energy that is required to bend them. A simple nanobeam model stands for the geometrical properties of the nanowires and the Coulomb interaction between polar surfaces can be built based on the energy balance.²³⁴ The bending force (F) acting on the nanobeam can be described by those geometrical parameters: L is the length of the beam, x is the bending displacement (deflection), y is the integration variable along the beam axis, r is the nanobeam radius, and d is the distance between two nanobeams. Based on the Euler-Bernoulli beam theory,²³⁵ the bending moment $M = -F(L - y)$ is related to the deflection by $M = -EI(d^2x/dy^2)$, where E is the Young modulus and I the area moment of inertia (for a beam with hexagonal cross section $I = 5\sqrt{3}r^4/16$). It can be deduced that $x = -FL^3/3EI$. Therefore, the total bending energy (E_b) for a system of two nanowires can eventually be expressed as:

$$E_b = 2 \times \int_0^L \frac{M^2}{2EI} dy = \frac{15\sqrt{3}Ex^2r^4}{16L^3} \quad (4.1)$$

where the Young modulus of different dimension GaAs nanowires has been characterized using *in-situ* compression measurements.²³⁶ The Young modulus was resolved to be $E=183$ GPa for nanowires with radius of 20 nm. Using typical values for the nanowire length of $L=1.6$ μm and interdistance $d=0.3$ μm (Figure 4.3c), Eq. 2.1 at the point of contact ($x=d/2$) leads to $E_b = 2.6 \times 10^{-16} J$.

From the difference of Coulomb attraction from polar microfacets with opposite charges before and after kissing (i.e. initial and final configuration), the electrostatic energy (E_e) gained by bending nanowires can be estimated from:

$$E_e = E_{final} - E_{initial} = \frac{-Q^2}{4\pi\epsilon} \times \left(\sum_{j=1}^n \sum_{i=1}^n \frac{1}{s_{ij2}} - \sum_{j=1}^n \sum_{i=1}^n \frac{1}{s_{ij1}} \right) \quad (4.2)$$

where ϵ is the vacuum permittivity, Q is the charge on the A- or B- polar surfaces (terminated with either Ga or As atoms), each contributing one dangling bond normal to the surface.²³⁷ s_{ij} is the distance between the i -st facet on one side and the j -st facet on the other side at rest, $s_{ij1} = \sqrt{d^2 + (i-j)^2 \cdot A^2}$, and $s_{ij2} = A \cdot \sqrt{i^2 + j^2 - 2ij \cos \theta}$ at the point of contact. Here d is the distance between two nanowires at rest, and A is the total axial length of the two {111} and {113} facets. The surface density of charges ($n_p = Q / q r A$) can be estimated assuming that the electrostatic attractive energy equals the mechanical bending energy ($|E_e| = |E_b|$) at the point of contact. For typical NW dimensions of $r \sim 20$ nm and $d \sim 0.3$ μ m (Figure 4.3c) and $A \sim 16$ nm (Figure 4.3d), this leads to $Q / q \sim 10$, and $n_p \sim 3 \times 10^{12}$ cm⁻². This is a reasonable charge density, agreed with a spontaneous polarization charge density of $\sim 10^{13}$ cm⁻² in polar III-V and II-VI materials.^{53, 238} Hence, our coupled experiment-model can be utilized in the extraction of surface charge densities on polar 3D surfaces, which is generally hard to measure by other techniques. Paragraph adapted from Ref. 232.

Numerical calculation is implemented in elucidation of geometrical parameters depended energetics, as illustrated in Figure 4.5a. It shows the zero total energy surface ($E_t = E_e + E_b = 0$) as a function of NW radius (r), interdistance (d) and junction height (L),

assuming surface density of charges $n_p \sim 3 \times 10^{12} \text{ cm}^{-2}$. When the total energy is smaller than zero, nanowire kissing become energetically favorable (indicated in the region above the zero energy surface), i.e. for small NW radii and distances, and for long junctions. It is worth noting that reduction of r not only decrease mechanical stiffness, but also diminish the total surface charge on the polar surfaces that contribute to the electrostatic attraction.

Vertical Y-junction arrays grown from pre-patterned Au discs further demonstrated and exploited the understanding learnt from the modeling (Figure 4.5b-e). An array of Au discs with large (Figure 4.5b, inset) and small (Figure 4.5c, inset) diameters arranged in dimer configuration was EBL patterned on the GaAs (111)B substrate. Nanowires grown from the first pattern of large diameter Au remained mechanically robust and vertical configuration, while those from the smaller size Au dimers in close vicinity leaded to nanowire kissing. Notably, the smaller size and interdistance of Au nanoparticles as shown Figure 4.5c resulted in longer nanowire growth thanks to a diffusion limited growth behavior¹³³ and possible synergetic effects due to NW proximity.²³⁹ There is a possibility for evolution from nanowire kissing to monolithic junction formation as demonstrated in Figure 4.5d, taken from one of the dimers in the array. Merging of two independent nanowires is clearly presented in Figure 4.5e, where the diameter of the merged nanowires is larger than the original nanowire, consistent with the volume enlargement of the fused Au nanoparticles. With further elongation of the junction, a step-like reduction of nanowire diameter and some surface roughness were observed due to instabilities of Au nanoparticle and Au diffusion down the NW stem.

Figure 4.5 (a) Zero total energy surface as a function of nanowire radius (r), interdistance (d), and height of the junction (L) for a surface density of charges of $n_p \sim 3 \times 10^{12} \text{ cm}^{-2}$. Kissing is energetically favorable in the area above the surface, where $E_t = E_e + E_b < 0$. (b)-(d) SA nanowire growth from EBL patterned arrays of dimers (a pair of Au nanodiscs). (b) Nanowires grow vertical and separated from each other for dimers with large Au nanoparticle size ($r=45 \text{ nm}$) and distance ($d=300 \text{ nm}$); (c) Nanowire kissing is induced by dimers with small nanoparticle size ($r=22.5 \text{ nm}$) and distance ($d=250 \text{ nm}$). The insets of (b) and (c) show the dimers patterned by EBL before the growth. (d) A vertical monolithic Y-junctions formed from the dimer upon merging of two kissing nanowires. (e) A magnified view of the junction in (d) showing the fusion of the two vertical nanowires and the subsequent growth of a single stem. Image adapted from Ref. 232.

Most of this section was published in Nano Letters, 2011, X. Dai, S. A. Dayeh, V. Veeramuthu, A. Larrue, J. Wang, H. Su, C. Soci. The dissertation author was the first author of this paper.

4.4 Y-junction devices and their characteristics

Transport properties of three-terminal Y-junction devices were investigated by electrical measurements. Symmetric ohmic contacts were fabricated on the three terminals of

the Y junction, assigned as S, D, G, respectively (Figure 4.6a). Each Single branch of the Y junction exhibits ohmic contact behavior and a direct low current modulation by global back gate. At the same time, a contact resistance $R_c = 2.82 \times 10^8 \Omega$ was extracted using transmission line (TML) method based on resistance dependence of the distance between contacts. Subsequently, the characterization of a three branches junction device was performed as follows: V_s is kept at 0 V, V_d is scanned continuously from 0 V to 1 V, while V_g is varied from 0 V to 2 V with a 0.5 V step size. Figure 4.6c displays that both $|I_s|$ and I_d increases with V_d at a fixed V_g . Moreover, $|I_s|$ also increases with increasing V_g . The direction of I_d changes when increasing V_g , but doesn't change at the point $V_d=V_g$. This behavior may be attributed to the asymmetric geometry of the Y junction branches since they have different lengths or diameters. Successively, a simple resistance model based on Kirchhoff's laws was extracted from the I-V curve (a). Preliminary electrical characterization of GaAs monolithic junctions assembled by our newly developed method demonstrate that the three branches are electronically interconnected, which is the basic requirement for more complex analysis and the future design of nanowire-junction devices, such as logic gate, electron waveguide Y-junction switches, nonlinear ballistic junctions, and Majorana fermion braiding devices.

Figure 4.6 (a) Device image and resistor equivalent circuit show applied voltage and default current direction. (b) Output curve of one branch with back gate voltage and contact resistance derivation (inset). (c) I_d - V_d and I_s - V_d curve with a continuously increasing V_d and increasing V_g from 0 V to 2 V with 0.5 V as the step size.

Chapter 5 Two-dimensional electron tubes in core-shell III-V nanowires: charge separation and photodetection

5.1 Introduction

Nanowire photodetectors promise increased sensitivity compare to planar thin films thanks to their high surface-to-volume ratio. Vertical aligned nanowire array constitute a promising building block to achieve large scale integration and enhanced efficiency and sensitivity of optoelectronic devices, thanks to the improved absorption properties coming from light confinement in the high refractive-index nanowires and the reduced reflectivity due to the enhancement of light scattering. However, such architectures rely on highly ordered nanowire arrays which require complex fabrication techniques. In the simplest scenario and for the sake of understanding, nanowire photodetectors are usually formed by horizontal nanowires randomly dispersed on an insulating substrate where an external bias is applied between top metal electrodes. Upon illumination (with light impinging perpendicular to the axis), the electrical conductivity increases due to the photoconductive effect, thus providing light-sensing capabilities. Device performances, i.e. response time, photoconductive gain, responsivity, and detectivity, are mainly determined by its geometry and material intrinsic properties.

The mechanism resulting in high photoresponsivity and photoconductive gain has been elaborated recently. The photoconductive process is composed of three distinct successive physical mechanisms: the absorption of light, the photogeneration of carriers, and the carrier transport. The addition of the photocarrier lifetime and the carrier transit time determines the gain of the photodetector. Defect-free nanowires with small interelectrode

distance lead to a small transit time. If the carrier lifetime is sufficiently long enough, photogenerated carriers can transit between the contacts several times before it is annihilated by either recombination or trapping.¹²⁵ Large diameter nanowires are expected to increase the carrier lifetime thanks to the charge separation induced by the surface states (large band bending); however, a low carrier concentration is obtained even in large-diameter GaAs nanowires with the presence of surface states (Figure 3.9b). As a result, a trade-off has to be found between the size of nanowires and the intrinsic 1D transport. Surface passivation by growing a shell around the perimeter of the nanowire becomes mandatory to optimize the carrier transport inside this type of nanowires. In combination of large diameter and core-shell structure, the nanowire can promote radial charge separation through the band alignment at heterointerface, support high-order of optical modes, enhance light absorption, ultimately increase the photocarrier lifetime and gain. In addition, III-V materials are adequate for light sensing since a wide spectral response can be covered by the variety of III-V heterostructures. Together with enhanced sensitivity to light promised by nanowire inherent large surface-to-volume ratio and their intrinsic high carrier mobility, III-V nanowires become excellent candidates in optoelectronic systems.

5.2 Heterostructured core-shell nanowire growth

Homogeneous nanowires grow in the longitude direction by absorbing the reactants into the catalyst alloys utilizing VLS mechanism. Afterwards, if the reactants changes and are absorbed at the nanowire surface, a shell will grow on the original nanowire surface, promoting the formation core-shell nanowire through vapor-solid (VS) growth (Figure 5.1a). Figure 5.1b exhibits GaAs/AlGaAs core-shell nanowire grown on GaAs (111)B substrate,

showing hexagonal cross-section. TEM image presents a clear boundary between GaAs and AlGaAs, demonstrating the successful realization of this type of growth. Alternatively, changing reactants in the radial growth regime will result in core-multi-shell structure (Figure 5.1c). Figure 5.1d illustrates the side-view of the as grown GaP/GaAs/GaP structure after removal of Au catalyst. From the top-view TEM image, one can distinguish interfaces between these layers, further confirmed by the elemental mapping.

Figure 5.1 Nanowire heterostructures. (a) Schematic of radial heterostructure together with the representative image of GaAs/AlGaAs core-shell structure showing in (b), consisting of a 45° tilted side-view, a top-view SEM images and a TEM image at the boundary. (c) Core-multishell illustration and (d) side-view SEM image of a GaP/GaAs/GaP nanowire with a plan-view TEM images, and elemental mappings (Image d adapted from Tetsuomi Sogawa's group)²⁴⁰

The precise control of III-V heterostructure growth condition enables the fabrication of complex custom-built nanowire architectures, thus broadening potential applications. For instance, Type II staggered band alignment, e.g. GaAs/InAs,²⁴¹⁻²⁴³ formed by periodically distributed band-edge alignment, is expected to provide good performances for photodetector since electrons and holes could be dragged into opposite direction, hence decreasing the probability of electron hole recombination; while the uncommon broken gap type III heterostructure GaSb(p)/InAs(n) NW can lead to efficient band-to-band tunneling and to possible higher current densities.²⁴⁴ Alternatively, GaAs/AlGaAs^{84, 245, 246} radial Type I heterostructure, where both electrons and holes tend to be localized in the lower bandgap material (GaAs), is applicable in the devices including HEMTs, photodetector and solar cells. It has been demonstrated that faster photoresponse of a GaAs/AlGaAs core-shell nanostructure with shell-to-shell electrodes compared to bare GaAs nanowire due to decreased nonradiative carrier traps at the surface.⁸⁴ Recently, a single GaAs/AlGaAs nanowire near-infrared laser working at room temperature has been reported.²⁴⁷ High efficiency solar cells have been achieved in nanopillar-array based on GaAs radial p-n junctions with the InGaP-passivating shell.²⁴⁸ Excellent performance of single nanowires for photovoltaic applications have also been observed in GaAsP p-i-n¹⁰⁸ and GaAs p-i-n¹⁰⁹ radial nanowires. These structures, however, are difficult to obtain since they require precise control over the doping of the active materials. There is still lack of study about systematic spectral analysis of room-temperature GaAs/AlGaAs nanowire photodetector.

Based on the optimization of growth condition discussed in Chapter 3, we designed and grew the core-multishell nanowire in three steps with one inserting GaAs layer to increase the diameter of the GaAs core. Simulation based on self-consistent Schrodinger-

Poisson equations predicts the formation of a homogeneous two-dimensional electron “tube” (2DET) at the heterointerface between the GaAs core (undoped) and n-type AlGaAs shell (doping of $5 \times 10^{17} \text{ cm}^{-3}$) (Figure 5.2). First, Au nanoparticles seeded GaAs nanowires with diameter of 80 nm were grown by VLS MOCVD (Figure 5.2a and d). A thick GaAs layer (~170 nm) was then deposited at higher growth temperature (Figure 5.2b and e). The high-temperature GaAs layer increases the diameter of core without bringing in substantial crystallographic defects, which are present in nanowires grown from large diameter nanoparticles (~200 nm).²⁴⁹ The complete structure ended up with a relatively thick AlGaAs shell (~30 nm) to prevent complete Al oxidation (Figure 5.2c and f). The final core-multishell nanowire has a total radius of around 240 nm and a hexagonal cross-section, as shown in the top-view SEM image in Figure 5.2f.

All the growth processes were conducted in a horizontal reactor (Aixtron 200) on GaAs (111)B substrates. Firstly, core GaAs nanowires were grown by MOCVD using 40 nm diameter gold nanoparticles as growth seeds. Metal organic precursors, TMGa and TBAs, were carried by hydrogen gas with the flow rate of 0.91, 12.91 $\mu\text{mol/s}$, respectively, corresponding to a V/III ratio of 14.25. The reactor pressure was fixed at 50 mbar with temperature of 430 °C during the growth. The diameter of the core GaAs increased to 80 nm with a length of 12 μm after 7 min growth, as shown in Figure 5.2d. The diameter of the core was then increased by GaAs inserting layer grown at 630 °C for 5 min, with respective TMGa and TBAs flow rates of 0.45 and 6.46 $\mu\text{mol/s}$, leading to a layer thickness around 170 nm. Finally, a ~30 nm AlGaAs shell was grown at 630 °C for 1 min, with TMGa, TBAs, and TMAI flow rates of 0.45, 6.46 and 0.17 $\mu\text{mol/s}$, respectively. The AlGaAs shell was n-doped

using SiH_4 gas at a flow rate of $3.13 \times 10^{-4} \mu\text{mol/s}$, which resulted in doping concentration of $5 \times 10^{17} \text{ cm}^{-3}$, as determined by SIMS in an equivalent thin film growth.

Figure 5.2 Schematic of (a) core GaAs nanowire ($r=40 \text{ nm}$), (b) core-shell GaAs/high-T GaAs nanowire ($40 \text{ nm}/170 \text{ nm}$), and (c) core-multishell GaAs/high-T GaAs/AlGaAs nanowire ($40 \text{ nm}/170 \text{ nm}/30 \text{ nm}$). The corresponding contour plots show the simulated spatial distribution of electron concentration in the cross-sectional plane. Scale bar is in log scale and unit is cm^{-3} . (d)-(f) SEM images of nanowires at three different growth stages (obtained with a tilt angle of 45°). The Au nanoparticles used to seed the VLS growth is visible on top of the wires. The inset of (f) is a top-view image of the core-multishell nanowire showing its hexagonal cross-section. Image adapted from Ref. 187.

The crystalline structure of core-multishell GaAs/high-T GaAs/AlGaAs nanowire was investigated by a high-resolution transmission electron microscopy (HRTEM, 200kV JEOL

2100F). For high resolution imaging purpose, we first thinned the nanowire on opposite sides along the edge of hexagon using focused ion beam (FIB). Then we cut the nanowire at its base and transferred it onto a TEM grid. A representative TEM image in Figure 5.3a shows the clear boundary between AlGaAs shell and GaAs as marked with yellow dashed line. HRTEM images of core GaAs, high-T GaAs and AlGaAs shell are respectively illustrated in Figure 5.3b-d, with FFT patterns of each region shown in the insets. FFT patterns obtained from this sample produce sharp spots characteristic of uniform diffraction from [101] zone axis of ZB GaAs and AlGaAs crystal structure. All three regions are characterized as a distinct ZB crystal structure and excellent crystal quality, demonstrating the effectiveness of high temperature overgrowth of the nanowire core.

Figure 5.3 (a) TEM image of the core-multishell GaAs/high-T GaAs/AlGaAs nanowire prepared by FIB thinning showing the different layers as indicated with yellow dashed line. HRTEM images taken with $\langle 101 \rangle$ viewing orientation showing excellent crystal quality of the three layers: (b) GaAs core, (c) GaAs inserting shell, (d) AlGaAs shell, all of them present pure ZB crystal structures. Insets are FFT patterns of these three layers. Scale bars, 2 nm. Image adapted from Ref. 187.

5.3 Core-shell nanowire photodetector

Another major challenge in III-V nanowire detector technology is posed by the formation of ohmic contact. Instead, a metal-semiconductor-metal (MSM) configuration, consisting of back-to-back Schottky diode structure, has been proposed and employed in the fabrication of photodetector devices in 1990s.^{93, 250-252} In the dark, thermionic emission

determines and limits the current transport of MSM photodetector primarily.²⁵³ Under illumination, the increment of carrier density enhances the tunneling probability across the Schottky barrier at the metal/semiconductor interface, where the self-built potential plays a crucial role in the carrier separation and transport, especially when it is reverse-biased.²⁵² Consequently, we applied the MSM structure to our core-multishell GaAs/high-T GaAs/AlGaAs type-I nanowire photodetector.

Optical measurement on a single GaAs and a core-multishell nanowire has been discussed in Section 3.4, where no obvious peak is observed in case of single GaAs nanowire, while the core-multishell nanowire exhibits a strong photoluminescence peak. Properties of electrical transport were characterized on a single core-multishell GaAs/high-T GaAs/AlGaAs nanowire with electrodes on core and shell separately. Nanowire was first dispersed on SiO₂/n⁺-Si substrates with alignment markers, then was selectively masked and etched in the mixture of citric acid and H₂O₂ solution to remove the AlGaAs shell and the high-T GaAs shell, ending up with a ~70-80 nm GaAs core. 100 nm thick Pt was successively deposited on the GaAs core and AlGaAs shell using FIB system. The final structure is illustrated in Figure 5.4a. I-V characterization was performed with a Keithley 6487 source-measure unit (SMU). A 450 W xenon (Xe) lamp with a power of 0.8 W/cm² was used to characterize the photoelectrical response. Figure 5.4b compares the representative I-V characteristics in the dark and under illumination. An asymmetric I-V curve with low dark current is measured, which is limited by the different Schottky barrier heights between Pt/GaAs and Pt/AlGaAs in the MSM structure.^{90, 250} The dark current is successfully suppressed in this case. Under illumination, the photocurrent increases rapidly in the voltage range of -1 V to 1 V, and then starts to lower the increasing slope. When a contact is under

reverse bias, its Schottky barrier height increases, providing a stronger local built-in electric field at the contacts. Thus photo-generated electrons and holes are efficiently separated by this field, resulting in an increment in photocurrent. The maximum current is limited by carrier drifting in the space-charge region near the contact and GaAs/AlGaAs hetero-interface, and diffusion inside the neutral region of the nanowire (carrier diffusion length and lifetime).²⁵² Under negative bias of -2 V and positive bias of 2 V at the AlGaAs shell with GaAs core grounded, a maximum current of -0.8 nA and 0.62 nA is observed. The different current values originate from the higher Schottky barrier height at Pt/AlGaAs interface than at Pt/GaAs interface. Consequently, the clear photocurrent to dark current on/off ratio is demonstrated in our device.

Figure 5.4 (a) SEM image of the device with one contact on the core and one on the shell. Scale bar is 2 μm . (b) Current-voltage relationship of a core-multishell nanowire in the dark and under Xe lamp illumination.

The photoresponsivity of the core-multishell nanowire photodetector as a function of the illumination wavelength is evaluated at room temperature with fixed V_{SC} at 2 V. Figure 5.5a shows the measured photoresponsivity spectrum, similar to a typical GaAs photodetector except the appearance of few peaks. It indicates that absorption occurs in the GaAs core rather than in the AlGaAs shell and suggests the presence of optical resonant modes within the nanowire leading to an increment in absorption. At $\lambda=855$ nm, responsivity, defined as the ratio of electrical output to the optical input, is 0.57 A/W, which is higher than the commercial GaAs photodetector.²⁵⁴ Specific detectivity is $7.20 \times 10^{10} \text{ cm}\sqrt{\text{Hz}}/\text{W}$, slightly lower than one reported planer GaAs photodetector.²⁵⁵ Photoconductive gain is 1.04, which desires future optimization. Spectral shape and amplitude of experimental photoresponsivity spectrum are in agreement with 2D Silvaco-Atlas simulated results (Figure 5.5b) predicted by solving Boltzmann transport equation, considering charge carrier density and distribution of the 2D electron tube under illumination. The optical behaviour of the nanowire is also investigated through full-wave optical simulations (COMSOL); Figure 5.5c shows the calculated optical absorption spectrum on which at least three absorption peaks can be identified at 655 nm, 800 nm and 850 nm. The strongest peak at 850 nm (mode 1) can be identified in the experimental spectrum, while the higher order modes at 800 nm and 655 nm are gradually masked by the noise during the room-temperature measurement. Optical absorption maps across the section of the nanowire (Figure 5.5d-f) help visualize the spatial distribution of electromagnetic energy within the device: it can be clearly observed how the three modes corresponding to the absorption peaks are indeed confined inside the GaAs core of the wire by the higher refractive index AlGaAs.

Finally, the manner of carrier transport inside our device was investigated using Silvaco-Atlas simulation tool. The distributions of holes, electrons and total carriers (holes and electrons) in the dark and under illumination with the Xe lamp at -2 V source bias (GaAs core side) are illustrated in Figure 5.6. In the dark, a high density electron gas is formed at the GaAs/AlGaAs interface (Figure 5.6b), while the electron density decreases on the source side with only GaAs core, which leads to a suppression of the 2DEG at one end of the core-multishell nanowire thus reduces the dark current. Under illumination, photons are absorbed in the GaAs part, producing electron hole pairs. The photo-generated electrons are accumulated at the GaAs/AlGaAs interface (Figure 5.6e), while holes are stored at the boundary between electrode and GaAs due to the raised Schottky barrier (Figure 5.6f). Holes are then collected by the source electrode while electrons are collected by the 2DEG and transferred to the drain electrode along this channel. Radial charge separation promised by the core-shell structure with MSM configuration thus decreases carrier recombination and increase the total photocurrent, demonstrating the feasibility of our design for efficient nanowire photodetectors.

Figure 5.5 (a) Experimental photoreponsivity as function of the excitation wavelength for a core-multishell nanowire photodetector under a bias of 2V: peaks can be observed on an otherwise typical GaAs photoresponse. (b) Simulated photoreponsivity spectrum. (c) Simulated optical absorption spectrum of a core-multishell nanowire: peaks in absorption, labeled as 1, 2 and 3, are observed at respectively 850nm, 800nm and 655nm. (d-f) Simulated optical absorption maps across the section of the nanowire at wavelengths corresponding to peaks 1, 2 and 3 respectively.

Figure 5.6 Profiles of 2D current distribution in the core-multishell GaAs/high-T GaAs/AlGaAs nanowire PD with $N_D=1 \times 10^{13} \text{ cm}^{-3}$ and $N_D=5 \times 10^{17} \text{ cm}^{-3}$ for GaAs and AlGaAs, respectively. The top row is simulation results in the dark, while the bottom row is simulation results under illumination. (a) and (d) are the total current density plots (hole and electron current), (b) and (e) are the electron current density, and (c) and (f) are the hole current density.

In conclusion, a novel core-multishell GaAs/high-T GaAs/AlGaAs nanowire photodetector utilizing MSM structure was proposed and demonstrated. Excellent crystal structure is observed with an enhancement in μPL spectrum compared to a single GaAs nanowire. The device yields a low dark current and high photo sensitivity in the wavelength range of 300 nm to 890 nm, presenting a high photocurrent to dark current ratio. Self-consistent solution of Schrödinger-Poisson equations manifests the presence of a 2DEG at the GaAs/AlGaAs interface, while carrier transport simulation reveals that electrons are collected at the core-shell interface and holes are accumulated at the Schottky contact between electrode and GaAs core. Full wave optical simulation revealed the presence of modes supported by the nanowire which are responsible for the appearance of peaks in the

measured photocurrent. Though unitary gain was observed in our experiment, future research on doping modulation, diameter dependence, and metal contacts engineering promises the possibility in achieving room-temperature photodetectors with high gain. Overall, this demonstration highlights the potential of combined optimization of crystallographic, transport and optical properties to design III-V nanowire photodetectors with high efficiency.

Most of this section was published in Nano Letters, 2014, X. Dai, Z. Wang, G. Adamo, S. Zhang, L. Hai, Y. Huang, C. Couteau, and C. Soci. The dissertation author was the co-first author of this paper.

Chapter 6 Quasi one-dimensional III-V Fins on Silicon: integrated tri-gate FinFETs

6.1 Introduction

The bottom-up technique offers great opportunities to control the synthesis of nanowires with perfect crystal structure, core-shell configuration for surface passivation, heterogeneous integration on Si platform, and even complex nanowire networks. However, nanowires synthesized from bottom-up technique are not yet incorporated for real applications in mainstream fab manufacture due to low yields, inefficient heterogeneous integration, and incompatibility with planar technology. To tackle these problems, here we focus on the implementation of 1D III-V nanowires into conventional CMOS in a top-down process. Some intrinsic issues of bottom-up III-V nanowires have been discussed in the previous chapters, such as high density of surface states and difficulties in making ohmic metal contacts, which can be solved by heterostructure growth for passivation and for carrier separation in photoconductive devices. Similar issues are expected to be encountered in the 1D III-V structure subject of discussion in this chapter; however, these Fin like structures are incorporated at high yield in a CMOS compatible process to a Si substrate, thereby demonstrating a potential path for large scale fabrication and deployment in future hybrid technologies.

III-V semiconductor materials are the core materials for high electron mobility devices. The excellent on-state performance of InGaAs MOSFETs (with large In composition) has been demonstrated,²⁵⁶⁻²⁵⁸ however, the off-state performance is not low enough to meet the ITRS requirement, and is affected by the narrower bandgap of the

compound semiconductor and its higher dielectric constant compared to Si.²⁵⁹ To achieve a better gate control capability and bridge the gap between planar CMOS technologies and quantum transport devices, a new type of three-dimensional structure, FinFET, has been proposed⁶¹ and developed successfully on Si.^{37, 62-64} The multi-gate structure can effectively improve the transistor electrostatics characteristics by lowering the supply voltage, suppressing the leakage current and reducing the SCE through a full control of the potential inside the conducting channel. Moreover, the FinFET architecture introduces fewer changes to a conventional planar transistor design compared to surrounding gate transistors and multibridge-channel MOSFETs, two of the other three-dimensional competing technologies.^{61, 64, 260}

On the other hand, in order to sustain the CMOS technology development, the thickness of conventional gate dielectric (SiO₂) kept decreasing in order to increase the gate capacitance and thereby the drive current ($I = \mu CW/L$). However, the reduction of the thickness of the gate induced a dramatic current leakage increase which deteriorates the device reliability when its thickness shrinks below 2 nm. To overcome this issue, a higher permittivity (higher-k) material with a less critical thickness (larger than the physical limit) would ensure to increase the gate capacitance $C = \epsilon A/t_{ox}$, and thus decreasing the probability of leakage effect through the gate oxide. High-k materials are normally deposited by Atomic Layer Deposition (ALD) method, a unique thin film deposition technique that exhibits excellent conformity and reproducibility for the growth of high density and low impurity homogeneous films. Based on the separate sequential pulse and purge of different precursors, ALD films are exceptionally conformal and uniform with a thickness controllable

in the Å range, which can't be achieved in conventional CVD with various precursors existing simultaneously during the coating process.

The combination of Fin configuration and high-k dielectric have also been adopted in high mobility III-V transistors. FinFET made of InGaAs channel material epitaxially grown on InP substrates with high-k gate dielectrics exhibited a good SS^{-1} and an improvement of both the SCE and DIBL.^{67, 73} It is of great importance to integrate this type of III-V devices onto the well-established Si platform, which offers various opportunities for high-speed electronics and hybrid optoelectronic systems for data processing and on-chip communication. To date, this present work is among the first to report a fab-compatible hybrid integration process of III-V layers to insulator-on-Si and demonstrate the first InGaAs FinFETs on a Si substrate. The transfer of high quality InGaAs layers to SiO₂/Si is achieved through the formation of an interfacial nickel-silicide (NiSi) layer that fuses the III-V/Si substrate pair together. Undoped InGaAs FinFET devices fabricated on Si with a Fin perimeter (P) of 60 nm to 250 nm and a channel length (L_{ch}) of 35 nm to 950 nm exhibited lower short channel effects for longer channels and reduced perimeters. InGaAs FinFETs on insulator-on-silicon with nickel source/drain (S/D) contacts and L_{ch} =390 nm, P =60 nm yielded a SS^{-1} =165 mV/dec and I_{max}/I_{low} = 3.2×10^6 at V_{DS} =0.05 V. At V_{DS} =0.5 V and V_{GS} - V_T =0.5 V, the lowest $DIBL$ =8 mV/V and highest I_{on} =34.9 μ A/ μ m have been achieved in our devices. The overall integration scheme and the competitive FinFET performances for an undoped InGaAs channel demonstrate a significant progress towards the advanced hybrid integration of III-V devices on Si.

6.2 Integration of III-V materials and devices on Silicon

The combination of the advances in the III-V FET technology and the Si CMOS platform is currently intensely investigated as a primary route towards the replacement of the silicon channel by a III-V alternative channel yet on the mainstream fab-standard Si substrates.^{261,262} Two main strategies are traditionally considered for the large scale integration of III-V onto Si: the heterogeneous integration using bonding techniques of extrinsic III-V layers, or the bottom-up direct monolithic growth of III-V materials on Si substrates. Significant progress has been accomplished recently in the monolithic direct growth of III-V materials on Silicon through the intermediary of buffer layers thinner than 2 μm on a 4° offcut (100) Si.²⁶³ It was shown that the thickness of these buffer layers could be further reduced in the case of GaAs⁸ and InP⁹ by using specific epitaxial techniques called “necking” or “aspect ratio trapping”, which require the pre-patterning of the surface of the Si wafer at the micro/nanoscale prior to the growth. However, all these growth techniques are not yet optimal since III-V channels present a large concentration of defects near the silicon. On the other hand, the hybrid integration through bonding techniques including Smart Cut®,^{264, 265} and direct covalent wafer bonding based on oxide layers,^{226, 266, 267} require extremely smooth surfaces (the typical surface roughness should be ≤ 0.5 nm). However, this strict mandatory requirement results overall in a low yield at the industrial level. Other hybrid integration approaches exploit intermediate bonding layers such as eutectics²⁶⁸ and polymer²⁶⁹ layers. The former is not fully CMOS compatible due to the low melting temperature of typical alloys (e.g. with usually non-Si-compatible Au composition) used during the bonding process, while the latter is affected by the poor thermal conduction properties and generally limits the thermal budget during the device post-processing (e.g. the

formation of metal alloy contacts). Recent advances in the direct layer transfer upon epitaxial lift-off (ELO) of thin compound semiconductor films using sacrificial layers have shown an enormous potential for the large-scale integration of III-V materials on heterogeneous substrates for photovoltaic,¹⁷⁻²¹ LED¹⁷ and FET²² applications. Among the main advantages, ELO and bonding have proved to enable a large area transfer of various III-V crystalline compounds on Si, without limitations imposed by the usual lattice mismatch constraints and without requiring complex processing steps.^{17, 20-21}

Three kinds of bonding schemes were investigated in this work, including the direct integration of InAs to Ni on Si with a Ni/III-V interface, the direct bonding of an InAs layer to insulator-on-Si through the Smart Cut techniques (with a III-V/insulator interface), and the integration of a thin In_{0.53}Ga_{0.47}As layer to insulator on Si.

Nickel silicide and germanide are widely reckoned as low resistance contacts compared to the elemental metal contact formed by only an individual Ni layer evaporated on Si or germanium. They are the standard metal contacts for both nMOS and pMOS devices in the semiconductor industry.²⁷⁰ The good chemical stability and the low resistivity of silicide and germanide for both bulk and nanoscale devices indicate the potential of the implementation of other alloyed contacts for the fabrication of state-of-art devices. To date, metal/III-V alloys have been less examined regarding their metal atom diffusion kinetics, alloy phase, conductivity and temperature windows of the global reaction. A modest resistivity of the Ni-InAs alloy formed through the solid source reaction between Ni and InAs nanowire at an annealing temperature of 220- 300 °C has been first reported in the literature in 2008.²⁷¹ More recently, the Ni-InGaAs alloy has attracted the interests of researchers to promote a low contact resistance and allow the self-aligned S/D formation of thin film

transistors.^{68, 272, 273} From these starting points, we demonstrated that the Ni-InAs alloy could also be used as an intermediate layer to bond InAs on the Si platform.

SiO₂/Si substrate was first cleaned by acetone, isopropanol, deionized water, Piranha (H₂SO₄:H₂O₂=3:1) and rinsed in deionized water, followed by the electron beam evaporation of a Ti/Ni (10/250 nm) metal stack as illustrated in Figure 6.1a. Concurrently, solvents and diluted buffer oxide etchant (BOE) were employed to clean the InAs surface prior to the bonding process. Further to surface treatments of both wafers, the InAs surface was brought into contact with the Ni/Ti/SiO₂/Si substrate. The two stacked wafers then endured a 300 °C rapid thermal annealing process in a forming gas ambient (a mixture of H₂ and N₂) for 5 min, resulting in the formation of a Ni_xInAs alloy and hence the wafer bonding (Figure 6.1b). The cross-section SEM image in Figure 6.1c shows the formation of a Ni_xInAs alloy layer at the interface between the InAs and SiO₂ layers, proving thus that the Ni layer was totally consumed in the solid-state nickelide reaction. The thin Ti adhesive layer cannot be observed clearly in this image due to its small thickness (10 nm) and weak contrast difference with the nickelide layer. HR-TEM image displays the single crystal atomically abrupt interface between InAs and NiInAs, which is different from the one formed between Si and NiSi. This bonding approach establishes a new platform for the heterogeneous integration of direct bandgap III-V materials onto Si for low cost high performance Si-based solar cells, with the NiInAs as a low resistance back contact to the III-V cell. Moreover, one can also pattern the Ti/Ni metal stack into pre-defined back electrodes to form the self-aligned low resistivity contacts. Consequently, functional devices, such as bio-sensors, can be fabricated after excess materials removal and patterned etching.²⁷⁴

Figure 6.1 Bringing InAs substrate in contact with (a) Ti/Ni deposition on solvent cleaned SiO₂/Si substrate and annealing at 300 °C for 5 min for Ni_xInAs alloy formation leads to wafer bonding as shown in (b). (c) Cross-sectional SEM and HR-TEM showing the formation of a Ni_xInAs alloyed layer bounded between InAs and SiO₂ and full consumption of Ni in the nickelide reaction. HR-TEM images showing the atomically abrupt interface between pristine InAs and Ni_xInAs. The TEM image was taken by Dr. Wei Tang.

To enable the versatility in the design of III-V devices, the transfer of III-V materials to insulator on Si becomes necessary. The Smart Cut® technique for thin film exfoliation and bonding was first proposed and demonstrated in 1995,²⁶⁴ and can be decomposed into the following fabrication steps: the hydrogen ion implantation of wafer A, the hydrophilic bonding of wafer A to a wafer B, a heat treatment of the two bonded wafers to induce splitting of wafer A, and a fine polishing the surface in the end. This technique is widely used to produce commercially available silicon-on-insulator (SOI) wafers, since the hydrogen implantation conditions (dose, ion energy, implantation rate and temperature, and post thermal treatment) are quite tolerant. However, the tolerance window shrinks in the case of III-V compound materials, where undesired surface blistering and micro-bubble formation

can easily occur. Considerable efforts have been devoted to optimize the implantation conditions of most common binary III-V materials, i.e. GaAs,²⁷⁵ InAs,²⁷⁶ InP,^{277, 278} GaN,²⁷⁵ and AlN,²⁷⁵ in order to achieve a whole layer exfoliation. One step further, Dayeh *et al.* reported that InAs nanowires can grow vertically on a patterned InAs islands based on the transfer of a thin InAs layer on SiO₂/Si using the Smart Cut bonding technique, enabling thus the heterogeneous integration of III-V to the CMOS technology for hybrid information processing.²²⁶ Most recently, Czornomaz et al. demonstrated an ultra-thin-body InGaAs MOSFET on SiO₂/Si using Smart Cut technique presenting high-performance.²⁶⁵

Aiming to bond a hydrogen implanted InAs wafer to SiO₂/Si substrate using nickel silicidation, we first conducted *Stopping and Range of Ions in Matter* (SRIM) simulation to predict the projected range on two kinds of substrates, bare InAs and another with 90 nm Si₃N₄ on InAs. The wafers were tilted by 7° with respect to the direction of H⁺ ion beam, at 20 keV with the total number of ions of 1000 at room temperature. Ions penetrate into the substrate, and collide with lattice atoms while gradually losing their energy and finally stop penetrating into the substrate. However, if the incident angle is coincident with crystallographic directions that offer much lower stopping possibility than other directions, ions can travel long distance without collision and result in an uncontrollable dopant profile. As a result, a 7° between implantation direction and wafer are commonly used in the experiment, together with a screening oxide or nitride layer on top of the wafer to prevent the so-called ion-channeling described above. Figure 6.2a and c display the ion distribution inside the InAs and Si₃N₄/InAs layers, which illustrates the trajectory of all the ions inside. From Figure 6.2b and d, one can tell the projected ranges (average depth of the implanted

ions) in InAs and Si₃N₄/InAs are ~ 1687 Å and ~ 1462 Å, respectively, so that depth inside of the InAs from the Si₃N₄/InAs sample is ~ 562 Å.

Figure 6.2 SRIM simulation of H⁺ ions implanted at 20 keV with 7° tilt respected to the InAs and Si₃N₄/InAs substrates at room temperature. Ion distribution and ranges in (a)-(b) are for InAs, while (c)-(d) for Si₃N₄/InAs.

In our experiment, a SiN layer was deposited using a plasma enhanced chemical vapor deposition process (PECVD) on an InAs (111)B substrate pre-cleaned using solvents. Then the H⁺ ions implantation was conducted with a dose= 5×10^{16} cm⁻² at 20 keV with the substrate titled 7° respect to the ion trajectory by Dr. Yongquan Wang of Los Alamos

National Laboratory. The SiN layer was then removed in BOE to eliminate the deterioration by ions and the surface contamination during the handling process of this layer, followed by another SiN and Al₂O₃ insulating stack deposited on the implanted InAs surface by PECVD and ALD at temperature of 80 °C and 90 °C, respectively. After the evaporation of Ti/Ni layers, a rapid thermal annealing was conducted at 400 °C in a forming gas environment to achieve III-V/Si bonding through nickel silicidation formation (Figure 6.3a-c). During this process, a pristine InAs film can also be exfoliated from the donor substrate and transferred to the Si side. The cross-section SEM image shows the formation of a NiSi layer at the interface between the insulating layers and Si (Figure 6.3d). The Ni is totally consumed during this reaction, and the NiSi-Si interface is rough due to large lattice mismatch between these two layers. The HRTEM image of the transferred layer in Figure 6.3d depicts the InAs channel layer with its original crystalline structure. The combination of the H-implantation and epitaxial lift-off with nickel silicidation allows not only the integration of III-V materials to Si, but also the electrical isolation between diverse other III-V devices (photovoltaics, LEDs, transistors, etc.) on the same Si platform. However, a suspected dual projected ranges, evidenced from the appearance of H bubble formation at different depths in the InAs layer, prevented reliable full layer exfoliation and transfer (islands were transferred instead) and hindered our further device fabrication on this platform.

Figure 6.3 (a) Hydrogen implantation at a desired projected depth. (b) PECVD deposition of SiN and ALD Al₂O₃ on InAs followed by Ti/Ni atop. (c) Bring the materials in (b) intact and anneal to form a NiSi bonding layer with exfoliation of the InAs donor substrate. (d) Cross-sectional SEM showing the formation of a NiSi layer at the interface between the insulator layers and Si. Ni is totally consumed during this reaction, and the NiSi interface is rough due to lattice mismatch between NiSi and Si. HRTEM shows single crystalline InAs transferred by this technique.

Alternatively, a similar approach was developed based on a solid-state diffusion of Ni deposited on a dielectric layer capping the III-V surface into an exposed Si surface to form an interfacial NiSi bonding layer. This process is fully compatible with CMOS technology and could in principle straightforwardly be deployed to allow multiple substrate reuses. As shown in Figure 6.4, the starting substrate consists of an undoped InGaAs layer (50 nm) grown on bulk semi-insulating InP wafer.³⁰ HfO₂ and SiO₂ dielectric layers were then successively

deposited, followed by the e-beam evaporation of Ti/Ni metal layers.³¹ By exploiting the NiSi alloying process fabrication step, an InGaAs/InP wafer can be fused to a Si host substrate. For the purpose of demonstrating this new bonding approach, the bulk InP substrate was subsequently thinned by mechanical lapping and completely removed by wet etching using a HCl:H₂O (3:1) solution. It is worth noting though that the insertion of a sacrificial ultra-thin layer of AlAs or InAlP between InGaAs and InP in the initial heterostructure enables exploiting the ELO technique and reuse the InP substrate for subsequent epitaxial growth.^{17-19, 33} Transfer yield of such process was greater than 90% even for the largest 2 cm × 2 cm InGaAs sample we tested, where only the edges were found to be prone to exfoliation.

Figure 6.4 Schematic process flow of an all-solid phase wafer bonding for an undoped In_{0.53}Ga_{0.47}As layer to Si substrate. ALD HfO₂ (15 nm) followed by PECVD SiO₂ layers (200 nm) deposited on InGaAs for isolation and Ni diffusion barriers. A Ti/Ni (15/100 nm) stack is e-beam evaporated on top, and the whole structure was brought in contact with Si and annealed at 400 °C to form a NiSi bonding interface. The InP substrate was removed, leaving then an InGaAs layer on insulator on Si.

In conclusion, three types of integration approaches have been explored in this work, including the direct Ni-InAs bonding, the InAs Smart Cut®, and the Ni-Si induced bonding and InGaAs layer transferring process. By inserting one sacrificial III-V layer, the last approach could be improved to constitute a standard ELO process and reuse the bulk substrate for regrowth, allowing thus reduction of the whole cost of fabrication. Our InGaAs FinFET transistor processes developed in the following part are based on the last transferred InGaAs layer on insulator on Si technique.

6.3 III-V Fin fabrication

To obtain a conducting Fin channel, a fine etching technique is necessary to transfer the patterned structures defined during the lithography into the III-V layers or substrates. A full understanding of both wet etching and dry etching mechanisms are commendatory. Both approaches have their merits and drawbacks, which are discussed below.

Wet etching produces high etch rates and has a high selectivity with respect to the etch mask during the whole etching process steps, i.e. the liquid reactant (acid/base solution) diffusion, the surface reaction and by-product desorption processes. While most wet etching processes are isotropic with III-V semiconductor materials (equal etch rate in all the crystallographic directions), few anisotropic wet etching processes favoring faster etch in one specific crystalline orientation have been developed over the years but present a great challenge for large scale device processing. A mixture of oxidizing base or solution in mixture of acid (HCl, HNO₃, H₂SO₄, Citric Acid (C₆H₈O₇)) are commonly used for III-V

materials wet etching, and the etching directionality highly depends on the III-V surface orientation and ratio between solutions. As the device feature size decreases and the global aspect ratio and packing density increase, wet etching becomes increasingly challenging to meet the technological requirements.²⁷⁹

Alternatively, dry etching techniques using plasma discharges provides a reproducible anisotropic etching methods, especially for the development of high aspect ratio structures, and have become predominant in the semiconductor industry. Among the different dry etching technique developed lately, the Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) has become the industry standard for the transfer of micro or nano-patterns with smooth morphologies and vertical sidewalls into III-V semiconductors. This technique is derived from the original Capacitively Coupled Plasma RIE (CCP-RIE) technique but differs from it by the use of two independent radio frequency (RF) generators at 13.56 MHz: one is inductively coupled to a gas mixture creating a high density plasma (ICP) while the other one is applied to the electrode (also called platen or sample chuck) to induce a bias for the acceleration of the reactive ions (RIE) normal to the electrode. These two RF generators enable us to tune the ions density inside the plasma independently from their energy (Platen), which is not possible in a traditional CCP-RIE reactor where only one RF source is available. For clarity, the power generated by the ICP and CCP RF sources will be referred in the future as P_{ICP} and P_{RIE} respectively ICP-RIE is a flexible plasma etching technique combining simultaneously chemical and physical etch mechanisms: the gas-phase reactants (mainly free radicals) are chemically reactive inside the plasma and participate in gas-solid reactions at the wafer level giving the chemical characteristics to the etching while the energized positive ions of the plasma are accelerated by the bias potential at the surface of the wafer and bring

substantial kinetic energy by their bombardment of the surface, inducing thus a physical assisted etching.

The initial studies of III-V semiconductor etching was conducted in the early 1980's, involving molecular Cl_2 to etch GaAs.²⁸⁰ Chlorinated gases, including Cl_2 , BCl_3 , CCl_4 , CHCl_3 , and SiCl_4 , are commonly used for III-V etching, combined with high ionization energy gases such as N_2 , Ar, He, etc. for the physical etching component. Oxygen and hydrogen can also be used to alter the gas chemistry by increasing or decreasing the reactive neutral concentration. More recently, other gases, such as CH_4 ,^{281, 282} IBr ,²⁸³ HBr ,^{282, 284} have been successfully introduced and have proved to be suitable reactants for a smooth and vertical etch.

To fabricate a working FinFET device, the first step is to define the Fin structure. Although this step is identical to the gate fabrication in the conventional CMOS process framework with a lithography and etch sequence, many challenges still remains because of the extremely small Fin critical dimensions desired (the typical width size is sub-20 nm) combined with the stringent requirements regarding its thin line edge and low sidewall roughness. Electron beam lithography is the best candidate for Fins patterning at this stage because the resolution of photolithography is limited in the sub-micron range and nano-imprint is not mature enough at the initial stage of a new process. The mandatory use of the ebeam lithography implies that adequate electron sensitive positive or negative resist needs to be considered. Moreover, it is well established that ebeam resists hold a low selectivity towards plasma etching due to the ions bombardment, impacting the masking strategy for the definition of the Fins.

Poly(methyl methacrylate) (PMMA), a commonly used positive resist offering a high resolution and contrast, was first considered at the initial stage of Fin patterning. A 495PMMA C2 was initially spun on InAs (111)B at 4000 rpm for 40s with a ramping speed of 500 rpm/s. The Fin patterns were then defined by electron beam lithography using JEOL JBX-6300FS EBL system with a current of 200pA, an acceleration voltage of 100 kV and a base dose of 1500 $\mu\text{C}/\text{cm}^2$. After development in MIBK:IPA (1:3) and a 5 min long low power O_2 plasma cleaning (20W) to remove the potential contaminations from the resist on the surface of the wafer, a 40 nm thick Ti layer was deposited by electron beam evaporation and subsequently lifted-off in acetone. Ti was chosen because of its ability to be etched selectively from InAs using an HF solution, since the etchant for Ni, the widely used etch mask, usually erodes InAs. The narrowest Fin feature achieved using the process outlined above is 50 nm couldn't be obtained, while the Ti patterns with larger width remained on the substrate with a slightly rough line edge.

A chlorine-based dry etch process utilized previously for successful InAs etching²⁸¹ constituted the starting point of our investigation. This process consisted of a BCl_3/N_2 gas mixture with respective gas flow of 10 SCCM and 5 SCCM (SCCM denotes for Standard Cubic Centimeter per Minute) with P_{ICP} and P_{RIE} set as 500 W, and 25 W respectively. The temperature of the plate was fixed at 60°C and the etch time at 60 s. All the morphology and topology analysis in the following relies on SEM characterization. From the results shown in Figure 6.5a, no visible etching can be clearly observed. However, residues forming dark droplets on the SEM pictures are accumulated around the patterned structure and were suspected to be the by-products formed during the reaction between BCl_3 and Ti^{285} or InAs at this low temperature. Indeed, it has been shown that the dry etching of In-based material with

a Chlorine based plasma require the heating of the sample at high temperature ($\sim 200^\circ\text{C}$ depending on the plasma conditions) to make InCl_x products volatile at the pressure level.²⁸¹ Alternatively, a wet etch with a mixture of monohydrate citric acid ($\text{C}_6\text{H}_8\text{O}_7\cdot\text{H}_2\text{O}=1:0.829$) and H_2O_2 with the ratio of 20:1 led to the isotropic etching of InAs with an undercut profile observed below the etch mask, as exhibited in Figure 6.5b. Hence, the masking strategy consisting of using a metal layer as hard mask does not give any satisfaction towards the fabrication of Fin in InAs. Other masking methods have to be considered.

Figure 6.5 (a) Dry etch on Ti masked InAs (111)B substrate showing nearly unetched pattern profiles probably due to by-products either from the reaction with Ti or InAs. (b) Wet etching with Ti masked InAs (111)B sample displaying an undercut, indicating an isotropic etching with the similar etching rate in both vertical and horizontal directions.

Two strategies are available to potentially overcome these limitations:

1. The first one relies on the use of an intermediate dielectric layer such as SiO_2 or SiN_x as hard mask since they present a higher selectivity towards the chlorine-based dry etching process. Planar SiO_2 or SiN_x can be first deposited on top of the III-V surface by a standard PECVD. A negative or positive ebeam resist is then used to define the Fin patterns

and serve as a first etch mask for the SiO₂ or SiN_x dielectric layer. Once the Fin structure is transferred into the hard mask, the remaining ebeam resist can be stripped by O₂ plasma.

2. The second method consists of using a highly etching resistant negative resist as an etch mask, such as the commercial NEB-31A, the hydrogen silsesquioxane (HSQ) and the SU-8.²⁸⁶

The first method proposed adds more complexity and one more fabrication step which can damage the existing process flow by introducing uncertainties regarding the critical dimension of the Fins patterns during the transfer into the dielectric layers (oxide and/or nitride layer etching). On the contrary, the second approach is more straightforward and satisfies the fabrication requirements for FinFET. Hence, in the following we will only consider a highly selective negative resist as etch mask in the whole developed process.

Resists presenting a high selectivity regarding dry etching techniques are the best etch mask candidates in the top-down process network. High resolution and line edge roughness are the basic requirements for the achievement of nearly perfect vertical sidewalls with smooth morphology. During the optimization of the etching conditions, a photoresist AZ5214E was first considered due to the already existing exposure recipe and its high throughput. After exposure and development, the resist is hard baked at 110 °C for 30 min to strengthen it so it can avoid the plasma induced erosion. Considering the dry etch process described previously (Figure 6.5a) as a starting point, an exhaustive study on the etching conditions was performed by tuning all the plasma parameters, including the chamber pressure, gas flow, RIE power, ICP power, temperature and time. It is needed to understand the process of RF discharges, the gas phase chemistry, the reactants and by-products

transport process, the diffusion of both ions and electrons, as well as the surface chemistry at the etch interface. To reach the right plasma conditions, the parameters of the etching recipe were varied between a chemical etch dominated region and a physical etch controlled region. Totally different surface morphologies can be achieved depending on the recipe conditions as illustrated in Figure 6.6, corresponding to the etching condition shown in Table 6.1.

The chamber pressure is one of the key parameter in plasma processing and has a direct impact on the etching regime. At lower pressure (4 mTorr), the global ion energy impinging at the surface of the sample increases due to the higher average free path of molecules/ions and the lower number of collisions in the plasma. Hence the physical component is predominant compared to the active chemical reaction. In combination with high BCl_3 flow, byproduct polymer is deposited on the sample surface, acting as nano masks for dry etch, leading to the grassy surface consequently (Figure 6.6a).²⁸⁷ Conversely, at high pressure (≥ 10 mTorr in this case), the plasma potential decreases and thus the physical sputtering decreases, in combination with the enhanced chemical assisted etching from high density of chemical radicals on the sample surface, a surface with dense and large humps are expected as shown Figure 6.6b.

Reactants flows, together with the RIE and ICP powers are other parameters affecting the quality of the etching. While keeping the same pressure in the chamber reactor, Figure 6.6a and c presents distinct difference regarding the sample surface roughness. An high concentration of inert gas (Ar in this case) and an elevated RIE power leads to a more physical reactive etching, where the surface is cleaner but the sidewalls are more slanted (Figure 6.6c). The high concentration of inert gas modifies the concentration of the chlorine reactive species, both ions and radicals, and globally lowers them. With both a low inert

reactants flow and RIE power in combination with a high BCl_3 flow and high ICP power, the scattering collision of ions increases and incident ions obtained a large angular spread, causing an undercut or lateral etch (Figure 6.6a).²⁸⁸

The sample temperature also plays an important role in III-V etching, especially for In-based compounds. The formation of a non-volatile etch product (InCl_3) on both sidewall and surface results in a non-uniform etching, and in worst cases such non-volatile products can even act as a micro mask.²⁸⁹ It is suspected that the droplet-like residues exhibited in Figure 6.6, which is generally observed at low temperature etching in our experiment, are these non-volatile by-products. By elevating the etching temperature or further increasing the ion bombardment, desorption and removal of InCl_3 can be accelerated.

Table 6.1 Etching recipes for results shown in Figure 6.6. (a) and (b) are mainly working in chemical reaction limited regime, while (c) is in physical etch dominant region.

Recipe	Pressure (mTorr)	BCl_3 (sccm)	Ar (sccm)	RIE (W)	ICP (W)	T (°C)	Time (s)	Etch depth (nm)
a	4	20	9	90	500	120	60	~550
b	10	10	5	90	500	120	30	~270
c	4	7	20	300	400	60	60	~550

Figure 6.6 Etching on InAs substrate under conditions corresponded to those in Table 6.1 using photoresist as the etch mask.

Different parameters combinations were evaluated to optimize the etching process in InAs. A good combination allowing a physical etch process was finally found and the plasma parameters are summarized in Table 6.2. The time dependence of this etching was then investigated. The Fin profiles displayed in Figure 6.7 corresponds to an etching time of 40 s, 20 s, 15 s and 10 s. The negative electron beam resist HSQ (XR-1541-004) with a thickness of ~ 90 nm was used as the etch mask in this experiment. A 40 s etch completely removed the fin pattern and only left the holding pads as shown in Figure 6.7a. The violent ion bombardment deteriorated the HSQ mask after 400 nm InAs etch, indicating the selectivity of this layer is weak regarding the BCl_3/Ar etch. By decreasing the etch time to 20 s, vertical sidewalls presenting a smooth surface morphology with only a few damages near the base of the Fin has been observed. Aiming at a 200 nm in Fin height, the etch time was further reduced. Figure 6.7c-d show samples with an excellent morphology and the remaining of the etch mask after 15 s and 10 s etch, respectively. In Table 6.2, the InAs etch rate first increases when increasing time duration and then decreases at the time of 40 s. At the initial stage, the temperature inside the chamber raised as time increased (the He cooling system on the sample holder, so that the back of the substrate is fixed at the temperature targeted), leading to an enhancement of chemical reaction and hence an increase of the nominal etch rate. However, when the etch reaches the chemical reaction-limited region, because of the non-volatile by-products accumulation, the etch rate started decreasing again and the surface deterioration of the sidewalls became pronounced.

Table 6.2 Etching recipes for the results shown in Figure 6.7

Recipe	Pressure (mTorr)	BCl_3 (sccm)	Ar (sccm)	RIE (W)	ICP (W)	T (°C)	Time (s)	Etch depth (nm)	Rate (nm/s)
a	10	3	20	225	350	60	40	~395	9.875
b							20	~290	14.5
c							15	~195	13
d							10	~110	11

Figure 6.7 Time dependence of InAs etching using the same etch recipe. (a) 40 s, (b) 20 s, (c) 15 s and (d) 10 s.

After tuning the dry etching process for InAs Fins, we further investigated the plasma etching of InGaAs on an InP substrate (200 nm InGaAs layer epitaxially grown on semi-insulating InP). Since both of the epilayers contain In and As elements, it was expected to achieve similar results with the same exact etch recipe. However, the dry etch system encountered some technical problem during the series of experiments and couldn't be stabilized at high RIE power anymore. From the previous InAs study, we knew that the recipe with low RIE power and with BCl_3 and Ar precursors usually lead to rough surface, which is also demonstrated in the case of InGaAs. As a result, a new recipe with low RIE power combined with Cl_2 and N_2 had to be developed to overcome this issue. We evaluated three types of recipes derived from one existing process optimized for InGaAsP on this dry etch system. The parameters of the three different etch ICP-RIE processes are summarized in Table 6.3. For the sample (a) a mixture of Cl_2 and N_2 was used with a RIE power of 30 W, an ICP power of 230 W at the temperature of 60 °C. The corresponding result is displayed in Figure 6.8a. The Fins sidewall morphology is hazy under the SEM, etching residues are accumulated around the Fin base as well as on the planar surface as can be seen in the inset. It is suspected that these residues are polymers compounds detached from the chamber walls or the by-products of the etching reaction. O_2 plasma is commonly used in lithography processes to remove the organic residues, hence we considered adding O_2 inside the reactants. Adding O_2 flow in the whole process resulted in a quite slanted but clean surface and a slow etch rate, highlighting the passivation and cleaning effects brought by O_2 (result is not shown here). Subsequently, a two-step etching process was proposed, with a first normal etching recipe to create the vertical sidewall first, followed by a second short time recipe where O_2 was added to clean the surface. As shown in Figure 6.8b, the surface is quite clean; however,

one can observe a line boundary coming from this two-step process in the inserted higher magnification image, which is not acceptable for the fabrication of Fins. Indeed, any angles in the sidewall profiles leads immediately to a variation across the electrical width of the device, thus, changing the threshold voltage across the width of device and deteriorating the subthreshold characteristics. Instead, we switched to a process with O₂ plasma only in the second step in order to remove the residue without attacking the Fins (Table 6.3c). As a result, the clean surface and sidewall morphology can be noticed in both Figure 6.8c and its inset.

Table 6.3 Etching recipes for the InGaAs results shown in Figure 6.8. (a) Single-step etching, (b) Two-step etching with O₂ flow added in the second step, and (c) Two-step etching with O₂ plasma as the second step.

Recipe	Pressure (mTorr)	Cl ₂ (sccm)	N ₂ (sccm)	O ₂ (sccm)	RIE (W)	ICP (W)	T (°C)	Time (s)	Etch depth (nm)
a	4	2	20	0	30	230	60	70	70
b	4	2	20	0	30	230	60	215	<200
	4	6	20	2	40	350	60	70	
c	4	2	20	0	30	230	60	60	~50
	-	-	-	2	-	200	60	40

Figure 6.8 Etching recipe for InGaAs (a) single-step etching without O₂, (b) two-step etching with O₂ as the reactant in second step, and (c) two-step etching with O₂ plasma for the second step.

Previous studies were carried out on III-V bulk substrate before bonding, while the

final FinFET fabrication on III-V on Si will be elaborated here. After transferring the InGaAs layers onto the Si substrate, the 3D device fabrication proceeded by defining arrays of 5 or 10 parallel InGaAs Fins with width ranging from 20 to 200 nm by electron-beam lithography. Negative electron beam resist HSQ was used as the etch hardmask for the Cl_2/N_2 inductively coupled plasma etching of the InGaAs Fins. After the dry etch, the HSQ etch mask was removed by O_2 plasma and dilute buffered oxide etchant (BOE wet etching) solution. The final height of the InGaAs Fins was reduced to 35 nm. S/D contacts were then patterned and a layer of Ni was deposited as electrodes. After lift-off, the native oxide of the InGaAs Fins was removed in diluted BOE in order to passivate the surface with sulfur by dipping the sample in a 10% $(\text{NH}_4)_2\text{S}$ solution for 10 min.³⁴ Extensive systematic studies of the capacitance-voltage characteristics of the HfO_2 layer on III-V substrates were conducted to reduce the leakage current and improve the interface quality (Section 6.4). A 5 nm thick HfO_2 layer was then deposited by ALD at 200 °C, with an equivalent oxide thickness (EOT) of 1.11 nm. Overlapping gate electrodes were finally aligned and patterned by electron beam lithography, followed by Ni metal deposition. The resulting devices consisted in arrays of InGaAs FinFETs with 5 or 10 parallel channels with channel length L_{ch} varying from 35 to 950 nm. All the dimensions discussed here were determined by SEM measurements.

Figure 6.9 Schematic and fabrication process flow of an undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel FinFET based on an all-solid phase wafer bonding for III-V substrates to Si. Fin structure were patterned and etched into an InGaAs layer on insulator on Si. After S/D Ni deposition and lift-off, pre-gate surface treatment using 10% $(\text{NH}_4)_2\text{S}$ followed and 5 nm ALD HfO_2 and Ni metal gate were deposited.

To investigate the directionality of the dry etching in both InAs and InGaAs, a cross-sectional TEM was performed. The HSQ layer was removed by cyclic O_2 plasma runs, dilute buffer oxide etch (BOE) and deionized water cleaning. A thin layer of Pt was deposited in-situ on the samples with the FIB system under a low ion current to avoid the ions damage on the surface of the sample across the gated region, followed by the removal of materials beside our targeting region by ion milling. A nano-manipulator was used to lift the thin slab out from its original substrate and mount it on a TEM grid. Finally, a slab thinning step is carried out to achieve the final thickness of ~ 100 nm or below for the HR-TEM purpose. Low resolution TEM images are shown in Figure 6.10: (a) represents ~ 135 nm thick InAs Fins on the bulk InAs substrate, and (b) features 40 nm thick InGaAs fins on $\text{HfO}_2/\text{SiO}_2/\text{Ti}/\text{NiSi}/\text{Si}$. The InAs sidewall is slanted because of the slightly deeper etch depth and low temperature conditions using the recipe in Table 6.2. InGaAs Fins exhibit a slight

rounded top surface caused by the etch mask deterioration during the dry etching process performed with recipe c in Table 6.3. The round shape presents some advantages compared to a perfect rectangular shape, which may get high electric fields and produce reliability issues at the corners.

Figure 6.10 Cross-sectional TEM images of (a) three InAs fins on bulk InAs with gate dielectric and tri-gate atop, (b) three finished InGaAs FinFETs with gate dielectric and tri-gate atop showed the whole structure of the devices on Si.

A full understanding of the role of the different parameters of the plasma enables a well-controlled etching of the Fins that present vertical sidewalls and smooth surface morphologies. This fabrication step is the first and most critical step for the fabrication of high performance FinFET devices. After the Fin definition, the high-k dielectric layer is investigated constituting the gate in the following section.

6.4 ALD optimization of high-k dielectrics for III-V transistors

To evaluate the quality of the dielectric layer and the interface between the dielectric and the metal gate, MOS capacitors are used as benchmarks. MOS capacitors constitute the key part of the MOSFET and consist of a semiconductor substrate, a dielectric layer, and a metal electrode (*gate*). The MOS capacitors characteristics are determined by Capacitance-Voltage (*C-V*) and Current Density-Voltage (*J-V*) measurements. Normally the dielectric layer is deposited and covered the whole surface of semiconductor substrate, followed by the metal electrodes patterned on top. Another layer of metal is deposited on the backside of the substrate acting as ohmic contact as shown in Figure 6.11a. Depending on the bias applied across the electrodes, the capacitor can operate in different regimes. When the gate voltage is positive and greater than the flatband voltage, the electrons are accumulated at the oxide-semiconductor interface (Figure 6.11b). The n-type MOS capacitor is then in accumulation regime, and the capacitance is defined as $C = C_{ox} = \epsilon_{ox}/t_{ox}$. When the gate voltage is lower than the flatband voltage, the capacitor operates in a depletion regime where the majority carriers are pushed away from the oxide-semiconductor interface, forming a depletion layer (Figure 6.11c). In this regime, the depletion region capacitance ($C_{dep} = \epsilon_{semi}/W_{dep}$) becomes more appreciable with the increasing depletion width, resulting in the total capacitor

equivalents to C_{ox} in series with C_{dep} . If the gate voltage keeps decreasing until the threshold voltage (V_{th}) and below, a sheet of minority carriers will form at the interface, commonly named as inversion layer, preventing the depletion layer to further expand. The minority carriers can be generated and recombined near the oxide-semiconductor interface in response to low frequency AC signal, leading to a total capacitance equal to C_{ox} (Figure 6.11d); whereas at high AC frequency, the minority carrier density is fixed with the DC bias and the depletion width fluctuates, resulting in C_{ox} and C_{dep} in series, as illustrated in Figure 6.11e. The ideal C-V relationship at both high and low frequency of an nMOS capacitor is shown in Figure 6.11f.

Figure 6.11 C-V characteristics for a NMOS capacitor. (a) Basic structure. (b) When $V_g > V_{fb}$, the capacitor works in the accumulation region with electrons accumulated at the oxide-semiconductor interface and $C = C_{ox}$. (c) When $V_t < V_g < V_{fb}$, capacitor works in

depletion region where $C = 1 / (1 / C_{ox} + 1 / C_{dep})$. When V_g further decreases below V_t , capacitor works in inversion region with $C = C_{ox}$ at low frequency in (d) and $C = 1 / (1 / C_{ox} + 1 / C_{depmax})$ at high frequency in (e). (f) Ideal C-V curve for NMOS capacitor.

The interface chemistry between high-k materials and III-V semiconductors is more complex than of the Si/SiO₂ system, especially because of the fast growing native oxide and on the III-V surface and the interfacial defects. High interface state density (D_{it}) and fixed oxide charge density (Q_f) are the detrimental effects on the device performance, which could be ultimately reduced through surface passivation of the high-k/III-V interface and post forming gas annealing.^{74, 290} To achieve a good interface quality and a small equivalent oxide thickness (EOT), intensive studies of ALD of HfO₂ on Si, InAs and InGaAs/InP have been carried on. The dielectric constant of HfO₂ is around 25, ~6.4 times than the one of SiO₂ (3.9). Hence the thickness of the HfO₂ gate could be ~6.4 times higher than the equivalent layer of SiO₂ presenting the same capacitance, but with thicker barrier for tunneling gate current. Each ALD cycle is composed of four distinct subsequent steps: one pulse of 75 °C Tetrakis(dimethylamino)hafnium (TDMAH), one purge of the chamber with a N₂ flow to remove the unreacted precursors and by-products, one pulse of 20 °C H₂O at and one final purge with N₂. Our study focused on the optimization of the deposition temperature, the growth precursor pulse time (H₂O and TDMAH), and the ex-situ and in-situ plasma treatment methods. An Al layer was used as the global bottom contact on a highly doped p-type Si and planner Ni for back contact of InAs. Ni was patterned on top of both substrates and acts as top contacts.

The investigations of the HfO_2 features were mostly performed on the less challenging Si substrate to adjust its basic insulating properties prior to optimizing the $\text{HfO}_2/\text{III-V}$ interface. Si was pre-treated with HF, rinsed in deionized water and immediately loaded into the ALD chamber. Figure 6.12 illustrates the temperature dependence leakage current density through 15 nm HfO_2 on Si. From 185 °C to 200 °C, the leakage current first decreases when the deposition temperature increase, and stabilize at a lower level for temperatures located between 200 °C and 250 °C. When the temperature reaches 300 °C, the leakage current increases dramatically. Consequently, the deposition temperatures of 200 °C and 250 °C were chosen in the optimizations of the other parameters.

Figure 6.12 Leakage current density through ALD HfO_2 on Si substrate decreases with deposition temperature rises from 185 °C (a) to 200 °C (b) and stays almost unchanged when

it further increases to 250 °C (c). When the temperature reaches 300 °C (d), the leakage current density increases dramatically to 1 A/cm² range.

Continuous leakage current study was carried out on Si substrate. While keeping the deposition temperature constant at 200 °C and the H₂O purge at 40 s, the influence of the H₂O pulse duration was investigated (Figure 6.13). As shown on the curves, the leakage current density first drops and then increases with the rise of the pulse time. As a result, the optimal condition enabling to minimize the minimum leakage current corresponds to a H₂O pulse duration of 0.3 s.

Figure 6.13 Studies of the impact of H₂O pulse time (a) 0.1 s, (b) 0.3 s, and (c) 0.5 s, on leakage current through 15 nm ALD HfO₂ on Si substrate showing the optimal time of 0.3 s (b) with the purge time of 40 s at 200 °C.

When switched to III-V material, the high-k/III-V interface is critical for the FET characteristics and performance. Normally, Al₂O₃ is used as the sole high-k dielectric in III-V transistors or as an intermediate layer between higher-k dielectric and the III-V material, which could effectively improve the interface quality.⁶⁷ In the case of our HfO₂ gate dielectric, ex-situ surface preparation methods, including diluted HF only, HCl only, HCl and (NH₄)₂S, O₂ plasma and diluted BOE, and diluted BOE and (NH₄)₂S, have been studied but

were not sufficient to display an obvious suppression of the leakage current on an InAs(100) surface. Alternatively, the in-situ treatment inside the ALD chamber was then investigated. The InAs samples were treated with diluted BOE, deionized water, 10% $(\text{NH}_4)_2\text{S}$, and deionized water, and were then immediately loaded into the ALD chamber with the temperature held at 200 °C. 5 cycles of alternating Trimethylaluminum (TMA) (stabilized at 20 °C with pulse/purge time of 0.4/5 s) and H_2 plasma (10 s H_2 gas stabilization time before 2 s ‘plasma-on’ time at 100 W ICP power, followed by 5 s purge time) were performed inside the ALD chamber prior to the HfO_2 growth.²⁹¹ Figure 6.14 illustrates the leakage current density difference between with and without this in-situ treatment on InAs substrate. Ex-situ studies were repeated in combination with this in-situ treatment, while the recipe of diluted BOE, deionized water, 10 min 10% $(\text{NH}_4)_2\text{S}$, and deionized water provided the smallest leakage current.

Figure 6.14 Suppression of leakage current through 15 nm HfO_2 on InAs after 5 cycles alternating TMA and H_2 plasma in-situ treatment in (b) compared with samples without this in-situ treatment in (a).

Employing the best H_2O pulse time and the best ex-situ, in-situ surface treatment methods, further investigation was carried out in terms of HfO_2 ALD deposition temperature

on InAs(100) surface. Two temperatures of 200 °C and 250 °C were utilized for the studies of C-V characteristics on the InAs sample, which were demonstrated to exhibit lower leakage current densities on Si surfaces as shown in Figure 6.11. As shown in Figure 6.15a, almost no modulation of the carriers was observed in case of ALD HfO₂ deposited at 200 °C on InAs. For the HfO₂ film deposited at 250 °C, typical C-V curves showing accumulation, depletion and inversion regimes of the MOS capacitor, were observed in Figure 6.15b. The relative dielectric constant could be calculated based on $C_{acc} = C_i = \epsilon_i / t_i$, we obtain:

$$\epsilon_{HfO_2} = C_{acc} \cdot t_{HfO_2} / \epsilon_0 = 1.03 \cdot 10^{-6} F / cm^2 \cdot 15 \cdot 10^{-7} cm / (8.854 \cdot 10^{-14} F / cm^2) \gg 17.5.$$

Figure 6.15 C-V characterization of 15 nm HfO₂ on InAs grown at different temperatures of 200 °C (a) and 250 °C (b), in which (b) shows a reasonable C-V curve indicating clear carrier accumulation, depletion and inversion regions.

Additional optimization of the TDMAH pulse time was studied with a fixed purge time of 15 s, deposition temperature of 250 °C, H₂O pulse/purge time of 0.3/40 s, and best ex-situ and in-situ plasma treatments determined from the studies on HfO₂/InAs interfaces discussed above. In our system, the injection of TDMAH is controlled by a booster function,

which includes 0.8 s for pre-empty time and 1.2 s for master fill time for the case of total pulse time of 1.9 s (this is the original pulse time in the recipe, which was used for all the studies mentioned above). The actual TDMAH pulse time is approximately 0.1~0.3 s. When we decreased the pulse time, we simultaneously scaled the time of all other steps in the booster function. Figure 6.16 exhibits the C-V characteristics of various TDMAH pulse time, where Figure 6.16c shows the best C-V characteristics with least dispersion in the accumulation regime and the highest normalized capacitance indicating highest high-k dielectric constant than those in Figure 6.16a-b.

Figure 6.16 C-V characteristics for different TDMAH pulse times. (a) 0.9 s (b) 1.4 s, and (c) 1.9 s. Better C-V characteristics or HfO₂/InAs interfaces were obtained at higher TDMAH pulses slightly improved dielectric constant for 1.9 s pulse time.

The optimal HfO₂ deposition condition is slightly different on the InAs substrate compared with the InGaAs substrate, where 50 nm undoped InGaAs is grown on semi-insulating (SI) InP(100) (grown by Intelligent epitaxy). Concentric circle patterns were employed in the C-V measurements because back contact couldn't be employed on the SI InP. Considering the compatibility in InGaAs FinFET gate last process, we have to avoid the formation of Ni-InGaAs alloy starting at 250 °C because pre-gate treatment in BOE will etch away the alloyed extension. Therefore, a 5 nm thick HfO₂ layer on InGaAs at 200°C with all

the other optimized criteria was deposited and characterized, and the results are shown in Figure 6.17. The entire accumulation regime was not observed due to the lower voltage sweep range from -1 V to 1 V compared to those used for InAs above, but a distinctive depletion regime was clearly obtained and these deposition parameters were then adopted in our FinFET fabrication process.

Figure 6.17 C-V curve of 5 nm HfO₂ deposited at 200 °C on undoped InGaAs on SI InP.

6.5 FinFETs transport properties

The whole structure of the first InGaAs FinFETs on insulator on Si is illustrated in Figure 6.18a in the form of a cross-sectional TEM image (along A-A' cut in Figure 6.9), showing the whole structure of three finished InGaAs FinFET devices on a stack of HfO₂/SiO₂/NiSi/Si. Figure 6.18b depicts a HRTEM image of a tri-gated InGaAs FinFET (13 nm top width and 36 nm slanted sidewall lengths) retaining single crystal quality (Figure 6.18c) with 5 nm conformally covered HfO₂ gate dielectric on the Fin top and sidewalls. The

bottom HfO₂ layer is used as a post-anneal HF-etch stop layer in our process and displays a polycrystalline structure (Figure 6.18d) due to high temperature used in NiSi bonding formation. The HfO₂ crystallization led to electrical shorts in devices made without SiO₂ layers where current paths between the FET device leads on top and through the HfO₂ to the NiSi layer and then to the electrode leads were created. The leakage through HfO₂ necessitated an insertion of a SiO₂ layer underneath for electrical isolation from the underlying NiSi layer. Cross-sectional TEM images of five final FinFET devices in Figure 6.18e-i demonstrate the same height of 35 nm with perimeter variation of 60 nm, 85 nm, 100 nm, 130 nm and 150 nm, where the slanted sidewall mainly comes from the HSQ mask sidewall erosion during plasma etching. Better etch mask will help make the Fin sidewall more vertical.

Electrical performance of all devices was measured after 5 min rapid thermal annealing at 200 °C in forming gas (H₂/N₂ mixture) ambient. The transfer characteristics of a representative device with ten InGaAs FinFET channels with $L_{ch}=390$ nm, $P=60$ nm are shown in Figure 6.19, where the current is normalized by the perimeter of the Fins, measured by TEM, and by the number of channels. This device exhibited an $I_{on}=18$ μ A/ μ m at $V_{DS}=0.5$ V and $V_{GS}-V_T=0.5$ V, where the threshold voltage $V_T=0.78$ V is extracted by the linear extrapolation of the maximum transconductance (g_m).³⁵ The on-current of these devices is limited by the contact series resistance due to the Schottky barrier nature between the Ni S/D contacts and the undoped InGaAs, which is also responsible for the increment of I_{DS} in the negative V_{GS} region from hole transport.³⁶⁻³⁷ An SS^{-1} of 165 mV/dec and a maximum current sweep ratio (I_{max}/I_{low}) of 3.2×10^6 at $V_{DS}=0.05$ V were observed. The interface quality for these FinFET devices on Si compares well to those on InP³⁸ and lags

behind some others with Al_2O_3 interfacial gate dielectric layers.²⁷ The gate leakage is as low as $10^{-6} \mu\text{A}/\mu\text{m}$ in all the V_{DS} cases.

Figure 6.18 (a) Cross-sectional TEM image of three finished InGaAs FinFETs with gate dielectric and tri-gate atop showed the whole structure of the devices on Si (Figure 6.9 A-A'). (b) HRTEM of a completed single InGaAs FinFET showing conformal amorphous 5 nm HfO_2 gate dielectric on top (13 nm), left (36 nm), and right (36 nm) edges of the Fin with Ni gate atop. Zoom-in images in (c) and (d) illustrate the preserved single crystal InGaAs channel after bonding and bottom crystallized HfO_2 formed during NiSi bond formation, respectively. Panels (e)-(i) depict the cross-sectional TEM images of FinFETs with various three side perimeters of 60 nm, 85 nm, 100 nm, 130 nm and 150 nm.

Figure 6.19 Measured transfer characteristics of an InGaAs FinFET on Si with $P=60$ nm and $L_{ch}=390$ nm at different V_{DS} biases showing the highest I_{max}/I_{low} of 3.2×10^6 and SS^{-1} of 165mV/dec at $V_{DS}=0.05$ V.

Figure 6.20 compares the normalized output and transfer curves for devices with the same $P=60$ nm of various $L_{ch}= 890$ nm, 690 nm, 500 nm, and 160 nm. Shorter channel length devices exhibit higher drive current (Figure 6.20d), more severe SCE, larger off current and worse SS^{-1} (Figure 6.20h), while the on-state performance does not scale linearly with L_{ch} due to large S/D contact resistance. With decreasing Fin perimeter for the same $L_{ch}=690$ nm, I_{DS} enhancement was observed as shown in Figure 6.21a-d. Such enhancement has been attributed to increased quantum confinement and increased carrier mobility resulting from reduced interface scattering.³⁹ In addition, the transfer curves indicate an improved SS^{-1} and on/off characteristics with decreasing perimeter as shown in Figure 6.21e-h.

Figure 6.20 (a)-(d) Output curves of InGaAs FinFETs with the same $P=60$ nm of different $L_{ch}= 890$ nm, 690 nm, 500 nm, and 160 nm showing an increasing current and worse saturation characteristics as the channel lengths decreased. The V_{GS} is varied from 0 to 2 V in steps of 0.5 V. The transfer curves of the same devices as described in (a)-(d) are depicted in (e)-(h). Scale bars of all inset SEM images are 1 μm .

Figure 6.21 When L_{ch} fixed to 690 nm, (a)-(d) illustrate the output and transfer characteristics of devices with different perimeters of 150 nm, 130 nm, 100 nm, and 60 nm, where larger on-current and better transfer properties (e)-(h) are measured at lower perimeter. Scale bars of all inset SEM images are 1 μm .

The scaling metrics for InGaAs FinFETs on insulator-on-Si with various gate lengths and Fin widths are summarized in Figure 6.22, including SS^{-1} , V_T and DIBL. Figure 6.22a shows that SS^{-1} is degraded for all V_{DS} values with reducing L_{ch} from 900 nm to 150 nm, and a higher SS^{-1} is observed for higher V_{DS} , as expected, due to SCE (Figure 6.22a). The lowest SS^{-1} of 150 mV/dec is obtained at $V_{DS}=0.01$ V for the device with $L_{ch}=390$ nm and $P=60$ nm. For a variable perimeter with same $L_{ch}=450$ nm depicted in Figure 6.22b, SS^{-1} improves dramatically from 420 mV/dec to 160 mV/dec with decreasing perimeter from 150 nm to 60 nm at $V_{DS}=0.01$ V. Channel length scaling that's immune to SCE can be achieved by narrowing the Fin width. Figure 6.22c exhibits impact of L_{ch} (35 nm to 700 nm) and perimeter (60 nm to 150 nm) on V_T , where V_T is obtained from the transfer characteristics in linear operating regime at $V_{DS}=0.5$ V. There is a slight increase of V_T with L_{ch} for all perimeters from 60 nm to 150 nm, but it increases dramatically with decreasing perimeter, pulling the device into a desired enhancement mode operation. With L_{ch} of ~ 400 nm, and as P increases from 85 nm to 150 nm, a negative shift in V_T of 1.4 V is required to deplete the channel. This trend is confirmed for $P=85$ nm, 100 nm, 130 nm, and 150 nm. For $P=60$ nm, V_T was found to be close to that of $P=100$ nm, both of which have a circular cross-sectional perimeter at the top portion of the Fin, compared to all other Fins. However, process variations cannot be excluded to explain this similarity. Figure 6.22d shows that the DIBL increases with reduced L_{ch} due to SCE, and this effect is suppressed by decreasing P as indicated in Figure 6.22d. DIBL degrades from 8 mV/V to 410 mV/V when L_{ch} decreases from 925 nm to 180 nm with P of 130 nm, while it decreases from 265 mV/V to 115 mV/V when P varies from 130 nm to 60 nm with the same L_{ch} of 400 nm. These metrics indicate that devices with longer L_{ch} and smaller P will have improved SS^{-1} , DIBL and I_{on}/I_{off} without

suffering much from SCE. More sophisticated processing, including retrograde channel doping,³⁸ decreasing EOT⁴⁰ (Supporting Information), gate first, self-aligned S/D³⁶ and utilizing gate all around 3D structure,²⁷ could help improving the gate control of the channel and further suppressing the SCE.

Figure 6.22 (a) SS^{-1} scaling metrics regarding of V_{DS} for InGaAs FinFETs on Si ($P=60\text{ nm}$) showing decreasing SS^{-1} with increasing L_{ch} . (b) Improved SS^{-1} properties obtained with P shrinking at fixed $L_{ch}=450\text{ nm}$. At high $V_{DS}=1\text{V}$, the more degraded SS^{-1} are observed in both (a) and (b) than those at lower $V_{DS}=0.01\text{ V}$. (c) Linear extrapolated V_T with various L_{ch} and P demonstrating a shift from higher V_T to lower V_T with increasing P , while V_T at the same P stays almost unchanged with L_{ch} . (d) DIBL scaling metrics with L_{ch} down to 35 nm and P of 60 nm , 85 nm and 130 nm .

Furthermore, SS^{-1} and DIBL dependence on the thickness of HfO_2 on FinFET devices with a fixed perimeter of 60 nm were investigated. Figure 6.23 summarizes the improved characteristics with thinner HfO_2 of 5 nm compared to those with thicker 7.5 nm HfO_2 . This demonstrated that better SS^{-1} resulted from enhanced gate control by increasing the gate insulator capacitance. The DIBL in the devices with L_{ch} of 490 nm could be reduced from 340 mV/V to 8 mV/V as exhibited in Figure 6.23b. This comparison predicts that even lower EOT than that used here, perhaps by applying either higher-k material or smaller thickness, could help further scaling of the device channel length with better immunity to short channel effects.

Figure 6.23 Comparison of SS^{-1} (a) and DIBL (b) vs L_{ch} for devices with 5 nm and 7.5 nm HfO_2 .

In conclusion, we demonstrated successful integration of thin III-V layers to Si by NiSi formation and the fabrication of the first InGaAs FinFETs on insulator on Si in a fab-compatible process, ensuring excellent off-state characteristics from the insulating barrier between III-V and Si compared to the epitaxial-grown doped barriers. Using this new

platform, we investigated the scaling metrics of InGaAs FinFETs with high-k dielectric and metal gate and showed that devices with smaller P and longer L_{ch} generally provide lower SS^1 and $DIBL$ and display improved SCE. This demonstration highlights the potential of high performance InGaAs FinFETs on Si for ultimately scaled III-V logic technology, and paves the way for incorporating a variety of III-V electronic and optoelectronic devices on a Si CMOS platform.

Most of this section was published in Advanced Functional Material, 2014, X. Dai, B. M. Nguyen, Y. Hwang, C. Soci and S. A. Dayeh. The dissertation author was the first author of this paper.

Chapter 7 Conclusions

7.1 Summary of this work

This thesis focuses on a variety of synthesis/fabrication approaches and transport studies of quasi one-dimensional III-V systems, including single nanowires, nanowire junctions, core-shell nanostructures, and Fin structures in view of their potential forthcoming application in highly integrated electronic and light detecting devices. Optimizations of growth parameters, introduction of radial overgrowth, configuration of selective contacts and multi-gate contacts enable the engineering of their electronic properties from material morphology, crystalline structure, surface states, spatial separation of carriers, and electrostatic control of the 1D transport channel. Various types of nanowire devices have been demonstrated, including Y-junction rheostats where a crystalline triple junction may be employed with narrow contacts to study ballistic transport in systems with multiple leads, core-multishell nanowire photodetector with high sensitivity working at room temperature, and tri-gate transistors with reduced short channel effect. In few respects these devices showed superior performance and characteristics than their conventional planar counterparts. In addition, we have shown how heterogeneous integration of low-dimensional III-V structures on Si is feasible by using a new bonding scheme based on formation of a robust NiSi bonding interface, which highlights the potential of incorporating high performance III-V electronic and optoelectronic devices on a Si CMOS platform for ultimately scaled technology.

The major accomplishments of this work can be summarized as follows:

1. Studies on the optimization of bottom-up synthesis of binary III-V compound nanowires by MOCVD were presented (Chapter 3). The influence of the different growth parameters (growth temperature, V/III ratio, catalyst diameter, growth time, etc.) on the nucleation, elongation, morphology, crystal structure, crystallographic defects and heterogeneous growth of III-V semiconductor nanowires (GaAs, InAs, and InP) were investigated, serving as a basis for the studies of transport characteristics in nanowire system. The inherent issues with III-V 1D systems of defects, surface states, and heterogeneous integration have been optimized for electronic applications by tuning growth parameters, building core-shell structure, and growing III-V nanowire heteroepitaxially on Si or epitaxially on bonded III-V layers on Si. These studies pave the way for the studies of more complex nanostructure growth and their electronic applications.
2. The self-assembly of complex nanowire architecture is designed toward controlled 3D integration and future applications in quantum transport devices for fundamental studies of ballistic transport (Chapter 4). Synthesis of GaAs nanowire monolithic junction in a single step was engineered and achieved based on the energy balance between the electrostatic energy from the interaction of polar surfaces and the mechanical energy required to bend the nanowires to the point of contact. TEM was employed to understand the formation mechanisms and the crystallographic properties of these monolithic junctions. Preliminary transport characterization demonstrated the electrical conductivity across the three branches of the junction and electrostatic control of the conductance of individual transport channels in a branch

by external biasing of the others, which enables the applications in electron waveguide Y-junction switches, nonlinear ballistic junctions, etc.

3. Controlled growth of heterostructures in the GaAs/AlGaAs alloys and their application in nanowire photodetector devices with high responsivity at room temperature were demonstrated, where the core-shell configuration effectively decreased surface state density and created a two-dimensional electron tube at the heterointerface (Chapter 5). Built-in electric fields at the semiconductor heterointerface and metal/semiconductor Schottky contact interface promoted photogenerated charge separation and thus enhanced the photodetectivity. Measured photocurrent spectrum suggested that the nanowire supported resonant optical modes in the near-infrared region as predicted by the full wave optical simulation, while the amplitude of the experimental data agreed well with predication of transport modeling.
4. An innovative fab-compatible heterointegration of III-V materials to Si and the first III-V FinFET devices on Si were demonstrated, exploiting transport characteristics in 1D systems obtained through top-down approaches based on knowledge acquired in electronic studies of single-crystal nanowires and heterostructures synthesized by bottom-up growth (Chapter 6). The transfer of high-quality, large-scale InGaAs layers to Si substrate through wafer bonding relied on the formation of a robust NiSi interface. The 1D channel was then fabricated on the transferred layer and gated from three-sides to achieve better electrostatic control and passivation of surface damage. Excellent transistor performances were obtained from such structure, showing lowest SS^{-1} of 150 mV/dec, and smallest $DIBL$ of 8 mV/V. Scaling metrics of InGaAs

FinFETs indicated that devices with a smaller perimeter and a longer channel length generally provided lower SS^{-1} and $DIBL$ and exhibited improved short channel effect.

Overall, the research performed in this work lies at the interface between conventional microelectronic processing and fundamental mesoscopic physics of quasi-1D structures, which was unique in the sense that the entire process flows from material synthesis to device design, fabrication and characterization were explored, allowing the iterative optimization of the device performance by looking at intrinsic (opto)electronic properties of materials, impact of surface states, band alignment of heterostructures, and electrostatic control of the conducting channels. Though these 1D structures have different geometries, they have in common advantages, disadvantages and same basic underlying physics in carrier transport. Working devices were demonstrated with excellent performance and designed to be compatible with industrial fabrication processes. Furthermore, investigation of the interplay between bottom-up and top-down techniques indicated that it would be an accepted paradigm for next generation devices. Whenever bottom-up technologies become mature for mass manufacturing, it would offer more opportunities by incorporating functionalities in future devices, following the More-than-Moore trend.

7.2 Perspective works

This work has shown the enormous potential of these unique structures to realize high-performance electronic and optoelectronics devices based on III-V compounds. Due to the time constraints, not all the promising ideas could be realized, but some of them may be the subject of future work. Specifically, we believe that these research directions may be of particular interesting and shall be pursued in the future:

1. Selective-area growth of nanowire array using nanoimprint lithography could increase the output for the fabrication of vertical nanowire devices at the wafer scale, hence easing their integration with already existing mainstream technologies (e.g. CMOS). Besides, the selective-area growth of nanowire array using advanced lithography tools is a revolutionary cost-disruptive breakthrough for the fabrication of nanowire LEDs or nanowire-based photovoltaics. The implementation of III-V nanowire arrays with different diameters, lengths, spacing and arrangements for photovoltaic application aims at increasing the solar-energy-conversion efficiency, by maximizing the effective absorption of the photons at a variety of incident wavelengths and angles, and optimizing the efficiency of the carrier collection with optimal nanowire sizes and interdistances.
2. For optimization of nanowire photodetectors, Type II heterostructures with staggered band-edge alignment, e.g. GaAs/InAs and ZB GaAs/WZ GaAs, are expected to play better roles through more effective charge carrier separation. Electrons and holes could be dragged to opposite direction at the heterointerface, hence decreasing the probability of recombination of the electron-hole pair inside the device and increasing the photoconductive gain, which provides better performances towards the realization of highly sensitive photodetectors.
3. Monolithic nanowire junctions offer a platform for the study of mesoscopic physics. The yield of self-assembly growth of nanowire junctions should be improved by designing catalyst size and interdistance. Introducing quantum dots or heterostructures inside such system offers diversities and opportunities in the fundamental studies. However, studies in GaAs compound system is limited by the

high density of surface states, requiring the optimization by introducing growth of AlGaAs shell on the as-grown monolithic junctions. Moreover, it is of great interest to study the growth and carrier transport in low bandgap materials, such as InAs and InSb, which provide an enhancement of quantum effect.^{20, 118} On the other side, vertical monolithic nanowire junctions can be engineered for 3D nanoprobe to detect and record intercellular information by recording the intracellular potential detected by the central branch as a form of current variation between the other two branches.

4. In case of FinFET devices, the fine tuning of the doping concentration of both the source and drain is a key parameter in order to achieve a lower S/D contact parasitic resistance and a better on/off performance. Furthermore, a selective etching process can partially remove the insulating layer below the gate region in order to form a gate-all-around structure, which will further improve the channel control. It is also worth and mandatory to explore new key routes towards the improvement of the devices performance, such as the surface passivation of III-V surfaces, the carrier confinement, and the influence on the transport property of a larger bandgap layer such as InP regrown on the existed InGaAs Fins. Further understating of the device transport properties (i.e. effective carrier mobility, temperature dependence, parasitic capacitance and resistance) are needed for the improvement of the device performance.

List of Publications

Journal Publications

1. “Novel Heterogeneous Integration Technology of III-V Layers and InGaAs FinFETs to Silicon”, **X. Dai**, B.-M. Nguyen, Y. Hwang, C. Soci, and S. A. Dayeh. *Advanced Functional Materials*, 2014.
2. “GaAs/AlGaAs Nanowire Photodetector”, **X. Dai**, S. Zhang, G. Adamo, Z. Wang, H. Liu, Y-Z. Huang, C. Couteau, and C. Soci, *Nano Letters*, 2014.
3. “Tailoring the Vapor-Liquid-Solid Growth toward the Self-assembly of GaAs Nanowire Junctions”, **X. Dai**, S.A. Dayeh, V. Veeramuthu, A. Larrue, J. Wang, H. Su, C. Soci, *Nano Letters*, 2011, 11, 4947-4952.
4. “Nanoscale Heterogeneous Reactions and Interfaces in Ge/Si and for III-V on Si Integrated Devices”, S. A. Dayeh, W. Tang, B.-M. Nguyen, **X. Dai**, Y. Liu, Y. Hwang, X.-H. Liu, R. Chen., *ECS Transactions*, 2013, 58, 115-125.
5. “Rocking Chair Defect Generation in Nanowire Growth”, S. A. Dayeh, X. H. Liu, **X. Dai**, J. Y. Huang, S. T. Picraux, C. Soci, *Applied Physics Letters*, 2012, 101, 053121-3.
6. “Anisotropic Photonic Properties of III-V Nanowires in the Zinc-Blende and Wurtzite Phase”, C. Wilhelm, A. Larrue, **X. Dai**, D. Migas, C. Soci, *Nanoscale*, 2012, 4, 1446-1454.
7. “Lower Size Limit of Dislocation Plasticity in Silicon”, Y. He, L. Zhong, F. Fan, B.-M. Nguyen, **X. Dai**, C. Wang, T. Zhu, S. X. Mao. 2014, *In preparation*.

Book Chapter

“III-V semiconductor nanowires: arsenides, phosphides, and antimonides” **X. Dai**, A. Olivier, C. Wilhelm, S. A. Dayeh, C. Soci, in Semiconductor nanowires: Materials, synthesis, characterization and applications, J. Arbiol and Q. Xiong Ed., Woodhead Publishing. 2014, *Invited review paper, under editorial review.*

Conference Contributions

1. International Conference on Materials for Advanced Technologies (ICMAT) June 26 to July 1 2011, Singapore, “Y-junction GaAs nanowires by a novel VLS growth mechanism”, **X. Dai**, V. Veeramuthu, A. Larrue, S.A. Dayeh, H. Su, C. Soci. (Presentation)
2. Material Research Society (MRS) Fall Meeting & Exhibit, 2011, Boston, “Self-Assembled GaAs Nanowire Junctions”, **X. Dai**, S.A. Dayeh, N. Meng, A. Larrue, H. Su, C. Soci. (Poster)
3. Institute of Physics Singapore (IPS) Meeting, February 23-24, 2012, Singapore, “Self-Assembly and Electrical Properties of GaAs Nanowire Junctions”, **X. Dai**, S.A. Dayeh, N. Meng, A. Larrue, H. Su, C. Soci. (Presentation)
4. LANL Annual Student Symposium, August 7-8, 2012, Los Alamos, NM, USA, “A Novel Approach for High Performance InAs FINFETs on Silicon”, **X. Dai**, B.M. Nguyen, Y. Hwang, C. Soci and S. A. Dayeh. (Poster)
5. CINT 2012 Users Conference, September 19-20, 2012, Albuquerque, NM, USA, “A Novel Approach for High Performance InAs FINFETs on Silicon”, **X. Dai**, B.M. Nguyen, Y. Hwang, C. Soci and S. A. Dayeh. (Poster)

6. Material Research Society (MRS) Fall Meeting & Exhibit, 2012, Boston, “Elasto-electrostatic Coiling of Vertically Grown Semiconducting Nanowires”, K. Taheri, **X. Dai**, C. Soci, M. Upmanyu. (Presentation)
7. 40th Conference On The Physics & Chemistry of Surfaces & Interfaces (PCSI-40), January 20-24, 2013, Waikoloa, “A Novel Approach for High Performance InAs FINFETs on Silicon”, **X. Dai**, B.M. Nguyen, Y. Hwang, C. Soci and S. A. Dayeh. (Poster)
8. Institute of Physics Singapore (IPS) Meeting, March 4-6, 2013, Singapore, “A Novel Approach for High Performance InAs FINFETs on Silicon”, **X. Dai**, B.M. Nguyen, Y. Hwang, C. Soci and S. A. Dayeh. (Presentation)
9. 224th Electrochemical Society (ECS) Meeting, Oct. 27 to –Nov. 01, 2013, San Francisco, “Nanoscale Heterogeneous Reactions and Interfaces in Ge/Si and for III-V on Si Integrated Devices”, S. A. Dayeh, W. Tang, B.-M. Nguyen, **X. Dai**, Y. Liu, Y. Hwang, X.-H. Liu and R. Chen. (Invited talk)
10. 4th Asian Spectroscopy Conference (ACS), Dec 15-18, 2013, Asian Spectroscopy Conference, “Photocurrent Spectroscopy of a Core-Shell GaAs/AlGaAs Nanowire Heterostructure”, **X. Dai**, S. Zhang, Z. Wang, G. Adamo, H. Liu, Y. Huang, C. Couteau, and C. Soci. (Poster)

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