High frequency high efficiency high dynamic range (3H) DC-DC converter IC

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**High Frequency High Efficiency High Dynamic
Range (3H) DC-DC Converter IC**

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Abstract

As demanded by the increasing powerful performance of electronic devices ranging from computer systems, embedded systems, and portable devices, high performance microprocessors are required to handle large scale computing and complicated algorithm. Therefore, it is urgent to develop a voltage regulator with fast load transient response and large current delivery capability to power the next generation microprocessor. The scope of this thesis is to design a dc-dc converter which delivers large current and responses fast to the load transient without increasing the output capacitor for multifarious electronic devices.

Hysteretic control method is a promising candidate to cope with the fast load transient response and tight voltage tolerance requirement due to its bandwidth closing to switching frequency. However, it suffers from wide variation of switching frequency which may result in an increasing output voltage ripple. Moreover, the harmonic components of variable switching frequency may close to the frequency of power supply resonant tanks formed by parasitic package inductance interconnects and on-die decoupling capacitances, therefore extra output voltage noise is excited. To address this issue, a fixed frequency hysteretic buck converter is proposed and presented in this thesis. It adopts a Phase Locked Loop to synchronise the switching clock with a reference clock to realize fixed frequency

operation. The prototype achieves fixed 1MHz switching frequency and 2.5mV output ripple at 1A load current.

In order to enable the fixed frequency hysteretic buck converter adopted to multiphase configuration for large current delivery capability in terms of thermal management and efficiency. Whereas it is difficult to apply multiphase configuration to hysteretic control method owing to its lack of synchronization. A multiphase hysteretic buck converter is proposed and presented in this thesis to explore how to apply the hysteretic control method to multiphase configuration. The proposed topology enables a multiphase configuration by adopting a Delay locked loop to achieve automatic phase synchronization. The Delay locked loop is used to generate multiphase synchronization accurate signals from the output of a hysteretic comparator directly without external synchronization signals.

Chapter 1

Introduction

1.1 Background

In this era of science and technology, the microprocessors are found in verity of applications in everyday life ranging from computer systems, embedded systems, and portable devices. These electronic devices become indispensable parts of our lives, prevailing from home to office, have made out lives smoother and faster [1]. Nowadays, vigorous growth of electronic devices has rendered it indispensable parts of our lives and heavily relied by human beings. As a result, people are expecting more powerful and comprehensive functional electronic devices to facilitate our daily lives.

In order to cope with the increasing demand of powerful performance and rapidly emerging of multitask capability of electronic devices, high performance microprocessors, as the heart of the electronic devices, are required to handle large scale computing and complicated algorithm [2]. Thus, the microprocessor increases with faster clock speeds, and higher transistor count, resulting in higher current demands. The number of transistors in integrated circuits doubles every two years, predicted by Moore's law, now the number of transistors in a microprocessor is over 13 billion, as opposed to thousands of transistors on a 4004 CPU die [3]. Fig.

1-1 shows the microprocessor transistor counts against dates of introduction.

Figure 1 - 1 CPU transistor counts against dates of introduction [3]

The power consumption of a microprocessor is proportional to the clock frequency f , all the logic gates' lumped capacitor C , and the square of the core voltage V_{CC}

$$P \propto C \cdot V_{CC}^2 \cdot f \quad (1.1)$$

In order to achieve higher performance, the clock frequency should be higher. Meanwhile, the scaling of transistor increases the capacitor. For

a fixed die size, with MOS transistor channel length, oxide thickness, and supply voltage all decreasing by about 0.7x per generation, the total circuit capacitance increases by 1.43x [4]. Accordingly, the power consumption increases.

The latest generation microprocessors “Ivy Bridge” for notebook come with 17~75W thermal design power (TDP), with core voltage 0.3-1.5V and maximum current 50A according to IMVP-6 [5]. Today’s voltage regulator modulator (VRM) faces a stringent challenge, not only by the high current but also by the strict transient response requirement. The microprocessor performs a fast dynamic load with high di/dt current slew rate up to $300A/\mu s$ from the sleep mode to active mode, and vice versa. During the load transient, the VRM’s output voltage cannot exceed the voltage tolerant band, which is extremely difficult without increasing output capacitor.

Therefore, it is very important and challenging to design power converter for the next generation microprocessor.

1.2 Objective and Scope

The demand of high performance voltage regulator for the next generation microprocessors is growing dramatically in this decade due to the increasing popularity of computer systems, especially portable devices. Design a dc-dc converter which delivers large current and responses fast to

the load transient without increasing the output capacitor for multifarious electronic devices is the primary objective.

This project, supported by Panasonic Industry Device Semiconductor Asia, is targeted for designing a high switching frequency DC-DC control IC which could power the game or notebook pc CPU. More detailed specifications and requirements given by the company are listed as:

- To reduce external component and size by 5MHz high switching frequency
- Input voltage = 12V and could go to 20V
- Output voltage = 1.5V with 0.5% accuracy
- Maximum load current = 50A

For low duty cycles, switching losses tend to dominate, especially at high frequencies. In this case, the multiphase interleaved buck topology offers a solution to this issue. The output ripple current frequency is multiplied by the number of phases, hence the capacitance value of the output capacitors can be reduced, meanwhile the output current undertook by each phase is alleviative for better thermal management. The maximum number of phases is limited at 6 with consideration of inductor value tolerance [6]. Here, 5 phase is selected to lower each phase switching frequency to 1MHz.

To achieve this design goal, a fast control method will be selected from the control methods, and other advanced technologies will be combined to form high performance architecture. To this end, a hysteretic buck converter with 1MHz fixed switching frequency which can delivery 10A current was explored; then, the potential to apply hysteretic control method in multiphase configuration has been proven.

1.3Organizations

This thesis consists of five chapters.

Chapter 1 introduces the background and motivation for high performance VRM. Challenging issues of fast load transient and large current deliver are ready to be addressed as objective of this project.

Chapter 2 presents a literature review of fundamental switching mode dc-dc converter topologies and different control methods. In the first part, basic operation principle of DC-DC converter with different topologies is theoretically analyzed. Focus on the buck converter, different control schemes are explained and compared. Additionally, power loss and efficiency of buck converter is discussed in this chapter. Some key equations are also deduced. Furthermore, multiphase configuration is introduced to address the large current delivery issue.

Chapter 3 presents the proposed fixed frequency hysteretic buck converter. This chapter describes a novel approach that embedding the hysteretic buck converter in a PLL to lock the switching frequency with a reference clock to make sure the hysteretic controlled buck converter operating at fixed frequency. Stability of the overall system is elaborative analyzed. Circuits' design of key building blocks are also illustrated. Simulations are performed in Cadence to study the operation of the proposed system.

Chapter 4 demonstrates a multiphase hysteretic buck converter. In this chapter, a proposed topology that enables the multiphase configuration applied to hysteretic control approach by adopting a delay locked loop to achieve automatic phase synchronization is described. The basic circuit design and non-ideal effect analysis are also included. The feasibility of the proposed system is first verified in Simulink. Then, the performance of the proposed system is evaluated in Cadence.

Finally, the conclusions and the future work are presented in Chapter 5.

Chapter 2

Literature Review

2.1 DC-DC Converter

Dc-dc converters are defined as power electronics circuits which convert a dc voltage to a different dc voltage level to meet some form of energy conversion requirement of electronic systems. The simplest approach of transferring a dc voltage to a lower dc voltage is linear voltage regulator. A serious drawback for power application of this method is its low efficient. An efficient alternative method to the linear regulator is the switching mode converter, which can be classified into three fundamental topologies: buck, boost and buck-boost (also known as inverting or flyback).

2.1.1 Buck Converter Basic Operation

Buck converter is also named step down converter which generates step down voltages. As shown in Fig. 2-1, the basic elements of the buck converter include switch $S1$, DC input V_{in} , free-wheeling diode $D1$, inductor L , output capacitor C , and load R_L . The switch $S1$ is switched "on" and "off" in series with the input voltage V_{in} to produce a rectangular voltage at point V_X . For a fixed frequency duty-cycle control signal, $S1$ conducts for a time T_{on} , while $S1$ turns "off" for a time T_{off} . The duty-

cycle D , the ratio between the on-time T_{on} and the period of the control signal T_s which is equal to $T_{on} + T_{off}$.

Figure 2 - 1 Buck converter topology

Buck converter's equivalent circuit is shown in Fig. 2-2. It operates through the switch $S1$ turning on and off. When $S1$ is "on", the voltage at V_x is pulled to V_{in} , so diode $D1$ is turned off since it is reverse biased. Then a current builds up on the inductor and increases with slope $\frac{V_{in}-V_o}{L}$. When the switch $S1$ is "off", the diode $D1$ turns on to continue the inductor current and the voltage at V_x is driven rapidly toward ground. Then the voltage drop across on the inductor is equal to $-V_o$ and forces i_L to decrease. During the whole period T_s , the voltage and current waveforms of the inductor are shown in Fig. 2-3.

Figure 2 - 2 Buck converter equivalent circuits (a) S1 in on (b) S1 is off

Figure 2 - 3 Voltage and current waveforms of the inductor L

From the equivalent circuits, the rectangular voltage at point V_x is ranging between V_{in} and ground. The average value of this rectangular waveform is $V_{in}T_{on}/T_s$. The low pass LC filter in series between V_{in} and the output V_o extracts the DC component and results in a clean, near-ripple-free DC voltage at the output with a magnitude V_o of $V_{in}D$.

In practice, the converter cannot keep its output voltage perfectly constant with a finite capacitor. It is readily to derive the ripple in output voltage from the voltage-current relationship of the capacitor. The current in the capacitor is $i_C = i_L - i_R$, shown in Fig. 2-4a. When the current flows into the capacitor, the capacitor is charging. The area of the shadow triangle above the time axis is the change in charge ΔQ

$$\Delta Q = \frac{1}{2} \left(\frac{T_s}{2} \right) \left(\frac{\Delta i_L}{2} \right) = \frac{T_s \Delta i_L}{8} \quad (2.1)$$

Resulting in

$$\Delta V_o = \frac{T_s \Delta i_L}{8C} = \frac{T_s}{8C} \frac{(V_{in} - V_o)DT_s}{L} = \frac{(V_{in} - V_o)D}{8LCf_s} \quad (2.2)$$

In this equation (2.2), ΔV_o is the peak-to-peak ripple voltage at the output, as shown in Fig. 2-4b, where f_s is the switching frequency in hertz.

Figure 2 - 4 Buck converter waveform. (a) Capacitor current. (b) Output ripple voltage

2.1.2 Boost Converter Basic Operation

Boost converter is another popular switching mode converter with the capability of producing a dc output voltage greater in magnitude than the dc input voltage. So it is also named step up converter according to its function. The boost converter shows in Fig. 2-5 can produce a higher regulated output voltage from a lower unregulated input voltage with a slightly different topology from buck converter.

Figure 2 - 5 Boost converter topology

Fig. 2-6 shows boost converter's equivalent circuits when switch is on and off. When $S1$ is "on", the voltage at V_x is connected to ground, so diode $D1$ is turned off since it is reverse biased. Then a current builds up on the inductor and increases with slope $\frac{V_{in}}{L}$. When the switch $S1$ is "off", the inductor delivers its stored energy to capacitor via diode $D1$. Then the voltage drop across on the inductor equals to $V_{in} - V_o$ and forces i_L to decrease. During the whole period T_s , the voltage and current waveforms of the inductor are shown in Fig. 2-7.

Figure 2 - 6 Boost converter equivalent circuits (a) S1 in on (b) S1 is off

Figure 2 - 7 Voltage and current waveforms of the inductor

The net change in inductor current over a cycle during steady state is equal to zero

$$\frac{V_{in}}{L}DT_s + \frac{V_{in}-V_o}{L}(1-D)T_s = 0 \quad (2.3)$$

Solving for V_o

$$V_o = \frac{V_{in}}{1-D} \quad (2.4)$$

The peak-to-peak ripple voltage at the output can be computed from the capacitor current waveform, as shown in Fig. 2-8.

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{(\frac{V_o}{R})DT_s}{C} = \frac{V_o D}{RCf_s} \quad (2.5)$$

Figure 2 - 8 Current waveform of the capacitor

2.1.3 Buck-boost Converter Basic Operation

The buck-boost converter is another basic switching mode converter, as shown in Fig. 2-9. The output voltage of a buck-boost converter can be either higher or lower than the input voltage.

Figure 2 - 9 Buck-boost converter topology

The equivalent circuits when the switch $S1$ turns on and off are shown in Fig. 2-10. When $S1$ is "on", the voltage at V_x is pulled to V_{in} , so diode $D1$ is turned off since it is reverse biased. Then a current builds up on the inductor and increases with slope $\frac{V_{in}}{L}$. When the switch $S1$ is "off", the same inductor current continues to flow down through inductor, pulling the current through diode $D1$ from output. Then the voltage drop across on the inductor is equal to V_o and forces i_L to decrease. During the whole period T_s , the voltage and current waveforms of the inductor are shown in Fig. 2-11.

Figure 2 - 10 Buck-boost converter equivalent circuits (a) S1 in on (b) S1 is off

Figure 2 - 11 Voltage and current waveforms of the inductor

The net change in inductor current over a cycle during steady state is equal to zero

$$\frac{V_{in}}{L}DT_s + \frac{V_o}{L}(1-D)T_s = 0 \quad (2.6)$$

Solving for V_o

$$V_o = -\frac{DV_{in}}{1-D} \quad (2.7)$$

The peak-to-peak output voltage ripple can be computed from the capacitor current waveform, as shown in Fig. 2-12.

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{(\frac{V_o}{R})DT_s}{C} = \frac{V_o D}{RCf_s} \quad (2.8)$$

Figure 2 - 12 Current waveform of the capacitor

2.1.4 Discontinuous Conduction Mode (DCM)

In the analysis above, the converters operate in the continuous conduction mode (CCM) based on the assumption that the current in the

inductor is continuous. However, when the load resistance R_L increases further, the inductor's current average value (dc value) is less than half of the ripple of peak amplitude ($\Delta i_L/2$). In this case, the converters enter the discontinuous conduction mode (DCM). Take buck converter for example, its equivalent circuit during DCM is shown in Fig. 2-13. In the light load condition, the inductor current and the diode current are both zero at the end of the switching period, because the diode current cannot be negative. Fig. 2-14 shows the voltage and current waveforms of the inductor.

Figure 2 - 13 Buck converter equivalent circuit during DCM

The boundary between the continuous and discontinuous conduction modes can be found by inspection of the diode current. During the CCM, the diode current is positive over the entire interval $DT_s < t < T_s$ provided that $I_o > \Delta i_L/2$. This relationship can be expressed as

$$\frac{V_o}{R} > \frac{\Delta i_L}{2} = \frac{(V_{in} - V_o)D}{2Lf_s} \quad (2.9)$$

Hence, the inductor value must be larger than the critical value L_{cri} to ensure CCM operation

$$L > L_{cri} = \frac{(1-D)R}{2f_s} \quad (2.10)$$

Figure 2 - 14 Voltage and current waveforms of the inductor

2.2 Control Scheme of DC-DC Converter

Typically, keeping the output voltage permanent and equal to the dc reference voltage with the presence of time-varying sources and loads is the primary intention of a dc-dc converter. However, there are applications where the reference signal and load condition may also be time-varying. Thus, a feedback control loop is equipped in a dc-dc converter to obtain

constant output voltage. The control method can be classified as either variable-frequency or fixed-frequency. In principle, variable-frequency converters can have (1) fixed T_{on} and variable T_{off} , (2) fixed T_{off} and variable T_{on} , (3) variable T_{on} and variable T_{off} . Naturally, plus width modulation (PWM) controlled fixed-frequency converter must have both variable T_{on} and variable T_{off} . Fixed frequency PWM control is, by far, the switching converter control technique that is most widely used today [7].

2.2.1 Voltage Mode PWM control

Voltage mode PWM control is the most popular control method due to its simplicity and straight forward control pattern. Fig. 2-15 shows a simplified block diagram of a voltage mode PWM control feedback loop. The output voltage V_o is sensed by the feedback loop and subtracted from a reference voltage V_{REF} to generate an error voltage V_E . From Fig. 2-16, it is easy to find that the ramp waveform V_{RAMP} and the error amplifier V_E crosses at a point which determines the width of the PWM signal. Since V_{RAMP} increases from zero to V_P within a switching period, the duty cycle of the modulator will be V_E/V_P .

Figure 2 - 15 Voltage mode PWM buck converter's schematic

Figure 2 - 16 Voltage mode PWM control waveform

In order to keep the loop stability, compensation network is required and normally designed to be between $f_s/6$ and $f_s/10$. Due to the finite bandwidth of the compensation network the error voltage cannot follow the slope of step load current. Furthermore, the controller cannot immediately accommodate to the load current step, since it must wait for the succeeding clock pulse to turn on the switch again.

2.2.2 Current Mode PWM control

Another well-known technique today, senses the peak current in the power switch or inductor, and turns the switch off at a programmed level of current. This technique is called current mode control, shown in Fig. 2-17. In voltage mode PWM control algorithm, its control signal is achieved by comparing an artificially generated ramp waveform with the error voltage. In terms of peak current mode PWM control, the output inductor current waveform replaces this comparison ramp and thus forms an inner current feedback loop. Whereas an outer voltage loop still exists, it is used to command the output inductor current rather than the duty cycle directly. With the open loop characteristics of a programmable current source, current mode PWM control effectively eliminates the inductor within the inner loop, changing the resonant two-pole output filter to a single lower frequency dominant pole, plus a higher frequency pole at or beyond the gain-bandwidth of the system [8].

In effect, current mode PWM control does offer good line rejection, since the ramp is derived from the current ramp, which is a function of the voltage across the inductor during the ON time. Since the error amplifier's function is to program an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop. This control method renders both simpler compensation and a higher gain bandwidth over a comparable voltage mode PWM circuit. Although current mode PWM control benefits faster inner loop over voltage mode, it suffers sub-harmonic instability if the duty cycle exceeds 50%. It can be eliminated by introducing slope compensation to the error voltage. However, the load transient response of current mode PWM control still limited by compensation network and waiting time for next clock cycle.

Figure 2 - 17 Current mode PWM buck converter's schematic

2.2.3 Hysteretic control

Complicated feedback loop compensation circuit is required by the PWM control approaches stated above for the converter to achieve stable operation at all conditions. The dynamic characteristics of the PWM controlled converter are relatively slow since the unity-gain bandwidth has to be at least a few times lower than the switching frequency. Unlike other control methods, hysteretic control does not include a slow feedback loop. Thus, it can react on the load transient in the switching cycle where the transient occurs. The delays in the hysteretic comparator and the drive circuitry determine its transient response time. The high-frequency noise filter in the input of the comparator also adds some additional delay, which depends mostly on the level of the selected technology, and so the hysteretic control is theoretically the fastest solution [9]. The bandwidth of the loop response is close to the switching frequency itself. Because there is no clock and no error amplifier, nor any compensation circuitry, the quiescent current, is very low, this makes the hysteretic control very suitable for modern battery-powered application in particular.

Fig. 2-18 shows a buck converter with a hysteretic controller. The feedback network R_F and C_F works as a high-pass filter from V_o to V_{FB} , resulting in a fast transient response. The feedback voltage is obtained through the RC network as a sum of the output voltage and the voltage

across the capacitor C_F . Since the RC integrator estimated the inductor current, current sensing can be eliminated.

Figure 2 - 18 Hysteretic buck converter's schematic

The feedback voltage variation ΔV_{FB} is

$$\Delta V_{FB} = \left(\frac{V_{in} - V_o}{R_F} \right) \times DT_s \times \left(\frac{1}{C_F} \right) = \frac{D(1-D)V_{in}}{R_F C_F f_s} \quad (2.11)$$

where f_s is the switching frequency and D is the duty cycle. ΔV_{FB} is restricted in the hysteresis window V_h , resulting in the switching frequency

$$f_s = \frac{D(1-D)V_{in}}{R_F C_F V_h} = \frac{D(1-D)}{\tau_{RC}(V_h/V_{in})} \quad (2.12)$$

where τ_{RC} equals $R_F C_F$.

If the hysteretic comparator's propagation delay cannot be ignored, the actual switching frequency is

$$f_s = \left[\frac{\tau_{RC}(V_h/V_{in})}{D(1-D)} + \frac{\tau_{ON}}{(1-D)} + \frac{\tau_{OFF}}{D} \right]^{-1} \quad (2.13)$$

where τ_{ON} and τ_{OFF} represent the propagation delays of switching turn on and turn off respectively [10]. Fig. 2-19 shows the feedback voltage and the control signals with and without propagation delay.

Figure 2 - 19 Voltage waveform of feedback voltage (a) without propagation delay (b) with propagation delay

2.2.4 V^2 control

Similar to current mode control, V^2 control is essentially a kind of control technique utilizing peak output voltage as control variable, thus V^2 control can also be called as peak voltage control. Its control signal is generated by comparing output voltage waveform instead of peak inductor

current with the error voltage. Fig. 2-20 shows the V^2 controlled buck converter, where the inner loop adopts the output voltage as feedback control variable.

Figure 2 - 20 V^2 control buck converter's schematic

V^2 control has the advantage of reacting promptly to the load change since this information is fed back directly to the PWM modulator without any lead or lag compensator [11]. It suffers sub-harmonic oscillation if the duty cycle exceeds 50% like current mode control, thus slope compensation is necessary to ensure the stability [12]. Additionally, switching action delay to the transient voltage deviation limits the speed of V^2 control transient response due to its trailing-edge modulation [13].

2.2.5 Constant on-time control

Unlike conventional voltage-mode control and current-Mode control that employ an oscillator, an error amplifier and compensation circuit, constant on-time (COT) control, as shown in Fig. 2-21, scarcely used a comparator in the feedback loop. At the beginning of each cycle, it initiates an on-time period when the feedback voltage falls below the reference voltage. The high-side MOSFET stays on for a fixed duration. At the end of on-time, the high-side MOSFET turns off until the feedback voltage falls below the reference.

Figure 2 - 21 COT control buck converter's schematic

The most attractive benefit of COT control is that it features light-load efficiency. At light load, the switching loss is the dominant loss, and the light load efficiency can be remarkably improved with a smaller switching frequency. The ability to achieve high efficiency at light loads is due to the fact that the off-time will become necessarily long at light loads. Having extended the off-time, the switching frequency will drop [14]. [15] [16] has elaborated that its instability issue is due to the phase shift of the capacitive component of output ripple. A common practice to address this issue is to use bulk output capacitors with higher ESR which in turn increases the output ripple.

2.2.4 Summary

Preliminary simulations have been done in Matlab to compare the load transient response performance of three different control methods listed above with the same configuration: inductor $L = 650nH$, inductor parasitic resistance $r_L = 1m\Omega$, capacitor $C = 16.8\mu F$, capacitor parasitic resistance $r_C = 2m\Omega$, input voltage $V_{in} = 12V$, output voltage $V_{out} = 1.5V$, switching frequency $f_s = 1MHz$. The inductor value is selected to limit the current ripple to 20% of maximum load, where the capacitor value is chosen to constrain the output voltage ripple less than $\pm 0.5\%$.

(a)

(b)

(c)

Figure 2 - 22 Load transient response to 5A-10A-5A load current step

(X Axis: 0.1ms/div; Y Axis: 0.2V/div) (a) Voltage mode PWM (b)

Current mode PWM (c) Hysteretic Control

The simulation results, as shown in Fig. 2-22 and listed in Table. 2-1, indicates that the minimum voltage overshoot and shortest settling time both result from hysteretic control method. Comparing with normal voltage mode and current mode PWM control approaches, hysteretic control provides a more competitive performance for fast load transient response application.

Table 2 - 1 Summary of voltage glitch and settling time

	VMC	CMC	Hysteretic
Voltage Glitch (V)	0.27	0.17	0.11
Settling Time (μ s)	7	5	3

2.3 Power loss and efficiency of buck converter for CCM

The power loss in a buck converter can be summed up as conduction losses caused by the parasitic resistive impedances and switching losses due to the parasitic capacitive impedances. In terms of the circuit component, the majority of the power dissipation is from the power MOSFET and the inductor [17].

I. MOSFET Losses

Conduction loss from the MOSFET switches occurs when they are turned on and conducting current, which are described as:

$$\begin{aligned}
 P_{cond} &= R_{DS} \times I_{DS(RMS)}^2 \\
 &= DR_{DS(HS)} \left(I_o^2 + \frac{\Delta i_L^2}{12} \right) + (1 - D)R_{DS(LS)} \left(I_o^2 + \frac{\Delta i_L^2}{12} \right) \quad (2.14)
 \end{aligned}$$

where $I_{DS(RMS)}$ is rms drain-to-source current and $R_{DS(HS)}$, $R_{DS(LS)}$ are drain-to-source on resistance of high-side, low-side MOSFET respectively.

MOSFETs are not ideal switches, switching losses occur once the MOSFET are transitioning between on and off state, which in a high-side MOSFET are described as:

$$P_{switch} = \frac{V_{in} \times I_o}{2} \times f_s \times (t_r + t_f) \quad (2.15)$$

where t_r is rising time for turning on the MOSFET and the t_f is falling time for turning off the MOSFET. The switching loss in low-side MOSFET is negligible because the voltage across it equals to a diode drop instead of V_{in} [18].

Although conduction and switching loss account for a majority of power losses in the MOSFET, there are other minor lossy areas in the switching cycles. One of these areas of loss is the power lost due to charging the gate of the MOSFET, expressed as:

$$P_{gate} = Q_G \times V_{DD} \times f_s \quad (2.16)$$

where the Q_G is the total gate charge and the V_{DD} is the MOSFET driver's gate drive voltage.

During each switching cycle, the output capacitance C_{OSS} ($=C_{GD}+C_{DS}$) of both low-side and high-side MOSFET must be charged. These losses can be approximated by the equation:

$$P_{Coss} = \frac{(C_{OSS(HS)}+C_{OSS(LS)}) \times V_{in}^2 \times f_s}{2} \quad (2.17)$$

II. Inductor Losses

In a synchronous buck converter operating at high-load currents, the equivalent series resistance of the winding of an inductor r_L will have a significant impact on system efficiency. This impact can be described as:

$$P_{inductor} = r_L \times I_o^2 \quad (2.18)$$

The overall efficiency of the buck converter with considering all the primary loss explained above is expressed as:

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{P_o}{P_o + P_{cond} + P_{switch} + P_{gate} + P_{Coss} + P_{inductor}} \quad (2.19)$$

where P_o is the output power. With fixed power MOSFET and inductor, the efficiency mainly depends on the input voltage and load current. Heavy load leads to high conduction losses associated with the inductor and power MOSFET resistances. Additionally, high input voltage results in high switching losses and large power dissipation for charging the capacitance of MOSFET.

Chapter 3

Fixed Frequency Hysteretic Buck Converter

Non-linear behaviour of hysteretic control approach makes hysteretic buck converter suffer from wide variation of switching frequency. Switching frequency variation may cause voltage ripple exceeding the tolerant band of voltage regulation according to formula (2.2). In addition, the harmonic components of variable switching frequency may close to the frequency of power supply resonant tanks formed by parasitic package inductance interconnects and on-die decoupling capacitances, therefore extra output voltage noise is excited. Thus, a hysteretic buck converter operating at fixed frequency is highly desirable.

3.1 Proposed fixed frequency hysteretic buck converter

The proposed fixed frequency hysteretic buck converter is shown in Fig. 3-1. A high pass filter including R_C , C_C and a Phase locked loop (PLL) are added to the fundamental hysteretic buck converter analyzed in chapter 2. The high pass filter is adopted owing to the DC output voltage error resulting from Inductor parasitic resistance r_L . And the PLL is employed due to variable switching frequency of hysteretic buck converter. In the following paragraph, both issues will be analyzed in detail.

Figure 3 - 1 Fixed frequency hysteretic buck converter

In the fundamental hysteretic buck converter, inductor parasitic resistance r_L results in a large DC output voltage error with heavy load current. A high pass filter including R_C , C_C couples ac component of V_F onto the sensed output voltage kV_O . By adopting this ac-coupling capacitor, DC output voltage error $r_L I_o$ is removed from the average output $\overline{V_o}$, which can be expressed as

$$\overline{V_o} = \left(1 + \frac{R_A}{R_B}\right) V_{REF} = \frac{1}{k} V_{REF} \quad (3.1)$$

Recall equation (2.12) which determines switching frequency of hysteretic buck converter.

$$f_s = \frac{D(1-D)V_{in}}{R_F C_F V_h} = \frac{D(1-D)}{\tau_{RC}(V_h/V_{in})} \quad (2.10)$$

Since the switching frequency is reciprocal to feedback capacitor C_F , switching frequency can be adjusted by varying the value of capacitor C_F . By replacing the capacitor C_F with a varactor, the hysteretic buck converter's switching frequency can be tuned by the variation of capacitance of such a varactor.

In order to achieve fixed frequency operation, phase lock technique is adopted. A phase frequency detector (PFD) compares the phase of the external reference clock and the switching clock generated by the hysteretic comparator. The comparison yields a plus signal proportional to the phase error. This plus signal can be positive or negative according to the status that the output clock is leading or lagging the reference clock. The width of the positive or negative pluses is assured by the phase difference between the input clock and the reference clock. The following charge pump (CP) converts PFD output signals to charging or discharging current which is proportional to the pulse width. The loop filter (LF) is used to extract the average of the phase detector error pulses in order to produce the control voltage. Then the control voltage across on the LF adjusts the capacitance of varactor appropriately. Accordingly, the hysteretic buck converter's switching clock is adjusted until it is align with the reference clock. Consequently, the operation frequency of the hysteretic buck converter is fixed and equal to the external reference frequency.

3.2 System stability

In terms of frequency, the fixed frequency hysteretic buck converter can be viewed as a PLL with the voltage controlled oscillator (VCO) representing the hysteretic buck converter itself. Hence, a charge pump PLL (CPLL) model, as shown in Fig. 3-2, is used to derive parameters for the PLL. The phase of the reference signal is denoted θ_i and the phase of the VCO is denoted θ_o . In this model, the gain of PFD and CP are $1/2\pi$ and I_{CP} respectively. The transfer function of the LF and VCO are denoted by $F(s)$ and K_V/s respectively.

Figure 3 - 2 CPLL model in s-domain

Fig. 3-3 illustrates a typical loop filter with component labels assigned. The capacitor C_1 cooperating with the CP current source forms an integrator and the resistor R introduces a zero to stabilize the PLL. However, an instantaneous voltage jump of $I_{CP}R$ establishes on the control voltage when the pump current I_{CP} is driven into the filter upon each cycle of the PFD. So there will be frequency excursions follows the voltage steps.

In order to mitigate the ripple, a small capacitor C_2 is added in parallel with the R and C_1 network. Since this capacitor introduces a pole, appropriate choice of C_2 has to be accounted for not degradation the phase margin.

Figure 3 - 3 Loop Filter for CPLL

The transfer function of loop filter $F(s)$ can be expressed as

$$F(s) = \frac{s + \frac{1}{RC_1}}{C_2 s \left(s + \frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right)} \quad (3.2)$$

The open loop gain of the third-order CPLL is

$$LG(s) = \frac{K_V I_{CP}}{2\pi} \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right)} \quad (3.3)$$

The loop has a zero $\omega_z = \frac{1}{RC_1}$ and three poles with two poles at origin and third pole $\omega_{p3} = \frac{1}{R\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$, its corresponding Bode plot is shown in Fig. 3-4.

Figure 3 - 4 CPLL loop gain Bode plot

The phase margin degradation due to the third pole is obvious and is mathematically expressed by [19], where ω_c is the crossover frequency

$$PM = \arctan\left(\frac{\omega_c}{\omega_z}\right) - \arctan\left(\frac{\omega_c}{\omega_{p3}}\right) \quad (3.4)$$

The maximum phase margin can be obtained by equating the first derivative of PM to zero

$$\frac{d(PM)}{d\omega} = 0 \quad (3.5)$$

As a result, the maximum phase margin occurs when

$$\omega_c = \omega_z \sqrt{1 + \frac{C_1}{C_2}} \quad (3.6)$$

Substituting equation (3.6) into the phase margin expression (3.4), the maximum phase margin can be obtained

$$PM(max) = \arctan\left(\sqrt{1 + \frac{C_1}{C_2}}\right) - \arctan\left(\frac{1}{\sqrt{1 + \frac{C_1}{C_2}}}\right) \quad (3.7)$$

Maximum phase margin as a function of C_1/C_2 is shown in Fig. 3-5, thus the capacitor ratio C_1/C_2 can be chosen for an optimal design.

Figure 3 - 5 Maximum phase margin of third order CPLL

In order to ensure the stability of the system, a PLL should have a phase margin of at least 45° , and preferably 60° or more.

The locked state of PLL will be perturbed by the phase errors θ_e resulting from a step of phase $\Delta\theta$ or a step of frequency $\Delta\omega$. A step of phase occurs when the load condition changes and a step of frequency occurs when the input voltage or reference voltage steps to a new value.

The phase error transfer function $E(s)$ is given by as

$$E(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{1}{1 + LG(s)}$$

$$= \frac{s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2}{s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2 + \frac{K_V I_{CP}}{2\pi C_2} s + \frac{K_V I_{CP}}{2\pi R C_1 C_2}} \quad (3.8)$$

After applying the means of the final value theorem of Laplace transforms, these errors are readily evaluated as followed

$$\lim_{t \rightarrow \infty} y(t) = \lim_{s \rightarrow 0} sY(s) \quad (3.9)$$

It is readily to determine the steady-state value of a function in the time domain from inspection of its transform in the Laplace domain. Application of the final value theorem to the phase error equation (3.8) yields

$$\lim_{t \rightarrow \infty} \theta_e(t) = \lim_{s \rightarrow 0} \frac{\left(s^4 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^3 \right) \theta_i(s)}{s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2 + \frac{K_V I_{CP}}{2\pi C_2} s + \frac{K_V I_{CP}}{2\pi R C_1 C_2}} \quad (3.10)$$

I. A step of phase $\Delta\theta$

Take a step change $\Delta\theta$ of input phase to evaluate the steady-state error. The Laplace transform of the input is $\theta_i(s) = \Delta\theta/s$, which may be substituted into equation (3.10) to give

$$\lim_{t \rightarrow \infty} \theta_e(t) = \lim_{s \rightarrow 0} \frac{\left(s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2 \right) \Delta\theta}{s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2 + \frac{K_V I_{CP}}{2\pi C_2} s + \frac{K_V I_{CP}}{2\pi R C_1 C_2}} = 0 \quad (3.11)$$

In other words, the loop eventually will track out any change of input phase; there is no steady-state phase error resulting from a step change of input phase.

II. A step of frequency $\Delta\omega$

Take a step change $\Delta\omega$ of input frequency to evaluate the steady state error. The input phase is a ramp $\theta_i(t) = \Delta\omega t$, so $\theta_i(s) = \Delta\omega/s^2$. Substitution of this value of θ_i into equation (3.10) results in

$$\lim_{t \rightarrow \infty} \theta_e(t) = \lim_{s \rightarrow 0} \frac{\left(s^2 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s \right) \Delta\omega}{s^3 + \left(\frac{1}{R(\frac{C_1 C_2}{C_1 + C_2})} \right) s^2 + \frac{K_V I_{CP}}{2\pi C_2} s + \frac{K_V I_{CP}}{2\pi R C_1 C_2}} = 0 \quad (3.12)$$

So that the static phase error resulting from a step change of frequency is zero. This desirable feature is achieved with a passive filter, whereas a conventional PLL requires an active filter with infinite DC gain. Therefore, the charge pump permits zero static phase error without the need for DC amplification. That's why a charge pump PLL is chosen.

Fig. 3-6 and Fig 3-7 illustrate transient responses to a step of phase and a step of frequency separately. Both settling time are affected by the phase margin associated with the loop filter parameters. To maintain a short settling time, a minimum phase margin of 45° is required for all

condition. Thus, the worst case should be considered since a higher gain of the hysteretic buck converter can degrade the phase margin.

Figure 3 - 6 Transient response to a phase step

Figure 3 - 7 Transient response to a frequency step

Here, the gain of hysteretic buck converter can be derived with the same definition of VCO's gain

$$K_v = \frac{d(f_s)}{dt} \quad (3.13)$$

Substitute equation (2.10) into (3.13) results in

$$\frac{d(f_s)}{dt} = \frac{d(f_s)}{d(C_F)} \frac{d(C_F)}{dt} = - \frac{D(1-D)}{(V_h/V_{in})R_FC_F^2} \frac{d(C_F)}{dt} \quad (3.14)$$

Equation (3.14) indicates that K_v is affected by two independent factors D and C_F . Thus, the peak value of K_v is obtained by setting $D =$

50%. Owing to nonlinearity of $\frac{d(C_F)}{dt}$, simulation is used to acquire the approximate K_v . A succession of tuning voltages is applied to the varactor, and then the corresponding switching frequencies are recorded. These discrete data are imported to Matlab for curve fitting and 1st derivation, as shown in Fig. 3-8. So the maximum $K_v = 1.75\text{MHz/V}$ can be figured out from Fig. 3-8(b).

Therefore, the worst case is that the overall system has the smallest phase margin occurs when the gain of hysteretic buck converter achieves the peak value. In this case, the stability of overall system can be guaranteed if it is stable in worst case.

Figure 3 - 8 Switching frequency with different control voltage

(a) Fitting curve (X Axis: V/div; Y Axis: MHz/div)

(b) 1st derivation (X Axis: V/div; Y Axis: (MHz/V)/div)

3.3 Circuit Implementation

The key building blocks includes hysteretic comparator, phase frequency detector and charge pump.

3.3.1 Hysteretic Comparator

The schematic of hysteretic comparator is shown in Fig. 3-9. It consists of an internal positive feedback path through the gate-drain connections of transistors M5 and M6. The voltage width of the hysteretic window is given by

$$V_h = 2\sqrt{2} \left(\frac{\sqrt{k}-1}{\sqrt{k}+1} \right) V_{eff1,2} \quad (3.15)$$

where k is the ratio defined by

$$k = \frac{(W/L)_5}{(W/L)_3} = \frac{(W/L)_6}{(W/L)_4} \quad (3.16)$$

Thus, the hysteretic window can be adjusted by appropriately design of the ratio k .

Figure 3 - 9 Schematic of hysteresis comparator

The hysteresis comparator can achieve a 50mV hysteresis window with 0.6V~1.5V threshold voltage. As shown in Fig. 3-10, an ideal 1MHz triangle waveform with range from 0.575V to 0.625V in (a) and range from 1.475V to 1.525V in (b) is feed into the comparator, it generates square waveform to control the power MOSFET.

(a)

(b)

Figure 3-10 Output for the comparator with threshold voltage at
(a) 0.6V and (b) 1.5V (X Axis: $2.5\mu\text{s}/\text{div}$; Y Axis: $0.25\text{V}/\text{div}$ for both)

3.3.2 Phase Frequency Detector

The phase frequency detector (PFD) is one of the most critical components within a PLL. It compares the phase difference between the input clock and the reference clock and then passes the phase error information to the subsequent circuits. PFD can be implemented in Gilbert multiplier and XOR gate. An improved PFD is based on flip-flops, as shown in Fig. 3-11, which consists of two flip-flops and one NAND gate [20].

The flip-flop based PFD is also known as phase frequency detector, since it is capable to detect both phase and the frequency difference. Its acquisition range is from -2π to 2π .

Figure 3 - 11 Flip-flops based PFD

3.3.3 Charge Pump

The phase error sensed by the PFD is transferred to the CP in the form of voltage pulses. The CP transforms the voltage pulses to charging or discharging current, so as to alter the voltage across the loop. In principle, the CP consists of two switches, one current source, and one current sink, as shown in Fig. 3-12.

Figure 3 - 12 A simplified Charge Pump diagram

The UP and DN switch are respectively controlled by the positive(UP) and negative(DN) pulses generated by the PD. UP pulse conduct current source to charge LF and DN pulse conduct current sink to discharge the LF. The charge conveyed from the CP to LF is determined by the pulse's width and current magnitude. This process continues until the output clock aligns with the reference clock. In the locked state, equal charging and discharging will still occur, resulting in a smaller jitter performance [21]. In this case, the charging current I_{UP} and discharging current I_{DN} must be kept identical therefore the voltage across the capacitor will be kept constant.

In the actual implementation, the mismatch between I_{UP} and I_{DN} invokes the phase error. The amount of the undesired phase shift caused by CP mismatch can be approximated by the following expression [22]

$$\phi_{offset} = 2\pi \frac{\Delta t_{on}}{T_{REF}} \frac{\Delta i}{I_{CP}} \quad (3.17)$$

where Δt_{on} , Δi , and T_{REF} are the time duration of pulse width, the current mismatch of the charge pump and the reference clock period.

Figure 3 - 13 Schematic of the zero offset charge pump with symmetric loads

A zero-offset charge pump proposed in [21] is adopted to minimize the mismatch, as shown in Fig. 3-12. The charge pump consists of two NMOS source coupled pairs each with a separate current source and connected by a current mirror made from symmetric load elements. As mentioned before, the control signals UP and DN are asserted as two identical pulses once in every clock cycle when DLL operates in locked state. With both the UP and DN inputs asserted, the symmetric loads in left side and right side operate as a current mirror, therefore the right source

coupled pair sinks the same current as that flowing through the current mirror. Since the current flowing into the LF is identical to that flowing out of the LF, the control voltage V_{ctrl} is kept constant. The charge pump will have zero static phase offset since no net charge transfers into the capacitor.

Fig. 3-14 shows UP and DN current mismatch percentage, measured by $((I_{UP} - I_{DN})/I_{UP}) \times 100$, with variable filter voltage, the markers at $\pm 5\%$ mismatch indicate that the PLL could operate with filter voltage ranging from 0.4V to 1.6V.

Figure 3-14 UP and DN current mismatch (X Axis: V/div; Y Axis: 25%/div)

3.4 Cadence Simulation Results

The overall proposed system was simulated in Cadence environment with Gloablfoundries 65nm process.

3.4.1 Tuning Curve

The hysteretic buck converter will operate at different frequency with different duty cycle according to equation (2.12). Thus, the PLL has to lock at different control voltage to align the switching clock with the reference clock. Fig. 3-15 illustrates the tuning voltage will lock at different value with different output voltage.

(a)

(b)

Figure 3 - 15 Tuning voltage with (a) $V_o = 0.9V$ (b) $V_o = 1.2V$

3.4.2 Load Transient Response

Fig. 3-16 illustrates that the transient response of the converter by applying a load step of $500mA$ current with the power stage configured with $650nH$ inductor and $10\mu F$ capacitor. A maximum $200mV$ overshoot of output voltage is observed.

Figure 3-16 Transient response to load step 0.5A-1A-0.5A

Fig. 3-17 shows zoom in the output voltage transient response to 0.5A load step. The overshoot voltage is decreased by smaller inductance due to its higher slew rate of inductor current. Increasing the output capacitor decreases the voltage droop at the expense of response time. For fixed converter parameters, the transient behavior can be improved by increasing output capacitance or decreasing the inductance.

Figure 3-17 Output voltage transient response to 0.5A load step with various inductor and capacitor combination

3.5 Performance Summary

In Panasonic, the controller and the power MOSFET are designed and fabricated separately, then different dies are connected via wirebonds and packaged together, this chip configuration is called “Multi Chip Packages”. Since the power MOSFET module is confidential, the efficiency could merely be estimated by given specification of power MOSFET. By calculation, the designed buck converter achieve a efficiency of 94.3% efficiency, the percentage of total power losses occurring in each area of loss is shown in the pie chart in Fig. 3-18.

Figure 3-18 Power loss breakdown pie chart

This work demonstrate a fixed frequency hysteretic buck converter which achieve a 12V/1.5V conversion operating at fixed 1MHz with 94.3% efficiency at 1A load. This control method employed fully analogue PLL

technology, which makes it is adaptive to hysteretic controlled dc-dc converter analysis as it could be modeled as VCO. Table 3-1 shows a comparison between previously reported hysteretic buck converters.

Table 3-1 Performance comparison

	[23]	[24]	[25]	This Work
Switching Frequency (MHz)	0.85	0.78	1.0	1.0
Process (μm)	0.35	0.5	0.13	MCP
V_{IN} (V)	3.0	2.7	2.5	12
V_{OUT} (V)	1.5	1.5	0.7	1.5
L (μH)	4.7	3.9	1	0.68
C (μF)	10	47	10	10
I_{MAX} (A)	0.5	0.8	0.9	1
Efficiency (%)	94.5	85.6	93.0	94.3

Chapter 4

Multiphase Hysteretic Buck Converter

In order to manage the fast load transient response and tight voltage tolerance requirement, hysteretic control approach is a promising candidate as demonstrated in previous chapter. For the purpose of large current delivery, the fixed frequency hysteretic buck converter can be extended to multiphase configuration. However, it is difficult apply multiphase configuration to hysteretic control method due to lack of synchronization. The proposed topology enables a multiphase configuration by adopting a Delay locked loop (DLL) to achieve phase synchronization without injecting external synchronize clock.

4.1 Multiphase Technology

In order to deliver required current to load, multiphase dc-dc converter is more suitable than single phase approach considering power dissipation and efficient. With multiphase operation, each phase carries the same amount current, allowing balanced heat dissipation. A basic 2-phases buck converter topology and its current waveform are shown in Fig. 4-1.

Figure 4 - 1 (a) Basic 2-phase buck converter topology (b) current waveforms

Multiphase converters interleave the inductor currents in individual channels, thus the total output current ripple is greatly reduced. For an N -phase buck converter, the current ripple cancellation effect is defined as the ratio of the amplitudes of output current and inductor current ripple. The ratio is given by the following expression [26]

$$\alpha = \frac{\Delta I_o}{\Delta I_L} = \frac{N \left(D - \frac{m}{N} \right) \left(\frac{m+1}{N} - D \right)}{D(1-D)} \quad (4.1)$$

where ΔI_o is the output current ripple, ΔI_L is inductor current flowing in each phase, D is duty cycle, N is the number of phases and $m =$

$\text{floor}(N \cdot D)$ is the maximum integer that does not exceed $N \cdot D$. Fig. 4-2 illustrates the ripple reduction effect as a function of duty cycle.

Figure 4 - 2 Current ripple cancellation in multiphase buck converters

The interleaving approach can reduce the output current ripple by α according to its duty cycle. Meanwhile it increases the ripple frequency by N -times, which makes it possible to reduce the output capacitance and improve the transient response.

4.2 Proposed Multiphase Hysteretic Buck Converter

Fig. 4-3 shows the proposed multiphase hysteretic control for five-phase buck converter. The converter composes of five single-phase synchronous buck converters. The first phase buck converter with hysteretic control operates independently to set the reference clock Clk_0 for

the DLL, the duty cycle and frequency of the reference clock is designed according to the reference voltage V_{REF} , hysteretic window V_h , and feedback network components parameters. This main hysteretic control loop determines the duty cycle and switching frequency which followed by the remaining phases. After the DLL locked, the control signals for the remaining phases (Clk_{72} , Clk_{144} , Clk_{216} , Clk_{288}) are appropriately offset by 72° , 144° , 216° , and 288° . All five single-phase converters are synchronized with clocks generated by DLL instead of external injection of synchronization signals.

Figure 4 - 3 Block diagram of hysteretic controlled 5-phase interleaved
buck converter

4.3 Circuit Implementation

The key building blocks include hysteretic comparator and a delay locked loop.

4.3.1 Hysteretic Comparator

The design of hysteretic comparator follows the one in previous chapter.

4.3.2 Delay Locked Loop Design

The block diagram of the DLL is shown in Fig. 4-4. A phase frequency detector (PFD) compares the phase of the reference clock generated by the hysteretic comparator and the delay line output. The comparison yields a plus signal proportional to the phase error. This plus signal can be positive or negative according to the status that the output clock is leading or lagging the reference clock. The width of positive or negative pluses is proportional to the phase difference between the input signal and the output signal from delay line. The charge pump (CP) converts the pluses to proportional current which will be filtered by the capacitor. Then the control voltage across on the capacitor adjusts the delay line appropriately. The delay line adjusts the phase of the output clock proportional to the difference between it and reference clock until the output clock is align with the reference clock.

Figure 4 - 4 Block diagram of DLL

I. Phase Frequency Detector and Charge Pump

The design of phase frequency detector and charge pump follow the ones in previous chapter. The loop filter is simply represented by a capacitor.

II. Voltage Controlled Delay Line

A delay line consists of a chain of variable-delay cell, which is controlled by voltage. The delay is adjusted by changing the effective resistance R_{eff} or capacitance C_{eff} since the delay of each delay cell is proportional to its time constant formed by the R_{eff} and C_{eff} . After the DLL locked, the total delay of the VCDL equals to one clock period T_s . In theory, all the delay cells in the VCDL are assumed as identical. Therefore, each delay cell offers a time delay of T_s/N for a N stage VCDL. Consequently, a series clock signals with ideal phase shift are generated.

To achieve precise delay generation, high supply noise immunity is required. A differential delay cell with symmetric loads [27] designed for this target is shown in Fig. 4-5. The symmetric load elements employed in the delay cell enables the delay cell to achieve high dynamic supply rejection through a first order cancellation of noise coupling. A self-biased replica-feedback current source bias circuit for the differential delay cell, shown in Fig. 4-6, dynamically adjusts the NMOS current source bias in delay cell therefore this current is held constant and highly independent of supply voltage.

Figure 4 - 5 Differential delay cell with symmetric loads

Figure 4 - 6 Self-biased replica-feedback current source bias circuit for the differential delay cell

4.4 Inductor Mismatch Issue

Inductor mismatch may result in imbalanced current distribution among the converter phases and reduction the ripple cancellation effect in interleaved converters.

I. Inductance mismatch

Assume an inductance mismatch ΔL results in ripple cancellation reduction through a particular i_{th} phase when all the other phases have the same inductance equal to L , while that phase has mismatched inductance $L_i = L - \Delta L$. As shown in Fig. 4-7, a small inductance mismatch ΔL leads to an extra current ripple, since inductor current of i_{th}

phase $I_{Li-\Delta L}$ deviates from the supposed inductor current I_{Li} when i_{th} phase has matched inductance with other phases.

Figure 4 - 7 Derivation of ripple voltage owing to inductance mismatch

This inductance mismatch results in an extra current ripple $I_{Li-\Delta L}$ with a peak-to-peak value of

$$I_{Li-\Delta L} = \frac{\Delta I_L}{1-\Delta L/L} \quad (4.2)$$

After integration of the extra current ripple by the output capacitor, an extra voltage ripple $\Delta V_{\Delta L}$ exhibits on the output voltage with a peak-to-peak value of

$$\Delta V_{\Delta L} = \frac{\Delta Q}{C_{out}} = \frac{\frac{1}{2} \left(\frac{T_s}{2} \right) \left(\frac{I_{Li-\Delta L}}{2} \right)}{C_{out}} = \frac{\Delta I_L}{8f_s C_{out} (1-\Delta L/L)} \quad (4.3)$$

II. Inductor parasitic resistance mismatch

As it was argued in [28], if the multiphase converter mismatched power train resistances among the phases, the output current distributes itself among the phases so as to minimize the power dissipation in the power train. The current sharing model of an N -phase converter is employed to analyze imbalanced inductor current and conduction power loss. As shown in Fig. 4-8, resistors $R_1, R_2, \dots, R_N$ model the dc resistance of each phase of the power train resistance, and $V_1, V_2, \dots, V_N$ model the average open-circuit voltage for each phase. However, the actual current mismatch may have undesirable consequences such as possible saturation of the inductors and increased conduction power loss. One possible power train resistance mismatch is due to inductor parasitic resistance mismatch. Assume i_{th} phase have a mismatched inductor parasitic resistance $R_{Li} = R_L + \Delta R$, while other phases have the same inductor parasitic resistance R_L .

Figure 4 - 8 DC current sharing model of an N -phase converter

As the inductor parasitic resistor of the different phases form a current divider for the output current I_o , the current flows through phase i is

$$I_{Li} = \frac{R_L/(N-1)}{1+R_L/(N-1)} I_o \quad (4.4)$$

The other phases with matched inductor parasitic resistor carry equal current I_L

$$I_L = \frac{R_{Li}}{R_L} I_{Li} = \frac{R_{Li}}{R_L} \frac{R_L/(N-1)}{R_{Li}+R_L/(N-1)} \quad (4.5)$$

The total conduction power loss due to the inductor parasitic resistor is

$$P_{loss,inductor} = \sum_{k=1}^N (I_{Lk})^2 R_{Lk} = \frac{\frac{R_{Li}}{R_L}}{1+(N-1)\frac{R_{Li}}{R_L}} I_o^2 R_L \quad (4.6)$$

Ideally when all phases have the same inductor parasitic resistor and the conduction power loss can be described as $I_o^2 R_L/N$. The inductor parasitic resistor mismatch introduces increased conduction power loss by α .

$$\alpha = \frac{P_{loss,inductor}}{I_o^2 R_L/N} = \frac{N}{(N-1)+\frac{1}{R_{Li}/R_L}} = \frac{N}{(N-1)+\frac{1}{1+\Delta R/R_L}} \quad (4.7)$$

For a 5-phase buck converter, 50% inductor parasitic resistor mismatch will increase the conduction power loss by 7%.

4.5 Cadence Simulation Results

The proposed multiphase hysteretic buck converter is first demonstrated in Simulink and then implemented in Cadence.

The multiphase hysteretic buck converter is configured to operate at 1MHz with an output voltage of 1.5V. The power stage of each phase consists of an $650nH$ inductor with $1m\Omega$ parasitic resistance. A $400\mu F$ capacitor is employed as output capacitor to limit the output voltage ripple within tolerant band.

4.5.1 Steady State Operation

Fig. 4-9 shows the five phase inductor currents and ripple cancellation effect on the output current. The ripple current of each phase is 2A, while the ripple current after cancellation is 0.85A, the ripple cancellation ratio is 42.5%.

Figure 4 - 9 Five phase inductor currents and ripple cancellation

(X Axis: $0.5\mu\text{s}/\text{div}$; Y Axis: $0.5\text{A}/\text{div}$)

The interleaving approach not only reduces the output current ripple but also increase the ripple frequency by 5-times. Since each phase operates at 1MHz, the output current ripple frequency is 5MHz. So the output voltage ripple is limited within 0.05mV, as shown in Fig. 4-10.

Figure 4 - 10 Output voltage is steady state (X Axis: $2\mu\text{s}/\text{div}$; Y Axis:

$0.1\text{mV}/\text{div}$)

4.5.2 Transient Response to Line Step

Fig. 4-11 shows the transient response to a line step from 12V to 8V, the output voltage has undershoot of 2mV and overshoot of 3.6mV during the transient.

Figure 4 - 11 Transient response to line step 12V-8V-12V (X Axis: 0.5ms/div; Y Axis: 2mV/div)

Since the switching frequency is related with input voltage, the DLL locks again when line step happens, shown in Fig. 4-12.

Figure 4 - 12 Tuning voltage for DLL (X Axis: 0.5ms/div; Y Axis: 50mV/div)

4.5.3 Transient Response to Load Step

Fig. 4-13 shows the transient response to a 25A load step. Although hysteretic control method is theoretical the fastest control method, the proposed system limit its reaction speed. For the best response during the transient, multiphase dc-dc converter turns on all channels simultaneously at load current step or off at load current step down, thus allowing the fastest recovery and a minimum dynamic tolerance of the output voltage [9]. However, the proposed system still keep phase-shifted manner during load current step, thus it cannot fully benefit from the advantage of the hysteretic control.

Figure 4 - 13 Transient response to 25A load step (X Axis: 0.5ms/div; Y Axis: 0.05V/div)

Fig. 4-14 (a) shows the output voltage at load step from 25A to 50A, the undershoot voltage is approximately 35mV and the recovery time is $3\mu s$, corresponding to 3 cycles at 1MHz. Fig. 4-14 (b) shows the output voltage at load step from 50A to 25A, the undershoot voltage is approximately 90mV and the recovery time is $5\mu s$, corresponding to 5 cycles at 1MHz.

(a)

(b)

Figure 4 - 14 Output voltage at load step

(a) 25A-50A (X Axis: $2\mu\text{s}/\text{div}$; Y Axis: $50\text{mV}/\text{div}$)

(b) 50A-25A (X Axis: $2\mu\text{s}/\text{div}$; Y Axis: $100\text{mV}/\text{div}$)

4.6 Cadence Simulation Results

Then the proposed system circuit is implemented in Globalfoundries 65nm process.

4.6.1 Single Phase Hysteretic Buck Converter

A square waveform of control signal is generated after the feedback voltage compares with 50mV hysteretic window, as shown in Fig. 4-15.

The switching frequency is approximately 1MHz with the feedback network configured with $R_F = 1k\Omega$ and $C_F = 8nF$.

Figure 4 - 15 Feedback voltage and control signal (X Axis: 5μs/div; Y Axis: 0.25V/div)

4.6.2 Delay Locked Loop in Locking State

Fig. 4-16 shows the tuning voltage for DLL, indicates a 20μs locking time.

Figure 4 - 16 Tuning voltage for DLL

Fig 4-17 shows the clock signals for five phases, adjacent two clocks have 72 degree phase shift.

Figure 4 - 17 Multiphase clocks for five phases

4.6.3 Transient Response

The performance of transient response to line voltage step and load current step are illustrated in Fig. 4-18 and Fig. 4-19 respectively. During the line step, a maximum 10mV overshoot is observed. The simulated undershoot/overshoot is 130mV/150mV during the load current step of 16A.

Figure 4 - 18 Transient response to line step 1.8V-1.5V-1.8V (X Axis:
32 μ s/div; Y Axis: 0.25V/div)

Figure 4 - 19 Transient response to load step 16A-32A-16A (X Axis:
38 μ s/div; Y Axis: 0.215V/div)

4.7 Performance Summary

By applying multiphase topology, the dc-dc converter could deliver maximum 50A current, meanwhile the extra components could be reduced with 5MHz effective frequency. The dc-dc converter could deliver 75W at approximately 89.3% efficiency using the model estimation. A comparison between previous research and this work are shown in Table 4-1.

Table 4-1 Performance comparison

	29	30	31	This Work
Phases	4	4	8	5
Switching Frequency (MHz)	30	233	100	1
Process (μm)	0.5	0.09	0.09	MCP
V_{IN} (V)	4.8	1.2	2.4	12
V_{OUT} (V)	3.3	0.9	1.2	1.5
L (nH)/phase	220	6.8	0.8	680
C (μF)	0.008	0.0025	8.8	400
I_{MAX} (A)	1	0.3	20	50
Efficiency (%)	83	83.2	79	89.3

Chapter 5

Conclusion and Recommendation

5.1 Conclusions

In order to power the next generation microprocessor, voltage regulator with fast load transient response and large current delivery capability is highly demanded. To the end, non-linear hysteretic control method is attracting more and more attention as demonstrated the fastest control scheme in theory by pioneers.

However, hysteretic control approach suffers from wide variation of switching frequency which may result in an increasing output voltage ripple. It cannot be accepted that the output voltage exceeding the tolerant band of voltage regulation. In addition, the harmonic components of variable switching frequency may close to the frequency of power supply resonant tanks formed by parasitic package inductance interconnects and on-die decoupling capacitances, therefore extra output voltage noise is excited. Thus, a hysteretic buck converter operating at fixed frequency is highly desirable.

The proposed fixed frequency hysteretic buck converter utilizing phase locked loop to realize constant switching frequency operation is presented in Chapter 3. By replacing the feedback capacitor with a varactor,

the switching frequency of hysteretic buck converter can be controlled by the varactor's tuning voltage. By doing so, the hysteretic buck converter now can be viewed as a voltage controlled oscillator. The proposed system employs a phase locked loop to align the switching clock with a reference clock to achieve fixed frequency operation. The stability issue is exhaustive analyzed in this chapter. Furthermore, the stability issue when load transient or duty cycle change occurs is also been considered during the design procedure. The proposed system is demonstrated in Cadence simulation environment and tapouted using Globalfoundries 65nm process.

In order to cope with large current delivery capability, multiphase configuration is more reasonable solution than single phase approach with regarding to thermal management and efficiency. Whereas it is difficult to apply multiphase configuration to hysteretic control method owing to lack of synchronization. A feasible topology described in Chapter 3 provides a possible solution to adopt the multiphase configuration to the fixed frequency hysteretic buck converter.

The proposed multiphase hysteretic buck converter is illustrated in Chapter 3. The proposed topology enables a multiphase configuration by adopting a Delay locked loop to achieve automatic phase synchronization. The converter composes of five single-phase synchronous buck converters. The main phase hysteretic comparator determines the duty cycle and switching frequency of the control signal. A DLL is adopted to generate

multiphase synchronization accurate signals from the output of a hysteretic comparator directly without external synchronization signals. The proposed system is first demonstrated in Simulink. Then the detailed circuit is carried out in Cadence simulation environment.

5.2 Suggestions for Future Work

Since the proposed system fixed frequency hysteretic buck converter and multiphase hysteretic buck converter have been demonstrated, these two architectures can be merged to form a multiphase hysteretic buck converter working in fixed frequency topology in the future.

When implement it in circuit, non-ideal effect appears. Since the synchronization signals are generated by the DLL, the accuracy of DLL is critical for overall performance. From the simulation results, the synchronization signals suffer from duty cycle error of 0.175%, 0.225%, 0.15%, and 0.15%. Duty cycle error will result in imbalanced current distribution, decreasing efficiency dramatically. Consequently, a more accurate DLL is required to generate precise multiphase clocks.

The proposed multiphase hysteretic buck converter turns on each phase sequentially instead of the best approach to turn on/off all phases on the same time during the load transient. The control strategy based on the optimum approach can be added to improve the load transient response.

Furthermore, DLL locking time can be decreased to exhibit faster load transient response.

Since none of two components have the same parameters, mismatch in inductors of each phase will introduce extra output voltage ripple and imbalance current distribution. To solve this problem, current mode is superior to voltage mode. Current mode commands the output inductor current so that the mismatch parameters can be ignored. Therefore, a current mode fixed frequency hysteretic buck converter can be further explored to evaluate the performance when it is employed in multiphase configuration. Moreover, the capacitor in the loop filter can be reduced by adopting capacitor multiplication technique.

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