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IMPLANTABLE NEURAL RECORDING IC FOR MOTOR PROSTHESIS

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2014

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**IMPLANTABLE NEURAL RECORDING
INTERFACE IC
FOR MOTOR PROSTHESIS**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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IMPLANTABLE NEURAL RECORDING INTERFACE IC FOR MOTOR PROSTHESIS

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ABSTRACT

Paralysis has impacted the lives of millions of people, limiting not just their movement and quality of lives but also their mental health. Cortical neural prosthetics is a possible way to cure and if not help these paralyzed patients—by capturing patients' thought straight from their brain, then processing the information and translating them to electronic control signals to the assistive technologies such as computer interfaces, robotic arms and nerve stimulators. By using these implantable microelectromechanical system (MEMS) electrode arrays that are implanted into the brain, researchers are able to watch the simultaneous activities of many neurons, to understand and appreciate the brain functions. The immediate mission of this research is hence to record neural signals from the human brain, not just adequately but appropriately.

In the design of neural recording interface, the neural amplifier must have an input-referred noise that is low enough to detect the weak neural signals, and the power dissipation needs to be ultra-low to avoid tissue damage. Thus, the trade-off between noise and power becomes very important. A noise efficiency factor (NEF) is used to evaluate this trade-off and a lower NEF means better noise-power trade-off. Based on the proposed noise reduction technique, the low noise front-end amplifier developed in this design is able to achieve less than $4\ \mu\text{V}_{\text{rms}}$ noise with about $1\ \mu\text{W}$ power consumption over a 5-kHz signal bandwidth. The NEF of the front-end amplifiers developed ranges from 2.2 to 3.6, which are among the lowest reported to-date. Balanced MOS-bipolar active pseudo-resistor structure has been adopted in the neural recording amplifiers to realize the ultra-low high-pass cutoff frequency and good signal linearity.

For chronic neural recording, the impedance of the implanted electrode interface with the tissue will increase with time, which must be considered during neural recording amplifier design because the amplifier interfaces directly with the electrode. To further enhance the recording quality of the neural amplifier, another impedance-boosting neural amplifier is developed to boost the input impedance of the amplifier by ten times, which greatly removes the interference arise from the electrode mismatch. The signal to noise ratio does not degrade much even with long term neural recording, and the reliability of the neural recording system is demonstrated to be better than the classic design represented by Harrison's work.

Multi-channel recording is essential because a good amount of useful information can be simultaneously recorded from a large population of neuronal cells and their networks to enable more robust and sophisticated control of prosthetic devices. A 100-channel neural recording interface integrated circuit (IC) is fabricated and verified through hardware measurements.

To further reduce the overall power consumption of the neural implant, a neural recording interface IC intended for simultaneous neural recording with action potential (AP) detection for data compression in wireless multichannel neural implants is presented. The proposed neural recording interface IC detects the neural spikes and sends only the preserved AP information for wireless transmission in order to reduce the overall power consumption. Wireless transmission of the recorded neural signal waveform is enabled only during the presence of neural spikes, and hence, the data rate can be effectively reduced by more than ten times when compared to the conventional wireless neural

recording system. Furthermore, the complete neural AP information can be securely preserved with adaptive AP recording windows.

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Chapter 1. INTRODUCTION

1.1 Background

Millions of people are affected by paralysis in the world, which greatly impact their lives. The common causes of paralysis, as shown in Figure 1-1, consists of stroke, spinal cord injuries, multiple sclerosis and so on [1]. In the above conditions, people who have lost their ability to make free will movement may still have the intention to move around. This condition may happen to patients who are more severely injured; for example, in the lock-in condition, where one loses control of all or nearly all muscles, or perhaps are unable to speak or make eye movements, but remains conscious and has active cortical processing. According to a medical survey [2], around 1.9 percent of people in the U.S. population (or a total of 5,596,000 people) had reported some form of paralysis according to the functional definition in the survey. Approximately 0.4 percent of the U.S. population reported being paralyzed due to a spinal cord injury. So far, there is yet to be a cure for the disease and paralysis cannot be solved through nerve repair (not yet). Though the damaged nerves can regrow, it is at an extremely slow rate and the damage is usually too severe to heal.

Cortical neural prosthetics is a possible way to improve the condition of the paralyzed patients. This approach is through direct brain recording of patient's intention and decoding the captured signals in order to control external devices such as robotic arms, computer interfaces, and nerve stimulators [1]. Using implantable microelectromechanical system (MEMS) electrode arrays, neuroscientists and clinicians were able to observe simultaneous activities of

many neurons in the brain. This has allowed neuroscientists and clinicians to understand the way that the brain processes information. Recent researches have shown that neuroprosthetic devices can be developed for paralyzed human if activities of multiple neurons can be observed [3]. Neuronal activity generated by intention is translated into an electrical signal which can be used to perform useful tasks [4]. This could be the possible cure for millions of paralysed people who are incapable of any movement. Thus, the first crucial step to achieving the dream biomedical control is to record neural signals from human brain, both effectively and accurately.

Figure 1-1. Causes of paralysis [2].

The human brain is an amazingly complicated composition, containing approximately 100 billion neurons [5], and every neuron speaks to approximately 1000 other neurons. Monitoring the activity of a single neuron has been achieved since early 1920s, which significantly expedited the research in the perception of how the brain works. Various methods have been carried out which let

researchers to figure out the behaviors of neurons, mainly on how they communicate with each other, how they process information and convey messages.

The development of micromachined microelectrode arrays in the 1980s and 1990s had aided researchers to capture the concurrent activities of many neurons in localized regions of the brain. The ability to capture the simultaneous electrical activities of multiple neurons in the brain helped enabled a broad range of scientific and clinical endeavours [3].

Some motor based prostheses have undergone successful trials. During the experiments, recordings from brain cells on monkeys and humans were translated to a signal that is able to move a robotic limb or move a cursor on the screen [6][7]. These proved that neural prosthesis based on intracortical neural recording could provide a valuable new neuro technology to restore independence for humans with paralysis. This finding has raised great expectation among the paralyzed patients for a neural prosthetic device.

1.2 Motivation and Challenges

As described in the background, recent experiments show that neural prosthesis could be a possible cure for humans with paralysis. In spite of their good demonstrated results, none of those laboratory experiments are ready for clinical use yet. Because their current setup consists of bulky laboratory instruments with multiple complex connections between patients and equipment through cables for the power and data transmission, which is not convenient and results in the

patient's safety issues. Furthermore, the cable connection through human skin will result in a risk of tissue damage and infection. Moreover, since the complicated laboratory instruments are not specifically designed for recording and decoding neural signals, human interaction might be necessary to monitor, debug and calibrate those instruments. This leads to critical challenge relating to the electrode-tissue interface where scars develop around the damaged tissue (owing to the insertion of the electrode) as the human body rejects the foreign objects. This causes tissue encapsulating around the electrode which isolates the electrode from the neurons. Therefore, the stability and quality of the neural recording will undoubtedly degrade over time, until the device fails in chronic implants.

The biggest barrier in the development of neural prosthesis system has been the lack of suitable instrumentation. To effectively perform durable simultaneous recordings from large volume of neurons, the best system should be a fully implantable neural recording chip that is able to amplify, digitize and transmit the neural signals wirelessly to the external devices for data processing.

The ultimate aim that is very much preferred by the neuroscientists and clinicians is to precisely learn the brain state dynamics, and to capture the complete neural signals in lossless format, and without missing any information. This requires a multi-channel neural recording interface chip that is capable of carrying out high-density simultaneous recording of neural signals over a multi-electrode array attached to the brain. The miniaturization of these high-density multi-channel neural recording systems creates several major circuit design challenges. Meanwhile, operating at a low power and low voltage helps to relax the

requirement for the power link and prevent tissue injury caused by overheating.

1.3 Research Objectives and Contributions

To expedite the development of the neuroprosthetic devices, a micro system will be designed and fabricated for the neural recording application.

1.3.1 Research Objectives

In this project, a mixed-signal integrated circuit (IC) will be developed, and attached to the back of the neural multi-electrode array through flip-chip bonding technology. The neural signals acquired by the electrode will be amplified, digitized and transmitted out of human body through a radio frequency (RF) link. An inductive power link is constructed to transfer to a micro-coil placed at the back of the IC. The whole implant must be coated to prevent it from reacting with human internal body fluids.

In this thesis, a detailed study on neural recording, the related circuit techniques, architecture design, and optimization approaches will be presented. Key circuit blocks for the neural electrode interface IC necessary for the development of ultra-low-power neural recording amplifiers and the accompanied multiplexing architectures for interfacing with a large-scale neural electrode array will all be described. The developed analog-mixed signal circuits will be integrated in the complete implantable wireless neural recording microsystem and validated through thorough electrical testing. The animal trials conducted will also be discussed.

The objective of this project is to develop analog front-end circuits for the neural recording interface to improve on its performance. The primary goals of this

project include the followings:

- To develop low power system architecture for the analog front-end circuits of the neural recording interface IC. The whole system should consume be less than 5 μ W per recording channel to avoid tissue damage.
- To design each individual circuit block for the low power, low noise analog front-end in order to achieve the functions of amplification and filtering. The performance of each module must be able to meet the design requirements and according to different applications, which may include the front-end amplifier, the programmable gain amplifier (PGA), filters, and the reference generator.
- The overall system is to occupy as small an area as possible. Full integration of the overall system is also necessary and any external components should be avoided to minimize the size of the implantable device.

1.3.2 Research Contributions

The low noise low power neural amplifier with best power noise trade-off has been developed and the amplifier reaches a noise efficiency factor (NEF) of 2.2. This has been the lowest value reported so far.

The high input impedance amplifier has been developed to suppress the common mode noise raised from the electrode impedance mismatch and signal attenuation because the electrode capacitance and the input capacitance of the neural

amplifier form a voltage divider. The input impedance of the neural amplifier is boosted by ten times through the impedance boosting loop, allowing the common mode interference to be suppressed down to ten percent.

Activity based neural recording channel has been designed for the purpose of low data transmission rate without sacrificing the loss in the signal information of neural spikes. Wireless transmission of the recorded neural signal waveform is enabled only during the presence of neural spikes. This allows the data rate to be effectively reduced by more than ten times when compared to the conventional wireless neural recording system. Furthermore, the complete neural action potential (AP) information is securely preserved with adaptive AP recording windows.

1.4 Organization of Thesis

The rest of this thesis is organized as follows.

Chapter 2: This chapter provides a literature review of previous works on neural recording interface ICs. The general design considerations for the neural recording interface IC are included and the related neural recording interface designs will also be presented.

Chapter 3: This chapter presents the analog front-end neural recording amplifier design focusing on the low noise low power trade-offs, including the development of the low-power low-noise system architecture. Detailed circuit description of the amplification block will also be included. Various approaches were applied to achieve an optimum power-to-noise trade-off. Hence, a

discussion on other improvements for the front-end amplifier has also been added to this chapter.

Chapter 4: This chapter presents the analog front-end neural recording amplifier design focusing on the high input impedance. There are some non-ideal effects induced during the electrode fabrication process due to process limitation. One of the most important non-ideal effects is the electrode impedance mismatch, where the variation can be up to 50 percent. To decrease the influence caused by such non-ideality, a neural amplifier with ultra-high input impedance (ten times larger input impedance) that helps to reduce noise due to electrode impedance mismatch down to 10 percent of the neural amplifier without input impedance boosting is successfully designed and will be described in this chapter.

Chapter 5: This chapter presents the analog front-end neural recording channel design intended for power saving on data transmission. Only the neural signals with neural activities are selected for transmission. Therefore, by turning off the data transmission during non-activity periods, the data rate can be effectively reduced by more than ten times as compared to the conventional wireless neural recording system.

Chapter 6: This chapter summarizes the research completed in this Philosophy of Doctorate research and draws the conclusions. Future works for the design of the low noise low power neural recording interface IC are also given and discussed in the chapter. This includes the impedance boosting circuit and the integration methodology for the complete system.

Chapter 2. LITERATURE REVIEW

2.1 Design Considerations

Neural signals are produced by the electrochemical activities of a certain class of cells in the brain, which are known as neurons. The neuron cell is a nerve cell that generates electrochemical signals to process and deliver information in human body.

When sending messages, the neurons generate some electrically-charged chemicals in the body that are known as ions. The nerve cells are on the other hand enclosed by a semi-permeable membrane; only some ions can go through the membrane while other ions cannot go through it.

During the process where the ions are moving in and out across the neuron membrane, action potentials (AP), also called "spike" by neuroscientists, are generated. Thereafter, the sodium channels open due to a stimulus. Compared to the inside of the neuron cell, its outside usually has much more sodium ions; this triggers the sodium ions flow into the inside of the neurons. A positive potential is generated because sodium ions are positively charged. This process is called depolarization. Upon attaining a voltage of about +30 mV, the potassium channels release and potassium then flows out of the neuron cells, which then reverse the depolarization process. At the same time, the sodium channels begins to close, causing the AP to revert by -70 mV. AP can go beyond -70 mV [5] since the potassium channels remains open for perhaps a little too long, as shown in Figure 2-1. Slowly, due to the recovery of the ion concentrations, the potential will return to the resting levels and the cell reaches -70 mV. The magnitude of

the AP waveform is nearly always the same for any type of neuron [8]. A group of neurons form a near dc background voltage, which is named local field potential (LFP).

Figure 2-1. A typical action potential signal [8]

In order to measure and record the potentials and currents in the excitable cells, the recording electrodes provide the interface between the human body and electronic measurement devices, and convert the neural information into measurable and quantifiable electrical signals.

Table 2-1. Neural signal characteristics reported

Neural Signal Parameter	Harrison 2003 [9]	Najafi 2009 [10]	Harrison 2007 [11]	Sun-Il Chang 2009 [12]
Neural AP amplitude (μ V)	Up to 500	20 to 500	>50 to 500	-
Neural AP bandwidth (Hz)	100 to 7k	0.1 to 10k	300 to 5k	-
LFP amplitude (mV)	Up to 5	-	-	-
LFP bandwidth (Hz)	From below 1	-	1 to 100	0.5 to 300
dc offset (V)	1 to 2	0.4	-	1 to 2

Depending on the electrode characteristics and instruments used to record the neural information, the recorded signal may vary due to the difference in electrode-tissue interface and the electronic devices. Some commonly used neural signal characteristics are tabulated in Table 2-1.

The voltage in the extracellular body fluid is picked up by an electrode which is connected to the input of the neural amplifier. Each neural amplifier in a multi-channel recording IC is connected to its own signal electrode. Typically, the neural amplifier has a time constant much longer than the switching time of the multiplexer; this is necessary to capture the rapid signals across an array of electrodes. Furthermore, the neural signals are too weak can be easily destroyed by the multiplexer switching activities. Figure 2-2 depicts the wire connection of the signal electrodes to the neural recording interface IC and also connections to the other two key electrodes, i.e. the reference electrode and the ground electrode [13].

Figure 2-2. Types of electrodes

The signal electrode dimension is comparable to the neuron cells size which produce the neural signal, which is about 10–50 μm . The surface contact area of the electrode affects the amplitude of the neural signal acquired. A smaller electrode area results in a higher amplitude of the neural signal captured, but at the same time the noise of the electrode also increases. Moreover, there are some other concerns that must also be taken into consideration, for example, large electrodes create tissue damage and small electrodes may cause signal attenuation. Here, only the general background knowledge on electrode design is discussed in order to arrive at a more suitable electrode neural amplifier interface.

The reference electrode is located near the signal electrodes in order to receive the most identical background noise as the signal electrodes. The neural amplifiers capture the difference of the signal voltage and the reference voltage as its input signal to suppress the background noise. The reference electrode can be a signal electrode, a multitude of signal electrodes, signal electrodes with a larger electrode area or a stripped wire fixed close to signal electrodes [14].

The ground electrode provides a ground path for the implanted devices, which collects all the bias currents and leakage current. It is generally very large and can be comparable to the surface of the implant device that contains the implanted devices, to diversify the current density with the aim to minimize tissue damage when the devices fail.

Sometimes the reference electrode and the ground electrode can be combined when the ground electrode is quite near to the signal electrodes. The ground electrode can pick up background noise just like the signal electrodes. The different inputs of the amplifier can exclude the common background noise from

the signal, hence, improving the signal-to-noise ratio (SNR). However, the ground electrode senses different background noises if it is placed far away from signal electrodes. In this case, the ground electrode is not suitable for used as a reference electrode.

The electrode interface is a very important factor, which affects the amplifier attributes. The simplest model of the electrode is a simple capacitor. There is no resistive element in this model because for most electrodes, the resistance contributes no more than 10 percent to the electrode impedance. The large variation of the capacitance values of the electrode impedance should be carefully considered during the design of the neural recording interface circuit.

Due to process variations, the reported electrode capacitance varies from 2:1 to 10:1 even under strict process control. The capacitance value can be five times larger for rougher metal surfaces as compared to that for smooth surfaces [14]. Moreover, the electrode capacitance value is dependent on the signal frequency. For example, the capacitance of a $1000\text{ }\mu\text{m}^2$ diameter electrode might be 200 pF. The magnitude of this electrode impedance is $0.8\text{ M}\Omega$ at 1 kHz.

2.2 General System Design Requirements

The neural recording system interfacing IC comes just after the neural multi-electrode array and is in charge of amplification, filtering, digitization and transmission of the acquired neural signals. To study the brain state dynamics more accurately, higher resolution of neural recording data is required; which means the number of recording channel must be larger enough to simultaneously

capture the neural signals. Due to the medical application, both neuroscience research requirements and clinical application requirements must be considered during circuit design process. For neuroscience research, a number of general guidelines must be observed, such as potentially improve SNR and reduction on power consumption. As for the clinical application, considerations to be noted are: reduced risk of infection and risk of tissue damage, improved user comfort level, enhanced mobility, and be more cosmetically acceptable. These are the general design requirements for the neural recording system.

The detailed requirements for the design of the neural recording systems are listed below:

- First of all, the main challenge is associated with the nature of neural signals. The amplitudes of neural signals vary from around 50 μV to about 2 mV and the frequencies span from less than 1 Hz to a few kHz. To capture such weak signals, the input-referred noise of the neural amplifier becomes the most critical parameter, particularly for the low frequency range, where minimizing the flicker noise becomes an imperative task. Due to signal weakness, the signal has to be amplified but only in the frequency band of interest to curtail interferences from other frequency bands.
- A good analog front-end design is required to handle the high dynamic range of the differing neural signals, since the AP and LFP can vary within a large range, from 1 mV to 2 mV. Therefore, fully programmable bandwidth and gain may be necessary.
- Besides, the neural signals captured from the electrodes are usually

accompanied by a high dc component, from the electrode-tissue interface [15][16][17][18]. Hence, a high-pass filter will be necessary, whose cutoff frequency is to be programmed to less than 1 Hz to ensure that the low frequency components of the neural signals remain undistorted.

- Small size and light weight are the constant requirements for portable or implantable devices. Compact size calls for a fully integrated system.
- To further minimize the volume of the device, battery-less operation is desirable, especially for the implantable devices, where the energy may be collected from human body or the environment. Wire through the skin would cause tissue damage, even infection. Thus, wireless power link is desirable for implantable devices. On top of that, low voltage operation is also an essential requirement, where the whole system needs to function properly at 1 V supply or even lower.
- Heat generated from the implantable device may damage tissues if the power density is larger than 80 mW/cm^2 [3]. Thus, to prevent the contact tissue from overheating, ultra-low power consumption is an ultra-important benchmark for the neural recording interface circuit.
- High input impedance of the neural recording amplifier is required to prevent the common mode rejection ratio (CMRR) reduction because of electrode impedance mismatch.
- It is especially crucial for multi-channel applications, where slightly higher power consumption for an individual channel design will result in much more heat dissipation if hundreds of channels are implemented. This calls for

carefully planned system architecture to balance the trade-off between the system performance and power consumption.

Since the neural signal amplitude and frequency are arbitrary, the signal and bandwidth cannot be well defined. Thus, noise figure is not suitable to be used to measure the noise performance of the analog front-end. The noise performance of the neural amplifiers is measured by the noise efficiency factor (NEF) as the figure-of-merit (FOM) [9], which is commonly accepted. Different topologies and techniques have been employed in order to achieve successively lower NEFs.

$$NEF = V_{rms,in} \sqrt{\frac{2I_{total}}{4kT \cdot \pi \cdot U_T \cdot BW}} \quad (2-1)$$

where $V_{rms,in}$ is the input-referred noise of the system. U_T is the thermal voltage. I_{total} refers to the total current consumption for the system and BW states the bandwidth of the system. An ideal single bipolar transistor (consider only thermal noise) has an NEF of 1. The NEF of all other systems will be larger than 1. So this parameter is also considered as a figure of merit (FOM) in the rest of the thesis.

2.3 Neural Recording Interface IC Design

2.3.1 Neural Recording System Structure

In recent years, the implementation of the neural recording system and design of each individual functional block have been intensively studied. Neural recording has been conventionally carried out employing high-accuracy laboratory

instrumentation equipment. Compared to the integrated neural recording microsystem, these instruments are usually large, fixed to the shelf, expensive, very limited number of recording channels, and sensitive to power line interference. As an alternative to laboratory instruments, the integrated neural recording microsystems overcomes all the above discussed drawbacks by fabricating the functional blocks all on a single chip, offering not just the small size and cost-effectiveness but low-noise, low-power, and long-term implantable solution. The general design strategies for neural recording interface IC are investigated and summarized in the following sections.

The architecture of the implanted neural recording system does influence the input signal to the amplifier as well as the design requirements of the neural amplifier. In this project, the architecture was implemented as shown in Figure 2-3. Neural amplifiers are attached closely to the electrode so that there will be little noise or interference introduced into the signal at the input of the amplifiers. Other blocks like power link and wireless transmission blocks are placed outside skull so as to relax the area and power limit on the amplifier, and therefore more well-established design techniques can be used. In addition, the analog to digital converter (ADC) was added to the front-end analog chip because the area of ADCs is very small as compared to that of the 100-channel neural amplifiers. The signal to noise ratio (SNR) can be further improved since the ADC is placed on the same chip with the neural recording amplifier. The signals transmitting through the wires will purely be digital, which can be much more immune to noise and interferences compared to analog signals.

Figure 2-3. Block diagram of neural recording system architecture used in this project.

Figure 2-4. Conventional structure of the multi-channel neural recording system [19].

In order to minimize the power consumption and chip area of the neural recording interface chip, the system architecture must be carefully planned. The basic and essential functions of a typical neural recording interface system are amplification, low-pass filter, high-pass filter, digitization and transmission. Recently, researchers have proposed many neural amplifiers for proficient neural

recording. Usually the power supply for the implantable device can be supplied by the wireless power link. At the same time, command and clock signal can be transmitted through the power link as well. The amplifier array directly interfaces with the multi-electrode array. The signal is passed on to the ADC for digitization and then transmitted as RF data to outside of the human body.

A detailed study on the design optimization of conventional integrated neural recording systems has been conducted by Liu Wentai's group [19]. The general system structure analyzed is shown in Figure 2-4. In terms of the number of recording channels per ADC, a mathematical model is created to calculate the best trade-off between the area occupation and the power consumption of the neural recording system. It concludes with the optimal multiplexing ratio in the condition that the product of area and power of the system is met. The optimum design for neural recording systems is 16 channels per ADC, yielding a minimum power and area product. If area is not a concern, having one channel per ADC will provide the best power efficient. In the actual neural recording system design, the front-end analog part is on the top of multi-electrode array. Thus, the area of the neural recording channels is repeatedly restricted by the concerns on the density of the recording sites, the fabrication cost, and the yield [18]. In this project, the 100-electrode array measures about 5 mm by 5 mm.

Another design reported by Harrison [3] realized these essential functions in a wireless 100-electrode neural recording system. Due to the high data rate generated from 100-channel neural signals, data reduction technique is induced in the system. The low-power ADC together with spike detectors were employed to decrease the data rate for transmission and at the same time the critical data on

spikes were preserved. Also, to record neural signals from an Utah Electrode Array in cat cortex, a two-chip system was used and the digitized signals were wirelessly transmitted to a receiver. The chip was reported to consume as large as 13.5 mW of power.

The recently reported neural recording system has the highest electrode density of 256 channels. It is developed by J. N. Y. Aziz [18] and the circuit is showed in Figure 2-5. To reserve the temporal correlation of neural signals among the adjacent channels, every electrode connects to its own voltage amplifier which has a dedicated memory. There is a trade-off between the data rate and the recording accuracy due to the employment of the switched-capacitor delta read-out circuit. Since telescopic topology is used in the amplifier, a high voltage supply is necessary to drive the amplifier, which is not desirable in the low voltage low power design. Although delta compression reduces the data rate and hence relaxing the requirement for wireless transmission, it may also result in losing of useful data and degradation of SNR, which is not preferred by neuroscientists.

The system structure of a conventional multi-channel neural recording interface IC is presented in Figure 2-6. A low-noise neural amplifier interfaces with electrodes to capture, amplifier and filter the signal, followed by a second-stage amplifier for further gain boosting. After that, the multi-channel neural signals will pass through an analog multiplexer before the digitization. Some designs perform data compression on-chip to reduce the volume of the data [18][20][21]. However, most data compression techniques may result in the loss of useful data or introduce additional noise and are of course not favored by doctors [22].

Figure 2-5. Block diagram of the recording system [18].

Figure 2-6. Conventional system architecture for multi-channel neural recording interface IC.

2.3.2 Low Noise Front-end Amplifier Design

The low noise front-end neural amplifier is one of the main modules in the neural

recording system interface IC. It is located at the most front-end of the system and most of the system parameters depend on the performance of the neural amplifier. The overall requirements for neural recording amplifier design are stated in Figure 2-7.

The gain of the front-end amplifier is usually designed according to the amplitude of the target signal, input-referred noise requirement, silicon area consumption, etc. If a large gain of more than 100 is required, a two-stage amplification will be necessary since it is not practical to implement using single amplifier due to the large silicon area consumption. The system gain of the recent published designs ranged from about several hundred to several thousand, and the gain of the neural amplifier is usually fixed at 100 or below to prevent amplifier saturation due to dc offset [23-36]. Since neural signals have different amplitudes and bandwidths, it is better to have the amplifier gain and bandwidth both programmable, which will be discussed later in Chapter 3.

Figure 2-7. Requirements for neural amplifier design [34].

Among those requirements, AC coupling, bandwidth configuration, noise performance and high input impedance are the most challenging consideration in the amplifier design.

2.3.2.1 High-pass Techniques

First of all, the dc offset voltage across the electrode is unpredictable. A high-pass filter eliminates the low-frequency components, including the dc offset at the electrode. Neural signals together with the electrode dc offset voltage can be amplified by the neural amplifier without saturating the output stage if the dc gain is low enough, otherwise with a high dc gain, the neural amplifier may suffer saturation. To avoid saturation of neural amplifier, a high-pass filter [23-30] is usually inserted to remove the dc components while keeping low frequency local field potentials.

In order to arrive at the ultra-low cutoff frequency required for the biomedical signal, large capacitor or resistor is required. But passive components are impractical for on-chip implementation due to silicon area limitation. The easiest and most direct way to realize the high-pass function is using external capacitors [23][28]. However, this approach will increase the design cost, and result in bulky devices, which is not suitable for implantable applications. One approach reported by T. Denison, where the high-pass filtering characteristic of the instrumentation amplifier is achieved and tuned using switched capacitor method [29]. This technique is helpful for realizing fully integrated system, but it requires additional control clocks and the switching switches lead to poor noise figure and high power consumption. An effective way to achieve ultra-low cutoff frequency

was first proposed by R. R. Harrison [9], where a huge resistance value in the range of $10^{12} \Omega$ can be achieved with negligible silicon area by employing a MOS-bipolar pseudo-resistor structure.

Figure 2-8. Schematic of the low noise amplifier proposed by R. R. Harrison [9]

Figure 2-9. Simulation results of the pseudo-resistor proposed by R. R. Harrison [9]

A digital-assist neural recording front-end was reported in 2012 [31], in which the very low frequency components was removed at the neural amplifier, i.e., the low noise amplifier (LNA) input by subtracting the feedback from the signal after digital signal processing (DSP), as depicted in Figure 2-10. The enhanced architecture is combined with a merged instrumentation amplifier-digital to analog converter (DAC) that permits noise-efficient offset cancellation, together with a voltage control oscillator (VCO)-based analog to digital converter (ADC) to achieve state-of-the-art performance in a power efficient way under a 0.5-V supply. This design, however, contains some inadequacies: first, because of the dc bias at the input through the inaccurate large-impedance pseudo resistors, the neural amplifier might need additional start-up circuit, since the amplifier is stable when both inputs are at 0 V; second, by adding the pseudo resistor at the input of the neural amplifier, the noise of the neural recording front-end is increased as compared to Harrison's design.

2.3.2.2 Low noise techniques

The noise performance is another important characteristic of the front-end neural recording amplifier, which determines the detection accuracy of the overall system. Minimizing the input-referred noise of the neural amplifier is very critical, which usually requires high quiescent current. However, the tight power budget may limit the current allocated to the front-end amplifier. As a result, achieving optimum trade-off between noise and power for the front-end amplifier becomes increasingly important. To boost the current efficiency of the amplifier, subthreshold operation of the input pair transistor is adopted [3][9], where the

transconductance g_m is proportional to the drain current. This is preferred as compared to the saturation operation of the input transistors where g_m is proportional to the square root of the drain current, resulting in lower power efficiency.

Another approach employs both NMOS and PMOS transistors as the input pair of the operational transconductance amplifier (OTA) to reduce the input-referred noise [26]. One circuit example is given in Figure 2-11 [27]. By doing so, the input transconductance becomes $(g_{mn}+g_{mp})$, where g_{mn} and g_{mp} are the transconductance of the NMOS and PMOS input transistors, respectively. This will reduce the thermal noise floor by approximately half and thus suppress the input-referred noise. One drawback of such design is that the quiescent current of the OTA structure depends heavily on the supply voltage and also the process variation. The PMOS and NMOS current source/sink of the OTA is not biased by a fixed reference voltage. The total bias current of the OTA is decided by the voltage overdrive ($V_{gs} - V_{th}$) and aspect ratio of the tail transistors. Any voltage variation of the power supply will completely impose the V_{gs} of the tail transistors and thereby change the quiescent current of the OTA significantly. As a result, such structure is not suitable for battery operation because the supply voltage of battery will not remain constant through its entire lifetime. In addition, the transistor threshold voltage of the fabricated chip may be different from the simulated level due to process variation. This will also contribute to variation of the OTA current. The changing of the bias current of the OTA will result in many undesirable outcomes, such as increased noise level, more power consumption, reduced open-loop gain, etc.

Figure 2-11. Schematic of amplifier structure proposed by M. Chae [27].

To further reduce the amplifier noise, various noise reduction techniques were proposed to improve the noise performance by cancelling partial circuit noise with additional power consumption. One good example of noise cancellation is the feed forward noise cancellation for wide band application, as demonstrated in Figure 2-12 [35]. In this method, an additional amplification stage is used to cancel the noise contribution from the input transistor. By increasing the current, the noise from the addition amplification stage can be minimized. This scheme breaks the relationship between the noise and input matching problem. Theoretically it can achieve a very low noise performance at the cost of power consumption. But for implantable devices, power is always a limitation.

Figure 2-12. Feed forward noise cancellation circuit [35].

Figure 2-13 illustrates another example of noise reduction using feedback [36]. In this approach, the noise at the output is suppressed by the two different feedback paths, according to the feedback theorem. But none of the device noise is completely cancelled. As we can see from those examples in Figure 2-12 and Figure 2-13, for the noise cancellation techniques used in amplifier design, usually there is an additional amount of power used in order to suppress noise. But the effectiveness of the noise reduction technique in terms of power has not yet to be evaluated.

Figure 2-13. Feedback noise reduction circuit [36].

Figure 2-14. Schematic of positive gain feedback neural recording amplifier [32]

2.3.2.3 Input impedance improvement

Another important factor, that needs to be considered during neural recording system design, is the input impedance of the neural amplifier. A voltage divider is formed between the electrode impedance and amplifier input impedance, which attenuates the signal at the input of the neural amplifier. Especially during chronic neural recording, the electrode impedance increases when time varies due to the encapsulation degradation. A generally accepted attenuation through the voltage divider is 10 percent. This is under the condition that all the impedance contributors to the input impedance of the neural amplifier are considered [14].

The input impedance is largest under the condition that it consists only of stray capacitances which are inevitable if the electrode is connected to the neural

amplifier [33]. T. Borghi proposed a positive-gain feedback amplifier [32], as shown in Figure 2-14, in which the input signal drives the gate of a CMOS differential stage directly. But this is not desirable in terms of patient's safety since there might be direct current flow from the biasing circuit of the input through the tissue. If a capacitor is introduced between the electrode and the amplifier, the input impedance will be much lower [3][9][27].

The open-loop amplifier is another possible way to improve the input capacitance. For open-loop amplifiers, the input impedance is no longer limited by the feedback capacitors, instead, the gate of the input transistors. Thus, the input impedance can be largely improved. A pseudo open-loop amplifier for neural interface systems was proposed by Sun-II Chang in 2009 [12], as shown in Figure 2-15. The proposed amplifier consumes 400 nA current at 2.5 V power supply. The measured input-referred noise is very low, of $1.69 \mu\text{V}_{\text{rms}}$ from 0.3 Hz to 1 kHz. The flicker noise is reduced through the application of chopper stabilization at the input and output the amplifier. The proposed pseudo open-loop neural amplifier has the benefit of high linearity and immunity to process and bias variations. However, the bandwidth of this design is limited by the chopper frequency. Thus, by consuming the same amount of power it is hard to achieve a large enough bandwidth to acquire detailed neural signal information, as required by neuroscientists. The detailed amplifier circuit schematic is shown in Figure 2-16. All the transistors of the first-stage amplifier operate in weak inversion region. The gain is obtained by the current ratio, which can provide stable operation for various supply current variations.

Figure 2-15. A pseudo open-loop amplifier proposed by Sun-II Chang [12].

In this case, dc offset at the electrode is avoided by using large parasitic electrode capacitance (C_E). But in real situations, the electrode consists of both the capacitive component and resistive components, as discussed earlier in Section 2.1. As a result, there is still electrode dc offset at the input of the amplifier, which should be eliminated to avoid preamplifier saturation.

Figure 2-16. Open-loop preamplifiers proposed in [12]: (a) 1st stage amplifier (weak inversion), and (b) 2nd/3rd stage amplifiers (strong inversion).

[37][38] proposed an instrumentation amplifier with impedance boosting loop

for the use with active electrode for EEG monitoring, as depicted in Figure 2-17. The positive feedback loop is used to increase the amplifier's input impedance. The loop supplies part of the current via C_{fb} into C_1 , thus reducing the current drawn from the electrode. Hence, the effective input impedance of the amplifier is improved. To minimize the loading effect from the impedance boosting loop, this system requires an additional buffer, which then consumes additional power and area.

Figure 2-17. Input-impedance boosting via partial positive feedback [37].

2.3.3 Activity Based Low Power Neural Recording Analog Front-end Design

In neuroscience research and clinical neuroprosthesis, simultaneous activities of

a large population of neurons have to be recorded, transmitted and processed for neural pattern classification and recognition [39][40]. Conventionally, a complete set of recorded raw data is preserved for data analysis [27]. However, for the recently emerging implantable wireless neural recording microsystem, the compression of this large volume of data becomes of great necessity to reduce the effective transmission data rate so as to lower the power consumption of the entire recording implant [41], which is the key to minimize the required power and size of the data transmitting coils, thereby alleviating the excessive heat dissipation caused by the implanted electronics.

In the neural recording system, the neural activity is recorded as action potentials (APs). And then neural activities are decoded from these recorded APs using different decoding methods such as the firing rate decoding, temporal decoding and population decoding [42]. Since AP represents the complete neural information, by detecting the APs and transmitting only APs, not only the signal integrity is preserved, the data volume required for neural information decoding [43] is also reduced.

In [3], only the occurrence of APs is detected, resulting in a data rate of 330 kbps from 100 recording channels. However, recording of a complete AP waveform is essential to better understand brain functionality and to predict the intended movements. In [44] and [45], the neural AP detection is conducted in digital domain and it outputs only the detected APs for transmission, achieving more than 90 percent data compression. It has relatively accurate control in AP waveform preservation since it performs AP detection after data quantization. However, the system requires large on-chip memory and computation resources

to store and process the quantized data from all the channels. It therefore consumes a significant amount of power, especially among the analog-to-digital converters (ADCs) that are constantly on. In [43], the AP is detected in the analog domain before quantization and an analog delay of $600\ \mu\text{s}$ is inserted in the front-end channel to preserve the AP waveform before crossing threshold voltages. No memory is required and the ADCs can be switched off using this AP detection strategy. However, the time delay implemented using the analog filter can be significantly affected by process variation and mismatch, which makes the preservation of complete AP waveform uncertain, especially when the recording is performed from a large number of channels simultaneously. Therefore, an AP detection method providing precise preservation of AP waveform without requiring large memory and computation resources or power penalty is highly in need.

Figure 2-18. Waveforms in the AP detector blocks. (1) Incoming AP waveform. (2) Enhanced AP. (3) Time window generated upon threshold crossing. (4) Time delay T_d applied, so the detected AP is available from its onset [43].

Chapter 3. DESIGN OF LOW NOISE ANALOG FRONT-END IC FOR NEURAL RECORDINGS

The neural amplifier is one of the most significant circuit blocks in the neural recording system. In terms of noise performance, the neural signals are usually being amplified by one hundred times from hundreds of microvolts to tens of millivolts via the neural amplifier. So the noise of the system is mainly contributed by the neural amplifier, while the noise generated from the subsequent circuits has much less impact. In terms of power and area, 100 neural amplifiers are required for a 100-channel recording system (one amplifier per channel), but it only requires less than ten multiplexers (MUX) and ADCs, depending on the multiplexing ratio; one transmitter; and other reference circuitry [46]. Therefore, in the analog front-end, the neural amplifiers occupy most of the area and consume most of the power. Hence, the trade-off among the noise performance, power consumption and layout area is utmost important in neural amplifier circuit design.

3.1 System Structure for Neural Recording Interface Front-end

The system architecture of the proposed neural recording system front-end is shown in Figure 3-1. To match the layout area with the multi-electrode array fabricated by Institute of Microelectronics (Singapore), 100 channels divided into ten recording blocks are implemented on the single chip. Each block includes four main circuit blocks: amplification block, digital control block, multiplexer and ADC. One ADC is required in every ten recording channels.

The neural signal is acquired by the electrode and passed on to the amplification block. The ADC in turn digitizes the amplified signal and sends it to the RF transmitter for wireless transmission. The clock is recovered from the carrier received through the RF coil. The power is also recovered from the RF coil and then passed through Low Dropout Regulators (LDO) to provide a stable supply voltage. A digital power supply and an analog power supply are provided through different LDOs to prevent interference from the digital block to the analog block. The digital control block is used to set bandwidth and gain parameters of each individual amplifier as well as to handle the reset and power down commands.

Figure 3-1. System architecture for proposed neural recording system.

For the amplification block, since the neural signal is too weak to directly interface with multiplexers, each channel has its own amplifier before multiplexed to ADC. Conventional two stage amplification is employed in order to prevent amplifier saturation and to save on silicon area. Unlike other structures where the second stage has a programmable gain, the proposed structure is

organized in the following manner (Figure 3-2).

Figure 3-2. Proposed neural recording interface analog front-end.

The local field potential usually has larger amplitude, and hence, the amplifier gain needs to be small to avoid saturation. In contrast, AP usually has smaller amplitude which implies that the amplifier needs a larger gain. Moreover, the AP and the LFP have different bandwidths. The LFP is in low frequencies while AP resides in slightly higher frequencies. Therefore, in order to record the neural signal more precisely and efficiently, systems allowing programmable gain and bandwidth are obligatory. The programmable gain can be 50 or 100 V/V, which is set in the first amplifier stage. The bandwidth can be programmed at 0.1 Hz to 300 Hz, 0.1 Hz to 5 kHz, or 300 Hz to 5 kHz, in the second amplifier stage. By changing the gain and bandwidth configurations, we can record either the LFP only, or AP only, or both.

Since the first-stage amplifier has much larger influence on the system noise

performance, the noise of the first-stage amplifier must be minimized at the expense of power consumption. Given a large current flowing in the amplifier, it is difficult to set a narrow bandwidth unless large capacitors or resistors are deployed, which would mean large silicon area. The second-stage amplifier usually consumes much less current compared to the first-stage amplifier because the noise requirement is relaxed a lot. Hence, it is better to implement the programmable bandwidth function in the second-stage amplifier to minimize the total silicon area consumption. On the other hand, the programmable gain is set at the first-stage amplifier. By either changing capacitor ratio or bypassing some gain elements, we can easily set the desired gain without any additional power or area consumption. Further discussion will be provided in the following sections. This thesis mainly covers the neural recording amplifier design.

3.2 Design Requirements for Neural Amplifiers

The detailed design requirements for neural amplifiers are discussed here.

3.2.1 Low Intrinsic Noise

The first prerequisite for the neural amplifier is that the noise level must be very low. Due to the thermal noise and $1/f$ noise, the amplifier induces additional noise to the signal that is inevitable. This is because the neural signal to be amplified is far too weak (several hundred of microvolts); the noise generated from the neural amplifier should therefore be suppressed to prevent the crushing of the neural signal.

Besides the intrinsic noise sources from the transistors, the interference noise

from circuits other than the neural amplifiers on the chip such as switching in multiplexer and clocking in digital circuitry, etc. must all be considered. The transient current noise due to switching might be coupled to neural amplifiers via parasitic capacitances between interconnects or the substrate, which degrades the noise performance of the neural recording system. This type of interference or noise can be suppressed via a carefully designed layout with a fully differential structure. The commonly acceptable requirement for the noise from the neural amplifier is such that the neural amplifier must have an input-referred noise less than 5-10 μV_{rms} , which is defined by the typical background noise of the extracellular neural recording [47].

3.2.2 Low Power Density

Effective and reliable neurological researches and diagnoses rely on multi-channel recordings of a huge population of neurons. Multi-channel high-density recording systems with 100 channels up to as many as 256 channels have recently been reported [18]. Since any amount of excessive heat dissipation by the recording microsystem induces damage to the surrounding tissue when it is implanted in the brain, the power consumption of the high-density recording electronics should be strictly restrained. In addition, implantable devices are usually powered through wireless power transfer links to obviate the need of large-capacity batteries or skin-piercing wires. The specific absorption rate of living tissue sets a stringent limit on power budget of the implant. A power density of 80 mW/cm^2 might result in necrosis in tissue [3]; hence, the power consumption of an implantable device should be limited by this amount of heat flux for a given implant size. Meanwhile, chip area is also the key constraint for

implantable devices—to minimize surgical damage. The simultaneous requirements of low power consumption, minimum chip area, and a large number of recording sites collectively impose a critical challenge to IC designers.

3.2.3 DC Offset Rejection

The next important requirement of neural amplifiers is the large dc offset voltage that must be handled during recording. A gold electrode in a buffered saline electrolyte can generate a dc offset voltage as high as ± 50 mV [15]. Due to large gain of the neural amplifier, this small offset may easily cause the amplifier to saturate. Thus, the neural amplifier must be able to reject the dc offset voltage while capturing the low-frequency neural signals.

Table 3-1. Design target for the neural recording front-end circuits.

Specification	Value	Comments
Supply voltage	1 V	0.18- μ m CMOS process
No. of channels	100	
Average current/channel	$< 3 \mu\text{A}$	
Amplifier current	$< 1.2 \mu\text{A}$	Front-end amplifier only
Gain	500 - 1000	Programmable gain
Input-referred noise	$< 5 \mu\text{V}_{\text{rms}}$	Integrated in the signal band
High-pass corner frequency	0.1 Hz	
Low-pass corner frequency	5 kHz	
THD	$< 1 \%$	
Input capacitance (impedance)	$< 20\text{pF}$	As small as possible
Channel isolation	$> 80 \text{ dB}$	Adjacent channels
Average area per channel	$< 0.4 \text{ mm}^2$	As small as possible

3.2.4 Lower Cutoff Frequency

The last requirement of the neural amplifier design is related to the cutoff frequency. The neural amplifier should only amplify the signal within the signal bandwidth while rejecting the out-of-band noise. Since the neural signals is located at below 1 Hz to 5 kHz [3], the neural amplifier should have a lower cutoff frequency of lower than 1 Hz to remove the dc offset at the electrode; and a higher cutoff frequency of about 5 kHz, to avoid excessive noise from being mixed with the output signal. All the above design specifications are summarized in Table 3-1, while the neural signal characteristics are described in Table 3-2.

Table 3-2. Neural signal characteristics defined for this project

	Bandwidth	Amplitude
Local Field Potential	0.1 Hz to 300 Hz	100 μ V to 2 mV
Action Potential	300 Hz to 5 kHz	30 μ V to 1 mV [48]

The rest of the thesis will describe the various techniques for designing neural recording amplifiers that can meet the specifications discussed above.

3.3 Design A: Neural Recording Amplifiers with Noise Reduction Techniques

Noise reduction has been one of the most important factors of the front-end amplifier (FEA) design. In order to reduce noise from active devices, the most

straightforward approach is to increase the operating current. However, the total amount of current consumption is preferred to be kept at the lowest, especially in battery powered systems such as portable electronics, as well as wearable and implantable biomedical devices [49][50][51]. Therefore, there is a strong trade-off between the noise performance and power consumption in the FEA design.

Recently, low-noise low-power FEAs with various noise improvement techniques have been reported [35][36][52]. These noise reduction techniques are implemented through adding extra circuitry, with an aim to cancel out a significant part of circuit noise. Inevitably, these extra circuitries add on to the total power consumption. One representative example of such technique is the feedforward noise cancellation scheme reported in [35], whereby an additional amplification stage is used to cancel the noise generated by the input transistor. By biasing with just a sufficient amount of current, noise from the additional amplification stage was minimized. This scheme therefore breaks the tie between noise performance and input matching in wideband RF FEA. Theoretically, it can achieve very low noise at the cost of increased power consumption. Another example, which is based on the noise feedback scheme, is reported in [36]. In this approach, the overall output noise is suppressed by engaging two different feedback paths—one for signal and the other for noise. However, none of these device noise components can be completely cancelled. From our investigation, it is found that most of the reported FEA noise cancellation techniques require additional circuitry, hence power consumption in order to suppress the noise. Nevertheless, the effectiveness of these noise reduction techniques has yet been evaluated considering the extra circuitry and power consumption required.

In this chapter, various techniques to improve the noise performance of analog front-ends (AFE) are analyzed and compared based on a noise efficiency factor (NEF), which is commonly used to evaluate the noise-power trade-off of FEA designs. First, various noise reduction techniques are introduced. This is followed by several sections, to analyze the well-known noise reduction techniques and for comparing the effectiveness of these reported techniques, mainly on the noise-power trade-off. Based on the analysis, a low-noise low-power neural amplifier is designed to achieve the best noise-power trade-off.

3.3.1 Noise Reduction Techniques

In this section, common CMOS noise reduction techniques will be reviewed to bring to light the noise reduction efficiencies.

3.3.1.1 Feedforward Noise Reduction

A number of noise reduction techniques make use of the property where the output noise and noise at the feedback point are in phase, while their respective signals are out of phase. The two noises can therefore cancel each other by amplifying the noise at the feedback point negatively and then summing it with the noise at the output. However, the signals will be added constructively.

Figure 3-3. Feedforward noise reduction model.

Figure 3-3 presents the model of a well-known feedforward noise reduction technique [35]. The output noise is sensed at AMP₁ output and fed back to node F. Noise from amplifier AMP₁ then combines with this feedback noise after amplification through the feedforward amplifier AMP₂. By doing so, the noise from AMP₁ can be totally cancelled when the gain of AMP₂ denoted by A_2 and the feedback factor denoted by β are carefully set to satisfy the condition, $\beta A_2 = 1$. Note that noise from AMP₂ is not reduced but can be suppressed by increasing current consumption of AMP₂.

3.3.1.2 Signal-Nullled Noise Feedback

In the feedback noise reduction technique [36] depicted in Figure 3-4, the output noise is sensed at the summing node S, feedback to node F through the signal-nulled feedback network consisting of β_1 and β_2 , amplified by AMP₂, and then

added at node S in the opposite phase. While the noise is suppressed, the signal is not affected if β_1 and β_2 are designed such that node F behaves as a virtual AC ground. In this configuration, the noise is suppressed by the global feedback loop and hence the noise from AMP₂ is also reduced. This is in contrast to the feedforward noise reduction approach. However, noise from either AMP₁ or AMP₂ cannot be completely eliminated. Consequently, for a better noise performance, the transconductances of the amplification devices in AMP₁ and AMP₂ need to be increased by consuming more power.

Figure 3-4. Signal-nulled noise feedback model.

3.3.1.3 Current Reuse

In the current reuse scheme, the multiple transistors are stacked in the same current branch to generate multiple transconductances from a single current branch. The resulting multiple transconductances are combined to provide a larger effective transconductance with the same amount of current consumed, when compared with a single device in a single branch. By obtaining a larger transconductance, a lower thermal noise can be achieved. One disadvantage of

this scheme is that due to the limited voltage headroom, the signal swing range and linearity performance can be degraded unless careful attention is paid to the design.

3.3.2 Noise-Power Trade-off Analysis

By evaluating the additional power required for different noise reduction techniques, the noise-power trade-off of the techniques can be analyzed through NEF.

In the following analysis, the same bandwidth and the same input transistor size are assumed. The noise from the feedback network is not included in the calculation because it can be avoided using capacitive feedback network. In the analysis to be discussed, the thermal noise has also been assumed to dominate.

3.3.2.1 Feedforward Noise Reduction

The feedforward noise reduction technique is used to break the relation between the noise and input matching in wideband RF FEAs. Figure 3-5 shows one representative example. By dissipating enough current at M_2 , a good noise performance can be achieved at the expense of power consumption.

Figure 3-5. Feedforward noise cancellation circuit [35].

Assuming the noise from R_S and R_F are negligible by using capacitors, the condition for noise cancelling in this circuit is that the negative gain and positive gain of the noise can be totally cancelled at the output node. The positive gain is from Y to the output through the source follower, which is approximately 1. The negative gain is from Y to X then to the output through M_2 , which is $\frac{g_{m2}}{g_{m3}} \left(\frac{R_F}{R_F + R_S} \right)$. Once the noise from M_1 is totally cancelled, the noise of the circuit is mainly contributed by M_2 .

By equating the positive gain to the negative gain, the noise from M_1 is completely cancelled when gain stage consisting of M_2 and M_3 satisfies that the below:

$$A_2 = \frac{g_{m2}}{g_{m3}} = 1 + \frac{R_F}{R_S} \quad (3-1)$$

where g_{m2} and g_{m3} are the transconductances of transistors M_2 and M_3 , respectively. The output noise is mainly contributed from the thermal noise of M_2 , which can be expressed as

$$\overline{V_{no}^2} \approx \overline{V_{no,M_2}^2} = \frac{4kT\gamma g_{m2}}{g_{m3}^2} \cdot \Delta f \quad (3-2)$$

where γ is the excess noise factor, and T is the absolute temperature. The NEFs with and without feedforward noise cancellation are calculated as (3-3) and (3-4), and their ratio is derived in (3-5).

$$NEF_{w/o,NS} = K \sqrt{\frac{4kT\gamma}{g_{m1}}} \cdot \Delta f \sqrt{I_1} \cdot \left(\frac{R_S + R_F}{R_F}\right) \quad (3-3)$$

$$NEF_{w,NS} \approx K \sqrt{\frac{4kT\gamma}{g_{m2}}} \cdot \Delta f \sqrt{I_1 + I_2} \cdot \left(\frac{R_S + R_F}{R_F}\right) \quad (3-4)$$

$$\frac{NEF_{w,NS}}{NEF_{w/o,NS}} = \frac{1}{2} \sqrt{\frac{I_1 + I_2}{I_1 \cdot I_2}} \quad (3-5)$$

where $K = \sqrt{2/(4kT \cdot \pi \cdot U_T \cdot BW)}$. According to (3-5), the minimum NEF with the feedforward noise cancellation technique can be achieved when I_1 and I_2 are set to be equal.

$$\left. \frac{NEF_{w,NS}}{NEF_{w/o,NS}} \right|_{\min} = \frac{\sqrt{2}}{2} \approx 0.71 \quad (3-6)$$

From (3-6), we can conclude that the noise-power trade-off is improved by up to $\sqrt{2}/2$ times, compared to circuit without noise cancellation. Note that M_3 also generates noise, which is ignored in the analysis above because g_{m3} is much smaller than g_{m2} . That means this optimum NEF is not achievable due to the excess noise from M_3 .

3.3.2.2 Signal-Nulled Noise Feedback

Figure 3-6. Signal-nulled noise feedback circuit [36].

The circuit using signal-nulled noise feedback technique was illustrated in Figure 3-6. The noise sources are contributed by the two amplifiers, AMP₁ and AMP₂, as described in (3-7).

$$\overline{v_n^2} = 4kT\gamma(g_m + g_{mfb})R_{out}^2 \cdot \Delta f \quad (3-7)$$

where g_m and g_{mfb} are the transconductances of amplifier AMP₁ and AMP₂, respectively, and R_{out} is the total output impedance. In this configuration, the signal-nulled noise feedback is valid if the ratio of C_1/C_2 is equal to the voltage gain of AMP₁, and node A does not carry any signal but noise. The output noise voltages, both with and without noise suppression are expressed in (3-8) and (3-9), respectively.

$$\overline{v_{no,w,NS}^2} = \frac{4kT\gamma(g_m + g_{mfb}) \frac{(R_S + R_F)^2}{(1 + g_m R_S)^2} \cdot \Delta f}{(1 + g_{mfb}/g_m)^2} \quad (3-8)$$

$$\overline{v_{no,w/o,NS}^2} = 4kTg_m \frac{(R_S + R_F)^2}{(1 + g_m R_S)^2} \cdot \Delta f \quad (3-9)$$

The NEF improvement is evaluated in (3-10).

$$\frac{NEF_{w,NS}}{NEF_{w/o,NS}} = \frac{v_{no,w,NS}}{v_{no,w/o,NS}} \sqrt{\frac{I_1 + I_2}{I_1}} \quad (3-10)$$

By substituting (3-8) and (3-9) into (3-10),

$$\frac{NEF_{w,NS}}{NEF_{w/o,NS}} = \sqrt{\frac{I_1 + I_2}{\sqrt{I_1} + \sqrt{I_2}}} \frac{1}{\sqrt{I_1}} \quad (3-11)$$

Therefore, the maximum NEF improvement by a factor of 0.91 is achieved when

$$I_2 = (\sqrt{2} - 1)^2 \cdot I_1.$$

$$\left. \frac{NEF_{w,NS}}{NEF_{w/o,NS}} \right|_{\min} = \sqrt{2\sqrt{2} - 2} \approx 0.91 \quad (3-12)$$

3.3.2.3 Current Reuse

An example of amplifiers using the current reuse technique is depicted in Figure 3-7.

Figure 3-7. Noise reduction circuit employing current reuse technique.

The output noise consists of the noise from both M_P and M_N :

$$\overline{v_{no}^2} = 4kT\gamma(g_{mp} + g_{mn})R_{out}^2 \cdot \Delta f \quad (3-13)$$

where g_{mp} and g_{mn} are the transconductances of M_P and M_N , respectively. It is assumed that the M_P and M_N are matched so as to have the same transconductance. Hence, the noise-power trade-off of this circuit can be derived as

$$NEF_{w,NS} = K \cdot \frac{\overline{v_{no}}}{g_{mp}R_{out} + g_{mn}R_{out}} \sqrt{I_{total}} \quad (3-14)$$

The NEF of the circuit using only NMOS or PMOS as the input transistor is given by

$$NEF_{w/o,NS} = K \cdot \frac{4kT\gamma g_{mn}R_{out}^2 \cdot \Delta f}{g_{mn}R_{out}} \sqrt{I_{total}} \quad (3-15)$$

The ratio of NEFs with and without the technique applied is calculated as

$$\frac{NEF_{w,NS}}{NEF_{w/o,NS}} = \frac{\sqrt{2}}{2} \approx 0.71 \quad (3-16)$$

The NEF is improved by a factor of $\sqrt{2}/2$. Note that no other noise sources have been ignored during the analysis.

The results of the noise-power trade-off analysis performed for different noise reduction techniques are summarized in Table 3-3. For the feedforward noise reduction technique, complete cancellation of the thermal noise from the input matching transistor is possible. However, the noise from the feedforward amplifier is not cancelled. This additional noise contribution can be suppressed by flowing more current into the feedforward amplifier, but at a penalty of degrading the current efficiency. For signal-nulled noise feedback technique, the noise from both main amplification and feedback amplification elements are suppressed, but none of them is completely cancelled. From Table 3-3, we can conclude that among these noise reduction techniques, although the current reuse technique is simple, but it is able to provide the maximum current efficiency, resulting in the best noise-power trade-off.

To further improve the noise-power efficiency, transistors operating in the weak inversion region are employed to maximize the current efficiency. However, this is often achieved at the expense of larger chip area. A combination of the noise reduction techniques discussed is also viable to help improve the design.

Table 3-3. Noise-power trade-off analysis summary

Noise reduction method	Minimum achievable NEF
Feed forward noise cancellation in [35]	$> \frac{\sqrt{2}}{2} NEF_{w/o,NS} \approx 0.71 \cdot NEF_{w/o,NS}$
Signal-nulled noise feedback in [36]	$\sqrt{2\sqrt{2}-2} NEF_{w/o,NS} \approx 0.91 \cdot NEF_{w/o,NS}$
Simple current reuse technique	$\frac{\sqrt{2}}{2} NEF_{w/o,NS} \approx 0.71 \cdot NEF_{w/o,NS}$

3.3.3 Circuit Implementation of Closed-loop Neural Amplifier

In order to achieve a well-defined voltage gain and robust performance, a closed-loop configuration is selected. The resistive feedback topology usually results in high noise and necessitates large current. The amplification is therefore realized through the capacitive feedback illustrated in Figure 3-8.

A fully differential structure helps to reduce the effect of the common-mode noise. The mid-band gain of the proposed neural amplifier is decided by the ratio of C_1/C_2 or $C_1/(C_2C_3/(C_2+C_3))$, where $C_1 = 20$ pF and $C_2 = C_3 = 0.4$ pF, to attain a gain of 34 dB or 40 dB. The pseudo-resistor in the feedback loop sets the dc level at the input of the OTA. The value of pseudo-resistor together with C_2 and C_3 determines the high-pass corner of the neural amplifier. The frequency of interest in neural signal recording can be as low as 1 Hz. It is thus challenging to capture such low-frequency signal components using the passive devices available on-chip. Since the pseudo-resistor can generate resistance in the order of up to Tera- Ω , a very low cutoff frequency can be realized without any external component.

To further enhance the gain of the recording channel, the band-pass filter (BPF)

following the neural amplifier is implemented, to provide an additional gain of 10. The BPF decides the low-pass cutoff frequency of the system, and the neural amplifier has a bandwidth higher than the signal bandwidth.

The neural recording amplifier design requires both low noise amplification and low power consumption, concurrently. Unfortunately, the noise performance and power efficiency of the amplifier are contradictory parameters to each other. In order to assess the effectiveness of a design in addressing trade-off between the above two parameters, NEF is often used (as defined in Chapter 2). A lower NEF indicates a better design in dealing with the trade-off, which implies a good noise performance while consuming low power.

Figure 3-8. Improved design for neural recording amplifier.

Minimum noise contribution from the recording circuit can be realized with higher power dissipation. However, as mentioned above, the front-end neural amplifier needs to consume as little power as possible so as to minimize the total system power consumption. To achieve good noise performance with limited power consumption, a comparative study and analysis on the various noise reduction techniques have been carried out above with the conclusion that the noise reduction using current-reuse technique has the best power efficiency, i.e. NEF. Both NMOS and PMOS transistors are stacked in the same current branch to generate a double transconductance g_m from a single current branch. Meanwhile, the subthreshold operation provides much better current efficiency and is hence adopted widely in various biomedical recording systems.

The g_m of a MOS transistor in deep subthreshold region can be approximated as [53][54]

$$g_m \cong \frac{I_D}{nU_T} \quad (3-17)$$

where n is the slope factor (a typical value of n is 1.5), I_D is the drain current, and U_T is the thermal voltage. Thus, Equation (3-18) models the subthreshold MOSFET's thermal noise power spectrum density [47]

$$\overline{i_n^2} = 4kTn\Gamma g_m \quad (3-18)$$

where k is the Boltzman constant, and T is the absolute temperature. The thermal noise factor Γ for a strong inversion region (Γ_{si}) is 2/3 and for a weak inversion region (Γ_{wi}) is 1/2. The input-referred thermal noise of an ideal differential pair operating in subthreshold region, both without and with current-reuse technique,

can be derived in (3-19) and (3-20), respectively.

$$\overline{v_{ni,w/o,cr}^2} = 2 \times \frac{\overline{i_n^2}}{g_m^2} \quad (3-19)$$

$$\overline{v_{ni,w/i,cr}^2} = 2 \times \frac{2 \cdot \overline{i_n^2}}{(2 \cdot g_m)^2} = \frac{\overline{i_n^2}}{g_m^2} \quad (3-20)$$

Hence, considering only the thermal noise, the input-referred noise power of the amplifier with the current-reuse technique can be reduced by half as compared to a circuit without such technique.

To design the neural amplifier, a fully differential current-reuse operational transconductance amplifier (OTA) is deployed to attain an optimized power-noise trade-off and hence a low NEF. The schematic of the proposed OTA is given in Figure 3-9. It is a two-stage fully differential voltage amplifier. In each stage, there is an independent common-mode feedback (CMFB) circuit to stabilize the dc voltage.

The large open-loop gain helps to enhance the gain accuracy of the closed-loop amplifier. The current-reuse technique is employed at the input stage to improve the current efficiency so as to attain maximum gm/I_d as well as having low noise. The four input transistors are biased in the weak inversion region to ensure low thermal noise. Meanwhile, large gate areas ($300\mu\text{m}/2\mu\text{m}$ for NMOS transistors and $200\mu\text{m}/1\mu\text{m}$ for PMOS transistors) are chosen to suppress the flicker noise. Transistor N3 and N4 provide CMFB for the input stage. At the output stage, the PMOS transistors are chosen as the amplification element as they contribute less flicker noise as compared to the NMOS transistors. A resistive sensing CMFB is used to define the output dc level. The two diode-connected MOS transistors

present large resistance in the CMFB circuit, not only to limit the current consumption by the output stage but also to maintain a sufficiently high gain at the output stage.

Figure 3-9. Schematic for OTA used in improved neural amplifier.

The input-referred thermal noise analysis of the proposed OTA results in the following expression:

$$\overline{v_{n,thermal}^2} \approx 2 \times \left\{ \frac{4kTn}{(g_{mn1} + g_{mp1})} \left[\Gamma_{wi} + \frac{\Gamma_{si} g_{mn3} + \Gamma_{wi} g_{mp3}}{g_{mn1} + g_{mp1}} \right] \right\} \Delta f \quad (3-21)$$

where Δf is the bandwidth. g_{mni} indicates the g_m of NMOS transistor Ni , while g_{mpi} is the g_m of PMOS transistor Pi . Note that the g_m 's of the paired transistors (e.g. g_{mn1} and g_{mn2}) are all the same. By biasing transistors N1-6 and P1-4 in such a way whereby g_{mn1} and g_{mp1} are much larger than other g_m 's, the noise contributions from N3-6 and P3-4 are minimized. Hence, 80 percent of total

amplifier current is allocated to the input stage. Transistors N5-6 are biased in strong inversion with small W/L ratio while transistors N1-2 and P1-2 are biased in weak inversion to yield maximum g_m 's so as to generate low thermal noise. The current-reuse technique doubles the input stage gain under the same current consumption and reduces the input-referred noise by $1/\sqrt{2}$, effectively.

The neural amplifier has its high-pass corner at a ultra-low frequency—by implementing a large time constant in its dc feedback path, which results in a long settling time at startup. To mitigate this issue, reset switches are added to set the OTA input nodes to half V_{dd} during the amplifier startup. This allows the OTA input nodes to charge to its desired dc level in a very short time and hence speed up the settling process considerably. For multi-channel recording, it may not be necessary to activate all the recording channels at the same time. In order to conserve the system power, sleep mode is implemented in the neural amplifier. In this mode, the quiescent current of the neural amplifier is reduced to 160 nA by adjusting the bias current. The non-zero sleep-mode current will maintain the dc bias at each node of the amplifier near the normal operation voltage and ascertain fast recovery when the amplifier is awakened from the sleep mode.

Monte Carlo simulation was performed on proposed designs to ensure that the chip works as expected. The result of the Monte Carlo simulation of the AC response of Design A for 100 samples with process and mismatch variations is given in Figure 3-10. The effect from process variation and mismatch has been minimized by drawing common-centroid layout, not using minimum size devices and keeping enough headroom for transistors.

Figure 3-10. Monte Carlo simulation result of Design A.

Table 3-4. Pseudo resistor size selection for this project

Pseudo Resistor size ($\mu\text{m}/\mu\text{m}$)	PR device	Measured Lower cutoff (Hz)
4/1	3.3V	0.375
1/1	1.8V	9.6
2/2	1.8V	6.9
4/0.3	3.3V	1.18
4/4	3.3V	0.2188
10/1	3.3V	0.5
10/0.18	1.8V	331
40/0.18	1.8V	628

The low current (200nA) of the current mirror and use of pseudo resistors usually cause the circuits to be sensitive to process variations. A 5-bit control bit is used in the current reference circuit (the standard PTAT circuit in textbook with current steering) to tune the bias current to the exact value. Moreover, eight pseudo resistors of difference sizes had been fabricated in this project for better selection of use in the neural amplifier, as shown in Table 3-4. The high pass

corner is therefore affected accordingly (4/1 is chosen for all the designs in this thesis).

3.3.4 Measurement Results and Discussion

The full recording channel consists of a neural amplifier, a programmable bandwidth band-pass filter (BPF) with a gain of ten, and a unity gain buffer to drive the subsequent ADC. The overall system was fabricated using standard 0.18- μm CMOS technology without using any off-chip component. The neural amplifier operates with a 1-V supply, from which it draws 800 nA when the low-pass cutoff frequency is set at 5 kHz for AP (or AP + LPF) recording and 160 nA when the low-pass cutoff frequency is set at 400 Hz for LFP recording. The neural amplifier consumes an area of $100\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$ and about 2/3 of the area is occupied by the input capacitors. Figure 3-11 shows the chip micrograph of the full neural recording channel.

Figure 3-11. Micrograph of proposed neural recording channel.

Test Bench Measurement

The measured frequency responses of the full recording channel are plotted in Figure 3-12 for different gain and Figure 3-13 and Figure 3-14 for different cutoff

frequency settings. The gain can be set at either 54.6 dB or 60.6 dB by changing the capacitance value in the feedback path of the neural amplifier, as shown in Figure 3-12.

The system bandwidth is from 0.2 Hz to 5.8 kHz if both AP and LFP need to be recorded. The high-pass cutoff frequency can be configured at 800 Hz to filter out the LFP as depicted in Figure 3-13, and the low-pass cutoff frequency can be configured at 430 Hz to remove the AP as demonstrated in Figure 3-14. Therefore, both AP and the LFP can be captured separately or simultaneously through choosing different configurations.

Figure 3-12. Frequency responses of the neural recording channel with programmable gain through capacitance variation.

Figure 3-13. Frequency response of proposed neural recording channel demonstrating programmable high-pass corner.

Figure 3-14. Frequency responses of proposed neural recording channel demonstrating programmable low-pass corner.

Figure 3-15 depicts the input-referred noise power spectrum density of the overall neural recording channel. The noise floor measured at 1 kHz is 43

nV/ $\sqrt{\text{Hz}}$. The integrated input-referred noise is 4.9 μV_{rms} , calculated by measuring the noise spectrum at the buffer output and dividing it by the recording gain, followed by integrating from 1 Hz to 20 kHz. On the other hand, the output noise spectrum is captured when the current consumption of the neural amplifier is 800 nA and the recording channel is in its full-bandwidth operation. The calculated NEF is 2.2. The NEF of the standalone neural amplifier will be even lower than this value if the noise from both the BPF and buffer are excluded.

Figure 3-15. Input-referred noise spectrum of a full neural recording channel.

Table 3-5 is a summary of performance of the full neural recording channel, with comparison to other state-of-the-art designs. All the numbers listed in Table 3-5 are obtained from the output of the unity gain buffer unless specified otherwise. As can be seen, this work achieves comparable performance to other designs with the lowest power consumption, and therefore the lowest NEF and $\text{NEF}^2 \cdot V_{DD}$ [31]. Hence, the high power efficiency and excellent noise-power trade-off of the

proposed neural amplifier are successfully demonstrated.

Table 3-5. Summary of performance and comparison with other works

Type	[3]	[31]	[18]	This work
Technology	0.5 μm	65 nm	0.35 μm	0.18 μm
Supply voltage (V)	3.3	0.5	3	1
Neural amplifier current (μA)	12.8	-	1.4	0.8 / 0.16 (sleep)
Neural amplifier gain (dB)	40	-	34	34/40
High-pass cutoff frequency (Hz)	300	0/300	1	0.38
Low-pass cutoff frequency (Hz)	5 k	300/10k	5 k	5.8 k
Input-referred noise (μV_{rms})	5.1	4.9	7	4.9
NEF	9.8 [13]	5.99	4.6	2.2
$\text{NEF}^2 \cdot V_{DD}$	316.9 [13]	17.99	63.48	4.84
PSRR (dB)	-	> 65	-	> 70
CMRR (dB)	-	> 56	-	> 60
THD@output	-	-	-	$\leq 1\%$ @ 0.89 V_{pp}

In vivo Biopotential Measurement

To further verify the functionality of the fabricated neural amplifier, *in vivo* neural recording has been carried out on an anesthetized rat. Glass electrodes made in the laboratory were used and the captured neural signals are presented in Figure 3-16. Field evoked potential recording was carried out and it shows the sample recordings from the medial perforant path-dentate gyrus monosynaptic pathway [55]. The recording channel is configured with a 60-dB gain and set to the full-bandwidth mode.

Figure 3-16. In vivo neural recording from an anesthetized rat: (a) long time trace, (b) short time trace.

A low-noise, sub-W neural recording amplifier with a superb NEF is therefore presented. The high power efficiency is realized through weak inversion operation and the adoption of current-reuse technique at the input stage of the

neural amplifier. The amplifier consumes 800 nA current from a 1-V power supply and occupies an area of 0.05 mm². The measured thermal noise is 43 nV/ $\sqrt{\text{Hz}}$ at 1 kHz and the input-referred noise is 4.9 μV_{rms} when integrated from 1 Hz to 20 kHz. It achieves an NEF of 2.2, one of the smallest values amongst the state-of-the-art designs. Neural signals from an anesthetized rat are successfully acquired using the developed prototype. The ultra-low power consumption and small area make it especially suitable for fully implantable multi-channel neural recording systems.

3.4 Design B: Open-loop Neural Amplifier Design

An important drawback of the current neural recording systems is their dependence on the electrode impedances, which can increase with implantation time, causing signal attenuation. The associated drawbacks increase the running costs and significantly hamper their use in consumer healthcare and lifestyle applications. A viable solution is to facilitate the neural recording amplifier to record neural signals even in the case of chronic implantable neural recordings, i.e. an amplifier with high input impedance, low noise and good electrode offset rejection is co-integrated. Previous closed-loop feedback amplifiers have their input impedance limited by the gain capacitors. To increase the input impedance, the gain has to reduce to accommodate the high impedance. Thus, there is trade-off between the gain and the input impedance of the amplifier. However, both large gain and large input impedance are desirable for neural recording amplifiers.

Open-loop operation is a possible way to resolve this problem. For open-loop

amplifiers, the input impedance is no longer limited by the feedback capacitors but the gate of the input transistors. The input impedance can therefore be greatly enhanced. An improved pseudo open-loop amplifier for neural interface systems was proposed based on Sun-II Chang's design in 2009 [12]—the structure of the amplifier is presented in Figure 3-18 and the detailed schematic is provided in Figure 3-19.

3.4.1 Open-loop Neural Amplifier Circuit Design

In this thesis, a low-power open-loop neural amplifier followed by an on-chip configurable band-pass filter (BPF) with small area occupation is successfully demonstrated. The proposed neural amplifier employs an open-loop structure and the current-reuse technique, with subthreshold operation to achieve an optimal trade-off between its noise performance and power consumption. The programmable gain is realized through switching on and off a gain stage. The power-supply rejection (PSRR) of the amplifier is on the other hand taken care of by employing a fully differential structure.

Figure 3-17. Structure of neural recording channel.

The architecture of a single neural recording channel is depicted in Figure 3-17. To reserve the temporal correlation of the neural signals among adjacent channels, every electrode connects to its own independent neural amplifier, followed by a dedicate BPF and a buffer.

A low-noise fully differential amplifier comprises the first stage of the channel. The dc offset voltage resulted from the electrochemical reactions on the electrode-tissue interface is more than tens of millivolt which is much higher compared to the amplitude of the neural signal. The neural signal from the electrode is capacitively coupled to the neural amplifier, rejecting the dc offset voltage and hence avoids the saturation. The amplification is performed through an open-loop configuration.

To further enhance the gain of each recording channel, the BPF with 10× gain is implemented via the capacitively-coupled input. The programmable bandwidth

is realized by changing the resistance value of the feedback resistor. The bandwidth control is placed at the second stage because the first-stage amplifier consumes large current to minimize the noise floor and hence a large compensation capacitor is required to limit its bandwidth to around 5 kHz, which is the desired bandwidth for neural signal recording. By placing the BPF at the second stage which consumes nano-ampere level current, chip area can be saved by using small capacitors. Since the input-referred noise generated by the second stage is divided by the gain of the first stage, the second stage contributes much less noise to the output as compared to the first-stage neural amplifier, the power consumption of the BPF is reduced, which does not affect much on the noise performance of the system. It is usually necessary to convert the captured neural signal to a digital format for further signal processing where an ADC is needed after the analog recording channel. The third stage is a unity-gain buffer to drive the sample and hold circuit of the subsequent ADC.

The design of the neural amplifier is particularly important as it determines the overall noise performance of the recording channel. The proposed amplifier consists of two amplification stages, as shown in Figure 3-18. With a 0.9-V power supply, it can consume a maximum current of 1.2 μA . Under normal operating condition, the first stage of the neural amplifier provides a gain of 50 with 1- μA current to ensure a low enough noise level. The second stage consumes 200 nA of current to achieve a gain of 2. The reference current of the neural amplifier are generated by an on-chip bandgap reference circuit [56]. The current drawn by the biasing circuit has not been included in the calculations of power consumption because many OTAs can share one generated reference current. The 1/f noise and thermal noise of the neural amplifier are suppressed by making the

input transistors larger and operating them in the weak inversion region. It is worth noting that for a given bias current, the g_m of the transistor operating in weak inversion is almost five times larger than that of the strong inversion transistor [57].

Based on the electrode characteristics discussed in [14], the electrode is noted to contain both resistive and capacitive components. The undesirable dc offset at the electrode-tissue interface will appear directly at the amplifier input through the electrode. Therefore, to remove the dc offset voltage, a capacitor is inserted at the input of the neural amplifier. Since the input capacitors have a sole purpose of blocking the dc voltage, the capacitance values can be made small to save on chip area. The proposed amplifier with its improved input impedance is particularly suitable for neural electrodes with large impedance.

The programmable gain is implemented in the neural amplifier in order to fulfill the high dynamic range requirement, to accommodate both LFP and AP. The gain is configured to 50 through bypassing the second stage of the neural amplifier. The output of the neural amplifier needs to be disconnected from the second-stage output node and tied to the first-stage output so that the first stage can maintain a gain of 50. Meanwhile, the second stage of the neural amplifier is turned off to save power.

Figure 3-18. Structure of proposed pseudo open-loop neural recording amplifier.

3.4.1.1 OTA Design

The open-loop amplifier overcomes disadvantages of closed-loop amplifier while providing good power efficiency, as reported in [12]. The reported amplifier makes use of the g_m ratio to realise the enhanced gain but a large portion of the current is wasted by directly drawing it to current sink, which is highly undesirable for implantable devices due to the tight power budget. Thus, to fully utilize the current, the proposed neural amplifier employs additional NMOS transistors as the gain element before drawing the current to the current sink. The schematic of the first-stage OTA is given in Figure 3-19. The gain of the first stage of the neural amplifier is obtained through summing the gains contributed by both the PMOS and NMOS input transistors. To offer high linearity without scarifying the performance, the load transistors are diode-connected and operate in subthreshold region. The transistor transconductance in weak inversion can be approximated to be linear with its drain current, as expressed below [58],

$$\frac{g_m}{I_D} \approx \frac{\kappa}{U_T} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot IC}} \approx \frac{2\kappa}{U_T} \quad (3-22)$$

where κ is the subthreshold slope factor of approximately 0.7, U_T is the thermal voltage, and I_D is the drain current. The output impedance can be approximated as

$$R_{out} = \frac{1}{g_{m3}} \times 2 = \frac{2U_T}{\kappa I_{D3}} \quad (3-23)$$

Thus, the ideal gain of the first stage of the neural amplifier is determined by the current ratios,

$$A_v = (g_{m1} + g_{m2}) \frac{2}{g_{m3}} \quad (3-24)$$

$$A_v = \frac{2(I_{D1} + I_{D2})}{I_{D3}} = \frac{2(I_{D1} + I_{D2})}{I_{D1} - I_{D2}} \quad (3-25)$$

where I_{D1} , I_{D2} , I_{D3} , g_{m1} , g_{m2} , and g_{m3} are the drain currents and transconductances of transistors M1, M2, M3, respectively. A gain of 50 can be obtained by carefully adjusting the aspect ratio W/L of the transistors in the current mirror circuit, to enable I_{D2} to be 92 percent of I_{D1} (500nA). Since the gain is current dependent only, the proposed open-loop neural amplifier has the advantage of high linearity and immunity to both the process and bias variations.

The two PMOS transistors, M3 and M4 that are connected in series operate in the weak inversion region, to serve as an active load resistor. The output dc voltage is provided by $V_{sg3} + V_{sg4}$. By resizing the W/L of M3 and M4, the output dc voltage can be set to half V_{dd} for maximum output swing.

A high-resistance pseudo resistor is employed to provide dc feedback at the amplifier input. Undesirable nonlinear distortion may arise due to changes in the

feedback resistance when there is large output voltage swing. This undesired phenomenon is suppressed by designing the pseudo resistor in a balanced way. Thus, with the dc bias voltage variation across the pseudo resistor, the worst-case nonlinearity is improved due to minimum disparity on the resistance values.

The second stage of the neural amplifier, as shown in Figure 3-20, is designed in a similar way except for the following changes. The input is dc coupled and its common mode voltage is defined at half V_{dd} by the output voltage level of the first stage. The current ratios and load transistors are adjusted to provide a gain of 2. The bulk of transistor M5 is tied to V_{dd} to provide a large threshold voltage. This allows the V_{sg} of M5 to be adjusted to half V_{dd} , which is the output dc voltage to attain the maximum output swing.

Figure 3-19. Schematic of proposed pseudo open-loop amplifier, 1st stage.

Figure 3-20. Schematic of proposed pseudo open-loop amplifier, 2nd stage.

Figure 3-21. Monte Carlo simulation of Design B.

The Monte Carlo simulation result of AC response for Design B is depicted in Figure 3-21. Compared to Design A in Figure 3-10, the variation of gain and cutoff frequencies is larger but is still within the acceptable range.

3.4.1.2 Noise Performance

To minimize circuit noise, the proposed amplifier is designed with minimum current branches so as to ensure little noise generation in signal path. Also to achieve the low-noise performance with diminutive power consumption, the transistor biasing conditions are also important. In this design, the input transistor pairs are implemented to operate in weak inversion region for an optimized current efficiency. Besides, the current reuse scheme is employed to further boost the current efficiency to a maximum so as to achieve the lowest NEF.

In this design, both M1 and M2 are stacked as input transistors in the same current branch to generate multiple transconductances from a single current branch. The resulting multiple transconductances are combined to provide a larger effective transconductance with the same amount of current consumed, when compared with a single device in a single branch. A lower input-referred noise can be achieved by obtaining a larger transconductance.

The thermal noise of the input-referred noise power of the neural amplifier can be expressed as

$$\overline{V_{n,thermal}^2} = \frac{C_1 + C_{gd1} + C_{gd2} + C_{gs1} + C_{gs2}}{C_1} \cdot 2 \left[\frac{4kT}{g_{m1} + g_{m2}} \gamma \left(1 + \frac{g_{m3} + g_{m4}}{g_{m1} + g_{m2}} \right) \right] \Delta f \quad (3-26)$$

where γ is 1/2 for a weak strong inversion region. The thermal noise from other transistors is negligible. The noise contributions of M3 and M4 can be minimized by appropriately biasing them with a tiny amount of current so that both g_{m3} and g_{m4} can be negligible as compared to g_{m1} and g_{m2} . C_1 is 20 pF which is

significantly larger than other capacitances. Hence, the first factor of the equation is nearly 1.

The flicker noise of the transistors is calculated through employing a noise generator of $[K/(C_{ox}WL)](1/f)$ at the gate. The total input-referred flicker noise of the neural amplifier is approximated using the following equation.

$$\overline{V_{n,1/f}^2} = \frac{C_1 + C_{gd1} + C_{gd2} + C_{gs1} + C_{gs2}}{C_1} \cdot \frac{2 \left[\frac{K_P g_{m1}^2}{C_{ox} W_1 L_1} + \frac{K_N g_{m2}^2}{C_{ox} W_2 L_2} + \frac{K_P g_{m3}^2}{C_{ox} W_3 L_3} \right]}{(g_{m1} + g_{m2})^2} \frac{\Delta f}{f} \quad (3-27)$$

The noise contributions from load transistors M3 and M4 are scaled down by a small factor of $[g_{m3}/(g_{m1} + g_{m2})]^2$, making it insignificant as compared to those generated by M1 and M2. The input transistor pairs designed to work in weak inversion possess large aspect ratio while exhibiting less flicker noise. The flicker noise coefficient K_P of PMOS transistors is larger than that K_N of NMOS transistors [31]. Thus, Transistor M2 is designed to have a channel length slightly larger than M1, to remain operating in weak inversion, so as to promote further reduction in the flicker noise without sacrificing its transconductance. The addition of the two noise sources in (3-26) and (3-27) comprises the total input-referred noise. From the simulation results, the thermal noise is noted to contribute more than 80 percent of the total noise in the proposed neural amplifier design.

3.4.1.3 Sleep mode

For multi-channel recording, it may not be necessary to activate all the recording channels at the same time. To preserve power consumption of the neural recording system, sleep mode is implemented in each neural amplifier. The neural amplifier in this design is not to completely switch off during sleep mode since its startup time is large due to the sub-hertz low cutoff frequency. In sleep mode, the second stage is turned off, and the output of the neural amplifier is tied to the first-stage output. The first stage of the neural amplifier consumes a very small current of 200 nA. The non-zero sleep-mode current will maintain the dc bias at each high-impedance node of the amplifier near the normal operating voltage and ascertain fast recovery when the neural amplifier is awakened from the sleep mode.

3.4.2 Measurement Results and Discussion

The full neural recording channel consisting of a programmable gain neural amplifier, a programmable bandwidth BPF with a gain of ten, and a unity gain buffer, was fabricated in the Global Foundry 0.18- μm standard CMOS process without any off-chip component. The neural amplifier circuit occupies $100\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$ of silicon area, and about 67 percent of the area is occupied by the dc blocking capacitors. The chip micrograph of one neural recording channel is shown in Figure 3-22. The neural amplifier operates under a 0.9-V supply, from which it draws 1.2 μA for the 60-dB gain configuration and 1 μA for the 54-dB gain configuration. The measured common mode rejection ratio (CMRR) over the signal bandwidth is 42 dB, while the PSRR is about 43 dB.

Figure 3-22. Micrograph of proposed neural recording amplifier.

Benchtop Characterization

The measured frequency responses of the full recording channel at different gain and bandwidth settings are plotted in Figure 3-23, Figure 3-24 and Figure 3-25. The mid-band gain can be set at either 57 dB or 52 dB by turning on or off the second stage of the neural amplifier, as illustrated in Figure 3-23. The slight reduction in the gain is caused by the parasitic capacitance of the input transistors.

The channel bandwidth varies from 0.15 Hz to 5.8 kHz if both AP and LFP need to be recorded. The low-pass cutoff frequency can be configured at 440 Hz to remove the AP, as demonstrated in Figure 3-24; and the high-pass cutoff frequency can be configured at 600 Hz to filter out the LFP as depicted in Figure 3-25. Therefore, both AP and the LFP can be recorded separately or simultaneously via choosing different bandwidth configurations.

Noise measurements for the neural recording channel were performed by recording data from the buffer output using dynamic signal analyzer and processing the data using MATLAB. Figure 3-26 describes the input-referred noise spectrum of the neural recording channel when the neural recording channel has a gain of 52 dB, with a bandwidth of 5.8 kHz. It shows a thermal noise level of 36 nV/ $\sqrt{\text{Hz}}$ at 1 kHz and a flicker noise corner frequency of

approximately 100 Hz.

Figure 3-23. Frequency responses of the neural recording channel with programmable gain.

Figure 3-24. Frequency responses of the neural recording channel with programmable low-pass corner.

Figure 3-25. Frequency response of the neural recording channel with programmable high-pass corner.

Figure 3-26. Input-referred noise spectrum of a full neural recording channel.

The input-referred noise is $5.1 \mu\text{V}_{\text{rms}}$, which is obtained by integrating the noise

spectral density starting from 1 Hz to 20 kHz, for the amplifier bandwidth of 5.8 kHz. The NEF of the proposed neural recording channel is 2.8 under the above conditions, which is low enough as compared with NEF values reported in the literature.

Table 3-6 summarizes the measurement results on the performance of the neural recording channel and the comparison with other recent state-of-the-art works from industrial and academic researchers [9] [18] [31] [46]. All the values listed in were obtained from the output of the unity gain buffer unless otherwise specified. The input-referred noise of the proposed design is not only comparable to other neural amplifier designs but of least power consumption, leading to the lowest NEF among the designs. The improvement of the NEF is attributed to the several design choices. The current reuse technique with weak inversion transistors provides a better trade-off between noise and power. This leads to low input-referred noise with a small current consumption. In addition, a power efficiency factor (PEF), where $PEF = NEF^2 \cdot V_{dd}$ is introduced in [31] to evaluate the performance of each design. When PEF is used as the metric for comparison, the proposed design is still the most energy-efficient work among the recent state-of-the-art designs.

Table 3-6. Summary of performance and comparison with other works

	[9] JSSC 2003	[12]EMBC 2009	[18] JSSC 2009	[31] JSSC 2012	This work
Technology	1.5 μm	0.25 μm	0.35 μm	65 nm	0.18 μm
Supply voltage (V)	± 2.5	2.5	3	0.5	0.9
Supply current (μA)	16	0.4	1.4	10 (including ADC, BPF)	1.2 (57 dB) 1 (52 dB) 0.2 (sleep)
Neural amplifier Gain (dB)	40	39.95	34	-	32/37
High-pass cutoff frequency (Hz)	0.13	0.51	1	-	0.15
Low-pass cutoff frequency (Hz)	7.5 k	292	5 k	10 k	5.8 k
Input-referred noise (μV_{rms})	2.1	1.69	7	4.9	5.1
NEF	3.8	2.43	4.6	4.3	2.8
$\text{NEF}^2 \cdot V_{dd}$	72.2	15.18	63.48	17.96	7.1
PSRR (dB)	42	82	-	64	42
CMRR (dB)	42	79	-	75	43
THD@output	1% @ 1.58 V_{pp}	$\leq 1\%$ @ 0.225 V_{pp}	-		1.05% @ 0.77 V_{pp}
Area of neural amplifier (mm^2)	0.16	0.043	0.02	0.013	0.05

In vivo Measurement

The system was further verified through *in vivo* measurement. A glass electrode made in laboratory (at the National University of Singapore Hospital) was inserted in the somatosensory cortex of an anesthetized rat's brain and connected with the neural recording interface circuit on the chip. Field evoked potential recording was carried out and it shows the sample recordings from the medial

perforant path-dentate gyrus monosynaptic pathway [55]. The amplifier input is connected to the electrode, with the reference and ground nodes connecting to the skin of the rat.

The waveform of the neural spikes recorded from the anesthetized rat within a 2.4-second period under the configuration of 52 dB gain and 5 kHz bandwidth is shown in Figure 3-27 (a). A zoom-in version of a single neural spike is also included in Figure 3-27 (b).

In this section, we have presented a 1.08- μ W neural amplifier, which has an input-referred noise of 4 μ V_{rms} over a bandwidth of 12 kHz. The neural amplifier removes the dc offsets produced at the electrode-tissue interface, and amplifies neural signals from the sub-hertz range to about 5.8 kHz. Because of the high g_m/I_d generated from transistors operating in weak inversion region and the boosted g_m from the current reuse technique, an optimum power-noise trade-off among the reported neural amplifiers is obtained. The proposed neural amplifier consumes only 1.08 μ W of power and occupies 0.05-mm² silicon area in a 0.18- μ m process, providing the possibility for even larger scale and higher density implantable neural recording systems.

Figure 3-27. Neural spike observed in rat's brain: (a) a 2.4-second recorded neural signal waveform and (b) a 12-ms recorded neural signal waveform.

Both benchtop characterization and *in vivo* testing was carried out on the fabricated design. The measurement results were analogous to the state-of-the-

art designs, with significantly lower power consumption and smaller chip size. The proposed neural recording interface IC is capable of simultaneous monitoring across a broad variety of neural signal modalities, from LFPs to APs. Besides, the fabricated chip is capable of *in vivo* neural signal acquisition, with excellent power-noise trade-off, and occupies an acceptable area. The data collected is of great importance for understanding the mechanisms underlying brain function, as well as for the information processing and propagation throughout the brain. The low-power consumption, small chip area and low circuit noise with programmable gain and bandwidth make the proposed neural recording channel suitable for large-scale high-density neural recording system, whereby it increases the system performance, robustness and the ability to deliver artificial sensation. The design therefore offers vast potential in accelerating the neural prosthesis design and development.

3.5 Circuit Integration

The 100-channel neural recording interface IC was fabricated using standard 0.18- μm CMOS process and the die micrograph is shown in Figure 3-28. The dimension of the fabricated IC, including pads, is 4.7 mm by 6.0 mm.

Figure 3-29 shows the overall system architecture of the 100-channel neural interface IC. There are ten neural recording blocks for conditioning and digitizing the captured neural signals. Each recording block contains ten analog recording channels (Design A is used in this system). After being multiplexed by a time-domain multiplexer, the conditioned analog signals are digitized by its

subsequent 9-bit SAR ADC. The system is tested under 1 V for the analog channels and ADC, and 1.8 V for the digital control module. The measurement results of the overall neural interface IC are described in detail in Table 3-7.

Figure 3-28. Micrograph of a 100-channel neural recording chip.

Figure 3-29. System architecture of the neural interface IC.

Table 3-7. Measured performance summary and comparison of the proposed neural interface IC with state-of-the-art designs.

	Harris on [3]	Chae [27]	Lee [59]	Rabae y [31]	Walker [60]	Chang [61]	This work
Supply voltage (V)	3.3	± 1.65	± 1.5	0.5	1.2	0.5 / 1	1 / 1.8
Process	0.5 μm	0.35 μm	0.5 μm	65 nm	0.13 μm	0.25 μm	0.18 μm
System gain (dB)	60	57 – 60	67.8 / 78	--	40 / 55	37.5 – 57.5	54.8 / 60.9
High-pass cutoff (Hz)	30 – 1k	0.1 – 200	0.1 – 1k	DC / 300	0.3	0.5 (tunable)	0.38 / 248
Low-pass cutoff (Hz)	5k	2k – 20k	8k	300 / 10k	10k	18k (tunable)	432 / 5.1k
Noise (μV)	5.1	4.9	4.32	4.9	2.2	4.26 / 5.62	4.9 (whole chain)
NEF	--	--	--	5.99	5	5.2 / 1.69*	2.2 (whole chain)
NEF ² VDD	--	--	--	17.96	30	27 / 2.86*	4.84 (whole chain)
THD	--	--	--	--	--	--	1% @ 0.9-V output
CMRR (dB)	--	90	134	75	--	35	> 60
PSRR (dB)	--	80	62.7	64	--	48	> 70
Sampling rate (kS/s)	15	640	58 – 709	20	31.25	31.25	24.5 – 245
SNDR (dB)	--	--	--	--	60.3	45.14	51.5
No. of bits	10	6 – 9	--	8	10	--	9.5
ENOB	--	--	8.3	7.15	--	7.2	8.3
INL/DNL	0.6 / 0.6	--	--	--	--	0.75 / 0.5	1.2 / 0.55
No. of channels	100	128	32	1	96	16	100
Total power (mW)	4.3 (one ADC)	3	1.2 (without ADC)	0.005	6.5	0.2	1.16 (including loss in power management)
Chip area (mm ²)	27.7 (one ADC)	51.8	16.2	0.013	25	2.88	28.2

**Data shown are for preamplifier only, while the rest of the data in the proposed design are for the whole analog recording chain.*

Chapter 4. DESIGN OF NEURAL AMPLIFIER WITH HIGH INPUT IMPEDANCE

Design A and Design B have achieved good performances in terms of noise and power. However, an important problem still exists, that is their performance depends largely on the electrode impedance. A voltage divider is formed between the electrode impedance and the amplifier input impedance, which then attenuates the input signal. Because of the continuously rising density of the multi-electrode arrays and the use of smaller electrodes [62], the surface area of each electrode tends to reduce and that contributes to larger electrode impedance [19]. Moreover, during chronically neural recording, tissue encapsulation occurs with time, creating high impedance around the electrode, leading to the insulation of the electrode in around hundred days [63]. All the above mentioned electrode behaviors degrade the performance of the neural recording amplifier, especially for those with low input impedance.

On top of the above, the electrode impedance mismatch can be up to 50 percent due to process variation [19]. The electrode impedance mismatch can in turn lead to the conversion of the common mode interference at the electrode to differential mode interference and hence saturates the neural amplifier. This is particularly significant in a high density recording system, in which each channel has its own signal electrode but only one reference electrode is deployed for the whole system. The reference electrode usually has a size which is much larger than that of a signal electrode. Therefore, because of the variation of the signal electrode and reference electrode, the common mode noise signal (such as electromagnetic (EM) or power line interference) appeared at the neural amplifier inputs

is transformed into differential signals since the different electrodes have different amount of attenuation. A possible solution to those issues is to design the neural recording amplifier with high input impedance without scarifying its noise performance and good electrode offset rejection.

4.1 Design C: Design of an Open-Loop Neural Amplifier with Improved Input Impedance

4.1.1 Circuit Design and Implementation

In Design B, the input impedance is limited by the gate-drain capacitance C_{gd} of the input transistors. The parasitic capacitance of the input stage of the amplifier together with the input dc blocking capacitor forms a closed loop feedback, which limits the gain of the amplifier. Eliminating C_{gd} and reducing the input capacitor is a possible way to improve the input impedance without scarifying the gain of the neural amplifier. Therefore, cross coupling capacitors are employed, as shown in Figure 4-1, to create a bridge connection between the gate and drain of the input transistors, which can effectively reduce the effect of the gate-drain parasitic capacitance [64]. By reducing the gate-drain parasitic capacitance, the input capacitance C_1' can be reduced without any degradation of the total gain of the first-stage amplifier. The block diagram of the open-loop neural amplifier with improved input impedance is given in Figure 4-2. If the feedback capacitors C_{fb1} and C_{fb2} are adjusted to be identical to the gate-drain parasitic capacitance ($C_{gd1}+C_{gd2}$), the charging and discharging current of the gate-drain capacitance ($C_{gd1}+C_{gd2}$) can be completely supplied by the bridge

connection via the feedback capacitors C_{fb1} . Thus, the effect from the gate-drain parasitic capacitance of the input transistors can be totally removed.

$$(V_{out1+} - V_{in+})sC_{fb1} = (V_{in+} - V_{out1-}) \cdot s(C_{gd1} + C_{gd2}) \quad (4-1)$$

$$C_{fb1} = \left(\frac{A_{CL} + 1}{A_{CL} - 1} \right) \cdot (C_{gd1} + C_{gd2}) \approx C_{gd1} + C_{gd2} \quad (4-2)$$

where the open-loop gain of the OTA A_{CL} is set to 100. Conversely, complete parasitic capacitance cancellation is difficult to achieve because of the process variation and mismatch in fabrication process. Therefore, $C_{fb1,2}$ is implemented using a tunable capacitor bank.

Due to the cross coupled capacitor effect, the load of the first stage of the neural amplifier is increased because of the addition feedback current, and therefore the bandwidth of the first stage is slightly reduced. To maintain the bandwidth of the neural recording channel, the bandwidth of BPF is considerably relaxed to allow the 3-dB cutoff frequency to be the same of the previous designs, i.e. Design A and Design B described in Section 3.3 and Section 3.4.

The input-referred noise of the neural amplifier can be estimated using the following equation:

$$\overline{v_{ni,amp,C}^2} \approx \frac{C_1 + C_{gd1} + C_{gd2} + C_{gs1} + C_{gs2}}{C_1} \cdot \overline{v_{n,thermal,B}^2} \quad (4-3)$$

Since the input capacitor C_1 has the value of 3.3 pF, which is comparable to $C_{gs1,2}$ and $C_{gd1,2}$, the noise of the neural amplifier increases by about 50 percent as compared to the open-loop amplifier without the cross coupled compensation capacitors, while the area of the neural amplifier is reduced by half.

Figure 4-1. Schematic of 1st stage OTA for the open-loop neural amplifier with improved input impedance: Design C.

Figure 4-2. Block diagram of open-loop neural amplifier with improved input impedance: Design C.

4.1.2 Measurement Results

The ac response of Design C is shown in Figure 4-3 and Figure 4-4. The figures were plotted by recording the signals at the output of the buffer. The high-pass corner frequency controls the value of the feedback pseudo-resistors with the feedback capacitors. In Figure 4-3 and Figure 4-4, the high-pass cutoff frequencies locate at about 0.3 Hz. Similar to Design A and Design B in Chapter 3, the high-pass cutoff frequencies can be programmed from about 0.3 Hz to 300 Hz by the following BPF, which is not showed in Figure 4-3. The low-pass cutoff frequencies can be programmed from about 300 Hz to 5 kHz by changing the bandwidth control voltage of the BPF, as described in [65].

Figure 4-3. Frequency responses of the neural recording channel with programmable low-pass corner.

Figure 4-4 shows the gain adjustment of this design. There are two gain levels: 51.8 dB and 56.4 dB. Compare to Design A and Design B, the gain of this neural amplifier is slightly reduced to 56.4 dB; this is due to inaccurate gain control of the open-loop configuration and imperfect parasitic capacitance cancellation. The input capacitor and residual parasitic capacitance of $C_{gd1,2}$ degrades the gain. Moreover, because of the inaccurate gain, the amount of current fed back to the input transistors is hard to determine, which affects the bandwidth of the neural amplifier. As shown in Figure 4-3, the feedback current is slightly smaller than that in simulation to avoid instability, the bandwidth of the whole neural recording channel increases to 7.4 kHz.

Figure 4-4. Frequency responses of the neural recording channel with programmable gain.

The input-referred noise of the neural recording channel is plotted in Figure 4-5.

It clearly shows that for low frequency application, the flicker noise is dominant. The integrated input-referred noise of the neural amplifier from 1 Hz to 20 kHz is $8.5 \mu\text{V}_{\text{rms}}$, when the neural amplifier operates at a gain of 56.4 dB with full bandwidth. This increase in noise is caused by the reduction of input capacitance as explained earlier. As a result, the NEF of this neural amplifier increases to 3.6.

Figure 4-5. Input-referred noise spectrum of a full neural recording channel.

4.2 Design D: Design of a Closed-loop Neural Amplifier with Improved Input Impedance

4.2.1 Circuit Design and Implementation

From the above mentioned three neural amplifier designs, we can see there is

trade-off among noise performance, power consumption and input impedance. To further improve the three parameters, we designed a closed-loop neural amplifier with improved input impedance (Design D), which breaks the tie between input impedance and the other two performance parameters. In this design, the power-efficient low noise neural amplifier Design A is employed with additional current feedback path to the input of the neural amplifier. The current drawn by the neural amplifier at its input is compensated from the feedback path. Therefore, the effective input impedance of the neural amplifier is significantly improved. The current feedback path is implemented using two capacitors C_3 and C_4 , as illustrated in Figure 4-6. To make the feedback current equal to the current drawn by the neural amplifier, the equation is shown below:

$$(A_{CL} \cdot V_{in} - V_{in}) \cdot sC_4 = V_{in} \cdot sC_1 \quad (4-4)$$

$$C_4 = \frac{C_1}{A_{CL} - 1} \quad (4-5)$$

The closed-loop gain of the neural amplifier A_{CL} is designed at 100. We assume the OTA has a sufficient dc gain to make the voltage at the inputs of the OTA ac ground and the parasitic capacitance. The exact equation of (4-5) is difficult to achieve due to process variations, which may cause the circuit to oscillate. In order to have some safety margin (let feedback current always be smaller than the feed forward current), we make $C_4 = C_2 = 200$ fF, the calculations on input impedance of the neural amplifier are shown below.

Without current feedback, the input impedance is

$$Z_{in,w/o_cf} = \frac{V_{in}}{A_{CL}V_{in}sC_2} = \frac{1}{A_{CL}sC_2} \quad (4-6)$$

With current feedback, the input impedance is

$$Z_{in,w_cf} = \frac{V_{in}}{A_{CL}V_{in}sC_2 - (A_{CL}V_{in} - V_{in})sC_4} = \frac{1}{sC_2} = A_{CL} \cdot Z_{in,w/o_cf} \quad (4-7)$$

The input impedance of the neural amplifier with the current feedback can be improved by 100 times. For practical implementation, there is leakage current at the capacitors (C_1 , C_2 and parasitic capacitance), gate leakage current of the OTA, and the leakage current flowing through the pseudo resistors. The parasitic capacitance in parallel with C_1 and C_2 ranges between 10 percent to forty percent of $C_{1,2}$. This will degrade the impedance boosting factor to about 10×. Therefore, more current than the theoretical value should be fed back to the input of the neural amplifier to supply those leakage currents. However, if the current provided from the feedback path is more than the current drawn by the neural amplifier, an undesirable positive feedback loop will form in the circuit. Hence, C_3 and C_4 must be made to a proper value to maximize the input impedance while maintaining the stability of the neural amplifier.

Furthermore, the parasitic capacitance is uncertain and the gain of the neural amplifier is not perfectly constant over the bandwidth, the current feedback capacitors C_3 and C_4 are designed to be tunable so as to best match the feedback current and feed forward current.

Figure 4-6. Schematic of the closed-loop neural amplifier with improved input impedance: Design D

4.2.2 Measurement Results

All the neural recording channels including the neural amplifiers, one band-pass filter and a buffer, are fabricated in a standard 0.18 μm CMOS technology. The BPF and buffer are identical for each recording channels except that the channel for Design C has a larger bandwidth. The micrograph of the chip is shown in Figure 4-7.

Figure 4-7. Chip graph of the fabricated neural recording channels.

The input impedance of Design D is characterized by connecting a small capacitor with the capacitance value comparable to the input impedance of the neural amplifier and measuring the amount of attenuation. Figure 4-8 describes the measured input impedance of the neural amplifier with current feedback as compared to the most typical input impedance (20 pF input capacitance) of the neural amplifier [9] [14] [18] [46] [66] published so far. The parasitic capacitance of the pad (several hundred fF) contributes to the total measured input impedance of the amplifier.

Figure 4-8. Measured input impedance of neural amplifier Design D.

The measured frequency responses of the analog front-end Design D is shown in Figure 4-9 and Figure 4-10. The measured high-pass cutoff of the neural recording channel is about 0.25 Hz. The measured low-pass cutoff frequency of the neural recording channel is 6.2 kHz. This meets the design specification. The programmable gain function is demonstrated in Figure 4-10. The measured dc gain of the neural recording channel is at 58.8 dB over a 3-dB bandwidth of 6.2 kHz. And it can be programmed to 53.5 dB by changing the gain control bit to satisfy the design requirement of the implantable neural recordings.

Figure 4-9. Frequency responses of the neural recording channel with programmable low-pass corner.

Figure 4-10. Frequency responses of the neural recording channel with programmable gain.

To measure the input-referred noise of the front-end neural amplifier, the differential inputs are connected to ground and the output is recorded by Agilent

Dynamic Signal Analyzer 35670A. The integrated input-referred noise of the neural amplifier is $4.5 \mu\text{V}_{\text{rms}}$ from 1 Hz to 20 kHz, and leading to an NEF of 2.2, which is one of the smallest values reported to-date, representing a good trade-off of power and noise for the neural amplifier.

Figure 4-11. Input-referred noise spectrum of a full neural recording channel.

Table 4-1 is a summary of detailed performance of the four full neural recording channels, with comparison to other state-of-the-art designs. All the numbers listed in Table 4-1 are obtained from the output of the unity gain buffer unless specified otherwise. The lowest NEF indicates an optimum trade-off between noise and power of the neural amplifier. Design D achieves comparable performance to other designs, and with the ultra-low power consumption and

large input impedance, leading to one of the lowest NEF and $NEF^2 \cdot V_{DD}$.

Table 4-1. Performance comparison with other state-of-arts.

	Design A	Design B	Design C	Design D	[62]	[67]
Technology (μm)	0.18	0.18	0.18	0.18	0.35	0.13
Supply voltage (V)	1	0.9	0.9	1	3.3	1.2
Amplifier current (μA)	0.8	1.2	1.2	1	23	28.9
Amplifier gain(dB)	34/40	32/37	31.5/36.4	38.8	34	56 (channel)
High-pass cutoff (Hz)	0.2	0.15	0.3	0.25	2.6	280
Low-pass cutoff (Hz)	430/5.8k	5.8 k	9.9k	6.2k	6.2k	10k
Input noise (μVrms)	4.9 (1 to 20 kHz)	5.1 (1 to 20 kHz)	8.5 (1 to 20 kHz)	4.5 (1 to 20 kHz)	2.3-2.9 (1 to 6 kHz)	2.2 (1 to 100 kHz)
NEF	2.2	2.8	3.6	2.2	5.1	4.5
$NEF^2 \cdot V_{DD}$	4.84	7.1	11.7	4.84	85.8	24.3
Input capacitance (pF)	20	20	3.3	≈ 2	25	20
PSRR (dB)	>60	42	44	55	70	-
CMRR (dB)	>70	43	48	67	65	-
Area (mm^2)	0.05	0.05	0.024	0.058	-	-

All the neural amplifiers were fabricated using standard 0.18- μm CMOS process. The open loop neural amplifiers (i.e. Design B and Design C) operate at lower supply voltage than the closed loop amplifiers (i.e. Design A and Design D) because of the additional pair of transistors at the input branch induced by the common mode feedback circuit required for the closed loop amplifiers [68 – 70]. The outputs of the open loop amplifiers are well defined and thus the common

mode feedback loop is not necessary. Due to the low gain of the open loop amplifiers, which is caused by the parasitic feedback loop, two gain stages are employed for the open loop amplifiers and this leads to a higher power consumption. The gain of the open loop amplifiers are generally less than that of the closed loop amplifiers because small current is hard to generate in the open loop amplifiers while the feedback allows for more accurate gain control in the closed loop configuration. Both Design C and Design D offer less gain compared to Design B and Design A because of the gain degradation caused by the additional positive feedback loop. All the high-pass corners are set by the pseudo resistor with feedback capacitors. Therefore, all the four designs have similar high-pass corners. The low-pass corners are configured at the second stage. Except for Design C that has relaxed its bandwidth due to the positive feedback, all other neural amplifiers have similar low-pass corners. The noise performance of the OTAs used in the four designs are very close to each other because of similar power consumption and similar transistor size with similar topology. Therefore, the input-referred noise is mainly affected by the input capacitance when the noise of OTA is referred to the input of the amplifier. The input-referred noise of Design C is significantly larger because of the reduced input capacitor. Other designs have comparable input-referred noise. As a result, Design D is able to deliver a largest input impedance and accurate gain though with a slightly larger area and low noise performance.

In vivo testing

Given the superior performance over other designs, Design D was further verified through *in vivo* measurement. A glass electrode made in laboratory was

implanted in the Medial Prefrontal Cortex (prelimbic area) of an anesthetized rat's brain and externally interfaced with the neural recording channel on the chip for field evoked potential recording. The amplifier input is connected to the electrode, with the reference and ground nodes connecting to the skin of the rat next to the electrode. The waveform of the neural spikes recorded from the anesthetized rat within a 50-second period is shown in Figure 4-12. A zoom-in version of a single neural spike is also included in Figure 4-13. Design D with large input impedance shows high rejection to interferences compared to Design A.

This section describes two neural amplifier designs with the enhancement on input impedance in order to suppress the partial differential noise due to electrode impedance mismatch. The positive capacitive feedback loop using cross couple capacitors is employed to supply the input current. Hence, the effective input impedance of the neural amplifier is increased.

(a)

(b)

Figure 4-12. Long time trace in vivo neural recording from an anesthetized rat: (a) Design A (b) Design D.

(a)

(b)

Figure 4-13. Short time trace in vivo neural recording from an anesthetized rat: (a) Design A (b) Design D.

Chapter 5. DESIGN OF NEURAL RECORDING ACTIVITY BASED ANALOG CHANNEL

In neuroscience research and clinical neuroprosthesis, simultaneous activities of a large population of neurons have to be recorded, transmitted and processed for neural pattern classification and recognition [39], [40]. Conventionally, a complete set of recorded raw data is preserved for data analysis [27]. However, for the recently emerging implantable wireless neural recording microsystem such as that shown in Figure 5-1, compression of large volume of data becomes mandatory, to reduce the effective transmission data rate so as to lower the power consumption of the entire recording implant [41] [71]. This is the key to minimize the required power and size of the data transmitting coils, thereby alleviating the excessive heat dissipation caused by the implanted electronics.

In this chapter, we present a neural recording interface IC with AP detection using a discrete-time finite impulse response (FIR) filter as a delay buffer to perform data compression while ensuring preservation of the AP waveform. The AP detection is carried out in analog domain before data quantization so that the ADCs and their driving buffers can be powered down during the non-AP period. The time delay for preservation of the complete AP waveform is implemented using the FIR filter in discrete-time domain where the time delay is defined by the clock period that is accurate and robust to process variation and mismatch.

Figure 5-1. Typical system architecture of the fully implantable wireless neural recording microsystem.

5.1 System Architecture

Figure 5-2 depicts the block level diagram of the proposed neural recording interface IC which comprises three main building blocks: (1) a low-noise neural amplifier for amplifying the neural signal acquired through the multi-electrode array (MEA) by 100 times; (2) an AP detection circuit that detects the AP and generates triggering signal to enable its subsequent functional blocks such as buffers, ADCs, multiplexers, and circuits in the RF transmitter; and (3) an analog buffer with digital delay implemented using an FIR filter to preserve the complete AP waveform.

Figure 5-2. Block diagram of neural recording interface IC.

5.2 Circuit Implementation

5.2.1 Low-Noise Neural Amplifier

The low-noise neural amplifier uses a similar architecture as Design A. The schematic diagram of the low-noise neural amplifier used in this work is shown in Figure 5-3. The high-pass cutoff frequency of the neural amplifier is set to 300 Hz so that the AP waveform can be recorded without being affected by the LFP signal. A fully differential current-reuse OTA [72] is used to achieve an optimal power-noise trade-off and hence a very low value of noise efficiency factor (NEF).

Figure 5-3. Circuit schematic of the low-noise neural amplifier.

5.2.2 Adaptive AP Detection Circuit

Figure 5-4 shows the block diagram of the AP detection circuit. A differentiator is used to detect the signal trend for earliest spike detection and to remove the dc offset from the neural amplifier. In order to avoid any influence of the offset generated by the differentiator during AP detection, the neural signal is AC-coupled to the AP detection circuit. A pseudo-resistor is used with a capacitor of 500 fF to implement a high-pass cutoff frequency of 100 Hz, resulting in full coverage of the entire AP signal bandwidth. The AC-coupled signal is further processed by two comparators—one for upper threshold detection and the other for lower threshold detection. The outputs from the two comparators are fed to an OR gate to generate a combined output—as an enable signal. The enable signal is used to control the subsequent quantization and wireless transmission circuit blocks. The threshold voltages, V_{TH+} and V_{TH-} , for the two comparators are produced by an adaptive threshold generation circuit which automatically sets the thresholds based on the noise level of the amplified neural signal. Typical operation waveforms of the AP detection circuit are shown in Figure 5-5. The output of the OR gate covers only a part of the complete AP waveform where the signal value exceeds either one of the threshold voltages. To preserve the complete AP waveform, a delay time of $T_{APD} = 400 \mu s$ is applied to the falling edges of both *enable_pos* and *enable_neg* using eight D flip-flops (DFFs) connected in series and the AP waveform before the onset of enable is stored using an analog buffer with a digital delay of $T_{FIR} = 300 \mu s$. T_{APD} and T_{FIR} are both empirically determined by observing the real neural waveforms recorded from rat brains [72],[73]. In Figure 5-5, the solid line depicts an illustration of

one neural spike and the dotted line is the output after the delay is added. As a result, the entire information of the AP waveform is well preserved for further storage, transmission, and processing.

Figure 5-4. Block diagram of spike detection circuit.

Figure 5-5. Operating waveforms of spike detection circuit.

Figure 5-6 presents the circuit implementation of the differentiator used for the AP detection. It consists of a differentiator with a differential to signal ended output stage. Due to the symmetry of the differentiator, the half equivalent circuit

analysis has been performed on the differentiator.

Figure 5-6. Differentiator circuit.

The transfer function of the differentiator is listed below:

$$\frac{v_{out1}}{v_{in}} = \frac{\frac{g_{curr-s}}{2} / g_{m,load} (1 + s \frac{2C}{g_{curr-s}})}{(1 + s \frac{2C}{g_{m1}})} \quad (5-1)$$

where g_{curr-s} and $g_{m,load}$ are the transimpedance of the transistor N_{curr-s} and N_{load} ; g_{m1} is the transconductance of the transistor N_1 . The dominant pole is at $g_{m1}/(2C)$, and the first zero is at $g_{curr-s}/(2C)$. The bandwidth ranges from 50 Hz to 8 kHz based on the post layout simulation, which completely cover the bandwidth of the AP signals. The total current consumption of the differentiator is 650 nA at 1 V supply, in which the input transistors N_1 consume 50 nA each, the load transistor N_{load} consume 25 nA, and the output stage consumes 500 nA.

Ac coupling is employed after the differentiator to remove any dc offset induced by the differentiator and reset the dc voltage of the signal to half V_{DD} . The signal is further processed by the adaptive threshold circuit shown in Figure 5-7.

The adaptive threshold circuit is to adaptively set the detection threshold which should be low enough to capture all the APs and high enough to reject most of the background noise. In this design, the background noise is assumed to have a Gaussian distribution with a mean of zero [74]. So the noise can be described by its rms value. The threshold voltage is set to be a ratio to the rms value and thus the threshold voltage can adaptively change with the neural signal under different noise background.

$$V_{TH+} - V_{cm} = V_{cm} - V_{TH-} \quad (5-2)$$

As seen in Figure 5-7, a pseudo resistor and a capacitor forms a low-pass filter with a low-pass corner frequency of less than 1 Hz. It serves the purpose of converting signal to a dc voltage level proportional to the duty cycle of the output of the comparator. So the threshold voltage varies with the background noise. V_{duty} is used to adjust the ratio of the threshold voltage to the rms value of the background noise through current control. The PPOLY resistors are used to convert the current to threshold voltages. The schematic of the low power continuous comparator is given in Figure 5-8. The input transistor is biased at weak inversion and has a large aspect ratio to minimize the comparator offset (the simulated offset voltage is 0.5 mV). The power consumption of the whole comparator is 400 nA under 1 V supply.

Figure 5-7. Adaptive threshold circuit.

Figure 5-8. Voltage comparator circuit.

Figure 5-9. Circuit implementation of delay element.

The pulse generated by the result of the spike detection is prolonged by the delay element to preserve the completeness of the AP waveform. The delay element is implemented using eight D flip-flops with four OR gates as shown in Figure 5-9. Each of the D flip-flops generates one clock delay, so the total delay created by the delay element is eight clock cycle (400 μ s).

5.2.3 Analog Buffer with Digital Delay

The analog buffer is implemented using the FIR filter of Figure 5-10. The main purpose of having the FIR filter in the system is to provide a well-defined linear delay to the neural signal so that the complete AP waveform can be passed to the subsequent blocks when the enable signal is triggered. The extra advantage of using the FIR filter as a delay buffer is that the out-of-band noise can be further suppressed by the sharp filtering characteristics. By estimating the time delay required for recording the initial part of the AP waveform from the neural signal recorded *in vivo*, an 8-tap FIR filter is implemented.

Figure 5-10. Block diagram of FIR filter.

Two conventional switched-capacitor buffers are connected in series to form a one-clock delay cell. Different filter coefficients are realized using switched capacitors with different weights—the setup comprises different number of multiple unit capacitors connected in parallel. The multiplication of the signal with the filter coefficient is accomplished via charge redistribution among the switched capacitors. First, the amplified neural signal is sequentially sampled on weighted capacitors ($C_{f0}, C_{f1}, \dots, C_{f8}$) by a set of switches. Next, the charges stored on the weighted capacitors are added together by another set of switches. To realize both positive and negative coefficient values, the switched capacitors are grouped into one array of positive coefficients and another of negative coefficients. The arrays of positive and negative coefficients are subtracted by its subsequent summing switched-capacitor amplifier. Details of the FIR coefficients are calculated based on the Matlab function tabulated in Table 5-1.

Table 5-1. Coefficients of the FIR filter.

Capacitor	Value (F)
C_{f0}	100 e-15
C_{f1}	50 e-15
C_{f2}	86 e-15
C_{f3}	295 e-15
C_{f4}	1.204 e-12
C_{f5}	295 e-15
C_{f6}	86 e-15
C_{f7}	50 e-15
C_{f8}	100 e-15
C_{sum_pos}	2.04 e-12
C_{sum_neg}	2.04 e-12

The one-clock delay block is implemented using two half-clock delay circuits.

Figure 5-11 depicts the circuit implementation of the half-clock delay circuit. A single sample-and-hold implements a delay of half a clock period.

Figure 5-11. A half-clock delay circuit.

All the switches used in the design are implemented using transmission gates.

The charge injection and clock feedthrough errors in the FIR filter are minimized

using small-size transistors with two dummy components at both sides of the switch, as shown in Figure 5-12. The size of the dummy switch is half of that of the switch. A good match of the dummy switch with the switch helps reduce the charge injection effect [1].

Figure 5-12. A switch and dummy switch circuit.

Figure 5-13. OTA circuit used in the half-clock delay block.

The schematic of the OTA used in the half-clock delay block is shown in Figure 5-13. The main design requirement of this OTA is low power consumption since the number of OTA is huge (18 OTAs for one channel). In order to achieve ultra-low power consumption, class AB output is employed—for better driving ability with small current. The total power consumption of each OTA is 180 nA under 1 V supply.

Figure 5-14. Layout and simulated performance summary of the designed neural recording interface IC.

Figure 5-15. Chip graph of fabricated 4-channel neural recording activity based analog channels.

5.3 Simulation Results and Discussion

The neural recording interface IC was designed in a standard 0.18- μm CMOS technology. It occupies a core area of 220 μm by 820 μm and does not require any off-chip component. The IC layout together with a summary of its simulated performances is presented in Figure 5-14. Figure 5-15 shows the chip graph of the 4 channel neural recording channels with bandgap reference and ADC.

The neural amplifier operates with a 1-V supply, from which it draws 1 μA providing 40-dB gain with a low-pass cutoff frequency of 5 kHz. The FIR filter consumes 5.6 μA and has a bandwidth of 5.7 kHz. The AP detection circuit consumes another 0.6 μA from the 1-V supply. Although the AP detection and delay circuit consumes extra power compared to the conventional neural

recording front–end design, the power saved in data storage, transmission and processing functions due to the reduced data volume should be much more significant [41], [73].

To verify the functionality of the proposed neural recording interface IC, simulations were performed using the actual neural signals pre-recorded from anesthetized rats [72], [73] as the input of the designed IC. Figure 5-16 shows the simulated outputs of the FIR filter and the spike detection circuit versus the pre-recorded neural signal input. Figure 5-17 provides a zoom-in view of the simulation results. Figure 5-17(a) is the input neural signal and Figure 5-17(b) is the spike detection output before the delay element. The two pulses in Figure 5-17(b) are resulted from the positive and negative phases of the neural spike, respectively. Figure 5-17(c) shows the enlarged spike recording window on the FIR output (Figure 5-17(d)) to preserve the complete AP waveform information. Table 5-2 provides a comparison between the different data compression techniques used for implantable wireless neural recording microsystems.

Figure 5-16. (a) Simulated outputs of the FIR filter and the spike detection circuit with (b) the pre-recorded neural signal from anesthetized rats (1.38-s long trace) as the input to the neural recording interface IC.

Figure 5-17. Zoomed-in simulation results with the pre-recorded neural signal from rats (6-ms short trace) as the input: (a) input neural signal, (b)

spike detection output before the delay element, (c) spike detection output after the delay element, (d) FIR filter output.

Table 5-2. Comparison of data compression techniques.

	Domain	Waveform preservation	Recording time per spike	Scalability
[41]	Digital	Partial	1 ms	Yes
[43]	Analog	Partial	2 ms	Restricted
[44]	Digital	Partial	2 ms	Yes
[45]	Digital	Poor	-	Yes
This work	Analog	Complete	Adaptive	Yes

A neural recording interface IC with lossless data compression based on spike detection and adaptive waveform windowing has been demonstrated for fully implantable multichannel wireless neural recording systems. Wireless transmission of the recorded neural signal waveform is enabled only during the presence of neural spikes, and hence the data rate can be effectively reduced by more than ten times [41] compared to the conventional wireless neural recording system. Furthermore, the complete neural AP information is securely preserved with adaptive AP recording windows. The functionality of the proposed recording interface IC design has been verified with intensive simulation using actual neural signal waveforms pre-recorded *in vivo*.

Chapter 6. CONCLUSION AND FUTURE WORK

6.1 Conclusion

The design and implementation of a fully implantable neural recording interface is presented in this thesis. The neural signal characteristics were introduced and various published system architectures were investigated. A review of various fully integrated neural recording systems was carried out together with a detailed discussion of the requirements and major concerns involved. In this project, sub-Hz low cutoff frequency, optimum noise-power trade-off and maximum input impedance are the key goals of the intended neural amplifier design.

In the low-power low-noise neural recording interface IC design, pumping a large current to suppress the noise floor is not a proper approach. Optimizing the noise-power trade-off is becoming more and more important. To design low-power low-noise neural recording amplifier, a comparative study and analysis on the various noise reduction techniques are conducted and discussed in this thesis. The power efficiencies of different noise reduction techniques were compared using the noise efficiency factor (NEF) as a gauging parameter. It is found that noise reduction using a simple current reuse technique yields the best power efficiency among the methods discussed in the thesis.

A neural recording front end amplifier (FEA) was designed using the current reuse technique. Circuit measurements showed excellent current efficiency, with an NEF of 2.2, which is the lowest (best) amongst the reported works [3][9][10][11][18][20][21]. The circuit operates at 1-V supply with current consumption of 1 μ A. The input-referred noise attained is 43 nV/ $\sqrt{\text{Hz}}$. The

measured high-pass cutoff frequency is less than 0.1 Hz, which is good enough for low frequency biopotential signal recording. Differential circuits were implemented to improve the CMRR and PSRR to well above 40 dB so as to reduce the effect from common mode interference and power line interference. Compared to the published structure in which power consumption greatly depends on the supply voltage and process variation [12][27], the proposed circuit is much more reliable in terms of its power consumption and performance, as its quiescent current is a well-defined stable value. In order to achieve ultra-low high-pass cutoff frequency with minimum chip area, a balanced MOS-diode pseudo-resistor structure is employed to achieve a balanced electrical property. The size of this neural amplifier is 100 μm by 500 μm . To promote the neural recording system integration, functions such as programmable gain, power down, and reset were added into the amplifier circuit for achieving larger dynamic range, higher power efficiency and faster startup. Besides the power consumption constraint, silicon area consumption is also a critical parameter for multi-channel designs. By moving the band-pass function in the system from the first stage to the second stage, the undesirable tie between the bandwidth, input-referred noise and chip area is successfully eliminated. Hence, the total area of neural recording channel can be reduced.

A pseudo open-loop amplifier was designed to improve the input impedance. In this approach, an input impedance of 20 pF is realised. Without the closed-loop feedback configuration, the amplifier operates in an unconditionally stable condition. The noise performance is also comparable to that of the closed-loop design. By choosing a suitable operation region for the input pair transistors and employing both NMOS and PMOS transistors as input pairs for better current

efficiency, the neural recording channel achieves a NEF of 2.2 to 3.6, which is among the lowest reported values. However, the input impedance can be further improved if the parasitic capacitance of the input transistors can be suppressed.

To further improve the performance of the neural recording analog front end, the input impedance of the neural amplifier should be increased as much as possible to bypass the negative effects, such as interferences and signal attenuation that are induced by the non-ideal microelectrode array. As a result, a positive feedback loop is inserted to both the closed-loop neural amplifier design and open-loop neural amplifier design. Based on the measurement results, the closed-loop neural amplifier with the input impedance boosting loop can achieve an input impedance of $80\text{ M}\Omega$ at 1 kHz (2 pF input capacitance), which is ten times larger compared to that of Harrison's conventional neural amplifier design. As is observed from the *in vivo* measurement result, the recording quality is greatly improved both in terms of noise immunity and interferences.

The 100-channel neural recording AFE chip was designed and fabricated using 0.18- μm CMOS technology. The proposed system facilitates power optimization of the individual functional block, where the average power per channel is about 50 percent less than that of the current state-of-the-art multi-channel designs. The designed neural recording AFE can achieve better or comparable performance of less than $5\text{-}\mu\text{V}_{\text{rms}}$ input-referred noise with much lower power consumption, providing an optimum and robust solution for the low-power low-noise neural recording interface design.

Due to the increasing number of recording channels, simultaneous neural recording generates huge amount of data for transmission, which consumes most

of the system power. To resolve this issue, a neural recording interface IC with lossless data compression based on spike detection and adaptive waveform windowing has been demonstrated for fully implantable multichannel wireless neural recording systems. The proposed neural recording interface IC detects the neural spikes and sends only the preserved AP information for wireless transmission in order to reduce the overall power consumption of the neural implant. Wireless data transmission of the recorded neural signal waveform is enabled only during the presence of neural spikes. Therefore, the data rate can be effectively reduced by more than ten times [41] compared to the conventional wireless neural recording system. To ensure the robustness of the neural recording system, the complete neural AP information is securely preserved with adaptive AP recording windows. The neural recording interface IC has been designed using standard CMOS 0.18- μm technology occupying a core area of 220 μm by 820 μm . The functionality of the proposed recording interface IC design has been verified with intensive simulation using actual neural signal waveforms pre-recorded *in vivo*.

6.2 Future Work

The research conducted over the past few years focuses mainly on the design of the neural recording interface circuits dedicated for neural signals acquisition. The proposed circuits realize the basic and primary functions of signal amplification and conditioning. Still there is a lot of work remaining to be done until a practically useful recording IC can be developed successfully.

First, for long term neural recording, the increase in electrode impedance due to scar tissue encapsulation will degrade the neural recording system performance. The large electrode impedance generates more noise and makes the recorded neural signal much weaker because a voltage divider is formed between the electrode impedance and the input impedance of the amplifier. Hence, the SNR is degraded significantly. Replacement of the implanted electrode may not be a preferred option as it requires complicated surgery and may cause infection and tissue damage. To mitigate this issue, amplifier with very high input impedance must be developed, considering the electrode impedance increases in chronic neural recording and smaller electrode has larger impedance.

Second, one of the most important requirements for a medical device is patient safety, which is rarely discussed in published amplifier designs. There might be tissue damage if there is dc current passing through the electrode under certain conditions like a failed neural amplifier and associated components. Additional safety circuitry must be designed to guarantee patient safety, which is defined by the kind and size of the tissue damage. To improve the robustness and safety of the system, some safety functions must be implemented, such as fail-safe circuit, to ensure no damages to human even if the operation fails. In the event that one neural amplifier fails, a possible approach is to permanently ground its input and have the recording system report the problem to the physician. Powering off the whole neural recording IC should be the safest method, which may sacrifice the benefits resulting from the good electrodes. The system should have a self-test or electrode-impedance measurement circuit to monitor and detect the excess leakage current on the electrode periodically, which has not been reported so far. To reduce the tissue damage, this monitoring function should be implemented

using biphasic, zero-mean current.

In summary, a wireless low-power fully implantable high-density neural recording system solution for neural prosthesis is the next step forward.

List of Publications

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