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Zhang, Jiye

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NANYANG
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**PROCESS INDUCED RELIABILITY OF THROUGH
SILICON VIA**

ZHANG JIYE

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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PROCESS INDUCED RELIABILITY OF THROUGH SILICON VIA

Zhang Jiye

School of Electrical and Electronic Engineering

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Summary

Insatiable consumer demand for multifunctional and high performance integrated circuits and systems has necessitated three-dimensional (3D) integration with through silicon via (TSV) technology. 3D integration has provided a scaling path to reduce the wire length and power consumption. At the same time, it increases the input/output (I/O) density and communication bandwidth. In its simplest form, TSV is fabricated by high-aspect-ratio etching of silicon and filling with copper (Cu) by electroplating. Integration of TSV poses new challenges. Due to large CTE (coefficient of thermal expansion) mismatch between Si and Cu, large compressive stress is induced in the Si which causes mobility variation and mechanical deformation. TSV has strong electrical coupling with the doped Si substrate through the MOS structure. TSV parasitic capacitance has the most predominant impact on the circuit operation. It is therefore imperative to control the electrical parasitic and stress for successful TSV integration. Thus it is essential to measure and analyze the stress characteristics of the TSV structure. Among several potential techniques, the micro Raman spectroscopy appears to be particularly promising and is applied to measure the local stress distribution in Si near Cu TSVs.

Copper filled TSV sample with diameter range from 4 to 10 μm with an interval of 1 μm were investigated. We also study the effects of different TSV liner materials on thermal stress relief. The two different liner materials are plasma enhanced tetraethylorthosilicate (PETEOS) SiO_2 and carbon doped SiO_2 Low- κ materials (SiCO).

Confocal micro-Raman system LabRam HR by Horiba Scientific was used for the Raman measurements. Results from the experimental investigation were compared with the theoretical prediction (FEM performed by COMSOL®). The overall correlation between theory and experiment is reasonably good.

It is found that the stress close to TSV decreasing rapidly while scaling down TSV from diameter of 10 μm to diameter of 4 μm due to the lower copper volume. By studying TSVs with different liner materials, we find it is also possible to control the stress level via the selection of a suitable liner material with a lower elastic modulus. The interesting findings can be attributed to the fact that the choice of a lower Young's modulus and a porous dielectric liner material could effectively reduce the compressive near surface stress in Si.

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Symbols and Abbreviations

$2D$	2 dimensional
$3D$	3 dimensional
λ	Wavelength
u	Carrier mobility
KOZ	Keep out zone
TSV	Through silicon via
ω	Frequency
A	Amplitude
σ	Stress
σ_{xx}	Principal stress in x direction
σ_{yy}	Principal stress in y direction
ε	Strain
κ	Value of dielectric
R	Resistance
C	Capacitance
L	The length of TSV
D	Diameter of TSV
RIE	Reactive ion etching

PETEOS	Plasma TEOS silicon oxide
SiP	System in package
VLSI	Very large scale integration

1 Introduction

1.1 Overview

Since 1958, Jacky Kilby invented the world's first integrated circuit; the transistor density on a single monolithic chip has been increased at an astonishing rate. Very large scale integration (VLSI) circuits are being aggressively scaled to meet the demand. Advances in VLSI technology are producing larger ICs with more transistors and longer interconnection bus lines, which result in much greater RC delays. This in turn has introduced some very serious problems for the semiconductor industry. Our future electronic system would require higher bandwidth to process massive data with low power consumption. The proposal of doubling the number of transistors on an IC chip every 24 months by Gordon Moore in 1965 has been the most powerful driver for the development of the microelectronics industry in the past 47 years. This law emphasizes lithography scaling and integration (in 2D) of all functions on a single chip, such as system-on-chip (SoC). As the minimum feature size of silicon device shrinks to nanometre, the scaling paradigm is threatened by interconnection limits including excessive power dissipation, insufficient communication bandwidth and signal latency[1]. As traditional 2D interconnection method shows that a chip is always divided into several blocks which are connected together with multiple layers of metal interconnections that can be very long. This brings the problem of signal delay, high power consumption and decreasing bandwidth.

1.2 Motivation for three dimensional integration

1.2.1 Conventional IC packaging technology

The semiconductor IC chips are usually packaged in components such as the plastic or ceramic quad flat pack (QFP), plastic or ceramic ball grid array (BGA), plastic or ceramic column grid array (CCGA), bump chip carrier (BCC), thin outline package (TOP), and wafer level chip scale package (WLCSP). These chips can be placed either face down or face up, rather on a substrate or on a lead frame. These components are then assembled on the PCB[2]. In some applications, the semiconductor IC chips can be directly attached on the PCB with either wire bonds or solder bumps.[3]

1.2.2 3D IC integration technology

1.2.2.1 FEOL, BEOL, and MEOL

FEOL (front end of line) is usually performed in the semiconductor fabrication plants to pattern the active devices, for example, transistors. The process is from a bare wafer to passivation, which covers everything except the bonding pads for the next level of interconnects, that is, BEOL.

BEOL (back end of line) is usually performed in packaging assembly and test houses, and it involves everything after passivation.

MEOL (mid end of line) is new and performed by combining some of the FEOL and BEOL technologies into a 3D IC integration technology, which involves, for example, TSV, microbumps, thin wafer handling, metallization, wafer bumping, back grinding, dicing, and testing. Thus, 3D IC integrations must be executed in the fabs and packaging assembly and test houses. However, since the fabs' equipment and

semiconductor personals are too expensive to make the 3D IC integration and final test right before the PCB assembly, eventually, the packaging assembly and test house will do it all.

1.2.2.2 More than Moore

Apart from SoC (system on chip), integration of all these functions can be achieved through either 3D IC integration or 3D Si integration, which are some of the more-than-Moore technologies. Based on the silicon platform technology, anything that involves the integration of electronics, photonics, mechanics, chemistry, heat, magnetics, biology, etc, for functionality and system performance when interacting with people and the environment is known as more-than-Moore.[4]

1.3 Through Silicon Via (TSV)

1.3.1 Introduction

Through silicon via (TSV) constructs a bridge from traditional 2D integration to 3D integration. It provides advanced vertical interconnects and system-in-package (SiP) solutions, such as chip-to-chip, chip-to-wafer, and wafer-to-wafer stacking.[1]

1.3.2 Manufacturing process for TSV 3D IC integration

Today the only volume product with TSV is Toshiba's CMOS image sensors. In order to reduce the footprint and enhance the performance of the product, they converted the wire bonding technology to flip-chip technology.

There are five key steps to make the TSV:

1. Via formation by either DRIE or laser drilling.

2. SiO₂ deposition by either thermal oxidation for passive interposers or PECVD (plasma enhanced chemical vapor deposition).
3. Barrier and seed layer deposition by physical vapour deposition (PVD).
4. Cu electro deposition or tungsten to fill the vias.
5. CMP of copper deposition residues (overburden).

1.3.3 The problem and challenges of TSV faced

During the design of integrated circuits, the monolithic construction of the devices involves etching the silicon and layering metals, insulators, and other semiconductors on top of the base substrate. Due to differences in the thermal expansion coefficients of the materials, the stresses are produced in the silicon substrate, this situation comes much worse for TSV enabled 3D technology. So one of the major challenges of 3D IC integration is the large thermal stress caused by the CTE (Coefficient of Thermal Expansion) mismatch between silicon and copper.

1.4 Scope of work

In this project, the thermal stress around through silicon via (TSV) are measured and studied. As many other works have already focused on TSV stress characterization with specific dimension, this thesis will put majority of its works on study of the dependency of stress distribution on variations of TSV diameters and pitches. Besides that, two kinds of TSV chips (TSVs with silicon oxide liner and SiCO liner) were fabricated and employed as the Raman spectroscopy samples for measuring stress induced in silicon. Combining with the electric characteristics of TSVs fabricated with two kinds of liner material, methods and suggestions are provided to solve the TSV reliability issues caused by the thermal stress. The stress

distribution was further coupled to carriers mobility change, and also the keep out zone for devices planting were mapped.

The specific objectives of the research project include:

- (a) Built model by COMSOL[®] finite element analysis tools. The model was applied to compute the stress distribution around TSV.
- (b) The Lorentzian peak fitting algorithm was developed to refine the resolution of Raman spectroscopy.
- (c) Compared the simulation results and the experimental data obtained through Raman spectroscopy. The modeling parameters were adjusted to meet the experimental results, so to make the simulation be more accurate and precise.
- (d) Coupled the stress to carriers mobility change and mapped the keep-out-zone (KOZ).

1.5 Thesis organization

The main focus of this project is on the investigation of thermal stress induced by mismatch of coefficient of thermal expansion (CTE), providing methods for mitigation of stress and mapping of keep-out-zone.

Chapter 2 is about the literature study of fundamental theory of laser spectroscopy. The near surface stress around TSV is favorably discussed and compared for the reason of that devices are planted within a depth of 200 nm.

Chapter 3 introduces the process steps for the sample preparation. The parameters of Raman spectroscopy are also indicated. Chapter 3 presents how the anisotropic properties of silicon are taken account into the finite element analysis.

In chapter 4, the experiment results are presented. It demonstrates that the miniaturization of the TSV dimension is not the only way to reduce the thermal mechanical stress in Si surrounding the TSV structure. It is also possible to control the stress via the selection of a suitable liner material with a lower elastic modulus. Finally, the keep-out-zone maps are plotted based upon the model simulation.

Chapter 5 summaries the contribution of this master thesis and the suggestions for the future work are provided.

2 Literature Review

2.1 Introduction of Stress

In continuum mechanics, stresses are dimensions of the internal forces acting within a deformable body. More specifically, it is a measure of the average force per unit area of an infinitesimal surface. These internal forces appear as against reaction to external forces applied to the body. The loaded body should behave as an continuously as assumed in mechanics, so these internal forces arise continuously throughout the whole body, which result in deformation of the body's shape to maintain a force balance status. Beyond certain limits of material strength, this can lead to a permanent shape change or structural failure.

The stresses studied in continuum mechanics are only the internal forces induced by the loading of external forces and the loaded body shape change, We may refer this size change as strain; most of the time, relative changes in deformation are considered rather than absolute values. A body is treated stress-free when there is no external forces act on it. Under such kind of situation the only forces present are those inter-atomic forces (ionic, metallic, and Van Der Waals forces). The atomic forces take responsibility to hold the body together and to keep its shape. Stresses generated during manufacture of the body to a specific configuration are also excluded.

The dimension of stress is the same as the pressure applied to the body, and thus the SI unit for stress is the Pascal (symbol Pa), which is equivalent to one Newton (force) per square meter (unit area), that is N/m^2 .

2.1.1 Simple stress theory introduction

In mechanics, for the simplest case of an axially loaded body is a bar subjected to tension or compression by a force passing through its axis. Assume a solid is under self-equilibrating forces, as shown in Figure 2.1. Now we divide the body into two parts. Internal forces act in the upper surface of the cross section, which represent the action of the lower part of the body on the upper part. Straightforwardly, as a

Figure 2.1 Internal forces in a solid body under a self-equilibrating system of forces

consequence of the equilibrium condition, the lower surface forces act with the same magnitude and in opposite directions. The forces F_n represent the result of the internal forces distributed in the section, which generally vary from point to point in practiced cases. We may consider the forces F_n is a homogeneous distribution in an infinitesimal area, dA . Dividing the infinitesimal force dF by the infinitesimal area dA , we get the internal force per unit of area or stress [5].

$$\sigma_{avg} = \frac{dF}{dA} \quad (2.1)$$

2.1.2 Combined stress

In complex application circumstances, mechanical bodies usually subjected to more than one type of stress at the same time; this brings out the concept of combined stress. In the case of two or more stresses act on one plane, i.e. bending and shear, the internal forces are categorized as biaxial stress. For combined stresses that act in all directions, i.e. bending, torque, and pressure, is triaxial stress.

Figure 2.2 shows the stress acting in a rectangular parallelepiped defined by three pairs of facets, which are perpendicular to the three coordinate axis and are located in an infinitesimal neighbourhood of point P [5].

Figure 2.2 Positive normal and shearing stresses

From Figure 2.2, there are three pairs of facets. Each pair of facets is perpendicular to a particular coordinate axis. The stress σ_{11} is positive if it have the same direction as the coordinate axis it parallels to, and also the facet is known as a positive facet for axis x_1 . According to the convention, the principle stress in the positive direction of axis x_1 , x_2 and x_3 are denoted as σ_{11} , σ_{22} and σ_{33} , respectively. The

shearing stresses on the facets i are denoted depending on the direction of the shearing stress vector.

2.2 Spectroscopic experiment

The structure of atoms and molecules are usually studied using spectroscopic investigation. Spectroscopy is used to refer to the broad area of technology dealing with the absorption, emission or scattering of electromagnetic radiation by molecules, ions, atoms, or nuclei.

Since 1960 Theodore H. Maiman operated the first functioning laser at Hughes Research Laboratories, there have been already 50 years that laser spectroscopy was still a very intense field of research. The laser spectroscopy distributed with the developments of laser instruments into areas of medicine, chemistry, mechanic, biology and material science etc. Moreover, laser spectroscopy has provided an ever-increasing number of applications. Over the last ten years, three Nobel Prizes have been awarded to nine scientists in the field of laser spectroscopy and quantum optics. The invention of new experimental techniques enabled this fast development of laser spectroscopy, such as refinement of currently existing laser type, the invention of new kind of lasers, the realization of optical parametric oscillators and amplifiers in the femtosecond range, the revolution in the measurements of absolute optical frequencies. These technical developments have stimulated many kinds of applications in industrial areas. the broaden applications of laser spectroscopy can be find in any possible way. In chemistry, laser spectroscopy is applied to determine molecule structures, and it is also an efficient method to tell the

material types. Moreover, laser spectroscopy provides new solutions for surface inspections, purity checks and analysis of chemical compositions.

2.3 Prediction and measurement of stress

There are two paths to map the distribution and magnitude of residual stresses in a certain component. One is prediction and the other one is experimental measurement. Experimental measurements are usually time consuming but they have the advantage of being applicable to a wide range of problems. Prediction is limited to fewer cases and very often entails an intensive computational effort [6].

2.3.1 Prediction of stress

Prediction refers to the theoretical or finite element based computation of residual stresses and is still an embryonic method. Residual stress prediction may be applicable now to relatively complex problems with the use of finite element based tools. Through all this research I used COMSOL[®] as the stress model simulation software, the uncertainties associated with material properties, material nonlinearities and actual loading conditions call for the developments of experimental residual stress measurement methods as the validating tools. Prediction can be applied easily for a particular kind of problem in which the material properties, constitutive equations, and values of residual stresses can be calculated or predicted using analytical or numerical methods.

2.3.2 Stress measurement

Measurement of residual stress is based on approaches completely different from the prediction methods. Since experimental measurement methods are applicable

to an object only where there is a pre-existing residual stress state. Under these conditions, the knowledge of the actual process that locks the residual stresses into a material is not necessary. It should be noted that stresses cannot be measured directly. All the measurements should be done indirectly such as deformations or strains. Several cases of stresses are possible with respect to the type of residual stresses that can be measured: (a) uniaxial, (b) biaxial, and (c) triaxial. They are differentiated by the number of principal stresses that are different from zero. For example, those cases the stress tensors can be expressed in a Cartesian coordinate system as,

$$\sigma_a = \begin{bmatrix} \sigma_{xx} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \sigma_b = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & 0 \\ \sigma_{yx} & \sigma_{yy} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \sigma_c = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}$$

In the simplest case of uniaxial residual stress, only $\sigma_1 = \sigma_{xx} \neq 0$, whereas in the most general case of triaxial residual stresses $\sigma_1 \neq 0$, $\sigma_2 \neq 0$, and $\sigma_3 \neq 0$. In actual mechanical components, residual stresses tend to be of the triaxial type. However, in most cases, assumptions can be made only considering the measurement of a biaxial (or even uniaxial) residual stresses state. For instance, boundary conditions require the existence of at most a biaxial stress at the surface of an object, which may have triaxial residual stresses in its interior, and conditions at the surface are often of interest since that is where failure due to fatigue or other mechanisms generally started. Any method intended to measure surface residual stresses can, thus, consider only biaxial stresses. A further simplifying assumption can be made to consider a uniaxial stress state instead in those cases where the residual stresses are biaxial with one of the principal stresses dominant over the other.

There are a bewildering number of methods devised to measure the residual stresses, which can be classified roughly as non-destructive, semi-destructive, and destructive.

2.3.2.1 Non-destructive methods-Raman spectroscopy

Non-destructive methods are based on the measurements of variations in the atomic, acoustic, magnetic, or thermoelastic properties in a given object containing residual stresses. Micro-Raman spectroscopy is increasingly used as a technique to study local mechanical stress in devices and structures in microelectronics [7]. It has the advantages of being a fast, non-destructive technique with micrometer resolution. The effects of strains and stresses on Raman frequency of the optical phonons of silicon are well known and extensively documented. However, it is still difficult to be used for practical applications encountered in microelectronics systems. Some qualitative information can be obtained directly from the measured Raman shift. It can, in general, be concluded that a Raman frequency larger than the stress free frequency indicates compressive stress in samples, while a Raman frequency smaller than the stress-free indicating tensile stress of the sample. However, this statements, which is often used, is not always correct. All nonzero stress tensor components, which are at most six different terms, influence the positions of the Raman peaks. For example, in a local oxidation of silicon (LOCOS) isolation structure, there are compressive stresses in the active area in the horizontal direction due to the field oxide. On the other hand, there are tensile stresses in the vertical direction at the bird's beak [7]. So depending on the relative magnitudes of these stresses, an upward

or a downward shift of the Raman peak from the stress-free value will be observed. In order to relate the measured Raman shifts of the stresses present in the sample, some

Figure 2.3 LOCOS birds beak

prior knowledge of the stress distributions in the sample are required. In other words, one has to presuppose a stress model. As we have already known that the stresses in the sample can be described by a very simple model, for example when one can assume that uniaxial stress or uniform biaxial stress is present in the system; calculations of the Raman shift as a function of this stress are straightforward and give simple linear relations between the observed Raman shift and the stress. However, in most practical examples encountered in microelectronics, the stress picture is quite complicated, such as in thin film-lines, in a LOCOS isolation structure, or at a trench isolation structure. As a result, the calculation of the relation between Raman shifts and stresses will also be complicated. Furthermore, the penetration depth of the laser beam in the material, the spot size, and the relative intensity of the different Raman modes have to be taken into account in order to give a correct interpretation of the data.

The effects of strain (ε_{ij}) on the Raman modes in (100) silicon are described by the secular equation

$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) & 2r\varepsilon_{12} & 2r\varepsilon_{13} \\ 2r\varepsilon_{12} & p\varepsilon_{22} + q(\varepsilon_{11} + \varepsilon_{33}) & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{22} + \varepsilon_{11}) \end{vmatrix} - \lambda I = 0 \quad (2.2)$$

where p , q and r are material parameters representing the phonon deformation potential. For unstrained silicon, there are three generated Raman modes with the same wavenumbers ($\omega_0 \sim 520.53 \text{ cm}^{-1}$) but different polarizations: two transverse optical modes (TO) and one longitudinal optical mode (LO). With strain, the three optical modes in general have different frequencies (ω_i) and different intensities, corresponding to three Raman peaks. The eigenvalues of the secular equation predict

the Raman frequency shifts, $\Delta\omega_i = \omega_i - \omega_0 \approx \lambda_i / (2\omega_0)$. The intensity of the Raman signal for each optical mode depends on the polarization vectors of the incident and scattered light. Most Raman systems have a backscattering configurations, where the incident light is nearly perpendicular to the sample surface. For backscattering from (100) silicon, only one of the three Raman modes is observable [8].

For the TSV specimen as illustrated in Figure 2.4, the near surface stress in Si is approximately biaxial, represented as $(\sigma_r, \sigma_\theta)$ in a cylindrical coordinate for the

Figure 2.4 Schematic of a fully filled TSV structure near the wafer surface

radial and circumferential stresses. For Raman scanning along the [110] direction, the frequency shift for the observable Raman mode is related to the stress components as

$$\Delta\omega_3 = \frac{\lambda_3}{2\omega_0} = \frac{p\varepsilon_{12} + q(\varepsilon_{11} + \varepsilon_{12})}{2\omega_0} (\sigma_r + \sigma_\theta) \quad (2.3)$$

where ε_{11} and ε_{12} are components of the elastic compliance tensor. Thus, the sum of the two stress components can be measured from the Raman shift. To determine the effective proportionality factor between the Raman shift and the stress sum for the

specific experimental conditions, calibration measurements by high-resolution X-ray diffraction (XRD) on an equibiaxially stressed film system were conducted by Suk-Kyu Ryu, yielding the relation [9]

$$\sigma_r + \sigma_\theta (MPa) = -434.5 \Delta\omega (cm^{-1}) \quad (2.4)$$

Note that the reference frequency ω_0 also depends on the system calibration, typically with 0.02 cm^{-1} spectral resolution, which corresponds to a stress resolution of 10 MPa.

2.3.2.2 *Destructive methods*

Methods for predicting the residual stresses are based on reproducing the exact steps that introduced them in a material starting with the stress free state. By contrast, experimental destructive and semi-destructive methods start with the final state and, in a sense, try to reverse the process that locked residual stresses in the first place. Destructive and semi-destructive measurement methods are based on the perturbation of the internal equilibrium that locked residual stresses.

Destructive sectioning is the oldest method applied to measure residual stresses [10]. The perturbation of the internal equilibrium state is the basic principle upon which destructive sectioning methods are based. The separation of part of a stressed material leads to its re-accommodation in order to achieve a new internal equilibrium condition, which manifests itself as a change in the geometric configuration. The corresponding displacements or strains can then be correlated to the pre-existing residual stresses. The energy releasing that accompanying the change in geometry tends to reverse the process that locked residual stresses into the material.

This reversing process can be total or partial depending on the amount of removed materials, the method used to remove it, and the existence of plastic regions. Sectioning methods usually divide an object into smaller pieces in several steps in order to measure the distribution of residual stresses across a section.

A variant of the sectioning method is the layer removal method, which can be considered destructive or semi-destructive depending on the amount of material removed. In this method, applicable mainly to prismatic or cylindrical objects, thin layers of material are removed in several steps either by machining or chemical etching. The magnitudes of residual stresses in each layer are then found by measuring the curvature, change in length, or distortion of the remaining material. The material removal method should not create additional residual stresses in the newly exposed sub-surface layers. To this effect, chemical etching or electrical discharge machining (EDM) is favored relative to mechanical removal methods such as milling or turning. However, the dimensional control tends to be rather difficult with chemical etching.

2.4 Raman spectroscopy

Raman spectroscopy is a method of determining vibrations of molecular, especially for the case of covalently bonded molecules. When radiation passes through a transparent medium, the species present scatter a part of the beam in omnidirectional. Raman scattering results from the same type of quantized vibrational changes associated with IR absorption. So, the wavelength difference between the incident light and the scattered visible radiation corresponds to wavelengths in the mid infrared region. In 1928, the Indian physicist, C.V. Raman, discovered that the

visible wavelength of a small fraction of the radiation scattered by certain molecules differs from that of the incident light and furthermore that the shifts in wavelength depend on the chemical structure of the molecules responsible for the scattering. Raman was awarded 1931 Nobel Prize in physics for this discovery and for his systematic exploration of it.

Raman spectra are acquired by irradiating a sample with a powerful laser of visible or near infrared radiation. The spectrum of the scattered radiation is measured at some angle, often at 90 degree, with a suitable spectrometer. To avoid fluorescence, the excitation wavelengths are usually well removed from an absorption band of the analyte. The general idea of Raman experiment is shown in Figure 2.5.

As incident radiation of frequency ν_{ex} , impinges on the sample, molecules of

Figure 2.5 Inelastic scattering in Raman Spectroscopy

the sample are excited from one of their ground vibrational states to a higher so called virtual state, indicated by the dashed level in Figure 2.5. When the molecules relax,

it may return to the first vibrational state as indicated and emit a photon of energy $E=h(\nu_{ex}-\nu_v)$, where ν_v is the frequency of the vibrational transition. Alternatively, if the mole is in the first excited vibrational state, it may absorb a quantum of the incident radiation, be excited to the virtual state, and relax back to the ground vibrational state. This process produces an emitted photon of energy $E=h(\nu_{ex}+\nu_v)$.

In both cases, the emitted radiation differs in frequency from the incident radiation by the vibrational frequency of the molecule ν_v . The spectrum resulting from the inelastically scattered radiation shows three peaks one at $\nu_{ex}-\nu_v$ (stokes), the second intense peak is at ν_{ex} for radiation that is scattered without a frequency change, and the third (anti stokes) is at $\nu_{ex}+\nu_v$. The intensities of the stokes and ant stokes peaks give quantitative information, and the positions of the peaks give qualitative information about the sample molecule. Elastic scattering can also occur with

Figure 2.6 Simplified Raman spectrometer layout

emission of a photon of the same energy as the excitation photon $h\nu_{ex}$. Scattered radiation of the same frequency as the source is termed *Rayleigh scattering*.

2.5 Widths and profiles of spectral lines

Spectral lines are never strictly monochromatic in both cases of absorption or emission spectrum. Although by employing interferometers with a very high resolution, people always observe a spectral distribution $I(\nu)$ around the central frequency. The spectral distribution corresponding to energy transition between upper and lower levels. The function curve $I(\nu)$ around the central frequency ν_0 is known as line profile, as shown in Figure 2.7.

Figure 2.7 Line profile of a spectral line shows the line wings and line kernel

The frequency difference between ν_2 and ν_1 , where $I(\nu_1)=I(\nu_2)=I(\nu_0)/2$, the full width is always known as the linewidth of the spectral line. When the angular frequency is taken account into consideration, the halfwidth is expressed in the form of $\omega=2\pi\nu$ with $\delta\omega=2\pi\delta\nu$, or in terms of the wavelength λ (in units of nm or Å) with $\delta\lambda=|\lambda_1-\lambda_2|$. From $\lambda=c/\nu$, we can get that

$$\delta\lambda = -(c / v^2)\delta v \quad (2.5)$$

However, the relative halfwidths are the same in all three formations:

$$\left| \frac{\delta v}{v} \right| = \left| \frac{\delta \omega}{\omega} \right| = \left| \frac{\delta \lambda}{\lambda} \right| \quad (2.6)$$

The spectral region within the halfwidth is called the kernel of the line, the regions outside ($v < v_1$ and $v > v_2$) are the line wings.

2.5.1 Natural linewidth

As atom absorb excitation energy, the excited atom can release its energy in the form of radiation. The classical model of a damped oscillator is applied to describe the behaviors of excited atomic electron. By using this model, the spectral distribution of spontaneous emission on the transition from E_i to E_k can be investigated. The radioactive energy loss results in a decreasing of the oscillation amplitude. The damping phenomenon is described by a damping constant γ . We could see that for real atoms the damping is extremely small, which mean that $\gamma \ll \omega$.

From the differential equation of motion, $x(t)$ can be obtained from solving of equation (2.7)

$$\ddot{x} + \gamma \dot{x} + \omega_0^2 x = 0 \quad (2.7)$$

where $\omega_0^2 = k / m$.

The real solution of (2.7) with the initial values $x(0) = x_0$ and $\dot{x}(0) = 0$ is

$$x(t) = x_0 e^{-(\gamma/2)t} [\cos \omega t + (\gamma / 2\omega) \sin \omega t] \quad (2.8)$$

There is no big difference between the frequency $\omega = (\omega_0^2 - \gamma^2 / 4)^{1/2}$ of the damped oscillation and the central frequency ω_0 of the undamped case. So for the case of small damping factor we can set $\omega = \omega_0$ and just drop the second term in (2.8) to simplify the computation. With this approximation, which is still very accurate for real atoms, we obtain the solution of (2.7) as

$$x(t) = x_0 e^{-(\gamma/2)t} \cos \omega_0 t \quad (2.9)$$

The frequency $\omega_0 = 2\pi\nu_0$ of the oscillator corresponds to the central frequency $\omega_{ik} = (E_i - E_k) / \hbar$ of an atomic transition $E_i \rightarrow E_k$.

2.5.2 Lorentzian line profile of the emitted radiation

As the oscillation decreases gradually, the amplitude $x(t)$ decrease with time t . The emitted radiation is no longer monochromatic. Instead, it shows a frequency distribution related to the function $x(t)$ in (2.9) by a Fourier transformation (Figure 2.8).

Figure 2.8 (a) Damped oscillation (b) Fourier transformation of $x(t)$ indicates the intensity $I(\omega - \omega_0) \propto |A(\omega)|^2$

Actually, the damped oscillation $x(t)$ is a superposition of a series monochromatic oscillations $\exp(i\omega t)$ with different frequencies ω and amplitudes $A(\omega)$

$$x(t) = \frac{1}{2\sqrt{2\pi}} \int_0^{\infty} A(\omega) e^{i\omega t} d\omega \quad (2.10)$$

The amplitudes $A(\omega)$ are calculated from (2.9) and (2.10) as the Fourier transform

$$A(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{+\infty} x(t) e^{-i\omega t} dt = \frac{1}{\sqrt{2\pi}} \int_0^{\infty} x_0 e^{-(\gamma/2)t} \cos(\omega_0 t) e^{-i\omega t} dt \quad (2.11)$$

The lower integration limit is taken to be zero because $x(t) = 0$ for $t < 0$. Equation (2.11) can readily be integrated to give the complex amplitudes

$$A(\omega) = \frac{x_0}{\sqrt{8\pi}} \left(\frac{1}{i(\omega - \omega_0) + \gamma/2} + \frac{1}{i(\omega + \omega_0) + \gamma/2} \right) \quad (2.12)$$

The real intensity $I(\omega) \propto A(\omega) A^*(\omega)$ contains terms with $(\omega - \omega_0)$ and $(\omega + \omega_0)$ in the denominator. In the vicinities of the central frequency ω_0 of an atomic transition where $(\omega - \omega_0)^2 = \omega_0^2$, the terms with $(\omega + \omega_0)$ can be neglected and the intensity profile of the spectral line becomes

$$I(\omega - \omega_0) = \frac{C}{(\omega - \omega_0)^2 + (\gamma/2)^2} \quad (2.13)$$

The constant C can be defined in two different ways:

For consideration of different line profiles it is useful to define a normalized intensity profile $L(\omega - \omega_0) = I(\omega - \omega_0) / I_0$ with $I_0 = \int I(\omega) d\omega$ such that

$$\int_0^{\infty} L(\omega - \omega_0) d\omega = \int_{-\infty}^{+\infty} L(\omega - \omega_0) d(\omega - \omega_0) = 1 \quad (2.14)$$

With this normalization, the integration of (2.13) yields $C = I_0 \gamma / 2\pi$.

$$L(\omega - \omega_0) = \frac{\gamma / 2\pi}{(\omega - \omega_0)^2 + (\gamma / 2)^2} \quad (2.15)$$

is called the normalized Lorentzian profile. Its full halfwidth at halfmaximum (FWHM) is

$$\delta\omega_n = \gamma \quad (2.16)$$

Any intensity distribution with a Lorentzian profile is then

$$I(\omega - \omega_0) = I_0 \frac{\gamma / 2\pi}{(\omega - \omega_0)^2 + (\gamma / 2)^2} = I_0 L(\omega - \omega_0) \quad (2.17)$$

with a peak intensity $I(\omega_0) = 2I_0 / (\pi\gamma)$.

3 Research methodology

3.1 Sample preparation

High aspect ratio TSV is often required to meet the demand for high density I/Os, especially when the top Si layers cannot be thinned down indefinitely due to challenges in subsequent handling. Therefore, in order to fabricate void free TSV, super-conformal filling of TSV with Cu is desired using bottom-up filling. We are

Figure 3.1 Process flow (a) 100 Å thermal oxide deposition;(b) Boron implantation;(c) 8 kÅ CVD oxide;(d) via formation by DRIE Si etch and using oxide as the hard mask; (e) liner deposition; (f) Ta barrier/Cu seed deposition, Cu-ECP, Cu-CMP and nitride passivation layer deposition; (g) contact opening; and (h) Al metallization and patterning.

targeting TSV with 4, 5, 6, 7, 8, 9 and 10 μm of diameter and an aspect ratio of 1:2 for ease of fabrication. Even though TSV with higher aspect ratio is often desired, the chosen aspect ratio is sufficient to study the TSV induced stress. Figure 3.1 shows the detailed fabrication process flow of the TSV structures. Prior to TSV fabrication, p^+ contact is formed on the Si substrate for grounding purpose. Si vias are etched by using a cyclic etching-passivation BOSCH process in a deep reactive ion etcher (DRIE) using oxide hard mask. After that, the dielectric liner is deposited in a plasma enhanced chemical vapour deposition (PECVD) chamber at temperature $<400^\circ\text{C}$ using tetraethylorthosilicate (TEOS) and black diamond precursors for oxide and low-K liner, respectively. For both the two kinds of TSV samples, the liners thickness is 200nm.

The black diamond is one of the common low-K dielectrics for the industry 90/65nm nodes from Applied Materials. Then, the Ta barrier and Cu seed are sputtered by using ENDURA deposition chamber. Subsequently, Cu electroplating (ECP) is carried out to fully fill the TSV and we use RENA system and Enthone chemical solution for the ECP process. The acid copper plating process was specially developed for filling blind micro-vias and plating through-holes simultaneously. The excess Cu overburden is then removed by chemical mechanical polishing (CMP) process which uses Rohm and Haas high polish rate slurry (the slurry is colloidal silica-based used in Cu CMP for bulk Cu removal). Contact holes are opened on oxide layer and Al is deposited and patterned to form contact pads for electrical probing. The area surrounding the TSV is grounded by performing Boron p^+ implantation and activation [11].

The major fabrication steps of TSV include DRIE Si etch, liner deposition and Cu filling. In order to have a robust TSV, the sidewall scallop roughness and the oxide hard mask undercut (also known as over-hang) which are caused by the cyclic etching and passivation of the BOSCH process must be kept as small as possible. If the scalloping roughness or the undercut is too significant, it would be a challenge for the subsequent liner deposition step to have a conformal liner deposition, which may induce high leakage current.

Figure 3.2 TSV having Cu as the core conductor with PETEOS liner

Similarly, it would be difficult for the Ta barrier and Cu seed layer sputtering processes to have a conformal barrier and seed layer deposition, which may lead to uncompleted Cu filling. Both side effects are detrimental to TSV yield and reliability. The BOSCH process alternates the short step of SF_6 plasma for the fast isotropic removal of silicon with short C_4F_8 plasma deposition step for the sidewall protection, and the C_4F_8 polymer is removed before starting the next round of etching step with SF_6 [11].

Table 3-1 is a comparison of TSV etching results using two different etching recipes. When a single photo-resist mask is used to etch the oxide hard mask and to etch the Si, the addition of a small quantity (20 sccm) of C₄F₈ during etching cycle improves both roughness and undercut (Process A vs Process B). The scallop roughness reduces from ~120 to ~70 nm, while the undercut reduces improves from ~240 to ~60 nm.

Table 3-1 Comparison of TSV Etching by using two different etching recipes

	Process A	Process B
Mask	Single	Single
Etching gas	SF ₆ , O ₂	C ₄ F ₈ , SF ₆ , O ₂
Passivation gas	C ₄ F ₈	C ₄ F ₈
Etch profile
Roughness (nm)	107-129	68-75
Undercut (nm)	239	60

In Figure 3.2 and Figure 3.3, TSV with PETEOS liner as well as Low-K liner are fabricated with conformal step coverage. No void or delamination is observed in the Cu core after filling.

Figure 3.3 TSV having Cu as the core conductor with Low-K liner

3.2 Raman measurements

Mircon-scale characterization of mechanical stresses is essential for the successful design and operation of many micro-machined devices. Assessment of the reliability of TSV requires accurate characterization of mechanical stress. In this section, the measurements steps in my experiment are introduced.

3.2.1 Raman setting

Raman measurements used 442nm ion laser with 2400 I/mm grating. The Laser power applied on the sample surface is 1mW to avoid damaging the sample due to high energy. The integration time for every Raman spectrum capture is 5 seconds. Due to the central frequency of silicon is at 520.53 cm^{-1} in our case, the wavenumber range of the measurement was set to $500\sim 550\text{cm}^{-1}$. Figure 3.4 shows the schematic

Figure 3.4 Schematics and real view of sample for Raman measurements

Figure 3.5 Raman line scan along $[110]$ direction

and real view of our sample. Line scan is performed along Si [110] direction as Figure 3.5 indicated. The line scan step is 125nm.

The confocal micro-Raman system LabRam HR by Horiba Scientific was used for the Raman measurements (Figure 3.7), equipped with 442 nm Ar excitation laser and a focused spot size of about 0.8 μm by a 100 $\times$ objective (NA=0.9). The lateral

Figure 3.6 3D image of Raman line scan spectrum along [110] direction

Figure 3.7 The confocal Raman system used.

resolution of the Raman measurements also depends on the laser scanning step, which was about between 0.1 and 0.3 μm in present study. The penetration depth of the laser radiation is approximately 200 nm into silicon in my study [12].

Figure 3.8 shows a representative Raman spectrum. The signal-to-noise ratio were measured in order to determine the optimum laser power for the Raman measurements. In particular, the laser power was reduced by using filters to a level that heating of the Si (in principle visible as line shift and broadening) was below the detection limit. The suitable laser power density was set to be around 1 $\text{mW}/\mu\text{m}^2$. In

Figure 3.8 A representative Raman spectrum

Figure 3.6, the drop in the intensity of Raman signal indicates the locations of the Si/copper TSV interfaces. Close to the interface, the sum of the two principle stresses in Si can be deducted directly from the Raman frequency shift with equation(2.4).

3.3 Finite Element Analysis model

The stress in the TSV structures may result from both thermal and athermal contributions. However, the athermal contributions are typically process dependent, which are unknown for the TSV specimen in my study. To account for the athermal contributions, we take an empirical approach by assuming a reference temperature at which the TSV samples are stress free. The choose of the reference temperature are based on our sample fabrication temperature as Table 3-2 show [11].

Table 3-2 Reference temperature used in FEA simulation

Material	Low-K liner	Copper	PETEOS SiO ₂
Stress free temp[K]	650	500	700
Stress profile temp[K]	300	300	300

3.3.1 Analysis of near surface stress

As a semi-analytical approach, the stress field induced by differential thermal expansion around a circular via embedded in silicon wafer can be obtained approximately by the method of superposition. The result consists of a 2D plane-strain solution to the classical Lamé problem subjected to a thermal load (ΔT).

Table 3-3 Mechanical properties

Materials	Young's Modulus[Pa]	Poisson ratio	Density[Kg/m ³]	CTE[1/K]
Silicon	170e9	0.28	2329	2.6e-6
Copper	120e9	0.34	8960	16.5e-6
Low-K	4.2e9	0.3	1500	12e-6
PETEOS	70e9	0.17	2200	0.5e-6

Silicon is treated as isotropic in order to study the general stress distribution near surface. The material parameters, α , E , ν , are the coefficient of thermal expansion (CTE), Young's modulus and Poisson's ratio, respectively. The parameter of different materials are shown in Table 3-3. [13]

Clearly as Figure 3.9 shows, the σ_x and σ_y stresses in Si are dominant, while

Figure 3.9 Near surface stress around an isolated TSV predicted by COMSOL

the other stress components are negligibly small except for the locations very close to the TSV/Si interfaces. Thus, the stress state in Si is nearly biaxial within the depth of 200 nm. Moreover, the σ_x and σ_y stresses are in opposite signs with relatively high magnitudes near the TSV/Si interfaces and approaching zero far away from the via[8].

3.3.2 Anisotropic properties of Silicon

Monocrystalline silicon is the single material most widely used in semiconductor fabrication (Figure 3.10). Because the anisotropic properties of silicon, with elastic behavior depending on the orientation of the structure, choosing

Figure 3.10 Cubic crystal directions

appropriate value of E for silicon can appear to be a daunting task. However, the possible value of E for silicon ranges from 130 to 188 GPa and the choice of E value can have a significant influence on the result of design analysis. So it is meaningful for us to put into silicon anisotropic properties into our FEM simulation [14].

The elastic anisotropic components of Si is taken into account by employing the research results by Matthew A.Hopcroft, William D.Nix, and Thomas

Figure 3.11 Crystal direction of (100) wafer

Figure 3.12 Distributions of biaxial stress near surface (Depth=0.2μm)

W.Kenny[14, 15]. For the case of Figure 3.11, the orthotropic stiffness matrix for silicon with three axes at $[110]$, $[\bar{1}10]$, and $[001]$ is:

$$\begin{aligned} E_x &= E_y = 169 \text{ GPa} & E_z &= 130 \text{ GPa} \\ \nu_{yz} &= 0.36 & \nu_{xy} &= 0.064 & \nu_{zx} &= 0.28 \\ G_{yz} &= G_{zx} = 79.6 \text{ GPa} & G_{xy} &= 50.9 \text{ GPa} \end{aligned}$$

$$\begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \sigma_3 \\ \sigma_4 \\ \sigma_5 \\ \sigma_6 \end{bmatrix} = \begin{bmatrix} 194.5 & 35.7 & 64.1 & 0 & 0 & 0 \\ 35.7 & 194.5 & 64.1 & 0 & 0 & 0 \\ 64.1 & 64.1 & 165.7 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.6 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.6 & 0 \\ 0 & 0 & 0 & 0 & 0 & 50.9 \end{bmatrix} \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \varepsilon_3 \\ \varepsilon_4 \\ \varepsilon_5 \\ \varepsilon_6 \end{bmatrix} \quad (3.1)$$

The contour of the biaxial stress sum, $\sigma_x + \sigma_y$, calculated at the depth of 0.2 μm under the silicon surface are shown in Figure 3.12.

We can see from Figure 3.13, the biaxial stress in [100] direction is smaller than that of [110] direction. It is due to the more density atom arrangement in [110] direction than that of [100] direction.

Figure 3.13 Silicon anisotropic properties

4 Experiment results and discussion

4.1 Introduction

By using the method mentioned in Chapter 3, all of my experiments were done

Figure 4.1 The sample real image and its die map

based upon two kinds of samples. The two types of samples are completely same only except the liner materials, one is PETEOS silicon oxide and the other one is black diamond Low-K material (SiCO).

Figure 4.2 The area Raman line scan were performed

As Figure 4.2 shows, there are TSVs of different diameters range from 4 to 10 μm with an interval of 1 μm . The TSV array pitch is 2 or 3 times of the diameter.

4.2 Scaling of TSV diameter

4.2.1 Scaling of TSV diameter under compressive stress

Based on the ITRS road map 2011, the greater accessibility of higher number of TSVs in a specified area depends on the smarter miniaturization of the interconnect dimension in 3D IC packaging. Of course, scaling of TSV dimension has an inevitable effect on resistance, capacitance, signal transport as well as the thermo-mechanical stress issue. We find that the lowering of TSV diameter is permissible

under thermo-mechanical stress issue, however, the signal transmission delay could be tunable via controlling the oxide layer capacitance to the lower end.

4.2.2 Stress measurement

The single Cu filled TSV with liner separation has been demonstrated as shown in Figure 4.3. The use of liner material in TSV interconnection technology has some implications. Firstly its role is to minimize the leakage current and secondly to consider as an annular material to absorb the stress under thermal treatment [15]. However it has an adverse effect to create the capacitance to make delaying the signal transmission. At the annealing process of Cu-TSV, we have observed that the Si-surface is under strong compressive stress at the closer vicinity of the TSV holes and that exponentially decreasing up to a certain distance of 1 μm from the TSV periphery and finally becomes almost constant until next of TSV. Similar observation has also

Figure 4.3 (a) The Model for Cu-filled TSV with oxide liner, we have used Eq. (1) & (2) to calculate resistance (R) and capacitance (Cox). (b) Represents the cross-sectional view of the real image of Cu-TSV.

reported by A.D. Trigg et. al. in their recent report[16]. This is due to the fact that high temperature annealing step initiates the grain growth inside the Cu pillar [17].

The μ -Raman analysis (directly refer to the stress measurement with the significant change in Raman peak shifting, considering the Si transverse optical phonon peak generally appears at 520.53 cm^{-1}) clearly reveal that the higher the TSV diameter, the higher will be the compressive stress at the closer vicinity of TSV; such as for $10\mu\text{m}$ TSV diameter the maximum stress experienced is 220 MPa , where as that of for $8, 6$ and $4\mu\text{m}$ are 123MPa , 105MPa and 85MPa , respectively (Shown in Figure 4.4a). This is due to the low Cu content for low diameter TSV, which results to lower stress accumulated for low diameter TSV as the stress originates due to the large difference in CTE value for Cu and Si. Interestingly our simulation study under finite element analysis (FEA) is nearly collinear with the experimental findings as well (Shown in Figure 4.4b). Thus for the increasing emphasis on miniaturization of modern packaging technology with 3D TSV array interconnection, it is safer to scaling down TSV diameter below $5\mu\text{m}$ to minimize the thermal stress issue.

Figure 4.4 (a) Represent the thermo-mechanical stress distribution for 4 to $10\mu\text{m}$ TSVs (b) The corresponding simulation curves.

4.2.3 Electrical characterization modeling

In the event of safer tuning of TSV diameter, we need to consider or verify another important aspect of change in resistance (R), capacitance (C) and their product such as the time delay (τ) with the lowering of TSV diameter. It is quite obvious that the successive scaling down of TSV diameter certainly reflect its exponential increase of resistance; however we have observed that the variation of capacitance due to oxide liner with TSV scaling strongly depends upon the liner thickness vs TSV diameter (Figure 4.5).

Figure 4.5 C-V plots for constant ratio and constant liner thickness mode for 50, 25 & 10 μm TSV length. The shaded area represents the lowest possible C_{ox} value for 50 μm TSV at any radius range from 0.5 to 10 μm .

Capacitance-Voltage (CV) measurements were taken keeping either constant liner thickness (200 nm) regardless of scaling down the TSV diameter or fixing the ratio of TSV radius (including liner thickness, r_1) vs copper pillar radius (r_0).

Decreasing the TSV radius from 10 to 0.5 μm , there is a constant value of capacitance while we go ahead with the fixing ratio mode (liner thickness is 4% of TSV diameter).

Figure 4.6 The plot represents the change of R and lowest possible C value with the scaling of TSV radius. The R increases exponentially at lower TSV radius while the C is constant at fixed ratio mode up to 2.5 μm and below decreases linearly with constant liner thickness mode.

However that is for constant liner thickness mode the capacitance is steadily decreased. These two curves cut at a point where the TSV radius is 2.5 μm . Thus to get lower capacitance, we should proceed with fixing ratio mode for TSV radius above 2.5 μm ; in contrast TSV radius below 2.5 μm we could safely follow constant liner thickness mode. This interesting trend has been verified for 50, 25 and even 10 μm TSV lengths. Thus it is understandable that with scaling down of Cu filled TSV diameter, the resistance is exponentially over shoot and in contrast capacitance can be restricted to constant value up to a certain lowering of TSV radius (up to 2.5 μm) and next linearly decreases with further scale down (Figure 4.6). Thus we may have a better control over the delay time (i.e the product of R and Cox) to the lower proximal limit with scaling down of TSV diameter, described in Figure 4.7.

We have demonstrated the safest way of scaling down the Cu filled TSV diameter up to the lowest limit of ITRS guide line ($4\mu\text{m}$). Our study shows that the lowering of TSV diameter is favourable under thermo-mechanical stress issue due to lesser content of Cu inside the TSV channel. However the exponential up facing resistance part could possibly be compensated via lowering capacitance influence at a fixed liner thickness (200nm) below $2.5\mu\text{m}$ TSV radius to minimize the delay in signal transmission.

Figure 4.7 The plots show the lowering of the R.C product (delay) at constant ratio mode ($>2.5\mu\text{m}$) and constant liner thickness more ($2.5\mu\text{m}<$). For example we consider yellow shaded region to get low capacitance value for $50\mu\text{m}$ TSV length.

4.3 Raman experiment data processing

With plasma excitation, high deposition rates are obtained at temperatures of $300\text{--}450\text{ C}^\circ$ from TEOS / oxygen. In single-wafer reactors rates of $5000\text{--}10,000\text{ \AA}/\text{min}$

can be achieved, using pressures around 6-10 Torr and very small electrode gaps (<6 mm). The problems encountered in thermal TEOS/ozone deposition (water absorption, stress, cracking) are also present in plasma-deposited films, but the availability of the plasma allows improved flexibility in dealing with them. Increasing RF power, increasing pressure while decreasing electrode gap, and increasing the oxygen/TEOS ratio, all help produce films which are "dry" and stable in air. Plasma TEOS films are often used to encapsulate thermal TEOS-ozone oxide or spin-on glass, to protect it from ambient moisture. A PETEOS underlayer has better step coverage ability than plasma-enhanced silane films, so the thermal or SOG oxide has an easier task filling trenches or holes with a PETEOS underlayer. However, PETEOS is a relatively poor moisture barrier, and thus conformality and reliability impact must be balanced.

4.3.1 PETEOS liner sample

Figure 4.8 is a collection of Raman spectras along a TSV row of 5 μm diameter with a pitch of 15 μm . The x -axis is the Raman frequency ranges from 500 cm^{-1} to 550 cm^{-1} . The y -axis stand for the Raman laser scan line. Raman shift

Figure 4.8 Raw data from Raman spectroscopy along TSV row as shown in Figure 4.2. The wave number is taken from 500 to 550 cm^{-1} .

originated from the Si-Si peak is then translated into biaxial stress as presented in Figure 4.9

In order to see the effects of diameter change on stress distribution, The data in Figure 4.9 were compile into one graph (Figure 4.10). The larger the diameter of TSV, the larger the thermal coefficient mismatch caused stress.

Figure 4.9 Stress distribution between two TSVs. From (a) to (f), the TSV diameter changes from 4 μ m to 9 μ m, and the pitch is 3 times of diameter.

Figure 4.10 Biaxial stress of PETEOS liner TSV sample.

4.3.2 Low- κ material liner sample

The Black Diamond II nano-porous low- κ film is the industry standard for the 45/32nm copper/low- κ interconnects, with a κ -value of approximately 2.5. Its predecessor, Black Diamond ($\kappa \sim 3.0$), is the industry-standard for the 90/65nm nodes. Creating nano-porous low- κ film is a two-step process consisting of PECVD deposition of an organosilicate glass “backbone” and a thermally labile organic phase, followed by an ultraviolet (UV) cure that removes the labile phase, thereby inducing porosity, and restructures and strengthens the remaining silicon-oxide matrix to form the final nano-porous film. Small average pore size and tight pore size distribution

Figure 4.11 Stress distribution between two TSVs. From (a) to (f), the TSV diameter changes from 4 um to 9 um, and the pitch is 3 times of diameter.

eliminate the need for pore sealing.

The Raman shift is translated into biaxial stress according to formula (2.4) as shown in Figure 4.11.

4.4 Thermal mechanical stress mitigation

Two-dimensional (2D) finite element analysis on Cu and dielectric liner interconnection structures have shown that the triaxial tensile stress in Cu significantly arises due to stiff barrier layers surrounding the Cu line.[18, 19] This stress is transmitted to the peripheral Si crossing through the liner barrier. Thus, the use of a softer liner with a higher compliance in principle imparts a lower stress on Si. Simulation on a poly (p-xylylene-type organo polymeric compound [15] commonly known as parylene, Young's modulus of 4 GPa) as a liner material in a TSV interconnection shows that it could relieve the thermal stress distribution in Si by 75 MPa. Theoretical postulation reveals that the incorporation of a low- κ dielectric (carbon-doped oxide, SiOC) in place of a traditional oxide-based dielectric significantly reduces the triaxial tensile stresses in Cu, but enhances plastic deformation, particularly in the via and its vicinity.[20] SiOC is commonly known as carbon-doped porous silica where the average porosity is in the range of 1-3 nm.[21, 22] Therefore, the application of SiOC as a liner material for TSV could potentially alleviate the thermal stress. There is limited experimental evidence of the buffering of the thermal mechanical stress effect on Si by using low- κ SiOC as the liner material in TSV. Owing to a low Young's modulus of 4.2 GPa for the low- κ dielectric as compared with 70 GPa for conventional plasma-enhanced tetraethylorthosilicate (PETEOS) dielectric, a significantly lower transmission of thermal stress to the Si

bulk at the close vicinity of Cu-TSV is expected. μ -Raman spectroscopy with high-groove-density (2400 gr/mm) diffraction grating was used and resulted in a high spectral resolution of $0.3 \text{ cm}^{-1}/\text{pixel}$ for the 442 nm laser source. Lorentzian peak fitting was then used to further refine the resolution to 0.03 cm^{-1} which corresponds to the stress sensitivity level of 15 MPa.

A 3D finite element analysis (FEA) model was constructed to determine the thermal stress distribution in the TSV samples. The material physical properties used in this simulation are summarized in Table 3-3.

Figure 4.12 Von Mises stress distribution

The model consists of TSV with $10 \text{ }\mu\text{m}$ diameter, $30 \text{ }\mu\text{m}$ pitch, and $10 \text{ }\mu\text{m}$ depth on the Si (100) surface. The conformal 200 nm oxide liner and Cu filling in the TSVs were also taken into account. A thermal load from the reference temperature ($200 \text{ }^{\circ}\text{C}$, assumed to be stress-free) to room temperature ($25 \text{ }^{\circ}\text{C}$) of $\Delta T=175 \text{ }^{\circ}\text{C}$ was

considered. For simplicity, a liner elastic and isotropic model was assumed to obtain a first-order intuition. As a result of the thermal load during cooling, the Cu core tended to contract at a higher rate than that of Si due to the larger CTE of Cu. Since Cu was confined in the TSV, thermal mechanical stress was induced and exerted on the surrounding Si. In reality, such near surface stresses could possibly be estimated via μ -Raman analysis using a 442 nm laser line with an approximate penetration depth of 200 nm into the Si surface. The stress state in the Si surface was considered to be nearly biaxial at this depth. Thus, the biaxial stress profile was extracted at a depth of 200 nm from the above simulation.

The effect of a dielectric liner on the Si stress distribution at the close vicinity of TSV interconnection was carefully studied by μ -Raman spectroscopy and is shown in Figure 4.13(a). It was observed that for a TSV structure with a similar diameter, the near-surface stress in Si surrounding the Cu-TSV decreased substantially when a low-

Figure 4.13 (a) Thermal mechanical stress distribution as a function of distance from the TSV edge (diameter: 6, 8, and 10 μm) with PETEOS and low-K dielectric liners. (b) Comparison of the stress profile of FEA simulation against experimental results for 10 μm -diameter TSV having PETEOS or Low-K liner.

κ liner is used rather than the PETEOS liner. At the immediate vicinity of the Si/TSV interface, the compressive stress decreased from 221 MPa (PETEOS liner) to 122MPa (low- κ liner) for the 10 μ m TSV diameter. A similar trend was also observed for 8 μ m TSV (stress decreased from ~123 to ~192MPa) and 6 μ m TSV (stress decreased from ~106 to ~59 MPa) samples. Hence, the low- κ liner can reduce the compressive stress near the TSV surrounding by 29 to 45%, compared with the PETEOS counterpart for the TSV diameter presented above. Thus, it can be concluded that under our experimental conditions, the observed thermal mechanical stress relief with a Low- κ should be attributed to the lower Young's modulus of 4.2 GPa and higher porosity than those of the PETEOS liner. The lower Young's modulus and higher porosity of the low- κ liner make it more compliant as a buffer layer to cushion the stress exerted by Cu-TSV on the surrounding Si.

Figure 4.13(b) illustrates a comparison of the stress profile between FEA simulation and Raman results for TSV having a diameter/pitch of 10/30 μ m using low- κ and PETEOS liners, respectively. Despite some discrepancies in the actual stress values, the FEA results predict characteristics similar to the experimental findings. In both cases, the stress profile is shown between two adjacent TSVs. Both methods reveal that the compressive stress is concentrated around the TSV, with the highest value at the immediate TSV edge and the stress tapers off rapidly with distance from the TSV edge. The FEA data reaffirm the Raman findings that a low- κ liner, due to its lower elastic modulus, acts as an effective buffer layer that reduces the thermal mechanical stress in Si surrounding the TSV. Reduction in stress in Si is beneficial as it improves the overall reliability of TSV integration and minimizes the device variability due to stress-induced mobility change. This will relax the

requirements for the keep-out zone (KOZ), which is critically important for density consideration in actual application.

The current results demonstrate that the miniaturization of the TSV dimension is not the only way to reduce the thermal mechanical stress in Si surrounding the TSV structure due to the lower Cu volume. It is also possible to control the stress level via the selection of a suitable liner material with a lower elastic modulus. The interesting findings can be attributed to the fact that the choice of a lower Young's modulus and a porous dielectric liner material could effectively reduce the compressive near surface stress in Si by 29 – 45% compared with the conventional liner such as PETEOS which is more rigid. In addition, an earlier report has shown that the integration of a low- κ material as a TSV liner could lead to a 28% reduction in the capacitance [11].

4.5 TSV keep-out-zone

Through silicon via (TSV) has emerged as an essential enabler for the next generation of integrated circuits and systems for continuous performance growth and

Figure 4.14 The thermal stress in Silicon as measured by μ -Raman spectroscopy along the [110] and [100] direction.

functional diversification. TSV is commonly fabricated by high aspect ratio deep silicon etching, lining with dielectric materials for electrical isolation and super-conformal filing with copper to provide the electrical path. Due to the large CTE mismatch between Si ($\sim 2.5 \times 10^{-6} \text{K}^{-1}$) and Cu ($\sim 17.5 \times 10^{-6} \text{K}^{-1}$), large thermo-mechanical stress is induced in the Si which causes carrier mobility variation. Silicon is an anisotropic crystalline material whose material properties depend on orientation relative to the crystal lattice. The dependency of the keep-out zone (KOZ) on crystal direction ([110], [100]) were studied in this section. The four curves in Figure 4.14 is measured by Raman spectroscopy along two silicon crystal direction [100] and [110]. The difference between the two directions reveal the anisotropic properties of silicon, and from the curve we can conclude that by using a more elastic low- κ material as the liner we can mitigate the thermal stress round the TSV.

The μ -Raman analysis (directly refer to the stress measurement with the significant change in Raman peak shifting, considering the Si transverse optical phonon peak generally appears at 520.53 cm^{-1}) were taken along the [100] and [110] of Si crystal direction. The near surface stress in silicon is biaxial. Figure 4.14 clearly reveal the anisotropic properties of Silicon, it is consistent with previous publications. In samples that employ silicon oxide (Young's modulus $\sim 75 \text{ GPa}$) as the liner material, the maximum biaxial stress in the [110] direction is about 210 MPa while that in the [100] direction is just about 110 MPa. Figure 4.14 also shows that the thermal stress around the TSV can be controlled by using a more elastic low- κ SiOC ($\sim 7.2 \text{ GPa}$) material as the liner.

4.5.1 Comparison of mobility variation between hole and electron

Two types of device channel direction were investigated, i.e. the current flow direction are along the [100] and [110] directions. The thermal stress were computed by finite element analysis software COMSOL[®] on (001) silicon with a thermal load of $\Delta T = -200\text{ }^{\circ}\text{C}$. After the simulation, the stress obtained from COMSOL will be coupled to carrier mobility change by using equation $\Delta u / u = \Pi_L \sigma_L + \Pi_T \sigma_T$. The piezoresistivity coefficients are shown in Table 4-1.

Table 4-1 Piezoresistivity coefficients for holes and electrons in [110] and [100] direction

Silicon Crystal Direction	(100) Wafer [110] Direction		(100) Wafer [100] Direction	
Piezoresistivity Coefficient	$\Pi_L (E^{-11}/Pa)$	$\Pi_T (E^{-11}/Pa)$	$\Pi_L (E^{-11}/Pa)$	$\Pi_T (E^{-11}/Pa)$
Electrons	-31.6	-17.6	-102	53.4
Holes	71.8	-66.3	6.6	-1.1

To evaluate the size of the keep-out-zone (KOZ), the absolute change in the value of mobility is taken into consideration. The KOZ is determined by the area with

Figure 4.15 Contour of the mobility change for (a) hole and (b) electron with the electric field and current density in [100] direction. The magenta lines indicate the 5% mobility change ($\phi = 5 \mu\text{m}$, and $\Delta T = -200 \text{ }^\circ\text{C}$, $b=3.157\mu\text{m}$ for electron).

a change of channel carrier mobility for more than 5% [24]. To define the KOZ, the characteristic distances between TSV edge and KOZ boundary are calculated and noted as d_T , d_L and b . Figure 4.15 is the case of channel direction that aligns with the [100] direction, the mobility change is orientation dependent. In Figure 4.15(b) the

boundary of the KOZ is marked by the magenta solid line. In contrast to electrons in Figure 4.15(b), the holes mobility change does not exceed 5% as shown in Figure 4.15(a).

Figure 4.16 is the case of channel direction that aligns with the [110] direction. Holes mobility variation (Figure 4.16b) is much larger than that of electrons when the current flow is in the [110] direction. Therefore, as Silicon devices are subjected to

Figure 4.16 Contour of the mobility change for (a) holes and (b) electrons when current flows in the [110] direction. The magenta lines indicate the 5% mobility change ($\phi = 5 \mu\text{m}$, and $\Delta T = -200 \text{ }^\circ\text{C}$, $d_T = 2.157 \mu\text{m}$, $d_L = 2.188 \mu\text{m}$, $b = 1.282 \mu\text{m}$ for hole).

same thermal load, to get a smaller KOZ map, the p-MOSFETs can be fabricated with channel direction aligned to the [100] direction, while for n-MOSFETs the channel direction can be aligned in the [110] direction.

4.5.2 TSV liner materials effects on KOZ map

Figure 4.17 The mobility variation contour for holes with current flow along the [110] direction for (a) Silicon oxide and (b) Low-κ SiOC as the liner material. The difference caused by using low-κ and silicon oxide as liner materials are expressed in terms of the distance from TSV edge: d_T , d_L in [110] direction and b in [100] direction.

Two types of TSV samples (silicon oxide or low- κ SiOC liners) are investigated. Both Figure 4.17(a) and Figure 4.17(b) show the holes mobility change contour with the current flow in the [110] direction. The boundary of the KOZ is marked by the magenta solid line. We extract the characteristic distances shown in Figure 4.17 and plot them in Figure 4.18, it is clearly shown that one can reduce the KOZ size by using a more elastic low- κ SiOC as the liner material.

Figure 4.18 Comparison of characteristic distances by using silicon oxide or low- κ as the liner material. It clearly shows that more elastic liner material can reduce the KOZ size.

The effect of thermal stress induced by copper TSV on carrier mobility change has been investigated. And it provide two ways to reduce the size of keep-out-zone for n-MOSFETs and p-MOSFETs. The p-MOSFETs should be fabricated with [100] alignment while for n-MOSFETs the channel direction should be in [110] direction. And also we find by using a more elastic liner materials we can mitigate the thermal stress around TSV and thus reduce the size of KOZ.

5 Conclusions

5.1 Conclusions

In this project, micro-Raman system LabRam HR by Horiba Scientific was set up for stress measurements. The Raman measurement mentioned in this report is a straightforward but tedious process. During the line scanning, sometimes, the sample shift entirely, which is caused by the movement of the sample platform driven by motor. Sometimes, the scan line deviated from the centre of the TSV circle, so it needed three or more scans to get the best data for one type of TSV. And the resolution of our Raman system is $\sim 0.3\text{cm}^{-1}$, so we need to do peak fitting for the raw data to reach a higher resolution of $\sim 0.03\text{cm}^{-1}$. Our experiment results were also verified by FEM simulation software COMSOL[®], the results were shown in Chapter 4. The objectives of the project is to investigate the coefficient of thermal mismatch (CTE) between silicon and copper TSV caused stress evolution while scaling of TSVs, and also we find that by using a more elastic low- κ material can not only reduce the parasitic capacitance but also mitigate the thermal stress around TSV. The effect of thermal stress induced by copper TSV on carrier mobility change has been investigated. And we provide two ways to reduce the size of keep-out-zone for n-MOSFETs and p-MOSFETs. The p-MOSFETs should be fabricated with [100] alignment while for n-MOSFETs the channel direction should be in [110] direction. And also we find by using a more elastic liner materials we can mitigate the thermal stress around TSV and thus reduce the size of KOZ.

5.2 Research contributions

The research contributions are summarized as follows:

- a) Investigation of the changes of thermal stress and electrical effects along TSV scaling. Demonstrate the safest way of scaling down the Cu filled TSV diameter up to the lowest limit of ITRS guide line (4 μm). Our study shows that the lowering of TSV diameter is favourable under thermo-mechanical stress issue due to lesser content of Cu.
- b) Study of two types of TSV samples with PETEOS and Low- κ as the liner materials revealed that the miniaturization of the TSV dimension is not the only way to reduce the thermal mechanical stress in Si surrounding the TSV structure due to the lower Cu volume. It is also possible to control the stress level via the selection of a suitable liner material with a lower elastic modulus. The interesting findings can be attributed to the fact that the choice of a lower Young's modulus and a porous dielectric liner material could effectively reduce the near surface stress.
- c) Finite element analysis applied the anisotropic properties of silicon. Plotted the TSV Keep-out-zone map. The effect of thermal stress induced by copper TSV on carrier mobility change has been investigated. And it provide two ways to reduce the size of keep-out-zone for n-MOSFETs and p-MOSFETs. The p-MOSFETs should be fabricated with [100] alignment while for n-MOSFETs the channel direction should be in [110] direction.
- d) Lorentzian peak fitting algorithm was developed and successfully improved the Raman measurement resolution from 0.3 cm^{-1} to 0.03 cm^{-1} .

5.3 Proposal for future work

There is not much meaning if we only talk about stress, as the other literature reported that the stresses around TSVs may degrade the performance of nearby devices through the piezoresistivity effect [23]. As the keep-out-zone maps in my project were only plotted based upon simulation results, we should couple our stress map to electrons/holes mobility change by using experimental data, and plot the keep away zone based on the percentage of mobility change. The Raman laser scan should not only cover the distance between the two TSVs. We should cover also the outside area so as to examine the area of impact and see if this area of impact will increase with temperature cycle. If there is any crack occurs, the stress near the vicinity will have a dip and a peak due to stress concentration at the tip of the crack. How big the area is to be determined by experiments.

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Appendix I

Publication List:

1. Ghosh, K.Z., Jiye Zhang, Lin Dong, Yuanwei Li, Hongyu Tan, Cher Ming Xia, Guangrui Tan, Chuan Seng, Integration of Low-K Dielectric Liner in Through Silicon Via and Thermomechanical Stress Relief. *Applied Physics Express*, 2012. 5.
2. J. Zhang, K. Ghosh, L. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "TSV Scaling with Constant Liner Thickness and the Related Implications on Thermo-mechanical Stress, Capacitance, and Leakage Current," International Conference on Solid State Devices and Materials (SSDM), Kyoto, Japan, September 25-27, 2012.
3. K. Ghosh, J. Zhang, L. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "Strategy for TSV Scaling with Consideration on Thermo-mechanical Stress and Acceptable Delay," International Microsystems, Packaging, Assembly Circuits Technology Conference (IMPACT), Taipei, Taiwan, October 24-26, 2012.
4. J. Zhang, L. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "The dependency of TSV keep-out zone (KOZ) on Si crystal direction and liner material", Nanyang Technological University; Singapore, Institute of Microelectronics, A*STAR, Singapore, and University of British Columbia, Canada