Design of CMOS 60GHz Giga-bps communication system with CRLH T-line for high output power density and wide tuning range

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

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Communication System with CRLH T-line
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School of Electrical & Electronic Engineering

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Summary

Thanks to advanced scaling of CMOS technology, the operating speed and cut-off frequency of CMOS transistor steadily keeps growing more than 10 times and approaches to the millimeter-wave (mm-wave) region (60GHz – 140GHz @ 65nm node). Compared with III-V technologies, CMOS has the benefit of high integration and low cost, and therefore draws extensive research attention for system-on-chip implementation. Recently, substantial research activities about the wide frequency bands at 60 GHz and beyond have been accumulated to develop the next generation high-data-rate (>Giga-bps) wireless terminals in CMOS such as Wireless-HD, WiGiga for high-definition TV, projector and screen. Along with the new opportunities, there are also new challenges in design of CMOS mm-wave high-data-rate communication system. For example, one needs to achieve sufficient output power to cover the high path loss at mm-wave frequencies; and also to achieve wide tuning range to cover the large spectrum for high-data-rate communication. However, these features are constraint by advanced CMOS technologies at mm-wave frequencies with low supply and breakdown voltages and large PVT variation. For example, one fundamental block for mm-wave IC design, transmission line (T-line), has fundamental limitations on circuit performance due to the traditional right-handed (RH) topology.

This work provides design analysis as well as on-chip demonstration to resolve the aforementioned design challenges for mm-wave integrated circuit (IC) design in CMOS technology. A transformation of mm-wave IC design with the use of metamaterial is mainly explored in this work. Metamaterial is not a new type of material, but a periodic unit-cell structure that can be implemented on-chip in common CMOS technologies. The unique feature of the metamaterial is to provide nonlinear negative phase shift that can be realized in compact area, which can be utilized for high efficiency output power combining as well as wide frequency tuning. Based on this observation, we have explored the application of on-chip metamaterial for two critical blocks in 60GHz high-data-rate communication system: power amplifier (PA) and voltage controlled oscillator (VCO).

For PA design, the target is to improve the output power density and bandwidth performance. With the use of one type of metamaterial transmission line (T-line), composite-right-left-handed (CRLH) T-line, a new 2D distributed in-phase power combining network is developed to provide distributed amplification and power combining within compact area simultaneously. As such, one can achieve high output power, high output power density and wide-band performance for CMOS 60GHz PA and transmitter, which are realized as follows:

- One 60GHz PA prototype with single-ended 2×2 power combining was first fabricated in UMC CMOS 65nm technology. Measured results show 8.3dB gain, 7.1% PAE, and 9.7dBm P1dB with 16GHz bandwidth (44 to 60GHz) and area of 0.39mm^2 . This work was further improved to have a differential topology with compact transformer matching, and was implemented in GF CMOS 65nm technology.
- Two 60GHz PA prototypes with differential 2×4 and 4×4 power combining were demonstrated. The measured results show state-of-art performance, with 13.2 dB gain, 8.7% PAE, 20GHz bandwidth (53 to 73GHz) and 13dBm output power with 74.5mw/mm^2 output power density for the 2×4 PA; and 17.5dB gain, peak PAE of 11.3%, 8.8GHz bandwidth (54 to 62.8GHz), and 16.6dBm output power with 95.2mw/mm^2 output power density for the 4×4 PA.
- Based on the above chip realization and verification, one 60GHz direct-conversion transmitter with the proposed 2×4 power combining was implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level.

For VCO design, the target is to improve frequency tuning range (FTR) with maintained low phase noise performance. One inductive tuning method is first proposed based on configuration of current return paths in the secondary coil of a transformer. Different from previous inductive tuning methods, the proposed VCO topology can achieve wide FTR for multiple sub-bands at 60GHz within compact area by only one transformer. Furthermore, a distributed CRLH T-line based VCO is designed in a Mobius-ring rotary-traveling-wave (RTW) topology to further improve FTR. RTW VCO is commonly adopted due to its advantages such as easy

placement of cross-coupled transistors, good matching of differential blocks and compact area. Based on inductive tuning, a tunable CRLH T-line is proposed. Because of the nonlinear dependence of phase-change with frequency, wide FTR mechanism can be achieved for RTW VCO in millimeter-wave region. The CRLH T-line is implemented in RTW-VCO with inductor-loaded transformer to realize sub-band selection over a wide FTR. Each sub-band is further covered by a varactor for fine-tuning. As such, one can achieve wide FTR with low phase noise in each sub-band for CMOS 60GHz VCO and PLL, which are realized as follows:

- Two 60GHz VCOs were demonstrated in 65nm CMOS with design targets for the maximum FTR and the balanced phase noise in each sub-band, respectively. As measured by experiments, the first VCO (asymmetric) achieves a wide FTR of 25.8% from 51.9 to 67.3GHz with phase noise variation of $\pm 8.2\text{dB}$ (-90.2 to -106.7dBc/Hz at 10MHz offset) in all sub-bands; and the second VCO (symmetric) realizes a low phase noise variation of $\pm 2.5\text{dB}$ (-105.9 to -110.8dBc/Hz at 10MHz offset) in all sub-bands with a FTR of 14.2% from 57.0 GHz to 65.5 GHz.
- The third RTW VCO chip was fabricated in GF 65nm RF-CMOS technology with area of 0.08mm^2 . The measured results show a current consumption of 14mA under supply voltage of 1V, a tuning range of 29.5% with center frequency at 89.3GHz, and a phase noise from -100.1dBc/Hz to -98.7dBc/Hz with 10MHz offset. A state-of-art figure-of-merit FOM_T of -177.78dBc/Hz is demonstrated.
- Based on the above chip realization and verification, one 60GHz PLL with the proposed symmetric inductive tuned VCO was implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level.

Chapter 1

Introduction

1.1 Motivation

Thanks to advanced scaling of CMOS technology, the operating speed and cut-off frequency of CMOS transistor steadily keeps growing more than 10 times and approaches to the millimeter-wave (mm-wave) region (60GHz – 140GHz @ 65nm node). Compared with III-V technologies, CMOS has the benefit of high integration and low cost, and therefore draws extensive research attention for system-on-chip implementation. Recently, substantial research activities about the wide frequency bands at 60 GHz and beyond have been accumulated to develop the next generation high-data-rate (>Giga-bps) wireless terminals in CMOS such as Wireless home network [1, 2], WiGiga [3-5] and Wireless-HD [6, 7] for high-definition TV, projector and screen.

Figure 1.1 Ultra-broadband wireless home network with the use of 60GHz high-data-rate wireless communication. [2]

For example, one ultra-broadband wireless home network architecture is shown in Fig. 1.1. With optical fiber backbone to transport data with ultra bandwidth, 60GHz high-data-rate wireless terminals at access points in each room can connect all electronic devices together, replacing various cables used today in the office or home, including gigabit Ethernet (1000 Mbps), USB 2.0 (480 Mbps), or IEEE 1394 (~800 Mbps) [1]. Smart house application may also be provided with a high data rate 60GHz wireless network controller.

Figure 1.2 *High-definition multimedia interface (HDMI) provided by WiGiga and Wireless-HD [3].*

Figure 1.2 shows another application of 60GHz high-data-rate wireless communication to provide high-definition multimedia interface (HDMI), where secure, uncompressed high-definition video distribution can be achieved wirelessly and in real time [3]. Furthermore, beamforming can also be supported by WiGiga and Wireless-HD to compensate the high path loss and establish alternative communication pathways when being blocked by an obstacle, such as through reflection from a wall [3, 8]. WiGiga can support data rate up to 7Gbps and forms the basis for IEEE 802.11ad standard [3]. Wireless-HD can support data rate of 10-28 Gbps [6].

Along with the new opportunities, there are also new challenges in design of CMOS mm-wave high-data-rate communication system. For example, one needs to achieve sufficient output power to cover the high path loss at mm-wave

frequencies; and also to achieve wide tuning range to cover the large spectrum for high-data-rate communication. Figure 1.3 shows the frequency allocation plan by IEEE 802.11.ad standard, where a wide spectrum of 5~9GHz is required with maintained high output power and linearity [9]. However, these features are constraint by advanced CMOS technologies at mm-wave frequencies with low supply and breakdown voltages and large Process-Voltage-Temperature (PVT) variation. What is worse, one fundamental block for mm-wave integrated circuit (IC) design, transmission line (T-line), is shown in Chapter 2 to pose fundamental limitations on circuit performance with the traditional right-handed (RH) topology.

Figure 1.3 60GHz Band Channel Plan and Frequency Allocations by Region [9].

On the other hand, as frequency pushes up into mm-wave region and transistor size shrinks down to below 100nm, previously ignored parasitic and secondary effects become much more pronounced and can no longer be ignored. A direct consequence is that many existing topologies and techniques for low frequency application no longer function properly. At the same time, high frequency leads to much more compact size for passive devices and active device density improves greatly due to advanced technologies. Therefore, devices and topologies which were previously too bulky to be implemented on chip can now be re-explored. A new realm with challenge and opportunity is open for mm-wave and beyond, where new techniques and circuit topologies should be explored.

1.2 Research Objective and Major Contributions

This work provides design analysis as well as on-chip demonstration to resolve the aforementioned design challenges for mm-wave integrated circuit (IC) design in CMOS technology. A transformation of mm-wave IC design with the use of metamaterial is mainly explored in this work. Metamaterial is not a new type of material, but a periodic unit-cell structure that can be implemented on-chip in common CMOS technologies. The unique feature of the metamaterial is to provide nonlinear negative phase shift that can be realized in compact area, which can be used to resolve the fundamental limitations from the conventional right-handed (RH) transmission line (T-line) commonly employed in high frequency design. Based on this observation, we have explored the application of on-chip metamaterial for two critical blocks in 60GHz high-data-rate communication system: power amplifier (PA) and voltage controlled oscillator (VCO).

For PA design, the target is to improve the output power density and bandwidth performance. With the use of one type of metamaterial transmission line (T-line), composite-right-left-handed (CRLH) T-line, a new 2D distributed in-phase power combining network is developed to provide distributed amplification and power combining within compact area simultaneously. As such, one can achieve high output power, high output power density and wide-band performance for CMOS 60GHz PA and transmitter, which are realized as follows:

- One 60GHz PA prototype with single-ended 2×2 power combining was first fabricated in UMC CMOS 65nm technology. Measured results show 8.3dB gain, 7.1% PAE, and 9.7dBm OP_{1dB} with 16GHz bandwidth (44 to 60GHz) and area of 0.39mm^2 . This work was further improved to have a differential topology with compact transformer matching, and was implemented in GF CMOS 65nm technology.
- Two 60GHz PA prototypes with differential 2×4 and 4×4 power combining were demonstrated. The measured results show state-of-art performance, with 13.2 dB gain, 8.7% PAE, 20GHz bandwidth (53 to 73GHz) and 13dBm output power with 74.5mw/mm^2 output power density for the 2×4 PA; and 17.5dB gain, peak PAE of 11.3%, 8.8GHz

bandwidth (54 to 62.8GHz), and 16.6dBm output power with 95.2mw/mm² output power density for the 4×4 PA.

- Based on the above chip realization and verification, one 60GHz direct-conversion transmitter with the proposed 2x4 power combining was implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level.

For VCO design, the target is to improve frequency tuning range (FTR) with maintained low phase noise performance. One inductive tuning method is first proposed based on configuration of current return paths in the secondary coil of a transformer. Different from previous inductive tuning methods, the proposed VCO topology can achieve wide FTR for multiple sub-bands at 60GHz within compact area by only one transformer. Furthermore, a distributed CRLH T-line based VCO is designed in a Mobius-ring rotary-traveling-wave (RTW) topology to further improve FTR. RTW VCO is commonly adopted due to its advantages such as easy placement of cross-coupled transistors, good matching of differential blocks and compact area. Based on inductive tuning, a tunable CRLH T-line is proposed. Because of the nonlinear dependence of phase-change with frequency, wide FTR mechanism can be achieved for RTW VCO in millimeter-wave region. The CRLH T-line is implemented in RTW-VCO with inductor-loaded transformer to realize sub-band selection over a wide FTR. Each sub-band is further covered by a varactor for fine-tuning. As such, one can achieve wide FTR with low phase noise in each sub-band for CMOS 60GHz VCO and PLL, which are realized as follows:

- Two 60GHz VCOs were demonstrated in 65nm CMOS with design targets for the maximum FTR and the balanced phase noise in each sub-band, respectively. As measured by experiments, the first VCO (asymmetric) achieves a wide FTR of 25.8% from 51.9 to 67.3GHz with phase noise variation of ± 8.2 dB (-90.2 to -106.7dBc/Hz at 10MHz offset) in all sub-bands; and the second VCO (symmetric) realizes a low phase noise variation of ± 2.5 dB (-105.9 to -110.8dBc/Hz at 10MHz offset) in all sub-bands with a FTR of 14.2% from 57.0 GHz to 65.5 GHz.
- The third RTW VCO chip was fabricated in GF 65nm RF-CMOS technology with area of 0.08mm². The measured results show a current consumption of 14mA under supply voltage of 1V, a tuning range of

29.5% with center frequency at 89.3GHz, and a phase noise from -100.1dBc/Hz to -98.7dBc/Hz with 10MHz offset. A state-of-art figure-of-merit FOM_T of -177.78dBc/Hz is demonstrated.

- Based on the above chip realization and verification, one 60GHz PLL with the proposed symmetric inductive tuned VCO was implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level.

In summary, the major contribution of this thesis is to explore and demonstrate CMOS on-chip realization of CRLH-T-line metamaterial to overcome the fundamental limitations posed by traditional RH T-line on power combining and wide-frequency-tuning in 60GHz big-data communication systems.

1.3 Organization of the Thesis

The rest of the thesis is organized as follows. Chapter 2 reviews the background for both 60GHz direct-conversion communication system and metamaterial transmission line (T-line) with identified challenges and opportunities. Chapter 3 further provides in-depth discussions for one type of metamaterial T-line named composite right/left-handed (CRLH) T-line, whose unique properties such as zero-phase-shift and nonlinear negative phase-shift are shown to be potential for mm-wave applications. With zero-phase-shift provided by CRLH T-line, a new 2D distributed in-phase power combining network is developed in Chapter 4 for CMOS PA design to improve the output power density and bandwidth performance. In Chapter 5, a new inductive tuning mechanism is first presented for CMOS VCO design to improve frequency tuning range (FTR). Combined with the nonlinear negative phase-shift provided by CRLH T-line, a tunable CRLH T-line is further developed for Mobius-ring rotary-traveling-wave (RTW) VCO to achieve wide FTR with maintained low phase noise and compact size. Based on the chip realization and verification in Chapter 4 and Chapter 5, a CMOS 60GHz communication system is further integrated in Chapter 6, where post-layout

verifications are carried out for transmitter, PLL, and the whole transceiver. The conclusion is drawn in Chapter 7 with suggested future work.

Chapter 2

Background and Literature Review

2.1 60GHz High-data-rate Communication System

2.1.1 60GHz applications

The ever-expanding data size in various applications and associated increasing processing capability and memory size in mobile devices call for high-data-rate communication systems which can handle multi-Gbps data rate with compact size and low power consumption on the order of hundreds of mW or lower. The 5~9GHz license-free band at 60GHz is attractive to meet these requirements.

The large spectrum at 60GHz allows high-data-rate to be achieved with simple modulation schemes such as Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK), which have lower requirement on PA linearity and can work in the more power-efficient regions and allow higher output power. Furthermore, simple baseband processing can be used which largely reduces power. Quadrature Amplitude Modulation (QAM), on the other hand, uses non-constant envelope and has a more stringent requirement on both front-end linearity and baseband, and thus is normally limited below 16-QAM for low power consumption.

The signal in 60GHz attenuates quickly in air. There is around 10~20dB/km attenuation from oxygen absorption and additional 40~50dB/km loss if it's raining. As a result, it consumes too much power and is too costly for long distance communication. However, these attenuations actually provide benefits for medium distance communication to re-use the same frequency band or for security issues. It was previously used for medium distance (1~2km) point-to-point link in applications like cellular backhaul and fiber extension [10, 11].

For short distance communication with lower power consumption, normally line-of-sight set-up is used due to the high attenuation from passing through (around 40~50dB) and reflection from (around 10~20dB) a wall. As a result, the

distance is normally targeted around ten meters or below to cover the distance within a room.

Recently, there have been extensive researches on short distance 60GHz communication systems [12-16]. As discussed in Chapter 1, potential applications are the wireless High Definition Media Interface (HDMI) where you can have an uncompressed high definition movie transferred from laptop and displayed on TV in real time; and Personal Area Network (PAN), where a wireless 60-GHz link could be used to replace various cables used in home, and connect all electronic devices together with high data rate 60GHz routers to provide smart house applications. The development of IEEE standards such as IEEE 802.11ad and IEEE 802.15.3c further accelerates the 60GHz applications.

2.1.2 CMOS 60GHz direct-conversion front-end

2.1.2.1 CMOS for 60GHz

60GHz was previously achieved with III-V technologies and then moved to CMOS as transistor's maximum frequency steps into mm-wave region. Compared with III-V technologies, CMOS shows various advantages. Firstly, a high integration can be provided due to the lower power consumption of digital signal processing in CMOS. A high integration also lowers cost from multi-die package and improves performance with elimination of high frequency IOs. Secondly, a low cost can be obtained. Except for the lower fabrication cost compared with III-V technologies and lower package cost, the testing cost can also be largely reduced with built-in-self-test (BIST) integrated on chip.

However, CMOS also brings various design challenges. For example, scaled CMOS transistors with lower supply voltage in advanced technologies can largely reduce size and dynamic power for digital processing. Unfortunately, many Figure-of-Merits (FOMs) in front-end such as output power, linearity, noise all degrades along with reduced supply voltage. Furthermore, large Process-Voltage-Temperature (PVT) variation tends to occur with advanced CMOS technologies, which makes RF design less accurate and poses requirement on extra bandwidth to

cover. These design challenges motivate extensive researches on circuit and system innovations for 60GHz applications in CMOS [12-16].

2.1.2.2 Direct-conversion

Direct conversion architecture has the advantage of energy efficiency and was used for 60GHz CMOS transceiver design in [17]. One simplified block diagram is shown in Fig. 2.1. On the transmitter side, baseband digital signal is first converted to analog signal through a digital-to-analog converter (DAC) and then up-converted to RF signal by mixing with the carrier (LO) generated by PLL through a mixer. The resulted RF signal is then amplified by a power amplifier (PA) and radiated out through the antenna. On the receiver side, the received RF signal from the antenna is first amplified by a low noise amplifier (LNA) and then down-converted to baseband signal by mixing the corresponding LO generated by PLL through a mixer, which is further converted to digital signal through an analog to digital converter (ADC).

Figure 2.1 Simplified Block Diagram for a 60GHz CMOS Direct-conversion Transceiver Front End.

2.1.2.3 Link budget

Link budget analysis can be used to estimate the maximum communication distance of a designed transceiver and determine the design specification with a targeted application. The basic idea is the total link budget obtained from the transceiver specification should cover the total loss during signal communication. For this reason, the loss through wireless communication is first studied.

There are mainly three types of losses during wireless communication for 60GHz: free space loss (FSL), atmospheric gaseous loss and rain attenuation loss.

The free space loss defines the attenuation between two isotropic antennas through free space, and largely depends on the frequency and distance:

$$FSL = \left(\frac{4\pi R}{\lambda}\right)^2, \quad (2-1)$$

where λ is the wavelength and R is the communication distance. When expressed in dB scale, the formula becomes:

$$FSL = 92.4 + 20 \log(f) + 20 \log(R). \quad (2-2)$$

where f is the frequency in GHz and R is the distance in km.

The free space loss may be directly considered as the communication loss for frequencies at 10Hz or below. However, at mm-wave frequencies, signals can be absorbed by atmospheric molecules when traveling through air. As shown in Fig. 2.2, signals with different frequencies are sensitive to different types of molecules, and the peaks of these absorptions define "atmospheric windows" between them. At 60GHz, signal can be largely absorbed by oxygen (O₂) atoms and attenuated by around 10~20dB/km.

Except for atmospheric absorption, signals can also be scattered by rain at mm-wave frequencies due to the similar size of wavelength to rain droplets. Figure 2.2 shows the rain attenuation at different frequencies and rain densities. At 60GHz, around 40~50dB/km attenuation can be caused during excessive rain.

Except for the above three main loss sources, there may be other loss factors depending on the real applications, such as signal path clearance, foliage losses, scattering and diffraction losses, etc. Unlike the three mentioned loss schemes, these losses can be largely avoided through proper setup of the communication system and thus is ignored here.

Figure 2.2 The attenuation of millimeter waves by atmospheric gases, rain, and fog. [18]

All above loss schemes affect communication distance depending on weather, area, and applications. For short range communication, as the communication distance is typically tens of meters or below, only the free space loss needs to be considered.

To ensure a successful wireless communication, a link budget larger than the total attenuation from all above loss schemes needs to be maintained. From the transmitter side, a high transmission power (T_{dBm}) is required to cover the signal path loss. From the receiver side, a low receiver sensitivity (R_{dBm}) at the required Bit Error Rate (BER) is demanded to pick up the largely attenuated input signal. Furthermore, a high antenna gain for both transmission antenna (G_{TX}) and receive antenna (G_{RX}) helps to further boost the link budget and relax the design requirements on transmitter and receiver. In short, the link budget in dB scale can be calculated as:

$$(2-3) \quad B = T_{dBm} - R_{dBm} + G_{TX} + G_{RX}.$$

Note the loss from connection lines and match between antennas and the transmitter and receiver should also be considered and is included here in G_{TX} and G_{RX} .

Except for all the above losses that can be considered, at least several dB margin is commonly left to consider all other possible losses, and is represented by the link margin (LM). For short range communication at 60GHz, the communication distance can then be estimated from following equations:

$$(2-4) \quad B = FSL + LM,$$

$$(2-5) \quad 20 \log(R) = T_{dBm} - R_{dBm} + G_{TX} + G_{RX} - LM - 92.4 - 20 \log(f).$$

From the above equation we can see there are three items which depend on the design: transmitter output power, receiver sensitivity, and antenna gain. A high gain antenna, however, is normally expensive and bulky and hard to be integrated with low cost mobile devices. As a result, a high T_{dBm} and low R_{dBm} with compact size and low power is the major design target at RF front-end.

2.1.2.4 Challenges and targets

There are several design challenges for RF front-end defined in above sections, such as to provide wideband performance to cover the wide spectrum at 60GHz along with large PVT variations with scaled CMOS technology nodes, provide high transmitter power and low receiver sensitivity given the low supply voltage, and maintain a compact, low power, low cost design. In this thesis, we mainly target for the transmitter side. More specifically, we target to achieve a high transmitter output power with wide bandwidth and compact size. For this reason, PA and VCO are mainly analyzed in this thesis, where on-chip metamaterial T-line is explored to overcome the fundamental limitations posed by traditional right-handed (RH) T-line. The limitations of conventional RH T-line are discussed in

Section 2.1.3, while fundamental properties of metamaterial are reviewed in Section 2.2.

2.1.3 Limitations of Conventional RH T-line

Many mm-wave applications such as high data-rate communication [12-16] and imaging [19-23] are recently demonstrated in CMOS technologies. Compared to lower frequencies, the effect of component parasitic becomes much more pronounced at mm-wave which greatly limits circuit performance. Distributed topology is therefore commonly adopted in mm-wave circuit designs as parasitic capacitance of transistor can be absorbed into the transmission line (T-line) design for convenient impedance matching with extended bandwidth [24, 25]. Due to its simple structure, low loss, well defined impedance, accurate modeling, and the ability to provide distributed transmission of EM-wave, transmission line becomes one fundamental block for mm-wave integrated circuit (IC) design.

Traditional right-handed (RH) T-line or T-line network has an equivalent circuit as shown in Fig. 2.3. Fundamentally, as the phase velocity is in the same direction as the group velocity (EM-energy), there is always a positive phase-shift in a RH T-line, linearly proportional to the T-line length. In many mm-wave integrated circuit (IC) designs, large phase-shifts are required that can induce large size with high loss, and hence may pose fundamental design limitations on mm-wave IC performance as illustrated with details below.

Figure 2.3 Equivalent circuit for unit cell of RH (a) T-line and (b) T-line network.

Let us start the discussion by CMOS PA. Given low supply and breakdown voltages, as well as lossy substrate of deeply scaled CMOS technologies, high PA output power (e.g. 15dBm for >5m with QPSK estimated from [15]) cannot be achieved by one single CMOS transistor. There are various power combining methods proposed to improve output power as well as power added efficiency (PAE). T-line is commonly utilized in power combining topologies to provide power transmission for the required impedance and phase transformation. As such, all combined transistors can be periodically loaded in the combining network where their output powers are merged in phase. Unfortunately, in many power combiner topologies, long T-line proportional to wavelength (λ) is often required to achieve the in-phase power combining of transistors. As a result, high output power normally leads to bulky combiner size which is not appealing for mm-wave system integration such as beam-forming. For example, Wilkinson power combiner [26] requires $\lambda/4$ T-line with large area and high loss. Zero-degree power combiner [27] only requires equal-length short T-line; but it still needs many branches to be combined with large power combiner area due to its 1D power combining nature. One 2D power combining is introduced in [28], where an electrical "funnel" is constructed by 2D T-line network, which still has a low PAE due to the difficulty of matching. As such, other than T-line, a high power combining efficiency topology, characterized by *output power density* (or the ratio of output power divided by area), is required for CMOS PA to deliver output power in compact area with minimized loss, and to achieve high output power and high output power density simultaneously at mm-wave frequency region.

Besides PA, T-line is also the fundamental block to build distributed CMOS VCO at mm-wave, normally to realize traveling wave with generated multi-phase and low-noise clock outputs [29-32]. Traditionally, distributed VCO is implemented with RH T-line with a phase shift linearly proportional to the T-line physical length [31-33]. Since a total phase delay of 360° is required for oscillation, a large area is induced with small frequency-tuning-range (FTR) using varactor and capacitor bank [31-33].

One can observe that various circuit performances such as the power combining efficiency of PA and FTR of distributed VCO can be fundamentally limited by the poor phase tuning feature of RH T-line. Recently, the investigation of meta-

material T-line [34] has introduced many innovations in CMOS mm-wave IC designs [35-40]. With the design of unit-cell to construct periodic interconnect structure on-chip, left-handed T-line or meta-material can be realized on-chip by the metal layers in CMOS process. Different from distributed RH T-line, the phase velocity is in an opposite direction of group velocity (EM-energy) in LH T-line. As such, the LH T-line has a negative phase-shift with magnitude inversely related to frequency with a much sharper phase change. As a result, large phase-shifts can be achieved with small-sized LH T-lines at a given frequency range. To absorb parasitic capacitance from transistors in distributed structure, composite right/left-handed (CRLH) T-line [34] is realized instead, where the LH feature is maintained in its LH region. When the phase-shifts contributed from its RH components and LH components are balanced, the CRLH T-line can provide a zero-phase within compact area. As such, one can utilize these unique physical features of CRLH T-line to explore distributed mm-wave IC designs and hence to resolve the fundamental limitations from the conventional RH T-line. Note that the previous work of CRLH T-line was mainly implemented at PCB level within GHz operation region [34, 41-47]. Because passive device size is inversely proportional to the operating frequency, one can realize the CRLH T-line on-chip in CMOS technologies with compact size and low loss at mm-wave frequency region. In the following section, fundamental properties of metamaterial will be first reviewed, followed by detailed discussions on CRLH T-line in Chapter 3.

2.2 Metamaterial

2.2.1 Review of metamaterial

One general definition for metamaterial is given in [48]: 'a metamaterial is a macroscopic composite of periodic or non-periodic structure, whose function is due to both the cellular architecture and the chemical composition'. Alternatively, it can be defined using material's physical property [48]. Figure 2.4 shows a diagram for material's relative permittivity and relative permeability. Most natural materials lies on the horizontal line ($\epsilon_r \geq 1$; $\mu_r \approx 1$) and very few locate in 2nd and 4th quadrant ($\epsilon_r \times \mu_r < 0$). But with metamaterial, theoretically one can construct a material located in any region of the coordinate system.

There is a special kind of metamaterial defined in the 3rd quadrant, where both ϵ_r and μ_r are negative, and backward propagating wave is supported. It is called left-handed material, due to the left handed system formed by electric field (E), magnetic field (H), and wave factor (k). It is also the traditionally defined metamaterial.

Metamaterial can be classified into two types: resonant type and non-resonant type. Their typical examples are Split Ring Resonator (SRR) and Left Handed (LH) Transmission Line (T-line), respectively. Resonant type metamaterial has the advantage of larger dynamic range for material parameter (ϵ_r and μ_r) shift, while non-resonant type has the advantage of wider bandwidth and lower loss [48].

Figure 2.4 Definition of Metamaterial [48].

2.2.2 Metamaterial Transmission line

As transmission line (T-line) is a distributed device, it is suitable for metamaterial implementation with periodic placement of metamaterial unit cells. As shown in Fig. 2.5, a T-line can be modelled as a cascaded array of unit-cells, with equivalent circuit for each unit-cell represented by a series per-unit length impedance (Z) and a parallel per-unit length admittance (Y). Based on theory in

[34], the permeability (μ) and permittivity (ϵ) can be related to Z and Y at frequency ω by following equations:

$$(2-6) \quad \mu = \frac{Z}{j\omega}, \epsilon = \frac{Y}{j\omega}.$$

Figure 2.5 T-line model and component mapping to physical properties.

Traditional metamaterial T-lines can also be divided into resonant type and non-resonant type, represented by SRR/CSRR loaded T-line and Composite Right/Left Handed (CRLH) T-line, with the layout structures and the according equivalent circuits shown in Fig. 2.6, Fig. 2.7 and Fig. 2.8, respectively. Here C and L are per-unit length capacitance and inductance which determine the metamaterial property of T-lines.

For T-line loaded with SRR (Fig. 2.6), L_1 and C_2 come from T-line, while C_1 and L_2 come from magnetic coupling of SRR on both sides of T-line. The calculation $\epsilon = \frac{Y}{j\omega} = C_2$ gives a positive real-part, while $\mu = \frac{Z}{j\omega} = \frac{L_1 + L_2 - \omega^2 C_1 L_1 L_2}{1 - \omega^2 C_1 L_2}$. As a result, the 1st and 4th quadrants in Fig. 2.4 can be covered. For example, the 4th quadrant can be obtained when

$$(2-7) \quad \sqrt{\frac{1}{C_1 L_2}} < \omega < \sqrt{\frac{L_1 + L_2}{C_1 L_1 L_2}},$$

where $\text{Re}(\mu)$ is negative and $\text{Re}(\epsilon)$ is positive. As shown in Fig. 2.4, magnetic plasma is formed in this region, where propagating waves become evanescent waves [48]. As a result, energy cannot propagate through the resonator and is reflected back to establish a standing-wave. As a result, SRR loaded T-line forms a high-Q resonator.

Figure 2.6 Equivalent Circuit for SRR T-line Unit Cell.

Similarly, for T-line loaded with CSRR (Fig. 2.7), L_1 comes from T-line, while C_1 , C_2 , and L_2 come from electric coupling of CSRR on the ground. The calculation $\mu = \frac{Z}{j\omega} = L_1$ gives a positive real-part, while $\varepsilon = \frac{Y}{j\omega} = \frac{C_1(1-\omega^2 C_2 L_2)}{1-\omega^2(C_1+C_2)L_2}$. As a result, the 1st and 2nd quadrants in Fig. 2.4 can be covered. For example, the 2nd quadrant can be obtained when

$$(2-8) \quad \sqrt{\frac{1}{(C_1+C_2)L_2}} < \omega < \sqrt{\frac{1}{C_2 L_2}},$$

where $\text{Re}(\mu)$ is positive and $\text{Re}(\varepsilon)$ is negative. As shown in Fig. 2.4, in this case, electric plasma is formed, where propagating waves also become evanescent waves [48]. As a result, energy cannot propagate through the resonator either and is reflected back to establish a standing-wave. As a result, CSRR loaded T-line can also be used to form a high-Q resonator.

Figure 2.7 Equivalent Circuit for CSRR T-line Unit Cell.

Both SRR and CSRR loaded T-lines are resonant type metamaterial T-lines, which can provide high-Q resonance with narrow bandwidth. CRLH T-line, on the other hand, is non-resonant type T-line which can provide a wideband performance with low loss. Originally, it is realized as left handed transmission line with capacitors connected in serial (C_s) and inductors connected in parallel (L_p). However, due to the unavoidable parasitic which are normally serial inductor (L_s) and parallel capacitor (C_p), the resulted transmission line is actually a combination of left-handed (LH) transmission line and normal right-handed (RH) transmission line, and therefore called Composite Right/Left Handed (CRLH) Transmission Line [34]. Figure 2.8 shows 1D realization of CRLH T-line, where C_s comes from inter-digital capacitors, L_p comes from long metal stripe connected to ground through a via, while both L_s and C_p come from parasitic.

Figure 2.8 Equivalent Circuit for CRLH T-line Unit Cell.

According to the calculations $\mu = \frac{Z}{j\omega} = L_s - \frac{1}{\omega^2 C_s}$ and $\varepsilon = \frac{Y}{j\omega} = C_p - \frac{1}{\omega^2 L_p}$, both μ and ε can be designed either positive or negative. As a result, all area in Fig. 2.4 can be covered. For example, the 3rd quadrant can be obtained when

$$\omega < \sqrt{\frac{1}{C_s L_s}} \text{ and } \omega < \sqrt{\frac{1}{C_p L_p}}, \quad (2-9)$$

where both $\text{Re}(\mu)$ and $\text{Re}(\varepsilon)$ are negative. As shown in Fig. 2.4, in this case the CRLH T-line behaves as a LH material with backward propagation wave and negative phase shift.

In this thesis, CRLH T-line is mainly explored for its on-chip applications for mm-wave front-end design in CMOS. Note the CRLH T-line can also be constructed by SRR [49], CSRR [50] or their modified versions [51] with broadband behavior.

2.2.3 Metamaterial T-line on PCB at GHz

Many papers have been published to explore metamaterial T-line's applications in IC design at PCB level [41-47, 52-55].

For resonant type metamaterial T-line, due to its high-Q resonance, SRR/CSRR loaded T-line can be used in VCO design to provide low phase noise [52].

For non-resonant type metamaterial T-line, CRLH T-line shows a flexible phase-shift feature which can be varied nonlinearly from negative to positive, and thus can be applied in the designs of filter [41], balun [53], hybrid [43], and power combiner/divider [42, 45, 47, 54], where benefits such as wide bandwidth [41, 43, 45, 53], compact area [47] and dual band capability [54] are obtained. The CRLH T-line could also be extended to 2D structure and facilitate in power combiner/splitter [46], antenna [55], and even lens [44] design.

However, there are few publications to explore metamaterial T-line's applications for CMOS circuit design [56, 57], mainly due to bulky size and high loss of on-chip realization of metamaterial at GHz.

As frequency pushes into mm-wave region and beyond, the on-chip passive elements become much smaller which makes metamaterial feasible for on chip implementation. For 60GHz, implementation of a large periodic array may still be unrealistic, but applications with a few unit cells show good potential. In this thesis, CRLH T-line is mainly explored for on-chip CMOS applications and used to overcome the fundamental limitations posed by conventional RH T-line for RF front-end designs at mm-wave frequencies. In the next Chapter, CRLH T-line's unique properties will be first analyzed in detail, followed by its two applications in mm-wave PA and VCO designs in Chapter 4 and Chapter 5, respectively.

Chapter 3

CRLH T-line Design

3.1 Fundamental of CRLH T-line

Metamaterial can be classified into two types: resonant type [58] and non-resonant type [34]. For applications that require wide bandwidth, non-resonant type metamaterial is preferred [48]. Typically, it is realized as left handed T-line with capacitors connected in series (C_s) and inductors connected in parallel (L_p). However, due to the unavoidable parasitic which are normally serial inductor (L_s) and parallel capacitor (C_p), the resulted T-line is actually a combination of left-handed T-line and normal right-handed (RH) T-line, and therefore called composite right/left handed (CRLH) transmission line [34]. Due to the distributive nature of T-line, one unit cell has the equivalent circuit as Fig. 3.1(a).

The circuit can be viewed as two resonators connected together. L_s and C_s form the serial resonator, while L_p and C_p form the parallel resonator. Their impedance (admittance) can be represented as Z_s and Y_p , respectively. Here, all components (L_s , L_p , C_s , C_p) are normalized to unit cell length. According to transmission line theory, the propagation constant (γ) and characteristic impedance (Z_0) can be calculated as:

$$\gamma = \alpha + j\beta = \sqrt{Z_s \times Y_p} = \sqrt{-\frac{\left[\left(\frac{\omega}{\omega_s}\right)^2 - 1\right] \times \left[\left(\frac{\omega}{\omega_p}\right)^2 - 1\right]}{\omega^2 \times L_p \times C_s}}, \quad (3-1)$$

$$Z_0 = \sqrt{Z_s \div Y_p} = \sqrt{\frac{\left(\frac{\omega}{\omega_s}\right)^2 - 1}{\left(\frac{\omega}{\omega_p}\right)^2 - 1}} \times \frac{L_p}{C_s}. \quad (3-2)$$

where ω_s and ω_p are resonant frequencies for serial and parallel resonators, respectively. In addition, α and β are attenuation constant and phase constant.

Figure 3.1 CRLH T-line: (a) Equivalent circuit for T-line unit cell, (b) Operating regions.

3.1.1 General case (Unbalanced case)

From (3-1) we can see that if signal frequency is below the two resonant frequencies,

$$\alpha = 0, \beta = -\sqrt{\frac{\left[1 - \left(\frac{\omega}{\omega_s}\right)^2\right] \times \left[1 - \left(\frac{\omega}{\omega_p}\right)^2\right]}{\omega^2 \times L_p \times C_s}}, \quad (3-3)$$

signal propagates backward. The transmission line operates in the left-handed (LH) region, where the phase contribution from LH components (L_p and C_s) dominate. In this region, a negative phase constant is achieved with low frequency, which can be used to replace traditional T-line to realize the same phase requirement with

much more compact size and low loss. Based on this region, a tunable negative-phase CRLH T-line is implemented, with detailed discussion in Section 3.3.

If signal frequency is above the two resonant frequencies,

$$\alpha = 0, \beta = \sqrt{\frac{\left[\left(\frac{\omega}{\omega_s}\right)^2 - 1\right] \times \left[\left(\frac{\omega}{\omega_p}\right)^2 - 1\right]}{\omega^2 \times L_p \times C_s}}, \quad (3-4)$$

signal propagates forward. The transmission line operates in the right-handed (RH) region, where the phase contribution from RH components (L_s and C_p) dominate. The circuit behaves similarly to the traditional RH T-line.

If signal frequency is between the two resonant frequencies,

$$\alpha = \sqrt{-\frac{\left[\left(\frac{\omega}{\omega_s}\right)^2 - 1\right] \times \left[\left(\frac{\omega}{\omega_p}\right)^2 - 1\right]}{\omega^2 \times L_p \times C_s}} > 0, \beta = 0, \quad (3-5)$$

signal doesn't propagate. The T-line operates in the band-gap region, where the phase contributions from LH and RH components cancel each other. A zero-phase can thus be realized to replace traditional RH $\lambda/2$ T-line with much more compact area and low loss. Based on this region, a Zero-Phase-Shifter (ZPS) is implemented, with detailed discussion in Section 3.2.

The relationship between β and frequency ω defines the dispersion diagram. Note here a lossless system is assumed. If lossy components are introduced, β cannot stay 0 in the band-gap region, and α can never become 0.

An example for ideal CRLH T-line unit cell is plotted in Fig. 3.1(b) with $L_s=100\text{pHm}^{-1}$, $L_p=100\text{pHm}^{-1}$, $C_s=50\text{fFm}^{-1}$, and $C_p=70\text{fFm}^{-1}$. The dotted line displays attenuation constant α , and solid line displays phase constant β . Negative (positive) phase constant is obtained in the left (right) hand region, where signal propagates backward (forward). Two additional stop-bands appear in the very low and high frequency regions due to CRLH T-line unit cell's nature as a band pass filter.

The CRLH T-line can be extended to a 2D system. The resulted left handed region can be characterized by negative refractive index n

$$n = \frac{c}{v} = \frac{c}{f\lambda} = \frac{c\beta}{\omega}. \quad (3-6)$$

An example with $L_s = 10^6 \text{pHm}^{-1}$, $L_p = 0.01 \text{pHm}$, $C_s = 0.005 \text{fFm}$, and $C_p = 7 \times 10^5 \text{fFm}^{-1}$ is shown in Fig. 3.2. Note the refractive index below 60GHz should be negative and is mirrored to the positive side for easier observation.

Figure 3.2 Refractive index for 2D CRLH Metamaterial.

3.1.2 Balanced case

One special case occurs when the serial and parallel resonators have the same resonance frequency ($\omega_s = \omega_p$), and this is called balanced case.

In this case, equations (3-1) and (3-2) reduce to:

$$\alpha = 0, \beta = \beta_R + \beta_L = \omega\sqrt{L_s C_p} - (\omega\sqrt{L_p C_s})^{-1}, \quad (3-7)$$

$$Z_0 = \sqrt{\frac{L_p}{C_s}}, \quad (3-8)$$

where β_R and β_L are phase constants contributed from RH and LH T-line portions.

Notice the phase constant can now be spitted into RH and LH portions, and has a uniform equation for all frequencies. Furthermore, unlike the characteristic impedance for unbalanced case whose value varies with frequency, the characteristic impedance for balanced case stays frequency independent.

With the dispersion relation between β and ω , the phase velocity (v_p) and group velocity (v_g) can be further obtained for the balanced case:

$$v_p = \frac{\omega}{\beta} = \frac{\omega_B^2 \sqrt{L_p C_s}}{1 - (\frac{\omega_B}{\omega})^2}, \quad (3-9)$$

$$v_g = \frac{\partial \omega}{\partial \beta} = \frac{\omega_B^2 \sqrt{L_p C_s}}{1 + (\frac{\omega_B}{\omega})^2}, \quad (3-10)$$

where $\omega_B = \omega_s = \omega_p$ is a constant. These two equations indicate opposite directions for v_p and v_g when $\omega < \omega_B$, suggesting LH region where a negative phase shift is obtained; and the same direction for v_p and v_g when $\omega > \omega_B$, suggesting RH region where a positive phase shift is obtained.

Figure 3.3 Dispersion diagram for CRLH T-line in balanced case with comparison to RH T-line.

The dispersion diagram for ideal CRLH T-line unit cell in balanced condition is shown in Fig. 3.3. The balanced resonance frequency ω_B is designed at 60GHz. As the figure shows, the LH region and RH region locate side by side without band gap between them.

Compared with conventional RH T-line which always has a positive phase-shift linearly proportional to the T-line length, CRLH T-line shows some unique features such as zero-phase-shift at ω_B and high nonlinear negative-phase-shift in the LH region. These features are analyzed in detail in the following sections.

3.2 CRLH T-line based Zero-Phase-Shifter

3.2.1 ZPS by CRLH T-line

For applications at mm-wave frequencies, the lumped capacitors and inductors to build CRLH T-line structure are more compact and less lossy and hence feasible for on-chip implementation in CMOS technology. More importantly, CRLH T-line can easily achieve the zero-phase-shift by combining the two phase-shifts in opposite directions for: 1) traditional right-handed T-line portion (L_s and C_p) and 2) left-handed metamaterial portion (L_p and C_s).

An intuitive method to design a CRLH T-line based ZPS is to bias the unit cell to operate in its band gap region, as shown in Fig. 3.1(b). According to (3-5), when the operating frequency is in the band gap region ($\omega_s \leq \omega \leq \omega_p$ or $\omega_p \leq \omega \leq \omega_s$) the phase constant equals to 0 ($\beta = 0$). In this case, signals passing through CRLH T-line will not have any phase advance or delay. In other words, a zero phase shift is achieved. This condition, however, assumes the impedance matching from port to T-line is always maintained. As (3-2) shows, CRLH T-line's characteristic impedance (Z_0) is normally frequency dependant, which affects the matching for the whole SEDFDA, therefore limits the actual bandwidth that can be achieved for zero-phase-shift region. A simple solution is to design the CRLH T-line in the balanced case. As (3-8) shows, in this case, Z_0 becomes frequency independent and is only determined by L_p and C_s . Although the band gap region in this case reduces to one frequency point, according to the following Chapter, as long as a small

phase shift is maintained, the CRLH T-line still works well in many applications with a wideband performance.

On the other hand, in a practical T-line model the attenuation constant takes all loss from parasitic into consideration and stays positive ($\alpha > 0$) in all regions. Therefore, to reduce T-line loss, α must be reduced as much as possible, which is the case for balanced condition.

In balanced case, according to (3-7) and (3-9), when the frequency equals to ω_B , the phase constant β becomes 0 and the phase velocity v_p becomes infinity. In other words, a zero-phase-shifter (ZPS) is obtained. The zero-phase CRLH T-line can replace $\lambda/2$ T-line in traditional RH design with the same phase requirement. Different from traditional RH T-line, CRLH T-line phase-shift does not depend on its physical length. As a result, the T-line can be designed in compact area with low loss. Furthermore, the large phase shift (π) in traditional $\lambda/2$ T-line means that a small percentage change can lead to a large phase error, which severely limits the bandwidth. The zero-phase CRLH T-line, on the other hand, centers at zero-phase and thus can achieve a smaller phase error. Therefore, the zero-phase CRLH T-line has appealing advantages to replace traditional $\lambda/2$ T-line with more compact size, lower loss and wider bandwidth.

In addition, for the sake of a low loss and wideband performance of CRLH T-line based ZPS, both attenuation constant and phase constant need to be kept small. Equation (3-1) gives the relation: $\alpha, \beta \propto \sqrt{\frac{1}{L_p \times C_s}}$. Although the formula is developed from a lossless system, the relation can be extended into lossy system. As a result, a large parallel inductor (L_p) and a large serial capacitor (C_s) reduce both T-line loss and phase error. To maintain the same serial and parallel resonant frequencies and thus the same operating frequency, a small parallel capacitor (C_p) and a small serial inductor (L_s) are required accordingly. In practice, C_p and L_s are realized by parasitic and wire connections to achieve maximized values for L_p and C_s .

3.2.2 Simulation and measurement results

To further characterize the performance of CRLH T-line based ZPS and verify its benefits compared with traditional $\lambda/2$ T-line, one ZPS unit cell is implemented in UMC 65nm logic and mixed-mode low leakage low-K CMOS technology with 6-metal layers (1 thick metal layer). The circuit is designed and verified by EM simulation (ADS-Momentum) before fabrication.

As shown in Fig. 3.4(a), a unit cell for CRLH T-line can be constructed by combining a series capacitor (C_s) with a parallel inductor (L_p). The right-handed part of CRLH T-line comes from the Coplanar Waveguide (CPW) transmission line that connects unit cells, and parasitic capacitance between unit cells and ground. Figure 3.4(b) shows the layout version of this unit cell, where L_p is a spiral inductor formed by top metal layer (M6). The thick metal ring around L_p serves as ground to improve isolation between unit cells and to form a better distribution of ground, as described in [59]. C_s is a MOM capacitor constructed with multiple metal layers (M4-M6) in an inter-digit manner for better quality factor at 60GHz range. Notice the two grounds of CPW are connected by metal 1 (M1) below, and the size of M1 can be adjusted to tune the total parallel capacitance to ground.

Figure 3.4 CRLH T-line based ZPS unit cell: (a) schematic (b) layout.

The ZPS unit cell is fabricated along with an open-short-thru de-embedding structure. L_p is implemented with inductance of 220pH and Q factor of 13.4 at 70GHz. C_s is implemented with capacitance of 150fF and Q factor of 19 at 70GHz.

The simulated and measured S parameters for CRLH T-line based ZPS are shown in Fig.3.5, and are compared with the measured results of the conventional $\lambda/2$ T-line. According to Fig. 3.5(a), the fabricated CRLH unit cell achieves a

30GHz bandwidth (57~87GHz) for a phase error less than 10° , which is 4 times wider than the 7GHz bandwidth (67~74GHz) for $\lambda/2$ T-line. The measured results agree well with EM simulation with a frequency shift-down of 4 GHz. According to Fig. 3.5(b), the return loss is greater than 14dB for the entire near-zero-phase-shift region, indicating 50 Ω characteristic impedance. The worst case insertion loss is kept below 1.2dB, which is 3 times smaller than $\lambda/2$ T-line. There is a 0.8dB deviation from EM simulation for insertion loss, which is due to inaccurate substrate parameters.

(a)

(b)

Figure 3.5 Simulated and measured S parameters for unit cell of CRLH T-line based ZPS. Both (a) phase and (b) loss performances are compared with measured results for conventional $\lambda/2$ T-line.

Moreover, measurement demonstrates a low loss ($<1.2\text{dB}$) wideband (30GHz) performance for the proposed CRLH T-line based ZPS, which proves the feasibility for metamaterial application for CMOS designs in mm-wave region. Compared with the traditional $\lambda/2$ T-line, 4 times wider frequency band and 3 times less loss are achieved with 11 times reduction of physical length (86 μm).

Note that to observe the left-handed property, its phase shift and effective phase constant can be obtained from S parameters [60]. Following is the formula used:

$$\gamma \times p = \cosh^{-1} \left(\frac{1 - S_{11} \times S_{22} + S_{12} \times S_{21}}{2 \times S_{21}} \right), \quad (3-11)$$

where p is the physical length of unit cell, $\gamma = \alpha + j\beta$ is the propagation constant. For this design, p equals to 86 μm .

From Fig. 3.6(a), we can see $\beta \times p$ and phase of S21 overlap with each other, which is justified by the fact that phase shift of unit cell approximately equals to the product of phase velocity (β) and unit cell length (p) under impedance match. A small β within a wide frequency range therefore leads to a wideband performance.

The dispersion diagram is plotted in Fig. 3.6(b), where the phase constant β is obtained by dividing the phase shift ($\beta \times p$) to unit cell physical length (p). Notice absolute value of β is taken for easier observation. A fall-down curve for $|\beta|$ is observed below the zero-phase-shift region, indicating the left-handed region. Above the zero-phase-shift region is the right-handed region, where β becomes positive and keeps rising. The low-pass stop-band and high-pass stop-band are located around DC and very high frequency, respectively, and are not shown in the plot.

Figure 3.6 Characterization of CRLH T-line unit cell: (a) ZPS performance, (b) propagation constant.

3.2.3 Differential ZPS

In many applications, differential topology is preferred for compact size, reduced loss and rejected noise. As it is unknown how to design on-chip active differential zero-phase-shifter, in this section, differential CRLH T-lines are designed to obtain zero-phase-shift with circuit and layout diagrams shown in Fig. 3.7. The serial capacitor C_s is realized with inter-digital capacitors for compact size. M1 shielding is used to improve C_s quality factor. The parallel inductor L_p is implemented by a loop inductor. Thick top metal is used to minimize ohm and

substrate loss. M1 shielding around the inductor reduces the loss in return ground and also improves isolation. Parasitic from transistors and connections form the RH T-line portion (L_s and C_p). Connection lines and M1 shielding are used to adjust L_s and C_p values for a zero-phase-shift at the targeted frequency ω .

Figure 3.7 Equivalent circuit and layout diagrams for one unit-cell of differential CRLH T-line based zero-phase-shifter.

Due to the differential design, the parallel inductor for the two differential branches can be merged together with reduced area and improved isolation. In addition, due to virtual ground on the central tap of the merged inductor, decoupling capacitor is removed with further reduced area. As a result, zero-phase-shift can be achieved at designed frequency with compact area. For example, the differential ZPS unit cell in Fig. 3.7 further reduces the size to only $61\mu\text{m} \times 81\mu\text{m}$ while achieving the same ZPS frequency point (60GHz) as the single-ended design.

3.3 Tunable Negative-Phase CRLH T-line

Another unique feature of CRLH T-line is the inverse relation between phase-shift and T-line size in its LH region. As (3-7) and Fig. 3.3 show, the magnitude of

phase constant in CRLH T-line is inversely dependent on its LH components (L_p and C_s) and frequency. In contrast, the phase change in RH T-line is linearly dependent on the LC values and frequency and stays positive. As such, the same phase shift in the RH T-line at a given frequency can be realized by CRLH T-line in the negative-phase region in Fig. 3.3 with much smaller LC values and thus T-line size. For example, as shown in Fig. 3.8, a $\lambda/4$ T-line can be realized by RH T-line at around 90GHz, but can be replaced with a CRLH T-line with -90° phase-shift at around 30GHz with similar lumped component values and thus similar size. As a result, the required $\lambda/4$ T-line can be realized at the same frequency by -90° CRLH T-line biased in the LH region with much more compact size.

Though the negative-phase in the LH region shows a higher sensitivity to frequency and thus smaller bandwidth compared to ZPS, it does not impact the frequency tuning range (FTR). In fact, except for compact size, another benefit for the negative-phased CRLH T-line is the potential to achieve a wide FTR for VCO design. The tunability of CRLH T-line is analyzed here with balanced condition as shown in Fig. 3.3 for simplicity, and similar analysis and conclusion can be extended to more general conditions.

Figure 3.8 Compact size for negative-phase CRLH T-line to achieve the same 90° phase-shift compared to traditional RH T-line.

As discussed in Section 2.1.3, T-line is normally used in VCO design to realize traveling wave to generate multi-phase and low-noise clock outputs, by achieving certain phase-shift requirement (e.g. 360 °phase-shift to form a loop). According to (3-7) in Section 3.1.2, the total phase shift of one CRLH T-line unit cell (θ) is contributed from two portions: the left hand portion $\beta_L p$, and the right hand portion $\beta_R p$:

$$\theta = \beta_R p + \beta_L p = \omega \sqrt{L_s C_p} - (\omega \sqrt{L_p C_s})^{-1}, \quad (3-12)$$

where p is the T-line's physical length. Note different from (3-7), lumped components here are not normalized value to consider the phase shift instead of phase constant.

As shown above, CRLH T-line operating in the nonlinear LH region can replace traditional RH T-line to achieve the same phase-shift requirement with much more compact size. When operating in nonlinear LH region, $\beta_L p$ dominates. The formula can thus be simplified to

$$\theta = \beta_L p = -(\omega \sqrt{L_p C_s})^{-1} = \text{constant}, \quad (3-13)$$

$$\omega = (-\theta \sqrt{L_p C_s})^{-1}. \quad (3-14)$$

By taking the product of the LH components (L_p, C_s) as P_L ; and the product of the RH components (L_s, C_p) as P_R , the tunability can then be analyzed as

$$\frac{\partial \omega}{\partial P_L} = \frac{1}{2\theta} (P_L)^{-\frac{3}{2}}. \quad (3-15)$$

The frequency tuning range (FTR) with CRLH T-line operating in nonlinear LH region can then be estimated as

$$FTR_{LH} = \frac{\Delta \omega}{\omega} \approx \frac{1}{\omega} \times \frac{\partial \omega}{\partial P_L} \times \Delta P_L = \frac{\Delta P_L}{2P_L}. \quad (3-16)$$

Similarly, the FTR with traditional RH T-line can be estimated as

$$FTR_{RH} \approx \frac{\Delta P_R}{2P_R}. \quad (3-17)$$

Based on (3-16) and (3-17), the FTR depends on the tunability of the lumped component itself ($\Delta P_R/P_R$ and $\Delta P_L/P_L$). Conventional RH T-line is mostly tuned by varactor and capacitor bank, where the tuning range is limited by the parasitic capacitance from transistors and constraint tuning ability of varactor and capacitor bank in millimeter-wave region. CRLH T-line, on the other hand, provides more choices of tunable elements such as inductive-loaded transformer [61] and avoids effect from parasitic capacitance. As will be explained in Chapter 5, a much wider tuning range can be achieved.

In conclusion, by using tunable negative-phase CRLH T-line in nonlinear LH region to replace traditional RH T-line, the FTR can be largely improved with much more compact size. Note that the high nonlinear dispersion curve in the LH region can be also used to generate dual-band or multi-band operation [62], which can further extend the tuning range.

3.4 Active CRLH T-line

Most of the time, transistors need to be loaded in T-line to achieve desired functions. For example, in power combiner design for mm-wave PA, transistors need to be periodically loaded in the combining network where the output power of each transistor is combined in phase. While in mm-wave RTW-VCO design, transistors need to be distributed in the T-line loop to compensate the loss and facilitate oscillation. When considering transistors as part of CRLH T-line, an active CRLH T-line or T-line network is obtained.

Traditional active CRLH T-line loads active devices as negative resistors to compensate the propagation loss. As shown in Fig. 3.9(a), by loading a tunnel diode, negative resistance is introduced. Simultaneous negative α and negative β are demonstrated in [63], indicating the loss is compensated with maintained LH property. The same results can be obtained in a differential manner by replacing the tunneling diode with a cross-coupled transistor pair, as shown in Fig. 3.9(b). The topology is used for CRLH T-line based RTW-VCO design in Chapter 5.

Figure 3.9 Traditional active CRLH T-line using tunnel diode or cross-coupled transistor to compensate the propagation loss, (a) with tunneling diode, (b) with cross-coupled transistors.

However, these active CRLH T-line topologies are not feasible for PA design which requires signal amplification with maintained amplitude. Alternatively, transistor output power can be in-phase combined by directly connecting their outputs with zero-phase connections, which can be realized by the zero-phase CRLH T-line introduced in Section 3.2 with transistor parasitic absorbed into the T-line design. Since zero-phase CRLH T-line can realize in-phase power combining both in parallel and in series, a 2D active CRLH T-line network is introduced in Chapter 4, where a compact and high output power combining can be achieved.

Chapter 4

CMOS 60GHz PA with High-output Power Density

4.1 Introduction

Power amplifier (PA) is one critical block in 60GHz transceiver which needs to provide sufficient output power over a wide spectrum to cover the high path loss during high-data-rate communication. Given the low supply voltage, lossy substrate, and large PVT variations with scaled CMOS technology nodes, to achieve the output power and bandwidth requirements of 60GHz CMOS PA becomes a challenge. Physical limitations of traditional RH T-line as discussed in Section 2.1.3 further pose challenges on CMOS PA design and sometimes lead to bulky area with high loss and low efficiency. In this Chapter, by utilizing the unique feature of composite-right-left-handed (CRLH) T-line to achieve a real zero phase shift as discussed in Section 3.2, a new 2D distributed in-phase power combining network is developed to provide distributed amplification and power combining within compact area simultaneously. As such, one can achieve high output power, high output power density and wide-band performance for CMOS 60GHz PA and transmitter.

4.2 Review of CMOS 60GHz PA

The primary design challenges of CMOS power amplifiers (PA) at 60GHz for high-data-rate communication systems (with ~9GHz bandwidth) [24, 27, 64-68] are mainly *low output power/output power density* (or the ratio of output power divided by area) and also *narrow bandwidth (BW)*.

First, high path loss at 60GHz has introduced primary design challenge for CMOS PA to achieve high output power for short-range communication. For example, 15dBm output power is required for a communication distance around 5

meters with QPSK modulation estimated from [15]. Although the maximum radiation power for 60GHz systems is allowed up to 40dBm according to the Federal Communications Commission (FCC) regulations [26], the low supply voltage and breakdown voltage of deeply scaled CMOS technologies severely limit the achievable output power for one transistor with reasonable gain. Lossy substrate aggravates this problem with limited power added efficiency (PAE). Various power combining methods have been proposed to improve output power and also PAE of CMOS PA at 60GHz. Unfortunately, high output power normally leads to bulky combiner size which is not appealing for system integration. A high power combining efficiency topology, defined as *output power density*, is required to deliver output power in compact area with minimized loss, achieving high output power and high output power density simultaneously for CMOS PA design at 60GHz.

Apart from the output power performance, bandwidth is another important figure-of-merit (FOM) because wideband performance is normally required to cover the wide spectrum along with large PVT variations for CMOS PA design at 60GHz. However, traditional power combining methods do not support the wideband performance because of the non-distributed design and the long T-lines. Furthermore, existing techniques such as negative feedback and resistive matching are no longer viable for 60GHz applications [69]. One recent technique by shifted matching is proposed in [69]. Although a flat wideband performance is achieved using this method, the measurement shows a low PAE.

At the same time, though distributed amplification is effective to achieve wide bandwidth with output of each transistor combined in series, traditional distributed amplifiers suffer from low PAE due to un-optimized power performance for transistors in each distributed stages as well as power wastage from resistive terminations. One single-ended dual-fed distributed amplifier (SEDFDA) is introduced in [70] to improve PAE and power gain. However, as will be explained in Section 4.5, it requires phase-shift of $\pm n\pi$ ($n=0,1,2,\dots$) to be maintained on gate and drain lines. Since traditional T-line is right-handed with its phase-shift proportional to length, only positive phase-shift such as π can be achieved with $\lambda/2$ T-line, and is thereby too bulky and lossy for on-chip applications.

In conclusion, achieving the output power and bandwidth requirements of 60GHz CMOS PA is a challenge due to low supply voltage, wide spectrum and large PVT variations for CMOS devices [69]. Physical limitations of traditional RH T-line further poses challenges on CMOS PA design as discussed in Chapter 3. Design iterations between output power density and BW have become more and more complicated, while sufficient power gain and linearity should still be maintained.

4.3 Review of Power Combining

Power combining can improve output power and PAE at 60GHz [27], [66]. Numerous power combining techniques have been published for 60GHz CMOS applications [26, 27, 66, 71-73]. The most straightforward method is to use Wilkinson power divider/combiner as implemented in [26]. It has the advantage of easy implementation, low loss, and good isolation between ports. However, the required $\lambda/4$ transmission line (T-line) occupies a large area. Two modified techniques are implemented in [66] and [27]. The first one merges the power combining/dividing function into the existing matching network, which is still bulky in area. The latter one, on the other hand, uses zero-degree power divider instead, which eliminates the resistor and only requires equal-length short T-line and is thus much more compact. However, to achieve a high output power, it still requires many branches to be combined with large power combiner area due to its 1D power combining nature. Another widely explored device for power combining is transformer. Distributed active transformer (DAT) has been proven as an efficient method for power combining [71, 72, 74]. However, the DAT topology limits the number of combined transistors, which in turn limits the achievable output power. As a result, to achieve a high output power, either a larger DAT size needs to be adopted or multiple branches need to be used, both of which degrade the output power density due to its 1D power combining nature. One 2D power combining is introduced in [28], where an electrical "funnel" is constructed by 2D T-line network, which still suffers from bulky size for impedance transformation, low PAE and difficulty of matching.

As discussed in Chapter 3, T-line is commonly utilized in power combining topologies to provide power transmission for the required impedance and phase transformation. As such, all combined transistors can be periodically loaded in the combining network where their output powers are merged in phase. Unfortunately, in many power combiner topologies, long T-line proportional to wavelength (λ) is often required to achieve the in-phase power combining of transistors. Since advanced technology only scales active devices while the passive devices remain relatively the same size, the power combiner size is normally dominated by the passive elements. As a result, due to the usage of long RH T-line, high output power normally leads to bulky combiner size which is not appealing for mm-wave system integration. On the other hand, CRLH T-line with its unique phase-change property could be used to replace RH T-line with the same phase requirement but much more compact size and lower loss. In the following section, an active in-phase distributed CRLH T-line network is proposed to improve the power combining efficiency and with high output power and high output power density achieved simultaneously at mm-wave frequency region.

4.4 Active In-Phase Distributed CRLH T-line Network

In order to achieve high *output power/output power density* performance with improved power combining efficiency and wide bandwidth, multiple transistors need to be periodically loaded in the combining network in compact size with distributed topology where the output power of each transistor is combined in phase. With compact CRLH T-line to replace traditional RH T-line, the challenge is how to load transistors in T-line network and have their output power combined in phase. The loading method for traditional active CRLH T-line reviewed in Chapter 3 is not feasible for PA design as negative resistor would cause oscillation. Alternatively, transistor output power can be in-phase combined by directly connecting their outputs with zero-phase connections, which can be realized by the CRLH T-line based zero-phase-shifter (ZPS) introduced in Chapter 3 with transistor parasitic absorbed into the T-line design. Since zero-phase CRLH T-line can realize in-phase power combining both in parallel and in series, a 2D active CRLH T-line network is introduced in Fig. 4.1.

As shown in Fig. 4.1, the power combining is achieved in 2 levels: *serial power combining* (1st level) realized in each branch; and *parallel power combining* (2nd level) further implemented at the output. Active CRLH T-line unit cells are realized by absorbing the parasitic capacitance of the loaded transistors into design. In the 1st level combining, by designing the active CRLH T-line with zero-phase-shift in the target frequency, all transistor outputs in each branch can be serially combined in phase. The load-pull optimization process is also simplified as load-line impedance of all transistors can be viewed directly fed to output. As a result, the optimized power performance can be achieved by simply feeding a load impedance $R_L = R_{opt}/N$ to the output of the branch, where R_{opt} is the optimized load-line impedance which can be easily calculated. For example, for class-A amplifier design, the optimized efficiency can be achieved by implementing: $R_{opt} = (V_{max} - V_{min})/I_{max}$, where V_{max} and V_{min} are transistor's maximum and minimum output voltage for class A operation and I_{max} is the maximum output current [75].

Figure 4.1 Proposed 2D active CRLH T-line network. By absorbing parasitic C from transistors into zero-phase CRLH T-line design, in-phase power combining is realized both in series and in parallel, resulting 2D distributed power combining.

Due to the power pre-combining in the 1st level, the size of parallel power combiner in the 2nd level can be largely reduced with use of compact transformers, which perform output matching at the same time. Moreover, a differential structure could be implemented in both CRLH T-line and PA with benefits of compact size and reduced loss. As a result, more (>10) power transistors can be combined for high output power with high power combining efficiency and wide bandwidth.

Note there may be various connection methods to achieve in-phase power combining using CRLH T-line based ZPS. However, as shown in Section 3.2 the exact zero-phase-shift is only realized at one frequency point. To achieve a wideband performance, the ZPS connections for the serial power combining is adjusted to resemble one distributed amplification topology named single-ended dual-fed distributed amplifier (SEDFDA) topology [70], but with the bulky $\lambda/2$ T-line replaced with compact zero-phase CRLH T-line, thus achieving wide bandwidth with much reduced size and loss.

In the following section, the feature of SEDFDA would be reviewed first followed by detailed analysis for on-chip implementation towards 60GHz PA design.

4.5 SEDFDA Based PA Design

4.5.1 Review of SEDFDA

Wide *bandwidth* is usually achieved by distributed amplification in mm-wave region. One major limitation for traditional distributed PA is its low PAE. As shown in Fig. 4.2(a), each transistor outputs different power; therefore the transistors cannot be optimized simultaneously [24]. The power wasted in the resistive terminations further degrades the efficiency. Both transmission-line and transistor sizes are tapered in [24] to realize the maximized output voltage swing at all distributed stages (Fig. 4.2(b)). Although each transistor still outputs different power, the same voltage swings are maintained due to scaled transistor sizes. However, the large scaling ratio between transistor stages limits the achievable number of distributed stages and thus output power. Furthermore, resistive terminations still consume power and degrade efficiency. A new distributed

amplifier called dual-fed distributed amplifier (DFDA) was proposed in [76], which can significantly improve the PAE limitation for distributed PAs. As shown in Fig. 4.2(c), the input signal is split into 2 paths and fed into both ends of the gate line. The two outputs from the drain line are then combined again as the output signal. It has been proven that when a phase-shift of $\pm n\pi$ ($n=0,1,2,\dots$) is maintained between transistors in both gate and drain lines, all transistors can see the same load, and output the same power [75]. As a result, they can be optimized simultaneously. Moreover, the resistive terminations are eliminated in DFDA, and there is no additional power wasted. As a result, the PAE limitation of distributed PAs can be resolved fundamentally. DFDA is further developed in [70] as single-ended to eliminate the need of hybrid. The resulted topology is shown in Fig. 4.2(d), which is called single-ended dual-fed distributed amplifier (SEDFDA). Both input and output signals propagate to the open-circuit ends and are reflected back. Since both forward and reflected signals add up to each other under certain phase-shift of the T-line, the power gain is further improved.

Note that both DFDA and SEDFDA require a phase-shift of $\pm n\pi$ ($n=0,1,2,\dots$) to be maintained between transistors in both gate and drain lines. Since zero-phase-shift ($n=0$) is impossible to be realized by the traditional T-line (which introduces phase-shift proportional to the T-line length), $\lambda/2$ T-line is used at PCB level to fulfill the phase-shift requirement, which is however too bulky and lossy for on-chip implementation. One type of metamaterial called composite right/left handed (CRLH) T-line can be used to realize a real zero-phase-shift, and is implemented for distributed amplifier design in [75] and [77] at PCB level for GHz region applications. However, at this frequency region, CRLH T-line is too bulky and lossy for on-chip implementation in CMOS technology.

With frequency pushed into mm-wave frequency region, such as 60GHz, the lumped capacitor and inductor to build CRLH T-line structures are more compact and less lossy and hence feasible for on-chip implementation in CMOS technology. In this chapter, CRLH T-line based ZPS is studied for the first time during the on-chip power amplifier design at 60GHz [35]. Detailed design considerations are studied for ZPS to achieve low loss and wideband performance for 60GHz PA applications.

Figure 4.2 Distributed amplifier (DA) topologies: (a) conventional DA, (b) tapered DA [24], (c) DFDA [76], (d) SEDFDA [70].

Both DFDA and SEDFDA have been analyzed in [75] and [78] but targeted for PCB design at GHz level, where T-lines are normally assumed ideal. For on-chip power amplifier design at 60GHz and beyond, T-lines are no longer ideal and the amplifier performance can be greatly affected. In the following, we present the design analysis background of SEDFDA, and then show the design implications when considering the non-ideal T-line targeted for on-chip 60GHz applications.

4.5.2 SEDFDA performance analysis under ideal T-line model

Figure 4.3 shows the equivalent circuit for one N -stage SEDFDA. The upper half is the gate line and the lower half the drain line. All parasitic components from transistors can be absorbed into the T-line model. Resulted T-lines for each section in both gate and drain paths are then characterized with characteristic impedance Z_g/Z_d , propagation constant γ_g/γ_d , and physical length l_g/l_d . The input impedance and load impedance are termed as Z_S and Z_L . Perfect open circuits are assumed for terminations on both gate and drain lines. The input signal travels along the gate line, meets open-circuit termination, and is reflected back again. Forward and backward signals add up together to form transistor gate voltage V_{gk} (for the k -th distributed stage), which controls the corresponding drain current I_{dk} . Assume $Z_S=Z_g$, gate voltages for all transistors can be calculated by directly adding the forward and backward voltages:

$$(4-1) \quad V_{gk} = V_{in}[e^{-k\gamma_g l_g} + e^{-(2N-k)\gamma_g l_g}].$$

Figure 4.3 Equivalent circuit for Single-ended Dual-fed Distributed Amplifier (SEDFDA).

One special property for distributed amplifier is that transistor drain voltage (V_{dk}) is affected by all transistor drain currents. Assume $Z_L=Z_d$, with a similar method as [75], all drain voltages for SEDFDA can be calculated:

$$V_{dk} = \frac{g_m V_{in} Z_d (A1 + A2 + B1 + B2)}{1 + \coth[(N-k)\gamma l_d]}. \quad (4-2)$$

where $A1, A2, B1, B2$ are:

$$\begin{aligned} A1 &= e^{-k\gamma_g l_g} \times e^{-k(\gamma_d l_d + \gamma_g l_g)/2} \times \frac{\sinh[(k-1)(\gamma_d l_d + \gamma_g l_g)/2]}{\sinh[(\gamma_d l_d + \gamma_g l_g)/2]}, \\ A2 &= e^{-(2N-k)\gamma_g l_g} \times e^{-k(\gamma_d l_d + \gamma_g l_g)/2} \times \frac{\sinh[(k-1)(\gamma_d l_d + \gamma_g l_g)/2]}{\sinh[(\gamma_d l_d + \gamma_g l_g)/2]}, \\ B1 &= e^{-k\gamma_g l_g} \times e^{(N-k)(\gamma_d l_d + \gamma_g l_g)/2} \times \frac{\sinh[(N-k+1)(\gamma_d l_d + \gamma_g l_g)/2]}{\sinh[(\gamma_d l_d + \gamma_g l_g)/2]}, \\ B2 &= e^{-(2N-k)\gamma_g l_g} \times e^{(N-k)(\gamma_d l_d + \gamma_g l_g)/2} \times \frac{\sinh[(N-k+1)(\gamma_d l_d + \gamma_g l_g)/2]}{\sinh[(\gamma_d l_d + \gamma_g l_g)/2]}. \end{aligned} \quad (4-3)$$

The load line impedance for all transistors can then be obtained:

$$Z_{dk} = \frac{V_{dk}}{I_{dk}} = \frac{V_{dk}}{g_m V_{gk}}. \quad (4-4)$$

If the same load line impedance can be maintained for all transistors, their power performance can be optimized simultaneously. For lossless T-line as the case for GHz region applications at PCB level, it can be achieved by maintaining a same phase shift $\pm n\pi$ ($n=0,1,2,\dots$) in both gate and drain lines:

$$Z_{dk} = NZ_d \quad \text{when } \beta_d l_d = \beta_g l_g = \pm n\pi \quad (n = 0, 1, 2, \dots). \quad (4-5)$$

where β_g and β_d are the phase constants for T-lines on gate and drain paths, respectively. In this case, all transistors can be fully utilized, and efficiency of the whole amplifier depends on that of each transistor. For example, for class-A amplifier design, the optimized efficiency can be achieved by implementing:

$Z_{dk} = (V_{max} - V_{min})/I_{max}$, where V_{max} and V_{min} are the maximum and minimum output voltage for class A operation and I_{max} is the maximum output current [75].

The improvement in efficiency can also be observed through the improvement in power gain. With (4-5) satisfied, the power gain can be calculated as:

$$Gain = \frac{P_{out}}{P_{in}} = 4N^2 g_m^2 Z_g Z_d. \quad (4-6)$$

which is 16 times larger than the conventional distributed amplifier with the same number (N) of transistors.

However, for on-chip distributed amplifier design at 60GHz and beyond, T-lines can no longer be assumed as ideal. Large parasitic components of transistor which are absorbed into the T-line design further degrade its performance. Both loss (denoted in Section 4.5.3) and phase error (denoted in Section 4.5.4) on the T-line can severely degrade amplifier performance, and therefore should be taken into consideration with detailed analysis as shown below.

4.5.3 Effect of T-line loss on SEDFDA

As frequency pushes up into mm-wave region and transistor size shrinks down to below 100nm, the lossy substrate, thin metal layer, and strong coupling between them severely degrades the quality factor of passive components. What is worse, the large and low-Q parasitics of transistor, which are absorbed into the T-line design, can severely degrade the effective Q-factor of T-line. For a practical on-chip amplifier such as PA design at 60GHz, loss on T-line must be taken into consideration.

Recall that (4-5) and (4-6) assumed ideal T-line in both gate and drain paths, i.e. $\alpha_d l_d = \alpha_g l_g = 0$, where α_g and α_d are the attenuation constants for T-lines on gate and drain paths, respectively. For the practical on-chip design, α_g and α_d can no longer be assumed zero and are used to represent the loss on T-line. As a result, the conclusion in (4-6) can be affected.

Figure 4.4 Effect of T-line loss on SEDFDA performance.

The impact of T-line loss to the SEDFDA design is further illustrated by one simulation example. Figure 4.4 shows the impact of T-line loss on SEDFDA power gain. Here g_m is assumed to be 20mS and characteristic impedance on both gate and drain lines are set as 50 Ω . Loss per distributed stage on T-line are defined as $\alpha_g l_g$ ($\alpha_d l_d$) and assumed identical on both gate and drain paths. As Fig. 4.4(a) shows, loss on T-line severely degrades the power gain in an exponential manner. For example, for a 10-stage SEDFDA, the power gain reduces from above 25dB to below 0dB as loss on T-line increases from 0dB/stage to 2dB/stage. It can also be

observed that the impact of loss on power gain becomes more severe as the number of stages (N) increases. This can be understood that as N increases the signal needs to propagate through more lossy stages to the output and therefore, it experiences more degradation. As a result, there exists an optimum N for a specific value of loss in order to achieve the highest power gain. This optimum N decreases as loss per stage increases. In other words, loss on T-line limits the maximum number of stages that can be implemented in the SEDFDA.

The advantage of SEDFDA over the conventional distributed amplifier is its improvement on power gain and efficiency. As (4-6) shows, an ideal SEDFDA can improve power gain by 12dB, and improves the efficiency proportionally. However, as loss on T-line increases, this advantage gradually diminishes. Figure 4.4(b) shows the impact of T-line loss on the power gain improvement, which is calculated by dividing the obtained power gain to the power gain of a conventional distributed amplifier with the same number of stages and with ideal T-line. As shown in Fig. 4.4(b), in high loss region the gain ratio decreases below 0dB. This effect again becomes more severe as N increases. In other words, loss on T-line again limits the maximum number of stages (N) that can be implemented in the distributed amplifier. For example, with loss of 2dB per stage, SEDFDA with stage number above 2 can have no advantage over conventional topology (with ideal T-line) on power and efficiency performance.

Note that although identical loss is assumed on both gate and drain lines here for easy simulation, similar conclusion can be drawn if divergent losses are used.

4.5.4 Effect of T-line phase error on SEDFDA

As mentioned above, the performance of SEDFDA is optimized when phase shift in both gate and drain lines are identical and equals to $\pm n\pi$ ($n=0,1,2\dots$). It is relatively easy to keep identical phase shift in gate and drain line, but very difficult to maintain the phase shift to a fixed value. The major reason is that phase shift in T-line is often frequency dependant. At 60GHz and beyond it is very expensive to implement phase compensation with extra circuits, and the large process variation further degrades the problem. Here we denote the difference between actual phase

shift and target value as "phase error" and analyze its impact on SEDFDA power performance.

Recall that to obtain the conclusions in (4-5) and (4-6) the phase shift condition $\beta_d l_d = \beta_g l_g = \pm n\pi$ ($n = 0, 1, 2, \dots$) must be satisfied, where β_g and β_d are the phase constants for T-lines. The identical phase shift ($\beta_d l_d = \beta_g l_g$) is relatively easier to achieve and is assumed βl . Since we target a phase shift of $\pm n\pi$, the phase error can then be represented as $\text{mod}(\beta l, \pi)$.

Figure 4.5 Effect of T-line phase error on SEDFDA performance.

Figure 4.5 shows the resulted simulation result, with the same parameters used as in Fig. 4.4. The phase error per stage is swept from -20° to $+20^\circ$. As Fig. 4.5

shows, the power gain degrades as phase error increases. Since phase error is normally proportional to frequency shift, this gain drop determines the bandwidth of SEDFDA. It also explains the trade-off of SEDFDA bandwidth over the conventional distributed amplifier, since the conventional topology only requires identical phase shift in gate and drain lines, and therefore has no such bandwidth limitation.

It can be observed that again as number of stages (N) increases, the power gain degradation by phase error becomes more severe. As a result, phase error on T-line also limits the maximum number of stages that can be implemented in SEDFDA.

4.5.5 CRLH T-line based SEDFDA

As discussed above, both loss and phase error of T-line can degrade SEDFDA performance and also limit the number of stages (N) to be implemented. As will be shown in the following section, the value of N affects the power handling capability of the proposed PA topology when using SEDFDA. A T-line that can achieve phase shift of $\pm n\pi$ ($n=0,1,2,\dots$) with low loss and small phase error is thereby required. Unfortunately, a 0° phase shift cannot be obtained in nature when using the traditional T-line since its phase-shift is proportional to a non-zero length. As a result, $\lambda/2$ T-line is used instead at PCB level for SEDFDA design, which achieves a phase shift of 180° . When implemented on chip, this T-line is very bulky and lossy. Furthermore, its large phase shift (π) means a small percentage change can lead to a large phase error, which severely limits the bandwidth. As a result, traditional T-line approach is impractical for on-chip implementation of SEDFDA.

Alternatively, as presented in Chapter 3, one non-resonant type metamaterial T-line called CRLH T-line is shown to be able to achieve a real zero-phase-shift, and can be utilized to replace $\lambda/2$ RH T-line for SEDFDA based on-chip PA design at 60GHz with compact size, low loss and wide bandwidth as shown in Chapter 3.

Figure 4.6 Traditional right-handed T-line analysis: lumped model and Smith Chart. Impedance on Smith Chart is obtained by loading the theoretical characteristic impedance Z_o and varying both parameter ωL and stage number n .

Except for compact T-line size itself, zero-phase CRLH T-line also allows more compact design of the whole distributed amplifier topology. In distributed amplifier design, as parasitic capacitance in transistor is to be absorbed into the T-line design, the effective T-line is realized with lumped model. Figure 4.6 shows the lumped model of traditional RH T-line. By equalizing Z_n and Z_{n+1} , following impedance is obtained:

$$Z_n = Z_{n+1} = \sqrt{\frac{L}{C} - \left(\frac{\omega L}{2}\right)^2} + j \cdot \frac{\omega L}{2}, \quad (4-7)$$

where n is the distributed stage number, $\omega < \omega_c = \frac{2}{\sqrt{LC}}$ which is the cut-off frequency of traditional RH T-line. At low frequency, the term $\frac{\omega L}{2}$ approaches 0, and Z_n is roughly equal to the T-line characteristic impedance $Z_o = \sqrt{\frac{L}{C}}$. However, as $\frac{\omega L}{2}$ becomes more significant at higher frequency, Z_n deviates from Z_o , causing impedance mismatch which degrades distributed amplifier's gain. Furthermore, as the Smith Chart in Fig. 4.6 shows, due to the additional term $\frac{\omega L}{2}$, the obtained Z_n moves in a circle near Z_o as n changes. The radius of this circle increases as $\frac{\omega L}{2}$ increases, leading to large impedance variation in different distributed stages. As a result, the power performance is degraded as transistors cannot be optimized

simultaneously. In order to achieve proper operation in high frequency such as mm-wave region, the inductance L needs to be reduced to keep $\frac{\omega L}{2}$ small. For a given Z_o , the capacitance C needs to be reduced proportionally. As large portion of C comes from parasitic capacitance in transistor, the transistor size in each distribution stage has to be reduced as well. As a result, in order to maintain the total transistor size and thus output power, more distributed stages need to be designed, which leads to larger layout size and lower output power density.

Zero-phase CRLH T-line, on the other hand, does not have this problem. As illustrated by Fig. 4.7, the impedance at each distributed stage can be matched exactly to the designed impedance and is irrelevant to the transistor parasitic or designed frequency. As a result, large transistor size can be adopted with reduced distributed stages, leading to a compact distributed amplification.

Figure 4.7 Zero-phase CRLH T-line analysis: lumped model and Smith Chart. Impedance at various nodes of CRLH T-line model is plotted on Smith Chart.

4.6 ZPS based 2D Distributed Power Combining for PA

Since *low output power/output power density* and *narrow bandwidth* are two primary design challenges for CMOS PA at 60GHz, this chapter introduces a new power combining topology to simultaneously improve PA's output power and bandwidth performance. One straightforward approach is to merge one power combining topology with high power combining efficiency and distributed amplification with wide bandwidth.

4.6.1 2D distributed combining topology

Since the design target is not for ultra wideband solution, a SEDFDA topology can be used to realize distributed amplification with extra bandwidth traded for better power performance. CRLH T-line based ZPS is implemented in SEDFDA to optimize all transistors' power performance simultaneously with compact size and low loss.

The proposed 2D active CRLH T-line network is further adopted as the power combining topology with high power combining efficiency. As discussed in Section 4.4, the ZPS connections in the proposed 2D active CRLH T-line network are adjusted such that each combining branch resembles a SEDFDA with ZPS connection. In this way, both high-efficient power combining and distributed amplification can be simultaneously achieved.

The resulted topology is shown in Fig. 4.1. Figure 4.8 shows the single-ended version of the proposed power combining topology. By using CRLH T-line realized ZPS, a new 2D distributed power combining network can be constructed. The CRLH unit-cell can replace the traditional $\lambda/2$ T-line for in-phase distributed amplification along horizontal direction to achieve the *serial power combining*. The *parallel power combining* for all horizontal branches is then realized by zero-degree power combiner with short equal-length T-lines along the vertical direction. With the *serial power combining* in the 1st level and *parallel power combining* in the 2nd level, a 2D distributed power combining network is realized for simultaneous distributed amplification and power combining. Such a topology can be further extended for phased-array applications by replacing ZPS with an array of tunable phase-shifters.

The proposed topology can simultaneously improve power and bandwidth performance of PA. For example, PA power performance can be viewed from two aspects: output power per area ($P_{out}/area$) and output power per DC power consumption (PAE). The 2D power combining network provides a high density of transistor, therefore improves $P_{out}/area$. The distributed topology provides a wide bandwidth, while the SEDFDA implemented with CRLH T-line based ZPS trades extra bandwidth with improved efficiency, thus improving PAE. As a result, the power performance can be improved together with bandwidth performance.

Figure 4.8 Single-ended version of proposed SEDFDA PA topology based on 2D distributed power combining network with the use of CRLH ZPSs.

Note that for a fixed transistor size, the total output power depends on distributed stages N and parallel combining branches M . Therefore, the power handling ability of the proposed PA partially depends on distributed stage number N , which is limited by T-line loss and phase error as mentioned in the Section 4.5.

4.6.2 Design optimization of ZPS based power combining

A detailed design consideration can be viewed in Fig. 4.9. With bandwidth performance fulfilled with distributed nature of the proposed topology, PAE and output power density (P_{out}/area) become two major targets during PA design. By knowing the application for the PA, the proper PA class can then be selected. Together with the selected technology, f_t/f_{max} optimization, PAE and P_{out}/area requirement, and layout skills, the sizing and biasing of the transistors can be initially determined.

Figure 4.9 Design consideration for the proposed 2D distributed power combining network.

However, the inter-dependency between parameters calls for certain design iterations. There are mainly three considerations shown in the diagram that may require design iterations.

1. To improve the power density performance ($P_{out}/area$), large size is preferred for transistors. However, large transistor size brings large parasitic components, which are the major contribution for L_s and C_p in ZPS design. As stated in Section 3.2, this leads to small L_p and C_s to maintain the same operating frequency, which in turn causes high loss and narrow bandwidth for the designed ZPS. As a result, PAE is degraded. A compromise therefore needs to be made between $P_{out}/area$ and PAE.
2. DC bias of transistors determines PA operating class. Both P_{out} and PAE performances for a single transistor is also determined by the bias. However, DC bias of transistors affects ZPS design through its optimized

load line impedance. As shown in the diagram, given DC bias, for optimized performance of all transistors, the load line impedance (Z_{dk}) is determined, which in turn determines the characteristic impedance of the drain line (Z_d).

As stated in Section 3.2, a balanced condition ($\omega_s = \omega_p$) is preferred for optimized ZPS performance, which leads to a characteristic impedance of $Z_o = \sqrt{\frac{L_p}{C_s}} = \sqrt{\frac{L_s}{C_p}}$ according to (3-8). However, the actual parasitic reactance from transistors (L_s' and C_p') is unlikely to follow the above relation for L_s and C_p . As a result, the size of L_s or C_p needs to be over-designed to generate wanted Z_d . Again, high loss and narrow bandwidth are caused for the designed ZPS, which degrades PAE performance. In summary, PAE is affected by both transistor DC bias and ZPS performance, and a compromise needs to be made between these two parts.

3. The parallel combining topology not only affects $P_{out}/area$ and PAE performances directly through its efficiency, but also affects them indirectly through the output matching. As stated in (4-5), with a fixed load line impedance Z_{dk} , the characteristic impedance for the drain line is $Z_d = Z_{dk}/N$, where N is the distributed stages. Assuming M distributed amplifiers (DAs) are combined in parallel, the output impedance can be calculated as $Z_{out} = Z_{dk}/(MN)$ if the Z_d for all DAs are combined in parallel, which is the case for zero-degree power combiner.

Though the combiner has the benefit of merging part of DA design into itself with reduced loss, a large combining network (large MN) may lead to very small output impedance and degrade the whole PA performance. In this case, other combining topologies which can combine the Z_d for all DAs in serial may be used, which generates output impedance of $Z_{out} = MZ_{dk}/N$ instead, thus relaxing the stress on output matching. This is the case for transformer combiners.

In summary, selections and design iterations may be made to choose the most suitable power combining topology. Note in Section 4.9, zero-degree power combiner is selected for parallel combining in one single-ended PA prototype with

a small 2×2 combining network; while in Sections 4.10 and 4.11, transformers are further implemented in differential PA prototypes with larger combining networks.

4.6.3 Differential design

The aforementioned 2D distributed power combining topology in Fig. 4.8 is implemented in single-ended manner. However, due to the single-ended topology with large matching network deployed, the benefit to achieve wideband high-density power combining is not fully demonstrated.

In this section, we introduce a differential 2D power combining network for 60GHz PA design in 65nm CMOS with further improved output power density. As discussed in Section 4.6.2, transformer matching and neutralization capacitor are also deployed to enable larger power combining network with further improved PA performance.

Figure 4.10 Differential version of proposed SEDFDA PA topology based on 2D distributed power combining network with the use of CRLH ZPSs.

With the use of differential CRLH T-line based ZPS designed in Section 3.2.3, one differential 2D power combining network can be realized as shown in Fig. 4.10, with benefits of reduced area due to merged parallel inductors and the elimination of de-coupling capacitors. Moreover, loss is also reduced due to confined EM field and nullified parasitic at virtual ground in the differential topology. In addition, the differential topology also allows easy implementation of techniques such as transformer matching and neutralization capacitor. Transformer matching provides DC isolation with easy biasing and compact area. Neutralization capacitor improves stabilization, simplifies matching, and also boosts gain with minimized external loss.

There are, however, two design challenges for the proposed differential topology. First, for a differential implementation, it is desired to design the circuit as symmetric as possible. An asymmetric implementation would cause mismatch in the differential signals and degrade the pre-mentioned benefits. However, since transistor pairs, differential ZPS, and differential input and output terminals are all connected together, it is almost impossible to have a fully symmetric implementation. Second, the input and output terminals in Fig. 4.10 are on the same side of the power combining network. This would lead to long overlapped interconnection, which severely increases parasitic and degrades performance.

Figure 4.11 The proposed layout for differential 2D power combining network.

To solve the abovementioned problems, one novel differential 2D power combining network is proposed in Fig. 4.11. For each differential gate-line and drain-line, the differential ZPS is implemented in the first distributed stage only. The differential signals then flow into separate directions to 2 single-ended ZPSs on both sides. In this way, the differential topology can be maintained highly symmetrical, while input and output terminals are placed on opposite sides of the power combining network. Though some of the ZPSs are realized single-ended, the whole topology is still differential, allowing techniques such as transformer matching and neutralization capacitor towards compact matching and stabilization.

4.7 Stabilization Techniques

Stability is an important concern for all amplifier designs. Normally, additional circuit components or special amplifier topologies are required which either degrade PA's performance or have more stringent system requirements. In this section detailed analysis is provided for PA stabilization methods at mm-wave frequencies and possible solutions to minimize the risk of instability while maintaining PA performance from degradation.

4.7.1 Common PA Stabilization Techniques

4.7.1.1 Neutralization

In mm-wave region, parasitic capacitance between transistor's gate and drain terminals forms a feedback loop in common source amplifiers, which degrades both power gain and stabilization. For differential topology, neutralization technique has been widely used recently [59, 79-81] to neutralize the feedback signal by introducing a negative path from drain of one differential transistor to the gate of the other transistor. As shown in Fig. 4.12, by introducing neutralization capacitors C_{neu} with similar capacitive coupling as the parasitic gate-drain capacitance C_{gd} , the feedback from the differential outputs cancel each other, and the PA can therefore be stabilized.

Figure 4.12 Neutralization technique for PA stabilization.

Neutralization technique is widely used recently for differential PA due to several advantages. Firstly, the topology is very simple. Only two very small capacitors are required with almost no layout overhead. Secondly, by neutralization of the feedback from C_{gd} , S_{12} of PA approaches 0. The amplifier becomes near unilateral, thus making input and output matching independent of each other, which greatly simplifies the matching process. Thirdly, C_{neu} actually introduces a positive feedback loop. By properly choosing C_{neu} value, in addition to achieving stabilization, the gain of PA can be slightly boosted.

However, neutralization technique does have some limitations. Firstly, this technique is sensitive to process variation because the PA is only stable within a small region of C_{neu} values. In fact, with a large C_{neu} value the topology shown in Fig. 4.12 becomes a cross-coupled transistor pair commonly used in VCO to generate negative resistor. As a result, the PA becomes a VCO. Secondly, due to additional capacitance loaded on the transistors, the parasitic of transistors almost doubled. This effect is more significant for input matching and for more advanced technology, as the gate impedance locates near the edge of Smith Chart, making the impedance matching narrow band.

4.7.1.2 Cascode

Cascode topology is commonly used at lower frequency regions for stabilization. It also helps to reduce miller effect from C_{gd} and improve power gain. In addition, cascode topology also shows advantage for advanced technology with low break-down voltages. Due to serial connection of transistor junctions, a higher supply voltage can be used, thus increasing the achievable output power. However, as frequency pushes higher, the large capacitance at the source of cascode transistor ($C_{gs}+C_{gd}$) would cause performance degradation. A matching network such as a serial inductor L_s can be added between the cascode transistor and the common-source transistor [73, 82]. As shown in Fig. 4.13, the added inductor (L_s) resonates out the two parasitic capacitors (C_{gs} and C_{gd}) by forming a low pass filter. The penalty is additional area and loss introduced by the serial inductor. A hybrid design is commonly used where the previous stages are realized by cascode for stability and higher gain, while the power combining stage is realized by common source topology for better efficiency [73], which however requires multiple supply voltage levels. Nevertheless, at 60GHz, normal cascode topology can still function properly without inserted matching network, and is used to achieve a higher output power with the requirement of a higher supply voltage such as 2V [27, 72, 83-85].

Figure 4.13 Cascode topology for PA stabilization.

4.7.1.3 RC network

The most conventional technique for PA stabilization is to use RC network [67, 71]. As shown in Fig.4.14, with serial or parallel RC networks, high and low frequency regions can be stabilized, respectively. More specifically, a parallel RC network put in serial connection forms a high pass topology, with larger serial resistance introduced at lower frequency region, thus stabilizing the low frequency. Similarly, a serial RC network put in parallel connection forms a low pass topology, with smaller parallel resistance introduced at higher frequency region, thus stabilizing the high frequency. These stabilization techniques can be used by itself or work together with other techniques. Its penalty is obvious. To achieve a targeted stabilization level, additional losses are often introduced in the operating region, degrading PA's power gain and efficiency.

Figure 4.14 RC networks for PA stabilization.

4.7.1.4 Technique selection

Three stabilization techniques are summarized above. There are other stabilization techniques. For example, by properly designing the matching network, the PA can be stabilized without using additional devices [26, 65]. However, as the matching needs to take stabilization into design consideration, the performance of PA may not be fully optimized.

Based on above analysis, neutralization technique shows the best performance without additional requirements and is selected in this work. Although other

techniques such as cascode topology and RC network may be less sensitive to process variation, additional performance penalties or system requirements can be caused.

In addition to above introduced stabilization techniques, automatic digital control could also be used to mitigate PVT-variations [86, 87]. In the following section, a power detector is implemented to quantify the output power level with a DC signal. This DC signal could then be used for possible self-healing or automatic digital control of PA.

4.8 Digital Control

As mentioned above, automatic digital control could also be used to mitigate PVT-variations [86, 87]. High frequency in mm-wave region and scaled CMOS transistor size below 100nm make transistor performance susceptible to process variation and make accurate modeling of both active and passive elements very challenging. Furthermore, power amplifier consumes large DC power and normally generates a high temperature variation. All these variations would cause the power transistor deviate from its optimal operating point, which degrades performances such as output power, efficiency, linearity, gain and stability. Furthermore, the operating environment is also likely to vary, such as the variation of antenna load impedance. Aging is another concern, where transistor performance would gradually change with time. Automatic digital control provides solutions to all above issues. With a feedback loop designed for self-healing, the PA biasing and matching can be automatically tuned for optimal performance.

Except to maintain optimum PA performance, another important function which can be provided by automatic digital control is to prevent circuit destruction [88]. The low breakdown voltage provided by scaled CMOS technologies makes transistors vulnerable to environment change. For example, a mismatch in antenna load impedance may cause a peak voltage higher than the breakdown voltage. With automatic digital control, biasing point of transistor can be monitored and controlled in the safe region, and emergency shutdown can also be provided.

Furthermore, external testing contributes a large portion of expense for circuit production. With the help of on-chip feedback and digital control, a built-in self-test (BIST) mechanism can be provided which is much cheaper [86].

In this thesis, digital control is explored and implemented for another purpose, which is the power back-off.

4.8.1 Power Back-off in PA

Power back-off is often required for PA to conserve battery power, avoid interference with adjacent channels, and fulfil linearity requirement for adopted modulation scheme [89-91]. The power back-off is usually realized from baseband side by reducing input power to PA. Note that the high output power efficiency region for PA normally locates near P_{1dB} and P_{sat} points. When input power reduces, the PA operating point is pulled away from the high efficiency region, leading to a large power waste, which is even worse for CMOS PA design at 60GHz. To maintain high output power efficiency, digital control can be introduced in PA design with back-off realized by self-tuning, which reduces the PA output power along with DC power to maintain a high efficiency.

There are many techniques to enhance PA output power efficiency for back-off. A few were successfully implemented at 60GHz and beyond [79, 89-91]. Architectures such as Doherty amplifier, out-phasing, and envelope elimination and restoration (EER) show boosted back-off efficiency at low frequency regions, but have high design complexity or large power consumption from digital data pre-processing [91]. Multi-mode operation by turning on and off different number of PA units is another popular technique at low frequency [92-98], but with two critical design issues at high frequency: power leakage to the PA units that are switched off, and mismatching due to the impedance variation of PA units at different modes [89]. There are two recent works [79, 89] with successful implementations of multi-mode operation at 60GHz. The work in [79] tunes the matching by shorting part of power combiner, but the obtained PAE for low power mode has a large degradation compared with high power mode. The work in [89] isolates the PA units in power-off mode by implementing a bulky quasi-quarter-wavelength transmission line to prevent current leakage.

In this work, power back-off is realized by controlling the current biasing of transistors without PA switched off during power back-off. It thus avoids the power leakage and impedance mismatch issues in [79, 89]. As DC power consumption is reduced along with output power, high output power efficiency can be maintained.

4.8.2 Power Detection

On chip power detection is widely used in mm-wave regions [86-88, 99, 100]. In addition to providing dynamic bias control so as to mitigate the effect of process, voltage and temperature variations (PVT-variations) [86, 87], it can also be used to cope with antenna impedance mismatch [86, 88], realize low-cost on-chip built-in self-test (BIST) [86, 99], and provide VSWR protection with consideration for transistor breakdown and system overload by offering protection mechanisms such as emergency shutdown [86].

As shown in Fig. 4.15, a power detection unit is normally formed by two parts: power coupler which senses the output power level, and power detector which transfers the sensed signal's power level to a DC signal. Different topologies are analyzed and designed in this section for power coupler and power detector, respectively.

Figure 4.15 *Power Detection Unit.*

4.8.2.1 Power Coupler

Power coupler senses the output power by coupling fraction of the output signal. In mm-wave regions, two types of power couplers are found in literature. The first type (Fig. 4.16(a)), which is also the more common one, is to use a capacitive coupling from the transmission line feeding to the output port [86, 88, 99]. The capacitive coupling level is usually designed low so that the output level is merely affected. The coupled signal often goes underneath of T-line (and its ground if it's CPW topology) and suffers more loss from substrate. Considering the low coupling level, the sensitivity of power detection is low. The second type of power coupler (Fig. 4.16(b)) is proposed in [100], with the power coupler merged into the DAT power combiner. The power coupling is achieved through direct line connection. As a result, the output power level would be affected, and the input impedance for power detector must be considered as part of the output matching network. The benefit is the easy connection to power detector and high sensitivity of the power detection unit.

Figure 4.16 Power Coupler topologies: (a) capacitive coupling from output [86, 88, 99]; (b) direct connection from output [100].

In this work, power detection is designed with the objective to control the DC power along with output power and improve PA efficiency during power back-off. Therefore, the degradation on output power level caused by power detection needs to be minimized, while the sensitivity requirement on power detection is not critical and can be relaxed. As a result, the first type of power coupler is selected.

The designed layout is shown in Fig. 4.17. A metal-plate capacitor is implemented at the conjunction of a two-branch combiner. The combiner is implemented at top metal level, and the coupled signal is fed to power detector through the second top metal level. Since micro-strip topology is adopted for transmission line design, the resulted power coupler is very compact.

Figure 4.17 Designed capacitive power coupler.

4.8.2.2 Power Detector

In mm-wave region, square-law power detector is commonly used for on-chip applications [86, 88], with the simplified schematic shown in Fig. 4.18. Coupled signals are fed into differential transistor pair Mn1 and Mn2, with their output terminals connected together. With an input signal of $V_{IN} \pm V_{ac} \cos \omega t$, the combined current flowing through the two transistors ($I_{d1} + I_{d2}$) can be approximated with a simple square-law equation for CMOS transistors:

$$\begin{aligned}
 I_{d1} + I_{d2} &= K_n \left(2\overline{V_{eff}}^2 + 2V_{ac}^2 \cos^2 \omega t \right) \\
 &= K_n \left(2\overline{V_{eff}}^2 + V_{ac}^2 \cos 2\omega t + V_{ac}^2 \right)
 \end{aligned}
 \tag{4-8}$$

where $\overline{V_{eff}} = V_{IN} - V_{th}$ is a offset which can be canceled though current mirror. K_n is the coefficient in square-law equation for NMOS transistors Mn1 and Mn2. The amplitude of ac signal is represented by V_{ac} .

Figure 4.18 Square-law power detector.

When this current is mirrored through the low pass filter, the high frequency term $V_{ac}^2 \cos 2\omega t$ is filtered out. As a result, the output current I_{out} becomes proportional to V_{ac}^2 , which represents the power level of the ac signal (P_{ac}):

$$(4-9) \quad I_{out} \propto V_{ac}^2 \propto P_{ac}.$$

As a result, the power level of input signal is detected and represented by the DC level at output terminal.

Figure 4.19 Designed single-ended square law power detector.

In this work, however, the output signal is single-ended, and so is the sensed signal from power coupler, as shown in Fig. 4.17. Therefore, the design in Fig. 4.18 is modified to single-ended, as shown in Fig.4.19. Although the fundamental and odd harmonics of AC signal can no longer cancel each other as the differential power detector does, they can still be filtered out by the low pass filter as the 60GHz operating frequency is far away from DC.

4.8.3 Digital Control System

The implemented digital control system is shown in Fig. 4.20. The power level of PA output is detected by an on-chip power detector, and is converted to a digital signal through an ADC that returns a digital input to configure the PA biasing current, which in turn controls the gain and power consumption of PA. The power detection unit, 3-bit ADC/DAC are realized on-chip, while digital signal processing is implemented off-chip. Detailed block designs are shown in the following section.

Figure 4.20 Designed digital control system.

4.8.4 Circuit Design

Detailed circuit designs for digital control blocks such as power detection unit, 3-bit ADC/DAC, as well as the power amplifier design are presented in this section.

4.8.4.1 Power Detection Unit

As discussed in Section 4.8.2, the design shown in Fig. 4.17 is used for power detection with minimized degradation on PA's output power performance.

4.8.4.2 3-Bit ADC

A flash ADC topology is adopted in this work for its simple topology. As Fig. 4.21(a) shows, the 3-bit flash ADC contains a resistor-array to generate reference voltages, 7 comparators to convert the analog input to digital signal, and a 8-to-3 encoder to convert the 7-bit thermometer code (D7D6D5D4D3D2D1) to 3-bit digital output (Q2Q1Q0).

Figure 4.21 ADC design: (a) flash ADC topology; (b) resistor array to generate reference voltage.

The layout for the resistor array is shown in Fig. 4.21(b), with 16 serial-connected resistors to generate 7 specific reference voltages from given power supply. Dummy resistors are used to reduce variation between resistor values.

Seven comparators are used to compare the analog input from power detector and each reference voltage, generating a 7-bit digital thermometer code. Due to different voltage levels of reference voltages, two types of comparators are designed, as shown in Fig. 4.22. N-type comparator with NMOS input transistors is used to compare higher level inputs, while p-type comparator with PMOS input transistors is used to compare lower level inputs.

Figure 4.22 Comparator topologies for ADC design: (a) n-type; (b) p-type.

The obtained 7-bit thermometer code (D7D6D5D4D3D2D1) is then converted to 3-bit digital output (Q2Q1Q0) with a 8-to-3 encoder. The layout is designed based on NAND gate and invertors, as shown in Fig. 4.23. The formula for the encoder is as follows:

$$\begin{cases} Q0 = \overline{D6} \cdot (\overline{D4} \cdot (\overline{D2} \cdot D1 + D3) + D5) + D7 \\ Q1 = \overline{D5} \cdot \overline{D4} \cdot (D2 + D3) + D6 + D7 \\ Q2 = D4 + D5 + D6 + D7 \end{cases} \quad (4-10)$$

Note the digital inputs DX ($X = 1 \sim 7$) and their inverts $\overline{DX}$ are passed to the encoder through transmission gates and invertors to ensure the similar time delay.

Figure 4.23 8-to-3 encoder for ADC design: (a) $Q0$, (b) $Q1$, (c) $Q2$.

4.8.4.3 3-Bit DAC

The DAC is used to control the PA's biasing current based on input digital signals. A simple comparator is designed to switch different biasing currents. As shown in Fig. 4.24, by using 3 comparators, the obtained biasing current I_b can be controlled by the DAC inputs:

$$I_b = I_{ref} \times (4 \cdot DAC3 + 2 \cdot DAC2 + 1 \cdot DAC1). \quad (4-11)$$

where DAC3, DAC2, and DAC1 are the 3-bit digital input, with which the biasing current can be varied from I_{ref} to $7I_{ref}$.

Figure 4.24 DAC topology.

4.9 60GHz PA Prototype with Single-Ended 2×2 Power Combining

One 60GHz PA prototype with proposed 2D distributed power combining is implemented in UMC 65nm logic and mixed-mode low leakage low-K CMOS technology with 6-metal layers (1 thick metal layer). The circuit is designed and verified by EM simulation (ADS-Momentum) before fabrication.

Figure 4.25 Schematic of 2-stage PA with a 2×2 distributed power combining network.

4.9.1 60GHz PA design

With ZPS designed and characterized in Section 3.2, the proposed 2D distributed power combining network is implemented in a PA for demonstration [101]. As shown in Fig. 4.25, a 2-stage PA is designed with a single transistor in the 1st-stage as driver; and a 2×2 distributed power combining array in the 2nd-stage, which has 2 power-combining branches and each branch has a 2-stage SEDFDA. All transistors are in single-ended common-source topology with transistor size of $64 \times 1 \mu\text{m}/60\text{nm}$. With a biasing current of 22mA, the simulated f_i is 172GHz. The parasitic capacitances from transistor gate and drain are absorbed during the ZPS design to realize the distributed amplification. As a result, the shunt inductor (L_p) in Fig. 3.4(b) is resized to single loop. Notice the size of L_s in the gate line is smaller than in the drain line due to a larger parasitic capacitance at transistor gate.

The power combiner implemented in the 2nd stage only has 2 branches, mainly to due to limitation of tape-out area. More branches can be used to enhance the power performance. Moreover, CPW transmission lines are used as parallel inductors for matching and DC biasing at the same time, therefore no additional biasing circuit is required.

Figure 4.26 Simulated and measured S parameters of PA under 1.2V supply.

4.9.2 Simulation and measurement results

Circuit simulation is done in both Cadence and ADS. The chip is measured on a CASCADE Microtech Elite-300 probe station and Agilent PNA-X (N5247A) with frequency-sweep up to 110GHz. Measurement for PA power performance is done at the center frequency (52GHz) with pads de-embedded.

Figure 4.26 shows the simulated and measured S parameters. An open-short de-embedding was performed to obtain the results. From simulation, the maximum gain is at 56.3GHz with 11.3dB. A 3dB bandwidth of 21GHz is achieved (40.3GHz ~ 61.7GHz). At 60GHz, a 9.8dB gain is obtained. The measured gain, on the other hand, has a peak value of 8.3dB at 52GHz. The 3dB BW is 16GHz (44 to 60GHz). Compared with simulation, the center frequency is not shifted much, but power gain drops 3dB and bandwidth shrinks 5GHz. Output matching confirms with the simulation while degradation occurs at the input matching. This input mismatch may be due to lack of device modeling, and can be used to justify the reduction of power gain.

Figure 4.27 Reverse isolation and stability of PA under 1.2V supply.

The measured reverse isolation and stability for PA are shown in Fig. 4.27. The circuit is unconditionally stable from DC to 110GHz, with reverse isolation better than -25dB over the entire range.

In addition, Fig. 4.28 shows the measured power performance at center frequency (52GHz). With 1.2V supply, OP_{1dB} of 9.7dBm and P_{sat} of 11dBm are

achieved. PAE drops to 7.1%. Note that both PAE and output power are limited by the number of power combining branches and distributed stages, and can be further improved when a larger 2D power combining network is employed, as will be demonstrated by following sections.

Figure 4.28 Measured power and PAE of PA at 52GHz under 1.2V supply.

Furthermore, Table 4.1 summarizes the presented work with comparison to the state-of-art 2-stage CMOS PAs at 60GHz. Comparison shows that the proposed PA can achieve the state-of-art performance for all FOMs.

Table 4.1 Comparison of state-of-art 2-stage 60GHz CMOS PAs

	This Work	[27]	[65]	[66]	[67]
Tech. (CMOS)	65nm	65nm	45nm	90nm	90nm
Supply (V)	1.2	1.2	1.1	1	1
Gain (dB)	8.3	14.3	6	8.2	5.6
OP_{1dB} (dBm)	9.7	11	11	10.1	9
P_{sat} (dBm)	11	16.6	13.8	11.6	12.3
PAE (%)	7.1	4.6	7	11.5	8.8
BW_{-3dB} (GHz)	16	15	19	13	22
Area (mm²)	0.39	0.46*	0.06*	1.03	0.25

*excluding pads

Lastly, Fig. 4.29 shows the chip micrograph. Including pads, the PA occupies an area of 0.39 mm², which is quite compact when compared to the traditional

design with the use of T-line. Note that the upper part of the photo is the 60GHz PA with 2×2 power combining network. The lower part of the photo is the de-embedding structures used to characterize the CRLH T-line based zero-phase-shifter.

In summary, the presented simulation and measurement results have demonstrated the feasibility of the proposed 2D distributed power combining as well as the implementation of metamaterial in mm-wave region by 65nm CMOS technology.

Figure 4.29 Die micrograph with block illustrations.

4.1060GHz PA Prototype with Differential 2×4 Power Combining

The proposed 2D power combining network with the use of CRLH T-line based ZPS is demonstrated in above section, proving its feasibility for 60GHz CMOS PA design. However, due to the single-ended topology with large matching network

deployed, the benefit to achieve wideband and high output power density is still not fully demonstrated. In this prototype, a differential power combining network introduced in Section 4.6.3 is implemented in 65nm CMOS technology with improved performances in both power density and bandwidth [36].

4.10.160GHz PA design

Differential CRLH T-lines presented in Section 3.2.3 are first designed and implemented in both gate and drain lines in the 2D active CRLH T-line network to obtain zero-phase-shift with circuit and layout diagrams shown in Fig. 4.30. The parasitic capacitances from transistor gate and drain are absorbed in ZPS design. The designed CRLH T-lines can realize zero-phase shift at 60GHz with compact size of $61\mu\text{m} \times 81\mu\text{m}$ and $76\mu\text{m} \times 81\mu\text{m}$ in gate and drain lines, respectively. Note a smaller L_p is implemented in gate line compared to drain line due to larger parasitic capacitance on transistor gate compared to transistor drain.

Figure 4.30 On-chip implementation of CRLH T-line (metamaterial) to realize zero-phase shift in standard CMOS technology for the 60GHz PA prototype with differential 2×4 distributed power combining network.

With the designed differential ZPS, one 3-stage PA is implemented with the central frequency at 63GHz in 65nm CMOS from Global Foundries 1P8M RF CMOS technology, as shown in Fig. 4.31. The first 2 stages work as drivers; and a 2×4 distributed power combining array is in the 3rd-stage, which has 2 power-combining branches with each branch being a differential 2-stage distributed PA.

Each transistor is in a common-source (CS) topology with size of $30 \times 1 \mu\text{m}/60\text{nm}$ for the first stage; and $60 \times 1 \mu\text{m}/60\text{nm}$ for second and third stages. With a biasing current of 14mA, the simulated f_{max} for the $60 \mu\text{m}$ transistor is 231GHz. After adjusted in-phase by ZPS, all horizontal distributed amplification branches are vertically combined by transformers, which simultaneously perform the impedance transformation. Under the differential structure, transformers are also adopted for inter-stage matching. Note one additional compact matching network is used for inter-stage matching between 2nd and 3rd stages, which may be merged into the differential ZPS design in the gate line to further reduce area and loss. Moreover, the stabilization is realized by compact neutralization capacitors.

Figure 4.31 Schematic of 3-stage differential PA with differential 2×4 distributed power combining network.

4.10.2 Simulation and measurement results

The design is verified by EM simulation (ADS-Momentum) before fabrication. Figure 4.32 shows the chip micrograph with an active area of 0.268mm^2 . It is measured on CASCADE Microtech Elite-300 probe station and Agilent PNA-X

(N5247A) with frequency-sweep up to 110GHz. Measurement is done at the center frequency (63GHz) with pads de-embedded.

Figure 4.32 Die micrograph of PA with 2D power combining network by zero-phase-shifter.

Figure 4.33 The measured S parameters of PA and its stability factor with center frequency (63GHz) under 1V supply.

Figure 4.33 shows the measured S parameters with an open-short de-embedding performed. One can observe that the power gain S21 is 13.2dB at 63GHz with the 3dB bandwidth of 20GHz (53 to 73GHz). The PA is unconditionally stable over entire measured frequency range.

Figure 4.34 The measured output power and PAE of PA at center frequency (63GHz) under 1V supply.

Figure 4.34 shows the measured power performance at 63GHz. Output power OP_{1dB} of 13dBm and PAE of 8.7% are achieved with 1V supply. Note that the output power performance can be further improved with more branches combined compactly.

Table 4.2 Performance Summary for the implemented 60GHz CMOS PA Prototype with Differential 2×4 Power Combining

Technology (nm)	65
Supply (V)	1
Gain (dB)	13.2
OP_{1dB} (dBm)	13
P_{sat} (dBm)	13.4
Peak PAE (%)	8.7
BW_{-3dB} (GHz)	20
Area (mm²)	0.268

Table 4.2 summarizes the performance of the proposed PA, which demonstrates a wideband high-density power combining. The performance will be compared with the state-of-art together with the next PA prototype in next section.

4.11 60GHz PA Prototype with Differential 4×4 Power Combining and Digital Control

To further improve output power, this section presents another 60GHz PA prototype with its combining network size increased to 4×4. Though the bandwidth is reduced a bit due to much longer signal lines in the output matching network, the 7GHz spectrum band at 60GHz can still be fully covered. Meanwhile, the output power and output power density are further improved, achieving the state-of-art. Both circuits are designed and verified by EM simulation (ADS-Momentum and EMX). Furthermore, the digital control loop shown in Fig. 4.20 is implemented for PA design to enhance efficiency during power back-off.

Figure 4.35 On-chip implementation of CRLH T-line (metamaterial) to realize zero-phase shift in standard CMOS technology for the 60GHz PA prototype with differential 4×4 distributed power combining network.

4.11.1 60GHz PA design

The designed differential CRLH T-line based ZPSs implemented in both gate and drain lines are shown in Fig. 4.35, with the parasitic capacitances from

transistor gate and drain absorbed in ZPS design. The designed CRLH T-lines can realize zero-phase shift at 60GHz with compact size of $49\mu\text{m}\times 76\mu\text{m}$ and $50\mu\text{m}\times 72\mu\text{m}$ in gate and drain lines, respectively.

Figure 4.36 EM simulation results of both loaded CRLH T-line and loaded $\lambda/2$ T-line for comparison. Slower S21 phase change of CRLH T-line indicates wider bandwidth, while the dB(S21) plot indicates lower loss. The dB(S11) plot shows wideband matching.

Figure 4.36 further compares the performance between zero-phase CRLH T-line and traditional RH $\lambda/2$ T-line with transistor parasitic capacitance and loss absorbed into design. As the top figure shows, as frequency changes, the phase shift in zero-phase CRLH T-line varies much slower than $\lambda/2$ T-line. For example, a phase change within $\pm 10^\circ$ can be maintained in 14GHz frequency range (53GHz to 67GHz) in the designed zero-phase CRLH T-line, while in $\lambda/2$ T-line it can only be maintained in 4.5GHz range (57.5GHz to 62GHz). In other words, zero-phase CRLH T-line can provide a much wider band performance than $\lambda/2$ T-line. The insertion loss is also compared in the lower figure. By absorbing parasitic capacitance and loss from transistor, the zero-phase CRLH T-lines show insertion

loss below 0.9dB and 1.4dB in 50GHz to 70GHz frequency range in the gate line and drain line, respectively, while $\lambda/2$ T-line contributes more than 3dB loss in both gate and drain lines. In conclusion, the implemented on-chip differential zero-phase CRLH T-line demonstrates much more compact size, wider bandwidth and lower loss than $\lambda/2$ T-line.

The PA implementation is shown in Fig. 4.37 with 3 stages and 58GHz as the central frequency. The first 2 stages work as drivers; and a 4×4 distributed power combining array is in the 3rd stage, which has 4 power-combining branches with each branch being a differential 2-stage distributed PA. Same transistor topology, size and biasing are adopted as the PA prototype presented in Section 4.10. As 4 branches are combined in parallel at the output instead of 2 branches, matching to 50Ω at output node would require 200Ω in each branch, which cannot be provided by on-chip T-line. As a result, signal distribution lines are absorbed into the output matching network, which reduces the PA bandwidth due to its long length.

Figure 4.37 Schematic of the 60GHz PA prototype with 3 stages and differential 4×4 distributed power combining network at 3rd stage.

Neutralization technique is used to boost PA's performance while ensuring stability. The risk of mismatch and performance degradation due to sensitivity of neutralization capacitor to process variation is minimized by adopting multiple large-value capacitors connected in serial. Since the capacitance of each capacitor is much larger than a single neutralization capacitor, its sensitivity to variation can be reduced.

The digital control system designed in Section 4.8 is integrated for this PA implementation to facilitate power back-off with enhanced efficiency. The system view for the digital control loop is shown in Fig. 4.20, where the output power level is sensed by a power coupler and converted to DC signal through a power detector. The detected signal is further converted to digital signal through a 3-bit ADC and passed to off-chip signal processing. The feedback digital signal is then converted to analog signal through a 3-bit DAC to control PA's biasing. The capacitive power coupler designed in Fig. 4.17 is selected to minimize the effect of power detection on PA's output power performance. The single-ended square law power detector designed in Fig. 4.19 is adopted to fit the single-ended PA output. The circuit designs for 3-bit ADC and 3-bit DAC have been discussed in Section 4.8.4.

Figure 4.38 Simulated voltage swings on both distributed stages in gate line and drain line of designed 2D distributed power combiner. Similar voltage magnitude indicates simultaneous power optimization for each transistor, while similar phase indicates in-phase power combining.

4.11.2 Simulation and measurement results

4.11.2.1 Simulation results

Figure 4.38 shows simulated voltage swings on transistor gate and drain of both distributed stages of the implemented differential 2D power combining network at 60GHz. As the figure shows, both gate and drain voltage swings have almost the same phase and amplitude in two distributed stages. As a result, the power performance of transistors in distributed amplifier can be optimized simultaneously and in-phase combined in series, thus improving the power gain and efficiency of the whole distributed amplifier.

Figure 4.39 Die micrograph of the 60GHz PA prototype with differential 4×4 distributed power combining network.

4.11.2.2 PA on-chip measurement results

The fabricated PA is measured on CASCADE Microtech Elite-300 probe station and Agilent PNA-X (N5247A) with frequency-sweep up to 110GHz. Measurement is done at the center frequency with pads de-embedded. Open-short is used for de-embedding.

Figure 4.40 The measured S parameters of the PA prototype and its stability factor under 1.2V supply. The PA achieves 17.5dB power gain at 58.3GHz with 8.8GHz bandwidth.

Figure 4.39 shows the chip micrograph with active area of 0.48mm^2 . Figure 4.40 shows the measured S parameters. The power gain (S_{21}) is 17.5dB at 58.3GHz with -3dB bandwidth of 8.8GHz (54 to 62.8GHz). The PA is unconditionally stable from DC to 110GHz.

Figure 4.41 shows the measured power performance at centre frequency (58.3GHz). With a power supply of 1.2V, $OP_{1\text{dB}}$ of 15.9dBm and P_{sat} of 16.6dBm are achieved. The peak PAE is 9.74%. Figure 4.42 further shows the measured power performance at 60GHz band (57~64GHz). Over the entire 60GHz band, $>15\text{dBm}$ $OP_{1\text{dB}}$ and $>16\text{dBm}$ P_{sat} are observed. The peak values for $OP_{1\text{dB}}$ and P_{sat} are 16.6dBm and 17.2dBm, respectively. The PAE maintains above 8% for the entire 60GHz band with a peak value of 11.3%.

Figure 4.41 The measured output power and PAE of the PA prototype at center frequency (58.3GHz) under 1.2V supply. The PA achieves 15.9dBm OP_{1dB} , 16.6dBm P_{sat} and peak PAE of 9.74%.

Figure 4.42 Measured power performance of the PA prototype over 60GHz band (57~64GHz), where $>15 \text{ dBm}$ OP_{1dB} and $>16 \text{ dBm}$ P_{sat} are observed with peak values of 16.6dBm and 17.2dBm, respectively. The peak PAE maintains above 8% with a peak value of 11.3%.

For 60GHz communication, high-order modulation requires linearity, indicated by OP_{1dB} . The measured output power performance of both PA prototypes presented in this section and Section 4.10 are compared with state-of-art in Fig. 4.43 in terms of both output power (OP_{1dB}) and also output power density (OP_{1dB}/Area). Note that PA with a higher output power (OP_{1dB}) tends to have a

lower output power density ($OP_{1dB}/Area$) due to extra loss and area. As Fig. 4.43 shows, the proposed power combining with 4 branches can achieve the state-of-art power performance for both OP_{1dB} (16.6dBm) and $OP_{1dB}/Area$ (95.2mW/mm²). The work in [26] achieves a higher output power with 4-way Wilkinson power combiners that lead to a large area and hence lower output power density. The work in [102] achieves a higher output power with combination of 16 branches by T-lines and transformers, which largely degrades the output power density. On the other hand, the work in [71] realizes higher output power density, but distributed-active-transformer (DAT) topology limits the number of combined transistors, which leads to a lower output power.

Figure 4.43 Power performance (OP_{1dB} and $OP_{1dB}/Area$) comparison of both differential PA prototypes with 2×4 and 4×4 power combining networks with state-of-art 60GHz CMOS PAs.

Table **Error! Not a valid bookmark self-reference.** summarizes the performance of both PA prototypes presented in this section and Section 4.10 with comparison to the state-of-art CMOS PAs at 60GHz with various power combining methods. Both proposed 2×4 and 4×4 distributed power combining with metamaterial-based zero-phase-shifter can achieve performance comparable to the state-of-art. The 2×4 PA prototype realizes 13.2dB power gain, OP_{1dB} of 13dBm, P_{sat} of 13.3dBm, peak PAE of 11.3%, with a very wide 20GHz bandwidth (53 to 73GHz). With a compact core area of 0.268mm², output power density of 74.5 dBm mm⁻² is achieved. The 4×4 PA prototype realizes 17.5dB power gain, 8.8GHz bandwidth and peak PAE of 11.3%. Most importantly, the 4×4 PA

prototype realizes 16.6dBm output power with 95.2mW/mm² output power density, indicating the top output power performance for CMOS PA at 60GHz towards effective short-range communication.

Table 4.3 Comparison of Both 60GHz CMOS PA Prototypes (PA1: with 2×4 Power Combining, PA2: with 4×4 Power Combining) and State-of-Art CMOS PAs at 60GHz with High Output Power by Various Power Combining Methods

	RFIC '09 [66]	TMTT '09 [74]	ISSCC '10 [100]	ISSCC '10 [26]	ISSCC '11 [71]	TMTT '12 [103]	RFIC '12 [104]	TMTT '13 [89]	RFIC '13 [102]	PA1	PA2
Technology (nm)	90	90	65	90	65	65	65	90	40	65	65
Supply (V)	1	3	1	1.8	1	1	1.2	1.2	1.2	1	1.2
Gain (dB)	4.4	26.6	19.2	20.6	20.3	20	20	15.7	29	13.2	17.5
OP_{1dB} (dBm)	12.1	14.5	15.1	18.2	15	12.5	13.5	14.7	17	13	16.6
P_{sat} (dBm)	14.2	18	17.7	19.9	18.6	16	15.6	18.5	22.6	13.4	17.2
Peak PAE (%)	5.8	12.2	11.1	14.2	15.1	6.6	6.6	10.2	7	8.7	11.3
BW_{-3dB} (GHz)	9.5	16	8	8	9	5	7	5.8	N.A.	20	8.8
Core Area (mm²)	0.47	0.55	0.83	1.03	0.21	1.47	1.26	0.39	2.16	0.27	0.48
OP_{1dB}/Area (mW/mm²)	34.6	51.2	39	64.1	150.6	12.1	17.8	76.7	23.2	74.5	95.2
Combiner Topology	4-way SE	DAT, 2-way diff.	4-way diff.	4-way SE	DAT, 2-way diff.	2-way SE	DAT, 4-way diff.	4-way diff.	8-way diff.	2x4 network	4x4 network

diff.: differential; SE: single-ended

4.11.2.3 Digital control loop measurement results on PCB

The digital control loop is also measured to test its functionality. As shown in Fig. 4.44(a), the output power level of PA is controlled by a 3-bit DAC with 8 modes. Mode 0 turns off the PA completely. Mode 1 to 7 varies PA's output power at center frequency (58.3GHz) from 10 to 15dBm. Note 1 or 2 dB drop in output power is observed compared to on-chip PA measurement since PCB bonding is used for digital control measurement, which provides degraded ground condition with lower supplied DC current. However, the improvement on PA efficiency

during power back-off is fully demonstrated. As shown in Fig. 4.44(a), the drain efficiency of PA is plotted, which varies from 8% to 5% during power back-off. For a fair comparison, another drain efficiency curve is plotted by varying the input power to PA with DAC turned off to achieve the same output power level. As shown in Fig. 4.44(a), though PA with DAC control also shows degradation in efficiency during power back-off due to deviation of biasing from optimum point as mentioned in Section 4.8.1, the efficiency is still largely improved compared with PA without digital control. For example, an improvement of 175% (by dividing the two drain efficiency values) is achieved for PA efficiency at Mode 1. The improvement on drain efficiency at different frequencies for different DAC modes and thus different back-off levels is further summarized in Fig. 4.44(b). An improvement from 170% to 190% is obtained at Mode 1 for the whole 60GHz band.

Figure 4.44 DAC control of PA output power and improved efficiency during power back-off. (a) Comparison of drain efficiency during power back-off for PA with and without DAC control to obtain the same output power at 58.3GHz. (b) Summarized efficiency improvement for different output power level (DAC modes) at different frequencies.

The power detection for PA's output power is further measured with the results shown in Fig. 4.45. Since square root detector is used which has output voltage proportional to square of signal's voltage swing, mW is used for the X-axis. Figure 4.45 shows the measurement results at center frequency (58.3GHz). The 3-bit ADC outputs 8 digital levels as PA's output power varies from 0 to 0.3mW.

Figure 4.45 ADC outputs for PA output power detection at 58.3GHz.

Figure 4.46 Modification for the power detector design

Note the detectable power range deviates from the originally designed power range near OP_{1dB} level. This can be explained by the designed power detector schematic shown in Fig. 4.46. As the output node Vo1 is a high impedance point, it

is sensitive to process variation. As a result, the transistor biasing (V_{bn}) needs to be adjusted to tune the V_{o1} level back, which shifts the power detection range. This problem can be easily fixed by adding an op amp after the originally designed power detector circuit to fix the output voltage level, as shown in Fig. 4.46.

4.12 Conclusion

In this chapter, a 2D distributed power combining network is proposed by replacing the bulky RH T-line in traditional power combiners with compact metamaterial-typed CRLH T-line. Compared with RH T-line, CRLH T-line shows unique features such as nonlinear phase-frequency dependence and zero-phase-shift capability, thus can replace bulky RH T-line with the same functionality but much more compact area. By periodically loading transistors in a proposed 2D active in-phase CRLH T-line network, transistor outputs can be in-phase combined both in series and in parallel within compact area in a distributed manner, thus achieving high output power, high output power density and wideband simultaneously. Three 60GHz PA prototypes with single-ended 2×2 power combining network and differential 2×4 and 4×4 power combining networks are implemented in 65nm CMOS technology. The 1st PA prototype with single-ended 2×2 power combining shows 8.3dB gain, 7.1% PAE, and 9.7dBm OP_{1dB} with 16GHz bandwidth (44 to 60GHz) and area of 0.39mm^2 . This work is further improved to have a differential topology with compact transformer matching. The 2nd PA prototype with differential 2×4 power combining shows 13.2 dB gain, 8.7% PAE, 20GHz bandwidth (53 to 73GHz) and 13dBm OP_{1dB} with 74.5mw/mm^2 output power density, realizing state-of-art power performance and wide bandwidth simultaneously. The power performance is further improved by the 3rd PA prototype with differential 4×4 power combining, which shows 17.5dB gain, peak PAE of 11.3%, 8.8GHz bandwidth (54 to 62.8GHz), and 16.6dBm OP_{1dB} with 95.2mw/mm^2 output power density, demonstrating the top power performance in literature. All three PA prototypes show state-of-art performance, demonstrating the benefit of the proposed power combining network for effective short-range communication.

Chapter 5

CMOS 60GHz VCO with Wide Frequency Tuning Range

5.1 Introduction

Voltage controlled oscillator (VCO) is another critical block required in 60GHz transceiver to provide sufficient tuning range to cover the wide spectrum and large PVT variations with maintained phase noise and compact area, which is becoming a challenge with conventional tuning methods in CMOS technology. In this Chapter, one inductive tuning method is first proposed based on configuration of current return paths in the secondary coil of a transformer, which demonstrates wide frequency tuning range for CMOS VCO at mm-wave frequencies and shows great potential for integration in 60GHz transceiver design. The inductive tuning method is further applied to realize a tunable CRLH T-line for Mobius-ring RTW-VCO design in mm-wave region. By utilizing the unique features of CRLH T-line to achieve a negative phase shift with compact area and wide tuning capability as discussed in Section 3.3, state-of-art performance is demonstrated.

5.2 Review of CMOS 60GHz VCO

Phase noise and tuning range are the two primary design targets for VCO designs. During last decade, substantial knowledge about the wide frequency bands at 60 GHz and beyond has been accumulated to develop the next generation big-data-rate wireless terminals [15, 35, 61, 105-119]. The recent IEEE 802.15.3c standard for wireless local personal network (WPAN) has defined radio-frequency (RF) allocation composed of 4 RF sub-bands at 60GHz, each with bandwidth of 2.16 GHz. Considering the large frequency range and also large process variation in nano-scale CMOS, the utilization of one single varactor cannot cover such a

wide range with good phase noise performance, which has introduced grand challenge for 60GHz VCO designed in CMOS technology.

At mm-wave frequencies, the most widely used VCO topology is LC VCO [105, 109, 120-122]. It consists of a LC tank as resonator, and a cross-coupled transistor pair to generate negative resistance. LC VCO is widely used at 60GHz and beyond due to its high oscillation frequency, low phase noise, simple structure and differential output. The challenge, however, is its limited tuning range due to the large parasitic capacitance from cross-coupled transistor pair.

Except for phase noise and tuning range, multi-phase or quadrature output is often required for many big-data communication and imaging applications at millimeter-wave frequencies [29, 30, 119, 120, 123, 124]. Multi-phase and quadrature oscillators are normally realized by traveling wave to generate multi-phase clock outputs with good phase noise performance [29-32]. Mobius-ring rotary-traveling-wave (RTW) VCO topology is commonly adopted due to its advantages such as easy placement of cross-coupled transistors, good matching of differential blocks and compact area [32].

Traditionally, RTW-VCO is implemented with conventional right-handed (RH) transmission line (T-line), with a phase delay directly proportional to the T-line physical length [31-33]. Since a total phase delay of 360-degree is required for oscillation, a large area is induced. Recently, left-handed (LH) T-line has shown to provide a superior performance at high frequency [125], and also unique features such as nonlinear dispersion curve [62]. Due to large parasitic capacitors from cross-coupled transistors that are RH in nature, the actual implemented T-line is a composite right/left hand (CRLH) T-line. By merging the phase shifts from LH and RH components together, CRLH T-line provides a phase delay independent of its physical size, and thus can be designed to be much more compact than conventional RH T-line for VCO. On the other hand, as big-data communication or imaging applications require a wideband to ensure high data rate and also to cover process variation by CMOS MMIC at advanced technology, tuning ability of RTW-VCO has not been thoroughly studied and achieved as far.

5.3 Review of Frequency Tuning

Multi-sub-band operation is normally adopted to enhance the total frequency tuning range (FTR) with reduced VCO gain (K_{VCO}) [105]. Conventionally, multi-sub-band operation is implemented with capacitive tuning by switched capacitor banks. When operation frequency scales up to 60GHz, the parasitic capacitance from the capacitor bank becomes too large and the quality factor of capacitor becomes too low [105, 126], which would severely limit the achievable FTR. Recently, inductive tuning has become a promising substitute to replace the capacitive tuning [105, 119, 126-132], and is normally implemented by a loaded transformer topology [105, 126, 127]. By tuning inductance instead of capacitance, the limit of parasitic capacitance on FTR is relaxed. As a result, very wide FTR or multi-band operation can be achieved [105, 119, 126-132]. The inductive tuning can also be combined with conventional capacitive tuning to realize more sub-bands to reduce K_{VCO} [119, 127]. Besides a wide FTR, inductive tuning can also provide the benefit of isolated DC noise from the tuning element.

The loads on transformer for inductive tuning can be categorized into three types: resistor [105], capacitor [127], and inductor [126]. Wide FTR is then achieved by controlling the value of the load. However, traditional loaded transformer topologies suffer from various limitations. For example, resistor-loaded transformer has a nonlinear tuning-curve with large effective K_{VCO} , which can make PLL difficult to lock [105]. Capacitor-loaded transformer suffers from a narrow FTR due to the limited tuning range and poor quality factor of the varactor at high frequency region [127]. Inductor-loaded transformer requires the use of multiple number of transformers, which constraint the effective number of sub-bands due to layout size and design complexity [126].

5.4 Loaded Transformer for Inductive Tuning

5.4.1 Inductive tuning analysis for loaded transformer

The mechanism of loaded transformers applied for inductive tuning can be explained by Fig. 5.1. The loaded transformer is utilized to tune the effective inductance (L_{eff}) in a LC-tank, while C_t consists of the total capacitance in the LC-

tank. Note the 3 types of loaded transformers can all be approximately equalized to a RC tank and analyzed with the same equivalent circuit as shown in Fig. 5.1.

Figure 5.1 Equivalent circuit model for inductive tuning of loaded transformer.

The transformer is assumed to be ideal with coupling factor k , and with L_1 and L_2 as the primary inductance and secondary inductance, respectively. The equivalent circuit with L_{eq} and R_{eq} can then be calculated as

$$(5-1) \quad \begin{cases} L_{eq} = L_1 \times \frac{R^2[1-\omega^2 CL_2(1-k^2)]^2 + \omega^2 L_2^2(1-k^2)^2}{R^2(1-\omega^2 CL_2)[1-\omega^2 CL_2(1-k^2)] + \omega^2 L_2^2(1-k^2)} \\ R_{eq} = \frac{R^2 L_1 [1-\omega^2 CL_2(1-k^2)]^2 + \omega^2 L_1 L_2^2(1-k^2)^2}{R k^2 L_2} \end{cases}$$

Thus the oscillation frequency becomes

$$(5-2) \quad \omega = \frac{1}{\sqrt{L_{eq} C_t}}$$

For resistor or inductor-loaded transformer, the FTR of the equivalent circuit can be estimated by considering the two extreme conditions of R in Fig. 5.1:

$$(5-3) \quad \begin{cases} L_{eq_max} = L_{eq}(R \rightarrow \infty) = L_1 \times \frac{1-\omega^2 CL_2(1-k^2)}{1-\omega^2 CL_2} \\ L_{eq_min} = L_{eq}(R \rightarrow 0) = L_1(1-k^2) \end{cases}$$

By substituting (5-3) into (5-2), the FTR for LC-tank oscillation frequency can be obtained:

$$(5-4) \quad \begin{cases} \omega_{\min} = \omega(R \rightarrow \infty) = \sqrt{\frac{\omega_1^2 + \omega_2^2 - \sqrt{(\omega_1^2 + \omega_2^2)^2 - 4\omega_1^2\omega_2^2(1-k^2)}}{2(1-k^2)}}, \\ \omega_{\max} = \omega(R \rightarrow 0) = \frac{\omega_1}{\sqrt{1-k^2}} \end{cases}$$

where $\omega_1 = \frac{1}{\sqrt{L_1 C_t}}$ and $\omega_2 = \frac{1}{\sqrt{L_2 C}}$. As shown in Fig. 5.1, ω_1 and ω_2 represent the resonant frequencies at the primary side and the secondary side of the transformer, respectively.

Note that ω_1 is pre-determined by parameters of the transformer and the LC-tank, while ω_2 would be affected by the load. By defining $\omega_2 = \alpha\omega_1$, where $\alpha > 0$ is the ratio between two resonant frequencies, we can further analyze the value of $\omega(R \rightarrow \infty)$ based on different α values. Since $\frac{\partial \omega(R \rightarrow \infty)}{\partial \alpha}$ stays positive for all α values, by taking the extreme conditions for α , the range for $\omega(R \rightarrow \infty)$ can be estimated as

$$(5-5) \quad \omega(R \rightarrow \infty) \approx \begin{cases} \omega_2, & 0 < \alpha \ll 1 \\ \omega_1, & \alpha \gg 1 \end{cases}.$$

According to (5-5), when ω_2 is much higher than ω_1 , $\omega(R \rightarrow \infty)$ equals to ω_1 , indicating negligible dependence between value of $\omega(R \rightarrow \infty)$ and the load. However, as ω_2 drops below ω_1 , $\omega(R \rightarrow \infty)$ is decreased, approaching the value of ω_2 instead. This is actually the mechanism for frequency-tuning of capacitor-loaded transformer.

The effect of ω_2 value on the quality factor for the effective LC-tank must be considered, which can be easily derived from (5-1) as

$$(5-6) \quad Q_{eq} = \frac{R_{eq}}{\omega L_{eq}} = \frac{R}{\omega L_2} \times \frac{(1 - \omega^2/\omega_2^2)[1 - (1-k^2)\omega^2/\omega_2^2]}{k^2} + \frac{\omega L_2}{R} \times \frac{1-k^2}{k^2}.$$

Note that here the loss from the transformer and the LC-tank is not included into the calculation and Q_{eq} quantifies the additional loss coupled from transformer load into the LC-tank. As (5-6) shows, this coupled loss is contributed by two portions. When $R \gg \omega L_2$, the first item on the right-side of the equation dominates.

When $R \ll \omega L_2$, the second item dominates. Clearly, in the case of $\omega(R \rightarrow \infty)$, the first item should be considered. Unfortunately, as ω_2 drops, $\omega(R \rightarrow \infty)$ approaches the value of ω_2 , forcing Q_{eq} degrades towards 0, which indicates a high degradation on the phase noise performance. As a result, the approach of lowering ω_2 value for larger FTR, suffers significant phase noise degradation. In fact, this is also one limitation for the capacitor-loaded transformer.

Therefore, for resistor or inductor-loaded transformer, the condition $\omega_1 \ll \omega_2$ is required in design optimization. The FTR can then be estimated by

$$\text{FTR} = \frac{\frac{\omega_1}{\sqrt{1-k^2}} - \omega_1}{\frac{\omega_1}{\sqrt{1-k^2}} + \omega_1} \times 2 = \frac{1 - \sqrt{1-k^2}}{1 + \sqrt{1-k^2}} \times 2. \quad (5-7)$$

According to (5-7), to achieve a large FTR, a large k is required. Moreover, according to (5-6), Q_{eq} approaches infinity when R approaches 0 or infinity, but drops when R moves from the two boundaries. This can explain the performance degradation for resistor-loaded transformer since its major tuning region locates away from these two boundaries.

5.4.2 Model of inductor-loaded transformer with switches

The three types of loaded transformer (resistor, capacitor and inductor) are shown in Fig. 5.2. In Section 5.4.1 they are analyzed by the same equivalent circuit shown in Fig. 5.1. Since both resistor and capacitor-loaded transformers have the loading at one fixed location on the secondary coil of the transformer, their circuit behavior can be fully emulated by the same equivalent circuit shown in Fig. 5.1. The inductor-loaded transformer, on the other hand, has switches located on several different locations on the secondary coil. When one part of the secondary coil is turned on and plays the major role in determining the effective inductance on the primary coil, the remaining part of the secondary coil can still affect the performance due to parasitic effect, which is ignored by the simple equivalent circuit in Fig. 5.1. As a result, one more comprehensive circuit model is developed in Fig. 5.3 that can provide a more comprehensive model for inductor-loaded transformer.

Figure 5.2 Traditional resistor-, capacitor-, and inductor-loaded transformers.

Figure 5.3 Equivalent circuit model for conventional inductor-loaded transformer.

Figure 5.3 show the circuit models for traditional inductor-loaded transformer. Three inductors (L_1 , L_2 , and L_3) are used to form the simplest topology, and are coupled with each other by the mutual inductances M_{12} , M_{13} , and M_{23} . The terminal voltage and loop current for each inductor are represented by (V_1, I_1) , (V_2, I_2) , and (V_3, I_3) , respectively. The loaded inductance is varied by switching on different combinations of L_2 and L_3 , with their switches represented by $(R_2, C_2, \overline{i_{n2}^2})$ and $(R_3, C_3, \overline{i_{n3}^2})$, respectively. The resulted L_{eq} and R_{eq} can then be calculated by solving the following equations:

$$(5-8) \quad \begin{cases} I_1 = V_1 \times \left(\frac{1}{R_{eq}} + \frac{1}{sL_{eq}} \right) + \overline{i_{neq}} \\ V_1 = sL_1 I_1 + sM_{12} I_2 + sM_{13} I_3 \\ V_2 = sM_{12} I_1 + sL_2 I_2 + sM_{23} I_3 \\ V_3 = sM_{13} I_1 + sM_{23} I_2 + sL_3 I_3 \\ V_2 + \frac{R_2 I_2}{1+sR_2 C_2} = \frac{R_2 \overline{i_{n2}}}{1+sR_2 C_2} \\ V_3 + \frac{R_3 I_3}{1+sR_3 C_3} = \frac{R_3 \overline{i_{n3}}}{1+sR_3 C_3} \end{cases}$$

where an equivalent noise current ($\overline{i_{eq}^2}$) parallel to the LC tank can be transferred from the noise components of the switches.

5.4.3 Switch design parameters

To have the performance analysis in (5-8), we need to extract and optimize switch parameters for performance.

As shown in Fig. 5.4, switch state parameter in (5-8) is approximated by a RC-tank, where R_{on} and R_{off} are used to represent its effective resistance for the on and off states. Furthermore, the effective capacitances are represented by C_{on} and C_{off} . One can build a RC-library model for switches by extracting RC-values based on the 65nm CMOS technology by sweeping as listed in Table 5.1. Note that since the minimum length of switch is used to minimize parasitic capacitance, the size of switch is determined by its width W_s .

For switch noise parameter in (5-8), the gate noise ($\overline{v_{gn}^2}$) and channel noise ($\overline{i_{chn}^2}$) of the switch are transformed to equivalent current noise sources ($\overline{i_{n_{on}}^2}$ and $\overline{i_{n_{off}}^2}$) that are parallelly added to the RC tank. Since transformer filters out the low frequency noise, flicker noise is not considered in the model for simplicity. As a result, the noise sources ($\overline{i_{n_{on}}^2}$ and $\overline{i_{n_{off}}^2}$) of the switch are estimated as thermal noise in equivalent model.

Figure 5.4 Equivalent circuit model for switches. R_{on} , C_{on} and $\overline{i_{n_on}^2}$ form the equivalent circuit of switch when it is turned on. R_{off} , C_{off} and $\overline{i_{n_off}^2}$ form the equivalent circuit of switch when it is turned off.

Table 5.1 Switch Parameters Extracted from CMOS 65nm technology

W_s (μm)	10	20	50	100	200	400
R_{on} (Ω)	41.4	20.5	8.16	4.07	2.04	1.02
R_{off} (Ω)	2.72K	1.36K	543	272	136	67.9
C_{on} (fF)	7.78	15.6	38.9	77.8	156	311
C_{off} (fF)	6.10	12.2	30.5	61.0	122	244

5.5 Inductor-Loaded Transformer by Switching Return-path

According to Fig. 5.1 and (5-1), there are 4 variables: R , C , L_2 , and k on the secondary coil of the transformer, which control the oscillation frequency. Resistor-loaded transformer tunes R , capacitor-loaded transformer tunes C , while inductor-loaded transformer tunes both L_2 and k . Conventionally, L_2 and k are tuned by switching on different combinations of transformers [126]. However, the large layout size of loop inductor and strong magnetic coupling with adjacent devices limit the number of transformers. Moreover, as more transformers are used, magnetic coupling from different transformers tend to cancel each other, and hence make the tuning less effective. As a result, the number of sub-bands achieved by the conventional inductor-loaded transformer topology often limits to 4 (with 2 transformers used) and below.

In this section, a new inductor-loaded transformer topology is proposed, which breaks through the limit of the conventional inductive tuning. The concept of the proposed topology can be explained in Fig. 5.5. Only one transformer is used for

the new inductor-loaded transformer, with switches placed at various locations on the secondary coil. When some combination of switches are turned on such that a close-loop is constructed in the secondary coil, a current return-path forms. Different sized current return-paths generate different magnetic fluxes, which are fed back to the primary coil and hence result in multiple sub-bands.

Figure 5.5 Proposed new inductor-loaded transformer by switching current return-paths with only one transformer.

5.5.1 Comparison with traditional loaded transformers

Since the proposed topology can increase the number of sub-bands by simply adding more switches, the sub-band number can be easily designed to be larger than 4 with compact layout area when compared to the conventional inductor-loaded transformer.

Moreover, different from the resistor-loaded transformer that has a highly nonlinear tuning-curve and large K_{VCO} , the new inductor-loaded transformer achieves a much smaller K_{VCO} through multi-sub-band operation within linear tuning-curve. As a result, the phase noise performance can be improved with no PLL locking difficulty. The small K_{VCO} may also be used to trade for a wider tuning range, which can be easily realized by implementing with a large coupling factor k , as explained in (5-7).

In addition, as mentioned in Section 5.4, frequency-tuning for capacitor-loaded transformer is realized by varying the value of C and thus ω_2 . However, according to (5-6), as C increases or ω_2 drops, Q_{eq} is severely degraded. As a result, the FTR that can be achieved is limited. Furthermore, the FTR for varactor or capacitor-bank is further limited by parasitic capacitance from switches and transformers.

Trade-offs between different loaded-transformer topologies are summarized in Table 5.2. However, one design challenge is how to deal with asymmetric current return-paths in certain sub-bands, which will be discussed in detail in Section 5.8.

Table 5.2 Trade-offs between Different Loaded Transformer Topologies

Topology	Benefits	Limitations
R-loaded transformer	<ul style="list-style-type: none"> • wide tuning range • large sub-band number 	<ul style="list-style-type: none"> • large effective K_{VCO}
C-loaded transformer	<ul style="list-style-type: none"> • large sub-band number 	<ul style="list-style-type: none"> • limited tuning range
Traditional L-loaded transformer	<ul style="list-style-type: none"> • wide tuning range 	<ul style="list-style-type: none"> • limited sub-band number
Proposed L-loaded transformer	<ul style="list-style-type: none"> • wide tuning range 	<ul style="list-style-type: none"> • asymmetric current return path

5.5.2 Model of proposed new inductor-loaded transformer with switches

Similar to the modeling of conventional inductor loaded transformer, a more comprehensive circuit model is developed in Fig. 5.6 for the proposed new inductor-loaded transformer which can take the parasitic effects from the off part of the secondary coil into consideration.

Figure 5.6 Equivalent circuit model for the proposed loaded transformer.

Figure 5.6 shows the circuit models for the proposed inductor-loaded transformer. Its secondary coil is split into two portions: L_2 and L_3 . The L_3 portion is switched on to form a current return-path so as to generate feedback to L_1 , while the remaining portion of the secondary coil (L_2) is left floating by keeping the switch terminating L_2 off. The change of loaded inductance is then emulated by varying the ratio between L_2 and L_3 . The resulted L_{eq} and R_{eq} can then be calculated by solving the following equations:

$$(5-9) \quad \begin{cases} I_1 = V_1 \times \left(\frac{1}{R_{eq}} + \frac{1}{sL_{eq}} \right) + \overline{I_{neq}} \\ V_1 = sL_1 I_1 + sM_{12} I_2 + sM_{13} I_3 \\ V_2 = sM_{12} I_1 + sL_2 I_2 + sM_{23} I_3 \\ V_3 = sM_{13} I_1 + sM_{23} I_2 + sL_3 I_3 \\ V_2 + V_3 + \frac{R_2 I_2}{1+sR_2 C_2} = \frac{R_2 \overline{I_{n2}}}{1+sR_2 C_2} \\ V_3 + \frac{R_3 (I_3 - I_2)}{1+sR_3 C_3} = \frac{R_3 \overline{I_{n3}}}{1+sR_3 C_3} \end{cases} .$$

5.5.3 Performance study

Based on the afore-developed switch and transformer models, performance for the proposed inductor-loaded transformer topology can be further analyzed to obtain the optimized design with respect to switch sizing W_s . With extracted switch parameters such as in Table 5.1, switch performance under various sizes W_s can be studied. Based on the design parameters summarized in Table 5.3, we have the following detailed performance study.

Table 5.3 Parameters for 60GHz VCO Design based on Proposed Loaded Transformer Topology

Switch	Transformer			Other
W_s (um)	L_{prim} (pH)	L_{sec} (pH)	k	C_t (fF)
10~400	80	80	0.1~0.7	100

Firstly, impact of switches to the FTR performance is studied in Fig. 5.7(a). Confirmed with our conclusion in (5-7), a larger coupling factor k leads to a wider FTR. When switch size is small, the FTR is also observed to increase with switch size. This can be explained by the analysis in Section 5.4, where a larger C_{on} would

raise the FTR when R_{off} is sufficiently large. However, as switch size further increases, R_{off} becomes too small to fully switch off the current return path, and FTR starts to decrease.

(a) FTR (%)

(b) Minimum Q factor in tuning range

(c) Maximum noise spectral density (V^2/Hz) at 10MHz offset in tuning range

Figure 5.7 Design optimization for (a) frequency tuning range, (b) the minimum quality factor in the tuning range and (c) the maximum output noise spectral density at 10MHz offset in tuning range.

Secondly, impact of switches to phase noise performance can be also analyzed. Switches on loaded transformer degrade the phase noise performance from two aspects. It can decrease output signal power by reducing the effective Q factor in LC-tank; and also increase phase noise by transferring noise power to output nodes. These two aspects are analyzed in Fig. 5.7(b) and (c), by examining the minimum Q factor of the LC-tank and the maximum output noise spectral density at the offset frequency. One can observe that there is an optimal switch size for the minimum phase noise degradation.

5.5.4 Design Optimization Flow

As such, we present a design flow in Fig. 5.8 to optimize the specific performances of the proposed inductor-loaded transformer topology. The targeted frequency ($f_{req.}$) and tuning range (FTR) define the minimum frequency (f_{min}) and maximum frequency (f_{max}) to be designed. With the proposed tuning topology, f_{min} is mainly determined by the inductance of the primary coil (L_{prim}) and the total capacitance in LC-tank (C_t). Due to the single-loop topology adopted for the

proposed transformer, the inductance on its secondary coil (L_{sec}) can be accordingly determined.

Figure 5.8 Design optimization flow for wide-tuning VCO based on the proposed inductor-loaded transformer, where performance metrics are frequency, FTR, K_{VCO} , power, and phase noise.

Firstly, with the given FTR and targeted K_{VCO} , we can calculate the number of sub-bands (N_{band}) needed, thus determining how many switches are required as well as their locations on the secondary coil. Each sub-band is then to be fully covered by a varactor pair as fine tuning. Therefore the tuning capacitance (C_{tune}) is determined for varactor design. Besides C_{tune} , the rest part of C_t is mainly contributed from the parasitic capacitance in the cross-coupled transistors, which can help determine the transistor sizes.

Next, given L_{prim} , L_{sec} , and C_t , f_{max} is mainly determined by the coupling factor k of the transformer. For a specific k value, an optimized switch size can be found to minimize the phase noise (PN) as Fig. 5.7(b) and (c) shows. Note that since both phase noise and power consumption are related to the sizing and biasing of cross-coupled transistors, a few design iterations are required to meet the targeted performance for all specifications.

5.5.5 Loaded-transformer simulation results

5.5.5.1 Model validation

The proposed model in Section 5.5.2 is used to analyze one asymmetrical implementation for the proposed loaded transformer, whose topology will be shown in Fig. 5.14 in Section 5.7. Transformer parameters are extracted from EM simulation, as summarized in Table 5.4. C_t from Fig. 5.1 is adjusted to be 92fF. Calculated VCO oscillation frequency and noise density contributed by switches are plotted in Fig. 5.9 both of which can roughly fit the simulation results from Cadence. This validates the proposed model. Note a larger deviation occurs at lower frequency bands, which is due to neglect of flicker noise in switch model, as will be addressed in Section 5.7.2.1 and 5.8.2.1.

Table 5.4 EM Extracted Parameters at 60GHz for the Proposed Loaded Transformer Implementation

L_1 (pH)	L_2 (pH)	M_{12} (pH)	k
154.2	175.5	77.3	0.470

(a)

Figure 5.9 Model validation: (a) oscillation frequency, (b) output noise density contributed by switches.

5.5.5.2 Comparison between loaded transformer topologies

The four topologies in Fig. 5.2 and 5.5 are simulated numerically in MATLAB for performance comparison. To achieve a fair comparison, while both resistor and capacitor-loaded transformers are simulated by the equivalent circuit shown in Fig. 5.1, the inductor-loaded transformers are simulated based on more comprehensive models shown in Fig. 5.3 and Fig. 5.6 to consider parasitic effects on the secondary coil. Parameters derived in Section 5.4.3 are used to assist numeric analysis for the proposed inductor-loaded transformer topology. The same parameters are utilized to simulate resistor-loaded transformer (Table 5.5), with its resistance linearly varied between the on and off resistances (R_{on} and R_{off}) of the 50 μ m switch in Table 5.1. The linear change can be achieved by splitting the switch into parallel array of smaller switches [105]. Similarly, for the capacitor-loaded transformer, a switched capacitor bank can be used to obtain linear and large tuning range than single varactor. The penalty is the parasitic from the switches in the capacitor bank, which is also the major limitation for its tuning range. With the extracted switch parameters in Table 5.1, the effective capacitance ratio when the switch is on and off for each bank ($C_{ratio}=C_{off}/C_{on}$) is analyzed. A value of 3.206 is obtained for C_{ratio} and is used for this analysis.

Table 5.5 Parameters for Different Loaded Transformers biased for 60GHz Band Oscillation

Loaded Transformer	R-loaded	C-loaded	L-loaded	Proposed
L_{prim} (pH)	80	60	80	80
L_{sec} (pH)	80	60	N.A.	80
Coupling factor	$k=0.5$	$k=0.5$	$k_{12}=k_{13}=0.5$ $k_{23}=0.4$	$k=0.5$
L_{ratio}	N.A.	N.A.	0.3	0→1
C_{ratio}	N.A.	3.206	N.A.	N.A.

All loaded transformers designed to provide the same oscillation frequency in 60GHz band. The adjusted parameters are summarized in Table 5.5, and the simulated tuning range and quality factor are shown in Fig. 5.10. To have a direct view of the extra loss coupled from the tuning elements into the LC-tank, similar definition of quality factor as (5-6) is used. With this definition, the quality factor represents how much degradation on the whole LC-tank quality factor (or phase noise performance) will be caused by the tuning elements loaded on the transformer.

(a)

(b)

(c)

(d)

Figure 5.10 Numeric simulation for tuning range and quality factor of different loaded transformers: (a) R-loaded transformer, (b) C-loaded transformer, (c) traditional L-loaded transformer, (d) proposed new loaded transformer.

Firstly, as Fig. 5.10(a) shows, the resistor-loaded transformer has a highly nonlinear tuning-curve with respect to tuning resistance. Most of the frequency tuning is realized in a narrow region of the tuning resistance, where the lowest quality factor also locates. Next, the capacitor-loaded transformer, as Fig. 5.10(b) shows, has a very linear tuning-curve. Besides its quality factor degradation in the lower frequency region, its major limitation is the narrow tuning range which comes from the limited tuning ability of varactor or capacitor bank. Lastly, for the traditional inductor-loaded transformer shown in Fig. 5.10(c), there are only 4 sub-bands within the tuning range. Besides its limitation on the number of sub-bands that can be achieved, the inductor-loaded transformer also suffers from high degradation on quality factor in the middle region (mode 3) of its tuning range. Different from the resistor-loaded transformer, this degradation comes from magnetic coupling from L_3 to L_2 when L_2 is switched on and L_3 is off. Recall that multiple transformers needed by the traditional inductor-loaded transformer would cause large area overhead as well.

In contrast, the proposed inductor-loaded transformer does not have this degradation. Due to the single-loop topology adopted for the transformer, the coupling between different portions on the secondary coil is much weaker. As Fig. 5.10(d) shows, a linear tuning curve is obtained with a large FTR, and with low degradation on quality factor in the whole tuning range at 60GHz by the proposed inductor-loaded transformer.

The performances of different loaded transformers are summarized in Table 5.6. The numeric simulations confirm with our observations in Section 5.5.1 that the proposed new inductor-loaded transformer can realize a wide FTR with high linearity and low K_{VCO} and also can achieve multiple sub-bands with compact size. Furthermore, low degradation on LC-tank quality factor and hence better VCO phase noise performance can also be maintained in the whole tuning range by the proposed inductor-loaded transformer. As shown in Fig. 5.10(d), a 20% FTR with linear tuning curve is achieved with a Q factor above 10 for all sub-bands.

Table 5.6 Performance Summary for Different Loaded Transformer Topologies based on Numeric Analysis

Loaded Transformer	R-loaded	C-loaded	L-loaded	Proposed
Tuning Range	Large	Small	Large	Large
Linearity	Low	High	Medium	High
Quality factor Degradation	High	Medium	Medium	Low
Band number	Large	Large	Small	Medium

5.6 Tunable CRLH T-line based RTW-VCO

As mentioned in Section 5.1, Mobius-ring RTW-VCO is often utilized to generate multi-phase or quadrature output for many millimeter-wave applications such as big-data communication and imaging. Conventional RTW-VCO is mostly tuned by varactor and capacitor bank due to the RH topology [31-33]. Due to constraint tuning ability of varactor and capacitor bank in millimeter-wave region, the achieved FTR is quite limited [31-33]. CRLH T-line, on the other hand, provides more choices of tunable elements to achieve a wide FTR in RTW-VCO design, but is not well explored at millimeter-wave region [125]. In this section, a tunable CRLH T-line biased in the LH region is studied for RTW-VCO to achieve compact size and wide FTR. Assisted with the inductive tuning techniques presented in above sections, a much wider FTR can be obtained.

5.6.1 CRLH T-line based RTW-VCO

The topology for Mobius-ring RTW-VCO is shown in Fig. 5.11. A Mobius-ring is evenly divided into N stages, with each stage loaded with a cross-coupled transistor pair. As wave travels along the Mobius-ring, certain phase delay must be fulfilled to create a positive feedback for VCO oscillation. At the same time, cross-coupled transistors should generate enough power to compensate the loss from the T-line. In summary, the start-up condition of Mobius-ring RTW-VCO is

$$g_m > \frac{2\exp(\alpha \cdot l)}{Z_o}; \beta l = \frac{M\pi}{N}. \quad (5-10)$$

where g_m is the transconductance of the cross-coupled pair, z_o , l , α , β are T-line characteristic impedance, physical length, attenuation constant, and phase constant, respectively. N is the stage number, and $M=\pm 1, \pm 3, \dots$ is an odd integer number.

In this section, negative-phase CRLH T-line introduced in Chapter 3 is deployed in the Mobius-ring RTW-VCO for both compact size and wide FTR. Assuming balanced condition for simplicity, with (3-7) and (5-10), the oscillation frequency for an N -stage Mobius-ring RTW-VCO by CRLH T-line can be obtained

$$\omega_{CRLH} = \frac{\pi}{2Nl\sqrt{L_s C_p}} \times \left(\sqrt{1 + \frac{4N^2 l^2}{\pi^2} \sqrt{\frac{L_s C_p}{L_p C_s}}} \pm 1 \right). \quad (5-11)$$

Here only the fundamental resonant condition $M=\pm 1$ is considered for simplicity of illustration. The plus and minus signs in (5-11) correspond to CRLH T-line working in the RH region and LH region, respectively.

Furthermore, phase noise is an important specification for VCO design. Generally, for N -stage RTW-VCO, the phase variation $\langle \Phi^2(t) \rangle$ is proportional to $1/N$ [31, 133-135], which is reduced by $1/N$ when compared to single stage.

In this work, the LH operation is selected for compact size and superior performance when implemented in multiple stages [125]. However, there is no study on how to tune the CRLH T-line based RTW-VCO, which will be addressed in the next part.

Figure 5.11 CRLH T-line based Mobius-ring RTW-VCO.

5.6.2 Wideband tuning for CRLH T-line based RTW-VCO

Note that in (5-11), there are 4 components that may be used for tuning: L_s , L_p , C_s , C_p . For easy analysis, we represent the product of the LH components (L_p, C_s) as P_L ; and represent the product of the RH components (L_s, C_p) as P_R . Then, the oscillation frequency in the LH region becomes

$$\omega_{CRLH_LH} = \frac{\pi}{2Nl\sqrt{P_R}} \times \left(\sqrt{1 + \frac{4N^2l^2}{\pi^2} \sqrt{\frac{P_R}{P_L}}} - 1 \right). \quad (5-12)$$

Conventionally, P_R is used to realize FTR by varactor as part of C_p [125]. Unfortunately, with the omitted L_s component and thus small P_R value in [125], the tuning ability by P_R is very limited, not to mention the already constraint tuning ability as well as the limited quality factor of varactor at high frequency. In fact, for a small P_R / P_L value, ω_{CRLH_LH} approaches the operation frequency of a pure LH T-line based RTW-VCO

$$\omega_{CRLH_LH} \Big|_{\frac{P_R}{P_L} \rightarrow 0} = \omega_{LH} = \frac{Nl}{\pi\sqrt{P_L}}, \quad (5-13)$$

which is independent of P_R with poor tuning ability. Furthermore, large portion of C_p is contributed by transistor parasitic with a fixed value, which severely limits

tuning range of the whole C_p value, not to mention the already constrained tuning ability as well as the limited quality factor of varactor at high frequency region.

Intuitively, a wider FTR should be obtained by tuning P_L since the LH-components dominate in the LH region. Since $\frac{\delta\omega_{CRLH}}{\delta P_L}$ stays positive for all P_L values, the FTR can be calculated

$$\Delta\omega_{CRLH_{LH}} = \frac{\pi}{2Nl\sqrt{P_R}} \times \left(\sqrt{1 + \frac{4N^2l^2}{\pi^2} \sqrt{\frac{P_R}{P_{L_{min}}}}} - \sqrt{1 + \frac{4N^2l^2}{\pi^2} \sqrt{\frac{P_R}{P_{L_{max}}}}} \right). \quad (5-14)$$

The extreme condition forms for a pure LH T-line with

$$FTR_{LH} = \frac{\frac{1}{\sqrt{P_{L_{min}}}} - \frac{1}{\sqrt{P_{L_{max}}}}}{\frac{1}{\sqrt{P_{L_{min}}}} + \frac{1}{\sqrt{P_{L_{max}}}}} \times 2 \approx \frac{\alpha_{P_L}}{2}, \quad (5-15)$$

where $\alpha_{P_L} = \frac{\Delta P_L}{P_L}$ measures the tunability of components in P_L . As (5-15) shows, the same result is obtained as the analysis for more general case in Section 3.3, and FTR_{LH} is directly proportional to α_{P_L} .

However, since the loss in C_s adds directly into the signal path, it is not feasible to tune C_s . On the other hand, one can realize a wide FTR by tuning L_p with a loaded transformer structure presented in above sections. More specifically, inductive-loaded transformer can achieve a large α_{P_L} , which is adopted in this work.

The mechanism for inductive-loaded transformer has been explained in Section 5.4. As (5-3) indicates, a large α_{P_L} can be easily obtained by implementing a large coupling factor k for the transformer. Furthermore, multiple inductors can be switched on and off to further increase α_{P_L} with a wide FTR achieved by creating multiple sub-bands.

The designed switched coupled-inductor for inductive tuning is shown in Fig. 5.12. Inductors are realized by the top Cu layer to guarantee a high quality factor.

Two transformers loaded with two switches are used to realize 4 sub-bands. As summarized in the tables shown in Fig. 5.12, the resulted L_{eq} can be varied over a large range from 47pH to 91pH. As such, wide FTR can be realized with 4 sub-bands: (75.67-83.11GHz), (79.65-87.78GHz), (86.18-94GHz) and (93.89-102.01GHz). To realize a continuous tuning, fine-tuning by varactor is used in each sub-band. To increase the tuning ability of varactor as (5-13) indicates so as to fully cover each sub-band, a relatively large L_s value is adopted in this design.

Figure 5.12 Layout implementation for inductor-loaded transformer where tuned inductance is determined by states of two switches.

The resulted tuning mechanism for the proposed CRLH T-line based RTW-VCO can be explained in Fig. 5.13. Inductive-loaded transformer creates multiple sub-bands by shifting the dispersion curve to different resonant frequency points. Each sub-band is then covered with fine-tuning by a varactor.

Compared with conventional RTW-VCO, the proposed CRLH T-line based RTW-VCO provides alternative choices of tunable elements. Assisted with the inductive tuning techniques presented in above sections, a much wider FTR can be obtained.

(a)

(b)

Figure 5.13 Tuning mechanism for the proposed tunable CRLH T-line based Mobius-ring RTW-VCO: (a) Equivalent circuit, (b) Dispersion diagram.

5.7 60GHz VCO Prototype with Asymmetric Implementation of Inductive Tuning

To further verify the proposed inductive tuning mechanism by switching return-path in Section 5.5, two 60GHz VCO prototypes are demonstrated in CMOS 65nm technology in this section [61] and the following section [136].

As shown in Section 5.5, to realize multiple sub-bands for the proposed inductor-loaded transformer, switches are loaded at various locations on the secondary coil of one transformer. As the number of switches increases, the total capacitance and resistance loaded on the transformer increases and decreases, respectively. According to the analysis in Section 5.4, for the conditions when switches are turned off, both a larger C and a smaller R would weaken the domination of the terms $R^2[1 - \omega^2 CL_2(1 - k^2)]^2$ and $R^2(1 - \omega^2 CL_2)[1 -$

$\omega^2 CL_2(1 - k^2)]$ in (1), resulting in a smaller FTR. As a result, the number of switches loaded on the transformer should be minimized while providing enough sub-bands.

As a result, one layout topology is designed in this section, which can realize the maximum number of sub-bands with the least number of switches, thus can achieve the maximized FTR. The penalty is an asymmetric layout implementation, which may cause certain degradation in the phase noise performance. This problem can be solved with another symmetric topology to be presented in Section 5.8.

5.7.1 60GHz VCO design

5.7.1.1 Loaded transformer design

The proposed topology targets for the maximum FTR, with layout implementation shown in Fig. 5.14. A transformer is loaded with 4 switches (S1~S4) at different locations. The inner loop is the primary coil, which serves as the inductor of the LC-tank. The outer loop is the secondary coil, which is loaded with 4 switches to control the current return-paths. Lengths of the 4 sections in the secondary coil are marked with unit length l . Different combinations of the switches and corresponding effective lengths of the current return-paths are summarized in Table 5.7. There are in total 7 modes or sub-bands established. For example, by turning on switches S1 and S2, the mode 3 is invoked with a current return-path formed with length $3l$. Moreover, as shown in Table 5.7, the effective length of return-path in secondary coil varies from 0 to $6l$ linearly, resulting in 7 evenly distributed sub-bands. Evenly distributed sub-bands can facilitate PLL design and also improve its performance.

Figure 5.14 Asymmetric layout implementation for the proposed new inductor-loaded transformer.

Table 5.7 Effective Return Path Lengths in Secondary Coil for Different Sub-band Selection Modes in Asymmetric Layout Implementation

Sub-band Selection Mode	0	1	2	3	4	5	6
On Switches	Nil	S1	S2	S1+S ₂	S1+S ₃	S2+S ₄	S3+S ₄
Effective Length of Return Path	0	l	$2l$	$3l$	$4l$	$5l$	$6l$

Note that more sub-bands can be realized by implementing more switches but may also degrade the phase noise performance. As derived in Section 5.4 and 5.5, a small switch R value is desired to minimize phase noise degradation. As such, the number of switches should be minimized when connected in serial in the activated current return-path. The proposed band selection method in Fig. 5.14 and Table 5.7 can minimize the number of switches in the current return-path to be 2 or below for all selection modes.

With an asymmetric allocation of switches, this layout implementation realizes 7 sub-bands with only 4 switches. As a result, a maximized FTR can be achieved. The trade-off is that the asymmetric switch locations and current return-paths would have a large phase noise variation due to different current return-paths in each sub-band.

5.7.1.2 VCO design

To verify the proposed inductive tuning, one VCO prototype is designed at 60GHz. The VCO can provide multiple frequency sub-bands to cover the wide frequency band at 60GHz.

As shown in Fig. 5.15, power supply is fed on the central tap. A varactor-pair is used for fine tuning within each sub-band. The LC-tank loss is compensated by a cross-coupled NMOS pair. Two output buffers are utilized for the power gain and isolation. The transformer is implemented with the top metal layer for high Q. To implement a proper k value, a gap size of $3.5\mu\text{m}$ is designed between transformer primary and secondary coils. Once the coupling factor of transformer is determined, an optimized switch size can be found. A size of $50\mu\text{m}/60\text{nm}$ is adopted for switch transistors.

With the tuning scheme proposed in Table 5.7, there are 7 sub-bands generated by the VCO. Compared with the symmetric implementation as will be shown in Section 5.8, the asymmetric VCO provides a wider FTR due to more sub-bands and fewer loaded switches thus smaller parasitic capacitance.

Figure 5.15 Schematic of the 60GHz inductive-tuning VCO with asymmetric implementation of the proposed new inductor-loaded transformer.

5.7.2 Simulation and measurement results

The designed 60GHz VCO is implemented in STM 65nm 1P7M CMOS 65nm technology. EM simulation (ADS-Momentum) is used for circuit design and verification before the fabrication. The extracted parameters for the designed transformer are summarized in Table 5.4, and the equivalent circuit parameters under various band selection modes are plotted in Fig. 5.16.

Figure 5.16 Parameter extraction for the asymmetric loaded transformer design under various band selection modes.

5.7.2.1 Phase noise analysis

To further analyze the proposed loaded-transformer influence on VCO phase noise (PN) performance, percentage of noise contribution from switches on loaded transformer to output is simulated and plotted in Fig. 5.17. The analysis is carried out at both offset frequencies of 1MHz and 10MHz. Around 10-15% phase noise is contributed from the proposed loaded transformer.

The drain-to-source thermal noise from the "ON" switches in current return path is also analyzed in Fig. 5.17. In high frequency bands, where a large current return path is formed, thermal noise from "ON" switches dominate the total noise contribution. However, at lower frequency bands, where large portion of secondary coil is left floating, noise contribution from "OFF" switches not in the current return path comes in.

The deviation of total switch noise between 1MHz offset and 10MHz offset shows the role of flicker noise from switches. In our numeric analysis in Section 5.5, flicker noise was ignored due to DC blocking and low up-conversion ratio of switches biased in triode region. However, a large AC signal on the secondary coil of transformer could drive the switch towards saturation region with negative voltage swing, leading to higher up-conversion ratio. In lower frequency bands, where large portion of secondary coil is left floating, a standing wave would be formed on the floating coil, introducing a large voltage swing at the floating end, which drives switches into saturation region. As a result, more flicker noise is up-converted and coupled to output. In higher frequency bands, the floating coil

becomes shorter and the contribution of flicker noise from switches become negligible, as indicated in Fig. 5.17.

Figure 5.17 Percentage of noise contribution from switches on asymmetric loaded transformer implementation at 1MHz offset and 10MHz offset. Both total noise from all switches and drain-to-source thermal noise from "on" switches are plotted.

Furthermore, a comparison is done with switches removed from loaded transformer and replaced with ideal open and short connections. This analysis aims to check the effect of switch alone on VCO performance, and is carried out with pre-layout simulation and with EM simulation for loaded transformer. The results are compared in Fig. 5.18 with the case where actual switches are used.

From low to high frequencies in Fig. 5.18, the loaded transformer is switched from Mode 0 to Mode 6 according to Table 5.7. In Mode 0, all switches are turned off and has minimum degradation on phase noise performance. In this case, the parasitic capacitance from switches lowers the oscillation frequency from around 65GHz to 60GHz. However, as switches are turned on to form a current return path, according to analysis in Section 5.4, parasitic capacitance from switches increases the FTR, while both parasitic capacitance and resistance from switches degrades the phase noise performance. Note as capacitance from switches further increases, the FTR would degrade again as shown in Fig. 5.7(a), and is the case for symmetric implementation.

Figure 5.18 Simulation comparison for VCO performance (phase noise and oscillation frequency) with and without switches.

5.7.2.2 Measurement Results

The measurements are then done on CASCADE Microtech Elite-300 probe station, with Agilent PNA-X spectrum analyzer, E5052 source signal analyzer, and 11970V harmonic mixer. A 67GHz bias-T is used to provide load to buffer.

As mentioned in Section 5.7.1.1, there tends to be a large variation for VCO phase noise performance at different sub-bands due to the wide FTR and different switching conditions. Since a large phase noise variation across sub-bands would significantly degrade the PLL performance, we introduce a new phase noise (PN) performance in this work with the following equation

$$\text{FTR} = \frac{\frac{\omega_1}{\sqrt{1-k^2}} - \omega_1}{\frac{\omega_1}{\sqrt{1-k^2}} + \omega_1} \times 2 = \frac{1 - \sqrt{1-k^2}}{1 + \sqrt{1-k^2}} \times 2. \quad (5-16)$$

where $\overline{PN}$ and σ_{PN} are the mean and variation of phase noise across all sub-bands. The phase noise variation (σ_{PN}) can then be used as a new figure-of-merit for wide FTR VCO design at 60GHz.

Figure 5.19 Die photo for the 60GHz asymmetric VCO with fabricated in STM 65nm CMOS technology.

The die photo for the designed asymmetric 60GHz VCO is shown in Fig. 5.19. Decoupling capacitors are implemented by MIM capacitors and used to stabilize DC signals. The total area is $852 \times 451 \mu\text{m}^2$, which is mainly constrained by PADs. The core area takes only $163 \times 190 \mu\text{m}^2$.

Figure 5.20 Measured tuning curves under different band selection modes for the 60GHz asymmetric VCO.

With 1V VDD and Vtune varied from 0.5 to 1.5V, the obtained tuning curves under different sub-band selection modes are plotted in Fig. 5.20. The entire tuning range is divided into 7 sub-bands. Within each sub-band, a tuning range of 2.5~4.5 GHz is achieved by a small varactor. Evenly distributed sub-bands are preferred for the easy PLL implementation, which can be achieved by adjusting locations of switches. The obtained oscillation frequency varies from 51.9 to

67.3GHz, which covers the whole 60GHz band in IEEE 802.15.3c standard and provides a FTR of 25.8%. The effective K_{VCO} in each band varies from 2.1 to 3.8 GHz/V. Note the tuning voltage (0.5~1.5V) is selected to provide maximum tuning range for varactor, and can be easily changed to 0~1V by adding a serial capacitor between varactor and power supply.

(a)

(b)

Figure 5.21 Measured phase noise performance for the 60GHz asymmetric VCO. (a) Phase noise at 60GHz. (b) Phase noise variation for all selection modes.

A sample of phase noise plot is shown in Fig. 5.21(a). At 60GHz, the phase noise is -106.7dBc/Hz at 10MHz offset. The measured phase noise performance for all modes is shown in Fig. 5.21(b). There is around 10dB deviation in phase noise from simulation, which may be due to the low output power, inaccurate noise model and non-ideal ground around VCO. Moreover, as expected in Section 5.7.1.1, degradation in phase noise variation is observed in Fig. 5.21(b), which

mainly comes from asymmetric sub-band selection topology. As a result, a large phase noise variation (σ_{PN}) of 8.2dB is observed.

5.8 60GHz VCO Prototype with Symmetric Implementation of Inductive Tuning

Though the topology presented in Section 5.7 can achieve a maximized FTR, the asymmetric layout would degrade the phase noise performance. To solve this problem, in this section, another topology is designed with a symmetric layout implementation and optimized tuning mechanism for the switches [136]. Both phase noise and phase noise variation are thus improved. The penalty is the use of more switches than the first topology, leading to a relatively narrower FTR. These two topologies can be utilized for different applications with different design targets. A comparison is also made between the two topologies.

5.8.1 60GHz VCO design

5.8.1.1 Loaded transformer design

The proposed topology in this section targets for a balanced performance of both FTR and phase noise variation in each sub-band, with symmetric layout implementation shown in Fig. 5.22. Since a symmetric topology with differential operation lowers undesired common-mode effects such as substrate and supply noise amplification and up-conversion [137], the phase noise performance is improved. In Fig. 5.22, the symmetric topology is realized by placing 3 pairs of switches (S1P/N~S3P/N) on the secondary coil of transformer with vertical symmetry.

Note that with symmetric switch locations, if the current return-path is also configured symmetrically, the number of sub-bands is highly limited. For N pairs of switches, only $N+1$ sub-bands can be created. To realize a targeted FTR and K_{VCO} , more pairs of switches would then be required to generate enough sub-bands, which would add loss to the loaded transformer and degrade phase noise performance. Furthermore, because switches with large size contribute large

parasitic capacitance to the loaded transformer, if a large number of switches are used, the FTR would be limited as indicated by Fig. 5.7(a).

Figure 5.22 Symmetric layout implementation for the proposed new inductor-loaded transformer.

Table 5.8 Effective Return Path Lengths in Secondary Coil for Different Sub-band Selection Modes in Symmetric Layout Implementation

Sub-band Selection Mode	0	1	2	3	4	5
On Switches	Nil	S3N+S3P	S2N+S3P	S2N+S2P	S2N+S1P	S1N+S1P
Effective Length of Return Path	0	l	$2l$	$3l$	$4l$	$5l$

In this section, the following tuning scheme is designed to overcome the aforementioned challenge. As shown in Fig. 5.22, one switch on each side of virtual ground is turned on in all sub-band selection modes except the default mode 0 where all switches are off. Different sub-bands are then changed by shifting the ON-switch locations on each side alternately. In this fashion, the number of sub-bands created is nearly doubled while maintaining a small difference in the

selected current return-path lengths on both sides. For N pair of switches, $2N$ sub-bands can be created.

One example is shown in Table 5.8, 6 sub-bands are generated using 3 pairs of switches. The effective length of return-path in secondary coil varies from 0 to $5l$ linearly when the mode is switched from 0 to 5. In addition, the maximum difference in the effective length on both sides is maintained within l . Compared with asymmetric implementation, the proposed symmetric implementation only introduces limited extra number of switches with small FTR reduction, but can significantly improve phase noise with constraint phase noise variation. As verified by measurement, this symmetrical configuration results in low phase noise with small variation across all sub-bands, while still maintaining a high FTR.

5.8.1.2 VCO design

To verify the proposed symmetric implementation of inductive tuning, another VCO prototype is designed at 60GHz which can also provide multiple frequency sub-bands to cover the wide frequency band at 60GHz.

As shown in Fig. 5.23, power supply is fed on the central tap. A varactor-pair is used for fine tuning within each sub-band. The LC-tank loss is compensated by a cross-coupled NMOS pair. Two output buffers are utilized for the power gain and isolation. The transformer is implemented with the top metal layer for high Q . Different from the asymmetric implementation, a gap size of $2.5\mu\text{m}$ instead of $3.5\mu\text{m}$ is designed between transformer primary and secondary coils. Once the coupling factor of transformer is determined, an optimized switch size can be found. Again, a different size of $64\mu\text{m}/60\text{nm}$ is adopted for switch transistors in the symmetric implementation compared with the size of $50\mu\text{m}/60\text{nm}$ in the asymmetric implementation. The size differences between two designs come from technology and topology differences, as will be discussed in Section 5.8.2.

With the tuning scheme proposed in Table 5.8, there are 6 sub-bands generated by the symmetric VCO. Compared to the asymmetric VCO introduced in Section 5.7 which can provide a wider FTR due to more sub-bands and fewer loaded switches thus smaller parasitic capacitance, the symmetric VCO significantly

improves the phase noise performance with highly suppressed phase noise variation and can still achieve a wide FTR.

Figure 5.23 Schematic of the 60GHz inductive-tuning VCO with symmetric implementation of the proposed new inductor-loaded transformer.

5.8.2 Simulation and measurement results

The designed symmetric 60GHz VCO is implemented in Global Foundries 65 nm CMOS 1P8M technology. EM simulation (ADS-Momentum) is used for circuit design and verification before the fabrication.

For a fair comparison to the asymmetric 60GHz VCO presented in Section 5.7, different transformer and switch sizes are designed for the two fabrications to achieve the same primary inductance L_I as well as equivalent Q-factors Q_{eq} . In this way, similar oscillation frequency as well as similar loss introduced by loaded transformer can be ensured. The extracted parameters for the transformer used for the symmetric VCO are summarized in Table 5.9, and the equivalent circuit parameters under various band selection modes are plotted in Fig. 5.24. Also note

that a square shape is adopted for the transformer for ease of switch allocation. Though an octagonal shape is theoretically less lossy, the effect is minimal for single-loop transformer at 60GHz according to simulation.

Table 5.9 EM Extracted Parameters at 60GHz for Symmetric Loaded Transformer Implementation

L_1 (pH)	L_2 (pH)	M_{12} (pH)	k
153.1	136.9	44.6	0.308

Figure 5.24 Parameter extraction for the symmetric loaded transformer design under various band selection modes.

5.8.2.1 Phase noise analysis

Similar to the asymmetric loaded transformer, percentage of noise contribution from switches on loaded transformer to output is simulated and plotted in Fig. 5.29 for symmetric loaded transformers at offset frequencies of 1MHz and 10MHz.

Compared with asymmetric implementation, less noise contribution is observed for symmetric implementation. Although similar Q_{eq} values in Fig. 5.16 and Fig. 5.24 indicate similar loss introduced by loaded transformers, a smaller k value means less noise coupling from switches, which gives better PN performance at the penalty of smaller FTR. As such, one can observe 4dB improvement of average PN performance for symmetric loaded-transformer design.

Similar to the asymmetric loaded transformer, the drain-to-source thermal noise from "ON" switches dominate the total noise contribution in high frequency bands, while noise contribution from "OFF" switches not in the current return path

becomes larger at lower frequency bands where large portion of secondary coil is left floating.

Again, the deviation of total switch noise between 1MHz offset and 10MHz offset shows the role of flicker noise from switches. In lower frequency bands, where large portion of secondary coil is left floating, a standing wave would be formed on the floating coil, introducing a large voltage swing at the floating end, which drives switches into saturation region. As a result, more flicker noise is up-converted and coupled to output. In higher frequency bands, the floating coil becomes shorter and the contribution of flicker noise from switches become negligible.

Figure 5.25 Percentage of noise contribution from switches on symmetric loaded transformer implementation at 1MHz offset and 10MHz offset. Both total noise from all switches and drain-to-source thermal noise from "on" switches are plotted.

5.8.2.2 Measurement Results

The measurements are then done on CASCADE Microtech Elite-300 probe station, with Agilent PNA-X spectrum analyzer, E5052 source signal analyzer, and 11970V harmonic mixer. Different from asymmetric VCO which requires a bias-T to provide load to buffer, in this design, the whole buffer is realized on-chip.

The die photo for the designed symmetric 60GHz VCO is shown in Fig. 5.26. The VCO core occupies an area of $140 \times 220 \mu\text{m}^2$. The overall chip size is $840 \times 750 \mu\text{m}^2$, including the test buffer and all the pads.

Figure 5.26 Die photo for the 60GHz symmetric VCO fabricated in Global Foundries 65nm CMOS technology.

The DC power dissipation of the VCO is 6 mW at supply voltage of 1.0 V. The lower power consumption compared to asymmetric 60GHz VCO is due to the designed high quality factor of the symmetrical transformer. Figure 5.27 shows the measured tuning curves with dependence on the control voltages. One can observe that the VCO can exhibit 6 sub-bands with oscillation in a wide FTR from 57.0 GHz to 65.5 GHz, which covers the whole 60 bands in IEEE 802.15.3c standard. The tuning range is 8.5 GHz with 14.2 % of the center frequency. The effective K_{VCO} in each band varies from 1.8 to 2.4 GHz/V.

Figure 5.27 Measured tuning curves under different band selection modes for the 60GHz symmetric VCO.

Moreover, Fig. 5.28 shows the measured phase noise at 10 MHz offset frequency of the VCO. In the required frequency range (58.32-64.80 GHz), the phase noise at 10 MHz frequency offset is lower than -105 dBc/Hz. Both the mean phase noise ($\overline{PN}$) and phase noise variation (σ_{PN}) has been significantly improved over the first asymmetric design due to symmetric tuning adopted, with $\overline{PN}$ improved to -108.3 dBc/Hz and σ_{PN} reduced to 2.5 dB. Though the trade-off is reduced FTR, a large tuning range of 14.2% is still achieved.

(a)

(b)

Figure 5.28 Measured phase noise performance for the 60GHz symmetric VCO. (a) Phase noise at 60.8GHz. (b) Phase noise variation for all selection modes.

In addition, the measured spectra of the output signals under different modes are shown in Fig. 5.29. The starting frequency under different modes distribute evenly as expected, with a small variation from 1GHz to around 1.6GHz. Note that this variation could be further suppressed by adjusting switch locations.

Figure 5.29 Measured output spectrum of equally-spaced starting frequencies under 6 different modes for the 60GHz symmetric VCO.

Table 5.10 Performance Summary and Comparison of Wide-Tuning 60 GHz VCOs

		[121]	[120]	[122]	Asym. VCO Prototype	Sym. VCO Prototype
Technology (CMOS)		90 nm	65nm	65 nm	65 nm	65 nm
Freq. (GHz)	f_{osc}	76.5	70.2	77	59.6	61
Freq. Tuning Range (%)	FTR	7.0	9.6	14.5	25.8	14.2
Phase Noise (dBc/Hz)	PN	-110.6	-106.0	-112	-106.7	-110.8
Phase Noise Mean (dBc/Hz)	$\overline{PN}$	-107.1	-99.5	-108.5	-98.5	-108.3
Phase Noise Variation (dB)	σ_{PN}	3.5	6.5	3.5	8.2	2.5
Power (mW)	P_{DC}	19.4	5.4	190	5.4	6.0
Area (mm ²)	A	0.01	0.003	0.15	0.031	0.031
Figure of Merit (dBc/Hz)	$FOM^{(1)}$	-171.9	-169.1	-163.4	-166.7	-176.2
Figure of Merit (dBc/Hz)	$FOM_t^{(2)}$	-168.8	-168.8	-166.7	-174.9	-179.3

$$^{(1)}FOM = \overline{PN} - 20 \log \left(\frac{f_{osc}}{\Delta f} \right) + 10 \log (P_{DC}/1mW)$$

$$^{(2)}FOM_t = \overline{PN} - 20 \log \left(\frac{f_{osc}}{\Delta f} \times \frac{FTR}{10} \right) + 10 \log (P_{DC}/1mW)$$

The performance of the symmetric VCO prototype is summarized in Table 5.10 and compared with the asymmetric VCO prototype as well as previously published 60GHz VCOs. The asymmetric VCO is able to achieve a very wide FTR of 25.8% with the moderate figure-of-merits (FOM and FOM_t) defined in ITRS. A large phase noise variation of 8.2dB is observed because of asymmetric design. The symmetric VCO shows improved phase noise with noise variation (σ_{PN}) of 2.5 dB is achieved in the table with a phase noise mean ($\overline{PN}$) of -108.3dBc/Hz while a high FTR of 14.2% is still maintained, leading to a state-of-art FOM_t of -179.4dBc/Hz .

5.9 90GHz VCO Prototype with CRLH T-line based RTW

The above two VCO prototypes verify the proposed inductive tuning method, which is applied in tunable CRLH T-line in Section 5.6 for RTW VCO design. To verify the proposed CRLH T-line based RTW VCO, one 90GHz VCO prototype is demonstrated in CMOS 65nm technology in this section [40]. Note a higher frequency is adopted to further demonstrate the advantages of CRLH T-line at higher frequencies.

5.9.1 90GHz VCO Design

The proposed tunable CRLH T-line based Mobius-ring RTW-VCO shown in Fig. 5.13(a) is fabricated in 65nm CMOS Global Foundries 1P8M RF CMOS technology as shown in Figure 5.30(a). To push the cut-off frequencies away from operation frequency region, each stage is implemented with 2 distributed CRLH T-line unit-cells. As a result, 180-degree phase shift is required due to the Mobius-ring connection, which leads to a 90-degree phase shift in each unit-cell. The EM simulation results for the designed unit-cell are shown in Fig. 5.30(b). At the frequency of interest 100GHz, one unit-cell can provide 90-degree phase-shift with loss at -1.86dB , which is compensated by the negative resistors realized by a cross-coupled pair. Note the unit-cell is biased to operating in the LH region, with the resonant mode in the RH region (-90-degree phase shift) highly suppressed.

(a)

(b)

Figure 5.30 (a) Die micrograph of the proposed VCO. (b) The EM simulation for one CRLH T-line unit-cell. Note that L_p is shared by two unit-cells and its value is purposely designed doubled.

5.9.2 Simulation and measurement results

The proposed VCO is fabricated 65nm CMOS Global Foundries 1P8M RF CMOS technology. The VCO core area is about 0.0812mm^2 . The output spectrum is measured by E4408B spectrum analyzer through one 11970W harmonic mixer.

The supply voltage for buffer is 1.2V and for VCO is 1V. The measured current for the core VCO is 14mA.

Figure 5.31 Measured frequency tuning range by 4 sub-bands.

Figure 5.32 Measured phase noise at 82.22GHz with 10 MHz offset frequency.

As shown in Fig. 5.31, by using the proposed tunable CRLH-T-line, a wide FTR of 29.6% is achieved from 76.59GHz to 102.01GHz, with a center frequency at 89.33GHz. The full FTR is formed from the four sub-bands controlled by two switches: (75.67-83.11GHz), (79.65-87.78GHz), (86.18-94GHz) and (93.89-102.01GHz). With a tuning voltage for varactor from 0V to 1.2V, each sub-band is fully covered. The measured phase noise varies from -100.1dBc/Hz to -98.7dBc/Hz with a sample plot shown in Fig. 5.32, where 6-9 dB deviation is observed compared with simulation, which may be due to inaccurate device and

noise models at such high frequency and imperfect ground provided during measurement. The measured output power is from -23dBm to -15dBm as shown in Fig. 5.33. The output power variation is about 8dBm.

Figure 5.33 Measured output power across the entire frequency tuning range.

As summarized in Table 5.11, the performance of the proposed VCO is further compared with other published millimeter-wave VCOs in 65nm CMOS technology. According to the Table 5.11, the phase noise is comparable with others, and the widest FTR and the best FOM_T are achieved by the proposed VCO.

Table 5.11 Performance Summary and Comparison

Parameters	[123]	[124]	[120]	This Work	Unit
f_{osc}	95.7	101	70.4	89.3	GHz
VDD_{core}	1.5	0.8	1.2	1	V
P_{DC}	9	11.9	5.4	14	mW
Phase Noise (PN) @10MHz	-106	-104.5	-106.1	-100.8	dBc/Hz
FTR (%)	3.6	11.2	9	29.6	%
FOM	-176.1	-173.8	-175.7	-168.4	dBc/Hz
FOM_T	-167.2	-174.8	-174.8	-177.8	dBc/Hz
Tech.	CMOS 65	CMOS 65	SOI CMOS 65	CMOS 65	nm

$$FOM = PN - 20 \log \left(\frac{f_{osc}}{\Delta f} \right) + 10 \log (P_{DC}/1mW)$$

$$FOM_T = PN - 20 \log \left(\frac{f_{osc}}{\Delta f} \times \frac{FTR}{10} \right) + 10 \log (P_{DC}/1mW)$$

5.10 Conclusion

This chapter studies techniques to achieve wide frequency tuning range for CMOS VCO at mm-wave frequencies. More specifically, a new inductive tuning by inductor-loaded transformer is proposed in this chapter to design a wide frequency tuning range (FTR) VCO for all sub-bands at 60GHz. Different from previously published inductive tuning methods, by configuring different current return-paths in the secondary coil of one transformer, wide multi-sub-band tuning can be achieved within compact area with only one transformer. With the use of the proposed new inductive tuning method, two VCO topologies are realized in 65nm CMOS with design targets for the maximum FTR and the balanced performance (FTR and phase noise), respectively. Measurement results show that the first VCO achieves a FTR of 25.8% from 51.9 to 67.3GHz, and a 10MHz-offset phase noise varied from -90.2 to -106.7dBc/Hz across all sub-bands; and the second VCO achieves a FTR of 14.2% from 57.0 GHz to 65.5 GHz, and a 10MHz-offset phase noise varied from -105.9 to -110.8dBc/Hz across all sub-bands. The demonstrated VCOs have shown great potential for integration in 60GHz transceiver design with wide-tuning ability.

The inductive tuning method is further applied to realize a tunable CRLH T-line for Mobius-ring RTW-VCO design in mm-wave region. Inductor-loaded transformer is implemented in CRLH T-line to realize 4 sub-bands. Each sub-band is covered by a varactor with fine-tuning. The proposed tunable CRLH T-line based RTW-VCO is fabricated in 65nm GF RF-CMOS technology with a wide FTR of 75.7-102GHz and area of 0.0821mm². The measured results show a current consumption of 14mA under supply voltage of 1V, a FTR of 29.5% with center frequency at 89.3GHz, and a phase noise of -100.8dBc/Hz with 10MHz offset at 82.2GHz frequency. The state-of-art figure-of-merit FOM_T is demonstrated at -177.78dBc/Hz.

Chapter 6

CMOS 60GHz Transceiver System Integration

6.1 Introduction

To further demonstrate the proposed power combining and frequency tuning techniques to achieve high output power density and wide tuning range for 60GHz applications, the proposed design blocks are integrated to construct a 60GHz communication system. Direct-conversion architecture is selected for the integrated 60GHz transceiver system. As mentioned in Section 2.1.2, with elimination of SAW-filter, direct-conversion architecture has the advantage of layout area and power consumption. The design challenge for 60GHz CMOS direct conversion transceiver, on the other hand, is to realize wideband gain and wide tuning range to cover the large spectrum with four channels for 60GHz high-data rate communication [138], which fits perfectly with this work for high output power density and wide tuning range design.

More specifically, based on chip realization and verification in Chapter 4, one 60GHz direct-conversion transmitter with the proposed 2×4 power combining is implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level. Based on the chip realization and verification in Chapter 5, one 60GHz PLL with the proposed symmetric inductive tuned VCO is implemented in GF CMOS 65nm technology with functionality verified by post-layout simulation at system level. The designed transmitter and PLL are further co-simulated with a 60GHz direct-conversion receiver to obtain the full functionality and performance verification for 60GHz wireless communication. Note the system level verifications in this Chapter are based on post-layout simulations without fabrication due to limited time and tape-out area. The key building blocks within each system, such as PA, VCO and divider chain, however, have been fabricated

with measurement results. The whole system may be fabricated in future for further verification in the system level.

6.2 60GHz Transmitter Design

Figure 6.1 shows the schematic of the designed 60GHz direct-conversion transmitter. It mainly consists of two parts: a 60GHz power amplifier and a 60GHz up-conversion mixer. The PA utilizes the proposed 2×4 power combining network in Chapter 4, while the mixer adopts a conventional Gilbert mixer topology.

Figure 6.1 Schematic of designed CMOS 60GHz direct-conversion transmitter.

Figure 6.2 shows the layout of the 60GHz transmitter implemented in GF CMOS 65nm technology, with an area of $1.56 \times 0.48 \text{ mm}^2$ excluding pads. Detailed designs for each block are discussed in following sub-sections.

Figure 6.2 Layout of designed CMOS 60GHz direct-conversion transmitter.

6.2.1 PA Design with 2×4 power combining

The 2D distributed power combining introduced in Chapter 4 is utilized for PA design in the 60GHz transmitter. As shown in Fig. 6.3, one 3-stage PA is implemented with the central frequency at 63.5GHz in 65nm CMOS from Global Foundries 1P8M RF CMOS technology. The first 2 stages work as drivers. A 2×4 distributed power combining array is selected for the 3rd-stage as a compromise between high output power and maintained DC power consumption. Common-source (CS) topology is used for all transistors with size of 30×1μm/60nm for the 1st stage; and 60×1μm/60nm for 2nd and 3rd stages.

Figure 6.3 Schematic of designed 60GHz PA with 3 differential stages and differential 2×4 distributed power combining network.

Different from the differential PA prototypes presented in Chapter 4, neutralization capacitors are removed from first 2 stages to reduce the sensitivity of PA's performance to process variation and minimize risk, while the stabilization is achieved through proper design of matching network. A large resistor of 1KΩ is added in series in the gate biasing to improve common-mode stabilization. Unconditional stable is checked with ports added between each stage, and ensured

for all corners and input power. Transformer matching is adopted for all matching networks.

6.2.2 Mixer design

Figure 6.4 shows the schematic of designed 60GHz up-conversion mixer. Gilbert mixer topology is adopted. In addition to higher conversion gain compared to passive mixers, Gilbert mixer also provides good linearity, isolation and LO rejection due to its double balanced structure. Two Gilbert mixer units are used for I/Q signals. The required quadrature LO signals are generated through a transformer based quadrature and two baluns. The converted I/Q RF signals are then merged together and fed to the PA through a buffer.

Figure 6.4 Schematic of designed 60GHz up-conversion mixer.

6.2.3 Simulation and measurement results

6.2.3.1 PA measurement results

The designed 60GHz PA itself is fabricated in Global Foundries 65 nm CMOS 1P8M technology and measured on CASCADE Microtech Elite-300 probe station and Agilent PNA-X (N5247A) with frequency-sweep up to 110GHz. Measurement is done at the center frequency with pads de-embedded. Open-short is used for de-embedding.

Figure 6.5 60GHz PA die photo.

Figure 6.5 shows the chip micrograph with active area of 0.37mm^2 . Figure 6.6(a) shows the measured S parameters. The power gain (S_{21}) is 16dB at 65.4GHz with -3dB bandwidth of 13.2GHz (57.1 to 70.3GHz). The PA is unconditionally stable from DC to 100GHz.

(a)

Figure 6.6 The measured S parameters of the 60GHz PA for transmitter design. (a) The PA achieves 16dB power gain at 65.4GHz with 13.2GHz bandwidth. (b) The PA is unconditionally stable over entire frequency range.

Figure 6.7 shows the summary of measured power performance at 60GHz band. With a power supply of 1.2V, OP_{1dB} of 14.4dBm and peak PAE of 8.5% is achieved at center frequency.

Figure 6.7 Measured power performance of the 60GHz PA for transmitter design.

6.2.3.2 Transmitter simulation results

The designed transmitter is simulated in Cadence. Figure 6.8 shows the simulated power spectral density (PSD) of the designed 60GHz transmitter. At the 3rd channel (62.64GHz), the transmitter can work with 3.54Gbps at OP_{1dB} and still

maintain below the mask defined by IEEE 802.15.3c standard for QPSK modulation.

Figure 6.8 Simulated power spectral density of designed 60GHz transmitter at 62.64GHz band with 3.54Gbps data rate. The requirement defined by IEEE 802.15.3c is reached.

Figure 6.9 further calculates the error vector magnitude (EVM). Output of transmitter is de-modulated and down-sampled in Matlab. The obtained EVM is -16.1dB, which fulfills the -14dB requirement by IEEE 802.15.3c standard for QPSK modulation.

Furthermore, both differential and common-mode stability are checked for each amplification stage by inserting port between adjacent stages. The LO is turned on to mimic the real operating condition, while both PVT and high power conditions need to be checked to ensure stability. The stability for PA alone has also been verified with measurement in Fig. 6.6(b).

Figure 6.9 Simulated error vector magnitude of designed 60GHz transmitter at 62.64GHz band with 3.54Gbps data rate. The requirement defined by IEEE 802.15.3c ($<-14\text{dB}$ for QPSK) is reached.

Table 6.1 summarizes the simulated transmitter performance with comparison to state-of-art 60GHz direct-conversion transmitters in CMOS technologies. Our work can provide a high output power (11dBm $\text{OP}_{1\text{dB}}$, 15.5dBm P_{sat}) within compact area (0.75mm^2) and with a DC power consumption of 319mW. Note a low power mode can be achieved by the digital control introduced in Section 4.8, where the DC power consumption is reduced to 118mW for maintained efficiency.

Table 6.1 Performance Summary and Comparison with State-of-art CMOS 60GHz Direct-conversion Transmitters

	Tech. (CMOS)	Vdd (V)	Freq (GHz)	CG (dB)	$\text{OP}_{1\text{dB}}$ (dBm)	P_{sat} (dBm)	Pdc (mW)	Area (mm^2)
ISSCC'11 [17]	65nm	1.2	60 band	18.3	9.5	10.9	186	3.5
ISSCC'10 [139]	65nm	1.2	75-95	8.5	2.2	6.6	120	1.2
JSSC'13 [138]	65nm	1.2	60 band	18	-2	6	137	1.43
JSSC'09 [13]	90nm	1.2	60 band			10	101.4	
ASSCC'08 [140]	130nm		60 band		2	5		8.4

RFIT'12 [141]	65nm	1.2	77		-2	0	130	2.7
ASSCC'11 [142]	65nm	1.2	60 band	16	5.4	6.5	181	2.5
RFIC'11 [143]	45nm	2	60 band	15	10		360	0.23
Simulation (High power mode)	65nm	1.2	60 band	28	11	15.5	319	0.75
Simulation (Low power mode)	65nm	1	60 band	20.6	6.7	12.4	118	0.75

6.3 60GHz PLL Design

Figure 6.10 shows the schematic of the designed 60GHz PLL. It mainly consists of a 60GHz VCO, a divider chain, a phase frequency detector (PFD), a charge pump, a low pass filter (LPF) and a reference clock. The 60GHz VCO adopts the proposed symmetric inductive tuning method in Chapter 5 to achieve a wide FTR. The divider chain includes a 60GHz divide-by-2 divider, a 30GHz divide-by-2 divider, a dynamic current-mode logic (DCML) divide-by-4 divider, and a programmable divider. The LPF is realized off-chip, and the reference clock is generated through a 54MHz crystal oscillator.

Figure 6.10 Schematic of designed CMOS 60GHz PLL.

Figure 6.11 shows the implemented layout of the 60GHz PLL in GF CMOS 65nm technology, with an active area of $0.68 \times 0.64 \text{mm}^2$ excluding pads. One testing point is inserted after the DCML divider for tuning of bias and debugging.

Figure 6.11 Layout of Designed CMOS 60GHz PLL.

Voltage-controlled oscillator (VCO) and high frequency divider are two major designing blocks in PLL at 60GHz. Considering the required wideband at 60 GHz and also process variation in nano-scale CMOS, a wide frequency locking range is typically required for 60GHz PLL design, which demands for wide frequency-tuning-range (FTR) of VCO and wide locking range of divider. In the following sub-sections, the design details for VCO and high frequency portion of divider chain are provided.

6.3.1 VCO Design with inductive tuning

The proposed new inductive tuning in Chapter 5 is utilized for VCO design in the 60GHz PLL. To achieve a wide FTR with maintained phase noise performance, the VCO prototype presented in Section 5.8 with symmetric inductive tuning is selected.

6.3.2 Divider design

Various frequency dividers have been explored for different applications. Generally, frequency dividers can be classified into digital and analog classes. The digital class of dividers can be sub-divided into current-mode logic (CML) dividers

[144] and dynamic divider [145]; and the analog class of dividers can be subdivided into Miller dividers [146] and injection-locked frequency dividers (ILFD) [115, 147, 148]. Dynamic dividers are easy to design that operate at low frequency with wide range and variable division-ratio. CML and Miller dividers can operate at higher operating frequency with wide locking range, but usually suffer from high power consumption. Compared with Miller frequency dividers and CML dividers, ILFD can achieve higher operating frequency with lower power consumption. Its major limitation, however, is the limited locking range.

In the design of divider chain in 60GHz PLL, according to different operating frequencies, the choice of the divider structure in each dividing stage will be different. The first stage divider operates at the highest frequency in the divider chain, and thus the ILFD is usually employed. The last stage divider operates at the lowest frequency in the chain, and thus dynamic divider is usually employed due to the simple structure and variable division-ratio. The remaining stages can be designed with CML and Miller dividers for their wide locking range. The major challenge is to design the first stage divider with a wide locking range to cover the wide frequency range at 60GHz. To increase the locking range of the ILFD, varactors are usually deployed to tune the self-oscillation frequency of ILFD. However, a large varactor will severely degrade the phase noise of ILFD and PLL. Capacitor banks can be used to realize multi-band operation [115]. However, as frequency scales up to 60GHz, the large parasitic capacitance from the capacitor bank becomes too large and the quality factor of capacitor decreases significantly [126, 149].

As introduced in Chapter 5, inductive tuning has recently become a promising substitute to replace the capacitive tuning, and is used in 60GHz VCO design to realize a wide FTR. Besides a wide FTR, inductive tuning can also provide the benefit of isolated DC noise from the tuning element. The same mechanism could be used in high frequency divider design to realize a large locking range. In this section, an inductor-loaded transformer is introduced into the conventional ILFD structure to improve its locking range by creating multiple frequency bands.

The locking range (LR) for an injection locked oscillator is given by [147]

$$LR = \frac{1}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (6-1)$$

where I_{osc} , I_{inj} and Q are the oscillator and injection current and quality factor of the LC-tank, respectively. Thus, for larger LR , the quality factor of the LC-tank should be balanced. The second important consideration of LR is on the effective injection current (I_{inj}) reaching the oscillator core. To enhance the LR , the internal injection power while using the same external injection should be maximized. The input signal can be injected at tail-node [6] or direct across the LC-tank [5]. Due to the loss of injection power in the parasitic capacitance of the tail-node injection, direct injection is employed to improve the injection efficiency in this work.

Figure 6.12 Schematic of switch-inductor loaded transformer based ILFD

The introduced switching inductor loaded transformer in Chapter 5 is utilized here for 60GHz divider design, where one new type of ILFD is proposed in this section. As shown in Fig. 6.12, the input injection transistor is placed across the LC-tank. The cross coupled transistors generate negative resistance to compensate

the energy loss in the LC-tank. The injection locking will occur when the self-oscillation frequency of the ILFD is close to the half of the input signal. The switching inductor loaded transformer can change the inductance of the LC-tank, and then finally change the self-oscillation frequency, which leads to multi-band operation for wide locking range.

Figure 6.13 Schematic of 30GHz ILFD.

Figure 6.14 Schematic of the 60GHz divider chain.

In addition to the divide-by-2 operation, another two divide-by-2 dividers are implemented at lower frequency region to realize a divide-by-8 divider chain. The second stage divider is implemented with Miller divider topology [146] as shown in Fig. 6.13. Transistors M3 and M4 are designed with smaller size than M1 and M2 to lower the Q-factor in LC tank, thus increasing the locking range. M5 and M6 are dummy transistors to provide balanced matching condition for differential inputs. The third stage divider is implemented with a common CML topology. Figure 6.14 shows the schematic for the whole 60GHz divider chain.

6.3.3 Simulation and measurement results

The designed 60GHz PLL prototype is implemented in Global Foundries 65 nm CMOS 1P8M technology. Both the 60GHz VCO and 60GHz divider chain have been fabricated separately with measurement results. The VCO measurement has been shown in Section 5.8.

6.3.3.1 Divider measurement results

Figure 6.15 shows the chip micro-photo of the fabricated divider, which occupies core area of 0.058 mm^2 . The DC power of the ILFD is 6.3mW under 0.75V power supply. The whole divider circuit is designed and verified with EM simulation (ADS-Momentum) before fabrication. The measurements are then done on CASCADE Microtech Elite-300 probe station with Agilent PNA-X spectrum analyzer.

Figure 6.15 60GHz divider chain die photo.

Figure 6.16 shows the measured input sensitivity curve. Two sub-bands are clearly observed by switching inductor loaded transformer. The first sub-band has a free-running frequency around 63GHz, and the second sub-band has a free-running frequency around 66GHz. With input power of 0dBm, and the locking range for the first band is from 60.8 to 65.1GHz, while the locking range for the second band is from 64.7 to 67GHz. The obtained total locking range is thus 9.7% from 60.8 to 67GHz, with a center frequency of 63.9GHz. Figure 6.17(a) shows the ILFD output spectrum at 63GHz after the first division, where a 31.5GHz signal is obtained. The functionality of the full divider chain is also examined. Figure 6.17(b) shows the divide-by-8 divider chain output spectrum at 63GHz, where a 7.875GHz output is obtained.

Figure 6.16 Measured sensitivity curve of the 60GHz ILFD.

Figure 6.17 Measured divide-by-2 and divide-by-8 output spectrums at 63GHz input signal..

6.3.3.2 PLL simulation results

The designed PLL is simulated in Cadence. Figure 6.18 shows the transient simulation of the locking process at the 3rd band (62.64GHz). The control voltage is settled to 783mV at around 7 μ s.

Table 6.2 summarizes the DC power consumption in each block of PLL. The total power consumption is 66.4mW including buffers.

Figure 6.18 Simulated locking process of designed 60GHz PLL at 62.64GHz.

Table 6.2 Simulated DC Power Comparison

Building blocks	Current (mA)	Supply (V)	Power (mW)
Charge Pump	2	1.2	2.4
PFD			
Programmable Divider	1.85	1.2	2.22
Shaping Buffer			
DCML /4 divider	3	1.2	3.6
30 GHz divider	5.5	1.2	6.6
60 GHz divider	9	0.8	7.2
LO buffer	15	1.2	18
Oscillator	22	1.2	26.4
Total			66.4

The PLL performance is summarized in Table 6.3 with comparison to state-of-art CMOS 60GHz PLLs. Our work can provide a wide tuning range (57-65.5GHz) with good phase noise performance (-95dBc/Hz @1MHz).

Table 6.3 Performance Summary and Comparison with State-of-art CMOS 60GHz PLLs

	[150]	[151]	[152]	[153]	This work (sim.)
Technology (CMOS)	90nm	90nm	90nm	65nm	65nm
VCO tuning range (GHz)	61.1-63.1	58-60.4	78.1-78.8	75.6-76.3	57-65.5
Phase noise (dBc/Hz @ 1MHz)	-80	-85.1	-85	-85.3	-95 -89
Supply (V)	1.2	1.2	1.2	1.2	1.2
Reference freq. (MHz)	60	234.1	75	700	27
Power (mW)	78	80	101	73	66.4
Core area (mm ²)	0.36	0.95	0.62	N.A.	0.41 (w/o LPF)

6.4 60GHz Transceiver Design

The designed transmitter (TX) and PLL are further co-simulated with a direct-conversion receiver (RX) in GF CMOS 65nm technology for evaluation of the whole 60GHz communication system. Figure 6.19 shows the layout of the whole 60GHz transceiver. Off-chip antennas will be bonded to TX and RX from PCB. Other off-chip components include a 54MHz crystal oscillator and a LPF, both for PLL operation. The total chip area is $1.8 \times 3.6 \text{ mm}^2$ including pads. Except TX and PLL introduced in previous sections, the RX and LO distribution will be discussed in following sections, as well as the co-simulation for the whole system.

Figure 6.19 Layout of Designed CMOS 60GHz TRX.

6.4.1 Review of 60GHz receiver

Direct-conversion receiver has been widely explored at 60GHz [12, 154-158], with key building blocks such as low noise amplifier (LNA), down-conversion mixer, and variable gain amplifier (VGA). The work presented in [159] has been adopted in this thesis for system simulation. The schematic of the 60GHz receiver is shown in Fig. 6.20(a). Note the receiver topology is modified from [159] to support I/Q branches.

Figure 6.20(b) shows the schematic of the 60GHz LNA. It consists of 4 stages. The 1st stage is implemented with inductive source generation to optimize the noise figure (NF) performance with reduced power gain. The following 3 stages are designed with common source topology to achieve high conversion gain. Again, the design is modified from [159] with one additional stage to provide enough driving capability for two branches instead of one.

Figure 6.20 Schematic of designed 60GHz direct conversion receiver: (a) system view, (b) LNA design.

The down-conversion mixer is realized with transconductance mixer topology for lower DC power consumption due to the biasing in sub-threshold region. Same as in transmitter design, a compact quadrature coupler is used to generate the required quadrature signals for operation of transconductance mixer.

The VGA is realized by a conventional 4-stage modified Cherry-Hooper amplifier with improved efficiency, high gain-bandwidth product and elimination of inductor. A wide gain tuning range of around 50dB can be achieved with 2mW power consumption.

6.4.2 LO distribution

Except for TX, RX and PLL, LO distribution is required for 60GHz communication system to distribute the LO signal from PLL to TX and RX with enough driving capability and sometimes multi-phase generation. Figure 6.21(a) shows the schematic for the designed LO distribution. The output LO signal from PLL is first split into two branches and fed to TX and RX with a Wilkinson power divider. Two driver stages shown in Fig. 6.21(b) are added after the divider to boost LO power. For the RX side, a quadrature coupler is used to generate I/Q LO signals. Two additional drivers shown in Fig. 6.21(c) are further added after the hybrid to provide enough driving power for RX. Note for the TX side, part of LO distribution is already discussed in Section 6.2 as part of the TX design, with a hybrid coupler and two baluns.

Figure 6.21 Schematic of designed 60GHz LO distribution: (a) overview, (b) driver 1 design, (c) driver 2 design.

6.4.3 System testing and verification

The designed 60GHz transceiver is to be bonded to two separate PCB boards, each with only one mode (TX or RX) activated. The antennas are designed on PCB and bonded to TX and RX, respectively. End-fire antenna [160] is selected for its high directivity and high gain. The estimated antenna gain is 9dBi with consideration of loss from bonding wires. The two PCBs are interfaced with external equipments such as power supply and arbitrary waveform generator (AWG), oscilloscope, which are all controlled with a laptop. On the TX side, the AWG generates modulated signals into TX, which are up-converted and radiated out. On the RX side, the received signal from antenna is down-converted and fed through oscilloscope and analyzed in laptop. Measurement results such as constellation diagram, error vector magnitude (EVM) and bit error rate (BER) can then be obtained.

Figure 6.22 Measurement setup of the designed 60GHz direct communication transceiver.

6.4.4 Simulation results

The whole 60GHz direct communication system is simulated in Cadence with setup shown in Fig. 6.23. The baseband modulated signal (BB) is generated through Matlab as input for TRX simulation in Cadence. The outputted BB signal is again fed to Matlab for analysis. One attenuator is inserted between TX and RX to emulate the free path loss during communication, which gives following relation:

$$(6-2) \quad T_{dBm} - R_{dBm} = A_{dB},$$

where T_{dBm} , R_{dBm} and A_{dB} are transmitter output power, receiver input power, and attenuation, respectively. Combined with equation (2-5) in Chapter 2, the attenuation can be decided for a given communication distance R :

$$(6-3) \quad A_{dB} = 92.4 + 20 \log(f) + 20 \log(R) - G_{TX} - G_{RX},$$

where f is the carrier frequency, G_{TX} and G_{RX} are antenna gains for TX and RX, respectively. Note the Link Margin (LM) in equation (2-5) is ignored for simulation.

Figure 6.23 Simulation setup of the designed 60GHz direct communication transceiver.

Figure 6.24 shows the simulated error vector magnitude (EVM) for a communication distance of 3 meters with 3.54Gbps data rate using QPSK modulation in the 3rd channel (62.64GHz). According to (6-3), an attenuation of 60dB is added between TX and RX, with 9dBi antenna gain assumed based on end-fire antenna topology [160] on PCB. The obtained EVM is -12.6dB. The eye diagram for both I and Q channels are further shown in Fig. 6.25. The simulation results are summarized in Table 6.4 with comparison to state-of-art CMOS 60GHz direct-conversion transceivers. With proposed power combining and frequency tuning techniques, this work can realize a high data-rate communication with longer distance. The drawback is relatively high power consumption to realize higher output power, which can be lowered with implemented low-power mode.

Figure 6.24 Simulated error vector magnitude of designed 60GHz transceiver at 3rd channel (62.64GHz) with 3.54Gbps data rate and a communication distance of 3 meters.

Figure 6.25 Simulated eye diagram of designed 60GHz transceiver at 3rd channel (62.64GHz) with 3.54Gbps data rate and a communication distance of 3 meters.

Table 6.4 Performance Summary and Comparison with State-of-art CMOS 60GHz direct-conversion transceivers

	Data rate / Modulation	Distance w BER<10⁻³	Integration (CMOS)	Power Consumption	Area (mm²)
UCB [13]	4Gb/s-QPSK, 7Gb/s-QPSK (loop-back)	1m with 25dBi external horn antenna	90nm, single-chip TRX inc. 30G PLL with 90 hybrid and BB	179mW (Tx mode) 138mW (Rx mode)	6.88
U. Toronto [12]	4Gb/s-BPSK	2m with 25dBi external horn antenna	65nm, single-chip TRx w/o LO	374mW (1.2V) 233mW (1V)	1
Tokyo Tech. [15]	3.52Gb/s-QPSK with 2.16G BW; 8Gb/s-QPSK with a wider BW; 11Gb/s-16QAM	2.7m/QPSK with 2dBi antenna in package	65nm, single chip TRx with 60GHz Q osc., PLL	186mW (Tx mode) 106mW (Rx mode) 66mW (PLL inc. buffer)	7.3 (TRx) 1.2 (PLL)
Tokyo Tech. [142]	10 Gb/s-QPSK 16 Gb/s-16QAM	>0.1m/QPSK; >0.0 2m/16QAM; with 2dBi antenna in package	65 nm, single-chip, TRx with 60 GHz quad. Osc, 20G PLL	181mW (Tx mode) 138mW (Rx mode)	4.8 (TRx) 1.2 (PLL)
This work (sim.)	3.54Gb/s-QPSK with 2.16G BW	~10m/QPSK (high power mode); ~6m/QPSK (low power mode); with 10dBi antenna in PCB	65nm, single chip TRx with 60GHz PLL	391mW (Tx high power mode) 190mW (Tx low power mode) 174mW (Rx mode)	6.48

Chapter 7

Conclusions and Future Research

7.1 Conclusions

CMOS on-chip composite right/left-handed transmission line (CRLH T-line) is explored in this thesis at mm-wave frequency to overcome the fundamental limitation posed by traditional right-handed (RH) T-line. Due to its nonlinear negative phase change in left-handed region, one can implement distributed transmission with unique in-phase (or zero-phase) as well as wide frequency-tuning-range (FTR) properties that can be utilized in active mm-wave circuit designs such as power amplifier (PA) and voltage-controlled-oscillator (VCO). As demonstrated in CMOS 65nm technology, one active in-phase CRLH T-line network is developed in Chapter 4 as 2D power combiner to improve both output power density and bandwidth performance of CMOS PA; while one tunable negative-phase CRLH T-line is developed in Chapter 5 to achieve wide FTR for CMOS VCO design. On-chip prototypes for both mm-wave PA and VCO demonstrate state-of-art measurement results. Along with the system verification in Chapter 6, the feasibility and effectiveness for on-chip metamaterial are fully demonstrated, suggesting its potential for CMOS mm-wave integrated circuit design.

Critical components such as PA and VCO are demonstrated with the use of CRLH T-line at 60GHz in CMOS 65nm with measurement results. For example, one 60GHz PA prototype with proposed 4×4 power combining network achieves 17.5dB gain, peak PAE of 11.3%, 8.8GHz bandwidth (54 to 62.8GHz), and 16.6dBm output power with 95.2mw/mm^2 output power density. One 60GHz VCO prototype with proposed inductive tuning method achieves a FTR of 25.8% from 51.9 to 67.3GHz with phase noise of -106.7dBc/Hz at 10MHz offset. In addition, the entire CMOS 60GHz communication is also integrated with validation by post-layout simulation.

7.2 Recommendations for Further Work

Based on above works, there are five recommended future works for this thesis.

The first recommended work is to fabricate and measure the 60GHz communication system for further verification in the system level. The 60GHz transceiver can be further implemented with digital calibration as discussed in Section 4.8 for performance optimization and minimize performance degradation caused by PVT variation such as DC offset, IQ mismatch, and signal imbalance for different combining branches. Furthermore, as mentioned in Section 4.6.1, the proposed 2D distributed power combining topology can be extended for phased-array applications by replacing ZPS with an array of tunable phase-shifters.

The second recommended work is to explore a larger 2D power combining network introduced in Chapter 4 for PA design. As discussed in Chapter 4, there is an optimized network size for the proposed combining topology. But as the combiner size increases from 2×2 to 2×4 and then to 4×4 , the power performance keeps improving and hasn't reached its optimum point yet.

The third recommended work is to explore higher frequency applications in mm-wave and THz region. As frequency further rises from 60GHz, the metamaterial size can be further reduced, which provides more compact size and also allows a larger unit cell array size. A larger array size may be used to generate more special properties of metamaterial, such as optical transformation. In some particular cases such as RTW VCO design in Chapter 5, metamaterial also shows more benefits at higher frequency, which can be further explored.

The fourth recommended work is to extend the metamaterial into more complex 2D arrays. The above mentioned works mainly focus on 1D CRLH T-line. Though a 2D combining network is proposed in Chapter 4, the connection is only at one end and not uniform in both directions. A 2D array can provide more metamaterial properties and can be explored for some special applications such as electrical funnel.

The fifth recommended work is to explore on-chip metamaterial in other building blocks in addition to PA and VCO. As mentioned in Chapter 2, metamaterial has been widely explored at PCB level within GHz region for various

design blocks and can be similarly extended for on-chip applications in mm-wave and THz regions.

Author's Publication

- J6. **Wei Fei**, Hao Yu, Haipeng Fu, Junyan Ren, and Kiat Seng Yeo, "Design and Analysis of Wide Frequency-tuning-range CMOS 60GHz VCO by Switching Inductor Loaded Transformer", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 3, pp. 699-711, Mar. 2014.
- J5. Yang Shang, Hao Yu, and **Wei Fei**, "Design and Analysis of CMOS based Terahertz Integrated Circuits by Causal Fractional-order RLGC Transmission Line Model", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol.3, no.3, pp355-366, Sep. 2013.
- J4. **Wei Fei**, Hao Yu, Yang Shang, Deyun Cai, and Junyan Ren, "A 96 GHz Oscillator by High-Q Differential Transmission Line loaded with Complementary Split Ring Resonator in 65nm CMOS", *IEEE Transactions on Circuits and Systems II (TCAS-II)*, vol.60, no.3, pp127-131, Mar. 2013.
- J3. **Wei Fei**, Hao Yu, Yang Shang, and Kiat Seng Yeo, "A 2D Distributed Power Combining by Metamaterial-based Zero-Phase-Shifter for 60GHz Power Amplifier in 65nm CMOS", *IEEE Transactions on Microwave Theory and Techniques (TMTT)*, vol.61, no.1, pp505-516, Jan. 2013.
- J2. Yang Shang, **Wei Fei**, and Hao Yu, "Analysis and Modeling of Internal State Variables for Dynamic Effects of Nonvolatile Memory Devices", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, vol.59, no.9, pp1906-1918, Sep. 2012.
- J1. **Wei Fei**, Hao Yu, Wei Zhang, and Kiat Seng Yeo, "Design Exploration of Hybrid CMOS and Memristor Circuit by New Modified Nodal Analysis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol.20, no.6, pp1012-1025, Jun. 2012.
- C8. **Wei Fei**, Hao Yu, Yuan Liang, and Wei Meng Lim, "A 54 to 62.8GHz PA with 95.2mW/mm² Output Power Density by 4×4 Distributed In-phase Power Combining in 65nm CMOS", *IEEE International Microwave Symposium (IMS)*, Jun. 2014.

- C7. Haipeng Fu, **Wei Fei**, Hao Yu, Junyan Ren, "A 60.8-67GHz and 6.3mW Injection-Locked Frequency Divider with Switching-Inductor Loaded Transformer in 65nm CMOS", *IEEE International Microwave Symposium (IMS)*, 2014.
- C6. Shunli Ma, **Wei Fei**, Hao Yu, and Junyan Ren, "A 75.7GHz to 102GHz Rotary-traveling-wave VCO by Tunable Composite Right /Left Hand T-line", *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013.
- C5. **Wei Fei**, Hao Yu, Wei Meng Lim, and Junyan Ren, "A 53-to-73GHz Power Amplifier with 74.5mW/mm² Power Density by 2D Differential Power Combining in 65nm CMOS", *IEEE International Symposium of Radio-frequency Integrated Circuits (RFIC)*, Jun. 2013.
- C4. Yang Shang, **Wei Fei**, and Hao Yu, "Fractional-order RLGC Model for Terahertz Transmission Line", *IEEE International Microwave Symposium (IMS)*, June 2013.
- C3. Yang Shang, Deyun Cai, **Wei Fei**, Hao Yu, and Junyan Ren, "An 8mW Ultra-low Power 60GHz Direct-conversion Receiver with 55dB Gain and 4.9dB Noise Figure in 65nm CMOS", *IEEE International Symposium of Radio-frequency Integration Technology (RFIT)*, Nov. 2012.
- C2. **Wei Fei**, Hao Yu, Kiat Seng Yeo, and Wei Meng Lim, "A 60GHz VCO with 25.8% Tuning Range by Switching Return-Path in 65nm CMOS", *IEEE Asia Solid-State Circuits Conference (A-SSCC)*, Nov. 2012.
- C1. **Wei Fei**, Hao Yu, Kiat Seng Yeo, Xiong Liu, and Wei Meng Lim, "A 44-to-60GHz, 9.7dBm P_{1dB}, 7.1% PAE Power Amplifier with 2D Distributed Power Combining by Metamaterial-based Zero-Phase-Shifter in 65nm CMOS", *IEEE International Microwave Symposium (IMS)*, Jun. 2012.

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