Electrical properties of AU-GE solder under high temperature

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2014

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ABSTRACT

Ruggedized electronics are defined as electronics that can withstand harsh operating environment. A key requirement for ruggedized electronics is reliability. One of the areas for reliability study is solder interconnects. Solder is used to deliver electric signal and power, and is a critical component in electronics package assembly. Operating under high temperature may impact its electrical property. Another reliability issue in solder interconnect is electromigration (EM). This issue will worsen with increasing current density due to miniaturization, or with a higher operating temperature as required in ruggedized electronics. The use of high temperature solders is relatively new with limited research, and this work aims to understand their reliability physics.

The effect of thermal aging on the electrical resistivity of bulk Au-Ge and electrical resistance on Au-Ge solder joint was studied. It is observed that the electrical resistivity in bulk Au-Ge will decrease with aging and stabilize to a lower value. This is due to the effect of Au grain growth which reduces the grain boundaries that leads to lesser electrons scattering. On the other hand, electrical resistance in Au-Ge solder joint increases after aging. This is contributed by the growth of intermetallic compound (IMC), and micro voids in electroless-Ni (P) layer. Ni will react with Ge to form IMC that contributes to the increase in electrical resistance. This study concludes that Au-Ge is potential candidates as a high temperature solder interconnection for ruggedized electronics, but its reliability is compromised by the Ni diffusion barrier. Lastly, EM behavior in Au-Ge was also studied. It shows that EM results in void growth that leads

to open failure, and polarity growth of IMC at the interface. Polarity growth causes the IMC growth to be enhanced at the anode side, while IMC growth is retarded at the cathode side during the EM stressing. This will further degrade the reliability of the Au-Ge solder under high temperature and current density.

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LIST OF ABBREVIATION

CMOS	Commentary Metal-Oxide Semiconductor
IO	Input/Output
FIB/SEM	Focus Ion Beam/Scanning Electron Microscope
UBM	Under bump Metallization
PVD	Physical Vapour Deposition
Au-Ge	Gold-Germanium
Au-Si	Gold-Silicon
Au-Sn	Gold-tin
ENIG	Electroless Nickel Immersion Gold
EM	Electromigration
Ni-Ge	Nickel-Germanium
Sn-Pb	Tin-Lead
IMC	Intermetallic Compound
XRD	X-Ray Diffraction
EBSD	Electron Backscatter Diffraction
EL-Ni(P)	Electroless-Nickel (Phosphate)
EDX	Energy-Dispersive X-ray Spectroscopy

Wt. %	Weight %
At. %	Atomic. %

CHAPTER 1: INTRODUCTION

1.1 Background

As deep earth exploration transits into deeper earth, it faces challenges like producing reliable microelectronics devices that will not degrade under high temperature and high pressure environment. Numerous physical issues limit the manufacturing of this type of reliable microelectronics devices. They are mainly related to packaging materials and assembly of the microelectronics devices. Another area of concern is the understanding of the reliability physics to evaluate the performance of microelectronics devices under these harsh environments. There are various reliability issues that are of interest in evaluating the performance of ruggedized electronics. One of the key issues is interconnects reliability. Interconnect is a metallic electrical conductor which provides electrical connections within the electronic package, as well as to the external world.

In this chapter, key metallization scheme will be discussed, and interconnect reliability associated with the metallization scheme will be highlighted. Finally, the objectives of the thesis will be presented.

1.1.1 On-Chip Metallization (Thin film interconnect line)

On chip metallization is found within a chip which connects individual semiconductor devices together through the metallization. The metallization found in the chip is made up of at least 2-6 levels of metal wirings, but as the miniaturization of complementary metal-oxide-semiconductor (CMOS) advances, the level of metal wiring also increases. Figure 1.1 shows the typical cross sectional view of the metallization scheme that connects the devices. Due to the trend of miniaturization, the current density in the metallization will increase, and

worsen electromigration (EM) [1]. Electromigration is dependent on the current density and temperature. With a high operating temperature in ruggedized electronics and miniaturization in circuits, this may be a critical reliability issue [2]. However, the reliability physics of electromigration in the interconnect is well established, and solution may be available to be used in a ruggedized environment.

1.1.2 Off-chip metallization (Solder bump)

Figure 1.1 Cross-sectional view of on chip metallization [3]

Solder bumps are generally used in flip chip packages. The primary function of a solder bump provides electrical connection between a silicon chip, printed circuit board, and providing mechanical support. The advantages of flip chip interconnection are the high number of Input/Output (I/O), shorter electrical paths and smaller form factor [4]. Figure 1.2 illustrates a cross sectional view of a solder ball in a package.

Figure 1.2. Schematic of a solder ball connecting the chip to substrate[5]

The common reliability issues of solder are associated with mechanical strength degradation, electromigration, thermomigration and electrochemical migration [6-9]. Particularly, electromigration in solder has become a concern due to miniaturization. It is expected that current in solder may increase from 0.2 A to 0.4 A for a future solder bump diameter of 50 μm in diameter [10].

The current widespread use of eutectic lead-free solder which has a melting point of 220°C , and the electromigration property of such solder has been investigated widely [11-13]. On the other hand, the high operation temperature of 300°C in ruggedized electronics promotes the usage of high temperature solders. However, limited research is done to evaluate the reliability performance of high temperature solders, and recent work that is only related to mechanical property is reported [14]. Furthermore, the usage of high temperature solders under high operating temperature of 300°C will result in intermetallic compound (IMC) formations which may impact its reliability. It will be of interest to study the effect of aging and stressing on the high temperature solders. Despite different metallization schemes in a

package, high temperature solder bump will be the project focus as it is a critical component in the packaging assembly.

1.1.3 Requirements of Commercial Electronics and Ruggedized Electronics

Typically, higher reliability is expected for ruggedized electronics. Table 1.1 shows a comparison of the requirements between commercial and ruggedized electronics. Typically, higher temperature is expected in ruggedized electronic [15, 16]. This translates to different types of packaging materials to be used as compared to commercial electronics. The maximum current density for an intermediate wire in commercial electronics can go up to 1.3 MA/cm² [17]. As the current density increases with scaling, electromigration is a concern here. However in ruggedized electronics, scaling happens slower and the maximum current density is often lower as compared to commercial electronics. The lifetime in the commercial electronics can be up to years but in ruggedized electronics, it can be range from months to years [18], which is dependent on the type of application and environment.

Table 1.1. Summary of the requirements

	Commercial Electronics	Ruggedized Electronics
Temperature (°C)	0 -70	>150
Current Density Max-Intermediate Wire (MA/cm ²) at 105°C	1.3	Less than 1.0
Lifetime	Intermediate - up to years	Military: Long-Up to years Oil and gas: Short, months

1.2 Objectives

This thesis evaluates the electrical property of Au-Ge under 300°C for up to 500 h. The objectives are:

- To study the effect of aging on the electrical resistivity of bulk Au-Ge solder
- To study the effect of aging on the electrical resistance of Au-Ge solder joint
- To investigate the effect of electromigration on Au-Ge solder joint

1.3 Scope

The impact of aging on the electrical resistivity of bulk Au-Ge and electrical resistance on Au-Ge solder joint will be studied in the first part of the thesis. Microstructure characterization such as Scanning Electron Microscopy (SEM) will evaluate the interfacial reaction of the solder with the Under Bump Metallization (UBM). Fabrication of the daisy chain test structure will use Physical Vapor Deposition (PVD) and electroless plating process. This test structure allows electrical testing and electromigration testing through the solder. Lastly, reliability of the solder will be evaluated based on its microstructure evolution and electrical property.

1.4 Organization of the report

The report structure is as follows:

Chapter one (Introduction) provides a background of the project, objectives and scope. Chapter two (Literature Review) discusses the electromigration effect on both on chip metallization and off chip metallization and Au-Ge property. Chapter three (Experimental Techniques) will give an insight on the fabrication of test vehicle and testing methods.

Chapter four (Effect of aging on Au-Ge) will discuss the effect of aging on bulk Au-Ge and solder joint's electrical property and microstructure. Chapter five (Effect of Aging on Au-Ge Solder's Joint) discuss the effect of electromigration on the Au-Ge. Lastly, in chapter six will be the Conclusion and Recommendations for future work.

CHAPTER 2: LITERATURE REVIEW

2.1 Property of High Temperature Solder: Au-Ge

The operating temperature of ruggedized electronics can be as high as 300°C, and the choice of the solder that fulfills the requirement is limited. Furthermore, the criteria of a high temperature solder requires a melting point that is higher than the operating temperature, while the processing temperature of the solder must be below 400°C. This is because temperatures above 400°C will induce damage to the active devices in the die. The convectional type of SnPb based solders are unable to be used due to its lower melting point. The possible candidates for high temp solders are shown in Figure 2.1. Among all the possible candidates, only Au-Ge and Gold Silicon (AuSi) has the potential to be used in ruggedized electronics because their melting point satisfies the requirement. Zn based solder is not considered because the solder will corrode under an acidic environment.

Figure 2.1. High temperature solders candidate [19]

Thermal aging test is used as a test to evaluate the reliability of solder joints. Thermal aging results in the growth of IMC which may impact the electrical resistance and mechanical property [20-22]. According to the thermal aging work by Nachlappan et.al [19], it shows a decrease in mechanical strength of Au-Ge but it is still able to fulfill the minimum mechanical requirement in ruggedized electronics, especially in oil and gas exploration. It also concluded that electroless nickel immersion gold (ENIG) serves as a prospective UBM candidate. The layer of gold in the surface finish creates a solder adhesion which will be consumed by the molten solder during melting, and once this layer is consumed, it provides good adhesion to the next layer of unoxidized metal [23]. Nickel serves as both a diffusion layer and wetting layer, and is reported to have a wetting angle of 14° . The nickel surface will form NiGe IMC, which can prevent dissolution of Ni into the Au-Ge solder [24]. However, little literature has evaluated the electrical property of Au-Ge under thermal aging.

Au-Ge is a two phase solder system as illustrated in Figure 2.2. It consists of only Au and Ge phase, and has an eutectic composition of Au-12Ge (Wt. %), with a melting point of 361°C . This phase diagram suggests the solubility of Ge into Au phase is very low, with a maximum of ~3% at 361°C .

Despite the advantage of Au-Ge solder, it is reported that gold based solder requires pressure and heat for bonding, known as thermo compression bonding. In similar experiments of using gold based solder Gold Tin (AuSn) as die attach, it requires at least 40 – 60 psi pressure for bonding [25]. The pressure will vary with the type of UBM

Figure 2.2. Au-Ge phase diagram [27]

used. Another concern for Au-Ge is the grain coarsening effect of the dispersed Ge phase during high temperature storage [14, 26]; such an effect will likely decrease the mechanical strength of the solder.

2.2 Mechanical reliability of Au-Ge

The mechanical reliability of solder joints is one of the concerns in the ruggedized electronics. Prolong ageing in high temperature environment will lead to the excessive growth of IMCs which make the solder prone to brittle failure as the IMC's nature are brittle. Various testing characterization such as tensile stress test, shear test, fatigue and nano-indentation are used to evaluate the mechanical properties of solders. Among all the characterization test, tensile and shear test allow the load capacity of the joint to be known. Existing literature had determined that Au-Ge solder has ball shear strength of 10.8 g/mil^2 after 500 hours (h) of aging. This value higher than the military standard of 5.6 g/mil^2 [28]. Other literature [29] had evaluated the die shear strength of the solder to

be 44 MPA after 1500 h of aging. Existing literatures conclude that the solder joint is mechanically reliable but strongly dependent on the type of barrier system been used.

2.3 Electromigration physics

Electromigration (EM) is defined as mass transport caused by high electric current density, where the charge transport is electronic [30]. EM occurs when an electric current is applied to an electrical conductive material [31, 32]. The electrons transfer momentum to the conductor's atoms during collision, which results in electron wind force F_1 , and causes the atoms to drift in the direction of the electron wind force. F_2 represents direct electrostatic force. These forces are illustrated in Figure 2.3. These two forces act in opposite directions, the direct force involves the movement of positive metal ions due to the application of electric field, while the electron wind force is exerted on the metal ions due to the electrons momentum transfer. The electromigration force can be expressed by the sum of the direct and electron wind forces summarized in equation 2.1.

$$F_{em} = F_1 \text{ (wind)} + F_2 \text{ (electrostatic)} \dots\dots\dots (2.1)$$

Figure 2.3. Forces acting on a metallic conductor due to current stressing

The electromigration force can be expressed further by equation 2.2 where the total momentum transfer between charge carriers and moving ions is related to the effective contribution to the resistivity associated with ions in the activated configuration for diffusion [33, 34].

$$F_{em} = e.E(Z^*_D - Z \left[\frac{\rho_d}{\rho} \right] \left[\frac{N}{n_d} \right]) \dots\dots\dots (2.2)$$

Where e is the electron charge, Z^*_D is the valence of metallic ions, Z is the valence of metallic atoms, E is the applied electric field, ρ is the resistivity of the normal lattice atoms, ρ_d is the partial resistivity due to scattering of charges by the atoms, N is the total volume concentrations of atom, n_d is the density of defects. The equation can be simplified into equation 2.3; because the electrons wind force is the dominant factor in the electromigration flux.

$$F_{em} = Z^*e\rho j \dots\dots\dots (2.3)$$

where Z^* represents the sum of the effective charge number of the electrostatic field force and wind force, ρ is the resistivity and j is the current density. This shows that electromigration is dependent on the current density. A high current density will result in voiding in the cathode side and cause an open failure which lead to a shorter lifetime. The flux of EM can be represented in equation 2.4, where J represents EM flux, D is the diffusivity, k is Boltzmann's constant, C is the concentrations and T is the absolute temperature. This shows that the flux is proportion to the force of EM and inverse proportion to the temperature.

$$J_{em} = \frac{CDF_{em}}{kT} \dots\dots\dots (2.4)$$

2.4 Effect of EM in Flip Chip Solder Interconnect

EM failure in solder was first observed in eutectic tin and lead (SnPb) solder through lattice diffusion [35]. It has a lifetime of a few hundred hours at 150°C under a current density of 8 kA/cm². EM causes the net atomic transport of solder atoms along the direction of electrons flow. Compared to on chip metallization Al or Cu where the current density for electromigration occurs at 1 MA/cm², EM in solder occurs at lower current density up to 10 kA/cm² [10, 36]. The reason for a more pronounced electromigration rate is explained by the lower melting point of Sn/Pb as compared to Cu, and fast diffusion path in solder [37, 38].

2.4.1 Voiding Effect

EM in solder is worsened by the unique geometry of interconnect line to bump configuration in flip chip interconnection. This results in current crowding which increases the current density at the solder joint corners. This increase can be one order of magnitude higher than the normal current density [39]. Under a higher electron wind force, it results in void nucleation near the current crowding region which has been reported in various literatures [39, 40]. Thus, the void grows and propagates through the solder, leading to open failure eventually. Figure 2.4 (a) shows the location of the void due to the current crowding effect, and Figure 2.4 (b) shows a simulated result identifying the location of highest current density. It was found that by adding a thick Cu under bump metallization (UBM) is able to reduce the current density from 11 kA/cm² to 7.5 kA/cm². Another alternative to reduce current crowding current density is to use a

thick Cu column [41, 42]. In on chip metallization, it was reported that the nucleation of void takes a longer incubation time, but it will propagate very fast during failure.

Figure 2.4. Effect of electromigration damages due to current crowding. (a) Void in the chip side where current crowding occurs, (b) Simulation shows the region of current crowding [39]

However in solder, EM is reported to have a long incubation time with slow resistance change. However once the void is nucleated, resistance will increase. After which the void will propagate towards the UBM and lead to failure [43]. Figure 2.5 shows the typical variation of voltage against time for the EM testing.

Figure 2.5. Resistance changes of a solder under electromigration stressing [44]

2.4.2 Phase Separation Effect

Another noticeable effect of solder EM is the phase separation in eutectic two-phase solder [35, 45]. This happens because the atomic diffusivity is different for the different phases/elements over a range of temperature. It was reported that in eutectic tin-lead Sn37Pb Wt. % based solder, Sn diffuses faster than Pb under 100°C, while Pb diffuses faster than Sn above 100°C [46, 47]. As a result under EM testing, Brandenburg and Yeh observed Pb migrates faster due to the electron wind force enhancing the phase separation as shown in Figure 2.6. This phase separation enhances the dissolution of the UBM in the chip/cathode end or the substrate. This results in the extensive formation of intermetallic compound (IMC) at one side [48], and leads to poor mechanical strength at the interface of the solder joints [49].

Figure 2.6. Cross sectional area of SnPb solder showing the effect of phase separation due to EM [35]

2.4.3 Impact of EM on the Mechanical Strength

IMC formation will influence the mechanical strength of the solder, and this can be affected by current stressing. Solid state interfacial reaction determines the type of IMC formation. Solid state interfacial reaction refers to the nucleation of new phase, and will occur when there is a chemical concentration gradient, appropriate thermodynamic and kinetic conditions. EM can influence the IMC formation at the anode or cathode side [50]. The enhancement or inhibition of IMC in either the anode or cathode side is dependent on the type of solders used. This effect is known as polarity effect [50, 51]. The enhancement of IMC is due to electron wind and chemical potential enhancing the IMC growth. Depending on the electron wind force direction, it can retard the IMC formation as well [52]. Figure 2.7 shows an example of polarity effect in solder where there is enhancement of IMC at the anode side after 120 h of stressing. The polarity effects of IMC will weaken the mechanical joint in the side that has the thicker IMC, and results in brittle joint [53-55].

Figure 2.7. Polarity effect in the solder. BEI micrographs of the Sn/Ni/Sn couple after reaction at 180°C with current density of 5000 A/cm² (a) for 24 h and (b) for 120 h [56]

CHAPTER 3: Experimental Techniques

The effect of aging on Au-Ge's electrical property and microstructure is studied in two parts. The first part involves bulk Au-Ge thin film, and the second part is on Au-Ge solder joint. In order to study the solder joint, a daisy chain test vehicle was fabricated. This set-up allows current to flow through the solder joint. When a higher current flow through the solder joint, the effect of electromigration on the solder joint can be analyzed. A brief description on the test sample, experimental set-up, experimental methodology and process methodology will be presented.

3.1 Procedures for Bulk Au-Ge thin film study

Bulk Au-12Ge Wt.% thin film of thickness 25 μm was obtained from William Materials. These samples were prepared by cutting them into an average size of 0.6 mm by length and 0.58 mm by width. The electrical resistances of the samples were measured by the four point probe method. The instruments used are Agilent 34401 multimeter and Keithley 2400 source meter. The set-up of the testing is shown in Figure 3.1. Current was supplied, and voltage measurement was taken with the voltage probes at a distance of 2.5 mm. Each sample was measured at ten different spots at a constant test length. A current sweep from -0.1 A to 0.1 A at a ramp rate of 0.01 A/s was used to measure the voltage. These samples were then aged in a furnace (Nabertherm) for up to 700 h at 300°C, and their resistances measured again. The electrical resistance is then converted into electrical resistivity, as shown in the next chapter.

Figure 3.1. Experiment set up for electrical resistivity measurement

The melting point of the solder was verified by Differential Scanning Calorimetry (DSC). The microstructure was studied by using Focused Ion Beam/Secondary Electron Microscopy (FIB/SEM). Further analysis such as Electron Backscatter Diffraction (EBSD) was used to determine the grain size changes after aging, and X-ray diffraction (XRD) was used in identifying the phases formed.

3.2 Electron Backscatter Diffraction Analysis (EBSD)

Electron backscatter diffraction (EBSD) is known as backscatter Kikuchi diffraction (BKD). It uses SEM microstructural-crystallographic technique to measure the crystallographic orientation. Normally, it is installed inside a FIB/SEM system. In EBSD, a stationary electron beam strikes a tilted crystalline sample and the diffracted electrons form a Kikuchi diffraction. This pattern shows the characteristic of the crystal structure and orientation of the sample region from which it was generated. It is able to index and identify the crystal orientation, grain size and grain boundary characterization.

EBSD has better resolution than XRD in determining the grain size. Hence, this technique was used to quantify the grain size of the *Au*.

3.3 Procedures for Au-Ge solder joint study

3.3.1 Design of test structure

The test structure consists of a test die ($6\text{ mm} \times 6\text{ mm}$) bonded onto a substrate die (8.1

Figure 3.2. Test layout (a) Test die (b) Test and substrate die pattern

$\text{mm} \times 7.8\text{ mm}$). The test structure follows a 28 I/O peripheral daisy chain design illustrated in Figure 3.2 (a), and an overall layout of the test structure is shown in Figure 3.2 (b).

This test structure was used to study the effect of aging and EM on the Au-Ge solder joint. The metallization scheme on the test die is summarized in Table 3.1. Test structure 1 was used in the aging study while test structure 2 was used in the electromigration (EM) study. The test structure is shown in Figure 3.3 (a). Au-Ge preform which measured 120 μm in diameter, and 100 μm in height is used as a solder bump to assemble the test die onto the substrate die as illustrated in Figure 3.3 (b).

Table 3.1. Metallization scheme on Test and Substrate die

Test Structure	Test Die	Substrate Die
1	<u>Metallization</u> 0.1 μm Ti, 5 μm Cu <u>Under bump metallization (UBM)</u> 5 μm Ni, 0.1 μm Au	<u>Metallization</u> 0.1 μm Ti, 1.5 μm Cu <u>Under bump metallization (UBM)</u> 3.5 - 4.0 μm Ni, 0.1 μm Au
2	<u>Metallization</u> 0.1 μm Ti, 1.5 μm Cu <u>Under bump metallization (UBM)</u> 3.5 - 4.0 μm Ni, 0.1 μm Au	<u>Metallization</u> 0.1 μm Ti and 1.5 μm Cu <u>Under bump metallization (UBM)</u> 3.5 - 4.0 μm Ni, 0.1 μm Au

Figure 3.3. Test structure (a) Metallization scheme (b) Layout of the daisy chain test structure

3.3.2 Fabrication overview

The fabrication of the test and substrate dies involved the use of stainless steel shadow mask which was attached onto the surface of the Silicon (Si). Physical vapor deposition (PVD) was used to deposit titanium (Ti) as an adhesion layer followed by copper (Cu) as the metallization onto the surface. The PVD method used was electronbeam deposition. Electroless Nickel Immersion Gold (ENIG) plating was carried out to create the UBM. The process flow is summarized in Figure 3.4. Prior to the plating, the surface of the Cu was cleaned using a commercial cleaning agent to remove organic impurity. Then the

Figure 3.4. Summary of the fabrication process flow

surface was etched for 10 sec in a commercial etchant that consists of sulphuric acid and copper sulphate to remove the Cu oxide. The process parameters used in ENIG fabrication is shown in Table 3.2. Electroless Nickel [El-Ni(P)] requires the use of pre-initiator solution to activate the surface with palladium, follows by electroless nickel plating. Lastly, it ended with immersion gold plating.

Table 3.2. Process Parameters of ENIG

Parameters	Preinitiator	El-Ni (P)	IG platting
PH at 25 °C	-	5.3	4.7
Temperature (°C)	43	88	82
Time (Minutes)	4	13.67	8
Deposition rate	-	16 microns/h	-

3.3.3 Bonding process

The bonding process starts by applying Indium tacflux NC 506 onto the solder pad, and followed by ball-dropping of Au-Ge preform. The first reflow process will be on the test die. The Au-Ge preform was placed on the test die, and subjected to reflow in an inert condition: 390°C for a dwell time of 1 min. The second reflow involve the use of flip chip bonder: Smart Equipment Technologies (SET) FC150. In the second bonding, the test die was aligned and bonded onto the substrate at a peak temperature of 390°C for a dwell time of 15 s. Due to the difference in the heating rate, two different bonding profiles was used in the bonding. The bonded samples were inspected by Shimadzu micro-focus X-ray system, and the sample used in the study has a void area less than 10% as shown in Figure 3.5.

Figure 3.5. X-ray image of bonded sample

3.3.4 Testing methodology

28 bumps daisy chain was adopted in this study. The test vehicle consists of a flip chip test die joined by Au-Ge solder onto a carrier (Die). The test vehicle will be connected electrically by wire bonding onto a dual in line package (DIP) as shown in Figure 3.6

The bonded test structure was thermally aged at 300°C for 500 h in an inert Argon environment, and the electrical resistance of a pair of daisy chain was measured by four

Figure 3.6. Schematic of a test vehicle in dual in line package

points method. In order to study the EM effect of the solder joint, the test vehicle was

placed into an EM equipment where high current density was supplied, and the temperature is at 300°C.

The microstructure of the solder joint bump was examined before and after aging under backscatter imaging mode (BEI) in JEOL JSM 6360A SEM. The IMC characterization was studied by Energy Dispersive X-ray (EDX), where the atomic.% of surface was analyzed. It was compared with the phase diagram to determine the actual phase. The thickness of the IMC was characterized by measuring a rectangular area through an imaging software call Fiji. After which, the length of the IMC was measured, and thickness is determined by the formula of $Thickness = \frac{Area}{Length}$.

CHAPTER 4: Effect of aging on Au-Ge

4.1 Characterization of Au-Ge

Characterization on the purchased Au-Ge solder was done to verify the samples' composition, morphology and melting temperature. This is to ensure the sample is of eutectic composition.

4.1.1 Morphology and EDX Analysis of Bulk Au-Ge

Figure 4.1 (a) shows the SEM top view of the Au-Ge surface, and Figure 4.1 (b) is the SEM tilted view. Ge is identified as the black color regions in both Figure 4.1 (a) and (b), while Au is identified by the white regions. This was verified by using point spot Energy Dispersive X-ray Spectroscopy (EDX). The morphology of the surface is rough with uneven topography as seen in Figure 4.1 (b).

The composition of the solder was verified in an area scan of 100 μm by 100 μm . The EDX analysis in Figure 4.2 shows the presence of two elements: Au and Ge. The approximate weight composition of the solder is 84% Au, and 16% Ge. This is close to eutectic composition of 88%Au12%Ge.

Figure 4.1. SEM images of bulk Au-Ge solder, (a) Top view of the solder, (b) Tilted view of the solder

Figure 4.2. EDX scan of Au-Ge solder, show Au and Ge only

4.1.2 DSC on Au-Ge

DSC testing was done to verify the melting point of the solder. It was heated from 30°C to 600°C, and cooled to 120°C. The heating and cooling rate is 10°C/min. Figure 4.3 illustrates the heating curve and cooling curve of Au-Ge solder. The red line represents the heating cycle which indicates heat has been absorbed, while the blue line is the cooling curve which suggests heat was given out. The melting point of the solder is indicated by a dip in the heating curve, which is 368°C. With reference to the Au-Ge phase diagram shown in Figure 2.2 [27], the melting point is close to the eutectic melting point of 361°C.

Figure 4.3. Heating and cooling curve of Au-Ge solder

4.2 Effect of Aging on Electrical Property of Au-Ge

4.2.1 Bulk Au-Ge

Figure 4.4 illustrates the electrical resistivity of the Au-Ge aged at different aging duration. The ex-situ resistivity was calculated by substituting the measured resistance

into equation 4.1, where ρ represents the resistivity; L represents the test length and A indicates the cross section area.

$$R = \frac{\rho \times L}{A} \dots\dots\dots (4.1)$$

In this plot, the resistivity of Au-Ge decreases with the aging duration. A steep drop in resistivity was observed in the first 100 hours, and the slope of the curve decreases after 200 hours. This implies the resistivity value is reaching its saturation.

The resistivity of a material is related to the conductivity formula, which is represented by equation 4.2.

$$\frac{1}{\rho} = \sigma = n e \mu_e \dots\dots\dots (4.2)$$

Where σ represents the conductivity, n is the number of free charged particles available in the material, e is the absolute magnitude of the electrical charge on an electron, and μ_e is the moving electron mobility. This equation illustrates that resistivity is inversely proportional to the parameters shown in the equation. This implies changes in the parameters will affect the resistivity. The biggest impact to the resistivity is the electron mobility.

Figure 4.4. Electrical resistivity values of bulk Au-Ge undergo aging at different duration

Electron mobility is influenced by the electrons scattering events, which can be due to crystal imperfections and vibrations of the atoms, leading to a reduction in electron mobility [57]. It is believed that the electron mobility in Au-Ge side may be affected by possible microstructure changes during aging. This may include an increase in grain size, which will lead to a decrease in grain boundaries. Various past studies in thin films have highlighted the effect of decrease in grain boundaries results in lower electrical resistivity [58-60]. A discussion in the subsequent section will correlate the effect of microstructure changes to the electrical resistivity of Au-Ge.

4.2.2 Au-Ge Solder Joint

An increase in resistance of the aged Au-Ge solder joint against the aging duration is shown in Figure 4.5. The plot shows that the resistance is increasing with the aging duration. The increase in electrical resistance may be contributed by the interfacial reaction of the solder with the UBM, which results in an increase in IMC thickness. Possible void formation in the solder may also contribute to the increase in resistance.

The result also suggests that the increase in resistance is not contributed by just the microstructure changes in the bulk solder. It is also determined by the interfacial changes that will lead to the increase. Analysis will be done in the subsequent sections to correlate the interfacial reactions to the electrical property.

Figure 4.5. Resistivity values of Au-Ge solder joint undergo aging at different duration

4.3 Characterization on Bulk Au-Ge

4.3.1 Microstructure of Bulk Au-Ge

Figure 4.6 (a-g) illustrates the microstructure of bulk Au-Ge. The black regions show the Ge phase, while the brighter regions indicate Au phase. The Ge phase is dispersed in the Au phase which illustrates two distinct phases in the Au-Ge at 0 h.

As the solder is aged, the Ge phase starts to coarsen. However, after 200 h of aging, further coarsening of Ge grains was not observed. Instead, the Ge phase seems to be clustering together as shown in Figure 4.6 (e-g). This growth shows a clear clustering of Ge regions after 300 h of aging.

After 700 h of aging, Au and Ge phases still remain as distinct phases. This is due to the low solubility of both phases in each other, and no IMC reaction has resulted between these two elements. This is expected from the phase diagram as shown in Figure 2.2. Figure 4.6 (b-d) depicts a noticeable change in the microstructure, which is observed to be the coarsening of Ge grains.

On the other hand, the growth of the Au grains cannot be clearly identified in the SEM. The details of the Au grain can be identified through EBSD, which will be elaborated in the subsequent section. The SEM images have illustrated that there is a microstructure change after thermal aging, and coarsening of Ge has been identified. These

microstructure changes are similar to that reported in literature, where the changes impact its mechanical property [19].

Figure 4.6. SEM images of bulk Au-Ge at (a) 0 h (b) 100 h (c) 200 h (d) 300 h (e) 400 h (f) 500 h and (g) 700 h

4.3.2 X-Ray Diffraction (XRD) on Bulk Au-Ge

The XRD results of the aged Au-Ge solder up to 500 h is shown in Figure 4.9. From the XRD result, only Au and Ge peaks are detected. This shows only that Au and Ge phases are present in the Au-Ge solder. The phase still remains as Au and Ge after aging, and no sign of any IMC formation is detected. This is within expectation as the phase

diagram describes the phases will remain as Au and Ge phases. This result confirms no formation of new phases, thus the electrical property will not be affected.

4.3.3 EBSD Analysis on Bulk Au-Ge

The EBSD pole diagram of the bulk Au-Ge from 0 to 700 h is shown in Figure 4.7 (a-h). The different color regions symbolize Au grains of different orientations. This analysis does not include Ge grains due to the limitation in the software's library. The color regions in the Au grains are randomly orientated. This suggests the Au phase in Au-Ge eutectic solder does not have any preferred orientation. It is observed that the Au phase still remains randomly orientated after aging.

Figure 4.7. XRD results of Au-Ge sample under aging for different durations

It is obvious to see that the Au grains in the EBSD pole diagrams are increasing with aging duration. The Au growth rate is quantified by obtaining the grain size from the EBSD analysis, and is plotted in Figure 4.8. The plot suggests the average Au grain size grew the most during the initial aging, followed by a slower growth, and eventually reaching saturation. The Au grain size increased from 1.65 μm at 100 h to 1.91 μm at 300 h, but grain growth saturated beyond 400 h.

Figure 4.8. EBSD images of Au-Ge at (a) 0 h (b) 100 h (c) 200 h (d) 300 h (e) 400 h (f) 500 h (g) 600 h and (h) 700 h

Figure 4.9. Average Au grain size of Au-Ge eutectic solder after aging for different durations

4.4 Microstructure of Aged Solder Joint

4.4.1 0 h solder joint

Figure 4.10 shows the cross-sectional BEI images of the Au-Ge solder at 0 h. The sample was bonded but voids can be observed in the bulk of the solder as shown in Figure 4.10 (a). These defects are believed to have occurred during the bonding of the die to the substrate. The morphology of the bulk solder bump joint at 0 h is dominated by Ge phase dispersed uniformly throughout the Au phase as seen in Figure 4.10 (a). A dark thin layer that has formed underneath is the intermetallic compound (IMC) as

highlighted in Figure 4.10 (b-c). This layer is believed to be rich in phosphorous (P) content. The El-Ni (P) layer is sandwiched between the Cu and IMC layer.

The thickness of the IMC formed at the chip and substrate side is different due to the thermal budget experienced by the chip side was larger than the substrate side during the assembly process. The IMC layer consists of both NiGe and Ni-rich Ge IMCs, which is usually attributed to be Ni_5Ge_3 (Ni at. % at 62.5 [4]) (unless specified the unit is in at. %) [19, 29, 61]. The IMC has mixed morphology, the Ni_5Ge_3 is flat and uniform but the NiGe looks more like big chunky type of IMC, which is similar to other IMCs reported in literatures [19, 29]. EDX analysis was carried out to verify the content of the IMC after the reflow as depicted in Figure 4.11 (a-d).

The quantitative EDX detected the NiGe to be in a range of 50-55% Ni-Ge, and Ni_5Ge_3 to be 61-72% Ni-Ge. The results are close to the elemental composition of the IMCs. The El-Ni (P) layer consists of 85-87% Ni and P content is 13-15%. However, the P-rich layer has 22-30% P. This P rich layer is close to the composition of Ni_3P phase, and it believed to have formed during reflow when the Ni is depleted to form the IMC. This causes the dark P-rich Ni to be left behind. This phenomenon is common in solder-reaction assisted crystallization of El-Ni (P) which occurs commonly in tin based solder, where Ni will transform to Ni_3P at temperature above 300°C [62, 63].

Figure 4.10. Cross sectional- BEI images of solder joint at 0 h. (a) zoom out view, (b) zoom in view at area 1, (c) zoom in view at area 2

Figure 4.11. EDX analysis of solder joint at 0 h. (a) NiGe IMC, (b) Ni₅Ge₃ IMC, (c) P rich layer (d) El-Ni (P) layer

4.4.2 100 h solder joint

After aging for 100 h, the Ge phase started to coarsen as shown in Figure 4.12 (a). This is consistent with what was observed in bulk solder in Figure 4.6. Another noticeable change is the growth of the IMC layer. It was observed that the Ni-rich Ge IMC grew thicker in both the chip and substrate side (Figure 4.12 (b-c)). On the other hand, NiGe IMC grew at a slower pace as less Ni_5Ge_3 transformed into NiGe.

A quantitative EDX analysis was carried out to verify the elements' atomic composition. The types of IMC remained the same (Appendix A.1). However, the El-Ni (P) layer shows an increase in the amount of P content to 28 at.%. It is observed that Ge which has a high affinity with Ni diffused through the IMC layer to react with Ni to form a new layer of IMC. This results in the depletion of Ni in the El-Ni (P) layer, thus the P content increased to 28 at.%. This mechanism is believed to be similar with what other literature have reported [29]. Similarly, the P content in the El-Ni (P) layer also increased at the substrate side. On the other hand, it also results in the decrease in El-Ni (P) layer thickness.

Figure 4.12. Cross sectional- BEI images of solder joint at 100 h. (a) zoom out view, (b) zoom in view at area 1, (c) zoom in view at area 2

4.4.3 300 h solder joint

After aging for 300 h, it is observed that the Ge phases clustered together. Furthermore, amount of Ge is observed to have decreased in the bulk solder. Figure 4.13 (a) shows that the Ge has reacted with Ni to form more IMC. It is observed that the IMC thickness in both the chip and substrate side increased. It is also observed that IMC partially grew into the Au phase on the chip side, and micro voids have formed in the Ei-Ni (P) layer.

A quantitative EDX analysis verified the elements' atomic composition (Appendix A.2). From the EDX results, the IMC at the chip side has been fully converted from Ni_5Ge_3 into NiGe . The growth of Ni_5Ge_3 into NiGe IMC is similar to other findings [64, 65]. This illustrates the transformation of Ni_5Ge_3 into NiGe after prolong aging, where more Ge reacted with Ni to form this IMC. However, the IMC at the chip side still remained as Ni_5Ge_3 , where the transformation into NiGe has not been completed. The amount of Ni in the Ei-Ni (P) still remained the same but there are traces of Cu detected in the bulk of the solder at the chip side. It is believed that this is due to the partial breakdown of the Ei-Ni (P) layer, which allows the Cu to diffuse into the Au side of the bulk solder.

Figure 4.13. Cross sectional- BEI images of solder joint at 300 h. (a) zoom out view, (b) zoom in view at area 1, (c) zoom in view at area 2

4.4.4 500 h of aging

The micrograph of the solder joint aged to 500 h is illustrated in Figure 4.14. After ageing for 500 h, it shows further IMC growth as well as voids in the bulk of the solder and at the interface. Furthermore, the thickness of the Ei-Ni (P) layer decreased, and this illustrates the growth of the IMC.

A quantitative EDX analysis reveals that the IMC at both chip and substrate side had been converted into NiGe IMC (Appendix A.3). The EDX analysis also detected that Cu trace amount in the bulk of the solder at the chip side; highlighting the possibility of breakdown of the diffusion barrier at the chip side. Moreover, it was found that the P content in the Ei-Ni (P) increased to 41 % at both the chip and substrate side. This shows that more nickel had reacted with the Ge to form the IMC.

Figure 4.14. Cross sectional- BEI images of solder joint at 500 h. (a) zoom out view, (b) zoom in view at area 1, (c) zoom in view at area 2

4.5 Discussion

4.5.1 Effect of aging on the bulk solder

In this study, it is observed that the bulk Au-Ge's electrical property will not be degraded after aging at 300°C for 700 h. The decrease in electrical resistivity is contributed by the microstructural changes. It is confirmed that both Au and Ge's grain sizes grew during thermal aging. However, it is believed that Au, which is the more conductive element, contributes significantly to the decrease in electrical resistivity. The grain growth of Au causes the grain boundary to decrease, which results in less electron scattering. Thus, this enhances the electron mobility, which leads to a lower resistivity of the solder.

4.5.2 Effect of aging on solder joint

The increase in resistance of the solder joint is observed to increase with aging. This result is different from that of the bulk Au-Ge where a drop in resistance was observed. This suggests that the electrical resistance in the solder joint is not dependent solely on the microstructure of the bulk solder. The solder joint's microstructure analysis shows the growth of the IMC throughout the aging. The increase in electrical resistance is believed to be dependent on the solder's interface area. One possible reason will be the growth of the IMC layer. It has been reported by other researchers that NiGe IMC has a resistivity of 17–24 $\mu\Omega\cdot\text{cm}$ [66, 67], while Ni_5Ge_3 has a resistivity value of 132 $\mu\Omega\cdot\text{cm}$ [68]. Both resistivity values of the IMCs are higher than Au-Ge resistivity value of 15.4 $\mu\Omega\cdot\text{cm}$. Hence, an increase in the IMC thickness increases the electrical resistance. On

the other hand, the increase in electrical resistance may be contributed by the micro voids found in the E1-Ni (P) layer too. This voiding is caused by the depletion of the Ni to form the IMC, which results in the formation of Kirkendall voids. On the other hand, more cracks can be seen at the IMC interface of the solder after 300 h of aging. This crack was likely created during the polishing stage. This suggests that the bonding at the interface is getting brittle, and may compromise the joint strength.

The IMC growth's schematic is illustrated in Figure 4.15 (a-d). The initial thickness of the Ni_5Ge_3 is different on the chip and substrate side. After 100 h of aging, the Ni_5Ge_3 IMC increases. After 300 h of aging, the IMC at the chip side was fully converted into NiGe IMC. It was found that Cu started to diffuse into the bulk of the solder after 300 h of aging.

Figure 4.15. Schematic of the IMC growth (a) 0 h, (b) 100 h, (c) 300 h and (d) 500 h

Furthermore at 500 h, there is further degradation in the nickel barrier as more voids is observed and higher amount of P is detected in the Ni layer. This implies the nickel barrier may not be an effective barrier for high temperature applications at long durations. The main driving force in the formation of the IMC is believed to be the diffusion of Ge through the IMC layer to react with Ni to form newer IMC layer, which makes it unstable over time.

The results of the aging is all been summarized in Table 4.1.

Table 4.1. Summary of the changes observed during the aging

Aging durations(h)	Observations seen in the SEM
0	<ul style="list-style-type: none"> ▪ Observed different IMC layers at the interface
100	<ul style="list-style-type: none"> ▪ Ge coarsening ▪ Growth of Ni_5Ge_3 IMC at substrate and chip side ▪ Change in the composition in El-Ni diffusion barrier
300	<ul style="list-style-type: none"> ▪ Ge clustering ▪ Growth of Ni_5Ge_3 IMC at substrate side ▪ Transformation of Ni_5Ge_3 IMC to NiGe at the chip side ▪ Observed Cu trace in the bulk solder ▪ Growth of micro voids in the El-Ni barrier
500	<ul style="list-style-type: none"> ▪ Growth of NiGe IMC at substrate and chip side ▪ Thickness of El-Ni layer decrease ▪ More micovoids can be observed in El-Ni layer

The reliability of the high temperature solder can be improved by using other barrier options such as TiW/Au or W diffusion layers. This barrier option was used for Au-Ge solders in other high temperature applications [29, 69], and proven to be robust.

This study concludes that Au-Ge solder is a potential candidate for off chip metallization for ruggedized electronics. Firstly, the study shows that the bulk electrical resistivity decreases after aging. Secondly, the electrical resistance in the Au-Ge solder joint increased after aging. This increase is contributed by the growth of the Ni_5Ge_3 and NiGe IMCs, and micro voids in the E1-Ni (P) layer. This microstructural change not only increases the resistance, but may negatively impact the solder joint strength. Thus, the reliability of using Au-Ge for solder bump in high temperature application strongly depends on the choice of the barrier. This can be improved by using a better barrier which reduces the formation of IMC.

CHAPTER 5: Effect of EM on Au-Ge solder's joint

5.1 Electrical Data of EM

The daisy chain test structure was tested with three difference current densities, and the plot of resistance vs. stressing time is shown in Figure 5.1 (a). The plot suggests two trends. The first trend describes a gradual increase in resistance and eventually leads to a jump in resistance, which results in an open failure. It is noted that the first trend is associate with a high stressing current density that is above 5000 A/cm^2 .

The second trend describes a gradual increase in resistance over the stressing time of

Figure 5.1. (a) Plot of Resistance vs. stressing time, (b) Zoom in view of 1507 A/cm^2 stressing

500 h. However at some point of the stressing, the resistance experienced a small jump. The zoom in view of the plot is illustrated in Figure 5.1 (b), but the increase is slow and does not lead to any open circuit failure. The current density used is lower as compared to trend one. The increase in resistance may be contributed by the aging effect which leads to the growth of IMC, and also possible microstructure changes due to electromigration (EM)

5.2 X-Ray Imaging

5.2.1 Failed sample

X-Ray imaging was used to identify any void formation during the stressing process. Figure 5.2 and Figure 5.3 show the X-Ray images of the stressed solders. In Figure 5.2, the solders were stressed under 6407 A/cm^2 , while in Figure 5.3 the solders were stressed under 9799 A/cm^2 . Each set of imaging was done at the same magnification. It is observed that pre-existing void present in the solder, illustrated by the white region in the solder. This pre-existing void can be due to the bonding process. However, after stressing, the void grew in size. It is believed that the void grew and propagated through the solder joint. As a result, current was unable to pass through the solder which resulted in an open failure. A further discussion in the subsequent section will explain the possible contribution to the voiding.

Figure 5.2. X-ray images of test structure stressed at 6407 A/cm^2 (a) Before Stressing (b) After Stressing

Figure 5.3. X-ray images of test structure stressed at 9799 A/cm^2 (a) Before Stressing (b) After Stressing

5.2.2 Unfailed sample

Figure 5.4 depicts the solder stressed under 1507 A/cm^2 . It is observed that there are no pre-existing voids. After 500 h of stressing, no growth of void was observed. This verifies the sample did not fail, and the sample survived under 500 h of stressing.

Figure 5.4. X-ray imaging of test structure stressed at 1507 A/cm^2 (a) Before Stressing (b) After Stressing

5.3 Microstructure of the stressed solder

5.3.1 Failed sample

Figure 5.5 shows the BEI image of the sample that failed under 6407 A/cm^2 . A big void is observed in solder 1, while no void is observed in solder 2. The voids shown in Figure 5.5 (a) are inter-link towards the solder joint which may be the cause of the open failure.

More IMC growth is observed at the anode side of solder 1 as compared to anode side of solder 2 shown in Figure 5.5 (b). To study the effect of EM on IMC growth, comparison is done between the interface of the top side of stressed solder (anode and cathode), and top side of an aged solder (control solder) that never went through current stressing shown in Figure 5.6 (a-c).

Figure 5.5. SEM Image of Stress Solder (a) Solder 1 (b) Solder 2

Figure 5.6. Top side of the stressed solder at 6407 A/cm² (a) Anode (b) Cathode (c) Control

It is observed that the type of IMC growth is the same, where NiGe is formed instead of Ni₅Ge₃. The comparison of the IMC thickness is also done on the bottom side of the stressed solder (anode and cathode) and control solder, shown in Figure 5.7.

Figure 5.7. Bottom side of the stressed solder at 6407 A/cm^2 (a) Cathode (b) Anode (c) Control

The IMC thickness of the solder at the top side is shown in Figure 5.8 (a). It is observed that highest IMC growth is located at the anode direction, followed by the control solder, and lastly the cathode direction. A similar observation is observed for the bottom side of the chip shown in Figure 5.8 (b). Both results suggest that the anode side of the chip will have the highest IMC growth while the IMC growth at the cathode side is the lowest.

Figure 5.8. IMC thickness of the solders (a) Top side (b) Bottom side

5.3.2 Unfailed sample

In the unfailed sample, no void was observed in the X-Ray images. Hence, the emphasis will be on the IMC interface. Figure 5.9 shows BEI images of the top side of the solder for three different samples, mainly the cathode, anode and control solder. It is observed that the IMC remain as NiGe, but the amount of P in the El-Ni (P) layer is different. This may be due to the amount of IMC reaction that varies across the solder. It is also observed that there are micro voids in the El-Ni (P) layer which is similar to voids formed in El-Ni (P) layer after thermal aging as discussed in the previous chapter.

Figure 5.9. Top side of the stressed solder at 1507 A/cm² (a) Anode (b) Cathode (c) Control

The BEI image of the bottom side of the chip at three different locations is shown in Figure 5.10. It is also observed the type of IMC remained the same.

Figure 5.10. Bottom side of the stressed solder at 1507 A/cm² (a) Cathode (b) Anode (c) Control

Figure 5.11 (a-b) illustrates the thickness of the IMC at the top side and bottom side. It is observed that IMC grew the most in the anode side of the solder, followed by the aged solder and cathode side. This observation is consistent with the observation in failed sample. It is believed that this effect is due to the polarity growth of the IMC as discussed in literatures.

Figure 5.11. IMC thickness of the solders (a) Top side (b) Bottom side

5.4 Discussion

In this electromigration study, it is observed that EM will induce two effects. The first effect is growth of voids commonly described by the literatures as pancake void. This growth of void will result in open circuit failure. It is well illustrated by the X-ray images that the voids grew during stressing. The second effect is the polarity growth of the IMC which results in enhanced IMC formations at the anode side while retarding the IMC growth at the cathode side.

The void growth may be caused by a mixture of reasons. Firstly, diffusion of Ge in the bulk solder into the Ni layer to form the IMC. This may result in vacancy in the solder which causes void growth. Secondly, a higher current density will result in joule heating which may induce additional heat onto the solder. Joule heating may be enhanced during the stressing due to growth of void, which induce further joule heating [70]. Lastly, pre-

existing void in the solder may also shorten the lifetime due to higher current density [71]. This pre-existing void may act as a site for the void growth to happen.

In the polarity growth of IMC, it is observed that the IMC is thicker at the anode side as compared to the cathode, while the IMC at the control solder side is thicker than the cathode side. It is believed that the electron wind force enhances the IMC formation at the anode side and also retards the IMC formation at the cathode side as illustrated in Figure 5.12. It is believed that the electron wind force is in the same direction as the Ge's concentration gradient which promotes the growth of IMC at the anode side. On the other hand at the cathode side, the electron wind force is against the direction of the Ge's concentration gradient, which results in less Ge diffusing to the cathode side to form the IMC.

Figure 5.12. Schematic of the effect of EM on the growth of IMC

Beside this, ionic diffusion may be a source that can influence the diffusion of Ge. Literature shows that Ge diffuses to the cathode side during the EM in $\text{Ge}_2\text{Sb}_2\text{Te}_5$ [72]. This is due to ionization of Ge in molten state under EM which changes the Ge to become a cation, which will diffuse to cathode side. However, Au-Ge is in crystalline state will not be influenced by ionic diffusion as it does not get ionized. It is reported by other EM literature that in crystalline form of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ [73], the Ge diffusion is contributed by hole wind force. This is due to the material is p-doped semiconductor, where mode of conduction is by holes. While in here, Au-Ge is a metal alloy which means that the mode of conduction is by electrons. This means that there will be electron wind force impacting the atoms which will result in the diffusion of the atoms in Au-Ge.

This study concludes that EM will take place in Au-Ge solder. Void growth accelerated by EM will result in failure in a state which will be a reliability issue in ruggedized electronics, while polarity growth of IMC will result in different IMC growth rate.

CHAPTER 6: CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusion

The project started out with the interest in evaluating the reliability of ruggedized electronics. It is important to understand the reliability physics as it can result in a robust system. Operating under a high temperature of 300°C may often result in IMC growth which may affect the property of the solder. Hence, understanding the interfacial reaction of the IMC is important in designing a robust system. Moreover, electrical driven failures like electromigration in high temperature solder may be a potential issue as minimization continues, where higher current density can be expected in solder joints.

The electrical resistivity of the bulk Au-Ge under aging has been evaluated. The results conclude that the electrical resistivity of Au-Ge will decrease after aging, and stabilize to a lower value. Au grain growth during aging will impact on the electrical property. The primary reason attributed to the decrease in electrical resistivity is the grain growth in Au, which results in less grain boundaries and thus less electron scattering.

The aging effect on the electrical resistance of the Au-Ge solder joint has also been studied. After aging, the electrical resistance in Au-Ge solders joint increases. This is attributed by the IMC growth at the interfacial and void growth in the Ei-Ni (P) layer. This shows the effect of interfacial reaction contributes more significantly to electrical resistance than the microstructure changes in the bulk solder. Moreover, Ei-Ni (P) may

not be a suitable barrier for high temperature long term application as it may suffer from a breakdown in the Ni(P) layer due to the reaction with Ge to form IMC. Other potential barrier system such as TiW/Au or W diffusion layers should be considered.

Lastly, the effect of EM on Au-Ge had been investigated. In the study, it shows that EM results in two effects, which are void growth and polarity growth of the IMC. In the void growth effect, it causes an open failure. While in the polarity growth of the IMC, it enhances the growth of IMC at the anode side, while retarding the growth of IMC at the cathode side. This may weaken the solder's mechanical property. The main driving force of EM in Au-Ge is the enhancement of Ge diffusion due to the electron wind force. To further improve its EM property, other type of barrier system can be considered which help to reduce the IMC formation.

Based on the present requirement, the current used in each bump is 0.2 A. This current limit was tested in the EM test and translates to a current density of 1507 A/cm^2 . It shows that the bump is able to survive for 500 h of stressing, but EM effect can be observed.

6.2 Future works

The objectives of the thesis are to study the possible effects of aging and EM on the Au-Ge solder. The mechanism on IMC formation under the effect of aging is understood. However, study on the kinetics on IMC formations under the effect of aging is not well investigated. Furthermore, in EM the polarity growth of the IMC

formation is not well quantified due to the limitations in our current test structure. The test structure used does not prevent joule heating which might affect the IMC formations.

6.2.1 Kinetics and polarity growth interfacial study of IMC formation

To further quantify the kinetics and polarity growth of the IMC formations in Au-Ge, a better test structure is proposed. This test structure is used in other literature [74] to study the interfacial reaction of Sn. This test structure is illustrated in Figure 6.1 and is used to study Sn-3.5Ag solder joints with Ni and Ni-P metallizations. This test structure prevents joule heating effect, and allows a better study in interfacial reaction as the joint dimensions are bigger which allow better polishing to be done. Thus, it will prevent any removal of materials away from the solder.

Figure 6.1. Schematic of the test structure to study the interfacial reaction of IMC

Aging and EM study can be done at different temperature to study the kinetics of IMC formations. The purposed temperature for study can be 100°C, 200°C and 300°C.

6.2.2 Mechanical Testing of the Au-Ge under EM

It is reported that the polarity growth of IMC formation may result in decreasing mechanical strength. Thus, mechanical testing can be carried out to observe the effect of EM on the joint's strength. The mechanical testing can be in the form of shear test or tensile test. Using the daisy chain test structure allow shear test to be carried out, while tensile testing is done by using the proposed test structure stated in the earlier section. It is believed that the polarity growth of IMC will result in brittle fracture at the anode side which has a higher amount of IMC.

6.2.3 Statistical lifetime study

A model on EM lifetime on Au-Ge can be built by studying the lifetime at different current density and temperature. This model allows the user to extrapolate the time to failure. This is critical as it allows the designer to design in the current density and dimensions to be used in Au-Ge solders to prevent any form of EM.

6.2.4 Different type of UBM

It is reported that TiW/Au or W is a better diffusion barrier. Another study can be done based on the same experimental conditions used in the thesis to verify whether such barrier system will result in better reliability. Aging study at 300°C and EM study can be done to verify its reliability.

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APPENDIX

A1 EDX analysis of solder joint undergo aging

Figure A.1. EDX analysis of solder joint at 100 h. (a) NiGe IMC, (b) Ni₅Ge₃ IMC, (c) El-Ni (P) layer

Figure A.2. EDX analysis of solder joint at 300 h. (a) NiGe IMC at chip side, (b) Ni₅Ge₃ at substrate side IMC, (c) El-Ni (P) layer and (d) Cu traces in the bulk solder

Figure A.3. EDX analysis of solder joint at 500 h. (a) NiGe IMC at chip and substrate, (b) El-Ni (P) layer

A2 List of Publications

- (1) **Lau, FL**, I Made, R, Putra, WN, Lim, JZ, Nachiappan, VC, Aw, JL & Gan, CL 2013, 'Electrical behavior of Au–Ge eutectic solder under aging for solder bump application in high temperature Electronics', *Microelectronics Reliability*, vol. 53, no. 9–11, pp. 1581-6.
- (2) **Lau, FL**, I. M. Riko, W. N. Putra, E. P. J. Rong, Z. Lim Jun, D. Lim Ju, C. Wong Chee, Z. Chen, V. C. Nachiappan, and G. C. Lip, "Study of electrical property of Au-Ge eutectic solder alloys for high temperature electronics," in *Electronics Packaging Technology Conference (EPTC), 2012 IEEE 14th*, 2012, pp. 30-33.