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Power Management ICs for portable device

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Abstract

Prolonging the running time of Portable devices motivate us continuously to improve the efficiency and power consumption of power management integrated circuits (ICs) in portable devices due to the little progress in the scaling of battery voltage.

In order to extend the working life, the energy harvesting technology is equipped in the device as a backup source or the main source for the portable device and wireless sensor, hence, the design challenge is that power management ICs can operate with extreme low power and low voltage. Therefore, an ultra-low voltage reference circuit with ultra-low power consumption of 180nW is proposed in this research work.

Portable device usually switches alternately between high load and low load. However, the control method is optimized to make the DC-DC converter so that it operates in high conversion efficiency particularly only in one load or another. As a result, Hybrid control method is proposed to maintain the high conversion efficiency of converter for a wide load range. Due to the fact that mobile portable device operate most of their time in low load condition, a novel Dead time and Reverse inductor current controller are developed to improve the efficiency of DC-DC converter dedicated for low load conditions.

Overall, the design objective focus on the improvement of efficiency for power management ICs so as to meet the requirement imposed by the source and load.

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Overall, the design objective focus on the improvement of efficiency for power management ICs so as to meet the requirement imposed by the source and load.

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Dedicated to my family...

Chapter 1

Introduction

1.1 Motivation

Nowadays, portable device has played a significant or even irreplaceable role during people's daily life [2, 3]. Those devices, such as the smartphones and tablet PC, have taken up majority of consumer electronic markets. Portable device is usually powered by batteries. Consequently, the running time of devices are mostly affected by the restriction of capacity of battery catering to the size of portable devices. However, longer running time is an important factor which can impact influence on customer decision about the bias for the consumer product. Therefore, maximizing the running time of device is a key goal to continually motivate us to design ultra-low power and high power conversion efficiency circuitry.

Batteries have a self-discharge characteristics that cell voltage is not flat over whole capacity (the cell voltage of Li-Ion batteries may varies from the 4.2 V to 2.8V). However a load circuitry must have an optimum operating voltage in which the circuitry consumes minimum operating power. As a result, the batteries do not directly connect to the load. Then a voltage regulation is built in the device as an interface between batteries and load to make the load operating voltage independent of batteries cell voltage thus maintaining the minimum power consumption, substantially prolonging the running time of device.

Consequently, voltage regulation circuitry must be designed with as low as possible power consumption and high power conversion efficiency since battery with a limited capacity in portable device. Besides that, a optimize power management scheme must be used to maintain power conversion efficiency for wide load range of portable device, especially in the light load of portable device which operate in idle mode.

In addition, in order to extend running time of portable device, hybrid source is also proposed to power the portable device. Recently, the energy harvested from ambient as a supplementary source is supplied to device which has become popular. Although energy harvesting technique increase the complexity of voltage regulation circuit, the hybrid source break the limit capacity of batteries, so

may significantly extend running time of device. Since the potential of energy harvesting, the interest on exploiting more effective and efficiency energy harvesting motive us to design state-of-art power management circuit about the energy harvesting application.

1.2 Goals and Contributions

The objective of this research is to explore power management Integrated Circuits (ICs), hence design and implement high efficiency and high-performance power management ICs applied in the portable device and Energy Harvesting system. The target of power management ICs is mainly DC-DC converter. Therefore, the goals of the research are summarized below:

- To discuss and analyze the power management ICs
- To learn the operating principle of DC-DC converter
- Study up-to-date topology to design a high efficiency DC-DC converter for portable device.
- Investigate the DC-DC converter applied in the Energy Harvesting system, and develop power management ICs to meet the Energy Harvesting application specification.

1.3 Organization of thesis

Chapter 2 introduced the fundamental of power management ICs and briefly review the conventional design method of Bandgap circuit and highlight design challenge of implementing high efficiency DC-DC converter at wide load range.

In the Chapter 3, a novel CMOS 65nm ultra-low voltage reference circuit of 435mV yielding a temperature coefficient of $30ppm/^{\circ}c$ and an ultra-low power consumption of 180nW is proposed and implemented. Furthermore, it yields a line regulation of with a supply voltage ranging from 0.6V to 1.2V. This is only possible with the implementation of an improved folded cascode current mirror op-amp.

Chapter 4 presented a twin frequency control buck DC-DC converter implemented by a CMOS 0.18μ process. The proposed buck converter regulate input voltage $2.0 \sim 3.0V$ from battery to provide output 1.2V at wide load range $10 \sim 50mA$. Hence, the twin cycle method was introduced about regulation of buck converter. Lastly, measurement of buck converter was discussed to verify the functionality of twin cycle control buck converter.

Finally, Chapter 5 summarise the works and gives the conclusion of the thesis, as a result, make the recommendation for the future work of the research.

Chapter 2

Fundamental of Power management ICs

This chapter discuss the Sources, Bandgap circuit and DC-DC converter imposed on the Power management ICs. The characteristics of Sources and the working principle of Bandgap circuit and DC-DC converter are introduced. Furthermore, the design equation and challenge for DC-DC converter are presented as well.

2.1 Introduction

Power management ICs is integrated in many state-of-the-art modern mobile applications such as portable device, biomedical implants sensors and stationary

wireless sensor and etc. It is seen as the interface between batteries and highly integrated load circuits system.

Power management ICs manage power requirement of the system, which normally include batteries management, voltage regulation and charging function. Therefore, the power consumption of system can be maintained at minimum level to utilize the capacity of battery leading to a much longer running and operating time of system. The market of those applications has grown tremendously in recent years which drive us to design high performance and high efficiency power management ICs. Aforementioned system is composited of 3 elements which are Source, Power Management and Load.

The composition of a normal operating system is illustrated in Figure 2.1:

FIGURE 2.1: Composition of power management system [4].

The characteristics of the source will significantly impact the design of power

management circuitry, and this will be discussed in next section. Power management circuitry basically include the following component below:

- Reference blocks which either generate a fixed voltage, current or time independent of process, supply voltage and temperature (PVT).
- Regulator blocks which either regulate voltage, current or time against load, supply and transient variations.
- Charger block which is used in case if that battery can be re-chargeable.
- Power Mixers which manage and mix power from sources when the hybrid source is applied.
- Supporting blocks which is used to ensure system reliability and functionality as well as providing protection.

This research focus on the reference block and DC-DC converter among the Regulator blocks. The working principles of both will be introduced in greater details.

2.2 Power sources

Power of the portable device is mainly provided from either batteries, ambient or both. Batteries is recharged either from external source or from energy harvested

from the ambient environment. If the energy of source is solely from ambient, an Ultra or Super capacitor is needed which has similar properties and functions with the battery.

2.2.1 Battery

Lithium Ion (Li-Ion) batteries is a dominant source of power in the market place to power the portable device due to lack of memory effect and much lower self-discharge compared to other types of batteries. The characteristic of discharge curve is illustrated in Figure 2.2:

FIGURE 2.2: Li-ion battery discharge curve [4].

Therefore, the following power manager must handle the input voltage varying from $4.2 \sim 2.8\text{V}$. However, the cell voltage of the Li-Ion batteries can be seen as a constant value at some times.

2.2.2 Ambient Source

The history of energy harvested from ambient dates back to the windmill and waterwheel. For centuries, human beings have taken advantage of renewable energy to drive mechanical and electrical loads. Those systems are called the large-scale energy harvesting systems. Therefore, humans also explored and implemented energy harvesting technique used in the recent microelectronic systems that consumes micro-power or even lower.

The power density of the ambient source is the key factor that design must be considered. According to the research, power densities of some harvesting technologies are illustrated in Table 2.1:

Methods	Power Density W/cm^{-2}
Solar cells	15 m
Piezoelectric	330μ
Vibration	116μ
Thermo-electric	40μ
Acoustic noise	960n

TABLE 2.1: Power densities of energy harvesting technologies [1].

The power density determine how much the level of power consumption for the subsequent power management ICs. Besides power density, the model of ambient source also must be investigated.

Looking at two common energy harvesting which are piezoelectric harvesting and solar energy harvesting.

FIGURE 2.3: Piezoelectric energy harvesting model [1].

A vibrating piezoelectric device has a capacitive impedance and may be driven by mechanical vibrations of varying amplitude and frequency. The source model is seen as an AC current source shown in Figure 2.3, consequently, an AC - DC rectifier is inserted before regulating voltage supplied to electric circuit.

FIGURE 2.4: Solar energy harvesting model [1].

For the solar energy harvesting illustrated in Figure 2.4 , the source is seen as DC voltage source. Therefore, the source can be directly regulated and supply to the electric circuit.

2.3 Voltage Reference

The voltage reference is one of the key building blocks in integrated circuit design, in which a fixed DC voltage of known amplitude V_{REF} that is independent of the power supply voltage, temperature, and process variation (PVT) is provided. A voltage reference is often used to compare input or output voltages to a certain level.

Bandgap circuit has been mainly taken to realize the voltage reference. There are three main figures of merit for voltage reference are: the output reference voltage dependence with temperature, voltage supply and the power consumption.

The concept of Bandgap circuit is based on compensating the voltage of a forward-biased diode (or base-emitter junction) which has a negative temperature coefficient with a voltage proportional to absolute temperature (PTAT). As illustrated in Figure 2.5, PTAT voltage is developed by amplifying the voltage difference of two forward-biased base-emitter (or diode) junction.

Accordingly, a conventional topology of Bandgap circuit is developed and shown in Figure 2.6. And the V_{REF} is:

$$V_{REF} = \frac{R_3}{R_2} \Delta V_{EB} + \frac{R_3}{R_{1A}} V_{EB2} \quad (2.1)$$

FIGURE 2.5: Voltage mode bandgap reference.

FIGURE 2.6: Conventional bandgap circuit.

In which, PTAT is:

$$V_{R2} = \Delta V_{EB} = V_{EB2} - V_{EB1} \quad (2.2)$$

$$\Delta V_{EB} = \frac{kT}{q} \ln \left[\left(\frac{I_{Q2}}{I_{Q1}} \right) \left(\frac{A_1}{A_2} \right) \right] \quad (2.3)$$

A is cross section area of junction. For the BJT transistor with equal collector current, $I_{Q1} = I_{Q2}$ and $A_1 = NA_2$. So:

$$\Delta V_{EB} = \frac{kT}{q} \ln(N) \quad (2.4)$$

ΔV_{EB} proportional to absolute temperature (PTAT) component has been formed.

Meanwhile, negative temperature coefficient called complementary to absolute temperature (CTAT) is been formed by V_{EB2} ($\frac{\partial(V_{BE})}{\partial T} = \frac{V_{be4}-V_{go}-3V_t}{T} \approx -2mV/^{\circ}C$).

R_{1A} and R_{1B} have same resistance, design R_1 to R_3 value properly to minimize the temperature coefficient (TCF) of V_{REF} as much as possible. Normally, the TCF of V_{REF} less than $10 \text{ ppm}/^{\circ}C$ is acceptable.

As seen in the Figure 2.6, there is an amplifier in the Bandgap circuit which is used to provide the voltage independent against supply voltage variation. The working principle is that, if V_{DD} increases leading to V_{SG} of the PMOS increasing, the drain current I_1 and I_2 would also increase. Consequently, both positive and negative inputs of amplifier increases. Because of voltage in positive input increasing larger than that in negative input, this differential will be amplified and cause the output of amplifier which is gate voltage of PMOS would also increase accordingly. Finally, it leads to V_{SG} of the 2 PMOS (M1 and M2) decreased to compensate the V_{DD} variation. The built in amplifier effectively improve the

power supply rejection ratio (PSRR) of Bandgap circuit.

2.4 Voltage Regulator

As mentioned before, the regulator circuit is the interface between the Source and Load. Regulator circuit either regulate voltage, current or time. This research focus on the voltage regulation because of the research about the portable and Energy Harvesting application.

Linear Regulator and Switching-mode Regulator are two of most known categories of voltage regulators. The fundamental system of two regulator are shown in Figure 2.7 and Figure 2.8:

FIGURE 2.7: Linear Regulator.

As seen in Figures, there are power transistors integrated in both Regulators. In Linear Regulators, power transistors are seen as a dependent current source with relatively high voltage drops at high currents, hence consumes numerous

FIGURE 2.8: Switching Regulator.

power which lead to low efficiency of system. Other than that, the size of Linear Regulators are heavy and large. Nonetheless, the merit of Linear Regulators is that they exhibit high noise immunity and is suitable for audio applications.

While in Switching-mode Regulator, power transistors are operated as switches. Either when transistors are turned on, the voltage drop across transistors is very low even if it conduct high current, or when transistors are turned off, it conducts almost zero current when the voltage drop is high, the conduction power loss of the transistors is very low. Therefore, the transistor as a switch inherently dissipate much less power than transistors operated as dependent current sources which leads to high efficiency in switching-mode converters, usually above 80 ~ 90%. However, switching losses increase proportionally to switching frequency, transistors switched at very high frequency that will weaken the efficiency in Switch-mode Regulator.

The comparison of two categories of voltage regulator are summarized as shown in Table 2.2

Linear Regulator	Switch-mode Regulator
Limited Output Range ($V_{OUT} < V_{IN}$)	Flexible ($V_{OUT} \leq$ or $\geq V_{IN}$)
Low cost (PCB,Si,etc)	Expensive(PCB,Si,etc)
Low Noise	Switching Noise
Fast	Slow
Low efficiency ($\eta \leq V_{OUT}/V_{IN}$)	High efficiency ($\eta \approx 80\% \sim 90\%$)
Low noise Apps	High efficiency Apps

TABLE 2.2: Comparison of voltage regulators

The common Linear Regulator is Low-dropout regulator (LDO), while the DC-DC converter is the one of most represented Switching-mode Regulator. The output voltage of the Linear Regulator is smaller than input voltage that is necessary for some applications such as audio application. Those applications requires an output voltage just slightly in below the input voltage. Therefore, LDO is connected right after DC-DC converter to eliminate the ripples at the output voltage of DC-DC converter. In addition, the power MOSFETs in the Linear Regulator is on continuously while MOSFETs in the Switching-mode Regulator is on-off alternatively. Lastly, the conversion voltage difference between input and output voltage in the Linear Regulator is small due to power efficiency degraded by the high voltage drop. However, the Switching-mode Regulator can converter a high voltage drop and achieve a reasonable power efficiency at the same time.

The focus of this research is on the DC-DC converter. As a result, the details about the topology and working principle of DC- DC converter will be discussed

in next section.

2.5 Introduction of DC-DC converter

The prime functions of a DC-DC converter is to convert a DC input voltage to the targeted DC output voltage within a tolerance range, and also maintaining the regulation on the output voltage against perturbations of input voltage, load current as well as the temperature. Finally, an unregulated dc input voltage is regulated through DC-DC converter to provide a dc output voltage with the ripple voltage below specific level.

Figure 2.8 depicted the common components of a DC-DC converter circuit. It composes of inductor, filter capacitor, MOSFETs as a controllable power switch and load. The diode and BJT sometimes are also used as power switches. However, the MOSFETs are most commonly used due to their high speed and with more flexible control scheme. In the portable device, an unregulated battery source voltage V_{IN} is converted to the desired output voltage V_{OUT} . The power switches are worked as chopping the input voltage V_{IN} to produce a square wave with an average voltage equal to the desired output voltage. Theoretically, 100% efficiency is approachable for the DC-DC converter if there are ideal components. In practice, non-ideal component attenuate efficiency of the DC-DC converter up to 90%.

There a wide variety of topologies for the DC–DC converter depending on arrangement of switches and filter components. Therefore, an input voltage can be regulated to a larger or smaller output voltage, and with same or opposite polarity. buck, boost and buck–boost DC-DC converter are three commonly used basic configurations which produced step-down, step-up and both functions respectively. These three topologies will be introduced below. The buck converter is typically used in the portable device in which battery input voltage is stepped down to supply the digital and analog blocks. Therefore, the buck converter will be discussed more detail.

2.5.1 Circuit description of buck DC-DC converter

Producing regulate and step down voltage is the objective of buck DC-DC converter. Therefore, the topology of buck DC-DC converter is illustrated in Figure 2.9:

FIGURE 2.9: Buck DC-DC converter.

Two MOSFETs are on and off alternatively at switching frequency $f_S = 1/T_S$, and controlled by Pulse Width Modulation (PWM) to chop the input voltage V_{IN} to acquire a desired step-down output voltage V_{OUT} . The transfer function of Buck converter is:

$$V_{OUT} = DV_{IN} \quad (2.5)$$

Where D is duty cycle and defined as $D = T_{PON}/T_S$ but which is always smaller than V_{IN} . That means that D is smaller than one.

Buck converter can operate in two working modes. The waveform of the inductor current determines the working mode that is in a continuous conduction mode (CCM) or in a discontinuous conduction mode (DCM). If the inductor current flows during whole period, converter is operating in CCM. While if the inductor current falls to zero and remains at zero for a time interval, then converter is operating in DCM. The waveforms for the converter operating in CCM and DCM are shown as in [Figure 2.10](#)

Two MOSFETs turn on and off leads to charge and discharge energy in inductor. Charging and discharging rate of inductor current i_L depends on the input voltage V_{IN} , output voltage V_{OUT} as well as the inductance L. Doing some assumptions, V_{IN} and V_{OUT} are seen as constant. And inductance L is also fixed as long as system is ready. Therefore, the DC analysis of converter in CCM and

FIGURE 2.10: Operating waveforms of Buck converter.

DCM are:

- 1) Converter in CCM

During time interval $0 < t \leq DT$, the PMOS switch is ON and NMOS switch is OFF. The voltage across the inductor L is given by:

$$v_L = V_{IN} - V_{OUT} = L \frac{di_L}{dt} \quad (2.6)$$

Therefore, the current in the inductor is:

$$i_L = \frac{1}{L} \int_0^t v_L dt + i_L(0) = \frac{1}{L} \int_0^t (V_{IN} - V_{OUT}) dt + i_L(0) = \frac{(V_{IN} - V_{OUT})t}{L} + i_L(0) \quad (2.7)$$

Where $i_L(0)$ is the initial current in the inductor L at time $t = 0$. Then peak to peak ripple current of inductor at the time interval $0 < t \leq DT$ is:

$$\Delta i_L = \frac{(V_{IN} - V_{OUT})DT}{L} \quad (2.8)$$

The current in the inductor is rising up at the rate of $\frac{(V_{IN} - V_{OUT})}{L}$ at this time interval as seen in the Figure 2.10(a).

During the time interval $DT < t \leq T$, the PMOS switch is OFF and NMOS switch is ON. The voltage across the inductor L is given by:

$$v_L = V_{IN} - V_{OUT} = L \frac{di_L}{dt} \quad (2.9)$$

Therefore, the current in the inductor is:

$$\begin{aligned}
 i_L &= \frac{1}{L} \int_{DT}^t v_L dt + i_L(DT) \\
 &= \frac{1}{L} \int_{DT}^t (-V_{OUT}) dt + i_L(DT) \\
 &= \frac{(-V_{OUT})(t - DT)}{L} + i_L(DT)
 \end{aligned} \tag{2.10}$$

Where $i_L(DT)$ is the initial current in the inductor L at time $t = DT$. Then peak to peak ripple current of inductor at the time interval $DT < t \leq T$ is:

$$\Delta i_L = \frac{(-V_{OUT})(t - DT)}{L} \tag{2.11}$$

As shown in the Figure 2.10(a), the current in the inductor is decline down at the rate of $\frac{-V_{OUT}}{L}$ at this time interval.

2) Converter in DCM

DCM can be divided to 3 time intervals as shown in 2.10(b). During the first time interval $0 < t \leq DT$, the PMOS switch is ON and NMOS switch is OFF.

The voltage across the inductor L is given by:

$$v_L = V_{IN} - V_{OUT} = L \frac{di_L}{dt} \tag{2.12}$$

Therefore, the current in the inductor is:

$$i_L = \frac{1}{L} \int_0^t v_L dt + i_L(0) = \frac{1}{L} \int_0^t (V_{IN} - V_{OUT}) dt + i_L(0) = \frac{(V_{IN} - V_{OUT})t}{L} + i_L(0) \quad (2.13)$$

In DCM, the $i_L(0) = 0$, however, in the CCM, $i_L(0) \neq 0$. Hence the current in the inductor is:

$$i_L = \frac{(V_{IN} - V_{OUT})t}{L} \quad (2.14)$$

Hence peak current of inductor at the time $t = DT$ is:

$$i_L(DT) = \Delta i_L = \frac{(V_{IN} - V_{OUT})DT}{L} \quad (2.15)$$

The current in the inductor at this time interval is illustrated in the Figure 2.10(b).

During the time interval $DT < t \leq (D + D_1)T$, the PMOS switch is OFF and NMOS switch is ON. The voltage across the inductor L is given by:

$$v_L = V_{IN} - V_{OUT} = L \frac{di_L}{dt} \quad (2.16)$$

Therefore, the current in the inductor is:

$$\begin{aligned}
 i_L &= \frac{1}{L} \int_{DT}^t v_L dt + i_L(DT) \\
 &= \frac{1}{L} \int_{DT}^t (-V_{OUT}) dt + i_L(DT) \\
 &= \frac{(-V_{OUT})(t - DT)}{L} + i_L(DT)
 \end{aligned} \tag{2.17}$$

Where $i_L(DT)$ is the initial current in the inductor L at time $t = DT$ and it is $\frac{(V_{IN} - V_{OUT})DT}{L}$, Then peak current of inductor at the time interval $DT < t \leq$

$(D + D_1)T$ is:

$$i_L(DT) = \Delta i_L = \frac{(-V_{OUT})(t - DT)}{L} = \frac{(-V_{OUT})D_1T}{L} \tag{2.18}$$

As seen in the Figure 2.10(b), the current in the inductor decline down at the rate of $\frac{-V_{OUT}}{L}$ and reach zero at $t = (D + D_1)T$.

During last time interval $(D + D_1)T < t \leq T$, both NMOS and PMOS switch are OFF. The current in the inductor is zero until next period.

The ripple of the inductor current in converter is:

$$\Delta i = T_{PON}(V_{IN} - V_{OUT})/L = T_{NON}V_{OUT}/L \tag{2.19}$$

Where in CCM, the $T_{P_{ON}} = DT_S$ and $T_{N_{ON}} = (1 - D)T_S$, While in DCM, the $T_{P_{ON}} = DT_S$ and $T_{N_{ON}} = D_1T_S$. The value of inductor current is the sum of DC load current $I_{OUT} = V_{OUT}/R_{load}$ and half the ripple of inductor current:

$$i_L = I_{OUT} + \Delta i/2 \quad (2.20)$$

Figure 2.11 depicted the inductor current waveforms of converter with the different load. The load current at the boundary can be derived:

FIGURE 2.11: Boundary waveform of Buck converter.

$$i_{OUT3} = \Delta i/2 = V_{OUT}/R_{load} \quad (2.21)$$

Inserting equation 2.19

$$R_{load} = 2f_S L/(1 - D) \quad (2.22)$$

Above equation is established only at the boundary consequently which give the freedoms of design whether the converter operate in CCM or DCM. The level

of DC load current determines the working mode of converter when switching frequency f_s , inductance L and duty cycle D are not variable.

As seen in Figure 2.9, inductor current is filtered before delivery to load. The output part of buck converter is composed of filter capacitor and load which is shown in Figure 2.12.

FIGURE 2.12: Output part of Buck converter.

The model of filter capacitor is seen as its capacitance C_{OUT} series with its equivalent series resistance (ESR) designated by r_C . Current and output voltage waveforms in the converter output circuit both in CCM and DCM are depicted in Figure 2.13

The Figure proves that the output voltage is not DC voltage alone in practice. Instead, the output voltage include both AC component and DC component. Because, the output current is provide by the inductor current. Theoretically, the impedance of filter capacitor is designed much small than load resistance R_{load} . As a result, all the DC component of the inductor current flows through the load

FIGURE 2.13: Working waveform at the output part of Buck converter.

resistor R_{load} , while all the ac component flows to filter capacitor branch and divided between the capacitor C_{OUT} and the load resistor R_{load} . Thus, the inductor current is approximately filtered at the output part of converter as $i_L \approx i_C + I_{OUT}$. Therefore, the AC component of output voltage V_{OUT} is equal to the sum of voltage across the filter capacitance C and filter capacitor ESR r_C . As seen in Figure 2.13, when Buck converter operate in the DCM, there is a time interval during which inductor current is zero, but load current is still continues due to that filter capacitor worked as source to provide current during this short period.

In order to regulate the input voltage to desired output voltage against the load, input voltage and temperature variation, the DC–DC converter need a control loop. The dominating control methods are Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). The control method also can be categorized to two methods which are Voltage-mode control and Current-mode control according to the feedback parameters.

2.5.2 PWM control and PFM control

Figure 2.14 illustrated the PWM controller of Buck converter. Pulse Width Modulator adjust the width of square wave leads to the change on duty cycle D of MOSFETs according to margin of that feedback output voltage compared with

FIGURE 2.14: PWM controller of Buck converter.

desired output voltage $V_{OUT} = DV_{IN}$. D is dynamic until the converter reach the steady state at that moment average V_{OUT} is equal to desired voltage. The function of Modulator is depicted in Figure 2.15: The feature of PWM control is

FIGURE 2.15: Pulse width modulator of PWM controller.

that switching frequency of the MOSFETs is the frequency of modulator and constant. PMOS or NMOS turn on alternatively. The PMOS is turned on when gate voltage is low, but the NMOS is turned on when gate voltage is high. Therefore, the control square wave generated from modulator can be used for both PMOS

and NMOS. But, the PMOS and NMOS are the Power MOSFETs with huge size, they cannot be turn on or off shortly. Hence, the original control square wave must generate two non-overlap square wave with proper dead-time ensuring that PMOS and NMOS does not turn on simultaneously. Then, two non-overlap square wave control the PMOS and NMOS separately. The dead-time for controlled square wave will be discussed more detail in the afterwards.

High efficient DC-DC converter at high load can be made when PWM control is applied. However, the efficiency of PWM controlled converter at light load will decrease largely. Some power losses of the PWM control converter is independent of load level, therefore those losses will have significant amount relative to the output power at light load. Furthermore, the switching loss also increase with the load current scales down. The Figure 2.16 illustrated the general partition of efficiency curve of a DC-DC converter. In region I (high loads), conduction loss

FIGURE 2.16: General efficiency curve of DC-DC converter at wide load range [5].

induced by high load current dominates power losses. In region II (light loads), the V-I overlap losses and current ripple induced conduction losses (i.e.rms losses)

contribute the major power losses. The V–I overlap losses result from switching losses associated with the voltage-current (V–I) overlap of the power train, which are proportional to load current, input voltage, and switching frequency, as a result, V–I overlap losses will decrease with the load current scale down. However, the conduction losses caused by the current ripple is independent of load current and remains constants. As the load current continues scale down, the conduction loss contributed from the ripple of inductor current will become dominant. In region III (very light loads), gate – drive losses when charging and discharging the gate capacitances of the power transistors during switching transitions become dominant power dissipation. Consequently, it is the best way for reducing the power losses to decrease the switching frequency of the power transistors.

As a result, the PFM control is proposed for making the converter at the light load continuously acquiring high efficiency. It is significant for extending the running time of portable device at the light load to maintain high efficiency because that portable device work in light load (that is idle mode) at most of time operate. The operating waveform of PFM is illustrated in the Figure 2.17: The switching frequency f_S of the MOSFETs is changing accordingly to the load current down or up. The PFM controller is idle at some period to decrease the power consumption associated with the ripple of inductor current which is independent of load current. Hence, DC-DC converter at light load can be maintained with high efficiency.

FIGURE 2.17: PFM control of DC-DC converter.

Same as PWM control not applied to converter at the light load, the PFM control will reduce the efficiency of converter at the high load. At the high load, PFM controller need many active cycles to charge output voltage up to desired value. This control method not only reduce the conduction losses caused by load current, but also increase the loss caused by the switching transaction of MOSFETs.

One drawback of PFM control is the unpredictable switching noise which happens during the switching period of MOSFETs. At that time, the converter exists seem as chaotic. This unpredictable noise make the PFM control converter not well-suited to wireless communications application.

2.5.3 Voltage-mode control and Current-mode control

Voltage-mode control is a control method with a single loop which feedback the converter output voltage. It is also called duty-cycle control which is identical to PWM control shown in Figure 2.14, The PWM method has illustrated that

it adjusts the duty cycle directly according to output voltage changes. While, Current-mode control is a multiple-loop control Method with two loops: an inner current loop and an outer voltage loop as shown in Figure 2.18. The method

FIGURE 2.18: Current-mode control Buck converter.

is called current-mode control because the inductor current is directly controlled, whereas the output voltage is controlled only indirectly by the current loop. In fact, the current-mode control can be divided to peak-current-mode control and average-current control depends on which kind of inductor current is sensed. As seen in Figure 2.18 which illustrated the peak-current mode control, the inner current loop controls the inductor peak current, while the outer voltage loop controls the output Voltage. Because the converter load is sourced by the inductor, the output load current is determined by the inductor average current. In Buck converter, the load current is equal to the average current.

Mainly three advantages are offered by current-mode control over voltage-mode control. Firstly, current-mode control inherently provides a fast pulse-by-pulse short circuit and overcurrent load protection, enhancing the converter reliability. Since maximum value of transistor switch current is limited by the control current, whenever the transistor switches current goes too high, the switches will turn off. In addition, the output load current may also be limited by clamping the control voltage. Hence, over current failure of transistors can be prevented and the load current can be controlled not higher than rated maximum level. Secondly, current-sharing problems happened in parallel converters which increase current capability and/or redundancy can be eliminated by applying current-mode control method. This is because the output load current is solely regulated by the control signal load. Therefore, same control signal can be provided to all units which are able to deliver same amount of load current. Thirdly, transformer imbalance that happens in symmetrical converters can be settled by current-mode control method. The transformer imbalance may be caused by the volt-second differences between the positive and negative pulses applied to the transformer. In addition, the current mode control method remove the series capacitor which is usually used in full-bridge converters to remedy the transformer imbalance.

But, for peak-current mode control, the inner current-loop inherently unstable when duty-ratio more than 0.5 which leads to subharmonic oscillation. Therefore,

the slope compensation is required to stabilize the control loop. Then this further increase the complexity of current-mode control circuit. Furthermore, peak-current mode control is susceptible to noise, especially when the inductor ripple is small. While the average-current mode is good immunity to switching noise because the scheme sense average current. In addition, the current sensor which is required in current-mode control brings some natural drawbacks. Firstly, resistor as a usual current sensor is connected in series with inductor as shown in Figure 2.18. Hence, power loss is generated by the current flow through the resistor. Moreover, transistor current capability is degraded by the series resistor which may result in a larger transistor size.

While, the benefit of voltage-mode control is that it is better noise immunity than current-mode control since the control loop only take feedback from output voltage. Furthermore, the voltage-mode control method have a simpler control circuit than current-mode control. This makes the voltage-mode control more popular. However, the simpler control circuit also bring the drawback. Firstly, output voltage level is an only parameter that can be controlled. Hence another essential parameter-output load current which determine the converter Figure of Merits is overlooked. Secondly, the voltage-mode control may have a very high current spike in the inductor. This increase difficulty of the inductor choosing [6].

2.5.4 Power losses of the converter

The power losses of the converter mainly contributed from three factors as shown in below:

1) Switching Loss which is caused by:

- Charging/Discharging MOS Non-Linear Output Capacitance.
- Gate Drive Power - Charging/Discharging of Gate Capacitance.
- Translational – Rise/Fall Time of Gate Driver.

2) Conduction Loss is load current dependent and associated with:

- On-resistance of MOS.
- Forward Drop of Body Diode – Dead-Time.
- Inductor/Capacitance Series Resistance.

3) Static Loss dissipated by:

- Dark/Standby Current.
- Leakage Current.

2.5.4.1 MOSFETs power consumption

The majority power consumption of the converter is dissipated by the MOSFETs of the converter, the total power losses of MOSFETs is:

$$P_{FET} = P_{r_{DS}} + P_{SW}/2 \quad (2.23)$$

Where, $P_{r_{DS}}$ is the conduction losses and the P_{SW} is the switching loss, and:

$$P_{r_{DS}} = r_{DS} i_{rms}^2 \quad (2.24)$$

$$P_{SW} = f_S C_{para} V^2 \quad (2.25)$$

i_{rms} is rms value of the ripple of inductor current at the steady state which is related to the input voltage V_{IN} , output voltage V_{OUT} and inductance L . The voltage V is also determined by input voltage V_{IN} and output voltage V_{OUT} when MOSFETs worked as a switch with on or off state to charge or discharge some node in the converter to certain voltage level. Therefore, i_{rms} and voltage V sometimes is seen as constant because the system spec of the converter already fix the input voltage V_{IN} , output voltage V_{OUT} and inductance L .

r_{DS} is the on resistance of MOSFETs, and C_{para} is the parasitic capacitance

of MOSFETs. Those are related to the size of MOSFETs or rather directly related to the Width of MOSFETs. r_{DS} is reverse proportional to the Width ,while C_{para} is proportion to Width. Therefore, seen in the equation 2.23, an optimum Width of MOSFETs can be made to realize the minimum power consumption in case of the system spec is fixed. However, load current is always changing for the portable device, then a lot of designs proposed adaptive size of MOSFETs cater to the wide load range in order to maintain the high efficiency.

2.5.4.2 Non-ideal switching losses of MOSFETs

Because of huge size of power MOSFETs, the parasitic capacitance appears in the gate of MOSFETs is very big. The Switching of MOSFETs is not same as that of ideal switch which can turn on or off sharply . Therefore, a dead-time is necessary during one MOSFETs turn off and another turn on immediately as seen in Figure 2.19. The switching activity of MOSFETs in DC-DC converters are almost same except difference switching sequence. Hence, the diode conduction loss will be discussed based on the buck DC-DC converter.

If the dead-time is too short shown in Figure 2.20, two MOSFETs will turn on simultaneously which make the input voltage V_{IN} directly connect to ground, the result can range from efficiency decreasing enormously to the breakdown of the

FIGURE 2.19: Non-ideal MOSFETs in the DC-DC converter.

DC-DC converter. Optimum dead-time can improve the converter power efficiency by more than 12.5% [7].

FIGURE 2.20: Dead-time too short.

However, as a result of the MOSFETs diode conduction depicted in Figure

2.21, the dead-time is neither designed too long. Research has proven that Power losses by body diode of MOSFETs take up 6% of the total useful output power. Furthermore, percentage is more prominent for low output voltage devices at high frequency.

FIGURE 2.21: Dead-time too long.

Other two non-ideal MOSFETs switching scenario happened when the converter operate at DCM. Figure 2.22 depicted that the NMOS turn off too late.

When NMOS turn off too late, a reverse current is sourced from the output filter capacitor which formulate a charge sharing with parasitic capacitor. This reverse current shunt the current sourced to the load current. Therefore, this scenario degrade the efficiency.

While, when NOMS turn off too early shown in Figure 2.23. Conduction loss of body diode at NMOS will come out. The body diode is turned on by the

FIGURE 2.22: NMOS turn off too late.

inductor current keeps flowing even if the NMOS turn off. Obviously, efficiency of converter is degraded in this scenario. In order to make a high efficient DC-DC converter, above discussions are fairly significant factors that must be considered when doing design.

FIGURE 2.23: NMOS turn off too early.

Chapter 3

Voltage Reference dedicated for Energy Harvesting application

In this chapter, a CMOS ultra-low voltage reference circuit with ultra-low power consumption of 180nW is proposed. The circuit, implemented in Global Foundries 65nm CMOS 1P6M process, operates at a supply voltage of 1V. It is based on sub-threshold MOSFETs using the technique of compensating a PTAT-based variable with the gate source voltage of a sub-threshold MOSFET. The novelty of circuit is the use of an improved folded cascode current mirror op-amp (IFCC-OPA) operating directly from a 1V power supply. The resulting voltage is equal to the extrapolated threshold voltage of a MOSFET at absolute zero temperature, which was about 435mV for the MOSFETs used. The proposed circuit achieves

an average temperature coefficient of $30 \text{ ppm}/^{\circ}\text{C}$, $12 \text{ ppm}/\text{V}$ in line regulation for a supply voltage range of $0.6 \sim 1.2\text{V}$, and a power supply rejection ratio (PSRR) of -38dB at 100Hz . The overall power consumption is only 180nW .

3.1 Introduction

In modern power management systems, a temperature compensated voltage reference independent of power supply and load current variations is of great interest to circuit designers and consumers [8]. The rationale is that it can be used in many of the digital and analogue circuitry which comprises of analog-to-digital converter (ADC), voltage regulators (LDO/HDO), flash memories and other portable communication devices [9, 10]. Furthermore, for the field of energy harvesting applications, there is a surge in demand for smaller chip area and lower power consumption devices. This phenomenon is obvious as there have been intensive research carried out in the field of energy harvesting as seen by the recent increase in research publication over the past few years. The rationale is that it is suitable to be used for portable mobile devices and wireless sensor networks [11, 12].

Voltage reference circuit is one of the most important building blocks for the power management system embedded in an energy harvesting device. Its objective is to generate a temperature compensated, regulated reference voltage

[11, 12]. However, integrated voltage reference embedded on chip for state-of-the-art mobile portable devices or wireless sensor system face severe design challenges.

Due to the limited available energy source, these devices must consume ultra-low power. Furthermore, the silicon area overhead should be minimized to reduce design cost. This is a vital pre-requisite criterion for implantable biomedical applications whereby a smaller device size will no doubt translate to a less invasive and safer surgery operation for patients. Recent research has shown that there is an escalating global interest for voltage references to be operated well across a wide range of supply voltage, in particular sub 1-V. The prominent rationale includes the fact that supplies voltages are powered by energy harvesting units typically provide only low output voltage [13]. Hence, there is a huge demand to develop an ultra-low power voltage reference circuit yielding a sub 1-V reference voltage, dedicated for energy harvesting device.

For the past decade, there have been several approaches to design voltage references in BJT technology. Bandgap reference using parasitic BJTs (bipolar junction transistors) is the most common method. Vertical parasitic bipolar transistor can be implemented in a CMOS process. A temperature compensated reference voltage is generated in bandgap reference circuit by combining two

voltages with opposing temperature characteristics: a complementary-to-absolute-temperature (CTAT) voltage and a proportional-to-absolute-temperature (PTAT) voltage. Sometime the method utilizes the combination of PTAT and CTAT current instead of voltage to generate a temperature-independent reference current. Bandgap references yields a minimum reference voltage of about 1.25 V and therefore requires a minimum supply voltage of 1.4 V. In the Chapter 2, we introduce the fundamental theory for the design of conventional Bandgap references circuit. It was shown that the output voltage of a bandgap reference has high power rejection and a very small temperature coefficient and is stable against process variations. However, the design challenge motivate us to achieve the low voltage and low power Voltage reference, therefore many state-of-arts techniques have been proposed.

First is to use a low-bandgap material (e.g., germanium) for the diodes in the bandgap reference circuit. This technique is to virtually lower the material bandgap, using an electrostatic field. To implement this method one has to replace the normal diodes by dynamic threshold MOS transistors (DTMOST) as it is proposed in [14]. Nevertheless, this method of low voltage BGR design has a number of drawbacks. The DTMOS transistors require a large layout and have a large gate capacitance. Also, DTMOS is a non-standard device and this makes the circuit less reproducible. Another method discussed in [15–19] involved the use

of resistive subdivision methods, known as current mode approach, can overcome the design challenge faced above. However, the tradeoff is the use of large value resistors which increase the silicon area overhead.

The Bandgap reference circuit is bipolar in nature and so when the supply voltage is below 1V, a conventional bandgap reference does not show good stability [17, 20, 21]. In conclusion, the trade-off in recent design techniques are evident that Bandgap reference circuit is not ideally suitable for low power and low voltage application. Therefore, non-bandgap voltage reference circuits are proposed.

3.1.1 Voltage Reference based on Transistor threshold Voltage Subtraction

The first step to realize a voltage reference is to find a stable unit voltage, such as the bandgap voltage used in Bandgap references circuit. One typical parameter in CMOS process is the threshold voltage which is temperature dependent and cannot be used as a reference over a wide temperature range.

$$V_{TH}(T) = V_{TH}(T_0) - \kappa T \quad (3.1)$$

Where $V_{TH}(T_0)$ is the sub-threshold voltage at temperature 0 K and temperature independent. κ is the temperature coefficient of V_{TH} .

In a multi-threshold technology, where transistors with different threshold voltages are fabricated, a subtraction of two threshold voltages may result in the cancellation of temperature-sensitive parameters of the threshold voltages. Therefore, threshold voltage subtraction can be used for the design of CMOS voltage reference [22, 23].

The simplified structure of such voltage reference is shown in Figure 3.1. NMOS transistor also can be used. Threshold voltage V_{th} in transistor M_1 is larger than it in transistor M_2 . Assuming equal current for both transistors and using:

$$V_{GS} = V_{TH} + \sqrt{\frac{I}{K}} \quad (3.2)$$

Where $K = \sqrt{\frac{1}{2}\mu C_{ox} \frac{W}{L}}$ for a saturated MOS transistor. The reference voltage is given by:

$$V_{ref} = |V_{GS1}| - |V_{GS2}| = |V_{TH1}| - |V_{TH2}| + \sqrt{I} \left(\sqrt{\frac{1}{K_1}} - \sqrt{\frac{1}{K_2}} \right) \quad (3.3)$$

Differentiating 3.3 with respect to the temperature:

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} &= \frac{\partial(|V_{TH1}| - |V_{TH2}|)}{\partial T} + \frac{1}{2\sqrt{I}} \left(\sqrt{\frac{1}{K_1}} - \sqrt{\frac{1}{K_2}} \right) \frac{\partial I}{\partial T} \\ &\quad + \frac{\sqrt{I}}{2} \left(\frac{1}{\mu_2 \sqrt{K_2}} \frac{\partial \mu_2}{\partial T} - \frac{1}{\mu_1 \sqrt{K_1}} \frac{\partial \mu_1}{\partial T} \right) \end{aligned} \quad (3.4)$$

FIGURE 3.1: Voltage Reference based on threshold subtraction.

In 3.4, the drain current, the mobility, and the threshold voltage are the three temperature-dependent factors. The drain current varies with temperature because of its dependence on the threshold voltage and the mobility. If the transconductance parameters of two transistors are the same, i.e. $K_1 = K_2$, the effect of temperature variations of the drain current on the reference voltage will be eliminated. In practice, exact matching of transistor parameters may not be easy and a low bias current is generally used to minimize the effect of the drain current on the reference voltage. For further improvement of the temperature behavior of the reference voltage, the drain currents can be set at the Zero Temperature Coefficient (ZTC) point of the transistors, where they are independent of temperature [22]. In order to reduce the variation of the reference voltage due to the temperature dependence of the mobility, the absolute values of the mobilities of the transistors, as well as their temperature dependence, must be made the same

[23].

Therefore, with proper circuit design and good process control for the realization of the transistors, a low temperature coefficient output voltage be obtained and be simplified to:

$$V_{ref} \approx |V_{TH1}| - |V_{TH2}| \quad (3.5)$$

In summary, this technique of implementing voltage references requires multi-threshold-voltage devices and ensure good process control to make temperature coefficient of the threshold voltages can cancel each other. In addition, the temperature dependency of reference voltage can be minimized by temperature-independent small bias current [24]. Therefore, the process variation and bias current level strongly influence the temperature-dependence of the reference voltage. Another disadvantage of these references is that the output voltage is based on the threshold voltage and cannot be controlled accurately. However, this is of little importance rather than its temperature dependence since it can be adjusted by laser trimming or compensated by system design [23].

3.1.2 Voltage Reference based on Weighted difference of gate-source voltage of transistor

A voltage reference based on gate-source voltage difference between a PMOS and a NMOS transistor is presented in [24]. The main advantage of this reference is that it can be realized in a standard CMOS process.

The proposed circuit is shown in Figure 3.2. Transistors $M_{S1} - M_{S3}$ form the start-up circuit. The bias circuit consists of transistors $M_1 - M_4$ and resistor R_B .

The bias circuit $I_B(T)$ is given by:

$$I_B(T) = \frac{2}{\mu_P(T_0) C_{ox} R_B^2} \left[\frac{1}{\sqrt{(W/L)_2}} - \frac{1}{\sqrt{(W/L)_1}} \right]^2 \left(\frac{T}{T_0} \right)^{m_p} = I_B(T_0) \left(\frac{T}{T_0} \right)^{m_p} \quad (3.6)$$

The reference core circuit is formed by transistors M_N and M_P and resistors R_1

FIGURE 3.2: Voltage Reference based on Weighted difference of gate-source voltage of transistors.

and R_2 . From the circuit, the reference voltage is given by:

$$V_{ref} = \left(1 + \frac{R_1}{R_2}\right) V_{GS_n} - |V_{GS_p}| \quad (3.7)$$

For proper operation of this circuit, all the transistors, especially M_P and M_N , should be biased in saturation. Therefore, consider all temperature dependent parameter, differentiated the 3.7 with temperature:

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} &= \left(1 + \frac{R_1}{R_2}\right) \frac{\partial V_{GS_n}}{\partial T} - \frac{\partial |V_{GS_p}|}{\partial T} \\ &= \left[-\left(1 + \frac{R_1}{R_2}\right) \kappa_{V_{TH_n}} + \kappa_{V_{TH_p}} \right] + \frac{m_p}{T_0} \sqrt{\frac{2MI_B(T_0)}{\mu_P(T_0)C_{ox}(W/L)_p}} \\ &\quad \times \left[\left(1 + \frac{R_1}{R_2}\right) \left(\frac{1}{2} + \frac{m_n}{2m_p}\right) \sqrt{\frac{\mu_P(T_0)(W/L)_p}{\mu_n(T_0)(W/L)_n}} \left(\frac{T}{T_0}\right)^{\frac{m_p+m_n-2}{2}} - \left(\frac{T}{T_0}\right)^{m_p-1} \right] \end{aligned} \quad (3.8)$$

Where M is the mirroring factor (as shown in Figure 3.2), $\kappa_{V_{TH_p}}$ and $\kappa_{V_{TH_n}}$ are the temperature coefficients of the threshold voltages of PMOS and NMOS transistors, and m_p and m_n are the mobility exponents of PMOS and NMOS transistors respectively. A temperature independent reference voltage can be obtained by making the first-order and higher-order TC term to be vanished in 3.8. The linear term can be eliminated by the resistor ratio, which is given by:

$$\frac{R_1}{R_2} = \frac{\kappa_{V_{TH_p}}}{\kappa_{V_{TH_n}}} - 1 \quad (3.9)$$

While, the high-order term can be eliminated at the $T = T_r$ (T_r is the room temperature) by transistor size ratio, which is given by:

$$\frac{(W/L)_p}{(W/L)_n} = \frac{\frac{\mu_n(T_0)}{\mu_p(T_0)} \left(\frac{T_r}{T_0}\right)^{m_p - m_n}}{\left(\frac{\kappa_{V_{TH_p}}}{\kappa_{V_{TH_n}}}\right)^2 \left(\frac{1}{2} + \frac{m_n}{2m_p}\right)^2} \quad (3.10)$$

So, the minimum required power supply can be obtained at the lowest operating temperature, T_{in} but V_{TH_n} and $|V_{TH_p}|$ are maximum, and it is given by:

$$V_{DD_{min}} = \left(1 + \frac{R_1}{R_2}\right) V_{GS_n}(T_{min}) + |V_{DS_5(sat)}| \quad (3.11)$$

Which shows that the circuit is able to operate with low-power supply voltage when low-threshold voltage devices are available.

In summary, the benefit of this technique is that implementation of voltage references can be reproducible in any standard CMOS technology. However, the minimum supply voltage is process dependent which make the application limited. Furthermore, the reference voltage is only less temperature independent at temperature higher than 0 °C

3.1.3 Voltage Reference based on Subthreshold MOSFETs

A voltage reference based on Subthreshold MOSFETs is presented in [25]. The implementation of voltage reference core circuit is illustrated in Figure 3.3. The

FIGURE 3.3: Voltage Reference based on Subthreshold MOSFETs.

circuit can be divided to two sub-circuits. Transistors $M_1 - M_4$ bias I_B , resistor R_1 , and capacitor C_{C1} forms one sub-circuit, in which the Current I_{R1} is determined by voltage V_{GS1} and given by:

$$I_{R1} = \frac{V_{GS1}(I_B)}{R_1} \quad (3.12)$$

This current is elaborated and bias to the another sub-circuit which is composed of transistors $M_5 - M_{11}$, resistors $R_2 - R_4$, and capacitor C_{C2} so that output voltage results as the sum of a PTAT component and a V_{GS} -based component, and the

output voltage is given by :

$$V_R = R_4 I_{R4} + V_{R3} = R_4 \left(\frac{V_{R3}}{R_3} - I_{R1} \frac{S_6}{S_4} \right) + V_{R3} \quad (3.13)$$

Where:

$$V_{R3} = \frac{S_5}{S_4} \frac{R_2}{R_1} V_{GS1}(I_B) + U_T \ln \left(\frac{S_8}{S_7} \frac{S_5}{S_6} \right) \quad (3.14)$$

Substitute to the equation 3.13,

$$V_R = \alpha V_{GS1}(I_B) + \beta U_T \quad (3.15)$$

where:

$$\alpha = \left(1 + \frac{R_4}{R_3} \right) \frac{R_2}{R_1} \frac{S_5}{S_4} - \frac{R_4}{R_1} \frac{S_6}{S_4} \quad (3.16)$$

$$\beta = \left(1 + \frac{R_4}{R_3} \right) \ln \left(\frac{S_8}{S_7} \frac{S_5}{S_4} \right) \quad (3.17)$$

Differentiate equation 3.15 with temperature, the condition, making the output

voltage $\frac{\partial V_R}{\partial T} = 0$, is given by:

$$\frac{\alpha}{\beta} = - \frac{U_T(T_0)}{K_G} \quad (3.18)$$

[24] achieved a voltage reference can operate at 1.2 V power supply and consumes 2.6 uW. One drawback of this technique is, if the lower power supply must be used, this technique have to adopt a low threshold process. Hence, the power

supply for this technique is process dependent. Second drawback is that bulky capacitor must be used to stabilize the circuit. This increase the die areas. In addition, this feedback loop suffers from a poor line regulation and output voltage variation with temperature due to limited loop gain. The last drawback is the power consumption although it can be decreased by increasing the resistance of resistor.

There is a new emerging technique which employs the concept of switched-capacitor (SC) to generate a regulated and temperature compensated voltage reference circuit. Its benefits include the elimination of any bulky and area-consuming resistors and reduce any undesirable offset voltage of the operational amplifier. However, it has its own trade-offs as the use of capacitors require precise matching in layout and will incur a large silicon area overhead.

In addition, switching losses are significant especially at a high operating frequency which will no doubt degrade the overall efficiency of the voltage reference circuit. Therefore, in this chapter, a new voltage reference circuit is implemented based on the sub-threshold MOSFETs with an improved line/load regulation, output voltage variation with temperature and a much lower power consumption. In order to achieve the objective above, an improved folded cascode current mirror is implemented depicted in Figure 3.14. The temperature compensated reference

voltage yields a value of 435 mV which has minimal variation with temperature and supply voltage.

3.2 Proposed voltage reference circuit

3.2.1 MOSFET in Sub-Threshold Region

The I-V characteristic of an NMOS transistor in the sub-threshold region has an exponential relationship and given by:

$$I_D = \mu C_{ox} V_T^2 S \exp\left(\frac{V_{GS} - V_{TH}}{m V_T}\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (3.19)$$

Where μ is the carrier mobility, S is the aspect ratio of the transistor, C_{ox} is the gate-oxide capacitance, $V_T = \pi r^2 (k_B T / q)$ is the thermal voltage, in which k_B is the Boltzmann constant, T is the absolute temperature and q is the electron charge. V_{TH} is the threshold voltage of MOSFET and m is the sub-threshold slope. When the $V_{GS} > 3V_T$, the current I_D can be simplified and expressed as:

$$I_D = \mu C_{ox} V_T^2 S \exp\left(\frac{V_{GS} - V_{TH}}{m V_T}\right) \quad (3.20)$$

then:

$$V_{GS} = mV_T \ln \frac{I_D}{\mu C_{ox} V_T^2 S} + V_{TH} \quad (3.21)$$

The structure of the voltage Generation Loop is presented in Figure 3.14.

Except for the transistor M_{NR} operated in the deep triode region, the rest of transistors in the structure are operated in the sub-threshold region.

The reference voltage V_{REF} is defined in the Voltage loop formed by gate source voltage of transistors M1-M5 and can be given by:

$$V_{REF} = V_{GS_5} + V_{GS_3} + V_{GS_1} - V_{GS_4} - V_{GS_2} \quad (3.22)$$

Each branch of the voltage loop is biased with same current I_D . Hence, from 3.20

and 3.21 the reference voltage can be derived as:

$$V_{REF} = V_{TH} + mV_T \ln \frac{3I_D}{\mu C_{ox} V_T^2 S_5} + mV_T \ln \frac{2S_4 S_2}{S_3 S_1} \quad (3.23)$$

In addition, the bias current I_D is defined on the transistor M_{NR} which is operated in deep triode region and is given by:

$$I_D = \frac{\Delta V_{DS_{NR}}}{R_{NR}} \quad (3.24)$$

and:

$$\Delta V_{DS_{NR}} = V_{GS_7} - V_{GS_6} \quad (3.25)$$

$$R_{NR} = 1/S_{NR}\mu C_{OX}(V_{REF} - V_{TH}) \quad (3.26)$$

Therefore, from the 3.21, the bias current I_D is given by:

$$I_{PTAT} = I_D = S_{NR}\mu C_{ox}(V_{REF} - V_{TH}) mV_T \ln \frac{S_7}{S_6} \quad (3.27)$$

The equation prove that this bias current I_D is proportional the temperature variation, as a result, the current I_D is named as a PTAT current. Moreover, approximately, the threshold voltage V_{TH} decreases linearly with temperature and is given by:

$$V_{TH}(T) = V_{TH}(T_0) - \kappa T \quad (3.28)$$

Where $V_{TH}(T_0)$ is the sub-threshold voltage at temperature 0K and temperature independent. κ is the temperature coefficient of V_{TH} . Hence, inserting equation 3.27 and 3.28 to equation 3.23 arrive that :

$$V_{REF} = V_{TH}(T_0) - \kappa T + mV_T \ln \left\{ \frac{6mS_{NR}S_4S_2(V_{REF} - V_{TH})}{S_5S_3S_1} \times \ln \frac{S_7}{S_6} \right\} \quad (3.29)$$

Differentiating equation 3.29 with temperature, temperature derivative of V_{REF} can be expressed as:

$$\begin{aligned} \frac{\partial V_{REF}}{\partial T} = & -\kappa + \frac{mk_B}{q} \ln \left\{ \frac{6mS_{NR}S_4S_2}{S_5S_3S_1(m-1)V_T} \ln \frac{S_7}{S_6} \right\} \\ & + \frac{(mV_T)^2}{T} \left\{ \frac{1}{V_{REF} - V_{TH}} \left(\frac{\partial V_{REF}}{\partial T} + \kappa \right) - \frac{1}{T} \right\} \end{aligned} \quad (3.30)$$

generally $V_{REF} - V_{TH}(T_0) \ll -\kappa$ and $mV_T \ll -\kappa T$, a temperature compensated reference voltage can be obtained by designing the aspect ratios S_i according to equation 3.30. Hence, it can be derived that: $V_{REF} = V_{TH}(T_0)$. Therefore, it can be proven that the temperature compensated voltage reference is a function of the threshold voltage of the MOS transistor.

3.2.2 Start-up Circuit of Voltage Reference

The objective of a start-up circuit as shown in Figure 3.4 is to start the circuit and allows it to operate well at the very beginning of power-on. Initially, the reference voltage V_{REF} , at the gate of transistor M34, is assigned with a value of 0V. This voltage causes the transistor M33 to turn on and pulls current down from the supply voltage to ground. Therefore, the gate of transistor M31 is pulled to VDD and it turns on. This will ultimately result in the turning on for transistor M22 and M23. Hence, the whole circuitry starts working and thereafter, the start-up circuit will be turned off. The rationale is to save power consumption.

A start-up circuit is required for every voltage reference circuit because of its bi-stable characteristics

FIGURE 3.4: Start-up of Voltage Reference.

3.2.3 Improved Folded Cascode Current Mirror Operational Amplifier

Our proposed voltage reference circuit has implemented an improved folded cascode current mirror operational amplifier (IFCC-OPA) as shown in Figure 3.5. This is used to increase the power supply rejection ratio so that it will reduce the line sensitivity of the circuit. The bias current is a replica of the current in the voltage generation loop circuit. Hence, the current in the input stage (IFCC-OPA) do not need to control its operation. The bias voltage V_{bias} , is generated in the startup circuit. The signal current generated by the input differential pair is folded and collected by two cascode current mirrors which increased the output impedance to make it more resilient to power supply ripples. This also increases

FIGURE 3.5: folded cascode op-amp of Voltage Reference.

the gain of the operational amplifier. Since the input gain stage is fully symmetrical, the systematic offset for the first and second stage of the push-pull topology circuit is practically zero. This allows excellent power supply and common-mode rejection ratio. The bias current in the improved folded cascode current mirror operational amplifier (IFCC-OPA) matches the current flowing in the voltage generation loop circuit, which in turn is designed to be ultra-low current which will lead to low power consumption.

However, since the bias current of the generation loop circuit resembles a PTAT feature, its power consumption will increase proportionally to absolute temperature. The compensation capacitance, $C1$, is included to ensure that the stability of the whole proposed voltage reference circuit under any operating conditions will not be compromised at all times.

3.2.4 Measurement results

The proposed circuit was implemented using Global Foundries 65nm CMOS 1P6M process. The die photo is depicted in Figure 3.6, and the total chip area (excluding pads) is about 0.024mm². The chip measurement is done by using the high temperature wafer probing machine - Cascade Elite 300 as shown in Figure 3.7.

In Figure 3.8, the output voltage V_{REF} versus V_{DD} shows that the proposed voltage reference circuit starts working properly from $V_{DD} = 0.5V$ to 1.3V. In addition, Figure also shows that the line sensitivity is 12 ppm/V with a supply voltage ranging from 0.6 ~ 1.3V.

Figure 3.9 depicted temperature dependence of the reference voltage V_{REF} under different supply voltage condition. And, the experiment temperature coefficient at $V_{DD}=1V$ and 1.2V are 31 ppm/°C and 32 ppm/°C respectively. However, for $V_{DD}=0.5V$, the temperature coefficient is higher.

FIGURE 3.6: Die photo of Voltage Reference.

FIGURE 3.7: Wafer Probing machine.

FIGURE 3.8: Measured V_{REF} with Supply Voltage. FIGURE 3.9: Measured V_{REF} with temperature.

The current drawn from supply voltage as a function of temperature at 1V is measured illustrated in Figure 3.10. This shows that the supply current is 180nA at 27 °C and its power consumption is 180nW.

FIGURE 3.10: Measured Supply Current with Temperature.

In Figure 3.11, the PSRR at room temperature, with a 1pF capacitor, is -38dB at 100Hz and starts to degrade after this frequency. In Figure, the measured output voltage V_{REF} of 5 dies with temperature is tested to evaluate the sensitivity to process and die-to-die variation. A temperature coefficient between 29 ppm/°C to 32 ppm/°C is observed. In Figure 3.13, the distribution and occurrence of output voltage V_{REF} at room temperature is depicted. It also shows that the average temperature coefficient of output voltage V_{REF} yields 30 ppm/°C and the coefficient of variation σ/μ gives a value of 0.35%.

FIGURE 3.11: PSRR of Voltage Reference.

FIGURE 3.12: Measured V_{REF} with Temperature (5 Dies).

FIGURE 3.13: Measured Occurrence with Temperature (5 Dies).

	VLSIC [26]	JSSC [27]	JSSC [28]	This Work
Tech [nm]	130	130	130	65
VDD [V]	0.7 – 1.8	> 0.75	0.7 – 1.8	0.6 – 1.2
V_{REF} [mV]	500	256	548	435
Temp Range [°C]	-50 to 130	-20 to 85	-40 to 120	-40 to 125
TC [ppm/°C]	29.3	40.0	114.0	30.0
$LineRegulation$ [ppm/V]	337.0	50.0	16.1	12.0
$PSRR$ [dB]@100 Hz	-	-	-56	-38.0
Power [nW]	210	170	100	180
Die Area [mm ²]	0.023	0.070	0.0246	0.024

TABLE 3.1: Comparison with past research works

Finally, Table 3.1 summaries the measurement results of this work in comparison with published voltage references for the past few years. From the comparison, the proposed voltage reference circuit achieves one of the lowest power consumption and temperature coefficient of 180nW and 30 ppm/°C respectively. As compared to [27], our proposed work achieves a slightly higher power consumption but a 66% reduction in silicon die area. However, as compared to [28], our proposed work consume a much high power consumption but achieve a 74% improvement in temperature coefficient. Overall, taking into account of tradeoff and all relevant parameters, our proposed voltage reference achieves the best circuit performance.

FIGURE 3.14: Proposed voltage reference.

Chapter 4

Twin frequency control buck

DC-DC converter

This chapter discuss the proposed Twin frequency control of buck DC-DC converter to realize a high efficiency at wide load current range from 10 ~ 50 mA.

Firstly, the literature review briefly describe the state of art control techniques to implement high efficient DC-DC converter at wide load ranges. Consequently, a new method called Twin frequency control was discussed. Twin frequency control method includes the PWM control at high load and PFM control at the light road.

The transition between the PWM and PFM depends on the level of load current which is detected by a current sensing circuit. The blocks of PWM control and PFM control are introduced.

4.1 Literature Review

As discussed in Chapter 2, dominant factor of power consumption in the converter shifts from high load to light load which impact the control method to maintain high efficiency of converter at wide load range. Hence, PWM control and PFM control are integrated together applied to the converter. Discussion in the chapter 2, the feature of PWM control is fixed switching frequency, while that of PFM control is varying the switching Frequency. There is two method to integrated PWM and PFM. One is that control blocks are the same expect fixing frequency in PWM and varying frequency in PFM [29], another is that PWM has different control blocks with PFM [30]. For the prior one, PWM control blocks themselves are able to vary the frequency. Shown in Figure 4.2, Oscillator is used to adjust frequency of the Pulse Modulator to switch PWM control to PFM control. While Figure 4.2 depicted that PFM and PWM are controlled separately.

The fundamental limitation about the PFM control is itself quiescent power on the light load. Generally, the blocks in PWM control normally is complicated and has more quiescent power. As a result, a low quiescent power blocks is designed for PFM control as seen in the Figure 4.2. The comparator is implemented with zero-bias-current which is called dynamic comparator. Subsequently, a digitalized PFM logic to provide control signal.

FIGURE 4.1: Hybrid control Buck converter.

FIGURE 4.2: Dual mode control Buck converter.

The method about switching control between PWM and PFM is also crucial. Sensing one of the operational parameters in the converter is the ordinary method to make control switch. That parameter has different or even opposite characteristic in the PWM compared to PFM. The change about the polarity of cross node voltage V_X at the buck converter during one switching cycle is different in heavy

node from that in light node [29]. In CCM, when switching cycle start, Switch MP is turned on and Switch MN is turned off, current is charged to inductor. At this moment, the voltage V_X end is Positive, whereas as the switch MP is turned off and switch MN is turned on, in order to maintain the original polarity the inductor current begins to discharge at the same time. At this time, the voltage in V_X end is negative. The polarity of voltage V_X will repeat alternatively with the power switch on/off at the heavy load. But once the inductor is at the light load, the switch MN is not turn off in time, the voltage V_X end will become positive when inductor current enters negative [an integrated cmos dc-dc converter for battery-operated systems]. The challenge in this method is sensing the polarity of node voltage V_X . Therefore, a high speed comparator must be designed. Another method is implemented by the external sensing circuit. This causes extra loss and more occupied volume.

Except both PWM and PFM control for DC-DC converter at the wide load range, a tri-mode converter was proposed. A drawback of dual-mode control is that without explicit monitoring of output current, performance deterioration is located between PWM and PFM. Consequently, a tri-mode is configured subsequently to operate over the wide workload range of interest with efficient power conversion [31]. However, additional sensor and monitor in response to the load

demand inevitably brings power consumption which limit the efficiency of multi-mode controller. Therefore, taking into account above literature reviews, a twin frequency control buck DC-DC converter was proposed and its block diagram was illustrated in Figure 4.2.

FIGURE 4.3: Proposed twin frequency control buck converter.

The load current is detected by the average load current sensing circuit and determine the system switching frequency of buck converter to implement switching between PWM and PFM control at wide load range.

4.2 Twin frequency control buck DC-DC converter

Table 4.1 gives the system specs for the proposed buck converter.

Parameters	Units	Our proposed work
V_{in}	V	2.0 ~ 3.0
V_{out}	V	1.25
I_{load}	mA	10 ~ 50
L_1	μH	47.0
C_1	μF	10.0
f_S	MHz	1.0

TABLE 4.1: System specs of proposed buck converter

The buck converter is designed to regulate input voltage V_{IN} range from the 2 ~ 3 V due to limitation of Global Foundries 0.18 μ process. The output voltage V_{OUT} is 1.25 V to drive the analog blocks of portable device. The objective of the proposed twin frequency control is to achieve a high power efficiency of buck converter dedicated at the light load.

The details about circuit implementation of controller in the proposed buck converter is discussed in the following.

4.2.1 PWM control at the heavy load (CCM)

Figure 4.4 illustrated the configuration of PWM control. Controller take feedback from cross node voltage V_X and output voltage V_{OUT} .

FIGURE 4.4: Proposed PWM controller.

Introduced in chapter 2, transfer function of PWM control is $V_{OUT} = DV_{in}$.

D is adjusted in pulse width modulator which has a fixed frequency f_s in the conventional method. However, integrating cross node voltage V_X is used to instead of pulse width modulator in proposed PWM control. Looking at the operating waveform of PWM controller shown in Figure

FIGURE 4.5: Operating waveform of proposed PWM control.

The voltage V_X is :

$$V_X(t) = \begin{cases} V_{IN} & (0 \leq t \leq DT_S) \\ 0 & (DT_S \leq t \leq T_S) \end{cases} \quad (4.1)$$

Then, the average of V_X is:

$$\begin{aligned} \overline{V_X} &= \frac{1}{T_S} \int_0^{T_S} V_X(t) dt \\ &= \frac{1}{T_S} \int_0^{DT_S} V_{IN} dt \\ &= DV_{IN} \end{aligned} \quad (4.2)$$

Compared to $V_{OUT} = DV_{IN}$, it is found that average V_X is equal to the output voltage V_{OUT} at the steady state for every switching cycle. Hence, the output voltage can be controlled indirectly by average V_X . The operation of PWM controller is: at $t = 0$, PMOS turn on by the system clock with frequency f_S . Simultaneously, the integrator starts to integrate. At $t = DT_S$, the output voltage of integrator V_{int} reaches the desired reference voltage V_{REF} , the PMOS turn off and NMOS turn on. At $t = T_S$, the buck converter repeat the cycle.

Integration in the PWM control is implemented by switch capacitor integrator. Traditional integrator has inverting configuration that output voltage is negative. This integrator is difficult to be implemented in an N-well process in

which negative voltage is not allowed. The operation of the integrator has two phase shown in Figure 4.6:

FIGURE 4.6: Intergration of proposed PWM control.

Two non-overlap square wave were used to control the switch with a switching period $T_S = 1/f_S$. During phase 1, voltage V_X charge the C_1 and the total charge stored will be:

$$Q_1(t) = C_1 V_X(t) \quad (4.3)$$

And During phase 2, the charge stored in C_1 is transferred to C_2 , compositing the charge stored in C_2 in previous switching period, and finish charge stored in C_2 is :

$$Q_2(t) = Q_1(t - T_S) + Q_2(t - T_S) \quad (4.4)$$

insert $Q_2(t) = C_2 V_{int}(t)$ and $Q_1(t) = C_1 V_X(t)$, then:

$$C_2 V_{int}(t) = C_1 V_X(t - T_S) + C_2 V_{int}(t - T_S) \quad (4.5)$$

If T_S is very short, let $T_S \rightarrow dt$, hence $V_{int}(t) - V_{int}(t - T_S) \rightarrow dV_{int}(t)$, the equation 4.5 can be expressed as:

$$C_2 dV_{int}(t) = C_1 V_X(t - T_S) \quad (4.6)$$

Because V_X is period value, and $V_X(t - T_S) = V_X(t)$, then:

$$dV_{int}(t) = \frac{C_1}{C_2} V_X(t) \quad (4.7)$$

As a result, the output voltage of integrator V_{int} at the heavy load can be derived as:

$$\begin{aligned} V_{int} &= \int_0^{T_S} dV_{int}(t) dt = \int_0^{T_S} \frac{C_1}{C_2} V_X(t) dt \\ &= \int_0^{DT_S} V_{IN} dt \end{aligned} \quad (4.8)$$

However, the drawback of integrator is that the system bandwidth is reduced due to the low switching frequency f_S of integration which is limited by the bandwidth of op-amp.

Another feedback from output voltage V_{OUT} is going through Error amplifier

to adjust the reference voltage to the integrator. Therefore, this feedback loop bring the load regulation for PWM controller. The schematic of Error amplifier is illustrated in Figure 4.4

Designing that R_1 and R_2 have same resistance, the corrected reference V'_{ref} is :

$$\begin{aligned} V'_{ref} &= \left(1 + \frac{R_2}{R_1}\right) V_{ref} - \frac{R_2}{R_1} V_{OUT} \\ &= 2V_{ref} - V_{OUT} \end{aligned} \quad (4.9)$$

The desired reference voltage V_{ref} will be corrected according to the output voltage V_{OUT} . The corrected V'_{ref} will decrease as the V_{OUT} increase while the corrected V'_{ref} will increase as the V_{OUT} decrease. Even if the V_{OUT} is larger than V_{ref} , the correction mechanism remains.

4.2.2 PFM control at the light load

The merit of proposed PWM controller is that it also can be used to regulate the input voltage of the buck convert at the light load. The operating waveform of PFM control when buck converter at the DCM is illustrated in Figure 4.7:

At the light load, the buck converter normally operated in the DCM. The operation of controller in the DCM is nearly same as that in the CCM. Except that there is an idle period D_2T_S at the moment that both power switch are turned

FIGURE 4.7: Operating waveform of PFM control at the DCM.

off. Hence, the cross node voltage V_X is:

$$V_X(t) = \begin{cases} V_{IN} & (0 \leq t \leq DT_S) \\ 0 & (DT_S \leq t \leq (D + D_1)T_S) \\ V_{OUT} & ((D + D_1)T_S \leq t \leq T_S) \end{cases} \quad (4.10)$$

According to equation 4.7, therefore, the output voltage of integrator V_{int} at the light load is:

$$V_{int} = \frac{f_s C_1}{C_2} \left(\int_0^{D_2 T_S} V_{OUT} dt + \int_0^{DT_S} V_{IN} dt \right) \quad (4.11)$$

The integrator starts integrating $V_X = V_{OUT}$ at $t = (D + D_1)T_S$ and integrating $V_X = V_{IN}$ at $t = 0$ of next period. The latter has larger integral slop due to $V_{IN} > V_{OUT}$ in Buck converter. Therefore, Compared to equation 4.8 at the PWM

control, the average V_X remain valid to control output voltage V_{OUT} indirectly in the DCM.

However, when the buck converter operated in the DCM and is in the dynamic process before reach steady state, the present output voltage V_{OUT} is determined by the previous output voltage. Hence, the error voltage will accumulate to the next cycle. Generally, the error voltage of output voltage is decreasing. But, it is not secured to ensure error voltage converge. Once the error voltage increase, the whole system of buck DC-DC converter will oscillate because of a positive feedback on the output voltage of converter. Besides that, the output voltage of converter is directly connected to integrator during idle period of converter as shown in Figure 4.7. This situation will definitely degrade the efficiency of the converter. As a result, a bigger inductor $47\ \mu\text{H}$ was selected to make the buck converter operate in the CCM even when load current goes down within the targeted load current range $10 \sim 50\ \text{mA}$. The inductance is designed based on the CCM/DCM boundary of converter as seen in the equation 2.22.

As discussed in Section 2.5.3 of Chapter 2, the dominant power consumption of DC-DC converter at the light load are the switching losses and current ripple induced conduction losses. The Switching loss is proportional to the switching frequency f_S of the DC-DC converter ($P_{SW} = CV^2 f_S$). Therefore, decreasing the

switching frequency f_s is direct and effective method to minimize the switching power consumption. In the proposed Buck converter, switching frequency f_s of converter is decreased according to the load level which is sensed by the proposed current sensing circuit depicted in Figure 4.9

Consequently, the Figure 4.8 depicted that the proposed twin cycle control fix the switching frequency of converter at the heavy load and scale down the switching frequency dedicated for maintaining power efficiency of converter at the light load.

FIGURE 4.8: the operating waveform of proposed PWM and PFM control.

4.2.3 Average current sensing circuit and Frequency divider

Either PWM or PFM control for the proposed buck converter is determined by the level of load current which is sensed by proposed current sensing circuit. Then, the switching frequency f_s of buck converter is varies by the Frequency divider

according to the level of load current differentiated by a thermometer code ADC.

The block diagram of average current sensing depicted in Figure 4.9, is an extension and improvement to prior work [32].

FIGURE 4.9: Current sensing circuit.

Figure 4.9 depicted that two parallel resistors R_{1N} and R_1 which have N:1 ratio of resistance are inserted right after the output capacitor. Because the inductor current with both ac and dc current is filtered, the current appears at the point after output capacitor is the dc load current.

The resistance of R_1 should be designed as small as possible compared to the load resistance to minimize the impact of R_1 series with R_{load} . Hence the resistance of R_1 is designed with 0.4Ω because of smallest load resistance R_{load} is 24Ω when load current is maximum designed level which is 50mA, and ratio N is set to 2.5K. The current sensing circuit make the voltage $V_1 = V_2$ and current

$I_1 = I_2$, then:

$$I_1 = I_2 \approx I_{load}/N \quad (4.12)$$

Transistors M5-M6 and M2-M3 form the current mirror lead to the current $I_{D_1} = I_{D_2}$ and $I_{D_2} = I_{D_3}$. Besides that, the gate of transistor M1 is connected to the gate of transistor M2. Hence, the current $I_{D_1} = I_{D_4}$ due to that the source voltage V_1 of M1 is also equal to the source voltage V_2 of M2 means that $V_{SG_1} = V_{SG_2}$. Therefore, the four branches of current are same that $I_{D_1} = I_{D_2} = I_{D_3} = I_{D_4} = I_1/2 = I_2/2$. And, the current $I_{sense} = I_1/2 = I_2/2$. Consequently, inserting equation $I_1 = I_2 \approx I_{load}/N$ then:

$$I_{sense} \approx I_{load}/2N \quad (4.13)$$

Finally:

$$V_{sense} \approx 10I_{load} \quad (4.14)$$

The voltage V_1 also track the voltage V_2 to maintain the voltage equally whenever the load changes. When the load increase suddenly, the voltage V_2 decrease accordingly. Then, the gate voltage of the M1 also decreased. Because of the V_{SG_1} bigger, the current I_{D_1} increase. Then, the current I_{D_2} and I_{D_3} also increase due to the current mirror M5-M6 and M2-M3. This will bring the voltage

V_2 back to equal to voltage V_1 . The sensed circuit will maintain the relation shown in equation 4.14.

FIGURE 4.10: 4-Bit Thermometer Code ADC.

FIGURE 4.11: Frequency divider.

The sensed voltage will pass through a 4 bits thermometer code ADC illustrated in Figure 4.10 to adjust the switching frequency of proposed buck converter. The switching frequency of converter will be halved in the Frequency Divider depicted in Figure 4.11: as the load current change for every 10 mA. The thermometer code changes from 0000 to 1111. Each bit chose the selection of 2x1 MUX which determine whether D flip flop is inserted. The basic clock frequency of converter is provided by a conventional ring oscillator.

4.2.4 Power Train

The power train of proposed buck converter is composited of one PMOS (MP) and one NMOS (MN) device as shown in Figure 4.3. Taking NMOS as example, the total power losses are the sum of the switching loss and conduction loss as follow:

$$P_{total\ loss} = C_{gdn} \cdot W_N \cdot V_N^2 \cdot f_S + C_{gsn} \cdot W_N \cdot V_N^2 \cdot f_S + (C_{gdn} + C_{dbn}) \cdot W_N \cdot V_{BATT}^2 \cdot f_S + \frac{I_N^2 \cdot R_{on,N}}{W_N} \quad (4.15)$$

whereby C_{gdn} , C_{gsn} , C_{dbn} refers to the respective parasitic capacitance per unit width of the device, V_{BATT} is the input voltage to the buck converter, f_s refers to the switching frequency of the power train, $R_{on,N}/W_N$ is the on-resistance per unit width, I_N refers to its RMS current and V_N is the gate voltage of the power NMOS transistor. Thus, the optimum width, $W_{opt,N}$, can be calculated when the

switching loss is equal to the conduction loss, given by:

$$W_{opt,N} = \sqrt{\frac{I_N^2 \cdot R_{on,N}}{C_{gdn} \cdot V_N^2 \cdot f_S + C_{gsn} \cdot V_N^2 \cdot f_S + (C_{gdn} + C_{dbn}) \cdot V_{BATT}^2 \cdot f_S}} \quad (4.16)$$

The optimized width for both the power NMOS and PMOS are shown in Figure 4.12 and Figure 4.13 where the graph of the switching loss intersects the conduction loss. The graph plot is based on the highest load current of 40mA and at a switching frequency of 1MHz. The aspect ratio and the on-resistance of the power transistors are shown in Table (power Mos).

FIGURE 4.12: Optimized sizing of NMOS power transistor.

The on-resistance and input parasitic capacitance in equation (optimize width) is based on the simulation results as well as the theoretical calculation of the resistance/capacitance of metal routing/contact/via and the silicon area occupied by the layout of the power train. Therefore, the layout of power transistor is vital when the optimize width is fixed.

FIGURE 4.13: Optimized sizing of PMOS power transistor.

4.3 Experiment result and conclusions

A proposed twin frequency buck DC-DC converter has been fabricated with Global Foundries $0.18\mu\text{m}$ 1P6M CMOS technology with an area of 1.3 mm^2 . The micrograph of the chip is shown in the Figure 4.14. A prototype of the proposed buck converter is also presented in Figure 4.15. Proposed work uses DIP package with 48 Leads as shown.

The performance of the proposed buck converter is measured as follow steps: firstly, the performance of our proposed PWM/PFM controller at light loading conditions. Secondly, comparison of the power efficiency between our proposed work and the conventional PWM/PFM controller. Lastly, design specification and performance comparison are summarized in Table I. The proposed PWM/PFM controller adjust the switching frequency of buck converter according the to the

FIGURE 4.14: Die Photo of the proposed buck converter.

FIGURE 4.15: Prototype of the proposed buck converter.

different load conditions. It achieves a peak efficiency of 92.7% when the buck converter operated at 250 kHz with $V_{BATT} = 2V$, $V_{OUT} = 1.25V$ and $I_{LOAD} = 30mA$, as shown in Figure 4.16. The top waveform is the cross point voltage V_x , the bottom one is the the output voltage V_{int} of integrator. The Figure 4.16 waveform proves that proposed buck converter is stabilized and achieved a high efficiency at low load as well.

FIGURE 4.16: Peak Efficiency Achieved - Waveform of V_X and V_{int} ($V_{BATT} = 2V, V_{OUT} = 1.25V$ and $I_{LOAD} = 30mA$ and $Freq = 250kHz$).

Furthermore, it is evident that our proposed controller does not enter DCM operation at light load. In contrast to many other research works/industrial products whereby the converter will enter DCM operation at light loads to reduce switching loss and thus allow a smaller inductor value to be used, a relatively larger inductor value of $47\mu H$ is chosen so as to reduce the ripple at the output voltage of the buck converter. The rationale is mentioned as previously in chapter 4. The proposed PFM control of buck converter at the DCM will cause the system unpredictable and even unstable. This is a trade-off for our PWM/PFM controller.

Figure 4.17 illustrated the power efficiency of our proposed PWM/PFM control and a conventional controller at the varying load ranges. A peak efficiency of about 92.7 % is achieved when proposed buck converter operating at 250KH with

2.0V input voltage and 30mA load current. It is shown that the efficiency of the converter is degraded as the input voltage increases. The reason is that the power consumption in converting the higher input voltage to a fixed output voltage is higher than that in converting the lower input voltage. Figure 4.18 depicted that the efficiency improvement that compares the proposed buck converter with the latest state of the art work. An improvement 4 ~ 6% on power efficiency is obtained across 10 ~ 50mA of load current. At the end, the Table 4.2 summarized the proposed specification and performance.

FIGURE 4.17: Power Efficiency of the proposed buck converter and the conventional PWM/PFM controller at different loading conditions (P - Proposed Work, C - Conventional Work).

In conclusion, the proposed buck converter achieves a peak efficiency 97.2% at the load range 10 ~ 50 mA. In addition, proposed PWM/PFM controller obtain an efficiency improvement compared to the latest research works. However, a significant interval at the cross voltage V_x shown in Figure 4.16 is observed whereby there

FIGURE 4.18: Efficiency improvement of the proposed buck converter as compared to the latest state of the art work.

are a body diode conduction loss which degrades the power efficient as discussed in Chapter 4. This is due to that a conventional fix deadtime controller is used in the proposed work. Hence, there is an ongoing current research into designing an adaptive deadtime controller to minimize the body diode conduction loss which will further improve the efficiency. Another improvement is to use the MOSFET segmentation technique as proposed in [33] can also help to further improve the power conversion efficiency.

	VLSIC [34]	JSSC [35]	JSSC [36]	This Work
Year	2008	2011	2013	2013
Tech [μ]	0.35	0.35	0.18	0.18
Input [V]	0.9~1.2	2.7~4.2	0.9~1.4	2.0~3.0
Output [V]	2.5	0.9	2.5	1.25
Peak η @ current [%]	87@80mA	89@55mA	88@40mA	92.7@30mA
External inductor [μH]	1.0	2.2	1.0	47
External Capacitor [μF]	4.7	4.7	10.0	10.0
Frequency [KHz]	670	200	800	250
Die Area [mm^2]	3.0	1.4	1.5	1.3
Power Transistors Implemented in this work				
Size	$M_N \frac{21168\mu m}{0.35\mu m}$		$M_P \frac{35672\mu m}{0.35\mu m}$	
Channel resistance [$m\Omega$]	80		95	
Bonding wire resistance [$m\Omega$]	200		200	
Total resistance [$m\Omega$]	280		295	
Total Gate capacitance [pF]	477.8		574.3	

TABLE 4.2: Comparison with state of art research works

Chapter 5

Conclusions and Recommendations

5.1 Conclusions

The power management ICs is the one of most important parts for the portable device to prolong the working time effectively. Increasing the power efficiency of power management ICs is the prime but also challenge objective. Therefore, the design challenge on the power management ICs is to minimize the power consumption on the power ICs itself. As a result, a voltage reference circuit which is an important block in the power management ICs was proposed. It consumes 180 nW at the same time that achieve a 30 *ppm*/ $^{\circ}c$ temperature dependency. The power

consumption of conventional bandgap circuit is too high to be implemented in the power management ICs of portable device which is supplied by energy harvesting sources. Those sources normally have below magnitude of micro watts. The proposed voltage reference make use of the temperature dependency of MOSFETs operating in the subthreshold region instead of the BJT in the bandgap circuit. Furthermore, the proposed voltage reference can be fabricated in normal CMOS process. Then, this voltage reference circuit is suit to be integrated in those energy harvesting supply portable device.

This thesis also discussed the DC-DC converter which is another one of very important power management ICs. A twin frequency control buck DC-DC converter achieves a peak efficiency 97.2% working with a load range from 10 ~ 50 mA was presented and fabricated. The power efficiency of the DC-DC converter degraded as the load decrease. The objective of proposed twin frequency control is to maintain the efficiency for the target load range. Therefore, the proposed twin frequency has a fixed switching frequency when buck converter at the heavy load and decrease switching frequency when buck converter at the light load. Consequently, this reduce the switching power losses which is dominant power consumption in the buck converter at the light load. The level of load is sensed by the proposed average current sensing circuit. The proposed twin cycle control method is innovated to reduce the power consumption of DC-DC converter with a wide

load range.

5.2 Future work

Although the proposed twin frequency control buck DC-DC converter achieves a peak efficiency 97.2% working with a load range from 10 mA to 50 mA, the converter still have potentials to reduce the power consumption.

5.2.1 Adaptive dead time controller

Dead-time is a period when one power transistor Switch turn off and another is starting to turn on. As discussed in section 2.5.4.2, dead-time can neither be too short nor be too long so that the power transistor non-ideal switching loss is minimized. A fixed dead-time is used in the proposed converter. However, optimize dead-time is related to the load current of converter. The proposed converter operate in wide load range, hence the optimized dead-time should be adaptive to the load current. As discussed before, none-optimized dead-time lead to the non-ideal switching happened when the diode of MOSFET switch is conducted. The dead-time controller make use of this phenomenon to adjust the dead-time until the non-ideal switch is vanished. As such, the converter efficiency can be further increased.

5.2.2 Zero current detector

A Zero current detector should also add in to the proposed converter. As discussed in section 2.5.4.2, when DC-DC converter operated in the DCM due to the low load current. A negative current may happened in the inductor when both power transistors switch turn off. This negative current brings huge power consumption especially when load current very low which caused negative current flow in inductor very long time. The proposed converter can achieve high efficiency that load current low to 10 mA. Zero current detector can make use of the current sensing circuit to prevent the negative current in the inductor. Therefore, additional zero current detector theoretically broadened the load current range for maintaining the high efficacy.

5.2.3 Extend to research on LDO

Besides that, the research on the power management ICs will extend to explore the LDO. Generally, LDO is an essential ICs right after the DC-DC converter integrated in the portable device. The DC-DC converter has a high spike output voltage due to the switching characteristic of DC-DC converter. Therefore, this high switching noise output voltage is not direct to supply the ICs in portable

device. The DC-DC converter output voltage is regulated by the LDO with reducing the spike of voltage. Another disadvantage of DC-DC converter is its bulky inductor which is not easy to squeeze into the portable device as its size shrink down dramatically. Consequently, LDO is become more and more popular power management ICs in replace of DC-DC converter.

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