Design of a variable rate low power SAR ADC with bypass window for biomedical application

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**DESIGN OF A VARIABLE RATE LOW POWER SAR ADC
WITH BYPASS WINDOW FOR BIOMEDICAL
APPLICATION**

BY

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Abstract

In recent years, there is an increasing demand for portable, wearable or implantable biomedical devices. These devices generally require extremely long battery life-time which in turn demands extremely low-power band-pass filters, low-noise amplifiers and low-power ADC. SAR ADC is typically adopted in these devices because of its higher power efficiency compared to other ADC architectures (e.g., flash ADC, pipeline ADC). Nevertheless, a big proportion of energy is still consumed by the conventional SAR ADC. Hence, extensive research is still required to further lower the power consumption.

Meanwhile, many biomedical signals vary slightly within a small range for a large portion of time. Incorporating this signal characteristic into the design, a bypass window technique that can increase the power efficiency of the SAR ADC in biomedical signal acquisition is proposed here. This technique is based on the idea that when the input signal is within a predefined range, several conversion steps for the first few significant bits are bypassed, i.e., fewer switching instances happen in the capacitive DAC and hence less power is consumed during the switching sequence. Besides, the design has a 2-stage low-power dynamic comparator and a TSPC DFF constructed phase generator, which helps to lower the overall power consumption further for our SAR ADC.

In the current project, the SAR ADC is designed and implemented in GLOBALFOUNDRIES 40nm CMOS process. The simulation results show that with sampling frequency from 0 to 2MHZ, this ADC can achieve a SNDR of 61.55dB and ENOB of 9.93bits. It can reduce 74% of the power dissipation if the bypass window function is triggered.

Table of Contents

ACKNOWLEDGEMENTS	ii
Abstract	iii
Table of Contents	iv
List of Figures	vii
List of Tables	x
List of Abbreviations	xi
1. Introduction	1
1.1 Design constraints of ADCs in biomedical application	1
1.1.1 Power constraints.....	2
1.1.2 Resolution and Sampling rate.....	2
1.2 Architecture selection	4
1.3 Contributions	5
1.4 Organization of the Report.....	6
2. ADC characteristics.....	8
2.1 ADC fundamentals.....	8
2.1.1 Resolution.....	8
2.1.2 Quantization Error	8
2.2 Static Performance	9
2.2.1 Differential Nonlinearity (DNL)	9
2.2.2 Integral Nonlinearity (INL)	9
2.3 Dynamic Performance	9
2.3.1 Signal-to-Noise Ratio (SNR).....	9
2.3.2 Spurious-Free Dynamic Range (SFDR)	10
2.3.3 Signal-to-Noise-and-Distortion Ratio (SNDR or SINAD).....	10

2.3.4	Effective Number of Bits (ENOB)	11
3.	SAR ADC Architectures	12
3.1	Conventional Binary-weighted Charge-Redistribution SAR ADC	13
3.2	Binary-weighted Capacitive Array with Attenuation Capacitors (BWA)	16
3.3	Variations on Conventional Architecture	18
3.3.1	Split Binary-Weighted Capacitive Array (SBW) or charge recycling approach	18
3.3.2	Monotonic switching method	20
3.3.3	Bypass window techniques.....	25
3.4	Summary	31
4.	The Proposed SAR Architecture-----A capacitor constructed bypass window technique.....	32
4.1	Problems with the scheme in the comparator constructed bypass window scheme	32
4.2	New proposal -----A capacitor constructed bypass-window technique	36
4.2.1	Architecture of the proposed SAR ADC	37
4.2.2	Concept of the capacitor constructed bypass-window technique	38
4.2.3	Window size determination	39
4.2.4	DAC Network Topology	40
4.2.5	Switching procedures and working flow	41
4.2.6	Behavior modeling and simulation.....	43
4.3	Summary	46
5.	Circuit design and simulation result	47
5.1	Device selection	47
5.2	DAC circuit design	48
5.2.1	Unit capacitor	48
5.2.2	DAC Layout	49
5.3	Switch design	50
5.3.1	Bootstrapped switches	51
5.3.2	Bottom plate switches.....	55

5.4	Performance of the sampling circuit	55
	Simulation result	56
5.5	Comparator	60
5.5.1	Operation	61
5.5.2	Comparator delay	63
5.5.3	Offset	63
5.5.4	Power consumption	64
5.6	SAR control logic	65
5.6.1	Asynchronous clock generation circuit	65
5.6.2	Control logic for the DACs and the error correction circuit.....	67
5.6.3	Bypass signal generation circuit.....	68
5.7	System simulation result	68
5.7.1	The functionality of the ADC	68
5.7.2	Common-mode noise immunity	70
5.7.3	Dynamic performance	71
5.7.4	Power reduction.....	73
6.	Conclusion & Future Work	76
6.1	Conclusion	76
6.2	Future work.....	76
6.2.1	Aspects for improvement	76
6.2.2	New proposal- A two-mode comparator constructed bypass window switching scheme for SAR ADC.....	77
	Bibliography	80

List of Figures

Figure 1-1 A typical biomedical device constituted by a sensor network, an Instrumental Amplifier (IA), an analog-to-digital converters (ADC) and a Digital Signal Processor (DSP)	1
Figure 1-2 Voltage and frequency ranges of EEG, ECG, EMG, and ENG signals	3
Figure 1-3 ADC architectures and their area of highest energy efficiency in the accuracy-speed space.....	4
Figure 3-1 Block diagram of a SAR ADC	13
Figure 3-2 Block diagram of a single end N-bit binary-weighted charge scaling capacitive SAR ADC	14
Figure 3-3 Block diagram of a single end N-bit binary-weighted charge scaling capacitive DAC with switches.....	14
Figure 3-4 Successive approximation algorithm.....	15
Figure 3-5 Voltage transfer curve of a 3-bit SAR ADC	16
Figure 3-6 Binary-weighted Capacitive Array with Attenuation Capacitors.....	17
Figure 3-7 b-bit split capacitor array for reduced switching energy	19
Figure 3-8 Switching energy consumption of the CBW and SBW structures normalized to CV_{ref}^2	20
Figure 3-9 (a) Conventional switching procedure and switching energy consumption (b) Monotonic switching scheme's switching procedure and switching energy consumption	22
Figure 3-10 A 10 bit differential monotonic switching scheme SAR ADC	23
Figure 3-11 Flow chart of the monotonic SAR ADC	23
Figure 3-12 Switching energy versus output code.....	24
Figure 3-13 (a) waveform of conventional switching procedure (b) waveform of monotonic switching procedure.....	25
Figure 3-14 Neural signals.....	26
Figure 3-15 (a) Conversion process of conventional and (b) Bypass window SAR ADC	28

Figure 3-16 Bypass window architecture circuit scheme	29
Figure 3-17 Power consumption of (a) DAC switching, (b) comparator, (C) SAR logic and (d) the whole ADC with 32-LSB bypass window	30
Figure 4-1(a) input voltage and V_r ($V_{com}=500mV$) (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC (c) waveform of internal clock and comparator inputs	33
Figure 4-2(a) input voltage and V_r ($V_{com}=505mV$) (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC (c) waveform of internal clock and comparator inputs	34
Figure 4-3 (a) input voltage and V_r ($V_{com}=505mV$) (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC (c) waveform of internal clock and comparator inputs	35
Figure 4-4 Architecture of the proposed ADC.....	37
Figure 4-5 Proposed switching scheme	38
Figure 4-6 Power consumption of different window size with uniformly distributed input signal	39
Figure 4-7 DAC network of the proposed 10-bit SAR ADC.....	40
Figure 4-8 Flow chart of the proposed ADC	42
Figure 4-9 High level diagram of the proposed SAR ADC	43
Figure 4-10 (a) input signal voltage ($V_{com}=500mV$) (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC (c) waveform of internal clock and comparator inputs	44
Figure 4-11 (a) input signal voltage ($V_{com}=510 mV$) (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC (c) waveform of internal clock and comparator inputs	45
Figure 5-1 Floor-plan of the DAC array (one side)	50
Figure 5-2 Schematic of the bootstrapped switch	51
Figure 5-3 Simplified schematic for the bootstrapped switch when $CLKS=0$ and $CLKB=1$	52
Figure 5-4 Simplified schematic for the bootstrapped switch when $CLKS=1$ and $CLKB=0$	53
Figure 5-5 Bootstrapped switch on-resistance as a function of the input signal.....	54
Figure 5-6 NMOS switch on-resistance as a function of the input signal.....	54
Figure 5-7 Test bench for sampling circuit	56

Figure 5-8 Simulated waveform of the voltage on DACs.....	57
Figure 5-9 Simulated 1024-point FFT spectrum at 2MS/s for SH circuit with input signal frequency of 119 kHz.....	58
Figure 5-10 Simulated 1024-point FFT spectrum at 2MS/s for SH circuit with input signal frequency of 994 kHz.....	59
Figure 5-11 Two-stage dynamic comparator	60
Figure 5-12 Output of the input gain stage of the comparator	62
Figure 5-13 Output of the comparator	62
Figure 5-14 Simulated comparator delay	63
Figure 5-15 Simulated comparator offset (500 Monte Carlo runs).....	64
Figure 5-16 Current flow through the comparator	65
Figure 5-17 Schematic and a timing diagram of the asynchronous logic	66
Figure 5-18 Control logic for the DACs and the error correction circuit	67
Figure 5-19 DEC signal generation circuit	67
Figure 5-20 Bypass signal generation circuit.....	68
Figure 5-21 Waveform in one sampling cycle when bypass window function is not activated ...	69
Figure 5-22 Waveform in one sampling cycle when bypass window function is activated	70
Figure 5-23 Simulated 1024-point FFT spectrum at 2MS/s with input frequency 994 kHz.....	72
Figure 5-24 Simulated 1024-point FFT spectrum at 2MS/s with input frequency 119 kHz.....	72
Figure 5-25 Power consumption of (a) DAC switching, (b) comparator, (c) SAR, and total block with 64-LSB bypass window	73
Figure 6-1 Flow chart of the proposed switching scheme	78
Figure 6-2 Input difference smaller than 8LSB	79
Figure 6-3 Input difference larger than 8LSB	79

List of Tables

Table 1-1 A comparison of different types of biomedical signals from human body.....	3
Table 3-1 Summary of the performance metrics of different SAR structure.....	31
Table 4-1 Output code @ different V_{com}	36
Table 4-2 Output code @ different V_{com}	46
Table 5-1 Leakage current @ $V_{ds}=1V$, $V_g=V_s=0$	48
Table 5-2 Output code @ different V_{cm} and different input scenario	71
Table 5-3 Comparison to State-of the-art works.....	75

List of Abbreviations

ADC	Analog-to-Digital Converter
CMOS	Complementary Metal-Oxide-Semiconductor CR Charge Redistribution
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DNL	Differential Nonlinearity
DFF	Dynamic Flip-Flop
ENOB	Effective-Number-of-Bits
FoM	Figure of Merit
IA	Instrumental Amplifier
INL	Integral Nonlinearity
LSB	Least Significant Bit
MSB	Maximum Significant Bit
MDAC	Multiplying Digital-to-Analog Converter
OpAmp	Operational Amplifier
RMS	Root Mean Square
SAR	Successive Approximation Register
SBW	Split Binary-Weighted Capacitive Array
SNDR	Signal to Noise and Distortion Ratio
SINAD	Signal to Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SFDR	Spurious-Free Dynamic Range
TSPC	True Single Phase Clocking

1. Introduction

There is a sharp increase in the demand for portable, wearable or implantable biomedical devices in recent years. These devices typically consist of many sub-blocks which are used for processing the biomedical signals acquired from human body. Fig 1-1 illustrates a typical structure of biomedical device [1].

Figure 1-1 A typical biomedical device constituted by a sensor network, an Instrumental Amplifier (IA), an Analog-to-Digital Converters (ADC) and a Digital Signal Processor (DSP)

As seen from Fig 1-1, a key building block in such systems is ADC. It is used to acquire biomedical signals, and then converting them from the analog to digital domain for signal processing. As such, the requirements for these biomedical devices could impose constraints on the design of ADCs in such systems. The following sections will discuss the different design constraints and their impacts on the selection of architecture used.

1.1 Design constraints of ADCs in biomedical application

There are mainly three design constraints on the ADC used in biomedical system: power consumption, resolution and speed. Detailed discussion on these constraints is presented in the following sub-sections.

1.1.1 Power constraints

Implantable biomedical devices are typically powered by small batteries and required to remain functional for an extremely long time, for example, 10 years. Thus, an extremely low power ADC is crucial since it helps to extend the lifetime of those valuable biomedical devices.

1.1.2 Resolution and Sampling rate

Biomedical signals normally have different characteristics [2]-[4], with the amplitude ranging from the order of tens of μV to tens of mV and the frequencies spanning from DC to a few kHz [5], [6]. Table 1.1 lists the common biomedical signals and their characteristics. These signals are also compared in the voltage-frequency space in Fig 1-2.

As shown in Fig 1-2, the bandwidth of different kinds of biomedical signals varies. In order to meet all the applications, the maximum sampling rate must satisfy the Nyquist rate requirement for the highest frequency application. However, power consumption scales with frequency in any digital or mixed-signal system. Therefore, it is desirable to reduce the sampling rate for low bandwidth applications. [1]

As seen from Table 1.1, biomedical signals are slow-varying signals, with frequency up to tens of kHz [6]. A typical sampling speed for neural signal is 1-MS/s [9], which is also set to be the target sampling frequency in this project. This target is adequate for biomedical applications, even for the neural recording application [9]. However, all the simulations are performed up to 2-MS/s, to cater for design margin after testing.

In order to lower power consumption for low signal bandwidth application, asynchronous clock architecture is adopted in our design. This architecture would enable us to lower the sampling frequency requirement and thus save power.

Another design consideration is the resolution of the ADC. Obviously, the selected resolution should be high enough to provide an adequate Signal-to-noise and distortion ratio (SNDR) [1]. A modest resolution of 8 to 10-bits would be enough for ADCs in most biomedical applications [7], [8].

Figure 1-2 Voltage and frequency ranges of EEG, ECG, EMG, and ENG signals

Table 1-1 A comparison of different types of biomedical signals from human body

Biomedical signals	Location	Amplitude	Bandwidth
ENG	Stimulus over a nerve	3-10 μ V	1 - 10 KHz
EMG	Skeletal muscle	1-10 mV	1 Hz - 3 KHz
ECG	Heart	0.1-1 mV	0.05 - 100 Hz
EEG	Brain	10- 100 μ V	0.5 -100 Hz

1.2 Architecture selection

As discussed in section 1.1, the design requirement of ADC for biomedical application is low power, low speed (less than 2MS/s) [16] and 10-bits resolution with variable sampling rate. Since such a resolution and speed is not difficult to realize, power efficiency could be of critical importance in the selection of proper ADC architecture [10].

Figure 1-3 ADC architectures and their area of highest energy efficiency in the accuracy-speed space

Fig 1-3 shows ADC architectures and their area of highest energy efficiency in the accuracy-speed space. As seen from Fig 1-3, the flash and time-interleaved ADCs are usually considered for high-speed and low-resolution architectures. Pipelined ADCs can be used in high-speed and medium-to-high resolution applications. However, one operational amplifier (OpAmp) is needed in each pipeline stage and the number of stages is usually equal to the resolution. These OpAmps that are working in closed-loop to form the multiplying digital-to-analog converter (MDAC) must have high gain and wide bandwidth. As a result,

the power consumption is large. The oversampling ADC, algorithmic ADC and integrating ADC also have one or more OpAmps, therefore, they are also not suitable architectures for low-power ADC design. On the other hand, the Successive Approximation Register (SAR) ADC can be realized by a capacitive array, a dynamic latched comparator and some digital logics. The simple structure and elimination of static current make SAR ADC a very popular architecture for power constraint and low-speed applications [10]. Some of the lowest FOM ADCs using SAR architecture in the low to moderate resolution and sample rate space has been reported recently, such as those reported in [16], [31] and [33], which will be summarized later in Table 5-3.

1.3 Contributions

The promising prospect of implantable biomedical device has already drawn extensive research interest in the field of low power SAR ADC design, pushing its power efficiency to be higher and higher[15], [16], [22]. Most of these works focus on the optimization of most power-hungry element in SAR ADC, the DAC capacitors array, at the cost of some other minor penalties [11]-[15].

However, only a few works incorporates the spike like characteristic of biomedical signal in the design of ADC. In other words, during most of the period, the bio-signal is quiet while the ADC is running regularly, wasting a great amount of energy. Guan-Ying Huang [16] noticed this phenomenon; he constructed a bypassing window by using two more comparators, an external reference, a few more gates and four full adders [16]. When the input signal is very small and within the window, some of the conversion steps will be skipped. Less conversion steps means less power consumption and higher power efficiency.

Although this idea is really fascinating, there is one big problem. It introduces asymmetry to the differential structure and breaks the common-mode noise immunity, as will be shown in Chapter 5, Section 1. This means that the common-mode noise will be coupled into such system and the accuracy of the biomedical signal acquiring system will deteriorate greatly.

The main contribution of the current work in this report is that a capacitor constructed, single-bypass-window technique is proposed and implemented in GLOBALFOUNDRIES 40nm CMOS process. This new architecture maintains the ability of bypassing some conversion steps when the input signal is within a predefined region and has a symmetrical structure. Simulation results show that it has the same ability of common-mode noise rejection as the conventional differential SAR ADC. The new structure can also reduce 74% of the overall power dissipation when the bypass window function is activated.

1.4 Organization of the Report

This report is organized into six chapters.

Chapter 1 briefly introduces the design constraints, the objective and the contribution of the work.

Chapter 2 explains some of the important performance metrics of ADC before discussing the ADC structure.

Chapter 3 reviews the fundamentals of Charge-Redistribution (CR) SAR ADC architectures. The conventional binary-weighted switching scheme is presented and analyzed. In addition, several variations of the CR SAR ADC that can reduce the switching energy are chosen to be discussed in detail.

Chapter 4 first analyses the problem in G.Y. Huang's comparator-constructed bypass window scheme. Then, a new capacitor-constructed bypass window scheme is proposed and discussed in detail. A behavior model is built to verify the effectiveness of the proposed architecture.

Chapter 5 covers the circuit level implementation of a 10-bit SAR ADC based on the proposed switching scheme. Circuits of the Sample-and-Hold switch, comparator and SAR logic are presented and discussed. The dynamic performance metrics and power saving are simulated and presented.

Chapter 6 concludes the current work and discusses the potential future work.

2. ADC characteristics

The fundamentals of ADCs are first defined in section 2.1. This is then followed by the performance metrics of ADCs, from static and dynamic perspective in section 2.2 and 2.3, respectively.

2.1 ADC fundamentals

Some key performance indicators are defined here, which will be used to characterize the ADC designed.

2.1.1 Resolution

The resolution of a converter usually refers to the number of digital input or output bits. It is the number of distinct analog levels corresponding to the different digital words [17].

2.1.2 Quantization Error

Quantization error, Q_e , is the difference between the actual analog input and the value of the converted output (staircase) given in voltage [18]. It is calculated as

$$Q_e = V_{in} - V_{staircase} \quad (2.1)$$

where V_{in} is the input signal and $V_{staircase}$ is given by

$$V_{staircase} = D * \frac{V_{ref}}{2^N} \quad (2.2)$$

where D is the converted digital code of V_{in} , N is the resolution of the ADC and V_{ref} is the reference voltage of the ADC.

2.2 Static Performance

Static characteristics including Differential Nonlinearity and Integral Nonlinearity are defined in this section [18].

2.2.1 Differential Nonlinearity (DNL)

DNL is the difference between the actual code width of a non-ideal converter and the ideal case [18].

2.2.2 Integral Nonlinearity (INL)

INL is a term describing the maximum deviation between the ideal output of an ADC and the actual output level [18].

2.3 Dynamic Performance

Dynamic characteristics may not be used in all ADC characterization, hence only some related dynamic indicators that will be used for the ADC designed in this project are discussed in this section.

2.3.1 Signal-to-Noise Ratio (SNR)

Signal to Noise ratio (SNR) is the ratio of the input signal power over the total noise power [19].

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (2.3)$$

If it is assumed that $V_{in} = V_{ref} * \sin \omega t$, then the input signal power is

$$P_S = \left(\frac{V_{ref}}{2\sqrt{2}} \right)^2 = \left(\frac{2^N V_{LSB}}{2\sqrt{2}} \right)^2 \quad (2.4)$$

where V_{LSB} is the value of 1 LSB in volt [18] and V_{ref} is the reference voltage of the ADC. The value of the noise power for an ideal data converter will be equivalent to the power of Quantization error [18]

$$P_N = Q_{e,\text{RMS}}^2 = \frac{1}{V_{\text{LSB}}} \int_{-0.5V_{\text{LSB}}}^{0.5V_{\text{LSB}}} V_{\text{LSB}}^2 dV_{\text{LSB}} = \left(\frac{V_{\text{LSB}}}{\sqrt{12}}\right)^2 \quad (2.5)$$

By inserting P_S and P_N into Equation 2.3, SNR of an ideal ADC is expressed as below:

$$\text{SNR} = 20 \log_{10} \frac{2^N V_{\text{LSB}}}{\frac{2\sqrt{2}}{\sqrt{12}}} = 6.02N + 1.76 \quad (2.6)$$

2.3.2 Spurious-Free Dynamic Range (SFDR)

SFDR is defined as the ratio of the RMS value of input signal to the RMS value of the next largest harmonic distortion tone (which is referred as “spurious”). SFDR is presented mathematically in Equation 2.7 [19].

$$\text{SFDR} = 20 \log_{10} \frac{V_{\text{ref}}}{V_{\text{Spurious}}} \quad (2.7)$$

2.3.3 Signal-to-Noise-and-Distortion Ratio (SNDR or SINAD)

SNDR, or SINAD, is defined as the ratio of the input signal power over the sum of the total noise power and harmonic components power. Equation 2.8 indicates the SNDR mathematically

$$\text{SNDR} = 10 \log_{10} \frac{P_S}{P_N + P_H} \quad (2.8)$$

where P_S and P_N are indicated in Equation 2.4 and 2.5, respectively. P_H is the sum of the harmonic components power.

2.3.4 Effective Number of Bits (ENOB)

ENOB is obtained from SNDR. ENOB is commonly used instead of SNDR, since it presents SNDR in the number of bits. ENOB is achieved using Equation 2.9.

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \quad (2.9)$$

3. SAR ADC Architectures

As the name implies, SAR ADC converts analog signal to digital code via binary successive approximation algorithm. This algorithm determines each output bit sequentially from the Most-Significant-Bit (MSB) to the Least-Significant-Bit (LSB) step by step. It is a popular architecture selection for medium resolution and medium speed applications since SAR ADC has the advantage of low power consumption.

A typical SAR ADC is made up mainly of the following four sub-circuits:

1. Sample-Hold (S/H) circuit which discretizes analog input voltage in the time domain.
2. Digital-to-Analog Converter (DAC) that internally generates a reference voltage for comparison. The voltage is an equivalent of the digital output of SAR ADC and is supplied to the comparator for comparison with V_{in} .
3. Comparator that compares V_{in} to the output of internal DAC and supply its comparison result to SAR register
4. A Successive-Approximation Register (SAR) supplies an approximate digital code of V_{in} to DAC

A simple block diagram of a basic SAR ADC is illustrated in Fig 3-1 and other variations will be discussed in detail in the following sections.

Figure 3-1 Block diagram of a SAR ADC

3.1 Conventional Binary-weighted Charge-Redistribution SAR ADC

Although there are many variations for implementing SAR architecture, charge-redistribution SAR ADC is one of the most common implementations. It uses a charge scaling capacitive DAC which is composed of an array of binary-weighted capacitors. The capacitive DAC not only provides a reference voltage for comparator as aforementioned, it also serves the sample and hold function, i.e., sampling and holding the charges acquired directly from the input voltage source. Thus, a specialized sample and hold circuit is eliminated, achieving a reduction on both area and power consumption. A simple single-ended N-bit charge scaling capacitive ADC and its sub-DAC are illustrated in Fig 3-2 and Fig 3-3 respectively.

Figure 3-2 Block diagram of a single end N-bit binary-weighted charge scaling capacitive SAR ADC

Figure 3-3 Block diagram of a single end N-bit binary-weighted charge scaling capacitive DAC with switches

As illustrated in Fig 3-2, the continuous input signal V_{in} is first sampled onto the bottom plates of the DAC while the top plates of all the capacitors are attached to V_{mid} in the sampling phase. Then, when it comes to conversion phases, the sampling switch is opened, leaving the top plate floating. The bottom plates of the capacitors are switched to either V_{ref} or ground (GND) according to the successive approximation algorithm. Since the top plate of

the capacitor is floating, the voltage on the top plate is then calculated as shown in Equation 3.1, using charge conservation law.

$$V_{DAC} = V_{mid} - V_{in} + (B_0 + 2B_1 + 2^2B_2 \dots + 2^{N-1}B_{N-1}) * \frac{V_{ref}}{2^N} \quad (3.1)$$

This voltage, V_{DAC} , will then successively converge towards V_{mid} and by comparing with V_{mid} , to determine each digital output bits. Fig 3-4 illustrates the flow chart of an N-bits SAR searching algorithm, controlling how the V_{DAC} converge to V_{mid} while determining the digital output code at the same time. In Fig 3-5, the voltage transfer curve of V_{DAC} of a 3-bit SAR ADC is displayed.

Figure 3-4 Successive approximation algorithm

Figure 3-5 Voltage transfer curve of a 3-bit SAR ADC

3.2 Binary-weighted Capacitive Array with Attenuation

Capacitors (BWA)

For the conventional binary-weighted charge-redistribution SAR ADC, the total capacitance and the size of the capacitors increases exponentially with the ADC resolution, as depicted in the Fig 3-3. Equation 3.2 illustrates the relationship between C_{total} and the resolution of the ADC

$$C_{\text{total}} = C_0 + C_0 + 2C_0 + 2^2C_0 + \dots + 2^{N-1}C_0 = 2^N C_0 \quad (3.2)$$

N is the resolution of the ADC and C_0 is the unit capacitance.

However, the total switching energy of the DAC capacitor array is proportional to the total capacitance of the DAC. Equation 3.3 from [21] illustrates this relationship and is listed below:

$$P_{\text{DAC}} \approx \frac{f_{\text{clk}} f_{\text{C}_{\text{total}}}}{N+1} \times \left\{ \left(\frac{5}{6} - 2^{-N} - \frac{1}{3} \times 2^{-2N} \right) V_{\text{ref}}^2 - \frac{1}{2} V_{\text{in}}^2 - 2^{-N} V_{\text{in}} V_{\text{ref}} \right\} \quad (3.3)$$

As seen from equation 3.2 and 3.3, the higher the resolution is, the larger the total capacitance and hence, consumes more power. Furthermore, larger capacitance will increase the R-C time constant which will impose a speed limit on the SAR ADCs [20]. To solve this problem, an attenuating capacitor is employed in the conventional binary-weighted capacitor array. This attenuating capacitor splits the array into two sub-capacitor array, one of them has k bits while the other has $m=N-k$ bits, as depicted in Fig 3-6 [21].

Figure 3-6 Binary-weighted Capacitive Array with Attenuation Capacitors

As seen from Fig 3-6, this new structure has a similar switching algorithm as the conventional charge redistribution SAR ADC while the total capacitance is 2^m times smaller than the conventional structure. Equations 3.4, 3.5 and 3.6 display the total capacitance of k array, m array and the attenuating capacitor, respectively.

$$C_{k_{\text{total}}} = \sum_{i=1}^k C_i = (2^k - 1)C_0 \quad (3.4)$$

$$C_{m_{\text{total}}} = C_0 + \sum_{i=k+1}^N C_i = (2^m - 1)C_0 \quad (3.5)$$

$$C_A = \frac{2^m}{(2^m - 1)} C_0 \quad (3.6)$$

However, there is some penalty for this solution. The bridge capacitor C_A is only a fraction of the unit capacitor, which cause poor matching with other capacitors. In addition, parasitic capacitance of the attenuating capacitor introduces mismatch between the LSB array and the MSB array, resulting in bad linearity and INL/DNL performance [20]. A detailed analysis is shown in [20] that if the unit capacitance is the same, the standard deviation of INL is $2N/4$ times larger than conventional SAR ADC. In order to get the same INL/DNL as the conventional structure, a much larger unit capacitor would be used, resulting in much higher power consumption [20].

3.3 Variations on Conventional Architecture

The aforementioned two structures are two basic structures popularly used in the SAR ADC. However, to further reduce the area and increase power efficiency, other small variations have been presented in the last few years.

3.3.1 Split Binary-Weighted Capacitive Array (SBW) or charge recycling approach

The primary power hungry elements in a SAR converter are the SAR logic and DAC. The conventional switching method is efficient when charging the capacitor array during the ‘up transition’. However, it is highly inefficient in the ‘down transition’, throwing away the charges that were stored on the array. The “up” transition here refers to the charging of the

next biggest capacitor to V_{ref} when the sampled input signal is larger than the DAC output in the previous clock cycle. The “down” transition means when the sampled input voltage is less than the DAC output voltage in previous clock cycle, the larger capacitor which was connected to V_{ref} in the previous clock is now discharged to ground and the next largest capacitor is now connected to V_{ref} .

The charge-recycling switching algorithm [22] [23] avoids discharging the larger capacitor to ground in a “down” transition, therefore, less energy is dissipated. The schematic b-bit capacitive DAC with the charge-recycle switching algorithm is shown in Fig 3-7 [22]. The total capacitance is $2^b C_0$, which is the same as that of the conventional switching algorithm. The MSB capacitor, which is the largest capacitor in the conventional DAC, is split into a binary-weighted sub-array. Therefore, the MSB array and the remaining LSB array are identical.

Figure 3-7 b-bit split capacitor array for reduced switching energy

Figure 3-8 Switching energy consumption of the CBW and SBW structures normalized to CV_{ref}^2

Simulation result of a 10-bit charge-recycle SAR-ADC switching energy is illustrated in Fig 3.8 [24]. The average switching energy is $426.2CV_{ref}^2$. The average switching energy saving is 37.5% compared with the conventional switching algorithm [22].

3.3.2 Monotonic switching method

Although SBW scheme is very effective in reducing the switching energy dissipation of the DAC array, it doubles the number of switches [25]. This would complicate the design of SAR logic and increase the power consumption of digital parts. In [25], C.C. Liu proposes a monotonic switching approach without splitting the capacitor array and adding more switches. Actually, it reduces the total capacitance by 50% and can reduce the switching power consumption by 81%.

3.3.2.1 Design Concept

Fig 3-9a illustrates the switching procedures and switching energy dissipation of a 3-bit conventional differential SAR ADC [25]. The conventional structure samples the input signal

on the bottom plates of the DAC capacitor array and the top plates are reset to V_{cm} , the common-mode voltage. In the conversion phase, the bottom plate of the largest capacitor is switched to V_{ref} while the other capacitors are switched to ground. The top plates of all the capacitors floats, creating a voltage $V_{DACp}=V_{cm}-V_{ip}+V_{ref}/2$ on the positive side and a voltage $V_{DACn}=V_{cm}-V_{in}+V_{ref}/2$. If V_{DACp} is higher than V_{DACn} , the MSB B_2 is 0. Otherwise, B_2 is one. This trial-and-error process will repeat 3-rounds, until it get the LSB B_0 . Meanwhile, the switches that connect the bottom plates of the DAC capacitors will be switched to V_{ref} or ground accordingly, consuming a great deal of power, as shown in Fig 3-9a.

However, C.C. Liu's scheme samples the input signals on the top plates of capacitors and then directly perform the first comparison after sampling, without switching any capacitors. This step consumes no power in this scheme while conventional scheme dissipates $4CV_{ref}^2$. Other steps for C.C. Liu's scheme also exhibit higher energy efficiency as shown in Fig 3-9b [25].

Another advantage for the monotonic switching scheme is that it can reduce the capacitance by 50%, as also shown in Fig 3-9a and Fig3-9b.

Figure 3-9 (a) Conventional switching procedure and switching energy consumption
(b) Monotonic switching scheme's switching procedure and switching energy consumption

3.3.2.2 Architecture and Working flow

Substrate noise, supply noise and other common-mode noise source will strongly affect the accuracy of the ADC. To achieve 10-bit resolution, a fully differential architecture should be implemented. The sample and hold (SH) switches directly connect the top plate of the DAC capacitor array and the input signals, as shown in Fig 3-10 [25]. The SH switches are implemented by Bootstrapped switches which have a better linearity [25].

Figure 3-10 A 10 bit differential monotonic switching scheme SAR ADC

Figure 3-11 Flow chart of the monotonic SAR ADC

As seen in Fig 3-10 and Fig 3-11, the top plates of the DAC array will be charged to V_{ip} and V_{in} at the sampling phase. Then, the SH switches will be switched off, leaving the top plates floating. The comparator will compare the voltages on the top plates, V_+ and V_- directly, without switching any capacitors. The output code will switch the next capacitors to V_{ref} or ground, changing V_+ and V_- accordingly. The next comparison starts when V_+ and V_- get stable. This process goes for a few rounds until the last bit has been determined [25].

3.3.2.3 Advantages

For a 10-bit conventional SAR ADC case, the average switching energy is $1365.3 \text{ CV}_{\text{ref}}^2$ if the digital output code has an equal probability. In comparison, the 10-bit monotonic switching scheme only dissipates $255.5 \text{ CV}_{\text{ref}}^2$, resulting in an 81% reduction in switching energy consumption [25]. Fig 3-12 [25] compares the switching energy of conventional, split capacitor [22], energy-saving [27] and the monotonic switching method versus the output code. The best power efficiency is achieved by the monotonic switching scheme.

Figure 3-12 Switching energy versus output code

3.3.2.4 Disadvantages

However, the penalty of the monotonic switching scheme is that the common-mode voltage on the comparator varies in the conversion phase, as shown in Fig 3-13b. This will cause variation in the comparator offset and also degradation in ADC linearity [25]. The

conventional SAR ADC will not suffer from this problem since its common-mode voltage is kept stable at V_{cm} , as shown in Fig 3-13a.

Figure 3-13 (a) waveform of conventional switching procedure
(b) waveform of monotonic switching procedure

3.3.3 Bypass window techniques

As aforementioned, all of the previous work focuses on the target of lowering the power consumption of the DAC capacitor array and achieves improvement of energy efficiency in every conversion. Compared to the conventional switching scheme, the monotonic [25] and input range prediction [26] have reduced switching energy by 81% and 90% respectively. However, for a modern SAR ADC, the DAC switching energy consumption only accounts for around 30% of the total power consumption [16]. The rest is consumed by digital SAR logic and comparator. Thus, further reduction of DAC switching energy could not have

significant effect on the total energy efficiency of the SAR ADC. Further research should place emphasis on the reduction of the digital component and comparator power consumption in general. One way is to lower the power dissipation of each component; the other is to lower the activities in conversion phase.

Many biomedical signals fluctuate within a very small range for a large portion of its period, as shown in Fig 3-14 which takes neural signal as an example [16]. For the previously mentioned structures [24]-[26], the ADC will not take this signal characteristic into account and work as normal. If an ADC can determine the magnitude of the input signal before starting conversion and change its switching sequences accordingly, then it is possible to reduce its activity when the input signal is located in a specified range. This means an overall power reduction for the whole ADC, rather than only the DAC sub-block.

Figure 3-14 Neural signals

In [16], G.Y. Huang proposes a bypass-window technique which depends on the input signal magnitude to determine its switching sequences. This scheme reduces the power consumption, for a specific kind of neural signals, by 46% [16].

3.3.3.1 Design concept

For a conventional SAR ADC, it always starts conversion from MSB down to LSB, regardless of the magnitude of the input signal. As seen from Fig 3-15(a) [16], when a very small signal is feed into the ADC, the voltages on the top plates of the DAC array, V_{DACP} and V_{DACN} , first diverges in phase 2. Then, after a few conversion steps, the two voltages, V_{DACP} and V_{DACN} , finally converges again. This conventional trial-and-error process is power inefficient, triggering unnecessary capacitor switching and comparator comparison. The consequence is that a great deal of power is wasted.

Fig 3-15(b) [16] illustrates how the bypass window technique works. When the input signal is located within a predefined small range, the ADC will bypass phase2 to phase5. No comparison and no capacitor switching happen in these skipped conversion steps. Thus, no power is dissipated and hence, power efficiency is improved.

Figure 3-15 (a) Conversion process of conventional and
(b) Bypass window SAR ADC

3.3.3.2 Architecture

A schematic view of the bypass window architecture for a 10 bit SAR ADC is displayed in Fig 3-16 [16]. Compared to the conventional structure, this bypass window scheme adds two coarse comparators and an external window reference voltage to construct the bypass window function. The SAR control logic is also slightly adapted, adding four full adders and a few other gates [16]. The DAC capacitor arrays, working in a similar way as the monotonic scheme, are split to two parts to overcome the common-mode voltage variation problem.

3.3.3.3 Advantages

Fig 3-17(a) compares the switching energy for an ADC with and without bypass window function versus digital output code. When the input codes are between 480 to 543, a reduction of 90% in switching energy is achieved. Fig 3-17(b) and Fig 3-17(c) compares the comparator and the digital component versus digital output code respectively. Fig 3-17(d) displays the overall power saving of the ADC with and without bypass window versus output code [16].

Figure 3-17 Power consumption of (a) DAC switching, (b) comparator, (c) SAR logic and (d) the whole ADC with 32-LSB bypass window

3.4 Summary

In this chapter, we have illustrated the fundamentals and have compared the advantages and disadvantages of different SAR architectures. The summary of the performance metrics are shown in Table 3-1.

Table 3-1 Summary of the performance metrics of different SAR structure

Architectures	Disadvantages	Advantages
Conventional	Simple structure	Large capacitance, Large power consumption
BWA	Poor matching	Smaller capacitance,
SBW	Number of switches doubles,	Switching energy dissipation is reduced
Monotonic	Comparator offset variation	Capacitance reduced by 50%, Power consumption reduced by 81%
Bypass window	Bad common-mode noise immunity	Power consumption is reduced when input signal is within a predefined window

4. The Proposed SAR Architecture-----A capacitor constructed bypass window technique

This chapter first discusses the problem in the comparator constructed bypass window scheme [16], followed by a proposal to counteract the problem. In Section 4.1, the problem in [16] is analyzed and then macro Verilog model is built to verify the analysis. Section 4.2 proposes the new scheme which can achieve bypass window function while maintaining symmetry for the differential SAR ADC. Detailed working flow for the proposed ADC is also presented and behavior models are also built to verify the effectiveness of the scheme in this section.

4.1 Problems with the scheme in the comparator constructed bypass window scheme

The bypass window technique proposed in [16] that use multiple comparators exhibits great power saving when the input signal is within the predefined range. Great potential has been demonstrated in the field of biomedical application since most biophysical signal varies within a small range in magnitude for a large portion of time [16]. However, G.Y. Huang's technique is vulnerable to the common mode noise, which would introduce error in signal acquisition. Fig 4-1, Fig 4-2 and Fig 4-3 illustrate a scenario that potentially happens in real system and is simulated in Cadence Virtuoso. When the differential input voltage $V_{ip}=535\text{mV}$, $V_{in}=465\text{mV}$ and $V_r=468.75\text{mV}$ (corresponding window size of $1/32V_{ref}$ and common voltage $V_{com}=500\text{mV}$), the output code of G.Y. Huang's scheme is the same as an ideal differential 10-bit ADC (1000100011), as depicted in Fig 4-1(b). Since $V_{ip} > V_r$, $V_{in} < V_r$, the bypass function will not be triggered, as shown in Fig 4-1(c).

Figure 4-1(a) input voltage and V_r ($V_{com}=500mV$)
(b) ADC output code after being transferred to voltage by an ideal 10-bit DAC
(c) waveform of internal clock and comparator inputs

Nevertheless, if the common-mode voltage of the input signal drifts 5mV to 505mV because of ground noise or aging effects on the previous stages, it will trigger the bypassing window function and introduce a 4mV error, as shown in Fig 4-2(b) and Fig 4-2(c).

Figure 4-2(a) input voltage and V_r ($V_{com}=505mV$)
(b) ADC output code after being transferred to voltage by an ideal 10-bit DAC
(c) waveform of internal clock and comparator inputs

Then, if V_r is increase by 5mV, from 468.75mV to 473,75mV, G.Y. Huang's scheme can get the same result as the ideal differential ADC again. Fig 4-3 exhibits this phenomenon in detail.

Figure 4-3 (a) input voltage and V_r ($V_{com}=505mV$)
 (b) ADC output code after being transferred to voltage by an ideal 10-bit DAC
 (c) waveform of internal clock and comparator inputs

Table 4-1 summarizes the simulation results, showing that G.Y. Huang's scheme damages the common-mode noise immunity and introduces an error into the ADC, as shown in the scenario 2. Only after the voltage of external reference, V_r , is adjusted according to the variation in the common-mode voltage of the differential input signals, the ADC in [16] can output the correct digital code. However, noise is unpredictable. Hence, it is impossible to vary the voltage of the external reference according to the noise in reality.

Table 4-1 Output code @ different V_{com}

	$V_{ip}(mV)$	$V_{in}(mV)$	$V_{com}(mV)$	$V_r(mV)$	G.Y. Huang' result(mV)	Ideal ADC(mV)
1	535	465	500	468.75	534.18	534.18
2	540	470	505	468.75	530.27	534.18
3	540	470	505	473.75	534.18	534.18
4	530	470	500	468.75	529.3	529.3
5	540	480	510	478.75	529.3	529.3

4.2 New proposal -----A capacitor constructed bypass-window technique

Noise is unavoidable in real system and would be coupled into the input signal through numerous ways. The common mode noise in band is unable to be filtered and will cause error in the data acquiring system proposed by [16], as seen in Table 4-1. This makes the proposed

scheme in [16] problematic when implemented in a practical system. In this proposal, the intrinsic DAC capacitor array is used to construct the bypass window function, while the common-mode noise rejection ability is still maintained. The new proposal also does not need external voltage references or any other additional power hungry comparators. Only a few dynamic flip-flops and a few digital gates are added, which would gain more benefits from technology evolution. In this section, the architecture, concept, working flow and the behavior simulation result of the proposed ADC will be presented.

4.2.1 Architecture of the proposed SAR ADC

As shown in Fig 4-4, the proposed architecture, similar to the conventional differential SAR architecture, also contains two sampling switches, two capacitive DAC networks, a comparator, and an asynchronous SAR logic. However, a digital error correction (DEC) circuit is added. This block is added to reconstruct and correct the output of the customized SAR logic before producing the valid result. The sampling switches and DAC capacitive array in [16] are adopted here to improve the linearity of the ADC except that the DAC capacitive arrays is further split to realize the bypass-window function.

Figure 4-4 Architecture of the proposed ADC

4.2.2 Concept of the capacitor constructed bypass-window technique

Figure 4-5 Proposed switching scheme

Fig 4-5 illustrates a 3-bit conceptual example of the proposed capacitor-constructed bypass-window scheme. The proposed scheme differs from the monotonic switching scheme [14] in that after the 'sign' is determined, it bypasses the first few comparisons in order to

reduce power consumption if the input signal $V_{\text{diff}} = |V_{\text{ip}} - V_{\text{in}}| < \frac{1}{16} V_{\text{ref}}$. One more comparison step is added and the largest capacitor, $2C$, is divided into two parts, $\frac{1}{8}C$ and $\frac{15}{8}C$, in order to realize the bypass window function.

4.2.3 Window size determination

Fig 4-6 shows the power reduction of different window size with uniformly distributed input signal [16]. As shown in this figure, the 128-LSB window size saves most of the power.

Figure 4-6 Power consumption of different window size with uniformly distributed input signal

However, for the spike like biomedical signal illustrated in Fig 3-14, of which magnitude is very small most of the time, a narrower bypass window is better for power reduction. For example, if the signal level of the input is within -24dBFS most of the time, a 64-LSB bypass window size is more suitable than 128-LSB for power saving. Therefore, the 64-LSB window size is used in this project, to first evaluate the effectiveness of the proposed capacitor constructed bypass window scheme. Thereafter, the concept can be easily expanded to other window size, to cater for other types of biomedical signals.

4.2.4 DAC Network Topology

The DAC capacitor array structure in [16] helps to reduce the common-mode voltage variation on the comparator and thus, improves the linearity of the ADC. Hence, it is adopted here with slight modification. The evenly divided capacitors, C_{9pa} and C_{9pb} , are further split into $C_{9pa1} = C_{9pb1} = \frac{1}{32}C_{total}$ and $C_{9pa2} = C_{9pb2} = \frac{7}{32}C_{total}$ in the proposed structure, as shown in Fig 4-7. Thus, a 64-LSB size bypass-window is realized.

$$C_{ia}=C_{ib}, i=6\sim 8; C_{j+1}=2C_j, j=6\sim 8; C_{k+1}=2C_k, k=1\sim 4; C_{6a}=C_5, C_1=C_0; \\ C_{9a1}=C_{9b1}=C_5, C_{9a2}=C_{9b2}=7C_5; C_{9a1}+C_{9a2}=C_{9a}=C_{9b}=C_{9b1}+C_{9b2}$$

Figure 4-7 DAC network of the proposed 10-bit SAR ADC

4.2.5 Switching procedures and working flow

Fig 4-8 depicts the working flow of the proposed SAR ADC. As seen from the diagram, the capacitive DAC samples the input signal via the bootstrapped switches in the sampling phase S [14]. At the same time, the bottom plates of capacitors, $C_{9b1,2}$, $C_{8b} \sim C_{6b}$ and $C_5 \sim C_1$, switch to GND while the bottom plates of capacitors, $C_{9a1,2}$ and $C_{8a} \sim C_{6a}$, switch to V_{ref} . The voltages on the top plates of the DAC networks are $V_{ip,S} = V_{ip}$, $V_{in,S} = V_{in}$. In the conversion phase, the proposed SAR ADC adopts a 64-LSB bypass window, which determine whether $V_{diff} = |V_{ip} - V_{in}| < \frac{1}{16} V_{ref}$ in the first two comparisons.

In phase 0, the comparator directly performs the first comparison to determine the ‘sign’ after sampling phase S. Since the operation of the differential SAR ADC is complementary, only the positive-end of operation is described, as shown in Fig 4. If $V_{ip,0} - V_{in,0} = V_{ip,S} - V_{in,S} > 0$, B_{10} is set to 1. Meanwhile, the bottom plate of C_{9pa1} switches to GND while the bottom plate of C_{9na1} switches to V_{ref} . Correspondingly, the voltage on the top plates of the negative and positive capacitor arrays changes accordingly, as shown in (4.1) and (4.2):

$$V_{ip,1} = V_{ip,0} - \frac{1}{32} V_{ref} \quad (4.1)$$

$$V_{in,1} = V_{in,0} + \frac{1}{32} V_{ref} \quad (4.2)$$

In phase 1, the comparator will perform the second comparison and determine whether $V_{ip,1} - V_{in,1} = V_{ip} - V_{in} - \frac{1}{16} V_{ref} > 0$. If $V_{ip} - V_{in} > \frac{1}{16} V_{ref}$, B_9 is set to be 1. If B_{10} and B_9 are 1, the ADC will then determine whether $V_{ip,2} - V_{in,2} = V_{ip} - V_{in} - \frac{1}{2} V_{ref} > 0$ in phase 2. Thereafter, the ADC will work in a similar way as the monotonic switching scheme. If $V_{ip,1} - V_{in,1} < 0$, $B_9 \sim B_6$ are set to be 0. The bypass window function will be activated and phase 2~4 will be bypassed.

Figure 4-8 Flow chart of the proposed ADC

4.2.6 Behavior modeling and simulation

To evaluate the effectiveness of the proposed idea, a behavior model for the proposed SAR ADC is built and illustrated in Fig 4-9. The Bootstrapped switches and Bottom plate switches are constructed in device level while the comparator and SAR logic are implemented by Verilog-A script.

Figure 4-9 High level diagram of the proposed SAR ADC

As shown in Fig 4-10, when $V_{ip}=530\text{mV}$ and $V_{in}=470\text{mV}$ ($V_{com}=0.5\text{V}$), the bypass function is activated. The output code of the proposed ADC is the same as the ideal ADC, which is 529.3mV .

Figure 4-10 (a) input signal voltage ($V_{com}=500\text{mV}$)
 (b) ADC output code after being transferred to voltage by an ideal 10-bitDAC
 (c) waveform of internal clock and comparator inputs

In Fig 4-11, when $V_{ip}=540\text{mV}$ and $V_{in}=480\text{mV}$, the common-mode voltage has 10mV variation. Simulation result shows that the proposed ADC can produce the same result as the previous scenario. This means that the proposed architecture can reject the common-mode noise and output the correct digital code.

Figure 4-11 (a) input signal voltage ($V_{com}=510\text{ mV}$)
(b) ADC output code after being transferred to voltage by an ideal 10-bit DAC
(c) waveform of internal clock and comparator inputs

Table 4-2 summarizes the simulation results, showing that the proposed SAR ADC has strong common-mode noise immunity. It can maintain conversion accuracy when there is common-mode noise in the system. A more detailed comparison between [16] and the proposed scheme on common-mode noise immunity will be presented on Section 5.8.

Table 4-2 Output code @ different V_{com}

	$V_{ip}(mV)$	$V_{in}(mV)$	$V_{com}(mV)$	The proposed ADC(mV)	Ideal ADC(mV)
1	535	465	500	534.18	534.18
2	540	470	505	534.18	534.18
3	540	470	505	534.18	534.18
4	530	470	500	529.3	529.3
5	540	480	510	529.3	529.3

4.3 Summary

In summary, the comparator-constructed bypass window scheme deteriorates the common-mode noise immunity of the differential structure, which would introduce error when acquiring data. However, the proposed capacitor constructed bypass window scheme maintains symmetry in the differential structure. Consequently, this new scheme has better common-mode noise rejection ability.

5. Circuit design and simulation result

This chapter discusses the implementation of the analog and digital circuits at transistor level. The main design objective for each circuit is stated and the strategies used to achieve these objectives are discussed. Section 5.1 analyzes the selection of the low leakage device. Then, in Section 5.2, the consideration on the DAC design is discussed.

5.1 Device selection

To improve the power efficiency of modern chips, the threshold voltage (V_T) of the MOSFETs has continually been reduced over the past decades. However, one trade-off that accompanies this trend is that the increasingly thinner gate-oxide thickness has resulted in an exponential increase in leakage current. This leakage power increases exponentially and accounts for a greater portion of the total power consumption in deep submicron technology. Equation 5.1 gives a detailed breakdown on the total power consumption in digital circuit, including the active and leakage component.

$$P_{\text{tot}} = P_{\text{act}} + P_{\text{leak}} = \alpha f C_{\text{load}} V_{\text{DD}}^2 + I_{\text{leak}} V_{\text{DD}} \quad (5.1)$$

In the context of SAR ADC, which only has dynamic circuit and no static components, leakage power is an important power consumer and should be taken with extra consideration. Thus, device with low leakage current is preferred in this design.

There are two types of devices in the GF40nm process library: HVTFET and Regular FET. Each type has different V_T and leakage current. Table 5-1 listed the characteristics of these two types of FETs.

Table 5-1 Leakage current @ $V_{ds}=1V$, $V_g=V_s=0$

	Leakage current	Size(W/L)
HVTNFET	5.45pA	115nm/40nm
REGNFET	57.6pA	115nm/40nm

As seen from the table, the leakage current of HVTNFETs is ten times smaller than REGNFETs. This is also true for HVTPFETs and REGPFETs. Therefore, HVTFETs are used as the sole devices for the digital components.

5.2 DAC circuit design

The most important component in a SAR ADC is its DAC. It consumes the largest portion of the total power [14] and its matching affects the linearity of ADC [1]. To achieve low power and good linearity, this section analyzes the choice of unit capacitor, DAC schematic and the layout considerations.

5.2.1 Unit capacitor

The basic building block for the whole DAC is the unit capacitor. Its capacitance determines the total capacitance of the DAC network, affecting the total power consumption of the DAC. Therefore, a small unit capacitor is preferred in low power SAR ADC design. However, there is capacitance deviation from the ideal unit capacitor due to process variations. This introduces mismatch in the DAC network and finally affects the linearity of the ADC. Therefore, a relatively large unit capacitor is preferred for good linearity. This means that a modest unit capacitor that can meet the linearity requirement should be chosen.

DNL is the difference between the actual code width of a non-ideal converter and the ideal case, as indicated by Equation 5.2, where ΔV_i is the transition code width for the i -th code (in units of LSB).

$$\text{DNL}_i = \Delta V_i - 1, \quad (5.2)$$

For an N -bit binary weighted ADC, the worst case DNL occurs at the MSB transition, from code $2^{N-1} - 1$ to 2^{N-1} . According to the analysis in [29], $\text{DNL}_{\max}$ can be expressed by

$$\text{DNL}_{\max} = \sqrt{2^N - 1} \frac{\delta_u}{C_u} \text{LSB} \quad (5.3)$$

where C_u is the nominal value of unit capacitor, δ_u is the standard deviation of unit capacitor and N is the resolution of the ADC.

Based on the required maximum DNL, resolution N and matching data from the vendor, the appropriate size of the DAC unit capacitor can be calculated by using Equation 5.3. In this ADC, a unit capacitance of $C_0 = 10\text{fF}$ was adequate, which was also verified by previous design [34].

5.2.2 DAC Layout

The topology of the DAC network has been shown and discussed in Section 4.2.4.

Layout is crucial for the DAC capacitor array. A good layout can introduce good matching, minimize fringe effects and non-linearity which is resulted from coupling. To mitigate against the first order gradient effects, common centroid layout is adopted here. Besides, a border of grounded dummy capacitors is used. This is crucial for providing an identical processing environment for the capacitors at the edge of the array. However, some mismatches will be introduced due to fringe effects. The capacitors in the center of the array

couple to neighboring capacitors which are not at ground. However, those capacitors on the edge couples to the grounded dummy capacitors. To minimize this source of mismatch, the distance of each capacitor is kept far away enough that edge effect is minor. Furthermore, the two smallest unit capacitors, C_0 and C_1 are placed at the edge of the DAC array to reduce parasitic capacitance introduced by metal connections. A floor-plan of the layout of the DAC capacitor array is shown in Fig 5-1.

Figure 5-1 Floor-plan of the DAC array (one side)

5.3 Switch design

In this design, bootstrapped switch is used to sample the input signal on the top plate of the DAC network. Meanwhile, the bottom plate switch network is used for bit cycling. The positive DAC array and negative DAC array have an identical switch network except that the control signal is different.

5.3.1 Bootstrapped switches

Bootstrapped switches have the advantage of better linearity. The on-resistance of sample transistor is nearly a constant value since its gate-source voltage is a fixed value, the supply voltage VDD. The bootstrapped switch in [25] is adopted in our design as sampling switches and is shown in Fig 5-2.

Figure 5-2 Schematic of the bootstrapped switch

5.3.1.1 Operation

When $CLKS=0$ and $CLKB=1$, $MN0$ is open and connects the bottom plates of capacitor C_0 to GND. $MN3$ and $MN4$ is also open and the gate voltage of $MP1$ is attached to GND. Since the net V_g is discharged to zero, $MN2$, $MN5$ and $MN6$ will be off. It also will let $MP1$ conduct and the capacitor C_0 be charged to VDD . A simplified diagram is illustrated in Fig 5-3, deleting all the switches which are off.

$CLKS=0,CLKB=1$

Figure 5-3 Simplified schematic for the bootstrapped switch when $CLKS=0$ and $CLKB=1$

When $CLKS=1$ and $CLKB=0$, the sampling switch will turn on in the sampling phase. Since $CLKB=0$, $MN4$ and $MN0$ is off, separating node V_g from GND. Since $CLKS=1$, $MP0$ is off while $MN1$ is on, connecting node V_a to node V_b . This will turn $MP2$, connecting node V_g to the top plate of the capacitor, C_0 . Then, it turns $MN2$, $MN5$ and $MN6$ on and sampling the input signal on the following capacitive DAC. A simplified diagram is illustrated in Fig 5-4 and all the 'on' transistors are replaced with simple breaks.

Figure 5-4 Simplified schematic for the bootstrapped switch when $CLKS=1$ and $CLKB=0$

5.3.1.2 On resistance

Due to the law of charge conservation, V_t varies in accordance to V_{in} . This will ensure the sampling transistor, $MN6$, has a constant gate-source voltage, making the on-resistance a small but nearly constant value, as shown in Fig 5-5. Due to body-effect, the on-resistance R_{on} of the bootstrapped switch still increases slightly from $135\ \Omega$ to $402.1\ \Omega$. In comparison to the bootstrapped switch, the R_{on} of the single NMOS switch has a step increase, from $135\ \Omega$ to $0.878\ M\Omega$, as shown in Fig 5-6. Therefore, the bootstrapped sampling circuit has better linearity than the single NMOS switch.

Figure 5-5 Bootstrapped switch on-resistance as a function of the input signal

Figure 5-6 NMOS switch on-resistance as a function of the input signal

5.3.2 Bottom plate switches

Since the bottom plate switches just switch between GND and V_{ref} , simple inverter buffers are adopted here as the bottom plate switches. However, the size of the switch buffers is scaled according to the driven capacitance. This ensures that unnecessary driving power consumption is avoided [25].

5.4 Performance of the sampling circuit

Sampling circuit consists of three basic sub-blocks, bootstrapped switches, DACs and bottom plate switches. The performance of the sampling circuit is also characterized using a testing structure, shown in Fig 5-7. The differential input signal is sampled onto the top plates of the DAC networks via two bootstrapped switches. The two bootstrapped switches are controlled by a system clock signal to switch between on and off. The bottom plate switches are constantly on in this test bench. The bootstrapped switches and bottom plate switches are built by using transistors, while the ideal capacitors are used here to build the two DACs. The 16bit resolution ADC is built by using Verilog-A code, therefore it is an ideal ADC.

After the input signals are sampled on to the DACs, the 16bit ideal ADC will converse it to digital code. Thereafter, the digital code will be processed by matlab code, doing Fast Fourier Transform (FFT) and calculating SNR, SINAD, and THD, etc.

Figure 5-7 Test bench for sampling circuit

Simulation result

Fig 5-8 illustrates the voltage waveform of input signals and the sampled signals on the DACs. As shown in this figure, the sampled signals exactly follow the input signals respectively, indicating that the sampling circuit has good performance. This is also evaluated using FFT analysis, as shown in Fig 5-9.

Figure 5-8 Simulated waveform of the voltage on DACs

Fig 5-9 shows an example of the 1024-point FFT spectrum with an input frequency of around 119 kHz and a sampling rate of 2 MS/s. As seen from the figure, the sample and hold (SH) circuit has very good linearity, with very small harmonics. The calculated SINAD is 84.3 dB, corresponding to 13.7 bits resolution, much higher than the target resolution, 10-bits.

Figure 5-9 Simulated 1024-point FFT spectrum at 2MS/s for SH circuit with input signal frequency of 119 kHz

Fig 5-10 shows an example of the 1024-point FFT spectrum with an input frequency of around 994 kHz, the Nyquist frequency, and a sampling rate of 2 MS/s. The calculated SINAD is 70.2 dB, corresponding to 11.4 bits resolution.

Figure 5-10 Simulated 1024-point FFT spectrum at 2MS/s for SH circuit with input signal frequency of 994 kHz

5.5 Comparator

Comparator is one of the main power consuming elements in SAR ADC. An energy efficient comparator is beneficial to improve the overall power efficiency of the ADC. Traditionally, dynamic comparator is adopted in SAR architecture because there is no static power consumption for this structure [1, 14-16 and 28]. Only dynamic current exists in this structure, thus its average power is proportional to the comparison rate of the comparator. In this paper, the structure proposed in [28] is adopted and is adjusted slightly. The circuit diagram is illustrated in Fig 5-11.

Figure 5-11 Two-stage dynamic comparator

5.5.1 Operation

As shown in Fig 5-11, the comparator has two stages, the input gain-stage and the output-latch stage. The input gain-stage is a clocked amplifier with differential inputs, INP and INN. The outputs of this amplifier, FP and FN, serve as the inputs of the output-latch stage. The output-latch stage is composed of a positive-feedback amplifier, which is for fast regeneration and to obtain a rail-to-rail output.

When in operation, this comparator has two phases, reset phase (when COMP_CLK=0) and evaluation phase (when COMP_CLK=1). During the reset phase, the PMOS transistors, MP1 and MP2, are on and charge the differential output nodes of the input-gain stage, FP and FN to VDD. Consequently, MN4 and MN7 will be switched on and pull the output node of the output-latch stage, OUTP and OUTN down to zero. When COMP_CLK transits from 0 to VDD, the evaluation phase will be started. The tail transistor MN3 is turned on and the output node of the input gain stage, FP and FN, will be pulled down from VDD to ground, as shown in Fig 5-12. The speed of this discharging process is different, with a strong relationship to the input signal voltage, INP and INN.

When FN and FP approximate the threshold voltage of the input pair transistors, MP5 and MP6, of the output-latch stage, the voltage difference between FN and FP will be amplified and latched onto the output nodes of the second stage, OUTP and OUTN. Fig 5-13 illustrates the regeneration process in the second stage.

Figure 5-12 Output of the input gain stage of the comparator

Figure 5-13 Output of the comparator

5.5.2 Comparator delay

Fig 5-14 illustrates the simulated delay of the comparator. As seen from this diagram, the delay is only 0.7ns when the input is 0.1LSB. Such a short delay ensures that the comparator in this design will not be bothered with meta-stability problem.

Figure 5-14 Simulated comparator delay

5.5.3 Offset

Fig 5-15 illustrates the simulated offset versus the number of occurrences. As shown in the bar diagram, the simulated offset is in the range of $\pm 12\text{mV}$, which has minor impact on the performance of the ADC.

Figure 5-15 Simulated comparator offset (500 Monte Carlo runs)

5.5.4 Power consumption

As shown in Fig 5-16, there is current flowing through the comparator only when the clock signal, COMP_CLK, transits from ground to VDD or from VDD to ground. No static current exists when the comparator is in operation. Therefore, the average power consumption of this comparator can be scaled down, at a rate which is proportional to the sampling rates.

Figure 5-16 Current flow through the comparator

5.6 SAR control logic

One of the cores of the SAR ADC is the SAR control logic, which determines how the ADC works. This section gives a breakdown of the SAR control. In section 5.6.1, the asynchronous clock generation logic is first described. Then in section 5.6.2, the error correction circuit and the control logic for the DACs is presented. The last section 5.6.3 is given to the bypass signal generation circuit.

5.6.1 Asynchronous clock generation circuit

Rather than using a high frequency external clock signal, the proposed SAR ADC uses an asynchronous logic to internally generate the conversion clock. This can relax the design constraint for the external clock signal and lower its power consumption. The schematic and

timing diagram of the asynchronous logic are illustrated in Fig 5-17. As shown in this figure, the externally provided system clock, CLKS, generates COMP_CLK, which has a much higher frequency and is used to control the dynamic comparator described in Section 5.5. CTRL [0:10] is the control signal which latches the output of the comparator and generates the control signals for the DACs.

Figure 5-17 Schematic and a timing diagram of the asynchronous logic

5.6.2 Control logic for the DACs and the error correction circuit

Fig 5-18 demonstrates the control logic for the DACs and the outputs of the ADC. The data error correction circuit (DEC) is also integrated in this circuit. The DEC signal is for triggering the DEC circuit and the circuit for generating the DEC signal is illustrated in Fig 5-19. As seen from Fig 5-18 and Fig 5-19, the DEC signal is effective only when B10=0 and B9=1. In such situation, the bypass window function would have also been activated as discussed in Section 5.6.3. By generating the DEC signal, the circuit aims to correct the output from 0000XXXXXX to 0111XXXXXXX by setting B8, B7 and B6 to 1 and resetting, hence correcting the output of the ADC.

Figure 5-18 Control logic for the DACs and the error correction circuit

Figure 5-19 DEC signal generation circuit

5.6.3 Bypass signal generation circuit

Fig 5-20 illustrates the bypass signal generation circuit. The bypass signal is a flag signal which triggers the bypass function. The bypass signal will only be activated when the input signal is in the predefined range. An example of the waveform is shown in Fig 5-17.

Figure 5-20 Bypass signal generation circuit

5.7 System simulation result

After characterizing all the sub-blocks, they are put together to construct the ADC to verify its function and performance. Section 5.7.1 presents the functionality of the ADC. Then the dynamic performance of the ADC is analyzed in section 5.7.2. Thereafter, section 5.7.3 compares the common-mode noise immunity of the proposed ADC with the bench mark structure in [16]. Finally, power consumption of the proposed ADC is analyzed.

5.7.1 The functionality of the ADC

Fig 5-21 illustrates the waveform of the input signals, the top plates of the DACs, the system clock signal CLKS and the internal comparator signal, COMP_CLK when the input signals are out of the predefined window. As shown in the figure, V_{DACP} and V_{DACN} vary around the

common-mode voltage, 0.5V, which ensures that the comparator has better linearity. When the bypass window is not activated, there are 11 phases for one sampling cycle.

Figure 5-21 Waveform in one sampling cycle when bypass window function is not activated

When the input signal is within the predefined bypass window, the bypass window function is activated. The ADC then has a different conversion process and the waveform of the input signal, voltages on the top plates of the DACs, CLKS, COMP_CLK and the bypass signal are illustrated in Fig 5-22. As seen from the figure, when input signal is within the predefined range, the bypass signal flags to zero after the second comparison phase. Then three of the comparison phases will be bypassed and there are only eight comparison phases left. Less comparison phase means less capacitor switching. Therefore, power consumption is reduced.

Figure 5-22 Waveform in one sampling cycle when bypass window function is activated

5.7.2 Common-mode noise immunity

Common-mode noise immunity is verified by circuit simulations and the results are shown in Table 5-2. From the table, V_{ip} , V_{in} and V_{com} represent the positive end, negative end and common-mode voltage of the differential input signal. Typically, V_{com} for an ideal signal is 500 mV while ΔV_{com} represents the common-mode voltage variation due to common-mode noise. V_r is the window reference voltage for the ADC in [16]. Only when both V_{ip} and V_{in} are larger than V_r , the bypass window function [16] will be triggered. The columns for “Ideal ADC”, “[16]” and “proposed” are the outputs of the Ideal differential ADC, ADC in [16] and the proposed ADC. As we can see from Scenario 1, 6 and 9, all three ADCs produce the same results when there is no noise presented. However, when positive common-mode noise presents, the comparator-constructed bypass-window scheme [16] might falsely trigger the

bypass window function and produce incorrect results, as shown in Scenario 2, 4 and 7. In contrast, the proposed ADC is able to produce the same result as the ideal ADC in all cases.

Table 5-2 Output code @ different V_{cm} and different input scenario

	V_{ip} (mV)	V_{in} (mV)	V_{com} (mV)	ΔV_{com} (mV)	V_r (mV)	Ideal ADC (mV)	[16]	Proposed (mV)
1	532	468	500	0	468.75	531.25	531.25	531.25
2	534	470	502	2	468.75	531.25	530.27	531.25
3	530	466	498	-2	468.75	531.25	531.25	531.25
4	537	473	505	5	468.75	531.25	530.27	531.25
5	527	463	495	-5	468.75	531.25	531.25	531.25
6	535	465	500	0	468.75	534.18	534.18	534.18
7	540	470	505	5	468.75	534.18	530.27	534.18
8	530	460	495	-5	468.75	534.18	534.18	534.18
9	525	475	500	0	468.75	524.41	524.41	524.41
10	530	480	505	5	468.75	524.41	524.41	524.41
11	520	470	495	-5	468.75	524.41	524.41	524.41

5.7.3 Dynamic performance

The output code of the proposed ADC is processed by matlab codes, to do FFT analysis and calculate the SINAD, SNR, and ENOB. Fig 5-23 shows the simulated FFT power spectrum with an input frequency of around 994 kHz. The calculated SNDR is 61.02dB, corresponding to an Effective-Number-of-Bits (ENOB) of 9.84bits.

Figure 5-23 Simulated 1024-point FFT spectrum at 2MS/s with input frequency 994 kHz

Figure 5-24 Simulated 1024-point FFT spectrum at 2MS/s with input frequency 119 kHz

The simulated FFT power spectrum with an input frequency of around 119 kHz is also presented here, in Fig 5-24. The calculated SNDR is 61.55dB, corresponding to an ENOB of 9.93bits. Both of the simulation results indicate that the proposed ADC has good and stable performance in the input signal frequency range.

5.7.4 Power reduction

Figure 5-25 Power consumption of (a) DAC switching, (b) comparator, (c) SAR, and total block with 64-LSB bypass window

As shown in Fig 5-25, when the output code is between 480 and 543, the 64-LSB size bypass window is triggered. The total power reduction can reach 74% when the bypass window function is activated. If the magnitude of a bio-signal is very small in 80% of its period, the overall power reduction would be 59%, as shown in Fig 5-25(d).

A comparison of the proposed ADC with other state-of-the-art SAR ADCs is demonstrated in Table 5-3. Figure-of-merit (FoM) is also shown in this table, where FoM is defined as:

$$\text{FoM} = \frac{P}{2f_{\text{in}} * 2^{\text{ENOB}}}$$

where P is the power consumption of the ADC and f_{in} is the frequency of the input signal.

As shown in the table, the proposed design has a comparably low FoM. The ISCAS'13 [33] outperforms the FoM of this work since it uses a low supply voltage and tri-level switching scheme. However, the tri-level switching scheme requires an additional accurate V_{cm} which in the work of [33], requires extremely good matching between C_0 and a dummy capacitor. This is not easy in practical design or needs complex calibration technique, adding more power consumption for additional circuit.

Table 5-3 Comparison to State-of the-art works

Specification	JSSC'12 [16]	JSSC'12 [31]	ISCAS'12 [32]	ISCAS'13 [33]	This work
Result type	Meas.	Meas.	Meas.	Sim.	Sim
Architecture	SAR	SAR	SAR	SAR	SAR
Technology	180nm	40nm	180nm	90nm	40nm
Supply voltage(V)	0.6	0.5	1	0.5	1
Sampling rate(kS/s)	1000	1100	500	1280	2000
Resolution(bits)	10	9	10	10	10
ENOB(bits)	9.18	7.5	9.24	9.69	9.93
Power(uW)	5.253	1.2	14.2	3.87	11.82
FoM(fJ/Conv.-step)	9.11	6.3	47	3.66	6.1

6. Conclusion & Future Work

6.1 Conclusion

A 1V, 10 bit, 2MS/s asynchronous SAR ADC with capacitor-constructed bypass-window is presented. The design is implemented in GF 40nm CMOS process. Pre-layout simulation result illustrates that the proposed ADC can reduce the overall power consumption by 74% if the bypass window function is activated with 80% of probability. Besides, the proposed ADC circuit maintains symmetry and has good common-mode noise immunity. At 2MS/s and 1V, the average power consumption is 11.82 μ W and its FoM is 6.1 fJ/Conversion-step.

6.2 Future work

This section first illustrates aspects at which modifications can be done to improve the performance of the capacitor constructed bypass window scheme. Then in Section 6.2.2, a new proposal is discussed.

6.2.1 Aspects for improvement

The goal of this work is to verify the effectiveness of the proposed capacitor constructed bypass window scheme. However, the size of the bypass window was not chosen according to the type of biomedical signal. Hence, it is proposed to incorporate an adaptive window size scheme. Then the ADC will determine the best window size automatically according to the input signal. Greatest power saving can be achieved for every type of biomedical signal for this scheme.

6.2.2 New proposal- A two-mode comparator constructed bypass window switching scheme for SAR ADC

As seen from the flow chart Fig 6-1, there is one comparator with two different accuracy modes, 7bits and 10bits, in the proposed SAR ADC architecture. This ADC first works in the 7 bits mode. If the difference of the input signals is larger than 8LSB, as shown in Fig 6-2, then the output of the comparator would be 1 or 0. If the difference is smaller than 8LSB, as seen from Fig 6-3, then the output is undetermined and the 10bit accuracy mode is activated. Many conversion steps will also be skipped and the switching power can be saved. It is also possible to add one more redundant comparison step in the flow chart to improve the accuracy of the ADC.

The fundamental of this two mode comparator stems from the tri-level comparator in [31]. When the difference of the input signal of the comparator is smaller than 8LSB, the 7-bit mode comparator is in meta-stable phase and is unable to output the comparison result. A meta-stable detector should be added into the comparator, same as the comparator in [31].

This scheme can also be expanded, for setting the accuracy of the comparator first to K-bits and then to N-bits (N is also the resolution of the ADC) in the two-mode operation.

This scheme is a preliminary proposal proposed by me. Further investigation will be done by other student.

Figure 6-1 Flow chart of the proposed switching scheme

Figure 6-2 Input difference smaller than 8LSB

Figure 6-3 Input difference larger than 8LSB

Bibliography

- [1] Marcus Yip, “A Highly Digital, Reconfigurable and Voltage Scalable SAR ADC,” in MIT MSC thesis, 2009
- [2] M.Yin and M. Ghovanloo, “A low-noise preamplifier with adjustable gain and bandwidth for bio-potential recording applications,” Proc. IEEE Int. Symp. Circuits and Systems, May 2007, pp. 321-324.
- [3] T. Denison et al., “A 2 uW 100nV/rHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials,” IEEE Journal of Solid-State Circuits, vol. 42, no.12, pp. 2934-2945, Dec. 2007.
- [4] M. Bach et al., “Standard for pattern electroretinography,” Documental Ophthalmological, vol. 101, pp. 11-18, 2000
- [5] Xiaodan Zou et al., “A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip,” IEEE Journal of Solid-State Circuits, vol. 44, no.4, pp. 1067-1077, Apr. 2009.
- [6] R.M. Rangayyan, Biomedical signal Analysis – A Case-Study Approach. John Wiley & Sons, 2002.
- [7] F. Chen, A. P. Chandrakasan, and V. Stojanovic, “A Low-power Area-efficient switching scheme for charge-sharing DACs in SAR ADC,” Proc. of IEEE CICC, Sept. 2010.

- [8] H. Y. Yang and R. Sarpeshkar, "A Bio-Inspired Ultra-Energy-Efficient Analog-to-Digital Converter for Biomedical Applications," *IEEE Trans. on Circuits and Systems-I*, vol. 53, pp. 2349–2356, Nov. 2006.
- [9] Vikram Chaturvedi et al., "An 8-to-1 bit 1-MS/s SAR ADC With VGA and Integrated Data Compression for Neural Recording" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, Feb. 2013.
- [10] Yuanchao, "Design of An Ultra-Low-power CMOS Analog-to-Digital Converter for biomedical applications," Qualification report, unpublished.
- [11] B.P.Ginsburg et al., "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *IEEE International Symposium on Circuits and Systems*, Vol.1, pp184-187, May 2005.
- [12] You-Kuang Chang et al., "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," *IEEE Asian Solid-State Circuits Conference*, pp. 228-231, Nov 2007.
- [13] Chang-Yuan Liou et al., "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp.280-281, Feb 2013.
- [14] Chun-Cheng Liu et al., "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no.4, pp. 731-740, Apr. 2010.
- [15] Harpe, P. et al., "A 7-to-10b 0-to-4MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step," *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp.472-474, Feb 2012.

- [16] Guan-Ying Huang et al., "A 1- μ W 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications," IEEE Journal of Solid-State Circuits, vol. 47, no.11, pp. 2783-2795, Nov. 2012.
- [17] Ken martin et al., Analog Integrated Circuit Design, 2nd Edition. Wiley, 2011.
- [18] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, Third Edition.

Wiley-IEEE Press, 2010
- [19] Atila Alvandpour, Data Converters, Class material, 2013
- [20] Guowei, "A Low-Power 10-bit 50 MS/s CMOS Successive Approximation Register ADC," UBC MSC thesis, 2010
- [21] Saberi, M. "Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters Used in Successive Approximation ADCs," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 58, no.8, pp 1736-1748, Aug 2011.
- [22] B.P.Ginsburg et al., "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," IEEE International Symposium on Circuits and Systems, Vol.1, pp184-187, May 2005.
- [23] You-Kuang Chang et al., "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," IEEE Asian Solid-State Circuits Conference, pp. 228-231, Nov 2007.
- [24] W. S. Liew et al., "A 1-V 60- μ W 16-channel interface chip for implantable neural recording," in Proc. IEEE CICC, pp 507-510, Sep. 2009.

- [25] Chun-Cheng Liu et al., "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure," IEEE Journal of Solid-State Circuits, vol. 45, no.4, pp. 731-740, Apr. 2010.
- [26] Hsin-Yuan Huang et al., "A 9.2b 47fJ/Conversion-Step Asynchronous SAR ADC with Input Range Prediction DAC Switching," IEEE International Symposium on Circuits and Systems, pp2353-2356, May 2012.
- [27] You-Kuang Chang et al., "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," IEEE Asian Solid-State Circuits Conference, pp. 228-231, Nov 2007.
- [28] Van Elzakker, M et al., "A 10-bit Charge-Redistribution ADC Consuming 1.9 μ W at 1 MS/s," IEEE Journal of Solid-State Circuits, vol. 45, no.5, pp. 1007-1015, Apr. 2010.
- [29] Wakimoto Tsutomu et al., "Statistical analysis on the effect of capacitance mismatch in a high-resolution successive-approximation ADC," IEEE Transactions on Electrical and Electronic Engineering, vol. 6, is S1, pp. 89-93, 2011
- [30] Ishida, K.; Kanda, K.; Tamtrakarn, A.; Kawaguchi, H.; Sakurai, T., "Managing subthreshold leakage in charge-based analog circuits with low- V_{TH} transistors by analog T- switch (AT-switch) and super cut-off CMOS (SCCMOS)," Solid-State Circuits, IEEE Journal of , vol.41, no.4, pp.859,867, April 2006
- [31] Shikata, A.; Sekimoto, R.; Kuroda, T.; Ishikuro, H., "A 0.5 V 1.1 MS/sec 6.3 fJ/Conversion-Step SAR-ADC With Tri-Level Comparator in 40 nm CMOS," Solid-State Circuits, IEEE Journal of , vol.47, no.4, pp.1022,1030, April 2012 .

- [32] Hsin-Yuan Huang; Jin-Yi Lin; Chih-Cheng Hsieh; Wen-Hsu Chang; Hann-Huei Tsai; Chin-Fong Chiu, "A 9.2b 47fJ/conversion-step asynchronous SAR ADC with input range prediction DAC switching," Circuits and Systems (ISCAS), 2012 IEEE International Symposium on , vol., no., pp.2353,2356, 20-23 May 2012.
- [33] Kuan-Ting Lin; Kea-Tiong Tang, "A SAR ADC with energy-efficient DAC and tri-level switching scheme," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.2243,2246, 19-23 May 2013
- [34] Chao Yuan; Lam, Y.Y.H., "A 281-nW 43.3 fJ/conversion-step 8-ENOB 25-kS/s asynchronous SAR ADC in 65nm CMOS for biomedical applications," Circuits and Systems (ISCAS), 2013 IEEE International Symposium on , vol., no., pp.622,625, 19-23 May 2013