Class D amplifier with pseudo-randomized carrier frequency modulation (PRCFM) for EMI mitigation

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**CLASS D AMPLIFIER WITH PSEUDO-RANDOMIZED
CARRIER FREQUENCY MODULATION (PRCFM) FOR EMI
MITIGATION**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING
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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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Summary

Class D amplifiers are found in nearly all portable electronic products for their small size and power efficiency. Due to their high frequency switching operation, they generate significant amount of electromagnetic interference (EMI) and usually off-chip filters are necessary in order for them to comply with the international regulatory EMI limits. With the continuous trend of product miniaturization, filter-less Class D amplifiers are gaining attention recently. Without the off-chip filter, designing a fully integrated filter-less Class D amplifier to meet the EMI requirements can be challenging.

This thesis develops and implements a pseudo-randomized carrier frequency modulation (PRCFM) technique in both analog and digital filterless Class D audio power amplifiers for EMI mitigation purposes so that these amplifiers fulfill the electromagnetic compatibility (EMC) requirement without the needs of off-chip filters. The PRCFM circuit is implemented with a frequency divider and a linear feedback shift register (LFSR). The proposed amplifier also features a peak detector to improve the power conversion efficiency when it operates under low audio input condition.

An analog filter-less Class D amplifier is designed and fabricated using 0.18 μm CMOS process technology with a size of 1 mm^2 and the proposed PRCFM circuit occupies only less than 1% of the total chip area. The effectiveness of the PRCFM

scheme for EMI mitigation is demonstrated experimentally. The PRCFM circuit consumes very little additional power and therefore has little impact on the power efficiency of the amplifier. In addition, the amplifier still maintains excellent total harmonic distortion (THD) over the audio band of interest (100 Hz - 6 kHz) and the typical modulation index range.

With the encouraging results, the PRCFM technique is further extended to a digital Class D amplifier and similar EMI mitigation performance has also been demonstrated. The digital Class D amplifier consists of a digital pulse width modulation (DPWM) circuit, a power stage, a PRCFM circuit and a low pass filter (LPF). Moreover, an efficient algorithmic sampling process and a hybrid pulse generation method are proposed to improve THD performance. The circuit is first simulated in Matlab Simulink and then implemented with field-programmable gate array (FPGA). Both simulated and measured results have shown that the PRCFM spreads the switching frequency of the Class D amplifier from 145 kHz to 295 kHz in 31 frequency steps using a pseudo-random (PR) pattern, which results in EMI reduction of 7.4 dB, with acceptable THD.

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List of Acronyms

$\Delta\Sigma$	Delta-Sigma
AD	2-level PWM, A stands for level of PWM and D is for class D
AV	Average detector
BD	3-level PWM, B stands for level of PWM and D is for class D
BPF	Band-Pass Filter
BTL	Bridge-Tied Load
CD	Compact Disc
CG	Clock Generator
CISPR	Comité International Spécial des Perturbations Radioélectriques
CRFB	Cascaded Resonator Feedback
DAC	Digital-to-Analog Converter
DEPWM	Double Edge PWM
DPWM	Digital Pulse Width Modulation
DSS	Direct Sequence spread Spectrum modulation
EMI	Electromagnetic Interference
FCC	Federal Communications Commission
FPGA	Field-Programmable Gate Array
FSS	Frequency hopping Spread Spectrum modulation
HSS	hybrid Spread Spectrum modulation
LEPWM	Leading Edge PWM
LFSR	Linear Feedback Shift Register
LISN	Line Impedance Stabilization Network
LPF	Low-Pass Filter
LSP	Less Significant Part
MSP	Most Significant Part
MUX	Multiplexer
NTF	Noise Transfer Function

OSR	Over Sampling Ratio
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PR	Pseudo-Random
PRCFM	Pseudo-Randomized Carrier Frequency Modulation
PRSSM	Pseudo-Randomized Spread Spectrum Modulation
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PSSM	Periodic Spread Spectrum Modulation
PWM	Pulse Width Modulation
QP	Quasi-Peak
RPPM	Random Pulse Position Modulation
SMP	Switching Mode Power
SNR	Signal-to-Noise Ratio
SSM	Spread Spectrum Modulation
TDL	Tapped Delay Line
TEPWM	Trailing Edge PWM
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator

Chapter 1

Introduction

1.1 Background and motivation

The history of audio power amplifiers can be dated as far back as 1909. With the invention of transistors in 1960s, the market for power amplifiers has been expanding, as every audio and video product requires some form of signal amplification.

In general, audio amplifiers are classified as Class A, Class B, Class AB, and Class D. Class A amplifier has the highest signal linearity with the least distortion but suffers low power efficiency, as the transistors at the output stage operate in the active region. Class B amplifier only turn on half of the transistors at the output stage and therefore its power efficiency is significantly improved at the expense of poor signal linearity. Class AB amplifier combines the merits of Class A and Class B amplifiers and its efficiency and signal linearity are dependent on how the transistors at the output stage are biased [1].

In the last decade, portability is a highly desired feature for consumer electronics, such as smart phones and MP3 players. The quest for such feature adds new challenges in product design, for examples, low power consumption and compact

packaging. Hence, a new class of amplifier, called Class D amplifier, becomes highly popular in battery operated portable devices for its excellent power efficiency over a large modulation index range, compared to its linear counterparts such as Class A and Class B amplifiers [2]. The excellent power efficiency is achievable as the transistors at the output stage operate as switches. In other words, the output power transistors are either fully “on” or fully “off” during the normal operation, thus the power dissipation in the transistors is negligible. Class D amplifier can easily achieve power efficiency higher than 80% [2-4]. Fig. 1.1 shows the power efficiency comparison for Class D, Class A and Class B amplifiers over the whole output dynamic range. It is clearly observed that the Class D amplifier has superior power efficiency than the ideal Class A and Class B amplifiers throughout the output dynamic range.

Fig. 1.1. Power efficiency comparison for Class A, Class B and Class D amplifiers [4]

A conventional Class D amplifier consists of four basic circuit blocks, a modulation circuit, an output stage, a negative feedback network and a LC low pass filter (LPF). The modulation circuit modulates the input audio signal with a high frequency carrier signal, resulting in a series of pulses. The output stage provides sufficient

power to drive the speaker load. Through the negative feedback network, it improves the total harmonic distortion (THD) and power supply rejection ratio (PSRR) of the Class D amplifier. Lastly, the LC filter blocks the high frequency carrier components and recovers the amplified audio signal. However, the LC filter occupies relatively a large physical space and results in additional design cost. As Class D audio amplifiers are usually designed for portable applications, size is one of the important design criteria. To circumvent this problem, a filter-less Class D amplifier architecture has been reported to eliminate the output filter while maintaining the efficiency advantage [5-8]. This is achievable with the aid of our human ear, which acts as a band-pass filter (BPF) (20 Hz - 20 kHz).

The high power efficiency performance of Class D amplifier is mainly due to the switching mode operation of the output stage. The MOS power transistors at the output stage acting as switches are turned either fully “on” or “off”. Ideally, there is no power loss in the transistors and the theoretical power efficiency for Class D amplifier is 100%. However, in reality, dynamic power loss exists due to the device’s imperfections, and such loss is proportional to the switching frequency of the output stage.

Similar to the other high frequency switching-mode circuits, Class D amplifiers also generate significant amount of electromagnetic interference (EMI). Fig. 1.2(a) shows a typical Class D output stage waveform. The repetitive pulses are expected to generate EMI mainly concentrated on the switching frequency and its harmonics extending up to several tens of MHz [9]. In addition, the reverse recovery current due

to the body diodes, as shown in Fig. 1.2(b), can cause overshoot and undershoot, which contributes additional high frequency EMI.

Fig. 1.2. EMI source in Class D amplifier

As Class D amplifier is part of an electronics product, it is also required to meet the stringent international EMI regulations imposed by Federal Communications Commission (FCC) and Comité International Spécial des Perturbations Radioélectriques (CISPR), and hence effective EMI mitigation techniques must be considered during the amplifier design phase. The most commonly used method for EMI mitigation is to attenuate high frequency EMI by adding a low pass filter. However, LC filter is difficult to be integrated into a chip and usually has to be added off-chip. Therefore, alternative EMI mitigation design techniques such as the soft switching [10, 11] and the spread spectrum modulation (SSM) techniques [12-14], which directly work on the switching frequency of the output stage have been reported in literature. These solutions mitigate EMI at the source and therefore offer attractive options to designers, as they eliminate the needs of off-chip filters.

The basic principle of soft switching is to slow down the switching transitions, i.e. dv/dt and di/dt . As a result, it reduces the EMI generated as well as the switching loss. However, the longer switching transition time limits the maximum switching frequency, which contradicts current trends of ever-increasing switching operating frequency. On the other hand, the SSM substantially reduces the EMI noise by spreading the EMI noise over a wider switching frequency range, instead of one fixed frequency and hence, it does not constraint the use of high frequency switching operations.

1.2 Objectives

The primary objectives of this thesis are as follows:

- a) To design a Class D amplifier based on pseudo-randomized carrier frequency modulation (PRCFM);
- b) To implement PRCFM in both analog and digital filter-less Class D amplifiers for EMI reduction purpose; and
- c) To investigate the parameters affecting EMI in Class D amplifier.

1.3 Major contributions of the thesis

Apart from an in-depth study of Class D amplifier and literature review on various spread spectrum schemes for switching mode circuits, the thesis has made the following contributions.

Firstly, a filter-less analog Class D amplifier with PRCFM has been successfully designed and fabricated. The proposed PRCFM circuit has been demonstrated to reduce the EMI effectively and yet exhibit acceptable THD over the interested modulation index range. The proposed Class D amplifier also features a peak detector to adjust the switching frequency when the peak voltage of the input audio signal is less than a threshold level. This is to reduce the dynamic power loss, and hence provides high power efficiency under the low output power operation. The Class D amplifier with PRCFM circuit is realized in CSM 0.18 μ m CMOS process and its performance is validated experimentally.

Secondly, a digital Class D amplifier with PRCFM has also been designed and excellent EMI reduction is demonstrated. The proposed Class D amplifier also features a novel digital pulse width modulation (DPWM) circuit, which consists of an algorithmic sampling process and a hybrid pulse generator. The proposed DPWM exhibits acceptable THD over the interested modulation index range as well as the audio band range. The circuit is realized by field-programmable gate array (FPGA) and its performance is verified experimentally.

Finally, the relationship between the noise floor in audio band and the number of pseudo-random (PR) bits used is studied. A first order estimation of EMI reduction with the number of PR bits is also derived so that the designer can optimize the PR modulation design to achieve the best EMI reduction as well as modulation size. In addition, the impact of PR modulation on THD is investigated and a solution using frequency divider is proposed to minimize such impact.

1.4 Organization of the thesis

The rest of the thesis is organized as follows. Chapter 2 presents the background knowledge of Class D amplifier and a literature review of various EMI mitigation schemes for the switching mode circuits. Chapter 3 introduces the proposed analog filter-less class D amplifier with PRCFM. Both measurement results and analysis are presented. Chapter 4 describes the proposed digital Class D amplifier with PRCFM. The simulation and measurement results are also presented. Finally, a conclusion and future work are drawn in Chapter 5.

Chapter 2

Literature Review

This chapter introduces the structure and working principles of conventional analog and digital Class D amplifiers followed by a review of various spread spectrum methods for switching-mode circuits.

2.1 Class D amplifier

2.1.1 Output stage

The main difference between Class D amplifier and its linear counterpart is the design of the output stage. The primary function of the output stage is to provide sufficient power to drive the speaker. Since most of the power loss is at the output stage, it is crucial to design an output stage with very low loss for good power efficiency.

The output stage of Class D amplifier consists of either NMOS or PMOS transistors acting as switches, operating either in the triode or the cut-off region. When the transistor is on, the voltage across the drain and source terminals is theoretically zero, regardless of the amount of current flowing through the transistor. On the other hand, there is virtually no current flowing through the transistor when the transistor is off. And the total supply rail voltage is developed across the drain and source

terminals of the transistor. As a result, the power dissipation in the switching transistor is ideally zero. Hence, theoretically, the power efficiency of the Class D output stage is 100%.

The output stage of the Class D amplifier is commonly implemented in either half-bridge or full-bridge configurations, as depicted in Fig. 2.1. The half bridge configuration, as shown in Fig. 2.1(a), is simpler and more flexible. On the other hand, the full bridge configuration, also known as the bridge-tied load (BTL) configuration, as shown in Fig. 2.1(b), is larger in size because it requires two half-bridge amplifiers. The major advantage of the BTL configuration is that the even harmonic components and DC offsets of the pulse width modulation (PWM) signal is cancelled due to the differential output topology. Another advantage is that the voltage across the load is doubled, so it can provide four times output power over that supplied by the half bridge configuration [15-18]. Hence, the BTL is a preferred topology compared to the half bridge in terms of performance.

In reality, the achievable power efficiency of Class D amplifier is about 95% because of the imperfection of the transistor switch, such as the on-resistance of the transistor and the inherent resistance of the metal connection. The power dissipation in the power transistor degrades the power efficiency performance of the amplifier [15]. Another error source of Class D amplifier is the switching timing error caused by the nonlinear parasitic capacitance and the dead time. At the output stage, the charging and discharging of the parasitic capacitance for the output stage result in nonlinear turn on and turn off switching time. The dead time is the time when both NMOS and

PMOS networks in the CMOS circuit are turned off, and is used to prevent the shoot-through current. Shoot-through is a phenomenon that the power rails are short-circuited because of the small MOS on-resistance when both the NMOS and PMOS power transistors are turned on. A huge shoot-through current would be generated and might probably damage the chip. In addition, the shoot-through current increases the conduction power loss as well [19]. A longer dead time contributes to significant THD error [20, 21]. However, a shorter dead time may not solve the shoot-through problem and increase the power loss. Thus optimization is usually needed for specific applications.

Fig. 2.1. (a) PDM generation and (b) PWM generation

2.1.2 Important Design Parameters of Class D Amplifier

Many parameters are used for the evaluation of the performance of audio amplifiers. Among these parameters, the power efficiency, THD, and EMI are the key ones. In this section, the power dissipation and THD for Class D amplifier are briefly described. The EMI issues will be discussed in details in Section 2.4.

Power Dissipation

As mentioned above, the output stage of Class D amplifier consumes the largest portion of the power in most designs. There are three main contributors of power dissipation at the output stages, namely the switching loss, the short circuit current loss and the parasitic resistance loss [15, 22].

The switching loss is caused by the charging and discharging of total parasitic capacitance at the output stage. The total parasitic capacitance consists of the gate capacitance, the interconnection capacitance and the diffusion capacitance. This dynamic power loss can be expressed as:

$$P_{SW} = \frac{1}{2} C_L V_{DD}^2 f_c \quad (2.1)$$

where C_L is the total parasitic capacitance, V_{DD} is the supply voltage and f_c is the switching frequency.

Equation (2.1) shows that to reduce switching loss for a given design, the most effectively ways are to limit the supply voltage and the switching frequency.

The short circuit power loss is due to the shoot-through current when both the NMOS and the PMOS are turned on simultaneously. The approximate power dissipation is given by

$$P_{SC} = I_{SC} V_{DD} \quad (2.2)$$

where I_{SC} is the shoot-through current.

Equation (2.2) indicates that the short circuit loss is proportional to the supply voltage. Taking note that the shoot-through occurs during the switching, so the power loss can be minimized by reducing the switching frequency too.

The third contributor of power loss is due to the parasitic resistance of the transistor. It includes the finite on-resistance of the transistor and the interconnect resistance. The power loss can be calculated as follow

$$P_{CL} = I_{ON}^2 R_P \quad (2.3)$$

where I_{ON} is the turn on current and R_P represents total parasitic resistance.

By observing equation (2.3), it is apparent that this loss can be significant when a huge turn on current flows through the transistors. Hence, parasitic resistance of the output stage should be minimized to limit such loss.

For a quick estimation, the power efficiency of a Class D amplifier can be expressed as

$$\eta = \frac{P_L}{P_L + P_{SW} + P_{SC} + P_{CL}} \times 100\% \quad (2.4)$$

where P_L is the power delivered to the speaker load.

In summary, the power efficiency of Class D amplifier is inversely proportional to the supply voltage V_{DD} , the switching frequency f_C and the parasitic resistance of the output stages R_P . Usually, V_{DD} and R_P are defined for a specific application, f_C is the remaining factor to improve the power efficiency performance.

Total Harmonic Distortion (THD)

The THD is an important figure of merit for audio signal quality that measures the harmonic distortion of the audio signal. It is defined as

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{nf}^2}}{V_f} \times 100\% \quad (2.5)$$

where V_f is the magnitude of the fundamental frequency component and V_{nf} is the magnitude of the n^{th} harmonic component.

Ideally, Class D amplifier has no harmonic distortion in the natural sampling process [23-25]. Taking the output PWM signal of a double edge PWM (DEPWM) as an example, based on the assumption and the derivation in [23], the spectrum of the signal is

$$\begin{aligned} v_o(t) = & k + A \cos(2\pi f_i t) + 2 \sum_{m=1}^{\infty} \frac{\sin m 2\pi f_c t}{m\pi} - 2 \sum_{m=1}^{\infty} \frac{J_0(m\pi M)}{m\pi} \sin(m 2\pi f_c t - \\ & 2m\pi k - 2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} \frac{J_0(m\pi M)}{m\pi} \sin(m 2\pi f_c t + n 2\pi f_i t - 2m\pi k - \frac{n\pi}{2}) \end{aligned} \quad (2.6)$$

where f_i is the frequency of the input signal and f_c is the switching frequency.

It clearly shows that there is no input harmonics and ideally the audio signal can be recovered by a simple LPF given that $f_i \ll f_c$. However, the non-idealities in the real components will contribute to the THD. To improve the THD, a closed-loop negative feedback is usually employed in Class D amplifier design. With the feedback, the THD of a Class D amplifier can be improved by a factor of $(1 + \beta A)$ compared to that without the feedback, where βA is the loop gain of the amplifier for natural sampling process.

2.2 Analog Class D amplifier

The conventional analog Class D amplifier consists of four basic blocks, namely a modulation circuit, an output stage, a negative feedback network and a LC LPF, as depicted in Fig. 2.2. In the modulation circuit, the input audio signal is compared with the high frequency carrier signal. The output is high when audio signal is higher than the carrier and vice versa. The resultant series of pulses is called PWM signal and the duty ratio (T_{on}/T) of it contains the information of the input audio signal. Subsequently, the PWM signal is fed into the output stage, which is normally a chain of inverters, to provide sufficient power to drive the speaker load. The negative feedback network is employed to improve the THD and PSRR of Class D amplifier. Lastly, the LC filter removes the high frequency carrier and reconstructs the amplified audio signal.

Fig. 2.2. Basic structure of a conversional Class D amplifier

2.2.1 Modulation techniques

Two common modulation techniques are adopted for Class D amplifier, the PWM [26-33] and the delta-sigma ($\Delta\Sigma$) modulation techniques [6, 34-37]. In the PWM technique, the audio signal is encoded with the pulse width, while the signal information is encoded with the pulse density in $\Delta\Sigma$ modulation.

Fig. 2.3(a) illustrates the generation of the pulse density modulation (PDM) signal. The number of output pulses over certain time period is proportional to the average value of the input audio signal. The pulse width is not arbitrary but quantized to multiples of the modulator operating period [4]. Higher order $\Delta\Sigma$ modulator is required for better signal performance. The reported $\Delta\Sigma$ modulation demonstrates high signal-to-noise ratio (SNR) and good PSRR due to the noise shifting nature of the $\Delta\Sigma$ modulation. The trade-off is higher operating frequency, which results in more switching loss and thus lower efficiency. The operation frequency of the $\Delta\Sigma$ modulator typically ranges from 3 MHz to 6 MHz. Other obstacles are the stability issue and the complexity of the higher order $\Delta\Sigma$ modulator, and hence it is more difficult to be implemented.

On the other hand, Fig. 2.3(b) illustrates the generation of the PWM signal. The input audio signal is compared with the triangular waveform of much higher frequency. The resultant pulse is high when the instantaneous audio signal is higher than the carrier and vice versa. Therefore, the average of the output PWM signal is given as

$$\bar{V} = \frac{1}{T} \int_0^{DT} V_{DD} dT = DV_{DD} \quad (2.7)$$

where T is the output PWM time interval, V_{DD} is the voltage supply and D is the duty ratio.

If the carrier frequency is much higher than that of the input audio signal, it can be assumed that the instantaneous audio signal v_{in} is unchanged in one carrier period. So the duty ratio can be expressed as

$$D = \frac{T_{on}}{T} = \frac{v_{in}}{V_A} = \frac{\bar{V}}{V_{DD}} \quad (2.8)$$

where T_{on} is the “on” time for the output PWM signal in one period and V_A is the maximum amplitude of the carrier. In this manner, D of the output PWM signal conveys the information of the input signal.

Although the PWM is a nonlinear process, it is proven that the input signal can be reconstructed by a simple LPF and no harmonic distortion is present in the baseband for the natural sampling PWM [24]. The major advantage of the PWM is its low THD at a relatively low carrier frequency (typically around 250 kHz), and thus low switching loss. Another advantage is its simplicity in design, as only a comparator is required. Therefore the PWM technique is much more popular for the above-mentioned reasons. However, its main drawback is the poor PSRR.

Generally, the PWM scheme can be further categorized into the leading edge PWM (LEPWM), the trailing edge PWM (TEPWM) and the DEPWM, as illustrated in Fig. 2.4, based on the shapes of the internally generated carrier waveforms. For the LEPWM, a sawtooth carrier with the waveform ramped downwards is employed, and thus the leading edge positions of the resultant PWM waveform occur at fixed time intervals. Similarly for the TEPWM, a sawtooth carrier with waveform ramped upwards is used. For the DEPWM, a triangular carrier is used, so both edges of the output PWM signal are determined by the magnitude of the input audio signal [24]. Hence, the amount of information carried in the DEPWM is doubled, compared to the LEPWM and the TEPWM.

Fig. 2.3. (a) PDM generation and (b) PWM generation

Fig. 2.4. Three types of PWM schemes

2.2.2 2-level PWM (AD) & 3-level PWM (BD) Modulation

In conventional Class D amplifier with BTL output stage configuration, the two differential output PWM waveforms are ideally 180° out of phase, as shown in Fig. 2.5. Therefore, the voltage across the load has two levels, $+VDD$ and $-VDD$. This configuration is called the AD modulation [38]. The major issue for this configuration is its large power dissipation, especially with no audio input signal. Under zero input condition, both output PWM signals have 50% duty ratio but out of phase with each other. As a result, there is always a VDD voltage drop across the load, thereby resulting in a large current flowing through the speaker load if a LPF is not present. This will lead to unwanted power dissipation even if the amplifier is in

idle mode. So a LC filter is necessary to remove the high frequency carrier and store the energy. The cut off frequency of the LPF is around the 20 kHz for the audio band. Typically, such filter can occupy about 70% of the PCB area and contribute about 30% of the total cost [7]. For highly portable applications such as smart phones and MP3 players, size is a primary concern for the design. Therefore, the filter-less architecture has been proposed to eliminate the bulky LC filter [5, 7, 8, 39-41].

Fig. 2.5. Output PWM signal of the AD modulation with zero audio input

Unlike the AD modulation, differential input PWM signals are used for the filter-less Class D amplifier instead of the differential output PWM signals. So the two PWM output signals are in phase with each other, as illustrated in Fig. 2.6. In this pattern, the voltages across the speaker load have three voltage levels, $+VDD$, $-VDD$ and ground. This ternary PWM method is called the BD modulation [38]. When there is no audio input signal, the two PWM output signals are exactly the same and theoretically, there is no current flowing through the load, as shown in Fig. 2.6(a). With this arrangement, the output LC filter can be eliminated. When the audio input is non-zero, the duty ratio for one PWM output signal will be greater than 50% while the other will be less than 50%. Since the two signals are in phase, the resultant

voltage across the load will be narrow $+VDD$ or $-VDD$ pulses, as depicted in Fig. 2.6(b). In other words, the load voltage is zero throughout most of the switching periods, and this will reduce the power dissipation substantially.

Fig. 2.6. Output PWM signal of the BD modulation (a) with zero audio input (b) with non-zero audio input

Without the LC filter, the signal transferred to the speaker will be a train of square pulses. One consideration for this unfiltered signal is the movement of the speaker cone caused by the square wave. However, the amount of cone movements at high switching frequency (typically 250 kHz) is very small since the cone movement is inversely proportional to f^2 for frequencies beyond the audio band [7]. In addition, the inductive voice coil in the speaker acts as an output filter to a certain extent [42]. The amplified audio signal is recovered mainly by the human ear, which acts as a natural BPF that passes audio signal in the frequency range of 20 Hz - 20 kHz.

Besides the size and cost advantages over the conventional Class D amplifier, it has been proven that the filter-less Class D amplifier can achieve less than 0.01% THD, which is comparable to conventional Class D amplifiers. In addition, the filter-less

Class D amplifier presents excellent power efficiency ($> 85\%$), as it reduces the power dissipation in the parasitical resistance significantly [5, 6, 40]

2.3 Digital Class D amplifier

For mobile applications, the input signal is usually in digital format. From the hardware design and power perspectives, a digital Class D amplifier is more advantageous than its analog counterpart, as no hardware intensive digital-to-analog (DAC) convertor is required, as shown in Fig. 2.7 [43]. A typical open loop digital Class D amplifier is composed of a DPWM, a power stage and a LPF, as illustrated in Fig. 2.8.

Fig. 2.7. Analog and digital Class D amplifier

Similar to analog Class D amplifier, the digital input signal is first modulated with the DPWM to produce a PWM square waveform. The output PWM waveform has a fixed frequency, but variable duty ratio ($D = T_{on}/T$), which is determined by the input signal. So the PWM waveform carries the input signal information and is used to control the output power stage. Since the amplified output waveform of the output

stage contains the input signal as well as the high frequency carrier, a LPF is needed to remove the carrier component and recovers the input signal.

Fig. 2.8. Block diagram of a digital Class D amplifier

2.3.1 DPWM

The most distinctive part of digital Class D amplifier from its analog counterpart is the DPWM. A typical DPWM process includes a sampling processor that converts the pulse code modulation (PCM) code to PWM code and a pulse generator that generates the PWM pulse according to the input PWM code.

Sampling Processor

The sampling processing in DPWM determines the digital value of the PWM pulse-width which is equivalent to the instantaneous magnitude of the input modulating signal sampled with a carrier. Three kinds of PWM sampling processing are commonly applied, namely natural sampling processing [44], uniform sampling processing [45-47] and algorithmic-based sampling processing [48-55]. Fig. 2.9

compares the sample processing results for these three kinds of processing, in which the δC and linear interpolation are two examples of algorithmic-based sampling.

The natural sampling processing, as illustrated in Fig. 2.9(a), is analogous to its analog counterpart that is implemented by comparing the signal with a fixed frequency carrier. It emulates the digital signal to analog one with high over-sampling rate, thus requires a very high clock frequency for high resolution [44]. For instance, to process a 44.1 kHz compact disc (CD) audio signal with 16-bit resolution and 380 kHz sampling frequency, it requires a $380 \text{ kHz} \times 2^{16} \approx 24.9 \text{ GHz}$ clock, which is not feasible for many audio applications. Moreover, high clock frequencies sharply increase the system power dissipation. The main advantage of this processing is the outstanding accuracy.

Fig. 2.9. Illustration of four sampling process schemes

As shown in Fig. 2.9(b), the uniform sampling process defines the pulse-width sample C directly from the regular sample B of the input signal. So the design is much simpler and the clock frequency is much lower. However, it is reported that this process exhibits high THD, of the order of 2% [44]. The THD is contributed by the mismatch of the regular sample C and the actual intercepted sample point A. Although the uniform sampling process is simple, it is not widely used nowadays due to its low accuracy.

In order to achieve high signal accuracy but lower clock frequency, the algorithmic-based processing is proposed. Examples of reported algorithmic-based processing include linear interpolation, delta-sigma and pseudo-naturally sampling. These processes, in general, are based on digital signal processing techniques. The advantages of algorithmic-based processing include high resolution, low THD and relatively lower clock frequency. However, the hardware requirements of this processing are relatively more complex resulting in higher power consumption. Linear interpolation is one simple example of the algorithmic-based sampling, as illustrated in Fig. 2.9(c). It approximates the pulse width by interpolating the adjacent input sampling points D and E . With the pair of similar triangles, it is easy to obtain that

$$T_d = T \frac{F-D}{E-D} \quad (2.9)$$

where T is the time period of one cycle and T_d is the pulse width. Notice E , D and F represent the amplitudes of the sampling points shown in Fig. 2.9(c).

So the linear interpolation is very simple and easy to implement as only straight forward addition and division are required. Another example is the δC sampling processor, which is depicted in Fig. 2.9(d). δ represents the difference between I and G, i.e. $I - G$, The core function of the δC sampling processor is to estimate the δ to get a result close to the natural sampling process. The detail derivation can be found in [48, 49] and it is given by

$$\delta \approx (H - G) \frac{(H + G)/2}{1} \quad (2.10)$$

and the pulse-width of the δC sampling processing is given by

$$T_p \approx T \left(G + (H - G) \frac{(H + G)}{2} \right) \quad (2.11)$$

The entire procedure verifies that the δC sampling processing can obtain pulse-width result close to the natural sampling process but with much lower sampling frequency and simpler computation. However, the sampling output of the δC processor is delayed with one clock because the next sampling point is involved in the calculation.

Pulse Generator

The pulse generator in DPWM generates the pulses corresponding to the digital values from the sampling processor. Based on the architectures, the pulse generators are categorized into three types, namely, the fast-clock-counter-based pulse generator [56-58], the tapped-delay-line-based pulse generator [1, 59], and the hybrid pulse generator which is a combination the above two generators [60-63].

An example of the fast-clock-counter-based pulse generator for DPWM is illustrated in Fig. 2.10. The counter is loaded by the input digital coded d at the beginning of each sampling cycle, and then counts down to generate the code-dependent pulses by comparing the output of the counter with zero [58]. So the resultant pulse-width is d/f_c , where f_c is the counter frequency as shown in the figure. The design is quite simple and an excellent linearity can be achieved in the digital-to-time domain conversion. However, an $f_c = 2^n f_s$ counter clock is required for n -bit DPWM resolution, where f_s is the sampling frequency. For a high switching frequency and a high resolution DPWM, the desired high counter frequency is the main restriction for this architecture.

Fig. 2.10. A typical fast-clock-counter-based pulse generator

A tapped delay line (TDL) is a special delay line with at least one tap. A delay line tap extracts an output signal from somewhere within the delay line [64]. A pulse generator based on this configuration is depicted in Fig. 2.11. Because the width of a given pulse from a reference clock is proportional to the number of delay cells connected in cascade, pulse generation is quantized as a function of the selected number of cells. This approach can be realized with a 2^n -to-1 multiplexer which is

controlled by the digital input code. The respective delay signal is selected to reset the output PWM signal. Although the circuit eliminates the need for high clock frequency, it requires accurate and matched delay cells. Note that the delay of each cell depends on both its supply voltage and size, factors that directly influence the output current capability and the output node capacitance, and thereby the delay. So the mismatch of the delay cells due to process variation is not unusual. Hence the digital-to-time domain conversion is nonlinear. Another drawback is the large size caused by the multiplexer and the TDL for high resolution signal [65]. For example, a pulse generator with 10-bit resolution requires $2^{10} = 1024$ delay cells, and the number of the cells would double for every additional bit.

Fig. 2.11. A tapped-delay-line-based pulse generator [65]

The solution to the disadvantages of the former two methods is the hybrid pulse generator. In this approach, a counter and a TDL is combined together to generate the PWM signal. Fig. 2.12 illustrates a 4-bit hybrid pulse generator, in which a 2-bit counter is used to provide a coarse pulse width and a 2-bit tapped delay line is

employed to generate the fine pulse width [66]. The reverse configuration is reliable, but the former configuration is preferred because the TDL can reach a much higher frequency accurately and easily than the counter-based approach. Although it has the merits in low counter frequency and small size, the hybrid approach suffers from other shortcomings like high THD. This is due to the mismatch of both sub-circuits and it has been found that the distortion is related to the degree of the hybridization of the two sub-circuits [48]. Extra block is required in order to achieve a low THD in hybrid structure design.

Fig. 2.12. A 4-bit hybrid pulse generator, together with operating waveforms [66]

The inaccuracy of the sampling processing and the pulse generation is one major source of error in Class D amplifier. Traditionally, the error can be corrected through feedback technique, but it is hard to implement feedback in a pure digital system. Other methods, like pre-compensation method such as $\Delta\Sigma$ noise shaper, have been proposed to reduce the error [67-69].

2.4 EMI Issue for Class D amplifier

EMI is an undesired disturbance that affects an electrical circuit due to electromagnetic conduction or radiation emitted from an external source or the circuit itself. The disturbance may interrupt, obstruct or otherwise degrade or limit the effective performance of the circuit [70]. EMI is caused either by the high instantaneous change in voltage (i.e. high dv/dt) or by the high instantaneous change in current (i.e. high di/dt). The rapid current and voltage variation can generate two kinds of noise, namely the conducted EMI and the radiated EMI. The conducted EMI disturbs other circuit through the connecting wires, buses, supply planes and ground planes. On the other hand, the radiated EMI affects other circuit by propagating through the free space. Usually, the conducted EMI dominates at low frequency (< 30 MHz), while the radiated EMI dominates at high frequency (> 30 MHz). Hence, the EMI regulatory standards specify conducted EMI limit from 150 kHz to 30 MHz, and the radiated EMI limit from 30 MHz to several GHz. As an example, an electronic product intended for US market must comply with FCC's EMI regulation. Fig. 2.13 shows the FCC Part 15 conducted EMI limit for Class B information technology equipment (ITE) products, which refers to products used in a residential environment [70].

Fig. 2.13. FCC conducted EMI limit for Class B devices [70]

There are two limit lines where the product under test must comply. The first limit is called the quasi-peak (QP) limit, where the EMI emission is measured by a receiver with a QP detector. The QP detector weighs the EMI signal according to its repetition rate. Another limit is called the average (AV) limit, where the emission is measured with an averaging detector of the receiver.

As mentioned earlier, Class D amplifier generates significant EMI due to its high frequency switching mode operation. To meet the required EMI regulatory limit with minimum design cost, EMI mitigation techniques during product design phase plays an important role for a highly competitive market.

The EMI generated by the switching operation during the power conversion process can be coupled to other circuits that shared the same DC power bus through conduction or directly coupled to other circuits on the same PCB through near-field coupling. It is well known that the Class D amplifier output stage is a major EMI generation source, which results in sharp spikes in both output PWM signal and the

power supply bus. These spikes will translate to a wide spectrum of harmonics in the frequency-domain and pose EMI threat to other circuits [71, 72].

2.4.1 EMI mechanism for Class D amplifier

As the typical switching frequency of the analog Class D amplifier is in the range of several hundred kHz, its emission spectrum usually falls within the conducted EMI emission range. The operating principle of the Class D amplifier output stage is depicted in Fig. 2.14. In phase one, the lower network conducts and the upper network is off. When entering the second phase, both networks are off and the body diode of the lower network is turned on. In the third phase, the upper network starts to turn on and the body diode remains conducting until the stored minority carriers are fully discharged. This reverse recovery current tends to have a sharp spiky shape in the resultant signal [9]. Since these interferences occur at the switching periods, the EMI emissions are expected to be mainly concentrated on the switching frequency and its harmonics, as reported in both analysis [72-75] and experiments [76-78].

Fig. 2.14. Recovery current noise mechanism [9]

2.4.2 Various EMI Mitigation schemes

The most straight forward EMI mitigation technique is to add a low pass passive filter after the output stage. Due to the relatively large L and C values, integration of LC low pass filter within a chip is prohibitive and off-chip LC filter becomes the only option. However, off-chip filter incurs not only the design cost but also cost in terms of area. From the cost perspective, it is more attractive to eliminate EMI at the source instead of adding EMI suppression components, such as filters and shields. Various EMI mitigation techniques for switching converters, such as DC-DC converter and AC-DC converter, have been reported, for examples, soft switching [10, 11, 79-82] and spread spectrum modulation (SSM) [12-14, 77, 78, 83-91], which directly work on the suppression of EMI caused by the high frequency switching of the output stage.

Soft switching slows down the switching transitions and as a result, reduces the transient current drawn from the power source during the transition period so that the magnitudes of high-frequency harmonics can be reduced [11]. However, with the trend of higher switching frequency, there is a limit on using such method to mitigate the EMI. On the other hand, the SSM reduces the EMI emissions by spreading the harmonics over a wider frequency spectrum, instead of concentrating the emissions in their respective harmonic frequencies, which makes it suitable for high frequency operation.

2.5 SSM

2.5.1 *Overview of SSM*

The spread spectrum technique is widely adopted in wireless communications, where the energy generated in a particular bandwidth is deliberately spread in a wider frequency range [92]. The resultant transmission bandwidth is independent of the bandwidth of the modulating signal. The spread spectrum system provides resistance to the unintentional interference and enables the multipath transmissions. This is accomplished because the spread signal behaves as Gaussian white noise due to the varying center frequencies. In general, the SSM can be categorized into direct sequence spread spectrum modulation (DSS), frequency hopping spread spectrum modulation (FSS) and hybrid spread spectrum modulation (HSS).

In the DSS, the input signal is firstly modulated by the normal modulation. After that, the spectrum of the modulated signal is spread by being directly modulated a second time using a very wideband spreading signal, as depicted in Fig. 2.15(a). For instance, a PR sequence of -1 and +1 value with the frequency much higher than the original frequency is used, thereby spreading the energy of the original input signal into a much wider band [93]. If the bandwidth of the spreading signal is larger than that of the input signal, the spread spectrum bandwidth is dominated by the spreading signal and is nearly independent of the input signal.

Fig. 2.15. Block diagram of (a) the DSS, (b) the FSS and (c) HSS

Unlike the DSS, the FSS indirectly spreads the input signal spectrum by changing the frequency of the carrier as shown in Fig. 2.15(b). So the resultant signal appears as a signal modulated carrier which is hopping from one frequency to the other, as the name stated. There are three sub-types of the FSS. The first one is the coherent slow FSS. As each spreading code here is used for k -bit data at one time, the hopping frequency band changes slower than the carrier frequency, which is referred to as slow frequency hopping. The slow frequency FSS essentially limits the hopping loss. The problem of this method is that it is quite complicate to build the frequency synthesizers that maintain the phase coherence from one hopping step to another. The second one is the non-coherent slow FSS. It is the same with the coherent slow FSS, except that it is much simpler and no effort is made to precisely recover the phases of the carriers. The tradeoff is the accuracy of the recovered signal due to the errors generated from the non-coherent carriers. The last SSM is the non-coherent fast FSS. In contrast to the slow frequency hopping, the hopping frequency band can

change many times per carrier period. However, the hopping loss for this method is severe [92].

The HSS is a combination of both the DSS and the HSS. The systems maintain the advantages of both DSS and HSS. However, the architecture is much more complex, because the input signal is modulated three times as illustrated in Fig. 2.15(c).

2.5.2 SSM for the switching mode power devices

Due to its excellent performance in redistributing the carrier energy to a wider spectrum range, the spread spectrum technique has also been extended in switching mode power (SMP) design as an EMI mitigation method since 1990s. It has been verified experimentally that the spread spectrum technique is an effective way to reduce the EMI emissions since it tackles the EMI at the source. The spread spectrum technique gains increasing research interests, and many spread spectrum methods have been reported till now [43, 83-86, 90, 94-97].

Based on the modulation schemes, these spread spectrum methods can be categorized into three types, the random pulse position modulation (RPPM), [43], the periodic spread spectrum modulation (PSSM) [83-85] and the pseudo-randomized spread spectrum modulation (PRSSM) [90, 94, 95]. For PSSM, the switching signal is modulated with a periodic modulation signals, such as a sinusoidal and a triangular waveform. The switching frequency range is determined by the frequency of the modulation signal. However, the PSSM introduces sidebands around the original frequency of the modulated signal [97]. To eliminate the sidebands in the frequency

of interest, PRSSM closely resembles the operation of true RSSM but with additional control so that it can randomly vary the switching frequency within the predefined range to avoid signal violation in the audio band [94].

RPPM

In the RPPM, the pulse position of the output PWM signal is randomized within each switching period, instead of being fully determined by the carrier frequency. However, the switching frequency for the RPPM is constant, similar to the conventional PWM scheme. So the RPPM is a DSS modulation as it directly modulates the input signal.

The RPPM is firstly implemented in Class D amplifier by Cellier *et al* [43]. In the BTL output stage configuration, there are two conditions when the differential load voltage is zero, i.e., both of the half bridge outputs are V_{DD} or ground simultaneously. In Cellier's design, these two conditions are swapped randomly in order to spread the high frequency spectrum of the output. A single random bit determines the decision of the zero swapping every half carrier period, as demonstrated in Fig. 2.16. In this manner, the pulse positions for the non-zero conditions are unaffected, and it is obvious that the PWM signal is unchanged for the BTL signal (the Out signal in the figure). From the simulation and measurement results, the high frequency spectrum components in the single PWM output, as depicted in Fig. 2.17(a), is spread, while the spectrum of the BTL signal is unchanged. Cellier *et al* also claimed that the efficiency of Class D amplifier is not significantly impacted by the spreading method, as shown in Fig. 2.17(b) [43]. However, it is worth to note that the noise

floor in the audio band is degraded by approximately 20 dB, although the authors argue that the degraded noise floor is still quite acceptable for loudspeaker applications. Another drawback is that the EMI emission in the BTL signal is not attenuated.

Fig. 2.16. RPPM modulation output PWM signals [43]

Fig. 2.17. (a) FFT of the output PWM signal with and without RPPM (b) efficiency vs. output power [43]

Fig. 2.18. (a) Sinusoidal, triangular and exponential modulation profiles (b) spectrum for the square waveform with and without PSSM [83]

PSSM

In the PSSM, the instantaneous frequency of the carrier is modulated with a time varying component that is proportional to the magnitude of the modulating signal. By definition, it is a FSS. Because the duty cycle for the switching mode devices contains the input information, the linearity of the carrier in each period is significant. As a result, the PSSM can only be realized using the slow frequency FSS. Three commonly used types of the modulation waveforms are sinusoidal profile, triangle profile and exponential profile, as shown in Fig. 2.18(a) [83]. Through this method, the initial energy of each harmonic is spread along a band of frequency (up and down the initial frequency), thus giving a wider spectrum with lower EMI peaks. Fig. 2.18(b) illustrates the spectra comparison of a pure sinusoidal signal with frequency f_c , and the same signal modulated by a sinusoid profile with a certain Δf_c . Balcells *et al* [83] derives two useful parameters to describe the characteristics of the PSSM. They are the modulation index m_f and the rate of the modulation δ , given by

$$m_f = \frac{\Delta f_c}{f_m} \quad (2.12)$$

$$\delta = \frac{\Delta f_c}{f_c} \quad (2.13)$$

where Δf_c is the peak deviation of the carrier frequency and f_m is the modulating frequency. The energy of harmonic components is spread into the band, which is described by

$$B_h = 2(f_m + \Delta f_c \cdot h) \quad (2.14)$$

where h is the order of harmonic components. Since the carrier frequency f_c is normally fixed, the spread band and the peak attenuation are proportional to δ and h . Also notice that high δ may be helpful in attenuating the lower order harmonics, but may cause overlapping at higher harmonics as illustrated in Fig. 2.18(b). Although the resultant spread spectrum is similar to each other, the triangular profile provides the maximum reduction of the whole envelop of the EMI spectrum under the same frequency condition. Nevertheless, the exponential profile is an easy method to cancel certain frequency and is less sensitive to the harmonic band overlap. However, the sinusoidal waveform is the easiest one to be implemented and analyzed.

The reported PSSM has presented two advantages. First, the PSSM provides control on the spread band. This is very important to the audio amplifier, because noise in the audio band should be avoided. The spread band shape and the maximum attenuation for certain profile and modulating frequency is fixed and proved by both analysis and experiments. The main drawback is the overlap of the spread band for higher order harmonic components, which reduces the EMI reduction benefits of the PSSM. Another obstacle that stops the PSSM from being implanted in the audio devices is the low modulation frequency f_m . As discussed above, the PSSM is a method of slow frequency FSS, thus f_m should be much smaller than f_c . In this case,

the modulating frequency may create an in-band inter-modulation distortion with the fundamental audio signal, or even worse since it falls into audio band. To our best of our knowledge, no Class D amplifier with PSSM has been reported in literature.

PRSSM

The PRSSM is proposed for the SMP devices and investigated in [87, 90, 94, 98]. Similar to the PSSM, the PRSSM is a slow frequency FSS. But the carrier frequency is modulated with randomized code instead of a periodic profile. It is achieved by digitally controlling the supply voltage or supply current of the carrier generator. True randomized SSM is difficult to realize in practice because the switching frequency is hopped in the entire spectrum. It is also not preferred for audio applications due to its uncontrollable switching frequency range. For this reason, the PR code is used. The PRSSM imitates the operation of the true randomized SSM but with additional control so that it can randomly vary the switching frequency within a predefined range to avoid signal violation in the audio band.

The PR code is usually realized using the digital methods. Fig. 2.19 depicts one method reported by [78, 89, 90]. The generator consists of 17 D flip-flop, 2 XOR and 3 inverters. It can create thermal code from zero to eight randomly. The frequency hopping is realized in terms of changing the frequency by altering the charge and discharge currents discretely in the fixed frequency intervals. Fig. 2.20 shows the spectrum comparison for the PWM output signal with fixed carrier frequency and that with PR carrier frequency. The authors show that the PRSSM can achieve 12dB reduction of EMI emission. However, the authors have not investigated the side

effects of PRSSM on THD and power efficiency, which are the important parameters for audio amplifiers. Normally, the PR code is uniformly distributed. In [99], it noted that the PR code with triangular distribution has a better EMI mitigation performance. The PR code with triangular distribution can be simply realized by summing two random numbers.

Fig. 2.19. Block diagram of the PR code generator [78]

Fig. 2.20. Spectrum for (a) the fixed carrier frequency and (b) carrier frequency with PRSSM [78]

Comparison and Summary

As mentioned above, the resultant BTL signal is unchanged in the RPPM. It is restricted by the fact that the duty cycle of the PWM signal contains the input signal information instead of the carrier periods. In comparison to the RPPM, both the PSSM and PRSSM are slow frequency FSS. The carrier frequency is modulated rather than the duty cycle. There are two main differences between these two modulation schemes. Firstly, the spectrum of the carrier frequency with PSSM is a continuous wider spectrum band, while that of the carrier frequency with PRSSM is

discrete in frequency steps. Secondly, there is a large energy at the frequency of the modulating profile for the PSSM, which might affect the audio band performance. On the other hand, the frequency spectrum of the PR code is similar to the white-noise and is covered by the existing noise floor for the PRSSM.

For the random modulation scheme RPPM and PRSSM, the voltage spectrum is random and different for different time intervals. So the power spectral density (PSD) should be used instead of the voltage spectrum, according to the random process theory. In particular, the autocorrelation function of a random process is the appropriate statistical average, concerning the characteristics of the random signal [87]. The characteristics for the different spread spectrum schemes and the normal PWM scheme are tabulated in Table 2.1.

In summary, the PRSSM is a more suitable spread spectrum scheme for audio applications. Hence, this thesis explores the use of pseudo-random technique for carrier frequency modulation and investigates its effectiveness for EMI reduction in both analog and digital Class D audio amplifiers.

Table 2.1. CHARACTERISTICS OF DIFFERENT SPREAD SPECTRUM SCHEMES

Modulation	Switching Period	Pulse Width	Pulse Position
PWM	Constant	Varied	Fixed
RPPM	Constant	Varied	Pseudo-Random
PSSM	Periodic	Varied	Fixed
PRSSM	Pseudo-Random	Varied	Fixed

Chapter 3

Analog Class D

Amplifier with PRCFM

This chapter presents a high-efficiency filterless Class D amplifier with PRCFM. The proposed PRCFM is realized by a clock divider and a LFSR, which is highly hardware efficient over conventional Class D amplifier with LC filter. In addition, the proposed Class D amplifier incorporates a peak detector to improve the power efficiency at low input power range. For the proposed PRCFM, the first order estimation for EMI reduction is described and means to reduce noise floor in audio band are also suggested. The proposed Class D amplifier with PRCFM is designed and integrated into a single chip with a size of 1 mm x 1 mm using 0.18 μ m CMOS process technology. The experimental results have demonstrated excellent EMI emission reduction, THD performance and power efficiency over both interested modulation index range and audio band.

3.1 Filter-less Class D amplifier architecture

Fig. 3.1 shows the proposed filterless Class D amplifier with PRCFM. It consists of four major building blocks, a carrier generator with PRCFM, a modulation circuit, a high-bridge output stage and a differential-to-single feedback network.

The proposed filterless Class D amplifier adopts the low voltage and chip area efficient architecture in [5]. The double-sided natural sampling PWM scheme eliminates common-mode distortion in the audio band. It utilizes an internally generated triangular waveform and a differential input signal pair. The single ended input signal, together with a feedback signal, is first fed into a pre-amplifier to generate the differential input signals. The outputs are subsequently connected to a summing integrator, which removes the high frequency residual in the feedback signal further. The results and the internally generated triangular waveform are compared by the two comparators to generate the nature sampling PWM signals as illustrated in Fig. 3.2. The frequency of the triangular waveform is controlled by the PRCFM. The output of the comparator goes high when the input signal is higher than the triangular waveform and vice versa. Since the input signals are differential in nature, the PWM waveforms (indicated as OUTP and OUTN) generated at the output of the two comparators are in phase but having different duty ratios. As a result, the voltage across the speaker is made up of narrow pulses. Hence, the speaker is only loaded when needed to ensure low power consumption.

Fig. 3.1. Block diagram of the proposed Class D amplifier

Fig. 3.2. Waveforms for the inputs, triangular signal, and differential signal across the speaker

3.2 Feedback network and summing integrator

To improve THD and gain linearity of the Class D amplifier, a common negative feedback mechanism as depicted in Fig. 3.3 is employed to attenuate the high frequency carrier. The feedback network is a second-order differential-to-single ended active LPF. The LPF is used to attenuate the high frequency carrier. However, a significant residue is still present on the feedback signal which causes distortion [100]. To reduce the distortion, a third-order integrator, as shown in Fig. 3.4 is employed to further attenuate the residue carrier signal. The third-order integrator is realized by cascading three first-order integrators together and the transfer function is given by:

$$H = \frac{R_f}{R_i} \cdot \frac{1}{(1 + 2\pi R_f C_f S)(1 + 2\pi R_{f1} C_{f1} S)(1 + 2\pi R_{f2} C_{f2} S)} \quad (3.1)$$

The pass band of the closed-loop response is designed to be flat in the audio band. The op-amp used here is designed in folded cascode configuration to provide a high

gain and to ensure that it is able to operate at a low supply voltage. The gain of the op-amp is around 80 dB to ensure high supply ripple rejection.

Fig. 3.5 shows the loop gain and phase responses of the close-loop Class D amplifier. The phase margin and gain margin are found to be 55° and 13 dB, respectively, which are deemed as an indication of stability of the designed high order amplifier.

Fig. 3.3. Second order low pass filter feedback network

Fig. 3.4. Summing integrator

Fig. 3.5. Loop gain and phase response for the designed closed-loop Class D amplifier

3.3 Peak detector

In typical audio applications, the crest factor of the audio signal can be as large as 15dB. Hence, the average signal of the audio signal is about 20% to 30% of full swing. The Peak Detector is introduced here to improve the power efficiency of the Class D amplifier when the modulation index (or input signal swing) is low.

The power loss of the Class D amplifier output stage due to switching capacitance is given by:

$$P_d \approx \frac{1}{2} C \cdot V_{DD}^2 \cdot f \quad (3.2)$$

where C is the output capacitance, V_{DD} is the supply voltage and f is the switching frequency.

The capacitance C is dominated by the parasitic capacitance of the output stage transistors. Since the sizes of the power PMOS and NMOS are designed in accordance with the “on” resistance of the transistors, the capacitance C cannot be reduced easily. Similarly, V_{DD} is usually chosen to meet the design specification. To reduce the power loss at low signal swing, the frequency of the switching frequency can be reduced when the magnitude of the signal swing falls below a predetermined threshold.

In the proposed Class D amplifier, this switching frequency control can be realized by a peak detector with a voltage-to-current converter, as shown in Fig. 3.6. The switching frequency reduces accordingly when the magnitude of the input signal is at a very low level or when the amplifier is in idle mode. This mechanism can be achieved by extracting the magnitude of the input signal through a peak detector circuit.

Fig. 3.6. Peak detector with voltage to current converter

The peak detector, which consists of M1, R1 and C1, samples the peak of the input signal and holds it for a certain period of time. The low pass filter, R2 and C2, then smoothens the output signal of the peak detector before it feeds to the converter. The sampled peak voltage is subsequently converted to the necessary current, through M2, to change the carrier frequency. The remaining part of the circuit is used to set the offset current as the input signal is always sitting on a reference DC voltage.

From the measurement results shown in Fig. 3.7, the switching frequency remains low (around 80 kHz) for low input and idle modes ($V_{pp} < 0.5$ V), to reduce power consumption. Since 80 kHz is four times of the audio range, it still satisfies the Nyquist theorem. The switching frequency increases linearly when the input signal voltage V_{pp} exceeds 0.5 V. Note that the switching frequency is tunable by setting the size of the M2.

Fig. 3.7. Switching frequency vs. input peak voltage

3.4 Carrier generator with PRCFM

Similar to the ordinary carrier generator, the triangular carrier waveform here is created by charging and discharging a capacitor, as depicted in Fig. 3.8 (upper part). The frequency of the carrier waveform can be adjusted by varying the charging current. The spreading frequency range is determined by the varying range of the current, which is realized and digitally controlled by the weighted PR binary number. Fig. 3.8 (lower part) shows the schematic circuit of the PR number generator. It consists of an 8-bit clock divider and a 5-bit LFSR, which contains an array of registers with linear feedback circuit implemented using a XNOR gate. Both the clock divider and shift registers are implemented by D flip-flop. The input clock frequency f of the generator is the same as the carrier signal. In this way, the frequency is hopped at the end of carrier period if the path delay can be eliminated, to maintain good carrier linearity, which is significant for the THD performance. The 8-bit clock divider first divides the input clock f to $f/28$. This substantially reduces the operating frequency of the LFSR and thus the frequency of frequency hopping. Hence, each switching frequency step would be sustained for $2^8 = 256$ carrier cycles. It will be shown in the later section that this design helps to improve noise performance in the audio band. The 5-bit LFSR subsequently generates 5-bit PR numbers. The 5-bit LFSR is connected such that the third and fifth register outputs are passed through the XNOR and then fed back to the first register, so that maximum PR sequence length ($2^5 - 1$) is obtained. In this case, 31 PR binary numbers (i.e. $2^5 - 1 = 31$) are generated and a 3-bit PR number is used to control the charging current.

Ideally without switching loss, the total energy of all the spread switching frequency steps is equal to the energy for one constant switching frequency. Assuming that the energy is uniformly distributed to all spread switching frequency steps, the resultant peak power noise can be calculated by first order estimation:

$$20 \log V_s = 20 \log \frac{V_T}{2^s} \approx 20 \log V_T - 6.02s \quad (3.3)$$

where V_s and V_T are the peak output amplitudes of the amplifier with and without PRCFM; and s is the number of the control bits.

If the switching frequency is spread to s different frequency steps, an EMI reduction of $6.02s$ dB is expected. Practically, the value of s is limited by the order of the LFSR for a certain design. For the proposed design, $s = 3$.

Fig. 3.8. Carrier generator with PRCFM

However, the output of the LFSR is actually not truly randomized to some extent and some periodic signals are present in the random number sequence. The nominal frequency of the periodic components is $f/2^{(n+m)}$, where f is the input switching frequency, n is the order of the LFSR, and m is the order of the frequency divider. To make matters worse, the resultant periodic frequency steps may fall into the audio band and this will increase the noise floor. Fig. 3.9 shows the relationship between the noise floor and the number of PR bits used if the clock divider is not present. It shows the relationship between the noise floor and the nominal operation period of the LFSR. Note that the noise floor in the audio band increases when the number of PR bits increases (i.e. the nominal period increases), as illustrated in Fig. 3.9. This trend is reasonable, as the nominal periodic frequency of the LFSR is closer to the audio band for higher order LFSR. On the other hand, a high order LFSR will result in more complex circuit implementation but better EMI reduction. To overcome this conflict, a frequency divider is added to optimize the noise and EMI reduction performance by further pushing the nominal periodic frequency out of the audio frequency range. For example, the nominal periodic frequency for this 8-bit divider design is about 24 Hz. It may be worthwhile to note that the noise floor can be further improved with a longer hopping period and be closed to that of the conventional amplifier eventually.

Fig. 3.9. Noise floor vs. frequency hopping period

Fig. 3.10. Generated one bit PR number

Fig. 3.10 demonstrates the generated one-bit PR number. It is pseudo-randomized and is only predictable with known initial state. Fig. 3.11 shows the switching frequency step and time period corresponding to each digital number for the designed PRCFM. The time period for each frequency step is estimated using $\Delta t \approx 1/(f/2^8)$. As a result, the frequency step is not uniformly distributed in time as illustrated in Fig. 3.11. Although uniform distribution can lead to an optimal design[101], taking into consideration the circuit complexity and spectrum spread,

non-uniform distribution manner is adopted in this design. It is due to the consideration of the THD issues and good noise reduction performance for a deviation from the uniform distribution.

Fig. 3.11. Switching frequency and corresponding time period vs. PR number

3.5 Comparator

As discussed above, the comparator is used to generate the PWM signal by comparing the instantaneous magnitude of the input audio signal and the carrier. Fig. 3.12(a) depicts the schematic diagram of the designed comparator. In order to maximize the dynamic range of the amplifier, the input of the comparator is designed to operate rail-to-rail. The cross coupling configuration is employed to provide fast and correct comparison because this is important for THD performance. Moreover, the wide swing structure is used to increase the immunity to the supply noise. Fig. 3.12(b) demonstrates the transient output response of the comparator, for V_{INN} is fixed at half V_{DD} and V_{INP} is fed by a square waveform. The sharp rising ($t_r = 10.586$

ns) and falling ($t_f = 7.821$ ns) edges of the output waveform shows that the designed comparator has the ability to perform fast switching operations.

Fig. 3.12 (a) Schematic diagram of the comparator and (b) its transient output response

3.6 Output Stage

The BTL configuration is used for the output stage for BD modulation. The main design consideration here is the drive capability. As the target load is $8\ \Omega$ and the output supply voltage is 3.3 V, the average load current is $3.3/8 = 0.4125$ A. Meanwhile, there is large parasitic pad and load capacitor, which is around 8 pF. As a result, an output configuration with four inverter chains is designed, as depicted in Fig. 3.13(a). The W/L ratio of PMOS and NMOS for each stage increases gradually, so that the output inverter chain has large drive capacitive but with minimum delay. The “ON” resistances for the PMOS and the NMOS are around 580 m Ω and 570 m Ω , respectively. Fig. 3.13(b) demonstrates output PWM waveforms with 250 kHz clock input signal. The signals in each stage have equal rise and fall time, which is around 1 ns.

Fig. 3.13. (a) Output inverter chain and (b) simulated output PWM waveforms

3.7 Measurement results

The proposed filterless Class D amplifier with PRCFM is designed and fabricated using CSM 0.18 μm CMOS process. To access the effectiveness of the PRCFM for EMI emission reduction, a control pin is added to the design to enable or disable the PRCFM function.

The conducted EMI measurement setup is shown in Fig. 3.14, in accordance with Comité International Spécial des Perturbations Radioélectriques (CISPR) 22 [102]. The Class D amplifier is powered by a DC source through the line impedance stabilization network (LISN) and the conducted emissions from the Class D amplifier are measured from the RF output of the LISN using the Advantest R3261C spectrum analyzer with R3551 pre-selector. Fig. 3.15 shows the measured conducted emissions from 150 kHz to 30 MHz. Without the PRCFM, conducted emissions at the carrier frequency of 215 kHz and its harmonics are clearly observed. With the PRCFM, the conducted emissions at the carrier and its harmonics are well spread with a spectrum

range of 24 kHz, which is about 10% of the nominal carrier frequency (215 kHz). By comparing the measurement results with and without PRCFM, it is clearly observed that conducted emissions with PRCFM are lower than those without PRCFM. Without PRCFM, the fundamental component has exceeded the CISPR 22 Class B limit and several harmonics at the lower frequency end are very close to the limit. With PRCFM, the emissions are well below the limit with very comfortable margin. The reduction of the emission of the fundamental component is about 15 dB, which correlates well with the theoretical expectation ($6.02 \times 3 = 18.06$ dB). The slight deviation is expected due to the switching loss. It is worth noting that further EMI reduction is achievable by using more frequency hopping steps, if needed.

Fig. 3.14. Setup for conducted emission measurement

Fig. 3.15. Conducted emission with and without PRCFM

The measurement setup for near-field radiated emissions is shown in Fig. 3.16. The near-field emission measurement is performed with a Dectetus AB near-field EM scanner system and measured with a Langer EMV-technik magnetic near-field probe. The probe is connected to a HP 8563E spectrum analyzer through a preamplifier (PA303). The measurement is split into two frequency bands, 150 kHz to 30 MHz and 30 MHz to 1 GHz with 9 kHz and 120 kHz measurement bandwidths, respectively.

Fig. 3.17 shows the near-field emissions emitted from the test chip with and without the PRCFM, in the frequency band 150 kHz to 30 MHz. It shows that the near-field radiated emission at the fundamental frequency is reduced by nearly 15 dB, which is consistent with the theoretical estimation. The measurement results also indicate that PRCFM is effective to reduce the near-field EMI coupling to other circuits that are in

the vicinity of the Class D amplifier, which is an added merit in view of the continuing trend of high density integration on the PCB.

Fig. 3.16. Setup for near-field radiated emission measurement

Fig. 3.17. Signal spectrum 150 kHz to 30 MHz of near-field radiated emission for both amplifiers

Fig. 3.18 shows the measured near-field radiated emissions of the Class D amplifier without and with PRCFM for 30 MHz to 1 GHz range. At frequency above 30 MHz, the near-field emissions decay significantly and no visible emissions are detected with the PRCFM enabled.

With an input sinusoidal signal of 1.8 V_{pp} at 1 kHz, the measured output waveforms of the proposed filterless Class D amplifier are shown in Fig. 3.19. Fig. 3.19(a) shows the positive and negative PWM output for each half-bridge output stage as well as the typical ternary-state PWM output waveform over the load, whereas Fig. 3.19(b) illustrates the demodulated audio output if a single stage LC LPF (which act as the human ear) is connected to the output.

Fig. 3.18. Signal spectrum 30 MHz to 1 GHz of near-field radiated emission for both amplifiers

Fig. 3.19. Output waveforms (a) ternary modulated signal and (b) audio output signal

Fig. 3.20 shows the THD performance comparison over the input modulation index range (0.4% - 95%) for 1 kHz input sinusoidal signal. The THD measurement results for the proposed circuits is well below 0.07% but larger than the simulation results. This is probably due to the non-idealities of the components. It is also noted that the THD performance of the proposed circuit does not degrade as compared to that of its normal filterless counterpart. In general, all the THD performance improves when the modulation index increases. This is because the switching frequency is lower when the modulation index of the input signal is smaller. However, the THD is still less than 0.04%, thereby showing that the peak detector does not degrade the performance of the THD.

Fig. 3.20. THD performance over full different input modulation index with input signal frequency of 1 kHz

Fig. 3.21. Four corner simulations comparison for a 1 kHz input frequency and 0.81 modulation index

Fig. 3.21 compares the typical simulation result of four corners for a 1 kHz input frequency and 0.81 modulation index. The worst case THD result happened at sf corner. However, the variation is within 0.01%, which is acceptable.

Fig. 3.22 summarizes the THD performance, obtained from both simulation and measurements, over the audio band (100 Hz - 6 kHz) at 0.81 modulation index. The results show that all the THDs are well below 0.09%. The THD performance for the proposed circuit does not degrade compared to that of its counterpart. In addition, the measurement results are consistent with the simulation results, where the differences are within 0.02%. As expected, the THD performance degrades when the frequency of the input signal increases.

Fig. 3.22. THD performance over different input frequencies with input modulation index of 0.81

In conclusion, the THD performance of the proposed Class D amplifier with PRCFM is good enough for typical audio applications.

Fig. 3.23 shows the PSRR comparison between the amplifier with and without PRCFM. A constant input signal is applied to generate 50% duty ratio PWM. A sinusoidal noise signal is injected to the power rail to simulate the supply noise condition. The results cover the audio frequency range from 100 Hz to 20 kHz. The results show that practically the PSRR is not affected by the PRCFM circuit, except marginal difference at lower frequency range.

Fig. 3.23. PSRR of VDD for both amplifiers

Fig. 3.24 shows the power efficiencies of the amplifiers for varying output power. The efficiency performance is measured with 1 kHz sinusoidal input waveform. Both amplifiers achieve $> 86\%$ efficiency, even for output power as low as 58 mW. For comparison, Fig. 3.24 also compares the power efficiency of the amplifier without the peak detector. As expected, the power efficiency of the amplifiers with peak detector is much better than that without the peak detector at low power range. The power efficiency of the proposed amplifier with PRCFM is slightly poorer than that of the normal one at low output power because the PRCFM circuit of the proposed amplifier dissipated some power.

Fig. 3.25 depicts the micrograph of the designed circuit using CSM 0.18 CMOS process. It occupies a total area of $1\text{mm} \times 1\text{mm}$, including pads. The PRCFM and peak detector circuits are labeled as blocks A and B, respectively. It is worthy to mention that the PRCFM and the peak detector circuits occupy less than 1% and 4%

of the total chip area, respectively. Fig. 3.26 shows the printed circuit board (PCB) of the test circuit. A performance comparison with other recently published Class D amplifier designs is tabulated in Table I. In the table, note that the chip size is including the pads, and the THD results are for a 1 kHz input sinusoidal waveform. From the table, it can be seen that the proposed design has better EMI emission reduction and power efficiency performances.

Fig. 3.24. Power efficiency over wide output power range

Fig. 3.25. Micrograph of the proposed Class D amplifier

Fig. 3.26. PCB for testing

Table 3.1. PERFORMANCE COMPARISON

	[6]	[103]	[5]	[77]	[78]	This work
Process	AMI 0.5 μm	90 nm	BiCMOS 1.2 μm	TSMC 0.35 μm	CSMC 0.5 μm	CSM 0.18 μm
Chip size (mm^2)	1.49	< 0.44	1.5 x 1.5	1.8 x 1.8	1.5 x 1.5	1 x 1
Spread spectrum circuit size (μm^2)	-	-	-	-	191 x 251	48 x 219
Topology	AD	BD	BD	AD	BD	BD
Supply voltage (v)	2.7	1.5	2.5 - 6.5	1.5	3.6	3.3
Switch frequency (kHz)	450	410	250	500 & 1000	300	80 - 270
Frequency variation (%)	-	-	-	$\sim \pm 8$	± 20	± 10
Load (Ω)	8	8	8	8	8	8
Output filter	Yes	No	No	Yes	No	No
Peak detector	No	No	No	No	No	Yes
THD (%)	0.02 – 0.25	0.03 - 0.05	0.04 - 0.4	0.05 - 0.2	0.03 - 0.1	0.05 - 0.09
Output power (W)	0.1 – 1.28	0.05 - 0.38	0.05 – 2.5	0.1 - 0.28	0.05 - 0.2	0.05 - 0.7
Power efficiency (%)	70 - 89	45 – 75	50 - 86	78 - 92	70 - 90	86 - 90
EMI reduction (dB)	-	-	-	~ 13.5	12	~ 15

3.8 Summary

A filterless Class D amplifier with pseudo-randomized carrier frequency modulation (PRCFM) scheme has been designed and realized using CSM 0.18 μm CMOS process with the objective of EMI mitigation. The proposed PRCFM circuit occupied less than 1% of total chip size and it features a higher power efficiency at low output power range with the use of a peak detector.

Measurement results have demonstrated that the proposed filterless Class D amplifier with PRCFM is effective in reducing the both conducted and near-field radiated EMI emissions by as high as 15 dB. By increasing the frequency hopping period, the noise floor due to inter-modulation in the audio band can be significantly reduced for the proposed Class D amplifier, which preserves good THD performance even though the carrier frequency has been pseudo-randomized modulated.

Chapter 4

Digital Class D Amplifier

with PRCFM

This chapter extends the implementation of PRCFM to digital Class D amplifier, which has become highly popular in digital mobile applications. Compared to its analog counterpart, it expects to emit higher EMI, as the digital circuit operates at much higher frequency, usually in the range of tens of MHz. Hence, effective EMI mitigation is even more important. On the other hand, the main challenge of implementing PRCFM in digital Class D amplifier is to maintain good THD performance because the sampled input data is highly related to sampling frequency in digital Class D amplifier. Therefore, a new sampling algorithm is proposed for the DPWM. The proposed architecture is firstly simulated in Simulink, then implemented in FPGA and finally verified experimentally.

4.1 Operation principle

Fig. 4.1 shows the block diagram of the proposed digital Class D amplifier with PRCFM. It has five major circuit modules, namely $\Delta\Sigma$ noise shaper, DPWM, PRCFM, output stage and LPF. The input signal, which is in 48 kHz 16-bit CD format PCM, is assessed by the 2nd order $\Delta\Sigma$ noise shaper. The 10-bit output signal of

$\Delta\Sigma$ noise shaper is subsequently modulated by DPWM, which consists of a novel algorithmic sampling processor and the hybrid pulse generator. The sampling processor re-samples the input signal with an internal carrier signal and then the pulse generator creates the PWM pulse accordingly. The output of the DPWM is fed into the power stage for amplification. Eventually, the input signal is reconstructed with LPF, where its cut-off frequency is 20 kHz. The re-switching frequency and the sampling frequency are controlled by the PRCFM, which hops the frequencies according to the digital control circuit.

Fig. 4.1. Block diagram of proposed Class D amplifier

4.2 Noise shaper

The input signal for the design circuit is a 16-bit PCM which samples at a rate of 48 kHz, and corresponds to a frequency resolution of about 3.15 GHz. To avoid using an excessive frequency rate for PWM generation, a $\Delta\Sigma$ modulation is employed before the DPWM. The aims of this modulation are:

- Oversample the input signal to increase the linearity of the signal;
- Reduce the resolution of the input signal from 16-bit to 10-bit, which significantly reduces the frequency of DPWM to enable ease of realization; and
- Shape the noise over the audio band.

The choices of over sampling ratio (OSR), the order of $\Delta\Sigma$ modulation, the architecture of modulation and the output resolution depend on the optimization of the performances, complexity and noise transfer function (NTF) required by a specific application. In this design, a 2nd order cascaded resonator feedback (CRFB) 10-bit structure with OSR of 16 is designed, as shown in Fig. 4.2. With this design, the NTF is

$$\text{NTF} = \frac{1}{1 + \frac{a_1}{a_0}z^{-1} + \frac{a_2}{a_0}z^{-2}} \quad (4.1)$$

where $a_0 = 0.1081$, $a_1 = 0.5585$ and $a_2 = 0.2162$.

And the output signal-to-noise ratio (SNR) can be shown as

$$\text{SNR(dB)} \approx 6.02Q + 1.76 + 20 \log(M) - 10 \log\left(\frac{\pi^{2L}}{2^{L+1}}\right) + (2L + 1)10 \log\left(\frac{f_s}{2f_B}\right) \quad (4.2)$$

where Q is the number of output bits, M is the modulation index, L is the order of the $\Delta\Sigma$ modulation and f_s/f_B is the oversampling ratio.

For $M = 1$, the theoretical peak SNR is about 94.22 dB, which is good enough for most applications [104-106].

Fig. 4.2. Block diagram of designed 2nd-order $\Delta\Sigma$ noise shaper

Fig. 4.3. Output spectrum of the designed $\Delta\Sigma$ noise shaper

Fig. 4.4. Predicted and simulated SNR of the designed $\Delta\Sigma$ noise shaper

Fig. 4.3 shows the output spectrum of the modulation. The results show that the noise is well pushed out of the audio band. Fig. 4.4 compares the simulated and predicted SNR of the $\Delta\Sigma$ noise shaper with regard to the input level. It shows that the simulated results match well with the predicted results and the peak SNR of 90 dB is achievable, which is good enough for most of portable audio applications.

4.3 PRCFM

The proposed PRCFM in the design performs the following functions:

- Generate the pseudo-random TDL frequency steps; and
- Generate the corresponding switching frequencies for the pulse generator as well as the re-sampling frequencies for the sampling processor.

The PRCFM circuit is designed based on frequency hopping technique. The working principles of the major sub-circuits will be explained in this section.

Fig. 4.5. Block diagram of PRCFM

The proposed PRCFM circuit spreads the signal spectrum by PR frequency hopping method. It includes three main sub-blocks, namely LFSR, frequency selector and frequency divider. The block diagram of the designed PRCFM is shown in Fig. 4.5.

Similar to the frequency hopping spread spectrum method in the telecommunication system, a LFSR is employed to generate a PR code for selecting the respective TDL frequency step in a frequency selector. Then the resultant TDL frequency is passed to a frequency divider to generate the corresponding re-sampling frequency and switching frequency. In addition, a LFSR clock is also generated in the frequency divider to trigger the LFSR operations.

In random spread spectrum system, the periodic PR codes are commonly employed instead of an infinite random sequence because the infinite random sequence might spread switching energy to the interested band. The PR codes can be generated by LFSR, where the feedback logic consists of modulo-2 adders entirely. The addition rules for the modulo-2 adder are defined in Table 4.1. This addition can be accomplished electronically using an exclusive-OR gate.

Fig. 4.6 shows the 5-bit LFSR configuration. The various boxes represent shift registers and the circle with “+” represents modulo-2 adder. At each clock cycle, the content in each shift register moves to the right by one unit. The last shift register content is fed back to the first one as well as the third unit through the modulo-2 adder, thereby preventing the shift register from emptying, i.e. all the shift registers should not contain zero.

Table 4.1. MODULO-2 ADDITION

+	0	1
0	0	1
1	1	0

Fig. 4.6. 5-bit LFSR configuration

As the feedback symbol and the produced results of the feedback logic would be zero all the time for zero state, the shift register would then continue to remain in the zero

state, and therefore output a constant code. As a result, a PR sequence produced by n -bit LFSR cannot exceed $2^n - 1$ states. For 5-bit LFSR, there will be 31 states. The PR sequence with $2^n - 1$ states for n -bit LFSR is called the maximum length sequence (M-sequence).

The M-sequence PR code is desirable in spread spectrum system since it has many properties of an infinite random binary sequence. For instance, the autocorrelation function of an M-sequence is periodic and binary valued. Moreover, the M-sequence becomes much more similar to the random binary sequence as the shift register length in LFSR is increased.

Not all the LFSR can be employed to generate an M-sequence PR code. The feedback logic in the LFSR determines the length of the output sequence. The connections for the M-sequence feedback logic can be found by the theory of error control codes. Fortunately, an extensive table of the necessary feedback connections for varying LFSR length is available [107] and part of it is shown in Table 4.2. The numbers in the brackets indicate the shift register number for the inputs of the modulo-2 adders.

Table 4.2. FEEDBACK LOGIC IN LFSR FOR M-SEQUENCE

Shift Register length	Feedback Logic
3	[3,1]
4	[4,1]
5	[5,2] [5,4,3,2] [5,4,2,1]
6	[6,1] [6,5,2,1] [6,5,3,2]

Fig. 4.7. 5-bit LFSR in Simulink

Due to the requirements of the LFSR in the PRCFM circuit, the higher shift register length is preferred in order to get a more noise-like frequency distribution. However, the circuit cannot achieve large frequency steps because of the frequency selector and frequency divider limitations. To achieve a balance between these constraints, a shift register length of five is chosen, which gives a 31 M-sequence PR code.

Fig. 4.7 illustrates the implemented circuit of the 5-bit LFSR in Simulink. The J-K flip-flop is used as a shift register when it is connected as a D flip-flop. The modulo-2 adder is realized by an exclusive-OR gate. The circuit is connected in according to the block diagram in Fig. 4.6, where the feedback logic is [5, 2]. The configuration has an advantage over the other two types of feedback logic for 5-bit LFSR, as it requires fewer feedback connections. An inverter is inserted between the clock and the flip-flops as each flip-flop is negative-edge triggered. The outputs of all the five flip-flops are extracted to form a 5-bit binary PR code by a built-in multiplexer (MUX).

Table 4.3. M-SEQUENCE GENERATED BY THE DESIGNED 5-BIT LFSR

Clock cycle	Feedback Symbol	State of LFSR				
		1(MSB)	2	3	4	5(LSB)
0		1	0	0	0	0
1	0	0	1	0	0	0
2	0	0	0	1	0	0
3	0	0	0	0	1	0
4	0	0	0	0	0	1
5	1	1	0	1	0	0
6	0	0	1	0	1	0
7	0	0	0	1	0	1
8	1	1	0	1	1	0
9	0	0	1	0	1	1
10	1	1	0	0	0	1
11	1	1	1	1	0	0
12	0	0	1	1	1	0
13	0	0	0	1	1	1
14	1	1	0	1	1	1
15	1	1	1	1	1	1
16	1	1	1	0	1	1
17	1	1	1	0	0	1
18	1	1	1	0	0	0
19	0	0	1	1	0	0
20	0	0	0	1	1	0
21	0	0	0	0	1	1
22	1	1	0	1	0	1
23	1	1	1	1	1	0
24	0	0	1	1	1	1
25	1	1	0	0	1	1
26	1	1	1	1	0	1
27	1	1	1	0	1	0
28	0	0	1	1	0	1
29	1	1	0	0	1	0
30	0	0	1	0	0	1
31	1	1	0	0	0	0

The initial value stored in the flip-flops can be any arbitrary 5-bit binary number except “00000” and the selection will not affect the sequence length. The initial value is chosen as “10000” for the given design. The theoretical evolution of the PR M-sequence generated by this configuration is tabulated in Table 4.3. Fig. 4.8 is the Simulink simulation results at 10 Hz operating frequency and are consistent with the theoretical results. Both results have proven that the LFSR returns to the initial state “10000” after 31 clock cycles and a non-repeated 31 M-sequence PR code is generated.

Fig. 4.8. Simulation result for 5-bit LFSR at 10Hz

The frequency selector in the PRCFM converts the generated PR codes to the respective frequencies, which are pre-defined to prevent them from overlapping in the interested frequency band. There are two major design issues to be considered. Firstly, the linearity of the PR code and its corresponding frequency and secondly, the phase coherence in frequency hopping. Both issues can result in performance degradation in the frequency selector.

Two types of frequency selectors are realized in Simulink. The first one is based on the multiple clock generators, while the second one is based on voltage controlled oscillator (VCO); and their block diagrams are shown in Fig. 4.9 and Fig. 4.10, respectively. In order to minimize the effect of the phase coherence, the input data in both designs is simultaneously sampled at the frequencies related to the selected output frequency to make frequency hopping happen at the end of each clock cycle. The phase non-coherence nevertheless still exists due to finite delay in the circuits.

Fig. 4.9. Frequency selector based on multi clock generator

Fig. 4.10. VCO frequency selector

The first design emulates the frequency selector structure that includes one fundamental clock generator with a digital controlled frequency divider. The PR codes change the divide ratio of the frequency divider, and variable frequency steps are thereby produced. The attractiveness of this architecture is its high conversion linearity and the readily available clock signals. However, its major drawback is the limited choices of the frequency step, as the fundamental frequency must be a multiple of each available frequency. Therefore, a very high fundamental frequency with fine resolution is necessary for a large number of frequency steps, which may reach the GHz range and can be difficult to implement for audio applications.

The second structure is based on the VCO method and the VCO output frequency is related to the VCO input voltage by

$$y(t) = A_c \cos(2\pi f_c t + 2\pi K \int_0^t x(\tau) d\tau + \phi) \quad (4.3)$$

where f_c is the quiescent frequency, K is the VCO gain, ϕ is the initial phase and $x(t)$ is the time-dependent input.

For an integer input code, equation (4.3) can be simplified as

$$y(t) = A_c \cos(2\pi f_c t + 2\pi K t x(t) + \phi) \quad (4.4)$$

So the output signal frequency is

$$\frac{\partial(2\pi f_c t + 2\pi K t x(t) + \phi)}{\partial t} \times \frac{1}{2\pi} = f_c + Kx(t) \quad (4.5)$$

From equation (4.5), it can be found that the output frequency of the VCO is linearly proportional to the input signal if the gain of the VCO is fixed. Hence, the VCO circuit achieves very good linearity and large frequency steps are readily available for selection. The major design issue is mainly contributed by the VCO. An adjustment block is added to produce a wanted square clock waveform since the VCO output is a sinusoid waveform. These design issues make the circuit more complicated.

Although both designs have pros and cons, from application perspective, the second design is preferred for the realization of PRCFM because of its wider frequency steps.

The frequency divider employed here is to produce switching frequencies, and LFSR frequencies from the input TDL spread frequencies. The reason for generating all the frequencies in the system from the same source is to synchronize these signals with the objective to reduce the noise. The designed 14-order frequency divider is shown in Fig. 4.11. It consists of 14 J-K flip-flops with both inputs tied to “high” state to act as T flip-flop for toggle operation. The functionality of the J-K flip-flop is tabulated in Table 4.4 and Q_{n-1} denotes the previous state of the flip-flop. Each flip-flop is triggered by the output of the previous flip-flop except that the first one is triggered by the TDL frequency. As a result, the output of each flip-flop is a square wave whose

period is two times the output of the previous one. Therefore, the frequency is halved through each flip-flop.

Fig. 4.11. 14-order frequency divider

Table 4.4. FUNCTIONAL TABLE FOR THE J-K FLIP FLOP

Q_{n-1}	J_n	K_n	Q_n
0	1	1	1
1	1	1	0

The switching frequency is $1/2^{10}$ of the TDL frequency for 10-bit DPWM resolution and therefore it is extracted from the 10th flip flop. Four additional flip-flops are used to generate the LFSR clock, so the LFSR clock frequency assigned is $1/2^{14}$ of the TDL frequency. It is $1/16$ of the switching frequency, which means that each frequency step lasts for 16 sampling points, similar to the slow frequency hopping method. This guarantees that the frequency is unchanged within the processing for each sample, thereby reduces the switching noise.

The potential error source for the inaccurate output frequency is the delay of the flip-flops. Although the delay for the individual flip-flop is negligible, say several ns, the propagation delay of several flip-flops can cause severe error. Hence, the total

number of flip-flops should be controlled to ensure the total delay is within the acceptable range.

With the integration of the 5-bit LFSR, the VCO frequency selector and the 14th-order frequency divider (refer to Fig. 4.5), a 5-bit PRCFM is realized. The complete circuit is simulated with 143.36 MHz VCO quiescent frequency and the switching frequency is varied from 145 kHz to 295 kHz in 31 frequency steps within 3 ms.

Fig. 4.12 shows the results for 100~150 μ s. The upper diagram is for the switching frequency and the lower one is for the LFSR frequency.

Fig. 4.12. Simulation results of the designed PRCFM

It is clearly observed that the frequencies of these signals kept changing in random manner. Also, it shows that the period of the LFSR is four times the switching frequency and the same frequency step is involved within each period of LFSR, as expected in the design.

The spectrum of the switching frequency for the PRCFM is measured. The spectrum is compared with that of the 220 kHz switching frequency, which is generated by a conventional clock generator (CG). The structure of the normal CG is exactly the same as that of the PRCFM, except that it does not have LFSR block. The results are shown in Fig. 4.13.

Fig. 4.13. Comparison of switching frequency spectrum for (a) conventional CG (b) PRCFM

It demonstrates that the spectrum spread over a wider frequency band and the emission of the spectrum reduces by about 13.3 dB ($39.67 \text{ dB} - 26.37 \text{ dB}$) with the proposed PRCFM. The reduction is quite close to the theoretical value, i.e. $10\log(31)$

= 14.91 dB . The emission can be further reduced by increasing the frequency steps. With the PRCFM, the harmonic emission is widely spread and the THD has also improved. However, the noise floor has increased substantially. It could be caused by the loss due to frequency hopping and can be solved by enlarging the period of frequency hopping.

4.4 DPWM

DPWM converts the input PCM signal to PWM signal. A high resolution DPWM is necessary to avoid signal distortion and accomplish precise output signal. On the other hand, high resolution DPWM requires high complexity and high operation frequency. With optimization of audio performance and circuit complexity, a 10-bit DPWM is designed and it includes an algorithmic sampling processor and a hybrid pulse generator.

4.3.1 Algorithmic Sampling Processor

A novel algorithmic sampling processor is proposed to improve the THD performance of the open loop digital Class D amplifier. The algorithm of the sampling processor can be visualized in Fig. 4.14. The input sinusoidal signal is modulated with a sampling carrier, which is illustrated as a solid sawtooth waveform with a period of T_s . The dashed sawtooth waveform with a period of T_p represents the generated PRCFM signal. In the same figure, S_1 is an arbitrary sampling point, while S_2 and S_3 are the next two adjacent sampling points. S_m and S_n denote the estimated re-sampling points by PRCFM signal. S_{ns} denotes the point found in natural sampling processing, which is the analogue intercepted point between the PRCFM signal and

the input signal. S_a denotes the point found in the proposed algorithmic sampling processing. Note that all these points are referred to the magnitude of the sampled points and it is assumed that the magnitude of the carrier waveform is unity.

As the PRCFM signal controls the pulse generator described in the next section, the purpose of the sampling process is to determine S_{ns} by using S_1 , S_2 and S_3 sampling points, and generates a T_{ns} pulse. Note that the estimated point S_a might be significantly different from S_{ns} and results in poor THD performance. The proposed method works by approximating the input sampling points S_m and S_n using the PRCFM signal. Mathematically, S_m and S_n can be calculated by

$$S_m = \frac{\Delta t_1}{T_s} \times (S_2 - S_1) + S_1 \quad (4.6)$$

$$S_n = \frac{T_p - T_s + \Delta t_1}{T_s} \times (S_3 - S_2) + S_2 \quad (4.7)$$

A first order linear interpolation is employed and T_{as} can be estimated using

$$T_{as} = T_p \frac{S_m}{1 + S_m - S_n} \quad (4.8)$$

By substituting equations (4.6) and (4.7) to equation (4.8), one gets

$$T_{as} = T_p \frac{\Delta t_1 \times (S_2 - S_1) + S_1 T_s}{T_s + (T_s - \Delta t_1) \times (S_1 + S_3 - 2S_2) - T_p \times (S_3 - S_2)} \quad (4.9)$$

The detailed derivation is given in Appendix B.

It is worthy to mention that only simple computation is required to obtain T_{as} and thus the algorithm can be easily realized in hardware implementation.

Fig. 4.14. Sampling algorithm

4.3.2 Hybrid Pulse Generator

The pulse generator serves the purpose of a digital-to-analog converter (DAC). It generates analog pulse according to the input digital sampled data. A 10-bit hybrid TDL/counter-based pulse generator is adopted in the design for its low carrier frequency and reasonable THD performance.

As mentioned in the literature study, the hybrid pulse generator integrates a counter and a TDL. The input data bits are divided into two parts, the first part is a most significant part (MSP), which feeds the counter to provide the coarse pulse width and the second part is a less significant part (LSP), which connects to the tapped delay line to provide the fine pulse width. It has been reported that the degree of hybridization affects the power consumption as well as the THD. For the same resolution of the pulse generator, more power is consumed and a higher counter frequency is required, when more resolution bits are allocated to the counter. As a tradeoff, the THD level is reduced due to the high linearity of the counter. In

addition, the circuit size can be reduced because of significant reduction of the number of the delay cells in the tapped delay line.

In the proposed design, a 10-bit hybrid pulse generator with 7-bit counter and 3-bit tapped delay line are chosen to provide the hybrid pulse generation. For synchronization purpose, each delay cell frequency is $2^3 = 8$ times of the counter frequency and $2^{10} = 1024$ times of the switching frequency. So each switching period is divided for 128 counter cycles and each counter cycle has 8 tapped delay cycles. Hence, the whole period is divided into 1024 time intervals. In each switching cycle, the counter is reset to zero initially and then counts up. In each counter cycle, only one delay cell is sequentially active in one time interval, beginning with the seventh delay cell.

The major design consideration of the hybrid pulse generator is the synchronization of the three related frequencies. The matching of the delay cells in the tapped delay line is another challenge, as both contribute to the imperfect output pulse signal.

Fig. 4.15. 3-bit tapped delay line in Simulink

Since the DPWM is aimed to operate in the variable frequency conditions, each D flip-flop is adopted as a delay cell, whose operating frequency can be directly controlled by the input TDL frequency. Each flip-flop follows the late state output by the previous flip-flop and thus only one pulse flows through these taps. The initial content of the tapped delay line is set to “000001”. An 8-to-1 multiplexer in the circuit outputs the selected tap according to the input LSP.

As expected, the output of each flip-flop is a pulsed waveform with 12.5% duty ratio and the period of the resultant clock waveform is eight times the delay cell period. So the output (Q8) of the last flip-flop in the tapped delay line can be used as the counter frequency, that makes the counter frequency and the tapped delay line frequency synchronized and eliminates the need for extra matched circuit.

Fig. 4.16. Hybrid pulse generator in Simulink

The complete block diagram of the 10-bit hybrid pulse generator implemented in Simulink is shown in Fig. 4.16. It consists of 3-bit tapped delay line and a 7-bit up-counter. The degree of the hybridization is assigned to minimize the THD while keeping the power consumption at an acceptable level. The tapped delay line is triggered by the input TDL clock generated from the PRCFM, while the up-counter is clocked by the tapped delay line. The output D flip-flop is set to “high” at every input clock cycle, where its period is $2^{10} = 1024$ times of that of the TDL clock.

The input data is split to 7-bit MSP and 3-bit LSP by the “demux” block, which is a built-in block in Simulink. The MSP is compared with the counter output through a comparator. The output “1” is generated when the coarse pulse cycle has been reached. When both coarse pulse cycle and the fine pulse cycle have been reached, the D flip-flop is reset to “0”.

In the Simulink simulation, a 10-bit digital input “0111110100” is input with 1 kHz TDL frequency and 0.98 MHz switching frequency and the resultant output PWM waveform is shown in Fig. 4.17.

The PWM waveform duty ratio is $(1.524 - 1.024)/1.024 = 500/1024$, which matches with $“0111110100”/“10000000000” \approx 500/1024$, a clear indication that the design functions well.

Fig. 4.17. Hybrid pulse generator simulation results for 0111110100

Fig. 4.18. 10-bit hybrid pulse generator operating waveforms

Fig. 4.18 shows the data flow and the output waveforms of the 10-bit hybrid pulse generator with an input data “1100000110” from FPGA. At the beginning of each switching cycle, the 10-bit loaded data “1100000110” is split to 7-bit MSP “1100000” and 3-bit LSP “110”, respectively. The output pulse is set to “1” through the output flip-flop. When the counter output matches the MSP “1100000” of the loaded input data and a pulse reaches the delay cell tap selected by the LSP “110”, the output flip-flop is reset and its output becomes “0” subsequently. As a result, a PWM pulse with 774/1024 duty ratio is generated.

4.5 Simulation & Measurement Results

For design verification purposes, the proposed digital Class D amplifier with PRCFM is first simulated in Simulink and then implemented in Altera Cyclone® II EP20C20F484C7N FPGA development board. All the circuit blocks in FPGA are coded with VHDL.

As the FPGA board contains many other chips and components besides the FPGA chip for multi-purpose design, the board power supply is rather noisy and it is difficult to isolate and measure the reduction of noise meaningfully due to PRCFM using the LISN method as described in Chapter 3. On the other hand, as explained earlier, the results at the load of Class D amplifier has the similar noise characteristics as that at power supply. So the EMI noise at the load was measured in this digital prototype design for verification of the effectiveness of PRCFM in EMI reduction. A National Instrument (NI) PXI-1031 spectrum analyzer with a NI PXI-8184 embedded controller is employed for the EMI emission measurement. The

measurement results are collected through LabVIEW 8.2 (Laboratory Virtual Instrument Engineering Workbench).

For all the simulations and measurements, the input is set to a 1.5 V, 1 kHz sinusoid signal with zero DC offset. The input signal is pre-sampled at 44.1 kilo-samples per second and coded to 16-bit unsigned binary so that it is analogue to the 44.1 kHz 16-bit CD data format. The center switching frequency is set to 220 kHz, which is about 5 times the data rate to meet the Nyquist Theorem requirement.

The results are compared with that of the conventional Class D amplifier. The compared conventional Class D amplifier is with the same architecture, except that normal CG and 1st-order linear interpolation sampling is used. The structure of the conventional CG is the same as that of proposed PRCFM, except that it puts a constant load on the frequency selector in order to generate a constant frequency. The time-domain waveform and frequency-domain spectrum are shown in Fig. 4.19. As expected, a pulse waveform with nearly 50% duty ratio is generated. The detected fundamental frequency is 208.33 kHz and the peak EMI emission indicated in the spectrum is -24.841 dB at 207.459 kHz. It is clearly observed that the EMI emissions are rather high at odd harmonics.

In contrast to the conventional CG, a clock with variable frequencies is generated from the proposed 5-bit PRCFM. The time-domain clock waveform is shown in Fig. 4.20. Every frequency step lasts for 16 cycles before it hop to the next frequency step. The frequency spectrum of the PRCFM signal is almost noise-like. The EMI

emissions at the harmonics are spread with the peak emission reduced to -39.621 dB at 132.034 kHz, which translates to an EMI reduction of 14.78 dB due to the spreading of 31 frequency steps. It shows the proposed PRCFM works well and reduces the EMI emissions effectively.

Fig. 4.19. Time domain & frequency spectrum results for conventional CG

Fig. 4.20. Time domain & frequency spectrum results for PRCFM

(a)

(b)

Fig. 4.21. Noise floor for (a) conventional CG (b) PRCFM

One of the tradeoffs for PRCFM is the increase in noise floor in the audio band. The noise floor for the conventional CG and the proposed PRCFM is -120.59 dB and -76.831 dB respectively, as indicated in Fig. 4.21. The possible cause for the increase in noise floor could be due to the period of the frequency hopping. To verify this, measurements for PRCFM with variable frequency hopping periods are conducted. The variable period is realized by adding certain number of J-K flip-flops in the frequency divider to manage the LFSR frequency, as each flip-flop reduces the output frequency by half and doubles the period. The relationship between the noise floor in the audio band and the maximum frequency hopping period for PRCFM is measured and plotted in Fig. 4.22. It shows that the noise floor does reduce with increase in frequency hopping period and eventually reaches a stable level, which is

close to the conventional result at about -120 dB. This trend is consistent with the explanation earlier.

Finally, the peak EMI emissions for different hopping periods are also measured and plotted in Fig. 4.23. It reveals that the emission reduction is relatively stable with the varied frequency hopping periods. The variation is around ± 3 dB and the maximum reduction is less than the theoretical reduction of 14.91 dB, which is expected.

Fig. 4.22. Noise floor vs. maximum frequency hopping period

Fig. 4.23. Peak EMI vs. number of clock cycles

Fig. 4.24. Output spectra of (a) Class D amplifier with PRCFM and (b) conventional Class D amplifier

The simulated output spectra of the Class D amplifier with PRCFM and the conventional Class D amplifier are shown in Fig. 4.24 (a) and (b), respectively. The magnitudes of the 1 kHz signal for both amplifiers are the same and stayed around 53.07 dB, which is a clear indication that Class D amplifier with PRCFM and the conventional Class D amplifier are working correctly. Fig. 4.24 (b) shows the EMI emissions of the conventional Class D amplifier, which are concentrated at the 220 kHz fundamental switching frequency and its harmonics. The peak emission is 52.43 dB at 219.3 kHz. For the Class D amplifier with PRCFM, the peak emissions at the fundamental frequency as well as its harmonics are spread over a wider frequency, as indicated in Fig. 4.24(a). The peak emission happened at 179.3 kHz with a level of 40.46 dB, which is 11.97 dB lower than that of the conventional Class D amplifier.

Fig. 4.25(a) and (b) show the measured spectra for the conventional digital Class D amplifier and the proposed Class D amplifier with PRCFM, respectively. The EMI emissions are spread out for the Class D amplifier with PRCFM. The peak emission for the conventional Class D amplifier is -27.008 dB, while the peak emission for

Class D amplifier with PRCFM is -34.434 dB, a reduction of 7.426 dB. The reduction obtained is much lower than the simulated value due to the background noise of the amplifier.

(a)

(b)

Fig. 4.25. Spectra for (a) conventional digital Class D amplifier (b) Class D amplifier with PRCFM

(a)

(b)

Fig. 4.26. Outputs & inputs for (a) Class D amplifier with PRCFM and (b) conventional Class D amplifier

One set of the output and input signal for the proposed Class D amplifier is illustrated in Fig. 4.26(a). The x-axis is the time-scale in ms for a total of 3 ms duration and the y-axis is the amplitude in V. The input signal is a sampled sinusoid signal with 44.1 kHz sampling frequency. On the other hand, the output is, as expected, a smooth 1 kHz sinusoid signal, but with a certain delay at the initial, compared to the input signal. This is possibly caused by the processing delay of the amplifier. Similarly, the output of the conventional Class D amplifier is a sinusoid signal with initial delay, as displayed in Fig. 4.26(b). Additionally, the two output signals are similar with almost the same delay, an indication that the Class D amplifier with PRCFM provides good EMI mitigation technique, while still maintaining the functionality of a conventional Class D amplifier.

Fig. 4.27. THD performance over full different input modulation index with input signal frequency of 1 kHz and output power range from 0.03 W to 0.28 W

Fig. 4.27 shows the THD performance comparison over the input modulation index range, which can be controlled by the amplitude of the input signal, for 1 kHz input

sinusoidal signal. With the proposed PRCFM, the THD results are below 0.5%, which degrades as compared to that of the conventional Class D amplifier, especially for higher modulation index. The THD noise is mainly contributed by the algorithmic sampling process. It is believed that the THD can be improved with better sampling algorithm but at the expense of circuit complexity. However, the THD performance of the proposed circuit is comparable to that of the conventional Class D amplifier at lower modulation index. The degradation in THD performance with higher modulation index is mainly caused by the clipping effect when the modulation index of the input signal is larger.

The specifications of the proposed design are summarized in Table 4.5.

Table 4.5. PERFORMANCE SUMMARY

Specification	Value
Supply Voltage	3.3 V
Input Amplitude	1.5 V
Input Data Sampled Frequency	44.1kHz
-3 dB Filter Bandwidth	20 kHz
Output Load	8 Ω
Output Amplitude	1.5 V
Output Power	< 0.28 W
DPWM Resolution	10 bits
Sampling Frequency	220 kHz
Switching Frequency	145 ~ 295 kHz
Frequency Steps	31
Nominal Period of PR Code	0.564 ms
THD	< 0.5 %
Peak EMI Reduction	7.4 dB

4.6 Summary

A digital Class D amplifier with PRCFM is proposed. The design is simulated in Simulink and then implemented in FPGA. As the PRCFM can be easily realized with relatively simple digital cells, it is a size-efficient EMI mitigation method. The proposed PRCFM circuit is verified by both simulated and measured results. Again, the PRCFM has demonstrated its effectiveness in reducing the EMI emissions of digital Class D amplifier through the spreading of the energy at the emission frequencies. In addition, a novel algorithmic sampling processor is developed to keep the THD performance of the proposed circuit below 0.5%.

Chapter 5

Conclusion &

Recommended Future

Works

5.1 Conclusion

With the current trends of higher operating speeds and size reduction of audio amplifiers, EMC will continue to be a challenging design issue for Class D amplifiers. By eliminating the external low pass filter in Class D amplifier design, this thesis describes in details the implementation of PRCFM for EMI mitigation.

The effectiveness of PRCFM for EMI reduction is first demonstrated in analog Class D amplifier. A filterless Class D amplifier with PRCFM has been designed and fabricated using CSM 0.18 μm CMOS process. The additional area occupied by the PRCFM circuit is less than 1% of total chip size. The measurement results have verified that the proposed PRCFM in the filterless Class D amplifier is very effective in reducing both the conducted and near-field radiated emissions without significantly affecting the THD and power efficiency performances. It also shows

that the noise floor in the audio band due to PR code generation frequency can be reduced by increasing the frequency hopping period.

Subsequently, the PRCFM is extended to digital Class D amplifier design. The PRCFM is size-efficient, as its implementation can be realized with simple logic cells. Again, through both simulation and measurement results, the PRCFM has proven to be effective in EMI mitigation of digital Class D amplifiers. To ensure that THD performance is not compromised, a novel algorithmic sampling process and a hybrid pulse generator are proposed.

In conclusion, the thesis has described the theory and implementation of PRCFM in both analog and digital Class D amplifiers. And its effectiveness for EMI mitigation has also been demonstrated experimentally.

5.2 Recommended Future works

One possible research area that worth exploring is to develop accurate mathematical model for Class D amplifier with spread spectrum modulation. The developed model can provide in-depth analysis the relationships amongst the key parameters, such as the switching frequency, the input signal frequency, the level of randomness, the amount of EMI reduction and so on. Similar to the models for DC-DC with spread spectrum modulation [72-75, 97]; one main obstacle is to accurately model the behavior of pseudo-random modulation. What's more, the variation of duty ratio, respective to varied input signal in Class D amplifier, make the modeling even more challenging. On the other hand, the performance optimization of the design is mainly

based on simple first-order estimation and experiments, with the lack of accurate model. So the accurate mathematic model for Class D amplifier with PRCFM is important so that the various parameters can be optimized for better EMI mitigation and audio performance. One possible approach is to develop a time domain Class D amplifier model instead of traditional frequency domain model [100], which provides accurate results and much simpler than the frequency domain model.

Nowadays, digital Class D amplifier is a standard in mobile applications. With repaid development and exploding of mobile devices such as smart phones and tablets, the development of Hi-Fi low power digital Class D amplifier is one emerging research area [55, 108]. To improve the performance of digital Class D amplifier with spread spectrum modulation, higher order noise shaper that improves the THD can be explored. A feedback network with digital-to-analog converter (DAC) is another good approach to improve the THD and PSRR. Last but not least, complex DPWM architecture, like natural sampling together with high order hybrid pulse generator, can be explored as well. The complexity and die size would be the trade-off. The stability of the high order system should be taken care as well.

Due to time constraint of this project, the proposed digital Class D amplifier was implemented in FPGA for the purpose of proof of concept and therefore the background noise is quite high, which affect the measurement results. The circuit can be implemented on stand-only chip for better measurement results.

References

- [1] D. Self, *Audio Power Amplifier Design Handbook*, 3rd edition, Newnes, 2002.
- [2] R. Hatfield, "Class D amplifiers empower mobile multimedia," *Wolfson Microelectronics Application Notes*, 2006.
- [3] M. Bloechl, M. Bataineh, and D. Harrell, "Class D switching power amplifiers: theory, design, and performance," in *IEEE Proceedings of SoutheastCon, 2004*, pp. 123-146.
- [4] E. Gaalaas, "Class D audio amplifiers: what, why, and how," *Analog Dialogue* vol. 40-06, June 2006.
- [5] P. Muggler, W. Chen, C. Jones, P. Dagli, and N. Yazdi, "A filter free Class D audio amplifier with 86% power efficiency," in *ISCAS 2004, IEEE Proceedings of the 2004 International Symposium on Circuits and Systems*, pp. I-1036-9 Vol.1.
- [6] A. Matamura, N. Nishimura, and B. Y. Liu, "Filterless multi-level delta-sigma class-D amplifier for portable applications," in *ISCAS 2009, IEEE International Symposium on Circuits and Systems, 2009*, pp. 1177-1180.
- [7] M. Score and D. Dapkus, "Optimized modulation scheme eliminates output filter," *109th Audio Engineering Society Convention*, Sep. 2000.
- [8] P. P. Siniscalchi and R. K. Hester, "A 20 W/channel Class-D amplifier with near-zero common-mode radiated emissions," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3264-3271, Dec. 2009.

- [9] J. Honda and J. Adams, "Class D audio amplifier basics," *International IOR Rectifier Application Note*, 2005.
- [10] Z. Dongbing, D. Y. Chen, and F. C. Lee, "An experimental comparison of conducted EMI emissions between a zero-voltage transition circuit and a hard switching circuit," in *PESC 1996, 27th Annual IEEE Power Electronics Specialists Conference*, pp. 1992-1997 vol.2.
- [11] Z. Huibin, L. Jih-Sheng, A. R. Hefner, Jr., T. Yuqing, and C. Chingchi, "Modeling-based examination of conducted EMI emissions from hard and soft-switching PWM inverters," *IEEE Transactions on Industry Applications*, vol. 37, pp. 1383-1393, Sep. 2001.
- [12] L. Yoonjae and R. Mittra, "Electromagnetic interference mitigation by using a spread-spectrum approach," *IEEE Transactions on Electromagnetic Compatibility*, vol. 44, pp. 380-385, May 2002.
- [13] K. B. Hardin, J. T. Fessler, and D. R. Bush, "Spread spectrum clock generation for the reduction of radiated emissions," in *IEEE International Symposium on Electromagnetic Compatibility*, 1994, pp. 227-231.
- [14] J. Paramesh and A. von Jouanne, "Use of sigma-delta modulation to control EMI from switch-mode power supplies," *IEEE Transactions on Industrial Electronics*, vol. 48, pp. 111-117, Feb. 2001.
- [15] N. Karsten, "Linearity and efficiency performance of switching audio power amplifier output stages - a fundamental analysis," *105th Audio Engineering Society*, Sep.1998.
- [16] J. S. Chang, M. T. Tan, Z. H. Cheng, and Y. C. Tong, "Analysis and design of power efficient class D amplifier output stages," *IEEE Transactions on Circuits*

- and Systems I-Fundamental Theory and Applications*, vol. 47, pp. 897-902, Jun. 2000.
- [17] L. Jun-Woo, L. Jae-Shin, L. Gun-Sang, and S. Kim, "A 2 W BTL single-chip class-D power amplifier with very high efficiency for audio applications," in *ISCAS 2000, IEEE International Symposium on Circuits and Systems, 2000*. pp. 493-496 vol.5.
- [18] S. C. Li and L. Vincent Chia-Chang, "A high efficiency 0.5W BTL class-D audio amplifier with RWDM technique," in *Proceedings of the ASP-DAC Design Automation Conference, 2004*. pp. 307-309.
- [19] F. Koeslag and T. Mouton, "Accurate characterization of pulse timing errors in Class D audio amplifier output stages," presented at the 37th Audio Engineering Society International Conference, Hillerod Denmark, 2009.
- [20] F. Koeslag, H. T. du Mouton, H. J. Beukes, and P. Midya, "A detailed analysis of the effect of dead time on harmonic distortion in a class D audio amplifier," in *AFRICON 2007*, pp. 1-7.
- [21] I. D. Mosely, P. H. Mellor, and C. M. Bingham, "Effect of dead time on harmonic distortion in class-D audio power amplifiers," *Electronics Letters*, vol. 35, pp. 950-952, Aug. 1999.
- [22] T. Ge and J. S. Chang, "Filterless class D amplifiers: power-efficiency and power dissipation," *IET Circuits, Devices & Systems*, vol. 4, pp. 48-56, Jan. 2010.
- [23] H. S. Black, *Modulation Theory*: Van Nostrand Reinhold Company, 1953.
- [24] Z. K. Song and D. V. Sarwate, "The frequency spectrum of pulse width modulated signals," *Signal Processing*, vol. 83, pp. 2227-2258, Oct. 2003.

- [25] S. Wei, J. S. Chang, G. Tong, and M.T. Tan, "Fourier series analysis of the nonlinearities in analog closed-loop PWM class D amplifiers," in *ISCAS 2006, IEEE International Symposium on Circuits and Systems, 2006*, pp. 4 pp.-1385.
- [26] S. Wei and J. S. Chang, "THD of closed-loop analog PWM Class-D amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, pp. 1769-1777, Jul. 2008.
- [27] H. Hou, C. Lin, and W. Chen, "A robust continuous time loop filter PWM class D amplifier with high linearity and good immunity to process variations," in *ASSCC 2009. IEEE Asia Solid-State Circuits Conference, 2009*, pp. 245-248.
- [28] M. Tan, J. S. Chang, Z. Cheng, and T. C. Tong, "Novel self-error-correction pulse width modulator for a class D hearing instrument amplifier," *IEE Proceedings - Circuits, Devices and Systems*, vol. 148, pp. 261-266, Oct. 2001.
- [29] C. Youngkil, T. Wonho, Y. Younhyun, R. Jeongjin, K. Sunwoo, and K. Jinseok, "A 0.018% THD+N, 88-dB PSRR PWM Class-D amplifier for direct battery hookup," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 454-463, Jan. 2012.
- [30] K. Sunwoo, K. Injeong, Y. Shinyoung, K. Sangheyub, L. Sangheon, H. Taeho, M. Byoungkwon, C. Yunyoung, S. Hosung, and K. Jinseok, "A 0.028% THD+N, 91% power-efficiency, 3-level PWM Class-D amplifier with a true differential front-end," in *2012 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012, pp. 96-98.
- [31] Z. Messghati, Y. Laghzizal, and H. Qjidaa, "Pulse width modulation for class D audio power amplifier in CMOS 0.18um Process with 85% of efficiency," in

- 2011 International Conference on Communications, Computing and Control Applications (CCCA)*, 2011, pp. 1-4.
- [32] C. Lin, B. S. Hsieh, and C. Chung, "PWM-based multilevel class-D amplifier with integrated over-current protection system," in *the 5th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2010, pp. 1394-1398.
- [33] J. Yu, M. T. Tan, W. L. Goh, and S. M. Cox, "A dual-feedforward carrier-modulated second-order Class-D amplifier with improved THD," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, pp. 35-39, Jan. 2012.
- [34] M. Harada, S. Hirano, T. Goto, and M. Sakurai, "An optimal design method of delta-sigma modulator for Class-D audio amplifier," presented at the ISCE: 2009 IEEE 13th International Symposium on Consumer Electronics, Vols 1 and 2, New York, 2009.
- [35] E. Gaalaas, B. Y. Liu, N. Nishimura, R. Adams, and K. Sweetland, "Integrated stereo delta sigma Class D amplifier," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2388-2397, Dec. 2005.
- [36] J. L. Pan, L. B. Yao, Y. Lian, and Ieee, "A sigma-delta Class D audio power amplifier in 0.35 μm CMOS technology," presented at the ISOCC: 2008 International Soc Design Conference, Vols 1-3, New York, 2008.
- [37] K. Kyoungsik, R. Jeongjin, C. Youngkil, R. Hyungdong, N. Hyunsuk, and L. Songjun, "Class-D audio amplifier using 1-bit fourth-order delta-sigma modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, pp. 728-732, Aug. 2008.

- [38] K. Nielsen, "A review and comparison of pulse-width modulation (PWM) methods for analog and digital input switching power amplifiers," presented at the 102th Audio Engineering Society Convention, Germany, 1997.
- [39] B. Pilloud and W. H. Groeneweg, "A 650mW filterless class-D audio power amplifier for mobile applications in 65-nm technology," in *ISCAS 2009, IEEE International Symposium on Circuits and Systems*, 2009, pp. 1173-1176.
- [40] Y. Lin, W. Liu, and M. Yeh, "A high efficiency filter-less class-D audio power amplifier," in *ASICON 2009, IEEE 8th International Conference on ASIC*, 2009, pp. 1062-1065.
- [41] C. Lin, H. B. Hsieh and Y. Lin "Enhanced design of filterless class-D audio amplifier," in *DATE 2009, Design, Automation & Test in Europe Conference & Exhibition*, 2009, pp. 1397-1402.
- [42] S. Poulsen and M. A. E. Andersen, "Practical considerations for integrating switch mode audio amplifiers and loudspeakers for a higher power efficiency," presented at the 116th Audio Engineering Society Convention, Berlin, Germany, 2004.
- [43] R. Cellier, E. Allier, C. Crippa, R. Bassoli, A. Nagari, G. Pillonnet, and N. Abouchi, "A fully differential digital input Class D with EMI spreading method for mobile application," presented at the 37th Audio Engineering Society International Conference, Hillerod, Denmark, 2009.
- [44] P. H. Mellor, S. P. Leigh, and B. M. G. Cheetham, "Improved sampling process for a digital, pulse-width modulated, class D power amplifier," in *IEE Colloquium on Digital Audio Signal Processing*, 1991, pp. 3/1-3/5.

- [45] P. H. Mellor, S. P. Leigh, and B. M. G. Cheetham, "Digital sampling process for audio class D, pulse width modulated power amplifiers," *Electronics Letters*, vol. 28, pp. 56-58, Jan. 1992.
- [46] P. H. Mellor, S. P. Leigh, and B. M. G. Cheetham, "Reduction of spectral distortion in class D amplifiers by an enhanced pulse width modulation sampling process," *IEE Proceedings on Circuits, Devices and Systems*, vol. 138, pp. 441-448, Aug. 1991.
- [47] A. Yoneya and A. Watanabe, "Low distortion digital pulse width modulation for audio class-D amplifier," in *ISCIT 2004. IEEE International Symposium on Communications and Information Technology*, 2004, pp. 515-518 vol.1.
- [48] B. H. Gwee, J. S. Chang, and H. Li, "A micropower low-distortion digital pulsewidth modulator for a digital class D amplifier," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, pp. 245-256, Apr. 2002.
- [49] H. Li, B. H. Gwee, and J. S. Chang, "A digital Class D amplifier design embodying a novel sampling process and pulse generator," in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems*, pp. 826-829 vol. 4.
- [50] V. Adrian, B. H. Gwee, and J. S. Chang, "A novel combined first and second order Lagrange interpolation sampling process for a digital class D amplifier," in *ISCAS 2004. IEEE Proceedings of the 2004 International Symposium on Circuits and Systems*, pp. III-233-60 Vol.3.
- [51] V. Adrian, B. H. Gwee, and J. S. Chang, "A combined interpolatorless interpolation and high accuracy sampling process for digital class D

- amplifiers," in *ISCAS 2005. IEEE International Symposium on Circuits and Systems*, 2005, pp. 5405-5408 Vol. 6.
- [52] V. Adrian and J. S. Chang, "A hybrid modulation scheme for digital Class D amplifier modulators," in *2010 2nd Circuits and Systems for Medical and Environmental Applications Workshop (CASME)*, 2010, pp. 1-3.
- [53] V. Adrian, J. S. Chang, and B. H. Gwee, "A low-voltage micropower digital Class-D amplifier modulator for hearing aids," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, pp. 337-349, Feb. 2009.
- [54] B. H. Gwee, J. S. Chang, V. Adrian, and H. Amir, "A novel sampling process and pulse generator for a low distortion digital pulse-width modulator for digital class D amplifiers," in *ISCAS 2003. IEEE Proceedings of the 2003 International Symposium on Circuits and Systems*, 2003, pp. IV-504-IV-507 vol.4.
- [55] L. Dooper and M. Berkhout, "A 3.4 W digital-in Class-D audio amplifier in 0.14 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 1524-1534, Jul. 2012.
- [56] S. L. Gupta and N. K. Saha, "Spark counter as a fast pulse generator," *Nuclear Instruments & Methods*, vol. 13, pp. 258-260, Aug. 1961.
- [57] M. E. Davies, "Multi-pulse generator based on 74LS169A counter chip," *Electronic Engineering*, vol. 51, pp. 19-19, Sep. 1979.
- [58] G. Wei and M. Horowitz, "A low power switching power supply for self-clocked systems," in *International Symposium on Low Power Electronics and Design*, 1996, pp. 313-317.

- [59] W. W. Wang, Z. H. Shen, X. Tan, N. Yan, and H. Min, "Improved delay-line based digital PWM for DC-DC converters," *Electronics Letters*, vol. 47, pp. 562-564, Apr. 2011.
- [60] V. Yousefzadeh, T. Takayama, and D. Maksimovi, "Hybrid DPWM with digital delay-locked loop," in *COMPEL 2006. IEEE Workshops on Computers in Power Electronics*, 2006, pp. 142-148.
- [61] I. Mori, K. Kimura, Y. Yamada, H. Kobayashi, Y. Kabori, S. A. Wibowo, K. Shimizu, M. Kono, and San Hao, "High-resolution DPWM generator for digitally controlled DC-DC converters," in *APCCAS 2008. IEEE Asia Pacific Conference on Circuits and Systems*, 2008, pp. 914-917.
- [62] J. Yu and Y. An, "Digital controlled high frequency switching mode power system," in *2010 Asia-Pacific Conference on Power Electronics and Design (APED)*, 2010, pp. 101-103.
- [63] A. de Castro and E. Todorovich, "High resolution FPGA DPWM based on variable clock phase shifting," *IEEE Transactions on Power Electronics*, vol. 25, pp. 1115-1119, May 2010.
- [64] J. O. Smith, *Physical Audio Signal Processing: for Virtual Musical Instruments and Digital Audio Effects*: W3K Publishing 2010.
- [65] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, "Digital pulse width modulator architectures," in *PESC 2004, IEEE 35th Annual Power Electronics Specialists Conference*, 2004, pp. 4689-4695 Vol.6.
- [66] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 18, pp. 438-446, Jan. 2003.

- [67] M. A. Teplechuk, T. Gribben, and C. Amadi, "True filterless Class-D audio amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2784-2793, Nov. 2011.
- [68] J. Liu, S. Chien, and T. Kuo, "A 100 W 5.1-channel digital Class-D audio amplifier with single-chip design," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 1344-1354, May 2012.
- [69] M. Berkhout and L. Dooper, "A 3.4W digital-in class-D audio amplifier," in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, 2011, pp. 87-90.
- [70] C. R. Paul, *Introduction to Electromagnetic Compatibility*, the second edition: Wiley-Interscience 2006.
- [71] M. Berkhout, "An integrated 200-W Class-D audio amplifier," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1198-1206, Jul. 2003.
- [72] K. K. Tse, H. S. H. Chung, S. Y. Huo, and H. C. So, "Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression," *IEEE Transactions on Power Electronics*, vol. 15, pp. 399-410, Mar. 2000.
- [73] K. K. Tse, C. Henry Shu-Hung, S. Y. Ron Hui, and H. C. So, "A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 618-627, Jun. 2002.
- [74] Y. Shrivastava, S. Y. Hui, S. Sathiakumar, H. Shu-Hung Chung, and K. K. Tse, "Harmonic analysis of nondeterministic switching methods for DC-DC power converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, pp. 868-884, Jun. 2000.

- [75] S. Y. Hui, Y. Shrivastava, S. Sathiakumar, K. K. Tse, and C. Henry Shu-Hung, "A comparison of nondeterministic and deterministic switching methods for DC-DC power converters," *IEEE Transactions on Power Electronics*, vol. 13, pp. 1046-1055, Nov. 1998.
- [76] R. Yang, B. Zhang, F. Li, and J. J. Jiang, "Experiment research of chaotic PWM suppressing EMI in converter," in *IPEMC 2006. CES/IEEE 5th International Power Electronics and Motion Control Conference*, 2006, pp. 1-5.
- [77] M. Yeh, W. Liou, H. Hsieh, and Y. Lin, "An electromagnetic interference (EMI) reduced high-efficiency switching power amplifier," *IEEE Transactions on Power Electronics*, vol. 25, pp. 710-718, Mar. 2010.
- [78] X. Ming, Z. Chen, Z. k. Zhou, and B. Zhang, "An advanced spread spectrum architecture using pseudorandom modulation to improve EMI in Class D amplifier," *IEEE Transactions on Power Electronics*, vol. 26, pp. 638-646, Feb. 2011.
- [79] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 42, pp. 595-603, Dec. 1995.
- [80] H. Guichao and F. C. Lee, "Soft-switching techniques in PWM converters," in *Proceedings of the International Conference on Industrial Electronics, Control, and Instrumentation*, 1993, pp. 637-643 vol.2.
- [81] T. Wu and S. Liang, "A systematic approach to developing single-stage soft switching PWM converters," *IEEE Transactions on Power Electronics*, vol. 16, pp. 581-593, Sep. 2001.

- [82] B. Lin and C. Chao, "Analysis, design and implementation of a soft switching converter with two three-level PWM circuits," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1-1, 2012.
- [83] D. Gonzalez, J. Balcells, A. Santolaria, J. C. Le Bunetel, J. Gago, D. Magnon, and S. Brehaut, "Conducted EMI reduction in power converters by means of periodic switching frequency modulation," *IEEE Transactions on Power Electronics*, vol. 22, pp. 2271-2281, Nov. 2007.
- [84] H. H. Chang, I. H. Hua, and S. I. Liu, "A spread-spectrum clock generator with triangular modulation," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 673-676, Apr. 2003.
- [85] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques," *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, pp. 569-576, Aug. 2005.
- [86] Y. Shrivastava, S. Sathiakumar, and V. G. Agelidis, "Analysis and verification of two-level random aperiodic PWM schemes for DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 24, pp. 2138-2147, Sep. 2009.
- [87] F. Mihali and D. Kos, "Reduced conductive EMI in switched-mode DC-DC power converters without EMI filters: PWM versus randomized PWM," *IEEE Transactions on Power Electronics*, vol. 21, pp. 1783-1794, Nov. 2006.
- [88] S. Kaboli, A. Moayedi, and H. Oraee, "Application of random PWM technique for reducing the high frequency harmonics in class-D amplifier," in *PEMD 2008. 4th IET Conference on Power Electronics, Machines and Drives*, 2008, pp. 406-410.

- [89] W. Haishi, Z. Bo, S. Jiang, and W. Rui, "Application of spread spectrum for EMI reduction in class D amplifier," in *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2010, pp. 129-131.
- [90] X. Ming, Z. Chen, Z.-k. Zhou, and B. Zhang, "An advanced spread spectrum architecture to improve EMI emissions in Class D amplifier," in *ICCCAS 2009. International Conference on Communications, Circuits and Systems*, 2009, pp. 661-665.
- [91] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini, "A 1 W 104 dB SNR filter-less fully-digital open-loop Class D audio amplifier with EMI reduction," *IEEE Journal of Solid-State Circuits*, , vol. 47, pp. 686-698, Feb. 2012.
- [92] R. E. Ziemer. (2007). *Fundamentals of Spread Spectrum Modulation*.
- [93] R. L. Peterson, *Introduction to Spread-Spectrum Communications*: Prentice Hall, 1995.
- [94] O. Trescases, W. Guowen, and N. Wai Tung, "A low-power DC-DC converter with digital spread spectrum for reduced EMI," in *PESC 2006. 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1-7.
- [95] D. Trevisan, P. Mattavelli, M. Zigliotto, and S. Saggini, "Limited-pool random carrier-frequency PWM for digitally controlled DC-DC converters," in *IECON 2006. 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 4929-4934.
- [96] A. M. Stankovic and H. Lev-Ari, "Randomized modulation in power electronic converters," *Proceedings of the IEEE*, vol. 90, pp. 782-799, May 2002.

- [97] K. K. Tse, C. Henry Shu-Hung, S. Y. Ron Hui, and H. C. So, "A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 618-627, Jun. 2002.
- [98] K. K. Tse, H. S. H. Chung, S. Y. R. Hui, and H. C. So, "A comparative investigation on the use of random modulation schemes for DC/DC converters," *IEEE Transactions on Industrial Electronics*, vol. 47, pp. 253-263, Apr. 2000.
- [99] V. Adrian, J. S. Chang, B. W. Gwee, and S. Tedjaseputro, "Spectral analysis of randomized switching frequency modulation scheme with a triangular distribution for DC-DC converters," in *ICC 2009. International Conference on Computing, Engineering and Information*, 2009, pp. 119-122.
- [100] J. Yu, M. T. Tan, S. M. Cox, and W. L. Goh, "Time-domain analysis of intermodulation distortion of closed-loop Class-D amplifiers," *IEEE Transactions on Power Electronics*, vol. 27, pp. 2453-2461, Mar. 2012.
- [101] K. E. K. Drissi, P. C. K. Luk, W. Bin, and J. Fontaine, "Effects of symmetric distribution laws on spectral power density in randomized PWM," *IEEE Power Electronics Letters*, vol. 1, pp. 41-44, Jun. 2003.
- [102] Information Technology Equipment: RadioDisturbance Characteristics—Limits and Methods of Measurement, CISPR 22 Feb. 1995.
- [103] B. Forejt, V. Rentala, J. D. Arteaga, and G. Burra, "A 700+-mW class D design with direct battery hookup in a 90-nm process," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1880-1887, Sep. 2005.

- [104] P. M. Aziz, H. V. Sorensen, and J. van der Spiegel, "An overview of sigma-delta converters," *IEEE Signal Processing Magazine*, vol. 13, pp. 61-84, Jan. 1996.
- [105] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation* 1ed. Wiley-IEEE Press, 1996.
- [106] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 1 ed. Wiley-IEEE Press, 2004.
- [107] S. S. Haykin, *Communication Systems*: Wiley, 2001.
- [108] M. Berkhout, L. Dooper, B. Krabbenborg, and J. Somberg, "A 4 Ω ; 2.3W Class-D audio amplifier with embedded DC-DC boost converter, current-sensing ADC and DSP for adaptive speaker protection," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2013, pp. 180-181.

Appendix A

Complete Schematic Diagram of the Proposed Class D Amplifier

MOS	W/L ($\mu\text{m}/\mu\text{m}$)	MOS	W/L($\mu\text{m}/\mu\text{m}$)	MOS	W/L($\mu\text{m}/\mu\text{m}$)
M1	10/1	M21	10/4	M41	2.4/0.35
M2	10/1	M22	10/4	M42	2.4/0.35
M3	20/1	M23	10/2	M43	10/0.35
M4	10/2	M24	10/4	M44	5/0.35
M5	5/2	M25	10/4	M45	10/0.35
M6	10/2	M26	10/1	M46	5/0.35
M7	10/2	M27	10/4	M47	50/0.35
M8	5/2	M28	10/4	M48	50/0.35
M9	10/2	M29	10/1	M49	100/0.35
M10	5/1	M30	10/4	M50	100/0.35
M11	5/2	M31	10/4	M51	10/0.35
M12	5/1	M32	10/1	M52	5/0.35
M13	5/3	M33	2.4/0.35	M53	10/0.35
M14	5/10	M34	5/5	M54	5/0.35
M15	10/4	M35	10/2	M55	50/0.35
M16	10/4	M36	10/2.4	M56	50/0.35
M17	10/2	M37	10/2	M57	100/0.35
M18	10/4	M38	5/5	M58	100/0.35
M19	10/4	M39	1/3		
M20	10/2	M40	2.4/0.35

Appendix B

Detailed Algorithmic Sampling

Derivation

Notice that a pair of similar triangles is formed between $\Delta S_1 S_m S_4$ and $\Delta S_1 S_2 S_5$, so we could get that

$$\frac{S_m - S_1}{S_2 - S_1} = \frac{\Delta t_1}{T_s}$$

$$S_m = \frac{\Delta t_1}{T_s} \times (S_2 - S_1) + S_1$$

Similarly, we can get that

$$\frac{S_n - S_2}{S_3 - S_2} = \frac{\Delta t_2}{T_s}$$

$$S_n = \frac{\Delta t_2}{T_s} \times (S_3 - S_2) + S_2$$

$$\Delta t_2 - \Delta t_1 = T_p - T_s$$

$$S_n = \frac{T_p - T_s + \Delta t_1}{T_s} \times (S_3 - S_2) + S_2$$

Notice that a pair of similar triangles is formed between $S_m S_a$ and $S_m S_n$, so we could get that

$$\frac{S_a - S_m}{S_n - S_m} = \frac{T_{as}}{T_p}$$

And another pair of similar triangles is formed between S_a and PRCFM sawtooth waveform, from which we can get

$$\frac{S_a}{1} = \frac{T_{as}}{T_p}$$

From the above two equations, it is easy to get

And the approximate duty pulse

$$T_{as} = T_p \frac{S_m}{1 + S_m - S_n}$$

By substituting S_n and S_m into the above equation, the equation can be simplified as

$$\begin{aligned} T_{as} &= T_p \frac{S_m}{1 + S_m - S_n} \\ &= T_p \frac{\frac{\Delta t_1}{T_s} \times (S_2 - S_1) + S_1}{1 + \frac{\Delta t_1}{T_s} \times (S_2 - S_1) + S_1 - \left(\frac{T_p - T_s + \Delta t_1}{T_s} \times (S_3 - S_2) + S_2 \right)} \\ &= T_p \frac{\Delta t_1 \times (S_2 - S_1) + S_1 T_s}{T_s + \Delta t_1 \times (S_2 - S_1) + S_1 T_s - ((T_p - T_s + \Delta t_1) \times (S_3 - S_2) + S_2 T_s)} \\ &= T_p \frac{\Delta t_1 \times (S_2 - S_1) + S_1 T_s}{T_s + (T_s - \Delta t_1) \times (S_1 + S_3 - 2S_2) - T_p \times (S_3 - S_2)} \end{aligned}$$

The Author's Publications

Journal

[1] **C. Jin**, M. T. Tan and K. Y. See, "Filterless Class D amplifier with pseudorandomized carrier frequency modulation for EMI reduction," *IEEE Transactions on Electromagnetic Compatibility*, vo. 155, no. 1, pp. 74-80, Feb. 2013.

Conferences

[1] **C. Jin**, M. T. Tan and K. Y. See, "High-efficiency filterless Class D amplifier with peak detector," 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS), Mar. 2012, pp. 1-4, Mar. 2012.