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COMPACT RECTENNA ARRAY ON-PACKAGE FOR WIRELESSLY POWERED SMALL DEVICE

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SUMMARY

Wirelessly powered small device, as the name implies, is a device that powered by receiving radiated RF power. Rectenna, i.e, rectifying-antenna, is an integration of receiving antenna and rectifier circuit. The receiving antenna captures the incoming RF power and rectifier circuit converts the RF power received into DC power to power up the device.

As technology advances, wirelessly powered small devices have evolved from simple UHF RFID tags to multi-functional devices like wireless sensor platform that integrates multiple functions such as sensing, computing and communication. Such devices are gaining research interests because of their potential to be deployed for long-term sensing in wide ranging of applications, such as embedded sensor for infrastructure health monitoring and medical application.

These devices are usually designed to be light and small for ease of deployment. Each device usually integrated with a single receiving antenna and the antenna usually occupies significant space. It can be miniaturized but at the expense of efficiency and bandwidth. Also the power received by a single antenna is limited, which limits the functions that can be performed as well as the communication range of the device from the transmitter/reader. Thus the motivation of the work is to explore and develop a feasible solution of rectenna array implementation to enhance its power receiving capability and yet maintain compactness at the same time.

This thesis documents the works accomplished to develop a compact rectenna array, which covers the elaboration of the motivation, design and simulation,

implementation and measurement of the prototype. The RF receiving capabilities of the arrays have also been evaluated with the antenna array integrated with rectifier circuits. The results also show that the proposed design was capable of enhancing the RF receiving capability of the device with proper design of the array with decoupling element. The proposed design can be easily tuned to work at different UHF bands and migrated to any other fabrication technology, such as 3D printing technology.

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LIST OF ABBREVIATIONS

WPT	Wireless Power Transfer
RF	Radio Frequency
UAV	Unmanned Aerial Vehicle
SSPS	Space Solar Power System
GEO	GEosynchronous Orbit
RFID	Radio Frequency IDentification
EIRP	Equivalent Isotropic Radiation Power
ERP0	Equivalent Radiation Power
WSN	Wireless Sensor Network
COTS	Commercial Off The Shelf
PCB	Printed Circuit Board
SMD	Surface Mount Device
MPPT	Maximum Power Point Tracking
LCP	Liquid Crystal Polymer
MIMO	Multi-Input Multi-Output
DM	Differential Mode
CM	Common Mode
VNA	Vector Network Analyser
AUT	Antenna Under Test

Chapter 1

Introduction

This chapter begins with the historical development of wireless power transfer (WPT) and its envisioned application scenario, from high power to low power WPT. It is followed by more detailed discussion on wirelessly powered devices that operate at low radio frequency (RF) power density environment, especially the design of power supply module of the device, in which the rectenna plays an indispensable role to the performance of the whole module. The constraints and challenges of rectenna design for wirelessly powered device, particularly the power reception and conversion efficiency aspects, will be discussed in greater depth. Finally, the motivation and objective of this thesis are described at the last section.

1.1 Wireless Power Transfer

Wireless Power Transfer (WPT), as the name implies, is the idea to transmit power wirelessly. Its objective is different from wireless communication, as it focuses on delivering of power rather than sending information. In general, WPT can be achieved through either far field radiation, near field inductive coupling [1] or mid-range resonant evanescent coupling [2]. This thesis focuses on the WPT through far field radiation. Hence, WPT mentioned hereafter means far field WPT.

The practical application of WPT originated from the idea of powering unmanned aerial vehicle (UAV) remotely by microwave power beam from the ground back in the 1950s [3], where “Rectenna”, an antenna integrated with a rectifier circuit, was

first developed. Rectenna consists of two parts, the receiving antenna and the rectifier circuit. The receiving antenna captures incoming RF power and then the RF power passes through rectifier circuit and converts into DC power. Since then, numerous research works have been carried out to explore the potential of WPT and to expand its application spectrum. The application of WPT can be roughly divided into two categories: high power and low power WPT, which have different targeted applications, where different design methodologies are adopted to develop the system.

1.1.1. High-power Wireless Power Transfer

Figure 1-1 High-power WPT over long distance

High-power WPT, as the name implies, is to transmit high RF power from transmitter to receiver, usually over long distance. In the typical scenario of high power WPT, the receiver and the transmitter have the knowledge of each other, and the power is beamed from transmitter to the receiver to minimize the loss, as illustrated in Figure 1-1. Thus on the receiver side, to maximize the power reception, rectenna array with multiple sub-arrays or rectenna units are employed [4, 5]. The receiver is positioned in a way that polarization of receiving antenna matches with the incoming electromagnetic (EM) wave and the DC outputs from all the sub-arrays or rectennas are combined and optimized to maximize the resultant DC output [6]. Figure 1-2 shows some examples of rectenna arrays for high power WPT.

Figure 1-2 Rectenna array with different scales for high power WPT. (a) A $3.2\text{m} \times 3.6\text{m}$ rectenna array of 2304 rectenna elements for long distance high power WPT. [7] (b) Rectenna array of 25 elements for high power WPT [8].

Over the years, the research on using high power WPT to power UAV remotely continues, as the UAVs nowadays become light-weight and small [9, 10]. So it is possible to power up a UAV by transmitting power from ground using microwave so that it can stay in the air for a much longer period of time without coming back to ground to re-fuel. Similarly, high power WPT has also been adopted to explore the possibility of powering ground robotic vehicles remotely [11, 12] so that the vehicles can stay in-field for long period without coming back to replace battery or re-fuel.

High power WPT can also be extended for many other applications. One application worth mentioning is the envisioned Space Solar Power System (SSPS). SSPS describes a system using satellites located on geosynchronous orbit (GEO) to generate electrical power from solar power and transmit the power wirelessly back to earth using microwave power. Large scale rectenna arrays are constructed on earth to receive the microwave power and convert the power into DC for supply needs. The distance of this kind of power transfer is over 36,000 km from GEO to

earth, and the power transferred can be as high as 5 Giga-watt [13, 14]. The attractiveness of SPSS is that there is far more solar power available on GEO than on earth and there is no shielding of atmosphere, so the satellite can be continuously exposed to sun so that the power generated can be high and stable [13]. SSPS has conceptualized a renewable and eco-friendly way of generating electrical power to replace the use of fossil fuels. This very idea stimulated a lot of research work on the development of rectenna arrays for long distance WPT [7, 8, 15].

Other than remote powering of air and ground vehicles and SSPS, high power WPT has also been explored for applications in other areas. Research works have been carried out to develop prototypes of wireless sensor and actuator devices with rectenna integrated that needs to be embedded into the infrastructure for Structural Health Monitoring (SHM) [16-18] [19]. With the devices powered by WPT, there is no need to either installing wire for powering or replacement of battery. Therefore deployment and maintenance cost can be reduced significantly [16]. Similar ideas has been applied in space application, in the work proposed in [20], WPT was used to power actuators of the space telescope to simplify the power distribution design by eliminating wiring for power.

1.1.2. Low-power Wireless Power Transfer

For low-power WPT, the receiver is usually a small and low power consumption device; and typically has no knowledge of the transmitter. So antennas with omnidirectional pattern are usually used to receive power for such device. Such antenna has lower gain and therefore the device is less efficient in receiving RF power from the transmitter than its counterpart in high power WPT. In typical application scenario, the device can only operate within certain range of transmitter

where enough power can be received and the transmitter can power up multiple devices in the range, as represented by the illustration shown in Figure 1-3.

Figure 1-3 typical application scenario of low power WPT with transmitter powering up multiple devices in range.

Low-power WPT can be further divided into two scenarios, depending on how the device receiving the RF power from the transmitter. One scenario is that the device is powered by harvesting RF energy existed in the ambient environment [21, 22]. While the other is that the device is powered by receiving RF power transmitted from a dedicated transmitter.

a) Devices powered by harvesting ambient RF energy

This scenario looks attractive that the device can be powered by harvesting RF energy from ambient environment. However, in fact, the device is powered up by receiving power from existing broadcast transmitters for communication purpose, such as TV transmitter, GSM base station, WiFi access point and other similar sources. Due to the wide coverage of the communication network, especially in urban area, RF power is almost universally available. The RF energy harvesting can be performed on single frequency band [23, 24] or wide-band that covers multiple frequency bands [21, 25, 26]. However, according to multiple surveys conducted [24, 27], the power level from these transmitters may not be high enough to power

up the device unless the device is positioned close enough to the transmitters. Besides, the power level also fluctuates significantly from time to time depending on the traffic load and different time periods of a day [28].

Quite a number of researches have been carried out in the direction of powering devices by harvesting ambient RF energy. It has been demonstrated in [23, 24] [28-30] that signals from TV broadcast tower was harvested and rectified and power up devices with low power consumptions such as digital clock, digital thermometer, and sensor node. In [24, 28], the devices are positioned only a few hundred meters from the TV broadcast tower, and it is reported in [24] that it took 1500 minutes to accumulate enough energy to make the digital clock operate for merely 10 seconds. In the work done in [23, 29, 30], the devices was positioned a few kilometres away from the TV broadcast tower but in both works the antenna is positioned at line-of-sight with the transmitter and the devices in [23, 30] even used high gain Yagi antenna to point at the transmitter in order to receive enough power. A citywide survey and evaluation was conducted and reported in [25], and the result showed that around half of the locations surveyed have high enough ambient RF energy to power up the prototype developed in the work.

The literature review has shown that although RF energy is almost universally available, RF energy harvesting is still far from universally feasible. There are constraints in locations and time period depending on whether the level of ambient RF energy is high enough to power up the device. To break these constraints requires continual research work on devices with lower power consumption and more efficient and sensitive RF energy harvesting circuit.

b) Device powered by dedicated RF power source

To ensure stable of RF energy, devices powered by a dedicated transmitter is a more feasible solution for low power WPT. One well-known application is radio frequency identification (RFID) [31], especially for RFID operating at ISM band (865-868 MHz in Europe, 902-928 MHz in the USA). As technology advances, more functions are added, besides the simple RFID function, such as sensor enhanced RFID tag [32], wireless sensor node utilizing RFID protocol [33, 34]. The majority of these devices are developed to operate at the UHF RFID frequency band around 900 MHz or 2.4 - 2.5 GHz ISM frequency band. The transmitted power in these frequency bands are capped by regulations of different regions in terms of Equivalent Isotropic Radiation Power (EIRP) or Equivalent Radiated Power (ERP). EIRP uses the ideal isotropic antenna as the reference radiator and is calculated from the total power transmitted by transmitter and the gain of the transmitting antenna by the following equation:

$$\text{EIRP (dBm)} = P_t(\text{dBm}) + G_a(\text{dB}) \quad (1-1)$$

Where P_t is the total power transmitted and G_a is the gain of the transmitting antenna. On the other hand, ERP uses half-wavelength dipole as the reference antenna and the relationship between EIRP and ERP is expressed as follows:

$$\text{EIRP(dBm)} = \text{ERP(dBm)} + 2.15 \text{ dB} \quad (1-2)$$

Table 1-1 presents a list of maximum EIRP of UHF frequency band and 2.45GHz ISM frequency band of several countries and regions.

Table 1-1 Regulation on maximum EIRP on UHF RFID frequency bands and 2.4GHz-2.5GHz ISM band from several countries and regions.

Country/Region	Frequency Band	EIRP (dBm)
USA[35]	902 – 928 MHz	36 dBm*
	2.4 – 2.5 GHz	36 dBm*
Europe[36]	868 – 868.6 MHz 868.7 – 869.2 MHz	16.15 dBm ^{&}
	869.3 – 869.4 MHz	12.15 dBm ^{&}
	869.4 – 869.65 MHz	29.15 dBm ^{&}
	869.7MHz - 870MHz	9.15dBm ^{&}
	2.4 – 2.5GHz	10 dBm
Singapore[37]	866 – 869 MHz 920 – 925 MHz	29.15 dBm ^{&}
	2.4 – 2.5 GHz	23 dBm
China[38]	920.5 – 924.5 MHz	35.15 dBm ^{&}
	2.4 – 2.5 GHz	20 dBm

*. Limit for frequency hopping with more than 75 channels and digital spread spectrum.

[&]. EIRP in the table is converted from ERP in the original document using equation (1-2).

Similar to high-power WPT, wirelessly powered a small device with wireless communication capability eliminates the need of wiring for power when deploying the system. Besides, since the power transmitted is relatively low, the transmitter can be designed to be compact and portable. As a result, the deployment and maintenance of such system becomes relatively easy, flexible and economical. A lot of research works have been reported to explore the possibility to implement the system in various applications.

One popular application is to integrate sensor into the device to develop wirelessly powered sensor node for Wireless Sensor Network (WSN) [39], which is the key component of many innovations, such as the concept of Smart Building or Building Automation [40]. Smart Building is the concept of making the living space intelligent by monitoring the environment condition of the building, such as

temperature, humidity, light and movement of person so that the building can adjust itself to create a comfortable and energy-efficient environment for people living within the building [41]. Such system requires a complicated sensor network with various sensor nodes, which will be very expensive to setup if cables are used for the powering and signalling for each sensor node [42]. The introduction of Wireless Sensor Network with each sensor node powered wirelessly can make such system affordable with the elimination of cabling. Prototypes of compact low-power consumption sensor node based on RFID protocol, which can sense temperature and light, have been developed [33, 34, 43]. In [44], a wirelessly powered temperature and humidity sensor node was developed and demonstrated by integrating rectenna into a Commercial-off-the-shelf (COTS) wireless sensor. There are also compact sensors under development for other applications. The work done in [45] proposed a compact antenna design for light-weight sensor node for weather tracking.

As technology advances, the spectrum of exploration has been expanded into medical application. Low power consumption wireless sensor node has great potential in developing long-term monitoring system of human health condition for various purposes such as chronic disease management, elder care, wellness enhancement, lifestyle monitoring and so on [46]. Different small wirelessly powered small sensors that can either attach to human body or imbedded into human organ or tissue for biomedical signal monitoring, have been developed [47] [48-50]. There is a device developed to attach onto human body to monitor heart condition [47]. There are also other devices developed to be implanted into eyes for intraocular pressure monitoring [48-50]. The device developed in [50] has temperature integrated which makes the measurement of pressure more precise and provide temperature data at the same time. In recent year, the issue of transmitting

wireless power into human tissue has been re-investigated and found out that the optimum frequency range lies in GHz range, which opens a new era for the development of miniaturized implantable device [51]. Research work is on-going to develop small wirelessly powered medical device that can be implanted into human body [52-56].

The above literature review has shown that continuous research has been carried out to expand the application spectrum of wirelessly powered devices, especially for medical applications and highly-compact sensor node to achieve long-term reliable and maintenance-free monitoring and sensing. For some applications, the working prototypes have been demonstrated, while others are still in development and making good progress. Investigating the designs of different proposed devices has revealed that the trend is for the device to be highly compact and light-weight in order to be easily deployed into the application environment. In addition, these devices must also be power efficient. Therefore, it is necessary to take a closer look into the design of the device to get some insight on how the device can be designed to be power efficient.

1.2 Wirelessly Powered Small Device

This sections looks into the structure of wirelessly powered small device. First, the overall structure and typical operating mechanism of the device is briefly described. Then the focus will be shifted to the design of power module for such device to lay ground for further detailed discussion on the design of rectenna, which is a part of the power module.

1.2.1. Overview

In general, any device to be powered by wireless RF energy can be represented by the circuit block shown in Figure 1-4. From the functional perspective, the device consists of two parts, the power module and the application specific module. The power module is to receive, convert and deliver DC power to the application specific module. Application specific module consists of components such as microprocessor, sensor, memory, ADC and communication antenna to fulfill the required function defined by the user.

Figure 1-4 Block diagram of a typical wireless RF powered device

As for the design of antenna, for devices communicating using back-scattering method like RFID, single antenna is used for both power-receiving and data communication. For other devices, separate antennas are used for RF power receiving and data transfer [57]. However, there is also dual-antenna system for back-scattering communication to improve communication reliability and reading range with one antenna for power receiving and the other for back-scattering data transfer [58].

Whether to integrate all the circuits on a single chip is a trade-off between compactness and cost effectiveness. For devices with very low power consumption and extreme compactness, such as RFID and medical implant, the circuit can be integrated onto a single chip. Thanks to the advancement in low-power circuit design and fabrication, the circuit consumes less and less power, so more and more functions can be integrated with the same amount of power available. There are commercial chips with very low power consumption that can be used to develop wirelessly powered small device, such as MSP430 low-power consumption microprocessor from Texas Instrument [59], has already been used for the design of energy harvesting devices [29, 33, 57].

With the scarcity of received power, wirelessly powered device is designed to operate in sleep-active cycle to minimize the power consumption. The device stays in sleep mode to minimize the power consumption, when there's enough amount of energy stored and incoming request, the device wakes up, execute the specified tasks and then goes into sleep mode again. Figure 1-5 shows a simple illustration of the power and energy consumption curve of a typical operating cycle.

Figure 1-5 Power and energy consumption curve during a typical sleep-active cycle

The negative power consumption $P_{harvest}$ indicates that the device is receiving and generating more DC power than it consumes during sleep mode, so that energy can be accumulated until the stored energy E_{target} is sufficient to execute the required tasks during the active period. During the active period, the power consumption rises up significantly to P_{op} . In Figure 1-5, the power consumption is treated as constant for simplicity, but in reality the power consumption varies with different tasks performed during the active period [60, 61]. At the end of active period, supply voltage drops to a certain level, the application specific circuit stops operating and device goes into sleeping mode again. The energy remained in the storage corresponding to the voltage level denoted as $E_{residue}$. Then the power consumption drops to the negative $P_{harvest}$, and energy gradually accumulates in the storage again until the next active period.

1.2.2. Power Module

Figure 1-6 Block diagram of receiving antenna and power module

After a brief overview on the structure and operating mechanism of wirelessly powered device, let's zoom into the structure of power module. The power module of a typical wirelessly powered device can be presented by the block diagram shown in Figure 1-6.

The receiving antenna receives the incoming RF power and RF-DC rectifier converts the received RF power into DC voltage. Matching circuit is inserted in between for maximum power transfer from receiving antenna to the rectifier circuit. To achieve high compactness, the matching circuit is usually integrated into the antenna. The receiving antenna is designed to have an impedance that is complex conjugate to the input impedance of the rectifier circuit [62]. The rectifier circuit is in general non-linear. Its performance is determined by the DC load as well as the level of incoming RF power. It is typical for the received RF power to fluctuate and it affects the DC output of the rectifier. Besides, the current consumption of the application specific circuit also varies during active period due to different power consumptions for different tasks. Thus a voltage converter is necessary to regulate and to maintain the DC supply for the circuit [63]. Maximum Power Point Tracking (MPPT) algorithm can be implemented to control the voltage converter to keep the rectifier circuit operating at maximum efficiency regardless of the variation of receiving RF power [64].

The energy storage unit stores the harvested energy and its capacity and size depends on the power requirement of the application specific circuits. For device with very small power consumption such as RFID and medical implant, an on-chip capacitor is usually sufficient to store the charge needed to power up the circuit. But for other devices with relatively higher power consumption, off-chip component such as super-capacitors and/or batteries are needed. Super capacitor can be charged easily like a capacitor and can be connected directly after the rectifier circuit. But the drawback of super capacitor is its high leakage current. Rechargeable battery used to be unflavoured due to a few drawbacks like bulky size, the need for complicated charging circuit and memory effect (NiMH battery) [65]. But the

emergence of thin-film Lithium battery makes battery a promising energy storage option for wirelessly power device.

Thin-film Lithium battery was developed by the driving force of developing a small form-factor power source for small consumer and medical devices and eventually it is even able to be integrated with circuits on IC [66]. Commercial products of small thin film Lithium battery are available, for example, battery from *cymbet* has a size of SMD component that can be assembled on printed circuit board (PCB) [67]. Thin-film battery developed by *Front Edge Technology* and *Power Stream Technology* are small and flexible [68, 69]. Prototypes of micro-sized thin-film batteries that can be fabricated on silicon wafer have also been developed and currently further research work is continued on developing 3D structure of thin-film battery for higher capacity [70].

1.3 The Design of Rectenna

The power efficiency of a wirelessly powered device can be characterized by a term called sensitivity. Sensitivity is defined as the minimum power required to power up the device [71] [72]. The sensitivity of a device is determined by the power consumption of application specific module, as well as the power receiving capability and conversion efficiency of the power module, where rectenna plays a determinant role. With an overview on the structure of power module, this thesis further focuses on the design of rectenna. This section presents a detailed introduction and review on rectenna design for small device, covering both parts of the rectenna, the rectifier circuit and the receiving antenna.

1.3.1. RF-DC Rectifier Circuit

Figure 1-7 Schematic of rectenna with single-diode rectifier

The simplest RF-DC rectifier is a single Schottky diode as shown in Figure 1-7. The structure is widely used in high power WPT [3, 4]. As transmitted power is high, the received power can generate sufficiently high DC voltage at the output of the rectifier circuit. Therefore a single Schottky diode with filters is sufficient to be used as a rectifier circuit to minimize the conversion loss.

However, for low power WPT, the power received is so low that the DC voltage obtained at the output of a single-diode rectifier is too low to operate the circuitry connected at the DC output. Thus rectifier circuits that are capable of both rectifying the incoming RF wave into DC and boost the DC voltage at the same time, which is called voltage multiplier, have been proposed for such device. Figure 1-8 shows a few topologies of such voltage multiplier circuits, the cascaded four-transistor cells [72] (Figure 1-8(a)), multi-stage Villard voltage multiplier (Figure 1-8(b)), two-stage modified Greinacher voltage multiplier [73] (Figure 1-8(c)) and multi-stage modified Dickson charge pump (Figure 1-8(d)). Majority of the voltage multiplier circuits are constructed with capacitors and diodes. There is even an algorithm proposed to generate different topologies of voltage multipliers with diode and capacitor network [74]. Voltage multipliers typically have repeated patterns, each called a stage. Each stage functions as a rectifier circuit alone to

rectify the incoming AC wave into DC. The DC voltage generated by each stage adds up to form the DC voltage which appears at the final DC output of the voltage multiplier circuit. Generally speaking, the more number of stages, the higher the DC voltage, but usually at the cost of lower conversion efficiency due to the increased loss caused by increased number of diodes or transistors.

Figure 1-8 Voltage multiplier circuits with different topologies. (a) Cascaded four-transistor cells[72] (b) Multi-stage Villard voltage multiplier (c)Two stage modified Greinacher voltage multiplier[73] (d) Multi-stage modified Dickson charge pump circuit

Among various rectifier circuits proposed, modified Dickson charge pump as shown in Figure 1-8(d) has been widely used for its simple structure. It can be easily implemented on PCB using discrete Schottky diode and capacitors. It is also

easy to implement on IC with diode-connected transistor to ensure compatibility with standard CMOS process, as illustrated in Figure 1-9 [75-77].

Figure 1-9 Diode connected MOSFET transistor

Like any rectifier circuit, there is inevitably voltage drop which equals to the turn-on voltage of the diode during the AC to DC conversion process. The input power to the rectifier circuit needs to be high enough such that the amplitude of AC signal is higher than the turn-on voltage of the diode for the rectifier circuit to operate. For a typical operating scenario of wirelessly powered device, the received power is so low that the amplitude of the input AC waveform is usually comparable to the turn-on voltage of the diode [75]. As a result, the output DC voltage is very low as the majority of voltage is lost to turn on the diode.

To increase the output DC voltage under very low input power condition, it is important to select a Schottky diode with low turn-on voltage. For case of voltage multiplier circuits on IC, different solutions were proposed to reduce the turn-on voltage of the diode-connected transistor by different researchers.

Figure 1-10 Conceptual illustration of biasing circuit to bias the gate of transistor. The battery sign represents biasing circuit.

One way of lowering the turn-on voltage is to add a biasing circuit to bias the gate of transistor so that the turn-on voltage of the diode-connected transistor can be reduced. Figure 1-10 shows the conceptual illustration of the idea, in which the biasing circuit is represented by battery sign. Different designs of biasing circuit have been proposed by various researchers [78-82]. In [79-81], the gate was biased by passive network which derive voltage from the energy storage. In [82], the biasing voltage is applied to the gate in series of timed pulses. In [78], a “floating gate” was created by inserting MOS capacitor between the gate and the drain of diode-connected PMOS. Then charge was injected and trapped inside the “floating gate” and the gate was biased by the voltage developed across the MOS capacitor. It was claimed that the charge can stay “trapped” for years.

Other than introducing biasing circuit to bias the gate, fabrication technology can be exploited to fabricate devices, diode or transistor, with low turn-on voltage. In [73], special process (Silicon-on-Sapphire) was used to fabricate Schottky diode with low turn-on voltage, but the fabrication cost is higher than the conventional CMOS process. There are works that use the native transistor from CMOS process for diode-connected transistor due to its extremely low turn-on voltage. With the dimension of transistor and the number of stages optimized for the specified input and output condition, the rectifier can also generate specified DC output with fair conversion efficiency at low input power without introducing extra biasing circuit [75, 76].

1.3.2. Receiving Antenna

For wirelessly powered devices where compactness is important, the receiving antenna has to be miniaturized in order to fit into the small space of the device.

There are many techniques to reduce the size of antenna, such as folding, meandering, material loading and using periodical structures [83]. Meandering is a simple and one of the most popular methods to reduce the size of the antenna. When an antenna is meandered, the radiation arm of the antenna is folded repeatedly, so parasitic inductors and capacitors are formed in the folded part which causes the antenna to have a much lower resonant frequency than the antenna with straight radiation arm [84]. Figure 1-11 shows an illustration of meander line antenna and conventional monopole with equal wire length. For meander-line antenna, the current flowing on the adjacent parallel section of meander line has opposite phase and contributes little to the radiation. Only the current flowing on the vertical sections contributes to the radiation, which is less efficient than conventional monopole as the current flows along the whole arm contributes to the radiation. Therefore, with equal wire length and diameter, the meander-line antenna is “less effective” in utilizing the current flow along the path to radiate comparing to conventional antenna, but produces the copper loss nevertheless along the wire. Meander-line antenna has achieved size-reduction with respect to the conventional monopole at the cost of smaller bandwidth and lower radiation efficiency [85]. Meander line antennas are so widely used that this work can’t survey all the literatures, and there are quite a number of works that uses meander line antenna as receiving antenna in RFID tag [58, 62, 86-89] or RFID-enabled device [44].

Figure 1-11 Straight monopole antenna and meander line monopole with same wire length.
Arrows represents the flow of current.

To the author's best knowledge, the majority of the miniaturized designs proposed for small wirelessly powered devices are based on planar design, where the antenna shares the same planar space with the circuits. It is suitable for RFID tag as the envisioned application of RFID to replace barcode. So it requires the RFID tag to be flat and flexible so that the tag can be pasted onto the surface of various goods. The RFID tag antenna occupies the majority of the space and the circuit component is only a tiny imprint. But for devices with multiple electronic components such as microprocessor, sensors and battery integrated, the space occupied by circuit is no longer insignificant. A planar design with circuits and antenna shares the same plane may not be the optimum solution to achieve high compactness.

Therefore antenna on package was proposed as a solution to efficiently utilize the small space available to achieve high degree of compactness. Instead of competing for space with electronic components on circuit board, the 3D space around the device is explored and antenna is implemented on the package of the device so that the internal space is freed up to house the electronic circuits. Various designs of 3D antennas on package have been proposed. The work done in [90] proposed an electrically small antenna printed onto a hemi-spherical case by directly printing

silver ink onto it, as shown in Figure 1-12(a). In [45], a meandered dipole antenna with parasitic radiator was fabricated on Liquid Crystal Polymer (LCP) and folded into a cubicle to achieve light-weight and omni-directionality, as illustrated in Figure 1-12(b). Figure 1-12(c) shows another design [53], where the antenna was fabricated along the edge of the cubicle for implantable medical device. In [91], a meandered dipole antenna was developed for narrow band sensor node operating at 2.4 GHz on the interior of a cube by 3D printing, as shown in Figure 1-12(d).

Figure 1-12 Various 3D Antenna-on-package design proposed. (a) Meandered antenna printed on hemisphere [90] (b) Meandered dipole with parasitic resonator on LCP cubicle [45] (c) Antenna- Design proposed in [53] (d) Folded meandered dipole proposed in [91]

1.4 Motivation of Thesis

1.4.1. Constraint of Single Receiving Antenna in Power Reception

The previous section has provided an overview on the rectenna design for wirelessly powered devices. For the rectifier design, various solutions were proposed to improve the efficiency of the rectifier circuit on IC. While for the receiving antenna design, the solution proposed is mainly on the issue of achieving high compactness to meet the tight space requirement of the small device. As part of rectenna that delivers power to the device, it is necessary to take a closer look at the receiving antenna's performance on power reception.

How much power the receiving antenna can receive is determined by the antenna's property and the environment where the device is positioned. The power received by an antenna $P_{received}$ can be calculated as follows:

$$P_{received} = S \frac{G\lambda^2}{4\pi} \quad (1-3)$$

$$\text{Where} \quad G = \tau D \quad (1-4)$$

S is the power density of the RF field at the receiving antenna and G is the gain of the receiving antenna, where the gain (G) of antenna is determined by the directivity (D) and radiation efficiency (τ) of the antenna, as expressed in equation (1-4).

For small device powered by wireless power from the transmitter, the field strength at the device ranges from less than $1\mu\text{W}/\text{cm}^2$ to a few tens of $\mu\text{W}/\text{cm}^2$ [42]. As elaborated earlier, the device has no knowledge of the transmitter, so omnidirectional antenna is usually used and miniaturized in order to be integrated

into the device, either on circuit or on package to achieve higher compactness. Omnidirectional antenna means the antenna has low directivity and reduction of antenna size inevitably causes the degradation of bandwidth and radiation efficiency. Equation (1-4) implies that low efficiency and low directivity leads to lower gain of receiving antenna and hence leads to lower power received, as indicated by equation (1-3).

As a result, compactness comes with a price of low RF power receiving capability. With regulation on the maximum power can be transmitted, the power from transmitter can't be indefinitely high. So the device needs to stay close enough to the transmitter so that the power density can be high enough for the receiving antenna to receive enough power to be converted into DC and power up the circuit. It becomes a limiting factor to deploy the device for various practical applications.

In order to increase the operating range, it is necessary to continuously push the sensitivity of the rectifier circuit to a lower level by improving the design of rectifier circuit so that the power module can operate with less power received. But less power received means less DC power for the application circuit. This poses challenge on the design of application specific circuits as the power consumption needs to be scaled down accordingly to meet the tight power budget.

On the other hand, improving the receiving antenna design to enhance its ability to receive more power, is a more plausible idea because as mentioned earlier, rectifier circuit is a non-linear circuit and the conversion efficiency is positively related to incoming RF power. If receiving antenna is able to receive more power, more RF power will go into the rectifier circuit and the circuit will also become

more efficient. So improving the receiving antenna design on the performance of power module has a bigger impact on wirelessly powered devices.

1.4.2. Proposed Solution

Having identified that improving the receiving antenna design is a more plausible idea, it is important to know the best way to implement it. Intuitively, it is easy to think using rectenna array to be an effective way to increase power received due to extra receiving antenna. There are results showing that more DC power can be obtained in terms of higher DC voltage with multiple rectenna units connected in series [92]. However, the obvious challenge is how to develop a highly compact rectenna array to enhance the power receiving capability of the device and maintain high compactness at the same time.

Conventional methods of making rectenna array physically compact are either increasing the operating frequency or miniaturize each antenna element. The spacing between antenna elements is always kept to no less than around half wavelength. So the question here comes to is whether there is a way to make the antenna array compact by reducing this spacing between the elements?

The answer to the question is “yes”. This design of compact antenna array with antenna element positioned in close proximity to each other has been addressed for MIMO communication. Several published works have shown that when antenna array elements get too close to each other, the inter-coupling effect between the elements degrades radiation efficiency of individual antenna element, which affects the performance of antenna array on signal communication [93] [94, 95]. Various compact antenna designs have been proposed with solutions to decouple antenna

array elements for improved signal communication such as more channel capacity and better SNR performance without increasing the transmitting power [96-101].

However, there is very little work exploring the design of compact antenna array for WPT purposes, in which the received power is the major concern. A compact dual-dipole array decoupled by inserting reflector and director for each element was proposed for RF power receiving, but the design is planar and how the inter-coupling impact the array performance in terms of RF power reception was not reported [102]. Inspired by the idea of antenna-on-package, this thesis aims to explore and develop a feasible solution of implementing compact antenna array on package to enhance RF power receiving capability and high compactness at the same time.

1.5 Objective

The objective of the thesis is to explore a compact antenna array design on package. Because of the compact design, the impact of the inter-coupling between array elements on the RF power reception performance of the array will be investigated. Solutions will be proposed to resolve the issue so that the proposed array enhances the RF power receiving capability. A prototype has been fabricated by printing silver ink on highly flexible PET sheet so that it can conform to the shape of the electronic package. The prototype is characterized experimentally, and the measurement results will be compared with the simulation result to verify the design methodology. Finally, the performance of prototype will be evaluated in terms of received RF power with the prototype connected to the rectifier circuits.

1.6 Scope of Thesis

This chapter starts with the development of wireless power transfer and states the objective and motivation of the thesis. The remaining chapters are organized as follows:

Chapter 2 describes the design of rectifier circuit to be used in this thesis. As Modified Dickson charge pump is adopted as the rectifier circuit, it is described in detail, including the operating mechanism, circuit analysis, modelling, as well as design considerations. The measurement result to evaluate the prototype developed is also covered.

Chapter 3 focuses on the design of compact antenna array. The design issues of compact antenna array are discussed and the proposed design is introduced. The design considerations on the isolation structure are also described.

Chapter 4 presents the measurement process and analyses the results. The measurement setup is introduced and the theory behind the measurement methodology is also be discussed in details. The measurement results are presented and analysed.

Chapter 5 concludes the thesis and discusses possible future work that is worth exploring further.

Chapter 2

Rectifier Circuit Design

As part of the “rectenna”, the rectifier circuit converts the received RF signal from the receiving antenna to DC. In this work, the rectifier circuit will be developed and integrated with the receiving antenna so that the performance of the rectenna can be evaluated. As mentioned in Chapter 1, the input impedance of the receiving antenna must be the complex conjugate to the input impedance of the rectifier circuit for maximum power transfer purposes. Besides impedance matching between the antenna and rectifier circuit, the performance of the rectenna is also influenced by its input received power and the output DC load. So it is important to understand the design of rectifier circuit and how the design can affect the input impedance and the performance of the rectifier circuit before the antenna array is designed.

This chapter describes the operating principle of Modified Dickson charge pump, which is chosen as the voltage multiplier circuit adopted in this thesis. Design considerations of the circuit will be elaborated, including the choice of diodes and the determination of number of stages. How the change of input power and DC load influences the input impedance and conversion efficiency will also be discussed. Finally, a prototype will be designed and developed with its performance evaluated by measurement.

2.1 Overview

Figure 2-1 shows an N-stage modified Dickson charge pump circuit. It is constructed by cascading several single-stage voltage doublers, as presented in Figure 2-2. A single-stage voltage doubler consists of two pairs of diodes and capacitors. Capacitor C_{2n-1} also serves as DC blocking capacitor, while capacitor C_{2n} is used to store charges after the AC signal is rectified by each stage. At the same time, C_{2n} also serves as a low-pass filter at the DC output to bypass the high frequency harmonics generated by the diode.

At steady state, each diode-capacitor pair (D_{2n-1} and C_{2n-1} , D_{2n} and C_{2n}) forms a half-wave rectifier and operates alternatively for each half cycle of input AC signal. For the n^{th} stage presented in Figure 2-2, the DC voltage generated at this stage adds up onto the reference voltage V_{n-1} of the previous stage and in this way the DC voltage adds stage by stage, until the n^{th} stage. The potential difference between the DC output of the n^{th} stage and the ground, which is the voltage (V_{2N}) over the capacitor C_{2N} of the last stage, becomes the resultant DC output of the rectifier circuit.

Figure 2-1 Multi-stage diode-capacitor AC-DC voltage multiplier

 Figure 2-2 The n^{th} stage of N-stage AC-DC voltage multiplier

2.2 Operating Mechanism

 Figure 2-3 Equivalent circuit when one of the diodes is turned on. (a) wave form of input signal (one cycle of sine wave) (b) equivalent circuit state at t_1 (c) Equivalent circuit state at t_2

This section elaborates the operating principle of the circuit for a complete cycle. The input voltage is assumed to have a waveform as shown in Figure 2-3(a) whose amplitude is denoted as V_{RF} . For simplicity, the diode is assumed to act like an ideal switch with a turn-on voltage of ΔV . The capacitors are assumed to be large enough that there is no voltage drop over C_{2n-1} and V_n can be assumed to be constant. The

input voltage level is assumed to be very low that V_{RF} is comparable with ΔV . Thus the diode can only be turned on at the vicinity of positive/negative peak of the wave. Let V_{n-1} be the output DC voltage at $(n-1)^{\text{th}}$ stage and V_n be the output DC voltage for the n^{th} stage.

As the cycle starts, $V_{in} = 0$ V, both diodes are off. Then as V_{in} goes down, V_{xn} goes down as well. When V_{in} reaches a point at the vicinity of $-V_{RF}$ where V_{xn} is ΔV lower than V_{n-1} , D_{2n-1} is turned on and for a short period of time t_1 (indicated in blue in Figure 2-3(a)) ΔQ_1 amount of charge stored on C_{2n-2} of the $(n-1)^{\text{th}}$ stage moves to C_{2n-1} , as represented by blue arrow in Figure 2-3(b). The time period t_1 is so short that it can be approximated that $V_{in} \approx -V_{RF}$ during this period. Thus at the end of period t_1 , the voltage over the C_{2n-1} can be expressed as:

$$V_{C_{2n-1}} = V_{n-1} - \Delta V + V_{RF} \quad (2-1)$$

As V_{in} rises from $-V_{RF}$, D_{2n-1} turns off and remains off for the rest of the cycle. When V_{in} reaches the vicinity of V_{RF} , diode D_{2n} is turned on and for a very short period of time t_2 , ΔQ_2 amount of charge flows from C_{2n-1} to C_{2n} . With the assumption of period t_1 , the voltage over capacitor C_{2n} at the end of t_2 can be represented by:

$$V_n = V_{C_{2n-1}} + V_{RF} - \Delta V \quad (2-2)$$

By solving equations (2-1) and (2-2) and eliminating $V_{C_{2n-1}}$, V_n can be obtained as follows:

$$V_n = V_{n-1} + 2(V_{RF} - \Delta V) \quad (n \geq 1) \quad (2-3)$$

Let $V_0 = 0$ to present the ground. If $n = 1$, which represents the 1st stage, by iterating (2-3) up to $n = N$, the relationship between the DC output V_{DC} and the amplitude V_{RF} of the input AC voltage for an N -stage rectifier can be obtained by:

$$V_{DC} = 2N \times (V_{RF} - \Delta V) \quad (2-4)$$

Equation (2-4) shows that if $V_{RF} \gg \Delta V$, the DC voltage is simply a multiplication of the amplitude of the input signal where the times of multiplication is determined by the number of stages, therefore the name “voltage multiplier”. As mentioned in Chapter 1, ΔV is significant comparing to V_{RF} , and many solutions have been proposed to reduce ΔV for the circuit implemented on IC. While for circuit implemented using discrete components on PCB, there is not much room to play on the optimization of the device, thus it is important to choose a diode with low turn-on voltage, such as Schottky diode. Study has shown that the turn-on voltage of the diode is determined by the DC current [103] and also Schottky diode comes with high reverse leakage current which can be significant for low power operation [75]. Both of these factors need to be considered when designing the voltage multiplier circuit for this work.

2.3 Design of Voltage Multiplier

In this thesis, to design the voltage multiplier for low input power, conversion efficiency and DC voltage generated at the DC output are the two major design concerns. The primary goal of designing the rectifier circuit is to generate sufficiently high DC voltage to enable the power management circuit, at the same time achieve high conversion efficiency. It is a challenging task due to the nonlinear nature of the circuit. The conversion efficiency and the output DC voltage of the

circuit is influenced by a few factors, such as the characteristic of the diode, the input power level, DC load and the number of stages. In addition, the rectifier must also be well matched with the antenna in order to achieve maximum power transfer. Therefore how the input impedance is affected by the above-mentioned factors needs to be properly analysed and investigated.

This section studies the influences of these factors on the performance of the voltage multiplier circuit through circuit simulation. To handle the nonlinear nature of the circuit, Harmonic Balance from ADS is chosen to simulate the circuit.

2.3.1. Selection of Diode

As mentioned in Section 2.1, the characteristic of the diode is critical to the performance of the voltage multiplier circuit. As the input power is low, the diode must have low turn-on voltage in order for the circuit to operate. Unlike designing such circuit on IC, where the diode or diode-connected transistor can be customized individually to optimize the performance for a certain input power and DC load [75], this degree-of-freedom is not available when designing the circuit using discrete components on the PCB. So it is important to choose a good diode with the desired characteristics. The literature review reveals that SMS7630 Schottky diode from Skyworks [104] and HSMS2850 Schottky diode from Avago [105] are popular choices for such rectifier circuits [21, 106]. Hence, the performances of these two diodes are evaluated using a single-stage Modified Dickson charge pump circuit, as shown in Figure 2-4.

Figure 2-4 Single stage Modified Dickson charge pump

The input is single-tone sine wave set at 900MHz whose amplitude is denoted as V_{in} . An ideal resistor R is connected at the DC output as the DC load and V_{dc} represents the DC voltage generated. For the capacitor used in the rectifier circuit, capacitor C_2 should be large enough so that the voltage ripple over C_2 is insignificant to ensure constant output DC voltage. Also, capacitor C_1 should be large enough so that the AC voltage drop over C_1 is small. For low-power application, a parameter sweep on the value of capacitor through simulation shows that capacitor size larger than 10 pF is sufficient to achieve both purposes. Larger capacitor further improves the performance but the improvement becomes quite insignificant. Therefore, for the development of this prototype, the capacitor value is chosen to be 10 pF. The diode is modelled by SPICE model parameters extracted from the datasheet of the component, and the parameters are listed in Table 2-1.

Table 2-1 List of SPICE Model parameters of HSMS2850 and SMS7630

Parameters	HSMS2850	SMS7630
I_s	3.1×10^{-6} A	5×10^{-6} A
R_s	25 Ohm	20 Ohm
N	1.06	1.05
T_t	-	1×10^{-11} sec
C_{jo}	0.18 pF	0.14 pF
V_j	0.35 V	0.34 V
M	0.5	0.4
B_v	3.8 V	2 V
I_{bv}	3×10^{-4} A	1×10^{-4} A

Xti	2	2
Eg	0.69	0.69

To evaluate the performance of the diode in the circuit, RF-DC conversion efficiency of the circuit is simulated with the load resistor R varies from $0\ \Omega$ to $250\ \text{k}\Omega$ for different value of V_{in} . RF-DC conversion efficiency is expressed by the ratio between the DC power dissipated on DC load and the real power received from the power source, denoted P_{DC} and P_{in} respectively in Figure 2-4:

$$RF - DC\ Efficiency = \frac{P_{DC}}{P_{in}} \quad (2-5)$$

The results for both diodes are summarized and plotted in Figure 2-5. In general, the results show that the behaviour of both diodes are quite close to each other but the maximum RF-DC conversion efficiency of SMS7630 is slightly better than that of HSMS2850. Therefore, SMS7630 is chosen for the construction of the voltage multiplier in this thesis and the circuit model of SMS7630 will be used for the all the analyses presented hereafter this section.

Figure 2-5 RF-DC conversion efficiency of SMS7630 and HSMS2850 vs. DC load for different input signal amplitude.

2.3.2. DC Voltage and Conversion Efficiency

The RF-DC conversion efficiency curves for SMS7630 as shown in Figure 2-5 is re-plotted in Figure 2-6(a), together with the DC voltage generated over the DC load plotted below in Figure 2-6(b). As highlighted by the vertical dotted line in the plot, there exists a constant DC load resistance where the RF-DC conversion efficiency of the circuit is maximum for input signal amplitude ranging from 0.1 V to 0.5 V. Similar characteristic has been found on single diode rectifier circuit and it indicates that the design of power management circuit can be simplified to keep the load constant to this optimum load rather than adjusting the load according to the input power [63].

Figure 2-6(b) shows that DC voltage increases with increasing R . The reason is that higher load resistance leads to lower DC current. Lower DC current requires less total charge passes through the diode during the turn-on period, which in terms, leads to lower instantaneous current passing through the diode and hence less voltage drop over the diode. Therefore, by observing equation (2-4), a higher DC voltage is generated at the output of the voltage multiplier.

Figure 2-6 RF-DC conversion efficiency and DC voltage of single-stage Modified Dickson charge pump vs. DC load for different input signal amplitude. (a) RF-DC conversion efficiency (b) DC voltage.

Comparing Figure 2-6(a) and (b), it shows that maximum conversion efficiency does not happen at maximum output DC voltage. However, the increase in output voltage slows down when load resistance increases beyond the optimum load. When the DC load is larger than the optimum load, as mentioned earlier, the DC current required is low and the DC voltage is high. Hence higher DC reverse biasing voltage is imposed on each diode, and leads to the increasing of leakage current. The power loss in this region is dominated by power loss due to this increasing leakage current. On the other hand, when the DC load is smaller than the optimum load, the DC current required is high hence the loss is dominated by the power loss caused by high instantaneous current passing through the diode. Therefore, when DC load increases, the power loss due to the instantaneous current decreases and the power loss due to the leakage current increases. It is expected that

at certain point, the two losses balances and the overall power loss reaches minimum point, where the conversion efficiency reaches the maximum.

Figure 2-7 Conversion efficiency and DC output voltage vs. input power for different no. of stages (a) RF-DC conversion efficiency (b) DC output voltage

For multi-stage voltage multiplier, equation (2-4) implies that DC voltage obtained increases with higher number of stages. As charge needs to pass through diodes of each stage to reach the DC output, there is power loss whenever the charge passes through the diode. Hence power loss increases with higher number of stages, which is reflected in the simulation result shown in Figure 2-7. Figure 2-7 shows the conversion efficiency and DC output voltage as input power sweeps from -20 dBm to -3 dBm for voltage multiplier circuit with different numbers of stages. For each design of different stages, the DC load is set to the optimum DC load, thus

the conversion efficiency shown in Figure 2-7(a) represents the maximum conversion efficiency. It can be observed that for the given range of input power investigated, the DC voltage increases and the maximum conversion efficiency drops with increasing number of stages.

2.3.3. Input Impedance

To understand the influence of input voltage and DC load voltage on the input impedance, the input equivalent circuit model of the voltage multiplier must be developed first. Refer to the single-stage circuit shown in Figure 2-4, as already mentioned in Section 2.2, the DC decoupling capacitor C_1 is usually large enough to minimize the AC voltage drop over the capacitor and the charge storage capacitor C_2 is large enough so that the voltage ripple over the capacitor can be minimized. Therefore at the operating frequency of 900 MHz, both C_1 and C_2 can be treated as short circuits. The charge pump circuit can be represented by the equivalent circuit as shown in Figure 2-8 looking from the RF input of the circuit [107]. C_p represents the parasitic capacitance to the ground associated with the decoupling capacitors and diodes of each stage, R_{loss} is the equivalent resistance to account for the power loss at each stage and R_{DC} is the equivalent resistance for the converted DC power. Therefore, the input resistance is the parallel combination of R_{loss} and R_{DC} , while the input capacitance is C_p . The change of input resistance and input capacitance are plotted against different DC load and amplitude of input signal, as shown in Figure 2-9.

Figure 2-8 Input impedance of single stage rectifier circuit

Figure 2-9(a) shows the plot of input resistance, while Figure 2-9(b) shows the plot of input capacitance. A general trend observed indicates that as the DC load increases, the input resistance increases and input capacitance decreases. It is also obvious that the input capacitance decreases as the amplitude of the input signal increases, but the response of the input resistance is somewhat mixed. Figure 2-9(a) shows that the input resistance increases with input signal level when the load resistance is high, but decreases with signal level when the input resistance is low. The reverse of the trend happens at around 22 k Ω . The plots also show the input resistance changes more drastically with the input signal level for high DC load resistance than low DC load resistance.

Figure 2-9 Input impedance vs. DC load for different V_{in} (a) Input resistance (b) Input capacitance

Figure 2-10 shows the change of input impedance as the input power varies from -20 dBm to -3 dBm when the load resistance is fixed to the optimum load resistance which is 14 kΩ for single stage. As the load resistance is lower than 22 kΩ, the input parallel resistance drops from 2.6 kΩ at -20 dBm input to 2 kΩ at -3 dBm input.

Figure 2-10 Input impedance vs. input power. DC load is fixed at the optimum load.

Figure 2-11 Input equivalent circuit of N-stage modified Dickson charge pump

For multi-stage rectifiers, the input equivalent circuit can be modelled as a parallel connection of each stage as shown in Figure 2-11. Since every stage is connected in parallel, as the number of stages increases, the input resistance drops and input capacitance increases, which is confirmed by the simulation result as shown in Figure 2-12. Figure 2-12 shows the parallel input impedance as the number of stages increases from single stage to 8 stages with the DC load fixed at the optimum load for each stage. It can be seen that for the input power level selected from -20 dBm to -5 dBm, the input resistance drops and the capacitance increases with increasing number of stages. The capacitance increases from less than 1 pF for single stage to around 2 pF for 8 stages. The input parallel capacitance is expected to be higher in actual implementation due to the parasitic capacitance introduced by IC pin, PCB layout and so on.

Figure 2-12 Simulated input impedance at 900MHz vs. No. of stages for different input power level

2.3.4. Design Guidelines with Discrete Components

The conventional design methodology of voltage multiplier says that the more stages, the higher the output voltage hence the merrier. This methodology only applies to the scenario where the source can source enough current to drive the circuit no matter how the load varies. In this case, the source can be modelled as an ideal voltage source. However, for the case of voltage multiplier circuit to rectify incoming RF waveform received by antenna, the current that the source can supplied is limited by the power received. Therefore, in this case, the source should be modelled as a power source. Hence it is necessary to know the estimated input power level and the DC output voltage and current requirement before the design of voltage multiplier.

The goal of the design should be to maximize the conversion efficiency while achieving the minimum DC voltage and current required. The simulation results showed that for a voltage multiplier with certain number of stages, there is a constant optimum load resistance where the conversion efficiency is highest for an input power range. Later analysis in 2.3.2 investigated the change of DC voltage and conversion efficiency for voltage multipliers with different stages respect to their optimum DC load. The result showed DC output voltage increases with increasing number of stages but at the expense of conversion efficiency. Hence, there is a trade-off between the conversion efficiency and output DC voltage when deciding the number of stages. For higher conversion efficiency, the number of stages should be as small as possible. In addition, as the number of stages increases, the increase in input capacitance and decrease in input resistance makes the input

impedance more reactive, which reduces the bandwidth that is achievable when the circuit matched with the receiving antenna [72].

In summary, to design a Modified Dickson charge pump circuit as a voltage multiplier for a rectenna, the first step is to select a diode with low turn-on voltage. Then, the optimum DC load should be identified for each circuit with different number of stages. Then the number of stages is chosen such that it is just enough to generate the required minimum output DC voltage with specified DC output current load for a defined minimum input power level, when the DC output is terminated with the optimum load resistance.

2.4 The Evaluation of Prototype

In this thesis, a voltage multiplier was designed and developed so that it could be integrated with the antenna array to evaluate the performance of the proposed antenna array on RF power receiving capability. Since this project was focused on the development of the compact antenna array, there was no requirement on the DC output. Therefore, conversion efficiency was the sole concern for the design of voltage multiplier. Following the design guide in last section, the number of stages should be minimized. Based on the simulation result presented in Figure 2-7 and considering the fabrication deviation, both one-stage and two-stage voltage multipliers are developed and their performances were evaluated.

Figure 2-13 Circuit schematic of voltage multiplier with matching network

The voltage multiplier circuit was realised on a PCB with discrete components. The diode chosen was SMS7630 based on the evaluation done in section 2.3.1. The capacitor was 10 pF GQM series capacitor from Murata. To evaluate the performance of the voltage multiplier circuit, a matching circuit was designed to match the input of the voltage multiplier circuit to the port impedance of the instrument. Figure 2-13 shows the schematic of the evaluation setup. The voltage multiplier and matching network were on separate PCBs and connected to each other using a SMA connector. The matching network was an L-network consisting of two variable capacitors so that it could be adjusted to match both the one-stage and two-stage designs.

The voltage multiplier circuit with matching network was connected to a Vector Network Analyzer (VNA) for adjustment of the matching network to match the VNA's input impedance (50Ω) at 900 MHz with an input power of -10 dBm. Once the matching was completed, the input was switched to RF signal generator with an input power -10 dBm and frequency of 900 MHz. Resistors of different values are then connected to the DC output and the DC voltage across the resistor was measured and recorded.

Figure 2-14 showed the conversion efficiency and the DC voltage of one-stage design and two-stage design as load resistance changes at an input power of -10 dBm. It showed that the 2-stage design achieves higher DC voltage with a slight drop in maximum conversion efficiency. There was some deviation between the measurement shown and the simulation results presented in Figure 2-7. The measured conversion efficiency was lower than that of the simulation result, which was expected because of the loss introduced by the matching network. Also, the parasitic components introduced by the PCB layout incurred additional loss, which

was not considered during the simulation. The 2-stage voltage multiplier circuit was chosen and to be integrated with the antenna array for further performance evaluation.

Figure 2-14 Comparison of conversion efficiency and DC voltage of 1-stage and 2-stage voltage multiplier circuit developed

Figure 2-15 Measured conversion efficiency and DC voltage vs. DC load at different input power. (a) RF-DC conversion efficiency. (b) DC voltage generated

Figure 2-15 showed the measured RF-DC conversion efficiency and the output DC voltage of the 2-stage design as the load resistance changes under different input power level. as observed in Figure 2-15(a), the efficiency curve exhibited

similar behavior as the simulation, where the conversion efficiency curves reaches its maximum at load resistance around $30\text{ k}\Omega$, and also the increase of voltage slows down when load resistance increases beyond this value. The voltage multiplier developed can achieve a maximum conversion efficiency of around 15% at low input power of -10 dBm . Figure 2-16 shows the conversion efficiency, DC voltage and DC power generated as input power varying from -20 dBm to -3 dBm for load resistances of $30\text{ k}\Omega$ and $500\text{ k}\Omega$. Figure 2-16(a) presents a clear picture on the influence of the input power on the conversion efficiency of the circuit. A 1 dB increase in the input power level leads to around 2% increase in conversion efficiency, which is no small amount considering the already low conversion efficiency at low input power region. For example, for the load of $30\text{ k}\Omega$, when the input power increases from -10 dBm to -9 dBm , where 1dB increase is equal to around 26% increase in input power, the output DC power increased for 42%. The impact of the increase input power is amplified by the non-linearity of the circuit.

Figure 2-16 Conversion efficiency, output DC voltage and output DC power vs. input power for DC load of 30 kΩ and 500 kΩ. (a) RF-DC conversion efficiency (b) DC voltage generated. (c) DC power

Other than the optimum load resistance of 30 kΩ, the performance of the voltage multiplier circuit with high-resistance load of 500 kΩ is also evaluated. As expected, the results show that although conversion efficiency is lower for 500 kΩ, higher DC voltage can be obtained. The high resistance load condition can be useful in the evaluation of performance of antenna array, as the power received can be extremely low in some scenario. With very low input power, the DC voltage will be too low to be measurable if the 30 kΩ resistor is connected at the DC output. But with high resistance load connected at the DC output, the voltage will be higher and measurable using conventional multi-meter.

Chapter 3

Compact Antenna Array Design

In Chapter 2, the design of voltage multiplier circuit has been described. Also, the relationship between input power level and conversion efficiency of the circuit has been discussed and demonstrated through both simulation and measurement results. The voltage multiplier circuit developed in Chapter 2 will be used for the performance evaluation of the receiving antenna.

This chapter focuses on the design of the proposed compact printed antenna array on package. It begins with the design of individual antenna array element and followed by the final structure of the antenna array. Then, the issue of inter-coupling between closely spaced antenna elements is discussed and a solution is proposed. Finally, the effectiveness of the proposed isolation structure is demonstrated experimentally.

3.1 3D Array On-Package Design

The design of the antenna array on-package starts with the design of individual element. First the design of the array element will be described in this section, where how the input impedance is affected by the different parameters of feeding loop will be investigated through simulation. After that, the design of array will be introduced. The simulated input impedance of each element will also be presented.

3.1.1. Array Element

The meander-line monopole as described in Section 1.3.2 is adopted as the antenna array element. As shown in Figure 3-1(a), the radiation body of monopole is folded in a 3D fashion on one side of the case and shorted to the folded ground that occupies the central part of the package. The antenna is fed by the feeding loop on PCB. The loop is placed in a way that the symmetrical axis of the loop aligns with the position where the monopole is shorted to the ground. In this thesis, the prototype is first fabricated by printing the antenna pattern with silver ink onto 0.1 mm thick PET sheet using screen printing technology. Then it is folded and fitted into a rectangular package and finally, attached to the PCB. The material of the composition of the prototype is presented in Figure 3-1(b).

Figure 3-1 Proposed 3D meander-line antenna on-package design. (a) 3D design overview (b) material used (c) Zoom-in on single monopole and feeding loop. All Dimensions are in mm.

Table 3-1 Comparison of antenna size and properties of different designs

Work	Operating frequency	Antenna size*	-10dB Bandwidth#	Radiation Efficiency#
[90]	1.7 GHz [^]	0.14 λ	3.9%	66%
[45]	930 MHz	0.13 λ	1.2%	78%
[91]	2.4 GHz	0.09 λ ⁺	2%	78%
Author's work	900 MHz	0.15 λ	4.1%	47%

*. Largest dimension of antenna in terms of wavelength at operating frequency

#. Simulation results are compared to eliminate the deviation introduced by testing fixture.

[^]. Design resonating at 1.7GHz chosen, -10 dB bandwidth extracted from Figure 2.

⁺. Dimension of the first cube used

For the antenna element in this design, as shown in Figure 3-1(c), the antenna size, including the folded ground in the centre, is 0.15 λ , where λ is the wavelength. Table 3-1 compares the size of the array element with the compact antenna-on-package designs from other literatures in terms of wavelength at the operating frequency and antenna performance. The reported designs in the literatures show limited bandwidth or low radiation efficiency for small antenna. Among all the designs, [90] was especially designed to maximize the space utilization so the performance of the antenna can approach Chu's limit. Comparing this work to the antennas presented in [45] and [91], this design has a lower radiation efficiency due to the loss of silver ink and inductive coupling but achieves a relative wider bandwidth.

The inductive coupling is selected as the feeding mechanism for two reasons; firstly, it eliminates direct electrical contact between the PCB and the case, which greatly simplifies the assembly process; secondly, the feeding loop also doubles up as part of the matching network to match the antenna with the input impedance of rectifier circuit, which can be tuned easily. The input impedance can be tuned by adjusting the distance d between the antenna and the feeding loop, as well as the dimension of the loop (a and b), as indicated in Figure 3-1(c) [86, 108].

3.1.2. Investigation on Input Impedance

The detailed structure of inductive coupling is shown in Figure 3-1 (c). The feeding loop is put in close proximity to the monopole antenna and the two terminals of the loop are directly connected to the excitation port. The inductive coupling can be modeled as a transformer as shown in Figure 3-2 [86, 109].

Figure 3-2 Circuit model for inductive coupling

At resonant frequency ω_0 of the monopole, the inductive reactance of the inductance (L_{Ant}) and capacitive reactance of the capacitance (C_{Ant}) of the antenna cancels each other. So the imaginary part of the input impedance is solely contributed by the inductive reactance of the feeding loop. The input impedance looking into the input terminal at frequency ω_0 can be expressed by the following equation [86]:

$$Z_{in} = j\omega_0 L_{loop} + \frac{(\omega_0 M)^2}{R_{Ant}} \quad (3-1)$$

Equation (3-1) shows that the imaginary term (reactive component) is determined by the size of the feeding loop while the real term (resistive component) is determined by the mutual inductance (M). The inductive coupling here is similar to the classic scenario that a loop being placed next to an infinitely long wire [108]. Therefore, the larger the loop and the closer the loop to the radiating arm, the stronger coupling between the loop and the monopole, hence higher M , which

results in higher resistive component according to equation (3-1). Figure 3-3 plots the input impedance at resonant frequency with varying a , b and d . The reactance curves in Figure 3-3(a) and Figure 3-3(b) clearly show that a larger loop size increases the input reactance. Also, the increase in a increases the input resistance due to the increase of mutual inductance. The behavior of input resistance is somewhat mixed as b increases, as shown in Figure 3-3(b), which may be attributed to the particular design of the folded monopole shorted to the folded ground on package, the distribution of magnetic field on the plane where the feeding loop is placed deviates from that of the classic scenario of loop placed close to infinitely long wire. To study the influence of d , the shape of the loop is maintained as a square (i.e. $a = b$). Figure 3-3 (c) shows that the input impedance with varying d and it is clearly observed that the input resistance increases with decreasing d due to the decrease in mutual inductance, while the input reactance remains almost unchanged.

(a) Input impedance vs. a for different value of b .

(b) Input impedance versus b for different value of a

(c) Input impedance versus d for different square loop size (the length of the edge of square loop indicated in bracket)

Figure 3-3 Input impedance versus changes of a , b and d . Input resistance is represented by solid line with scale on left side. Input reactance is represented by dashed line with scale on right side.

Based on the earlier results, the input impedance of the antenna can be tuned closer to the target impedance by adjusting a first and then by adjusting b and d to achieve the required input resistance and input reactance, respectively. As the focus of this chapter is on the design of a compact antenna array, the dimensions of a , b and d are conveniently specified, as listed in Table 3-2 and remain unchanged throughout the design process. The input impedance of the antenna can always be

fine-tuned to match the input impedance of rectifier circuit specified for a certain application.

Table 3-2 Dimensions of feeding loop chosen for fabrication.

Parameter	Dimension(mm)
a	10.5
b	10.5
d	0.5

3.1.3. Two-element Array

The two-element array is formed by mirroring the monopole and the feeding loop to the other side of the ground as shown in Figure 3-4. The length of the monopole is adjusted for resonance at 900 MHz. The complete antenna array on package only occupies a highly compact volume of $56 \text{ mm} \times 35 \text{ mm} \times 12 \text{ mm}$, which is $0.17 \lambda \times 0.1\lambda \times 0.04 \lambda$ at 900 MHz. The largest dimension of the package is about 0.2λ . Figure 3-5 and Figure 3-6 show the planar design of the antenna array and the PCB layout of the feeding loops, respectively. With such compactness, the edge-to-edge distance between the two array elements is merely 0.078λ (26 mm). A strong inter-coupling is expected and it will be confirmed by the simulation and measurement results in subsequent sections.

Figure 3-4 Antenna array on case

Figure 3-5 Planar design of antenna array on case

Figure 3-6 PCB layout of the feeding loop

Figure 3-7 shows the simulated input impedance of the reference antenna array with dimensions shown in Figure 3-5. The design of feeding loop follows the dimension shown in Table 3-2. Both the resistance and reactance shown in Figure 3-7 follow the characteristic of a typical antenna fed by a loop through inductive coupling, where the resistance peaks at the resonant frequency [108]. Because of the symmetry, impedance plots of element 1 (Z_{11}) and element 2 (Z_{22}) are identical.

Figure 3-7 Input impedance vs. frequency for reference antenna array design

3.2 Inter-Coupling Effect

The effect of inter-coupling between closely spaced antennas was reported for MIMO communication antennas [93, 95, 110]. An equivalent circuit has also been developed to model the inter-coupling between two dipole antennas to investigate its effect on radiation efficiency and diversity gain [93]. The investigation reveals that the degradation of radiation efficiency of array element is caused by closely spaced antenna elements, where part of the power that is supposed to be radiated, coupled into the adjacent elements and dissipated by the connected loads. Further literature review also indicates that the closely spaced elements have other impacts on the performance of signal communication, such as diversity gain and channel capacity. In this chapter, there is a need to look at this issue from RF power receiving perspective, i.e., to understand how the inter-coupling affects the capability of an antenna array in capturing incoming RF power.

3.2.1. Inter-Coupling Effect in Transmission

It is easier to understand the effects of inter-coupling issue and its impact on the array performance from transmission point of view. To facilitate the analysis, a two-dipole array is modelled with CST, a commercial full-wave EM solver, as illustrated in Figure 3-8. Two vertical dipoles are positioned in parallel with the feeding port on the same plane, where point “O” is the centre of the plane. A metal with conductivity of 1×10^6 S/m is chosen for the dipole antenna. The length of dipole is tuned such that it resonates at 900 MHz.

Figure 3-8 Schematic illustration of two closely-spaced dipoles

As shown in Figure 3-8, one of the dipoles is excited by a power source, denoted as “active element”, while the other is connected to the load, denoted as “passive element”. Matching circuits are inserted to match the impedance of each dipole to the source or load connected at the resonant frequency, respectively. With the source and load well matched, the amount of coupling can be presented in terms of the magnitude of S_{21} at the resonant frequency. Due to the symmetry of the array, only the simulation result of the active element will be presented. Figure 3-9 shows S_{21} and radiation efficiency of the array at 900 MHz with varying distance between the two dipoles. The efficiency η to be investigated here follows the definition of efficiency given in [95]:

$$\eta = \frac{\text{Power radiated by the array}}{\text{Power delivered to the active element}} \quad (3-2)$$

The distance between the two dipoles is expressed in fraction of wavelength. Figure 3-9 clearly shows that as the distance between the dipoles decreases, S_{21} increases and radiation efficiency reduces concurrently. The gain of the active element decreases due to the drop of radiation efficiency, as indicated in Figure 3-10. Figure 3-10 also shows that the maximum gain of the active element reduces with decreasing separation distance.

Figure 3-9 Level of inter-coupling between the two elements as presented by S_{21} and radiation efficiency of the array plotted against distance in wavelength.

Figure 3-10 Maximum gain of active element vs. distance between elements

The radiation pattern of the active element for different separation distance between the dipole elements can be obtained through simulation. The simulated results allow us to have a better picture on how the gain of active element is affected by the coupling. Figure 3-11(a) and Figure 3-11(b) show the simulated *E*-plane radiation pattern and *H*-plane radiation pattern in terms of gain, respectively. Similar to single dipole, following the coordinate system shown in Figure 3-8, the *E*-plane radiation coincides with the *x-y* plane while the null in the *H*-plane is along the *z* axis. It is observed that the radiation pattern of the active element roughly retains the “donut” shape of a typical dipole even it is affected by the existence of another dipole in proximity. Only the *E*-plane pattern appears to be slightly anisotropic.

Figure 3-11 Simulated radiation pattern (a) *E*-plane (*x-y* plane) (b) *H*-plane (*y-z* plane)

By taking a closer look at both radiation patterns in Figure 3-11, it is obvious that the *E*-plane radiation pattern shrinks with decreasing distance between the dipoles. For comparison purposes, the radiation pattern of a single dipole is also plotted in solid line as a reference. By comparing the radiation pattern of the active element to that of the single antenna, the active element becomes less efficient than a single dipole in terms of gain when the distance between two dipoles is less than 0.15λ . When the distance reduces to 0.03λ , the gain reduction can be more than 3 dB in some direction. The performance of the array is even worse than that of a single antenna in these directions.

3.2.2. Inter-Coupling Effect in Reception

Due to the influence of the inter-coupling, how the power is delivered to the load connected to the array element is more complicated than that of single antenna. The same antenna array as shown in Figure 3-8 is used to illustrate how power is delivered to the load in receiving mode. Take active element for example, when the RF power is received by the active antenna array element, part of the power is re-radiated, part of the power is dissipated in antenna, part of the power is coupled to the passive element nearby and the remaining power is delivered to the load. The power coupled to the passive element, is again partially re-radiated, partially dissipated in antenna, and the remaining delivered to the load connected. The same phenomenon also happens in passive element. For ease of analysis, assuming that the antenna array operates at resonant frequency and matched to the load, all the reactive components cancel out due to resonance. Also, It is assumed that only the active element is receiving power from incoming EM wave, and the passive element only receives power coupled from the active element. With the above assumptions, the equivalent circuit model at resonant frequency can be developed as shown in Figure 3-12 [95].

Figure 3-12 Circuit model of closely spaced array in receiving mode

In Figure 3-12, the circuit on the left represent the active element that is receiving the incoming RF power. V_c is the open-circuit voltage induced on active element

due to the incoming electromagnetic field. R_{rad} and r denote the radiation resistance and loss resistance of the antenna element, respectively. R_{Load} is the load connected to both the active element and passive element. The induced voltage in the active element causes a current I_1 flows in the active element. The coupling from the active element to the passive element is denoted as $Z_c I_1$, where Z_c is the mutual impedance between the active and the passive element [111].

The circuit on the right represents the passive element, whose design is identical and thus it has the same R_{rad} , and r . $Z_c I_2$ represents the coupling from the active element to the passive element.

Applying KVL in the active element circuit leads to:

$$V_c = Z_c I_2 + I_1 (R_{rad} + r + R_{Load}) \quad (3-3)$$

Similarly, applying KVL in the passive element circuit results in:

$$Z_c I_1 = I_2 (R_{rad} + r + R_{Load}) \quad (3-4)$$

Under conjugate matching at the active element, with the reactive parts already canceled, R_{Load} needs to satisfy the following requirement:

$$R_{Load} = R_{rad} + r + \frac{Z_c I_2}{I_1} \quad (3-5)$$

Let the power delivered to the load connected to the active element be P_{active} and that to the passive element be $P_{passive}$. In practical situation, the passive element also captures incoming RF wave and part of the power is delivered to the load connected to the active element due to inter-coupling, whose amount is also $P_{passive}$ due to symmetry. Therefore, the total power P_{Load} delivered to the load connected to the active element is the sum of P_{active} and $P_{passive}$:

$$P_{Load} = P_{active} + P_{passive} \quad (3-6)$$

From equations (3-3)-(3-5), P_{Load} can be determined as:

$$P_{Load} = \frac{1}{4} \frac{V_c^2}{\sqrt{(R_{rad}+r)^2 + Z_c^2} + R_{rad}+r} \quad (3-7)$$

Under the situation of no inter-coupling, i.e, $Z_c = 0$, equation (3-6) reduces to:

$$P_{Load} = \frac{1}{8} \frac{V_c^2}{R_{rad}+r} \quad (3-8)$$

Equation (3-8) is basically the power delivered to load of a well-matched single antenna, which is obviously larger than the (3-7) if V_c is the same. The above analysis shows that under the same field strength, the inter-coupling effect reduces the maximum possible power that can be received by the array elements.

To verify the conclusion drawn from (3-7), Simulation is performed on the antenna array with plane EM wave directing towards +y direction, as shown in Figure 3-8. The wave is linearly polarized with E-field along z-direction, and the power intensity is $3.3\mu\text{W}/\text{cm}^2$. The real power delivered to the load connected to the active element is recorded as distance between array elements is swept. The result is plotted in Figure 3-13. The dashed line on top shows the real power received by a single dipole under the same field. It is clear to tell that the power received by the active element is well below that of the single antenna due to the inter-coupling effect. This simulation result agrees well with the conclusion drawn from equation (3-7).

Figure 3-13 Real power received by active element vs. Distance between array elements.

As mentioned in the previous chapter, the conversion efficiency of the rectifier circuit degrades if its input power drops. If the array is used for receiving RF power from a transmitter, for the topology with each element connected with the rectifier circuit, the situation worsens as the efficiency of the rectifier degrades due to the reduction of the received input power from the antenna element.

The earlier analysis, through mathematical derivation and simulation, shows that to design a compact rectenna for RF power receiving, simply placing more antenna elements in a compact space does not necessarily help to receive more power. In fact, it can degrade the performance of the array and can make it less efficient than a single element. To ensure the array to perform as intended, either the distance between the elements needs to be carefully maintained to make sure the gain does not degrade or to have additional measures to reduce the coupling between closely-spaced radiating elements.

3.3 Calculation of Inter-Coupling Level

3.3.1. Motivation

Figure 3-14 2-port network model for 2-element array

Before moving on to discuss the design solution for inter-coupling reduction, there is a need to quantify the level of inter-coupling between the antenna array elements. In Section 3.2, the magnitude of S_{21} provides the level of inter-coupling between the two dipoles. The basic theory behind is that the antenna array can be modelled as a two-port network, as presented in Figure 3-14. Ports 1 and 2 correspond to elements 1 and 2 of the array, respectively. Both ports 1 and 2 are terminated with the respective loads 1 and 2. Γ_1 and Γ_2 are the reflection coefficients of at loads 1 and 2; and Γ_{in} and Γ_{out} are the reflection coefficients seen by ports 1 and 2 of the array.

For conventional antenna array, each element is designed to match $50\ \Omega$ at the operating frequency range. When measured or simulated with a $50\ \Omega$ termination, the magnitude of S_{21} (or S_{12}) within the operating frequency range provides the level of coupling directly between the two elements, as the reflection at the input port is low enough to be ignored. However, for antenna array design with the purpose of maximizing RF power received, the input impedance of the array element needs to be inductive in order to match the capacitive input impedance of the rectifier circuit.

When the array is measured or simulated with a 50 Ω termination, most of the power reflects back at the input port and the amount of coupling to the other element and consumed by its terminated load is too small. As a result, S_{21} (or S_{12}) obtained in such condition is too low, which does not truly reflect the actual coupling between the two elements when both ports are matched to their respective loads, the rectifier circuits.

For simulation, impedance matching can be relatively easy to achieve by changing the impedance of the load. However, it becomes cumbersome during the design and optimization process, where numerous design iterations are needed. In this chapter, a method has been developed to calculate the coupling level between the two antennas elements with both ports matched from the S-parameters obtained by 50 Ω port termination.

3.3.2. Method of Calculation

To calculate the level of inter-coupling with both ports matched, as shown in Figure 3-14, a power source is inserted next to load 1 so that power goes from load 1 into Port 1 and element 1 of the array is excited. Part of the power couples to element 2 and consumed by load 2. The level of coupling can be expressed by the ratio between power consumed by load 2 (P_2) and the power that goes into port 1 (P_{in}):

$$\frac{P_2}{P_{in}} = \frac{|S_{21}|^2(1-|\Gamma_2|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_2|^2} \quad (3-9)$$

$$\text{where} \quad \Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_2}{1-S_{22}\Gamma_2} \quad (3-10)$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_1}{1-S_{11}\Gamma_1} \quad (3-11)$$

Equation (3-9) gives a general expression to the level of coupling, whereas the level of coupling of interest is the level of coupling when both port 1 and port 2 are simultaneously matched, which, for the convenience of future discussion, is denoted as CPL. The condition of simultaneously matching can be expressed by equations below:

$$\Gamma_1 = \Gamma_{in}^* \quad (3-12)$$

$$\Gamma_2 = \Gamma_{out}^* \quad (3-13)$$

Now the problem becomes to obtain CPL from equation (3-9), when equation (3-12) and (3-13) holds. Since there are four equations ((3-10)-(3-13)) and four unknowns ($\Gamma_1, \Gamma_2, \Gamma_{in}$ and Γ_{out}). Γ_1 , and Γ_2 , can be readily solved in accordance with the procedure found in [112].

$$\Gamma_1 = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad \text{and} \quad \Gamma_2 = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (3-14)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (3-15)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (3-16)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (3-17)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (3-18)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (3-19)$$

Once Γ_1 and Γ_2 are found, Γ_{in} can be obtained through (3-10) and CPL can be obtained through equation (3-9).

To verify the proposed method, the antenna array on-package with dimension shown in Figure 3-5 is simulated under the following two cases:

- Case 1: both ports connected directly to 50 Ω . It is the conventional simulation scenario which produces very high S_{11}/S_{22} and low S_{21} .
- Case 2: both ports matched to 50 Ω through matching network at 900 MHz.

The matching network is an L network consists of two capacitors.

CPL is computed from the S-parameters obtained for Case 1 from 800 MHz to 1 GHz and plotted together with the magnitude of S_{21} for both cases in Figure 3-15. Comparing S_{21} for both cases, it can be clearly seen that S_{21} of Case 1 is much lower than S_{21} of Case 2. The comparison has demonstrated that when there is a strong reflection at the input port, how significant S_{12}/S_{21} deviate from the true level of coupling between two elements when the ports are matched. On the other hand, the calculated CPL agrees well with S_{21} for Case 2 at 900 MHz, where there is minimum reflection at both ports, as presented by minimum point of S_{11}/S_{22} curve. S_{21} of Case 2 gradually falls below CPL and finally joins with S_{21} curve of Case 1 as frequency moves away from 900 MHz, which is due to the increase of reflection at the input port.

Figure 3-15 Comparison between calculated CPL, S21 with two ports unmatched, S21 with both ports matched at 900MHz.

The advantage of using the proposed method to calculate CPL is that the calculating procedure can be integrated into the post data processing of the simulation software. So CPL can be calculated automatically from the obtained s-parameters after each simulation. It is very helpful when it comes to the exploration on solutions to reduce the coupling between the array elements later as iterations of parameter sweeps are needed. Also, it is more convenient during measurement as the level of inter-coupling can be predicted from the measured S-parameters from 50 Ω measurement instrument without going through the trouble of constructing the actual matching network.

3.4 Inter-Coupling Reduction between Array Elements

Using two elements antenna array as an example, Section 3.2 has illustrated the impact of inter-coupling on the power-receiving capability of the antenna array. The analysis shows that the array becomes less efficient than single element antenna the distance between two elements becomes too close. For the compact antenna array proposed in this thesis (Figure 3-4 to Figure 3-6), the distance between the elements is as close as 0.078λ . Figure 3-15 plotted the inter-coupling level indicated by CPL. The simulation result indicates a very strong inter-coupling with CPL of around -5 dB at 900MHz.

To reduce the amount of inter-coupling between two closely spaced antennas, there are various ways being proposed for MIMO communication, such as using a neutral line to cancel the induced current at the passive element [98, 99], adding slot to the ground plane to divert the ground current [113] and inserting an isolation structure between radiating elements [100, 101].

3.4.1. Coupling Cancellation by Isolation Element

The mechanism behind the isolation element in the reduction of inter-coupling can be explained by Figure 3-16. Figure 3-16(a) shows two antennas positioned very close to each other, where the antenna on the left is driven by a source and the one on the right is connected to a load. Following the terminologies defined in Section 3.2, the antenna on the left is denoted as “active element” and the antenna of the right is denoted as “passive element”.

Figure 3-16 Conceptual illustration of inter-coupling between the antenna elements without and with isolation structure. (a) Coupling from active element to passive element (b) Coupling from active element to the passive element with isolation element in between

As shown in Figure 3-16(a), the current flowing in the active element is denoted as the driving current I . When the two antennas are very close (usually less than 0.1λ), the current induced on the passive element is approximately 180° out of phase

with respect to the current on the active element [114]. The path that the power is coupled from active element directly to the passive element to induce the current with this reverse direction current is marked as Path 1. The current induced due to coupling through Path 1 is denoted as $I_{path1} = \alpha I$, where α is the coupling coefficient between two elements through Path 1.

With an extra element called isolation element inserted at the middle of the two elements, as shown in Figure 3-16(b), a current is induced on the isolation element with 180° phase different with respect to the driving current. The magnitude of this current is βI , where β is the coupling coefficient between the active element and the isolation element. Similarly, the current in the isolation element induces another current on the passive element, with the same coupling coefficient β because of symmetry. Therefore, on the passive element, the magnitude of the current induced by current on the isolation element is $\beta^2 I$ and the phase of the current is 180° with respect to the phase of the driving current. Let the path that the coupled from the active element through isolation element to the passive element be Path 2 and the current induced on the passive element due to coupling from this path be I_{path2} .

Based on the above reasoning, I_{path2} and I_{path1} are in out of phase and in phase with respect to the driving current, respectively. It means I_{path2} and I_{path1} is out of phase. Therefore, the current flowing on the passive element can be expressed by:

$$I_{passive\ element} = I_{path1} - I_{path2} = \alpha I - \beta^2 I \quad (3-20)$$

If the isolation element is properly designed where $\alpha = \beta^2$ so that I_{path1} and I_{path2} cancel each other, the current flowing on the passive element is nearly zero and no power will be dissipated by the connected load. Hence, with the insertion of

isolation element, the coupling between the active and passive element becomes nearly negligible.

3.4.2. Design of Isolation Element

For the compact antenna array proposed in this thesis, the isolation element is inserted between the two array elements at the other end of the ground plane and is bent down occupying the front side of the package, as shown in Figure 3-17(a). The isolation element is a symmetrical meander line monopole that shares the ground with the array element. Planar design of the proposed array is shown in Figure 3-17(b). The insertion of the isolation element shifts the resonant frequency of the radiating elements, thus the length of monopole has to be adjusted to make the array element restores the resonant frequency at 900 MHz.

Figure 3-17 Proposed antenna array with isolation element inserted. (a) Proposed design on PCB with isolation element component (b) Planar design of the proposed array with isolation element, all dimensions in mm.

Figure 3-18 CPL calculated from simulation result for both reference design and the proposed design.

Figure 3-18 shows the comparison of CPL computed from the simulation results of both the reference array design on package shown in Figure 3-4 and the proposed design with an isolation element shown in Figure 3-17. It clearly shows that the insertion of the isolation element has reduced CPL below -10 dB across the whole frequency range from 800 MHz to 1 GHz. The dip of CPL of the proposed design shows that it is minimized at the resonant frequency. Parametric studies on different dimensions of the isolation element show that the frequency where the dip occurs as well as the magnitude of the minimum level is mainly determined by the total arm length of the isolation element. The height of the parasitic component, the space between the folded meander line section and the overall width of isolation element all can be adjusted to tune the performance of the isolation element. Some are very sensitive that very little change in the value causes huge frequency shift of the “dip”, while for others this is not the case.

Thus it is necessary to identify parameters that are most efficient to be adjusted to optimize the performance of the isolation element. After a series of investigations, it is found out that the length of L_{iso} and L_{end} are the most effective parameters.

To further study how the values of the two parameters affect the isolation performance, the two parameters are swept and the CPL is computed from the simulation results. The computed CPL results are plotted in Figure 3-19.

Figure 3-19 Coupling (CPL) with the variation of L_{iso} and L_{end} . All dimensions are in mm.

The plots show that the frequency where minimum CPL occurs is more sensitive to the change of L_{iso} than that of L_{end} . With the similar change in dimension, 1 mm for example, the minimum CPL shifts more significantly as compared to the change of L_{iso} . It is easy to understand by intuition as the change of L_{iso} varies the overall width of the whole isolation component, while L_{end} only affects the length of the end section. The minimum CPL shifts towards lower frequency as the value of L_{iso} or L_{end} increases and shifts towards higher frequency when the value of L_{iso} or L_{end} decreases. The magnitude of minimum CPL decreases when the “dip” is close to the resonant frequency of the array element.

With the above investigations, the dimension of isolation component is adjusted by tuning L_{iso} and L_{end} to move the minimum CPL to the resonant frequency of the array by the following steps:

- Firstly, L_{iso} is tuned to move the minimum CPL around the resonating frequency;
- Then, L_{end} is adjusted to fine tune the curve so that minimum CPL coincides with the resonant frequency of the antenna array; and
- After a series of optimizations, the value of L_{iso} and L_{end} are finalized with the dimensions given in Table 3-3.

Table 3-3 Finalized dimensions of the variable for the proposed design

Name	Dimension (mm)
L_{iso}	20.4
L_{end}	6

3.5 Impact of Isolation Element

As mentioned in section 3.4.1, the isolation was achieved due to the cancellation of induced current on the passive element that is coupled through different paths. This section verifies the theory by investigating the simulated surface current distribution of the proposed design and the reference design. The 3D radiation pattern is also investigated to see how the insertion of isolation element affects the radiation pattern of the antenna array.

3.5.1. Surface Current Distribution

To investigate how the isolation element reduces the coupling between the two elements, the normalized surface current for both the proposed design and the referenced design are simulated and presented in Figure 3-20. Only the surface current on the antenna array is presented for ease of comparison and the surface

current on the feeding loop is not presented. The magnitude of the surface current is normalized to the maximum current flowing on the active element.

Figure 3-20 Normalized surface current for the proposed design and reference design. The port feeding the active element is excited. (a)reference design (b) proposed design (c)Current flow on isolation element

Figure 3-20(a) shows the surface current distribution of the reference design. It is noted that due to the inter-coupling, there is induced current on passive element which is of the same magnitude as the surface current on the active element. As for the proposed design with the isolation element, as shown in Figure 3-20(b) and (c), significant surface current is induced on the isolation element while the surface current on the passive element is greatly reduced. Comparing to the magnitude of surface current on the active element, the reduction is about 30 dB. By looking at

the surface current distribution, it demonstrates how the surface current on the passive element is suppressed due to the cancellation of induced current, as explained earlier.

3.5.2. Radiation Pattern

This section investigates the radiation pattern of the antenna array through simulation. Firstly, the 3D coordinate system for the radiation pattern is presented in Figure 3-22(a). The antenna array is placed at the origin of the coordinate system with monopole 1 and port 1 on the negative- x axis while monopole 2 and port 2 on the positive- x axis.

Figure 3-21 3D coordinate system and 3D radiation pattern of reference array design

Due to the symmetry, the radiation patterns of both array elements of reference design are identical. Thus only the radiation pattern of monopole 1 is presented in Figure 3-22(b). It can be seen that the radiation pattern retains the “donut” shape of a typical monopole with its null align with x -axis. Figure 3-22 shows the 3D normalized radiation pattern of array elements of the proposed design. Due to the current flow on the isolation component, the “donut” shape tilts towards the radiating element. As shown in Figure 3-22(a), the “ring” of maximum radiation

tilts toward the negative x -axis when monopole 1 is active and towards the positive x -axis when monopole 2 is radiating.

Figure 3-22 3D Radiation pattern of proposed design (a) radiation pattern of monopole 1 (b) radiation pattern of monopole 2

3.6 Fabrication of Prototype

The prototype is fabricated by first printing silver ink onto 0.1 mm PET sheet using screen printing technology, as shown in Figure 3-20(a) and (b). The screen printing technology has the advantage of being able to be fabricated for large-scale reel-to-reel, which will eventually make the fabrication cost of each antenna array very low. This technology has already been explored by author's research team to fabricate flexible Frequency Selective Surface (FSS) on PET sheet [115, 116]. Therefore, in this work, this technology was also explored to fabricate the prototype.

Then the printed sheet is folded into a rectangular shape and then integrated with the PCB that houses the feeding loop, as shown in Figure 3-20(c) and (d). The fabricated prototype will be characterized and evaluated for its performance in reception of RF power, which will be covered in Chapter 4.

Figure 3-23 Fabricated prototypes. (a) Unfolded reference antenna array by printing silver ink on PET sheet (b) Unfolded proposed array printed (c) Folded reference array assembled on PCB (d) Proposed array assembled on PCB.

Chapter 4

Experimental Results and Analysis

Based on the design in Chapter 3, a prototype is designed and fabricated. This chapter presents and discusses the measurement results, covering the characterization of two-port S-parameter network, radiation pattern, radiation efficiency. The prototype is integrated with the voltage multiplier developed and the performance of the rectenna array will be evaluated.

Unlike conventional antenna designed with singled-ended feeding port that can be directly connected with a $50\ \Omega$ connector, performing accurate measurement on small antenna with balanced feeding have been shown to be no easy task [117, 118]. Differential probes need to be developed to perform the measurement. In this thesis, to perform measurement on two differential ports of the two array element concurrently and to obtain two-port S-parameter matrix can be even more complicated, as elaborated in this chapter. Section 4.1 is dedicated to the measurement of two-port S-parameter matrix of the prototype with details of the theory behind and the measurement setup.

The measurements on radiation pattern and the radiation efficiency as well as the performance of antenna array integrated with voltage multiplier are all performed in a anechoic chamber. Section 4.2 covers the measurement on radiation pattern and radiation efficiency. Finally, Section 4.3 evaluates the performance of the rectenna.

4.1 Measurement of Input impedance

4.1.1. Measurement Setup

The feeding loop is a balanced structure and therefore conventional single-ended probe or connector cannot be used for the measurement of the input impedance of the antenna. In this thesis, the measurement method described in [117] is adopted. Two differential probes are designed and fabricated by cutting equal length of coaxial cables and soldering the outer conductor together. The two differential probes are attached to the feeding port of each feeding loop. Figure 4-1 shows the photograph of the prototype with the two differential probes attached. In order to shift the measurement plane from the SMA connector to the tip of the probe, the delay in the probe has to be accounted for and compensated. The delay time is obtained by dividing the length of the probe (L) to the guided TEM wave velocity (v_g) within the cable, which is given by:

$$Delay(s) = \frac{L}{c} \sqrt{\epsilon_r} \quad (4-1)$$

where c is the speed of light in vacuum.

Figure 4-1 Antenna array on case with differential probes attached.

All the measurement results are collected using R & S ZVB8 vector network analyser (VNA). The VNA has four ports that allow concurrent measurement of two differential ports. The delay of the probe is pre-set in the VNA and is compensated automatically during the measurement.

Figure 4-2 Setup for Input impedance measurement using VNA

The measurement setup is illustrated in Figure 4-2. The differential port 1 is connected to ports 1 and 3 of the VNA, while differential port 2 is connected to ports 2 and 4 of the VNA. The antenna array is surrounded by absorbers to minimize possible reflections from other objects in the environment.

The data acquired is a 4×4 single-ended S-parameter matrix. The equations for the calculation of the input impedance from the two-port S-parameter matrix obtained by a single differential probe are given in [117]. In order to calculate the input impedance of both ports and the CPL between the two ports, the four-port single-ended S-parameter matrix needs to be converted into two-port differential S-parameter matrix. To the best of the author's knowledge, the equations that perform such a conversion are not reported in the literature. Hence, for the benefit of the

readers, the conversion developed by the author will be elaborated in following sections.

4.1.2. Mixed-mode S Parameters

When measuring the antenna-under-test (AUT) using differential probe, other than the conventional single-ended S-parameter, mix-mode S-parameter can also be used to characterize the AUT from the perspective of common-mode (CM) response, differential-mode (DM) response and the conversion between the two modes. From the mixed-mode point of view, a single-port network is modeled as a two-port network with one port for DM and the other for CM [119]. The characteristic of the single-port network is presented by mixed-mode s-parameter matrix, as shown in Figure 4-3.

Figure 4-3 Mixed mode presentation for single-port antenna

In Figure 4-3, Z_{Ld} and Z_{Lc} are the DM and CM load impedances, respectively. Z_d and Z_c are the DM and CM input impedance of the AUT, respectively. If the characteristic impedance of the single-ended port is Z_0 , then the characteristic impedance is $2Z_0$ for DM and $Z_0/2$ for CM. The respective mixed-mode s-parameter can be calculated from the single-ended s-parameter with the following equations:

$$S_{dd} = \frac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22}) \quad (4-2)$$

$$S_{dc} = \frac{1}{2}(S_{11} - S_{21} + S_{12} - S_{22}) \quad (4-3)$$

$$S_{cd} = \frac{1}{2}(S_{11} + S_{21} - S_{12} - S_{22}) \quad (4-4)$$

$$S_{cc} = \frac{1}{2}(S_{11} + S_{21} + S_{12} + S_{22}) \quad (4-5)$$

For the antenna described in this thesis, the two terminals of the feeding loop are connected to the two terminals of the voltage multiplier input (RF in and ground). There is no common ground for the two terminals at the input of the voltage multiplier. Thus for this scenario, the input impedance of AUT is the differential mode input impedance Z_d when $Z_{Ld} = 2Z_0$, and Z_{Lc} is an open circuit. Z_d can be obtained by the following equation:

$$Z_d = 2Z_0 \frac{1+S_{dd}-S_{cc}-(S_{dd}S_{cc}-S_{dc}S_{cd})}{(1-S_{dd}-S_{cd})(1-S_{cc}+S_{cd})} \quad (4-6)$$

Converting the mixed-mode s-parameters in equation (4-6) into single-ended s-parameters using equations (4-2) to (4-5) results in the following equation for the input impedance with single-ended s-parameters:

$$Z_d = 2Z_0 \frac{1-S_{11}S_{22}+S_{12}S_{21}-S_{12}-S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \quad (4-7)$$

which is identical to the equation proposed in [117]. This implies that equation (4-6) is nothing but a mathematical counterpart to (4-7) in mixed-mode S-parameter domain. Hence it validates the analysis presented in this section using mixed mode S-parameters with common-mode termination open-circuit. The same condition will be used in the analysis in the two-differential-probe scenario which is presented in the next section.

4.1.3. 4-Port Single-end S-matrix to 2-Port Differential S-matrix Conversion

An AUT with single-port can be modelled by a two-port network with one port for DM and the other port for CM. Following the same idea, the antenna array with two ports can be modelled by a four-port network with two ports for DM and the other two ports for CM, as presented in Figure 4-4.

Figure 4-4 4-port presentation of a 2 differential port network

In Figure 4-4, Z_{Ld1} and Z_{Ld2} represent the DM load of ports 1 and 2, while Z_{Lc1} and Z_{Lc2} represent the CM load of ports 1 and 2, respectively. Z_{c1} and Z_{c2} , and Z_{d1} and Z_{d2} denote the CM and DM input impedances of port 1 and port 2, respectively.

Table 4-1 Table of single-ended S-parameter to mixed-mode S-parameter conversion

S_{dd11} $= \frac{1}{2}(S_{11} - S_{31} - S_{13} + S_{33})$	S_{dd12} $= \frac{1}{2}(S_{12} - S_{32} - S_{14} + S_{34})$	S_{dc11} $= \frac{1}{2}(S_{11} - S_{31} + S_{13} - S_{33})$	S_{dc12} $= \frac{1}{2}(S_{12} - S_{32} + S_{14} - S_{34})$
S_{dd21} $= \frac{1}{2}(S_{21} - S_{41} - S_{23} + S_{43})$	S_{dd22} $= \frac{1}{2}(S_{22} - S_{42} - S_{24} + S_{44})$	S_{dc21} $= \frac{1}{2}(S_{21} - S_{41} + S_{23} - S_{43})$	S_{dc22} $= \frac{1}{2}(S_{22} - S_{42} + S_{24} - S_{44})$
S_{cd11} $= \frac{1}{2}(S_{11} + S_{31} - S_{13} - S_{33})$	S_{cd12} $= \frac{1}{2}(S_{12} + S_{32} - S_{14} - S_{34})$	S_{cc11} $= \frac{1}{2}(S_{11} + S_{31} + S_{13} + S_{33})$	S_{cc12} $= \frac{1}{2}(S_{12} + S_{32} + S_{14} + S_{34})$
S_{cd21} $= \frac{1}{2}(S_{21} + S_{41} - S_{23} - S_{43})$	S_{cd22} $= \frac{1}{2}(S_{22} + S_{42} - S_{24} - S_{44})$	S_{cc21} $= \frac{1}{2}(S_{21} + S_{41} + S_{23} + S_{43})$	S_{cc22} $= \frac{1}{2}(S_{22} + S_{42} + S_{24} + S_{44})$

The four-port mixed-mode s-parameters can be converted from the four-port single-end s-parameters using the conversion equations shown in Table 4-1. The port arrangement followed the port arrangement of the measurement setup shown in Figure 4-2, where port 1 and port 3 are grouped into differential port 1, while port 2 and port 4 are grouped into differential port 2.

The scenario of analysis is the same with one-port analysis, where only the DM is measured with CM open circuited. Under this condition, $Z_{Ld1} = Z_{Ld2} = 2Z_0$, while Z_{Lc1} and Z_{Lc2} are open circuited. As shown in Figure 4-4, let the reflection coefficient of DM load for port 1 and port 2 be Γ_{d1} and Γ_{d2} , respectively. Similarly, let the reflection coefficient of CM load for port 1 and port 2 be Γ_{c1} and Γ_{c2} . Under the above-mentioned scenario, the load reflection coefficients are:

$$\Gamma_{d1} = \Gamma_{d2} = 0 \quad (4-8)$$

$$\Gamma_{c1} = \Gamma_{c2} = 1 \quad (4-9)$$

With the two ports open-circuited, the four-port network can be reduced to a two-port network with two DM ports, as shown in Figure 4-5. So now the problem is how to calculate the s-parameters for the converted two-port network from the s-

parameters of the original four-port network under the port conditions described by equations (4-8) and (4-9).

Figure 4-5 Converted 2 port S-matrix with differential mode load only

There are equations to calculate the new S-parameter matrix from the original S-parameter matrix when the load impedance connected to the ports of network changed from one value to another [120]. The original equations are lengthy and complicated because they were formulated for general cases. For the work presented in this thesis, the two ports are open-circuited and only four parameters are needed instead of sixteen. Thus for the new S-parameters in the matrix, as shown in Figure 4-5, can be determined with the following equations:

$$S_{d11} = \frac{1}{D} (S_{dd11} - S_{dd11}S_{cc11} + S_{dc11}S_{cd11} - S_{dd11}S_{cc22} + S_{dc12}S_{cd21} + C_{22}) \quad (4-10)$$

$$S_{d12} = \frac{1}{D} (S_{dd12} + S_{dc11}S_{cd12} - S_{dd12}S_{cc11} + S_{dc12}S_{cd22} - S_{dd12}S_{cc22} - C_{21}) \quad (4-11)$$

$$S_{d21} = \frac{1}{D} (S_{dd21} + S_{dc11}S_{cd12} - S_{dd12}S_{cc11} + S_{dc22}S_{cd21} - S_{dd21}S_{cc22} - C_{12}) \quad (4-12)$$

$$S_{d22} = \frac{1}{D} (S_{dd22} - S_{dd22}S_{cc11} + S_{dc21}S_{cd12} - S_{dd22}S_{cc22} + S_{dc22}S_{cd22} + C_{11}) \quad (4-13)$$

Where

$$D = 1 - S_{cc11} - S_{cc22} + S_{cc11}S_{cc22} - S_{cc12}S_{cc21} \quad (4-14)$$

$$\begin{aligned} C_{11} = & S_{dd22}(S_{cc11}S_{cc22} - S_{cc12}S_{cc21}) + S_{dc21}(S_{cc12}S_{cd22} - S_{cd12}S_{cc22}) \\ & + S_{dc22}(S_{cd12}S_{cc21} - S_{cc11}S_{cd22}) \end{aligned}$$

(4-15)

$$C_{12} = S_{dd21}(S_{cc12}S_{cc21} - S_{cc11}S_{cc22}) + S_{dc21}(S_{cd11}S_{cc22} - S_{cc12}S_{cd21}) \\ + S_{dc22}(S_{cc11}S_{cd21} - S_{cd11}S_{cc21})$$

(4-16)

$$C_{21} = S_{dd21}(S_{cc12}S_{cc21} - S_{cc11}S_{cc22}) + S_{dc21}(S_{cd11}S_{cc22} - S_{cc12}S_{cd21}) \\ + S_{dc22}(S_{cc11}S_{cd21} - S_{cd11}S_{cc21})$$

(4-17)

$$C_{22} = S_{cd11}(S_{dc12}S_{cc21} - S_{dc11}S_{cc22}) + S_{cc11}(S_{dd11}S_{cc22} - S_{dc12}S_{cd21}) \\ + S_{cc12}(S_{dc11}S_{cd21} - S_{dd11}S_{cc21})$$

(4-18)

With the single-ended to mixed mode conversion equations given in Table 4-1 and equations (4-10) to (4-18), the two-port S-parameter matrix can be obtained from the 4×4 single-ended S-parameter matrix obtained from the measurement. Then the input impedance and CPL can be computed once the S-parameter matrix is obtained.

4.1.4. Measurement Results

Figure 4-6 Simulation and measurement result of input impedance (a) reference design (b) proposed design

Figure 4-6 shows the measured and simulated input impedances of each port for both the reference and the proposed designs. In general, the measurement results agree well with the simulation results. The slight discrepancy between the measurement and simulation results is expected, as the fabrication and assembly of the antenna array onto PCB can never be perfectly symmetrical.

Figure 4-7 shows the plots of calculated CPL based on measurement results for both the proposed and reference designs. The two curves show similar characteristics as predicted by the simulation results in Figure 3-18. For the reference design, CPL increases with frequency and peaks at -6 dB. On the other hand, CPL is below -12 dB for the proposed design throughout the frequency range of interest. At 903 MHz, CPL of the proposed design achieves a minimum value of -27 dB, which is 17 dB lower than that of the reference design at the same frequency.

Figure 4-7 Comparison of calculated coupling between the proposed design and reference design

4.2 Radiation Pattern and Radiation Efficiency

4.2.1. Measurement Setup

The radiation pattern measurement of the prototype is performed in an anechoic chamber. Differential matching networks and baluns are designed and implemented on the PCB so that the antenna array is matched with the 50Ω measurement system,

as shown in Figure 4-8. The differential matching network consists of three capacitors; two capacitors on the differential trace with identical value C_1 and one capacitor bridging across the differential line with value C_2 . The differential matching network matches the input impedance of antenna array to the impedance of the differential port of balun, which is $100\ \Omega$, and the single-end port of the balun is matched to the $50\ \Omega$ measurement system.

Figure 4-8 Antenna radiation measurement setup with balun and differential matching networks.

The values of capacitors used in the differential matching network are listed in Table 4-2 for both reference and proposed design. Due to the in-symmetry of the fabricated prototype, the values of C_1 and C_2 for port 1 and port 2 are slightly different.

Table 4-2 Values of capacitors for the differential matching network

Design and Port		C1 (pF)	C2 (pF)
Reference Design	Port 1	4.3	1.7
	Port 2	4.3	1.8
Proposed Design	Port 1	2.4	1.8
	Port 2	2.7	1.8

The measurement setup in the anechoic chamber is illustrated in Figure 4-9(a). Figure 4-9(b) shows the details on how the AUT is mounted on the positioner. Due to the constraint of the setup in the chamber, only one measurement port is available at the positioner. Thus during the measurement, the port to be measured is

connected to the measurement instrument while the other port is terminated with 50 Ω load.

Figure 4-9 Measurement setup in anechoic chamber.(a)Simple schematic illustration of measurement setup in anechoic chamber, drawing not to scale. (b) Photo of AUT fixed on positioner

4.2.2. Measurement Result and Analysis

Figure 4-10 presents the normalized radiation pattern measured at 900 MHz for the proposed and reference designs. In general, the measured radiation patterns agree well with the simulation results. For the reference design, the H plane

radiation coincides with the y - z plane. For the proposed design, the H plane tilts towards the active element for around 45° . For power receiving purpose, other than normalized radiation pattern, it is more meaningful to look at the radiation pattern in terms of gain. The radiation patterns in terms of gain of both designs are plotted and compared in Figure 4-11. It is clearly observed that the antenna gain of the proposed design is larger than that of reference design in both E and H planes, an indication of higher overall gain for the proposed design.

Figure 4-10 Normalized radiation pattern of proposed design and reference design.

Figure 4-11 E plane (left) and H plane (right) radiation pattern in terms of gain of proposed design and reference design at 900MHz.

The observation is also supported by the radiation efficiency plot shown in Figure 4-12. The radiation efficiency is obtained by pattern integration. Figure 4-12 compares the radiation efficiency of each element between the proposed and reference designs. The loss due to reflection, balun and matching network are characterized and compensated. The plots show that the reference design is rather inefficient due to significant inter-coupling between elements. On the other hand, with the isolation structure inserted, significant improvement in radiation efficiency is observed. At 900 MHz, the radiation efficiencies of ports 1 and 2 are 48% and 50%, respectively.

Figure 4-12 Radiation efficiency vs. frequency.

Figure 4-13 shows the plot of maximum gain for each element of the proposed and reference designs. Comparing with the plots in Figure 4-12, the maximum gain curves follow the same trend as the radiation efficiency. The maximum gain of each element of the proposed design is at least 1 dB higher than that of the reference design throughout the frequency range of interest. At 900 MHz, the difference can be as large as around 3 dB, which corresponds to double the radiation efficiency at this frequency, as shown in Figure 4-12. Maximum gains of 0.4 dBi and 0.3 dBi are achieved for ports 1 and port 2, respectively, for the proposed design.

Figure 4-13 Plots of maximum gain vs. frequency. Proposed design is compared with the reference design. The passive ports are matched.

4.3 Performance of Rectenna Array

4.3.1. Measurement Setup

To investigate the antenna array's power receiving capability as a whole, the antenna array is integrated with the voltage multiplier developed earlier with a load connected at the output. The measurement is also performed in the anechoic chamber. The measurement was performed with two types of transmitting antennas,

linearly polarized and circularly polarized. As mentioned in Chapter 3, the array was designed in a way that each element to be connected to the rectifier circuit and the DC output would be combined. As elaborated in Chapter 2, the voltage multiplier used was a two-stage modified Dickson charge pump. As the purpose of the measurement is to investigate the impact of antenna array design on the power received, the voltage multiplier circuit with the matching network is directly connected to the balun that is attached to the antenna array, as presented in Figure 4-14. For measurement using log-periodic antenna, 500 k Ω resistor was connected to the DC output of the rectifier to so that high enough DC voltage can be detected during the measurement. Then for the measurement using circularly polarized antenna, the measurement was carried out for both 500kOhm and 30 k Ω load resistor. For both transmitting antennas, both the scenarios of serial and parallel combinations of DC output were evaluated. With each load, the matching network is tuned to match the input impedance of rectifier circuit to 50 Ω at 900MHz with an input power level of – 10 dBm.

Figure 4-14 Antenna array connected to rectifier circuits and resistor. (a) Serial connection (b) Parallel connection

Figure 4-15 Measurement setup for array-rectifier circuit integrated system in anechoic chamber.

Figure 4-15 shows the measurement setup. The AUT is fixed on the positioner and signal generator is employed as a signal source to provide continuous power into the transmitting antenna. Both linear polarized antenna and circularly polarized antenna are used as the transmitting antenna to send power to the AUT. The DC output voltage of the rectenna is measured.

(a)

(b)

Figure 4-16 Photo of the measurement setup. (a) Transmitter and AUT. (b) RF signal generator and NI instrument to record the DC voltage.

Figure 4-16 shows the details of the measurement setup. The distance between the transmitter and the array is 1.5 m. The linear polarized antenna used is EMCO 3146 log-periodic antenna, with a bore sight gain of 4.9 dBi at 900 MHz. The circularly polarized antenna used is Times-7 A6031 circularly polarized antenna, as shown in Figure 4-16(a), which has a bore sight gain of 4 dBi at 900 MHz and the axial ratio at bore sight is less than 2 dB [121]. The RF signal source used is Agilent N5182B MXG vector signal generator. The signal frequency is adjusted to 900 MHz with the output power set at 23 dBm for log-periodic antenna and 26 dBm for circularly polarized antenna. NI PXI-5922 digitizer card is chosen to measure the DC voltage at the rectifier output for its high accuracy and high sampling rate. Labview program is also developed for data acquisition and result display purposes.

4.3.2. Measurement Result

The array is rotated along three axial planes and the output DC voltage across the load resistor is measured. Then, the DC power is computed for both types of transmitters.

Log-periodic Antenna

Figure 4-17 Measured DC power when log-periodic antenna is transmitter.

When linearly polarized log-periodic antenna is used as a transmitter, measurements are performed for transmission of both vertical and horizontal polarizations. The results for log-periodic antenna are presented in Figure 4-17. The performance of the proposed design is superior in both vertical and horizontal polarizations in the x - y and x - z planes, respectively. The performance of the two

designs in y - z plane is somewhat close, which is expected as the plane of maximum radiation of the reference design just falls onto this plane.

To provide a clearer picture for ease of comparison of both designs, the ratio between the DC power generated by the proposed design and the DC power generated by the reference design is computed by subtracting P_{DC} of the reference design (dBm) from P_{DC} of the proposed design (dBm), as given in (4-19):

$$DC \text{ power ratio (dB)} = P_{DC \text{ proposed}}(dBm) - P_{DC \text{ referece}}(dBm) \quad (4-19)$$

The power ratio results are presented in dB and plotted as shown in Figure 4-18.

Figure 4-18 Ratio of DC power between the proposed design and reference design for log-periodic antenna.

The comparison further confirms the earlier observation. The result for the linearly polarized log-periodic antenna implies that the superiority of the proposed design is not a clear-cut conclusion for all measurement cases. For example, the

performance of the proposed design is not as good as the reference design for parallel connection in x - z plane when the transmitter is in horizontal polarization, and similarly, in x - y plane when the transmitter is in vertical polarization. Other than these two cases, the proposed design outperforms the reference design for the rest of the cases.

Circularly Polarized Antenna

For circularly polarized transmitting antenna A6031, measurements are performed for both cases where 500kOhm and 30kOhm are connected as DC load. Figure 4-19 presents the measurement result from 500k Ohm case and 30k Ohm, respectively. A similar plot of comparison by taking the ratio between DC power of the proposed design over the DC power of the reference design is presented in Figure 4-21. Comparing to the results obtained from linearly polarized transmitting antenna (Figure 4-17 and Figure 4-18), it is clearer to see that the proposed design generated more DC power than the reference design in majority of the directions investigated.

In conclusion, through the comparison of the measurement results for different transmitters as well as different polarizations, the proposed design exhibits better performance as compared to the reference design. Especially the superiority of proposed design is clearly demonstrated for circularly polarized transmitter, which will be the transmitter being used in actual case as the orientation of the receiving antenna is not known. Hence through the measurement result, the proposed decoupled antenna array is capable of receiving more power while maintaining compact package size.

Figure 4-19 Measured DC power with 500 k Ω load. Curves on the left side shows the result for parallel connection and curves on the right side shows the series connection.

Figure 4-20 Measured DC power with 30 k Ω resistor connected as DC load. Curves on the left side shows the result for parallel connection and curves on the right side shows the series connection.

Figure 4-21 DC power ratio between the proposed design and reference design for A6031 polarized antenna.

Chapter 5

Conclusions and Future Work

5.1 Conclusion

This thesis has proposed and described the design of a compact rectenna array on package for RF energy harvesting purposes.

Chapter 1 reviewed the historical development of wireless power transfer (WPT) and its envisioned application scenario, from high power to low power WPT. It followed by more detailed discussion on wirelessly powered devices that operated at low radio frequency (RF) power density environment, which had been gaining wide research interest because of their potential to be deployed as sensor node for long-term sensing applications, from embedded sensor for intelligent space and infrastructure monitoring, to medical implant device for health monitoring. The literature review had clearly shown the trend for the need of highly compact and light-weight devices with good RF energy harvesting capability.

Following the literature review, this chapter looked into the design of the device, especially the design of power supply module of the device, in which the rectenna plays an indispensable role to the performance of the whole module. The constraints and challenges of rectenna design, particularly the power reception and conversion efficiency aspects were discussed in greater depth. It was found that the power reception capability was limited by the single miniaturized receiving antenna at the costs of efficiency and bandwidth.

Hence, the motivation of the thesis is to design, develop and implement a feasible solution of rectenna array to enhance power receiving capability for RF energy harvesting and yet maintained highly compact.

In Chapter 2, the design of the “rectifier” of the “rectenna” was introduced. It covered the development of the rectifier circuit to be integrated with the receiving antenna to evaluate the performance of the rectenna array. The operating principle of Modified Dickson charge pump, which was chosen as the voltage multiplier circuit adopted in this thesis, was elaborated in details. Design considerations were elaborated, including the choice of diodes and the determination of number of stages. The impacts of input power and output DC load on input impedance and conversion efficiency were also discussed. Finally, a prototype was designed and developed with its performance evaluated experimentally.

With the development of rectifier circuit mentioned in Chapter 2, Chapter 3 presented the design of the proposed compact antenna array on package. The designs of individual antenna array element and antenna array were described. The inter-coupling effect between closely spaced antenna elements and its impact on the radiation property of array element was elaborated and then the proposed solution was proposed. The design methodology of an isolation element to improve the antenna array performance was introduced and elaborated. The reason for better antenna performance of the proposed design was investigated and analysed through comprehensive simulation.

With the design aspects well covered in Chapter 3, Chapter 4 focused on the measurement of the fabricated prototype. Unlike conventional antenna with single-end $50\ \Omega$ port, accurate S-parameter measurement of small antenna with balanced

feeding was not as straight forward. Therefore, the theory behind characterization of the prototype was covered first and followed by the discussions of measurement results.

The measurements of the radiation properties of the prototypes were performed in an anechoic chamber. Both the gain and radiation efficiency were measured and the results showed the proposed design achieved significantly higher radiation efficiency and hence, higher gain. Finally, the antenna array was integrated with the developed rectifier circuits and the performance of the rectenna array was evaluated. The experimental results demonstrated that the proposed design had superior performance in most directions.

In conclusion, this thesis has proposed and demonstrated a feasible solution of compact on-package antenna array implementation to enhance RF energy harvesting capability. The proposed structure provided a method to make the device receive more RF power and yet maintain compactness.

5.2 Comparison to Literature

As mentioned in Chapter 1, conventional compact rectenna arrays designed for low power WPT achieves compactness either by increasing the operating frequency or miniaturize each antenna element. To the author's best knowledge very few designs in literature achieves compactness by decreasing the space between array elements. Table 5-1 compares the work in the thesis with several rectenna arrays designed for low-power WPT in literature.

Table 5-1 Comparison of measurement result with other compact rectenna array design

Works	Operating frequency	Largest Dimension (mm)	Element Spacing	No. of Elements	Power Density ($\mu\text{W}/\text{cm}^2$)	Max DC power (μW)	Average DC power per Element (μW)
[106]	2.45GHz	126	0.5λ	4	12.73	186	46.5
[122]	5.8GHz	128	0.48λ	4	1.2	6	1.5
[102]	2.4GHz	83	0.024λ	2	601.72	14000	7000
This work	0.9GHz	67	0.078λ	2	1.7	58.4	24.2

In [122] achieves compactness by increasing the operating frequency to 5.8GHz, while [106] achieves compactness by miniaturizing each antenna element. It can be seen from the 2nd column that the space between array elements of these designs is maintained around half the wavelength. [102] is the design that achieves compactness by reducing the space between array elements to merely 0.024λ , but it is a planar design and operates at much higher power density. Comparing to this work, this work achieves a more compact size even at lower frequency by implementing the antenna array on package.

When it comes to the performance of the rectenna array, the 6th column compares the maximum DC power reported when the antenna array is illuminated with incoming RF power. In addition, the average DC power generated per element is also calculated and listed in the last column. As each element may receive different amount of power and the performance of the rectifier circuit may also differ for each element, the DC voltage generated by each element is not necessarily the same. Also, the way these elements were combined also affects the final DC output. Nevertheless, the average DC power per element serves as a good figure of merit to show how efficient the array works under certain illumination condition. The comparison shows that the work reported in this thesis has comparable

performances with the other works presented, and yet it can achieve a much more compact physical size even at lower operating frequency.

5.3 Future Work

The proposed design can be easily extended to other frequency bands, such as the ISM or RFID frequency bands listed in Table 1-1. The design can also be tuned and fabricated by many currently available fabrication technologies. The very idea of decoupled compact rectenna array on-package can also be extended to multiple elements on-package with the similar solutions. This will open the door for more receiving antennas to be integrated without degrading the RF power receiving ability.

As for this very design of compact dual-antenna array on-package, other than higher receiving power, the diversity achieved by the decoupled array can be utilized to exploit and develop power efficient MIMO communication scheme to reduce the power consumption of the RF front-end to make the device become more power-efficient. The whole design can be miniaturized to a size of medical implant. With dual antenna system and associated power-efficient communication scheme developed, it is possible to make the medical implant more power efficient and achieve a higher data communication quality compared to the conventional medical implant design with single antenna.

AUTHOR'S PUBLICATIONS

Journal Publication

L. B. Wang, K. Y. See, **J. W. Zhang**, B. Salam, and A. C. W. Lu, "Ultrathin and Flexible Screen-Printed Metasurfaces for EMI Shielding Applications," *IEEE Transactions on Electromagnetic Compatibility*, vol. 53, pp. 700-705, 2011.

J. W. Zhang, K. Y. See, and T. Svimonishvili, "Printed Decoupled Dual-Antenna Array On-Package for Small Wirelessly Powered Battery-Less Device," *IEEE Antennas and Wireless Propagation Letters*, vol. 13, pp. 923-926, 2014.

Conference Publication

C. M. Tan, K. Y. See, **J. W. Zhang**, M. J. Xu, C. C. Boon, K. S. Yeo, *et al.*, "A possible reality on battery-less low-power portable electronics," in *the 5th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2010, pp. 630-633.

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