High- κ /metal gate for advanced transistor applications

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NANYANG
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HIGH-K/METAL GATE
FOR ADVANCED TRANSISTOR
APPLICATIONS

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SUMMARY

Silicon-based metal-oxide-semiconductor field effect transistors (MOSFETs) have become the most important components in many electronic devices because of the increasing number of fields in which they have been applied and the continual improvement in their performance over the past fifty years. This performance improvement has been achieved by decreasing the size of the transistor in accordance with Moore's Law scaling because transistor miniaturization results in a reduction of the unit cost per function and in improved performance. However, this scaling of the traditional gate oxide (i.e., SiO_2) cannot continue indefinitely because it would eventually reach the atomic level. To continue the scaling-down of MOSFETs, advanced high- κ materials must be developed to replace SiO_2 as the gate dielectrics.

Electronic structures consisting of various $\text{HfO}_2/\text{SiO}_2/\text{Si}$ -substrate gate stacks have been characterized using X-ray photoelectron spectroscopy (XPS) and the corresponding MOS capacitors to understand the instability of the flat-band voltage (V_{fb}). The hafnium (Hf) silicate formed at the $\text{HfO}_2/\text{SiO}_2$ interface is found to play a key role in generating an internal electric field, which is the origin of the V_{fb} variation. This electric-field formation at the interface between SiO_2 and Hf silicate can be attributed to the generation and accumulation of oxygen vacancies (V_o) in the Hf silicate layer as well as the accumulation of the resultant oxygen ions in the SiO_2 layer caused by the difference in the areal densities of oxygen atoms in the two layers. The internal electric field is thus established by interface dipoles consisting of positively charged V_o and negatively

charged oxygen ions. The magnitude of the internal electric field is higher when a thicker Hf silicate layer is formed because more V_o can be accommodated. The magnitude decreases after post-deposition annealing (PDA) at an elevated temperature because of phase separation in the Hf silicate layer.

Investigations of the interface dipole are important for characterizing a high- κ gate stack. The pulsed capacitance–voltage (CV) technique, which can precisely determine the transition state, is used to investigate the properties of the dipole. After the analysis of a series of MOS capacitors with different gate dielectrics — SiO_2 , HfO_2 , $\text{HfO}_2/\text{SiO}_2$, $\text{HfO}_2/\text{Al}_2\text{O}_3$, and $\text{Al}_2\text{O}_3/\text{HfO}_2$ — an interface-dipole relaxation model is proposed. It is found that the variation of the interface dipole with the applied gate voltage results in hysteresis between the negative-to-positive and positive-to-negative voltage-ramp CV curves. The magnitude of this hysteresis is observed to be dependent on the viscosity of the local oxide network, the dipole elasticity, the gate-oxide thickness, and the pulse ramp rate.

Si-based MOSFETs are used not only in low-power applications but also in high-power electronic devices. The development of Si-based high-power MOSFETs has been constrained by the material limitations of silicon. GaN, which has a large band gap, a high electric breakdown field, and the ability to build a two-dimensional electron gas (2DEG) channel by forming a heterostructure with GaN-based materials (e.g., AlGaN), has become one of the most attractive candidates for replacing silicon in high-power transistors.

The interface properties of Al₂O₃-capped Ga-face GaN and GaN/AlGaIn/GaN are systematically studied, and these studies are of fundamental importance to the performance improvement of high-power MOSFETs. First, the role of gallium oxide (GaO_x) in the surface band bending of n-type GaN is investigated via angle-resolved X-ray photoelectron spectroscopy (ARXPS) because of the unavoidable formation of GaO_x during the GaN based devices fabrication process. This GaO_x formation introduces positively charged states that could compensate for the negative polarization-induced charge of the GaN, changing the initial upward surface band bending. Cleaning with hydrofluoric acid (HF) is found to effectively remove the GaO_x layer and the accompanying positive states. According to the ARXPS results, a calculation based on electrostatics is performed to determine the net charge density. Secondly, the interface region between GaN as well as GaN/AlGaIn/GaN and the Al₂O₃ is studied. The regrowth of GaO_x still occurs during atomic layer deposition (ALD) after HF cleaning, despite the application of trimethylaluminum (TMA)-only cycles to convert GaO_x into Al₂O₃ during the initial stage. This suggests that there should be a lower limit on the thickness of the resultant Al₂O₃ layer that is necessary to block oxidizing agents during subsequent Al₂O₃ deposition in ALD. The valence-band offset between GaN and Al₂O₃ is determined using core-level and valence-band spectra. The band offset varies with the thickness of the Al₂O₃ deposition, which can be explained by an upward band bending at the GaN surface and the intrinsic limitations of the XPS method for band-offset determination. Thirdly, the electronic structures of Al₂O₃-capped GaN and GaN/AlGaIn/GaN samples are investigated via XPS and Hall-effect measurement. It is found that the interfacial GaO_x layer remains nearly intact after relatively low-temperature annealing. However, this

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LIST OF ABBREVIATIONS

A	Capacitor electrode area
$a.u.$	Arbitrary unit
AC	Alternating current
ALD	Atomic layer deposition
ARXPS	Angle resolved X-ray photoelectron spectroscopy
B	A constant
BE. KE	Binding energy and kinetic energy of core electrons
c	Viscosity constant
CL	Core level
CMOS	Complementary metal oxide semiconductor
CV	Capacitance voltage
CVD	Chemical vapor deposition
D, S, G	Drain, source, and gate of a FET
$d_0, d', \text{ and } d''$	Distance between positive and negative charge center at different states
DC	Direct current
dV_{ac}	AC voltage signal
E_B	Breakdown field
E_{ox}	Gate oxide field
EOT	Equivalent oxide thickness
F_c	Frictional force

F_e	Electrostatic force
F_s	Restoring force
FIBL	Fringing-induced barrier lowering
GaO _x	Gallium sub-oxide
HEMT	High-electron-mobility transistor
HF	High-frequency (in chapter 5)
HF	Hydrofluoric acid (in other chapters)
HRTEM	High-resolution transmission electron microscopy
Hf	Hafnium
$h\nu$	Photon energy of X-ray source
I_c	Displacement current
ITRS	International Technology Roadmap for Semiconductors
I_t	Tunneling current
IC	Integrated circuit
IL	Interfacial layer
J_{DT}	Direct tunneling current density
k_s	Spring constant
L	Channel length
m	Dipole mass
m^i	Ion mass
m^*	Electron effective mass
MIS-HEMT	Metal-insulator-semiconductor high-electron-mobility transistor
MOS	Metal oxide semiconductor

MOSFET	Metal oxide semiconductor field effect transistor
n	Refractive index
N	Number of ions per unit volume
NBTI	Negative Bias Temperature Instability
nMOS	N channel MOS
O^{2-}	Oxygen ion
P	Power
PDA	Post deposition annealing
pMOS	P channel MOS
PVD	Physical vapor deposition
q_d	Dipole charge
Re	Rhenium
s	Ramp rate
SMU	Source-monitor unit
t	Time
TEM	Transmission electron microscopy
TDDDB	Time Dependent Dielectric Breakdown
$T_{high-\kappa}$	High- κ thickness
TMA	Trimethyl-aluminum
T_{ox}	Gate oxide thickness
t_r, t_f	Transition time
T_{SiO_2}	SiO ₂ thickness
VBM	Valence band maximum
VBO	Valence band offset
V_{dc}	DC voltage

V_{diel}	voltage drop across the dielectric
V_o	Oxygen vacancy
XPS	X-ray photoelectron spectroscopy
ZrSi	Zr-silicide
Z_T	Ion's transverse effective charge
α	Dimensional scaling factor
β	voltage scaling factor
ω_{TO}	Frequency of the transverse optical phonon
σ	Areal density of oxygen atoms
σ_c	Net sheet charge density
σ_{high-k}	Areal density of oxygen atoms in high- κ
σ_{SiO_2}	Areal density of oxygen atoms in SiO ₂
v_s	High-field peak velocity
τ_x	X-ray penetration depth
ϕ_{m,eff,SiO_2}	Work functions obtained when using SiO ₂ as the gate dielectric
$\phi_{m,eff,high-\kappa}$	Work functions obtained when using high- κ as the gate dielectric
Φ	Spectrometer work function of XPS
Φ_b	Distance between the Fermi level and the conduction-band edge
ϕ_B	Band offset between Si and the gate oxide
2DEG	Two-dimensional electron gas

LIST OF SYMBOLS

C	Capacitance
D_{it}	Density of interface states
e	Electronic charge
E	Electric field
E_c	Conduction band energy
E_f	Fermi energy
E_g	Bandgap energy
E_v	Valence band energy
ΔE_v	Difference in valence band energy
h	Planck's constant
g_m	Transconductance
κ	Dielectric constant
N_A	Substrate doping
N_c	Density of states in the conduction band
N_D	Density of donor impurity atom
Re	Rhenium
T	Temperature
V	voltage
k	Boltzmann's constant
V_{fb}	Flat band voltage
V_g	Gate voltage
V_t	Thermal voltage
V_{th}	Threshold voltage
ε	Permittivity
ε_0	Permittivity of free space

μ	Carrier mobility
Σ	Sum

Chapter 1   Introduction

1.1. Background

At present, a large amount of information can be obtained via the Internet, and long-distance communication can be accomplished via satellite systems. These marvelous capabilities have been achieved through the development of the transistors and integrated circuits (ICs). IC technology pervades every aspect of our daily lives. The electronic gadgets that are built using IC technology include mobile phones, computers, MP3 players, laser scanners, and laptops. To satisfy the demand for faster, cheaper, and thinner electronic devices, the semiconductor industry has been developing rapidly.

IC technology entered a period of rapid growth after the first transistor was invented in 1947 at Bell Telephone Laboratories by William Shockley, John Bardeen, and Walter Brattain. Significant improvements in the fabrication process and structural design of transistors were achieved during the first ten years following the creation of the first transistor. In 1958, the first IC was demonstrated by Jack Kilby. Two years later, the first metal-oxide-semiconductor field-effect transistor (MOSFET) on a silicon substrate was reported by Kahng and Atalla. Since the development of the first IC, circuit design has grown steadily in sophistication and functionality to enable an ever-increasing number of practical applications. Silicon was chosen as the ultimate semiconductor substrate in the IC industry because of its low fabrication cost and the excellent properties

of native silicon dioxide (SiO_2), which can provide a thermally and electrically stable, high-quality SiO_2/Si interface as well as outstanding electrical isolation properties.

In 1965, Gordon Moore predicted that the transistor count per IC would double approximately every 18 months [1]. This statement later became known as Moore's Law, which the semiconductor industry has been following faithfully (Fig. 1.1). Currently, a new generation of technology is released approximately every three years. In accordance with Moore's Law scaling, not only has the density of transistors per IC chip increased but the performance of the transistors has also been enhanced.

Figure 1.1. Transistor-count trend and Moore's Law [2]

The International Technology Roadmap for Semiconductors (ITRS) is an evaluation of the semiconductor industry's future technological requirements and guides the direction of research to realize these objectives. The drive current that is responsible for the speed of a transistor is controlled by the metal-oxide-semiconductor (MOS) capacitance, which is largely determined by the thickness of the SiO_2 . A reduction in this thickness leads to a larger capacitance, which enables an increased drive current. Based on the scaling of the gate-oxide thickness, starting with a 65-nm node, the SiO_2 thickness is ~ 1.5 nm. The parasitic gate leakage current caused by carrier tunneling in such a thin oxide layer is relatively high, which results in large power consumption [3]. The speed of an IC is determined primarily by the drive current of the MOSFET, whereas the power dissipation depends largely on the off-state leakage current. It is a formidable task to achieve the desired drive current while simultaneously suppressing the leakage current by decreasing the SiO_2 thickness.

To further enhance the drive current by continuing this scaling, gate dielectrics with higher permittivity (high- κ) have been used in the fabrication of transistors to replace the conventional SiO_2 [4, 5]. Because of their large κ values, high- κ materials offer two attractive advantages. First, high- κ materials can be deposited with a greater physical thickness than SiO_2 without compromising the gate dielectric capacitance. Therefore, these materials offer a significant reduction in gate leakage current, thus reducing the power consumption [6]. Second, high- κ materials with a large physical thickness have the potential to be further scaled down to provide a significantly larger capacitance than can be achieved using SiO_2 to keep pace with Moore's Law scaling. Consequently, the implementation of high- κ materials in MOSFETs has emerged as a

topic of considerable interest in academic and industrial research since the beginning of the 1990s [3, 4, 6, 7]. In 2007, HfO_2 high- κ dielectric and metal gates were implemented in a MOSFET for the 45-nm technology generation [5]. In 2009, second-generation high- κ /metal gate transistors, at the tightest gate dimensions, were presenting remarkable drive currents for 32-nm or 28-nm logic technology [4]. The implementation of high- κ /metal gates in MOSFETs will be unavoidable in the effort to achieve the speed and power requirements stipulated by the ITRS.

Silicon-based MOSFETs not only demonstrate impressive performance in low-power applications but also exhibit excellent properties in high-power electronic devices. High-power electronic devices are typically operated under harsh conditions (e.g., at high temperatures). It is known that the temperature limit of a silicon p-n junction is 150°C [8]. Above this temperature, such a p-n junction may suffer reliability problems or lose functionality. This limitation places a barrier on the development of Si-based high-power MOSFETs when they are attempting to satisfy the requirements of high power density, high reliability, and high efficiency [8]. To overcome this limitation, high-power transistors must be developed using novel materials. For high-power applications, wide-band-gap and high-carrier-mobility materials, such as diamond, silicon carbide (SiC), and GaN, are expected to replace silicon in the near future. Among these three candidates, diamond offers the best theoretical performance. However, it is difficult and complicated to process diamond because it is a hard material and requires a high temperature for processing. Much effort must be directed toward solving these processing issues before diamond can be widely used in high-power electronic devices. SiC and GaN have comparable electrical characteristics, such as a large band gap, a high breakdown field,

and high carrier mobility. However, the ability of GaN-based material to form a two-dimensional electron gas (2DEG) by a heterojunction makes it more attractive than SiC. The advantage of a 2DEG is its higher electron mobility, which arises because channel electrons are separated from the dopants, thereby reducing ionized impurity scattering. Moreover, GaN-based III-V materials can be grown on silicon substrate [9-11]. This GaN-on-silicon wafer is compatible with the standard MOSFET processing, making the fabrication of such power transistors economically feasible.

GaN-based high-electron-mobility transistors (HEMTs) take advantage of the properties of a 2DEG and have been widely used in high-power and high-frequency electron devices. However, the performance of the conventional HEMT is limited by the intrinsically high leakage current of the Schottky gate as well as surface-defect-induced gate leakage and drain-current collapse at high frequency [12-17]. Recently, it has been demonstrated that the adoption of a high- κ as the gate dielectric and surface passivation layer in metal-insulator-semiconductor HEMTs (MIS-HEMTs) could help to mitigate the above issues [9, 15, 18, 19]. MIS-HEMTs, which combine the merits of HEMTs and the MIS devices, offer the advantages of a positive threshold voltage, a low leakage current, and excellent reliability [20, 21]. They are deemed the most promising next-generation high-power transistors.

1.2. Motivation

It has been observed that HfO₂-based high- κ gate dielectrics in combination with metal gates exhibit excellent electrical characteristics, and they have already been

implemented in the manufacturing of advanced MOSFETs [4, 5, 22]. Although significant improvements in processing and devices performance have been achieved, V_{fb} reliability issues still prevent HfO_2 /metal gates from being widely applied [23, 24]. To improve the performance of HfO_2 -based high- κ gate stacks, a clear understanding of the electronic structure of the gate stack becomes necessary to study these reliability issues.

The interface between the high- κ material and the substrate is believed to play a key role in determining the performance of a transistor [25, 26]. However, the properties of the interface have not been comprehensively studied. The pulsed capacitance–voltage (CV) technique, which can detect transition states with a microsecond timing resolution, is able to precisely observe the transient states of the interface. Therefore, the use of the pulsed CV technique to characterize the interface is expected to provide useful insight into the properties and behavior of the interface.

GaN is one of the most attractive options for use in high-power electronic devices. However, GaN does not have a stable native oxide such as SiO_2 in the case of Si. High- κ materials must be adopted as the gate dielectric and surface passivation layer. The implementation of GaN materials in high-power transistors faces two major challenges. First, GaN possesses polarization-induced bound charges that are related to the interface quality and V_{fb} control. Second, GaN reacts readily with oxygen, which is present in the ambient atmosphere or the oxidant precursor during high- κ deposition, to form a gallium oxide (GaO_x) layer that generates certain surface states on the surface [17, 27-30]. These surface states exacerbate the gate leakage current and cause the drain-current collapse at high frequency [12, 16, 31]. To date, the mechanism of the passivation of the surface states and the role of GaO_x in the surface band bending of GaN have not yet been

clarified. It is desirable to investigate the mechanism of the passivation of the surface states as well as the electronic structures of the high- κ /GaN gate stack because these topics are essential to the successful application of GaN in high-power transistors.

1.3. Objectives

The interface between HfO_2 and the SiO_2/Si substrate is of importance in controlling the V_{fb} stability of MOS devices. Therefore, the first objective of this thesis is to seek a thorough and clear understanding of this interface. Electronic structures of HfO_2 of different thicknesses on SiO_2/Si substrates and the thermal stability of the $\text{HfO}_2/\text{SiO}_2/\text{Si}$ gate stack are analyzed to investigate the interface properties using X-ray photoelectron spectroscopy (XPS) and the corresponding MOS capacitors.

The interface between the high- κ material and the substrate is believed to be responsible for the V_{fb} instability. Pulsed CV measurements, which can capture the transient states of MOS capacitors, are able to supply useful information for the investigation of this interface. The second objective of this thesis is to use pulsed CV to gain a deep understanding of the interface. This is achieved by means of a series of CV measurements of capacitors with various gate dielectric structures: SiO_2 , HfO_2 , $\text{HfO}_2/\text{SiO}_2$, $\text{HfO}_2/\text{Al}_2\text{O}_3$, and $\text{Al}_2\text{O}_3/\text{HfO}_2$.

A systematic study to characterize Al_2O_3 -capped GaN and GaN/AlGaN/GaN samples is important to the implementation of GaN in high-power electronic devices and is the final objective of this thesis. Al_2O_3 has been adopted as the gate dielectric and passivation layer because of its superior surface-state passivation effect, high breakdown

field, and large energy-band (conduction-band and valence-band) offsets between Al_2O_3 and GaN [17, 18, 32]. The role of native GaO_x on the surface band bending of GaN, which is of prime importance to the investigation of the $\text{Al}_2\text{O}_3/\text{GaN}$ interface because GaO_x is inevitably formed during Al_2O_3 deposition, is investigated using angle-resolved X-ray photoelectron spectroscopy (ARXPS). The interface chemistry and valence-band offset between GaN and Al_2O_3 are studied using XPS to elucidate the origin and mechanism of the surface passivation caused by Al_2O_3 . In addition, a series of thermal-annealing studies on Al_2O_3 -capped GaN and GaN/AlGaN/GaN samples is planned to study the reliability of the interfacial layer and the effect of annealing on the 2DEG.

1.4. Organization of the thesis

This report consists of seven chapters. The organization is as follows:

- *Chapter one* introduces the background, motivation, objectives, organization, and original contribution of this thesis.
- *Chapter two* provides a literature review on the achievement and the issues of high- κ gate stack as well as the studies related with the implementation of GaN into high-power transistors.
- *Chapter three* focuses on the characterization methods and the procedure details of XPS, Keithley 4200, and Agilent B1500.
- *Chapter four* presents a comprehensive study on the electronic structure of the $\text{HfO}_2/\text{SiO}_2/\text{Si}$ gate stack by XPS and the corresponding MOS capacitors.

- *Chapter five* presents the investigation of interface properties in the high- κ /metal gate-stack from pulsed CV Measurement.
- *Chapter six* presents the systematic study of interface properties of Al_2O_3 -capped GaN and GaN/AlGaIn/GaN.
- *Chapter seven* provides the conclusion of the thesis, as well as suggestions and recommendations for future works.

1.5. Original contributions

The major contribution of this thesis is the presentation of systematic studies of the properties of interfaces between high- κ gate dielectrics and semiconductor substrates. These research achievements can be summarized as follows.

The electronic structures of HfO_2 layers of various thicknesses on SiO_2/Si substrates are investigated. It is found that the Hf silicate that forms between HfO_2 and SiO_2 plays a key role in the formation of oxygen vacancies (V_o) because the V_o formation energy in the Hf silicate layer is lower than that in the bulk HfO_2 . Furthermore, the V_o are believed to be generated at the Hf silicate/ SiO_2 interface because of the difference in the areal density of oxygen between the two materials, resulting in the penetration of oxygen ions into the SiO_2 layer. Positively charged V_o and negatively charged oxygen ions give rise to an internal electric field at the Hf silicate/ SiO_2 interface. A thicker Hf silicate layer can accommodate more V_o , thus causing a stronger internal electric field to form. The XPS results are verified by the consistency with the V_{fb} and equivalent oxide thickness (EOT) values extracted for MOS capacitors. In addition, another electronic structure is

considered to investigate the thermal stability of the $\text{HfO}_2/\text{SiO}_2/\text{Si}$ structure. It is observed that the Hf silicate decomposes at an elevated PDA temperature because of phase separation, and the magnitude of the internal electric field is found to decrease accordingly.

An investigation of the interface dipole located between the high- κ material and the Si substrate is conducted using the pulsed CV technique. Unusual hysteresis is observed between the forward and reverse CV curves because their magnitudes vary only with the voltage ramp rate, not with the voltage pulse width. Through a comparison between the pulsed CV results and those obtained using the static CV method, the carrier trapping/detrapping explanation is ruled out. Moreover, an analysis of capacitors with different gate dielectric structures eliminates the high- κ bulk-related explanation. Finally, an interface-dipole relaxation model that can successfully explain the dependence of the hysteresis on the ramp rate, the viscosity of the local oxide network, and the elasticity of the dipole as well as the thickness of the dielectric is proposed.

A systematic study of the properties of the interfaces between Al_2O_3 and Ga-face n-type GaN as well as Ga-face GaN/AlGaN/GaN is presented. First, the role of native GaO_x on the surface band bending of n-type GaN is analyzed using ARXPS. Positively charged donor states associated with the formation of native GaO_x are critical in determining the direction and magnitude of the band bending. These positive charges compensate for the negative charges induced by spontaneous polarization and thus alter the band bending. A hydrofluoric acid (HF)-treated GaN surface is investigated, and the HF cleaning is found to effectively remove the GaO_x layer, yielding a low surface charge density. A calculation of the net charge density is performed based on an electrostatics

analysis of the surface region. The density of the net positive charges is calculated to be $2.09 \times 10^{12}/\text{cm}^2$ for a GaN surface with native GaO_x , whereas a net negative charge with a density of $1.0 \times 10^{12}/\text{cm}^2$ is obtained after the HF cleaning treatment. Secondly, the interface region between the n-type GaN and the Al_2O_3 dielectric is investigated using XPS. An increase in the Ga-O/Ga-N bond-intensity ratio following Al_2O_3 deposition implies that the growth of an interfacial GaO_x layer occurred during the ALD process. This finding may be ascribed to GaN oxidation, which may still occur following the reduction of a thin native GaO_x layer by trimethylaluminum (TMA) during the initial TMA-only cycles. The valence-band offset between GaN and Al_2O_3 , which is determined using both core-level and valence-band spectra, is found to vary with the thickness of the deposited Al_2O_3 . This observation may be explained in terms of upward energy-band bending at the GaN surface (caused by the spontaneous-polarization-induced negative bound charge on the Ga-face GaN) and the intrinsic limitations of the XPS method for band-offset determination. Thirdly, the electronic structures of Al_2O_3 -capped GaN and GaN/AlGaIn/GaN samples are investigated via XPS and Hall-effect. The interfacial GaO_x layer formed during Al_2O_3 deposition remains nearly intact following low-temperature PDA. However, a structural change is observed in the GaO_x layer after PDA at 800 °C. Accordingly, the density and mobility of the 2DEG are found to decrease and increase, respectively, after PDA, indicating that a reduction in the Al_2O_3 /GaN-interface defect density has occurred. These findings imply that the observed improvement in the 2DEG mobility should be ascribed to a thermally induced change in the interfacial layer.

Chapter 2   Literature review

2.1. Scaling rules and selection guidelines for high- κ gate dielectrics

Si-based electronic gadgets (e.g., mobile phones, computers, printers, and laptops) have become an indispensable part of our daily lives. This primacy has been established by the continual development of electronic devices exhibiting progressively higher performance speed, greater density, and lower power consumption. In 1965, Gordon Moore forecasted that for industry to meet these technological requirements and expand the market, the transistor count per IC would double approximately every 18 months [1], a prediction currently known as Moore's Law.

2.1.1.   MOSFET scaling rules

Based on Moore's Law of scaling, various scaling rules have been proposed for the scaling of both the size and performance of devices [33-35], including constant-field scaling, constant-voltage scaling, generalized scaling, and quasi-constant voltage scaling. The details of the scaling rules are presented in Table 2.1. The basic concept of the constant-field scaling rule is explained in Fig. 2.1. When a scaling factor α is applied to shrink a FET to a smaller size while maintaining similar behavior, all dimensions and

voltages should be decreased by the scaling factor α while increasing the substrate doping by the same factor α . Therefore, the electric-field configuration inside the smaller-size FET remains the same as that of the original device [36, 37]. However, it is difficult to simultaneously scale both voltages and dimensions by the same factor because V_{th} is difficult to modify [38]. Consequently, drain current will be reduced by a factor more than α , which erodes the scaling benefit. Therefore, constant-voltage scaling is proposed to address this issue, in which voltages remain constant as device dimensions are scaled. However, constant-voltage scaling leads to a high electric field, resulting in large leakage current, high power consumption, and reliability issues. To achieve the best transistor performance and reach a practical compromise, generalized and quasi-constant voltage scaling rules have been introduced to compensate for the flaws of the constant-field and constant-voltage scaling rules. The generalized and quasi-constant voltage scaling rules suggest that voltages should be reduced less aggressively than device dimensions to optimize the trade-off between MOSFET miniaturization and performance. In practice, quasi-constant voltage scaling is often adopted in MOSFET fabrication.

Table 2.1 The scaling parameters for constant-field scaling, constant-voltage scaling, generalized scaling, and quasi-constant voltage scaling [33-35].

MOSFET Device and Circuit Parameters	Scaling rules			
	Constant E	Constant V	Generalized	Quasi-constant V
Device dimensions (T_{ox}, L)	$1/\alpha$	$1/\alpha$	$1/\alpha$	$1/\alpha$
Supply voltage (V)	$1/\alpha$	1	$1/\kappa$	$1/\alpha^{1/2}$
Gate oxide field (E_{ox})	1	α	α/κ	$\alpha^{1/2}$
Gate delay	$1/\alpha$	$1/\alpha^2$	κ/α^2	$1/\alpha^{3/2}$
Substrate doping (N_A)	α	α	α^2/κ	α
Power Density (P/A)	1	α^3	κ^3/α^3	$\alpha^{3/2}$

(α : Dimensional Scaling Factor; κ : Voltage Scaling Factor)

Figure 2.1 A schematic diagram to explain the principles of the constant-electric-field scaling rule. V_g is the voltage applied to the gate. S and D denote the source and drain, respectively [36].

2.1.2. Limitations of SiO_2 as the gate dielectric

As is well known, silicon wafers are widely used in MOSFET fabrication because of their low cost and the remarkable properties of the native oxide SiO_2 . SiO_2 has a high electric breakdown field, a large band gap of ~ 9 eV, and excellent electrical isolation properties. Moreover, the conduction-band and valence-band offsets at the SiO_2/Si interface are 3.5 eV and 4.4 eV, respectively. This large band offset can help to prevent substrate injection (i.e., Electrons (holes) in the substrate jump into the conduction (valence) band when the band offset at gate dielectric/substrate interface is less than 1 eV), thereby significantly reducing the gate leakage current.

However, a decrease in the transistor size causes the gate length and the gate-oxide thickness to decrease quickly, as shown in Fig. 2.2. The SiO_2 thickness may

eventually become comparable with the diameter of the Si atom if projected scaling trend were to just continue. In a very thin SiO₂ layer, the direct tunneling current flowing from the gate to the substrate, as illustrated in Fig. 2.3, becomes extremely large. The direct tunneling current density J_{DT} , as shown in Equation (2.1), exponentially increases as the gate oxide thickness and the band offsets decrease [39, 40].

$$J_{DT} = \frac{B}{T_{ox}^2} \exp\left(-2T_{ox} \sqrt{\frac{2m^*}{\left(\frac{h}{2\pi}\right)^2} \left(\phi_B - \frac{V_{diel}}{2}\right)}\right) \quad (2.1)$$

where, B is a constant, T_{ox} is the thickness of the gate oxide, ϕ_B is the band offset between Si and the gate oxide, V_{diel} is the voltage drop across the dielectric, and m^* is the effective electron mass in the dielectric.

Figure 2.2. The physical gate length and EOT of high-performance logic technology according to the 2012 Semiconductor Roadmap.

Figure 2.3 Direct tunneling current flows from the gate to the substrate when the gate oxide thickness T_{ox} is too small.

Figure 2.4. Leakage current versus voltage for SiO_2 layers of various thicknesses [41].

As shown in Fig. 2.4, when the SiO_2 thickness is less than 20 Å, the gate leakage current density caused by direct tunneling of electrons becomes too high, exceeding 1 Acm^{-2} at 1 V. Therefore, the power dissipation increases to an unacceptable level [6, 42-45]. Moreover, the electric breakdown field becomes extremely low when the gate oxide is too thin. Further, the carrier tunneling through such a thin gate dielectric film could generate electron or hole traps and defect states inside the gate dielectric. After several operation cycles, the gate dielectric quickly degrades, leading to many reliability problems [46, 47], such as short device lifetime and large power consumption.

Another disadvantage of a thin SiO_2 layer is boron penetration [48-50]. During post-implantation annealing, the boron from the P^+ polysilicon gate may penetrate through the thin SiO_2 layer into the channel, as shown in Fig. 2.5. This uncontrollable boron penetration causes a positive shift in V_{th} [49] and results in V_{th} instability. Moreover, the channel carrier mobility decreases because of carriers scattering by ionized boron atoms.

Figure 2.5. Boron penetration through the thin SiO_2 layer into the channel during thermal annealing [49].

2.1.3. Advantages of high- κ gate dielectrics

Transistors are capacitance-controlled devices and the drive current of a transistor depends largely on the MOS capacitance. To solve the scaling issues faced by using SiO_2 as the gate dielectric, it is suggested to find solutions from the MOS capacitance. The determined item of MOS capacitance is the gate oxide capacitance which is given by equation (2.2):

$$C = \frac{\epsilon_0 A k}{T_{ox}} \quad (2.2)$$

where ϵ_0 is the permittivity of free space, A is the area of the capacitor electrode, k is the dielectric constant, and T_{ox} is the gate-oxide thickness.

Figure 2.6 Using high- κ material to replace SiO_2 as the gate dielectric could reduce the direct tunneling current while maintaining the same electrical characteristics.

According to equations (2.1) and (2.2), replacing SiO₂ with a physically thicker layer of material having a higher dielectric constant (relative permittivity) κ could decrease the tunneling current without compromising the gate dielectric capacitance. As shown in Fig. 2.6, after such a replacement, the electrical characteristics of the two transistors are nearly identical since the required gate oxide capacitance has not changed. Material with a higher κ value than that of SiO₂ is called high- κ material. From the perspective of device design, it is convenient to define a quantity known as the EOT to evaluate a high- κ material in terms of its equivalent silicon dioxide thickness.

$$EOT = \left(\frac{3.9}{\kappa}\right)T_{high-\kappa} \quad (2.3)$$

where 3.9 and κ are the static dielectric constant of SiO₂ and the high- κ material, respectively. $T_{high-\kappa}$ is the physical thickness of the high- κ material.

A schematic diagram of the direct tunneling current through a thin SiO₂ layer and a thicker high- κ layer (i.e., with the same EOT as the SiO₂ layer) is presented shown in Fig. 2.7. The tunneling current is significantly reduced for the high- κ gate dielectric because the current must traverse a large thickness.

Figure 2.7. A schematic diagram comparing the direct-tunneling process across a thin SiO_2 layer and a thicker high- κ layer. The two layers have the same EOT.

2.1.4. Selection guidelines for high- κ gate dielectrics

The use of SiO_2 as a gate dielectric has been studied and implemented in MOSFET fabrication for decades. When replacing SiO_2 with a high- κ material, there are many considerations involved in selecting a suitable candidate, such as the κ value, band offset, morphology, deposition tools, thermodynamic stability, gate compatibility, and gate-stack reliability.

2.1.4.1. κ value

The key feature of a high- κ material is its high κ value. A high- κ material has a larger physical thickness than that of SiO_2 for the same EOT. Because of this large thickness, the tunneling current is significantly reduced. Moreover, the high- κ material can be further scaled down for future generations of technology. The κ value should be

over 12, preferably 20-25, to satisfy the scaling requirements. However, a high- κ material with κ larger than 25 is ruled out for the following three reasons.

First, the κ value arises from the lattice contribution [6]:

$$\kappa = n^2 + \sum \frac{Ne^2 Z_T^2}{m^i \omega_{TO}^2} \quad (2.4)$$

where n is the refractive index, N is the number of ions per unit volume, e is the electronic charge, Z_T is the ion's transverse effective charge, m^i is the reduced ion mass, ω_{TO} is the frequency of the transverse optical phonon, and the sum is over the ions.

A large κ value arises when a material possesses a large Z_T and a small frequency of a polar optical mode ω_{TO} . As a result, ionic polarizability begins to appear in high- κ dielectric [6, 51]. Moreover, low-energy surface optical phonon modes arising from the polarization couple to the inversion channel carriers, resulting in the carrier mobility degradation [51, 52].

Second, fringing-induced barrier lowering (FIBL) is another issue. The energy barrier between the source and the drain is reduced by the presence of a strong fringing field at the edge of the high- κ dielectric. Carriers can flow from source to drain without the device being turned on. This phenomenon can degrade the off/on characteristics [53] and cause reliability problems.

Third, the κ value varies inversely with the band gap, which is another important factor in selecting a high- κ candidate. The relation between the κ value and the band gap is illustrated in Fig. 2.8. It is found that a large κ value tends to accompany a small band

gap. It would not provide a large enough barrier at the interface to block current flow and leads to a large leakage current.

Figure 2.8. Static dielectric constant versus band gap for candidate gate dielectrics [6, 54].

2.1.4.2. Band offset at the high- κ /Si substrate interface

The band gap is a critical feature based on which materials are classified as metals, semiconductors, and insulators. A gate dielectric should be an insulator and have a large band gap to guarantee that the band offset at the high- κ /Si substrate interface is greater than 1 eV to suppress the emission of electrons or holes from the substrate into the energy bands of the gate dielectric [6, 54], as illustrated in Fig. 2.9.

The band-offset values at various high- κ /Si substrate interfaces are presented in Fig. 2.10. According to equation (2.1), a large band offset facilitates a small leakage current. Therefore, a high- κ material with a large band offset is preferred. Because the band gap and the κ value are inversely proportional to each other, careful optimization is required to balance these two parameters. Therefore, a high- κ material is favored when its κ value is in the range of 20-25 as well as its band offsets are over 1 eV.

Figure 2.9. Schematic diagram of band offsets determining electron or hole emission into the gate-dielectric band states.

Figure 2.10. Calculated conduction-band and valence-band offsets for various oxides with respect to Si [54].

2.1.4.3. High- κ material morphology

The glassy phase (amorphous) and the crystalline phase are two candidate morphologies for high- κ gate dielectrics. Crystalline high- κ materials face certain difficulties, such as grain boundaries serving as leakage-current paths, κ -value variations caused by changes in orientation throughout a crystalline film, and anisotropic electrical properties. Because of these issues, the crystalline phase is not suitable for high- κ gate dielectrics application. Amorphous high- κ films do not suffer from the problems mentioned above if they do not receive high temperature (i.e., over 600 °C) process. Moreover, they have a uniform quality and are easy to deposit [42]. Therefore, an amorphous high- κ film would appear to be a more suitable choice.

However, the PDA and post-implantation annealing processes may introduce crystallization into an amorphous high- κ film. This crystallization phenomenon results in the formation of many grain boundaries, which provide leakage-current paths, thereby inducing large leakage currents. Therefore, Intel introduced a gate-last process [5]. Dummy gates are deposited first to allow the structure to endure the high-temperature steps of the flow (i.e., S, D annealing); then a high- κ dielectric is deposited after the complete removal of the dummy gates. This gate-last approach maintains the amorphous phase and high quality of high- κ films, which benefits device reliability and mobility [4, 7].

2.1.4.4. Deposition of high- κ materials

As the EOT is being scaled down, the thickness of a high- κ gate dielectric is equivalent to several atomic layers. To fabricate a conformal and pin-free insulating high- κ film, the deposition tools must satisfy certain strict requirements. Physical vapor deposition (PVD) tends to cause plasma-induced damage and is a line-of-sight deposition method, which cannot provide good coverage. Thus, PVD is not preferred for the deposition of high- κ films. Chemical vapor deposition (CVD) and Atomic layer deposition (ALD) are methods that involve the use of a volatile compound as a metal precursor and H_2O or ozone as an oxidant. They can provide conformal coverage over complex shapes. However, CVD cannot precisely control the film thickness; therefore, ALD, which is a tool for cyclic deposition and oxidation [55, 56], is adopted in the deposition of high- κ films. ALD can be used to grow the thinnest films among all potential deposition approaches and the most conformal films, which can fill even deep trenches. The films deposited via ALD fulfill the thickness requirements for a gate dielectric. Therefore, ALD is preferred over other traditional deposition tools for the deposition of high- κ materials.

The cyclic deposition process of ALD is illustrated in Fig. 2.11. The substrate is exposed to a metal precursor, such as HfCl_4 , after a precursor pulse. When the surface is fully covered by the precursor such that a saturated monolayer has been achieved, the excess precursor is purged using N_2 gas. Subsequently, an oxidant H_2O pulse is applied to fully oxidize the adsorbed layer into the oxide and a volatile byproduct (e.g., HCl). The excess H_2O and byproduct are then similarly purged using N_2 gas. Finally, a layer of

HfO₂ is deposited on the substrate, and the deposition thickness is controlled by the number of cycles performed. The thickness of a high- κ film can be measured using a VB-250 Spectroscopic Ellipsometer, which has a thickness resolution of 2 Å

Figure 2.11. Schematic illustration of the cyclic process of atomic layer deposition.

2.1.4.5. Thermodynamic stability of high- κ materials

Most high- κ materials are unstable against reactions with the silicon substrate and the polysilicon gate during fabrication. Three common reaction products are silicon suboxide, silicide, and silicate. The ternary-phase diagram is an important tool for predicting and comprehending the relative stability of a given three-element system [57-59]. The Gibbs free energy governs the relevant chemical reactions in an M-O-Si system. This

quantity can be used to predict the interfacial reactions between a high- κ material and Si, as shown in figure 2.12.

Figure 2.12. A reaction flow chart depicting the reactions (unbalanced, as shown) governed by the Gibbs free energy in a particular M–Si–O system [59].

Studies have found that an interfacial SiO_x layer or silicate was formed during HfO_2 deposition, which can be detected using high-resolution transmission electron microscopy (HRTEM) [6]. SiO_x and silicate have smaller κ values than that of HfO_2 , which could cause the transistor performance to degrade. Similarly, SiO_x and ZrSi (a metallic material called silicide) are found at the ZrO_2/Si substrate interface and the $\text{ZrO}_2/\text{polysilicon}$ gate interface during ZrO_2 deposition, respectively [50]. The latter is

formed when the oxygen is deficient during ZrO_2 deposition. The ZrSi leads to a drop in the gate dielectric capacitance caused by a large leakage current. This capacitance drop reduces the drive current and hence the transistor speed. To eliminate this chemical reaction, some processes are induced. The gate-last process is an effective method to avoid the high thermal steps that may trigger an interfacial reaction. Moreover, metal gates have been adopted to avert such reactions at the high- κ /polysilicon-gate interface [4, 7].

2.1.4.6. Metal gates

V_{th} can be easily adjusted by changing the dopant implantation of the polysilicon gate, which is an extremely convenient variable in device design. However, because of Moore's Law scaling and the application of high- κ dielectrics, challenges related to the high- κ /polysilicon-gate structure have emerged. First, the polysilicon gate can become depleted just as the Si substrate. The depletion region increases the EOT, which degrades the capacitance gain of the gate dielectric that should be achieved according to the scaling rules. Second, the polysilicon can react with the high- κ material to form silicide, which is a metallic material that may form a path for a gate leakage current, resulting in a drop in the MOS capacitance [50]. The third concern is Fermi-level pinning. High- κ materials may react with polysilicon to form interfacial bonds, which may pin the Fermi level and V_{th} [60]. A fixed V_{th} is disadvantageous in device design and application.

Because of these considerations, the polysilicon gate electrode is replaced with a metal gate because the use of a metal gate could eliminate the poly depletion effect, the

chemical reaction at the high- κ /polysilicon-gate interface, and the phonon scattering caused by polarization in the high- κ material [51].

TiN, the Fermi level of which is located at the midgap of the Si substrate, can be used in both nMOS and pMOS structures. Moreover, TiN is stable when it is in contact with high- κ materials [61]. TiN has been studied extensively and has already been applied in industrial fabrication [24, 62] and may be used in the 14-nm node [63]. However, as the size of the technology node decreases below 14-nm node, the V_{th} when TiN is used as the gate becomes too large; thus, it becomes difficult to turn on the device. Therefore, a dual band-edge work function metal gate may be required to satisfy the V_{th} requirement. For example, TiN could serve as the gate for a pMOS structure, whereas TiN alloyed with Al can be used in an nMOS structure [4, 64, 65] .

2.1.4.7. High- κ gate-stack reliability

Reliability is an important factor in the selection of high- κ materials. It has been observed that all high- κ materials contain an extremely large amount of fixed charges compared with SiO₂, regardless of the high- κ deposition method [66]. The presence of these fixed charges is attributed to charge-trapping centers, which are likely to be present in the high- κ bulk as well as the interfacial layer and the high- κ /gate-electrode interface, resulting in variation in V_{th} and a degradation of the device [66].

When investigating the reliability of a high- κ gate stack, the Negative-Bias Temperature Instability (NBTI) should be a top priority in a study of the reliability of a high- κ gate dielectric because it can seriously affect the device and potentially cause circuit failure. Time-Dependent Dielectric Breakdown (TDDB) is another serious failure

mechanism for high- κ materials, and it is also suspected that the V_o in high- κ dielectrics are responsible for TDDB [66, 67].

2.2. HfO₂ high- κ gate dielectrics

Among the candidate high- κ gate dielectrics, HfO₂ receives considerable attention because it possesses excellent scalability along with a large κ value (>20), a relatively large band gap of 5.8 eV, and compatibility with the conventional transistor process [23, 61, 62, 68]. The semiconductor industry has implemented HfO₂/metal gates in a gate-dielectric-last manner for sub-28-nm technology nodes [4, 7, 63, 65]. Transistors with HfO₂/metal gate stacks can achieve EOT scaling and reduced gate tunneling current, leading to faster operation and lower power consumption. However, certain issues related to processing, physics, and device design still remain to be clarified.

2.2.1. Interfacial layer at the HfO₂/Si-substrate interface

It is difficult to obtain a high-quality HfO₂/Si interface that is as ideal as that observed for SiO₂ because an interfacial layer (IL) is present following the deposition of HfO₂ on a Si substrate using most vapor-phase growth tools. During the initial stage of HfO₂ deposition, the silicon substrate is oxidized to form a SiO_x layer [69]. Park et al. [70] have reported that this SiO_x layer gradually becomes a hafnium silicate film because of Si diffusion from the substrate. By contract, Harada et al. [71] have suggested that the formation of this Hf silicate layer is caused by the interdiffusion of Hf and Si. Moreover, Yeo et al. [69] have reported that a PDA process can enhance the diffusion, thus leading to a

thicker Hf silicate layer. The IL formed at the HfO_2/Si -substrate interface is schematically illustrated in Fig. 2.13. From this figure, it can be seen that the thickness of the IL increases as a result of the application of a PDA process [69]. In addition, Cho et al. have suggested that not only Hf silicate but also Hf silicide may be formed because of the presence of oxygen deficiencies or a reaction between the hafnium precursor and the Si substrate [72, 73].

Figure 2.13. A trilayer $\text{HfO}_2/\text{Hf-silicate}/\text{Si-substrate}$ structure formed after HfO_2 deposition. The thickness of the Hf silicate layer is increased after the application of a PDA process because of increased Si diffusion from the substrate.

The IL has been experimentally confirmed using XPS and transmission electron microscopy (TEM) [69, 70, 72]. A Si 2p XPS spectrum is presented to demonstrate the presence of the interfacial layer in an HfO_2/Si -substrate structure. The sample was prepared by depositing ~3 nm of HfO_2 via ALD on a hydrofluoric acid (HF)-cleaned P-type silicon wafer, followed by PDA annealing at 600 °C in N_2 for 30 s. As shown Fig. 2.14, the XPS peak located at 99.0 eV represents the crystalline Si substrate, whereas the small peak at a BE of 102.8 eV (highlighted by a red circle) represents Si-O bond of the SiO_x interfacial layer.

Figure 2.14. The interfacial layer detected in the Si 2p XPS spectrum of a HfO₂/Si substrate.

A Hf silicate layer also appears at the HfO₂/SiO₂ interface [73-75]. Chen et al. [76] have used Fourier transform infrared spectroscopy to confirm the appearance of Hf-O-Si chemical bonds (from the Hf silicate layer) at the HfO₂/SiO₂ interface after annealing at a high temperature. Cho et al. [73] have observed that Hf silicate is more easily formed during the initial stage of HfO₂ deposition because of the abundance of Si atoms at the interface. This is because Hf atoms from the metal precursor can bond with Si atoms to form Hf silicate under oxygen-deficient conditions. Similarly, a Hf silicide layer is also observed at the HfO₂/SiO₂ interface interface [73].

The IL has a smaller κ value than that of HfO₂, which would increase the EOT and thus compromise the capacitance gain achieved by using HfO₂. Moreover, the IL has

low film quality because of defect states and dangling bonds, which would cause the device performance to degrade due to a large leakage current [70, 72].

2.2.2. Thermal stability of the interfacial layer

In transistor fabrication, some high-temperature processes are necessary. For example, rapid thermal annealing at a high temperature is used to active the dopants after implantation. The effects of this high temperature on the IL have been systematically studied by Cho et al. [77]. It has been observed that crystallization/phase separation occurs in the Hf silicate layer when the annealing temperature is over 800 °C. The degree of phase separation is related to the Si concentration in the film. When the SiO₂ fraction in the Hf silicate is greater than 75%, no phase separation is detected, even when the annealing temperature is 900 °C. The phase separation occurs at the interface, causing many SiO₂ and HfO₂ grains to form in the film and introducing many grain boundaries, which serve as paths for the leakage current [62]. Furthermore, Wu et al. [62] have reported that the phase separation is also affected by the density of V_o in the Hf silicate. These authors have proposed a useful multi-deposition-multi-room-temperature annealing technique to repair the V_o to improve the IL quality. After this annealing treatment, the number of grains and the leakage current are significantly reduced.

2.2.3. The instability of V_{th}/V_{fb}

V_{th}/V_{fb} instability is observed in transistors or capacitors in which HfO₂ is employed as the gate dielectric [23, 24, 26, 78]. Several mechanisms have been proposed to explain this instability [24, 26, 60, 78]. Hobbs et al. [60] have reported that the Fermi-

level pinning at the poly-Si/HfO₂ interface is the origin of the instability. The Hf-Si bonds at the interface act as interface dipoles generated by the transfer of electrons from Hf atoms to Si atoms. This transfer is limited for a n-poly gate because there is no available level that can accommodate the electrons. However, the situation is reversed for a p-poly gate because there are many states accessible to electrons, resulting in an increased E_f . The formation of Hf-Si bonds pins the Fermi level below the poly-Si conduction band, resulting in a high V_{th} . However, this Fermi-level pinning cannot explain the V_{th} instability of transistors with metal gates. Cartier et al. [78] have used a rhenium (Re)-metal-gate/HfO₂/Si-substrate structure to explain the role of V_o in this instability. The transference of charges from V_o located in the HfO₂ to the Re gate leads to the formation of an interface dipole. Consequently, the effective gate work function and V_{fb} are modified, as illustrated in Fig. 2.15. The magnitude of the V_{fb} shift is related to the V_o concentration in the HfO₂ near the Re gate [78].

Figure 2.15. Schematic diagrams illustrating the charge transfer from V_o to the Re gate, leading to the formation of a dipole to modulate the V_{fb} shift [78].

Kamimuta et al.[24] have compared the effective gate (n+ poly-Si, TaN, TiN, W, and Pt) work functions obtained when using SiO₂ as the gate dielectric (ϕ_{m,eff,SiO_2}) with the work functions $\phi_{m,eff,high-\kappa}$ obtained when using high- κ materials (HfO₂, Al₂O₃, and Y₂O₃), as illustrated in Fig. 2.16. The $\phi_{m,eff,high-\kappa}$ values are seen to lie along a line parallel to the ideal line (S=1 indicates that there is no Fermi-level pinning at the high- κ /metal interface), indicating that the high- κ /gate interface is neither a location of interfacial dipole formation nor the primary reason for the V_{fb} shift. Therefore, it is suggested that the dipole formed at the high- κ /SiO₂ interface that should be responsible for the V_{fb} shift of capacitors with non-Si-based metal gates [79].

Figure 2.16. The $\phi_{m,eff,high-\kappa}$ shift of every high- κ material is well fitted by a parallel shift of the ideal line (S=1) [24]. ©2007 IEEE

Sivasubramani et al.[80] have proposed that the differences in the electronegativities and ionic radii are the physical origin of this interface dipole. The V_{th} shift varies as a function of the net dipole moment, which is determined by the Hf-O and

rare earth (RE)-O chemical bonds at the high- κ /SiO₂ interface. However, this model cannot explain the experimental results in which negative V_{fb} shifts are observed [79]. Kita et al. [26] have illustrated the physical origin of the interface dipole present at the high- κ /SiO₂ interface. As shown in Fig. 2.17, the high- κ material and SiO₂ both possess the common element oxygen. After the materials come into contact with each other, the bonds of these O atoms will reach an equilibrium state at the interface through self-adjustment. The difference in the oxygen atom density (σ) between the two materials drives O diffusion from the high- κ material (higher σ) to SiO₂ (lower σ) at the interface, leading to the generation of V_o on the high- κ side and oxygen ions on the SiO₂ side [26]. An interface dipole is thus formed by the positively charged V_o and the negatively charged O^{2-} at the high- κ /SiO₂ interface. The magnitude and direction of the dipole are determined by the O-atom diffusion at the interface.

Figure 2.17. A schematic illustration of the physical origin of the dipole formation at the high- κ /SiO₂ interface based on the difference in σ . (a) The O atoms diffuse from the higher- σ material to the lower- σ material because of the σ difference at the interface. Thus, (b) an interface dipole is formed by the O^{2-} and V_o^{2+} , leading to V_{fb} instability [26].

The magnitude of the interface dipole is difficult to control, leading to irreproducible properties. Therefore, a great deal of research must be conducted to determine how to precisely control V_{th} . The IL and interface dipole are both observed in HfO_2 high- κ gate stack, therefore, it is necessary to investigate the role of the IL in the interfacial dipole formation.

2.3. GaN application in high-power advanced transistors

The replacement of SiO_2 with high- κ materials as the gate dielectrics in low-power MOSFET applications has allowed for the continuation of Moore's Law scaling and satisfied requirements for higher speed and lower power consumption. However, in the high-power application field, the development of Si-based MOSFETs has been constrained by the intrinsic material limits of silicon.

High-power operation typically generates a great deal of heat, which increases the temperature of the devices. The temperature limit of a Si p-n junction is 150°C [8]. If a Si-based MOSFET is operated above this temperature, it may lose functionality or suffer reliability issues. Moreover, a high electric breakdown field is also required by high-power devices. The electric breakdown field of Si is 250 kV/cm because of its small band gap of 1.12 eV [8]. To increase the electric breakdown field, a transistor with larger area is needed, which would lead to increased costs and reduced yield. Therefore, increasing the effectiveness of Si in MOSFET to satisfy the requirements for high-power application is not feasible.

Transistors based on wide-band-gap materials can be operated in high-temperature conditions and have high electric breakdown fields. Therefore, diamond, SiC, and GaN are under consideration to replace silicon in high-power electronic devices. Table 2.2 lists the physical characteristics of Si, diamond, SiC, and GaN.

Table 2.2. Physical characteristics of Si, SiC, GaN, and diamond [8].

Material properties	Various materials			
	Si	4H-SiC	GaN	Diamond
Band gap E_g at 300K (eV)	1.12	3.26	3.4	5.45
Dielectric constant κ	11.8	9.7	9	5.5
Breakdown field E_B (MV/cm)	0.25	3	4	10
High-field Peak velocity v_s (10^7 cm/s)	1	2	2.2	3
Electron mobility μ (cm^2/Vs)	1500	800	1350	2200
Hole mobility μ (cm^2/Vs)	600	102	850	850

Diamond has the best theoretical characteristics, as shown in Table 2.2. However, diamond is a hard material that requires a very high temperature for processing. The difficulties related to high-temperature processing have not yet been resolved. In addition, there is a lack of shallow n-type dopants for diamond [81]. As a result, for the time being, its immature fabrication process means that diamond is not suitable for power-device fabrication. SiC and GaN have comparable material properties, such as a large band gap and a high breakdown field. Because GaN based material has the ability to form a 2DEG channel by a heterojunction, this unique characteristic makes GaN superior to SiC. The

benefit of a 2DEG is its high electron mobility because ionized impurity scattering is reduced. This reduction is achieved by the separation of the channel electrons and dopants through the formation of a quantum well near the heterojunction interface. Electrons flow into the quantum well, which has a low energy potential, leaving ions behind in the bulk.

GaN-based HEMTs have been widely used in high-power devices and satellite communication for military and commercial purposes [82, 83]. However, surface-defect-related gate leakage currents and drain-current collapse occur at high frequency, and the intrinsically high leakage current of the Schottky gate degrades the performance of the traditional HEMT [12-14, 16, 17]. MIS-HEMTs could help to alleviate the above issues [9, 15, 18, 19] and are deemed the most promising next-generation high-power electronic devices. Moreover, they offer positive threshold voltages, low leakage currents, and excellent reliability [20, 21].

Lee et al. [21] have reported that a fully recessed AlGaN/GaN MOSFET with Al_2O_3 as the gate dielectric could have a subthreshold slop of 80 mV/decade, a high ON/OFF current ratio of $\sim 10^8$, and a breakdown voltage of 600 V. Tsai et al. [20], using a high- κ $\text{LaAlO}_3/\text{SiO}_2$ gate dielectric, have fabricated a recessed-gate GaN MOSFET that has a low V_{th} of 0.1 V and a high transconductance g_m of 136 mS/mm. This rapid progress in the implementation of high- κ gate stacks in GaN-based MIS-HEMTs has significantly improved the performance of high-power electronic devices.

2.3.1. Passivation of GaN surface states

A GaO_x layer can be readily grown on a GaN surface with a small amount of oxygen exposure [84]. Dong et al. [27] have reported that such a GaO_x layer with a disordered structure could introduce midgap electronic donor states, as determined via scanning tunneling microscopy and first-principles studies [17, 29]. These surface states exacerbate the gate leakage current and cause drain-current collapse in HEMTs [12, 16, 31].

In the past few years, various insulators have been tested for the passivation of the surface states, such as SiO_2 [85], Si_3N_4 [18, 86], ZrO_2 [14], HfO_2 [87], and Al_2O_3 [15, 88]. According to the current understanding, the passivation of surface states is achieved by decreasing the thickness of the GaO_x layer by means of a chemical reaction between the passivation material and the GaO_x [89, 90]. According to the Gibbs free energies, ZrO_2 (-1042 kJ/mol), HfO_2 (-1088 kJ/mol), and Al_2O_3 (-1582 kJ/mol) are more stable than Ga_2O_3 (-998 kJ/mol; represents GaO_x). Therefore, GaO_x may be reduced through reaction with metal precursors of the above three materials.

Hinkle et al. [90] have observed a significant reduction in the XPS intensity from Ga-O bonds after the deposition of 1 nm of Al_2O_3 or HfO_2 on GaAs, where Al_2O_3 has the more significant effect. Similarly, Prabhakaran et al. [91] have confirmed that the GaO_x on a GaN surface can also be reduced after reacting with Al. Maeda et al. [18] have proposed a bilayer method of surface passivation using two different high- κ materials. This method is motivated by the fact that an insulator on GaN acts not only as the

passivation layer but also as the gate dielectric in an MIS-HEMT. Therefore, it is necessary to balance the surface-passivation effect and the gate-dielectric capacitance.

Dong et al. [27] have proposed another approach to reducing the surface states by changing the GaO_x morphology via an elevated-temperature treatment. The disordered native GaO_x layer can thus be transformed into an ordered oxide with a stoichiometry and a structure similar to those of bulk Ga_2O_3 , thereby reducing the surface states. Bae et al. [92] have used a low-temperature treatment to enhance the quality of the GaO_x formed at the SiO_2/GaN interface and thus reduce the interface defect density, whereas Therrien et al. [93] have demonstrated a microscopic mechanism that can lower the defect density at the high- κ/GaN interface through the formation of a high-quality Ga_2O_3 layer during remote-plasma-assisted oxidation.

To date, the origin of the surface-state passivation has not yet been fully elucidated. A systematic study is needed to investigate the physical mechanism of this effect because it is crucial to improve the performance of GaN-based power devices.

2.3.2. The properties of the high- κ/GaN interface

GaN is a spontaneous-polarization material because the center of the distribution of positively charged atoms does not coincide with that of the negatively charged atoms in the structure [94]. Ambacher et al. [94] have reported that Ga-face GaN in the wurtzite structure possesses negative surface charges induced by this spontaneous polarization. These negative charges will be compensated by the substrate donor charges, leading to upward band bending at the GaN surface [95].

When a high- κ material has been deposited on GaN, an interfacial GaO_x layer readily forms because the GaN surface is highly reactive with oxygen [29, 96]. This GaO_x is believed to act as a key factor in determining the properties of the high- κ /GaN interface. The band offsets between SiO_2 and HfO_2 as well as Si_3N_4 and the GaN substrate have been investigated via XPS measurements to elucidate the interface properties [87, 97, 98]. Cook et al. [87, 97, 98] believe that an interface dipole induced by Ga-O bonds at the interface accounts for the band-offset variation. Similarly, Coan et al. [31] believe that the interfacial layer is the primary origin of the dipole formed at the gate-dielectric/GaN interface. However, the magnitude and direction of the interface dipole differ in similar XPS studies [31, 87].

Esposito et al. [99] have reported the detection of a fixed net positive charge at the Al_2O_3 /GaN interface by analyzing the V_{fb} shift of MOS capacitors. Ganguly et al. [32] have observed the same phenomenon at the Al_2O_3 /AlN interface. Therefore, the interface charge is also an interesting explanation of the interfacial properties [32, 99].

In summary, the physical origins of GaN surface passivation and the interfacial properties of surface-passivated GaN are not yet clear. Therefore, a systematic study of the high- κ /GaN interface is crucial for implementing GaN in high-power transistors.

2.4. Summary

Based on Moore's Law of scaling, the Si based transistor has realized the performance improvement and yield enhancement. However, the scaling of SiO_2 cannot go on forever, as the gate leakage reaches an unacceptable level.

Therefore high- κ materials are introduced to replace SiO_2 as the gate dielectric. After a series of requirements consideration, HfO_2 with excellent characteristics has been implemented into semiconductor industry. However, some processing, physics, and devices issues have not obtained a clear understanding.

In the high-power transistor field, the development of Si-based transistor has been constrained by the intrinsic material limits of silicon. GaN with large band gap and high breakdown field becomes attractive in replacing Si as the substrate. Whereas, understanding the surface passivation and interfacial properties need to take much effort.

Chapter 3   Characterization methods

3.1.   X-ray Photoelectron Spectroscopy

X-ray Photoelectron Spectroscopy (XPS), as a surface-analysis technique, can detect all elements in the periodic table, except H and He. Moreover, XPS can reach a depth of ~10 nm from the sample surface [100]. These capabilities enable XPS to obtain both elemental and chemical information from surfaces and underlying interfaces, such as the elemental composition, the chemical state, the valence-band maximum (VBM), and so on.

3.1.1.   Principles of XPS technique

In 1905, Einstein proposed the photoelectric effect to explain the photoelectrons that are emitted from a metal surface when it is irradiated with light. The photoelectric effect is the basic principle of XPS measurement.

As shown in Fig. 3.1, there are two types of electrons in an atom: core-level electrons and valence electrons. The core-level electrons are bound to the nucleus with an attraction energy, defined as BE, which can be used to define a specific element [101]. In XPS measurements, the Fermi energy level is usually calibrated to 0 eV. When an electron gains sufficient energy from the incident light, $h\nu$, it is ejected from the sample

with a certain kinetic energy (KE). Once the XPS detector determines the KE of the electron, the BE can be calculated using equation (3.1).

$$BE = h\nu - KE - \Phi \quad (3.1)$$

where BE and KE are the binding energy and kinetic energy of the photoelectron, respectively. $h\nu$ is the photon energy of the X-ray source, and Φ is the spectrometer work function. Al Ka (1486.6 eV) or Mg Ka (1253.6 eV) is often used as the photon energy of choice. Moreover, the BE calibration reference always uses surface adventitious carbon (C 1s, 285 eV) or a noble metal such as Au.

Figure 3.1. Schematic diagram of the atomic BE and the principle of XPS.

3.1.2. XPS application

3.1.2.1. Elemental composition

An XPS survey scan yields a series of peaks, which represent specific elements. Based on the particular peaks observed, the elemental composition of a sample can be determined. Figure 3.2 presents the XPS survey-scan spectrum of bulk SiO_2 , in which O $1s$, Si $2p$, and C $1s$ (adventitious carbon) peaks are observed. The areas below the peaks along with an appropriate sensitivity factor can be used to determine the stoichiometry of a sample.

Figure 3.2. XPS survey-scan spectrum of SiO_2 for the detection of the elemental composition.

3.1.2.2. BE variation

The XPS technique derives its chemical sensitivity from the fact that nearest-neighbor atoms have a direct effect upon the BE. To be specific, the BE is affected by the surroundings of a core electron, such as the chemical-bond type, the electric field, and photoemission differential charges. Therefore, a change in these surroundings can be reflected by a BE shift. For example, the Si 2*p* BE of bulk silicon is ~99.0 eV. When Si atoms are oxidized to form SiO₂, the Si 2*p* BE shifts to a larger value of 103.0 eV. This shift occurs because O is a highly electronegative element and the outer-shell electrons of Si are attracted by O, resulting in less electrostatic shielding of the core electrons. As a result, the attraction energy between the nucleus and the core electrons becomes stronger, leading to a larger BE. On the other hand, if Si forms a chemical bond with an atom that is less electronegative than Si, a smaller Si 2*p* BE will be obtained.

3.1.2.3. XPS peak splitting

An XPS peak always consists of several smaller peaks that represent different chemical states or chemical bonds. The extraction of an accurate BE value depends on the ability to perform proper peak splitting. In this thesis, the XPS spectra were curve-fitted with a combination of Gaussian and Lorentzian line shapes, using a Shirley-type background subtraction [102]. For instance, in the O 1*s* XPS spectrum of the HfO₂/SiO₂ structure, presented in Fig. 3.3, there are three chemical-bond peaks that overlap with each other. Gaussian-Lorentz curve fitting is used to split the combined peak into three separate chemical-bond peaks: Si-O, Hf-O-Si, and Hf-O.

Figure 3.3. Gaussian-Lorentz curve fitting is used to separate the chemical bonds in the $\text{HfO}_2/\text{SiO}_2$ structure.

3.1.2.4. VBM measurement

As shown in Fig. 3.1, there are two types of emitted photoelectrons, core-level electrons and valence-band electrons. Core-level electrons originate from the inner shell of the atom, whereas valence electrons with low BE values (<20 eV) originate from the valence band. The detection of valence electrons yields the valence-band spectrum, and the VBM can be obtained by extrapolating the leading edge of the valence-band spectrum to the baseline (the cross points in Fig. 3.4) from its specific spectrum [103]. In Fig. 3.4,

the valence-band spectrum of bulk HfO_2 is given, and it can be seen that the VBM is determined to be 2.7 eV using this method.

Figure 3.4. The VBM of bulk HfO_2 can be obtained by extrapolating the leading edge of the valence band spectrum to the baseline.

3.1.2.5. Band gap of oxides

The band gap of some oxides can also be obtained via XPS measurements. The core-level electrons emitted from a sample suffer inelastic losses because of single-particle excitations (which correspond to the acceleration of a single electron from the valence band to the conduction band, leaving a hole behind) [103, 104]. The onset of single-particle excitations causes the electrons from the core level to appear at an energy equal to the band gap E_g below the core level [103]. This phenomenon can be used to

determine E_g and is explained in the diagram presented in Fig. 3.5. The O 1s energy-loss spectrum of bulk HfO₂ is provided in Fig. 3.6. Using this method, E_g can be estimated to be 5.2 eV. This value is consistent with the value derived through optical measurement.

Figure 3.5. Schematic diagram illustrating the formation of the O 1s energy-loss spectrum.

Figure 3.6. An example demonstrating the measurement of the band gap of HfO₂ using the XPS O 1s energy-loss spectrum.

3.1.2.6. Valence-band offset

Once the VBM and E_g have been obtained, the valence-band offset (VBO) can be deduced [105]. There are two methods of obtaining the VBO. Using a SiO₂/Si structure as an example, the first method of obtaining the VBO is illustrated in Fig. 3.7. Once the VBMs of the Si bulk and the SiO₂ bulk have been determined, the VBO is equal to the difference between these two VBMs. This method is represented by equation (3.2). However, this method does not take an interface change into account when SiO₂ is deposited on Si substrate.

$$\Delta E_V = E_V^Y - E_V^X \quad (3.2)$$

where the subscript v denotes the VBM. X and Y represent the two contact materials.

Figure 3.7. The VBO between Si and SiO₂ obtained from the VBM spectra.

Another method, proposed by Kraut [105], does account for the change in the interface in the calculation. The VBO can be precisely obtained by equation (3.3).

$$\Delta E_V = (E_{CL}^Y - E_V^Y) - (E_{CL}^X - E_V^X) - (E_{CL}^Y(i) - E_{CL}^X(i)) \quad (3.3)$$

where the subscripts CL and v denote the BE for the “core level” and the VBM, respectively. The bulk and interface BEs are represented, respectively, by the notations (b) and (i). X and Y represent the two contacting materials.

3.1.2.7. The XPS measurement settings used in this thesis

XPS measurements were performed using a VG ESCALAB 200i-XL system equipped with a monochromatic Al K (1486.6 eV) X-ray source. All high-resolution spectra were collected in the constant-pass-energy mode with a pass energy of 20 eV. The BE calibration was effected using pure nickel (Ni), gold (Au), silver (Ag) and copper

(Cu) standard samples by setting the Ni Fermi edge, Au 4f_{7/2}, Ag 3d_{5/2} and Cu 2p_{3/2} peaks at BEs of 0.00 ± 0.02 eV, 83.98 ± 0.02 eV, 368.26 ± 0.02 eV and 932.67 ± 0.02 eV, respectively. All XPS spectra were curve-fitted with a combination of Gaussian and Lorentzian line shapes, using a Shirley-type background subtraction [102].

3.2. Keithley 4200

The MOS capacitors used in this thesis were fabricated in the NTU N2FC cleanrooms using a two-mask process. After the fabrication of the capacitors was completed, an electrical characterization measurement was performed using a Suss PM8 200-mm manual probe station and a Keithley 4200 Semiconductor Characterization System, which are shown in Fig. 3.8(a) and Fig. 3.8(b), respectively. The Suss PM8 200-mm manual probe station serves as a platform for all related electrical measurements, and its main components are a probe chamber, a microscope, a gas distribution panel, a vibration isolation table, a chuck, and platen controls.

(a)

(b)

Figure 3.8. (a) Suss PM8 200mm manual probe station and (b) Keithley 4200 Semiconductor Characterization System.

The Keithley 4200 Semiconductor Characterization System is the primary instrument used to perform all related electrical measurements. It consists of four highly accurate source-monitor units (SMUs) with a current resolution of 0.1 fA. These SMUs are individually connected to four probe heads placed on the Suss 200-mm manual wafer probe station via Kelvin tri-axial cables with low leakage currents. These probe heads are primarily used to hold steady the tungsten needles, which can individually connect to device terminals or to ground.

3.2.1. CV measurement using the Keithley 4200

The Keithley Model 4200-SCS is equipped with the 4200-CVU integrated CV option to enable CV measurements to allow a semiconductor device to be simply tested

and analyzed. Two simultaneous voltage sources are used to perform CV measurements on MOS capacitors, as illustrated in Fig. 3.9. A direct-current (DC) voltage V_{dc} that is swept as a function of time is used to detect substrate regions at various depths. An alternating-current (AC) voltage signal dV_{ac} of fixed magnitude and frequency applies a small-signal bias to the capacitor.

Figure 3.9. AC and DC voltage of the CV sweep measurement.

A CV measurement of a MOS capacitor with the TiN/HfO₂/P-Si substrate structure is presented in Fig. 3.10. Using the CV measurement results, the EOT and V_{fb} can be extracted using a quantum-mechanical C–V simulator [106]. The values of these quantities are found to be 2.4 nm and -0.06 V, respectively. Other electrical characteristics also can be obtained from the CV data, such as the bulk doping density and the interfacial charge density.

Figure 3.10. CV measurement of a capacitor with a TiN/HfO₂/P-Si substrate structure using the Keithley 4200.

3.3. Agilent B1500A

The Agilent B1500A, similar to the Keithley Model 4200, is a piece of electrical measurement equipment. The basic components are shown in Fig. 3.11: a semiconductor characterization system and two wave generators (one is for the gate voltage, and the other is for the substrate voltage). It can be used to perform current or voltage measurements at any point along a voltage pulse or arbitrarily generated voltage waveform, and the use of the B1500 is therefore preferred for the measurement of the transition state of a device, which has long been a highly desired measurement capability in many measurement applications.

Figure 3.11. Agilent B1500A Semiconductor Characterization System.

3.3.1. Pulsed CV measurements

The pulsed CV method was implemented using the Agilent B1530A WGFMU module in a B1500A semiconductor device analyzer. A pulsed CV measurement sequence on a capacitor (the same capacitor used in Fig. 3.10.) is provided in Fig. 3.12. After the application of a trapezoidal voltage waveform produced by the gate-voltage generator, a displacement current I_c flows through the capacitor. The gate voltage and I_c are detected by WGFMU CH1 and CH2, respectively. The capacitance is determined as follows:

$$C = -I_c \left(\frac{dV_g}{dt} \right) \quad (3.4)$$

where dV_g/dt is gate voltage ramp rate

Figure 3.12. The pulsed CV measurement sequence on a capacitor.

In this measurement, the gate-voltage waveform varies between -1 V and 1 V, and the pulse width and transition times are 80 μs and 10 μs , respectively. After a calculation using equation (3.4), the capacitance is extracted, as shown in Fig. 3.13. It is found that the capacitance is almost identical to the result measured using the Keithley 4200 (shown in Fig. 3.10), thereby confirming the accuracy of the pulsed CV measurement.

Figure 3.13. Pulsed CV measurement of a capacitor with a TiN/HfO₂/P-Si substrate structure using the Agilent B1500.

Chapter 4 Investigation of HfO₂ high- κ dielectrics electronic structure on SiO₂/Si substrate

4.1. Introduction

HfO₂-based high- κ dielectrics are currently being implemented in the manufacturing of advanced complementary metal oxide semiconductor (CMOS), and the industry is converging to the integration of HfO₂-based high- κ materials in a gate-dielectric-last manner for sub-28-nm technology nodes [4, 7, 63]. However, one of the major concerns for gate-dielectric-last devices is the reliability of the HfO₂ dielectrics because of their relatively low thermal budget. Three major reliability issues are listed here. First, Hf silicate and Hf silicide layers form at the HfO₂/SiO₂ interface because of an intermixing reaction between HfO₂ and SiO₂. The presence of these interfacial layers increases the EOT, reduces the gate-dielectric capacitance, and causes the gate current to deteriorate [69, 70, 107]. Second, V_{th} instability has been observed because of an internal electric field formed at the HfO₂/SiO₂ interface [79]. Both interfacial layers and internal electric field are observed at HfO₂/SiO₂ interfaces. However, the relation between them has not been studied clearly. Third, the impact of PDA on the V_{th} instability has not been investigated elaborately because of the lack of a link between the phase separation and

the internal electric field. To understand and resolve these issues, it is necessary to obtain a better understanding of the electronic structure of HfO₂ high- κ gate stacks.

In this chapter, HfO₂ layers with various thicknesses on SiO₂/Si substrates are investigated via XPS and the corresponding MOS capacitors. A thin layer of HfO₂ is fully consumed in the reaction with SiO₂ to form Hf silicate, whereas only part of a thick HfO₂ layer participates in this intermixing reaction. This is because the Hf-silicate-formation reaction can become saturated beyond a certain thickness of HfO₂. The Hf silicate layer is considered to be an important factor in generating V_o because the V_o formation energy is lower in this layer than in bulk HfO₂. Furthermore, V_o is believed to be generated at the Hf-silicate/SiO₂ interface because of the difference between the areal densities of oxygen in the two materials, which causes oxygen ions to diffuse from the Hf silicate to the SiO₂. An internal electric field is thus formed between the positively charged V_o and the negatively charged oxygen ions. A thicker Hf silicate layer can accommodate more V_o , thus leading to the formation of a stronger internal electric field. Because of this internal electric field, the O 1s, Si 2p and Hf 4f BEs shift to higher values as the thickness of the HfO₂ increases. The magnitude of the internal electric field can be determined via XPS BE measurements, which can be verified using the V_{fb} values obtained from the corresponding capacitors.

The thermal stability of an HfO₂-based gate stack is also characterized in this chapter. Four samples with identical HfO₂/SiO₂/Si gate structures that received PDA treatment at various temperatures were studied using XPS and the corresponding capacitors. It was found that the Hf-O-Si/Si-O bond-intensity ratio increases after annealing at 400 °C because the intermixing reaction is intensified. However, this ratio

begins to decrease when the PDA temperature is equal to or higher than 600 °C. This reduction of the ratio is ascribed to the phase separation in the Hf silicate layer, which is exacerbated by high-temperature annealing. Considering these findings, the intermixing reaction and phase separation are considered to be the primary causes of the variation in the internal electric field.

4.2. Investigation of electronic structures for HfO₂ with different thicknesses on SiO₂/Si substrate

4.2.1. Experimental details

After ~ 4.5 nm SiO₂ was thermally grown on a p-type Si wafer, different thicknesses of HfO₂ were deposited by ALD, followed by a PDA at 600 °C for 30 s in N₂. It is noted that SiO₂ interfacial layer was grown to mimic the actual device structure, which is generally needed for the sake of device mobility and reliability. Moreover, the thick SiO₂ layer was adopted to reduce the influence from the SiO₂/Si interface and the substrate injection [70]. The samples with 0, 0.5 and 4.0 nm thicknesses of HfO₂ were denoted as S1, S2 and S3, respectively, as shown in Fig. 4.1. The XPS were carried out for all the samples and the XPS spectra reported in this part were referenced to substrate Si 2*p* peak at BE of 99.0 eV. Moreover, the corresponding samples using the similar gate dielectrics were used for capacitor fabrication (C-S1, C-S2, and C-S3) with sputtered TiN (~100nm) as the gate electrode before receiving a forming gas anneal at 425 °C for 30

min.. Capacitance-voltage (CV) measurement on these capacitors was carried out using a Keithley 4200.

Figure 4.1. (a) Process flow for the fabrication XPS samples as well as capacitors and (b) schematic diagrams of the gate stacks for XPS samples S1 to S3 and capacitors C-S1 to C-S3.

4.2.2. Results and discussion

The XPS core-level spectra of O 1s, Si 2p and Hf 4f for all three samples are depicted in Fig. 4.2. For sample S2, two peaks can be fitted in the O 1s spectrum, which are assigned to Si-O and Hf-O-Si bonds respectively. The appearance of Hf-O-Si peak indicates the formation of hafnium silicate due to the interaction of HfO₂ and SiO₂ during

the annealing process. No peak corresponding to HfO₂ is observed owing to the complete intermixing of the 0.5 nm HfO₂ with SiO₂ [108]. For sample S3, three peaks can be identified, which correspond to the bonds of Si-O, Hf-O and Hf-O-Si, respectively [73]. Comparing samples S2 with S3, it can be concluded that a thicker Hf silicate can be formed after annealing with a thicker HfO₂ film. However in S3, the intermixing reaction does not consume the entire 4.0 nm HfO₂ layer (i.e. Hf silicate formation reaction can be saturated beyond a certain thickness of HfO₂) [108, 109]. It is also noticed that BE for O 1s shift to higher BE side with the increase of the HfO₂ deposition thickness.

Figure 4.2. The XPS O 1s (a), Si 2p (b), and Hf 4f (c) core-level spectra obtained from different samples. Gaussian curve fitting is used to analyze the O 1s and Si 2p spectra.

Si 2*p* spectra recorded from all three samples are displayed in Fig. 4.2(b). The lower BE peak is assigned to contributions of photoelectrons from the silicon substrate (denoted as Si 2*p*^{sub}) and the higher BE peak is attributed to the photoelectrons from SiO₂ and Hf silicate (denoted as Si 2*p*^{oxide}). For samples S2 and S3, both Si-O and Hf-Si-O bonds can be observed, which is consistent with O 1*s* spectra obtained from same samples. Again it is observed that Si 2*p*^{oxide} shifts to a higher BE with the increased thickness of HfO₂. For Hf 4*f* spectra in Fig. 4.2(c), sample S3 exhibits the same trend of BE shifts with respect to sample S2. The binding energies of the peaks are summarized in Table 4.1.

Table 4.1. Summary of the binding energies of O 1*s*, Si 2*p*^{oxide}, Si 2*p*^{sub}, and Hf 4*f* for different samples.

Sample NO.	HfO ₂ thickness (nm)	Binding Energy Peak (eV)					
		O 1 <i>s</i>			Si 2 <i>p</i> ^{oxide}		Hf 4 <i>f</i>
		Si-O	Hf-O-Si	Hf-O	Si-O	Hf-Si-O	Si2 <i>p</i> ^{sub} substrate
S1	0	532.7			103.3		99.0
S2	~0.5	532.7	531.1		103.4	102.4	99.0 17.3
S3	~4.0	533.1	531.8	531.3	103.9	103.3	99.0 17.8

To illustrate the data presented in Fig. 4.2 and Table 4.1, a model is schematically proposed in Fig. 4.3. Based on the information from Fig. 4.2, different thicknesses of HfO₂ can lead to the different gate dielectric structures as shown in Fig. 4.3(a). Namely, in sample S2, all 0.5 nm HfO₂ is fully reacted with SiO₂ to form Hf silicate. While in sample S3, only part of the 4.0 nm HfO₂ is involved in the intermixing reaction and a thicker Hf silicate layer is formed as compared to sample S2.

Figure 4.3 (a) A model to explain the electronic structure of HfO₂ deposited on SiO₂/Si substrate. The different gate dielectric structures and internal electric fields between SiO₂ and Hf silicate are formed due to different thicknesses of HfO₂ layers. (b) A schematic band alignment diagram of HfO₂/Hf-silicate/SiO₂/Si system and its relationship with XPS binding energies.

It was reported that the V_o formation energy in Hf-O-Si layer is lower than that in bulk HfO₂, and thus V_o tend to be formed in the Hf silicate layer rather than HfO₂ [110]. Further, it is believed V_o can be generated at the interface between SiO₂ and Hf silicate owing to their oxygen areal density difference (i.e. oxygen ions can penetrate into the SiO₂ layer, creating V_o in Hf silicate) [26, 62, 110]. Considering these, Hf silicate layer plays a critical role in explaining the XPS data. In Fig. 4.3(a), sample S3 can accommodate more V_o due to the thicker Hf silicate layer. Furthermore, V_o is regarded as positively charged while oxygen ion is negatively charged [6, 111]. An internal electric field can thus be built between V_o and oxygen ions [6, 26, 78, 111], leading to the corresponding band bending. A stronger internal electric field can be expected with larger density of V_o in S3 with respect to S2 as is shown in Fig. 4.3(a).

The corresponding energy band diagram for sample S3 is given in Fig. 4.3(b). The Fermi energy level of silicon substrate is calibrated as 0 eV during XPS measurement. Owing to the internal electric field between SiO₂ and Hf silicate, the Fermi energy level would be shifted down in Hf silicate layer (and thus HfO₂ layer), that will lead to the increase of the measured XPS BE [112]. Note that with the stronger internal electric field, a larger shift of the XPS BE is observed. However, it is noted that the model cannot explain BE variation for Si-O bonds quantitatively. This BE variation should be caused by photoemission differential charging in SiO₂ and HfO₂ layers. The magnitude of the differential charging effect can be obtained by comparing BE values (for Si-O bond) of samples S2, S3 with sample S1. Using Si 2p (from bond Si-O) as the reference, 0.1 eV and 0.6 eV shifts to a higher BE are observed for samples S2 and S3 respectively. For Hf 4f, the BE shift is a combinative effect of internal electric field and

the differential charging. The magnitude of BE variation can be obtained by comparing BE values obtained from references of the Si 2*p* peak (at BE of 99.0 eV) to BE values obtained from the C 1*s* peak (at BE of 285.0 eV). The values are 0.2 eV and 1.0 eV for samples S2 and S3 respectively. As a result, the internal electric field can be calculated to be 0.1 eV and 0.4 eV for samples S2 and S3 respectively.

Figure 4.4. The corresponding capacitors' data in term of their EOT and the V_{fb} are compared.

Fig. 4.4 summarizes the corresponding capacitors data in terms of their EOT and the V_{fb} . The EOT variation is consistent with Hf silicate formation, which also confirms the appearance for bond Hf-O-Si in O 1*s* and Si 2*p* spectra [109]. Moreover, V_{fb} shifts to the positive voltage side continually with increasing HfO₂ due to the stronger internal

electric field. This observation supports our proposed model in Fig. 4.3(a) and the magnitude (0.1 eV and 0.4 eV for samples S2 and S3, respectively) agrees with the predictions from the calculated internal field values.

4.2.3. Conclusion

In conclusion, the electronic structure of ALD HfO₂ on the SiO₂/Si is investigated by XPS. The Hf silicate that is formed between HfO₂ and SiO₂ plays a key role in V_o generation/accumulation and thus the build-up of an internal electric field. The internal electric field formation at the interface of SiO₂ and Hf silicate and photoemission differential charging can explain the XPS BE changes of O 1s, Si 2p and Hf 4f spectra with the increase of the thickness of HfO₂.

4.3. Thermal stability of the HfO₂/SiO₂/Si structure

4.3.1. Experimental details

After ~ 4.0 nm of SiO₂ was thermally grown on a p-type Si wafer, ~ 3.0 nm of HfO₂ was deposited via ALD, followed by PDA at various temperatures for 30 s in N₂. A sample without HfO₂ deposition (the SiO₂/Si structure alone) and an as-deposited sample were prepared for comparison; these samples are denoted by S1 and S2, respectively. The samples annealed at 400 °C, 600 °C, and 800 °C are labeled as S3, S4, and S5, respectively. The gate-dielectric structures for samples S1-S5 are presented in Fig. 4.5. XPS measurements were performed for all samples. To reduce the influence of the

internal electric field on the chemistry study of the interfacial layer, Hf 4*f* XPS spectra were referenced to C 1*s* at a BE of 285.0 eV, whereas Si 2*p* spectra reported here were referenced to Si 2*p* at a BE of 99.0 eV. Moreover, corresponding samples using the similar gate dielectrics to those of the XPS samples were used for capacitor fabrication (C-S1, C-S2, C-S3, C-S4, and C-S5) using sputtered TiN (~100 nm) as the gate electrode. CV measurements on these capacitors were conducted using a Keithley 4200.

Figure 4.5. (a) Process flow for the fabrication XPS samples as well as capacitors and (b) schematic diagrams of the gate stacks for XPS samples S1 to S5 and capacitors C-S1 to C-S5.

4.3.2. Results and discussion

The XPS core-level spectra of Hf 4f for samples S2 to S5 are presented in Fig. 4.6(a). For sample S2, Hf-Si-O bond is observed in sample S2, implying the occurrence of Hf-silicate formation during ALD deposition. The Hf-Si-O/Hf-O peak-intensity ratio is 0.03. There is an obvious small peak (at 14.9 eV) that is assigned to the Hf-Si bond, indicating the formation of Hf silicide [113]. This peak disappears after PDA because the Hf-Si bond is transformed into the Hf-Si-O bond. For sample S3, a thicker Hf silicate layer formed because of the intensification of the intermixing reaction between HfO₂ and SiO₂ after PDA at 400 °C [69], resulting in a larger Hf-Si-O/Hf-O ratio of 0.14. However, this ratio decreases to 0.08 in sample S4 after a 600 °C annealing. Interestingly, sample S5 follows the trend of sample S4, and the ratio becomes even smaller after PDA at 800 °C. In addition, it is found that the Hf 4f BE of Hf-Si-O bonds varies as a function of the ratio, shown in Table 4.2.

The Si 2p spectra recorded for all samples are displayed in Fig. 4.6(b). The lower BE peak is assigned to photoelectrons from the silicon substrate (denoted as Si 2p^{sub}) and is set to 99.0 eV as a reference, and the higher BE peak is attributed to the photoelectrons from SiO₂ and Hf silicate (denoted as Si 2p^{oxide}). For sample S1, the Si-O peak from the SiO₂ layer is located at 103.0 eV. After HfO₂ deposition, both Si-O and Hf-Si-O bonds from the Si 2p^{oxide} peak can be observed for samples S2 to S5 because of the formation of Hf silicate [77]. For sample S2, the peak at 103.2 eV is assigned to the Hf-Si-O bond, and the peak at 103.9 eV is ascribed to the Si-O bond. The Hf-Si-O/Si-O bond-intensity ratio is 0.8. When sample S2 is compared with S1, a significant BE increase is detected

because of the formation of Hf silicide. The Hf-Si bonds of this layer are predicted to be positively charged shallow traps. These positive charges bend the energy band downward and result in a large BE [110]. The Hf-Si bond is combined into the Si $2p^{\text{sub}}$ peak, and its contribution is too small to be extracted. For sample S3, the ratio is larger than that of sample S2, indicating the formation of a thicker Hf silicate layer. The observed decrease in the Si $2p^{\text{oxide}}$ BE is attributable to the elimination of the Hf silicide layer and the formation of a thicker Hf silicate layer (i.e., the Si $2p$ signal from the Hf-Si-O bond has a smaller BE when the HfO₂ mole fraction in Hf silicate layer is increased due to intermixing reaction [77]) after the annealing process. However, for sample S4, the Hf-Si-O/Si-O ratio shifts to a smaller value than that for S3. This observation indicates that the thickness of the Hf silicate layer is reduced after annealing at 600 °C. For sample S5, the Hf-Si-O/Si-O ratio is the smallest among all the samples, and the BE of the Si-O bond is the same as that of sample S1. It is noticed that the Hf-Si-O/Si-O ratio varies consistently with Hf-Si-O/Hf-O ratio. The binding energies of all peaks are summarized in Table 4.2.

Figure 4.6 The XPS Hf 4*f* (a) and Si 2*p* (b) core-level spectra obtained for the various samples. The Hf 4*f* XPS spectra are referenced to the C 1*s* BE of 285.0 eV, whereas the Si 2*p* spectra reported here are referenced to the substrate Si 2*p* peak at a BE of 99.0 eV for convenience of analysis.

Table 4.2 Summary of the BEs of Si 2*p*^{sub}, Si 2*p*^{oxide}, and Hf 4*f*, the ratios of Hf-Si-O/Si-O and Hf-Si-O/Hf-O, and the magnitudes of the internal electric fields for different samples.

Sample No.	PDA temperature(℃)	Binding Energy (eV)								Internal Electric Field (V)
		Aligned to Si 2 <i>p</i>					Aligned to C 1s			
		Si 2 <i>p</i> ^{Sub}		Si 2 <i>p</i> ^{oxide}		Hf 4 <i>f</i>				
		substrate	Si -O	Hf-Si-O	Hf-Si-O/Si-O ratio	Hf -O	Hf-Si-O	Hf-Si-O/Hf-O ratio	Hf-Si	
S1	\	99	103	\	\				\	\
S2	as-dep	99	103.9	103.2	0.8	16.7	17.1	0.03	14.9	0
S3	400	99	102.8	101.9	2.4	16.7	17.8	0.14		1
S4	600	99	102.6	101.7	1.1	16.7	17.5	0.08		0.4
S5	800	99	103	102.3	0.3	16.7				-0.3

According to section 4.2, the Hf silicate plays a key role in generating an internal electric field at the interface between the SiO₂ and the Hf silicate. The magnitude of this electric field was obtained for all samples using the method proposed in section 4.2 [25]. Using sample S1 as the reference, the variations in the internal electric fields of samples S2 to S5 are presented in Fig. 4.7. It is found that the magnitude of the electric field varies consistently with the XPS intensity of Hf silicate layer. It is because a thicker Hf silicate layer could accommodate more V_o [25]. In addition, V_{fb} values of the corresponding capacitors with similar gate stacks to the XPS samples are also presented in Fig. 4.7 for comparison. Each value is an average of ten test devices. The trend in V_{fb} is similar to that of the internal electric fields of the corresponding XPS samples. The discrepancy between the two sets of samples (i.e., the XPS samples and the capacitors) may be attributable to the XPS resolution limit and variations in the thicknesses of the gate stacks between the corresponding samples.

Figure 4.7. Comparison of the internal electric fields obtained from the XPS results and the corresponding capacitors.

Figure 4.8. I_g - V_g curves for capacitors C-S1 to C-S5, with an area $100 \mu\text{m} \times 100 \mu\text{m}$.

Moreover, the I_g - V_g curves for capacitors C-S1 to C-S5 are presented in Fig. 4.8. After the deposition of 3 nm HfO₂, the breakdown voltage becomes larger while the leakage current becomes smaller after a comparison between samples C-S1 and C-S2. After receiving a PDA at 400 °C, there is a significant increase in the breakdown voltage and a decrease in leakage current as compared to sample C-S2. However, the breakdown voltage begins to decrease when the PDA is over 600 °C.

The above experimental results can be explained by considering the various PDA treatments that lead to different gate-dielectric structures. Schematic illustrations of the electronic structures of the HfO₂/SiO₂/Si gate stacks are presented in Fig. 4.9. During the initial stage of HfO₂ deposition, the Hf precursor reacts with the SiO₂ substrate to form a thin Hf silicide layer (in samples S2 and C-S2) and a Hf silicate layer. This Hf silicide layer is located at the Hf silicate/SiO₂ interface, and the Hf-Si bonds are expected to constitute positively charged defects [110]. These positive charges bend the energy bands downward, as shown in Fig. 4.9; therefore, S2 has a larger Si 2p^{oxide} BE than that of S1. Hf silicide is a metallic material that can reduce the internal electric field between the Hf silicate and the SiO₂ layer. This effect is confirmed by the similar V_{fb} values of capacitors C-S1 and C-S2, as shown in Fig. 4.7 [25]. After PDA at 400 °C (in S3), the Hf silicide disappears as a result of being transformed into Hf silicate, as indicated by the fact that the peak assigned to the Hf-Si bond cannot be observed in the Hf 4f spectrum. Moreover, the reaction between HfO₂ and SiO₂ is intensified, leading to the formation of a thicker Hf silicate layer, as indicated the large ratios in the Hf 4f and Si 2p spectra. This thick Hf silicate layer gives rise to a large internal electric field in sample S3, as shown in Fig. 4.7. In this thicker Hf silicate layer, a Hf (Si) atom is bonded with more Si (Hf) atoms,

resulting in a larger (smaller) BE [77]. In addition, according to I_g - V_g curves shown Fig. 4.8, capacitor C-S3 has the best device due to the quality of the gate stack is improved after annealed at 400 °C. When the PDA temperature is increased to 600 °C, crystallization/phase separation introduces small HfO₂ and SiO₂ grains (small crystal structures) into the hafnium silicate layer in this material system, as schematically depicted in Fig. 4.9 [77, 114]. As a result, the Hf-Si-O bonds are decomposed into Hf-O and Si-O bonds, leading to a smaller Hf-Si-O/Si-O ratio and a smaller internal electric field. The particularly sharp Hf 4f peak and the similar BE value to that of bulk HfO₂ prove that the Hf-Si-O bond intensity is reduced significantly because of the phase separation. Moreover, the breakdown voltage starts to decrease. When the PDA temperature is increased to 800 °C, the phase separation becomes even more obvious, as indicated by the very small Hf-Si-O/Si-O ratio and internal electric field. The variation in the BE and the Hf-Si-O/Si-O ratio are attributed to the intermixing reaction and the phase separation.

Figure 4.9 A schematic model of the electronic structures of HfO₂ deposited on the SiO₂/Si substrates. Different PDA processing temperatures lead to different gate-dielectric structures and different internal electric fields.

4.3.3. Conclusion

In conclusion, the electronic structures of HfO₂/SiO₂/Si gate stacks after different PDA treatments were investigated via XPS and the corresponding MOS capacitors. PDA processing at 400 °C can enhance the formation of Hf silicate by causing an intermixing reaction of HfO₂ and SiO₂, whereas at high temperatures (above 600 °C), PDA processing also triggers phase separation. This phase separation results in the decomposition of Hf silicate. Fluctuations in the Hf silicate layer lead to variations in the internal electric field and BEs.

4.4. Summary

A systematic study of the electronic structures of HfO₂ on SiO₂/Si substrates is presented in this chapter. It is found that the Hf silicate that forms at the HfO₂/SiO₂ interface plays a key role in generating an internal electric field. This field generation is ascribed to the generation of V_o in this layer by virtue of the low V_o formation energy of the Hf-O-Si bond. Moreover, the resultant oxygen ions diffuse from the Hf silicate layer to the SiO₂ layer because of the difference in the areal density of oxygen between the two materials. Thus, an internal electric field is formed between the positively charged V_o and the negatively charged oxygen ions. A stronger internal electric field arises when a thicker Hf silicate layer is formed because a thicker Hf silicate layer can accommodate more V_o . Further, an investigation of the thermal stability of the HfO₂-based gate stacks and the corresponding internal electric fields is also presented. It is found that the

intermixing reaction is intensified by relatively low-temperature (400 °C) annealing, resulting in the formation of a thicker Hf silicate layer. However, phase separation is observed in this layer following high-temperature (above 600 °C) annealing. The decomposition of the Hf silicate results in a decrease in the internal electric field. The variation in the internal electric field is confirmed by the V_{fb} values measured for the corresponding MOS capacitors.

Chapter 5   Investigation of the interface dipole in HfO₂ based gate stack

5.1. Introduction

High- κ /metal gate-stacks are expected to be widely used in sub-28-nm CMOS manufacturing due to the severe limitations of the traditional polysilicon/oxy-nitride gate stack. Although significant process improvements have been made, a basic challenge still lies in the inherently high density of the as-grown oxide defects that lead to V_{th} instability when charged during operation [115-118]. To characterize the effect of charge trapping/detrapping at oxide defects, fast measurement techniques such as the pulsed current–voltage [119-121] and capacitance–voltage (CV) [122, 123] have been recently developed. These measurement methods can obtain a complete characteristic through CV measurement in a relatively short time, as opposed to the high-frequency (HF) CV measurement.

In this chapter of our study on the TiN/HfO₂ gate-stack using the pulsed CV method [122, 123], we came upon a capacitance hysteresis effect that could not be explained in terms of oxide charge trapping/detrapping. Relative positions of the CV curves derived from bidirectional fast voltage-ramp are found to be opposite to those obtained using the quasi-static voltage sweep method [115]. This means that the two sets of CV data could not be reconciled based on the same oxide charge trapping explanation.

The lack of any role of oxide charge trapping is also manifested by the fact that the hysteresis is independent of the voltage-pulse width (which equals the time allowed for charge trapping/detrapping to take place). On the other hand, the hysteresis is found to vary sensitively with the voltage-ramp rate—a larger hysteresis is observed under a faster voltage ramp. This result suggests that the hysteresis is a transient effect arising from a delayed system response to a fast-changing voltage input. An explanation based on interface dipole relaxation is shown to be able to describe most features of the experimental results.

5.2. Experimental details

P-type Si MOS capacitors with different gate dielectrics were fabricated. Capacitor A has a 3.2-nm SiO₂, grown by rapid thermal oxidation. Capacitor B has a 4.1-nm HfO₂, formed directly on the Si substrate via ALD. Capacitors C and D each has a bi-layer dielectric stack. In the former, the dielectric stack comprises a 1-nm Al₂O₃ on top of a 4.1-nm HfO₂. In the latter, the dielectric stack is made up of a 4.1-nm HfO₂ on top of a 1-nm Al₂O₃. After gate dielectric deposition, all samples received a 600 °C annealing for 30 s in nitrogen. The samples were then capped with a ~ 100 nm TiN gate electrode before receiving a forming gas anneal at 425 °C for 30 min. N-type capacitors (capacitor E) with a 3-nm HfO₂ on top of a 1.5-nm SiO₂ (intentionally grown prior to the HfO₂ deposition) and p-type MOS capacitors with a thicker (13.6 nm) HfO₂ (capacitor F) were also fabricated and measured. The gate stacks for all the capacitors are shown in Fig. 5.1.

Figure 5.1 (a) Process flow and (b) schematic diagram of the gate stacks for capacitors A-F.

HF CV measurement was performed via the CVU module in a Keithley SCS4200 semiconductor characterization system. The frequency of the small signal was 1 MHz and the small-signal amplitude was 50 mV. The measured CV curves were corrected for the substrate series resistance effect [124]. The pulse CV method was implemented via the Agilent B1530A WGF MU module in a B1500A-semiconductor device analyzer.

Trapezoidal gate voltage V_g pulses of varying widths and transition times (t_r) were realized with the arbitrary waveform generator. The default t_r was 20 μs , unless stated otherwise. The capacitance is determined using equation (3.4).

Fig. 5.2 shows an example of a series of trapezoidal V_g pulses of varying widths and the corresponding I_c measured at the transition edges. The pulsed CV curves presented later are each the average of 10 test devices. All measurements were made at 300 K.

Figure 5.2. A series of gate voltage waveforms of varying widths applied on capacitor B and the associated displacement currents at the transition edges. All devices measured have an area $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$.

5.3. Results and discussion

5.3.1. High-frequency CV measurement results

The EOT, V_{fb} , and the mid-gap interface-state density D_{it} of capacitors A–D are summarized in Table 5.1. The former two were extracted from the HF CV curve, by a quantum-mechanical CV simulator [106]. The mid-gap D_{it} was obtained via the conductance method [124].

Table 5.1. EOT, V_{fb} , and D_{it} of test devices

Capacitor	Gate Stack	EOT (nm)	V_{fb} (V)	D_{it} (cm ⁻² eV ⁻¹)
A	SiO ₂	3.2	-0.34	1.12 x 10 ¹¹
B	HfO ₂	2.4	-0.064	2.87 x 10 ¹¹
C	Al ₂ O ₃ /HfO ₂	2.6	0.057	3.03 x 10 ¹¹
D	HfO ₂ /Al ₂ O ₃	2.8	0.23	1.14 x 10 ¹¹

Fig. 5.3(a) and (b) depict the HF CV curves of capacitors A and B, respectively. A hysteresis can be observed between the forward ($V_{low} = -1\text{V} \rightarrow V_{hi} = +1\text{V}$; curve F) and reverse ($V_{hi} = +1\text{V} \rightarrow V_{low} = -1\text{V}$; curve R) CV curves (inset 1 and 2). It should be noted that curve F is constantly situated to the left of curve R, i.e. the former always has a more negative V_{fb} . When the p-Si is biased in accumulation, holes are captured by the oxide traps, charging them up positively. As a consequence, curve F registers a more negative V_{fb} during the forward sweep. On the other hand, electrons are captured by the oxide traps when the p-Si is biased in inversion. Thus, curve R registers a more positive V_{fb} during

the reverse sweep. The same results are obtained by beginning the measurement at $V_g = V_{hi} = 1$ V and sweeping toward $V_{low} = -1$ V and then back to $V_{hi} = 1$ V.

Figure 5.3. Forward F ($V_{low} = -1$ V $\rightarrow$ $V_{hi} = 1$ V) and reverse R ($V_{hi} = 1$ V $\rightarrow$ $V_{low} = -1$ V) HF CV curves of (a) Capacitor A (SiO₂) and (b) capacitor B (HfO₂). Inset 1 and 2 are magnified views, showing the relative shift of the two curves.

When the duration for which the device is biased in accumulation or inversion is lengthened (by decreasing the V_g step size), a larger relative shift between curves F and R is observed (Fig. 5.4). This observation is consistent with the role of oxide charge trapping. A longer time in the accumulation or inversion regime enables a greater number of oxide traps to be charged up, thus resulting in a larger hysteresis.

Figure 5.4. The hysteresis comparison between two measurement steps is shown for capacitors A and B. It shows that the hysteresis is increased for a smaller voltage step.

5.3.2. Pulsed CV measurement results

Fig. 5.5(a) and (b) show the pulsed CV curves of capacitors A and B, respectively. A few salient differences as compared to Fig. 5.3(a) and (b) should be highlighted. (Another salient feature is the “capacitance hump” in curve R. A similar observation is reported in [122] and [123]. When the capacitor is switched rapidly from inversion to accumulation, the p–n junction formed between the channel and substrate is forward biased. The injection and subsequent recombination of the channel carriers with majority carriers in the substrate produce an additional current superimposed on the displacement current, distorting the CV curve near the weak inversion regime. As this part is not focused on this feature, it will not be discussed further.) The part of curve R near V_{fb} is negatively shifted with respect to curve F. The relative shift between curves F and R (i.e. the hysteresis) is unaffected by a wide variation (five orders of magnitude) of the pulse width. Similar observations apply to capacitors C and D, shown in Fig. 5.6(a) and (b), respectively, as well as to an n-Si capacitor (capacitor E, with a HfO₂/SiO₂ gate-stack) shown in Fig. 5.7(a).

These features of the pulsed CV curves are unlike those of the HF CV curves [Fig. 5.3(a) and (b)], where curve R is shifted toward more positive V_g relative to curve F and the extent of relative shift between curves F and R is increased when a slower sweep is used. The opposite relative shift between curves F and R and the apparent lack of dependence of the hysteresis on pulse width imply that oxide charge trapping is not responsible for the hysteresis seen in the pulsed CV curves.

Figure 5.5. Forward and reverse pulsed CV curves of (a) capacitor A (SiO₂) and (b) capacitor B (HfO₂), obtained using the gate voltage waveforms shown in Fig. 5.2. The pulse width was varied from 10 μ s to 1 s.

Figure 5.6. Forward and reverse pulsed CV curves of (a) capacitor C (Al₂O₃/HfO₂) and (b) capacitor D (HfO₂/Al₂O₃).

Figure 5.7. (a) Forward and reverse pulsed CV curves of capacitor E. $V_{low} = -1$ V; $V_{hi} = +1$ V. (b) Forward and reverse pulsed CV curves of capacitor B (HfO₂). The V_{low} was fixed at -1 V in both cases but the V_{hi} was varied.

Additional experimental evidence that supports this inference is shown in Fig. 5.7(b). In both measurements, the bidirectional voltage ramp began at the same V_{low} ($=-1$ V) but ended at different V_{hi} (0 and +0.5 V). For $V_{hi} = 0$ V, the capacitor was biased in depletion, whereas for $V_{hi} = +0.5$ V, the capacitance reached a plateau, indicating that inversion had occurred. The different Si surface conditions and the oxide fields are expected to impact oxide charge trapping during the time when the voltage was at V_{hi} and thus cause curve R in each case to be shifted differently from curve F. However, the hysteresis is almost identical in both cases.

The effect of a varying t_r on the pulsed CV hysteresis is also examined, as shown in Fig. 5.8. Unlike previous results where a five order-of-magnitude variation of the pulse width produces no apparent impact on the hysteresis, a factor of two variation of t_r yields an obvious change. A shorter t_r (or faster transition rate) gives rise to a larger hysteresis and vice versa. This observation implies that the hysteresis is a transient effect due to the inability of the dielectric stack to respond to a rapidly changing oxide field. When t_r is increased to 200 μ s, curves F and R become almost indistinguishable (near V_{fb}), indicating that the response time of the dielectric stack is of the order of $\sim 10^{-4}$ s. This relatively long response time rules out the role of bulk ionic and electronic polarizations, which have response time of the order of picoseconds or shorter. It is thus believed that interface polarization, which generally dominates low-frequency dielectric response, is responsible for the observed pulsed CV hysteresis.

Figure 5.8. Forward and reverse pulsed CV curves of capacitor B (HfO₂) as a function of the pulse transition time. The pulse width was fixed at 80 μ s.

5.3.3. Interface dipole relaxation model

The impact of high- κ /SiO_x interface dipoles on V_{fb} shift has been recently discussed [23, 24, 80, 125]. Several explanations for interface dipole formation have been proposed. Some authors attributed interface dipole formation to the presence of a Hf silicate layer at the HfO₂/SiO_x interface [25]. The V_o formation energy in the Hf silicate is reported to be lower than that in the HfO₂ [110]. Thus, preferential formation of V_o in the Hf silicate results in dipole generation at the HfO₂/SiO_x interface. Kita and Toriumi [26] attributed interface dipole formation to the intrinsic difference in the areal density of

oxygen between the HfO₂ and SiO_x layers. As a result, diffusion of oxygen across the HfO₂/SiO_x interface occurs, giving rise to interface dipoles. This model could satisfactorily explain the magnitude and polarity of V_{fb} shift in most high- κ /metal gate-stacks reported so far. To date, however, the effect of high- κ /SiO_x interface dipoles on V_{fb} has mostly been treated in a static manner.

Figure 5.9. Schematic diagrams of the HfO₂/SiO_x gate stack showing the separation of an interface dipole at a given gate voltage [26]. For simplicity, the dipole moment is assumed to be perpendicular to the interface but the conclusion applies to dipoles of any orientation. (a) During quasi-static voltage sweep, the dipole can exactly follow the change in the oxide field and thus the separation d_0 is the same in either direction of the voltage sweep. During a fast voltage sweep, however, a lag in the dipole separation occurs, giving (b) a larger separation d' for a negative to positive sweep and (c) a smaller separation d'' for a positive to negative sweep.

An HfO₂/SiO_x interface dipole model for the pulsed CV hysteresis is shown in Fig. 5.9. Based on Kita and Toriumi [26], the positive (negative) end of the dipole is located in the HfO₂ (SiO_x). (This dipole orientation is assumed for the simplicity of discussion. As will be explained later, the relative positions of the pulsed CV curves F and R (Figs. 5.5–5.8) are independent of the dipole orientation.) Because the areal density of O atoms at the HfO₂ interface is larger than that of the SiO_x, a net transfer of O atoms to the SiO_x occurs, giving rise to dipoles with the positive (negative) end situated in the HfO₂ (SiO_x).

When V_g is negative (-1 V), the oxide field stretches the dipole apart, to a distance of d' . If V_g is now “swept” rapidly towards the positive regime to a new value V_g^* , the dipole may not be able to fully respond to the changing oxide field, i.e. the dipole spacing remains at $\sim d'$ for some time even after V_g has changed to V_g^* . Due to this larger dipole spacing (than the equilibrium value), which now places the negative end closer to and the positive end further from the Si substrate, curve F would register a positive shift in V_{fb} relative to the quasi-static case. This V_{fb} shift or $\delta V_{fb}'$ is given by $Q \times (d' - d_0)/\epsilon$, where Q is dipole charge per unit area, ϵ is permittivity of the HfO₂/SiO_x interface region, and d_0 ($< d'$) is equilibrium dipole spacing at V_g^* . On the other hand, the dipole spacing is reduced to d'' under a positive V_g ($+1$ V). Similarly, if V_g is now swept rapidly towards the negative regime to the new value of V_g^* , the dipole spacing may remain at $\sim d''$ ($< d_0$) due to the lag in dipole response. As a result, the V_{fb} of curve R would be shifted negatively with respect to that of the quasi-static case, i.e. $\delta V_{fb}'' = Q \times (d'' - d_0)/\epsilon$. The total hysteresis is thus given by $\Delta V_{fb} = Q \times (d' - d'')/\epsilon \propto Q \times \Delta d$.

In the above discussion, we have assumed that the dipole moment is directed towards the gate. It should be mentioned that the orientation of the dipole does not affect the relative positions of curves F and R, although it has an impact on the exact value of V_{fb} . If the dipole moment in Fig. 5.9 is reversed, the same relative shift of the two curves would also be observed. In this case, even though the dipole spacing $d' < d_0$ under a negative V_g , the reduced spacing would result in the positive end being situated further from and the negative end closer to the Si substrate. Therefore, curve F would still exhibit a positive V_{fb} shift relative to the quasi-static case. Conversely, V_{fb} would be shifted negatively under the reverse V_g ramp. This explains the pulsed CV hysteresis result of capacitor A with a SiO₂ gate oxide (Fig. 5.5(a)). Although the dipole moment at the SiO₂/Si interface is opposite to that of the HfO₂/Si interface [126, 127], the same relative shift between curves F and R is observed.

An approximate analytical expression for ΔV_{fb} in terms of the rigidity of the interface dipole and the voltage ramp rate may be obtained by considering the “ball and spring” representation shown in Fig. 5.10. The balls denote atoms which form the positive and negative ends of the interface dipole. Electrostatic interaction between the positive and negative poles is represented by the spring. When the distance between the two poles is larger than the equilibrium separation d_0 , the spring exerts an attractive (restoring) force F_s which attempt to bring the two poles closer to one another [Fig. 5.10(a)]. Conversely, the spring exerts a repulsive force F_s that tends to bring the two poles further apart when the interspacing is less than d_0 [Fig. 5.10(b)].

Figure 5.10. “Ball and spring” representation of the HfO₂/SiO_x interface dipole. Also shown are the electrostatic force (F_e) due to the applied oxide field, the restoring force (F_s) on the dipole due to displacement from the equilibrium position ($x = d_0$), and the “frictional” force (F_c) arising from the “viscosity” of the surrounding network. (a) depicts the lag in dipole response when V_g is ramped from -1 V to 1 V while (b) shows the corresponding lag under a reverse ramp (i.e. 1 V to -1 V).

For simplicity, the negative pole is assumed to be fixed and only the positive pole moves in response to the applied V_g ramp. The electrostatic force exerted by the applied oxide field may be expressed as

$$F_e = E_{ox} \times q_d = -\left(\frac{V_{g0} \pm s \times t}{T_{ox}}\right) \times q_d \quad (5.1)$$

where E_{ox} is oxide electrical field, q_d is dipole charge, V_{g0} is gate voltage prior to the start of the ramp, s is ramp rate, t is time after the start of the ramp, and T_{ox} is gate oxide thickness. The ‘+’ (‘-’) sign applies for the positive ramp. The ‘+’ (‘-’) sign applies for the positive (negative) ramp. The restoring force F_s on the positive pole, due to displacement x from the equilibrium separation d_0 , may be expressed using Hooke’s law as

$$F_s = k_s \times x \quad (5.2)$$

where k_s is a spring constant—a measure of the elasticity of the chemical bond between the positive and negative poles. As the dipole respond to the changing oxide field, it also experiences a “frictional” force (exerted by surrounding atoms) which may be expressed as

$$F_c = -c \times \frac{dx}{dt} \quad (5.3)$$

where c is a constant denoting the “viscosity” of the local oxide network. Considering the net force ($F_e + F_s + F_c$) and applying Newton’s second law on the positive end of the dipole of mass m yields a second-order time differential equation in x whose solution is of the form

$$x = A \times e^{-\frac{c \times t}{2m}} \times \sin \left(t \times \sqrt{\frac{k_s}{m} \left(1 - \frac{c^2}{4k_s \times m} \right)} + \phi \right) - \frac{q_d \times V_g}{T_{ox} \times k_s} \pm \frac{s \times c \times q_d}{T \times k_s^2} \quad (5.4)$$

where $V_g = V_{g0} \pm s \times t$. The sine term describes damped harmonic oscillation with a phase offset ϕ , the second term gives the equilibrium position under a given V_g and the third term denotes the displacement lag.

For a given V_g , if one assumes that the phase of the damped oscillation under forward sweep is ϕ , the corresponding phase under reverse sweep may be expressed as $2\pi - \phi$. The respective time t_f and t_r needed to reach a given V_g under the forward ($V_{g0} = -1$ V) and the reverse ($V_{g0} = 1$ V) sweep are $(1 + V_g)/s$ and $(1 - V_g)/s$. The corresponding displacement x_f and x_r are given by

$$x_f = A \times e^{-\frac{c \times t_f}{2m}} \times \sin \phi - \frac{q_d \times V_g}{T_{ox} \times k_s} + \frac{s \times c \times q_d}{T_{ox} \times k_s^2} \quad (5.5a)$$

$$x_r = A \times e^{-\frac{c \times t_r}{2m}} \times \sin(2\pi - \phi) - \frac{q_d \times V_g}{T_{ox} \times k_s} - \frac{s \times c \times q_d}{T_{ox} \times k_s^2} \quad (5.5b)$$

The difference in the displacement of the positive pole under the forward and reverse sweeps at the given V_g is then given by

$$\begin{aligned} \Delta d &= A \times e^{-\frac{c}{2m \times s}} \times \left(e^{-\frac{c \times V_g}{2m \times s}} + e^{\frac{c \times V_g}{2m \times s}} \right) \sin \phi + \frac{2s \times c \times q_d}{T_{ox} \times k_s^2} \\ &\geq 2A \times e^{-\frac{c}{2m \times s}} \times \sin \phi + \frac{2s \times c \times q_d}{T_{ox} \times k_s^2} \end{aligned} \quad (5.6)$$

noting that $\exp[-c \times V_g / (2m \times s)] + \exp[c \times V_g / (2m \times s)] \geq 2$.

Figure 5.11. Forward and reverse pulsed CV curves of a MOS capacitor (capacitor F) with 13.6 nm HfO₂ as the gate dielectric, fabricated at the same time as capacitor B.

Figure 5.12. Forward and reverse pulsed CV curves of capacitor B (HfO₂) at temperature of -40 °C (a) and 125 °C (b).

Though simple, equation (5.6) succinctly captures the dependence of Δd on c , s , k_s , and T_{ox} . Equation (5.6) predicts that for a give gate dielectric and ramp rate, Δd (and hence the capacitance hysteresis) decreases with increase in the dielectric thickness T_{ox} . Increasing T_{ox} reduces the oxide field for a given V_g and thus the displacement lag. This is validated in Fig. 5.11, which shows that the relative shift between curves F and R is reduced for capacitor F with a thicker HfO₂ gate dielectric (EOT = 3.7 nm) fabricated at the same time as capacitor B. The ratio of the hysteresis of capacitor B to capacitor E is 1.6 ($\approx 153/95$), which is in good agreement with the ratio of the respective EOTs (3.7/2.4).

Different temperatures measurements of capacitor B are given in Fig. 5.12. The two temperatures of -40 °C and 125 °C are adopted in the measurement due to two considerations: First, the device will not be degraded at the temperatures; second, doing the experiment in these two temperatures can result in two significant difference results, which can verify the role of c in the equation (5.6). At -40 °C, the hysteresis is decreased by 43 mV (153 mV-110 mV) when compared to the data obtained at room temperature (shown in Fig. 5.5(b)). Whereas, a significant increment (220 mV-153 mV = 67 mV) in the hysteresis is observed from a measurement at 125 °C. These observations indicate that the hysteresis varies proportionally with the temperature and a high temperature enables a larger c (i.e. higher viscosity of the local oxide network) which increases the displacement lag under a given ramp rate and the dielectric thickness T_{ox} . In addition, the second term in equation (5.6) is found to play a key role in determining the magnitude of the hysteresis.

It should be mentioned that a lag in interface dipole response should in principle also exist during HF CV measurement, due to the rapidly changing ac signal. However, the hysteresis in the forward and reverse HF CV curves is due mainly to oxide charge trapping and not the interface dipole relaxation effect. Since the amplitude of the ac signal is typically very small (~ 50 mV), we believe that the lag is much lesser than that for the pulsed CV measurement, during which a significant change in V_g (~ 1 V) occurs over a short time interval ($\sim \mu$ s). Moreover, the capacitance obtained from the HF CV method is an average value derived over many ac cycles. Averaging would further suppress the transient hysteresis effect. On the other hand, real-time measurement is made under the pulsed CV method and any transient hysteresis effect can be observed clearly.

5.4. Summary

We observed, from pulsed CV measurement on the high- κ /TiN gate MOS capacitor, a capacitance hysteresis which could not be explained in terms of charge trapping/detrapping in the gate dielectric. First, relative positions of the CV curves and the associated V_{fb} shifts derived from bidirectional fast voltage sweeps were opposite to those obtained from the quasi-static sweep method. Second, the hysteresis is found to be independent of a five order-of-magnitude variation in the pulse width. On the other hand, the hysteresis was observed to depend sensitively on the voltage ramp rate, which implies that it arises out of a lag in the dielectric response to the fast changing oxide field. An interface dipole relaxation mode that could explain the dependence of the hysteresis on

the ramp rate, viscosity of the local oxide network, elasticity of the dipole as well as the thickness of the dielectric was proposed. As verified experimentally, the model showed that the hysteresis would be more severe when the thickness of a given gate-stack is decreased. The model also suggested possible mitigation of the hysteresis effect through a reduction of the factor $(c q_d)/k_s^2$ via process optimization. Since having a certain dipole density may be crucial for V_{th} tuning, understanding how the elasticity of the dipoles could be controlled (so as to effectively suppress the hysteresis effect) needs to be further investigated.

Chapter 6 Investigation of the interfacial properties of Al₂O₃-capped GaN and GaN/AlGaIn/GaN heterostructure

6.1. Introduction

GaN, with its large band gap, high breakdown field, and ability to form 2DEG by a heterojunction, has attracted considerable interest for use in high-power transistors. However, issues of surface-state-related gate leakage currents and drain-current collapse at high frequency as well as the intrinsically high leakage current of the Schottky gate are slowing down the development of traditional GaN-based power HEMTs [12, 16, 17, 31]. Currently, it has been demonstrated that MIS-HEMT can help to mitigate the issues [9, 15, 18, 19] and become the most promising candidate of high-power transistors.

The origin of the surface defects of HEMT lies in the formation of GaO_x [12, 16, 17]. A GaO_x layer will inevitably grow on a GaN surface because of reactions with ambient oxygen [128], and such a layer also forms during insulator deposition because GaN can react with the oxidant (e.g. H₂O or O₃ during ALD deposition) and O species diffusing through the initially thin insulator layer [27, 92, 129]. A common explanation of the surface passivation mechanism is based on the Gibb's free energy [90]. A

reduction of the surface states can be achieved by reducing the GaO_x layer via a reaction between the GaO_x and an insulator with a more negative Gibb's free energy. Among the various insulators that have been investigated (e.g., SiO₂ [130], Si₃N₄ [86, 131], Al₂O₃ [15, 88, 132], HfO₂ [9], etc.), Al₂O₃ has emerged as one of the most favorable choices by virtue of its more negative Gibb's free energy of -1582.3 kJ/mol compared to that of GaO_x (~ -998.3 kJ/mol) [89]. Moreover, its wide band gap ($\sim 7-9$ eV), large dielectric constant (~ 9) and high breakdown field (~ 10 MV/cm) [129, 132] make Al₂O₃ attractive as a surface passivation layer. Studies of the ALD of Al₂O₃ on GaAs have indeed indicated the reduction of the native oxide through reaction with the TMA precursor [89, 90]. However, there are few studies of the ALD of Al₂O₃ on GaN, especially with regard to the properties of the Al₂O₃/GaN interface. Thus, a systematic study of GaN surface passivation by Al₂O₃ is of utmost practical importance.

Although the density of states can be decreased by reducing the GaO_x layer using TMA, the regrowth of GaO_x cannot be completely avoided during Al₂O₃ deposition via ALD [129]. Optimizing the quality of the GaO_x after Al₂O₃ deposition is another possible approach to the elimination of defect states. Several methods of achieving this goal have been reported [27, 92]. However, the exact mechanism of the film-quality improvement remains to be clarified. In this chapter, the interfacial properties of Al₂O₃ on GaN are systematically characterized using XPS.

6.2. The role of GaO_x on GaN surface band bending

6.2.1. Experimental details

A GaN-on-Si (111) wafer (labeled as wafer A) purchased from a commercial company was used for the ARXPS measurements. The epitaxial wurtzite structure of Ga-face GaN comprises a 1- μm Si-doped ($N_D=4\times 10^{17}/\text{cm}^3$) GaN layer on top of a 0.2- μm intrinsic GaN layer. A transition layer connects the GaN epilayers and the Si substrate. Ga-face GaN is preferred in device applications because of its smooth surface morphology and high material quality [133]. The wafers were degreased for 5 minutes in acetone, followed by immersion in isopropyl alcohol and a rinse in flowing deionized (DI) water. The native GaO_x was etched by dipping the sample into a diluted hydrofluoric acid solution (HF:H₂O = 1:20) for ~3 minutes, followed by a rinse in DI water. The first sample with native GaO_x (taken from an opened wafer holder and without the HF dip) is labeled as S1, whereas the other sample after the HF dip is denoted by S2. ARXPS measurements were conducted using a Thermo Scientific Theta Probe system equipped with a monochromatic Al K α (1486.6 eV) X-ray source. The photoelectrons were collected at six different angles (θ) of 25°, 35°, 45°, 55°, 65°, and 75° relative to the sample normal. The XPS spectra reported here were referenced to the C 1s peak at a BE of 285.0 eV, and the spectra were curve-fitted with a combination of Gaussian and Lorentzian line shapes, using a Shirley-type background subtraction.

Figure 6.1. Process flow for the fabrication of samples S1 and S2.

6.2.2. Results and discussion

The Ga 3*d* core-level spectra obtained at various detection angles for sample S1 are presented in Fig. 6.2(a). Two peaks, which are attributed to the Ga-N and Ga-O bonds, can be fitted in each Ga 3*d* spectrum. The Ga-O peak component originates from the native GaO_x layer. The BE of the Ga-N peak component is plotted as a function of θ in Fig. 6.2(b). No significant BE shift is observed with increasing θ . The variation in BE is ~0.1 eV, within the experimental error. A similar observation applies to the N 1*s* core-level spectra presented in Fig. 6.3.

Figure 6.2. (a) The Ga 3d core-level spectra and (b) the BE of the component peak corresponding to the Ga-N bond as a function of the detection angle (relative to the sample normal) for sample S1.

Figure 6.3. (a) The ARXPS N 1s core-level spectra and (b) the corresponding variation in the BE of the Ga-N bond for sample S1.

For sample S2, shown in Fig. 6.4(a), there are also two peaks, corresponding to the Ga-N and Ga-O bonds, observed in the Ga 3*d* spectrum after curve fitting. The Ga-O peak component is attributed to the regrowth of a GaO_x layer after the HF cleaning [128]. However, this GaO_x layer is thin with respect to that of sample S1 because the Ga-O/Ga-N bond-intensity ratio (0.26 in sample S1) decreases by half (0.13) in sample S2 for XPS measurements performed under more surface-sensitive conditions (at the largest detection angle (75 °)). Because the saturation oxygen coverage on GaN is approximately several monolayers [84, 92], the decrease in the Ga-O/Ga-N ratio after HF cleaning is not significant (from 0.26 to 0.13). The associated BE of the Ga-N bond (sample S2) is presented in Fig. 6.4(b). The BE shifts to lower values with increasing θ and reaches saturation when θ is larger than 45°. The maximum change in the BE over the θ range is ~0.3 eV. The N 1*s* core-level spectra of S2 exhibit a similar BE tendency as do the Ga 3*d* spectra, as shown in Fig. 6.5. These observations differ appreciably from those for sample S1. All BEs are summarized in Table 6.1.

To characterize the GaO_x layer on top of the GaN, the O 1*s* XPS spectra (obtained at 75 °) of samples S1 and S2 are presented in Fig. 6.6. Each O 1*s* spectrum can be fitted with two component peaks, corresponding to the Ga-O bond and absorbed O species (O_{abs}). The O_{abs} originate primarily from ambient oxygen impurities [134]. It is inevitable that GaN will absorb oxygen species from the ambient atmosphere during processing because the GaN surface is active toward oxygen adsorption and oxygen has a very high solubility in GaN [29, 96]. For sample S1, the GaO_x layer fully covers the GaN surface because sample S1 was exposed to the ambient atmosphere for several months, and hence, the Ga-O component peak has a much greater intensity than the O_{abs} peak. For sample S2,

the Ga-O/O_{abs} peak-intensity ratio indicates that the two components are of comparable magnitude. This observation indicates that the regrowth of the GaO_x layer may be caused by the reaction between the GaN and the absorbed oxygen impurities. It suggests that the GaO_x layer of S1 is much thicker than that of S2.

Figure 6.4. (a) The Ga 3d core-level spectra and (b) the BE of the component peak corresponding to the Ga-N bond as a function of the detection angle (relative to the sample normal) for sample S2.

Figure 6.5. (a) The ARXPS N 1s core-level spectra and (b) the corresponding variation in the BE of the Ga-N bond for sample S2.

Figure 6.6. The O 1s core-level spectra obtained at a detection angle of 75 ° for samples S1 and S2.

Table 6.1. Summary of the Ga 3d and N 1s BEs at various detection angles for samples S1 and S2.

Samples	Core level	Chemical bonds	Detection angles θ					
			25°	35°	45°	55°	65°	75°
S1	Ga 3d	Ga-N	19.72	19.83	19.79	19.8	19.81	19.79
		Ga-O	20.66	20.57	20.65	20.64	20.61	20.66
	N 1s	Ga-N	397.34	397.45	397.46	397.46	397.46	397.46
S2	Ga 3d	Ga-N	19.80	19.69	19.57	19.58	19.60	19.53
		Ga-O	20.73	20.41	20.34	20.36	20.47	20.35
	N 1s	Ga-N	397.43	397.35	397.26	397.18	397.21	397.1

In Fig. 6.7, schematic diagram is presented to illustrate the ARXPS results. The Fermi energy level E_f of GaN was calibrated to 0 eV for the XPS measurements. After incident photons with an energy of $h\nu$ penetrate into the samples, the emitted photoelectrons are collected at various θ . Because the BE is the weighted average of the detected photoelectrons, not just the signal on the surface [135], a larger θ leads to a shallower XPS information depth, as illustrated in Fig. 6.7. Consequently, a measurement with varying θ can be used to obtain a complete profile of the surface energy bands.

It has been reported that the spontaneous polarization of Ga-face GaN results in the presence of negative bound charges at the surface [32, 95, 99, 136]. As a result, positive compensating substrate charges form near the GaN surface region, and the distribution of these charges results in upward band bending [16, 27, 95, 137]. However, a disordered layer of GaO_x will inevitably form on the surface because GaN reacts with oxygen [27, 29]. The Ga-O bond of the GaO_x layer generates surface states that extend from the valence band to the band gap [17, 27]. These surface states are neutral when filled and positive when empty, giving them donor characteristics [27]. In the case of upward band bending, some donor states may lie above E_f , in which case electrons are able to transfer from the occupied donor states into empty conduction-band states, resulting in positively charged donor states at the surface [12, 17, 27, 138]. These positive charges compensate for the negative polarization charges and attenuate the upward band bending, which results in a slight downward band bending. This phenomenon may explain why the BE value of sample S1 does not change or increases only slightly with increasing θ , as shown in Fig. 6.2(b). However, the trend in the BE variation of sample S2 is found to differ significantly from that of sample S1 because the HF cleaning was able to effectively

remove the GaO_x layer and the associated positively charged states [139]. Although a layer of GaO_x is detected in sample S2, it may be too thin to exert a comparable effect on the polarization, or the HF cleaning process may have reduced the surface roughness and thereby reduced the surface states [139, 140]. Therefore, upward band bending is observed, and the BE shifts gradually to lower values with increasing θ in sample S2.

Figure 6.7. A schematic diagram to explain the ARXPS results. The effective information depth varies with the photoelectron detection angle θ , and this effect can be exploited to obtain a complete profile of the surface energy bands. Because θ_1 is smaller than θ_2 , the BE1 value obtained at θ_1 is smaller (larger) than the BE2 value measured at θ_2 in the downward (upward) band-bending case.

The interface dipole model is ruled out as an explanation of the ARXPS results by the following explanation. If an interface dipole is formed on the surface, it will not change the BE of the Ga-N bond because the electric field is within the dipole. As a result, sample S1 should exhibit the same trend in the BE shift as does sample S2. However, such behavior is not observed from our ARXPS results. This conclusion is also verified by the continuous reduction in the BEs of Al₂O₃/GaN structures with increasing Al₂O₃ thickness [129] and the shift in the flat-band voltage as a function of the gate-oxide thickness in GaN capacitors [99].

To obtain the positive charge density using the surface potential Φ_b (i.e., the distance between the Fermi level and the conduction-band edge, which can be determined from the band-bending magnitude), the negative-polarization-induced charges, the compensating substrate charges, and the positive donor states are considered in an electrostatics analysis, as illustrated in Fig. 6.8. According to the Poisson equation, the net volume charge density p_1 on the GaN surface can be expressed as

$$p_1 = \frac{d^2\Phi_b}{dx^2} \times \left(-\frac{\epsilon}{e}\right) \quad (6.1)$$

where x is the coordinate, e is the electron charge, and ϵ is the permittivity of GaN.

Because $\frac{E_C - E_f}{e} = \Phi_b$ and the thermal voltage $V_t = \frac{k \times T}{e}$, the electron density n in the GaN substrate can be expressed as

$$n = N_c \exp\left(-\frac{\Phi_b}{V_t}\right) \quad (6.2)$$

where E_c is the conduction-band energy, N_c is the effective density of states in the conduction band and has a value of $2.3 \times 10^{18}/\text{cm}^3$, k is Boltzmann's constant, and T is the temperature.

For simplicity, it is assumed that there are only two types of charges (i.e., holes are ignored because their density is too small in n-type GaN) in the substrate: electrons and positively charged substrate donors. In this case, the density of the substrate charges p_2 can be expressed as

$$p_2 = N_D - n = N_D - N_c \exp\left(-\frac{\Phi_b}{V_t}\right) \quad (6.3)$$

where N_D is the density of donor impurity atom.

Without an external applied voltage, the structure should be charge neutral in equilibrium and thus the sum of the various charges is zero. Therefore, $p_1 + p_2 = 0$ and the following equation is obtained.

$$\frac{d^2 \Phi_b}{dx^2} = \frac{e \times N_D}{\epsilon} - \frac{e \times N_c}{\epsilon} \exp\left(-\frac{\Phi_b}{V_t}\right) \quad (6.4)$$

This equation can be solved to obtain the relation between Φ_b and the net sheet charge density σ_c (corresponding to p_1) on the surface.

$$\sigma_c = \frac{\epsilon}{e} \times \sqrt{\frac{2e}{\epsilon} \times (N_c \times V_t \times \exp\left(-\frac{\Phi_b}{V_t}\right) + N_D \times \Phi_b) + D} \quad (6.5)$$

where D is a constant.

Figure 6.8 Schematic band diagrams including various charges for (a) sample S1 and (b) sample S2. The combined effect of the surface charges induces a potential Φ_b at the surface, which can be deduced from the charges distribution. In this manner, the relation between Φ_b and the net surface charge density σ_c can be obtained.

In the substrate region, it is assumed that n is equal to N_D . According to this boundary condition, Φ_b is found to be 0.0453 V (shown in Fig. 6.8) from equation (6.2), and D is calculated to be -5.7×10^9 from equation (6.5). The maximum value of the band bending determined using ARXPS is regarded as the variation in the conduction-band edge. For sample S1, as shown in Fig. 6.8(a), a value of -0.0547 V (0.1 V - 0.0453 V) is substituted for Φ_b in equation (6.5), and a net positive charge density is found to be $2.09 \times 10^{12}/\text{cm}^2$. It has been reported that the spontaneous-polarization-induced negative sheet charge is $1.8 \times 10^{13}/\text{cm}^2$ [94, 99]. Therefore, the positive surface charge density induced by the native GaO_x is calculated to be $2.009 \times 10^{13}/\text{cm}^2$ ($1.8 \times 10^{13}/\text{cm}^2 + 2.09 \times 10^{12}/\text{cm}^2$), which is consistent with the value of $2.27 \times 10^{13}/\text{cm}^2$ deduced from capacitance–voltage measurements of the Al₂O₃/GaN structure [99]. For sample S2, as shown in Fig. 6.8(b), a value of 0.3453 V (0.3 V + 0.0453 V) is substituted for Φ_b in equation (6.5), and a net negative charge density is calculated to be $1.0 \times 10^{12}/\text{cm}^2$. Therefore, the density of positive charges in the surface region should be $1.7 \times 10^{13}/\text{cm}^2$ ($1.8 \times 10^{13}/\text{cm}^2 - 1.0 \times 10^{12}/\text{cm}^2$). The density of positive charges was significantly reduced by the HF cleaning.

6.2.3. Conclusion

The role of GaO_x in determining the surface band-bending properties of GaN was investigated via ARXPS and an electrostatics analysis. The presence of the positive donor states induced by the formation of native GaO_x is considered to be an important factor in determining the band bending. In addition, the HF cleaning process is observed to

effectively remove the GaO_x layer and the corresponding defect states. The charge density on the surface can be obtained quantitatively using the proposed mathematical equation.

6.3. Interfacial chemistry and valence band offset between GaN and Al₂O₃

6.3.1. Experimental details

The structure as well as the cleaning procedure received of GaN-on-Si (111) (wafer A) substrate is identical to those stated in section 6.2.1. After HF cleaning, Al₂O₃ was deposited by ALD, with TMA and H₂O as the metal precursor and oxidant, respectively. The chamber temperature was held at 250 °C during deposition. The Al₂O₃ deposition started off with two TMA pulses, aimed at reducing the native oxide layer [89, 90]. This was followed by regular deposition cycles consisting of a TMA pulse and then a H₂O pulse. The Al₂O₃ thickness was measured using a VB-250 Spectroscopic Ellipsometer. Samples with 0, 1.3, and 4.0 nm thick Al₂O₃ were fabricated and they are denoted as S1, S2, and S3, respectively, in the following discussion. To check the impact of the TMA and H₂O pulse sequence, another set of samples S4 and S5 each having a 4.0 nm Al₂O₃ was prepared without the initial two TMA pulses. The Al₂O₃ in S4 was deposited with H₂O pulse first followed by TMA pulse while that in S5 was deposited

with TMA pulse first and then H₂O pulse. The process flows and the gate stack structures are given in Fig. 6.9.

Figure 6.9. (a) Process flow and (b) schematic diagram of the structures for samples S1-S5.

A similar experiment of different Al₂O₃ thicknesses deposition on Ga-face GaN/AlGaIn/GaN (labelled as wafer B) was also done in this part. The GaN-epilayers had the following physical structure: GaN (2 nm)/Al_{0.26}Ga_{0.74}N (18 nm)/GaN (1 μm)/transition layer/Si (111) substrate. All layers were unintentionally doped. After wafer cleaning, Al₂O₃ was deposited by ALD with TMA pulse first. Samples with 0, 1.0, and 5.0 nm thicknesses Al₂O₃ were fabricated and they are denoted as T1, T2, and T3, respectively. XPS measurements were carried out for all the samples.

6.3.2. Results and discussion for Al₂O₃ capped GaN

The Ga 3*d* core-level spectra for S1-S3 are depicted in Fig. 6.10(a). Each Ga 3*d* spectrum could be deconvoluted into two components, corresponding to the Ga-N and Ga-O bonds. Existence of the Ga-O spectrum in S1 (without Al₂O₃ deposition) may be attributed to the inevitable reoxidation of the GaN surface after cleaning. The ratio of the Ga-O to Ga-N peak for this sample is 0.15. This ratio is 0.24 for S2 (1.3 nm Al₂O₃), implying that the growth of GaO_x occurred during Al₂O₃ deposition. For S3 (4.0 nm Al₂O₃), however, the Ga-O/Ga-N ratio of 0.26 is not significantly different from that of S2. This implies that the GaO_x growth occurs mainly during the initial ALD cycles and it saturates after a thicker Al₂O₃ is deposited. Fig. 6.10(b) shows the Ga 3*d* spectra and the corresponding Ga-N and Ga-O components for S4 and S5. The Ga-O to Ga-N peak ratios of 0.22 and 0.23 for S4 and S5, respectively, are comparable and similar to those for S2 and S3, indicating that the sequence of the TMA and H₂O pulses has no apparent impact on the growth of GaO_x during Al₂O₃ deposition.

Figure 6.10. The XPS Ga 3d core-level spectra for (a) S1-S3 and (b) S4 and S5.

Reduction of the native oxide by TMA was observed during ALD of Al₂O₃ on GaAs [89, 90]. In our case, however, the growth of GaO_x is observed during ALD of Al₂O₃ on GaN. The difference may be explained. In [90] and [89] Al₂O₃ deposition was

made either directly on a wafer removed from a sealed holder[90] or after pre-heating at 320 °C for 30 minutes [89]. The native oxide was relatively thick and its subsequent interaction with the initial TMA-only cycles might have led to part of it being converted into Al₂O₃. In our case, however, the native oxide was thinner because 1) the wafer was dipped in HF before it was loaded into the ALD chamber for Al₂O₃ deposition; 2) the wafer stage was pre-heated to the deposition temperature to enable the ALD process to begin soon after the wafer was loaded. Although the regrowth of GaO_x before the start of the ALD process was inevitable due to the high temperature, it could not explain the similar Ga-O/Ga-N bond ratio of S2-S5. In S2 and S3, since TMA-only cycles were initially applied, part of the regrown native oxide would have been converted into Al₂O₃ and thus the Ga-O/Ga-N bond ratio should be lower than those for S4 and S5. Instead, comparable Ga-O/Ga-N bond ratios are obtained, implying that the extent of GaO_x growth was similar in all samples regardless whether TMA-only cycles were used initially (S2 and S3) or the TMA and H₂O pulses were reversed (S4 and S5). We believe that after the TMA-only cycles, the resultant Al₂O₃ layer in S2 and S3 might be too thin (due to the initially thin native oxide) to prevent the oxidation of GaN in subsequent deposition cycles involving the H₂O pulse. Parasitic oxidation of GaN during plasma-assisted SiO₂ deposition was observed and was believed to have been caused by O species diffusing through the initially thin SiO₂ layer [141]. We reckon that there should be a lower limit to the thickness of the native oxide so that the Al₂O₃ formed via the initial TMA-only cycles is sufficiently thick to suppress the growth of GaO_x during subsequent Al₂O₃ deposition. At the same time, the native oxide should be thin enough so that it could be fully converted into Al₂O₃ by the TMA-only cycles.

It is interesting to point out that the BE of the Ga 3*d* peak is shifted progressively towards smaller values as the Al₂O₃ thickness is increased (Fig. 6.10(a)). A similar observation applies to the N 1*s* spectra shown in Fig. 6.11(a). No difference is, however, seen in the Al 2*p* spectra for S2 and S3 (Fig. 6.11(b)). For both cases, only a single peak with a BE of ~74.3 eV, similar to that for the Al-O bond in bulk Al₂O₃, is evident. Table 6.2 summarizes the BEs of the Ga 3*d*, N 1*s* and Al 2*p* peaks for S1-S3.

Table 6.2. Summary of the BE of the intensity peak(s) in the Ga 3*d*, N 1*s*, and Al 2*p* spectra as well as the GaN/Al₂O₃ VBO for S2 and S3.

Sample No.	Al ₂ O ₃ thickness (nm)	Binding Energy (eV)					
		Ga 3 <i>d</i>		N 1 <i>s</i>	Al 2 <i>p</i>	VBO (Ga 3 <i>d</i>)	
		Ga-N	Ga-O				
S1	0.0	19.7	20.5	0.15	397.3	-	-
S2	1.3	19.4	20.1	0.24	397.1	74.3	0.7
S3	4.0	19.3	19.9	0.26	397.0	74.4	0.9

Figure 6.11. (a) The XPS N 1s core-level spectra for S1-S3. (b) The XPS Al 2p core-level spectra for S2 and S3.

The nearly identical Al 2*p* spectra of S2 and S3 implies that the reduction in the BE of the Ga 3*d* and N 1*s* peaks are not related to the bulk property of the deposited Al₂O₃. A possible reason for the observed BE shifts is dipole formation at the GaN/Al₂O₃ interface. However, interface-dipole induced BE shift should saturate after the deposition of several monolayers of Al₂O₃ and may not adequately explain the continuous reduction of BE seen with the increase in Al₂O₃ thickness. To probe this further, the VBO between Al₂O₃ and GaN is determined using the method first proposed by Kraut *et al.*[105], as summarized in the following equation:

$$\text{VBO} = \left[E_{\text{CL}}^{\text{Al}_2\text{O}_3}(\text{b}) - E_{\text{V}}^{\text{Al}_2\text{O}_3}(\text{b}) \right] - \left[E_{\text{CL}}^{\text{GaN}}(\text{b}) - E_{\text{V}}^{\text{GaN}}(\text{b}) \right] - \left[E_{\text{CL}}^{\text{Al}_2\text{O}_3}(\text{i}) - E_{\text{CL}}^{\text{GaN}}(\text{i}) \right] \quad (6.6)$$

The subscript CL and v denote the BE for the “core-level” and “valence band maximum (VBM)”, respectively. The bulk and interface BEs are represented, respectively, by the notation (b) and (i). The BE difference between core-level and VBM of bulk Al₂O₃ and GaN, which correspond to the first and second square-bracket terms in (6.6), are given in Fig. 6.12. The VBM of each sample is determined by extrapolating the leading edge of the valence band spectrum to the base line (the cross-over points in Fig. 6.12) [142]. Using the BE for the Al 2*p* and Ga 3*d* spectra as the core-level BE of bulk Al₂O₃ and GaN, respectively, the corresponding BE difference between the core-level and VBM are determined as 71.8 eV and 17.6 eV, as shown in Fig. 6.12. The value for the last square-bracket term in (6.6) is obtained from the difference in the core-level BE for Al 2*p* and Ga 3*d* (Table 6.2). The value is 54.9 eV (= 74.3 eV – 19.4 eV) for S2 and 55.1 eV (= 74.4 eV – 19.3 eV) for S3. Therefore, the VBO between Al₂O₃ and GaN are

0.7 eV ($=71.8 \text{ eV} - 17.6 \text{ eV} - 54.9 \text{ eV}$) and 0.9 eV ($=71.8 \text{ eV} - 17.6 \text{ eV} - 55.1 \text{ eV}$) for S2 and S3, respectively.

Figure 6.12. The Al 2*p* (a) and Ga 3*d* (b) core-level and valence band spectra for bulk Al₂O₃ (deposited by ALD) and GaN. The square and circle symbols represent the core-level and valence band spectra, respectively. The VBM is extrapolated from the intersection point between the leading edge of the valence band spectrum and the base line.

Figure 6.13. (a) Schematic cross-sectional diagrams showing GaN without and with deposited Al₂O₃ of different thicknesses. (b) Corresponding schematic energy band alignment diagrams for the cross-sectional diagrams in (a). The XPS binding energy for the Ga 3d and Al 2p core levels are measured with respect to the Fermi level E_f .

It should be mentioned that since S2 and S3 were fabricated under identical conditions, the GaN/Al₂O₃ interface and hence, the VBO should be similar for both samples. This is supported by the identical VBO's (= 0.9 eV) for S4 and S5, which were also fabricated under the same conditions. A possible explanation for the difference in the VBO's of S2 and S3 is given as follows. It is known that spontaneous polarization in GaN results in a surface bound charge, which is negative in the case of the Ga-face GaN [32, 95, 99, 136]. As a consequence, a compensating space charge comprising positive donors is formed near the GaN surface [16, 27, 137]. The impact of this positive space charge on XPS measurement of the Ga 3d electrons from samples having different Al₂O₃ thicknesses is depicted by the schematic diagrams in Figs. 6.13(a)-(c). It should be noted that the Fermi level E_f in GaN serves as the reference energy level (0 eV) for XPS measurement. Because the negative surface bound charge depletes the n-type GaN, an upward bending of the energy bands occurs near the surface [87, 95] (Fig. 6.13 (b)). Thus, the difference between E_f and the core level (as well as the VBM) in GaN decreases towards the surface.

Since the X-ray penetration depth (τ_x) for a given energy remains approximately constant, the probe depth in the GaN layer in S3 having a thicker Al₂O₃ is shallower than that in S2 (Fig. 6.13(c)). Thus, the GaN photoelectrons sensed during XPS measurement of S3 comes mainly from nearer the surface region where the difference between E_f and the core level (and VBM) is smaller. Hence, the resultant XPS spectra, which are determined from the weighted average of photoelectrons emitted from a certain depth in the sample, are shifted towards smaller energies, and the extracted VBO₃ is larger, as compared to those of S2 (Fig. 6.13(c)). To further confirm the effect of the upward

surface band bending in GaN on the VBO between GaN and Al₂O₃, the VBM difference between bulk Al₂O₃ and GaN before contact is calculated to be 0.5 eV. This value is evidently smaller than the VBO of 0.7 eV for S2 (VBO₂) and 0.9 eV for S3 (VBO₃). The latter two values are larger due to the upward band bending at the GaN surface as explained above.

6.3.3. Results and discussion for the Al₂O₃-capped GaN/AlGa_{0.5}N/GaN heterostructure

The study on the structure of Al₂O₃ capped GaN/AlGa_{0.5}N/GaN heterostructure follows the similar procedure. The Ga 3*d* core-level spectra for T1-T3 are depicted in Fig. 6.14(a). Each Ga 3*d* spectrum could be deconvolved into two components, corresponding to the Ga-N and Ga-O bonds. For T1, an inevitable reoxidation of the GaN surface after cleaning is observed and the Ga-O/Ga-N ratio of this sample is 0.15. Due to the growth of GaO_x during Al₂O₃ deposition, the ratio increases to 0.24 and 0.22 for samples T2 and T3, respectively. The BE of the Ga 3*d* peak is decreased gradually as the Al₂O₃ thickness is increased (Fig. 6.14(a)). However, no difference is seen in the Al 2*p* spectra for T2 and T3 (Fig. 6.14(b)). There are two obvious peaks, recorded as Al-N and Al-O bonds. The Al-N bond is from the AlGa_{0.5}N layer while the Al-O bond is from deposited Al₂O₃ layer, with the BE of ~73.5 eV and 74.4 eV, respectively. Table 6.3 summarizes the BEs of the Ga 3*d* and Al 2*p* peaks for T1-T3.

Figure 6.14. The XPS Ga 3d (a) and Al 2p (b) core-level spectra for T1-T3.

Table 6.3. Summary of the BEs of the intensity peak(s) in the Ga 3*d* and Al 2*p* spectra as well as the GaN/Al₂O₃ VBO for T2 and T3.

Sample NO.	Al ₂ O ₃ thickness (nm)	Binding Energy (eV)					VBO
		Ga 3 <i>d</i>			Al 2 <i>p</i>		
		Ga-N	Ga-O	GaO/ GaN	Al-N	Al-O	
T1	0.0	19.4	20.2	0.15	73.5	-	-
T2	1.0	19.4	20.2	0.24	73.6	74.4	0.8
T3	5.0	19.1	19.8	0.22	73.5	74.3	1.0

According to the equation (6.6), the VBO at the Al₂O₃/GaN interface are 0.8 eV (=71.8 eV – 17.6 eV – 55 eV) and 1.0 eV (= 71.8 eV – 17.6 eV – 55.2 eV) for T2 and T3, respectively. The VBO shifts progressively towards a larger value as the thickness of Al₂O₃ is increased. This observation indicates that the energy band bends upward at the Al₂O₃/GaN/AlGaIn/GaN interface, which is consistent with the observation from the Al₂O₃/GaN interface. Since the Ga 3*d* BE and VBM of bulk GaN are used in the calculation to represent the GaN heterostructure in the second square-bracket term of equation (6.6), there may have a little discrepancy with the actual value. However, it does not affect the conclusion of the results.

6.3.4. Conclusion

Our study on the interface region between GaN or GaN/AlGaIn/GaN and Al₂O₃ using XPS yields two main findings: 1) The growth of a thin interfacial GaO_x layer following the ALD of Al₂O₃ is still observed, despite the use of TMA-only cycles in the initial stage to convert the native oxide to Al₂O₃. This suggests a lower limit to the native

oxide thickness so that the resultant Al₂O₃ layer is thick enough to block GaN oxidation during subsequent Al₂O₃ deposition involving the oxidizing agent. 2) The BE of the Ga 3*d* and N 1*s* spectra are decreased and the extracted VBO between GaN/Al₂O₃ is increased when the thickness of the Al₂O₃ is increased, whereas the Al 2*p* spectra are unaffected. These observations could be consistently explained by the upward surface band bending due to a polarization induced negative surface bound charge in the Ga-face GaN and they highlight an intrinsic limitation of the XPS method for band offset determination.

6.4. Effect of PDA on the interface electronic structure of the Al₂O₃-capped GaN and GaN/AlGaIn/GaN heterostructure

6.4.1. Experimental details

The structure of n-type GaN-on-Si (111) (wafer A) and GaN/AlGaIn/GaN heterostructure (wafer B) wafers as well as the cleaning procedure are identical to those stated above. After wafer cleaning, the Al₂O₃ was grown by ALD, with TMA and H₂O as the metal precursor and oxidant, respectively. After ALD deposition, the samples were subjected to PDA in N₂ for 30 s at varying temperatures. The Al₂O₃ thickness is 3.0 nm for all samples, as measured by the Spectroscopic Ellipsometer VB-250. For wafer A, the sample with as-deposited Al₂O₃ (i.e., without PDA) is denoted as S1, while samples

subjected to PDA at 400, 500, 600, and 800 °C are denoted as S2, S3, S4 and S5, respectively. For wafer B, the bare sample (i.e., without Al₂O₃ deposition) is denoted as H1 and the as-deposited sample is denoted as H2. Samples subjected to PDA at 500 and 800 °C are denoted as H3 and H4, respectively. The process flows and the gate stack structures for all the samples are given in Fig. 6.15. XPS measurements were carried out using a monochromatic Al *Kα* X-ray source of energy 1486.7 eV. The XPS spectra reported here are referenced to C 1s at 285.0 eV and the spectra are curve-fitted with a combination of Gaussian and Lorentzian line shapes, using a Shirley-type background subtraction.

Figure 6.15. (a) Process flows and (b) schematic diagram of the gate stack structures for samples S1-S5 and H1 to H4.

6.4.2. Results and discussion

The Ga 3*d*, N 1*s* and Al 2*p* core-level XPS spectra for S1-S5 are depicted in Fig. 6.16(a), (b) and (c), respectively. The corresponding results for H1-H4 are shown in Fig. 6.17(a)-(c). Table 6.4 and 6.5 summarize the key parameters (e.g., BE of the spectral peaks).

The presence of a Ga-O signal in the Ga 3*d* spectra of Fig. 6.16(a) and 6.17(a) should be noted. Relative to H1, the higher Ga-O to Ga-N bond density ratio in H2 (Table 6.5) implies that additional GaO_x was formed at the Al₂O₃/GaN interface during ALD [129]. In control experiments where TMA-only cycles were applied at the beginning of the ALD process, a similar increase of the Ga-O/Ga-N ratio was observed [129]. This implies that the finite delay between the introduction of the sample into the ALD chamber and the start of the ALD process is not the main reason for the GaO_x formation, since the TMA-only cycles would have reduced the GaO_x formed at this stage [89, 90]. The results therefore show that GaO_x growth also happened during ALD as the oxidizing species may penetrate the initially thin Al₂O₃ layer.

Figure 6.16. (a) Ga 3d, (b) N 1s, and (c) Al 2p core-level XPS spectra of samples S1-S5. Gaussian-Lorentz curve fitting was used. Except for the Al 2p peak which is not affected by PDA, the Ga 3d and N 1s peaks can be seen to shift towards lower binding energy with increase in the PDA temperature.

Figure 6.17. (a) Ga 3d, (b) N 1s, and (c) Al 2p core-level XPS spectra of samples H1-H4 showing similar behaviour as those for samples S1-S5.

Table 6.4. Binding energy of XPS spectra peaks, Ga-O/Ga-N bond density ratio and the interface barrier height Φ_b for samples S1-S5. Φ_b is defined as the energy difference between the Fermi level and the conduction band minimum at the surface or interface (cf. Fig. 6.19(b)). It may be expressed as $E_g + E_{\text{Ga } 3d}^{\text{dif}} - \text{BE}_{\text{Ga } 3d}$, where E_g is GaN band gap (3.4 eV[31]), $\text{BE}_{\text{Ga } 3d}$ is binding energy of the Ga 3d peak, $E_{\text{Ga } 3d}^{\text{dif}}$ is difference between the valence band maximum and $\text{BE}_{\text{Ga } 3d}$ (independent of Al₂O₃ passivation [143]).

Sample No.	PDA temperature (°C)	Binding energy (eV)					Φ_b
		Ga 3d			N 1s	Al 2p	
		Ga-N	Ga-O	Ga-O/ Ga-N	Ga-N	Al-O	
S1	as-dep	19.5	20.2	0.31	397.6	74.3	2.8
S2	400	19.6	20.2	0.29	397.3	74.3	2.7
S3	500	19.4	19.9	0.29	397.1	74.4	2.9
S4	600	19.4	20.1	0.26	397.1	74.3	2.9
S5	800	19.1	19.8	0.26	396.8	74.3	3.2

Table 6.5. Binding energy of XPS spectra peaks, Ga-O/Ga-N bond density ratio and the interface barrier height Φ_b for samples H1-H4.

Sample No.	PDA temperature (°C)	Binding energy (eV)						Φ_b
		Ga 3 <i>d</i>			N 1 <i>s</i>	Al 2 <i>p</i>		
		Ga-N	Ga-O	Ga-O/ Ga-N	Ga-N	Al-O	Al-N	
H1	bare	19.7	20.6	0.12	397.2		73.5	2.6
H2	as-dep	19.4	20.0	0.24	396.9	74.4	73.5	2.9
H3	500	19.4	20.1	0.21	397.0	74.4	73.6	2.9
H4	800	19.3	19.9	0.22	396.8	74.4	73.5	3.0

The tendency for the increase of the Ga-O/Ga-N bond density ratio to slow down, indicating that the GaO_x growth tends towards saturation beyond a certain Al₂O₃ thickness [129], supports this inference. While GaO_x formation may happen during the ALD of Al₂O₃, it is interesting to point out that the Ga-O to Ga-N bond density ratio

remains almost unchanged after PDA (Table 6.4 and 6.5). This implies that there is no apparent evidence of GaO_x reduction by the deposited Al₂O₃ after PDA.

To examine the impact of PDA on the Al₂O₃/GaN interface defect properties, Hall-effect measurements were performed on H1-H4 (based on the van der Pauw method[144]) to extract the density and mobility of the 2DEG. Results are shown in Fig. 6.18. For the as-deposited sample (H2), the density and mobility of the 2DEG are comparable to those of the bare sample (H1). The observation suggests that the properties of the GaN surface are not significantly altered by the deposited Al₂O₃ but are determined mainly by the first few monolayers of GaO_x formed. Moreover, there seems to be no major differences between the GaO_x/GaN interface formed during the ALD and that on the bare sample, due possibly to the relatively low ALD temperature (250 °C). The lack of any substantial impact of the 500 °C PDA on the 2DEG density and mobility corroborates this inference. The increase in the 2DEG mobility after the 800 °C PDA implies that the surface scattering effect and thus the interface defect density are reduced [88, 145]. The corresponding decrease in the 2DEG density supports this conclusion. It has been widely accepted that the surface defects are a main source for the 2DEG [27, 138]. Thus, the decrease in the 2DEG density indicates that the surface defect density is being reduced after PDA.

Figure 6.18. (a) Concentration and (b) mobility of the two-dimensional electron gas in samples H1-H4, as determined from Hall-Effect measurement (300 K).

Studies on the Al₂O₃-capped AlGa_{0.3}N/GaN heterostructure have broadly attributed the improved 2DEG mobility to the surface passivation effect of the deposited Al₂O₃ layer [88, 132]. The detailed mechanisms, however, are not yet clarified. One explanation, based on Gibb's free energy calculation, attributes the passivation effect to the removal of GaO_x by the Al₂O₃, thus resulting in a lower interface defect density [89, 139, 146]. On the other hand, our results show that an interfacial GaO_x layer is formed at the same time

as the Al₂O₃ and that the GaO_x layer is stable during PDA (for the range of temperature studied). These results imply that it is not Al₂O₃ deposition but the subsequent thermal treatment that leads to the improved 2DEG mobility. A possible reason is the conversion of the disordered GaO_x into Ga₂O₃ [27, 84]. In conjunction with the charge redistribution in disordered GaO_x that occur during PDA, an improved match between the Ga₂O₃ and the GaN surface may then be achieved [147]. It has been shown that the defect density at the SiO₂/GaN interface could be substantially reduced by the growth of an ultrathin Ga₂O₃ layer prior to the SiO₂ deposition [92]. Thus, it is believed that the commonly reported mobility enhancement of the Al₂O₃/GaN HEMT stems mainly from the improved Ga₂O₃/GaN interface after subsequent thermal treatment. Nonetheless, the extent by which structural transformation of the GaO_x layer could happen under a given PDA condition is expected to depend on the type of dielectric used and the associated interface strain. Further study is in progress to understand this.

The impact of PDA on the BE of the core-level spectra peaks is also examined (Table 6.4 and 6.5). No visible impact on the BE of the Ga 3*d* peak, relative to the as-deposited sample, can be seen for PDA temperature up to ~400 °C. A slight reduction of the BE is observed at the 500 °C PDA and the decrease becomes evidently larger at the 800 °C PDA. A similar observation applies to the N 1*s* peak. Given that PDA has no apparent impact on the BE of the Al 2*p* peak, the observed BE decrease is mainly due to changes at the Al₂O₃/GaN interface. Similar results are obtained on the GaN/AlGa_{0.3}N/GaN samples (H3 and H4) shown in Fig. 6.17. For these samples, the Al 2*p* spectra can be deconvolved into two components – other than the usual Al-O component, another

component due to the Al-N bonds can be observed (Fig. 6.17(c)), since the AlGaIn layer was also probed. The substantially lower Al-N peak of H2 as compared to that of H1 indicates that with the deposition of the 3-nm Al₂O₃, the XPS probe depth is now confined to the interface region between the 2-nm top GaN layer and the Al₂O₃. Since PDA also has no apparent effect on the BE of the Al 2*p* peak, the BE decrease for the Ga 3*d* and N 1*s* peaks are thus because of changes at the GaN/Al₂O₃ interface.

The change in the BE of the XPS spectra may be explained in terms of the change in the GaN surface band bending, as a result of the decrease in the interface defect density after PDA, as illustrated in Fig. 6.19. Spontaneous polarization of the Ga-face GaN results in a negative surface bound charge (of density $\sim 10^{13} \text{ cm}^{-2}$) [94, 95, 99] which depletes the n-type GaN (or AlGaIn), causing the energy band at the surface to bend upwards as shown. Fig. 6.19(a) illustrates how this upward surface band bending, in conjunction with a varying XPS probe depth in GaN, influence the BE obtained from XPS measurement. For a shallower probe depth (long-dash), surface photoelectrons having smaller BEs (measured with respect to the 0 eV Fermi level) made up a greater proportion of the photoelectrons detected during XPS measurement, as compared to the case of a deeper probe depth (dotted). Thus, the measured BE would be smaller when the XPS probe depth is shallower. This explains the BE decrease of the Ga 3*d* and N 1*s* peaks of H2, relative to those of H1[129], since the XPS probe depth in GaN is reduced after the deposition of the 3-nm Al₂O₃. It is essential to note that the upward band bending is lowered by the surface states which charge up positively [87, 95] and thus partially screen the negative surface bound charge (Fig. 6.19(b)).

Figure 6.19. (a) Schematic diagram showing upward bending of the energy band near the surface (line AA') of the Ga-face GaN. The effect of a shallow (long-dash) and deep (dotted) XPS probe depths on the measured XPS BE is illustrated. (b) The positive trapped charge at the Al₂O₃/GaN interface reduces the upward surface band bending in the as-deposited sample (solid) and hence increases the measured XPS BE relative to that of the annealed sample (short-dash) in which the density of the positive interface trapped charge is decreased.

The presence of positively charged surface states is commonly revealed through the negative-voltage shifted CV curve of the metal/Al₂O₃/GaN structure [32, 99]. After PDA, the density of the interface states is reduced, as can be deduced from the changes in the density and mobility of the 2DEG, as well as the positive-voltage shift of the CV

curve reported by other studies [92, 148, 149]. As a consequence, the surface band bending is increased and the effect of the reduced XPS probe depth (after Al₂O₃ deposition) on the XPS BE decrease becomes more prominent, as depicted in Fig. 6.19(a). A higher PDA temperature results in a greater reduction of the interface defect density [92, 145, 148] and thus a more apparent decrease of the XPS BE. Changes in the surface band bending after PDA may be manifested through the corresponding changes in the interface barrier height Φ_b (Fig. 6.19(b)), as summarized in Table 6.4 and 6.5.

6.4.3. Conclusion

The interface electronic properties of Al₂O₃-capped GaN and GaN/AlGaIn/GaN heterostructure after PDA at varying temperatures are investigated by XPS and Hall-Effect measurements. The similar 2DEG density and mobility in the bare and as-deposited samples imply that the deposited Al₂O₃ has no direct impact on the interface electronic properties, which are mainly controlled by the interfacial GaO_x. More importantly, the lack of any significant reduction of the GaO_x after a relatively high annealing temperature (800 °C) further implies that the decrease in the interface defect density has mostly resulted from structural changes that happen to this GaO_x layer during thermal treatment, as opposed to its elimination by the deposited Al₂O₃ as commonly perceived. The decrease of the XPS BEs for the Ga 3*d* and N 1*s* core levels after PDA may be explained by the increase of surface energy band bending arising from the reduction in the interface positive trapped charge.

6.5. Summary

The interfacial properties of Al₂O₃ on GaN-based substrate are systematically investigated in this chapter. In the first part, the physical origin of the surface band bending on Ga-face GaN is studied experimentally and theoretically. The negative bound charges at the surface that are induced by the spontaneous polarization of GaN lead to upward band bending. However, these negative charges are compensated by positively charged states associated with the formation of GaO_x, thus altering the surface band bending. It is observed that the application of a (HF) cleaning treatment to the GaN surface can effectively remove the GaO_x layer and achieve a low surface charge density. These observations are acquired using angle-resolved X-ray photoelectron spectroscopy (ARXPS). Based on a theoretical analysis of the electrostatics of the surface region, it is found that a net positive charge with a magnitude of $2.09 \times 10^{12}/\text{cm}^2$ is present on a GaN surface with a native GaO_x layer on top, whereas a net negative charge with a density of $1.0 \times 10^{12}/\text{cm}^2$ is present on an HF-cleaned GaN surface.

In the second part, the interfacial regions between the Al₂O₃ dielectric and Ga-face GaN as well as a GaN/AlGaIn/GaN heterostructure are investigated via XPS. The regrowth of the interfacial GaO_x layer occurs during the ALD process because of an increase in the Ga-O/Ga-N bond-intensity ratio following Al₂O₃ deposition. This observation is attributed to GaN oxidation, even when the thin native GaO_x layer is reduced by TMA during the initial TMA-only cycles. The valence-band offset between the GaN-based substrate and Al₂O₃, which is determined using both core-level and valence-band spectra, is observed to change with the thickness of the deposited Al₂O₃.

This observation is ascribed to an upward energy-band bending at the GaN surface and the intrinsic limitations of the XPS method for band-offset determination.

The interfacial electronic structures of Al₂O₃-capped GaN and GaN/AlGaIn/GaN are investigated using XPS and Hall-effect. The interfacial GaO_x layer formed during Al₂O₃ deposition remains nearly intact following relatively low-temperature PDA. However, after elevated-temperature annealing, the occurrence of a thermally induced structural change is observed in the GaO_x layer. The density and mobility of the 2DEG are found to decrease and increase, respectively, after PDA, indicating that a reduction in the Al₂O₃/GaN-interface defect density has occurred. These findings imply that the observed improvement in the 2DEG mobility should be ascribed to the structural change in the interfacial layer, as opposed to the notion that the improvement results from the reduction of the GaO_x by the Al₂O₃.

Chapter 7 Conclusion and recommendations

7.1. Concluding remarks

7.1.1. Investigation of HfO₂ high- κ dielectrics electronic structure on SiO₂/Si substrate

HfO₂-based high- κ gate dielectrics have been implemented in the manufacture of advanced transistors. However, because of their relatively low thermal budget, HfO₂ gate dielectrics suffer from reliability issues that lead to V_{fb} instability. A systematic investigation of the electronic structures of HfO₂/SiO₂/Si gate stacks is beneficial to understanding the origin of these issues.

In the first part of this study, HfO₂ layers of various thicknesses prepared via ALD on SiO₂/Si substrates were characterized. The formation of hafnium silicate between the HfO₂ and the SiO₂ in such structures is believed to play a key role in generating an internal electric field, which can be ascribed to V_o formation/accumulation at the interface between the SiO₂ and the Hf silicate. A thicker Hf silicate layer can accommodate more V_o , thus giving rise to a stronger internal electric field. The XPS BEs of the O 1s, Si 2p, and Hf 4f spectra shift to higher values with increasing HfO₂ thickness,

and this shift can be explained in terms of the internal electric field and the photoemission differential charges. The magnitude of the internal electric field can be obtained using the suggested method based on XPS results. Electrical measurements of the corresponding MOS capacitors support the observed XPS results.

In the second part of the study, the thermal stability of the $\text{HfO}_2/\text{SiO}_2/\text{Si}$ gate stack was investigated. The formation of Hf silicate reaches a maximum following PDA treatment at 400 °C because of the intensification of the intermixing reaction between HfO_2 and SiO_2 . Accordingly, the internal electric field reaches its largest value because of the thick Hf silicate layer. However, phase separation occurs in the Hf silicate layer when the annealing temperature is over 400 °C, resulting in the decomposition of the Hf silicate layer and a decrease in the internal electric field. V_{fb} values extracted for the corresponding MOS capacitors support the XPS results.

7.1.2. Investigation of the interface dipole of HfO_2 -based gate stacks

The internal electric field is formed by a large number of small interface dipoles comprising positively charged V_o and negatively charged oxygen ions. These interface dipoles were studied using the pulsed CV technique. Unusual hysteresis is observed while measuring the CV curve of the high- κ /metal gate stack. The CV curve obtained for negative-to-positive (forward) voltage ramping exhibits a consistently more positive V_{fb} than that obtained for positive-to-negative (reverse) voltage ramping. The relative positions of the forward and reverse CV curves are opposite to those measured using the

quasi-static voltage-sweep method. Moreover, the hysteresis is found to vary only with the voltage ramp rate, not with the voltage pulse width. These observations are attributed to lag in the interface dipole's response. An interface-dipole relaxation model that accounts for the ramp rate, the viscosity of the local oxide network, the elasticity of the dipole, and the thickness of the dielectric is proposed to characterize this hysteresis.

7.1.3. Study of the properties of the interfaces between Al_2O_3 and GaN as well as GaN/AlGaIn/GaN heterostructure

GaN-based HEMTs are promising candidates for next-generation power devices because of their superior high-frequency and high-temperature performance. Further enhancement in device performance has been achieved through the introduction of an Al_2O_3 layer between the metal gate and the underlying semiconductor.

In the first part of this study, the origin of the surface band bending of GaN was studied experimentally and theoretically. The spontaneous-polarization-induced negative charges and the positive charges generated by the interfacial GaO_x layer are considered to be the sources of this band bending. A method of extracting the surface charge density is proposed based on an analysis of the electrostatics in the surface region.

In the second part of the study, the interfacial chemistry and VBO of the Al_2O_3 /GaN interface were investigated via XPS. The regrowth of a GaO_x layer has been observed during the ALD process, which can be explained in terms of the oxidation of GaN caused by oxygen diffusion through the initially thin Al_2O_3 film. The VBO of the Al_2O_3 /GaN interface is observed to increase as a function of the Al_2O_3 thickness. This

observation is ascribed to upward band bending at the GaN surface and the intrinsic limitations of the XPS method for band-offset determination.

In the third part of the study, the effect of PDA on Al_2O_3 -capped GaN and GaN/AlGaIn/GaN interfaces was investigated via XPS and Hall-effect measurements. The interfacial GaO_x layer remains nearly intact after relatively low-temperature annealing. However, a structural change occurs in this layer during annealing at 800 °C, resulting in an uniform GaO_x interfacial layer. Interestingly, a higher mobility and a lower density of the 2DEG are observed following PDA, indicating that a reduction in the Al_2O_3 /GaN-interface defect density has occurred.

7.2. Recommendations for future study

Based on the achieved results and conclusions, the following future studies are proposed.

The gate stack with a thick SiO_2 layer was studied to obtain the interface properties. Based on the achievement, it is suggested to investigate the gate stacks with a thin or unintentional SiO_2 layer to increase the quality of HfO_2 based gate stack and reduce the EOT.

The TMA precursor for Al_2O_3 deposition can convert GaO_x into Al_2O_3 , leading to a reduction in the density of the surface states. However, the oxidant can penetrate an initially thin Al_2O_3 layer, resulting in the regrowth of GaO_x . Therefore, the process of

reducing the surface states using TMA should be optimized to obtain an interface of the highest possible quality.

GaO_x will inevitably form during ALD deposition, the improvement of the GaO_x quality by applying PDA treatments is another possible approach to reducing the defect states. However, the annealing temperature and the duration of the annealing have yet to be optimized. Therefore, much effort can be put into these aspects of improving the quality of IL.

Publications

- 1) **T. L. Duan**, H. Y. Yu, L. Wu, Z. R. Wang, Y. L. Foo, and J. S. Pan “Investigation of HfO₂ high- κ dielectrics electronic structure on SiO₂/Si substrate by x-ray photoelectron spectroscopy” *Applied Physics Letters*, Vol. 99, pp. 012902-3, 2011.
- 2) **T. L. Duan**, and D. S. Ang, “Capacitance Hysteresis in the High- κ /Metal Gate-Stack From Pulsed Measurement,” *Transactions on Electron Devices*, Vol. 60, no. 4, pp. 1349-1354, 2013.
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