Investigation of interconnect layout on CU/Low-K TDDB reliability

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**INVESTIGATION OF INTERCONNECT LAYOUT
ON CU/LOW-K TDDB RELIABILITY**

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

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INVESTIGATION OF INTERCONNECT LAYOUT ON CU/LOW-K TDDDB RELIABILITY

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ABSTRACT

As technology advances, the physical dimension of the Cu/low-k backend interconnect becomes smaller. To improve the resistance-capacitance (RC) delay, the low-k dielectric constant has to reduce further. Unfortunately, reducing the dielectric constant often comes with the price of lowering the mechanical, electrical, thermal and chemical properties of the low-k dielectric. As a result, the reliability study of the Cu/low-k dielectric system becomes vital.

This study focuses on a specific electrical reliability problem, which is the time dependent dielectric breakdown (TDDB) of low-k dielectric. Traditionally, TDDB reliability study involves stressing standard large area test structures at accelerated conditions, then extrapolating the lifetime data obtained to actual layout at use conditions. However, standard test structure is not representative of the actual patterns seen in the real circuits. Small area finger test structures were created previously to emulate real geometries found in circuits, and the breakdown mechanism of the finger test structures was studied.

Nonetheless, it is still not fully understood how the lifetime data gathered from this small area finger test structures actually relate to the lifetime data gathered from the conventional test structure. Therefore, an effort was made here to compare the data from small area finger test structures to traditional comb-comb test structures. It was found that lifetime data collected from small area test structures cannot be extrapolated to the lifetime of large area test structures and vice versa. The reason for this is most likely due to the drop in the voltage along the long metal line of the conventional comb-comb test structure, lowering the electric field in the dielectric as the metal line stretches further from the voltage source, rendering it ineffective. This is an inherent

weakness in large area test structures. Therefore, if the actual layout consists of mainly short metal lines, it is more prudent to use small area test structures instead of relying on the conventional test structures for data collection.

Along with the test structures stressed, the test conditions used during accelerated testing are not realistic compared to the actual stresses the dielectric will sustain under use condition. In real layouts, the metal lines are not isolated; hence it is important to investigate the effect on TDDB lifetime when there are other active lines in close proximity. The presence of adjacent metal lines was observed to reduce the TDDB lifetime, due to the interaction of the electric field. Through our developed model, this effect will reduce as technology scales, but only if the electric field in the dielectric can be kept constant.

Other than having close neighbouring lines, in actual circuits there will be current flowing in the metal line. This effect is also not factored in traditional TDDB testing. Current in the metal lines can lead to electromigration (EM). The reduction of the dielectric spacing due to compressive stress induced during EM was identified to be the main failure mechanism. It is important to consider this, because by not taking this effect into account during standard TDDB testing, the extrapolated breakdown lifetime at use conditions will be over-optimistic.

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CHAPTER 1: BACKGROUND AND MOTIVATION

1.1 Copper and low-k interconnect system

Moore's law observes that the number of transistors on integrated circuits doubles every two years [1]. In order to adhere to this guiding principle, physical feature size is reduced and chip size is increased to improve the packing density. Summarized in Table 1.1 is the interconnect dimension as technology improves from 40 nm technology to 22 nm technology in 2016 [2]. The total interconnect length doubles, and Metal 1 wiring pitch halves in the span of 5 years.

Table 1.1 Physical dimension of interconnect wires from ITRS 2011 [2]

	2011	2012	2013	2014	2015	2016
DRAM 1/2 pitch (nm)	40.09	35.72	31.82	28.35	25.26	22.5
MPU Physical Gate Length (nm)	24.20	22.09	20.17	18.41	16.4	15.34
Number of Metal Levels	12	12	13	13	13	13
Total Interconnect Length (m/cm ²) (Metal 1 and intermediate)	2632	3125	3704	4167	4762	5291
Metal 1						
Metal 1 wiring pitch (nm)	76	64	54	48	42	38
Metal 1 A/R (for Cu)	1.80	1.80	1.90	1.90	1.90	2.00

Scaling with the technology nodes, the reduction in the cross-sectional dimension of the metal line and dielectric spacing in the back end of line has led to a severe increase in the resistance-capacitance (RC) delay. In fact, interconnect delay for feature sizes less than 0.25 μm exceeds the gate delay, as seen in Fig. 1.1 [3].

Figure 1.1 RC delay against Technology node [3]

Time delay due to parasitic resistance and capacitance in the wires can be approximated by equation (1.1) [4]

$$t_{RC} = 2\rho k\epsilon_0 \left(\frac{4L^2}{P^2} + \frac{L^2}{H^2} \right) \text{-----(1.1)}$$

where ρ is the metal resistivity, k is the dielectric constant, ϵ_0 is the permittivity of free space, L is the wire length, P is the metal pitch and H is the height of the metal wire. Since the metal length will lengthen and metal dimension will shrink with technology, only the resistivity of wire and dielectric constant can be changed to improve the time delay.

Copper metal line and low-k dielectric materials were used to replace the traditional aluminium and silicon dioxide dielectric in the backend interconnect. Copper, with its lower resistivity of $1.7 \mu\Omega\text{-cm}$ compared to $3.0 \mu\Omega\text{-cm}$ of aluminium will naturally lower the resistance in the metal line. At the same time, copper has the added advantage of having higher activation energy for lattice and grain boundary diffusion, leading to better resistance to electromigration (EM) compared to aluminium [4, 5]. Substituting silicon dioxide, which has a dielectric constant of 3.9, with low-k materials with dielectric constants of 3 or less, reduces the capacitance. In addition to improving the RC delay, power consumption [6, 7], crosstalk between metal lines [6, 8] are also reduced with the introduction of low-k materials [6]. Power consumption is given by equation (1.2)

$$P = CV^2f \text{ --- (1.2)}$$

where C is the capacitance, V is the operating voltage and f is frequency. Replacing SiO_2 with low-k dielectrics will reduce the capacitance, which is directly proportional to power consumption according to equation (1.2).

1.1.1 Low-k dielectric materials

Low-k dielectrics can be classified into organic, inorganic or a hybrid of the two. Some of the common low-k dielectrics and their dielectric constants are summarized in Table 1.2 [7].

Table 1.2 Summary of common low-k dielectrics [7]

Dielectric constant	Organic Polymers	Hybrids	Inorganics
4.0-4.2			SiO ₂
3.0-4.0		Hydrogen silsesquioxane (HSQ)/FOX TM	Fluorinated silica (SiO _x F _y)
2.4-3.0	Flare	Methylsilsesquioxane (MSQ)/HOSP TM	
	Poly(arylene ether)	Aurora TM	
	Polyimide	Coral TM	
	Benzocyclobutene	Z3MS TM	
	SiLK	Black Diamond TM	
		Polyset TM	
		Dendriglass TM	
		Orion TM	
2.0-2.4	Porous SiLK TM	NCS TM	Nanoglass TM
	Parylene	LKD TM	
		XLK TM	
		Zirkon TM	
<2.0	Polytetrafluoroethylene		Xerogel Aerogel

Lowering of the dielectric constant can be achieved by decreasing the polarizability of the molecular bonds, or by increasing the free volume [7, 9]. Polarizability of the molecular bond of SiO₂ can be lowered by doping the materials, replacing the Si and O atoms with low polarizable atoms, such as F or C, forming fluorinated silica (FSG) and carbon-doped SiO₂ (SiOCH) respectively [10-12]. Molecular density can be reduced by substituting H with bulky side group, which will limit the packing density of the chain, thus increasing the free volume. For example, studies were done on polyimide containing bulky side groups such as fluorine [13] or a methyl substituent [14] to increase the free volume of the molecule chain, which in turn decreases the dielectric constant. To further increase the free volume of dielectric materials, pores were introduced into the structures to achieve ultra-low-k values of 2.4 and below.

1.1.2 Deposition of the low-k

Low-k materials are fabricated by two main methods, namely spin-on or chemical vapour deposition (CVD) method. A summary of the deposition method for the common low-k materials are summarized in Table 1.3 [15].

Table 1.3 Deposition Method of common low-k materials [15]

Deposition Method	Material
CVD	Fluorinated Silicate Glass
	Methylated Silica
	Parylenes
	Fluorinated Amorphous Carbon
Spin-on	Polyimides
	Hydrogen silsesquioxane (HSQ)
	Methylsilsesquioxane (MSQ)
	Fluorinated Polyimides
	Poly(arylethers)
	Thermoset Polymers
	Polytetrafluoroethylene (PTFE)
	Porous Inorganics (Xerogels, Templated Silica)
	Porous Organics

Only the deposition for dense and porous SiOCH will be touched on as SiOCH is the main dielectric in use by industry, and is also the dielectric fabricated for use in this study.

Traditionally, SiO₂ film is deposited by chemical vapour deposition dense (CVD) using silane (SiH₄) as the precursor. It is therefore not surprising that SiOCH fabrication is typically performed in radio-frequency plasma-enhanced chemical vapour deposition (RF PECVD) [16], even though it is also possible to fabricate SiOCH films by spin-on method [17]. Cyclic precursors tetramethylcyclotetrasiloxane

(TMCTS) [18] and octamethylcyclotetrasiloxane (OMCTS) [19] were found to produce films of better qualities. The deposition temperature can go up to 400°C.

Porous SiOCH can also be fabricated using PECVD. Although by simply adjusting the plasma condition will allow pores to be formed, it is more efficient to create pores by the subtractive method, which allows for better control [7, 16]. The subtractive process involves removing a fraction of the deposited film. This can be done by mixing the TMCTS precursor with a thermally unstable CH_x phase. This phase is subsequently removed during the annealing process at 400- 430°C for 4 hours, leaving behind pores. The resulting porosity and dielectric constant that can be achieved depends on the unstable phase to precursor ratio.

However, having pores will lead to many reliability issues such as leakage current, low mechanical strength, absorption of moisture and time dependent dielectric breakdown being exacerbated as the percentage of porosity increases [20, 21]. As a result, there are recent studies concentrating on non-porous ultra- and super low-k SiOCH [22, 23]. This is achieved by neutral-beam-enhanced chemical vapour deposition (NBECVD). In order to reduce the dielectric constant, the polarization of the film is minimized by controlling the ratio of Si-O bonds to Si-(CH_3)_x bonds. This control is not possible using PECVD, as collision with the electrons in the plasma causes the precursor to be too dissociated. NBECVD eliminates this problem, and hence films with the same structure as the precursor can be deposited. This allows for precise control of the structure of the resulting film.

1.2 Integration Issues of Cu/low-k Interconnect System

Although there are many benefits to be gained from the migration of Al/SiO₂ to Cu/SiOCH, there were process integration challenges that must be dealt with. That includes the fast diffusion of Cu in both silicon and oxide, which can lead to increased oxide and junction leakage, lower oxide breakdown voltage. Hence there is a need for a barrier layer to contain the copper [24-27]. Copper also has the problem of having poor adhesion to oxide. The Ta/TaN bilayer aids in this aspect, as Cu adheres well to Ta, and TaN will adhere better to the oxide [27].

Another problem is the difficulty in etching copper lines, as it does not form volatile by-products. A dual damascene process was adopted to deposit the copper metal line instead [4, 25, 28, 29]. It involves filling copper into pre-etched trench and via in the dielectric, instead of first depositing and patterning the metal, then filling with dielectric, as was done for Al/SiO₂ system.

1.2.1 Damage during processing

Due to the dual damascene process, patterning steps have to be performed on the deposited dielectric film [7, 25]. Plasma etching is used to remove dielectric and photo resist. Oxygen-based plasma can deplete the carbon in SiOCH film. It can make the film more susceptible to moisture adsorption or the formation of silanol bond, thus increasing the dielectric constant [30].

Wet cleaning is performed after via etch for dual damascene process, to remove any Cu or polymeric by-products before copper filling. However, liquid can be absorbed by the film during the wet cleaning process. Worsening the situation is the presence of

pores in the structure, making the low-k dielectric increasingly susceptible to absorption of liquid during wet cleaning and damage during plasma etching [31].

1.2.2 Deposition of Metal Diffusion Barriers

A barrier layer is necessary to prevent the diffusion of Cu, and at the same time help Cu adhere well to the dielectric. The barrier has to be thin to reduce the resistivity of the metal wire, and must be continuous to prevent Cu diffusion. This becomes more challenging as the dimensions become smaller and dielectric becomes more porous.

Atomic layer deposition (ALD) is a promising alternative deposition method to physical vapour deposition (PVD) and chemical vapour deposition (CVD). ALD film is conformal and has excellent step coverage. The starting surface must have sufficiently reactive and high enough density of the functional group to react with the precursor. If these conditions are not met, the film will not be continuous, and may contain pinholes. Another problem is the diffusion of the precursor into the dielectric during deposition [32]. This can be reduced by using precursors with large molecules, or by sealing the pores of the dielectric [7].

1.2.3 Compatibility with CMP

As mentioned, low-k dielectrics have reduced mechanical properties as compared to SiO₂. This makes the film more vulnerable to damage during chemical–mechanical polishing (CMP) [25, 33]. CMP is used to planarize the Cu after electroplating. The low strength means that the film can crack or deform during CMP. Delamination is often seen during the CMP process. This is due mainly to the weak adhesive strength between the dielectric and other layers [34].

1.2.4 Requirements on Properties of Low-k Materials

Stringent requirements on the chemical, mechanical, thermal and electrical properties of the materials have to be met to ensure successful integration of the Cu/low-k system [35, 36]. Some electric, mechanical and thermal properties of porous low-k material is summarized in Table 1.4 [37]. There were much concern regarding the thermal properties of low-k, as its thermal conductivity is only about 70% of that of SiO₂ [38]. Compared to SiO₂, low-k dielectrics have lower mechanical strength, leading to problems such as dishing and erosion of the dielectric during chemical-mechanical polishing (CMP) [39].

Table 1.4 Comparison of low-k and SiO₂ electrical, mechanical and thermal properties [39]

Property	Organic Dielectric (SiLK™)	Si _w C _x O _y H _z	Silicon Dioxide
Dielectric Constant	2.62	2.7-3.0	3.9-4.5
Leakage Current (A/cm ²) at 1 MV at 150°C	3.3 x 10 ⁻¹⁰	~1 x 10 ⁻¹⁰	~2 x 10 ⁻¹¹
Breakdown field (MV/cm)	~4	6 - 10	>8
Modulus (GPa)	2.7	9 - 15	72
Hardness (GPa)	0.25	1.3 - 2.4	8.7
Toughness (MPa-m ^{1/2})	0.62	~0.28	0.8
Thermal Conductivity (W/mK)	0.19	0.4	1.07

Low-k materials also possess poorer electrical breakdown strength as compared to SiO₂. According to the ITRS roadmap, the electric field in the interconnect will exceed 2 MV/cm within the next few generations [2]. This raises the likelihood of the dielectric failing by time dependent dielectric breakdown (TDDB). Given the impact of integration processes on low-k reliability, reliability study becomes vital.

1.3 Experimental Technique

1.3.1 Test Vehicle

Reliability studies are based on data collected from electrical characterization of the metal-dielectric system; hence this section will summarize the common test vehicles and experimental methods employed to perform the characterization.

The test vehicles are typically in a metal-insulator-metal (MIM) capacitor configuration [40]. The metals are separated by the insulator with by a dielectric spacing, s . The capacitance of the structure can be described by the equation (1.3)

$$C = \frac{k\epsilon_0 A}{s} \text{ --- (1.3)}$$

where k is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space and A is the area of the metal-insulator interface.

Two frequently used shapes are the comb-comb test structure and the comb-serpentine test structure, as depicted in Fig. 1.2.

Figure 1.2 Planar view of the (a) Comb-comb (b) Comb-serpentine test structure

During electrical stressing for the comb-comb structure, the metal line of one of the comb contacts will be stressed, while the other contact will be grounded. Similarly for the comb-serpentine, the comb contact and the serpent contact will be biased at different potential, to induce electric field in the insulator. The test structures are prepared using the same process as that in a full IC chip. The process involves deposition followed by etching of the dielectric to form the trench, after which the barrier layers are deposited by sputtering. A thin layer of Cu is sputtered, which is then used as the seed layer for electrochemical plating to fill the trench with Cu. Excess Cu is removed by CMP, and a capping layer, usually silicon carbon nitride (SiCN), will be deposited [41]. As the process is similar to that of the full IC chip, the MIM test structure can be used to study the impact of the processing on the reliability.

1.3.2 Electrical test

Voltage ramp

Voltage ramp and constant voltage stress are two of the common electrical tests performed to evaluate reliability. Voltage ramp testing involves measuring the leakage current as the stress voltage sweeps from low to high [40]. Stress voltage increases until a breakdown occurs in the dielectric, creating a path for large amount of current to flow through. Failure is often defined as the voltage where an abrupt increase of one order magnitude in the leakage current is observed [42, 43].

The conduction mechanism of charged particles in dielectrics can often be deduced from the results of this test. Further elaboration will be given in Section 1.4 on leakage mechanisms.

The ramp rate used in the testing can affect the magnitude of breakdown voltage obtained. Osburn and Ormond showed that by using a relatively slower ramp rate of 0.05 MV/cm·s compared to a higher ramp rate of 2.0 MV/cm·s, the breakdown voltage decreased by around 7%. They attributed the faster breakdown to subjecting the dielectric to longer times at the high temperature [43]. Studies have been done on varying the ramp rate applied [44-46]. Haase [44] and Cheng [45] looked at the effect of varying voltage ramp on different metal line width and dielectric spacing. Plawsky [46] used the different voltage ramp to differentiate between intrinsic and extrinsic failures of the low-k dielectric by analyzing the slope of the I-V curve.

Constant voltage stress

Constant voltage stress is also known as time dependent dielectric breakdown (TDDB), or bias temperature stress (BTS). It involves applying a constant potential difference between two electrodes while measuring the leakage current over a period of time until failure occurs, often conducted at a single elevated temperature [40].

From this test, breakdown lifetime data is gathered, and used for further reliability studies. Section 1.5 will elaborate on this methodology of reliability study.

1.4 Leakage Mechanisms in Cu/low-k Interconnect System

Ideally, the perfect insulator should exhibit zero conductance, but in reality, all insulators will show some degree of carrier conduction if the electric field or temperature is high enough.

Schottky emission and Poole-Frenkel conduction [47-52] are by far the most common conduction mechanisms observed in low-k dielectric, although ohmic conduction [41, 53, 54] and space-charge-limited conduction (SCLC) [47-49] were also found in some low-k materials.

Schottky emission (SE), also known as thermionic emission, is the injection of electrons from the metal contact into the dielectric under thermal excitation. It is controlled by the equation

$$J = A^* T^2 \exp \left[\frac{-q \left(\Phi_B - \sqrt{\frac{qE}{4\pi k \epsilon_0}} \right)}{k_B T} \right] \text{-----} (1.4)$$

where A^* is the effective Richardson constant, T is the temperature, Φ_B is the potential barrier height, q is elementary charge, E is the electric field, ϵ_0 is the permittivity of free space and k_B is the Boltzmann constant. Electrons that have sufficient energy to jump across the potential barrier will contribute to the current density. The potential barrier is the difference between the metal work function and the electron affinity of the dielectric. When an external electric field is applied, the potential barrier decreases by $\sqrt{qE/4\pi k \epsilon_0}$, with an image potential correction. To check if the conduction mechanism fits to SE, $\log(J)$ is plotted against $\sqrt{E}$. The k value is then extracted from the slope. If the k value extracted is the same as the dielectric constant, the conduction mechanism is determined to be SE. SE is a surface-limited process.

Poole-frenkel (PF) conduction mechanism, on the other hand, is a carrier-transport limited process. It is related to the field-enhanced, thermal excitation of electrons in dielectric with intrinsic traps. The columbic traps attract electrons, and electrons conduct by jumping from trap to trap. The current density follows the equation

$$J \propto E \exp \left[\frac{-q \left(\Phi_B - \sqrt{qE/\pi k \epsilon_0} \right)}{k_B T} \right] \text{-----} (1.5)$$

Similar to SE, an external field can reduce the barrier height Φ_B . To check if the conduction mechanism is PF, $\log(J/E)$ is plotted against $\sqrt{E}$. k value can be extracted from the slope of this graph, and compared to the dielectric constant used for the testing.

Ohmic conduction is seen when temperature is high and electric field applied is low. Thermally excited electrons hop from one isolated state to another. This mechanism is exponentially dependent on the temperature. In low- k materials, this mechanisms was exhibited in the electric fields ranging of <0.2 MV/cm by [53], $0.25 - 0.5$ MV/cm by [41] and < 1 MV/cm by [54] when tested on conventional comb-comb test structures.

SCLC occurs in insulators or semiconductors containing trapped charges. The presence of the trapped charges inhibits the injection of incoming charge carriers. This conduction mechanism was seen in polymeric low- k , benzocyclobutene (BCB) [47] and methyl-silsesquiazane (MSZ) [48]. It has also been suggested by Chen [49] that SCLC mechanism can happen in porous ultra-low- k when the Ta barrier is defective.

Fowler-Nordheim and direct tunnelling are conduction mechanisms that occur most frequently in thin dielectrics such as MOS gate oxide [7, 55]. Interconnect dielectric is relatively thick and thus both tunnelling mechanisms are unlikely to occur, and hence will not be discussed in detail.

Summarized in Table 1.5 and Fig. 1.3 are the basic conduction mechanisms found in dielectrics [40, 56].

Table 1.5 Basic conduction mechanisms [40, 56]

Conduction Mechanism	Equation
Schottky emission	$J = A^* T^2 \exp \left[\frac{-q(\Phi_B - \sqrt{qE/4\pi k \epsilon_0})}{k_B T} \right]$
Poole-Frenkel emission	$J \propto E \exp \left[\frac{-q(\Phi_B - \sqrt{qE/\pi k \epsilon_0})}{k_B T} \right]$
Direct tunnelling	$J \propto E^2 \exp \left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3qhE} \right]$
Fowler-Nordheim emission	$J \propto E^2 \exp \left[\frac{-4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E} \right]$
Space-charge-limited current	$J = \frac{8k\mu V^2}{9d^3}$
Ohmic	$J \propto E \exp \left(\frac{-\Delta E_0}{k_B T} \right)$
Ionic conduction	$J \propto \frac{E}{T} \exp \left(\frac{-\Delta E_0}{k_B T} \right)$

Figure 1.3 Energy band diagrams of conduction mechanism for (a) direct tunnelling, (b) F-N tunnelling, (c) Schottky emission and (d) PF conduction [56]

1.5 Interconnect Reliability

Reliability is defined as the ability of the system to perform its function under a set of conditions for a specified length of time. In the context of low-k dielectric reliability, this means that the low-k dielectric must be able to function as an insulator under use

temperature and voltage for a minimum ten years [57]. SiO₂ interconnect was capable of lasting for 10 years under an electric field of 2 MV/cm under a temperature of 100°C [58].

The bathtub curve is widely used to describe lifetime reliability engineering [59]. The curve is shown in Fig. 1.4. It describes the failure rate of semiconductor devices over time. The curve is divided into three distinct sections: infant mortality, constant failure rate and wear-out regions. Infant mortality is also known as early failure rate region. Failures in this region are associated with gross defects, usually caused by manufacturing defect. Failure in this region decreases with time. The second region is also known as the random failure region. Failure in this region is low and constant with time. The failures could be due to small defects, or due to external stresses such as random electrostatic discharge (ESD). The final region is the wear-out region, where the failure increases with time as the devices degrade.

Figure 1.4 Bathtub curve describing failure rate of devices over time

1.5.1 Accelerated testing

Lifetime reliability is a measure of how long a device can perform its function under certain conditions. However, under normal use conditions, the device can last for decades. It is therefore more practical to use accelerated conditions for testing and obtaining lifetime results, then extrapolate the lifetime under accelerated conditions to lifetime under use conditions using accelerated models [57]. Typical acceleration conditions include temperature acceleration, voltage acceleration, humidity, mechanical pull and radiation, to name a few. Important extrapolations for dielectric reliability accelerated testing include temperature and voltage, area scaling and transformation to target percentile [60]. Target percentile is typically set at 0.1% to ensure highly reliable products [57]. Voltage, temperature and area transformation will be described in detail as they are relevant to the current study. Graphical representation of the transformation is illustrated in Fig. 1.5.

Figure 1.5 Main transformations performed for dielectric reliability accelerated testing [60]

Temperature acceleration

Most failure mechanisms have temperature dependence and hence can be accelerated by elevated temperature [61, 62]. The temperature dependence typically follows the Arrhenius equation, shown in equation (1.6)

$$\text{Reaction Rate} \propto \exp\left\{\frac{-E_a}{kT}\right\} \quad (1.6)$$

where E_a is the activation energy, k is the Boltzmann constant and T is the temperature.

Since time to failure, τ , is proportional to $\frac{1}{\text{Reaction Rate}}$, therefore

$$\tau = A \exp\left(\frac{E_a}{kT}\right) \quad (1.7)$$

where A is a constant. Letting the accelerated stress temperature be T_{stress} , the lifetime obtained from the testing is τ_{stress} . Assuming the use temperature is T_{use} , the predicted lifetime under use conditions will be τ_{use} . Temperature acceleration factor AF_T can then be described by the equation

$$AF_T = \frac{\tau_{use}}{\tau_{stress}} = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)} \quad (1.8)$$

Voltage Acceleration

Lifetime dependence of dielectric on voltage can be described by the Eyring model [62]

$$\tau = A \exp\{-V_s \times \gamma\} \text{ --- (1.9)}$$

where A is a constant, V_{stress} is the stress voltage and γ is the voltage acceleration factor.

Letting τ_{stress} be the lifetime obtained under V_{stress} , τ_{use} will be the lifetime obtained under V_{use} , which is the voltage under use conditions. The voltage acceleration factor, AF_v will be written as

$$AF_v = e^{\gamma(V_{stress}-V_{use})} \text{ --- (1.10)}$$

Area scaling

Although strictly not an accelerated testing condition, as area used in test structures are actually smaller than actual layout, area scaling is nevertheless a transformation necessary to relate and predict lifetime of actual IC chips using data gathered from test structures. Typical test structure length can range from 0.02 m to 2 m [63, 64]. In a 1 mm by 1 mm 32 nm IC chip, the interconnect length can go up to 37 m, according to the ITRS roadmap [2]. Hence, statistical models are necessary to predict the breakdown lifetime of circuits at use conditions from test structures at accelerated testing.

Area scaling effect has been extensively studied [65-70], the most commonly used model to extrapolate the lifetime with respect to area is the Poisson area scaling law. The derivation of the law is as follows.

Poisson defect distribution is assumed over the area, and is given by the equation

$$F = 1 - \exp\left(-\frac{D}{A}\right) \text{-----} (1.11)$$

where F is the cumulative probability failure, D is the defect density and A is the area of the device. Poisson defect distribution assumes that the defects are randomly distributed and are independent point defects, such as particle contamination [5]. The cumulative failure distribution F_2 for a device with an area A_2 , can be expressed by the following distribution with respect to the cumulative failure F_1 of another device with an area A_1

$$F_2 = 1 - (1 - F_1)^{\frac{A_2}{A_1}} \text{-----} (1.12)$$

Assuming the lifetime of the device follows the Weibull distribution, the failure time can be expressed by Weibull cumulative distribution equation, yielding

$$TF_2 = TF_1 \cdot \left(\frac{A_2}{A_1}\right)^{-\frac{1}{\beta}} \text{-----} (1.13)$$

where β is the shape factor, TF is time to failure and A is the area. Using equation (1.13), we can extrapolate the lifetime of the test structure to that of the real structure. There are several underlying assumption made for this equation. First is that the defect density is the same for both devices. The shape factor is assumed to be the same for both devices and lastly, the breakdown lifetime must occur under the same electric field stress.

When the test structures are stressed at elevated temperature and voltage, and has a different area compared to actual IC chips, all three transformations are present and must be taken into account. The formula used to predict the lifetime under use conditions from the lifetime under accelerated conditions will be as follows

$$TF_{use} = AF_T \times AF_V \times Area\ Ratio \times TF_{stress} \text{ --- (1.14)}$$

1.5.2 Data Analysis

The breakdown of the dielectric has a statistical nature. Often a large number of samples are tested under the same conditions, a range of breakdown lifetime will be collected, and therefore a statistical distribution function is necessary to describe the distribution of the time-to-failures.

The two most commonly used distributions to describe dielectric lifetime is the Weibull distribution and the lognormal distribution [60].

Weibull distribution

Weibull is a ‘weakest link’ type distribution, which means that once failure occurs at one particular site, the entire system will fail [67, 71, 72]. This is in accordance with the physical failure mechanism of dielectric breakdown, where a failure occurring at a single defect will cause the entire dielectric to suffer catastrophic failure. The Weibull probability distribution function is given by the equation

$$f(t) = \left(\frac{\beta}{\alpha}\right) \left(\frac{t}{\alpha}\right)^{\beta-1} \exp\left[-\left(\frac{t}{\alpha}\right)^\beta\right], t > 0 \quad (1.15)$$

where t is the time, α is the characteristic breakdown lifetime at the 63.2 percentile, and β is the shape parameter. The probability distribution function can be used to estimate the probability of failure occurring within a specified time interval. By integrating the probability distribution function, the cumulative failure distribution takes the form

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\alpha}\right)^\beta\right] \quad (1.16)$$

It describes the fraction of device population that would have failed by time t . Equation (1.16) can be linearized into

$$\ln[-\ln(1 - F)] = \beta \ln(t) - \beta \ln(\alpha) \quad (1.17)$$

Equation (1.17) is frequently used in the Weibull plot, where $\ln[-\ln(1 - F)]$ is plotted against $\ln(t)$. $\ln[-\ln(1 - F)]$ tends to zero when F is approximately 0.632. Hence α is the characteristic time when 63.2% of the devices fail. The shape parameter β will be the slope of the plot. The entire bathtub curve can be described using the Weibull cumulative failure distribution. When $\beta < 1$, the failure rate is decreasing, it describes the infant mortality region. For $\beta = 1$, the failure rate is constant and hence refers to the constant failure region. When $\beta > 1$, it represents the wear-out region.

Lognormal distribution

Lognormal probability distribution function is given by [67, 71, 72]

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma t} \exp \left[- \left(\frac{\ln t - \ln t_{50}}{\sigma\sqrt{2}} \right)^2 \right] \text{-----} (1.18)$$

The cumulative distribution function is

$$F(t) = \frac{1}{\sqrt{2\pi}\sigma} \int_{-\infty}^{\ln t} \exp \left[- \left(\frac{\ln t - \ln t_{50}}{\sigma\sqrt{2}} \right)^2 \right] d(\ln t) \text{-----} (1.19)$$

Although lognormal distribution is sometimes used to analyze the dielectric breakdown lifetime [73], there is little physical justification for using it. Contrary to the Weibull distribution, which is a ‘weakest link’ distribution, lognormal distribution is a wear-out over time distribution. For this reason, it is generally used to describe the electromigration lifetime distribution, which is a wear-out failure mechanism. Also, Weibull distribution scales with area scaling, similar to TDDB breakdown, while lognormal does not. Hence although there are instances where lognormal distribution can fit the TDDB lifetime distribution just as well as Weibull distribution, Weibull is more commonly used for TDDB lifetime distribution.

Several assumptions are made during reliability testing [57]. The first is that the variation in the test results is random and independent. The second assumption is that the sample size taken is representative of the population. The last assumption is that the discrete results (i.e. lifetime) obtained can be represented by a continuous function (Weibull, lognormal).

1.5.3 TDDDB Models

Dielectric breakdown occurs when a critical defect density is reached. When sufficient number of traps accumulates in the dielectric, a percolative path forms and connects the cathode and anode. Current flows through this path, shorting the two electrodes.

There are several TDDDB models developed by various groups for Cu/low-k interconnect system. The differences between the models are in the type of defects that accumulates, as well as the mechanism by which the defects forms. The most commonly used model is the E model and $\sqrt{E}$ model.

The thermochemical E model is based on the thermal bond-breakage mechanism under the application of an external electric field [74]. The external electric field stretches the polar molecular bond, weakening them and therefore becomes more prone to breakage, lowering their activation energy. Failure occurs when sufficient broken bond forms a percolative path from the cathode to anode. Equation (1.20) describes the breakdown time of the dielectric.

$$t_{bd} = A_0 \cdot e^{\frac{\Delta H}{k_b T}} = A_0 \cdot \exp\left(\frac{\Delta H_0 - \rho_{eff} \cdot E}{k_b T}\right) = A_0 \cdot e^{\frac{\Delta H}{k_b T}} \cdot e^{-\gamma E} \text{ --- (1.20)}$$

where A_0 is a material-dependent constant, ΔH is the activation energy, ΔH_0 is the zero-field activation energy, ρ_{eff} is the effective dipole moment, k_b is the Boltzman constant, T is the temperature in K, and γ is the field acceleration parameter.

The proposed physical mechanism for the $\sqrt{E}$ model by Chen is the electron-fluence driven, Cu-catalysed SiCOH breakdown, as illustrated in Fig. 1.6 [75]. This model is described by the equation

$$t_{bd} \propto \exp \left[\frac{1}{k_B T} (E_D + 2\varphi_s - 2\beta_s \sqrt{E}) \right] \text{--- (1.21)}$$

where $\beta_s = (q^3/4\pi\epsilon_0\epsilon)^{1/2}$, φ_s is the contact potential barrier, E is the electric field and k_B the Boltzmann constant.

Fig. 1.6 illustrates the failure mechanism proposed by Chen [75]. Electrons are injected from the cathode following Schottky emission, and transported through the dielectric. Some electrons are thermalized by the high field and high temperature, gaining enough energy to ionize the Cu atoms at the anode into Cu^+ ions. Cu^+ is then injected into the dielectric, damaging it. The ions then recombine with electrons to form Cu atoms. As the concentration of Cu reaches a critical level, it can form connected clusters to cause a short.

Figure 1.6 Energy band diagram showing failure mechanism proposed by Chen [75]

Power law model was proposed by to model the breakdown lifetime for dielectrics with dielectric constant between 2.5 to 3.2 [76]. Power law model [57, 77-79] is described by equation (1.22)

$$t_{bd} \propto V^n \text{ --- (1.22)}$$

where V is voltage and n is the power law exponent.

1/E model is based on high energy hole-induced damage and is often used to model gate oxide lifetimes [80, 81]. [82] observes that when Cu is fabricated directly on top of SiO₂, the lifetimes fits the 1/E model. 1/E model is described by equation (1.23)

$$t_{bd} \propto \exp\left(\frac{\gamma}{E}\right) \text{ --- (1.23)}$$

where γ is the acceleration factor and E is the electric field.

1.6 Motivation and Objective

As mentioned earlier, the area used in the TDDB test structure is very different from the dielectric area in the real IC chips. Not only is the area very distinct, so is the layout geometry of the test structure and actual layout design. A schematic diagram of the test vehicle was given in Fig. 1.2. They consist of long parallel line, with dielectric sandwiched in between metal lines. A study was done on the layout geometry of the actual circuit interconnect designs. Other than long parallel lines, they also contain head-to-head, head-to-line shapes [83, 84]. A scanning electron microscope (SEM) image of Metal 1 circuit layout is shown in Fig. 1.7. The conventional test structures

are not representative of the actual layout in IC chips. Small area finger test structure was designed and tested by Tan [85], which is one of the common geometry seen in the actual layout design. Due to the difference in geometry and area between the small area and conventional test structures, more study should be done to understand how the data gathered from the small area test structures relate to the conventional structure.

Figure 1.7 SEM image of Metal 1 circuit layout showing different geometries [86]

It was pointed out by Muraka [9] that interaction with the surrounding is one of the failure mechanisms for dielectric breakdown. Failure mechanisms could be broadly classified into intrinsic and extrinsic failures. Intrinsic failure mechanisms consist of inherent weakness in the thermal, chemical, electric properties of the low-k dielectric.

Extrinsic factors that could lead to failure include defects generated during process integration, such as scratching during CMP or damage during plasma. Extrinsic factors such as interaction with the environment can also lead to premature failure. Although this environment usually refers to the atmosphere in which the IC chip is placed in, such as high humidity or high temperature ambience, the micro-environment of the device-under-test should be taken into consideration as well. Unlike TDDB test structures, metal lines and dielectrics in the real layout are seldom isolated. Having a dense structure in the IC chip raises the likelihood that there will be other active lines nearby. Electric fields generated by different metal lines can overlap and interact, thus affecting the dielectric breakdown lifetime.

Moreover, unlike TDDB testing where a single DC voltage is biased for a metal electrode so that the entire electrode is at the same potential, in real circuits there will be current running in the metal lines. Having current in the metal line will bring about another common reliability problem in the backend interconnect, which is electromigration (EM) in the metal lines [87]. There is little understanding on the effect of one reliability issue on another. It was highlighted in ITRS 2011 that there is inadequate knowledge on the interaction between different reliability failure mechanisms, such as between EM and stress-induced voiding (SIV), and between TDDB and EM [2].

1.6.1 Objective

The objective of this thesis is to investigate the effect of the test structure layout on the TDDB lifetime when

- the area of the test structure is different

- neighbouring wires are in close proximity
- current is flowing in the long electrode metal line

1.6.2 Thesis Scope and Organization

This thesis consists of five chapters, and is organized as follows: Chapter 1 provides the overview of the Cu/low-k interconnect system, the background on reliability study methodology along with the motivation and objective of this project.

Chapter 2 presents the results for area scaling of the finger test structures, intermediate test structures as well as comparison to comb-comb test structures.

Chapter 3 focuses on the findings for field interaction between adjacent metal electrodes. TDDB lifetime data is presented; an empirical formula is proposed to calculate the effective electric field that takes into account the nominal electric field together with the interaction electric field.

Chapter 4 concentrates on the effect of electromigration on TDDB lifetime. The physical failure analysis is shown, and a method is proposed to qualitatively relate the compressive stress in the metal anode to the TDDB lifetime.

Finally, Chapter 5 summarizes the key findings, and suggests the future work for furthering this study.

CHAPTER 2: AREA SCALING

As covered in Chapter 1 on the reliability models, electrical testing and statistical data are collected from test vehicles such as comb-comb structures and comb-serpentine structures under accelerated conditions. These test structures will not have the same area as the actual IC chips; hence there is a need to use area scaling models to predict the lifetime of the actual IC chips using the lifetime data gathered from test structures.

2.1 Introduction

2.1.1 Small area test structure

Conventional comb structures are convenient for statistical testing of TDDDB because of their large area. They are able to capture failures due to process integration [25]. However, the shape of the comb may not be representative of the shapes found in actual layout. Finger structures were designed by Tan to emulate possible structures that can be seen in actual layout. A study of the layout geometry and their effect on breakdown lifetime was also done by Bashir [83]. Fig. 2.1 shows the geometries that are present in the actual layout, aside from parallel line. Their study confirms that the irregular geometries affect the failure times of the dielectric [83, 84].

Figure 2.1 Geometries found in actual layout [83]

Tan's small area test structure also has the advantage of confining the breakdown path, making it convenient for physical failure analysis as it fits the size of a transmission electron microscope (TEM) sample, allowing the challenging fault localization procedures to be omitted [54, 88].

Two different types of test structures were designed. They are the finger structure and corner structure, shown in Fig. 2.2(a) and (b) respectively.

Figure 2.2 (a) Finger structure (b) corner structure [54]

Voltage ramp tests and TDDB stressing were done on these 2 structures. It was found that delamination was the main mode of failure for both structures. Fig. 2.3(a) is the TEM image of the finger structure after voltage ramp testing. Delamination was found between the capping layer and the low-k layer. For the corner structure shown in Fig. 2.3(b), similar delamination was found, with occasional debonding in the dielectric and undoped silicate glass (USG) buried capping layer. No copper was observed to have diffused into the dielectric region.

Figure 2.3 TEM image of (a) finger structure and (b) corner structure after voltage ramp tests [54]

Delamination at the same region was also found after TDDB tests. In addition to the delamination, minor burn marks and copper diffusion were also found, as seen in Fig.

2.4. The breakdown was similar for both finger and corner structures.

Figure 2.4 TEM image after TDDB testing [54]

2.2 Comb-comb and Finger Test Structures

In this study, the small area finger test structure designed by Tan was extended to investigate the effect of area scaling on the reliability of small areas. The electrical data of conventional comb-comb structure can be used as a reference to see how the finger structure performs with respect to the comb structures.

2.2.1 Experimental Details

The schematic diagrams and SEM images of the finger test structures and comb-comb test structures are given in Fig. 2.5. There are three small area finger test structures, namely the 1 finger, 5 fingers and 10 fingers test structures. The schematic diagram of the three finger test structures are shown in Fig. 2.6. Each finger of the test structure is $0.2\ \mu\text{m}$ wide, with a $0.1\ \mu\text{m}$ dielectric spacing between opposing fingers. The distance between each finger is $19\ \mu\text{m}$, which is far enough to ensure no interaction between the electric fields. Fig. 2.7 is a TEM image of the cross-section of the finger test structure. The comb structure is $0.615\ \text{m}$ long, with a dielectric spacing of $45\ \text{nm}$. The area ratios of the comb and finger structures are summarized in Table 2.1. Finger test structures have a dielectric spacing of $0.2\ \mu\text{m}$, while comb-comb test structures have a dielectric spacing of $45\ \text{nm}$.

Figure 2.5 (a) Schematic planar view and (b) SEM planar view of comb-comb test structure (c)

Schematic planar view and (d) SEM cross section image of finger test structure

Figure 2.6 Planar schematic of (a) 1, (b) 5 and (c) 10 finger test structures

Figure 2.7 TEM cross section image of finger test structure

The wafers were fabricated using 45 nm technology. The low-k dielectric in the test structures is SiOCH, which has a dielectric constant of 2.7. The copper metal line with 170 nm thickness, has a Ta/TaN barrier layer of 11 nm, and SiCN as the capping layer with a thickness of 6 nm.

Table 2.1 Summary of the finger test structures and comb-comb test structure area ratio

	Comb structure	Finger test structures		
		1 finger	5 fingers	10 fingers
Area Ratio	2.73×10^6	1	5	10

Commonly used ramp rate ranges from 0.6 V/s to 1.0 V/s for low-k interconnect [40, 89, 90]. In this study, a voltage ramp of 1 V/s was applied during the voltage ramp tests. Voltage was ramped from 0 V to 100 V. A single ramp rate was used on all the test structures to make the breakdown voltages obtained comparable. Test temperature for all test structures was set at 70°C, 100°C and 140°C.

As a guideline, the stress voltage chosen is around 80% of the breakdown voltage, which is low enough so that immediate failure does not occur, and at the same time high enough to ensure that failure occurs within a reasonable length of time. For finger structures, TDDB was conducted at 5.5 MV/cm, 6.25 MV/cm and 6.5 MV/cm. For comb structures, the dielectric was stressed at 2.94 MV/cm, 3.02 MV/cm and 3.96 MV/cm. 12 devices were tested for each experimental condition. Failure criteria for both finger and comb test structures were taken to be the voltage where an abrupt increase in leakage current of one order in magnitude occurs. For comb-comb test structures, no abrupt increase in leakage current was observed; hence a leakage current of 10 nA was taken to be the failure criteria. TDDB testing was also conducted at temperatures of 70°C, 100°C and 140°C.

All electrical testing was conducted on Agilent HP4156C semiconductor parametric analyzer at the wafer level. Sourcing and measuring were done using the high resolution source-measurement unit (SMU). The analyzer is capable of measuring up to 1 femto ampere resolution.

2.2.2 Results and discussion

Breakdown Field

Results on breakdown voltage were obtained from ramp voltage testing. Shown in Fig. 2.8 are examples of the results from voltage ramp tests of comb and 10 finger test structures at 100°C. As can be seen, comb-comb test structures with its larger test area will have much more leakage path, leading to the higher leakage current as compared to finger test structures. The breakdown voltages for the different structures are given in Table 2.2. As expected, larger area structures have lower breakdown voltages.

The breakdown trend seen in finger test structures and comb-comb test structures are different. In finger test structure, leakage current increases with time, until catastrophic breakdown occurs, as characterized by the abrupt more than one order increase in current magnitude. However for comb-comb test structures, no such jump in current was seen. The leakage current increases gradually with stressed voltage, indicating the breakdown is soft breakdown as opposed to hard catastrophic breakdown. The larger area of comb-comb test structure allows it to capture multiple defects. Hence the current will be distributed to numerous leakage paths; this could be the reason for the soft breakdown observed.

Figure 2.8 Plot of leakage current against electric field for (a) fingers and (b) comb-comb test structures

Table 2.2 Summary of breakdown voltage of finger and comb-comb test structures

Test Structure	Breakdown electric field at 100°C (MV/cm)
Comb structure	4.04 ± 0.13
10 fingers test structure	8.20 ± 0.89
5 fingers test structure	8.60 ± 0.46
1 finger test structure	9.00 ± 0.62

To determine the breakdown mechanism of both types of structures, the voltage ramp results were fitted to various conduction mechanisms including Schottky Emission (SE), Poole-Frenkel (PF) emission, and ohmic conduction mechanism. The closest fit obtained was for the SE, where $\ln(J)$ was plotted against $\sqrt{E}$ curve. SE is the result of electrons overcoming the potential energy barrier between the metal and the dielectric. The curve is shown in Figure 2.9. The dielectric constant was extracted from the slope of the curve was 2.98, which is relatively close to the 2.7 of the SiOCH dielectric constant in our test structures. Hence, it is believed that comb structures conduct mainly by Schottky emission.

Figure 2.9 Schottky emission plot for comb-comb test structures

Similar to the comb-comb test structure, the conduction mechanism for the finger test structures were also determined to be Schottky emission. Plotted in Fig. 2.10 is the $\ln(J)$ versus $\sqrt{E}$ curve. The k value extracted from this curve is 2.28, which is also relatively close to the dielectric constant of the 2.7 of the low- k material.

Looking at the profile of the I-V curves in Fig. 2.8, the curve is relatively straight. It shows no significant change in the gradient of the plot. Neither of the finger test structures or comb-comb test structure exhibits a change in conduction mechanism from Schottky emission to Poole-Frenkel emission as was often seen in Cu/low- k interconnect systems [47].

Figure 2.10 Schottky emission plot for finger test structures

Breakdown lifetime

Fig. 2.11 shows examples of leakage current curve for finger and comb-comb test structures plotted against time. The comb was stressed at 3.02 MV/cm while the finger test structures at 6.5 MV/cm, at 100°C. The leakage current trend for both types of structure is similar, showing an initial decrease in the leakage current, followed by an abrupt increase indicating hard breakdown. Very little increase in leakage current was observed prior to the jump, which implies that no soft breakdown was happening.

Figure 2.11 Leakage current against time plot for fingers and comb-comb test structures

The breakdown lifetime results were collected and plotted into Weibull plots to extract the characteristic lifetime and shape parameter. Figure 2.12 shows the Weibull plots of the finger structures as well as the comb structure. Finger structures were stressed at 6.5 MV/cm at 100°C. Comb structure was stressed at 3.02 MV/cm at the same temperature of 100°C. Beta values extracted from all structures is summarized in Table

2.3. Comparing the beta value for the test structures is important because as mentioned earlier in Section 2.1, the Poisson area scaling law makes the assumption that the beta values for the different test structures with different areas will have the same beta value. Beta values for finger test structures fall in the range of 1.44 to 1.85. The beta value for the comb structure is 1.41. Both comb and finger structures show similar beta values. When the beta value is more than one, it shows that the devices under tests are in the wear-out region, where failure rate will increase with time.

Figure 2.12 Weibull plot of failure times from finger test structure (6.5 MV/cm) and comb test structures (6.5 MV/cm), at 100°C

Table 2.3 Summary of beta values extracted from Weibull plot

Test Structure	Beta values
Comb structure	1.41 ± 0.14
10 fingers test structure	1.85 ± 0.29
5 fingers test structure	1.44 ± 0.13
1 finger test structure	1.59 ± 0.10

Fig. 2.13 shows the experimental results of all 3 finger structures at various electric fields; 5.5 MV/cm, 6.25 MV/cm, 6.5 MV/cm at 100°C. Each line represents a different electric field. As can be seen from the curves, the lifetimes from 1 finger, 5 fingers and 10 fingers test structures form a linear relationship with the area ratio, showing that the three different areas do indeed adhere to the Poisson area scaling law.

Figure 2.13 Breakdown lifetimes plotted against area ratio for finger test structures under electric fields of 5.5 MV/cm, 6.25 V/cm and 6.5 MV/cm

In order to compare the breakdown lifetimes of finger test structures to that of comb-comb test structure, lifetimes obtained from finger test structures must be extrapolated to the same electric field as the comb-comb test structure. Extrapolation of the lifetime was performed using four different breakdown models, which includes the E model, $\sqrt{E}$ model, $1/E$ model and the power law. All these models were discussed in details in Section 1.5.3 of this thesis. The equations for the various models and the constants that were extracted are summarized in Table 2.4.

Table 2.4 Summary of breakdown model equations and constants used in extrapolation of finger test structures lifetime

TDDDB models	Equations	Constants
E model	$\ln TF \propto \frac{\Delta H_0}{k_B T} - \gamma \cdot E$	$\gamma = 1.29 \text{ cm/MV}$
$\sqrt{E}$ model	$\ln TF \propto \frac{\Delta H_0}{k_B T} - \gamma \cdot \sqrt{E}$	$\gamma = 6.27 \text{ cm/MV}$
Power law	$TF \propto E^{-n}$	$n = 7.63$
$1/E$ model	$\ln TF \propto \frac{Q}{k_B T} + G \cdot \frac{1}{E}$	$G = 45.1 \text{ cm/MV}$

Fig 2.14 shows the results of the lifetime extrapolation for the finger test structures using the four breakdown models, under a low electric field of 3.02 MV/cm, which is the same as the one used in stressing comb-comb test structures.

The beta value calculated from comb test structure is 1.41 ± 0.142 . The uncertainty in the lifetime estimation value for comb test structure is captured in Fig 2.14 where the beta value of $\beta_{\max}$ and $\beta_{\min}$ are considered. The plotted line for $\beta_{\max}$ represents the shortest possible lifetime estimation obtained from the experimental lifetime data. When the comb structure lifetime is used to extrapolate to the same area as a 1 finger test structure using the Poisson area scaling law, more than 5 orders in magnitude of

over-estimation in the breakdown lifetime was obtained. This could mean that either the finger test structures had failed prematurely or the comb-comb structure was not failing as fast as expected.

The shorter-than-expected breakdown lifetime of the finger test structures may be attributed to the field enhancement caused by the shape of the structure [54, 91]. The nominal electric field used for calculation was obtained from the design spacing, but in fact, the electric field in the dielectric is strongly dependent on the shape of the electrodes. Hence the actual electric field experienced by the comb-comb test structure and the finger test structure was not 3.02 MV/cm. Hence the assumption that Poisson area scaling law makes, which requires that the dielectric breakdown lifetime must be obtained under the same electric field, cannot be upheld. In order to investigate the field enhancement quantitatively, finite element modelling (FEM) simulation of the electric field induced by the actual physical image of the test structures was used.

Figure 2.14 Breakdown lifetime against area ratio plot for comb-comb and finger test structures using nominal electric field at 3.02 MV/cm and 100°C

Temperature Split

A temperature split experiment was performed for the finger test structures at the stress field of 6.5 MV/cm. The lifetime was recorded for a stress temperature of 70°C, 100°C and 140°C. The results of this experiment are shown in Fig 2.15.

Figure 2.15 Plot of breakdown lifetimes at temperatures 70°C, 100°C and 140°C, at 6.5 MV/cm

As expected, the breakdown lifetime of the dielectric becomes shorter as the stress temperature is increased. The TDDB activation energy extracted from the best fit slope from the all the data points from 1 finger, 5 fingers and 10 fingers test structure is 0.36 eV.

2.2.3 FEM Simulation of Electric Field

A software COMSOL Multiphysics was used to simulate the electric field in the test structures. In order to obtain an accurate electric field simulation in the dielectric, the physical shape of the metal electrodes used is paramount. To obtain an exact picture of the shape of the metal electrodes, planar SEM and TEM images of the comb-comb and finger test structures were acquired respectively. The SEM and TEM images, together with the corresponding electric simulation obtained are shown in Fig. 2.16.

As mentioned, the nominal electric field obtained from the designed spacing for all the test structures is 3.02 MV/cm. For the finger test structures, the electric field enhancement is caused by the curving at the ends of the metal lines, while the field enhancement for the comb-comb test structure arises from the line edge roughness on the sides of the metal line, as seen from Fig. 2.16 (b) and (d), respectively. Studies have shown that severe field enhancement often arises at the ends of the metal line in comb-comb and comb-serpentine test structure, which becomes the site of initiation for failure to occur [92, 93]. Such is not the case for this study, because the metal is pulled back at the metal tip, leaving a dielectric spacing that is twice as large as the dielectric spacing in the test area. This pull-back can be seen from the SEM image in Fig. 2.16 (f).

The FEM electric field simulations corroborates that the maximum electric field of the comb-comb test structure and finger test structures are different, and they are both higher than the nominal electric field of 3.02 MV/cm. In the actual test structures, the dielectric spacing is not sandwiched between two planar electrodes, this leads to non-uniform electric field in the dielectric. For the finger test structures, all the metal tips are of the same shape, and the maximum electric field extracted from the simulation is 10.7 MV/cm. For the comb-comb test structure, simulations were performed for the comb tips and in the middle of the comb. The maximum electric field at the comb tip is 4.99 MV/cm whereas the middle of the comb metal line has a maximum electric field of 7.13 MV/cm. Thus, finger test structures experienced more severe electric field enhancement as compared to the comb-comb test structures. This may explain the non-correlation in area scaling between the extrapolated lifetimes of finger test structures and the comb breakdown lifetime.

Figure 2.16 (a) Planar TEM image and (b) FEM simulation of electric field distribution of 1 finger test structure, (c) Planar SEM image and (d) FEM simulation of electric field distribution of comb-comb test structure, (e) Planar SEM image and (f) FEM simulation of electric field distribution of comb-comb test structure's corner

Extrapolation Using Maximum Electric Field

To verify if electric field enhancement is the reason for premature dielectric breakdown of the finger test structures, Fig 2.14 was plotted once again. Instead of using nominal electric field, the maximum electric field was used for the extrapolation. The resulting curve is shown in Fig. 2.17.

As can be seen, an over-optimistic lifetime of the small area finger test structure was still obtained, although the over estimation has decreased from 5 orders of magnitude to around 2 orders. Electric field enhancement does explain some of the discrepancy, but clearly, there are other factors affecting the breakdown of the test structures.

Figure 2.17 Breakdown lifetime against area ratio plot for comb-comb and finger test structures using maximum electric field at 7.13 MV/cm and 100°C

2.3 Intermediate Test Structure

The finger test structures and comb-comb test structures used in this experiment were very distinct in terms of both area magnitude and shape, and hence other consideration such as different defect density may come into play.

Here, to fill in the gap between the small area finger test structures and large area comb-comb structure, intermediate test structures with area magnitude in between finger and comb-comb test structures were designed.

2.3.1 Experimental Details

Intermediate test structures are basically two parallel copper lines with the low-k dielectric sandwiched in between in a capacitor configuration. There are three intermediate structures, with varying copper line length ranging from 20 μm , 100 μm to 200 μm .

The dielectric spacing for all three structures is the same at 0.1 μm . A schematic diagram of the intermediate structure is illustrated in Fig. 2.18.

Figure 2.18 Schematic planar diagram of intermediate test structures

The test structure was fabricated using 40 nm technology. The metal line is copper, and the dielectric is SiOCH with a dielectric constant of 2.6. The barrier layer is Ta/TaN bilayer with a SiCN cap.

TDDb was conducted at electric fields of 2.75 MV/cm, 3.0 MV/cm and 3.5 MV/cm, at an elevated temperature of 125°C. 12 devices were tested for each condition. Failure time was taken when the leakage current increased abruptly by one order of magnitude.

2.3.2 Results and Discussion

A typical leakage current curve obtained from TDDb testing on the 20 μm, 100 μm and 200 μm intermediate test structures is shown in Fig. 2.19. They were stressed under an electric field of 3.5 MV/cm, at 125°C.

Figure 2.19 Leakage current against time plot for intermediate test structures at 3.5 MV/cm and 125°C

The leakage profile of the intermediate structures is similar to that of the finger and comb-comb test structures, where an initial dip in leakage current was seen, followed by a catastrophic failure evidenced by the abrupt increase of more than one order of magnitude. No soft breakdown was seen in these structures as well. The leakage current for the 200 μm test structure is the highest while the 20 μm test structure has the lowest leakage current, as expected due to the smaller test area of the 20 μm test structure. The shape factor β obtained from the intermediate structures ranges from 1.18 to 1.62. This is quite close to the β values for the finger and comb-comb test structures obtained previously.

The TDDB lifetime of the intermediate test structures was plotted against the area in Fig. 2.20. The intermediate test structures clearly do not adhere to the Poisson area scaling law. The characteristic breakdown lifetime for the 200 μm test structure is unexpectedly high.

Figure 2.20 Breakdown lifetime against area ratio plot for intermediate test structures

This non-Poisson behavior may be explained by the voltage drop along the metal line (Fig. 2.21(a)). Jeong [64] studied the effectiveness of the voltage along the comb-serpentine test structure. The voltage along the line is plotted along the length in Fig. 2.21 (a). Fig. 2.21 (c) illustrates the difference in the stressing conditions between Case 1 and Case 2. For experiments conducted for this study, stressing conditions are similar to Case 1.

Figure 2.21 (a) Plot showing the voltage along the serpentine metal line (b) Breakdown lifetime plotted against area of comb-comb and comb-serpentine test structure (c) Schematic diagram illustrating Case 1 and Case 2 [64]

There is a drop in the voltage along the metal line because of deviation from the ideal condition, where the copper metal is assumed to be a perfect conductor and the low-k is a perfect insulator. In reality, there is metal resistance in the copper line, and there will be leakage in the dielectric, albeit at a low level before dielectric breakdown occurs.

As a result, the electric field in the dielectric decreases as they move further from the voltage source. This greatly reduces the probability of failure occurring, as the length of line actually taking part in the TDDB is effectively reduced.

COMSOL Multiphysics software was used to simulate the voltage against length, and the result is plotted in Fig. 2.22 for lines of various lengths. It can be seen that for longer lines, the voltage actually drops faster than shorter lines.

Figure 2.22 Voltage against length for metal lines of different lengths

The T63.2 for all three fingers, intermediate and comb-comb structures were extrapolated to the same electric field, 3.02 MV/cm and temperature, 125°C. The temperature is scaled using the activation energy of 0.36 eV, which was obtained from the temperature split experiment. The result is plotted in Fig. 2.23. It exhibits the same trend as the lifetime results portrayed in Fig. 2.21 (b).

The lifetime initially decreases with an increase in area in a conventional manner, due to the larger area containing more defects and hence has a higher probability of failure.

After the area ratio exceeds around 5000, the lifetime actually increases with increasing area. This is where the voltage drop effect starts to play a part, and led to the increase in lifetime.

Figure 2.23 $\ln(T_{63.2})$ against $\ln(\text{Area Ratio})$ for fingers, intermediate and comb-comb test structure at 3.02 MV/cm, 125°C

The aim of the intermediate structure is to study additional factors leading to the longer than expected lifetime of comb structures. The finding from this study is that there is significant voltage drop along the long metal lines, leading to less effective field induced in the dielectric further from the voltage source. Voltage drop is not significant for short lines; hence electric field is relatively constant across the entire dielectric.

Another possible factor was suggested by Chen [94], which is the fatal-area ratio. Due to roughness of metal line edges from processing, the electric field is significantly higher at areas where the two electrodes are much closer. Hence the effective area being stressed is much reduced as compared to the design area, as shown in Fig. 2.24. Therefore the reduction in breakdown lifetime is not as much as expected based on calculation from design area.

Figure 2.24 Schematic demonstrating the effective area stressed by electric field

2.4 Summary

Lifetime scaling from small area test structure does not provide an accurate picture of the lifetime of comb-comb test structure through area scaling. Likewise, extrapolating lifetime using data from comb-comb test structure will also not yield a true lifetime of small area test structures. This is due to many variables between the two types of

structures. The discrepancy in the extrapolation result could be due to the difference in layout geometry, which will lead to different electric fields than designed. It can also be due to voltage drop along the line, causing the effectiveness of voltage to decrease as the metal line stretches further from the voltage source.

This is a precisely what is happening when conventional test structures; lifetimes are used to scale to real IC chips. Real IC chips contain total interconnect lengths that are much longer than the test structures used, and the geometry frequently found in real layout design is distinctly different from the long parallel lines of the conventional comb-comb and comb-serpentine test structures. It is therefore important to separate the different layout geometry into different populations for reliability study, in order to accurately identify the weakest layout geometry in the interconnect. The circuit lifetime extrapolation should be based on the lifetime of the weakest layout geometry. Because TDDB is based on the weakest link theory, the circuit lifetime will only be as long as the breakdown lifetime of the weakest layout geometry.

The conventional test structure has the advantage of being able to capture process defects related failures, and is therefore necessary during process and fabrication optimization. Even though the lifetime data from small area test structure is also not directly scalable to comb, small area test structure can serve its own purpose as well of estimating lifetimes of small area. It is a convenient and valid method to use this structure to study effects on TDDB, because the geometry is a true reflection of the geometry layout. Moreover, small area test structure is more suitable than conventional comb-comb structure for studying individual failure mechanism.

CHAPTER 3: FIELD INTERACTION

Interaction with the external environment is one of the extrinsic failure mechanisms for dielectric breakdown, which can cause premature failure to occur [9]. Although the external environment refers to the macro-surrounding in which the IC chip is operating in, such as high humidity or high temperature ambience, the micro-environment of the device-under-test should be taken into consideration as well. Unlike TDDDB test structures, metal lines and dielectrics in the real layout are seldom isolated. With the scaling of the technology, real estate on the IC chips are becoming denser, and this raises the likelihood that there will be other active lines nearby running simultaneously. Electric fields generated by different metal lines can overlap and interact, thus affecting the dielectric breakdown lifetime.

3.1 Electric field enhancement

Dielectric lifetimes are extremely sensitive to the electric field applied during TDDDB testing. Electric field enhancement has been attributed to be the cause of many deviations from conventional dielectric behaviour, such as lowering of the dielectric lifetime [95], and causing non-Poisson behaviour when doing area scaling. Electric field enhancements are frequently induced by the shape of the electrode geometry; in ultra-low-k dielectrics, the pores can cause field enhancement as well.

Electric field can be enhanced by curvature in the electrode [91]. This is often seen in the sharp corner of the metal tip at the end of the comb in a comb-comb test structure. The curvature is due to corner rounding during the lithography process, even though metal lines are drawn to be rectangular, the end product will not have sharp corners. In

neighbouring electrodes. This chapter focuses on understanding the effect of the non-uniform field caused by the field interaction between neighbouring metal lines on the dielectric breakdown lifetime.

3.2 Experimental Details

A schematic of the test structure is shown in Fig 3.1(a). The test structure consists of three pairs of electrodes. Each metal line will be termed as a finger structure. The dielectric spacing in between each pair of electrodes is approximately 100 nm. The distance in between the neighboring metal line varies from 0.1 μm , 0.2 μm , 0.4 μm to 3 μm . Fig 3.1(b) shows the planar TEM image of the 0.1 μm test structure. The copper metal line has Ta/TaN barrier layers and SiCN cap. The structures are fabricated using 40 nm technology.

Figure 3.1 (a) Schematic of planar view of test structure, (b) Planar TEM image of 0.1 μm structure

Fig 3.2 compares the shape of the metal line of the 0.1 μm and 3 μm structures. The shape of the metal line tip is important as the shape can severely affect the enhancement factor. The shape is found to be similar; hence any field enhancement

that occurs will be due to the proximity of the adjacent metal line, and not caused by the curvature of the cathodes and anodes.

Figure 3.2 (a) Single finger of 0.1 μm structure (b) Single finger of 3 μm structure

Physical failure for the backend dielectric frequently occurs at the top of the metal line, just under the capping layer [88]. The reason is attributed to the tapering of the metal wire. With the tapering, the top of the metal line has the shortest dielectric spacing and hence will experience the strongest electric field. Therefore, the failure will be most likely to occur in that region. To check if the metal line used in this experiment is tapered, a cross sectional cut was done and the SEM image is shown in Fig. 3.3(a). The metal line is indeed tapered, and illustrated in Fig. 3.3(b), the top of the metal line experiences the highest electric field. As such, it is very likely that failure will occur at the capping layer-metal line interface.

Figure 3.3 (a) SEM cross-sectional image of 0.1 μm structure (b) COMSOL electric field simulation of the cross-sectional image of 0.1 μm structure

Two types of electrical testing were carried out, the voltage ramp test and time dependent dielectric test. Voltage ramp test was carried out at a rate of 1 V/s, ranging from 0 V to 100 V. Temperature was held at 125°C.

Time dependent dielectric breakdown was conducted at 3.5 V/cm, 3.75 MV/cm and 4 MV/cm, at a temperature of 125°C. 15 devices were tested for each condition. Failure was taken to be the time or voltage when an abrupt jump of one order in the leakage current was observed.

3.3 Results and discussion

3.3.1 Voltage ramp results

Fig. 3.4 plots examples of the leakage current curve against voltage for the different test structures. The trend is similar for all the structures. From 0 V to 30 V, the leakage

current was lower than the resolution of the measurement system, only noises can be seen. From 30 V onwards, the leakage current increases almost linearly with the increase in voltage, until catastrophic failure occurs, which is indicated by an abrupt jump of one order or more in current magnitude. The leakage current trend is similar to all the structures.

Table 3.1 summarizes the results from the voltage ramp test. The breakdown voltage decreases as the adjacent metal lines get closer. This indicates that the proximity of the neighbouring metal line has an effect on the breakdown strength of the dielectric.

Figure 3.4 Plot of leakage current against voltage, at 125°C

Table 3.1 Summary of results from voltage ramp tests

Test Structures	Breakdown Voltage (V)
0.1 μm	48.6 ± 2.7
0.2 μm	53.1 ± 2.3
0.4 μm	54.0 ± 1.6
3 μm	56.7 ± 3.2

From the voltage ramp curve, the leakage mechanism can be deduced. Fig. 3.5 plots leakage current against square root of electric field, which fits to the Schottky Emission as the conduction mechanism. From the gradient of the linear portion of the curve, the dielectric constant fitted is 2.58; this is similar to the 2.7 of the dielectric used in this set of experiments. The conduction mechanism is the same for all the structures. The proximity of the neighbouring metal line does not affect the conduction mechanism, only the breakdown voltage.

Figure 3.5 Plot of leakage current against square root of electric field

3.3.2 TDDB Results

The time dependent dielectric breakdown curves are plotted in Fig. 3.6. The leakage current starts off in the order of 10^{-12} A, and then slowly decreases to 10^{-14} A. The decrease in leakage current is due to charge trapping. Failure is defined by an abrupt ten times increase in the leakage current. Failure is hard and catastrophic, no soft breakdown was seen to occur at all. The leakage current trend is similar for all structures.

Figure 3.6 Plot of leakage currents against time at 35V, 125°C

Fig. 3.7 is the Weibull probability plot for TDDB. The shape factor and the characteristic lifetime were extracted from this plot. The shape factor is similar for all structures. This further confirms that all the structures failed by the same mechanism, and is unaffected by the closeness of the adjacent metal line.

Figure 3.7 Weibull plot of TDDB lifetimes at 35V, 125°C

Fig. 3.8 shows the characteristic lifetime $T_{63.2}$ plotted against the distance between neighboring metal fingers. There is clearly a difference in the $T_{63.2}$ of the dielectric for the different structures, with the structure having the closest neighboring line the shortest lifetime. This shows that the field interaction between adjacent fingers does indeed have an effect on the lifetime of the dielectric.

Figure 3.8 Plot of $T_{63.2}$ against distance between neighbouring lines

Fig. 3.9 shows the relationship between the breakdown lifetime and the applied nominal electric field. The breakdown lifetime is assumed to scale according to the $\sqrt{E}$ model. The field acceleration parameter, γ , can be extracted from the slope of Fig. 3.9. Based on the best fit gradient from the four test structures, the γ extracted is $49 \text{ (cm/MV)}^{1/2}$.

Figure 3.9 Plot of breakdown lifetime against nominal electric field

Fig. 3.10(a) shows the leakage-time curve for a 0.2 μm test structure, and Fig. 3.10(b) shows the stressing parameters. The grounded fingers on the right are measured individually. The current from the 35 V fingers on the left is equivalent to the summation of the leakage current from Fingers 1, 2 and 3 on the right. For this particular test result, Finger 2 (red line) was the one that failed after 100 s. Even with the enhanced electric field, failure always occurs at only one finger. This is consistent with the TDDDB weakest link theory, where failure at one site will lead to failure of the whole system, even if the failure may not always occur at the site of highest electric field.

Figure 3.10 (a) Leakage-time curve of individual fingers on 0.2 μm test structure (b) Stressing parameters of individually grounded test structure

3.4 Relationship between E_{eff} and distance between fingers

COMSOL Multiphysics software was used to simulate the electric field distribution in the different test structures. From the cross section image of the metal line and dielectric (Fig. 3.3), it is likely that dielectric failure will occur at the top of the metal line; hence the following study on the electric field will focus only on the 2-D surface of the metal line.

The direction of the diagrams obtained from the FEM simulation will be defined as depicted in Fig. 3.11. The corresponding electric field simulation based on the diagrams will focus only on the x-component of the electric field.

Figure 3.11 Definition of the x- and y-directions used in FEM simulations

Fig 3.12 shows the horizontal cross-sectional electric field across the middle of a pair of electrode fingers for all four test structures. The electric field of all four test structure overlaps, with the maximum electric field of 4.59 MV/cm occurring at the tip of the metal line. The voltage applied was set at 35 V, and the dielectric spacing is 100 nm, the nominal electric field calculated from these two parameters is supposed to be 3.5 MV/cm. The maximum field is higher than nominal electric field because the tip of the metal line is curved, giving rise to field enhancement. As established earlier, the shape of the individual metal tip is similar for all four structures; hence the field enhanced maximum field should be comparable as well.

Fig 3.13 portrays the vertical cross-sectional electric field cutting across the tip of one metal line to the tip of the adjacent metal line. As can be seen, the electric field in between adjacent metal fingers is much higher for the closer fingers. This field interaction decreases with increasing distance apart. For the 3 μm structure, the field interaction between adjacent fingers reaches zero, which means that the electric field of each electrode pairs does not overlap.

Figure 3.12 Horizontal cross-sectional electric field across the middle of a pair of electrode fingers

Figure 3.13 Vertical cross-sectional electric field cutting across the tip of one metal line to the tip of the adjacent metal line (a) Electric field distribution of 3 μm and (b) 0.4 μm structures

As can be seen from the TDDB results, neither the nominal electric field nor the maximum electric field is sufficient to describe the difference in dielectric breakdown lifetime for the test structures. For all four test structures, both the nominal electric field and the maximum electric field are similar, at 3.02 MV/cm and 4.59 MV/cm, respectively. However, a difference in the TDDB lifetime was clearly observed. This difference can only be attributed to the field interaction between the adjacent metal lines. Hence, an approach was proposed to calculate the effective electric field affecting the dielectric lifetime based on the electric field interaction.

Before deriving the effective electric field, it will be convenient to define the terminologies used. The terms are summarized in Table 3.2. Illustrated in Fig. 3.14 is the distance apart, d and dielectric spacing, s .

Table 3.2 Summary of the symbols used in the derivation and their description

Symbol	Term	Description
d	Distance apart	Distance between adjacent metal fingers of the same potential
s	Dielectric spacing	Width of the dielectric between a pair of electrodes
E_{nom}	Nominal electric field	Electric field calculated from the uniform electric field equation, $E_{nom} = Voltage/s$
E_{int}	Interaction electric field	Electric field due to the overlapping electric fields between adjacent pair of electrodes
E_{eff}	Effective electric field	Electric field due to combination of effect from nominal and interaction electric field
$T_{63.2}$	Time to failure	Characteristic lifetime when 63.2% of the population fails
V	Voltage	Potential applied to the electrode

Figure 3.14 Schematic diagram showing distance apart, d and dielectric spacing, s

Let the effective electric field, E_{eff} be the sum of the nominal electric and electric field caused by interaction between neighbouring fingers, where $E_{nom} = V/s$, V is the voltage and s is the dielectric spacing.

$$E_{eff} = E_{nom} + E_{int} \text{ --- --- --- --- --- (3.2)}$$

Assuming the breakdown of the dielectric follows the Root E model, the lifetime of the dielectric is related to the effective electric field by the equation

$$\ln(T_{63.2}) \propto -\gamma\sqrt{E_{eff}} \text{ --- --- --- --- --- (3.3)}$$

Substituting equation (3.2) into equation (3.3),

$$[\ln(T_{63.2})]^2 = \gamma^2 E_{nom} + \gamma^2 E_{int} + A \text{ --- --- --- --- --- (3.4)}$$

Equation (3.4) will be used for the 0.1 μm , 0.2 μm and 0.4 μm structures. For the 3 μm structure, the field interaction between adjacent test structures falls to zero, hence $E_{int,3\mu\text{m}} = 0$. Equation (3.4) will be reduced to

$$[\ln(T_{63.2_{3\mu\text{m}}})]^2 = \gamma^2 E_{nom} + A \text{ --- --- --- --- --- (3.5)}$$

E_{nom} is obviously the same for all structures, as this is the uniform electric field. By taking the difference between Equation (3.4) and (3.5), for the 0.1 μm structure

$$\gamma^2 E_{int,0.1\mu\text{m}} = \left| [\ln(T_{63.2_{3\mu\text{m}}})]^2 - [\ln(T_{63.2_{0.1\mu\text{m}}})]^2 \right| \text{ --- --- --- --- (3.6)}$$

This equation implies that any difference in the lifetime between the 3 μm and 0.1 μm structures is due solely to the electric field interaction. E_{int} can be empirically fitted with a curve to correlate the effective electric field to the distance apart.

Fig. 3.15 shows the plot of E_{int}/V against distance apart, and the fitting curve obtained from all the experimental results. The equation fitted is shown in equation (3.7).

$$\frac{E_{int}}{V} = 0.39 \cdot \exp^{-\frac{d}{0.35}} \text{---(3.7)}$$

From the E_{int} equation, the E_{eff} equation can be written as

$$E_{eff} = 0.39V \cdot \exp^{-\frac{d}{0.35}} + \frac{V}{s} \text{---(3.8)}$$

Figure 3.15 Plot of interaction electric field normalized to applied against distance apart

The equation implies that the effective electric field decays with distance apart by an exponential equation. At a very large distance apart, the first part of the equation becomes zero, and the effective field is equivalent to the nominal electric field.

3.5 Implications of the Model

The model can be used to predict the effective electric field and subsequently the time to breakdown when the test conditions are changed, or when the test structure itself is changed. This is useful for understanding the impact of the neighbouring metal lines as the technology scales smaller, and for extrapolation of test data to use conditions.

3.5.1 Change in distance d

With a change in the distance apart, the E_{eff} and the lifetime can be predicted by the model directly, as shown in Fig. 3.16.

As the distance between neighbouring metal lines increases, the electric field due to adjacent line's interaction decreases exponentially, and hence effective electric field decreases exponentially as well. At very far distance apart, the E_{eff} becomes the same as E_{nom} as the interaction between adjacent metal lines tapers off. The dielectric lifetime decreases exponentially at the same time, illustrated in Fig. 3.16(b).

Figure 3.16 (a) Plot of E_{eff} against distance apart at different d (b) $\ln(T63.2)$ against distance apart at different d at 35V

3.5.2 Change in stress voltage

The model can be used to predict the breakdown lifetime when the same test structures are stressed at different voltages. This is necessary for extrapolation of accelerated testing at high voltage to lower voltage at use condition.

Fig. 3.17(a) shows the electric field distribution across the anode and cathode. The maximum electric field increases as the applied voltage increases. Fig. 3.17(b) shows the electric field distribution across the tip of the metal line of adjacent metal lines for the 0.1 μm structure, stressed at three different voltages of 35 V, 37.5 V and 40 V. The electric field shows a direct increase in the magnitude, with no change in the pattern.

Figure 3.17 Plots of electric field distribution across (a) cathode and anode, (b) neighbouring metal line tip, at different stress voltages

The increase in voltage causes both the E_{nom} and E_{int} to increase. The effective electric field is thus a direct translation upwards at higher voltages. Fig. 3.18(a) shows the prediction of the effective electric field using the model and also the effective electric field extracted from experimental data at different electric field.

From the effective electric field, the time to breakdown for dielectric can also be calculated, as shown in Fig. 3.18(b). The lines represent the lifetime as predicted by the model, and the points are the experimental data. The experimental data and the prediction show a good fit. As the applied voltage decreases, the effect of the distance apart on the dielectric breakdown becomes less and less apparent. This means that at use conditions, the impact of having neighbouring metal wires close by will be

diminished. At higher voltage, there will be more field interaction between adjacent fingers, hence when the distance apart decreases, the fall in T63.2 will be more drastic as observed in Fig. 3.18(b).

Figure 3.18 (a) Plot of E_{eff} against distance apart at different voltages (b) $\ln(T63.2)$ against distance apart at different voltages

3.5.3 Change in dielectric spacing, constant voltage

As technology scales down, the dielectric spacing between cathode and anode will inevitably become smaller. It is important to understand the effects of decreasing dielectric spacing on the lifetime of structures with different distances apart. This section focuses on changes in the dielectric spacing, while keeping the voltage constant.

Fig. 3.19(a) shows the cross-sectional electric field distribution across the dielectric spacing as the dielectric spacing changes. It can be seen that the maximum electric field changes drastically as expected. At the same time, from Fig. 3.19(b), even though the maximum electric field increases significantly as dielectric spacing decreases, the field interaction at the centre in between the two metal lines does not differ by much.

Figure 3.19 Plots of cross-section electric field distribution across (a) cathode and anode, and (b) neighbouring metal line tip as the dielectric spacing changes, with constant applied voltage for $d = 0.1 \mu\text{m}$

From Fig. 3.20(a), it can be observed that the increase in E_{eff} due to decrease in dielectric spacing is the same, regardless of the distance apart. When the applied voltage is kept constant, the E_{nom} will increase. E_{int} remains unaffected since V is unchanged. Thus, E_{eff} increases in direct proportion to the inverse of spacing, as illustrated in Fig. 3.20(c).

$$E_{eff} \propto \frac{1}{s} \text{-----} (3.9)$$

Since E_{eff} increases as spacing decreases, dielectric lifetime will also decrease. As can be seen from Fig. 3.20(b), at large distance apart, the decrease in dielectric spacing has

no effect on the dielectric breakdown lifetime. However, the effect of the distance apart on the dielectric breakdown becomes more significant as the dielectric spacing decreases, as clearly seen in Fig. 3.20(d).

Figure 3.20 (a) Plot of E_{eff} against distance apart and (b) $T63.2$ against distance apart for different dielectric spacing (c) Plot of E_{eff} against dielectric spacing and (d) $T63.2$ against dielectric spacing for different distance apart at the same voltage

3.5.4 Change in dielectric spacing, constant E_{nom}

This section focuses on the effect of changing dielectric spacing, while keeping the E_{nom} constant, i.e. scaling the voltage proportionally with the dielectric spacing.

Fig. 3.21(a) shows the cross-sectional electric field distribution across the dielectric spacing as the dielectric spacing decreases with a constant nominal electric field. It can be seen that the maximum electric field decreases as the dielectric spacing decreases. It can be seen from Fig. 3.21(b) that the interacting electric field between neighbouring metal lines decreases with the decrease in dielectric spacing as well.

Figure 3.21 Plots of electric field distribution across (a) cathode and anode, and (b) neighbouring metal line tip as the dielectric spacing changes, with constant applied nominal electric field at $d = 0.1 \mu\text{m}$

When the dielectric spacing decreases, while keeping the E_{nom} constant, the voltage applied will decrease. With the decrease in applied voltage, E_{int} decreases. This leads to the decrease in E_{eff} as the dielectric spacing decreases, as shown in Fig. 3.22(a). This may seem counter intuitive to the more obvious conclusion of electric field increasing

as dielectric decreases. However, it has to be kept in mind that the potential applied has to decrease to keep the E_{nom} constant (Fig. 3.22(b)). This drop in applied voltage causes the E_{int} between adjacent metal fingers to drop. Hence with the E_{nom} constant and E_{int} decreasing with dielectric spacing, E_{eff} will decrease as well. The decrease in E_{eff} will cause the dielectric lifetime to increase as dielectric spacing decreases. Contrary to the conclusion drawn in Section 3.5.3, the effect of the distance apart on the both the effective electric field and dielectric breakdown becomes less obvious as dielectric spacing becomes smaller, as seen in Fig. 3.22(c) and (d), respectively.

Figure 3.22 (a) Plot of E_{eff} against distance apart and (b) T63.2 against distance apart at different dielectric spacing (c) Plot of E_{eff} against 1/spacing and (d) Normalized T63.2 against 1/spacing at different distance apart at constant nominal electric field

3.6 Limitations of the Model

Although the proposed model is able to predict the TDDB lifetime from the effective electric field from the changes in applied voltage on geometric spacing, it has some limitations. The model makes the assumption that there is no change in the curvature of the metal line tip in the different layout. If by changing the distance apart d , or spacing s , or the line/space pitch alters the shape of the metal tip, the effective field will change and the model may not apply directly. Temperature effect is not studied in this experiment as well.

Fig. 3.23 shows the electric field distribution of possible metal tip geometries when the metal line width and dielectric spacing changes. The differences in the geometry could be caused by lithography process.

Figure 3.23 Electric field distribution of test structures with different line width at (a) 0.05 μm (b) 0.1 μm and (c) 0.2 μm

Fig. 3.24 compares the cross-sectional electric field across the dielectric spacing when the metal tip geometry is different. For easy comparison, the applied voltage, line width, dielectric constant is held constant. It can be seen that the maximum electric field of the two metal lines are not at the same location, although the magnitude of the maximum electric field is similar. While the maximum electric field of the rounded tip is at the curved tip, the square metal tip line has a maximum electric field at the corner of the metal line.

Figure 3.24 Electric field distribution across centre of finger for test structures with different line shape at the metal tip

Fig. 3.25 shows the cross-sectional electric field across the metal tip. The interaction electric field between the neighbouring metal lines has a different profile for the two

metal tip geometries. The electric field becomes difficult to compare and therefore hard to extrapolate the lifetime from one shape to another.

Figure 3.25 Electric field distribution across tip of finger for test structures with different line shape at the metal tip

3.7 Summary

To study the effect of field interaction on the dielectric lifetime, four small area test structures with varying distance between neighbouring metal lines were designed. The maximum electric field for all four structures is the same at 4.59 MV/cm, yet there is a difference in the dielectric breakdown lifetime.

The difference in the lifetime can be attributed to the field interaction between the neighbouring metal lines; hence there is a need to find the effective electric field rather than using the maximum or nominal electric field. Empirical fitting was done to find the relationship between the effective electric field and the distance apart from

experimental TDDB data. The effective electric field decreases with increasing distance between adjacent lines. From the model, the interaction electric field can be extracted.

The model can be used to predict the effect of neighbouring metal lines on time to dielectric breakdown when test or use condition changes. In particular, the effect when extrapolating lifetime from accelerated testing conditions to use conditions, and also the effect when technology scales smaller.

First, when extrapolating lifetime from test to use conditions, the effect of the neighbouring electrode tends to diminish. This is due to interaction field decreasing at lower voltages. Second is the prediction when technology scales smaller. From the FEM simulations, it can be seen that the effect of neighbouring metal lines can be reduced if the applied voltage can be scaled proportionally with the dielectric spacing. However, from the ITRS roadmap, it is known that the voltage will not be able to scale as fast as the dielectric spacing, thereby causing the nominal electric field to increase. Hence for future technology, the effect of adjacent metal lines will become more pronounced, and hence should be taken into account when performing TDDB lifetime predictions.

CHAPTER 4: EM/TDDDB INTERACTION

During normal TDDDB testing, a voltage is applied to a metal electrode, resulting in the entire electrode being at the same potential. However in real circuits, current will be running in the metal lines. Having current in the metal line will bring about a common reliability problem in the backend interconnect, which is electromigration (EM) in the metal lines [87]. TDDDB was described in detail in Chapter 1; EM will be introduced in the following section.

4.1 Electromigration

Electromigration is the movement of the metal atoms as a result of momentum transfer from electrons moving in the applied electric field [99, 100]. A schematic diagram is shown in Fig. 4.1. From the movement of the metal atoms a tensile stress will develop which will lead to formation of void at the cathode. At the same time, compressive stress will result at the anode end of the metal line which will lead to metal extrusion.

Figure 4.1 Schematic diagram showing EM in metal line

The current-induced atomic flux in the metal line is given by equation (4.1) [101]

$$J = -\frac{DC}{kT} \left(\rho j Z^* q - \Omega \frac{\partial \sigma}{\partial x} \right) \text{-----} (4.1)$$

where D is the diffusivity, C is the atomic concentration, k is the Boltzmann's constant, T is the temperature, ρ is the resistivity, j is the current density, Z^* is the effective charge number, q is the fundamental charge, Ω is the atomic volume, and σ is the back stress.

The mechanical stresses in the metal line can be evaluated by a physical model was developed by Korhonen [102]. The model describes the stress evolution along the metal line, and is given by the equation

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[\frac{DB}{kT} \left(\Omega \frac{\partial \sigma}{\partial x} + Z^* q \rho j \right) \right] \text{-----} (4.2)$$

where B is the effective modulus.

For EM reliability study, EM lifetime is traditionally extrapolated using the Black's equation [87, 103, 104], expressed as

$$t_{50} = A j^{-n} \exp \left(\frac{\Delta H}{kT} \right) \text{-----} (4.3)$$

where t_{50} is the median time to failure, A is a constant, j is the current density, n is the current exponent and is either 1 or 2 depending on whether the failure is void growth or nucleation growth dominated [105], and ΔH is the activation energy.

4.2 Interaction between TDDB and EM

Fig. 4.2 shows how EM and TDDB can possibly interact. TDDB occurs in the intra-metal dielectric, whereas EM occurs in the metal line. The two reliability issues are usually tested and discussed separately, seldom are the interaction of the two phenomena discussed. An exception is the paper from Li [106]. The paper attempts to perform EM in the metal line followed by TDDB in the dielectric to study the effect of the EM on TDDB lifetime. However, they were unable to separate the EM and TDDB due to the design of their structure. This is because test structures used for the experiments consist of assisting metal lines surrounding the EM metal line. A schematic diagram of the test structure is shown in Fig. 4.3. During EM stressing, there will be electric field induced in the dielectric due to the potential difference between the EM line and the assist line. This resulted in uncertainty in the TDDB data gathered.

Figure 4.2 Schematic diagram of EM and TDDB interaction

Figure 4.3 Schematic diagram of test structure used by Li [106]

In this study, the two reliability issues are separately induced in a single test structure. The tests were conducted on a newly designed test structure. It allows TDDB to be completely absent during EM stressing so that the dielectric will not degrade during EM stressing. The effect of EM on TDDB lifetime can then be qualitatively studied. Possible ways that TDDB and EM will interact are:

1. Compressive stress in the anode due to EM could have affected the adhesion between the capping layer and the low-k dielectric, leading to faster delamination of the capping layer [88], causing TDDB to occur earlier.
2. Compressive stress in the anode may lead to stress-induced diffusion [107] coupling with Cu diffusion already present in the dielectric during TDDB testing. This will cause Cu to out diffuse more easily, hence shortening dielectric lifetime.
3. The tip of the metal line could have deformed physically due to the compressive stress, thereby reducing the dielectric spacing, leading to decreased lifetime [108].

4.3 Experimental Details

A test structure was designed as shown in Fig. 4.4. Small area finger test structure was discussed in the previous section, and is the basis of the test structure for TDDB testing. The test structure comprises a long metal line of 200 μm in length, with via-below-line symmetrical structure, designed for performing EM testing. The via-below line structure was used as it has longer lifetime and will be less likely to fail abruptly as compared to via-above-line test structures [109]. Another metal line is placed tip-to-tip with the long metal line, where the dielectric in between will be used for TDDB testing.

The copper metal line has Ta/TaN barrier layers and SiCN as the capping layer. The dielectric is SiOCH, with a dielectric constant of 2.7. The structures were fabricated using 40 nm technology.

Electromigration was first performed at 350°C, with a constant applied voltage of 342 mV at the anode and grounded at the cathode. The current density generated in the copper metal line is around 3 MA/cm². The cathode was biased at 0 V, while the anode at 342 mV. The opposing metal line was biased at 342 mV, so that no electric field exists in the dielectric during EM stressing. The stressing condition of the structures during EM is shown in Fig. 4.5(a).

EM was carried out using constant voltage stressing instead of constant current stressing, which is the common practice for EM testing [87, 99, 103]. This is done so as to have a better control over the electric field in the dielectric. Eight structures were stressed for each time duration of 0, 1, 2, 3, 4 and 5 hours.

After EM stressing, all the structures underwent TDDB testing, where they were stressed at a voltage of 35 V, with a temperature of 125°C until breakdown. During TDDB testing, both ends of the metal line were stressed at the same potential of 35 V, so that there will be no current flowing. The other metal line was grounded to induce an electric field in the dielectric, as shown in Fig. 4.5(b). TDDB breakdown is defined as when there is one order increase in the magnitude of the leakage current observed.

Figure 4.4 Cross-sectional schematic image of test structure

(a) Stressing EM only

(b) Stressing TDDB only

Figure 4.5 Schematic of biasing conditions of test structures during (a) EM and (b) TDDB stressing

Physical failure analysis after the electrical testing was performed using scanning electron microscope (SEM) or transmission electron microscope (TEM). Sample preparation for TEM was done using focus ion beam (FIB).

4.4 Results and Discussion

4.4.1 EM stressing

Preliminary EM testing was performed. Fig. 4.6 shows the percentage increase in resistance-time curve during EM stressing. The aim was to stop the stressing before any catastrophic failure occurs and the time to failure time obtained was around 6 hours. For the experiment, the maximum EM stressing time was set at 5 hours, so that EM failure would not occur. Although there were some test structures that suffered early failures, only the unfailed test structures were subsequently used for TDDB testing.

Figure 4.6 Percentage increase in resistance of copper metal line against time under EM stressing

4.4.2 Voltage ramp test

The k value extracted from the $\ln(\text{Current})$ against $\text{Root } E$ plot (in Fig. 4.7) is 2.82, which is close to 2.7 of the dielectric constant use in the test structures. The conduction mechanism was concluded to be Schottky emission. The conduction mechanism is similar to that found in the test structures used in Chapters 2 and 3.

Figure 4.7 $\ln(\text{Current})$ against $\text{Root } E$ plot for Schottky emission

4.4.3 TDDB Results

Depicted in Fig. 4.8 is the Weibull plot for all the TDDB testing. The characteristic lifetime $T_{63.2}$ and the shape factor values were extracted from this plot. The shape factor values are summarized in Table 4.1. The shape factor extracted is similar for the different EM test conditions; there is no systematic change in the shape factor as EM time duration increases. Since the shape factor provides information on the TDDB failure mechanism, it can be concluded that all the test structures failed by the same

failure mechanism, i.e. the EM pre-stress has no effect on the subsequent TDDB failure mechanism.

Figure 4.8 Weibull plot for TDDB results

Table 4.1 Summary of beta values obtained from all test conditions

EM duration (hours)	Weibull slope, β
0	1.22
1	1.78
2	1.06
3	1.75
4	1.18
5	1.15

Fig. 4.9 shows the $T_{63.2}$ plotted against the EM duration. It clearly shows that EM in the metal line has an adverse effect on the dielectric breakdown. The lifetime of the dielectric decreases significantly with the increase in the EM time duration.

Figure 4.9 Plot of TDDB lifetimes against the duration of EM stressing.

From the leakage current curves during the TDDB testing in Fig. 4.10, it can be seen that the current profile is not affected by the EM. The current first decreased, indicating charge trapping, followed by an abrupt increase in the leakage current signifying the breakdown of the dielectric. This profile is the same for all structures, with or without first performing EM stressing.

There is, however, a difference in the magnitude of the leakage current. The initial leakage current of the structures with 3 hours and above of EM stressing is significantly higher than the structure with no EM stressing (Fig. 4.10(a)). This implies that there is already a degradation of the dielectric prior to the TDDB testing, caused by the EM stressing. This degradation in the dielectric would lead to a decrease in the TDDB lifetime, as well as a higher leakage current.

Figure 4.10 Plot of leakage current during TDDB testing for EM duration of (a) 3 hours to 5 hours (b) 0 hour to 2 hours, at the applied voltage of 35 V

For the structures with 1 and 2 hours of EM stressing, seen in Fig. 4.10(b), the initial current leakages of these structures are similar to that of the structure with no EM. This indicates that there is little or no significant damage to the dielectric after the EM stressing. However, even though no damage to the dielectric can be deduced from its leakage current profile during EM stressing, there is considerable reduction in the lifetime of the 1 and 2 hours structures. This is significant because EM in the metal could be adversely affecting the lifetime of the TDDB, but it may not be detected as there is no indication that can be observed from the leakage current profile.

4.4.4 XSIM

A software program, XSIM, was used to calculate the stress in the metal line at different conditions of EM. It is a 1D electromigration simulator that solves the Korhonen-Clement model numerically in a Matlab environment, written by Choi [108, 110]. It simulates the electromigration-induced hydrostatic stress across the metal line. Fig. 4.11 shows the stress evolution across the metal line at different times. At time

zero, it is assumed that the entire metal line is stress free. As time increases, materials are being transported from the cathode to anode; tensile stress builds up at the cathode, compressive stress at the anode. When a void forms at the cathode, it relaxes the stress, while compressive stress continues to increase at the anode.

Figure 4.11 Stress evolution with time across the metal line as simulated from XSIM

Fig. 4.12 summarizes the compressive stress at the anode after the various EM duration. Compressive stress increases as time increases, with a trend that is similar to the dielectric breakdown lifetime. This strongly implies that the reduction in the TDDDB lifetime may be due to the compressive stress induced in the metal line during EM.

Figure 4.12 Plot of compressive stress in the anode against the EM duration

EM stressing always ended before there is any significant increase in the resistance of the metal line, meaning that the metal line has not failed by EM. Although the metal line has not failed, voids have already started forming in the metal line. Aside from the stress in the metal line, XSIM can also calculate the void size due to the EM flux. Summarized in Table 4.2 is the void size obtained from the simulation, while Fig. 4.13 is the SEM images of the voids found in the metal line after EM stressing. Voids are not observed in the samples after 1 and 2 hours of stressing. Only after 3 hours of EM are voids observable in the SEM images. The values from the simulation are comparable with the actual voids found in the experiments. This implies that the stress simulated from this software should be close to the actual values as well.

Table 4.2 Summary of void sizes simulated from XSIM

EM Duration (hours)	Void size (nm) from XSIM	Void size (nm) from experiment
1	22	N.A.
2	50	N.A.
3	78	64
4	105	136
5	133	165

Figure 4.13 SEM images of voids at the cathode end of the line after EM stressing

4.5 FAILURE MODEL

As mentioned in the introduction, compressive stress in the metal due to EM may affect TDDDB by causing easier delamination of the capping layer, easier Cu out-diffusion or bulging of the metal line or a combination of the factors.

Delamination of the capping layer, and also migration of Cu into the dielectric are common failure mechanisms for Cu/low-k interconnect systems, such as seen by Tan [54]. To verify the possible failure mechanism, a detailed failure analysis of the

structures was carried out after TDDB stressing. Shown in Fig. 4.14(a) is the cross-sectional TEM image of the metal line and dielectric after 1 hour of EM, followed by TDDB testing. Instead of delamination of the capping layer, delamination at the bottom of the metal line was observed. The cathode end was seen to be misaligned relative to the anode side, and appears to have been raised upwards. Delamination in small area finger structures, if seen, always occurs at the capping layer. It is believed that this bottom delamination is not because of the compressive stress in the anode. Instead, it is due to the presence of a via at the anode side of the metal line. Fig 4.15 plots the electric field induced in the dielectric of such a structure. It can be observed that the electric field at the corner of the via is enhanced, causing the bottom of the cathode to have a higher electric field than the top of the cathode line. This could have led to the bottom delamination. This is confirmed by Fig. 4.14(b), where a similar bottom delamination was seen in the dielectric failure with no EM stressing. Hence, the compressive stress in the anode is not the cause of the delamination failure mechanism of TDDB.

Figure 4.14 (a) Cross-sectional TEM image of dielectric failure after 1 hour of EM stressing followed by TDDB testing (b) Cross-sectional SEM image of dielectric failure after TDDB breakdown, with no EM stressing

Figure 4.15 Electric field distribution for EM/TDDDB test structure

Fig. 4.16 shows the physical failure analysis of another test structure after 1 hour of EM followed by TDDDB stressing at 35 V. A similar bottom delamination as observed in Fig. 4.14 was seen here as well. In addition to the bottom delamination, a crack at the top of the cathode line was detected. This crack is most likely caused by the upward movement of the metal line as it delaminated at the bottom. It can also be clearly seen that the Ta barrier has out-diffused, especially near to the top of the metal line. Fig 4.16(c) shows the results of the EDX line scan from the red line in Fig. 4.16(b). It shows slight amount of Ta and Cu in the middle of the dielectric, indicating Cu as well as Ta out-diffusion.

Figure 4.16 (a) TEM image of test structure after 1 hour EM followed by TDDB, (b) Higher magnification of TEM image of failure site, (c) EDX line scan of red line in (b)

Compressive stress in the anode will not affect the electron injection into the dielectric as electron injection occurs from the cathode. The generation and mass transfer of Cu ions occur at the anode. The generation of Cu ions can be by traps [111], ionization by electrons [75], from copper oxide residues due to chemical-mechanical polishing (CMP) [89, 112] or Schottky emission [113]. The Cu ions are then assumed to migrate across the low-k dielectric by Poole-Frenkel emission [111], through diffusion and drift [75, 114, 115]. Having a compressive stress in the metal line could have affected

some of the mechanisms; enhanced/retarded Cu diffusion due to stress-driven diffusion [116], or increased Poole-Frenkel conduction mechanism due to stress-induced trap generation [117]. These could have led to the increase in Cu ion migration, and thus reduced TDDB lifetime. However, looking at the TEM image (Fig 4.17) of the metal line after 5 hours of EM, the most dominant cause should be the increase in drift of the Cu ions that caused the shortened lifetime [108]. From Fig. 4.17, we can see that there is significant bulging of the line from the compressive stress induced by EM. It is believed that this deformation of the metal line, would lead to the reduction in the dielectric spacing and thus increasing the electric field. The increased electric field would have led to an increase in the bond breaking mechanism, as well as increasing the drift of Cu ions, thus affecting the TDDB lifetime.

Figure 4.17 Planar TEM image of metal line after 5 hours of EM stressing, prior to TDDB testing

With these experimental results, a methodology has been developed to study the effect of EM on TDDB lifetime. The flowchart in Fig. 4.18 summarizes the process flow.

Figure 4.18 Flowchart showing process flow of investigation of EM effect on TDDB lifetime

The process begins by setting the stress voltage, temperature and EM stress duration into the XSIM program. The program will compute the compressive stress induced in the anode end of the metal line. From here, the relationship of how compressive stress evolves with time can be deduced. By inputting this relationship into the FEM simulation, the displacement of the metal tip caused by the compressive stress can be estimated. Subsequently, the electric field can then be determined, and hence the TDDB breakdown lifetime can be evaluated using the TDDB breakdown model.

To begin, the effect of the compressive stress induced by EM stressing on the metal tip was considered. The magnitude of metal line tip displacement is the magnitude of encroachment into the dielectric spacing. Hence, to model the effect of reduction in dielectric spacing s on the TDDB lifetime, let nominal electric field E be

$$E = \frac{V}{s_0 - \Delta s} \text{-----} (4.4)$$

where s_0 is the original dielectric spacing, and Δs is the reduction in dielectric spacing. Assuming the interconnect systems follows the $\sqrt{E}$ model, the time to failure can be modelled as

$$TF \propto \exp\left(-\gamma \sqrt{\frac{V}{s_0 - \Delta s}}\right) \text{-----} (4.5)$$

The deformation of the metal line over time can be modelled using COMSOL Multiphysics, as illustrated in Fig. 4.19. Fig. 4.19 shows the tip of the metal line after deformation from 5 hours of EM stressing.

Figure 4.19 FEM simulation of anode metal tip after 5 hours of EM stressing

The relationship of Δs with time can be obtained from the fitting shown in Fig. 4.20(a).

It was determined from the plot that Δs and EM duration time, t is related by the equation

$$\Delta s = 1.22t^{0.54} \text{ --- (4.6)}$$

Substituting equation (4.6) into the $\sqrt{E}$ model in equation (4.5), equation (4.7) is obtained

$$\ln(T63.2) = \left(-\gamma \sqrt{\frac{V}{s_0 - [1.22t^{0.54}]}} \right) + A \text{ --- (4.7)}$$

Fig 4.20(b) is the graphical representation of equation (4.7).

Figure 4.20 (a) Relationship of Δs against time at 350°C (b) Lifetime T63.2 against $\sqrt{E}$, at 35V, 125°C

4.6 Implications of the model

As technology scales, the voltage applied and dielectric spacing will scale as well. In this section, the effect of EM on TDDB lifetime is studied as the voltage and dielectric spacing scales, and when EM and TDDB stressing is occurring at the same time.

The proposed model in Fig. 4.18 was used to evaluate the breakdown lifetime at 125°C. The simulation for the compressive stress using XSIM assumes that the failure mechanism, and therefore the activation energy, for EM is the same at 350°C and 125°C. The EM effect on compressive stress leading to changes in dielectric spacing Δs , was simulated from XSIM and COMSOL, respectively, at 125°C. The current density in the metal line during EM and TDDB stressing is constant at 3MA/cm², which is the same as the value used in the experiments.

Numerical method was used to calculate the T63.2 using equation (4.7). Starting from EM stress time $t = 0$ s, the TDDB breakdown lifetime T63.2 can be calculated. If $T63.2 < t$, the device has not failed, and EM time t can continue to $(t+1)$ second. At $(t+1)$ second, the metal tip would have deformed more and dielectric spacing reduced further. Thus T63.2 will keep decreasing as EM continues. The calculation will carry on until $T63.2 = t$.

4.6.1 Change in applied voltage, V

As evidenced by Fig. 4.21, as the voltage applied decreases, both the TDDB lifetime with and without EM stressing will increase with decreasing voltage. Also observed from Fig. 4.21, the effect of EM on TDDB lifetime will increase with the decrease in voltage.

Figure 4.21 T63.2 against voltage with and without EM, at 125°C

As voltage applied decreases, the electric field applied in the dielectric decreases, leading to an increase in the dielectric breakdown lifetime. This implies that at lower voltages, the EM stressing time will be longer as well, with the same flux in the metal line. Higher compressive stress will build up at the anode with longer EM stressing time, causing more deformation of the metal tip. Therefore this increase in the EM duration will cause the EM effect on the TDDB lifetime to become more pronounced at lower voltages. As a result, the difference in the breakdown lifetime with and without EM will become larger as the biasing voltage decreases.

This is significant because voltage extrapolation is used to predict the lifetime at use condition. Extrapolating the lifetime from high voltage during stress condition to lifetime at low voltage in use condition without factoring in the effect of EM gives an over-optimistic lifetime.

4.6.2 Change in dielectric spacing, s with constant V

As the dielectric spacing decreases, with the applied voltage kept constant, the applied electric field will increase, causing the TDDB lifetime of both test structures with and without EM stressing to decrease. This is shown in Fig. 4.22. The effect of EM stressing on TDDB lifetime is also seen to weaken with the decrease in dielectric spacing scales smaller.

The dielectric lifetime with and without EM in the metal line gets closer as the dielectric spacing decreases. This is because the TDDB lifetime is dominated by the intrinsic TDDB behavior effect rather than the EM effect at smaller dielectric spacing.

$$E_{short} = \frac{V}{s_{short} - \Delta s} > \frac{V}{s_{long} - \Delta s} = E_{long} \text{ --- (4.8)}$$

where s_{short} is shorter dielectric spacing, and s_{long} is longer dielectric spacing, E_{short} is the electric field present in test structures with shorter dielectric spacing, and E_{long} likewise for longer dielectric spacing.

At larger dielectric spacing, the biasing electric field is lowered, as shown in equation (4.8). Hence, the TDDB lifetime will be longer. With the longer stressing time, the EM duration increases as well, causing more compressive stress to build up at the anode, leading to more deformation of the metal tip. Hence the EM stressing effect becomes more pronounced, and the difference between the breakdown lifetime of test structures with and without EM stressing will becomes larger with increasing dielectric spacing.

Figure 4.22 T63.2 against dielectric spacing with and without EM, at 125°C

4.6.3 Change in dielectric spacing, s with constant E

If both the voltage applied and the dielectric spacing was to scale at the same rate, the applied electric field on the dielectric will remain constant. As the dielectric spacing scales in this case, the effect of EM on the TDDB lifetime will increase marginally, as illustrated by Fig. 4.23. When no EM is present in the metal line, the TDDB lifetime remains constant regardless of the dielectric spacing, as the applied electric field is constant.

Figure 4.23 T63.2 against dielectric spacing with and without EM, at 125°C

At stress time $t = 0$,

$$E_{short,t=0} = \frac{V_{low}}{S_{short}} = \frac{V_{high}}{S_{long}} = E_{long,t=0} = E_{no\ EM} \text{ --- (4.9)}$$

$E_{short,t}$ is the electric field present in test structures with shorter dielectric spacing after stressing for a time t , and $E_{long,t}$ likewise for longer dielectric spacing. $E_{no\ EM}$ is the electric field biased for test structures with no EM stressing, and is therefore constant throughout the TDDB testing.

With EM present, the electric field in the dielectric will gradually increase with time, leading to the drop in TDDB lifetime. For test structures with a smaller spacing, the increase in electric field is more significant. This is because for the same Δs induced after EM stressing for a certain time t ,

$$s_{short} - \Delta s < s_{long} - \Delta s \text{ --- (4.10)}$$

Therefore,

$$E_{short,t} = \frac{V_{low}}{s_{short} - \Delta s} > \frac{V_{high}}{s_{long} - \Delta s} = E_{long,t} \text{ --- (4.11)}$$

From equation (4.11), it can be seen that the electric field for shorter dielectric spacing devices will increase more than that for devices with longer dielectric spacing. This leads to the shortened TDDB lifetime.

However, as stated in equation (4.9), the initial electric field magnitude is the same for test structures that did not experience EM, short dielectric spacing test structures with EM stressing and longer spacing test structures with EM stressing. The TDDB lifetime for all dielectric spacing is maintained at more than 99% of the TDDB lifetime without EM stressing. The EM effect on the TDDB lifetime is in fact minimal when the voltage is able to scale proportionally with the dielectric spacing, thereby keeping the electric field bias constant.

4.6.4 Limitation of the model

An assumption made for this model is that TDDB will not affect EM in the metal line i.e. EM-induced compressive in the metal line will not be changed by TDDB in the dielectric. The model also assumes that the metal line will not fail catastrophically by EM.

4.7 Summary

To study the effect of EM on TDDB, we designed a test structure that allows complete separation of the two phenomena. EM was first performed on the metal line, followed by TDDB on the adjacent dielectric. It was found that current in the metal line does have an adverse effect on the TDDB lifetime. This is believed to be due to the bulging of the metal line caused by the compressive stress built up during EM at the anode side, which led to the decrease in dielectric spacing. A reduction of the dielectric spacing will then increase the electric field, which will cause increased bond breaking of the dielectric, and also increased Cu ion migration leading to increased leakage current and thus earlier failure of the dielectric.

From the experimental results, a model is proposed to predict the effect of EM on TDDB lifetime. It was found that the EM effect on TDDB is largely dependent on the magnitude of the electric field applied. If the electric field applied becomes smaller, the EM effect on TDDB lifetime becomes higher. This is due to the longer breakdown lifetime, allowing EM to stress longer and hence higher compressive stress will build up. The opposite is true when higher electric field is applied. When the applied electric field is constant, the EM effect on TDDB breakdown lifetime is minimal.

CHAPTER 5: CONCLUSION

This chapter will summarize the work done in this project, and key conclusions will be emphasised.

5.1 Summary

The objective of this thesis is to study the effect of layout of the test structures on TDDB lifetime. The first part of the thesis focuses on the effect of having different areas on TDDB. Small area finger test structures were previously designed by Tan to study the failure mechanism of Cu/low-k interconnect structures. The small area test structure mimics a geometry seen in actual design layout. At the same time, the small area helps to contain the breakdown, so that physical failure analysis can be performed at the precise spot, eliminating the need for fault isolation such as TIVA and OBIRCH.

Thermally induced voltage alteration (TIVA) [118] and Optical Beam Induced Resistance Change (OBIRCH) [119] are fault localization techniques for failure analysis. They pinpoint the locations of electrical faults in the circuit and their operation principles are similar. With the device biased; OBIRCH uses a constant voltage, while TIVA applies a constant current, while a laser scans the surface of the circuit. When the laser encounters an electrical fault, localized heating occurs, which translates into a change in the resistance of the metal. This is detected by a change in output current for OBIRCH and a change in measured voltage for TIVA. The location of detection can be overlapped with a physical optical image of the circuit to map the exact failure location.

The Cu/low-k interconnect system was found to fail by delamination of the low-k dielectric from the capping layer, and also Ta and Cu migration into the dielectric during TDDB. However, there is insufficient study on how the TDDB results from the small area test structures relate to that of the conventional TDDB test structures. Hence for this study, three small area finger test structures with different areas were used to study the area scaling effect, and also relate the TDDB results to that of conventional comb-comb test structure.

It was found that the TDDB lifetime of small area test structures can be related by the Poisson area scaling law. However, when the same Poisson area scaling law was used to relate TDDB results of conventional comb-comb test structures to that of the small area test structures, the results do not match. Extrapolation of the results from conventional large comb-comb test structure to a small area will lead to an over-optimistic lifetime data. Analysis of the actual electric field distribution of the test structures was done to explain the discrepancy. FEM electric field stimulation was done using actual physical images from either SEM or TEM. The electric field simulation obtained reveals that the electric field was enhanced in both the small area and conventional test structures used. The enhancement was more severe for finger test structures than comb-comb test structure. The Poisson area scaling law was once again applied, this time using the maximum electric field obtained from the FEM simulation, but this again was not enough to explain the lifetime discrepancy satisfactorily.

Next, test structures with intermediate length between the small area test structures were designed and studied. The TDDB results from the intermediate test structures do not scale according to the Poisson area. Instead, the 200 μm test structure has a longer

lifetime compared to the 100 μm test structure. This result was seen for all three electric field split, and therefore not due to experimental errors. One possible explanation is due to the leakage in the dielectric, leading to the voltage dropping across the metal line. The voltage drops more as the metal line gets longer, and for longer metal lines, the voltage drop is faster. Hence the electric field is less effective for longer metal lines, and may explain why the longer 200 μm test structure has a lower breakdown lifetime than the 100 μm test structure. This can also explain why conventional comb-comb test structure has a longer than expected lifetime, compared to the extrapolated lifetime data from small area finger to large area comb-comb test area.

It can be learnt from this study that

- Poisson area scaling law is not able to relate the lifetime data gathered from small area test structures and large area conventional test structures.
- Large area conventional test structure has an inherent weakness of not being able to maintain the voltage across the long metal lines. Thus, it is not valid to use the lifetime data gathered from this test structure to predict the lifetime for actual circuits, especially when the actual circuit is filled with short metal lines with various geometries, and not long parallel metal line such as those in the conventional test structures.
- If the circuit layout contains mainly small area structure, it is necessary to use small area structures to predict the lifetime at use conditions instead of using a generic test structure to do the forecasting.

The second and third part of the project extends the idea of small area test structures to study the effect of actual layout on TDDB lifetime. The second part centres on the ramification of having neighbouring same potential electrodes in close proximity. As metal lines in actual circuits are not isolated, having active lines nearby will logically affect the electric field induced. This will certainly influence the breakdown lifetime as dielectric breakdowns are strongly dependent on the electric field applied. Four test structures were used in this study, each containing three pairs of finger electrodes. The distance apart between the electrodes differs, ranging from 0.1 μm , 0.2 μm , 0.4 μm to 3 μm .

Experimental results show that having electrodes in close proximity shortens the lifetime of the dielectric. Using FEM simulation, it was confirmed that the electric field was maximum at the tip of each finger. The maximum electric field for all four test structure was the same at 4.59 MV/cm, due to the curvature of the finger tip. All test structures have the same maximum electric field as the curvature is the same. Another point determined from the FEM simulation is that at 3 μm , the electrodes are spaced sufficiently far apart so that the electric field for each pair of electrode has no influence on the other. Using this information, an empirical formula was proposed to relate the TDDB lifetime to the distance apart from neighbouring electrodes.

It can be deduced from this relationship that

- TDDB lifetime decreases exponentially as the distance apart between the electrodes increases. The electric field interaction between the electrodes tapers off after approximately 1 μm apart.

- The electric field interaction between adjacent metal line decreases with decreasing voltage applied.
- As dielectric spacing scales smaller, the effect of adjacent metal lines on TDDB structure will get smaller if the voltage scales in proportion to maintain the electric field. However, according to the ITRS roadmap, the electric field in the interconnect will get higher as technology scales. This means that the effect of neighbouring wire will become more apparent at smaller technology.

The third and final part of the research focuses on the effect of current in the metal line on TDDB lifetime. This current will lead to EM occurring in the metal line. The test structure allows EM to be induced in the metal line, after which EM stressing is stopped, and TDDB stressing is performed in the adjacent dielectric. EM stressing was carried out for different times, ranging from 0 hour to 5 hours. The test structures have not failed by EM before undergoing TDDB testing. The TDDB results indicate that EM has a negative influence on the TDDB lifetime. A software, XSIM, was used to simulate the compressive stress in the metal anode after EM stressing, and it shows a similar trend to the TDDB lifetime.

It was learnt from this experiment that

- the failure mechanism is most likely due to the bulging of the metal line tip induced by the compressive stress from EM. Physical failure analysis verifies that the metal line tip has indeed deformed after EM.
- A methodology was proposed to study the impact of EM on TDDB lifetime. As the voltage applied during TDDB decreases, the effect of EM on TDDB lifetime increases.

- As dielectric spacing scales smaller, the effect becomes more significant if the electric field is kept constant. If the electric field increases as dielectric spacing becomes smaller, the effect actually becomes smaller although the actual TDDB lifetime decreases more significantly.

From this study it can be seen that the layout of the test structure and stressing conditions have a huge impact on the dielectric lifetime obtained. It is therefore not applicable to use a generic test structure to predict the lifetime of the circuit at use conditions. Instead, the geometry of the circuit should be analyzed, and the most vulnerable location identified. The accelerated testing should be performed on test structures with similar geometry to the most vulnerable spot. Furthermore, it was ascertained that the impact of neighbouring wires will become stronger as technology scales smaller. Although the effect of EM on TDDB lifetime becomes smaller, it is still significant. Therefore, these influences should be factored in during the prediction of TDDB lifetime at use conditions.

5.2 Future Work

Possible future work are suggested here to improve the work

- For area scaling, effect of the voltage drop can be further confirmed by using test structure with several points to apply potential.
- For EM and TDDB interaction and field interaction, no study was done on the effect of the interaction on activation energy. The time-to-breakdown for dielectric has temperature dependence as well. A temperature split has to be performed in order to extract the activation energy. Extracting the activation energy can provide information on the breakdown mechanism as well.

- For EM and TDDB interaction, the effect of the cathode side (void side) on TDDB lifetime was not studied. The cathode experiences tensile stress, until the void forms, after which the stress becomes zero. It is unknown if the tensile stress will affect the dielectric breakdown. It may even extend the dielectric lifetime as it prevents Cu and Ta from out-diffusion.
- For EM and TDDB interaction, EM and TDDB can be studied using the fundamental mass transport of the mobile defects, by extending the kinetic analysis developed by Korhonen for EM.
- For EM and TDDB interaction, anode via was seen to have an effect on the electric field. Since XSIM is a 1-D simulation, COMSOL Multiphysics can be used to simulate EM as well as TDDB to simulate in 2-D to take via into account.

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