Amorphous indium gallium zinc oxide thin film transistor and memory device for future device applications

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**AMORPHOUS INDIUM GALLIUM ZINC OXIDE THIN
FILM TRANSISTOR AND MEMORY DEVICE FOR FUTURE
DEVICE APPLICATIONS**

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SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

2014

**AMORPHOUS INDIUM GALLIUM ZINC OXIDE THIN
FILM TRANSISTOR AND MEMORY DEVICE FOR
FUTURE DEVICE APPLICATIONS**

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School of Electrical & Electronic Engineering

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ABSTRACT

Amorphous Indium Gallium Zinc Oxide (IGZO) is an important material which can be used in transparent thin film transistors (TFTs) due to its high field effect mobility for the next generation flat panel displays. Evolution of electrical properties and TFT characteristics of amorphous IGZO thin films synthesized with radio-frequency (RF) sputtering technique with O₂ plasma immersion has been studied. The a-IGZO thin film with O₂ plasma immersion can greatly enhance the Hall mobility while largely reduce the electron concentration. The influence of post-deposition O₂ plasma immersion has been studied. The electrical properties and the transistor performance can be attributed to the repair in the oxygen-related defects of the IGZO thin films. The threshold voltage (V_{th}) is an important parameter in TFTs performance which is determined by the electron concentration in the transistor channel layer; however it is not easy to control the V_{th} as the oxygen vacancies which are related to the electron concentration can be easily generated during the fabrication process. An exposure of the back channel of an IGZO TFT to ultraviolet (UV) activated oxygen can effectively shift the V_{th} of the TFT. There is a linearly relation between the V_{th} and the exposure time while the on-state current greatly increase with the exposure time. Other TFT parameters such as the field-effect mobility and sub-threshold swing are not significantly affected by the exposure. An exposure to UV-activated oxygen is a simple way to control the V_{th} , and the TFT can be easily changed from the enhancement mode to the depletion mode with this technique. The effect of the exposure on the V_{th} is attributed to the increase in the electron concentration of the channel layer as a result of the creation of

oxygen vacancies by exposure. Beside UV-activated oxygen exposure treatment, UV light is commonly used in the cleaning process to remove the particles and impurities on the thin film in the TFT fabrication. An UV exposure can cause a shift in the threshold voltage of IGZO TFT, which poses a problem to normal device operation. The effect of short-duration UV exposure on the V_{th} of amorphous IGZO TFTs and its recovery characteristics are investigated. The illuminated devices showed a slow recovery in threshold voltage without external bias. However, an instant recovery can be achieved by the application of positive gate pulses, which is due to the elimination of the positive trapped charges as a result of the presence of a large amount of field-induced electrons in the interface region. In the last chapter, the memory devices (e.g. non-volatile memory (NVM) and write once read many times memory devices (WORM)) based on O_2 plasma-treated IGZO thin films has been demonstrated. The WORM device has a normally-OFF state with a very high resistance as a result of the O_2 plasma treatment on the IGZO thin films. The device could be switched to an ON state with a low resistance by applying a voltage pulse. The WORM device has good data-retention and reading-endurance capabilities.

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LIST OF ABBREVIATIONS

a-Si:H	hydrogenated amorphous silicon
TFT	thin film transistor
AMLCD	active matrix liquid crystal displays
LCD	liquid crystal display
PDA _s	personal digital assistants
PC _s	personal computers
GPS	global position systems
CMOS	Complementary metal–oxide–semiconductor
OLED	organic light-emitting diode
QFHD	quad full high definition
HD	high definition
3D	three-dimensional
LTPS	low-temperature polycrystalline-Si
SPC	solid-phase crystallization
ELA	Excimer-laser annealing
AMOLED	active matrix organic light-emitting diode
ZnO	zinc oxide
FPD _s	flat panel displays

IGZO	indium gallium zinc oxide
a-IGZO	amorphous indium gallium zinc oxide
TOS	transparent oxide semiconductors
a-Si	amorphous silicon
poly-Si	polycrystalline silicon
AOS	Amorphous oxide semiconductor
PECVD	plasma enhanced chemical vapor deposition
UV	ultraviolet
WORM	write once read many times
XPS	X-ray photoelectron spectroscopy
V_{th}	threshold voltage
SSDM	Solid States Devices and Materials
ICMAT	International Conference on Materials for Advanced Technologies
c-Si	crystalline silicon
LDA	local-density approximation
CBM	conduction band minimum
PLD	pulse laser deposition
RF	radio frequency
VBM	valence band maximum
In_2O_5	indium oxide
Ga_2O_5	gallium oxide
UHV	ultra-high vacuum
IZO	indium doped zinc oxide
SCLC	space charge-limited conduction model

TE	thermionic emission
FETs	field-effect transistors
S/D	source/drain
Al	aluminum
Ti	titanium
Au	gold
SiO ₂	silicon dioxide
NBIS	negative bias illumination stress
IMID	International Meeting on Information Display
LGE	LG Electronics
PEN	polyethylene naphthalate
ROs	ring oscillators
HfO ₂	hafnium oxide
SC-1	standard cleaning
H ₂ SO ₄	sulfuric acid
TMA	Trimethylaluminium
ONO	oxide nitride oxide
C-V	capacitance-voltage
I-V	current-voltage

LIST OF SYMBOLS

μ_{eff}	field-effect mobility
S.S	sub-threshold swing
ρ	resistivity
A	area
R	resistance
t	thickness
V	voltage
I	current
I_{DS}	drain to source current
V_{DS}	drain to source voltage
Hz	Hertz
Pa	Pascal
μ_{sat}	saturation mobility
V_{GS}	gate to source voltage
$I_{\text{on}}/I_{\text{off}}$	on current versus off current ratio
V_{p}	pinch-off voltage
I_{off}	off-state current
I_{on}	on-state current

I_G	leakage current
g_m	transconductance
N_t	total trap density
q	charge of an electron
k	Boltzmann constant
ΔV_{th}	threshold voltage shift
β	stretched-exponential exponent
τ	characteristic trapping time of carriers
Ω	Ohm
μ	Hall mobility
n	electron concentration
μm	micro-meter
O_L	low binding energy
O_M	medium binding energy
O_H	high binding energy
C_i	gate capacitance
P_{inc}	power of the incident light
V_o	oxygen vacancies
W	channel width
L	channel length

Chapter 1 INTRODUCTION

1.1 Overview

1.1.1 Limitation of a-Si-H channel thin film transistor

Since the first hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) was successfully fabricated by Spear and Lecomber in 1970s,^{1, 2} a-Si:H has become the most useful electronic material in the TFTs devices that dominate the most active matrix liquid crystal displays (AMLCD) market.³⁻⁵ For the past few decades, liquid crystal displays (LCD) had experienced a strong growth and expanded rapidly which were exclusively used in the information equipment and visual equipment due to their good uniformity on the large area panel and low cost for the mass production fabrication. TFTs LCDs have been made into almost all kinds of visual display products, such as mobile phones, digital cameras, personal computers (PCs), camcorders, personal digital assistants (PDAs), game machines, TVs and global position systems (GPS), etc. The size of mother-glass has been enlarged from the first generation of 320 mm × 400 mm to the current 10th generation of 3130 mm x 2880 mm as the development trend of the displays requires a wider range of visual interfaces and a higher resolution.^{6, 7}

Figure 1.1 Mother-glass substrate size vs. application⁷

Nowadays, amorphous-Si (a-Si) TFT is a matured technology in the LCD industry. Just like Moore's law for Complementary metal oxide semiconductor (CMOS) technology, in order to make the production cost more effective, the development trend for LCD industry is focused on the size increase of mother-glass. The a-Si:H thin film can be easily deposited at a relatively low temperature ($< 350\text{ }^{\circ}\text{C}$) by plasma enhanced chemical vapor deposition (PECVD) to meet the thermal budget requirement. Although this technique has been well established to deposit highly uniform a-Si:H thin film which could support up to Generation 8 (Gen 8), the typical mobility of a-Si:H ($\sim 0.5 - 0.8\text{ cm}^2/\text{Vs}$) is insufficient to drive the ultra-large size (e.g. 90 inches) AMLCD with the compensation circuits. The situation for the AMLCD is changing in the recently years. The limitation of channel mobility in TFTs is a critical issue for the next generation display application. For example, the mobility for the ultra-high definition LCD required must be larger than $1\text{ cm}^2/\text{Vs}$, otherwise an extremely complex compensation circuit must be implemented in the a-Si-H based TFT displays.^{8,9}

The trend for AMLCD is toward to the larger size and higher resolution. To drive the quad full high definition (QFHD) resolution with 3840×2160 pixels (2K4K) at large size displays, the frame rate must be higher than 120 Hz to suppress the motion blue effect.¹⁰⁻¹³ The charging time

required for full-high definition display at 240 Hz would be only 3.7 μs for conventional driving methods, which was too short for the charging with a-Si TFTs on a large area panel display.¹⁴ Figure 1.2 shows the channel mobility of TFTs required for current and future displays.¹⁵ As can be seen in the figure, the conventional a-Si:H TFT nearly could not support the LCDs with pixels number of 10 million at high frame rate of above 120 Hz for the full-HD resolution due to the limited mobility ($\sim 0.5 - 0.8 \text{ cm}^2/\text{Vs}$). Although this shortage can be optimized or compensated by some alternative methods, e.g. combining the Cu-gate metallurgy with the gate electrode planarization technology¹⁶, using the buried-busline structure in the TFT devices with additional photolithography step,¹⁷ the driving circuit and the fabrication process would be very complicate for the mass production. The latest development of high quality image LCD is generally required to operate at 240 Hz or above. For example, the three-dimensional (3D) displays have appeared and grown very fast in the market with this 240 Hz driving technology. As the two picture frames for both left and right eye images are needed to be simultaneously switched for the stereoscopic images, the frame rate are required to be doubled compared to the conventional displays.¹⁸ Therefore, it is not a good choice to drive the low mobility a-Si:H based TFTs on large size LCDs at high frame rates. As the requirement for the future displays goes higher and higher (e.g. higher resolution, larger display panel size, etc.), the mobility requirement will be even higher in future.

Figure 1.2 Required carrier mobility vs number of pixels for future displays¹⁵

As high-mobility material for the channel is desired for the next generation display, low-temperature polycrystalline-Si (LTPS), which has a higher mobility and excellent stability compared to a-Si, has been adopted for the TFTs.¹⁹ There is an additional step in fabricating LTPS TFTs known as the crystallization process, which includes either non-laser crystallization annealing or laser annealing. The most simple and cost-effective method for non-laser crystallization is to anneal the a-Si thin film at 600°C or above for several hours which is known as solid-phase crystallization (SPC). The mobility after SPC can reach up to 800 cm²/Vs.^{20, 21} However, the long annealing time and high processing temperature for SPC are not suitable for large-area glass substrates. Laser annealing is a new technique which can be used to fabricate polycrystalline-silicon (poly-Si) TFTs at low temperature. Excimer-laser annealing (ELA) technique has been commonly used for TFTs mass production as it can produce excellent crystallinity phase at ~ 200°C - 300°C in few seconds. The device mobility of poly-Si TFTs with laser annealing could reach to 160 cm²/Vs.^{22, 23} However, the beam length of laser is narrow, the ELA method could not support large-size (e.g. Gen 8) mother-

glass due to the low throughput and laser-beam instability. Furthermore, the high maintenance cost is another major obstacle for the development of ELA method. In order to overcome these issues, a new TFT channel material, which can satisfy the requirement of high carrier mobility, relative low process temperature and excellent uniformity, is required for large size active matrix organic light-emitting diode (AMOLED) displays. It is believed that the replacement of the conventional TFT channel layer with metal oxide materials could be one of the alternative solutions.

1.2 Motivation

The a-Si:H TFT, which acts as the switching transistor in the AMLCD, has been a matured technology. The typical field effect mobility of a-Si:H TFT synthesized by plasma enhanced chemical vapor deposition (PECVD) ($0.6 \sim 0.8 \text{ cm}^2/\text{Vs}$) is too low to meet the minimum requirements of next generation displays; therefore, a new high mobility semiconductor material is highly desired. IGZO is one of the potential candidates for TFT channel which can stably withstand up to 500°C in amorphous phase. The high mobility and large area uniformity for a-IGZO TFTs have been demonstrated. On the other hand, there are some shortcomings for IGZO TFTs, such as the threshold voltage instability, process parameter variations etc. A systematic study on IGZO TFTs and memory device application of a-IGZO is carried out in this work.

1.3 Objectives

The aim of this project is to achieve enhanced understanding on the device behaviors of TFTs based on a-IGZO material. The objectives of this project are listed as below:

- To fabricate a-IGZO TFTs and investigate the device behaviors and performance including the transfer characteristics, field effect mobility, I_{on}/I_{off} ratio and sub-threshold swing, etc.
- To investigate the effect of O_2 plasma treatment on electrical performance of a-IGZO TFTs.
- To study the influence of ultraviolet (UV) -activated oxygen exposure on the threshold voltage of a-IGZO TFTs.
- To study the instability of a-IGZO TFTs under UV illumination and evaluate their recovery characteristics.
- To fabricate transparent nonvolatile memory (NVM) device and write once read many times memory (WORM) based on a-IGZO material.

1.4 Organization of thesis

This thesis consists of seven chapters:-

- *Chapter One* highlights the background, motivation, objectives and original contributions of this study.
- *Chapter Two* presents the literature review on the electronic structure of IGZO, characterization of IGZO thin films, device operation and instability issues of a-IGZO TFTs.
- *Chapter Three* presents a-IGZO TFT fabrication process, evaluates the electrical properties of the device and the effect of O_2 plasma treatment on the transistor performance.
- *Chapter Four* investigates the effect of exposure to UV-active oxygen treatment on a-IGZO TFTs.

- *Chapter five* investigates the electrical instabilities in a-IGZO TFTs under UV illumination and discusses the UV photodetector application of a-IGZO TFTs.
- *Chapter six* presents the memory applications based on a-IGZO thin films including the transparent NVM and WORM memory.
- *Chapter seven* presents the overall conclusion of this thesis and the recommendations for the future work.

1.5 Original contributions

The research focuses on the post O₂ plasma immersion effect on the a-IGZO TFTs and the recovery characteristics of UV-illuminated IGZO TFTs. The WORM memory application of the a-IGZO thin films is also investigated. The original contributions are listed as follows:

- The TFT with the bottom-gate structure based on a-IGZO thin film was successfully fabricated with the standard TFT fabrication process. The resistivity of the a-IGZO thin film can be easily tuned by varying the ratio of oxygen/argon flow rates during the RF sputtering deposition. It was found that the device performance of the TFT was poor when there was no oxygen gas involved during the sputtering process. However, the TFT exhibited a good transistor performance after an O₂ plasma immersion was carried out on the surface of IGZO channel.
- The effect of O₂ plasma treatment on the IGZO TFTs was investigated. The X-ray photoelectron spectroscopy (XPS) analysis was carried out to study the chemical properties of the IGZO thin film. Enhancement in the Hall mobility and decrease in the electron concentration by O₂ plasma immersion are observed. The electrical performance of the TFT such as field-effect mobility, off current, sub-threshold swing and on current to off current ratio (I_{on}/I_{off}) is greatly improved. These

improvements were attributed to the reduction of the oxygen-related defects in the active channel of the a-IGZO TFTs. Based on the effect of O₂ plasma immersion on the a-IGZO channel, high performance a-IGZO TFTs have been demonstrated.

- The effect of the exposure of the back channel of a-IGZO TFTs to UV-activated oxygen has been studied. The exposure can effectively shift the threshold voltage (V_{th}) to the more negative voltage regime. A linear relationship between V_{th} shift and duration of the UV-activated oxygen exposure was observed. This exposure method could be considered as a simple way to modulate the V_{th} after device fabrication. The TFTs could be easily switched from the enhancement mode to the depletion mode by the exposure.
- The effect of UV illumination on the threshold voltage of a-IGZO TFTs was investigated. The V_{th} exhibited a negative shift after UV illumination, and the shift showed a slow recovery characteristics without external bias; however, an instant recovery could be achieved by the application of a positive gate pulses. The examination on the resistivity and electrical characteristics suggests that the instant recovery is due to the elimination of the positive trapped charges as a result of the field induced free electrons at the interface region.
- Memory applications of IGZO thin films are demonstrated. A transparent a-IGZO based non-volatile memory (NVM) was fabricated. The memory behaviors have been studied. WORM memory based on O₂ plasma-treated IGZO thin films was demonstrated also. The WORM device based on a simple Al/IGZO/Al structure shows a large ON/OFF memory window, long data-retention time and good reading endurance.

Our research works have been published in established international conferences and peer reviewed journals, such as the Solid States Devices and Materials (SSDM) symposium,

International Conference on Materials for Advanced Technologies (ICMAT) symposium, Applied Physics Letter, Electrochemical Society Solid State Letter, and Thin Solid Film.

Chapter 2 LITERATURE REVIEW

2.1 Introduction

Of the various types of AOS TFTs, a-IGZO TFTs have been most widely and intensively investigated in recent years. The a-IGZO is expected to be the new channel material of TFTs, as it can satisfy almost all of the requirements of next-generation flat panel displays such as HD-OLED and 3D AMLCD. These new displays are not easy to construct using traditional silicon material because they require a high level of mobility. The typical a-IGZO TFTs exhibit a field-effect mobility (μ_{eff}) of 2~20 cm²/V-s, low off-currents of the order of 10⁻¹² A, sharp sub-threshold swings (S.S) and a high $I_{\text{on}}/I_{\text{off}}$ ratio. This chapter includes a review of recent IGZO material investigations and the present status of TFT applications.

2.1.1 Background

The first report on TFT fabricated with single crystal metal oxide (e.g. zinc oxide (ZnO)) was published in 1968,²⁴ but not much progress was made subsequently. This situation, however, started to change in the late 1990s since intensive research works on metal oxide semiconductors (e.g. ZnO²⁵) had been published. Recently, significant progress in the research of ZnO TFTs has been reported.²⁶⁻²⁸ [ENREF 27](#) [ENREF 28](#) These studies show that metal oxide semiconductors are promising candidates to replace the a-Si:H as the channel layer of TFTs for flat panel displays (FPDs) applications. However, some critical

issues must be taken into account for metal oxide based TFTs, for example, it is not easy to fabricate a normally-off TFT based on poly-ZnO channel layer as the electron concentration of ZnO thin film is extremely high due to the grain boundaries. Another common issue among all the metal oxide semiconductors is the instabilities of electrical properties due to the adsorption and desorption of oxygen and water molecules from the ambient environment.

A high-quality single-crystalline Indium Gallium Zinc oxide (IGZO) was proposed as the alternative material for the channel layer that can overcome some of the issues. The density of residual carriers in single-crystalline IGZO is much lower than that of ZnO, thus an IGZO channel layer could easily result in a normally-off TFT.²⁹ The amorphous IGZO (a-IGZO) thin film was proposed as the channel layer for TFTs as it does not suffer from the grain boundary issue that is typically found in ZnO based TFTs. The first TFT based on a-IGZO thin film was successfully demonstrated by K. Nomura et al. in 2004.³⁰ When a-IGZO is used as the channel layer in a TFT, the TFT shows much better performance compared to a-Si-H TFTs and organic TFTs,³⁰ The transparent oxide semiconductors (TOS), such as ZnO³¹⁻³³, In-Zn-O^{34, 35}, Zn-Sn-O³⁶, Zn-In-Sn-O³⁷⁻³⁹, La-In-Zn-O⁴⁰ and In-Ga-Zn-O⁴¹⁻⁴⁴, have attracted much interests due to the controllable carrier concentration, wide bandgaps and high transparenence in the visible range, which make them very promising for the transparent TFTs application for the next generation flat-panel displays. In addition, AOS can be deposited at room temperature, making the TFTs fabrication on flexible or plastic substrates possible.

Oxide semiconductor based TFTs could provide unique properties that combine the advantages of a-Si and poly-Si based TFTs. The key parameters for the TFTs technology among the a-Si, poly-Si and oxide semiconductor are summarized in Table 1.1. As can be seen in the table, oxide TFTs can be deposited by a simple sputtering process at room temperature, which can easily support the size of mother-glass up to Gen 8. Without the need of annealing, the channel layers exhibits the excellent uniformity and stability in mobility and

threshold voltage. The channel mobility of metal oxide TFTs is about 10 times higher than that of a-Si:H TFTs. In addition, the process for oxide semiconductor TFT is fully compatible with the a-Si:H TFTs mass production technology, thus, no significant modifications are needed for the existing production line. Moreover, the oxide TFTs can be fabricated at room temperature, which makes it possible for the mass production of AMOLEDs on flexible plastic substrates or cheap soda-lime glass.

	a-Si TFT	Poly-Si TFT	Oxide TFT
Semiconductor	Amorphous Si	Polycrystalline Si	Amorphous IGZO
TFT uniformity	Good	Poor	Good
Channel mobility	1 cm ² /V-sec	~100 cm ² /V-sec	10-40 cm ² /V-sec
Cost	Low	High	Low
Process temperature	150°C-350°C	250°C-550°C	27-400°C

Table 2.1 Comparison of TFT technologies based on a-Si, poly-Si, and oxide semiconductor.⁴⁵

In the last ten years, the industrial players have successfully demonstrated several prototypes based on AOS TFTs, such as electronic paper (e-paper), AMOLED and AMLCD as shown in Figure 2.0. Although various types of AOS with even higher mobility have been investigated, these prototypes for display application are all based on a-IGZO material.

Figure 2.0 Recent a-IGZO TFTs prototype flat panel devices. (a) 2 inch, VGA, 400 ppi, flexible back and white paper, Toppan 2009.⁴⁶ (b) 4 inch QVGA color electronic paper, Toppan 2008.⁴⁷ (c) 2.5 inch transparent OLED display, LGE and ETRI, 2009.⁴⁸ (d) 3.5 inch, flexible QCIF AMOLED by LG, 2007.⁴⁹ (e) 19 inch QFHD AMOLED by Samsung Mobile Display Co. Ltd, 2009.⁵⁰ (f) 37 inch FHD AMLCD by AUO, TAOS 2010.⁵¹

High carrier mobility in the TFTs is just one of the minimum requirements for the flat panel devices; other requirements such as controllability of carrier concentration, degradation of electrical performance, uniformity of the thin film by sputtering process and the fabrication flow compatibility with current TFT technology are even more important. a-IGZO can satisfy all these requirements; thus, it is the most promising TFT channel material for the next generation flat panel displays.

2.1.2 Origin of large electron mobility for IGZO material

Intrinsic crystalline silicon exhibits an electron mobility of $1,500 \text{ cm}^2/\text{Vs}$, and a-Si:H shows a significantly degraded mobility of less than $1 \text{ cm}^2/\text{Vs}$. Similar to the case of Si, it is

believed that the properties of a-IGZO should show considerable degradation (e.g., carrier mobility) compared with the corresponding single crystalline phase. IGZO is a ternary oxide that consists of In_2O_3 , Ga_2O_3 and ZnO with the structure of the edge-sharing MO_6 octahedra. The ns orbitals of these metal elements have the potential to form conduction band bottoms, which could form electron transportation paths in a-IGZO.⁵² Figure 2.1 shows the crystal structure diagram of the InGaZnO_4 system. Nomura et al. examined the local coordination and electronic structures of a-IGZO thin films and proposed a method for calculating the a-IGZO electronic structure at the local-density approximation (LDA) level from the wave plane. The supercell pseudoband calculation shows that the conduction band minimum (CBM) of a-IGZO is composed of In 5s orbitals hybridized with O 2p (Figure 2.1). Although a-IGZO has no localized state in the vicinity of the conduction band bottom, there is a rather large overlap between the neighboring In 5s orbitals. The electronic states at the edge of the conduction band are primarily formed by the overlap among these In 5s orbitals.⁵³ Therefore, the electron transportation path in a-IGZO is insensitive to variations in the metal-oxide chemical bond angle caused by structural randomness during the amorphous phase. The Ga to oxygen (Ga-O) ionic bond in the IGZO system is much stronger than that of the Zn and In ions that could suppress the carrier generation from the oxygen vacancy formation. Thus, the a-IGZO could stably withstand up to $\sim 500^\circ\text{C}$, a temperature higher than that of ZnO due to the incorporation of Ga ions.³⁰ The a-IGZO thin film can be deposited using several methods such as pulse laser deposition (PLD),^{54, 55} radio frequency (RF) magnetron sputtering,⁵⁶ DC magnetron sputtering⁵⁷ and the sol-gel solution process.⁵⁸ RF magnetron sputtering is the most attractive method due to its high deposition rate and large-area mass production capability.

Figure 2.1 Wave function ($|\psi|^2$) composed of In 5s orbitals hybridized with O 2p in an a-IGZO structure. The red wave represents the CBM.⁵³

The CBM of a conventional amorphous covalent semiconductor (e.g., a-Si:H) is composed of Si sp^3 hybridized orbitals, the anti-bonding and bonding states of which have a strong spatial directivity. The magnitude of overlap between the vacant orbitals of the neighboring atoms is very sensitive to variations in the bond angles. The carrier transport in Si is controlled by nearest-neighbor hopping or Mott's variable range hopping at a low temperature.⁵⁹ The deep and high-density localized states, which are in the middle of the CBM and the valence band maximum (VBM), are formed by the distorted chemical bonds in amorphous structures. Hence, the amorphous silicon has a much lower mobility due to carrier trapping than that of the crystalline silicon (Figure 2.2(a)). The essential drawback of conventional amorphous covalent semiconductors is the significant deterioration in carrier mobility from the single crystal to amorphous phases compared with metal oxide semiconductors, which still have a relatively high electron mobility even in the amorphous phase ($> 10 \text{ cm}^2/\text{Vs}$). Figure 2.2(b) shows the electronic structure of IGZO material in the single crystal and amorphous phases. The high mobility of a-IGZO is attributed to the strong

iconicity of the oxides. The conduction band in AOS (e.g., IGZO) is mainly made up of the overlap between the metal ion's (e.g., Ion) ns orbitals. Electrons can be transported within these metal ion's ns orbitals due to the isotropic properties. A strained amorphous structure does not significantly affect the electron-conducting path due to the direct overlap between the ns orbitals and neighboring metal ions' orbitals. The conducting path and carrier mobility can be preserved even in the amorphous phase, when there is a sufficient ns orbital overlap between the metal ions. The spherical symmetry structure of the metal ions' ns orbitals renders the metal oxide semiconductors insensitive to structural deformation, maintaining high mobility in the amorphous state.

Figure 2.2 Schematic diagram of the orbital structure of the electron transport pathway in (a) conventional covalent bond semiconductors (e.g., Si) and (b) ionic oxide semiconductors.³⁰

The electron paths are formed by the major consistent (e.g., Indium, gallium and zinc) and unoccupied s orbitals in IGZO, and the amount of metal ions determines the magnitude of the electron mobility. Figure 2.3 shows the Hall mobility of a-IGZO films as functions of the chemical composition of ZnO, In₂O₃ and Ga₂O₃ at room temperature.⁶⁰ As can be seen in

the figure, indium doped zinc oxide (IZO) and ZnO are more mobile than IGZO in the as-deposited states. The carrier concentration of the channel layer must be maintained at a relatively low level for TFT to have a high on/off current ratio and a low off-state current. It is not ideal to adopt IZO or ZnO thin film in the TFT channel, as both exhibit a very high carrier concentration in their as-deposited states.^{34, 61} Incorporating Ga^{3+} could suppress the formation of oxygen deficiencies and the generation of mobile electrons in IGZO thin film due to the strong Ga-O bonds.⁶² As shown in Figure 2.3, electron mobility deteriorates with the addition of gallium content. The Ga element could be considered the stabilizer in the IGZO system, as it is used to obtain a stable AOS material and a reliable TFT. Hosono's comparative study of a-IZO and a-IGZO showed that a-IGZO thin film can have five orders of magnitude reduction in its carrier concentration compared with that of a-IZO under the same deposition condition.⁶³

Figure 2.3 Hall mobility in cm^2/Vs (outside parentheses) and carrier concentration in 10^{18}cm^{-3} (in parentheses) as functions of the chemical composition of ZnO, In_2O_3 and Ga_2O_3 at room temperature.⁶⁰

In addition to the channel's low mobility requirement, low light transmittance at a visible range and photon absorption are major drawbacks of using a-Si:H in optoelectronics and transparent circuits. Although a-Si:H is widely used in TFT backplanes, light-induced instability is a critical issue in Si-based circuits due to the small band gap.⁶⁴ Metal oxide semiconductors (e.g., ZnO, IGZO, IZO, etc.) are wide band gap materials with an overall transmittance of over 80% in the visible range. The high transmittance level allows the display or sensor to be operated in the direction transmission mode to improve the pixel aperture ratio. Thus, AOS has attracted much attention in the research field in terms of its application to future innovative vision-free products and optoelectronics,⁶⁵ such as transparent electronic and see-through displays. In summary, a-IGZO possesses unique physical properties and superior electrical performance in TFT applications. IGZO is one of the most promising materials for switching or driving elements in future display applications.

2.2 Characterization of IGZO thin film

The properties of IGZO thin film and TFT devices can be measured using various semiconductor characterization techniques. This section presents a review of the semiconductor characterization equipment used in this study, which includes the four-point probe, X-ray spectroscope and I-V characterization system.

2.2.1 Four-point probe measurement

The “four-point probe” proved to be a convenient tool for measuring the resistivity of semiconductor material. The results were expressed as a functional relationship between the resistivity, measured voltage and current readings depending on the sample geometries. The resistivity of the bulk was obtained by measuring the voltage through the inner two probes (probes 2 and 3 in Figure 2.4) and the current passing through the two outer probes (probes 1 and 4 in Figure 2.4).⁶⁶ Figure 2.4 shows the configuration setup of the four-point probe.

Figure 2.4 Schematic of the four-point probe configuration

The equipment consists of four tungsten metal tips that can travel up and down to the stage during the measurement. The four tips are spaced apart equally at ~ 1 mm (s). The two inner probe voltages are measured when a current is supplied through the two outer probes. The metal tips are assumed to be infinitesimal for the deviation. The differential resistance between the two terminals can be expressed as follows:⁶⁷

$$\Delta R = \rho \left(\frac{dx}{A} \right) \quad \text{Eq. (2.1)}$$

where ρ is the resistivity of the sample and A is the area of sample. When the thickness of the sample film is thin enough (e.g., $t \ll s$), it can be assumed that the current flow is a ring between the outer two tips. Thus, the following integration can be carried out:

$$R = \int_{x_1}^{x_2} \rho \frac{dx}{2\pi x t} = \int_s^{2s} \frac{\rho}{2\pi x} \frac{dx}{t} = \frac{\rho}{2\pi x} \ln(x) \Big|_s^{2s} = \frac{\rho}{2\pi t} \ln 2 \quad \text{Eq. (2.2)}$$

where $\pi / \ln 2$ can be denoted as constant $k = 4.53$. The resistivity of the thin film can be

finalized as follows:

$$r = \frac{\rho t}{\ln 2} \frac{V}{I} = 4.53 t \frac{V}{I} \quad \text{Eq. (2.3)}$$

2.2.2 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy is a quantitative spectroscopic technique used to analyze fundamental parameters such as the chemical elemental composition, chemical state and electronic state of the elements at the surface of a sample. The measurement is carried out at an ultra-low vacuum level ambient of less than 1×10^{-9} Torr. The sample surface is irradiated with a focused monochromatic X-ray beam (150 W, 1.5 KV and 10 mA). The electrons of an atom from the sample's core shell are emitted out from the top surface and collected by the electron energy analyzer. The electron detector can record a number of electrons, which are emitted from the surface at 1-10 nm of the material under ultra-high vacuum (UHV) conditions. The XPS spectrum is collected in 1-eV intervals ranging from 0 to 1,100 eV, and calibrated by aligning it to the reference position of C 1s. Figure 2.5 shows the basic component setup of the XPS system.

Figure 2.5 Schematic diagram of a typical XPS system with the critical components.

The measurement spectrum plot shows the counts of electrons detected at various binding energies. Each chemical element of the material has a set of peaks at a specific

binding energy. These peaks reflect the composition of the material. For example, the XPS spectrum of IGZO thin film can be used to analyze the amount of each element, which includes indium oxide (In_2O_3), gallium oxide (Ga_2O_3) and ZnO, on the irradiated surface areas. This technique is useful for examining changes in material chemistry before and after surface reactions, such as in O_2 plasma and UV-activated oxygen treatments.

Figure 2.6 Deconvolution of the O 1s region of In-doped ZnO thin film.⁶⁸

Figure 2.6 shows the typical XPS spectrum of the O 1s region in IZO thin film.⁶⁸ The O 1s peak (red line) spectrum of the metal oxide thin film can be fitted by three near Gaussians centered at different binding energy levels. Each peak represents a chemical element of the oxygen state, including the O^{2-} ions, O^{1-} ions and O_2 species. For example, the lower binding energy peak at 530.79 eV is related to the O^{2-} ions that are fully bonded with the nearest metal atoms.⁶⁹ In this study, a surface treatment was performed on the IGZO thin film. The XPS result was used to analyze the oxygen content in the IGZO thin film before and after treatment.

2.2.3 Current-voltage (I-V) measurement

In this study, the current-voltage (I-V) characteristic was measured using a Keithley 4200 semiconductor characterization system with a switching matrix. The device operation performance of a-IGZO TFTs is typically evaluated by measuring the drain-to-source current versus the gate-to-source voltage (I_{DS} versus V_{GS}) and the drain-to-source current versus the drain-to-source voltage (I_{DS} versus V_{DS}). The device performance parameters (e.g., S.S, field effect mobility, on-current/off-current ratio, etc.) are derived from the measured I-V curves reviewed later. Figure 2.7 shows the typical output characteristics of an a-IGZO TFT.

Figure 2.7 Typical output characteristics of a transparent flexible TFT using the IGZO channel.⁶³

In addition to evaluating device performance, the I-V characteristic is used to determine the current conduction mechanism in thin film. Figure 2.8 shows the I-V characteristic curves of a metal electrode/IGZO/metal electrode cell as reported by Kim et al.⁷⁰ As shown in Figure 2.8(a), the IGZO thin film exhibits a difference in current conduction between the non- and after-forming processes, indicating the different

mechanisms involved. The current conduction mechanism can be identified by the logarithmic scale of the I - V characteristics. For example, the space charge-limited conduction model (SCLC) follows $I \propto V^n$ in the plot of $\log I$ - $\log V$,^{71,72} Ohmic conduction follows $I \propto V$ and thermionic emission (TE)⁷³, and so on. As Figure 2.8(b) shows, the current conduction in the RESET state follows Ohmic conduction at the low voltage region and switches to SCLC in the high voltage region. This indicates that the current conduction in the thin film changes from Ohmic behavior to SCLC when the device switches from the SET to RESET states.

Figure 2.8 (a) Small voltage bias region of I - V characteristics of an Au/IGZO/Pt thin film cell during the non-forming and after-forming processes. (b) I - V characteristics of an Au/IGZO/Pt thin film cell in a logarithmic scale. Resistance switching I - V characteristic curves of (c) an Au/IGZO/Au cell and (d) a tungsten tip on an W/IGZO/Al cell.⁷⁰

The dual sweeping I - V measurement method is commonly used to investigate the switching effect of the device. Resistance switching effects are usually observed in the metal oxide thin film. Figures 2.8(c) and (d) demonstrate the switching effect in the IGZO thin film

along with Au and Al electrodes by sweeping the bias from 0 to 5 V and back to 0 V. Both the Au/a-IGZO/Au and W/a-IGZO/Al devices show the switch from a high-resistance state to a low-resistance state, indicating that the switching effect can occur in different metal electrodes with different work functions. An external bias can form or rupture the conduction path between two electrodes, causing resistive switching during current conduction.⁷⁰

2.3 IGZO TFT structure and fabrication

The typical TFT device structure is composed of gate electrodes, gate insulator layers, TFT channel layers and source/drain electrode contacts. The structure can be further classified into top/bottom gates with top/bottom contacts based on the fabrication process. Figure 2.9 shows two structures that are commonly adopted in AOS TFTs. The top gate structure is widely used in the mass production of TFTs. It requires only a minimum of two mask patterning steps with an epitaxial layer for TFT fabrication. The top electrode and gate insulator layer protect the channel layer from external damage by exposing it to atmospheric water molecules, oxygen gas and light illumination. Many improvements have been made on this structure to enhance the performance of the device and decrease the instability caused by photo sensitivity⁴⁸ and parasitic capacitance⁷⁴.

Figure 2.9 Typical device structures adopted in AOS TFTs.¹⁴⁷

The bottom gate structure is always used in laboratory research. The heavily doped commercial Si wafer can be considered a gate electrode due to its ultra-low resistivity. The

bottom Si gate can eliminate one patterning step from the TFT fabrication process compared with the top gate structure. The TFT can thus be easily fabricated using a single mask to pattern the source and drain contacts. To suppress leakage current as the thickness of the gate insulator becomes increasingly thinner, an additional mask is required to pattern the active channel. The bottom gate structure has several disadvantages. Firstly, a-IGZO TFTs present some critical electrical instability issues caused by channel surface absorption and desorption reactions to ambient oxygen and water molecules in the surrounding atmosphere.^{75, 76} Secondly, the gate electrodes and source/drain contacts present a large area of overlap when the entire Si substrate is used as a gate electrode. The slow circuit response causes a large parasitic capacitance in the TFTs. Thirdly, as flat panel display is an electronically modulated optical device made up of a number of segments filled with liquid crystals and arrayed in front of backlight to produce image in color, the Si substrate blocks the most of the backlight. Therefore, this structure is not recommended for use in practical flat panel displays. In terms of the electrode contacts, either a top source/drain or bottom source/drain contact structure is suitable for AOS TFTs. The bottom source/drain contact structure is more difficult to form, as it requires more care than the bottom contact structure.⁵⁶ In addition, the top contact layer can effectively minimize the interface oxidation between the source/drain electrode and active channel layer, and is widely used in AOS TFTs for this reason.

Figure 2.10 Two types of typical inverted staggered structures.¹⁴⁷

The inverted staggered structure was developed from the bottom gate structure with either an etch stopper or appropriate passivation. Figure 2.10 shows the two types of inverted staggered structures. One type is known as a channel-etch structure, in which the surface of the back channel layer is etched together with the source/drain contact. This method requires a thick channel layer, as the channel is partially removed after formation. Formerly, the channel-etch structure was used only in a-IGZO TFTs for AMOLED display panels, as the etch process damaged the channel and thereby degraded the performance of the device. The other type is an etch-stopper structure, in which an extra etching protection layer is deposited on top of the channel layer before the deposition of the source/drain contact.⁷⁷ Although this structure can help prevent the permanent degradation of TFT characteristics caused by the back channel etch process, an extra mask is required. The etch-stopper structure offers a better gate-bias thermal stability than the channel-etch structure, which suppresses the formation of interfacial byproducts on the active layer during the patterning process. Jeong et al. examined these two structures and showed that passivated back-channel-etch Al-Zn-Sn-O TFTs exhibited a much better temperature and bias stability than a structure without a protective layer.^{78, 79} To improve the contact resistance of the source/drain electrodes and obtain a good Ohmic contact between the electrodes and channel, a co-planar structure has been adopted in a-IGZO TFTs that places the source/drain contacts on the same plain as the channel layer.^{80, 81}

The common bottom gate TFT structure was used in this study to investigate the fundamental electrical properties due to its ease of fabrication. Involving mask layers in the TFT fabrication effectively eliminated most of the process-induced variation issues. The structure used in the experiment was similar to the TFTs used in an actual display or imager

backplane. A brief discussion of the fabrication processes of the common gate a-IGZO TFT with PLD and RF sputtering is presented as follows.

A) Common bottom gate a-IGZO TFT fabricated by pulse-laser deposition

The common-gate inverted-staggered a-IGZO TFT is the most convenient test structure for studying fundamental electrical properties. The device starts with a heavily doped (n++) silicon wafer substrate, which serves as a gate electrode. The silicon dioxide (SiO₂) dielectric layer is then grown on the top surface via thermal oxidation, followed by the deposition of the a-IGZO active layer via PLD with a polycrystalline IGZO target. Figure 2.11 shows the schematic diagram of a PLD system. The KrF excimer laser pulses (with a wavelength of 248 nm) are focused on the target through external lenses and mirrors. The laser energy density is usually set at 1.5-3 J/cm² per pulse. The carrier concentration of the channel can be tuned from $\sim 10^{13}$ to 10^{20} cm⁻³ by varying the oxygen pressure in the chamber from 0.1 to 7.0 Pa during the deposition.⁸² The substrate is placed in an ultra-high vacuum chamber and kept away from the target at a distance of 3 cm.

Figure 2.11 Schematic setup of a PLD system⁸³

Macro-island patterning before the source/drain (S/D) electrode deposition is necessary to decrease the gate leakage current in the channel layer. This island can be defined by the lithograph process and patterned by the wet etch process with a diluted acid solution. The aluminum (Al) S/D electrodes are subsequently deposited through the mask openings via thermal evaporation. A titanium (Ti) and gold (Au) stacked layer can also be used to form the Ohmic contact between the electrodes and IGZO channel, which exhibit similar electrical properties to aluminum electrodes. Finally, the fabricated devices are subjected to the annealing process in air at 300°C for 5 minutes. Figure 2.12 shows the TFT fabrication process flows using the PLD method.

Figure 2.12 Detailed process of fabricating a common-gate top-contact a-IGZO TFT by PLD: (a) deposition of SiO_2 dielectric layer via oxidation; (b) deposition of a-IGZO thin-film via PLD; (c) macro-island formation by lithography and wet etch process; (d) evaporation of Al source/drain with mask.

B) Common bottom gate a-IGZO TFT fabricated by radio-frequency sputtering

Although the TFT structure discussed previously is easy to fabricate, the loss of control resulting from channel current confinement is a critical issue with the macro-island structure. An application of positive bias from the gate electrode can induce an electron cloud at the channel/dielectric interface, making the entire a-IGZO layer highly conductive. If the deposited a-IGZO layer is not etched properly at the edge of the macro island, a large amount of current leaks through the dielectric layer from the gate electrode. To overcome this issue,

an additional patterning process for the active island is used to separate the channel layer for each individual TFT.

Figure 2.13 Process flow for making a common-gate inverted-staggered a-IGZO TFT via RF sputtering: (a) deposition of SiO_2 dielectric layer by oxidation; (b) deposition of a-IGZO active layer by RF magnetron sputtering, with the active channel patterned by lithography and the wet etch process; (c) photoresist (PR) patterning and blanket deposition of the Au/Ti stack layers; (d) photoresist stripped off.

Figure 2.13 illustrates the fabrication flow of the common-gate inverted-staggered a-IGZO TFT structure according to the RF sputtering process. Following the process discussed earlier, the TFT fabrication starts with a heavily doped n-type silicon substrate wafer overlay with SiO_2 . An a-IGZO thin film is then deposited according to the RF sputtering process. The sample is then placed on the electrode facing the IGZO target, which is mounted at the counter electrode. Figure 2.14 shows the schematic setup of the RF sputtering system. The

shutter between the target and substrate helps to prevent contamination resulting from the sample loading/unloading and preconditioning. The thickness of the deposited thin film is controlled by the opening and closing of the shutter. A high-frequency generator is used to generate electromagnetic power in the MHz region (normally operated at 13.56 MHz).⁸⁴

Figure 2.14 RF sputtering configuration in a-IGZO deposition.⁸⁵

The chamber pressure must be maintained at 1.0×10^{-4} Pa before the thin film deposition. The IGZO target is pre-sputtered with pure argon gas for 10 min to remove the surface native oxide and contamination particles at 0.13 Pa throughout the process. The sputtering deposition is then carried out with a mixture of oxygen and argon gases at room temperature. The electrical properties of IGZO thin film strongly depend on the oxygen gas ratio in the mixture of oxygen and argon gases during deposition. Figure 2.15 shows the electrical properties of IGZO thin film prepared by the RF sputtering process as a function of the oxygen gas flow.⁸⁶

Figure 2.15 Dependence of the oxygen gas rate on the electrical properties of IGZO thin film prepared by the RF sputtering process.⁸⁶

The electron mobility and carrier concentration of a-IGZO thin film can be controlled precisely to suit the application of TFT devices. Shin and Choi reported the optical properties of a-IGZO sputtered in different oxygen ambient in addition to its electrical properties, as shown in Figure 2.16.⁸⁷

Figure 2.16 Effect of oxygen ratio on the optical transmission spectra of a-IGZO thin film prepared by RF sputtering.⁸⁷

The overall optical transparency of a-IGZO in the visible range is greater than 80% with or without oxygen content involved during the deposition. The peak wavelengths of the a-IGZO thin film deposited in oxygen ambient shifts to the shorter wavelength values compared with the film deposited without oxygen content. This suggests that the optical band gap can be controlled by the oxygen flow during the a-IGZO thin film deposition process.⁸⁷ After a-IGZO thin film deposition, the a-IGZO active island is patterned by lithography and the wet etching process. Finally, the S/D electrodes are patterned by the lift-off technique as follows: the photoresist is initially patterned by photolithography followed by a blanket deposition of the gold/titanium (Au/Ti) stacked layer, as shown in Figure 2.13(c). The photoresist is then stripped off to remove the unwanted Au/Ti material except for the S/D electrodes (Figure 2.13(d)).

2.4 Device operation characterization of a-IGZO TFTs

The device performance of a TFT is determined by several parameters, including field effect mobility (μ_{FE}), saturation mobility (μ_{sat}), threshold voltage, the on/off state current ratio and the S.S. These parameters can generally be extracted from the transfer characteristics by measuring the source-to-drain current (I_{DS}) versus the gate-to-source voltage (V_{GS}) at a fixed source-to-drain voltage (V_{DS}) level in compliance with the gradual channel approximation, and from the output characteristics by measuring the I_{DS} in terms of V_{DS} at a fixed V_{GS} . Figure 2.17 shows the output characteristic (I_{DS} – V_{DS}) of a-IGZO TFTs with various V_{GS} levels at room temperature.⁶³ The device exhibits a typical n-type channel behavior transistor in the enhancement mode. In the region with a low drain voltage, I_{DS} linearly increases with V_{DS} , which is known as the linear region, and saturates after a specific pinch-off voltage (V_p), which is known as the saturation region.

Figure 2.17 Typical output characteristics of an a-IGZO TFT device.⁶³

The drain current in the linear and saturation regions follows Eqs. (2.1) and (2.2) with several parameters, respectively:-^{88, 89}

$$I_{ds} = \frac{W}{L} \mu_{FE} C_{ox} [(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2] \quad \text{Eq. (2.4)}$$

$$I_{ds} = \frac{W}{2L} \mu_{sat} C_{ox} (V_{GS} - V_{th})^2 \quad \text{Eq. (2.5)}$$

where V_{th} is a constant known as the threshold voltage. W and L denote the channel width and length of the device, respectively. C_{ox} is the capacitance of the gate insulator and μ is the device mobility. The measured I_{DS} value is generally lower than the value calculated with the preceding equations. This can be attributed to the defects generated in the channel, gate dielectric layer and charge trapping at the channel/gate insulator interface. Figure 2.18 shows the typical transfer characteristics (I_{DS} versus V_{GS}) of a-IGZO TFTs at a drain voltage of 2 V. The off-state current (I_{off}) is defined as the drift current when the transistor is off with a magnitude of less than 10^{-10} A. The on-state current (I_{on}) is normally in the mA range when the V_{GS} value is greater than V_{th} .

Figure 2.18 Typical transfer characteristics of an a-IGZO TFT device.⁶³

The I_{on}/I_{off} ratio is an important parameter for future HD flat panel displays, which will require a small enough leakage current to achieve low standby power consumption and a high enough current to turn on imaging pixels. The I_{on}/I_{off} of a-IGZO TFTs is still not high enough compared with the commercially used a-Si:H TFTs, which have large I_{on}/I_{off} ratios of $> 10^8$. The gate leakage current (I_G) in this case is almost the same as I_{DS} in the off state. It is difficult to improve the I_{off} in an a-IGZO device when its magnitude is limited by I_G . It is also not easy to improve the quality of the dielectric layer due to the relative low TFT device fabrication process temperature.

The performance of a TFT device is commonly evaluated by its field-effect mobility (μ_{FE}). The μ_{FE} can be extracted from the linear regime of transfer characteristic curves using the following equation derived from Eq. (2.1):

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}} \quad \text{Eq. (2.6)}$$

The g_m is the transconductance, which is obtained from the gradient of I_{DS} versus V_{GS} . Here, V_{DS} should be as small as possible to ensure that the TFT is running in the linear regime. Saturation mobility (μ_{sat}) is defined as the carrier mobility of TFT when it is operating in the saturation regime under the condition that V_{DS} is significantly larger than the pinch-off voltage ($V_{DS} \gg V_p$). It can be obtained using the following equation

derived from Eq. (2.2):

$$\mu_{sat}^{\frac{1}{2}} = \frac{2Lg'_m}{WC_{ox}V_{DS}}, g'_m = \frac{\delta\sqrt{I_{ds}}}{\delta V_{GS}} \quad \text{Eq. (2.7)}$$

S.S is another important TFT parameter, and is defined as the minimum gate voltage value required to obtain an increase of one decade of drain current in a transfer characteristic curve. It can be extracted from the sub-threshold region of a transfer characteristic curve at the maximum slope point using the following equation:⁹⁰

$$S.S = \left(\frac{\delta \log I_{DS}}{\delta V_{GS}} \right)^{-1} \quad \text{Eq. (2.8)}$$

It is worth noting that the S.S value reflects the quality of a TFT device quality and is related to the total trap density (N_t), including both the density of the deep bulk states in the channel (N_{bulk}) and the density of defects in the channel/gate dielectric interface (N_{it}), as follows:⁹¹

$$N_t = N_{bulk} + N_{it} = \left[\frac{S \log(e)}{kT / q} - 1 \right] \frac{C_{ox}}{q} \quad \text{Eq. (2.9)}$$

where q is the charge of an electron and k is the Boltzmann constant..

2.5 Reliability and instability of a-IGZO TFTs

The stability of a TFT device is determined by the significant variations in its threshold voltage during long-term normal operation and by the marked degradation in its field effect mobility. The threshold voltage shift (ΔV_{th}) of each driving transistor can lead to variations in respective pixel brightness, as the light intensity of the OLED elements is directly proportional to the drain current density. Thus, the image quality of a display can be affected by the variation in V_{th} .⁹² The voltage stress-induced ΔV_{th} is a critical issue that must be considered in pixel circuit designs for current-driven displays. For example, Figure 2.19 shows one pixel circuit of AMOLED. The ΔV_{th} induced by the driving current at T1 must be evaluated to address any instability.⁹³

Figure 2.19 Integrated circuit of one pixel for the AMOLEDs⁹³

It is necessary to maintain the ΔV_{th} of the AOS TFTs at a relative low value to successfully implement the AOS TFTs into AMLCD and AMOLED displays, and to simultaneously achieve a high μ_{FE} value to ensure reasonable lifetime operation. Recent research efforts in this area have focused on the improvement of long-term stability. For example, studies have established the instability of AOS TFTs that use IGZO thin film as an active layer under gate bias stress conditions. Unlike a ZnO-based TFT, wherein a positive/negative gate bias stress results in a corresponding positive/negative shift in the transfer characteristics, respectively,⁹⁴ a threshold voltage shift in an a-IGZO TFT is only observed under positive voltage gate bias stress conditions. Although a parallel threshold voltage shift can be induced by the positive gate bias stress in a-IGZO TFTs, no significant effect on transfer characteristic curves has been observed under negative gate bias stress conditions.^{95, 96} Figure 2.20 shows the transfer characteristic curve of an a-IGZO TFT before and after applying a 30/-30 V bias to the gate electrode for a duration of 500 s.⁹⁵

Figure 2.20 Transfer characteristics of an a-IGZO TFT before and after applying a gate bias stress at a drain voltage of 1 V. The stress voltage is set at 30/-30 V for a duration of 500 s.⁹⁵

As the figure shows, the transfer characteristic curve positively shifts after a positive bias stress when a sub-threshold swing is applied, and the transfer curve with a negative bias stress overlaps that of the pre-stress curve. The positive ΔV_{th} induced by the positive gate bias is attributed to either electron trapping at the channel/dielectric interface or electron injection into the gate dielectric layer. However, the electrons can be depleted from the channel/dielectric interface when a negative bias is applied to the gate. No holes are induced at the interface, as the IGZO is an n-type metal oxide semiconductor. The time dependence of ΔV_{th} under bias stress conditions can be modeled based on the trapping mechanism using the following stretched-exponential equation:^{97, 98}

$$\Delta V_{th} = V_0 \left\{ 1 - \exp \left[1 - \left(\frac{t}{\tau} \right)^\beta \right] \right\} \quad \text{Eq. (2.10)}$$

where V_0 is the pre-stress V_{th} value, β is the stretched-exponential exponent, t represents the stress time and τ is the trapping time constant of the carriers. Figure 2.21 shows

the time dependence of ΔV_{th} in a-IGZO TFTs under different constant V_{GS} stress levels for a duration of 10^4 s.⁹⁶

Figure 2.21 Time dependence curves with ΔV_{th} in a-IGZO TFTs under different gate bias stress conditions. The inset shows the extracted V_0 under various gate bias stress conditions.⁹⁶

The time dependence curve with ΔV_{th} fits well with Eq. (2.7) at all of the stress conditions, with V_{GS} ranging from 10 to 25 V. The mechanism of the electron trapping probably occurs within the IGZO channel layer due to the strong non-directional ionic chemical bonds in the IGZO bulk, as proposed by Hoshino.⁹⁹

The TFTs in AMLCD are always working under visible light illumination from the backline of the panel. As such, the instability of the device under this illumination is another important issue to be considered for AOS TFT flat panel displays. The sub-threshold current can be induced at the “OFF” state due to excess photo-generated carriers when the TFT is exposed to visible light. The “OFF” pixels do not fully turn off due to this high sub-threshold current. In addition, switching TFTs always experience a negative gate bias for most of their operation time, as the TFTs working in the “OFF” state are 500 times longer than those working in the “ON” state in a commercial AMLCD device.¹⁰⁰ Therefore, device degradation is commonly observed when AOS TFTs are working under light illumination with a negative

gate bias. Some research groups have recently studied the effect of negative bias illumination stress (NBIS) on a-IGZO TFTs. The transfer curves exhibit a large negative V_{th} shift under green light illumination with a negative gate bias stress, as shown in Figure 2.22.¹⁰¹

Figure 2.22 Transfer curves of a-IGZO TFTs as a function of the applied -20 V NBS time (a) in the dark and (b) under green light exposure for 10^4 s.¹⁰¹

There are two plausible explanations for the negative V_{th} shift in a-IGZO TFTs under the NBIS condition. First, electron-hole pairs could be generated in the channel layer under light illumination, and the photo-generated free holes could be attracted to the gate dielectric layer/channel interface and injected into the gate insulator layer under a negative gate bias, as shown in Figure 2.23.¹⁰²⁻¹⁰⁴

Figure 2.23 Schematic band diagram of a hole trapping model in an a-IGZO TFT.¹⁰²

The trapped holes provide a positive bias effect at equilibrium on the n-type IGZO channel, which results in the negative shift in the transfer curve. Although this procedure is considered to be a possible instability mechanism, it explains only the parallel shift in the transfer curve, without accounting for the significant degradation in μ_{FE} and S.S. It does not explain the current conduction variation at the sub-threshold region in the transfer curve.

Due to the limitations of the charge-trapping model, the sub-gap defect states in the channel layer have been considered as another mechanism explaining the NBIS effect. The creation of sub-gap states under light exposure can be detected by capacitance-voltage (C-V) measurements that are commonly attributed to oxygen vacancies (V_o) in the metal oxide semiconductor.¹⁰⁵ Most of the oxygen vacancies (V_o) fully occupy the states near the VBM in a-IGZO.^{106, 107} Figure 2.24 shows the instability caused by the creation of a V_o^{2+} state.¹⁰¹

Figure 2.24 Schematic illustrations of a corresponding instability mechanism for a-IGZO under negative bias illumination stress conditions.¹⁰⁵

V_o can be photo-excited and ionized to V_o^{2+} under a large negative bias condition, as the quasi-Fermi level at the interface surface is lower than the mid-gap level. The gate bias dependence on the negative bias instability under illumination was examined by Himchan Oh^{105,108} and found that the threshold voltage was strongly related with the corresponding instability modes for different gate bias regimes. The holes cannot move rather freely unlike the photon-induced holes under small negative voltage stress, however, If the large negative

bias is applied, substantial portion of the photoexcited V_{O^+} or $V_{O^{2+}}$ states can survive without neutralization by virtue of lowered Fermi-level. The created V_{O^+} or $V_{O^{2+}}$ states can act as positive fixed charges and be attracted to the dielectric/channel interface by a negative gate bias. The photo-generated electrons excited from the V_O state into the conduction band can survive without recombining with the excess holes, as these holes are trapped in the stable $V_{O^{2+}}$ states under the NBIS condition. These electrons are donated as free carriers in an a-IGZO semiconductor. The transfer curves shift to negative due to these positive charges and the increase in electron density.^{105, 108}

2.6 Present applications of displays and circuits based on a-IGZO

2.6.1 Display applications with a-IGZO TFTs

Oxide TFT has been widely used in LCD and OLED displays. Development research into display applications started in 2004 after Nomura successfully demonstrated the first IGZO TFTs. Several prototypes have been presented at the International Meeting on Information Display (IMID) and Society Information Display (SID) since 2005. Toppan Printing Co. Ltd. announced the first display prototype to use AOS TFTs in 2005, which took the form of flexible back-and-white e-paper.¹⁰⁹ LG Electronics (LGE) subsequently began work on AOS TFTs and demonstrated the first AMOLED display in 2006.¹¹⁰ Samsung SDI and the Samsung Advanced Institute of Technology (SAIT) also reported AMOLED displays in 2007.¹¹¹ Until 2008, the display size of AMOLEDs operating at high scanning frequencies (e.g., 240 Hz) with AOS TFTs reached only 12.1 inches.¹¹² Due to the high mobility and good uniformity for large-area deposition, more high-end displays using a-IGZO TFTs have since been demonstrated, such as ultra-high definition LCD TVs and 3DTVs. At TAOS 2010, AU Optronics Corp. presented the largest FPD to use AOS TFTs: a 37-inch AMLCD.⁵¹ Several other companies have also demonstrated flexible or transparent displays. Since

Toppan reported the first AOS TFTs prototype fabricated on the flexible substrate,¹⁰⁹ it has developed and worked out more flexible displays, such as black-and-white e-paper with the world's highest resolution of 400 ppi (Figure 2.25(a))⁴⁶ and a 4-inch electrophoretic display using polyethylene naphthalate (PEN) plastic substrate at a resolution of 320×240 (Figure 2.25(b)).⁴⁷

Figure 2.25 (a) 2-inch VGA flexible black and white e-paper with 400 ppi;⁴⁶ (b) flexible electrophoretic display with PEN substrate;⁴⁷ (c) 6.5-inch flexible full-color top-emission AMOLED panel, bent to a curvature of approximately 2 cm.¹¹³

In 2007, LGE presented the first flexible AMOLED using stainless steel foil as a substrate.⁴⁹ The next year, the company developed a 3.5-inch OLED display on a stainless steel plate with a resolution of 176×220 .¹¹⁴ Samsung Mobile Display Co. Ltd. (SMD) announced a 6.5-inch a-IGZO TFTs AMOLED display prototype fabricated on a polymer substrate. It showed that an a-IGZO TFT-based AMOLED display could withstand significant bending to a curvature of approximately 2 cm without degrading its electrical properties (Figure 2.25(c)).¹¹³ Commercial products that use AOS TFT technology are currently focused on small-sized flexible OLED displays and large-sized high-end AMLCD and AMOLCD. Although the mainstream is focused on researching the development of a low-temperature process and high-performance circuit design with low-cost fabrication, the high transmittance property of AOS will become a new research field in the near future due to its specific important applications. It is believed that transparent electronics will soon become commonplace, as some companies have already demonstrated transparent display prototypes. For example, Samsung SDI demonstrated a 4.1-inch full-color OLED display

driven by a-IGZO TFTs with a transmittance of $\sim 20\%$.¹¹¹ Moreover, AUO presented a 2.4-inch transparent OLED display with a-IGZO TFT touch panel at the SID conference in 2010.¹¹⁵ Transparent displays have attracted a great deal of attention from several display companies. In 2011, Samsung announced the mass production of the first transparent 22-inch LCD panel with a resolution of 1680×1050 and a transparency of 15%.¹¹⁶

2.6.2 Inverters and ring oscillators with a-IGZO TFTs

Inverters and ring oscillators (ROs) are basic components in digital circuit design. A simple inverter circuit consists of two transistors that can output a logic voltage level in opposition to the corresponding input voltage level. Figure 2.26 shows the voltage transfer curve of an inverter that uses two AOS TFTs. When the input voltage (V_i) is high, the transistor Q_1 turns on and current flows through the control transistor Q_1 and pulls the output voltage terminal (V_o) to the ground or “low” level. When the V_i is low, the control transistor Q_1 is off, causing V_o to pull the output to the V_{DD} or “high” level.¹¹⁷

Figure 2.26 Voltage transfer curve of a transparent inverter using AOS TFTs.¹¹⁷

ROs can be used to evaluate the performance of a circuit and thereby define the technology range of a TFT application. ROs typically consist of odd-numbered inverters that are connected together in series. Those based on a-IGZO TFTs perform much better than other channel materials such as organic semiconductors, a-Si:H and other oxide semiconductors. The propagation delay achieved using a-IGZO TFTs fabricated on a glass substrate can reach the 0.24 $\mu\text{s}/\text{stage}$ with an oscillation frequency of 410 kHz.¹¹⁸

Figure 2.27 (a) Schematic diagram of an 11-stage oscillator with two buffer stages, (b) the optical layout image of the circuit, (c) the output characteristic curve of the ring oscillator with a-IGZO TFTs.¹¹⁹

As shown in Figure 2.27, a dynamic circuit implemented with an a-IGZO TFT was recently successfully demonstrated on a flexible plastic substrate.¹¹⁹ The circuit, which has an input voltage of 20 V and contains 11-stage oscillators with two buffers, has a propagation delay of 0.48 $\mu\text{s}/\text{stage}$ at a frequency of 94.8 KHz. This result is only slightly slower than that of the a-IGZO-based ROs on a glass substrate.

Chapter 3 HIGH PERFORMANCE INDIUM GALLIUM ZINC OXIDE THIN FILM TRANSISTORS WITH O₂ PLASMA IMMERSION

3.1 Introduction

Amorphous IGZO is a promising semiconductor material that can be used as the channel layer in transparent TFTs due to its high field effect mobility and feasibility of the room temperature fabrication for the next-generation displays.³⁰ It has been known that the electrical properties including carrier mobility and carrier concentration of IGZO thin films and device behaviors of IGZO TFTs are affected by thin film deposition conditions and or treatment of the thin films.¹²⁰⁻¹²³ In particular, the oxygen content in an IGZO thin film, which can be varied with thin film deposition condition (e.g. with/without O₂ flow during sputtering deposition⁸⁶) and or treatment of the thin film (e.g. argon plasma treatment¹²⁰), can largely affect the electrical properties of the thin film and device performance of the IGZO TFTs.

In this chapter, bottom-gate structure TFTs was fabricated with a-IGZO thin film prepared by RF sputtering. We examined the electrical properties of the fabricated TFTs with SiO₂ and HfO₂ as the dielectric layer, respectively. The a-IGZO TFTs with HfO₂ dielectric exhibited an excellent performance, such as high field-effect mobility, low sub-threshold

wing, high $I_{on/off}$ ratio and low operating voltage. We studied the influence of post-deposition O₂ plasma immersion on the electrical properties and transistor performance of the IGZO thin films synthesized by RF sputtering technique. It is observed that an O₂ plasma immersion can largely enhance the Hall mobility while greatly reduce the electron concentration of the IGZO thin films. The O₂ plasma immersion does not have a significant impact on the threshold voltage of the TFT; however, it leads to a huge reduction in the off current and enhancement in the on/off current ratio, respectively. The XPS analysis indicates that the influence of O₂ plasma immersion on the electrical properties and the device performance can be attributed to the reduction of the oxygen-related defects in the IGZO thin film.

3.2 Experiment and device fabrication

Prior to the a-IGZO TFTs device fabrication, a standard cleaning (SC-1) process and a dip in diluted HF acid were firstly conducted to remove the native oxide and contaminants on heavily-doped n-type Si wafers with resistivity of $\leq 0.001 \text{ } \Omega\text{-cm}$. Two different dielectric materials (SiO₂, HfO₂) were selected as gate insulator for a-IGZO TFTs for comparison. For SiO₂ gate dielectric stack, a 50nm thick SiO₂ thin film was grown on the substrate by thermal dry oxidation at 850°C. For high-k dielectric, a 35 nm HfO₂ thin film was deposited onto the Si wafer at 300 °C with atomic layer deposition (ALD) process using Tetrakis (ethylmethyldamino) hafnium of 99% in purity. A 50nm thick IGZO thin film was deposited on the SiO₂/HfO₂ dielectric layer by RF sputtering using a single IGZO target (In:Ga:Zn mole ratio = 1:1:1) with a fixed RF power at 200W. It is unsuitable to grow Zn-containing amorphous oxide thin film in the co-sputtering method with oxygen gas as the local structural order of IGZO will increase substantially with the introduction of oxygen gas, causing the crystallization or phase separation by the oxygen bombardment effect¹²⁴. As discussed later, oxygen plasma immersion is an alternative way to reduce the resistivity of IGZO thin film

without oxygen involved in the sputtering process. If there is oxygen gas during the sputtering, the IGZO thin film has low resistivity, which makes the improvement by O₂ plasma immersion insignificant. Therefore, the sputtering was carried out in Ar ambient without oxygen. The deposition rate was ~ 5 nm/min. Before open the shutter, 10 mins pre-sputtering was conducted on the target to remove the surface contamination. The active region of the TFTs was defined with photolithography and patterned by wet etch process with diluted sulfuric acid (H₂SO₄). Finally, 10nm Ti with 200 nm Au source and drain electrodes were formed by e-beam evaporation. The basic pressure was maintained at 2×10^{-6} Torr and deposition rate is 1 Å/s. The electrode structures are patterned by lithography and lift-off process.

Figure 3.1 Schematic diagram and fabrication process of the a-IGZO TFTs

The electrical properties were measured with Keithley-4200 semiconductor characterization system. The Hall mobility and electron concentration of the IGZO thin films

were measured with a Hall measurement system at room temperature. A schematic diagram and fabrication process of the a-IGZO TFTs structure is shown in Figure 3.1. The TFTs with various channel widths (W) of 10 – 1000 μm and channel lengths (L) of 10 – 100 μm were fabricated. XPS measurement was performed to analyze the oxygen content change in the IGZO thin films. The XPS PEAK FITTING PROGRAMME of version 4.1 was used to analyze the measured XPS data.¹²⁵

3.3 Electrical characterization of a-IGZO TFTs

Figure 3.2 shows the transfer curves of a-IGZO TFTs before and after O₂ plasma immersion with a drain voltage of 0.1 V. The as-fabricated TFTs exhibited a high current conduction in the milli-ampere range. The device exhibited characteristics that could not be turned off under a negative gate voltage regime. The high conductivity in the channel is attributable to the high electron concentration in the IGZO thin film. The electron concentration of the a-IGZO thin film was controlled by the Ar/O₂ mixing ratio during the RF sputtering process. A high electron carrier concentration and a low resistivity in the channel were obtained when no oxygen gas was involved in the sputtering process.⁸⁶ To address this issue, O₂ plasma immersion of a different duration was conducted on the IGZO thin film after the RF sputtering deposition.

Figure 3.2 Transfer curves of an a-IGZO TFT with and without O₂ plasma immersion.

The TFTs with O₂ plasma immersion performed excellently, with a low I_{off} value, a small S.S value and a high $I_{\text{on}}/I_{\text{off}}$ ratio. The O₂ plasma treatment can be considered a critical process for TFT fabrication when there is no oxygen gas involved during the RF sputtering deposition process. The influence of post-deposition O₂ plasma immersion on the electrical properties and TFT performance of IGZO thin films synthesized using the radio-frequency (RF) sputtering technique is discussed in the next section. The output characteristics of the bottom gate a-IGZO TFTs with SiO₂ and HfO₂ dielectric layers under various V_{GS} in the range of 0 ~ 10 V are shown in Figures 3.3(a) and (b), respectively.

Figure 3.3 (a) Output characteristics of an a-IGZO TFT with $W/L = 20 \mu m / 20 \mu m$ with an SiO_2 gate dielectric. V_{DS} was swept from 0 to +20 V at V_{GS} varied from +2 to +10 V. b) Output characteristics of an a-IGZO TFT with $W/L = 20 \mu m / 20 \mu m$ with an HfO_2 gate dielectric. V_{DS} was swept from 0 to +5 V at V_{GS} varied from +1 to +5 V.

During each measurement, the drain-to-source voltages were swept from 0 to 20 V and 0 to 5 V, respectively. A very clear distinction between the linear and saturation regions was observed. For the SiO_2 dielectric, a minimum drain voltage of 4 V was required to ensure that the TFTs were operating in the saturation region. However, for the HfO_2 dielectric, only 1 V for drain voltage was enough to drive the TFTs, indicating that a-IGZO TFTs with high k dielectric levels can be driven at a relative low voltage (< 1 V). This finding is promising for low-power applications.

Figure 3.4 Transfer characteristics of an IGZO TFT with a) SiO₂ and b) HfO₂ dielectric after O₂ plasma treatment, with W/L= 20 μ m / 20 μ m.

Figure 3.4 shows the transfer characteristics of the TFT with SiO₂ and HfO₂ dielectrics. The field-effect mobility was extracted at a low drain voltage ($V_{DS} = 0.1$ V) using Eq. (2.3). The dielectric constant of HfO₂ synthesized by ALD at 300°C was ~ 20 , as previously reported.¹²⁶ Both W and L were 20 μ m. Figure 3.4 also shows the square root of the drain current versus the gate voltage, which was used to obtain the saturation mobility according to Eq. (2.4). The S.S was extracted at the maximum slope point of $V_{GS} = 0$ V from the sub-threshold region using Eq. (2.5). For the HfO₂ a-IGZO TFT, the calculated S.S of a-IGZO TFT with HfO₂ was about 250 mV/decade. This value was compatible or even superior

to that of the a-Si:H-based TFT. The TFT with low S.S values gave rapid responses. The off-state current reached as low as 10^{-12} A. There was an increase in I_{off} when a larger negative V_{GS} was applied (i.e., -2 ~ -5 V), which can be attributed to capacitance loading during measurement or the lack of confinement of the channel current. It is expected that the I_{off} (and on/off current ratio) could have been further improved by incorporating an active island in each individual transistor. The device performance results for the a-IGZO TFTs examined in this study are shown in Table 3.1.

	μ_{FE} (cm ² /Vs)	μ_{sat} (cm ² /Vs)	S.S (V/dec)	$I_{\text{on}}/I_{\text{off}}$
IGZO with SiO ₂	24.6	24.4	0.7	10^7
IGZO with HfO ₂	26.8	25.5	0.25	10^8
Ref. 1 ³⁰	10	-	0.24	10^5
Ref. 2 ¹²⁷	9.51	8.3	0.42	10^8
Ref. 3 ¹²⁸	5.01	-	2	10^5

Table 3.1 Comparison of the device performance parameters, including the field effect mobility, saturation mobility, sub-threshold swing and $I_{\text{on}}/I_{\text{off}}$ ratio.

Table 3.1 compares the overall performance of the devices examined in this study and the IGZO TFTs examined by another research group. The a-IGZO TFTs synthesized by RF sputtering in Ar ambient air followed by O₂ plasma treatment exhibited a higher field-effect and saturation mobility. The field-effect and saturation mobility obtained were almost comparable, implying that the field-effect mobility was independent of the drain voltage. Meanwhile, the device exhibited excellent characteristics, including a low S.S value, an extremely high $I_{\text{on}}/I_{\text{off}}$ ratio and a low threshold voltage. The overall performance of a-IGZO

TFTs in this study was remarkable compared with those examined by other researchers. The findings are very promising for future flat panel display applications.

3.4 Effect of N₂ annealing on the electrical performance for a-IGZO TFTs

As identified earlier, wide band and transparent AOS TFTs with a high mobility and a low process temperature are highly attractive for replacing a-Si:H TFT as the switch devices in next-generation FPDs. The application of transparent TFTs not only improves the electrical characteristics of a panel, but also increases its transparency. Furthermore, the low operating voltage helps to save power. Among the many candidate materials for the TFT channel layer, IGZO is especially appealing due to its superior mobility performance. This section focuses on enhancing the performance of a-IGZO TFTs with post-deposition thermal annealing. Oxygen is located within both the bulk IGZO layer and surrounding environment, and can affect both channel resistivity and other aspects of electrical performance. In addition, because oxygen may make the device unstable under the voltage stress condition,¹²⁹ N₂ gas was used as the ambient gas to examine the effect of thermal annealing on a-IGZO TFTs. When the film was annealed at above 500 °C, diffraction peaks attributable to InGaZnO₄ crystal appeared, indicating that crystallization had begun.¹³⁰ Therefore, the annealing temperature was set at 300°C.

Figure 3.5 (a) Transfer characteristics and (b) leakage current of IGZO TFTs before and after annealing in N₂ ambient at 300°C for 1 h.

Prior to the post-annealing process was performed in the nitrogen atmosphere of a furnace tube at 300°C for 1 h, the oxygen plasma immersion was conducted on the IGZO thin film surface for 75 s. The electrical characteristics of the devices were measured with a semiconductor parameter analyzer (Keithley 4200). Figure 3.5(a) shows the effect of annealing on the transfer characteristics of the devices. It indicates that the annealing did not

have a significant effect on the V_{th} level, which was maintained at ~ 1.0 V. The concentration of the oxygen vacancies did not increase at an annealing temperature of 300°C. Comparing the transfer characteristics before and after the post-annealing process, the S.S level improved suddenly from 250 to 160 mV/decade. Although thermal annealing did not affect the on-state current, the off-state current decreased by about one order of magnitude. This can be attributed to the decrease in the leakage current from the gate electrode to the channel as shown in Figure 3.5(b). Since The IGZO thin film is prepared by RF sputtering process, the overall improvement in the performance may be a result of the strengthened atomic bonding (reduction in the loosely bound oxygen content).¹³¹ However, the actual mechanism behind the formation of the trap states is still not clear and requires further investigation.

3.5 Operation temperature dependence of a-IGZO TFTs

Some issues related to the material and device physics of a-IGZO TFTs are not yet fully understood. In contrast to a-Si:H, the most distinctive characteristic of a-IGZO is its carrier generation mechanism. The dominant carrier transport mechanism in a-IGZO is mainly attributed to the point defects in the bulk system. The density of the point defects in a-IGZO, which significantly affects its electrical conductivity, is primarily determined by the method and condition of the thin film deposition. Ambient temperature is responsible for the generation of point defects, which have a considerable effect on not only a-IGZO conductivity, but also IGZO TFT characteristics. Therefore, it is important to examine the sensitivity of a-IGZO TFT characteristics to the ambient temperature that affects the density of the point defects in the IGZO channel.

Figure 3.6 Transfer characteristics at different temperatures for an inverted-staggered bottom-gate IGZO TFT.

Measurements were taken using the Keithley 4200 semiconductor characterization analyzer's cryogenic probing system to evaluate the temperature dependence of the a-IGZO TFT electrical components. Figure 3.6 shows the evolution of the transfer characteristics as a function of the operation temperature from +77 to +500 K. The gate voltages were swept from -5 to 5 V at a fixed drain voltage of 0.1 V. V_{th} was extracted from the transfer curves.

The S.S value at or less than room temperature was much smaller than that at 500 K, suggesting that the interfacial trap density at a low temperature was much smaller than that at a high temperature. The physical implication of the change in interfacial trap density is discussed with the respective temperature-dependent V_{th} instability findings. V_{th} negatively shifted by approximately 1.8 V as the temperature of the device increased from 77 to 500 K. This negative ΔV_{th} result can be explained as follows. The sub-threshold current in TFTs is related to the thermal activation energy involved. Thermally activated electrons can be injected into the conduction band from the deep-level traps with the lateral electrical field at high temperatures. The increase in state density at the interface can create a large number of

extra localized states in the band gap as a result.^{132, 133} It is well known that the amount of free electrons in the oxide semiconductor materials is mainly determined by the generation of oxygen vacancies. Oxygen vacancies can be induced when thermally excited oxygen atoms jump out of their original sites and move into interstitial sites, leaving behind two free electrons. The negative shift in V_{th} with the increasing operation temperature can be attributed to the increase in these free electrons. The generation of point defects increases the internal energy and simultaneously the entropy of the system, minimizing the amount of free energy.^{129, 134} In addition, the off-state current increases along with the operation temperature. Point defects (oxygen vacancies) can be generated in the high k dielectric layer at a high temperature, resulting in a larger percolation path. Electrons can be easily tunneled through the dielectric layer, causing great amount of leakage current. In this case, the off-state current was limited by the leakage current. When the operation temperature was larger than 400 K, the device was almost not functional due to the large leakage current, indicating that the maximum operation temperature for a-IGZO TFTs should be less than 400 K.

In addition to the negative shift of the transfer curve with increasing temperature, there was a noticeable change in the drain current, which can be attributed to the temperature dependence of the mobility, as shown in Figure 3.7. The field-effect mobility of a-IGZO TFTs was found to increase as the operation temperature increased, probably due to trapping enhancement at lower temperatures.

Figure 3.7 Field effect of mobility versus operation temperature.

In conclusion, the transfer curves of a-IGZO TFTs were observed to shift almost rigidly to lower (more negative) gate voltages as the operation temperature increased. The extent of this shift appeared to increase with as the trap density increased. In addition, a significant decrease in channel mobility occurred when the operation temperature fell below 200 K.

3.6 Effect of O₂ plasma immersion on electrical properties and transistor performance of indium Gallium Zinc Oxide Thin Films

In this section, we have conducted a study on the influence of post-deposition O₂ plasma immersion on the electrical properties and TFT performance of the IGZO thin films synthesized with RF sputtering technique. It is observed that an O₂ plasma immersion can largely enhance the Hall mobility while greatly reduce the electron concentration of the IGZO thin films. The O₂ plasma immersion does not have a significant impact on the

threshold voltage of the TFT; however, it leads to a huge reduction in the off current and enhancement in the on/off current ratio, respectively. The XPS analysis indicates that the influence of O₂ plasma immersion on the electrical properties and the device performance can be attributed to the reduction of the oxygen-related defects in the IGZO thin films caused by O₂ plasma immersion.

The a-IGZO TFTs were fabricated as described in chapter 3.2. After deposition of a-IGZO thin film by RF sputtering process. The deposited IGZO thin films were subjected to an O₂ plasma immersion for different durations. The electrical properties including the Hall mobility and electron concentration of the IGZO thin films were measured with a Hall measurement system at room temperature. XPS measurement is carried out by using Kratos AXIS spectrometer with monochromatic Al K α (1486.71 eV) X-ray radiation to analyze the oxygen content change in the IGZO thin films due to the O₂ plasma immersion. Figure 3.8 shows the schematic structure diagram of the fabricated TFT.

Figure 3.8 Schematic diagram of the TFT structure

Figure 3.9 shows the Hall mobility (μ), and electron concentration (n) of the IGZO thin films obtained from the Hall measurement as a function of the O₂ plasma immersion time. The resistivity (ρ) of the IGZO thin films can be calculated with $\rho = 1/q\mu n$, where q is the electron charge, and the result is shown in Figure 3.9(c).

Figure 3.9 Hall mobility, electron concentration and resistivity of the IGZO thin films as a function of O₂ plasma immersion time.

The as-deposited IGZO thin film without any O₂ plasma immersion had a very low resistivity ($5.6 \times 10^{-3} \Omega\cdot\text{cm}$) due to the absence of oxygen gas during the RF sputtering deposition. However, as can be observed in Figure 3.9(c), the resistivity of the IGZO thin films can be largely increased by an O₂ plasma immersion. For example, the O₂ plasma immersion for 75 s causes the resistivity increase to $1.9 \times 10^{-1} \Omega\cdot\text{cm}$. The increase in the resistivity is actually due to the large decrease in the electron concentration in the IGZO thin films. As shown in Figure 3.9(b), the electron concentration decreases from $1.3 \times 10^{21} \text{ cm}^{-3}$ to

$2.2 \times 10^{18} \text{ cm}^{-3}$ after the O₂ plasma immersion for 75 s. On the other hand, O₂ plasma immersion can significantly enhance the Hall mobility. The Hall mobility increases from 0.84 cm²/Vs to 14.4 cm²/Vs after the O₂ plasma immersion for 60 s; however, a prolonged immersion does not lead to a significant increase in the Hall mobility. The metal oxides such as ZnO and IGZO are typical n-type semiconductors with electron concentration at the order of 10^{21} cm^{-3} ; the electrons in the conduction band of the oxide semiconductors are originated from the interstitial metal ions and oxygen vacancies which both can act as donors in the oxide semiconductor.¹³⁵ It has been reported that the electrical properties of IGZO thin film are strongly affected by the oxygen content in the thin films.^{75, 129, 136} Therefore, it is expected that the effect of the O₂ plasma immersion on the electrical properties observed in this work is due to the change in the oxygen content in the IGZO thin films caused by the O₂ plasma immersion.

To confirm this, we have conducted an XPS measurement on the IGZO films with and without O₂ plasma immersion. Figure 3.10(a) shows the XPS spectra of O 1s core level before and after plasma immersion for 5 min. As can be observed in the figure, the O₂ plasma immersion leads to a large change in the O 1s spectrum. In the metal oxide system, typically the O 1s peak comprises of three Gaussian profiles centered at 530.1 eV, 531.4 eV, and 532.4 eV represented by low binding energy (O_L), medium binding energy (O_M) and high binding energy (O_H), respectively.^{69, 137}

Figure 3.10 (a) O 1s core level XPS peak of IGZO thin films before and after the O₂ plasma immersion for 5 min; (b) de-convolution of the XPS peak into the three Gaussian profiles denoted as O_L, O_M and O_H for the IGZO thin film before the O₂ plasma immersion; and (c) de-convolution of the XPS peak for the IGZO thin film after the O₂ plasma immersion.

The O_L component is attributed to the O²⁻ ions binding with Ga, In and Zn ions. The O_M component is related to the deficiently bonded oxygen in the IGZO material which contains the non-stoichiometric oxide species such as In₂O_{3-x}, ZnO_{1-x}, Ga₂O_{3-x}.^{121, 138} The O_H peak represents the chemisorbed oxygen presented on the film surface and the grain boundaries of the a-IGZO film.¹³⁹ Figure 3.10(b) and Figure 3.10(c) show the three Gaussian profiles before and after the O₂ plasma immersion, respectively. Based on the comparison

between Figure 3.10(b) and Figure 3.10(c), it can be observed that O_L and O_M decrease while O_H increases after the O₂ plasma immersion. The atomic ratio of O_L/O_M increases from 1.7 before the immersion to 2.3 after the immersion, indicating that there is less deficiently bonded oxygen in the IGZO matrix after the O₂ plasma immersion. As a result, the electron concentration decreases due to the reduction of the oxygen-related defects which act as donors in the n-like IGZO semiconductor. The reduction of the defects which act as carrier scattering centers also enhances the carrier mobility. On the other hand, the large amount of the chemisorbed oxygen on the film surface and at the grain boundaries produced by O₂ plasma immersion may also play a significant role. The adsorption behavior of oxygen on IGZO surface during the plasma immersion is known to be quite complex,¹³⁹ and the detail is not known yet. Another possible mechanism which is the argon bombardment effect may be involved in the RF sputtering and O₂ plasma immersion process due to the crystallization or phase separation.^{124, 140} However, the degrees of structural order increase with oxygen content were only observed in co-sputtered film, while single-target-sputtered IGZO did not. In this study, the IGZO thin film was sputtered with single IGZO target and no oxygen was introduced in the sputtering process. Even though O₂ is mixed during the RF magnetron sputtering, the amorphous structure of IGZO film is also stable up to 773K in air proved by some researcher.¹³⁴ We believe that the oxygen bombardment effect is insignificant in our a-IGZO thin film. The IGZO thin film properties with O₂ plasma immersion should be driven by oxygen stoichiometry change rather than oxygen bombardment (i.e. crystallization or phase separation).

The electrical characteristics of the TFTs after an O₂ plasma immersion with various durations have been measured. Note that the transistor characteristics of the TFT without any O₂ plasma immersion could not be measured because the TFT channel could not be turned off and the TFT exhibits no field effect due to the very low resistivity in the IGZO channel layer.

Figure 3.11(a) and 3.11(b) show the output and transfer characteristics of the TFTs, respectively, after the O₂ plasma immersion of 45 and 135 s.

Figure 3.11 Output and transfer characteristics of the TFTs ($W/L = 20 \mu m/20 \mu m$) with the IGZO layer after the O₂ plasma immersion for 45 s or 135 s. The output characteristics are measured at the gate voltage $V_G = 7$ V, and the transfer characteristics are measured at the drain voltage $V_D = 0.1$ V.

Clear transistor behaviors can be observed after the O₂ plasma immersion of 45 s. Much better transistor performance is obtained after the O₂ plasma immersion of 135 s, e.g. the off current is much lower. The linear field-effect mobilities extracted at a low drain voltage ($V_{DS} = 0.1$ V)⁷⁷ are 8.7 and 12.6 cm²/Vs for the immersion of 45 and 135 s, respectively. The enhancement of the field-effect mobility indicates that the O₂ plasma

immersion can effectively reduce the oxygen-related defects which act as the scattering centers in the channel layer.

Figure 3.12 shows the evolution of the electrical characteristics of the TFTs with W/L = 20 μm /20 μm with O₂ plasma immersion time. As shown in Figure 3.12(a), an O₂ plasma immersion does not have a significant effect on the threshold voltage, and the threshold voltage maintains at ~ 5.5 V. This indicates that the O₂ plasma immersion does not cause a significant change in the work function of the IGZO layer or produce a large amount of charge trappings. The saturation almost remains unchanged after the O₂ plasma immersion (larger than 45 s) as shown in Figure 3.12(b), but compared to the as-fabricated TFT without O₂ immersion, the saturation current with O₂ immersion is much lower. The reduction of I_{sat} after O₂ immersion is attributed to the decrease of the electron concentration in the IGZO channel layer. By increasing the O₂ plasma immersion time, the sub-threshold current decreases drastically. As compared to the situation without O₂ plasma immersion, the immersion for 135 s causes the reduction in the off current by a factor of 3.6×10^8 [Figure 3.12(c)] and enhancement in the on/off current ratio by a factor of 1.4×10^7 [Figure 3.12(d)].

Figure 3.12 Evolution of the device performance of the TFTs with O₂ plasma immersion time: (a) threshold voltage (V_{th}); (b) saturation current (I_{sat}) measured at $V_G = 10$ V and $V_D = 2$ V; (c) off current measured at $V_G = 0$ V and $V_D = 1$ V; (d) on/off current ratio (The on current is measured at $V_G = 10$ V and $V_D = 1$ V while the off current is measured under the same condition as in (c)); and (e) the sub-threshold swing (S.S).

In the earlier discussion, the electron concentration in the channel decreases more than two orders of magnitude after O₂ plasma immersion, the conduction path at dielectric/channel interface can be depleted easier. The leakage current is also related to the point defect states in the IGZO channel. Thus, the drastic reduction in the off current could be attributed to the decreases of both the electron concentration and the defect states that participate in the current transport (electron hopping from one defect state to another

contributes to the current conduction). On the other hand, O₂ plasma immersion also leads to a large decrease of the sub-threshold swing (S.S), e.g., the S.S is ~ 1.5 V/decade for the immersion of 45 s, but it decreases to 0.46 V/decade for the immersion of 135 s as shown in Figure 3.12(e). Obviously, a huge reduction in the off current together with a mild decrease in the on current would show a large decrease in the S.S. The reduction of the traps near or at the IGZO/HfO₂ interface caused by the O₂ plasma immersion could be a factor for the decrease of the S.S also.

In conclusion, O₂ plasma immersion greatly affects the electrical properties of the IGZO thin films and the electrical characteristics of the TFTs. As compared to the situation without O₂ plasma immersion, the Hall mobility increases by 17 times while the electron concentration decreases by over 600 times after the immersion of 75 s; and the immersion of 135 s causes the reduction in the transistor's off current by a factor of 3.6×10^8 and enhancement in the on/off ratio by a factor of 1.4×10^7 . O₂ plasma immersion also significantly enhances the field-effect mobility and reduces the sub-threshold swing, while it does not produce a significant impact on the threshold voltage. XPS analysis indicates that the effect of O₂ plasma immersion on the electrical properties and the transistor performance can be attributed to the reduction of the oxygen-related defects in the thin films.

Chapter 4 EFFECT OF EXPOSURE TO ULTRAVIOLET-ACTIVATED OXYGEN ON AMORPHOUS INDIUM GALLIUM ZINC OXIDE THIN FILM TRANSISTORS

4.1 Introduction

Transparent oxide semiconductors have attracted much attention for the application of flat-panel displays due to their high carrier mobility ($> 1 \text{ cm}^2/\text{Vs}$) and high transparency in visible range.^{31, 36, 141} Amorphous indium gallium zinc is one of the most attractive TOS that can be used in the next generation AMLCD due to its few superior properties including relatively high mobility, good uniformity, low temperature process, high optical transparency, high threshold voltage stability, etc. It has been recently reported that the threshold voltage of a-IGZO TFTs is affected by the process parameters such as target composition, deposition pressure, post annealing temperature and channel thickness.^{142, 143} The oxygen content and the thickness of the a-IGZO channel layer are also reported to play an important role in the electrical characteristics including the V_{th} of the TFTs.^{123, 144} The V_{th} is determined by the electron concentration in the active layer of the TFT, thus it is related to the oxygen vacancies which provide the free charge carriers for electrical conduction in the oxide layer. Controlling the V_{th} is required in the TFT application; however, it is not an easy task as the oxygen vacancies can be easily generated during the fabrication processes.

In this chapter, we have demonstrated that the V_{th} can be easily changed by exposing the back channel of the IGZO TFT to ultraviolet-activated oxygen. The V_{th} of the TFT is observed to be highly sensitive to the UV-activated oxygen, and a linear relationship between the ΔV_{th} and the duration of exposure is observed. However, the exposure does not have a large impact on other TFT parameters including the sub-threshold swing and field-effect mobility.

4.2 Device fabrication and experiment

The IGZO TFTs fabrication were started on a heavily-doped n-type Si wafer with resistivity lower than $0.001 \Omega\cdot\text{cm}$, which served as the bottom gate of the TFTs. Firstly, a 30 nm Al_2O_3 layer was deposited onto the Si substrate by an atomic layer deposition (ALD) process to form the gate insulator. The study reported on the influence of the IGZO film thickness on IGZO TFTs that 50-nm thickness is an optimal thickness for the best performance.¹⁴⁴ A 50 nm IGZO thin film was subsequently deposited on the Al_2O_3 thin film layer by RF sputtering at room temperature using a IGZO target (In:Ga:Zn mole ratio = 1:1:1). The IGZO thin film was then subject to the exposure to UV-activated oxygen for different durations at room temperature. Photolithography process followed by wet etching was used to pattern the active region. Finally, 200 nm thick Al source and drain electrodes were formed by electron-beam evaporation and patterned through the standard lift-off processes to form the TFT structures. The channel length (L) and channel width (W) of the a-IGZO TFTs were 20 μm and 20 μm , respectively. The device structure of the bottom-gate TFTs device structure and the experimental setup for the UV-activated oxygen treatment are shown in Figure 4.1.

Figure 4.1 Schematic of the bottom-gated TFT structure and experimental set-up for exposure to UV-activated oxygen.

An UV lamp with the light wavelength of 254 nm was used as the UV excitation source. As shown in the figure, exposure of the surface of the IGZO layer to UV-activated oxygen was carried out inside the chamber, where highly reactive oxygen was generated when the UV light interacted with the oxygen gas introduced into the chamber at room temperature.¹⁴⁵ The resistivity and carrier concentration of the IGZO thin films with different exposure durations were measured with the four-point probe technique and the Hall-effect measurement, respectively, before the formation of the source and drain of the TFTs. Current-voltage characteristics of the TFTs were measured with a Keithley 4200 semiconductor characterization system. All the measurements were conducted at room temperature.

4.3 Result and discussion

To compare the effect of UV exposure in oxygen ambient with that in atmosphere, the UV exposure was carried out in a nitrogen atmosphere also. No significant difference between the oxygen and nitrogen ambient in the effect on the resistivity, electron

concentration and mobility was observed. Figure 4.2(a) shows the resistivity of the IGZO thin film as a function of the duration of exposure to the UV-activated oxygen. The as-deposited IGZO thin film had a relatively high resistivity of $8.0 \Omega\cdot\text{cm}$. After the exposure of 60 s, the resistivity dramatically decreased to $2.0 \Omega\cdot\text{cm}$. The resistivity further decreased to $1.0 \Omega\cdot\text{cm}$ with the 180 s exposure, and became saturated for longer exposures. The experiment was repeated with the IGZO thin films with the thicknesses of 30 and 70 nm, and no significant difference was observed.

Figure 4.2 Influence of exposure to UV-activated oxygen on the electrical properties of the IGZO thin film: (a) resistivity; (b) carrier concentration; and (c) electron mobility of the IGZO films.

On the other hand, as shown in Figure 4.2(b), the electron concentration of the IGZO thin film increased with the exposure time. However, the electron mobility of the a-IGZO thin film, which was calculated with $\mu = I/qn\rho$ where q is the electron charge, n is the electron concentration and ρ is the resistivity, remained at $\sim 10 \text{ cm}^2/\text{Vs}$ as shown in Figure 4.2(c). This indicates that the electron mobility was not significantly affected by the exposure.

XPS measurement was performed on the IGZO films before and after the exposure of 5 min. It should be pointed out that XPS is surface-sensitive but the electrical measurements are related to the bulk properties of the IGZO thin films. In addition, the top surface of the TFT channel layer was exposed to the UV-activated oxygen, although the oxygen could diffuse into the channel region through the 50 nm IGZO layer. Nevertheless, the XPS study can provide us some useful information about the effect of the exposure on the IGZO thin films. Figure 4.3(a) shows the XPS spectra of O 1s core level of the IGZO thin film before and after the exposure.

Figure 4.3 (a) O 1s core level XPS peaks of IGZO films without and with the exposure of 5 mins to UV-activated oxygen; (b) de-convolution of the XPS peak of the IGZO film without the exposure into the three Gaussian profiles denoted as O_L , O_M and O_H , respectively; and (c) de-convolution of the XPS peak of the IGZO film with the exposure.

As discussed before, the O 1s spectrum of IGZO film can be usually deconvoluted into three Gaussian peaks denoted as the low binding energy peak, medium binding energy peak and high binding energy peak. O_L (530.1eV) is from the lattice oxygen atoms in a fully-coordinated environment with the metal ions; O_M (531.1eV) is attributed to the oxygen deficient regions of the metal oxide; and O_H (532.3eV) is due to the adsorbed O_2 , H_2O or M-OH species on the film surface.^{58, 69, 137, 138} The deconvolutions of the XPS spectra of the

IGZO thin film before and after the exposure are shown in Figure 4.3(b) and 4.3(c), respectively. The exposure resulted in a large increase in the O_M signal but a drastic decrease in the O_H signal. The atomic ratio of O_M / O_L increased from 0.39 before the exposure to 1.46 after the exposure, indicating that the exposure generated a lot of oxygen vacancies in the IGZO layer. Although the actual mechanism for the situation is not clear yet, a plausible explanation is given in the following. UV light interacts with oxygen gas to produce oxygen radicals and ozone. The UV-activated oxygen is very reactive. It could remove the oxygen species absorbed on the surface, leading to the decrease in the O_H signal. It could also react with the IGZO layer forming deficient metal oxides. Thus increase in the O_M signal was observed after the exposure. There were more oxygen vacancies in the IGZO layer after the exposure as a result of the formation of deficient metal oxide. On the other hand, the UV light itself could generate oxygen vacancies or other defects in the IGZO layer also. Since the oxygen vacancies are considered as a donor in the IGZO material, the electron concentration increases due to the creation of oxygen vacancies as a result of exposure to the UV-activated oxygen.

Figure 4.4(a) and 4.4(b) shows the influence of the exposure to UV-activated oxygen on the transfer characteristics and output characteristics of the TFTs, respectively.

Figure 4.4 Transfer (a) and output (b) characteristics of the IGZO TFTs ($W/L = 20\mu\text{m}/20\mu\text{m}$) for various durations of exposure to the UV-activated oxygen. The transfer characteristics were measured at the drain voltage of 0.1 V. The inset in (a) shows the corresponding transfer characteristics in linear scale of the drain current.

As can be observed in Figure 4.4(a), the exposure led to a reduction in the off-state current at large negative gate biases. The phenomenon is not fully understood yet. One plausible explanation is as follows. The off current at large negative gate biases is related to the interfacial defect states at the IGZO/ Al_2O_3 interface, while the on-state current is due to the free electrons in the IGZO channel layer. With the exposure, oxygen vacancies are generated in the channel layer, leading to an increase in the electron concentration in the

channel layer; however, the activated oxygen could also passivate the interfacial defect states,^{146, 147} causing a reduction in the off current. Figure 4.4(a) also shows that an exposure led to a shift of transfer curve to the negative-gate voltage indicating the decrease in V_{th} . As shown in Figure 4.4(b), an exposure caused a large increase in the saturated drain current, which was due to the decrease in V_{th} .

The V_{th} values obtained from the transfer characteristics of Figure 4.4(a) are shown in Figure 4.5(a). As can be observed in Figure 4.5(a), V_{th} decreased linearly with the exposure time. As discussed early, the post-deposition treatment could create oxygen vacancies in the IGZO layer, leading to a higher concentration of free electrons in the channel. As pointed out by E. N. Cho, et al.,¹⁴⁸ a higher concentration of free electrons in the channel layer leads to a lower threshold voltage. This is because the IGZO TFTs have an n-type conduction channel. With more free electrons in the channel layer, the TFTs can be turned on at a lower gate voltage. Therefore, the decrease in V_{th} with the duration of exposure to UV-activated oxygen can be attributed to the increase of the concentration of free electrons in the IGZO channel layers. The effect of exposure to UV-activated oxygen on V_{th} provides a simple way to control the threshold voltage of IGZO TFT, and the operation mode of the TFT can be changed from the enhancement mode to the depletion mode by a sufficiently long exposure (e.g. longer than 90 s in this work).

Figure 4.5 Influence of exposure to UV-activated oxygen on the device parameters of the IGZO TFT: (a) threshold voltage; (b) field-effect mobility; (c) sub-threshold swing; and (d) on-state current measured at $V_D = 3$ V and $V_G = 3$ V.

The field-effect mobility of the TFTs has been obtained with the following formula¹²⁰ at the small drain voltage of 0.1 V,

$$\mu = \frac{Lg_m}{WC_iV_D}$$

where C_i and g_m are the gate capacitance per unit area and maximum transconductance, respectively. Figure 4.5(b) shows μ as a function of exposure time. μ was $11.7 \text{ cm}^2/\text{Vs}$ before the exposure, and then it slightly increased to $12.1 \text{ cm}^2/\text{Vs}$ after the exposure of 30 s and

basically remained unchanged for further exposures. Figure 4.5(c) shows the effect of exposure on the S.S of the TFTs which was extracted from the transfer characteristics with the formula $S.S = \delta V_G / \delta \log(I_D)$.¹²⁷ The S.S slightly decreased after the exposure of 30 s but remained unchanged for further exposures. The improvement in the field-effect mobility and the S.S. by the exposure of 30 s could be explained by the passivation of the defects at the interface of Al₂O₃/IGZO by the UV-activated oxygen diffusing through the IGZO layer to the interface. However, as the interface of the gate insulator/channel was not directly exposed to the UV-activated oxygen, such effect is not very significant. On the other hand, as shown in Figure 4.5(d), the on-state current greatly increased with the exposure time, which was due to the decrease of the V_{th} .

4.4 Conclusion

In summary, the effect of exposure to UV-activated oxygen on both the electrical properties of the IGZO thin film and the electrical characteristics of the IGZO TFTs has been investigated. The exposure can effectively shift the threshold voltage of the TFT to a lower value, and a linear relationship between the V_{th} shift and the exposure duration is observed. The decrease in the V_{th} is found to be due to the increase in the electron concentration in the IGZO channel layer. On the other hand, the on-state current significantly increases with the exposure, which is due to the decrease in the V_{th} . Other device parameters including the field-effect mobility and sub-threshold swing are not significantly affected by the exposure. The study shows that exposure to UV-activated oxygen is a simple way to control the V_{th} , and the TFT can be easily changed from the enhancement mode to the depletion mode with this technique.

Chapter 5 ELECTRICAL INSTABILITIES IN AMORPHOUS INDIUM GALLIUM ZINC OXIDE THIN FILM TRANSISTOR UNDER ULTRAVIOLET ILLUMINATION AND ITS APPLICATION

5.1 Introduction

Thin film transistor based on a-IGZO is promising in the application of next generation FPD due to its high field-effect mobility, low thermal budget and good stability.^{30, 45, 149} In the display application, device instability induced by both light illumination and gate bias could be a serious issue.^{99, 150} On the other hand, ultraviolet light is commonly used in the cleaning to remove the particles and impurities on the surface in the TFT fabrication.¹⁵¹ It has been reported that an UV exposure can cause a shift in the threshold voltage of IGZO TFT,^{152, 153} which poses a problem to normal device operation. In this work, we demonstrate that an instant recovery can be achieved by the application of positive gate pulses. The mechanisms of the UV-induced instability and the recovery have been investigated in this work.

5.2 Device fabrication

The fabrication process of the TFT devices started on a heavily-doped n-type Si wafer with a resistivity of less than $0.001 \Omega\text{-cm}$ which served as the gate electrode. A 30 nm Al_2O_3 gate insulator was firstly deposited with ALD process at 250°C using Trimethylaluminium (TMA) of 99% in purity. Subsequently, a 50 nm thick IGZO film was sputtered onto the Al_2O_3 thin film via radio frequency (RF) sputtering. The IGZO target is 2 inches in diameter and 3 mm thick, with mole ratio of $\text{In} : \text{Ga} : \text{Zn} : \text{O} = 1 : 1 : 1 : 4$. The sputtering was carried out in the argon/oxygen ambient with RF power of 100 W during sputtering. The chamber pressure was maintained at 3 mTorr. The pattern of a-IGZO channel was delineated through standard photolithography followed by the wet etching process. Finally, Ti/Au (10 nm/200 nm) pad were deposited by electron-beam evaporation to form the source and drain electrodes. The channel length and channel width were $20 \mu\text{m}$ and $20 \mu\text{m}$ respectively. A schematic cross-section diagram of the TFT is shown in the inset of Figure 5.1. I-V characteristics of the TFTs were measured with a Keithley 4200 semiconductor characterization system at room temperature. A HAMAMATSU LC8 365 nm UV spot light source with power density of $5 \text{ mW}/\text{cm}^2$ was used in the UV exposure experiments.

5.3 Effect of UV-induced instability in a-IGZO TFTs

To examine the stress effect of the gate bias (V_G) on the TFT, + 10 V and - 10 V were applied to the gate of the device respectively for 5 minutes without any exposure to UV illumination, with the source and drain maintained at zero bias. The transfer characteristics of the TFT before and after the applications of the positive and negative biases are shown in Figure 5.1. As can be observed in the figure, the gate bias did not produce a significant change in the transfer characteristic of the TFT, indicating that trap generation and or charge

trapping in the TFT due to the gate bias stress were negligible. Therefore, the gate stress effect can be ignored for the UV-exposure study discussed below.

Figure 5.1 Transfer characteristics of the TFT measured at the source-drain voltage of 0.1 V before and after constant gate bias stresses at +10 V and -10 V, respectively for a duration of 5 minutes. The inset shows the schematic cross-sectional diagram of the bottom gate IGZO TFTs with Al_2O_3 gate dielectric.

The experiment of UV exposure with various durations was conducted on an as-fabricated TFT. The gate electrode was float during the exposure. The transfer characteristic of the TFT was measured in dark after each UV exposure. Figure 5.2(a) shows the transfer characteristics of the TFT before UV exposure and after the exposures of 3, 10 and 60 s. As shown in the figure, an UV exposure led to a shift in the transfer characteristic to the negative voltage side, showing a decrease in the threshold voltage of the TFT. Figure 5.2(b) shows the threshold voltage shift as a function of the exposure duration. As can be observed in the figure, an exposure led to a decrease in the threshold voltage, with a fast decrease rate for short exposure durations ($< \sim 10$ s) and a slow decrease rate for longer durations ($> \sim 10$ s).

Figure 5.2 (a) Transfer characteristics of the fresh device and after the UV exposures of 3 s, 10 s and 60 s. (b) Threshold voltage shift as function of UV exposure time.

This negative shift in the threshold voltage could be attributed to two mechanisms: (1) the increase in the free electron concentration in the channel; (2) the positive charge trapping at the channel/dielectric interface or in the dielectric layer. In the first mechanism, the concentration of free electrons in the channel layer is increased as a result of the creation of oxygen vacancies, which act as donors providing free electrons in the channel layer, during UV illumination. The threshold voltage decreases with increasing free-electron concentration because the IGZO TFT has an n-type conduction channel. The creation of oxygen vacancies

during UV illumination could be due to the reaction of the UV-activated oxygen from the ambient with the oxide layer¹⁵³ or the direct creation of the oxygen vacancies by UV illumination.¹⁵⁴ In the second mechanism, electron-hole pairs are generated by UV illumination, and the photon-generated holes are trapped at the channel/dielectric interface or in the dielectric layer, leading to a decrease in the threshold voltage after the UV light is off.

^{103, 154, 155} The two mechanisms have been examined with the experiments, respectively.

Figure 5.3 Resistivity of the IGZO layer versus UV exposure time.

The first mechanism can be tested by examining the exposure duration dependence of the resistivity of the IGZO channel layer. A resistor structure with two top contacts on IGZO film was also deposited on a glass substrate. The structure and dimensions of channel and top contacts in the resistor were identical to the channel and source/drain electrode of a-IGZO TFTs. The resistivity of the IGZO layer deposited on a glass substrate was measured with a four-point probe in dark. Figure 5.3 shows the channel resistivity as a function of the UV exposure duration. It can be observed from the figure that there was no significant change in the resistivity within 160 s of UV exposure. The resistivity is related to the density of the free

electrons of the material, which can be described as $\rho = 1/q\mu n$, where q is the electron charge, μ is the hall mobility and n is the electron concentration. In the previous study, the a-IGZO channel could interact with oxygen species when expose to UV illumination. The increase in electron concentration of channel would result in the negative shift in threshold voltage. The resistivity of IGZO channel remained unchanged after UV exposure, indicating that the UV exposure did not produce a significant change in the free-electron concentration of the channel. In the contrast as shown in Figure 5.2(a), an exposure of 60 s caused a decrease of 0.6 V in the threshold voltage of the TFT. Therefore, the UV exposure-induced decrease in the threshold voltage cannot be attributed to the increase of the free-electron concentration as a result of oxygen vacancy generation in the oxide layer by UV illumination. Thus, this mechanism is eliminated from further consideration. The second mechanism will be discussed in the next section.

5.4 Recovery from ultraviolet-induced threshold voltage shift in a-IGZO TFTs by positive gate bias

For the second mechanism, the recovery characteristics effect of UV exposure on the threshold voltage of a-IGZO TFTs was investigated. If the negative shift in the threshold voltage is due to the positive charge trapping at the channel/dielectric interface or in the dielectric layer, the post-exposure threshold voltage is expected to show a very slow change with waiting time. This was indeed observed in the waiting-time experiment. In the experiment, the TFT was firstly exposed to UV illumination for duration of 120 s with power density of 5 mW/cm². This exposure caused a large decrease of 0.75 V in threshold voltage. Subsequently, its threshold voltage was monitored in dark ambient for an extended period of time without applying any electrical bias. (The device was kept in a dry cabinet to ensure that

the device was not exposed to any UV light in the environment and not affected by the humidity factor⁷⁶ during the extended period). Figure 5.4 shows the waiting-time dependence of the post-exposure threshold voltage at room temperature.

Figure 5.4 Post-UV exposure V_{th} measured in dark at various waiting times. The device was first exposed to UV illumination for 120 s.

As can be seen in the figure, the recovery in the threshold voltage after UV exposure of 120 s was very slow, e.g. the waiting time of 1×10^6 s led to a recovery of only 0.1 V in the threshold voltage. It is believed that the slow recovery in the threshold voltage was due to the release of the positive charges trapped at the channel/dielectric interface or in the dielectric layer, which was a very slow process at room temperatures without the assistance of applied fields.

In contrast to the very slow recovery under the condition without applied bias, it is found that the threshold voltage could be easily recovered with a positive gate pulse. To verify this, the TFT was test with following sequence condition: The as-fabricated TFT was firstly exposed to UV exposure for 120 s, then the device was kept in the dark and dry ambient for an period of 10^5 s with condition without applied bias, after that, a voltage pulse

of -10 V was applied to gate electrode with duration of 1 s, finally, another voltage pulse of $+10$ V was applied to the gate electrode, the transfer characteristics curves were measured after each condition step. Figure 5.5 shows the transfer characteristics of the TFT with the following sequent conditions, including the as-fabricated device, after UV exposure of 120 s, after a waiting time of 10^5 s in dark, and after applications of voltage pulses of -10 V/1 s and $+10$ V/1 s.

Figure 5.5 Transfer characteristics of the TFT with the following sequent conditions, including the as-fabricated device, after UV exposure of 120 s, after a waiting time of 10^5 s in dark and after application of voltage pulses of -10 V/1 s and +10 V/1 s.

As shown in Figure 5.5(a), the 120s UV exposure caused a large shift in the transfer curve towards a lower threshold voltage. The device was then kept in dark for 10^5 s, and only a small recovery was observed (Figure 5.5(b)). Subsequently, a -10 V pulse with 1 s duration was applied to the gate electrode; no significant change in the transfer characteristic was

observed (Figure 5.5(c)). However, when a +10 V pulse with 1 s duration was applied to the gate electrode, the transfer curve was shifted back to the original state immediately (Figure 5.5(d)), showing that the UV-induced shift could be fully recovered by the application of the positive voltage pulse. As IGZO is an n-type metal oxide semiconductor, electrons are the majority carriers in the IGZO channel layer. Electrons were accumulated in the interface region under the positive gate voltage. Therefore, the V_{th} recovery is expected from the neutralization of the positive charges (i.e. holes) trapped in the interface region as a result of the presence of a large amount of free electrons in the region. Our result indicates that application of a positive gate pulse is a simple and effective way to recover from the UV-induced threshold voltage shift.

An investigation of the influence of pulse voltage / duration on the recovery performance was conducted. Figure 5.6(a) shows the threshold voltage recovery after 120 s UV exposure as a function of the gate bias duration with the pulse voltage fixed at +10 V. ΔV_{th} just after the UV exposure was ~ -0.65 V; the magnitude of the ΔV_{th} decreased with the pulse duration; and it reached 0 V when the pulse duration was 1 s, indicating that the device was fully recovered. No further positive V_{th} shift was observed for the pulse durations longer than 1 s.

Figure 5.6 (a) Threshold voltage recovery as a function of the gate pulse duration with the pulse voltage fixed at +10 V (ΔV_{th} just after the 120 s UV exposure was ~ -0.65 V). (b) Threshold voltage recovery as a function of pulse voltage with pulse duration fixed at 1 s (ΔV_{th} just after the 120 s UV exposure was ~ -0.70 V).

Figure 5.6(b) shows the threshold voltage recovery as a function of pulse voltage with pulse duration fixed at 1 s. The threshold voltage shift induced by the 120 s UV exposure is ~ -0.7 V; this value remained unchanged after the application of the pulse of +5 V/ 1s. However, the magnitude of ΔV_{th} decreased linearly with the pulse voltage, and it reached ~ 0 V at the pulse voltage of 10 V.

In conclusion, the negative threshold voltage shift caused by UV exposure is attributed to the positive charge trapping in the dielectric layer and or at the channel/dielectric interface. The illuminated TFTs show a slow recovery in threshold voltage without external

bias. However, an instant recovery can be achieved by the application of positive gate pulses, which is due to the elimination of the positive trapped charges as a result of the presence of a large amount of field-induced free electrons in the interface region.

5.5 Ultraviolet photodetector application based on a-IGZO TFTs

In the past few years, wide band gap semiconductors such as SiC, InGaAs and GaN have been the most useful materials for UV detection.¹⁵⁶⁻¹⁵⁹ [ENREF 150](#) Metal oxide material has attracted much attention for its application as a UV detector. For example, ZnO is a wide and direct band gap semiconductor and a prospective alternative material to GaN in optoelectronic applications due to its low growth temperature, large exciton binding energy and high radiation hardness.¹⁶⁰⁻¹⁶² The UV detection mechanism based on ZnO thin film is attributed to the oxygen chemisorption and photodesorption behavior on the surface.^{163, 164} A UV detection application based on an a-IGZO TFT structure is considered in this section based on the previous examination of UV illumination instability and the recovery characteristics of a-IGZO TFTs. The photoelectric properties were characterized using a Keithley 4200 semiconductor characterization system in air and a UV spotlight source at a wavelength of 365 nm. Their high UV photosensitivity and fast responsivity made the a-IGZO TFTs suitable for UV photodetector application. Figure 5.7 shows the schematic of the TFT structure used for the experiment.

Figure 5.7 Schematic diagram of the TFT structure.

The photocurrent measurements were performed on a-IGZO TFTs in dark conditions and under UV illumination over various durations at room temperature. Figure 5.8 shows the typical I-V characteristics from the source-to-drain electrode with a gate electrode under a floating condition after different UV illumination durations. The responsivity was calculated according to the following relation:¹⁶⁵

$$R = \frac{I}{P_{inc}} \quad \text{Eq. (5.1)}$$

where I is the measured photocurrent and P_{inc} is the power of the incident UV light. The current read at 2 V after a UV illumination of 60 s was 5.68×10^{-8} A, and the illuminated area of the sample was $20 \times 20 \mu\text{m}$. Thus, the extracted responsivity of the device was 2.84 A/W. This value was higher than the ultraviolet photoconductive detector based on ZnO thin film,^{166, 167} but still lower than that of the GaN based detector of $\sim 2,000$ A/W.¹⁶⁸

Figure 5.8 I-V characteristics of source-to-drain electrodes with a gate electrode in a floating condition after different UV illumination durations.

The current measured in the a-IGZO TFTs significantly increased with the UV illumination duration. For example, the current (measured at 2 V) increased from $\sim 5.6 \times 10^{-12}$ A to $\sim 5.7 \times 10^{-8}$ A (an increase of 4 orders in magnitude) as the UV illumination duration increased from 0.1 to 60 s. The electron-hole pairs generated as photon energy at a wavelength of 365 nm were larger than the band gap of the IGZO material. The photogenerated holes had the potential to leave behind unpaired electrons and trap at the channel/dielectric interface or dielectric layer. The unpaired electrons were collected by the anode during UV illumination, leading to an increase in the photocurrent. This result suggested that the charge carriers generated under UV illumination plays a major role in the current generation mechanism.

Figure 5.9 Photocurrent of an a-IGZO TFT measured at an applied bias of 2 V as a function of excitation intensity.

Figure 5.9 shows the intensity dependence of the photocurrent measured at a bias of 2 V. The UV illumination intensity was set to range from 2 to 10 mW/cm². The photocurrent linearly increased with the UV light intensity, and the EHP photogeneration efficiency was proportional to the absorbed photon flux. It was determined to be suitable for practical application, as no saturation region was observed.

Figure 5.10(a) shows an increase in the photocurrent upon exposure to UV illumination and current decay after the UV light was removed. The device was initially exposed to UV illumination for duration of 100 s, after which the current was monitored under dark conditions at an applied bias of 2 V. The current decayed by only one order of magnitude after a waiting time of 10⁵ s. For example, the initial photocurrent just after UV illumination was $\sim 1.43 \times 10^{-7}$ A, and the current remained at $\sim 2.2 \times 10^{-8}$ A after a waiting time of 10⁴ s. This slow recovery can be attributed to the hole trapping mechanism, as discussed previously. It was difficult to relieve the hole trapping induced by UV illumination

at the channel/dielectric interface or dielectric layer without any bias. However, as shown in Figure 5.10(b), the current was recovered with the application of a positive gate pulse.

Figure 5.10 (a) Significant increase in the photocurrent upon exposure to UV illumination. However, it decayed after the UV light was removed. (b) Time dependence of the photocurrent under a modulated UV light source.

Figure 5.10(b) shows the time dependence of the photocurrent under modulated UV light. Rise time refers to the time taken to reach 90% of the maximum response current from 10%, and fall time refers to the time required to reach 10% of the maximum current from 90%.¹⁶⁹ As Figure 5.10(b) shows, the photocurrent reached 90% of the saturation current with

a rise time of 50 s. As a positive gate pulse of +10 V/1 s was applied to the device, the photocurrent immediately recovered to the initial status at a fast fall time, indicating a high sensitivity and excellent repeatability. However, a negative gate voltage pulse had no effect on the current conduction. When a positive voltage pulse was applied to the gate electrode, the trapped holes at the channel/dielectric interface or dielectric layer were released from both. With the release of the trapped holes, the accumulated electrons induced were removed from the interface as a result of the photocurrent recovery. Because a negative gate voltage pulse attracted the trapped holes and kept them at the interface and dielectric layer, no obvious changes were observed in the current.

Figure 5.11 Evolution of the source-to-drain current of a photodetector based on a-IGZO TFTs. The device was exposed to multiple 1-s UV pulses.

To examine the sensitivity of a-IGZO TFTs to UV light, the source-to-drain current was measured by sweeping the voltage from 0 to 2 V with multiple 1-s UV light pulses applied to an a-IGZO TFT channel. As Figure 5.11 shows, a change in the source-to-drain current was observed. There was an abrupt increase in the current with the corresponding applied UV pulses, indicating the good sensitivity of a-IGZO TFTs to UV light. The current

decayed after the UV pulses, which can be attributed to the recombination of the generated EHPs. Finally, the current reached a saturation state due to the hole trapping at the interface or dielectric layer.

In summary, a UV photodetector based on an a-IGZO TFT structure was examined. The responsivity of the detector was measured at 2.84 A/W under an incidental UV light with a wavelength of 365 nm at an applied bias of 2 V. The device's high UV photosensitivity and rapid response revealed it to be suitable for UV photodetector applications. The photocurrent exhibited a slow decay time, which can be attributed to hole trapping at the dielectric/channel interface and dielectric layer. However, recovery was instantly achieved by applying a positive gate pulse.

Chapter 6 MEMORY APPLICATIONS BASED ON INDIUM GALLIUM ZINC OXIDE THIN FILM

6.1 Transparent nonvolatile memory devices based on a-IGZO thin film

6.1.1 Introduction

Transparent electronic have become one of the most attractive research fields for the next generation of innovative vision-free products and optoelectronics.¹⁷⁰⁻¹⁷² IGZO is a very promising transparent semiconductor material for transparent electronics, as the film can provide a high carrier mobility in its amorphous state, with a high transmittance in the visible spectrum via transparent oxide transistors and transparent logic circuits.¹⁷³⁻¹⁷⁶ Several types of nonvolatile memory (NVM) structures have been used depending on the information storage mechanism required, such as ferroelectric thin film, resistive thin film and the charge-trapping stack (a sandwich structure with a charge blocking layer, a charge trap or floating layer and a charge tunneling layer).¹⁷⁷⁻¹⁷⁹ Among these structures, the NVM structure incorporating a floating gate device is the most frequently used in silicon-based electronics.¹⁸⁰ The memory states are represented by the threshold voltage shift, which is achieved by storing or releasing the charges in the floating layer. In this study, a transparent NVM device

with a bottom-gate a-IGZO TFT structure and a charge-trapping stack layer was fabricated and its electrical properties and memory behavior were examined.

6.1.2 Fabrication of transparent a-IGZO NVM memory

The a-IGZO TFT NVM device was fabricated on a cleaned ITO glass substrate, which served as the bottom gate. An oxide nitride oxide (ONO) gate insulator layer, which served as the charge storage layer, was deposited on the ITO glass. In synthesizing the ONO layer, a 35-nm HfO_2 charge block layer was initially formed via ALD. A 20-nm Si_3N_4 charging layer was then deposited via PECVD, followed by the deposition of a 10-nm HfO_2 tunnel layer via ALD. A 50-nm-thick IGZO film was then deposited on the ONO layer via RF sputtering with a single IGZO target, similar to the process carried out for the IGZO TFTs. The TFT active layer was then wet etched, followed by the formation of the source/drain according to the photolithography process. Finally, 20-nm thick ITO transparent source/drain electrodes were formed via RF sputtering. Figure 6.1 shows the schematic diagram of the device structure. The electrical characteristics were measured with a Keithley 4200 semiconductor characterization system at room temperature.

Figure 6.1 Schematic diagram of the transparent a-IGZO NVM device.

6.1.3 Memory behavior of a-IGZO NVM devices

Figure 6.2 shows the typical program characteristics of a transparent a-IGZO NVM device. The positive shift in V_{th} represents the programming process and the negative shift in V_{th} represents the erasing process. The transfer curves of transparent a-IGZO NVMs are similar to those of TFTs.

Figure 6.2 Transfer curves of the a-IGZO NVM device with a $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ charge-trapping layer as the gate insulator under different charging conditions.

The electrical parameters of the NVM were extracted according to the standard method. The threshold voltage, linear field effect mobility, S.S and on/off state current ratio were 2.4 V, $10.4 \text{ cm}^2/\text{V s}$, 430 mV/decade and 10^7 , respectively. The programming action (i.e., the charging process) was carried out via F-N tunneling.¹⁸¹ As shown in Figure 6.2, the transfer curve positively shifted with the charging bias at 10 V. The electrons induced at the channel/dielectric layer interface were tunneled through the thin HfO_2 layer and trapped in the Si_3N_4 layer under a positive gate bias, resulting in a positive shift in the transfer curves. Thus, the V_{th} increased as the charging time increased, e.g., V_{th} increased from 2.4 to 3.4 V, showing a memory window of 1 V.

Figure 6.3 Threshold voltage of the a-IGZO NVM device as a function of the programming bias for 1 ms.

Figure 6.3 shows the threshold voltage of the a-IGZO NVM device as a function of the programming bias for 1 ms. A linear relationship between the V_{th} and magnitude of the programming bias can be observed. The electrons in the a-IGZO channel tunneled through the dielectric layer with a large applied voltage via F-N tunneling. The electric field in the top HfO_2 was approximately the applied programming bias divided by the oxide thickness.¹⁸¹ The higher programming bias resulted in a higher injection of electrons into the ONO layer. These electrons were trapped in the Si_3N_4 layer and confined between the top and bottom HfO_2 layers, causing an increase in the threshold voltage.

Figure 6.4 Programming/erasing characteristics of the a-IGZO NVM device.

The programming/erasing characteristics of the transparent IGZO NVM were obtained via F-N tunneling, and the result is shown in Figure 6.4. The programming and erasing biases were set at 30 and -30 V, respectively. The charging/discharging durations varied from 0.1 ms to 1 s. When the programming time was less than 1 ms, no significant threshold voltage shift was observed. The threshold voltage started to increase when the programming time was longer than 1 ms. To erase the programmed device, a negative gate bias was applied to the gate with the S/D electrodes grounded. However, the threshold voltage showed little change with the erasing time. Even when a larger gate bias (close to the ONO dielectric breakdown voltage) was applied, no obvious threshold voltage shift occurred in the IGZO NVM device. As Figure 6.4 shows, the erasing efficiency of the device was much poorer than that of the programming process. It is believed that this poor erasing characteristic is related to the special material properties of IGZO thin film. Unlike the conventional ONO memory where the electron/holes can be induced in the Si substrate when the device is in depletion/accumulation region, the IGZO device usually exhibits

unintentional n-type conduction, supplying only one type of carrier of electron for channel conductance. Therefore, in the IGZO device, few holes are available for positive charge injection into the gate insulator as to neutralize the stored negative charges.¹⁷⁹ Furthermore, when negative bias is applied to the gate electrode, the device is in the off state region, the channel exhibits very high resistance, the effective electrical field from the Si_3N_4 layer to the substrate is very low; thus, it is not easy to extract the trapped electrons out from the charge trapping layer.

Figure 6.5 Retention characteristics of the a-IGZO NVM device after being programmed at 20 V with a duration of 1 s.

The charge retention characteristics of the a-IGZO NVM device were investigated at room temperature. As shown in Figure 6.5, the device was initially programmed with a bias of 20 V for 1 s via F-N tunneling, which caused the threshold voltage to shift from 2.5 to 3.4 V. The threshold voltage of the device was then monitored for an extended period under dark conditions. The threshold voltage gradually decreased after a waiting time of 10^3 s. The charges stored in the Si_3N_4 layer were laterally transferred along the Si_3N_4 layer, similar to

the process used in conventional NVM devices. To improve retention capability, a proper isolation must be provided to confine the trapped charges in the Si_3N_4 layer.

In summary, the memory characteristics of the transparent NVM device based on a-IGZO thin film were examined. The device showed asymmetric programming and erasing characteristics with a small erase window. The poor erasing characteristic can be attributed to the a-IGZO channel: because it was an n-type semiconductor, no holes could be induced under a negative gate bias condition. A novel device structure is required to improve the erasing efficiency, and proper device isolation is required to achieve good retention capability.

6.2 Realization of write-once-read-many-times memory device with O_2 plasma-treated indium gallium zinc oxide thin film

6.2.1 Introduction

Write-once-read-many-times memory devices could be used in high-speed, permanent archival storage application for videos, images and other noneditable database. WORM memories based on organic materials, such as small molecules and polymers have been demonstrated.¹⁸²⁻¹⁸⁷ WORM devices have also been realized with various inorganic thin film materials. e.g., a WORM memory device was realized based on the charging-controlled modulation in the current conduction of an Al/Al-rich Al_2O_3 /p-type Si diode,^{188, 189} and a WORM device based on conduction switching of a NiO thin film in a metal-insulator-metal structure fabricated on a flexible substrate was reported.¹⁹⁰ In the present work, a WORM memory device based on O_2 plasma-treated IGZO thin films is demonstrated. The device has a simple Al/IGZO/Al structure. Its memory operation is based on the switching from an OFF state to an ON state by applying a voltage pulse. The device has a normally-OFF state with a

very high resistance (e.g. the resistance at 2 V is $\sim 10^9 \Omega$ for a device with the radius of 50 μm) as a result of the O_2 plasma treatment on the IGZO thin films; and it can be switched to an ON state with a low resistance (e.g. the resistance at 2 V is $\sim 10^3 \Omega$ for the radius of 50 μm) by applying a voltage pulse (e.g. 10 V / 1 μs). The WORM device exhibits good data-retention and reading-endurance capabilities.

6.2.2 Experiment

The schematic of the WORM device based on IGZO thin film is illustrated in the inset of Figure. 6.6. A 30 nm Al_2O_3 layer was deposited on a p type Si substrate which server as the buffer layer by ALD process at 250 $^\circ\text{C}$ with 99% purity TMA. A 200 nm thick Al layer was then deposited on the Al_2O_3 layer by RF magnetron sputtering to form the bottom electrode. After that, IGZO film was deposited onto the Al layer by RF magnetron sputtering of an IGZO target with the mole ratio of In : Ga : Zn : O = 1 : 1 : 1 : 1 in a mixed Ar/ O_2 ambient at a flow rate ratio of 10/1. During sputtering, the RF power was set at 100 W and the sputtering pressure was 3 mTorr. In order to investigate the influence of the thickness on the memory behavior of the WORM devices, IGZO thin films with the thicknesses of 50, 100, 200 and 400 nm were deposited, respectively. The deposited IGZO thin films were then subjected to an O_2 plasma treatment for 10 minutes at room temperature with a microwave plasma asher (PVA Tepla, 300 autoloader-pc). The O_2 plasma is generated by exciting the oxygen gas (O_2 flow rate = 820 ml/min, pressure = 1 mbar) at the frequency of 2.45GHz with the power of 800 W. In our previous study, it was found that O_2 plasma treatment can greatly increase the resistivity of the IGZO thin film as a result of the reduction in the concentration of the oxygen vacancies in the IGZO thin film.¹⁹¹ The as-deposited IGZO thin film has a very low resistivity ($5.6 \times 10^{-3} \Omega\cdot\text{cm}$); however, the O_2 plasma treatment for 75 s causes the resistivity increase to $1.9 \times 10^{-1} \Omega\cdot\text{cm}$, and the resistivity is extremely high (the resistivity is too high to be measured with a four-point probe.) after the plasma treatment of 10 minutes.

The increase in the resistivity is due to the large decrease in the free electron concentration in the IGZO thin films, e.g. the electron concentration decreases from $1.3 \times 10^{21} \text{ cm}^{-3}$ of the as-deposited film to $2.2 \times 10^{18} \text{ cm}^{-3}$ after the O_2 plasma treatment of 75 s. The XPS measurement shows that the O_2 plasma treatment can greatly reduce the concentration of the oxygen vacancies which act as donors in the IGZO thin film.¹⁹¹ With the O_2 plasma treatment, the resistance of the OFF state of the WORM device is very high such that the OFF-state current is very low, which is very useful to the operation of the WORM device. Finally, the top Al electrode was deposited using RF magnetron sputtering and patterned into circular pads with radius of 50 μm by photolithography and lift-off process. The electrical characterization of the devices was carried out with a Keithley 4200 semiconductor characterization system at room temperature.

6.2.3 Result and discussion

Figure 6.6 shows the current-voltage characteristics of the device as fabricated and after the applications of voltage pulses of 4 V / 1 ms and 8 V / 1 ms, respectively. The I-V characteristics were measured by sweeping the voltage from 0 to 2 V. The device is initially in the high-resistance state (i.e., the OFF state) with the current at the order of nA. As shown in the figure, there is no significant change in the current conduction after the application of the voltage pulse of 4 V / 1 ms. However, the current drastically increases after applying the voltage pulse of 8 V / 1 ms. For example, the current measured at 2 V increases from $3.92 \times 10^{-9} \text{ A}$ to $2.52 \times 10^{-3} \text{ A}$ (~ 6 orders) after the application of the voltage pulse; and the current then remains at the same order (10^{-3} A) in the repeating voltage sweepings. This means that the device can be switched from a high-resistance state (the OFF state) to a low-resistance state (the ON state) by applying a voltage pulse. The ON state can be maintained without returning back to the OFF state in the subsequent positive or negative voltage sweepings. The irreversible switching is ideal for the WORM device application.

Figure 6.6 I-V characteristics of the WORM device before and after the application of voltage pulses. The inset shows the schematic diagram of the Al/IGZO/Al WORM device structure.

Resistance switching has been observed in many metal oxide systems, and various switching mechanisms such as cation migration or conductive filament (CF) of oxygen vacancies have been proposed.¹⁹²⁻¹⁹⁶ The switching between a high-resistance state and a low-resistance state is generally reversible. However, in the present work, the switching from the OFF state to the ON state in the O_2 plasmas-treated IGZO layer is non-reversible. A plausible mechanism is shown in Figure 6.7.

Figure 6.7 Schematic illustrations of the changes in oxygen vacancies in the IGZO layer as a result of O_2 plasmas treatment or the application of a writing voltage.

Before O_2 plasmas treatment, there is a high concentration of oxygen vacancies in the as-deposited IGZO film, thus the film's resistivity is very low. Oxygen plasma is known to contain various excited oxygen species, including O^+ , O_2^+ , and O^* .¹⁹⁷ During the O_2 plasma treatment, oxygen radical atoms diffuse into the IGZO layer from the surface, reaching tens

of nanometers in depth to fill the oxygen vacancies.^{160, 198} This greatly reduces the free electron concentration in the film's surface region, and thus the OFF state is observed. However, when a voltage is applied to the device, some of the lost oxygen vacancies in the surface region are regenerated as a result of electrochemical reactions under the influence of electric field. With the formation of CFs by the oxygen vacancies connecting the two electrodes, the ON state is achieved.

Figure 6.8 Device currents measured at 2 V as a function of either (a) the pulse voltage with the pulse duration fixed at 1 μ s or (b) the pulse duration with the pulse voltage fixed at 7 V.

Figure 6.8 shows the influence of the application of a voltage pulse (i.e., writing the WORM memory) on the current of the device measured at 2 V. Figure 6.8(a) shows the current as a function of the pulse voltage with pulse duration fixed at 1 μ s. As can be observed in the figure, the writing of the WORM device has a threshold voltage of ~ 7 V (note that the threshold voltage depends on the pulse duration as well as the IGZO film thickness). When the writing voltage is lower than ~ 6 V, the device remains at the initial high-resistance state with the current of $\sim 10^{-9}$ A; the current drastically increases to $\sim 10^{-4}$ A when the voltage reaches ~ 7 V, and it further increase to $\sim 10^{-3}$ A at the pulse voltage of 10 V. This indicates that the ON state can be easily achieved with a voltage pulse of greater than 7 V (for the pulse duration of 1 μ s). Figure 6.8(b) shows the current as a function of the pulse duration for the pulse voltage fixed at 7 V. The device shows a high-speed writing performance. As can be seen in the figure, the pulse duration of 1 μ s results in an increase in the current by about ~ 4 orders at the pulse voltage of 7 V, which provide a memory window large enough for the memory operation (note that for the same increase in the current, a shorter pulse duration is required for a high pulse voltage, as suggested by Figure 6.8(a)). Also as expected, a longer pulse duration results in a larger increase in the current (and thus a larger memory window).

Figure 6.9 (a) Retention characteristic of the OFF and ON states; and (b) reading endurance of the OFF and ON states. The current is measured at 2V.

Figure 6.9(a) shows the data-retention performance of the WORM devices. The currents of both the OFF state (i.e. the state before writing) and the ON state (i.e. the state after writing) were measured with a reading voltage of 2 V at room temperature. The OFF state current measurement was firstly measured for 10^5 s. Subsequently, a voltage pulse of 8 V with 1 μ s duration was applied to switch the device from the OFF state to the ON state; then the current of the ON state was measured in the time frame of 10^5 s. It is observed that there is no significant change in the OFF state currents and only a very small reduction in the ON

state currents after 10^5 s. The predicted current ratio of the ON state to the OFF state (the memory window) is still larger than 4 orders after 10 years. The reading endurance of the WORM device has been also characterized, as shown in Figure 6.9(b). No significant degradation is observed for the OFF and ON states after 10^6 readings at 2 V, showing an excellent reading endurance.

Figure 6.10 Threshold voltage and corresponding electric field for writing for the pulse duration of 1 ms as a function of the IGZO film thickness. For each thickness, ten devices at different locations on a die were measured.

The influence of the IGZO film thickness on the threshold voltage of writing (i.e. the minimum pulse voltage required to produce a current increase by 4 orders for a given pulse duration) has been examined. Figure 6.10 shows the threshold voltage as a function of the film thickness for the pulse duration of 1 ms. As expected, the threshold voltage decreases with decreasing film thickness. However, as shown in the same figure, the corresponding electric field increases as the film thickness decreases, indicating that a larger electric field is required for a thinner IGZO layer to switch from the OFF state to the ON state. This observation can be explained as follow. As pointed out early, O_2 plasma treatment reduces

oxygen vacancies in IGZO surface layer.¹⁹¹ The impact of the reduction in oxygen vacancies in a thinner IGZO layer would be more significant than that in a thicker IGZO film with the same amount of O₂ plasma treatment on the surface. The CFs connecting the top and bottom electrodes are more difficult to be formed in a thinner IGZO layer due to the reduction of oxygen vacancies in the surface region. Thus, a high electric field is required for switching from the OFF state to the ON state to occur in a thinner IGZO layer.

6.2.4 Conclusion

In conclusion, a WORM memory device based on a simple Al/IGZO/Al structure with good performance has been demonstrated. Its memory operation is based on the switching from an OFF state to an ON state by applying a voltage pulse. The device has a normally-OFF state with a very high resistance due to the reduction of oxygen vacancies in the film surface region by the O₂ plasma treatment. An ON state is achieved when CFs connecting the two electrodes are formed due to the regeneration of the lost oxygen vacancies in the IGZO surface region under the influence of the applied field. A sufficiently large memory window (e.g., with the ON/OFF current ratio of $\sim 10^4$) can be achieved by applying a low-voltage pulse (e.g., 7 V) with short duration (e.g., 1 μ s). The WORM memory has good data-retention and reading-endurance capabilities.

Chapter 7 CONCLUSION AND RECOMMENDATIONS

7.1 Conclusion

This study examined the electrical and optoelectronic properties of TFTs based on indium gallium zinc oxide material with a focus on device fabrications, thin film characterizations and physical analyses. It explored potential applications based on the TFT structure, such as ultraviolet photodetectors, transparent NVM and write-once-read-many-times memory. Its key findings are summarized in this chapter.

7.1.1 High performance indium gallium zinc oxide thin film transistors with O₂ immersion

TFTs with a bottom gate structure were fabricated based on IGZO thin film as the active layer, and the electrical characteristics of the a-IGZO TFT were examined. During the deposition of the IGZO thin film, the RF sputtering process was carried out only in an argon ambience. The device initially performed poorly due to the high electron concentration in the a-IGZO channel. After O₂ plasma immersion was conducted on the post-deposition IGZO channel, the a-IGZO TFT exhibited excellent operational characteristics, namely, a drain-to-current on/off ratio of 10^7 , an S.S of 0.25 V/decade and a field-effect mobility of 26.8 cm²/Vs. The evolution of the electrical properties of a-IGZO TFTs with O₂ plasma immersion

was also investigated. The O₂ plasma immersion on the surface of a-IGZO thin film resulted in an enhancement in the Hall mobility and a decrease in the carrier concentration. XPS was conducted on the IGZO thin film to analyze the effect of the O₂ plasma immersion on the electrical properties of the TFTs. The O₂ plasma immersion was found to greatly improve transistor performance, which may be attributed to the reduction of oxygen-related defects in the IGZO thin film.

7.1.2 Effect of exposure to ultraviolet-activated oxygen on the electrical characteristics of amorphous indium gallium zinc oxide thin film transistors

The threshold voltage of the a-IGZO TFTs was determined by the electron concentration in the channel layer, which was related to the oxygen vacancies. However, because the oxygen vacancies could have easily been generated in the IGZO thin film during the fabrication steps, it was not easy to control the threshold voltage of the a-IGZO TFTs. The threshold voltage could be tuned simply by exposing the IGZO channel to UV-activated oxygen. As a result, the threshold voltage was highly sensitive to the UV-activated oxygen. The threshold decreased linearly with the exposure time. XPS measurements were performed on the IGZO thin film before and after its exposure to UV-activated oxygen to analyze the effect on the electrical characteristics of the a-IGZO TFTs. The shift in threshold voltage of the TFTs can be attributed to the increased electron concentration in the channel layer due to the oxygen vacancies created by the UV-activated oxygen exposure. In addition, the on-state current increased with exposure time, although other device parameters such as the field effect mobility and S.S were not significantly affected. These results indicate that exposing post-fabrication a-IGZO TFTs to UV-activated oxygen is a simple and effective method for

controlling the threshold voltage of a device, and that TFTs can be easily switched from the enhancement to the depletion mode using this proposed technique.

7.1.3 Electrical instabilities in indium gallium zinc oxide thin film transistors under UV illumination and its application

UV illumination cleaning is usually applied during TFT fabrication to remove particles and impurities from the thin film surface. This study investigated the electrical instability induced by UV illumination in a-IGZO TFT, and found that UV exposure led to a negative shift in the threshold voltage of the device. The decreased rate of the threshold voltage was examined and showed a rapid decrease rate for a short exposure duration of less than 10 s and a slow decrease rate for a longer exposure duration. The mechanism of shifting the threshold voltage via UV illumination can be attributed to photogenerated hole trapping at the channel/dielectric interface or dielectric layer. The proposed mechanism was consistent with the recovery characteristic effect in the threshold voltage of TFT after UV exposure. The threshold voltage recovery induced by UV exposure was very slow due to the positive charge trapping at the dielectric/channel interface or dielectric layer. However, the threshold voltage was easily recovered by applying positive voltage pulses to the gate electrode. Based on these results, a UV photodetector application with an a-IGZO TFT structure was proposed. The detector showed a high responsivity of 2.84 A/W with an incident wavelength of 365 nm under an applied bias of 2 V. The slow decay was recovered by positive gate bias pulses due to the elimination of the positive trapped charges as a result of the presence of field-induced electrons in the interfacial region.

7.1.4 Memory application based on indium gallium zinc oxide thin film

Transparent NVM devices based on a-IGZO thin film were examined in this study. The oxide-nitride-oxide sandwich structure was used for the charge-trapping layer. The charging/discharging characteristic and retention of the device were also examined. The device exhibited good program characteristics with a positive bias, but poor erasing characteristics. The asymmetric programming and erasing characteristics can be attributed to the a-IGZO channel, which made it difficult to induce holes under a negative gate bias. In addition, this study demonstrated a write-once-read-many-times memory device based on O₂ plasma-treated IGZO thin films with an Al/IGZO/Al structure. The device exhibited a normal “OFF” state with very high resistance of $\sim 10^9 \Omega$ at 2 V as a result of subjecting the IGZO thin film to O₂ plasma treatment. The device could be switched to the “ON” state at a resistance of $\sim 10^3 \Omega$ with a voltage pulse. The state change resulting from the voltage pulse can be attributed to the formation of a conductive filament connecting the two electrodes due to the regeneration of the lost oxygen vacancies in the IGZO surface region under the influence of the applied field. The WORM device exhibited a larger memory window and good data retention and reading-endurance characteristics. Therefore, IGZO shows promise for transparent archival storage applications.

7.2 Recommendations for future work

This study sought to provide a better understanding of the electrical and optoelectronic properties of a-IGZO TFTs, especially their applications in NVM and write-

once-read-many-times memory. To complete the study, the following recommendations for future work are proposed.

7.2.1 Fully transparent nonvolatile memory based on IGZO nanocrystals embedded in SiO₂

It was found that the electron concentration of a-IGZO thin film could be increased or decreased using various techniques. For example, post-deposition O₂ plasma immersion was found to greatly decrease the electron concentration in a-IGZO thin film, and exposure to UV-activated oxygen proved an effective way to increase the electron concentration. Based on these findings, an a-IGZO nanocrystal may be used as a charge storage layer in NVM applications. In this study, a-IGZO nanocrystals were successfully synthesized by RF sputtering followed by a rapid thermal process (RTP). Figure 7.1 shows a scanning electron microscope (SEM) image of the a-IGZO nanocrystals. The metal oxide material could replace the charge storage layer for fully transparent NVM applications.

Figure 7.1 SEM image of a-IGZO nanocrystals synthesized by RF sputtering followed by a rapid thermal process.

7.2.2 Study of the evolution of the dielectric function of IGZO thin film with decreasing film thickness

The nanoscale structure of ZnO thin film and associated devices exhibits unique properties that are different from their bulk counterparts due to quantum confinement. Both the real and imaginary parts of the dielectric function decreased significantly as the film thickness decreased, accompanied by an increase in both the band gap and exciton binding energies.¹⁹⁹ As IGZO nanocrystals have been proposed for use in devices, it would be interesting to investigate the film-thickness dependence of the complex dielectric function of ultrathin IGZO film, and to examine the film's quantum confinement effect.

7.2.3 Optimization of electrical stability of a-IGZO TFTs induced by UV illumination

As mentioned in Chapter 5, a negative shift in the threshold voltage of a-IGZO TFTs was observed upon UV illumination. Future research must investigate the optimization of electrical stability issues for a-IGZO TFTs under UV illumination. An additional passivation layer made of materials such as SiO₂, Si₃N₄ and polymers is commonly deposited on the surface of the a-IGZO channel to improve the reliability of the device.²⁰⁰⁻²⁰² Future research should examine the mechanism used to improve device stability with a passivation layer under UV illumination.

LIST OF PUBLICATIONS

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- [1] **P. Liu**, T. P. Chen, Z. Liu, C. S. Tan and K. C. Leong, “Effect of O₂ plasma immersion on electrical properties and transistor performance of indium gallium zinc oxide thin films”, *Thin Solid Films*, **545**, 533 (2013).
- [2] **P. Liu**, T. P. Chen, X. D. Li, Z. Liu, J. I. Wong, Y. Liu and K. C. Leong, “Effect of exposure to ultraviolet-activated oxygen on the electrical characteristics of amorphous indium gallium zinc oxide thin film transistors”, *ECS Solid State Letters* **2**, Q21 (2013)
- [3] **P. Liu**, T. P. Chen, X. D. Li, Z. Liu, J. I. Wong, Y. Liu and K. C. Leong, “Recovery from ultraviolet-induced threshold voltage shift in indium gallium zinc oxide thin film transistors by positive gate bias”, *Applied Physics Letters* **103**, 202110 (2013)
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