High frequency noise modeling of deep-submicron MOSFETs

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**HIGH FREQUENCY NOISE MODELING OF DEEP
SUB-MICRON MOSFETS**

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Abstract

At high frequency of gigahertz, the channel thermal noise is dominating the noise of MOSFETs. The channel thermal noise model in short channel MOSFETs deviate from long channel noise model. A simple analytical model for the high frequency channel thermal noise of deep sub-micron MOSFETs in strong inversion region is developed. The model is derived based on both the local noise source approach and the local current noise source approach, including the short channel effects, such as channel length modulation effect, velocity saturation effect, hot carrier effect and mobility reduction due to vertical field. To improve the accuracy of the channel thermal noise model especially in drain bias domain, a novel effective mobility model is developed, in which the drain-induced vertical field is incorporated. The new noise model is verified with measured results across different dimensions, frequencies, and biasing conditions.

The on-wafer high frequency drain current noise characterization of MOSFETs shows a frequency-dependent trend that contradicts with the white noise assumption of the channel thermal noise. A substrate-induced drain current noise model is introduced to model the additional frequency dependent drain current noise. Y-parameter analysis is performed on the small-signal equivalent circuit of MOSFET, which includes a substrate network. A new parameter extraction technique is introduced to obtain the model parameters of MOSFET. Eventually, the total drain current noise model, including the channel thermal noise, the gate resistance thermal noise, and the

substrate-induced drain current noise, is verified with the on-wafer measurement data and is found to accurately predict the noise characteristic of MOSFETs.

A gate current noise model including a newly derived short-channel induced gate noise model and the gate resistance thermal noise model is developed, followed by the corresponding cross-correlation model. Based on the proposed drain current noise model, the gate current noise model and the cross-correlation model, the four noise parameters are computed and verified with on-wafer measurement noise data.

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Chapter 1 Introduction

1.1 Motivation

Nowadays, MOSFETs are popular in RFIC design as MOSFETs are cost effective, having low power consumption while providing high level of integration. Its continuous down scaling to nanometer channel length has successfully enhanced the RF performance of the device in such that unity gain frequencies up to hundreds of gigahertz can be achieved [1]. Nevertheless, a low noise RF circuit requires the high frequency noise performance of nanometer MOSFETs to be modeled accurately in a physical-based manner. Simple and accurate physical-based noise model is needed to reduce the design cycle of RFICs.

With the downscaling of device channel length and increasing of operation frequency, on-wafer measurement and device modeling work on silicon MOSFETs have become more and more significant and challenging for RF IC design. The noise model that includes physical noise mechanism based on long channel MOSFETs is no longer appropriate to predict the noise characteristic of short-channel devices of which the short channel effects become significant. Thus, it is crucial to understand the noise behavior of the MOSFETs with presence of the short channel effects. So far, the short channel effects, which are considered in channel thermal noise, are channel length modulation (CLM) [2-4], velocity saturation effect (VSE) [2, 5-10] and hot carrier effect (HCE) [2, 6, 7, 10-14]. This has led to many publications and at the same time, unfortunately, some controversy as to which of the short channel effects should be

considered and the proper way to include them in the thermal noise model. Moreover, the mobility degradation due to vertical field, which could be of utmost important for short channel MOSFETs noise modeling in drain bias domain, has least concern in the literatures to date.

Besides, much efforts [2, 3, 5-13, 15-17] has been given on the study of channel thermal noise, which is white noise. However, the on-wafer high frequency noise measurement demonstrates non-white-noise characteristic on drain current noise. The frequency-dependent part is normally assumed to be measurement error and lack of concern on its origin. Nevertheless, with down-scaling of channel length, the frequency dependent excessive noise is found to be more severe, and thus it is extremely unlikely to be measurement error. The white noise characteristic can only be observed in the drain current noise at frequency higher than 5 to 10 GHz for deep sub-micron RFCMOS, and even more than 10 GHz for nanometer RFCMOS. Therefore, other noise sources such as substrate resistance thermal noise need to be studied and modeled.

Apart from drain current noise model, the gate current noise model and their cross-correlation are important for the calculation of the most common four noise parameters, consisting of the minimum noise figure, noise resistance, optimum source conductance and susceptance, that govern the noise performance of MOSFETs and thus become the primary concern of RFIC design. Therefore, it is important to study the impact of short channel effects and noisy substrate on the four noise parameters.

1.2 Objective

This research is aim to develop a high frequency noise model to predict the noise performance of deep sub-micron RFCMOS accurately across different operating conditions such as frequency, gate bias and drain bias, and different dimensions such as channel length and channel width. The proposed noise models include the channel thermal noise model with proper consideration of various short channel effects, drain current noise model with inclusion of important noise source such as substrate thermal noise, gate current noise model consisting of short-channel induced-gate noise and gate resistance thermal noise, and the cross-correlation model between the gate current noise and drain current noise. Beside, the model parameter extraction methodology is part of the goal.

1.3 Overview

In chapter 2, the basic knowledge of noise is explained. The derivation of conventional channel thermal noise models are presented in detail. Some published models with short channel effect are reviewed. The noise measurement and the de-embedding technique are discussed.

In chapter 3, the impact of the short channel effects, such as channel length modulation, velocity saturation effect, and hot carrier effect, on the channel thermal noise model is discussed. Based on both the local voltage noise source approach and the local current noise source approach, the high frequency channel thermal noise models are derived in four different cases. First, the effect of channel length modulation only is considered. Second, channel length modulation and velocity

saturation effect are included in the derivation. Third, channel length modulation and hot carrier effect are taken into consideration. The fourth case is to incorporate all the three abovementioned short channel effects into the channel thermal noise model. The noise models are then compared with the measurement data to figure out which is the most accurate way to include the short channel effects in the channel thermal noise model.

In chapter 4, a new effective mobility model is presented to consider the mobility degradation effect due to the gate field and the drain-induced vertical field. The effective mobility model is incorporated to the high frequency channel thermal noise model as proposed in chapter 3. The simulated channel thermal noise spectral density are compared with the extracted noise data across different frequencies, gate biases, drain biases, channel length, and channel width.

In chapter 5, the impact of lossy substrate network on the high frequency noise performance of MOSFETs is discussed. The substrate-induced drain current noise is introduced to explain the non-white-noise characteristic of the measured drain current noise in GHz range. The substrate network with the substrate resistance thermal noise source is introduced in the proposed small signal equivalent circuit of MOSFET. A new model parameter extraction method is demonstrated. Thereafter, the extracted small signal parameters are being optimized and utilized in noise model calculation. By adding the substrate-induced drain current noise model to the channel thermal noise model derived in previous chapter, the total drain current noise model is developed and experimentally verified. Thereafter the gate current noise, the cross correlation, and the

Chapter 1 Introduction

four noise parameters of proposed model is examined with on-wafer measurement noise data.

In Chapter 6, the conclusion is drawn by giving a summary and suggesting the future works.

Chapter 2 Fundamental Noise Theory

2.1 Overview of Noise

Noise is an unwanted disturbance which interferes with the desired signal in electronic systems and devices. Noise is spontaneous fluctuation in the current, voltage and temperature of the systems and devices under test. There are a few types of noise sources in MOSFETs, such as thermal noise, flicker noise and shot noise. Noise becomes an utmost important consideration in the application of electronic circuits and system as it imposes a fundamental limitation to the performance of the electronics and the accuracy of the measurements. Hence, it is of paramount important to understand the source of the noise and how it is being described in MOSFETs.

2.1.1 Thermal Noise

The presence of thermal noise is due to the thermal agitation of the electrons inside an electronic conductor under thermal equilibrium. It is also known as Johnson noise [18] or Nyquist noise [19]. Thermal noise is determined by the electrical resistance and temperature of the device under thermal equilibrium [18].

$$\overline{v_n^2} = S_{v_n} \Delta f = 4kTR\Delta f \quad (2.1)$$

$$\overline{i_n^2} = S_{i_n} \Delta f = \frac{4kT\Delta f}{R} \quad (2.2)$$

where k is the Boltzmann's constant with $k = 1.38 \times 10^{-23} \text{ J/K}$, R (in Ohm) is the resistance of the conductor, T (in Kelvin) is the absolute temperature, and Δf (in Hertz) is the small section of bandwidth where the noise is measured.

Since the flicker noise becomes negligible at high frequency range of GHz, the thermal noise of channel resistance and parasitic resistances become the dominant source of noise [3, 7, 9, 12, 15-17, 29, 62-64] for MOSFETs operating in strong inversion region, at high frequency of GHz regime. In future technologies, where channel length scaling continues, the channel thermal noise increases and becomes even larger [3, 7, 9, 12, 15-17, 29, 62-64], due to the channel length modulation effect. There is no doubt the channel thermal noise will continue to be the dominant noise source for MOSFETs in future technologies. Hence, they need to be investigated and modelled properly in order to predict the high frequency noise performance of MOSFETs in strong inversion regime.

2.1.2 Flicker Noise

Flicker noise is produced due to the imperfections in manufacturing technology. It is also called $1/f$ noise as the noise spectral density is inversely proportional to the frequency. Flicker noise is larger in MOSFET due to the rougher Si/SiO₂ interface of MOSFET, which produce abundance of charge trapping defects and impurities. Larger MOSFET will produce lesser flicker noise because of the larger gate oxide capacitance that able to smooth the fluctuation in channel charge. Generally, flicker noise can be modeled in (2.3) [17, 20].

$$\overline{i_n^2} = \frac{K g_m^2}{f W L C_{ox}'} \Delta f \quad (2.3)$$

where K is a constant, g_m is the transconductance of the device, W is the device width, L is the device length and C_{ox}' is the gate oxide capacitance per unit area.

Flicker noise is the dominant source of noise for MOSFETs in lower frequency of kHz and MHz range [21]. Although the influence of flicker noise is expanding into hundreds of MHz for short channel MOSFETs, it is still much smaller than thermal noise in GHz range.

2.1.3 Shot Noise

When a DC current flows across a junction, carriers travel across potential barriers of the junction randomly and independently. The entry of a discrete unit of charges at the boundary of the barrier is independent of the arrival time of both the preceding and the succeeding unit. This discrete nature of electron cause random fluctuations of current, which results in the shot noise [7, 22]. It is also known as white noise since it is independent of frequency. Generally, shot noise can be modeled to be (2.4) [7, 22].

$$\overline{i_n^2} = 2q I_{DC} \Delta f \quad (2.4)$$

where q is the electron charge with $q = 1.6 \times 10^{-19} \text{ C}$, and I_{DC} is the DC current of the device.

The channel thermal noise dominates noise source of MOSFETs in strong inversion region, whereas the shot noise dominates noise source of MOSFETs in weak

inversion region [7, 17, 65, 66]. The characteristic is known to be similar to the bipolar junction transistor. In moderate inversion region, both of the channel thermal noise and the shot noise contribute to the total drain current noise [65].

2.2 Four Noise Parameters

Noise factor F of a circuit was first defined by Friis in 1940's [23], to be the signal-to-noise power ratio at input $(S/N)_{in}$ over the signal-to-noise power ratio at output $(S/N)_{out}$ of the circuit at the ambient temperature of 290K.

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} \quad (2.5)$$

Noise factor also can be expressed in dB, which is called noise figure NF.

$$NF(dB) = 10 \log_{10}(F) \quad (2.6)$$

As the signal flows through the system, the signal-to-noise power ratio of the system is degraded, which is described by the noise figure of the system. As a result, a low noise figure is desired since only little noise is added by the circuit itself when then signal passes through it.

Basically, the noise figure of the system is calculated based on the noise sources insides the system and the source admittance driving the system. Normally, the noise figure versus source admittance plot exhibits a parabolic shape at each frequency point for a linear system. This behavior can be characterized completely by the four noise parameters, which are the minimum noise factor F_{min} , the noise resistance R_n which can be used to determine the sensitivity of the noise figure when $Y_s \neq Y_{opt}$, and

optimum source admittance $Y_{opt} = G_{opt} + jB_{opt}$ where the minimum noise factor can be achieved. The relationship between the noise factor and the four noise parameters is indicated in (2.7) - (2.9) [24].

$$F = F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \quad (2.7)$$

$$F = F_{min} + \frac{4R_n}{Z_0} \cdot \frac{|\Gamma_{opt} - \Gamma_s|^2}{|1 + \Gamma_{opt}|^2 (1 - |\Gamma_s|^2)} \quad (2.8)$$

$$\Gamma_{opt} = \frac{1 - Z_0 Y_{opt}}{1 + Z_0 Y_{opt}} \quad (2.9)$$

where Y_s is the source admittance, Z_0 is the characteristic impedance which is usually at 50Ω , Γ_s is the source reflection coefficient, and Γ_{opt} is the optimum source reflection coefficient.

Since the four noise parameters are defined based on the intrinsic noise source of the system, it is also called intrinsic noise sources. To date, the four noise parameters are widely used in the RF circuit design and modeling since it is able to describe the noise performance of the system effectively. In the real design, low NF_{min} , R_n and small different between Y_s and Y_{opt} are important to obtain a good noise figure. A low noise figure is desired since only little noise is added by the circuit itself when the signal passes through it. Since the gate current noise source and the drain current noise source are correlated, there is an optimum value for source admittance, called Y_{opt} . A minimum noise figure is achieved when these two noise sources have maximum cancellation between each other. In addition, when the source admittance Y_s shifts away from the Y_{opt} , the noise figure becomes larger. Thus, a small difference between

Y_s and Y_{opt} is desired. Since the noise resistance R_n determines how fast noise figure increases when source admittance Y_s shifts away from Y_{opt} , the low R_n is desired also, to obtain low sensitivity to source noise impedance mismatch.

2.2.1 Derivation of Four Noise Parameters

Figure 2.1 illustrates the circuit used in the noise figure calculation in two-port network representation [20]. A noise source $\overline{i_s^2}$ is connected to a noisy network in the calculation of the noise in the calculation of the noise factor F of the network. The noisy network in Figure 2.1 can be represented by a noiseless network with the noise voltage $\overline{v_n^2}$ and the noise current $\overline{i_n^2}$ at the input of the noiseless network. In fact, the noise current $\overline{i_n^2}$ contents two components, i_c and i_u , which are correlated with v_n and uncorrelated with v_n respectively. The noise factor F is determined by the noise sources and the source admittance Y_s , as shown in (2.10) – (2.14) [20].

Figure 2.1 Circuit for noise factor calculation in two-port network configuration [20].

$$F = \frac{\overline{i_s^2} + |\overline{i_n} + Y_s \overline{v_n}|^2}{\overline{i_s^2}} \quad (2.10)$$

Substitute i_n with $i_c + i_u$,

$$F = 1 + \frac{\overline{[(i_c + i_u) + Y_s v_n]^2}}{\overline{i_s^2}}. \quad (2.11)$$

The component i_c is correlated with v_n , and thus replacing i_c with $Y_c v_n$ yields

$$F = 1 + \frac{\overline{[(Y_c v_n + i_u) + Y_s v_n]^2}}{\overline{i_s^2}}. \quad (2.12)$$

Since i_u is uncorrelated with v_n , (2.12) can be written as (2.13).

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{v_n^2}}{\overline{i_s^2}} \quad (2.13)$$

Expanding the complex variable Y_c and Y_s , (2.13) becomes (2.14).

$$F = 1 + \frac{\overline{i_u^2} + [(G_c + G_s)^2 + (B_c + B_s)^2] \overline{v_n^2}}{\overline{i_s^2}} \quad (2.14)$$

where $Y_c = G_c + jB_c$ is the correlation admittance. Defining the noise sources $\overline{i_s^2}$, $\overline{i_u^2}$ and $\overline{v_n^2}$ in the thermal noise form in (2.15) – (2.17), and substitute (2.15) – (2.17) into (2.14), (2.18) can be derived [20].

$$\overline{i_s^2} = 4kT\Delta f G_s \quad (2.15)$$

$$\overline{i_u^2} = 4kT\Delta f G_u \quad (2.16)$$

$$\overline{v_n^2} = 4kT\Delta f R_n \quad (2.17)$$

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_n}{G_s} \quad (2.18)$$

In order to obtain the minimum noise factor, (2.18) is differentiated with respect to the source admittance Y_s , and Y_s become Y_{opt} when $\frac{\partial F}{\partial Y_s} = 0$. By substituting (2.22) into (2.18), the noise factor can be derived to be (2.24) and further rearrange to be (2.27) [20].

$$\frac{\partial F}{\partial B_s} = \frac{2(B_c + B_s)R_n}{G_s} \quad (2.19)$$

$$B_{opt} = -B_c \quad (2.20)$$

$$\frac{\partial F}{\partial G_s} = \frac{-G_u - [G_c^2 - G_s^2 + (B_c + B_s)^2]R_n}{G_s^2} \quad (2.21)$$

$$G_u = [G_{opt}^2 - G_c^2 - (B_c + B_{opt})^2]R_n \quad (2.22)$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \quad (2.23)$$

$$F = 1 + \frac{(G_{opt}^2 - G_c^2)R_n + (G_c + G_s)^2 R_n}{G_s} + \frac{[(B_c + B_s)^2]R_n}{G_s} \quad (2.24)$$

$$F = 1 + \frac{(G_{opt}^2 - G_c^2)R_n + [(G_c + G_{opt}) + (G_s - G_{opt})]^2 R_n}{G_s} + \frac{[(B_c + B_{opt}) + (B_s - B_{opt})]^2 R_n}{G_s} \quad (2.25)$$

$$F = 1 + \frac{[-(G_c + G_{opt})^2 + 2G_{opt}^2 + 2G_{opt}G_c]R_n + [(G_c + G_{opt})^2 + (G_s - G_{opt})^2 + 2(G_c + G_{opt})(G_s - G_{opt})]R_n}{G_s} + \frac{[(B_c + B_{opt}) + (B_s - B_{opt})]^2 R_n}{G_s} \quad (2.26)$$

$$F = 1 + 2R_n(G_c + G_{opt}) + \frac{[(G_s - G_{opt})^2 + (B_s - B_{opt})^2]R_n}{G_s} \quad (2.27)$$

The minimum noise factor can be achieved when $Y_s = Y_{opt}$, and the noise factor can be further simplified to be (2.29) [20].

$$F_{min} = 1 + 2R_n(G_c + G_{opt}) \quad (2.28)$$

$$F = F_{min} + \frac{|Y_s - Y_{opt}|^2 R_n}{G_s} \quad (2.29)$$

2.2.2 Drain Current Noise and Gate Current Noise Power Spectral Density with Four Noise Parameters

The relationship between the noise correlation matrix C_A and the four noise parameters can be written as [20]

$$C_A = 2kT \begin{bmatrix} R_n & \frac{NF_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{NF_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \quad (2.30)$$

where $Y_{opt} = \frac{1}{Z_0} \left(\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \right)$ and Y_{opt}^* is the complex conjugate of Y_{opt} . Z_0 is normally at 50Ω .

The noise correlation matrix C_A can be transformed into its admittance representation C_Y by the matrix operation of (2.31) [20, 25].

$$C_Y = T_Y C_A T_Y' \quad (2.31)$$

where T_Y' is the complex conjugate transpose of T_Y given by (2.32).

$$T_Y = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} \quad (2.32)$$

In (2.32), Y_{11} and Y_{21} are the two-port admittance parameters. The general two-port network and the Y-parameter analysis are demonstrated in Appendix C.

(2.33) to (2.38) show the steps of performing the matrix operation of (2.31).

Each of the elements of matrix C_Y is related to the four noise parameters and Y-parameters to be (2.35), (2.36), (2.37) and (2.38) respectively [20, 25].

$$C_Y = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} \cdot 2kT \begin{bmatrix} R_n & \frac{NF_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{NF_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \cdot \begin{bmatrix} -Y_{11}^* & -Y_{21}^* \\ 1 & 0 \end{bmatrix} \quad (2.33)$$

$$C_Y = \begin{bmatrix} C_{Y11} & C_{Y12} \\ C_{Y21} & C_{Y22} \end{bmatrix} \quad (2.34)$$

$$C_{Y11} = 2kT \left[|Y_{11}|^2 R_n - Y_{11}^* \left(\frac{NF_{min}-1}{2} - R_n Y_{opt} \right) - Y_{11} \left(\frac{NF_{min}-1}{2} - R_n Y_{opt}^* \right) + R_n |Y_{opt}|^2 \right] \quad (2.35)$$

$$C_{Y21} = 2kT \left[-Y_{11}^* Y_{21} R_n - Y_{21} \left(\frac{NF_{min}-1}{2} - R_n Y_{opt}^* \right) \right] \quad (2.36)$$

$$C_{Y12} = 2kT \left[-Y_{21}^* \left(-Y_{11} R_n + \frac{NF_{min}-1}{2} - R_n Y_{opt} \right) \right] \quad (2.37)$$

$$C_{Y22} = 2kT |Y_{21}|^2 R_n \quad (2.38)$$

The drain current noise power spectral density S_{i_d} , the gate current noise power spectral density S_{i_g} and their correlation term of $S_{i_g i_d}^*$ can be computed from the noise correlation matrix C_Y by the following equations [20, 25].

$$S_{i_d} = 2C_{Y22} = 4kT |Y_{21}|^2 R_n \quad (2.39)$$

$$S_{i_g} = 2C_{Y11} = 4kT \left[|Y_{11}|^2 R_n - Y_{11}^* \left(\frac{NF_{min}-1}{2} - R_n Y_{opt} \right) \right]$$

$$-Y_{11} \left(\frac{NF_{min}-1}{2} - R_n Y_{opt}^* \right) + R_n |Y_{opt}|^2 \Big] \quad (2.40)$$

$$Y_{cor} = \frac{NF_{min}-1}{2R_n} - Y_{opt} \quad (2.41)$$

$$S_{i_g} = 4kTR_n \left[|Y_{11}|^2 + |Y_{opt}|^2 - (Y_{11}^* Y_{cor} + Y_{11} Y_{cor}^*) \right] \quad (2.42)$$

$$S_{i_g} = 4kTR_n \left[|Y_{11}|^2 + |Y_{opt}|^2 - 2\Re(Y_{11} Y_{cor}^*) \right] \quad (2.43)$$

$$S_{i_g i_d^*} = 2C_{Y12} = 4kT \left[-Y_{21}^* \left(-Y_{11} R_n + \frac{NF_{min}-1}{2} - R_n Y_{opt} \right) \right] \quad (2.44)$$

$$S_{i_g i_d^*} = 4kT (Y_{11} - Y_{cor}) R_n Y_{21}^* \quad (2.45)$$

2.3 Channel Thermal Noise Models for MOSFETs

For MOSFETs operating in GHz range, there are a few ways to represent the high frequency noise of MOSFETs. One of the well-known configurations is the van der Ziel's approach [7], as shown in the Figure 2.2.

Figure 2.2 Van der Ziel representation of high frequency noise in MOSFET [7].

In Figure 2.2, S_{i_d} is the total drain current noise power spectral density in A^2/Hz , and S_{i_g} is the total gate current noise in A^2/Hz , and they are partially correlated.

To date, the drain current noise is assumed to be the same as the channel thermal noise [2, 3, 5-13, 15-17], and thus S_{i_d} is the channel thermal noise in [2, 3, 5-13, 15-17]. The channel thermal noise is well-known to be the dominant source of noise for MOSFETs operating in high frequency of GHz regime [2, 3, 5-13, 15-17].

2.3.1 Klaassen-Prins Equation

The channel thermal noise for long channel MOSFETs has been characterized by F. M. Klaassen and J. Prins [26] in 1967, with the Klaassen-Prins equation [27]. In the current-voltage model, the drain current is expressed by the non quasi-static one-dimensional DC differential equation, as shown in (2.46).

$$I_{DS} = g(V_y) \frac{dV_y}{dy} \quad (2.46)$$

In (2.46), V_y is the surface potential along the channel at distance y from the source, in such that V_y is 0 at the source terminal and gradually increases to V_{DS} at the drain terminal, and $g(V_y)$ is the local channel conductivity, which can be expressed by (2.47) for MOSFETs.

$$g(V_y) = \mu C'_{ox} W (V_{GT} - \alpha V_y) \quad (2.47)$$

where μ is the carrier mobility, C'_{ox} is oxide capacitance per unit area, W is the channel width of the MOSFET, α is the bulk charge effect coefficient, $V_{GT} = V_{GS} - V_{TH}$ with V_{GS} is the gate-source voltage, and V_{TH} is the threshold voltage.

The local fluctuation in the channel will cause a small voltage change Δv on the channel voltage V_y , and this will cause a small current change Δi_{ds} flowing through the device. In order to model the local fluctuation, it is important to understand the origin that causes the noise. Thereafter, the transfer of the local fluctuation to the drain terminal of the MOSFET is determined [17].

In the derivation of the channel thermal noise spectral density of MOSFET, the Langevin equation with a zero average current noise source i_n is introduced. After adding the small current change Δi_{ds} , the small voltage change Δv and the Langevin noise source i_n into (2.46), (2.48) can be obtained.

$$I_{DS} + \Delta i_{ds} = g(V_y + \Delta v) \frac{d(V_y + \Delta v)}{dy} + i_n \quad (2.48)$$

In (2.48), only the small signal components are involved in the noise calculation. Hence, the small current change Δi_{ds} can be derived to be (2.49).

$$\Delta i_{ds} = g(V_y) \frac{d(\Delta v)}{dy} + \frac{dg}{dV_y} \Delta v \frac{dV_y}{dy} + i_n = \frac{d}{dy} [g(V_y) \Delta v] + i_n \quad (2.49)$$

By integrating over the whole channel and considering the boundary condition of $\Delta v(0) = \Delta v(L) = 0$, (2.49) becomes (2.50).

$$\Delta i_{ds} = \frac{1}{L} \int_0^L i_n dy \quad (2.50)$$

As the current noise is averagely zero, the channel thermal noise spectral density can be derived to be

$$S_{i_d} = \frac{\overline{\Delta i_{ds} \Delta i_{ds}^*}}{\Delta f} = \frac{1}{L^2} \int_0^L \int_0^L \overline{i_n i_n^*} dy dy' \quad (2.51)$$

where Δf is the bandwidth of the noise measured.

The thermal noise or Nyquist theory [19] is applied in the development of the Klaassen-Prins equation. The gradual channel region of MOSFET is split into smaller sections with the length of dy , as illustrated in Figure 2.3.

Figure 2.3 Cross section of MOSFET, with the gradual channel region of MOSFET split into smaller sections of length dy .

In Figure 2.3, it is assumed that each small section with the length dy acts as a resistor with the value ΔR . Hence, the local current fluctuation $\overline{i_n i_n^*}$ can be calculated using the Nyquist theory [19].

$$\overline{i_n i_n^*} = 4kTg(V_y)\Delta f\delta(y - y') \quad (2.52)$$

where δ is the Dirac delta function. The channel thermal noise spectral density S_{i_d} of (2.53) [26, 27] can be obtained by substituting (2.52) into (2.51).

$$S_{i_d} = \frac{4kT}{L^2} \int_0^L g(V_y) dy = \frac{4kT}{I_{DS}L^2} \int_{V_0}^{V_L} g^2(V_y) dV_y \quad (2.53)$$

Nevertheless, the drawback of the Klaasen-Prins equation of (2.53) is that it consists of complicated integration steps.

2.3.2 Tsividis' Thermal Noise Model

Compared to the Klaasen-Prins equation, Tsividis' model [17] is much simpler. In Tsividis' thermal noise model [17], two assumptions are made, in which the carrier mobility is constant along the channel and the velocity saturation effect is negligible. With these assumptions, the drain current equation can be expressed as

$$I_{DS} = -\mu W Q'_I(y) \frac{dv_y}{dy} \quad (2.54)$$

where y is the direction along the channel, and Q'_I is the inversion layer charge per unit area with $Q'_I < 0$. By integrating (2.54) from source side to drain side, (2.55) can be obtained.

$$I_{DS} = -\frac{W}{L} \mu \int_{V_{SB}}^{V_{DB}} Q'_I(V_y) dV_y \quad (2.55)$$

where L is the device channel length.

The gradual channel region of MOSFET is split into smaller sections with the length of Δy , which centered around $y = y_1$. It is assumed that each small section with the length Δy acts as a resistor with the value ΔR . With $\Delta V_y = I_{DS} \Delta R$,

$$\Delta R = \frac{\Delta y}{-\mu W Q'_I(V_y)}. \quad (2.56)$$

Together with the Nyquist theory [20] and the thermal noise theory in section 2.1.1, the small voltage noise Δv across the resistor ΔR can be written as (2.57).

$$\frac{\overline{(\Delta v)^2}}{\Delta f} = 4kT \Delta R = \frac{4kT \Delta y}{-\mu W Q'_I(V_y)} \quad (2.57)$$

This small voltage noise will cause a small current noise in the drain current, as illustrated in Figure 2.4 (a) and (b) [17].

Figure 2.4 Schematic for the noisy segment, with (a) is in Thevenin representation, and (b) is in its equivalent circuit of Norton representation [17]

From Figure 2.4, there are two transistors with length of y_1 and $L - y_1$ respectively. If the local voltage noise $\Delta v = 0$, the two transistors are connected together, in which is equivalent to a single transistor with length L . If the local voltage noise $\Delta v \neq 0$, the drain bias of the transistor with length $L - y_1$ at the right side and the source bias of the transistor with length y_1 at the left side will be disturbed. This will cause a different potential distribution along the channel for these two transistors. Thus the drain current will be affected as well. Let the new drain current to be $I_{DS} + \Delta i_{ds}$, (2.55) can be written as (2.58) and (2.59) respectively [17].

$$I_{DS} + \Delta i_{ds} = -\frac{W}{y_1} \mu \int_{V_{SB}}^{V_1} Q'_I(V_y) dV_y \quad (2.58)$$

$$I_{DS} + \Delta i_{ds} = -\frac{W}{L-y_1} \mu \int_{V_1+\Delta v}^{V_{DB}} Q'_I(V_y) dV_y \quad (2.59)$$

where V_1 is the point that voltage starts to fluctuate. With the assumption of Δv is very small, (2.60) can be derived.

$$I_{DS} + \Delta i_{ds} = -\frac{W}{L} \mu \int_{V_{SB}}^{V_{DB}} Q'_I(V_y) dV_y + \frac{W}{L} \mu Q'_I(V_y) \Delta v \quad (2.60)$$

As only the small signal components are involved in the noise calculation, the current noise can be written as

$$\Delta i_{ds} = g(V_y) \Delta v = \frac{W}{L} \mu Q'_I(V_y) \Delta v \quad (2.61)$$

Based on Nyquist's theory [19], the contribution of the small section Δy at $y = y_1$ to the channel thermal noise is

$$\frac{\overline{(\Delta i_{ds})^2}}{\Delta f} = -4kT \frac{\mu}{L^2} W Q'_I(V_y) \Delta y. \quad (2.62)$$

The noise contribution from each section of the channel is assumed to be uncorrelated, in such that the total channel thermal noise power spectral density can be obtained by summing the noise from all these small sections in the channel. Thus, the channel thermal noise can be derived to be (2.64) [17].

$$S_{i_d} = \frac{\overline{i_{ds}^2}}{\Delta f} = \int_0^L \frac{\overline{(\Delta i_{ds})^2}}{\Delta f} = -4kT \frac{\mu}{L^2} \int_0^L W Q'_I(y) dy \quad (2.63)$$

$$S_{i_d} = 4kT \frac{\mu}{L^2} (-Q_{inv}) \quad (2.64)$$

The total inversion layer charge Q_{inv} is defined as [17]

$$Q_{inv} = W \int_0^L Q'_I(y) dy \quad (2.65)$$

where

$$dy = \frac{-\mu W}{I_{DS}} Q'_I(V_y) dV_y \quad (2.66)$$

$$Q'_I(V_y) = -C'_{ox} [V_{GB} - V_{SB} - V_{TH} - \alpha(V_y - V_{SB})]. \quad (2.67)$$

For strong inversion region approximation [17],

$$Q_{inv} = -WLC'_{ox}V_{GT} \left[\frac{2}{3} \left(\frac{1+\eta+\eta^2}{1+\eta} \right) \right] \quad (2.68)$$

with

$$\eta = \begin{cases} 1 - \frac{V_{DS}}{V_{DSat}}, & V_{DS} \leq V_{DSat} \\ 0, & V_{DS} > V_{DSat} \end{cases}. \quad (2.69)$$

The channel thermal noise model in [17] is developed for long channel MOSFETs in which the short channel effects such as velocity saturation and hot carrier effects are absent.

2.3.3 Van der Ziel's Model

Van der Ziel [7] has included the velocity saturation and the hot carrier effects in the Klaassen-Prins equation. The velocity saturation effect is included in the channel conductance $g(V_y)$ in the drain current equation.

$$I_{DS} = g(V_y) \frac{dV_y}{dy} = \mu W C'_{ox} (V_{GT} - \alpha V_y) \frac{\frac{E_y}{1 + \frac{E_y}{E_C}}}{1 + \frac{E_y}{E_C}} \quad (2.70)$$

$$g(V_y) = \mu W C'_{ox} (V_{GT} - \alpha V_y) - \frac{I_{DS}}{E_c} \quad (2.71)$$

where E_y is the lateral electric field, E_c is the critical electric field with $E_c = \frac{2v_{sat}}{\mu}$, and v_{sat} is the saturated velocity of the carrier.

In saturation region where $V_{DS} > V_{DSat}$, the hot carrier effect is taken into account in the channel thermal noise derivation, as shown in (2.72).

$$S_{id} = \frac{4kT}{L^2 I_{DSat}} \int_0^{V_{DSat}} \left(\frac{T_e}{T} \right) g^2(V_y) dV_y \quad (2.72)$$

where V_{DSat} is the drain saturation voltage, I_{DSat} is the drain saturation current, T is the device temperature, and T_e is the effective electron temperature along the channel. For MOSFETs, the effective electron temperature T_e increases as the electric field strength increases. Since the exact dependence between them still remains unknown till now, an approximation is made to simplify the calculation, in such that [7]

$$\frac{T_e}{T} = \left(1 + \frac{E_y}{E_c} \right)^n \quad \text{with } n = 0, 1, 2 \quad (2.73)$$

where n is accounted for the hot carrier effect. When $n = 0$, $T_e = T$ and the hot carrier effect is negligible. When $n = 1, 2$, the hot carrier effect is taken into consideration, with different dependence with the electric field strength.

Meanwhile, (2.70) is reorganized to obtained (2.74).

$$1 + \frac{E_y}{E_c} = \frac{\mu W C'_{ox} (V_{GT} - \alpha V_y)}{\mu W C'_{ox} (V_{GT} - \alpha V_y) - \frac{I_{DS}}{E_c}} \quad (2.74)$$

By substituting (2.71), (2.73) and (2.74) into (2.72), (2.75) can be derived.

$$S_{id} = \frac{4kT}{L^2 I_{DSat}} \int_0^{V_{DSat}} \mu W C'_{ox} (V_{GT} - \alpha V_y)^n \times \left[\mu W C'_{ox} (V_{GT} - \alpha V_y) - \frac{I_{DS}}{E_c} \right]^{2-n} dV_y \quad (2.75)$$

Eventually, the channel thermal noise spectral density can be characterized by [7, 28]

$$S_{i_d} = 4kT\gamma_{sat}g_{d0} \quad (2.76)$$

where

$$g_{d0} = \left[\mu C'_{ox} \left(\frac{W}{L} \right) \right]^2 \frac{V_{GT} \left[V_{GT} V_{DSat} - \frac{V_{DSat}^2}{2} \right]}{\left[1 + \frac{V_{DSat}}{E_{cL}} \right] I_{DSat}} = \mu C'_{ox} \left(\frac{W}{L} \right) V_{GT} \quad (2.77)$$

and γ_{sat} is different for different hot carrier effect or different n , as shown in (2.78) to (2.80).

$$\gamma_{sat} = \frac{1 - \frac{b}{a} + \frac{1}{3} \left(\frac{b}{a} \right)^2}{1 - \frac{1}{2} \left(\frac{b}{a} \right)} (1 + 2a)^{1/2} \quad (for\ n = 2) \quad (2.78)$$

$$\gamma_{sat} = \frac{1 - \frac{b}{a} + \frac{1}{3} \left(\frac{b}{a} \right)^2}{1 - \frac{1}{2} \left(\frac{b}{a} \right)} (1 + 2a)^{1/2} - b \left(1 - \frac{1}{2} \left(\frac{b}{a} \right) \right) \quad (for\ n = 1) \quad (2.79)$$

$$\gamma_{sat} = \frac{1 - \frac{b}{a} + \frac{1}{3} \left(\frac{b}{a} \right)^2}{1 - \frac{1}{2} \left(\frac{b}{a} \right)} (1 + 2a)^{1/2} - b \left(\frac{2+b}{1+b} \right) \left(1 - \frac{1}{2} \left(\frac{b}{a} \right) \right) \quad (for\ n = 0) \quad (2.80)$$

Here, a and b can be defined as (2.81) and (2.82).

$$a = \frac{V_{GS} - V_{TH}}{E_{cL}} \quad (2.81)$$

$$b = \frac{V_{DSat}}{E_{cL}} \quad (2.82)$$

2.3.4 Channel Length Modulation Effect (CLM): Model of Chen and Deen

Chen and Deen [3] include the channel length modulation effect in their channel thermal noise model calculation. The approach used in the model of Chen and Deen is based on the “two-section channel model” [3, 16, 29, 30], where the channel of

Figure 2.5 Schematic of the channel of MOSFET, which is partitioned into region I (gradual channel region) and region II (velocity saturation region) [3]

MOSFET is partitioned into two regions. Region I is the gradual channel region and region II is the velocity saturation region, as illustrated in Figure 2.5.

From Figure 2.5, the total channel length L of the MOSFET is approximated to be the drawn channel length L_{drawn} . The length of the gradual channel region L_{eff} and the length of the velocity saturation region ΔL can be determined by (2.83) to (2.88) [31].

$$L_{eff} = L - \Delta L \quad (2.83)$$

where

$$\Delta L = \frac{1}{\alpha_y} \ln \left[\frac{\alpha_y(V_{DS} - V_{DSat}) + E_D}{E_c} \right] \quad (2.84)$$

with

$$E_D = E_c \sqrt{1 + \left[\frac{\alpha_y(V_{DS} - V_{DSat})}{E_c} \right]^2} \quad (2.85)$$

$$\alpha_y = \lambda \sqrt{\frac{3}{2} \frac{C'_{ox}}{x_j \epsilon_{si} \epsilon_0}} \quad (2.86)$$

$$E_c = \frac{2v_{sat}}{\mu_{eff}} \quad (2.87)$$

Here, x_j is the junction depth of drain and source, λ is a fitting parameter to account for channel length modulation effect, and μ_{eff} is the effective mobility of the carrier.

In the model of Chen and Deen [3], it is assumed that the lateral electric field of each small section in Region I is much smaller than the critical electric field. Hence, the local mobility is approximated to be the effective mobility μ_{eff} and the velocity saturation effect near the boundary of region I and II is assumed to be negligible [3].

In the gradual channel region (region I), the Nyquist theory [19] is applied in the derivation of the channel thermal noise model, in such that the mean square value of the current noise contributed by the channel resistance ΔR of a section Δy at the position y_1 can be written as [32]

$$\overline{\Delta i_{ds}(y_1)^2} = g_{DS}^2(y_1) \cdot \overline{\Delta v(y_1)^2} = g_{DS}^2(y_1) \cdot 4kT(y_1) \Delta R(y_1) \Delta f \quad (2.88)$$

$$\overline{\Delta i_{ds}(y_1)^2} = - \frac{4kT(y_1) \Delta f W \mu_{eff} Q(y_1) \Delta y}{L_{eff}^2} \quad (2.89)$$

with

$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c V_{BS}) \left(\frac{V_{GS} + 2V_{TH}}{T_{ox}} \right) + U_b \left(\frac{V_{GS} + 2V_{TH}}{T_{ox}} \right)^2} \quad (2.90)$$

where μ_0 is low field mobility, T_{ox} is the oxide thickness, and U_a , U_b , U_c are mobility model parameters.

Besides, the hot carrier effect also being taken into account by relating the electron temperature T_e and lattice temperature T with

$$T_e(y_1) = T \left[1 + \delta \left(\frac{E_y(y_1)}{E_c} \right)^2 \right] \quad (2.91)$$

where δ is fitting parameter, and $E_y(y_1)$ is the lateral electric field at position y_1 . The total drain current noise spectral density S_{i_d} for the gradual channel region can be derived to be

$$S_{i_d} = \frac{\overline{i_{ds}^2}}{\Delta f} = -\frac{4kT}{L_{eff}^2} \times \int_0^{L_{elec}} \left[1 + \delta \left(\frac{E_y(y_1)}{E_c} \right)^2 \right] W \mu_{eff} Q(y_1) dy \quad (2.92)$$

$$S_{i_d} = \frac{4kT}{L_{eff}^2} \mu_{eff} (-Q_{inv}) + \delta \frac{4kT I_{DS}}{L_{eff}^2 E_c^2} V_{DSat} \quad (2.93)$$

where Q_{inv} is the total inversion layer charge in the gradual channel region. When the device operates in linear mode, the L_{eff} will become L and the V_{DSat} will become V_{DS} in the total drain current noise spectral density equation of (2.93).

On the other hand, Chen and Deen [3] also pointed out that the velocity saturation region (region II) does not contribute to the total channel thermal noise. Two reasons were given to support their view. Firstly, Nyquist theory is not applicable in this region. This is because Ohm's law cannot be applied in this region which cause the

local resistance ΔR cannot be defined. Thus, there will be no thermal noise contribution from the velocity saturation region to the total channel thermal noise. The fact that thermal noise theory fails in this region, leads to explorations of other noise mechanisms, such as drifting-dipole noise [9] and diffusion noise [67, 68]. However, since the carriers in this region travel at their saturated velocity, they will not respond to the electric field fluctuation caused by noise proposed in [9, 67, 68]. This is the second reason given by [3] explaining why the velocity saturation region does not contribute to the total channel thermal noise.

In conclusion, the total channel thermal noise spectral density is only contributed by the gradual channel region, as shown in (2.94).

$$S_{i_d\text{-total}} = S_{i_d\text{-regionI}} = \frac{4kT}{L_{eff}^2} \mu_{eff} (-Q_{inv}) + \delta \frac{4kT I_{DS}}{L_{eff}^2 E_c^2} V_{DSat} \quad (2.94)$$

The second term of (2.94) is accounted for the hot carrier effect. However, δ is found to be zero experimentally in [3]. As a result, according to [3], the hot carrier effect is negligible in the channel thermal noise model calculation, which agree with [15]. Eventually, the final expression for total channel thermal noise is shown in (2.95).

$$S_{i_d} = \frac{4kT}{L_{eff}^2} \mu_{eff} (-Q_{inv}) \quad (2.95)$$

2.3.5 Velocity Saturation and Hot Carrier Effects

Besides the channel length modulation effect (CLM), the other two short channel effects that drawn much attentions are the velocity saturation effect (VSE) and the hot carrier effect (HCE). Many publications have been generated to include the

velocity saturation effect [2, 5-10] and the hot carrier effect [2, 6, 7, 10-13] into the channel thermal noise model. Generally, channel length modulation effect is included in the above mentioned publications.

Some publications [5, 8] claimed that the velocity saturation effect is important in the channel thermal noise model derivations, and the hot carrier effect is negligible. In [8], the channel thermal noise model is derived based on the Tsividis' thermal noise model [17], claiming that the long channel noise model can be used for short channel MOSFETs by substituting the total channel length L with the effective channel length of gradual channel region L_{eff} , and the constant mobility μ with the effective mobility μ_{eff} .

$$S_{i_d} = \begin{cases} 4kT \frac{\mu}{L^2} Q_{inv} & \text{for long channel} \\ 4kT \frac{\mu_{eff}}{L_{eff}^2} Q_{inv} & \text{for short channel} \end{cases} \quad (2.96)$$

Here, the velocity saturation effect is taken into account in the total inversion layer charge Q_{inv} calculation, which is different from the Tsividis' thermal noise model [8].

$$Q_{inv} = \int_0^L W Q'_I(y) dy = \frac{W^2 \mu_{eff}}{I_{DS}} \int_0^{V_{DS}} (Q'_I)^2 dV_y - \frac{W}{E_c} \int_0^{V_{DS}} Q'_I dV_y \quad (2.97)$$

$$Q_{inv} = \frac{W^2 \mu_{eff} C_{ox}^2}{I_{DS}} \left[V_{GT}^2 V_{DS} - \alpha V_{GT} V_{DS}^2 + \frac{\alpha^2}{3} V_{DS}^3 \right] - \frac{W C_{ox}}{E_c} \left[V_{GT} V_{DS} - \frac{\alpha}{2} V_{DS}^2 \right] \quad (2.98)$$

The channel thermal noise can be derived to be (2.99) for the triode region and (2.100) for the saturation region [8].

$$S_{i_d} = 4kT \mu_{eff}^2 C_{ox}^2 \frac{W^2}{L^2 I_{DS}} \left[V_{GT}^2 V_{DS} - \alpha V_{GT} V_{DS}^2 + \frac{\alpha^2}{3} V_{DS}^3 \right] - 4kT \frac{W C_{ox}' \mu_{eff}}{L^2 E_c} \left[V_{GT} V_{DS} - \frac{\alpha}{2} V_{DS}^2 \right] \quad (2.99)$$

$$S_{i_d} = 4kT \mu_{eff}^2 C_{ox}'^2 \frac{W^2}{L_{eff}^2 I_{DS}} \left[V_{GT}^2 V_{DSat} - \alpha V_{GT} V_{DSat}^2 + \frac{\alpha^2}{3} V_{DSat}^3 \right] - 4kT \frac{WC_{ox}' \mu_{eff}}{L_{eff}^2 E_c} \left[V_{GT} V_{DSat} - \frac{\alpha}{2} V_{DSat}^2 \right] \quad (2.100)$$

On the other hand, [5] considered the velocity saturation effect in the current-voltage and noise model. They derived the lateral electric field E_y from the drain current equation of (2.101).

$$I_{DS} = \mu_{eff} W C_{ox} (V_{GT} - \alpha V_y) \frac{E_y}{1 + \frac{E_y}{E_c}} = \mu_{eff} W C_{ox} (V_{GT} - \alpha V_y) \frac{\frac{dV_y}{dy}}{1 + \frac{dV_y}{E_c dy}} \quad (2.101)$$

$$V_y = \frac{1}{2\alpha} \left[2(V_{GT} - V_0) - [(2V_{GT} - V_0)^2 - 4\alpha E_c V_0 y]^{\frac{1}{2}} \right] \quad (2.102)$$

$$V_0 = \frac{I_{DS}}{W C_{ox}' v_{sat}} \quad (2.103)$$

$$E_y = \frac{dV_y}{dy} = \frac{E_c V_0}{[(2V_{GT} - V_0)^2 - 4\alpha E_c V_0 y]^{\frac{1}{2}}} \quad (2.104)$$

In [5], Asgaran *et al.* derived their channel thermal noise model using the Nyquist theory [19]. The channel thermal noise model can be derived to be (2.107) in linear regime and (2.108) in saturation regime [5].

$$S_{i_d} = 4kT \int_0^{L_{eff}} g^2(V_y) dR \quad (2.105)$$

$$g(V_y) = \frac{\mu_{eff} W C_{ox}' (V_{GT} - \alpha V_y)}{L_{eff}} \cdot \frac{1}{1 + \frac{E_y}{E_c}} \quad (2.106)$$

$$S_{i_d} = 4kT \frac{4V_{GT}^2 + V_0^2 - 2V_0 V_{GT}}{3V_{GT}^2 (V_{GT} - V_0)} \alpha I_{DS} \quad (2.107)$$

$$S_{i_d} = 4kTI_{DS} \left[\frac{1}{V_{DSat}} + \frac{\alpha^2 V_{DSat}}{3V_{GT}^2} \right] \quad (2.108)$$

Nevertheless, some publications [11-13] claimed that hot carrier effect is crucial in the channel thermal noise model derivation. In [12], Peter Klein assumed that the carriers are in thermal equilibrium for long channel MOSFET, and the channel thermal noise model is

$$S_{i_d} = 4kT \frac{\mu_{eff} Q_I}{L^2} \quad (2.109)$$

with

$$Q_I = WLC'_{ox} V_{GT} \frac{1+\eta^2/3-\eta}{1-\eta/2} \quad (2.110)$$

$$\eta = \frac{A_{bulk}(\psi_{SL}-\psi_{S0})}{V_{GT}} \quad (2.111)$$

where A_{bulk} is the correction factor for the linearized bulk charge, ψ_{S0} and ψ_{SL} are the surface potential at source side and drain side respectively. However, the thermal equilibrium condition is not hold for short channel devices due to the increasing of the lateral electric field E_y with decreasing of the channel length. Thus, an equivalent noise temperature T_e [33] is introduced to represent the hot carrier effect in the noise model.

$$T_e = T + \frac{2}{3k} q \bar{v} \tau_e E_y \quad (2.112)$$

Here, q is the charge, $\bar{v}$ is the average drift velocity, and τ_e is the energy relaxation time. At high electric field where $\bar{v} \approx v_{sat}$, (2.112) can be written as (2.113).

$$T_e \approx T + \frac{2}{3k} q v_{sat} \tau_e E_y \quad (2.113)$$

According to [12], the difference between (2.112) and (2.113) is insignificant.

Applying (2.113) in the channel thermal noise model yields

$$S_{i_d} = 4kT \frac{\mu_{eff} Q_I}{L^2} + \frac{8}{3} q v_{sat} \tau_e \frac{1}{L} I_{DS} \quad (2.114)$$

with v_{sat} is typically at 10^5 m/s and τ_e is assumed to be in the order of 10^{-12} s [33].

There are also some publications [6, 7, 10] that include both velocity saturation effect and hot carrier effect in their models. In [6], J. Jeon *et al.* defined the local current noise source to be

$$\overline{\Delta i_n^2} = 4q D_n (-Q'_I) \cdot \frac{W}{\Delta y} \cdot B \quad (2.115)$$

where D_n is the noise diffusion coefficient, and B is the bandwidth. In the presence of high electric field in short channel MOSFETs, the small sections in the channel are no longer in thermal equilibrium. However, J. Jeon *et al.* [6] utilized the Einstein's-like relation, which is only valid when the carriers are in thermal equilibrium [28], such that

$$D_n = \left(\frac{kT_n}{q} \right) \mu'_n \quad (2.116)$$

where μ'_n is the AC mobility of carrier, and T_n is the noise temperature, which is assumed to be the same as the carrier temperature T_e . Hence, the local current noise source can be derived to be (2.117) and the local voltage noise source can be derived to be (2.118).

$$\overline{\Delta i_n^2} = 4kT_e \frac{(-Q'_I) W \mu'_n}{\Delta y} \cdot B = 4kT_e g_{ac} B \quad (2.117)$$

$$\overline{\Delta v_n^2} = \frac{\overline{\Delta i_n^2}}{g_{ac}^2} = 4kT_e \frac{1}{g_{ac}} B \quad (2.118)$$

In the derivation of channel thermal noise model, J. Jeon *et al.* include the local noise source in the similar way with [17].

$$I_{DS} + \Delta i_{ds} = \frac{-\frac{W}{y_1} \mu_{eff} \int_0^{V_1} Q'_I(V_y) dV_y}{1 + \frac{V_1/y_1}{E_c}} \quad (2.119)$$

$$I_{DS} + \Delta i_{ds} = \frac{-\frac{W}{L_{eff}-y_1} \mu_{eff} \int_{V_1+\Delta v_n}^{V_{DS}} Q'_I(V_y) dV_y}{1 + \frac{[V_{DS}-(V_1+\Delta v_n)]/(L_{eff}-y_1)}{E_c}} \quad (2.120)$$

$$\Delta i_{ds} = \frac{1}{L_{eff}+V_{DS}/E_c} \cdot \frac{W \mu_{eff} Q'_I(V_y)}{1+E_y/E_c} \cdot \Delta v_n \quad (2.121)$$

Together with the hot carrier effect [7], the total channel thermal noise can be obtained by summing the local noise source over the entire channel.

$$S_{i_d} = \frac{-4kT_0}{(L_{eff}+V_{DS}/E_c)^2} \int_0^{L_{eff}} \left(\frac{T_e}{T} \right) \times W \mu_{eff} Q'_I(y) dy \quad (2.122)$$

By defining $\beta = 1 + \frac{V_{DS}}{E_c L_{eff}}$, $V_{GT} = V_{GS} - V_{TH}$, and $V_0 = \frac{I_{DS}}{WC_{ox}v_{sat}}$, three cases can be obtained by considering different hot carrier effect on carriers [7].

a) When $n = 2$,

In linear region:

$$S_{i_d} = 4kT \frac{1}{\beta^2} \cdot \frac{4V_{GT}^2 + 10V_0^2 + 7V_0V_{GT} + \frac{3}{2} \left(\frac{V_0^3}{V_{GT}} \right) - V_0 \ln \left(\frac{|2V_{GT}-V_0|}{V_0} \right)}{3V_{GT}^2(V_{GT}-V_0)} \alpha I_{DS} \quad (2.123)$$

In saturation region:

$$S_{i_d} = 4kT \cdot \frac{4V_{GT}^2 + 10V_0^2 + 7V_0V_{GT} + \frac{3}{2} \left(\frac{V_0^3}{V_{GT}-V_0 \ln(|2V_{GT}-V_0|/V_0)} \right)}{3(V_{GT}-V_0)(V_{GT}+V_0)^2} \alpha I_{DS} \quad (2.124)$$

b) When $n = 1$,

In linear region:

$$S_{i_d} = 4kT \frac{1}{\beta^2} \cdot \frac{4V_{GT}^2 + 4V_0^2 + 4V_0V_{GT}}{3V_{GT}^2(V_{GT} - V_0)} \alpha I_{DS} \quad (2.125)$$

In saturation region:

$$S_{i_d} = 4kT \cdot \frac{4V_{GT}^2 + 4V_0^2 + 4V_0V_{GT}}{3(V_{GT} - V_0)(V_{GT} + V_0)^2} \alpha I_{DS} \quad (2.126)$$

c) When $n = 0$,

In linear region:

$$S_{i_d} = 4kT \frac{1}{\beta^2} \cdot \frac{4V_{GT}^2 + V_0^2 + V_0V_{GT}}{3V_{GT}^2(V_{GT} - V_0)} \alpha I_{DS} \quad (2.127)$$

In saturation region:

$$S_{i_d} = 4kT \cdot \frac{4V_{GT}^2 + V_0^2 + V_0V_{GT}}{3(V_{GT} - V_0)(V_{GT} + V_0)^2} \alpha I_{DS} \quad (2.128)$$

2.3.6 Summary of Existing Models and their Drawbacks

In general, the existing channel thermal noise models are derived based on the basic theory by Klaassen-Prins [26], with additional short channel effects such as channel length modulation, velocity saturation and hot carrier effects. When considering only the channel length modulation effect, model of Chen and Deen [3] assumed that the velocity saturation effect is negligible. Meanwhile, the hot carrier effect is included in their model derivation, and thereafter claimed to be negligible experimentally by [3]. However, the assumption in [3] which ignores the velocity

saturation effect is questionable. The total inversion layer charge Q_{inv} in BSIM4 [32, 40] is used in [3], where the velocity saturation effect is included. This contradicts with their previous assumption.

In [8], the authors claimed that the long channel noise model derived based on the Tsividis' thermal noise model [17], can be used for short channel MOSFETs, by substituting the total channel length L with effective channel length of gradual channel region L_{eff} , the constant mobility μ with the effective mobility μ_{eff} , and the long channel total inversion layer charge Q_{inv} with the short channel Q_{inv} . In [8], the short channel Q_{inv} was derived from the current equation with the velocity saturation effect. Similarly, [5] considered the velocity saturation effect in the drain current equations only, and substituted the corresponding short channel lateral electric field E_y into the long channel Klaassen-Prins equation. Nevertheless, it is inappropriate to replace the parameters with velocity saturation effect into the long channel noise model, without re-derived the noise model.

In order to take into account the hot carrier effect into channel thermal noise model, an equivalent noise temperature T_e is introduced, since the thermal equilibrium condition is no longer hold for short channel devices. In [12], T_e is introduced to include the average drift velocity and energy relaxation time, which is different from van der Ziel's model. Moreover, it is not clear on how to determine the energy relaxation time accurately.

On the other hand, there is publication such as [6], where all these three short channel effects are included in their channel thermal noise model. However, the

introduction of AC carrier mobility μ'_n and ac conductance g_{ac} in the channel thermal noise derivation is questionable.

In summary, it can be seen that the proper way to include the short channel effects in the channel thermal noise model still remains controversial. Hence, it is important to study the impact of short channel effects such as channel length modulation, velocity saturation and hot carrier effects on channel thermal noise model in detailed. After that, physical based silicon verified channel thermal noise model is desired, which leads to the works in Chapter 3.

2.4 Measurement and De-embedding

The on-wafer high frequency noise measurement [34-36] was performed using ATN NP5B Microwave Noise Parameter System. The frequency range measured is from 5 GHz to 25 GHz for high frequency noise characterization. The device under test (DUT) structures were NMOS transistors fabricated using GLOBALFOUNDRIES' 0.13 μm RFCMOS technology process, with gate bias of 0.4 V to 1.2 V and drain bias of 0 V to 1.2 V. From the measurement, S-parameters and four noise parameters [36] were obtained for each operating frequencies and biasing conditions. The measured data obtained is de-embedded using the DUT and OPEN structures [2], to minimize the parasitic errors of interconnects and pads [2, 37].

Firstly, the measured S-parameters were converted to Y-parameters for both the DUT and OPEN structures. Y-parameter de-embedding [2] is performed in order to obtain the intrinsic Y-parameters for noise calculation.

$$Y_{INT} = Y_{DUT} - Y_{OPEN} \quad (2.129)$$

The noise correlation matrix of the DUT C_A^{DUT} was calculated using the measured four noise parameters [20].

$$C_A^{DUT} = 2kT \begin{bmatrix} R_n^{DUT} & \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}(Y_{opt}^{DUT})^* \\ \frac{NF_{min}^{DUT}-1}{2} - R_n^{DUT}Y_{opt}^{DUT} & R_n^{DUT}|Y_{opt}^{DUT}|^2 \end{bmatrix} \quad (2.130)$$

After that, the noise correlation matrix C_A^{DUT} was converted into its admittance representation C_Y^{DUT} . Together with the correlation matrix of the OPEN structure C_Y^{OPEN} , the correlation matrix of the intrinsic structure C_Y^{INT} can be obtained by de-embedding the parallel parasitic components from the DUT structure[2].

$$C_Y^{DUT} = T_Y C_A^{DUT} T_Y' \quad (2.131)$$

$$C_Y^{OPEN} = 2kT\Re(Y_{OPEN}) \quad (2.132)$$

$$C_Y^{INT} = C_Y^{DUT} - C_Y^{OPEN} \quad (2.133)$$

The power spectral density of the drain current noise S_{i_d} , gate current noise S_{i_g} and their cross-correlation were extracted [25] from the correlation matrix of the intrinsic structure C_Y^{INT} [38, 39].

$$S_{i_d} = 2C_{Y,22}^{INT} \quad (2.134)$$

$$S_{i_g} = 2C_{Y,11}^{INT} \quad (2.135)$$

$$S_{i_g i_d} = 2C_{Y,12}^{INT} \quad (2.136)$$

$$c = \frac{S_{i_g i_d}}{\sqrt{S_{i_d} \times S_{i_g}}} \quad (2.137)$$

2.5 Conclusion

Different types of noise source and the four noise parameters were discussed. The relationship between the four noise parameters and the drain current noise, gate current noise, and their cross-correlation were established. Some well known models for the channel thermal noise, which is the primary noise origin of MOSFET operating at high frequency, were presented. Early models such as Tsividis' thermal noise model were developed for long-channel MOSFETs. Whereas, for short-channel MOSFETs, there are controversy as to which of the short channel effects should be included and how they should be encountered for in deriving the channel thermal noise model.

Chapter 3 Short Channel Effects on Channel Thermal Noise Model

3.1 Overview

The channel thermal noise is the dominant noise source for RFCMOS, as discussed in Chapter 2. Consequently, many publications have been generated to derive the channel thermal noise by including the short channel effects such as channel length modulation (CLM) [2-4], velocity saturation effect (VSE) [2, 5-10] and hot carrier effect (HCE) [2, 6, 7, 10-14]. Some publications [5, 8] pointed out that the velocity saturation effect is crucial to be taken into account in the channel thermal noise model. Meanwhile, other publications [11-13] have a different view, in which they suggested that the hot carrier effect has greater influence on the channel thermal noise instead. Hence, the proper way to include the short channel effects in the channel thermal noise model still remains controversial.

In this chapter, the impact of the velocity saturation and the hot carrier effects on the channel thermal noise model is discussed. The channel thermal noise model including different short channel effects is derived using two well known approaches which are the local voltage noise source approach and the local current noise source approach. Thereafter the derived short channel thermal noise models are verified with on-wafer noise measurement data.

3.2 Channel Thermal Noise Model Derivation

3.2.1 Channel Thermal Noise Model including Channel Length Modulation Effect only

When the velocity saturation effect is absent, the drain current equation can be expressed as [17]

$$I_{DS} = -\mu(y)WQ'_I(y)E_y = -\mu(y)WQ'_I(y)\frac{dV_y}{dy} = -\frac{W}{L_{eff}}\mu_{eff}\int_0^{V_{DSeff}} Q'_I(V_y)dV_y \quad (3.1)$$

where E_y is the lateral electric field, V_y is the channel voltage, $Q'_I = -C'_{ox}(V_{GT} - \alpha V_y)$ is the inversion layer charge density, $V_{GT} = V_{GS} - V_{TH}$, μ_{eff} is the effective mobility, $L_{eff} = L - \Delta L$ is the length of the gradual channel region, and V_{DSeff} is the drain bias smoothening function obtained from BSIM4 [40]. The model parameters are extracted from the DC current-voltage characterization.

There are two well-known approaches to derive the channel thermal noise. First approach is the local voltage noise source approach. Here, the channel thermal noise is calculated based on Tsividis' method [17]. Figure 3.1 shows the noisy segment of MOSFET, with (a) is in the Thevenin representation and (b) is in its equivalent circuit of Norton representation. The gradual channel region of MOSFET is split into smaller sections with the length of Δy . Assuming that each small section with the length Δy acts as a resistor with the value ΔR , $\Delta V_y = I_{DS}\Delta R$ can be obtained. By considering the effect of the local noise source on the drain current, the new drain current can be written as [17, 41]

$$I_{DS} + \Delta i_{ds} = -\frac{W}{y_1}\mu_{eff}\int_0^{V_1} Q'_I(V_y)dV_y \quad (3.2)$$

Figure 3.1 Schematic of the noisy segment of MOSFET, with (a) is in Thevenin representation, and (b) is in its equivalent circuit of Norton representation [17, 42]

$$I_{DS} + \Delta i_{ds} = -\frac{W}{L_{eff} - y_1} \mu_{eff} \int_{V_1 + \Delta v}^{V_{DS_{eff}}} Q'_I(V_y) dV_y \quad (3.3)$$

where Δi_{ds} is the current noise, Δv is the voltage noise, y_1 is the length of the transistor at the left side, and V_1 is the point where the channel voltage starts to fluctuate. (3.2)

and (3.3) is summed up in order to obtain (3.4).

$$I_{DS} + \Delta i_{ds} = -\frac{W}{L_{eff}} \mu_{eff} \left[\int_0^{V_{DS_{eff}}} Q'_I(V_y) dV_y - \int_{V_1}^{V_1 + \Delta v} Q'_I(V_y) dV_y \right] \quad (3.4)$$

As only the small signal components are involved in the noise calculation, the current noise Δi_{ds} is derived to be

$$\Delta i_{ds} = \frac{W}{L_{eff}} \mu_{eff} \int_{V_1}^{V_1 + \Delta v} Q'_I(V_y) dV_y \quad (3.5)$$

$$\Delta i_{ds} = \frac{W}{L_{eff}} \mu_{eff} Q'_I(V_y) \Delta v \quad (3.6)$$

$$\frac{\overline{(\Delta i_{ds})^2}}{\Delta f} = \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 [Q'_I(V_y)]^2 \frac{\overline{(\Delta v)^2}}{\Delta f} \quad (3.7)$$

Together with Nyquist theory [19] of (3.8) and $\Delta V_y = I_{DS} \Delta R$, the channel thermal noise S_{i_d} is derived and simplified in (3.11) [17, 41].

$$\frac{\overline{(\Delta v)^2}}{\Delta f} = 4kT \Delta R \quad (3.8)$$

$$S_{i_d} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 [Q'_I(V_y)]^2 \Delta R \quad (3.9)$$

$$S_{i_d} = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \quad (3.10)$$

$$S_{i_d} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) \left(\frac{V_{GT}^2 - \alpha V_{GT} V_{DSeff} + \frac{\alpha^2}{3} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) = S'_{i_d} \quad (3.11)$$

Second approach is the local current noise source approach. Here, the channel thermal noise is calculated using van der Ziel's noise model [7]. From the drain current equation of (3.12), the current noise Δi_{ds} , the voltage noise Δv and the Langevin noise current $i_n(y)$ can be added in (3.12) to become (3.13).

$$I_{DS} = g(V_y) \frac{dV_y}{dy} \quad (3.12)$$

$$I_{DS} + \Delta i_{ds} = g(V_y + \Delta v) \frac{d(V_y + \Delta v)}{dy} + i_n(y) \quad (3.13)$$

Considering only small signal parts for noise, the current noise Δi_{ds} can be expressed as

$$\Delta i_{ds} = g(V_y) \frac{d(\Delta v)}{dy} + \frac{dg}{dV_y} \Delta v \frac{dV_y}{dy} + i_n(y) \quad (3.14)$$

$$\Delta i_{ds} = \frac{d}{dy} [g(V_y) \Delta v] + i_n(y) \quad (3.15)$$

By integrating over the whole channel and taking boundary conditions of $\Delta v(0) = \Delta v(L_{eff}) = 0$, the channel thermal noise is written as (3.17) [7].

$$\Delta i_{ds} = \frac{1}{L_{eff}} \int_0^{L_{eff}} i_n(y) dy \quad (3.16)$$

$$S_{i_d} = \frac{1}{L_{eff}^2} \int_0^{L_{eff}} \int_0^{L_{eff}} \overline{i_n(y) i_n^*(y')} dy dy' \quad (3.17)$$

Together with Nyquist theory [19] of (3.18), the channel thermal noise spectra density S_{i_d} can be derived to be (3.19) [7, 26].

$$\overline{i_n(y) i_n^*(y')} = 4kTg(V_y)\Delta f\delta(y - y'). \quad (3.18)$$

$$S_{i_d} = \frac{4kT}{L_{eff}^2} \int_0^{L_{eff}} g(V_y) dy \quad (3.19)$$

From (3.12), (3.20) can be obtained. Combining (3.19), (3.20) and $g(V_y) = W\mu_{eff}Q'_I(V_y)$, the channel thermal noise spectra density S_{i_d} is derived as shown in (3.21) [7, 26].

$$dy = g(V_y) \frac{dV_y}{I_{DS}} \quad (3.20)$$

$$S_{i_d} = \frac{4kT}{L_{eff}^2 I_{DS}} \int_0^{V_{Dseff}} g^2(V_y) dV_y = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{Dseff}} [Q'_I(V_y)]^2 dV_y \quad (3.21)$$

From the above derivations, it can be observed that (3.10) is same as (3.21).

Thus, it can be concluded that the channel thermal noise derived using both the local

voltage noise source approach and the local current noise source approach give the same result.

3.2.2 Channel Thermal Noise Model including Channel Length Modulation and Velocity Saturation Effects

With the presence of velocity saturation effect, the drain current equation is

$$I_{DS} = -WQ'_I(y)\mu(y)\frac{E_y}{1+\frac{E_y}{E_c}} \quad (3.22)$$

with E_c is the critical electric field.

First, the local voltage noise source approach or the Tsividis' method [17] is utilized in the channel thermal noise model derivation. Using the same method as in Section 3.2.1, the new drain current equations are expressed in (3.23) and (3.24) [41].

$$I_{DS} + \Delta i_{ds} = \frac{W}{y_1} \mu_{eff} \left(\frac{1}{1+\frac{V_1}{E_c y_1}} \right) \int_0^{V_1} Q'_I(V_y) dV_y \quad (3.23)$$

$$I_{DS} + \Delta i_{ds} = \frac{W}{L_{eff}-y_1} \mu_{eff} \left(\frac{1}{1+\frac{V_{DSeff}-(V_1+\Delta v)}{E_c(L_{eff}-y_1)}} \right) \int_{V_1+\Delta v}^{V_{DSeff}} Q'_I(V_y) dV_y \quad (3.24)$$

As only the small signal components are involved in the noise calculation, the current noise Δi_{ds} can be written as

$$\Delta i_{ds} = \frac{W}{L_{eff}} \mu_{eff} \left(\frac{1}{1+\frac{V_{DSeff}}{E_c L_{eff}}} \right) \int_{V_1}^{V_1+\Delta v} Q'_I(V_y) dV_y \quad (3.25)$$

$$\Delta i_{ds} = \frac{W}{L_{eff}} \mu_{eff} \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right) Q'_I(V_y) \Delta v \quad (3.26)$$

The channel thermal noise model including the channel length modulation and velocity saturation effects can be derived to be (3.29) and simplified to be (3.30) [41].

$$S_{i_d} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right)^2 \int_0^{V_{DSeff}} [Q'_I(V_y)]^2 \Delta R \quad (3.27)$$

$$S_{i_d} = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right)^2 \int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \quad (3.28)$$

$$S_{i_d} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right) \left(\frac{V_{GT}^2 - \alpha V_{GT} V_{DSeff} + \frac{\alpha^2}{3} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (3.29)$$

$$S_{i_d} = S'_{i_d} \times \frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \quad (3.30)$$

Second, the channel thermal noise is derived based on the local current noise source approach or the van der Ziel's noise model [7]. From the drain current equation of (3.31), the current noise Δi_{ds} , the voltage noise Δv and the Langevin noise current $i_n(y)$ can be added in (3.31) to become (3.32).

$$I_{DS} = \frac{g(V_y) \frac{dV_y}{dy}}{1 + \frac{1}{E_c} \frac{dV_y}{dy}} \quad (3.31)$$

$$I_{DS} + \Delta i_{ds} = \frac{g(V_y + \Delta v) \frac{d(V_y + \Delta v)}{dy}}{1 + \frac{1}{E_c} \frac{d(V_y + \Delta v)}{dy}} + i_n(y) \quad (3.32)$$

Considering only small signal parts for noise and approximating them to their first order, the current noise Δi_{ds} can be written to be (3.33).

$$[\Delta i_{ds} - i_n(y)] \left[1 + \frac{1}{E_c} \frac{dV_y}{dy} \right] + I_{DS} \left[\frac{1}{E_c} \frac{d(\Delta v)}{dy} \right] = \frac{d}{dy} [g(V_y) \Delta v] \quad (3.33)$$

By integrating over the whole channel and taking boundary conditions of $\Delta v(0) = \Delta v(L_{eff}) = 0$ and $V_y(0) = V_y(L_{eff}) = 0$, the channel thermal noise becomes (3.35).

$$\Delta i_{ds} = \frac{1}{L_{eff}} \left(\frac{1}{\frac{V_{DSeff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}}} \right) \int_0^{L_{eff}} i_n(y) dy \quad (3.34)$$

$$S_{i_d} = \left(\frac{1}{\frac{V_{DSeff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}}} \right)^2 \frac{1}{L_{eff}^2} \int_0^{L_{eff}} \int_0^{L_{eff}} \overline{i_n(y) i_n^*(y')} dy dy' \quad (3.35)$$

Together with Nyquist theory [19], the channel thermal noise S_{i_d} is derived as shown in (3.37).

$$S_{i_d} = \left(\frac{1}{\frac{V_{DSeff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}}} \right)^2 \frac{4kT}{L_{eff}^2} \int_0^{L_{eff}} g(V_y) dy \quad (3.36)$$

$$S_{i_d} = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \left(\frac{1}{\frac{V_{DSeff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}}} \right)^2 \int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \quad (3.37)$$

The channel thermal noise model of (3.37) is found to be same as (3.28), which draw the conclusion that both approaches produce the same result.

3.2.3 Channel Thermal Noise Model including Channel Length Modulation and Hot Carrier Effects

When the hot carrier effect is taken into consideration, the effective carrier temperature along the channel T_e is greater than the lattice temperature T . Besides, the effective carrier temperature T_e increases as the electric field strength increases. Even though the relationship between the effective electron temperature T_e and the electric field strength E_y is still remain unknown, a common assumption is made to simplified the calculation, in such that [7]

$$\frac{T_e}{T} = \left(1 + \frac{E_y}{E_c}\right)^n \quad (3.38)$$

where n is accounted for the hot carrier effect and $n = 0, 1, 2$. When $n = 0$, it can be seen that $T_e = T$ and the hot carrier effect is negligible. When $n = 1$ or $n = 2$, the hot carrier effect is taken into account, with different dependence with the electric field strength.

When the velocity saturation effect is absent, the drain current equation can be written as (3.1). To include the hot carrier effect, the temperature T in the channel thermal noise expression S_{i_d} for both the local voltage noise source approach of (3.10) and the local current noise source approach of (3.21) is replaced by T_e , to become (3.39) [41].

$$S_{i_d} = \frac{4kT_e}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DS_{eff}}} [Q'_I(V_y)]^2 dV_y \quad (3.39)$$

Together with (3.38), (3.39) becomes (3.40).

$$S_{i_d} = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^n [Q'_I(V_y)]^2 dV_y \quad (3.40)$$

From (3.1), $E_y = \frac{I_{DS}}{-W\mu_{eff}Q'_I}$ and thus the channel thermal noise is derived as [41]

$$S_{i_d} = S'_{i_d} + 4kT \frac{W\mu_{eff}}{L_{eff}^2} \left[\frac{C'_{ox}}{E_c} \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) \right] \quad \text{with } n = 1 \quad (3.41)$$

$$S_{i_d} = S'_{i_d} + 4kT \frac{W\mu_{eff}}{L_{eff}^2} \left[\frac{2C'_{ox}}{E_c} \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) + \left(\frac{C'_{ox} V_{DSeff}}{L_{eff} E_c^2} \right) \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) \right] \quad \text{with } n = 2. \quad (3.42)$$

The detailed derivation of (3.41) and (3.42) is demonstrated in Appendix A.1.

3.2.4 Channel Thermal Noise Model including Channel Length Modulation, Velocity Saturation and Hot Carrier Effects

With the presence of the velocity saturation effect, the drain current equation is expressed as (3.22). To include the hot carrier effect, the temperature T in the channel thermal noise expression S_{i_d} for both the local voltage noise source approach of (3.28) and the local current noise source approach of (3.37) is replaced by T_e , to become (3.43) [41].

$$S_{i_d} = \frac{4kT_e}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \quad (3.43)$$

Together with (3.38), (3.43) can be written as (3.44).

$$S_{i_d} = \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{\frac{V_{DSeff}}{1 + \frac{E_c L_{eff}}{E_c}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^n [Q'_l(V_y)]^2 dV_y \quad (3.44)$$

From (3.22), $E_y = \frac{I_{DS}}{-W\mu_{eff}Q'_l - (I_{DS}/E_c)}$ and thus the channel thermal noise is derived as [41]

$$S_{i_d} = S'_{i_d} \left[\frac{1}{\frac{V_{DSeff}}{1 + \frac{E_c L_{eff}}{E_c}}} \right] - 4kT \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{\frac{V_{DSeff}}{1 + \frac{E_c L_{eff}}{E_c}}} \right]^2 \left[\frac{C'_{ox}\alpha}{E_c W \mu_{eff}} \right] \\ \times \left[V_0^2 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) - V_{DSeff}(V_1 + V_0) + \frac{V_{DSeff}^2}{2} \right] \quad \text{with } n = 1 \quad (3.45)$$

$$S_{i_d} = S'_{i_d} \left[\frac{1}{\frac{V_{DSeff}}{1 + \frac{E_c L_{eff}}{E_c}}} \right] - 4kT \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{\frac{V_{DSeff}}{1 + \frac{E_c L_{eff}}{E_c}}} \right]^2 \left\{ \left[\frac{2C'_{ox}\alpha}{E_c W \mu_{eff}} \right] \right. \\ \times \left[V_0^2 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) - V_{DSeff}(V_1 + V_0) + \frac{V_{DSeff}^2}{2} \right] + \\ \left. \frac{(V_0 C'_{ox}\alpha)^2}{I_{DS}} \times \left[-2V_0 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) + V_{DSeff} - \frac{V_0^2}{V_{DSeff} + V_0 - V_1} + \frac{V_0^2}{V_0 - V_1} \right] \right\} \\ \text{with } n = 2 \quad (3.46)$$

where $V_0 = \frac{I_{DS}}{W\mu_{eff}C'_{ox}\alpha E_c}$ and $V_1 = \frac{V_{GT}}{\alpha}$. The detailed derivation of (3.45) and (3.46) is given in Appendix A.2.

With gradual channel approximation,

$$\left(1 + \frac{E_y}{E_c} \right) \approx 1 + \frac{V_{DSeff}}{E_c L_{eff}}. \quad (3.47)$$

By substituting (3.47) into (3.44), the channel thermal noise S_{i_d} for $n = 1$ can be simplified to S'_{i_d} [41]. The validity of the approximation will be verified in Section 3.3.

3.2.5 Difference of the Derivation in This Work against Literature Reported Models

In general, the channel thermal noise models are derived based on the basic theory by Klaassen-Prins [26]. There are two common approaches to derive the channel thermal noise, which are local current noise source approach, used in the van der Ziel's model [7], and local voltage noise source approach, used in Tsividis' thermal noise model [17]. Nevertheless, whether these two approaches will converge to the same channel thermal noise equation, after adding the short channel effects such as channel length modulation, velocity saturation and hot carrier effects, are yet to be verified. Besides, how they affect the channel thermal noise model remain controversy.

In order to have a clearer insight of the impact of these added short channel effects on the channel thermal noise, each of them are studied in more detail. Referring to section 2.3.6, the assumption in model of Chen and Deen [3] which ignores the velocity saturation effect is questionable. Moreover, [3] included the total inversion layer charge Q_{inv} of BSIM4 [32, 40], where the velocity saturation effect is included. This contradicts with their previous assumption. Hence, the proper way would be as shown in the derivation in section 3.2.1 which adopts basic drain current equation to calculate the inversion layer charge.

In order to include the velocity saturation effect into the channel thermal noise model, section 3.2.2 derived the channel thermal noise model in a different way as

other existing model, such as [5] and [8]. The drawbacks of [5] and [8] have been discussed in section 2.3.6. In fact, the proper way to include the velocity saturation effect into the channel thermal noise should start from the drain current equation such as (3.22) and (3.31), and thereafter derived the channel thermal noise using local voltage noise source approach or local current noise source approach, as presented in section 3.2.2. It is inappropriate to replace the parameters with velocity saturation effect into the long channel noise model, without re-derived the noise model.

In order to take into account the hot carrier effect into channel thermal noise model, an equivalent noise temperature T_e is introduced, since the thermal equilibrium condition is no longer hold for short channel devices. In [12], T_e is introduced to include the average drift velocity and energy relaxation time. This approach is different from the way used in section 3.2.3, where T_e is in function of the electric field strength E_y .

On the other hand, there is publication such as [6], where all these three short channel effects are included in their channel thermal noise model. However, the introduction of AC carrier mobility μ'_n and ac conductance g_{ac} in the channel thermal noise derivation is questionable, as discussed in section 2.3.6. Meanwhile, in section 3.2.4, the velocity saturation effect is included in drain current equation, and the hot carrier effect is included in the channel thermal noise derivation by replacing the temperature T to equivalent noise temperature T_e . Either the local voltage noise source approach or local current noise source approach yields the same channel thermal noise equation.

3.3 Experimental Results and Discussion

Figure. 3.2 illustrates the comparison of channel thermal noise model with different value of n , which are model of (3.30) when $n = 0$, model of (3.45) when $n = 1$, and model of (3.46) when $n = 2$, together with the measurement data. The comparison is done on NMOS with dimension of channel length $L = 0.13 \mu\text{m}$ and channel width $W = 20 \mu\text{m}$, across different frequencies, gate bias and drain bias. It can be seen that the model of (3.30) where $n = 0$ underestimates the channel thermal noise, while the model of (3.46) where $n = 2$ overestimates the channel thermal noise. Only the model of (3.45) with $n = 1$ can best predict the channel thermal noise characteristic versus frequency, gate bias and drain bias.

The channel thermal noise model including different short channel effects are shown in Figure 3.3, together with measurement data. The comparison is done on NMOS of $L = 0.13 \mu\text{m}$ and $W = 20 \mu\text{m}$, across different frequencies, gate bias and drain bias. There are two important parameters in justifying the channel thermal noise model. These two parameters are the local noise source and the transfer function to transfer the local noise source to the output at the drain side. When the velocity saturation effect is taken into consideration, the local resistance ΔR is increased, let say by a factor of k , resulting in the increase of the local voltage noise source generated in this small section of length Δy . Nevertheless, the mobility degradation causes the

Figure 3.2 Channel thermal noise power spectral density versus (a) frequency, (b) gate bias, and (c) drain bias, for NMOS of $L/W = 0.13\mu\text{m}/20\mu\text{m}$. The measurement results and the simulated results are represented by symbols and lines respectively [41].

Figure 3.3 Channel thermal noise power spectral density versus (a) frequency, (b) gate bias, and (c) drain bias, for NMOS of $L/W = 0.13\mu m/20\mu m$. The measurement results and the simulated results are represented by symbols and lines respectively. Model of (3.11) with CLM and model of (3.45) with CLM, VSE and HCE produce the same result in all domains. Excellent agreement is found for both the model of (3.11) and (3.45) with the extracted data [41].

transfer function of the local noise source to the drain side reduced by a factor of k^2 . Hence, the channel thermal noise at the drain terminal is reduced. This can be seen in Figure 3.3, where the model of (3.30) underestimates the channel thermal noise versus frequency, gate bias and drain bias [41].

When the hot carrier effect is taken into account, the electron temperature T_e is higher than the lattice temperature T , resulting in the increment of the local voltage noise source, by a factor of k . Since the transfer function of the local noise to the drain side is remained unchanged, the channel thermal noise with the channel length modulation and hot carrier effects is increased. This can be observed in Figure 3.3, in which the model of (3.41) overestimates the channel thermal noise characteristic versus frequency, gate bias and drain bias [41].

When both the velocity saturation and hot carrier effects are taken into consideration, the increment of the local resistance ΔR due to velocity saturation effect, and the higher electron temperature T_e due to hot carrier effect, causes the local voltage noise source to increase by a factor of k^2 . Besides, the transfer function of the local noise source to the drain side is decreased by a factor of k^2 due to velocity saturation effect. Thus, the channel thermal noise model including both the velocity saturation and hot carrier effects remains the same as though those two effects are not taken into consideration. Although the velocity saturation effect results in the decrement of the channel thermal noise, such decrement is completely cancelled out by the increment of the channel thermal noise caused by the hot carrier effect when $n = 1$. This characteristic can be observed in Figure 3.3, in which the model of (3.45) is very close to the model of (3.11) for all operating conditions, with difference of less than 1%. This also leads to the conclusion that the approximation made in last part of Section 3.2.4 is

Figure 3.4 Channel thermal noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively [41].

Figure 3.5 Channel thermal noise power spectral density versus gate bias for NMOS of different channel length and channel width $W = 20 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [41].

Figure 3.6 Channel thermal noise power spectral density versus drain bias for NMOS of different channel length and channel width $W = 20\mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [41].

valid. Besides, it can be seen that only the model of (3.11) and the model of (3.45) are able to match the noise measurement results for all the frequencies, and bias domains.

Hence, the model of (3.11) with the channel length modulation effect only is sufficient to describe the channel thermal noise across frequency, gate bias and drain bias [41].

The comparison of the channel thermal noise model of (3.11), (3.30), (3.41), (3.45) and measurement data for different channel length are shown in frequency domain in Figure 3.4, in gate bias domain in Figure 3.5, and in drain bias domain in Figure 3.6. The model of (3.30) which includes the channel length modulation and velocity saturation effects only underestimates the noise characteristic for all the channel length. Meanwhile, the model of (3.41) which includes the channel length modulation and hot carrier effects only overestimates the channel thermal noise for all the channel length. The error for the model of (3.30) and the model of (3.41) are more observable for smaller channel length devices. Meanwhile, the model of (3.11) with

channel length modulation effects only and the model of (3.45) with all three short channel effects can accurately predict the channel thermal noise in all three domains [41].

3.4 Conclusion

By including the channel length modulation effect, the velocity saturation effect and the hot carrier effect, the channel thermal noise model was derived and verified to be accurate with the on-wafer measurement data for deep sub-micron MOSFETs in gate bias domain and drain bias domain. Such noise model was found to be close with the noise model derived with the channel length modulation only. Apparently, the noise reduction caused by the velocity saturation effect is cancelled out by the noise increment caused by the hot carrier effect when $n = 1$ for all frequencies and biases. Thus, the channel thermal noise model including merely the channel length modulation is simple and sufficient for short channel NMOS.

Chapter 4 Effective Mobility Modeling for Channel Thermal Noise

4.1 Overview

One of the dominant sources of noise for MOSFETs operating in the GHz range is the channel thermal noise. Although efforts have been done to model the short channel MOSFETs by including the short channel effects to the channel thermal noise model, such as channel length modulation effect [2, 3], velocity saturation effect [2, 5-10] and hot carrier effect [2, 6, 7, 10-13], the mobility degradation due to the vertical field is of least concern. In fact, the mobility degradation due to vertical field is of utmost important for short channel MOSFETs noise modeling in drain bias domain.

4.2 Derivation of Effective Mobility Model

4.2.1 Existing Model

When the electric field in the channel is high, the surface roughness scattering is the dominant scattering mechanism. According to Matthiessen's rule [17], the local mobility of the carrier in the channel $\mu(y)$ can be expressed in term of the low field mobility μ_0 and the mobility due to surface roughness scattering μ_s .

$$\frac{1}{\mu(y)} = \frac{1}{\mu_0} + \frac{1}{\mu_s} \quad (4.1)$$

$$\mu(y) = \frac{\mu_0}{1 + \frac{\mu_0}{\mu_s}} \quad (4.2)$$

The local carrier mobility in the channel $\mu(y)$ can be approximated in term of the average vertical electric field in the channel, $E_{x,ave}$ as [17, 42]

$$\mu(y) = \frac{\mu_0}{1 + \alpha_0 E_{x,ave}} \quad (4.3)$$

where α_0 is a fitting parameter. For MOSFET, the average vertical electric field $E_{x,ave}$ can be expressed as [17]

$$E_{x,ave} = \frac{C'_{ox}}{2\epsilon_s} (V_{GB} - V_{FB} - \psi_s + \gamma\sqrt{\psi_s}) \quad (4.4)$$

where

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C'_{ox}} \quad (4.5)$$

$$\psi_s = \psi_0 + V_y = 2\phi_F + V_y \quad (4.6)$$

with

$$2\phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right). \quad (4.7)$$

Here, V_{GB} is the gate to bulk voltage, V_{FB} is the flat-band voltage, ψ_s is surface potential along the channel, ψ_0 is the surface potential at source side, V_y is the channel voltage, ϵ_s is the permittivity of silicon, N_A is the substrate doping concentration, and n_i is the intrinsic carrier concentration. Hence, the local carrier mobility in the channel $\mu(y)$ is expressed as (4.8) [17].

$$\mu(y) = \frac{\mu_0}{1 + \frac{\alpha_0 C'_{ox}}{2\epsilon_s} (V_{GB} - V_{FB} - [2\phi_F + V_y] + \gamma\sqrt{2\phi_F + V_y})} \quad (4.8)$$

The effective mobility of MOSFET μ_{eff} can be defined to be [17]

$$\mu_{eff} = \frac{1}{\frac{1}{L} \int_0^L \frac{1}{\mu(y)} dy}. \quad (4.9)$$

In order to simplified the derivation, the channel voltage V_y is assumed to increase gradually along the channel, in such that

$$\frac{dV_y}{dy} = \frac{V_{DS}}{L}. \quad (4.10)$$

Therefore, the effective mobility μ_{eff} can be derived by combining the effective mobility definition of (4.9), assumption of (4.10) and the local carrier mobility of (4.8) [17].

$$\mu_{eff} = \frac{\mu_0}{\frac{1}{V_{DS}} \int_0^{V_{DS}} [1+f(V)] dV_y} \quad (4.11)$$

$$f(V) = \frac{\alpha_0 C'_{ox}}{2\epsilon_s} (V_{GB} - V_{FB} - [2\phi_F + V_y] + \gamma \sqrt{2\phi_F + V_y}) \quad (4.12)$$

From (4.11) and (4.12), the effective mobility model can be simplified as [17].

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1 [V_{GT} - (1-\frac{\alpha}{2})V_{DS}]} \quad (4.13)$$

where α is the bulk charge effect coefficient, θ_1 is a fitting parameter, $V_{GT} = V_{GS} - V_{TH}$ with the threshold voltage $V_{TH} = V_{TH0} - \sigma V_{DS}$, and σ is a channel length dependent parameter to include the drain-induced barrier lowering effect (DIBL) [17, 43]. The effective mobility model of (4.13) is often simplified to (4.14), by ignoring the drain bias dependent term in (4.13) [17].

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1 V_{GT}} \quad (4.14)$$

4.2.2 Proposed Effective Mobility Model

As stated in section 4.2.1, the drain bias dependent term in (4.13) is often being ignored and (4.14) is commonly used in the channel thermal noise model. Nevertheless, it is found that there is a substantial discrepancy between (4.13) and (4.14), indicating that the above-mentioned assumption is questionable. Instead, the drain bias portion in the effective mobility model is significant and cannot be ignored. More efforts are needed for derivation of the effective mobility model [30, 42, 44].

The effective mobility model with drain bias dependency and channel length dependency are discussed in [44] and [30] respectively. In [44], the drain bias dependent effective mobility is modeled empirically to be

$$\mu_{eff} = \frac{\mu_0}{\sqrt{1+(\theta_1 V_{GT})^2+(\theta_2 V_{DS})^2}} \quad (4.15)$$

where θ_1 and θ_2 are fitting parameters. It is found that the drain bias dependent term of the effective carrier mobility can be related to the channel length of device, which is modeled empirically in [30] to be

$$\mu_{eff_proposed} = \frac{\mu_0}{\sqrt{1+(\theta_1 V_{GT})^2+[(1-2L'_{total})V_{DS}]^2}} \quad (4.16)$$

where $L'_{total} = L_{total} \times 10^6$, and L_{total} is the total channel length.

In fact, the effective carrier mobility is governed by the vertical electric field in the channel of MOSFET.

Figure 4.1 Cross section of MOSFET, illustrating the two-dimensional electric field pattern when biases are applied in gate and drain terminal [42].

The vertical electric field is produced in channel when the gate voltage and drain voltage are applied to their terminals. Generally, the electric field lines, which appear in the channel when the drain bias is applied, can be polarized into vertical and lateral components, as shown in Figure 4.1 [17, 42, 43]. Among these two components, the drain-induced barrier lowering (DIBL) has accounted for the lateral electric field. Meanwhile, the vertical component of the electric field in the channel has not been included in the existing effective mobility model.

In [42], the vertical component of the electric field is known as drain-induced vertical field (DIVF). In order to model the drain-induced vertical field (DIVF), the relationship between the average vertical electric field $E_{x,ave}$, the drain bias and the channel length need to be investigated. The average vertical electric field $E_{x,ave}$ is extracted from the DC measurement data, and compared with the existing average vertical electric field of (4.4) [17], versus drain bias in Figure 4.2. The detailed extraction method of average vertical electric field $E_{x,ave}$ is presented in Appendix B. It can be observed that there is a discrepancy between the extracted average vertical electric field and the existing model of (4.4). The excess vertical electric field is DIVF,

and it is proportional to the drain bias. After that, the slope of the excess vertical electric field versus drain bias, which is $\frac{\Delta E_{x,ave}}{\Delta V_{DS}}$ is plotted against channel length in Figure 4.3. It is found that the excess vertical electric field is inversely proportional to $\sqrt{L}$. The magnitude of DIVF becomes larger with the decreasing of channel length since the drain side and the source side becomes closer to each other. Hence, the existing average vertical electric field in (4.4) is modified to include the DIVF, in such that the new average vertical electric field E_{x,ave_new} is

$$E_{x,ave_new} = \frac{C'_{ox}}{2\epsilon_s} \left(V_{GB} - V_{FB} - [2\phi_F + V_y] + \gamma \sqrt{2\phi_F + V_y} + \sqrt{\frac{\beta}{L}} V_{DS} \right) \quad (4.17)$$

where β is the DIVF parameter, with β and L are in nm .

Figure 4.2 Comparison of the extracted average vertical electric field $E_{x,ave}$ and the existing average vertical electric field of (4.4) versus drain bias, of the NMOS with channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at gate bias of $V_{GS} = 1.2 V$. The discrepancy between the extracted average vertical electric field and the model of (4.4) is DIVF, and found to be proportional to drain bias.

Figure 4.3 Slope of the excess vertical electric field with respect to drain bias, $\frac{\Delta E_{x,ave}}{\Delta V_{DS}}$, versus channel length, of the NMOS with channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at gate bias of $V_{GS} = 1.2 V$. The excess vertical electric field is inversely proportional to $\sqrt{L}$.

With the new average vertical electric field of (4.17), the new local carrier mobility in the channel $\mu_{new}(y)$ can be written as (4.18) [42].

$$\mu_{new}(y) = \frac{\mu_0}{1 + \frac{\alpha_0 C'_{ox}}{2\epsilon_s} \left(V_{GB} - V_{FB} - [2\phi_F + V_y] + \gamma \sqrt{2\phi_F + V_y} + \sqrt{\frac{\beta}{L}} V_{DS} \right)} \quad (4.18)$$

Together with the definition of effective mobility of (4.9) and assumption of (4.10), the new effective mobility model is shown to be (4.19) [42].

$$\mu_{eff_new} = \frac{\mu_0}{\frac{1}{V_{DS}} \int_0^{V_{DS}} [1 + f(V)] dV_y} \quad (4.19)$$

$$f(V) = \frac{\alpha_0 C'_{ox}}{2\epsilon_s} \left(V_{GB} - V_{FB} - [2\phi_F + V_y] + \gamma \sqrt{2\phi_F + V_y} + \sqrt{\frac{\beta}{L}} V_{DS} \right) \quad (4.20)$$

From (4.19) and (4.20), the new effective mobility μ_{eff_new} can be simplified as (4.21) [42].

$$\mu_{eff_new} = \frac{\mu_0}{1 + \frac{\alpha_0 C'_{ox}}{2\epsilon_s} \left(V_{GT} + \left[\sqrt{\frac{\beta}{L}} - \left(1 - \frac{\alpha}{2} \right) \right] V_{DS} \right)} \quad (4.21)$$

The new effective mobility model is thereafter being further simplified to [42]

$$\mu_{eff_new} = \frac{\mu_0}{1 + \theta_1 V_{GT} + \left[\sqrt{\frac{\theta_2}{L}} - \theta_1 \left(1 - \frac{\alpha}{2} \right) \right] V_{DS}} \quad (4.22)$$

where θ_1 and θ_2 are fitting parameters with θ_2 is in nm . Comparing to the conventional effective mobility model of (4.13), (4.22) has an additional channel length dependent term of $\sqrt{\frac{\theta_2}{L}} V_{DS}$, to include the DIVF to the effective mobility model.

Meanwhile, comparing to the simplified effective mobility model of (4.14), the composite effect of DIVF and bulk charge screening effect has been included in (4.22),

with additional channel length and drain bias dependent term of $\left[\sqrt{\frac{\theta_2}{L}} - \theta_1 \left(1 - \frac{\alpha}{2} \right) \right] V_{DS}$.

The channel thermal noise model, as discussed in Chapter 3, is repeated as (4.23) for convenience [41].

$$S_{i_d} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) \left(\frac{V_{GT}^2 - \alpha V_{GT} V_{DSeff} + \frac{\alpha^2}{3} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (4.23)$$

In order to improve the model accuracy, it is proposed that the new effective mobility model of (4.22) should be used in the channel thermal noise model of (4.23), in such

that the drain-induced vertical field (DIVF) is being taken into consideration. After that, the proposed model is verified with the on-wafer measurement results in section 4.3.

4.3 Experimental Results and Discussion

The effective mobility models of (4.13), (4.14) and (4.22) with respect to drain voltage are compared for smaller channel length of $L = 0.13 \mu\text{m}$ and larger channel length of $L = 0.50 \mu\text{m}$ in Figure 4.4. The comparison is done on NMOS with channel width $W = 20 \mu\text{m}$, at gate bias of $V_{GS} = 1.2 \text{ V}$. The bulk charge effect coefficient α and the fitting parameters θ_1, θ_2 are extracted the DC characterization to be $\alpha = 1.05$, $\theta_1 = 0.7$ and $\theta_2 = 6.4 \text{ nm}$. The same set of values for the fitting parameters $\theta_1 = 0.7$ and $\theta_2 = 6.4 \text{ nm}$, is used for all the dimensions and operating conditions. From Figure 4.4, the effective mobility model of (4.14) is flat with respect to drain bias, since the equation has been simplified with the drain bias term being ignored. Meanwhile, the existing effective mobility model of (4.13) shows the trend that the carrier mobility increases with the drain bias. When the drain bias increases, the depletion region charges will increase as well, causing the screening effect. The screening effect acts like a layer in such that lesser carriers are being dragged towards the rougher Si-SiO₂ surface by the vertical electric field. Thus, the carrier mobility is increased. Besides, it can be seen from Figure 4.4 that the simplified effective mobility model of (4.14) is deviated significantly from the existing effective mobility model of (4.13), indicating that the influence of the drain bias dependent term is substantial and cannot be ignored.

[42]

(a)

(b)

Figure 4.4 Effective mobility versus drain bias, for NMOS of (a) $W/L = 20\mu\text{m}/0.13\mu\text{m}$. and (b) $W/L = 20\mu\text{m}/0.50\mu\text{m}$, at gate bias of 1.2V. Different effective mobility models are compared to establish their drain bias dependency. The new effective mobility model of (4.22) which includes DIVF describes the compound effect of the drain bias and the channel length on the carrier mobility. [42]

For longer channel length MOSFETs, the channel conditions such as the electric field are mainly determined by the gate and substrate. However, as the channel length becomes shorter, the channel conditions are determined not only by the gate and substrate, but also by the source and drain which are comparatively near to all the small sections in the channel as well. When the drain voltage increases, the vertical electric field will increase as well, which is same as described in the drain-induced vertical field (DIVF), and hence causing degradation to the carrier mobility. In Figure 4.4, the DIVF is taken into consideration in the new effective mobility model of (4.22) to describe the composite effect of the drain voltage and channel length on the carrier mobility. In fact, two important parameters need to be investigated in order to justify the carrier mobility, which are the DIVF and the bulk charge screening effect. These two effects increase as the drain voltage increase. Nevertheless, they have different impacts on the carrier mobility, in such that the carrier mobility is proportional to the bulk charge screening effect, but inversely proportional to the DIVF. Since the bulk charge screening effect is larger than the DIVF, the overall increment trend of the carrier mobility with respect to drain bias can be observed in Figure 4.4. Another observation from Figure 4.4 is that the slope difference between the existing effective mobility model of (4.13) and the new effective mobility model of (4.22) is larger for shorter channel length MOSFET. In other words, the effective mobility is less dependent on the drain bias for shorter channel length device of $L = 0.13 \mu\text{m}$, as compared to larger channel length device of $L = 0.50 \mu\text{m}$. This is because of the larger DIVF effect as the channel length becomes shorter. [42]

The channel thermal noise model of (4.23) with and without DIVF, the model of [3], and the noise data extracted from on-wafer measurement are compared versus

frequency in Figure 4.5, versus gate bias in Figure 4.6, versus drain bias in Figure 4.7, and versus channel length in Figure 4.8. The comparison is done on NMOS with channel length $L = 0.13 \mu\text{m}$, $L = 0.25 \mu\text{m}$ and $L = 0.50 \mu\text{m}$, and channel width $W = 20 \mu\text{m}$. Figures. 4.5 to 4.8 shows that the spectral density lines of the channel thermal noise model of (4.23) with existing effective mobility model of (4.14) and the model of [3] show similar results in all four plots. Both channel thermal noise models used the similar effective mobility model which is the function of gate voltage and threshold voltage only.

Figure 4.5 Channel thermal noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [42]

Figure 4.6 Channel thermal noise power spectral density versus gate bias for NMOS of different channel length and channel width $W = 20\mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [42]

Figure 4.7 Channel thermal noise power spectral density versus drain bias for NMOS of different channel length and channel width $W = 20\mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. Only the proposed model of (4.23) with (4.22) which includes the DIVF have the proper slope with respect to drain voltage for the channel thermal noise [42]

In the channel thermal noise modelling, it is crucial to ensure the accuracy of noise prediction at $V_{DS} = 0$ V before proceeding to other biasing points, as the short channel effects such as velocity saturation effect and hot carrier effect are not exist at $V_{DS} = 0$ V. This causes all the above-mentioned short channel thermal noise models reducing back to the classical long channel thermal noise model, and they will produced the same results at $V_{DS} = 0$ V, as shown in Figure 4.7. Nevertheless, proper slope with respect to drain bias for channel thermal noise can only be achieved if the DIVF is included in the effective mobility model and the channel thermal noise model as shown by the line representing model of (4.23) with (4.22) in Figure 4.7. The improvement becomes more substantial for shorter channel length devices, since the DIVF effect is larger for them. Another observation from Figures 4.5 and 4.6 is that the proposed model with DIVF, in which the proper slope with respect to drain bias is obtained, is able to improve the model accuracy with respect to frequency and gate bias as well. For example, at gate voltage $V_{GS} = 1.2$ V and drain voltage $V_{DS} = 1.2$ V, the channel thermal noise model of (4.23) with effective mobility model of (4.14) and the model of [3] deviates from the measured noise data for roughly 12%. Maximum error of up to 25% is observed in the channel thermal noise model of (4.23) with existing effective mobility model of (4.13). Here, the channel thermal noise model of (4.23) with effective mobility model of (4.22), in which the DIVF is introduced, can greatly improve the model accuracy for all the devices of interest, in such that only less than 3% error is found for those channel length at this biasing point. This improvement will subsequently reduce the error in the noise related parameters such as four noise parameters and noise figure at circuit level. Hence, the DIVF effect need to be included in the channel thermal noise modeling in order to model the noise of MOSFETs

accurately with respect to frequency, gate voltage and drain voltage for different channel length. [42]

The simulated channel thermal noise with respect to the channel length is shown in Figure 4.8. From Figure 4.8, only the proposed model of (4.23) with (4.22), which includes DIVF, is able to describe the channel length characteristic of the channel thermal noise accurately, while another three models fail to do so. The nature of the DIVF, which is larger as channel length scaled down, causing the accuracy of the noise model versus channel length improved. Excellent agreement is achieved between the measurement data and the channel thermal noise model of (4.23) with (4.22). This indicates that the proposed model including DIVF is able to explain the noise performance of the 0.13 μm RFCMOS very well. [42]

Figure 4.8 Channel thermal noise power spectral density versus channel length, for NMOS of channel width $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{V}$. The measurement results and the simulation results are represented by symbols and lines respectively. As the channel length is scaled down, the improvement brought by the DIVF effect becomes more significant. Only the proposed model of (4.23) with (4.22) can accurately describe the channel length characteristic of the channel thermal noise. [42]

The scalability of the proposed model is examined for different channel width versus frequency in Figure 4.9, versus gate bias in Figure 4.10, and versus drain bias in Figure 4.11. The devices used are NMOS with channel length of $L = 0.13 \mu\text{m}$ and channel width of $W = 4 \mu\text{m}$, $W = 12 \mu\text{m}$ and $W = 20 \mu\text{m}$. It is found that the channel thermal noise at $V_{DS} = 0 \text{ V}$ is modeled well for all the models, indicating that low field mobility μ_0 and the fitting parameter θ_1 used in all the channel thermal noise models are of appropriate values. Besides, the improvement of the slope characteristic with respect to drain bias using the proposed model is found to be extended to other MOSFETs with different channel width. This leads to the conclusion that by taking into account the DIVF effect, the proposed model of (4.23) with (4.22) is scalable across different channel length and channel width when operates in different frequencies and biases. Theoretically, the channel thermal noise is linearly proportional to the total width of the MOSFETs. [42]

Figure 4.9 Channel thermal noise power spectral density versus frequency for NMOS of different channel width and channel length $L = 0.13 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [42]

Figure 4.10 Channel thermal noise power spectral density versus gate bias for NMOS of different channel width and channel length $L = 0.13 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [42]

Figure 4.11 Channel thermal noise power spectral density versus drain bias for NMOS of different channel width and channel length $L = 0.13 \mu\text{m}$. The measurement results and the simulation results are represented by symbols and lines respectively. [42].

4.4 Conclusion

A new effective mobility model was developed to be electric field dependant by introducing the drain-induced vertical field (DIVF). This new effective mobility model was incorporated in the high frequency channel thermal noise model, which has been discussed in chapter 3, to improve the accuracy of the model especially in the drain bias domain. The drain-induced vertical field is developed and proved to be a function of drain voltage and device channel length. By utilizing the new field dependent effective mobility model, the slope of the channel thermal noise model with respect to drain voltage was in correct trend. Moreover, the improvement due to DIVF effect becomes more significant when the channel length is scaled down. Simulation results of the proposed model establish excellent agreement with the extracted noise measurement data with respect to frequencies, gate voltage and drain voltage for different channel length and channel width. Hence, the proposed model with the DIVF effect is scalable.

Chapter 5 Substrate-Induced Drain Current Noise Model and Four Noise Parameters

5.1 Overview

To date, publications for high frequency noise modeling [2, 3, 5-13, 15-17] are focus on the channel thermal noise modeling, and the drain current noise is often assumed to be the same as the channel thermal noise, which is white noise. However, the on-wafer high frequency noise measurement shows that the drain current noise decreases gradually with frequency and remains flat at higher frequency. The part of the drain current noise where it is frequency dependent is normally assumed to be measurement error and its origin is of least concern. Nevertheless, the frequency dependent characteristic is found to be more significant for shorter channel length RFCMOS, in such that the drain current noise only exhibit white noise characteristic at frequency higher than 5 to 10 GHz for deep submicron RFCMOS, and even more than 10 GHz for nanometer RFCMOS. This trend can no longer be explained by the measurement error[45].

In this chapter, the substrate-induced drain current noise is introduced to explain the origin of the excess noise which exhibits the frequency dependent characteristic in the drain current noise data extracted from on-wafer high frequency noise measurement. Substrate noise was reported in [46-53] to dominate the drain current noise in MHz range. In fact, a noticeable level of substrate noise [46-53] can be observed in GHz range. The drain current noise model is developed to include the substrate-induced drain current noise. A new methodology which involves small signal

analysis is proposed to extract the model parameters of the substrate-induced drain current noise model. Besides of the drain current noise model, the gate current noise model and their cross-correlation for MOSFETs will be formulated. Eventually, four noise parameters will be calculated based on the proposed noise models and verified with on-wafer noise measurement noise data.

5.2 Model Formulation

5.2.1 Drain Current Noise Model

The channel thermal noise model [41] for high frequency RFCMOS, as discussed in Chapter 3, is repeated in (5.1) for convenience.

$$S_{i_{d_ch}} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) \left(\frac{V_{GT}^2 - \alpha V_{GT} V_{DSeff} + \frac{\alpha^2}{3} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (5.1)$$

The effective mobility μ_{eff} [42] in (5.1) includes the drain-induced vertical field (DIVF), as discussed in Chapter 4, and is repeated in (5.2) for convenience.

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 V_{GT} + \left[\sqrt{\frac{\theta_2}{L}} - \theta_1 \left(1 - \frac{\alpha}{2} \right) \right] V_{DS}} \quad (5.2)$$

Figure 5.1 shows the schematic representation of a MOSFET with proposed substrate network modeled by a substrate resistance R_{bb} in parallel with a substrate capacitance C_{bb} , and a noise source $S_{v_{bb}}$. According to Nyquist theory [19], the thermal noise $S_{v_{bb}}$, which origins from the substrate resistance R_{bb} , can be written as (5.3).

$$S_{v_{bb}} = 4kT R_{bb} \quad (5.3)$$

The substrate network in Figure 5.1 acts like a low pass filter, in such that the substrate resistance thermal noise at node V_b is

$$S_{v_b} = \frac{4kTR_{bb}}{1+\omega^2 R_{bb}^2 C_{bb}^2}. \quad (5.4)$$

Figure 5.1 Schematic representation of a MOSFET, together with proposed substrate network formed by substrate resistance, substrate capacitance, and substrate resistance thermal noise [45].

The substrate resistance thermal noise at node V_b is thereafter coupled to the drain terminal through the bulk transconductance g_{mb} , and results in an excess frequency dependent noise. This excess noise is given the name of substrate-induced drain current noise $S_{i_{d_sub}}$ [45] and is derived to be [45-47]

$$S_{i_{d_sub}} = S_{v_b} \times g_{mb}^2 = \frac{4kTg_{mb}^2 R_{bb}}{1+\omega^2 R_{bb}^2 C_{bb}^2} \quad (5.5)$$

The substrate network parameter extraction is presented in Section 5.3. Meanwhile, the low pass filter characteristic of the substrate-induced drain current noise will be verified in Section 5.4.

The total drain current noise S_{i_d} [45] at GHz regime is contributed by the well-known white channel thermal noise $S_{i_{d_ch}}$ [41, 42], the proposed substrate-induced drain current noise $S_{i_{d_sub}}$ [45], and the gate resistance thermal noise $S_{i_{d_Rg}}$ [54, 55]

$$S_{i_d} = S_{i_{d_ch}} + S_{i_{d_sub}} + S_{i_{d_Rg}} \quad (5.6)$$

with [54, 55]

$$S_{i_{d_Rg}} = 4kTg_m^2R_g \quad (5.7)$$

The characteristic of each part of the noise and their summation will be verified in Section 5.4.

5.2.2 Gate Current Noise and Correlation between Drain Current Noise and Gate Current Noise

When MOSFETs operate at high frequency of GHz, it is reported that they performed like a RC distributed network, with the distributed capacitance is the capacitance coupling to the gate terminal and the distributed resistance is the channel [7]. The wave equation of the distributed line which represents a MOSFET with low substrate conductivity can be written as (5.7) [7].

$$\frac{d^2}{dy^2} [g(V_y)\Delta V_y] = j\omega W C'_{ox} \Delta V_y \quad (5.8)$$

The gradual channel region of MOSFET is split into smaller sections with the length of Δy . The voltage noise Δv produced in the small section of the channel will leak to the gate terminal and results in the gate current noise [7, 56]. The total gate current noise Δi_g can be obtained by integrating along the channel [7].

$$\Delta i_g = j\omega W C'_{ox} \int_0^{V_{DSeff}} \Delta v dy \quad (5.9)$$

$$\Delta i_g = j\omega W C'_{ox} \Delta i_{ds} \left[- \int_0^{V_1} \frac{y}{g(V_y)} dy - \int_{V_1}^{V_{DSeff}} \frac{y - L_{eff}}{g(V_y)} dy \right] \quad (5.10)$$

$$\Delta i_g = j\omega W C'_{ox} \Delta i_{ds} \left[- \int_0^{V_{DSeff}} \frac{y}{g(V_y)} dy + \int_{V_1}^{V_{DSeff}} \frac{L_{eff}}{g(V_y)} dy \right] \quad (5.11)$$

Since the drain current equation for MOSFET is given by

$$I_{DS} = g(V_y) \frac{dV_y}{dy} \quad (5.12)$$

where

$$g(V_y) = -W \mu_{eff} Q'_l(V_y) - \frac{I_{DS}}{E_c} \quad (5.13)$$

it can be derived that

$$y = \frac{1}{I_{DS}} \int_0^{V_y} g(V_y) dV_y = \frac{1}{I_{DS}} \int_0^{V_y} W \mu_{eff} C'_{ox} (V_{GT} - \alpha V_y) - \frac{I_{DS}}{E_c} dV_y \quad (5.14)$$

$$y = \frac{1}{I_{DS}} \left[W \mu_{eff} C'_{ox} \left(V_{GT} V_y - \frac{\alpha}{2} V_y^2 \right) - \frac{I_{DS}}{E_c} V_y \right] \quad (5.15)$$

After that, integration is performed for both integral parts of (5.11).

$$\int_{V_1}^{V_{DSeff}} \frac{L_{eff}}{g(V_y)} dy = \int_{V_1}^{V_{DSeff}} L_{eff} \frac{dV_y}{I_{DS}} = \frac{L_{eff}}{I_{DS}} [V_{DSeff} - V_1] \quad (5.16)$$

$$\int_0^{V_{DSeff}} \frac{y}{g(V_y)} dy = \int_0^{V_{DSeff}} \frac{1}{I_{DS}} \left[W \mu_{eff} C'_{ox} \left(V_{GT} V_y - \frac{\alpha}{2} V_y^2 \right) - \frac{I_{DS}}{E_c} V_y \right] \frac{dV_y}{I_{DS}} \quad (5.17)$$

$$\int_0^{V_{DSeff}} \frac{y}{g(V_y)} dy = \frac{L_{eff}}{I_{DS}} \left[\left(1 + \frac{V_{DSeff}}{E_c L_{eff}} \right) \left(\frac{\frac{1}{2} V_{GT} V_{DSeff} - \frac{\alpha}{6} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) - \frac{1}{E_c L_{eff}} \left(\frac{V_{DSeff}^2}{2} \right) \right] \quad (5.18)$$

Substituting (5.16) and (5.18) into (5.111), the gate current noise Δi_g can be derived to be

$$\begin{aligned} \Delta i_g = \frac{j\omega W C'_{ox} \Delta i_{ds} L_{eff}}{I_{DS}} & \left[V_{DSeff} - V_1 - \left(1 + \frac{V_{DSeff}}{E_c L_{eff}} \right) \left(\frac{\frac{1}{2} V_{GT} V_{DSeff} - \frac{\alpha}{6} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \right. \\ & \left. + \frac{1}{E_c L_{eff}} \left(\frac{V_{DSeff}^2}{2} \right) \right] \end{aligned} \quad (5.19)$$

and further simplified to be

$$\Delta i_g = j\omega W C'_{ox} \left(\frac{L_{eff}}{I_{DS}} \right) \Delta i_{ds} [V_{as} - V_y] \quad (5.20)$$

with

$$V_{as} = V_{DSeff} + \frac{1}{E_c L_{eff}} \left(\frac{V_{DSeff}^2}{2} \right) - \left(1 + \frac{V_{DSeff}}{E_c L_{eff}} \right) \left(\frac{\frac{1}{2} V_{GT} V_{DSeff} - \frac{\alpha}{6} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (5.21)$$

The gate current noise spectral density is written as

$$\frac{\overline{\Delta i_g^2}}{\Delta f} = \omega^2 W^2 C'^2_{ox} \left(\frac{L_{eff}^2}{I_{DS}^2} \right) \left(\frac{\overline{\Delta i_{ds}^2}}{\Delta f} \right) [V_{as} - V_y]^2. \quad (5.22)$$

Thus, the induced gate noise spectral density $S_{i_{g-ch}}$ can be derived by integrating over the whole channel.

$$S_{i_{g-ch}} = \int_0^{V_{DSeff}} \frac{\overline{\Delta i_g^2}}{\Delta f} dV_y \quad (5.23)$$

$$S_{i_{g-ch}} = \omega^2 W^2 C'^2_{ox} \left(\frac{L_{eff}^2}{I_{DS}^2} \right) \left(\frac{4kT}{I_{DS}} \right) \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right) Q_I'^2 [V_{as} - V_y]^2 dV_y \quad (5.24)$$

Together with the gradual channel approximation of $\left(1 + \frac{E_y}{E_c}\right) \approx 1 + \frac{V_{DSeff}}{E_c L_{eff}}$, which has been used in Chapter 3, the induced gate noise spectral density $S_{i_{g-ch}}$ can be derived to be (5.25) [45].

$$S_{i_{g-ch}} = \frac{4kT\omega^2 W^4 C_{ox}'^4 \mu_{eff}^2}{I_{DS}^3 \left(1 + \frac{V_{DSeff}}{E_c L_{eff}}\right)} \left[\frac{\alpha^2}{5} V_{DSeff}^5 - \frac{\alpha}{2} (\alpha V_{as} + V_{GT}) V_{DSeff}^4 + \frac{1}{3} (\alpha^2 V_{as}^2 + 4\alpha V_{GT} V_{as} + V_{GT}^2) V_{DSeff}^3 - V_{GT} V_{as} (\alpha V_{as} + V_{GT}) V_{DSeff}^2 + V_{GT}^2 V_{as}^2 V_{DSeff} \right] \quad (5.25)$$

There is a correlation between the channel thermal noise and the induced gate noise, due to the fact that both of them origins from the thermal noise generated in the channel. Their cross-correlation is expressed in (5.26) [45].

$$\frac{\Delta i_g \Delta i_{ds}^*}{\Delta f} = j\omega W C_{ox}' \left(\frac{L_{eff}}{I_{DS}}\right) \left(\frac{\Delta i_{ds}^2}{\Delta f}\right) [V_{as} - V_y] \quad (5.26)$$

After that, integration is performed over the whole channel region to obtain the power spectral density of the cross-correlation term $S_{i_g i_{ds}^*}$.

$$S_{i_g i_{ds}^*} = \int_0^{V_{DSeff}} \frac{\Delta i_g \Delta i_{ds}^*}{\Delta f} dV_y \quad (5.27)$$

$$S_{i_g i_{ds}^*} = j\omega W C_{ox}' \left(\frac{L_{eff}}{I_{DS}}\right) \left(\frac{4kT}{I_{DS}}\right) \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c}\right) Q_I'^2 [V_{as} - V_y] dV_y \quad (5.28)$$

$$S_{i_g i_{ds}^*} = \frac{j4kT\omega W^3 C_{ox}'^3 \mu_{eff}^2}{L_{eff} I_{DS}^2} \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right) \left[-\frac{1}{4} \alpha^2 V_{DSeff}^4 + \frac{\alpha}{3} (\alpha V_{as} + 2V_{GT}) V_{DSeff}^3 - \frac{V_{GT}}{2} (2\alpha V_{as} + V_{GT}) V_{DSeff}^2 + V_{GT}^2 V_{as} V_{DSeff} \right] \quad (5.29)$$

The noise generated by the substrate resistance in Figure 5.1 is coupled to the gate terminal by the gate-bulk capacitance C_{gb} , producing the substrate-induced gate current noise spectral density $S_{i_{g-sub}}$, which is given by [45]

$$S_{i_{g-sub}} = S_{vb} \times (j\omega C_{gb})^2 = \frac{4kTR_{bb}(\omega C_{gb})^2}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \quad (5.30)$$

and its correlation with the substrate-induced drain current noise is [45]

$$S_{i_{g-d-sub}} = S_{vb} \times (j\omega C_{gb}) \times (g_{mb} R_{bb}) = \frac{j4kTg_{mb}R_{bb}(\omega C_{gb})}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \quad (5.31).$$

Nevertheless, substrate-induced gate current noise $S_{i_{g-sub}}$ is negligible compared to the channel induced gate noise $S_{i_{g-ch}}$ because the gate-bulk capacitance C_{gb} is very small.

Besides the channel induced gate noise $S_{i_{g-ch}}$ and the substrate-induced gate current noise $S_{i_{g-sub}}$, another source of the gate current noise is coming from the gate resistance [57, 58], which can be shown in (5.32) [45, 54, 55].

$$S_{i_{g-Rg}} = 4kT\omega^2 C_{gg}^2 R_g \quad (5.32)$$

The cross-correlation due to the gate resistance is expressed in (5.33) [45, 54].

$$S_{i_{g-d-Rg}} = j4kT\omega C_{gg} R_g g_m \quad (5.33)$$

The total gate current noise S_{i_g} is

$$S_{i_g} = S_{i_{g-ch}} + S_{i_{g-Rg}} \quad (5.34)$$

Meanwhile, the cross-correlation between the total drain current noise and the total gate current noise is written in (5.35).

$$S_{ig_i^*} = S_{ig_i^*_{ch}} + S_{ig_i^*_{Rg}} \quad (5.35)$$

5.2.3 Four Noise Parameters

As discussed in Chapter 2, the noise spectral density can be obtained from the measured four noise parameters by using (5.36) to (5.39) [38, 39].

$$S_{i_d} = 4kT|Y_{21}|^2 R_n \quad (5.36)$$

$$S_{i_g} = 4kTR_n \left[|Y_{11}|^2 + |Y_{opt}|^2 - 2\Re(Y_{11}Y_{cor}^*) \right] \quad (5.37)$$

$$S_{ig_i^*} = 4kT(Y_{11} - Y_{cor})R_n Y_{21}^* \quad (5.38)$$

$$Y_{cor} = \frac{F_{min}-1}{2R_n} - Y_{opt} \quad (5.39)$$

On the other hand, from the modeled noise spectral density, four noise parameters can be computed using (5.36) to (5.39) as well [35]. The noise resistance R_n can be expressed as

$$R_n = \frac{S_{i_d}}{4kT|Y_{21}|^2} = \frac{S_{i_d}}{4kT \left[(\Re(Y_{21}))^2 + (\Im(Y_{21}))^2 \right]}. \quad (5.40)$$

In order to obtain the optimum source admittance Y_{opt} , Y_{cor} is calculated first.

$$Y_{cor} = G_{cor} + jB_{cor} \quad (5.41)$$

$$Y_{cor} = Y_{11} - \frac{S_{ig_i^*}}{4kTR_n Y_{21}^*} = \Re(Y_{11}) + j\Im(Y_{11}) + \frac{S_{ig_i^*} \cdot \Im(Y_{21}) - jS_{ig_i^*} \cdot \Re(Y_{21})}{4kTR_n |Y_{21}|^2} \quad (5.42)$$

$$G_{cor} = \Re(Y_{11}) + \frac{S_{ig_i^*} \cdot \Im(Y_{21})}{4kTR_n |Y_{21}|^2} \quad (5.43)$$

$$B_{cor} = \text{Im}(Y_{11}) - \frac{S_{ig} i_d^* \text{Re}(Y_{21})}{4kTR_n |Y_{21}|^2} \quad (5.44)$$

From (5.39),

$$G_{cor} + jB_{cor} = \frac{F_{min}-1}{2R_n} - G_{opt} - jB_{opt}. \quad (5.45)$$

The imaginary part of the optimum source admittance B_{opt} can be obtained from (5.45) to be (5.46).

$$B_{opt} = -B_{cor} \quad (5.46)$$

From

$$Y_{opt} = G_{opt} + jB_{opt}, \quad (5.47)$$

the real part of the optimum source admittance G_{opt} can be calculated to be

$$G_{opt} = \left(|Y_{opt}|^2 - B_{opt}^2 \right)^{\frac{1}{2}} \quad (5.48)$$

where $|Y_{opt}|^2$ can be obtained from (5.37).

$$|Y_{opt}|^2 = \frac{S_{ig}}{4kTR_n} - |Y_{11}|^2 + 2[\text{Re}(Y_{11})G_{cor} + \text{Im}(Y_{11})B_{cor}] \quad (5.49)$$

The minimum noise factor F_{min} can be expressed as (5.50).

$$F_{min} = 1 + 2R_n(Y_{cor} + Y_{opt}) = 1 + 2R_n(G_{cor} + G_{opt}) \quad (5.50)$$

The noise figure at 50Ω source impedance NF_{50} can be calculated from the minimum noise figure using (2.29).

$$F_{50} = F_{min} + \frac{\left| \frac{1}{50} - Y_{opt} \right|^2 R_n}{\frac{1}{50}} = F_{min} + \frac{\left(\frac{1}{50} - G_{opt} \right)^2 + (-B_{opt})^2}{\frac{1}{50}} R_n \quad (5.51)$$

$$NF_{50} = 10 \log F_{50} \quad (5.52)$$

5.3 Model Parameters Extraction

Figure 5.2 Small signal equivalent circuit of MOSFET including the gate-to-substrate and the drain-to-substrate networks for small signal analysis and model parameters extraction [45].

Figure 5.3 Simplified small signal equivalent circuit of MOSFET including the drain-to-substrate network, with the gate-to-substrate network is eliminated for simplicity [45].

Figure 5.2 shows the proposed small signal equivalent circuit of a MOSFET with the proposed gate-to-substrate and drain-to-substrate networks, for small signal analysis and model parameters extraction. In Figure 5.2, R_g is the gate resistance, C_{gs} is the gate-to-source capacitance and C_{sd} is the source-to-drain capacitance. C_{gd} and C_{dg} are two non-reciprocal capacitances caused by the drain and gate voltage, with C_{gd} is the capacitance effect on the gate due to the drain terminal and C_{dg} is the capacitance effect on the drain due to the gate terminal. The transcapacitance $C_m = C_{dg} - C_{gd}$ is used to capture the different capacitance effect between the gate and drain terminals by each other [59, 60]. The parameter g_m is the transconductance of the MOSFET, g_{mb} is the bulk transconductance of the MOSFET and g_{ds} is the output conductance of the MOSFET. Here, the proposed drain-to-substrate network includes the substrate resistance R_{bb} , the substrate capacitance C_{bb} and the drain-to-bulk capacitance C_{db} , while the proposed gate-to-substrate network includes the substrate resistance R_{bb} , the substrate capacitance C_{bb} and the gate-to-bulk capacitance C_{gb} . In order to extract the parameter values of g_{mb} , R_{bb} and C_{bb} from small signal Y-parameter analysis, a noiseless RC substrate network is added to the drain side of the sub-circuit, through the drain junction capacitance C_{db} , and a current source $g_{mb}V_{bs}$ is added to the drain-to-source network. With this configuration, the model parameters can be extracted by performing detailed analysis on Y_{22} , which will be demonstrated in the following extraction. The substrate thermal noise can be calculated at the node V_b , and thereafter being transferred to drain side via the current source $g_{mb}V_{bs}$.

The presence of the gate-to-substrate admittance Y_{gb} will cause non-linearity of the imaginary part of Y_{11} in frequency domain. Nevertheless, the linear trend of the

measured $Im(Y_{11})$ versus frequency leads to the fact that $Y_{gb} \ll \omega(C_{gs} + C_{gd})$, and the gate-to-substrate admittance Y_{gb} can be assumed to be negligible for simplicity. Thus, the small signal equivalent circuit in Figure 5.2 can be simplified and redrawn in Figure 5.3.

Y-parameters analysis [61] is performed on the simplified small signal equivalent circuit in Figure 5.3, and the Y-parameters equations are derived as shown in (5.53) to (5.58) [45]. The detailed analysis of Y-parameters and their definitions are demonstrated in Appendix C.

$$Y_{11} = \frac{\omega^2(C_{gd}+C_{gs})^2 R_g + j\omega(C_{gd}+C_{gs})}{1 + \omega^2 R_g^2 (C_{gd}+C_{gs})^2} \quad (5.53)$$

$$Y_{12} = \frac{-\omega^2 C_{gd}(C_{gd}+C_{gs})R_g - j\omega C_{gd}}{1 + \omega^2 R_g^2 (C_{gd}+C_{gs})^2} \quad (5.54)$$

$$Y_{21} = \frac{g_m - \omega^2 C_{dg}(C_{gd}+C_{gs})R_g - j\omega[(C_{gd}+C_{gs})R_g g_m + C_{dg}]}{1 + \omega^2 R_g^2 (C_{gd}+C_{gs})^2} \quad (5.55)$$

$$Y_{22} = Y_{sub} + g_{ds} + j\omega(C_{sd} + C_{gd}) + g_{mb} \left[\frac{V_{bs}}{V_{ds}} \right] + \frac{\omega^2 C_{gd} R_g [(C_{gd}+C_{gs})R_g g_m + C_{dg}] + j\omega C_{gd} R_g [g_m - \omega^2 C_{gd} R_g (C_{gd}+C_{gs})]}{1 + \omega^2 R_g^2 (C_{gd}+C_{gs})^2} \quad (5.56)$$

where

$$\frac{V_{bs}}{V_{ds}} = Y_{sub} \left[\frac{(1 - j\omega C_{bb} R_{bb}) R_{bb}}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \right] \quad (5.57)$$

$$Y_{sub} = \frac{\omega^2 R_{bb} C_{db}^2}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2} + \frac{j\omega C_{db} + j\omega^3 R_{bb}^2 C_{db} C_{bb} (C_{db} + C_{bb})}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2} \quad (5.58)$$

Using the simplified small signal equivalent circuit in Figure 5.3, an extraction technique is proposed to extract the small signal parameters in the circuit by using the on-wafer measured Y-parameters. The small signal parameters in Figure 5.3 can be extracted from the on-wafer Y-parameter measurement data. For the following parameters extraction, the NMOS of channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at biasing voltage $V_{GS} = V_{DS} = 1.2 V$ will be used as an example. The gate resistance R_g , the gate-to-source capacitance C_{gs} and the gate-to-drain capacitance C_{gd} can be extracted from Y_{11} of (5.53) and Y_{12} of (5.54). For simplicity, an assumption is made in such that

$$\omega^2 R_g^2 (C_{gd} + C_{gs})^2 \ll 1. \quad (5.59)$$

The gate-to-drain capacitance C_{gd} can be obtained from the slope of the plot $Im(Y_{12})$ versus ω , as shown in Figure 5.4.

Figure 5.4 Plot of $Im(Y_{12})$ versus ω . The symbol is the measurement data and the line denotes the slope of the plot, from which the gate-to-drain capacitance $-C_{gd}$ can be obtained.

Figure 5.5 Plot of $Im(Y_{11}) + Im(Y_{12})$ versus ω , with the slope is the gate-to-source capacitance C_{gs} .

Meanwhile, the gate-to-source capacitance C_{gs} can be obtained from the slope of the plot $Im(Y_{11}) + Im(Y_{12})$ versus ω , as illustrated in Figure 5.5.

$$C_{gs} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega} \quad (5.61)$$

Figure 5.6 Plot of $Re(Y_{11})$ against $[Im(Y_{11})]^2$, with the slope is the gate resistance R_g .

By plotting $Re(Y_{11})$ against $[Im(Y_{11})]^2$ in Figure 5.6, the slope of the plot is the gate resistance R_g .

$$R_g = \frac{Re(Y_{11})}{[Im(Y_{11})]^2} \quad (5.62)$$

Thereafter, the assumption of (5.59) is verified using the extracted values of C_{gd} , C_{gs} , and R_g .

The transconductance of the MOSFET g_m and the drain-to-gate capacitance C_{dg} can be extracted from Y_{21} of (5.55). The assumption of (5.59) is applied here as well for simplicity. $Re(Y_{21})$ is plotted against ω^2 in Figure 5.7, and the transconductance of the MOSFET g_m is the value of $Re(Y_{21})$ when $\omega^2 = 0$ or the y-intercept point.

$$g_m = Re(Y_{21})|_{\omega^2=0} \quad (5.63)$$

Figure 5.7 Plot of $Re(Y_{21})$ against ω^2 , with the transconductance of the MOSFET g_m is the y-intercept point.

$Im(Y_{21})$ is plotted against ω in Figure 5.8, and the slope m_1 is used to calculate the drain-to-gate capacitance C_{dg} .

$$m_1 = -[(C_{gd} + C_{gs})R_g g_m + C_{dg}] \quad (5.64)$$

$$C_{dg} = -m_1 - (C_{gd} + C_{gs})R_g g_m \quad (5.65)$$

Figure 5.8 Plot of $Im(Y_{21})$ against ω , with the slope m_1 is used to calculate the drain-to-gate capacitance C_{dg} .

After that, the source-to-drain capacitance C_{sd} , the bulk transconductance g_{mb} and the proposed drain-to-substrate network which consists of substrate resistance R_{bb} , substrate capacitance C_{bb} and drain-to-bulk capacitance C_{db} , can be extracted from Y_{22} of (5.56). $Re(Y_{22})$ versus ω^2 is plotted in Figure 5.9, and the output conductance g_{ds} is the value of $Re(Y_{22})$ when $\omega^2 = 0$ or the y-intercept point.

$$g_{ds} = Re(Y_{22})|_{\omega^2=0} \quad (5.66)$$

Figure 5.9 Plot of $Re(Y_{22})$ against ω^2 , with the output conductance of the MOSFET g_{ds} is the y-intercept point.

The portion of (5.56) which consists of the parameters extracted in (5.59) to (5.65) is renamed as Y_a .

$$Y_a = \frac{\omega^2 C_{gd} R_g [(C_{gd} + C_{gs}) R_g g_m + C_{dg}] + j\omega C_{gd} R_g [g_m - \omega^2 C_{gd} R_g (C_{gd} + C_{gs})]}{1 + \omega^2 R_g^2 (C_{gd} + C_{gs})^2} \quad (5.67)$$

Together with (5.67), (5.56) can be rearranged to be (5.68).

$$Y_{22} - Y_a = g_{ds} + j\omega (C_{sd} + C_{gd}) + \left[1 + \frac{g_{mb} R_{bb} (1 - j\omega C_{bb} R_{bb})}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \right] \times \left[\frac{\omega^2 R_{bb} C_{db}^2}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2} + \frac{j\omega C_{db} + j\omega^3 R_{bb}^2 C_{db} C_{bb} (C_{db} + C_{bb})}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2} \right] \quad (5.68)$$

Let the R represents the real parts and I represents the imaginary parts, in such that

$$R = Re(Y_{22}) - g_{ds} - Re(Y_a) \quad (5.69)$$

$$I = Im(Y_{22}) - \omega C_{gd} - Im(Y_a) \quad (5.70)$$

it can be derived that

$$R + jI = \left[1 + \frac{g_{mb}R_{bb}(1-j\omega C_{bb}R_{bb})}{1+\omega^2 R_{bb}^2 C_{bb}^2} \right] \times \left[\frac{\omega^2 R_{bb} C_{db}^2}{1+\omega^2 R_{bb}^2 (C_{db}+C_{bb})^2} + \frac{j\omega C_{db} + j\omega^3 R_{bb}^2 C_{db} C_{bb} (C_{db}+C_{bb})}{1+\omega^2 R_{bb}^2 (C_{db}+C_{bb})^2} \right] + j\omega C_{sd}. \quad (5.71)$$

(5.71) is rearranged to become (5.72) and expanded to (5.73).

$$\begin{aligned} & [R + jI - j\omega C_{sd}][1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2][1 + \omega^2 R_{bb}^2 C_{bb}^2] \\ &= [\omega^2 R_{bb} C_{db}^2 + j\omega C_{db} + j\omega^3 R_{bb}^2 C_{db} C_{bb} (C_{db} + C_{bb})] \\ & \quad \times [1 + \omega^2 R_{bb}^2 C_{bb}^2 + g_{mb}R_{bb}(1 - j\omega C_{bb}R_{bb})] \end{aligned} \quad (5.72)$$

$$\begin{aligned} & [R + jI - j\omega C_{sd}] \\ & \quad \times [1 + \omega^2 R_{bb}^2 C_{bb}^2 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2 + \omega^4 R_{bb}^4 C_{bb}^2 (C_{db} + C_{bb})^2] \\ &= \omega^4 R_{bb}^3 C_{db} C_{bb}^2 [g_{mb}R_{bb}(C_{db} + C_{bb}) + C_{db}] \\ & \quad + \omega^2 R_{bb} C_{db} [g_{mb}R_{bb}(C_{db} + C_{bb}) + C_{db}] + j\omega^5 R_{bb}^4 C_{db} C_{bb}^3 (C_{db} + C_{bb}) \\ & \quad + j\omega^3 R_{bb}^2 C_{db} C_{bb} [C_{db} + C_{bb} + C_{bb}(1 + g_{mb}R_{bb})] + j\omega C_{db}(1 + g_{mb}R_{bb}) \end{aligned} \quad (5.73)$$

Here, the source-to-drain capacitance C_{sd} is being ignored first to simplify the parameter extraction, and (5.74) can be obtained.

$$[R + jI][1 + \omega^2 c + \omega^4 d] = \omega^4 a + \omega^2 b + j[\omega^5 e + \omega^3 f + \omega g] \quad (5.74)$$

with

$$a = R_{bb}^3 C_{db} C_{bb}^2 [C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}] \quad (5.75)$$

$$b = R_{bb} C_{db} [C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}] \quad (5.76)$$

$$c = R_{bb}^2 [C_{bb}^2 + (C_{db} + C_{bb})^2] \quad (5.77)$$

$$d = R_{bb}^4 C_{bb}^2 (C_{db} + C_{bb})^2 \quad (5.78)$$

$$e = R_{bb}^4 C_{db} C_{bb}^3 (C_{db} + C_{bb}) \quad (5.79)$$

$$f = R_{bb}^2 C_{db} C_{bb} [C_{db} + C_{bb} + C_{bb} (1 + g_{mb} R_{bb})] \quad (5.80)$$

$$g = C_{db} (1 + g_{mb} R_{bb}) \quad (5.81)$$

The real part of (5.74) is (5.82) while the imaginary part of (5.74) is (5.83).

$$R = \frac{\omega^4 a + \omega^2 b}{1 + \omega^2 c + \omega^4 d} \quad (5.82)$$

$$I = \frac{\omega^5 e + \omega^3 f + \omega g}{1 + \omega^2 c + \omega^4 d} \quad (5.83)$$

At high frequencies,

$$\frac{\omega^2}{R} = \frac{1 + \omega^2 c + \omega^4 d}{\omega^2 a + b} \approx \omega^2 \frac{d}{a} + \frac{c}{a} = \omega^2 m_r + c_r \quad (5.84)$$

$$\omega \frac{I}{R} = \frac{\omega^4 e + \omega^2 f + g}{\omega^2 a + b} \approx \omega^2 \frac{e}{a} + \frac{f}{a} = \omega^2 m_i + c_i \quad (5.85)$$

$\frac{\omega^2}{R}$ and $\omega \frac{I}{R}$ are plotted versus ω^2 in Figure 5.10 and Figure 5.11 respectively. Their slope m_r and m_i , and their y-intercept point c_r and c_i , will be used to extract g_{mb} , R_{bb} , C_{bb} and C_{db} .

Figure 5.10 Plot of $\frac{\omega^2}{R}$ versus ω^2 , with slope of m_r and y-intercept point of c_r

Figure 5.11 Plot of $\frac{\omega}{R}$ versus ω^2 , with slope of m_i and y-intercept point of c_i

$$m_r = \frac{d}{a} = \frac{R_{bb}}{C_{db}} \left[\frac{(C_{db} + C_{bb})^2}{C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}} \right] \quad (5.86)$$

$$c_r = \frac{c}{a} = \frac{1}{R_{bb}C_{db}C_{bb}^2} \left[\frac{C_{bb}^2 + (C_{db} + C_{bb})^2}{C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}} \right] \quad (5.87)$$

$$m_i = \frac{e}{a} = R_{bb}C_{bb} \left[\frac{C_{db} + C_{bb}}{C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}} \right] \quad (5.88)$$

$$c_i = \frac{f}{a} = \frac{1}{R_{bb}C_{bb}} \left[\frac{C_{db} + C_{bb} + C_{bb}(1 + g_{mb}R_{bb})}{C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}} \right] \quad (5.89)$$

Combining (5.86) and (5.88), it can be derived that

$$\frac{m_i}{m_r} = \frac{C_{db}C_{bb}}{C_{db} + C_{bb}} \quad (5.90)$$

Since $C_{bb} \gg C_{db}$, the drain-to-bulk capacitance C_{db} can be derived to be (5.91).

$$C_{db} = \frac{m_i}{m_r} \quad (5.91)$$

From series expansion of (5.83) at low frequencies, it can be seen that

$$I = \omega g + \omega^3(f - cg) + \dots \approx \omega g + \omega^3(f - cg) \quad (5.92)$$

$$\frac{I}{\omega} = g + \omega^2(f - cg). \quad (5.93)$$

Figure 5.12 Plot of $\frac{I}{\omega}$ versus ω^2 , with the y-intercept point is g .

Figure 5.12 shows the plot of $\frac{I}{\omega}$ versus ω^2 , in which the y-intercept point is g . With the value of g in Figure 5.12, C_{db} in (5.91) and (5.81), $g_{mb}R_{bb}$ can be calculated as shown in (5.94).

$$g_{mb}R_{bb} = \frac{g}{c_{db}} - 1 \quad (5.94)$$

After that, (5.86) and (5.87) is combined, in such that

$$\frac{m_r}{c_r} = R_{bb}^2 C_{bb}^2 \left[\frac{(C_{db} + C_{bb})^2}{C_{bb}^2 + (C_{db} + C_{bb})^2} \right] \quad (5.95)$$

$$R_{bb}^2 C_{bb}^2 = \frac{m_r}{c_r} \left[\frac{C_{bb}^2 + (C_{db} + C_{bb})^2}{(C_{db} + C_{bb})^2} \right]. \quad (5.96)$$

Together with (5.88), it can be derived that

$$m_i^2 = R_{bb}^2 C_{bb}^2 \left[\frac{C_{db} + C_{bb}}{C_{db}(1 + g_{mb}R_{bb}) + g_{mb}R_{bb}C_{bb}} \right]^2 \quad (5.97)$$

$$m_i^2 = \frac{m_r}{c_r} \left[\frac{C_{bb}^2 + (C_{db} + C_{bb})^2}{C_{db}^2(1 + g_{mb}R_{bb})^2 + (g_{mb}R_{bb}C_{bb})^2 + 2C_{db}(1 + g_{mb}R_{bb})(g_{mb}R_{bb}C_{bb})} \right] \quad (5.98)$$

Rearranging (5.98) to be function of C_{bb} , (5.99) and (5.100) can be obtained.

$$\begin{aligned} C_{bb}^2 \left[2 - \frac{m_i^2 c_r}{m_r} (g_{mb}R_{bb})^2 \right] + C_{bb} \left[2C_{db} - 2 \left(\frac{m_i^2 c_r}{m_r} \right) (g_{mb}R_{bb}C_{db})(1 + g_{mb}R_{bb}) \right] \\ + C_{db}^2 \left[1 - \left(\frac{m_i^2 c_r}{m_r} \right) (1 + g_{mb}R_{bb})^2 \right] = 0 \end{aligned} \quad (5.99)$$

$$pC_{bb}^2 + qC_{bb} + r = 0 \quad (5.100)$$

with

$$p = 2 - \frac{m_i^2 c_r}{m_r} (g_{mb}R_{bb})^2 \quad (5.101)$$

$$q = 2C_{db} - 2 \left(\frac{m_i^2 c_r}{m_r} \right) (g_{mb}R_{bb}C_{db})(1 + g_{mb}R_{bb}) \quad (5.102)$$

$$r = C_{db}^2 \left[1 - \left(\frac{m_i^2 c_r}{m_r} \right) (1 + g_{mb}R_{bb})^2 \right] \quad (5.103)$$

Since $C_{bb} > 0$, the substrate capacitance C_{bb} can be calculated to be (5.104).

$$C_{bb} = \frac{-q + \sqrt{q^2 - 4pr}}{2p} \quad (5.104)$$

Thereafter the substrate resistance R_{bb} and the bulk transconductance g_{mb} can be calculated to be (5.106) and (5.107) respectively.

$$R_{bb} = \frac{1}{C_{bb}} \sqrt{\frac{m_r}{c_r} \left[\frac{C_{bb}^2 + (C_{db} + C_{bb})^2}{(C_{db} + C_{bb})^2} \right]} \quad (5.105)$$

$$R_{bb} = \frac{1}{C_{bb}(C_{db} + C_{bb})} \sqrt{\frac{m_r}{c_r} [C_{bb}^2 + (C_{db} + C_{bb})^2]} \quad (5.106)$$

$$g_{mb} = \frac{1}{R_{bb}} \left[\frac{g}{C_{db}} - 1 \right] \quad (5.107)$$

Figure 5.13 Plot of $I - \frac{\omega^5 e + \omega^3 f + \omega g}{1 + \omega^2 c + \omega^4 d}$ versus ω , with slope is the source-to-drain capacitance C_{sd} .

In previous steps of (5.74) to (5.107), the source-to-drain capacitance C_{sd} is ignored for simplicity in the extraction of C_{db} , C_{bb} , R_{bb} and g_{mb} , and (5.74) is obtained. Putting back the C_{sd} to (5.74), (5.83) can be modified to become (5.108).

$$I - \frac{\omega^5 e + \omega^3 f + \omega g}{1 + \omega^2 c + \omega^4 d} = \omega C_{sd} \quad (5.108)$$

$I - \frac{\omega^5 e + \omega^3 f + \omega g}{1 + \omega^2 c + \omega^4 d}$ is plotted versus ω in Figure 5.13, and the source-to-drain capacitance C_{sd} is the slope of the plot.

The extracted small signal parameters for output admittance Y_{22} , which are g_{mb} , R_{bb} , C_{bb} , C_{db} , and C_{sd} are optimized to accurately describe the output admittance and the drain current noise characteristic. The extracted and optimized value of these parameters will be compared in next section.

5.4 Experimental Results and Discussion

The Y-parameters calculated from the extracted model parameters in the small signal equivalent circuit in Fig. 5.3 is verified with the on-wafer measurement Y-parameters in Fig. 5.14. The model verification is done on the NMOS of channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at biasing voltage $V_{GS} = V_{DS} = 1.2 V$. Good agreement between the simulated and measured Y-parameters indicates that the model parameters extracted are of appropriate values.

Figure 5.14 Y-parameters versus frequency for NMOS of $L/W = 0.13\mu m/20\mu m$ at $V_{GS} = V_{DS} = 1.2 V$. The measurement results and the simulation results are represented by symbols and lines respectively. Good agreement between the extracted and the simulated Y-parameter is achieved [45].

Table 5.1 Comparison of the extracted and the optimized values of the small signal model parameters for NMOS of $L/W = 0.13\mu m/20\mu m$ at $V_{GS} = V_{DS} = 1.2 V$ [45]

Model Parameter	Extracted Value	Optimized Value
g_{mb} , mS	4.23	4.5
R_{bb} ($\times 10^2$), Ω	5.22	5.5
C_{db} , fF	6.24	5.7
C_{bb} , fF	42.7	42.7
C_{sd} , fF	3.13	3.13

The extracted small signal parameters for output admittance Y_{22} are optimized to best predict the output admittance and drain current noise performance. The comparison between the extracted small signal parameters and their optimized values for NMOS with channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at biasing voltage $V_{GS} = V_{DS} = 1.2 V$ are shown in Table 5.1. It can be seen that the optimized values and the extracted values are in the same order of magnitude and they are comparable. Meanwhile, the values for all the small signal model parameters of NMOS with channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$ are shown in Table 5.2. By using the same extraction technique, the model parameters at other biasing conditions and dimensions can be obtained.

Table 5.2 The small signal model parameters for NMOS of $L/W = 0.13\mu m/20\mu m$ at $V_{GS} = V_{DS} = 1.2 V$

Model Parameter	Value
R_g, Ω	16.6
C_{gs}, fF	22.5
C_{gd}, fF	9.95
C_{dg}, fF	14.6
g_m, mS	16.0
g_{ds}, mS	1.4
g_{mb}, mS	4.5
$R_{bb} (\times 10^2), \Omega$	5.5
C_{db}, fF	5.7
C_{bb}, fF	42.7
C_{sd}, fF	3.13

Fig. 5.15 illustrates the comparison of the channel thermal noise, the substrate-induced drain current noise, the gate resistance thermal noise at drain terminal, and their summation, with the measurement data in frequency domain. The comparison is done on the NMOS with channel length $L = 0.13 \mu m$ and channel width $W = 20 \mu m$, at biasing voltage $V_{GS} = V_{DS} = 1.2 V$. The log scale of Fig. 5.15(a) is depicted in Fig. 5.15(b). It can be observed that the drain current noise is frequency dependent and the white channel thermal noise is no longer sufficient to explain its characteristic. Such characteristic can be predicted well by the proposed substrate-induced drain current noise model. For short channel MOSFET, the substrate-induced drain current noise become significant since it is in the same order of magnitude with the channel thermal noise. The substrate network consisting of a substrate resistance and a substrate capacitance act like a low pass filter in such that the substrate-induced drain current noise decreases with frequency, as illustrated in Fig. 5.15(b). It can be expected that at higher frequencies of tens of GHz, the substrate-induced drain current noise become negligible as compared to the channel thermal noise. Consequently, the drain current noise exhibits white noise characteristic at higher frequencies.

(a)

(b)

Figure 5.15 Drain current noise versus frequency in (a) linear scale and in (b) log scale for NMOS of $L/W = 0.13\mu\text{m}/20\mu\text{m}$ at $V_{GS} = V_{DS} = 1.2 \text{ V}$. The measurement results and the simulation results are represented by symbols and lines respectively. By including the substrate-induced drain current noise, the frequency dependent characteristic of the drain current noise can be describe accurately [45]. In (b), the substrate-induced drain current noise shows the low pass filter characteristic with respect to frequency.

Figure 5.16 Drain current noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20 \mu\text{m}$, at $V_{GS} = V_{DS} = 1.2 \text{ V}$. The measurement results and the simulation results are represented by symbols and lines respectively. The frequency dependent characteristic for drain current noise is more substantial for shorter channel length devices [45].

The drain current noise, with and without substrate-induced drain current noise, versus frequency, for different channel length, is shown in Fig. 5.16. At longer channel length of $L = 0.50 \mu\text{m}$, only small difference between the drain current noise model with and without substrate-induced drain current noise can be observed. Hence, the drain current noise exhibits white noise characteristic, which is similar to channel thermal noise. When the channel length shrinks and the device bulk transconductance g_{mb} becomes larger, the frequency dependent characteristic starts to become more significant and cannot be ignored for simplicity. In fact, the substrate-induced drain current noise power spectral density is proportional to the square of g_{mb} . This is why the substrate-induced drain current noise at the drain terminal is larger, although the local voltage noise of the substrate is smaller in the short-channel device due to the smaller R_{bb} . In shorter length MOSFET, the control of the substrate or the “back-gate”

is larger just as the gate would, causing more noise to be transferred to the drain terminal. Up to 20% of error can be found at shorter channel length of $L = 0.13 \mu m$ if the frequency dependent substrate-induced drain current noise is not included in the drain current noise model. Hence, it is important to include the proposed substrate-induced drain current noise to improve the accuracy of the model.

In Figs. 5.17 and 5.18, the drain current noise model with and without substrate-induced drain current noise are compared with the measurement data, versus frequency for different gate voltage, and for different drain voltage, respectively. The device used is the NMOS with channel length of $L = 0.13 \mu m$ and channel width of $W = 40 \mu m$. From Figs. 5.17 and 5.18, it can be seen that the frequency dependent of the drain current noise is significant for all the gate voltages and drain voltages. With the incorporation of the substrate-induced drain current noise model, the noise prediction with respect to frequency can be greatly improved. Besides, the proposed model can capture the drain current noise characteristic accurately with respect to gate bias and drain bias at different frequency of 5 GHz and 15 GHz, as depicted in Figs. 5.19 and 5.20 respectively.

Figure 5.17 Drain current noise versus frequency for different gate bias, of NMOS of $L/W = 0.13\mu\text{m}/40\mu\text{m}$ at $V_{DS} = 1.2\text{ V}$. The measurement results and the simulation results are represented by symbols and lines respectively [45].

Figure 5.18 Drain current noise versus frequency for different drain bias, of NMOS of $L/W = 0.13\mu\text{m}/40\mu\text{m}$ at $V_{GS} = 1.2\text{ V}$. The measurement results and the simulation results are represented by symbols and lines respectively [45].

Figure 5.19 Drain current noise versus gate bias for NMOS of $L/W = 0.13\mu m/40\mu m$ at frequency of 5 GHz and 15 GHz. The measurement results and the simulation results are represented by symbols and lines respectively.

Figure 5.20 Drain current noise versus drain bias for NMOS of $L/W = 0.13\mu m/40\mu m$ at frequency of 5 GHz and 15 GHz. The measurement results and the simulation results are represented by symbols and lines respectively.

Figure 5.21 Gate current noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20\mu m$, at $V_{GS} = V_{DS} = 1.2 V$. The measurement results and the simulation results, which are represented by symbols and lines respectively, agree well with each other [45].

Figure 5.22 Cross-correlation between gate current noise and drain current noise versus frequency for NMOS of different channel length and channel width $W = 20\mu m$, at $V_{GS} = V_{DS} = 1.2 V$. The measurement results and the simulation results, which are represented by symbols and lines respectively, agree well with each other [45].

The comparison of the gate current noise model and its cross-correlation with drain current noise model, with the measurement data, versus frequency for different channel length, is illustrated in Figs. 5.21 and 5.22 respectively. When the channel length is scaled down, both of the gate resistance noise and the induced gate noise decrease. As compared to the gate resistance noise, the induced gate noise, which is proportional to L_{eff}^3 , decreases faster with the down-scaling of channel length. Therefore, for short channel devices, the gate current noise level is much lower than the drain current noise level. This causes the gate current noise to have lesser impact on the overall noise performance of short channel MOSFETs. Meanwhile, the cross-correlation term presents the similar phenomenon in Fig. 5.22. Moreover, both the gate current noise and the cross-correlation term show the increasing trend with frequency. From Figs. 5.21 and 5.22, it can be observed that good agreement between the measurement data and the modeled values can be acquired.

The noise figure at 50 Ω source resistance with and without the substrate-induced drain current noise is compared with the measurement data versus frequency in Fig. 5.23, while the normalized noise resistance with and without the substrate-induced drain current noise is compared with the measurement data versus frequency in Fig. 5.24. It is demonstrated that by including the proposed substrate-induced drain current noise, the modeling of the NF_{50} and R_n normalized can be greatly improved, with the correct trend with respect to frequency can be obtained. This is important for IC designer to predict and optimize their circuit performance.

Figure 5.23 The noise figure at $50\ \Omega$ source resistance versus frequency for NMOS of different channel length and channel width $W = 20\ \mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\ \text{V}$. The measurement results and the simulation results are represented by symbols and lines respectively. By including substrate-induced drain current noise, great improvement can be achieved [45].

Figure 5.24 The normalized noise resistance versus frequency for NMOS of different channel length and channel width $W = 20\ \mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\ \text{V}$. The measurement results and the simulation results are represented by symbols and lines respectively. By including substrate-induced drain current noise, great improvement can be achieved [45].

Figure 5.25 The minimum noise figure versus frequency for NMOS of different channel length and channel width $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{ V}$. The measurement results and the simulation results, which are represented by symbols and lines respectively, agree well with each other [45].

Figure 5.26 The optimum source admittance versus frequency for NMOS of different channel length and channel width $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{ V}$. The measurement results and the simulation results, which are represented by symbols and lines respectively, agree well with each other [45].

Figs. 5.25 and 5.26 show the minimum noise figure NF_{min} and optimum source admittance Y_{opt} , for different channel length, versus frequency, of NMOS with $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{ V}$. The simulation results are demonstrated to agree well with the on-wafer measurement results. Thus, the high frequency noise performance of NMOS can be modeled accurately with the proposed noise models.

5.5 Conclusion

In this chapter, a substrate-induced drain current noise was introduced to explain the frequency dependencies of the drain current noise. A model parameter extraction technique was proposed by utilizing a small signal equivalent circuit. The frequency dependent behavior observed in the drain current noise has been captured in the proposed model which is verified with measurement data. The noise figure at $50\ \Omega$ source resistance and noise resistance were computed and verified experimentally. Excellent agreement was found between the measured data and the simulated noise values shows that the proposed noise model is accurate and the model parameters are well extracted. By including the substrate-induced drain current noise model, the model accuracy of the drain current noise and four noise parameters has been improved significantly, especially for shorter channel length devices.

Chapter 6 Summary of Proposed Noise Models

6.1 Overview

In this chapter, the proposed drain current noise model, gate current noise model and their correlation are summarized. Thereafter, four noise parameters are calculated based on the proposed drain current noise model, gate current noise model and their correlation.

The proposed noise models and four noise parameters are verified with on-wafer Y-parameters and noise parameters measurement results, and found to agree well.

6.2 Model Formulation

6.2.1 Drain Current Noise Model

The proposed total drain current noise model S_{i_d} is given by (6.1), which consists of the channel thermal noise $S_{i_{d_ch}}$, substrate-induced drain current noise $S_{i_{d_sub}}$, and gate resistance thermal noise $S_{i_{d_Rg}}$. The channel thermal noise $S_{i_{d_ch}}$ of (6.2) takes into account the short channel effects, which are channel length modulation, velocity saturation and hot carrier effects, while the drain-induced vertical field effect (DIVF) is included in the effective mobility equation of (6.5). It is found that the noise reduction due to the velocity saturation effect can cancel out the noise increment due to the hot carrier effect. Meanwhile, the substrate-induced drain current noise model of (6.3) is introduced to model the frequency dependent characteristic for short channel

RF MOSFETs. The small signal parameters in (6.3) can be extracted using the parameter extraction technique demonstrated in Section 5.3.

$$S_{i_d} = S_{i_d\text{-}ch} + S_{i_d\text{-}sub} + S_{i_d\text{-}Rg} \quad (6.1)$$

where

$$S_{i_d\text{-}ctn} = 4kT \left(\frac{W}{L_{eff}} \mu_{eff} C'_{ox} \right) \left(\frac{V_{GT}^2 - \alpha V_{GT} V_{DSeff} + \frac{\alpha^2}{3} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (6.2)$$

$$S_{i_d\text{-}sub} = \frac{4kT g_{mb}^2 R_{bb}}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \quad (6.3)$$

$$S_{i_d\text{-}Rg} = 4kT g_m^2 R_g \quad (6.4)$$

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 V_{GT} + \left[\sqrt{\frac{\theta_2}{L}} - \theta_1 \left(1 - \frac{\alpha}{2} \right) \right] V_{DS}} \quad (6.5)$$

$$L_{eff} = L - \Delta L \quad (6.6)$$

$$\Delta L = \frac{1}{\alpha_y} \ln \left[\frac{\alpha_y (V_{DS} - V_{DSat}) + E_D}{E_c} \right] \quad (6.7)$$

$$E_D = E_c \sqrt{1 + \left[\frac{\alpha_y (V_{DS} - V_{DSat})}{E_c} \right]^2} \quad (6.8)$$

$$\alpha_y = \lambda \sqrt{\frac{3}{2} \frac{C'_{ox}}{x_j \epsilon_{si} \epsilon_0}} \quad (6.9)$$

$$E_c = \frac{2v_{sat}}{u_{eff}} \quad (6.10)$$

$$V_{GT} = V_{GS} - V_T \quad (6.11)$$

$$V_{DSeff} = V_{DSSat} - \frac{1}{2} \left[V_{DSSat} - V_{DS} - \delta_s + \sqrt{(V_{DSat} - V_{DS} - \delta_s)^2 + 4\delta_s V_{DSSat}} \right] \quad (6.12)$$

$$V_{DSat} = \frac{1}{1 + \frac{V_{GT}}{E_c L}} \left(\frac{V_{GT}}{\alpha} \right) \quad (6.13)$$

Here, C'_{ox} is oxide capacitance per unit area, α is bulk charge coefficient, μ_0 is low field mobility, θ_1 and θ_2 are fitting parameters, g_{mb} is bulk transconductance, R_{bb} is substrate resistance, C_{bb} is substrate capacitance, λ is a fitting parameter to account for channel length modulation effect, x_j is junction depth, ϵ_{si} is silicon dielectric constant, ϵ_0 is vacuum permittivity, v_{sat} is carrier saturated velocity.

6.2.2 Gate Current Noise Model

The proposed model of total gate current noise S_{i_g} is given by (6.14), which consists of the channel induced gate noise and gate current noise generated by the gate resistance. The substrate-induced gate current noise $S_{i_{g-sub}}$ is negligible compared to the channel induced gate noise $S_{i_{g-ch}}$ because the gate-bulk capacitance C_{gb} is very small.

$$S_{i_g} = S_{i_{g-ch}} + S_{i_{g-Rg}} \quad (6.14)$$

$$S_{i_{g-ch}} = \frac{4kT\omega^2 W^4 C_{ox}'^4 \mu_{eff}^2}{I_{DS}^3 \left(1 + \frac{V_{DSeff}}{E_c L_{eff}}\right)} \left[\frac{\alpha^2}{5} V_{DSeff}^5 - \frac{\alpha}{2} (\alpha V_{as} + V_{GT}) V_{DSeff}^4 + \frac{1}{3} (\alpha^2 V_{as}^2 + 4\alpha V_{GT} V_{as} + V_{GT}^2) V_{DSeff}^3 - V_{GT} V_{as} (\alpha V_{as} + V_{GT}) V_{DSeff}^2 + V_{GT}^2 V_{as}^2 V_{DSeff} \right] \quad (6.15)$$

where

$$I_{DS} = \frac{1}{1 + \frac{V_{DS}}{E_c L}} \mu_{eff} C_{ox}' \frac{W}{L_{eff}} \left(V_{GT} - \frac{\alpha}{2} V_{DSeff} \right) V_{DSeff} \quad (6.16)$$

$$V_{as} = V_{DSeff} + \frac{1}{E_c L_{eff}} \left(\frac{V_{DSeff}^2}{2} \right) - \left(1 + \frac{V_{DSeff}}{E_c L_{eff}} \right) \left(\frac{\frac{1}{2} V_{GT} V_{DSeff} - \frac{\alpha}{6} V_{DSeff}^2}{V_{GT} - \frac{\alpha}{2} V_{DSeff}} \right) \quad (6.17)$$

$$S_{i_{g-Rg}} = 4kT\omega^2 C_{gg}^2 R_g \quad (6.18)$$

6.2.3 Model of Correlation between Gate Current Noise and Drain Current Noise

The proposed model of correlation between the gate current noise and the drain current noise $S_{i_g i_d^*}$ is given by (6.19), which is contributed from the channel region and gate resistance thermal noise.

$$S_{i_g i_d^*} = S_{i_g i_{d-ch}^*} + S_{i_g i_{d-Rg}^*} \quad (6.19)$$

$$S_{i_g i_{d-ch}^*} = \frac{j4kT\omega W^3 C_{ox}^3 \mu_{eff}^2}{L_{eff} I_{DS}^2} \left(\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right) \left[-\frac{1}{4} \alpha^2 V_{DSeff}^4 + \frac{\alpha}{3} (\alpha V_{as} + 2V_{GT}) V_{DSeff}^3 \right. \\ \left. - \frac{V_{GT}}{2} (2\alpha V_{as} + V_{GT}) V_{DSeff}^2 + V_{GT}^2 V_{as} V_{DSeff} \right] \quad (6.20)$$

$$S_{i_g i_{d-Rg}^*} = j4kT\omega C_{gg} R_g g_m \quad (6.21)$$

6.2.4 Four Noise Parameters

Four noise parameters can be computed using the proposed current noise models and the calculated Y-parameters.

$$R_n = \frac{S_{i_d}}{4kT|Y_{21}|^2} = \frac{S_{i_d}}{4kT[(Re(Y_{21}))^2 + (Im(Y_{21}))^2]}. \quad (6.22)$$

$$G_{cor} = Re(Y_{11}) + \frac{S_{i_g i_d^*} \cdot Im(Y_{21})}{4kT R_n |Y_{21}|^2} \quad (6.23)$$

$$B_{cor} = Im(Y_{11}) - \frac{S_{i_g i_d^*} Re(Y_{21})}{4kT R_n |Y_{21}|^2} \quad (6.24)$$

$$B_{opt} = -B_{cor} \quad (6.25)$$

$$G_{opt} = \left(|Y_{opt}|^2 - B_{opt}^2 \right)^{\frac{1}{2}} \quad (6.26)$$

$$|Y_{opt}|^2 = \frac{S_{ig}}{4kTR_n} - |Y_{11}|^2 + 2[Re(Y_{11})G_{cor} + Im(Y_{11})B_{cor}] \quad (6.27)$$

$$NF_{min} = 1 + 2R_n(Y_{cor} + Y_{opt}) = 1 + 2R_n(G_{cor} + G_{opt}) \quad (6.28)$$

The noise figure at 50Ω source impedance NF_{50} can be calculated from the four noise parameters using (6.29) and (6.30).

$$F_{50} = F_{min} + \frac{|\frac{1}{50} - Y_{opt}|^2 R_n}{\frac{1}{50}} = F_{min} + \frac{(\frac{1}{50} - G_{opt})^2 + (-B_{opt})^2}{\frac{1}{50}} R_n \quad (6.29)$$

$$NF_{50} = 10 \log F_{50} \quad (6.30)$$

6.3 Model Verification

Figure 6.1 Y-parameters versus frequency for NMOS of $L/W = 0.13\mu m/20\mu m$ at $V_{GS} = V_{DS} = 1.2V$. Good agreement between the extracted and the simulated Y-parameter is achieved [45].

Y-parameters calculated using the proposed small signal parameter extraction method is verified with on-wafer measurement data in Figure 6.1.

Figures 6.2-6.10 demonstrate the model verification for the proposed drain current noise model, gate current noise model and their correlation against extracted noise results, in frequency, drain bias and gate bias domains, for different channel lengths and widths. The computed noise figure at 50Ω source impedance NF_{50} and noise resistance R_n are verified in Figures 6.11 and 6.12 respectively. Good agreement between the proposed models and silicon data are found, indicating the proposed models are accurate.

Figure 6.2 Drain current noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{ V}$.

Figure 6.3 Channel thermal noise power spectral density versus gate bias for NMOS of different channel length and channel width $W = 20 \mu\text{m}$.

Figure 6.4 Channel thermal noise power spectral density versus drain bias for NMOS of different channel length and channel width $W = 20 \mu\text{m}$.

Figure 6.5 Channel thermal noise power spectral density versus channel length, for NMOS of channel width $W = 20\mu\text{m}$, at $V_{GS} = V_{DS} = 1.2\text{V}$.

Figure 6.6 Drain current noise versus frequency for different gate bias, of NMOS of $L/W = 0.13\mu\text{m}/40\mu\text{m}$ at $V_{DS} = 1.2\text{V}$.

Figure 6.7 Drain current noise versus frequency for different drain bias, of NMOS of $L/W = 0.13\mu\text{m}/40\mu\text{m}$ at $V_{GS} = 1.2 \text{ V}$.

Figure 6.8 Channel thermal noise power spectral density versus gate bias for NMOS of different channel width and channel length $L = 0.13\mu\text{m}$.

Figure 6.9 Gate current noise power spectral density versus frequency for NMOS of different channel length and channel width $W = 20\mu m$, at $V_{GS} = V_{DS} = 1.2 V$.

Figure 6.10 Cross-correlation between gate current noise and drain current noise versus frequency for NMOS of different channel length and channel width $W = 20\mu m$, at $V_{GS} = V_{DS} = 1.2 V$.

Figure 6.11 The noise figure at 50 Ω source resistance versus frequency for NMOS of different channel length and channel width $W = 20 \mu m$, at $V_{GS} = V_{DS} = 1.2 V$.

Figure 6.12 The normalized noise resistance versus frequency for NMOS of different channel length and channel width $W = 20 \mu m$, at $V_{GS} = V_{DS} = 1.2 V$.

Chapter 7 Conclusion and Future Works

7.1 Summary

An accurate model for high frequency noise of MOSFETs is crucial for the designer to predict and optimize RF integrated circuit and system performance. The purpose of this research is to develop a scalable model to accurately predict the noise performance of the sub-micron RFCMOS transistors across different operating conditions such as frequency, gate bias and drain bias, and different dimensions such as channel length and channel width.

Several published models with short channel effects were reviewed. The impact of the short channel effects such as channel length modulation, velocity saturation effect and hot carrier effect on the channel thermal noise model are evaluated. The channel thermal noise model was derived to include such short channel effects in four different cases; that are by including only the channel length modulation, with both channel length modulation and velocity saturation effect, with channel length modulation and hot carrier effect and the last case is to include all three effects. The experimental results show that by including the carrier heating effect and the channel length modulation effect, the models overestimate the channel thermal noise. On the other hand, by including the velocity saturation effect and the channel length modulation effect, the model underestimates the channel thermal noise. In fact, the noise reduction due to the velocity saturation effect can cancel out the noise increment due to the carrier heating effect. Apparently, excluding these two effects and considering only the channel length modulation yielded the same result as including all

three effects in the channel thermal noise modeling. For the sake of simplicity and accuracy of the model, it is proposed to include channel length modulation effect only in the noise model.

In this work, a new effective mobility model was formulated and incorporated in the proposed channel thermal noise model of deep sub-micron MOSFETs. The model includes the mobility degradation effect due to the vertical field. The drain-induced vertical field was introduced and found to be additive to the average vertical field and hence further degrades the carrier mobility. The incorporating of the proposed mobility model in the noise model improved the model accuracy of predicting drain bias dependencies of the channel thermal noise. The improvement is great especially in short-channel device. Applying the proposed effective mobility model, the proposed channel thermal noise model was verified to have excellent agreement with the measured data for all operating conditions such as frequencies, gate biases and drain biases, as well as for all dimensions. Besides, the scalability of the model was demonstrated. The analytical model is simple and easy to be implemented in the simulation environment.

The substrate-induced drain current noise model was derived from the proposed small signal substrate network model. A new model parameter extraction technique was presented. The drain current noise model was formulated by summing the channel thermal noise, the gate resistance thermal noise, and the proposed substrate-induced drain current noise at drain terminal. The model accuracy was significantly improved especially in frequency domain. Moreover, the noise model was found to be more accurate in gate bias and drain bias domain at few GHz range. The proposed model was

capable to capture the frequency dependencies of the drain current noise, by including the substrate-induced drain current noise. As the channel length is scaled down, substrate-induced drain current noise becomes more prominent. Excellent match with on-wafer measurement data was obtained for drain current noise, gate current noise, their cross-correlation term and all the four noise parameters demonstrating that the proposed noise model is accurate and the model parameters were well extracted.

7.2 Future Work

As the device technology becomes more advance and the channel length continued to scale down to nanometer range, there is a need for high frequency noise modeling to keep track to further predict the noise performance in nanometer scales. Thus, the proposed model needs to be investigated in the even shorter channel length devices, for example in the RFCMOS 65nm technology devices and RFCMOS 28nm technology devices, in order to verify the scalability of the model.

In this thesis, the proposed noise model is for the devices operating from moderate to strong inversion, and mostly in saturation region. Normally, different assumptions and different models are used for different operating region. The characteristic of noise for weak inversion is also different from the moderate and strong inversion region. As a result, we need to investigate the weak inversion noise mechanism and the smoothening function for the proposed model so that the model can be valid from weak to strong inversion, and triode to saturation region. Eventually, a fully unified model needs to be derived.

The persistent drive in the semiconductor industry for faster, smaller and cheaper integrated circuits has directed the industry not only to the smaller node like 22nm, but also to the advanced CMOS technologies, such as extended-drain FETs (EDFETs) and silicon-on-insulator (SOI) FETs. However, the implementation of these technologies brings along certain challenges to device modeling, especially in high frequency noise modeling. The impact of velocity saturation and hot carrier effects on the high voltage RF EDFETs requires careful examinations. Moreover, it is also important to investigate how significant the contributions of substrate-induced drain current noise to the total drain current noise of RF EDFETs and RF SOI FETs in the high frequency regime. Another worth study topic is how the layout design affects the RF and high frequency noise characteristic. For example, comparison can be performed on the RF and high frequency noise performances for the isolated and non-isolated RF EDFETs.

Appendix A. Derivation of Channel Thermal Noise Models

A.1. Channel Length Modulation and Hot Carrier Effects

From (3.40),

$$S_{i_d} = \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^n [Q'_I(V_y)]^2 dV_y. \quad (A.1)$$

From (3.1), $E_y = \frac{I_{DS}}{-W\mu_{eff}Q'_I}$ and the channel thermal noise can be derived to be [41].

(1) When $n = 1$,

$$\begin{aligned} S_{i_d} &= \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right) [Q'_I(V_y)]^2 dV_y \\ &= \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \left[\int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y + \frac{1}{E_c} \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W\mu_{eff}Q'_I} \right] [Q'_I(V_y)]^2 dV_y \right] \\ &= S'_{i_d} + 4kT \frac{W\mu_{eff}}{L_{eff}^2} \left[\frac{C'_{ox}}{E_c} \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) \right] \end{aligned} \quad (A.2)$$

(2) When $n = 2$,

$$\begin{aligned} S_{i_d} &= \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^2 [Q'_I(V_y)]^2 dV_y \\ &= \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \int_0^{V_{DSeff}} \left(1 + 2 \frac{E_y}{E_c} + \left[\frac{E_y}{E_c} \right]^2 \right) [Q'_I(V_y)]^2 dV_y \\ &= \frac{4kT}{I_{DS}} \left(\frac{W}{L_{eff}} \mu_{eff} \right)^2 \left[\int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y + \frac{2}{E_c} \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W\mu_{eff}Q'_I} \right] [Q'_I(V_y)]^2 dV_y \right. \\ &\quad \left. + \left(\frac{1}{E_c} \right)^2 \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W\mu_{eff}Q'_I} \right]^2 [Q'_I(V_y)]^2 dV_y \right] \\ &= S'_{i_d} + 4kT \frac{W\mu_{eff}}{L_{eff}^2} \left[\frac{2C'_{ox}}{E_c} \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) \right. \\ &\quad \left. + \left(\frac{C'_{ox} V_{DSeff}}{L_{eff} E_c^2} \right) \left(V_{GT} V_{DSeff} - \frac{\alpha}{2} V_{DSeff}^2 \right) \right] \end{aligned} \quad (A.3)$$

A.2. Channel Length Modulation, Velocity Saturation and Hot Carrier Effects

From (3.44),

$$S_{i_d} = \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^n [Q'_I(V_y)]^2 dV_y. \quad (A.4)$$

From (3.22), $E_y = \frac{I_{DS}}{-W\mu_{eff}Q'_I - (I_{DS}/E_c)}$ and thus the channel thermal noise can be derived

as shown below [41].

(1) When $n = 1$,

$$\begin{aligned} S_{i_d} &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right) [Q'_I(V_y)]^2 dV_y \\ &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \left[\int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \right. \\ &\quad \left. + \frac{1}{E_c} \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W\mu_{eff}Q'_I - (I_{DS}/E_c)} \right] [Q'_I(V_y)]^2 dV_y \right] \\ &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 [A + B] \end{aligned} \quad (A.5)$$

$$A = S'_{i_d} \left[1 + \frac{V_{DSeff}}{E_c L_{eff}} \right] \quad (A.6)$$

$$\begin{aligned} B &= \frac{1}{E_c} \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W\mu_{eff}Q'_I - (I_{DS}/E_c)} \right] [Q'_I(V_y)]^2 dV_y \\ &= \frac{-I_{DS}C'_{ox}\alpha}{E_c W \mu_{eff}} \int_0^{V_{DSeff}} \frac{V_y^2 - \frac{2V_{GT}}{\alpha} V_y + \left(\frac{V_{GT}}{\alpha} \right)^2}{V_y + \left(\frac{I_{DS}}{E_c W C'_{ox} \alpha \mu_{eff}} \right) - \left(\frac{V_{GT}}{\alpha} \right)} dV_y \end{aligned} \quad (A.7)$$

$$\text{Let } V_0 = \frac{I_{DS}}{W\mu_{eff}C'_{ox}\alpha E_c} \text{ and } V_1 = \frac{V_{GT}}{\alpha},$$

Appendix A Derivation of Channel Thermal Noise Models

$$\begin{aligned}
 B &= \frac{-I_{DS}C'_{ox}\alpha}{E_c W \mu_{eff}} \int_0^{V_{DSeff}} \frac{V_y^2 - 2V_1 V_y + V_1^2}{V_y + V_0 - V_1} dV_y \\
 &= \frac{-I_{DS}C'_{ox}\alpha}{E_c W \mu_{eff}} \left[V_0^2 \ln \left(\frac{V_{DSeff} + V_0 - V_1}{V_0 - V_1} \right) - V_{DSeff}(V_0 + V_1) + \frac{V_{DSeff}^2}{2} \right]
 \end{aligned} \tag{A.8}$$

$$\begin{aligned}
 S_{i_d} &= S'_{i_d} \left[\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right] - 4kT \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \left[\frac{C'_{ox}\alpha}{E_c W \mu_{eff}} \right] \\
 &\quad \times \left[V_0^2 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) - V_{DSeff}(V_1 + V_0) + \frac{V_{DSeff}^2}{2} \right]
 \end{aligned} \tag{A.9}$$

(2) When $n = 2$,

$$\begin{aligned}
 S_{i_d} &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \int_0^{V_{DSeff}} \left(1 + \frac{E_y}{E_c} \right)^2 [Q'_I(V_y)]^2 dV_y \\
 &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \left[\int_0^{V_{DSeff}} [Q'_I(V_y)]^2 dV_y \right. \\
 &\quad \left. + \frac{2}{E_c} \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W \mu_{eff} Q'_I - (I_{DS}/E_c)} \right] [Q'_I(V_y)]^2 dV_y \right. \\
 &\quad \left. + \left(\frac{1}{E_c} \right)^2 \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W \mu_{eff} Q'_I - (I_{DS}/E_c)} \right]^2 [Q'_I(V_y)]^2 dV_y \right] \\
 &= \frac{4kT}{I_{DS}} \left[\frac{\frac{W}{L_{eff}} \mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 [A + 2B + C]
 \end{aligned} \tag{A.10}$$

$$\begin{aligned}
 C &= \left(\frac{1}{E_c} \right)^2 \int_0^{V_{DSeff}} \left[\frac{I_{DS}}{-W \mu_{eff} Q'_I - (I_{DS}/E_c)} \right]^2 [Q'_I(V_y)]^2 dV_y \\
 &= \frac{1}{E_c^2} \int_0^{V_{DSeff}} \frac{I_{DS}^2 (C'_{ox})^2 (V_{GT}^2 - 2\alpha V_{GT} V_y + \alpha^2 V_y^2)}{(W \mu_{eff} C'_{ox})^2 (V_{GT}^2 - 2\alpha V_{GT} V_y + \alpha^2 V_y^2) - 2W \mu_{eff} C'_{ox} \left(\frac{I_{DS}}{E_c} \right) (V_{GT} - \alpha V_y) + \left(\frac{I_{DS}}{E_c} \right)^2} dV_y \\
 &= \frac{1}{E_c^2} \int_0^{V_{DSeff}} \frac{I_{DS}^2 (C'_{ox})^2 \alpha^2 (V_y^2 - 2V_1 V_y + V_1^2)}{(W \mu_{eff} C'_{ox} \alpha)^2 \left[(V_y^2 - 2V_1 V_y + V_1^2) - 2 \left(\frac{V_0}{\alpha} \right) (V_{GT} - \alpha V_y) + V_0^2 \right]} dV_y
 \end{aligned}$$

Appendix A Derivation of Channel Thermal Noise Models

$$\begin{aligned}
&= \left(\frac{I_{DS}}{W\mu_{eff}E_c} \right)^2 \int_0^{V_{DSeff}} \frac{V_y^2 - 2V_1V_y + V_1^2}{V_y^2 + 2(V_0 - V_1)V_y + V_1^2 + V_0^2 - 2V_0V_1} dV_y \\
&= (V_0C'_{ox}\alpha)^2 \int_0^{V_{DSeff}} \frac{(V_y - V_1)^2}{V_y^2 + 2(V_0 - V_1)V_y + (V_0 - V_1)^2} dV_y \\
&= (V_0C'_{ox}\alpha)^2 \int_0^{V_{DSeff}} \frac{(V_y - V_1)^2}{[V_y + (V_0 - V_1)]^2} dV_y \\
&= (V_0C'_{ox}\alpha)^2 \left[V_{DSeff} - 2V_0 \ln \left(\frac{V_{DSeff} + V_0 - V_1}{V_0 - V_1} \right) - \frac{V_0^2}{V_{DSeff} + V_0 - V_1} + \frac{V_0^2}{V_0 - V_1} \right] \quad (A.11)
\end{aligned}$$

$$\begin{aligned}
S_{i_d} &= S'_{i_d} \left[\frac{1}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right] - 4kT \left[\frac{\frac{W}{L_{eff}}\mu_{eff}}{1 + \frac{V_{DSeff}}{E_c L_{eff}}} \right]^2 \left\{ \left[\frac{2C'_{ox}\alpha}{E_c W \mu_{eff}} \right] \right. \\
&\quad \times \left[V_0^2 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) - V_{DSeff}(V_1 + V_0) + \frac{V_{DSeff}^2}{2} \right] + \\
&\quad \left. \frac{(V_0C'_{ox}\alpha)^2}{I_{DS}} \times \left[-2V_0 \ln \left(\frac{V_{DSeff}}{V_0 - V_1} + 1 \right) + V_{DSeff} - \frac{V_0^2}{V_{DSeff} + V_0 - V_1} + \frac{V_0^2}{V_0 - V_1} \right] \right\} \quad (A.12)
\end{aligned}$$

Appendix B. Extraction of Average Vertical Electric Field

The DC current I_{DS} can be expressed as

$$I_{DS} = \frac{\mu_{eff} C_{ox}' W}{L \left(1 + \frac{V_{DSeff}}{E_c L_{eff}} \right)} \left(V_{GT} V_{DSeff} - \frac{1}{2} \alpha V_{DSeff}^2 \right) \quad (B.1)$$

where

$$V_{GT} = V_{GS} - V_{TH},$$

$$V_{TH} = V_{TH0} - \sigma V_{DS},$$

$$E_c = \frac{2v_{sat}}{\mu_{eff}},$$

$$V_{DSeff} = V_{DSat} - 0.5(V_{DSat} - V_{DS} - \theta + \sqrt{(V_{DSat} - V_{DS} - \theta)^2 - 4\theta V_{DSat}}),$$

$$V_{DSat} = \frac{V_{GT}}{\alpha} \left[\frac{1}{1 + \frac{V_{GT}}{E_c L}} \right].$$

From DC I-V measurement, with the biasing condition V_{GS} and V_{DS} given, the μ_{eff} can be obtained by solving the current equation using the measured value $I_{DS,mea}$. The solver can be implemented using MATLAB.

$$I_{DS}(\mu_{eff}) - I_{DS,mea} = 0 \quad (B.2)$$

After that, the average vertical electric field $E_{x,ave}$ can be obtained from

$$\alpha E_{x,ave} = \frac{\mu_0}{\mu_{eff}} - 1. \quad (B.3)$$

Appendix C. Small Signal Y-parameters Analysis

Figure C.1 General two-port network for small signal analysis.

Figure C.1 illustrates the general two-port network widely used in the small signal analysis, indicating port 1 and port 2 for RF FET. By using the port definition shown in Figure C.1, Y-parameters analysis [61] is performed on the simplified small signal equivalent circuit in Figure 5.3 [45].

(1) Formulation of Y_{11}

$$\begin{aligned}
 Y_{11} &= \left. \frac{I_1}{V_1} \right|_{V_2=0} = \frac{j\omega(C_{gd}+C_{gs})\left(\frac{1}{R_g}\right)}{j\omega(C_{gd}+C_{gs})+\left(\frac{1}{R_g}\right)} = \frac{j\omega(C_{gd}+C_{gs})}{j\omega(C_{gd}+C_{gs})R_g+1} \\
 &= \frac{j\omega(C_{gd}+C_{gs})}{j\omega(C_{gd}+C_{gs})R_g+1} \times \frac{1-j\omega(C_{gd}+C_{gs})R_g}{1-j\omega(C_{gd}+C_{gs})R_g} \\
 &= \frac{\omega^2(C_{gd}+C_{gs})^2 R_g + j\omega(C_{gd}+C_{gs})}{1+\omega^2 R_g^2 (C_{gd}+C_{gs})^2} \tag{C.1}
 \end{aligned}$$

Appendix C Small Signal Y-parameters Analysis

(2) Formulation of Y_{12}

$$Y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} \quad (\text{C.2})$$

$$I_1 = \frac{-V'_g}{R_g} \quad (\text{C.3})$$

$$j\omega C_{gd}(V_2 - V'_g) - \frac{V'_g}{R_g} = j\omega C_{gs}V'_g \quad (\text{C.4})$$

$$j\omega C_{gd}V_2 = \left[j\omega(C_{gd} + C_{gs}) + \frac{1}{R_g} \right] V'_g \quad (\text{C.5})$$

$$V'_g = \frac{j\omega C_{gd}}{j\omega(C_{gd}+C_{gs})+\frac{1}{R_g}} V_2 = -I_1 R_g \quad (\text{C.6})$$

$$\begin{aligned} Y_{12} &= \left. \frac{I_1}{V_2} \right|_{V_1=0} = \frac{-j\omega C_{gd}\left(\frac{1}{R_g}\right)}{j\omega(C_{gd}+C_{gs})+\frac{1}{R_g}} = \frac{-j\omega C_{gd}}{j\omega(C_{gd}+C_{gs})R_g+1} \\ &= \frac{-j\omega C_{gd}}{j\omega(C_{gd}+C_{gs})R_g+1} \times \frac{1-j\omega(C_{gd}+C_{gs})R_g}{1-j\omega(C_{gd}+C_{gs})R_g} \\ &= \frac{-\omega^2 C_{gd}(C_{gd}+C_{gs})R_g - j\omega C_{gd}}{1+\omega^2 R_g^2 (C_{gd}+C_{gs})^2} \end{aligned} \quad (\text{C.7})$$

(3) Formulation of Y_{21}

$$Y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} \quad (\text{C.8})$$

$$C_m = C_{dg} - C_{gd} \quad (\text{C.9})$$

$$C_m \frac{dV'_g}{dt} = j\omega C_m V'_g \quad (\text{C.10})$$

Appendix C Small Signal Y-parameters Analysis

$$-V_g'(j\omega C_{gd}) + \frac{V_1 - V_g'}{R_g} = V_g'(j\omega C_{gs}) \quad (C.11)$$

$$V_g' = \frac{V_1}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (C.12)$$

$$\begin{aligned} I_2 &= g_m V_g' - C_m \frac{dV_g'}{dt} - V_g'(j\omega C_{gd}) \\ &= \frac{V_1}{1 + j\omega(C_{gs} + C_{gd})R_g} [g_m - j\omega(C_m + C_{gd})] \end{aligned} \quad (C.13)$$

$$\begin{aligned} Y_{21} &= \left. \frac{I_2}{V_1} \right|_{V_2=0} = \frac{g_m - j\omega(C_m + C_{gd})}{1 + j\omega(C_{gs} + C_{gd})R_g} = \frac{g_m - j\omega(C_m + C_{gd})}{1 + j\omega(C_{gs} + C_{gd})R_g} \times \frac{1 - j\omega(C_{gs} + C_{gd})R_g}{1 - j\omega(C_{gs} + C_{gd})R_g} \\ &= \frac{g_m - \omega^2 C_{dg}(C_{gd} + C_{gs})R_g - j\omega[(C_{gd} + C_{gs})R_g g_m + C_{dg}]}{1 + \omega^2 R_g^2 (C_{gd} + C_{gs})^2} \end{aligned} \quad (C.14)$$

(4) Formulation of Y_{22}

$$Y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0} \quad (C.15)$$

$$(V_2 - V_g')(j\omega C_{gd}) = \frac{V_g'}{R_g} + V_g'(j\omega C_{gs}) \quad (C.16)$$

$$V_g' = V_2 \left[\frac{j\omega C_{gd}R_g}{1 + j\omega(C_{gs} + C_{gd})R_g} \right] \quad (C.17)$$

$$\begin{aligned} I_2 &= V_2(Y_{sub} + g_{ds} + j\omega C_{gd} + j\omega C_{sd}) + g_{mb}V_{bs} + g_m V_g' - C_m \frac{dV_g'}{dt} \\ &= V_2(Y_{sub} + g_{ds} + j\omega(C_{gd} + C_{sd})) \\ &\quad + V_2 \left[\frac{j\omega C_{gd}R_g}{1 + j\omega(C_{gs} + C_{gd})R_g} \right] (g_m - j\omega C_m) + g_{mb}V_{bs} \end{aligned} \quad (C.18)$$

Appendix C Small Signal Y-parameters Analysis

$$\begin{aligned}
Y_{22} &= \left. \frac{I_2}{V_2} \right|_{V_1=0} \\
&= Y_{sub} + g_{ds} + j\omega(C_{gd} + C_{sd}) \\
&\quad + \frac{j\omega C_{gd} R_g}{1 + j\omega(C_{gs} + C_{gd})R_g} \times \frac{1 - j\omega(C_{gs} + C_{gd})R_g}{1 - j\omega(C_{gs} + C_{gd})R_g} + g_{mb} \left| \frac{V_{bs}}{V_{ds}} \right| \\
&= Y_{sub} + g_{ds} + j\omega(C_{sd} + C_{gd}) + g_{mb} \left[\frac{V_{bs}}{V_{ds}} \right] \\
&\quad + \frac{\omega^2 C_{gd} R_g [(C_{gd} + C_{gs})R_g g_m + C_{dg}] + j\omega C_{gd} R_g [g_m - \omega^2 C_{gd} R_g (C_{gd} + C_{gs})]}{1 + \omega^2 R_g^2 (C_{gd} + C_{gs})^2} \quad (C.19)
\end{aligned}$$

where

$$\begin{aligned}
\frac{V_{bs}}{V_{ds}} &= Y_{sub} \left[\frac{(1 - j\omega C_{bb} R_{bb}) R_{bb}}{1 + \omega^2 R_{bb}^2 C_{bb}^2} \right] \\
Y_{sub} &= \frac{\omega^2 R_{bb} C_{db}^2}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2} + \frac{j\omega C_{db} + j\omega^3 R_{bb}^2 C_{db} C_{bb} (C_{db} + C_{bb})}{1 + \omega^2 R_{bb}^2 (C_{db} + C_{bb})^2}
\end{aligned}$$

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- 3) S. N. Ong, K. S. Yeo, K. W. J. Chew, L. H. K. Chan, X. S. Loo, C. C. Boon, and M. A. Do, "Impact of velocity saturation and hot carrier effects on channel thermal noise model of deep sub-micron MOSFETs," in *Solid-State Electron.*, vol. 72, pp. 8-11, Jun. 2012.
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