On the "switching defects" in the SiON and high-k gate dielectrics subjected to bias-temperature stressing

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2014

Boo, A. A. (2015). On the "switching defects" in the SiON and high-k gate dielectrics subjected to bias-temperature stressing. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/64784>

<https://doi.org/10.32657/10356/64784>

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**ON THE “SWITCHING DEFECTS” IN THE
SION AND HIGH- κ GATE DIELECTRICS
SUBJECTED TO BIAS-TEMPERATURE
STRESSING**

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School of Electrical and Electronic Engineering

**A thesis submitted to the Nanyang Technological University in
fulfillment of the requirement for the degree of Doctor of
Philosophy**

ACKNOWLEDGEMENTS

First and foremost, I would like to express and extend my sincere thanks to my project supervisor, Dr. Ang Diing Shenp, for his continuous support throughout my 4 years of Phd study, and also for his constructive guidance and advices which stimulate me to think logically and rationally. He encouraged me to build up the knowledge on semiconductor through effective reading and he taught me how to deliver the ideas clearly through professional writing. His patience and understanding, together with his research and teaching experience, have contributed immensely to the enlargement of my knowledge and research ability. Without his dedicated supervision, this research work would not be able to generate so much interesting and vital results which are needed in understanding the underlying real mechanisms of NBTI/ PBTI.

Next, I would love to express my sincere thanks to Dr. Pey Kin Leong (Formerly from NTU, now at SUTD), Dr. Lap Chan, Dr. Ng Chee Mang and Mr. Leong Kam Chew (from GlobalFoundries Ptd. Ltd.) for their decisive support on my GF-NTU Graduate Research Scholarship application and continuous encouragements during my postgraduate study. Besides, they have also provided us with a lot of opportunities to know more about the current market and industry. I am very grateful to have the chance to attend many of the classes conducted by Dr. Lap Chan and Dr. Ng Chee Mang during my first year of Ph.D study. Besides, I appreciate the help from all the engineers of

GlobalFoundries for their expertise and advice on electrical measurements and equipment support.

Last but not least, I appreciate the assistance and cooperation provided by my team members, Mr Tung Zhi Yan, Mr. Du GuoAn, Mr. Teo Zhi Qiang, Mr. Ho Jun Jie, Mr. Gao Yuan, Mr. Yew Kwang Sing and Mr. Gu Chenjie for their contribution to help me complete my project.

A million thanks to everyone again. I had a wonderful and fruitful journey as a Phd research student.

ABSTRACT

Since 1960s, the most commonly cited model to explain NBTI (negative-bias-temperature-instability) mechanism was the Reaction-Diffusion (R-D) model which described the evolution of Si/ SiO₂ interface states (ΔN_{it}) contributing to NBTI based on a hydrogen-transport mechanism. However, there were still many debates regarding the commonly observed instantaneous threshold voltage (V_{th}) shift during stress and relaxation phase. Some believed that this instantaneous V_{th} shift could be solely explained by the generation and passivation of N_{it} at the Si/ SiO₂ interface based on the framework of R-D model. On the other hand, there were reports which indicated that NBTI has two mechanisms involved: 1) hole-trapping (N_{ot}) and 2) interface states generation (N_{it}) which were used to explain the fast and slow V_{th} shift observed using fast measurements. Recent reports have revealed a major intrinsic limitation of the R-D model through dynamic stress experiments. It is found that no evidence of self-limiting recovery, one of the key features of the transport-based R-D model, after repeating the stress and relaxation cycles alternately for many times. It is also observed that the $|\Delta V_t|$ recovery is cyclic in nature and its amount of recovery per cycle is shown to remain constant, independent of the number of stress/ recovery cycles. This behaviour observed is inconsistent with the R-D model, which stipulated that interface states relaxation should decrease progressively with the stress/ recovery cycle. Several groups have ascribed this cyclic nature of DNBTI to the charging/ discharging of oxide traps based on

thermal activation result. However, till date, the underlying nature of this fast component is still yet to be identified. It is now generally accepted that there are two main components which contribute to NBTI degradation: 1) a relatively permanent component (P) which does not recover spontaneously upon the release of stress 2) a transient, “switching” hole-trapping component (R) which is able to recover spontaneously upon the removal of gate bias. The constituent of P is believed to be the P_b centers (interface states) while the constituent of R is proposed to be the oxygen vacancy defects. We discovered that the link between NBT instability and bulk trap generation is actually found in this transient “switching” hole-trapping component (R). In this work, evidence shows that substantial interface degradation under NBT stressing does not result in any apparent bulk trap generation. It is noticed that oxide trap generation only occurs when a correlated *decrease* of R is observed. Analysis suggests that the generated oxide traps are due to a portion of the transient trapped holes being transformed into a more permanent form of defect. Besides, experimental evidences showed that this NBT stress induced transient hole-trapping evolution could be thermally-activated and it correlates with the generation of stress induced leakage current. A similar observation applies to the HfO_2 gate p-MOSFET, implying that the observed hole-trapping transformation is a common mechanism for bulk trap generation across different gate oxide technologies. The activation energy of this observed hole-trapping evolution, which has non-Arrhenius temperature dependence, has been examined for both SiON and HfSiON p-MOSFETs. Most importantly, this transformation is

observed to be frequency independent. These results further imply that pre-existing oxide defects, usually deemed as irrelevant to NBTI, have a definite role on long term device parametric drifts. And, evidences have been provided on the possible correlation among NBTI, TDDB and ESD. The later part of this report is focused on BTI of MOSFETs with HfSiON gate dielectric. Previously, Du *et al.* has revealed an abnormal slow recovery characteristic of La-doped HfSiON n-MOSFETs subjected to positive-bias elevated temperature stress. This La-induced new degradation mechanism has been further affirmed and supported by our new experimental results based on our understanding of transient trapped holes transformation. The La impact has been distinguished from the conventional PBTI mechanism. Thus, the transformation of NBT stress induced transient hole-trapping at pre-existing oxide defects observed in this work is crucial as it marks the start of a new series of investigations and understanding of the devices' reliability, with the aim to have a more accurate lifetime prediction (which is very much affected by scaling). Lastly, a plausible explanation for the nature of the transient "switching" hole-trapping evolution has been proposed and discussed in light of the new experimental findings.

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(2×2×2) of dimensions $10.23 \times 10.23 \times 10.23 \text{ \AA}^3$ and density 10.45 g/cm^3 . Molecular dynamic simulation was then used to achieve a pseudo-amorphous structure for both cases. There are a total of 96 atoms (64 O atoms and 32 Si or Hf atoms) in each supercell. The electronic structure was described based on density functional theory using the PBE approximation. An oxygen vacancy defect is manually created at each of the 64 O lattice points by removing an O atom and allowing the system to fully relax at the Γ point. [Courtesy: C. J. Gu] **(111)**

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stress at -2.6 V, 125° C on conventional SiON devices. $|\Delta I_d|$ is normalized to its first point. The data shows that recovery is independent of the recovery voltage. [120] (169)

Figure 7-4: Long time recovery data captured after 100 s of stress on three types of devices (1) High- κ transistors with La_2O_3 capping, (2) High- κ transistors without La_2O_3 capping, and (3) SiON transistors. The gate recovery voltage V_g^r is set to V_{DD} and the stress temperature is 125° C. The recovery speed is seen to be similar for all types of devices (slope: -0.13) except for transistors with La_2O_3 capping layer, 1-Hik-N-La (slope: -0.05). [120] (170)

Figure 7-5: The remaining $|\Delta I_d|$ at various gate oxide thicknesses, ranging from 1.8 nm to 4.5 nm, as a function of recovery time. The recovery data is captured after 100 s of stress on devices with various dielectric thicknesses. Stress temperature is 125° C. [120] (170)

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Figure 7-7: Shows the decrease in R after subjecting the device to a 40 dynamic PBTI cycles of stress ($E_{ox} = 8\text{ MV/cm}$, $V_g \text{ relax} = 0$ V) as a function of temperatures for both undoped and La-doped High- κ MOSFETs. (174)

Figure 7-8: (a) The evolution of I_g (shown is the I_g at the 40th cycle) of the undoped p-MOSFETs and (b) La-doped n-MOSFETs after 40 dynamic BTI cycles of stress ($E_{ox} = 8\text{ MV/cm}$, $V_g \text{ relax} = 0$ V) at different temperatures. A substantial increase in the I_g is observed at 100° C for the doped n-MOSFET even in the absence of ΔR . (175)

Figure 7-9: Undoped High- κ / metal gate p-MOSFETs stressed at a constant voltage of (a) $V_g = -2$ V (NBT) (b) $V_g = +2$ V (PBT). After every 2000 s of constant V_g stress, I_g was measured by sweeping V_g from +1.5 V to -1.5 V or vice-versa. This test sequence was repeated up to a cumulative stress time of 40, 000 s (E_{ox} applied were comparable for all transistors). Similar experimental conditions were done on a La-doped high- κ / metal gate n-MOSFET (c) $V_g = -2$ V (NBT) (d) $V_g = +2$ V (PBT) to compare the effect of (with/ without) La on the gate leakage tunneling spectra. (177)

Figure 7-9: La-doped High- κ / metal gate n-MOSFETs stressed at a constant voltage of (c) $V_g = -2$ V (NBT) (d) $V_g = +2$ V (PBT). After every 2000 s of constant V_g stress, I_g was measured by sweeping V_g from +1.5 V to -1.5 V or vice-versa. This test sequence was repeated up to a cumulative stress time of 40, 000 s (E_{ox} applied were comparable for all transistors). (a)- (d) are compared to study the effect of (with/ without) La on the gate leakage tunneling spectra. (178)

Figure 7-10: $\Delta I_g (I_g @ 40,000 \text{ s} - I_g @ \text{fresh}) / I_g @ \text{fresh}$ was calculated for both undoped p-MOS and La-doped n-MOS capacitors. (a) La-doped n-capacitors track a higher I_g degradation independent of V_g applied regardless of NBT/ PBT stress. (b)

Higher degradation is always observed for La-doped n-capacitors across different temperatures regardless of NBT/ PBT stress. **(179)**

Figure 7-11: The evolution of I_g in both sweeping directions (a) $1.5 < V_g < -1.5$ V (down sweep) (b) $-1.5 < V_g < 1.5$ V (up sweep) for the La-doped n-MOSFET. Under the influence of La, the I_g degradation is shown to be irreversible and have less gate polarity dependence. No I_g is observed to recover despite a 9 s discharge at -1.5 V. **(182)**

Figure 7-12: The evolution of I_g in both sweeping directions (a) $-1.5 < V_g < 1.5$ V (up sweep) (b) $1.5 < V_g < -1.5$ V (down sweep) for the undoped p-MOSFET. The I_g spectra remains practically unchanged as no hole-trapping transformation has been activated at 100° C (refer Fig. 7-7). **(183)**

Figure 7-13: (a) Local network of HfO_2 , showing a substitutional La atom in an “unrelaxed” state, due to rapid cooling during spike annealing. (b) Applied electric field and thermal energy (during Bias-Temperature stress), coupled with the greater ionicity of the La-O bond, induce local structural relaxation via relative displacement of the La and O atoms. The resultant formation of $V_o - I_o$ Frenkel pairs induce relatively deep electronic trap levels (below the Si valence band edge) as illustrated in Fig. 7.15. [120] **(185)**

Figure 7-14: First-principles simulation reveals a non-negligible lowering of the local network energy, rendering the structural relaxation process irreversible (i.e. defect formation is permanent). [120] **(187)**

Figure 7-15: (a) A simple schematic energy band diagram showing the trapping process of the electrons at the stress-induced $V_o - I_o$ Frenkel pairs during PBTI. (b) Since formation of the $V_o - I_o$ Frenkel pair is permanent and the I_o level is relatively deep, recovery speed of the La-doped n-MOSFETs is reduced significantly. [120] **(188)**

LIST OF SYMBOLS

V_{FB}	: Flatband voltage
ϕ_{MS}	: The difference between the workfunction of the metal and semiconductor. This workfunction equals the sum of the electron affinity, the difference between the conduction band energy and the intrinsic energy divided by the electronic charge and the bulk potential as expressed by the following equation
ϕ_F	: Bulk Potential
k	: Boltzman constant
q	: Electrical charge, 1.602×10^{-19} Coulumb
n_i	: Intrinsic carrier concentration, $1.5 \times 10^{10} \text{ cm}^{-3}$ at $T = 300 \text{ K}$
ϵ_0	: Permittivity constant with a value of 8.85×10^{-12}
ϕ_s	: Workfunction of the semiconductor material
Q_f	: Fixed charge density
Q_{it}	: Interface trap density
Q_{ot}	: Oxide charge density.

CHAPTER 1: INTRODUCTION

1.1 Introduction to MOSFETs

Driven by the commercial requirements on low cost and high performance, the **metal–oxide–semiconductor field-effect transistor** (MOSFET) continues to scale down over the decades following the famous Moore's law [1], [2], which states that the number of transistors placed on an integrated circuit (IC) could increase exponentially, approximately doubling every two years. The performance of semiconductor products has been continuously improved by scaling down the dimensions of the MOS transistors over the past half. Down-scaling in the device dimension, particularly in the transistor gate length, induces a higher transistor current, which enables the device to switch faster and hence leads to faster computations for the chip, besides achieving lower power dissipation. As the transistor size becomes tinier, the number of transistors which could be integrated onto a single chip increases. As a consequence, the complexity and functionality of the ICs are also increased while the manufacturing cost per chip is still kept low. However, the operation temperature of MOSFETs could not be scaled down together with the dimensions, causing the off current to degrade. As a result, the threshold voltage would be higher, resulting in the power density to increase over time. Moreover, the supply voltage is not able to scale as much as the linear dimensions of the MOSFET in order to ensure its performance when the transistor density

becomes higher [3]. Hence, the electric field of the transistor during operation becomes larger and as a result, more severe reliability problems would be generated.

As the channel length and width of the MOSFETs are shrinking, the oxide thickness is also required to scale down proportionally. This is done to guarantee the gate has the control over the channel. However, problems arise when the gate oxide for the newer generation technology is scaled down to less than 2 nm, which consists of only a few atomic layers. Quantum tunneling takes place and the leakage current increases exponentially for such ultra-thin gate oxide [4]. Adding nitrogen into SiO_2 was reported to help curb the leakage current related reliability. Another suggestion was to replace SiO_2 / SiON with other materials with higher dielectric constant. These materials ensure a physical gate dielectric thickness which is large enough to prevent leakage current, while having a small electrical oxide thickness (EOT) to retain good control over the gate [5].

High- κ gate dielectrics have been chosen for 45 nm technology node and beyond to have a high capacitance and good control over the gate [6], [7]. Hf-based oxides, including HfO_2 , HfSiO_x , and HfSiO_xN_y , are the widely discussed candidates for high- κ dielectrics due to (1) their high dielectric constant; (2) large energy band barrier to suppress leakage current; and (3) excellent thermal stability with Si and compatibility with existing CMOS process. However, the

impacts of using high- κ dielectrics on reliability are complicated due to the complex dielectric compositions, though high- κ material was reported to be able to reduce the electric field across the dielectric successfully.

1.2 Reliability Issues of MOSFETs

Negative-Bias Temperature Instability (NBTI) has long been reported to be one of the most researched reliability issues. It has attracted considerable attention due to its significant impact which limits the circuit performance since 1966 [8] and it has been ascribed to the progressive shift of device parameters, such as the threshold voltage, transconductance, drain current, *etc.* of the p-channel metal-oxide-semiconductor field-effect transistor (p-MOSFET). NBTI refers to the degradation of p-MOSFET performance due to the accumulation of positive trapped charges along the Si/ SiO₂ interface under negative gate bias at elevated temperature. Fig. 1-1 illustrates the NBTI stressing of a p-MOSFET upon applying a negative gate bias on the gate with the other terminals grounded. More and more interface defects and positive charges would be generated near the Si/ SiO₂ interface and in the bulk SiO₂ after a period of time under such gate bias at an elevated temperature (75~125° C). The NBTI degradation of p-MOSFET results in smaller drive current I_{dsat} , higher threshold voltage $|V_{\text{th}}|$, smaller carrier mobility μ and etc. Degradation in the drive current of the p-MOSFETs in a complementary MOS (CMOS) circuit by NBTI is crucial as it would cause speed reduction and continuous drift in other performances eventually.

Figure 1-1: Schematic diagram of *p*-type MOSFET under NBTI stress. “+” denotes positive charge in the gate oxide or at the Si-SiO₂ interface.

Since the beginning of this decade, NBTI has attracted widespread attention from both industry and academia. It has been observed in the Si/ SiO₂ technology that NBTI seems to play a more significant degrading role in a *p*-MOSFET than PBTI. It has also been reported that NBTI is the dominant factor on device lifetime [9] and has, thus become one of the bottlenecks in the silicon integrated circuits industry, especially when the industry is driven into the direction of producing devices with smaller dimensions. The gate electric field has increased due to scaling and the chip operating temperature has increased due to higher packing density. Apart from that, the replacement of buried channel counterpart by surface *p*-channel MOSFET, the increasing amount of nitrogen added to the thermally grown SiO₂ to suppress boron penetration, besides curbing gate tunneling leakage issues and etc...have caused NBTI degradation to be worsen. In 1966, Jeppson and Svensson [10] have introduced

the first model to explain NBTI phenomena. The Reaction- Diffusion (R-D) model was based solely on the process of interface traps generation. This model was then widely adopted to explain some NBTI experimental observations [11]- [13], such as the instantaneous threshold voltage shift during the onset of NBTI stress, power law time exponent ($n \sim 1/6$) of NBTI evolution and temperature activated process with activation energy of 0.1 ~0.2 eV and etc.

Lately, it is reported that there is an underestimation of NBTI degradation by conventional DC measurement. This is due to the measurement delay, which allows corruption of the spontaneous recovery effect on the total threshold voltage shift ($|\Delta V_t|$) upon termination of stress [14]. This results in the emergence of some fast measurement methodologies, such as the pulse I_d - V_g [14]- [15], fast V_t [11] characterization technique and on-the-fly $I_{d,lin}$ [16]- [17], which will be discussed further in Chapter 3 later. With these, many new insights of NBTI degradation, which were not observed using conventional DC measurement, have surfaced. These new observations have triggered some questions and doubts regarding the soundness of R-D model. However, the consistency benchmarking of NBTI in the face of fast and significant recovery is still in the midst of debate due to the lack of a practical measurement standard. This has rendered experimental data which are extremely sensitive to measurement delay and thus, making the comparison of different sources difficult.

There were many debates within the NBTI community regarding the commonly observed transient $|V_{th}|$ shift during stress and relaxation phase. Recent reports based on dynamic NBTI using fast measurements have indicated that NBTI induced threshold voltage shift ($|\Delta V_t|$) comprises of a recoverable (R) component and a relatively permanent (P) component [18]- [20]. Several believe that the relatively more permanent $|V_{th}|$ shift can be solely explained by the generation and passivation of interface traps at the Si/ SiON interface based on the framework of (R-D) theory [11], [17]. However, results derived from dynamic NBTI experiments [19]- [20] do not support the notion that NBTI is driven by hydrogen transport. Hence, there is another camp of thought which suggests the existence of another additional mechanism involved during NBTI – hole- trapping, which might be caused by repetitive charging/ discharging of the oxide traps. This notion is supported by studies based upon electron spin resonance measurement which have confirmed that these “switching” hole-traps are related to oxygen vacancy defects in the gate dielectric. Thus, this helps to explain the fast responsive $|V_{th}|$ shift observed during dynamic NBTI [21]- [22].

The nature of the recoverable component (R) is observed to exhibit a “non-RD” characteristic in which it possesses a cyclic behavior and the amount of $|\Delta V_t|$ which can be recovered in every relaxation cycle remains constant throughout all dynamic NBTI cycles. It is then suggested that the P component is contributed mainly by P_b centers at the Si/ SiO₂ interface and the R component is ascribed to the oxygen vacancy defects in the bulk oxide. One widely

proposed candidate for the R component is the E' centers (arise from oxygen vacancies, $O_3 \equiv Si^+ \cdot Si \equiv O_3$) while the other is the k_N centers ($N_3 \equiv Si^+ \cdot Si \equiv N_3$). There is also a current viewpoint which relates R to the activation of pre-existing traps which occurs during stressing. Though temperature dependence study has revealed distinct activation energies, implying different defect nature of the P and R components, the nature of the underlying defects remains unclear till today [19]. Therefore, there is increasing interest in revealing the nature of the R component in order to have a clearer picture of NBTI degradation. In this thesis, further interesting investigations/ new insights regarding the “switching” hole-trap (R) component and its transformation will be presented and discussed. Based on all these new observations and insights, the interdependence of some reliability problems, such as NBTI, Electrostatic Discharge (ESD), and Time-Dependent Dielectric Breakdown (TDDB)/ Stress-Induced Leakage Current (SILC) will be reviewed and explored.

As the industry is now advancing into high- κ / metal gate dielectric with the aim to overcome several obstacles which arise from scaling, PBTI degradation is unfortunately, noticed to draw as much interest as in NBTI. PBTI on high- κ / metal gate n-MOSFETS is slowly gaining momentum because severe threshold voltage shift was reported for both positive bias and negative bias in the High- κ transistors [23]- [25]. When High- κ devices were first implemented in the initial stage, the bias temperature degradation was observed to be more significant as compared to those conventional SiON gate oxides. This degradation was

believed to be due to some filling of the pre-existing bulk traps in the complex Hf-based (HfSiON) dielectric compositions. Fortunately, with the optimization of Atomic Layer Deposition technique, NBTI/ PBTI induced threshold voltage shift in High- κ devices has now become comparable to those observed for silicon-based oxides. However, these Hf-based gate dielectrics still possess a number of fundamental issues, such as the issues with fixed charges and trapped charges, the reduction of channel mobility and many more, which have to be resolved for successful High- κ integration into the silicon CMOS technology [23], [26]. Though it is understood that the High- κ / metal gate dielectric itself has higher density of pre-existing defects by nature, the physical mechanism of the High- κ / metal gate BTI is still unclear yet up to the present moment.

1.3 Motivation

With the aggressive down-scaling of the gate oxide thickness into the direct-tunneling regime, such as the oxide thickness becomes < 3.5 nm, NBTI degradation in p-MOSFETs has replaced HCI-induced degradation in n-MOSFETs to be the limiting factor of the lifetime in CMOS circuits [27]- [28]. The characterization of NBTI has therefore, become very critical especially after NBTI recovery has been universally observed upon the removal of stress [29]- [32]. NBTI measurement results were reported to be highly sensitive of the measurement delay as it allowed most of the $|\Delta V_t|$ to recover during measurement. With the emergence of some fast measurements, such as “On-The-Fly” and Ultra-Fast-Switching measurement, it has been shown that NBTI induced

threshold voltage shift ($|\Delta V_t|$) comprises of a recoverable “switching” hole-trap (R) and a relatively permanent interface defect (P) component [14], [18]. Most importantly, the cyclical, constant nature of the R component after 30 cycles of stress/ relaxation does not agree well with the R-D model. In our recent work, it is interesting to observe that the constant nature of the $|\Delta V_t|$ recovered during the ensuing relaxation cycle upon the removal of stress in DNBTI could alter in the presence of high oxide field and moderately high temperature during NBTI. R is observed to be able to transform into a permanent change state. Similar hole-trapping evolution in the $\text{HfO}_2/\text{HfSiON}$ gate p-MOSFETs has also been observed. This indicates the possibility of the observed hole-trap transformation to be a common bulk trap mechanism across different gate stack technologies. Till date, most of the lifetime prediction models are based on a constant capture/ emission time for a charge state. This discovered “switching” hole-trap transformation into relatively permanent charge states marks a significant milestone of understanding the physical common origin of the defect precursor, which is speculated to be shared among some oxide degradation mechanisms. Therefore, it is crucial to review these reliability issues in order to have a more accurate lifetime prediction model which could assist in CMOS circuit design. A series of investigations should be carried out to probe the underlying mechanism further and to support our inference on the interactions of NBTI-ESD- TDDB, which was once showed to be not correlated to each other.

Last but not least, drastic threshold voltage shift was reported in the High- κ transistors under both positive bias and negative bias. And, the degradation was found to be much more severe as compared to those conventional silicon-based gate dielectrics [23]- [25]. Much attention should be placed on the study of the reliability issues generated by the complex Hf-based gate oxides. The situation becomes more complicated when the high- κ oxides are doped with rare earth materials, such as Lanthanum (La) and Zirconium (Zr). Although Du *et al.* has reported an abnormal slow recovery by La- doped HfSiON in the n-MOSFETs, there is still an urgent need to study and to separate the involvement of PBTI/ NBTI from this abnormal slow recovery mechanism which is proposed to be induced by La solely.

1.4 Objectives

The objectives of this thesis are:

(1) To study the recovery mechanism of BTI-induced degradation by using Ultra-Fast Switching (UFS) measurement. Attention will be focused on the “switching” hole-trap (R) component by monitoring and examining the effect of the

(a) gate oxide field

(b) temperature

on its cyclical and constant behaviour during dynamic NBTI. Investigation on its transition from a recoverable charge state into a relatively permanent defect form will also be done.

(2) To establish the linear correlation between the transformation of the “switching” hole-trapping mechanism and the generated bulk traps in the gate oxide. Some important observations and features on their non-Arrhenius temperature dependence and frequency study will be discussed further.

(3) To reveal, to review and to discuss the interdependence of NBTI-ESD- TDDB and the possibility of them sharing a common defect precursor.

(4) To further investigate the impact of Lanthanum on PBTI for High- κ HfSiON gate oxides. Besides, it is also aimed at studying and distinguishing the role played by PBTI/ NBTI on the abnormal slow recovery observed in the La-doped High- κ devices reported by Du *et al.*

1.5 Scope of Thesis

This thesis mainly focuses on the study of Bias- Temperature Instability on ultrathin SiON p-MOSFETs and La-Doped HfSiON Gate Dielectrics. This report will first discuss about some views on the “non-RD” characteristics of dynamic NBTI, followed by observations and evidences which help to understand the interesting behaviour of R , and lastly on the application of this observed “switching” hole-trap transformation process to study the correlation of BTI with other oxide degradation mechanisms. Lastly, PBTI on the La-doped HfSiON n-MOSFETs will be presented. Below are some descriptions of various chapters in this report.

CHAPTER 1 gives an overview of the research background, such as an introduction on the early history and development of MOS devices, problems which arise from gate dielectric scaling, and the key issues of gate oxide reliability. The motivation and objectives of this project are also presented in this chapter.

CHAPTER 2 depicts a literature review of NBTI and its recent highlights. The review encompasses the history of NBTI, the framework and some discrepancies of the R-D model. It also reports about the existence of a “switching” hole-trap (R) component which attributes to NBTI, observed only by using fast measurement methods. This chapter also summarizes the background of other reliability issues such as Electrostatic Discharge (ESD) and Time-Dependent-Dielectric Breakdown (TDDB). Lastly, a brief overview of the incorporation of Lanthanum (La) on High- k transistors’ reliability is presented.

CHAPTER 3 presents the measurement method used in this project. It starts off with the development of the ultra-fast switching (UFS) method and how it improves Bias-Temperature Instability (BTI) measurement. The experimental setup of the new UFS method and the schematic diagrams of the electrical circuit are also systematically shown. The working principles of the method are explained, followed by the validation of the measured data. This method is verified in this work for an accurate characterization of NBTI threshold voltage shift in comparison with conventional DC measurements.

CHAPTER 4 discusses about the observations made for the recoverable (R) component of dynamic NBTI. To probe further into the nature of the R component, high oxide fields and temperatures are applied to study its impact on the R component. The “transformation” of R into a relative permanent charge state could be thermally activated. This newly discovered finding helps us to understand about the correlation between NBT and bulk oxide traps generated during Stress-Induced Leakage Current (SILC). A plausible explanation for the defect origin of the “switching” hole-traps has been proposed in light of the new experimental findings.

CHAPTER 5 focuses on the activation energy of the R transformation as a function of the temperature using two distinct methods, the UFS and SILC. $\Delta I_g / I_{g0}$ (SILC) is used to gauge the generation of bulk traps whereas ΔR (UFS) is used to monitor the reduction of “switching” hole-traps during DNBTI. The activation energy obtained for both are compared. ΔR and $\Delta I_g / I_{g0}$ are observed to have non-Arrhenius temperature dependence. There is “roll-off” region which separates the Arrhenius plot into two regimes, namely the high and low temperature region. Besides, this chapter also shows the time exponent (n) across various temperatures obtained using both methods. Interestingly, n for ΔR and $\Delta I_g / I_{g0}$ is noticed to be similar to that of the classical α value reported during SILC measurement (0.21 – 0.45). These results strongly support the hidden, linear correlation between BTI and the bulk traps. Apart, its frequency dependence is also investigated.

CHAPTER 6 reveals and revisits the interdependence of NBTI, ESD and TDDB. Evidences are presented to further support our speculation of these 3 gate oxide reliability mechanisms (which were studied separately in the past) sharing a common defect precursor. The impact of the newly discovered transformation process on some lifetime prediction models will also be discussed.

CHAPTER 7 focuses mainly on the BTI of MOSFETs with HfSiON gate dielectric. Experimental results by Du *et al.* have shown an abnormal slow recovery characteristic and a new degradation mechanism induced by Lanthanum (La) incorporation. This chapter examines the role played by PBTI/NBTI on this slow abnormal recovery nature. It also studies the irreversibility behaviour of the La-doped gate oxide. Further evidences will be provided to support Du *et al.*'s conclusion that this identified, new degradation mechanism stems unambiguously from the presence of La in the gate oxide. A preliminary atomic model based on simulation suggested by Du *et al.*'s is found to be able to explain our experimental observations on the La-related defect.

CHAPTER 8 summarizes the work which has been discussed in this thesis, and lastly, outlines some recommendations for future research.

CHAPTER 2: LITERATURE REVIEW

2.1 Principle Operation of p-MOSFETs

The basic theory of p-MOSFET is based on the charge-controlled channel whereby the gate voltage is applied across the gate dielectric to induce inversion charges in the channel. However, the presence of any positive or negative charges within the gate dielectric would affect the inversion layer. The gate voltage, at which the transistor is turn on/ off, i.e. the threshold voltage, would then be shifted, as shown in the equations below:

The p-MOSFET threshold voltage, V_{TH} is denoted by Eqn. 2-1:

$$V_{TH} = V_{FB} - 2\phi_F - \frac{|Q_B|}{C_{OX}} \quad (\text{Eqn. 2-1})$$

where, $\phi_F = (kT/q) \ln(N_D/n_i)$, $|Q_B| = (4qK_s\epsilon_0\phi_F N_D)^{1/2}$ and C_{OX} is the oxide capacitance per unit area. The flatband voltage, V_{FB} is expressed by the Eqn. 2-2:

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{OX}} - \frac{Q_{it}(\phi_s) + Q_{ot}}{C_{OX}} \quad (\text{Eqn. 2-2})$$

where Q_f is the fixed charge density, Q_{it} is the interface trap density and Q_{ot} is the oxide charge density.

As can be seen in Eqn. 2-2, the three parameters which affect the threshold voltage shifts are the interface trapped charge density Q_{it} , oxide charge density Q_{ot} and the fixed charge density Q_f .

$$\Delta V_{TH}(t) = -\frac{\Delta Q_{it}(t) + \Delta Q_{ot}(t)}{C_{ox}} \quad (\text{Eqn. 2-3})$$

The density of fixed charges Q_f is normally associated with the process conditions of the gate dielectric growth and it is considered negligible in the current advance MOSFET technology. Therefore, the only two possibilities which could cause the threshold voltage shift in p-MOSFET during operations are very likely to be 1) the interface trap density Q_{it} and 2) the oxide charge density Q_{ot} . It is highlighted that interface trap density Q_{it} depends on the surface potential Φ_s , because the occupancy of the interface trapped charge is surface potential dependent. As denoted in Eqn. 2-3, any changes in both of or either one of these charge densities during NBTI stress will result in a threshold voltage shift.

2.2 The Role of Interface Traps During NBTI Degradation

Before 1999, research on NBTI of p-type MOSFET was sporadic and was mainly a subject of academia. It was not paid much attention in industry, as there was a more severe instability problem due to hot carrier injection (HCI). The gate oxide thickness has been reduced aggressively, from 95 nm in the 1970's to the current 2 nm or thinner as to achieve a higher current drive and a lower power operation. However, the supply voltage could not be scaled down proportionally in order to maintain the circuit operation margin. Thus, the oxide electric field is increasing along with the scaling down of MOSFETs, leading to a more severe NBTI-induced degradation on p-MOSFET. On the other hand, as MOS devices were scaled down, a surface channel p-type MOSFET replaced

the buried-channel device to alleviate the short channel effect (SCE) [42], [43]. Boron used for p^+ -gate doping during the fabrication of surface PMOS devices could diffuse and penetrate through the gate oxide into the channel. This may cause a shift in the flat-band voltage and generate defects in the gate oxide. Therefore, nitrogen was then introduced into the gate oxide to reduce boron penetration and to reduce leakage current. In 1999, a more severe degradation of ultra-thin oxynitride gate p-MOSFETs subjected to NBT stress was reported by Kimizuka *et al.* [33]. And, it was further discussed by the author that, with further scaling of the gate oxide, the lifetime due to NBTI degradation would become shorter than that of HCI (Fig. 2-1). As a result, lots of attention has been placed on the impact of NBTI and its mechanism in the subsequent years till date.

Kimizuka, Symp. VLSI Tech. 73 (1999)

Figure 2-1: Examines the transition of lifetime limitation mechanisms as a function of gate oxide thickness. When the thickness of the gate oxide is reduced to be < 3.5 nm (after 1999), degradation due to NBTI begins to limit the device lifetime. [33]

Before the implementation of the fast measurements, it has been widely postulated the interface traps generated at Si/ SiO₂ interface during NBTI stress as one of the main charges contributing to NBTI degradation. It is known that Si is tetrahedrally bonded in the substrate, with each Si atom bonded to four Si atoms in the wafer bulk. During oxidation, lattice mismatch occurs. The bonding configuration at the surface will become as depicted in Fig. 2-2, where most of the Si atoms are bonded to oxygen atoms while some of the remaining Si bonds are left dangling ((100) orientation). As a result, these unsatisfied bonding configurations form an interface defect states which are generally known as the interface trap. It is an interface trivalent Si atom with an unpaired valence electron at the Si/ SiO₂ interface, which is often denoted by $[\text{Si}_3 \equiv \text{Si}\cdot]$. (The “ $\equiv$ ” represents three complete covalent bonds to other Si atoms (the Si₃) and the “ $\cdot$ ” represents the fourth, unpaired electron in a dangling orbital (dangling bond)).

These interface traps are undesirable as they contribute to the threshold voltage shift, as shown in Eqn. 2-3. Thus, to prevent these interface traps from being electrically active, the common practice performed in the wafer fab is to perform hydrogen forming gas annealing to passivate the dangling bonds $[\text{Si}_3 \equiv \text{Si}-\text{H}]$. Unfortunately, the bonding energy formed between silicon and hydrogen is reported to be relatively weak ($\sim 1-3$ eV), based on first principle calculations [36]. Therefore, under nominal stress conditions, the Si-H bonds would be broken, causing the interface traps to be regenerated again which will cause an

impact on the V_t shift. The details of the impact of these interface traps on NBTI would be discussed further using a well accepted model, the Reaction-Diffusion (R-D) model.

Figure 2-2: Structural model (100) Si surface.

Detailed studies on the structure of this interface trap at the Si/ SiO₂ interface have revealed a family of defects known as P_b centers dominating interface traps. This P_b center [44]- [47] is a $[\text{Si}_3 \equiv \text{Si}\cdot]$ center with its unbounded central-atom orbital perpendicular to the interface and directed into a vacancy in the oxide immediately above it, as shown in Fig. 2-1. The electronic spin resonance (ESR) measurement has detected two P_b center variants, the P_{b0} and P_{b1} centers, which have been identified to have important contribution to NBTI degradation [48]. However, the nature and structure of P_{b0} and P_{b1} centers still remain debatable. Initially, the P_{b1} center was thought to be a Si atom backbonded to two substrate Si atoms, with the third saturated bond attached to an oxygen atom, designated as $[\text{Si}_2\text{O} \equiv \text{Si}\cdot]$. But, this idea was soon found to be inaccurate due to the calculated energy levels of this defect. The calculation seemed not to agree well with the experimental results [49]. Apart from that, there were also

other reports which have suggested the P_{b1} center to be an asymmetrically oxidized dimer, with no first neighbor oxygen atoms [47]. At last, in the late 90's, all of these debates came to an end. It was unambiguously established that both P_{b0} and P_{b1} are chemically identical to the P_b center [50]. Unfortunately, there was a charge state difference between these two centers indicating that P_{b0} was electrically active, while some authors believed the P_{b1} to be electrically inactive. The two different effects were found to be the result of strain relief in (100) silicon, due to the naturally occurring mismatch induced stress in the Si/SiO₂ layer during oxide growth.

2.3 The Role of Hole/ Oxide Traps during NBTI Degradation

Apart from the interface state generation, hole-trapping was observed as another major contributor to the threshold shift. After the implementation of fast measurements such as the Ultra-Fast measurement, "On-The-Fly" and etc, it was realized that there existed another degradation mechanism, in addition to the widely accepted degradation ascribed to the interface trap. This mechanism is now generally known as hole-trapping, which is postulated to be caused by the presence of oxide traps in the current SiON gate dielectric. Ang *et. al* has provided experimental results which highlights the generation of positive trapped charges, apart from the generation of interface traps during NBTI stressing on ultrathin SiON p-MOSFETs. Several other research groups have also further affirmed this observation. By using fast electrical measurements, it was shown that the generation of hole traps is a temperature insensitive process

with a low activation energy (~ 0.06 eV). Though evidence has pin-pointed out the presence of hole-trapping in NBTI degradation, the nature of this kind of oxide defect and its chemical reaction towards NBTI degradation mechanism still remain unknown till today. Initially, the NBTI community believed that trapping of H^+ , released via the dissociation of Si-H bonds, would give rise to a positive trapped charge which results in additional threshold voltage shift. However, the transport of H^+ in the gate oxide was not consistent with the time dependence of parametric shift. There were also some groups who believed that trapping of holes in the gate oxide would give rise to a positive trapped charge. Later in 1995, by using electron spin resonance (ESR) measurement, P.M. Lenahan has reported that E'_γ center (a hole trapped at an oxygen vacancy) in SiO_2 gate dielectric has the behaviour of a “switching” oxide-trap [51]. Besides, there were also observations made by Nicklaw *et. al* about the various categories of E' center in the gate oxide [52]. From a simulation study of the growth of SiO_2 using molecular dynamics, he showed that ~ 90 % of the E' centers exhibited minimal structural relaxation upon the capture of a hole. In fact, the increase in the strained Si - Si distance was so marginal that the remaining unpaired spin was still equally shared between the two Si atoms. This enabled a spontaneous reformation of the Si – Si bonds to happen once an electron was recaptured. Other categories of E' center may vary in the degree of structural relaxation [52]. In addition, more paramagnetic defects have been highlighted in the SiON dielectric. They are commonly known as the k_N centers, which may also be a possible candidature for the “switching” oxide-traps [53].

Nevertheless, with the continuous scaling down of the gate oxide thickness to tens of nanometer, instead of interface traps vs. hole/ oxide traps, some researches would rather regard them as the relatively permanent (P) component vs. recoverable (R) component in the context of dynamic NBTI (DNBTI). This would be elaborated further in the next few sections.

2.4 The Recovery Mechanism Observed During NBTI

As NBTI has come to the forefront of critical reliability phenomena in advanced CMOS technology in these recent years, the recovery (or relaxation) during NBTI has received increased attention. The stress damage was observed to recover very rapidly once the NBTI stress was removed. It may take many seconds to generate the NBTI damage, but it took split seconds to recover. There were arguments about whether NBTI damage recovers completely or partially. Ershov *et. al* proposed that there were two degradation components: a permanent component which remains after stress removal and a reversible component that recovers [54]. Huard *et. al* who has done extensive measurements, only found partial recovery [55], while Rangan *et. al*, on the other hand, showed complete recovery with the device being reset to its original state after the stress was removed [56]. They attributed NBTI degradation to the interface trap generation (N_{it}) and hole-trapping (N_{ot}) and claimed that the recovery was due to N_{ot} recovery with N_{it} remaining largely unchanged during the recovery phase. Fig. 2-3 shows the threshold voltage and interface trap

density change during stress and recovery periods. Both $|\Delta V_t|$ and ΔN_{it} change proportionally during stress, but only ΔV_t shows a significant drop during the recovery phase with ΔN_{it} remaining almost constant. In contrast, Yang *et. al* showed that the threshold voltage recovery after stress cessation to be primarily due to interface trap passivation and not due to the hole de-trapping mechanism [57]. This passivation effect could be enhanced by positive gate bias during the recovery phase. Not long ago, Teo *et al.* has discussed about the NBTI recovery phase from another perspective [19]- [20], [161]. The author has observed a fast and a slow recovery component during the relaxation phase of dynamic NBTI (40 cycles). Evidences further showed that dynamic NBTI is made up of a symmetric “switching” hole-trap mechanism superimposed on a background of relatively permanent deep-level hole-traps and interface-state generation. The amount of $|\Delta V_t|$ recovered by the “switching” hole-trap was shown to be constant, independent of the number of stress/ recovery (SR) cycles applied. This behavior is inconsistent with the hydrogen-transport model, which stipulates that the amount of $|\Delta V_t|$ recovered should decrease with an increase in the number of SR cycles [20], [166]. It has also been reported in [78], [144], [161] that a popular candidate suggested to play a role in the “switching” hole-trap was the E' center.

It should be mentioned that most of the studies on NBTI reported to-date have focused either only on the stress data or on a limited amount of stress and recovery data (typically 1 stress and relaxation cycle). P-MOSFETs operating

under negative gate voltage at high temperature tend to degrade with stress time due to the accumulation of interface traps and oxide trapped charges. However, p-MOSFETs in circuit operation do not always work under a static gate biasing condition. During the operation of a p-MOSFET in a CMOS inverter, the applied gate voltage is switching between “high” and “low” voltages, while the drain voltage is alternating between “low” and “high” voltages correspondingly. Similar dynamic modes are also observed when p-type MOSFETs function as part of DRAM, SRAM, sense amplifier, etc. Therefore, the performance of p-MOSFETs under dynamic stress has attracted considerable momentum in the recent years.

Figure 2-3: Relative shift observed for (a) $|\Delta V_{th}|$ and (b) ΔN_{it} versus stress time under a negative and positive gate bias. [34, 35]

2.5 The Reaction-Diffusion (R-D) Model

The most widely cited explanation for NBTI is none other than the reaction-diffusion (R-D) model [36]. It was proposed by Jeppson and Svensson in 1977 to provide a systematic explanation for NBTI studies [58]. This model was

derived purely based on the interface trap theory and was primarily used to describe the mechanism of interface state generation at the Si/ SiO₂ interface, which translated to the threshold voltage shift (ΔV_{th}) in the contemporary p-MOSFETs. As the research on NBTI advances, R-D model though remained accepted, has been widely fine-tuned by Alam *et.al*, Manahapatra *et.al* [59], [60] and Ogawa *et.al* [61] to explain many key experimental features, such as:

1. Threshold voltage degradation due to NBTI is given by $\Delta V_t \sim A \exp(-nE_D/kT) t^n$ with $n \sim 0.25$ and $E_D \sim 0.5 \text{ eV}$. [60], [62].
2. As NBTI became a long term reliability concern, many research groups looked for and found long-term reduction of NBTI time-exponent n from 0.25 to 0.13-0.16. [38], [63].
3. Once NBTI stress is removed, a fraction of interface traps will self-anneal [61]- [62], [64].
4. Temperature dependence of NBTI reveals a characteristic of dispersive transport [65], [66].

2.5.1 Framework of R-D Model

The essence of the R-D model may be summarized as follows. When a negative gate stress is applied to the gate terminal of the p-MOSFETs, there would be inversion of holes generated in the channel during the degradation process. Some of these energetic inversion holes would be captured via field assisted tunneling by the passivated Si-H covalent bonds at the interface. As a result, dangling Si bonds (P_b centers) are formed and hydrogen is liberated at the Si/

SiO₂ interface by an electrochemical reaction involving Si-H bonds and holes from the inversion layer. This newly released hydrogen from the broken Si-H covalent bonds would diffuse away from the interface, leaving behind a positively charged interface state (Si⁺) which is responsible for a threshold voltage shift and a lower transconductance of the p-MOSFETs. On the other hand, when the gate stress is removed during the recovery process, since the dissociation of the Si-H bonds that forced forward the diffusion of the hydrogen away from the interface is removed, the dangling Si-H bonds would be re-passivated by the available hydrogen which is very near at the interface instantaneously; while those remaining hydrogen which are further away from the interface would slowly diffuse back and recombine with the broken Si-H bonds at a slower rate.

Figure 2-4: Model for hole-assisted field-enhanced thermal dissociation of Si-H bond resulting $k_f \propto E_c \exp(\gamma_T E_{ox}) \exp[-(E_F - aE_{ox}) / k_B T] \propto E_c \exp(\gamma E_{ox})$. Resultant field acceleration factor can be written as $\gamma = \gamma_T + a / k_B T$. [36]

These two were the initial proposed mechanisms taking place during NBTI stress and recovery. The former hole capture event and interface state

generation were termed as the “reaction phase” while the latter hydrogen diffusion away from the interface was termed as the “diffusion phase” as illustrated in Fig.2-5. In recent years, modification to the classical version to incorporate dispersive transport behavior in the amorphous gate oxide has been made [66], [67]. The move was aimed at enhancing the flexibility of the basic model to cater wide variations in state-of-the-art gate oxide technology, which were believed to be at the root of recent experimental discrepancies. Nevertheless, the basic premise that NBTI is driven by a hydrogen-transport mechanism remains unchanged.

Figure 2-5: (top) Schematic description of the reaction-diffusion model used to interpret interface-trap generation during NBTI stress. Broken Si–H bonds at the Si–SiO₂ interface create Si⁺ (interface traps) and H. Initial interface–trap generation rate depends on Si–H bond dissociation (reaction), while the later rate depends on H removal (diffusion). Some H dimerized into H₂ since H is a slow diffuser. The H may diffuse (middle) or drift (bottom) away from the interface depending on the charge state of the diffusing species. [37]

2.5.2 Discrepancies of the R-D Model

As mentioned earlier, the interface trap generation was ascribed to the dissociation of Si-H bonds and subsequent diffusion of hydrogen species away from Si/ SiO₂ interface. Upon the removal of stress, hydrogen remaining at the interface would re-passivate Si-H bonds and reduce the interface trap generation. This model was successful then due to its ability to match the evolution of the p-MOSFETs' parameter drift, such as the $|\Delta V_t|$. Furthermore, the R-D model self-consistently explained the recovery which took place when stress was removed, in terms of hydrogen back-diffusion and re-passivation of interface traps. However, only when the discrepancies begin to surface due to the effect of NBTI recovery [38], [68], researchers were forced to abandon conventional Stress-Measure-Stress (SMS) approach.

Deviation of experimental stress data from the prediction of the R-D model has been discovered. Major observations such as much smaller exponent n of ~ 0.1 yielded by fast measurement [69] and larger exponent artificially yielded by longer measurement delays [38] casted serious doubt over the experimental basis of R-D model [58]. It was later proposed that it was molecular hydrogen (H₂) which diffused away from the interface during diffusion phase, instead of atomic hydrogen. This reason given was that atomic hydrogen was inherently unstable and would dimerize to form H₂ molecules. Improvement was then made to the R-D model to include dimerization of H₂ as an important stage in the initial evolution of the exponent n , from a relatively large value to a

subsequent value of ~ 0.178 [36]. Exponent of drift curves smaller than 0.167 were ascribed to trapped holes (ΔN_h), sensed at the same time as the interface traps (ΔN_{it}) by fast measurement methods [69]. Lee *et al.* has reported successful separation of individual contribution of ΔN_{it} and ΔN_{ot} towards the as-measured $|\Delta V_t|$ [70] as it was argued that ΔN_{ot} contribution to the as-measured $|\Delta V_t|$ must first be excluded before the underlying mechanism for ΔN_{it} could be revealed. Apart from that, deviations of the experimental recovery data from the prediction of the R-D model were also reported. R-D model predicted a slower initial recovery, with most of the subsequent recovery taking place over about three decades of time which differs from experimental observations [71]. Later, this discrepancy was reported to be able to be reconciled by a combined dispersive hole and hydrogen transport model [72]. A dispersive hydrogen transport model has also been employed by some authors [66], [67] to explain the variation of exponent n with temperature, i.e. the non-Arrhenius behavior of NBTI. The dispersive model was a natural extension of the Reaction-Diffusion (R-D) model [140]. Kaczer *et al.* showed that the dispersive hydrogen transport model (disorder-controlled hydrogen kinetics) was able to explain the temperature dependence of the NBTI and this model could be further extended to include the transport of charged hydrogen [66]. Kaczer *et al.* proposed that the incorporation of nitrogen introduced deeper localized hydrogen states into the gate SiO₂ layer, thus increasing the dispersion of hydrogen transport. As a result, the NBTI exponent for SiON was reduced. Most importantly, this dispersion parameter was reported to be linked with the temperature-dependent

NBTI power-law exponent [66]. Other authors [70], [73]- [74], however, showed that $|\Delta V_t|$ due to ΔN_{it} display Arrhenius behavior, accounting for the hole-trapping component of $|\Delta V_t|$. Teo *et al.* reported that the NBTI power-law time exponent of ~ 0.16 was due to the contamination of hole-trapping mechanism being (after eliminating ΔN_{ot} , the actual exponent for ΔN_{it} was observed to be ~ 0.27) [19]. Apart, it was argued that a consistent exponent n of $\sim 0.25-0.27$ was also noticed over a wide temperature range after excluding the effect of ΔN_{ot} from the total NBTI degradation. This ruled out dispersive transport as the mechanism for the increase in exponent n with temperature [19]. Hence, the need for a dispersive transport framework to reconcile only the recovery characteristic appeared illogical. It was shown that the discrepancy between model simulation and experimental recovery characteristics may be resolved by taking various hydrogen transport properties in the polysilicon gate and SiO_2 into consideration [75]. Several other issues remained, though this enhanced R-D model was able to explain the greater recovery of thick SiO_2 . One example was the existence of “non-universal” behaviour, as a result of imposing different hydrogen diffusion speeds in the SiO_2 and polysilicon model simulation [72]. Besides, being essentially a transport-based model, the enhanced R-D model suffered from an intrinsic limitation similar to the classical R-D model such as the “non-RD” characteristics observed in DNBTI experiments recently.

2.5.3 Predictions of the R-D Model in Regards to Dynamic NBTI

An important feature of the hydrogen-transport model which is not frequently discussed but evident in the [H] profiles in Fig. 2-6, relates to the fact that a fraction of the hydrogen species continue to diffuse away from the Si/ SiO₂ interface, even during the recovery phase [64]. This implies that 1) ΔN_{it} relaxation would not be complete in a given SR cycle 2) the amount of ΔN_{it} relaxation per SR cycle should reduce progressively with the increase in the number of SR cycles. The reason behind is, in each cycle more hydrogen is moved away from the Si/ SiO₂ interface during stress and relax phases, hence further limiting the amount of ΔN_{it} relaxation in the ensuing cycles. The hydrogen is close to the Si/ SiO₂ interface when the number of SR cycle is small, resulting in a relatively large ΔN_{it} recovery. The results depicted in Fig.2-7 are borne out by the R-D simulation. As can be seen in Fig. 2-8, after the 30th SR cycle, the hydrogen “diffusion front” has advanced significantly further away from the Si/ SiO₂ interface, accompanied by a corresponding substantial decrease in the hydrogen concentration at the interface. The latter outcome is also in agreement with the self-limiting recovery characteristic shown in Fig. 2-7 (b).

Figure 2-6: Evolution in the hydrogen concentration [H] profile and the corresponding interface state generation, ΔN_{it} under dynamic NBTI in the context of the reaction-diffusion model. (a) The stress period, t_s is fixed while the recovery period, t_r is varied. A longer t_r leads to greater recovery of ΔN_{it} due to more back diffusion of hydrogen. (b) t_s is varied while t_r is fixed. A longer t_s leads to lesser recovery of ΔN_{it} since hydrogen has been transport further away from the Si/SiO₂ interface and thus more time is required for a given amount of hydrogen to diffuse back towards the interface. It should be pointed out that even during the recovery interval, some hydrogen continues to move away from the interface (see typical profiles at the end of the recovery period). This gives rise to self-limited recovery. [38]

Figure 2-7: (a) Evolution of interface state generation, ΔN_{it} under dynamic NBTI. The data were obtained from simulation based on the reaction-diffusion model (molecular hydrogen diffusion). Gate oxide thickness: 2 nm; gate stress voltage: -2.6 V; gate recovery voltage: -1 V and temperature: 100°C . (b) Amount of ΔN_{it} recovered per cycle, ΔN_{it}^r as a function of the number of stress/ recovery cycles. ΔN_{it}^r is observed to decrease as the number of cycles increases, exhibiting a self-limiting recovery behavior. [39]

It should be noted again that almost all NBTI studies reported to-date have focused either only on the stress data or on a limited amount of stress and recovery data, typically only one stress and relaxation cycle. If the hydrogen-transport model were indeed valid, it should remain consistent over many cycles of dynamic NBTI. The experimental results shown in Chapter 4 are, however, not borne out by the R-D simulation and framework. In Chapter 4, the experimental results show that although the initial few cycles of stress/ recovery

(SR) may appear to confirm the hydrogen-transport model, characteristics of later cycles deviate substantially. These results will be elaborated in details in the chapter.

Figure 2-8: Profiles of hydrogen concentration $[H]$ as a function of distance x into the oxide at the end of selected stress cycles. As stress/ recovery cycling progresses, $[H]$ at the SiO_2/Si interface decreases (arrow A) and the diffusion front advances further away from the interface (arrow B), indicating that more hydrogen has been transported away from the interface. These changes lead to the self-limiting recovery behavior depicted in Fig. 2-7 (b), since the amount of hydrogen back-diffusion (and hence available for re-passivation of interface states) in a given recovery interval would become gradually lesser as more hydrogen is transported further away from the interface with stress/ recovery cycling. [39]

Figure 2-9: (a) Power-law time dependence of as-measured threshold voltage shift $|\Delta V_t|$ (open symbol). The relatively small exponent of ~ 0.1 is ascribed to hole-trapping. An exponent of 0.167, obtained after subtracting a constant contribution of hole-trapping, supports the proposition of H_2 -diffusion-limited interface state generation. [20]

Figure 2-9: (b) Evolution of as-measured $|\Delta V_t|$, showing, at the onset of stress (recovery), abrupt increase (decrease) attributed to fast trapping (detrapping of holes and repassivation of ΔN_{it} by interfacial H_2). The relatively slow recovery thereafter is ascribed to the back diffusion of H_2 . [20]

Figure 2-10: (a) Evolution of $|\Delta V_{t,r}|$ (normalized to the $|\Delta V_{t,r}|$ of the first cycle) during dynamic NBTI. The right axis shows $|\Delta V_{t,h}|$, “correction” due to hole-trapping. (b) Comparison of $|\Delta V_{t,r}|$ and $|\Delta V_{t,s}|$. Also shown is $|\Delta V_{t,EoR}|$, i.e., $|\Delta V_t|$ at the EoR, exhibiting a gradual increase with SR cycling. [20]

2.6 *P* and *R* Components in the Context of Dynamic NBTI

Recent research indicates that two components dominantly contribute to NBTI degradation [69], [76]- [78]: while one component dominates the recovery (*R*) the other one has been suspected to be more or less permanent (*P*). In this study, the permanent component is generally known as defect which is unable to restore back to its precursor structure within the given time window of our studies, but its electrical state is still able to alter/ transit from one state to the other. As NBTI research advances, there is a change of term from interface traps vs. hole/ oxide traps to permanent (*P*) vs. recoverable (*R*) component. This change of terms is done because it is getting harder to distinguish between the interface and bulk oxide defects when the gate oxide is becoming thinner and thinner due to scaling effect. Hence, there are several groups of researchers who prefer to adopt the term permanent component due its long recovery time characteristic observed during DNBTI and vice versa for the recoverable component. The main constituent of the *P* component is believed to be the P_b centers (interface dangling bonds) [79] while the physical origin of *R* is still strongly debatable till date. Our work has shown that some fraction of *P* might be related to the “switching” hole-traps.

As for the *R* component, it has been mentioned earlier in Section 2.3, a widely proposed candidate for it at/ near the Si/ SiO₂ interface is the E' centre ($O_3 \equiv Si^+ \cdot Si \equiv O_3$, as illustrated in Figure 2-11), arising from the oxygen vacancy defect [80] or the k_N centre ($N_3 \equiv Si^+ \cdot Si \equiv N_3$) [20], due to its repetitive and cyclic

behavior responsible for the $|\Delta V_t|$ fluctuations during dynamic NBTI. Owing to their proximity to the Si substrate, the hybridized, “dangling” sp^3 orbital on one of the Si atoms can readily exchange electronic charge (via quantum mechanical tunneling) with the underlying Si, causing the E' or k_N defect centers to rapidly “cycle” back and forth a positively charged state and a neutral state [80].

Figure 2-11: Schematic illustration of the E' center model for NBTI [10]. An important feature of this model is the significant asymmetrical structural relaxation which occurs upon hole capture ($1 \rightarrow 2$), which results in one of the Si atom moving past the plane containing the oxygen atoms and getting back-bonded to a neighboring oxygen atom. This significant structural relaxation reduces the likelihood of the reformation of Si-Si bond ($3 \rightarrow 1$). Transition from state 3 to 2 (during stressing) and from state 2 to 3 (during relaxation) are believed to explain the cyclic shifts observed in the threshold voltage $|\Delta V_{th}|$. [161]

However, there are also some groups which believe that this cyclical and repetitive behavior of R might be just a simple charging/ discharging process at the pre-existing trapped-hole sites near the interface during stress and it has therefore, nothing to do with BTI. This report will study deeply and mainly on the underlying mechanism of the R component.

2.7 Interdependence of Gate Oxide Reliabilities:

Reliability mechanisms of CMOS transistors have been studied intensely throughout the years to understand their nature of failure in the silicon-based gate oxide. However, these degradation mechanisms were studied separately and least attention has been placed on the interaction and interdependence of these reliabilities with one another. Issues concerning the reliability of gate dielectrics constitute one of the most serious challenges in the scaling of ULSI devices. An understanding of a particular gate oxide degradation mechanism is no longer sufficient in realizing highly reliable devices. There is an urgent need to consider the interactions among different gate oxide reliabilities carefully in order to have a more accurate device lifetime prediction. Our group has noticed and reported the possibility of the “switching” hole-trapping responsible for the $|\Delta V_t|$ fluctuation observed during dynamic NBTI to share a common defect origin with the bulk traps generated during Stress-Induced Leakage Current (SILC). An in depth discussion about this will be presented in Chapter 6. Though it has been generally agreed that gate oxide breakdown occurs after a sufficiently high density of neutral electron traps has been built-up in the gate oxide [183], the degradation mechanism especially about how these defects/traps are generated still remains as a matter of debate.

2.7.1 The Interrelation of Time Dielectric Dependent Breakdown (TDDB)/ Stress Induce Leakage Current (SILC) with NBTI

Although the SiO₂ degradation mechanism still remains controversial, the 2 proposed models for the wear-out process were none other than the widely cited “Interfacial Hydrogen Release Model” (HR) [184] and the “Anode Hole Injection Model” (AHI) [185]. In the HR model, traps are created by the diffusion of the released hydrogen from the anode by injected hot electrons while in the AHI model, defects are created in the gate oxide by the injected hot holes generated by impact ionization at the anode when attacking the weak spots (strained Si-H or Si-O bonds). It has also been reported in [186] that hydrogen release played a vital role in the deterioration in the gate oxide interface and bulk based on AHI, HR model and NBTI.

Figure 2-12: NMOS transistors with L/ W = 0.225 μm/ 20 μm were stressed at V_g = -5.6 V for 200 s. T_{ox} = 3.7 nm. SILC measured at V_g = -3.5 V. [182]

As proposed in the Anode Hole Injection (AHI) Model, there would be a transfer of energy from the tunneling electrons which enter the anode to the electrons in the valence band. This results in the generation of energetic holes

which may be injected into the gate oxide. A fraction of these injected holes would be trapped in the gate oxide. A new electron trap could be created again if a trapped-hole recombined with the subsequent injected electron. Hence, the AHI model is supported by data which shows a one-to-one relation between hole fluence and trapped electron density [183]. It has been suggested by J. Wu that a model for gate oxide breakdown which involves the release of interfacial hydrogen may not be accurate. The author has shown that the gate oxide reliability of devices annealed in deuterium was similar to that of devices annealed in the hydrogen [182]. Both theoretical considerations and STM results implied that it would be more difficult for energetic electrons to break the Si-D bonds as compared to the Si-H bonds due to its smaller desorption yield (~50 times smaller than that of a hydrogen-passivated surface). Based on this, it is understood that transistors passivated with deuterium at their Si/ SiO₂ interface should have more resistance towards hot carrier induced degradation. In [182], it was also observed that D₂ annealed devices did not have better gate oxide reliability than the H₂ annealed devices. The D₂ annealed gate oxides were found to be no less leaky than the normal forming gas annealed gate oxides as shown in Fig. 2-12. Apart from that, although the D₂ annealed oxides appeared to show a slightly longer time-to-breakdown than the H₂ annealed oxides (Fig 2-13, 2-14), the mean lifetime values were statistically indistinguishable.

Figure 2-13: T_{BD} of PMOS transistors. $L/W = 0.225\ \mu\text{m}/20\ \mu\text{m}$. $T_{ox} = 2.2\ \text{nm}$. Stress condition: $V_g = 4.5\ \text{V}$. [182]

Figure 2-14: T_{BD} of NMOS transistors. $L/W = 0.225\ \mu\text{m}/20\ \mu\text{m}$. $T_{ox} = 3.7\ \text{nm}$. Stress condition: $V_g = 6.3\ \text{V}$. [182]

On the other hand, although it has been reported that interface state generation and Stress-Induced Leakage Current (SILC) could be eliminated by substituting hydrogen with deuterium into the gate oxide [187], the other camp of thought infers that the released hydrogen from the Si/SiO₂ interface strongly correlates to the trap creation in the gate oxides. This marks a contrast to the AHI model. Besides, based on RD model, NBTI degradation is thought to be caused by interface state generation where the dissociation of the Si-H bonds by holes at the interface, followed by the diffusion of the released hydrogen into the gate

oxide. Hence, due to this similarity in the hydrogen release and diffusion, it has been inferred that SILC and NBTI have a common origin [188], [189]. Y. Mitani has reported that the hydrogen-related mechanism is an origin for not only NBTI degradation but also trap creation in the SiO_2 bulk. In [186], the author has discussed about the correlation between NBTI and SILC and concluded that the released hydrogen from the interface generated by NBTI stressing could create the bulk traps of SILC even when the energetic carriers were not injected into the gate oxide (under low NBT voltage). Furthermore, no SILC generation was observed under the incorporation of fluorine into the Si/ SiO_2 interface. It is widely accepted that the amount of hydrogen can be monitored by incorporating fluorine into the interface. Therefore, the absence of SILC generation under the presence of fluorine simply implies that no bulk traps are generated when the released hydrogen is dramatically suppressed by the fluorine. This, again, re-emphasize that hydrogen release plays a vital role during oxide degradation. It also highlights the possible correlation between NBTI and SILC.

Some of the proposed mechanisms for hydrogen-related gate oxide degradation are multi-vibrational hydrogen release (MV-HR), “Hydrogen Bridge” and others which are based on first principal calculations. The MV-HR was proposed based on the multi-excitations of Si-H bond [209]. And, in accordance with the amount of injected electrons, the vibration energy of hydrogen bonds at the interface would be excited up to an anti-bonding state. The breaking of the

Si-H bonds would occur once the excited energy exceeds the barrier energy. Besides, the “Hydrogen Bridge” takes place when the released hydrogen diffuses and breaks into the oxygen vacancies in SiO₂ network.

Though the results reported by J. Wu are consistent with AHI model, it does not constitute proof of the AHI model. But, most importantly, it sheds doubt on the HR model which purports that the release of interfacial hydrogen is a necessary step in the gate oxide wear-out process. Further investigation and evidences concerning the mechanism for hydrogen-related defect generation are still required even though M. Yatani has observed the correlation between the released hydrogen from Si/ SiO₂ interface and gate oxide deterioration and has thus further inferred that the gate oxides degradation could be explained comprehensively by considering the hydrogen release from Si/ SiO₂ interface. Our group has also observed the correlation between dynamic NBTI and SILC, *but*, in the **absence** of any hydrogen-related defects. An in-depth study on the conditions applied during dynamic NBTI stress was then carried out. It has been shown that the generation of bulk traps was actually a consequence of the “switching” hole-traps, manifested in a form of V_t fluctuation observed during dynamic NBTI, being transformed into a permanent charge state. Our results also implied that the voltage and temperature applied during NBTI stress would have an impact on the cyclic and constant recoverable behaviour of the “switching” hole-trapping process. Detailed evidences and observations would be reported in Chapter 4-6 later.

Figure 2-15: Schematic diagram for hydrogen- related trap creation. Can released H from Si/ SiO₂ interface diffuse into SiO₂ and create traps? [188]

2.7.2 Electrostatic Discharge (ESD) VS. NBTI

Another crucial degradation reported in the silicon-based gate oxide along with the scaling effect is the Electrostatic Discharge (ESD) [81]. With scaling, devices are less susceptible to the very short but large magnitude pulses applied during ESD testing. ESD is a natural phenomenon which occurs when charge is transferred from one surface to the other when they come into contact with each other. This is due to the difference in the electron affinity between the two types of atoms or molecules that made up the surfaces. The surface that loses electrons becomes positively charged and vice versa (triboelectric charging) and the electric charge will remain static on the surfaces until it comes into contact with another surface which is grounded or oppositely charged. ESD happens when a spark is observed when charges are rapidly flowing from one to another surface. The resulting discharge current and voltage generated are found to be damaging for integrated circuits and are becoming an urgent issue to be

resolved in the electronic industry. The three most widely discussed models for ESD event are the Human Body Model (HBM), Machine Model (MM) and Charge Device Model (CDM). The HBM models the “process” of a charged human body being discharged into a “grounded” IC while the MM models a charged metal surface discharging through a charged device or into a grounded device. On the otherhand, the CDM models a charged die within an IC being discharged when it comes into contact with a grounded metal surface. The three models are schematically represented in the following Fig. 2-16.

Figure 2-16: ESD stress models HBM, MM and CDM with typical parameters. [137]

Transmission Line Pulse (TLP) is generally used to evaluate ESD robustness of the HBM stresses. A sequence of rectangular pulses is applied by the TLP tester between the two terminals and a simple DC leakage between the two is

measured after each pulse. This is done to monitor the inception of device failure. The waveforms of the three categories of the ESD events are depicted in the Fig. 2-17 below. Amongst all, it is observed that CDM event has a very low rise time and a very narrow pulse width (~1ns). Charged Device Model (CDM) which accounts for the common oxide damage in the industry, emulates the fastest ESD event [82]. However, due to its difficulty in simulating the same pulse experienced by the device during real life application, the research about CDM is still not intensive enough. Hence, to improve CDM reliability testing, the TLP technology which is only able to provide a minimum of 200 ps rise time and 100 ns pulse width, has encountered lots of modification. Very Fast Transmission Line Pulse (VFTLP) tester has been suggested due to its capability of generating pulses (pulse width ~1 ns) which are comparable to CDM event. A DC measurement is performed after each pulse as an indicator to monitor the device's degradation [83].

Figure 2-17: RLC-Discharge current waveforms of the three basic ESD stress models HBM, MM and CDM for typical circuits in comparison with a TLP square pulse. [137]

Recent technology requires severe scaling down of MOS transistors. Hence, sub-nanosecond time-dependent characterization of gate oxide reliabilities and oxide breakdown mechanism become crucial for gate oxide modeling and lifetime prediction. It has been understood that ESD pre-stressing has caused the subsequent NBTI degradation to worsen on thin oxide devices while NBTI pre-stressing has only little dependence on the subsequent ESD performance [84]. However, it should be noted that the evidences/ explanations provided were less comprehensive as the effect of the applied NBTI pre-stressing conditions on the “switching” hole-traps was not considered and studied carefully. Moreover, the ESD tests were performed using a TLP tester.

As mentioned earlier, it has been reported that the recoverable “switching” defects (R) would remain constant throughout when nominal DNBTI conditions were applied [20]. However, as discussed in [85]- [86], there is a tendency for the recoverable “switching” traps (R) seen during dynamic NBTI to become relatively permanent under moderately high temperature or gate oxide field. As a result, transformation of the oxygen vacancies from E'_{δ} -type to E'_{γ} -type would occur [85], [87]. Almost no comprehensive studies have been conducted to study the NBTI-ESD or NBTI-ESD-TDDB correlation. One study has been reported on the NBTI-ESD interaction in 2007 [84]. The author showed that the ESD behavior has little dependence on NBTI pre-stressing. It was thus, suspected that the carrier tunneling during IV measurement performance neutralized the oxide charge which was introduced during NBTI pre-stressing.

Though this result presented supports part of our observations, this study is not conclusive enough. As mentioned earlier, the ESD performance was investigated using a TLP tester which was not able to simulate extremely short pulses experienced by the device in real fabrication experiment [84]. Moreover, due to the statistical nature of trap generation, individual measurements may lead to inaccurate conclusion. Hence, a larger sample size is suggested for characterization in order to improve the repeatability of the results observed. With the emergence of more evidences showing that the recoverable nature of V_t fluctuations during DNBTI could alter depending on the conditions applied during NBTI tests, there is a need to reassess the impact of NBTI pre-stressing on the subsequent ESD and TDDB degradation respectively.

In our work, the gate oxides were evaluated under the Very Fast Transmission Line Pulse (VFTLP) tester which is able to simulate CDM with a 1 ns pulse width. The breakdown voltage/ leakage current measured using the VFTLP tester is suspected to have the same defect origin observed during dynamic NBTI and TDDB. In Chapter 6, we provide evidences which support the interdependence of these degradation mechanisms. Plausible explanations on the nature of the defect origin will be discussed further.

2.8 High- κ / Metal Gate Transistors

2.8.1 Motivation of Using High- κ Gate Dielectric

Over the decades, silicon dioxide has been regarded as the perfect gate oxide material and has therefore been used extensively in the industry. As transistors have decreased in size due to scaling effect, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance. This thereby, increases the drive current and device performance. However, the device's performance reaches its bottleneck when the thickness scales below 2 nm when the leakage current increases drastically due to tunneling, resulting in a high power consumption. This causes the device to be unreliable. Therefore, by replacing silicon dioxide gate dielectric with a High- κ material, it allows a larger gate to substrate capacitance to be achieved while keeping the gate leakage current within an acceptable range.

The gate oxide in a MOSFET is often modeled as a parallel plate capacitor. The capacitance, C of this parallel plate capacitor is shown in the formula below (ignoring quantum mechanical and depletion effects from the Si substrate and gate).

$$C = \frac{\kappa \epsilon_0 A}{t} \quad (\text{Eqn. 2-4})$$

Where

A is the capacitor area

κ is the relative dielectric constant of the material (3.9 for silicon dioxide)

ϵ_0 is the permittivity of free space

t is the thickness of the capacitor oxide insulator

Based on Eqn. 2-4, in order to compensate the reduced capacitance due to the thinning down of the gate oxide as a result of scaling, one method is to alter the κ value by replacing silicon dioxide with a High- κ material. By doing so, a thicker gate oxide could be selected to overcome the severe leakage problems which arise from further reduction of t , as well as to improve gate oxide reliability.

High- κ gate dielectrics have been studied as an alternative gate oxide for 45-nm technology nodes and beyond to replace conventional SiO_2 or silicon oxynitrides (SiO_xN_y) dielectric. To-date, it has been successfully integrated in the CMOS process [88]. In general, some of the principal requirements reported for the High- κ dielectric are as such 1) high dielectric constant 2) thermal and chemical stabilities when in contact with the Si substrate and 3) high band offset with electrodes (i.e., barrier height) to suppress leakage current. Hf-based oxides, including HfO_2 and HfSiO_x , have been regarded as the promising candidates for High- κ dielectrics due to their excellent thermal stability with Si. Furthermore, dielectric-stack optimization has improved the mobility of HfSiON devices, which was once underestimated due to transient charging during conventional characterization and the lack of understanding of the transient-charging behaviors in High- κ [89]- [90]. A band-edge metal solution for n- and p- MOSFETs has also been suggested to curb dopant penetration in

the poly-Si/ High- κ stacks, besides improving the inversion oxide-thickness (T_{inv}) scalability, the threshold voltage (V_{th}) controllability which is caused by Fermi-level pinning, and some other poor reliability issues [91]- [95].

2.8.2 PBTI/ NBTI on High- κ Metal Gate Devices

It has been reported in [96]- [98] that obvious threshold voltage shifts were observed under both positive bias and negative bias in High- κ gate stacks transistors. PBTI on High- κ gate n-MOSFETs has therefore, gained momentum and interest from the research community and the industry. Initially, the degradation was worse compared to conventional SiON gate dielectrics. It was suspected that charge trapping, the filling of pre-existing bulk traps in the complex deposited HfSiON, caused the threshold voltage to shift and the drive current to degrade over device operation time [99]. This has, however, later been overcome with the optimization of Atomic Layer Deposition technique and additional deposition of SiO₂ interfacial dielectrics underneath the High- κ layer. Till then, BTI induced threshold voltage shift in High- κ devices was observed to be comparable to those observed for silicon-based oxide devices. Although the significant threshold voltage shift has been resolved, there are still a number of fundamental issues, such as fixed charge, reduced channel mobility and trapped charge to be overcome before integrating High- κ / metal gate stack into the CMOS mainstream [96], [100].

There are two kind of defects contributing to the significant positive threshold voltage shift (ΔV_{th}) of PBTI on n-MOSFETs, 1) the voltage stress-induced defect [101]- [102] and 2) the preexisting electron traps [103]. It was interestingly shown by D. P. Ioannou that trap generation processes could be activated under certain stress conditions, in addition to electron trapping in the preexisting precursors [104]. Besides, investigations done to study Stress-Induced Leakage Current (SILC) have indicated that it was also possible to attribute trap generation to the predominant V_{th} increasing mechanism at operation conditions. Thus, based on these observations, D. P. Ioannou has proposed a two-mechanism-based semi-empirical PBTI model. Apart from that, it was also shown that the preexisting and stress-induced traps exhibited similar detrapping kinetics, as observed in the V_{th} instability relaxation experiments carried out at a carefully selected range of bias and temperature conditions. These results suggested that both types of defects may share the same physical nature.

2.9 Impact of Lanthanum (La) on NBTI/ PBTI of High- κ Metal Gate Transistors

As poly-Si/ High- κ stacks are limited by dopant penetration, threshold voltage (V_{th}) controllability by Fermi-level pinning and inversion oxide-thickness (T_{inv}) scalability [91]-[93], [95], a band-edge metal solution for n- and p-MOSFETs has been proposed. And, a lot of effort have been put in material screening to

search for suitable band-edge electrode materials [92], [105]- [106]. Apart from that, a simple rare-earth metal-doping technique has also been suggested for V_{th} modulation [107]-[109], [110]. Among various rare-earth metals, lanthanum has been observed to be a strong candidate for n-MOSFETs because of its good carrier mobility, low V_{th} , and good EOT scaling. Besides La, a few other rare-earth metals such as erbium (Er) and gadolinium (Gd) could be possible candidates to achieve n-MOSFETs V_{th} modulation [107], [111]. However, due to their difference in electronegativity and dipole radii, the incorporation of these elements into the $HfO_2/HfSiO$ gate oxide would degrade the carrier mobility, resulting in less of a V_{th} control margin and a higher EOT. After careful consideration, La was selected to be introduced into High- κ metal gate stack to modulate V_{th} of High- κ gate n-MOSFETs. La, which is electropositive would diffuse into the High- κ / SiO_2 interface to form a dipole during a high-temperature- dopant- activation step. It shifts the band offset and hence, helps to tune the effective work function of the electrode.

Figure 2-18: (a) V_o as an electron trap site in the monoclinic HfO₂ (b) Corresponding V_o site neighboring two substitutional La atoms at Hf sites. The difference in the electron trap levels between HfO_x and HfLaO_x is found to be 0.5 eV. [40]

Various models were reported in the attempt to explain the V_{th} / flat-band-voltage (V_{fb}) modulation in HfO₂ or HfSiO gate dielectric under the influence of La. One of the widely cited models was the positive charge by oxygen vacancy and interface dipoles model [107]- [109], [112]- [114]. Unlike the V_{th}/V_{fb} modulation caused by additional positive charge generation in the dielectric, devices with La showed excellent carrier mobility due to the short range of the dipole electric field [107], [115].

Though HfO₂ gate dielectric with La incorporation seems to be a promising, strong candidate for future n-MOSFET integration, the impacts of the La-induced dipole on the devices' performance and dielectric reliability have yet to

be studied and discovered thoroughly. It was reported that La did not degrade BTI in the early studies [110]. In fact, the lifetime of La incorporated oxides was still able to meet the requirement set [116]. In [110], the author discovered that La incorporation could improve PBTI performance as La was observed to suppress pre-existing defects [117], but on the other hand, enhance stress-induced degradation. Pre-existing defects and stress-induced defects are two categories of defects which affect PBTI in HfSiON of n-MOSFETs. In [120], Du *et al.* tried to probe the nature of the defect under the influence of La. The origin of the defects was thought to be oxygen vacancy related defects, generated under positive stress. In order to understand the effect of the La incorporation into Hf-based oxide, the author has estimated the formation energies of an oxygen vacancy (V_o), which acted as an electron trap site [118] in HfO_x and HfLaO_x from first-principles calculations [119]. It was found that the electron trap level was raised by 0.5 eV, as a result of the increase in the V_o formation energy around La atoms as depicted in Fig. 2-18, contributing to the suppression of the electron traps. This simulation result was also consistent with Du *et al.*'s experimental observation, i.e., pre-existing carrier traps were suppressed by the La incorporation. However, La incorporation, on the other hand, could also render the dielectrics more sensitive to thermal and stress-induced defects. It is now understood that the La-O molecules are weakly bonded as compared to the Hf-O bonds. This might be due to the larger atomic size of La (lower valence number; longer ionic radius, distance between Hf-O is smaller than that of La-O) resulting in a weaker Coulombic force attraction

between the La and O atoms as compared to the Hf-O bond. Thus, the La-O bonds are relatively easier to be broken upon applying a stress onto it. Furthermore, it is also understood that Hf-O bond is less ionic as compared to the La-O bond (La is less electronegative than Hf).

Figure 2-19: Schematics of La-O and Hf-O bonding. The attractive Coulomb force between La and O is weaker than that between Hf and O because of the effect of the lower valence number of La compared to Hf and the longer bond length of La-O. [41]

These properties (larger atomic size of La and the more ionicity of the La-O) result the La-O bond to be rendered and cause it to be more sensitive to an electric field. This might be the reason to the increase generation of stress-induced defects in the La-doped HfSiON devices. Du *et. al.* also elaborated further by explaining about the generation of V_o , which in return, induced the formation of the interstitial oxygen (I_o) whose energy level was located near the valence band maximum of Si [41]. The V_o - I_o pair theory was proposed based on trap-assistant theory in La-doped HfSiON gate dielectrics. Due to the increase in the conduction which is caused by the trap-assisted valence electrons, the V_o - I_o Frenkel pairs are easily generated under a stress, which is also believed to be

“enhanced” by the higher ionicity of the La-O bond and the weaker Coulombic force between the La and O atoms as discussed earlier.

2.10 Chapter Summary

In summary, the history of NBTI and the widely cited Reaction-Diffusion model are briefly introduced in this chapter, followed by the discrepancies of the R-D model based on the recovery phenomena observed during dynamic NBTI studies. The behavior of the “switching” hole-trap which is shown to be constant, independent of the number of stress/ recovery (SR) cycles applied, is inconsistent with the hydrogen-transport model, which stipulates that the amount of $|\Delta V_t|$ recovered should decrease with an increase in the number of SR cycles. Besides, reports about the interdependence of NBTI, TDDB and ESD are mentioned and studied. This chapter also summarizes the background and associated reliability issues of High- κ / metal gate stack, used on 32nm technology onwards. Lastly, the impact of Lanthanum on reliability is briefly discussed.

CHAPTER 3: NEGATIVE-BIAS TEMPERATURE INSTABILITY (NBTI) CHARACTERIZATION TECHNIQUES

This chapter first discusses about various characterization/ measurement methods and their revolutionary progressions as Negative-Bias Temperature Instability (NBTI) research progresses throughout the years, all the way back from the 1960s till to-date. It also briefly explains the drive to have a fast measurement method in order to eliminate/ reduce the impact of recovery during NBTI measurement. Special emphasis and elaborations would be done in the later section on a kind of fast measurement technique, named *Ultra-Fast Switching* (UFS) method which was developed by our group members. This technique has been used extensively in this project.

3.1 Introduction and Motivation: Slow vs. Fast Measurement Techniques

It was reported in literature reviews that, NBTI test results were strongly affected by the spontaneous recovery upon the release of electrical stress [121]- [122]. This often occurred especially when there was a delay in the measurement. Some of the factors which NBTI results were noticed to be extremely sensitive of, were 1) the positive gate bias applied [123] and 2) the measurement delay [124]- [125]. Hence, a precise measurement of the threshold voltage shift ($|\Delta V_{th}|$) is in need to establish a more comprehensive picture of the physics and mechanisms behind NBTI degradation.

Slow measurement has been used to characterize Negative-Bias Temperature Instability (NBTI) degradation until the emergence of fast measurements to minimize measurement delay. Generally, conventional slow measurement method has the following sequence: stress-measure-stress. Measurements are first performed on fresh devices to obtain the initial states when the devices are not stressed. After that, electric field stressing is exerted on the devices. In order to monitor the continuous parametric shift of the devices (usually the drain current is measured), measurements are done by interrupting the stress numerous times. With the $I_d - V_g$ curves obtained, the shift in threshold voltage (ΔV_{th}) and subthreshold swing degradation could be easily extracted and calculated.

As can be seen in the conventional DC NBTI measurement, the measuring sequence is stress – measure – stress..., in which the gate stress voltage is interrupted periodically according to the user-defined time array and the gate voltage is swept from 0 to the operating voltage with a small drain bias voltage in order to measure the $I_d - V_g$ curve. The periodical interruption of stress results in measurement delay and has allowed large amount of the $|\Delta V_{th}|$ recovery to take place. The measurement delay is observed to range from a few seconds to tens of seconds accordingly. Thus, to avoid being misled in understanding NBTI degradation mechanisms, the recovery effect in $|\Delta V_{th}|$ due to the measurement delay as observed in the conventional DC measurement should be avoided. As reported to-date, various fast measurement methods have already been developed to minimize or to eliminate the recovery effect

as mentioned above. There were generally two main approaches used in eliminating or reducing the measurement delay when measurements were taken. It first started off with the idea of taking NBTI measurements at its stress voltage *without* terminating the electrical stress. One well-known example which was often reported was the **On-The-Fly** (OTF) measurement method. This technique keeps the variations on the gate voltage during measurement to its minima [126] and captures the I_d degradation and real time G_m . In order to get rid of a potential recovery effect, the fundamental way is to maintain on the stress gate voltage, $V_{g, \text{stress}}$ for the whole duration of the experiment. By applying small pulses on the gate voltage around the stress value $V_{g, \text{stress}}$ every time a measurement is required, as depicted in Fig. 3-1. By this way, not only the linear drain current I_{dlin} at stress voltage $V_{g, \text{stress}}$ is monitored but also linear drain currents at $V_{g, \text{stress}} \pm \Delta V_{\text{sense}}$ [129]. Based on Eqn. 3-1, $G_m (V_{g, \text{stress}})$ variation with time along the stress could be evaluated and the $|\Delta V_{th}|$ could thus be calculated from $|\Delta I_d|$.

$$g_m(V_g, t) \cong \frac{\Delta I_{dlin}}{\Delta V_{gsense}} \quad (\text{Eqn. 3-1})$$

However, one serious setback observed in OTF is the limitation of not being able to measure the threshold voltage shift before the first measurement point. It should be mentioned that the $|\Delta V_{th}|$ calculated at stress voltage differs from $|\Delta V_{th}|$ extracted in subthreshold region [127]. Measurements which are obtained at stress conditions might trigger additional degradation mechanisms which may lead us in over-

estimating NBTI impact on the transistors, especially during its normal operation [128].

Figure 3-1: A simple schematic of the on-the-fly measurement methodology. The shift in the linear drain current as well as the associated variations in the transconductance g_m can be monitored. [Data after Ref. [129]]

Besides, there are also other established measurement methods such as the **Fast Switching (FS)**, **Ultra-Fast V_t (UF V_t)** and **Ultra-Fast I_dV_g (UF I_dV_g)**. These techniques mentioned adopt the second approach where measurements are taken by applying an extremely short interruption to bring the voltage level from the stress voltage down to a desired measurement level. Hence, the probability of inducing additional (unwanted) degradations during stress conditions would be reduced. The FS technique measures the drain current degradation by raising the gate voltage in the transistor's linear or saturation region. By assuming that $|\Delta V_{th}|$ is linearly proportional to $|\Delta I_d|$, $|\Delta V_{th}|$ could be easily obtained. As for the Ultra- Fast I_dV_g (UF I_dV_g), short

pulses are injected by the pulse generator to bring the gate voltage back to the stress voltage from the measurement voltage in an extremely short duration ($\sim 1 \mu\text{s}$) [130]. The low noise pre-amplifier converts the drain current to voltage and the oscilloscope captures it subsequently together with the gate voltage. Hence, by reconstructing the results from the oscilloscope, $|\Delta V_{\text{th}}|$ can be extracted from the generated I_d - V_g curves. Lastly, the Ultra- Fast V_t (UF V_t) measurement [131] uses a negative feedback loop to transit gate voltage to V_{th} . Its measurement time can be within $1 \mu\text{s}$.

With the effort from all our group members, an Ultra-Fast Switching (UFS) method has been developed by combining customary pulsed I - V set-up with a simple $I_{\text{d,lin}}$ correction method. One point to highlight regarding this UFS methodology is, it is developed with the capability of minimizing the measurement delay down to sub-100 ns, which are much faster as compared to the other methods mentioned just now. It also has the ability to achieve gate pulsing down to 40 ns, taking advantage of the hardware setup which is based on Keithley 4200 Pulse IV setup. Besides, the drain current can be sampled at measurement voltage with similar measurement delay of 40 ns. This Ultra-Fast Switching (UFS) methodology set up will be discussed in details in the following Section 3.4.

3.2 Hardware Setup of the Ultra-Fast Switching Measurement Technique

3.2.1 DC vs AC Stressing

Half a century ago, DC voltage was more commonly preferred for BTI characterization as compared to AC voltage stressing due to its simple equipment set up. Besides, DC voltage stressing was observed to produce more stable experimental results. However, emphasis has been placed on AC stressing in the industry later because AC stressing was found to be able to simulate the real operation conditions of the transistors despite the involvement of the pulse generator, switching matrix and a more complicated controlling program in its hardware setting. A schematic drawing of the DC and AC (bipolar stress) is shown in Fig. 3-2.

In this project, DC stressing will only be applied when gate leakage current measurement is performed. In general, the gate of the devices were first swept within the range of -1 (or 1.5) $V > V_g > +1$ (or 1.5) V to obtain the fresh gate leakage current, $I_g - V_g$ curves. Thereafter, the devices were stressed with a constant DC voltage ($E_{ox} = \sim -10$ MV/ cm) for an intended period before making another voltage sweep to obtain its $I_g - V_g$ curve again after the constant voltage stress. This sequence of test was repeated for numerous times over a wide range of temperatures (the experimental conditions will be elaborated further in Chapter 4). The degradation in the gate oxide is simply reflected in the gate leakage current spectra $((I_g - I_{g0}) / I_g)$.

Figure 3-2: A simple schematic showing the static and bipolar gate stress voltage waveforms. For bipolar stress, a 100-kHz trapezoidal voltage pulse switching between V_g^s (equal to that of static stress) and a positive gate relaxation voltage V_g^r ($= +1.5$ V) are applied to the gate. The pulse transition time is 40 ns and the duty cycle is 50 %.The total stress time for bipolar stress is 2x of the time applied for static stress to achieve a net equivalent in the stress period. [135]

3.3 Components in Keithley Pulse-IV Setup

3.3.1 Port Power Divider

A 3-Port Power Divider is used to divide the electrical power equally among its three connectors using a 16.67Ω resistor in each port. The Power Divider is used on the gate of a FET to provide an impedance matched signal path.

Figure 3-3: (a) Schematic of 3-Port Power Divider, (b) Simplified schematic of Remote Bias Tee (RBT).

3.3.2 Remote Bias Tee (RBT)

The function of the RBT (Remote Bias Tee) adapter is to couple the DC bias and pulse output from pulse generator. The output of the RBT provides pulse output riding on the DC bias. The simplified schematic of the RBT is shown in Fig. 3-3 (b). The capacitor of RBT functions as a low-impedance component for high speed pulses, and as a high-impedance element for DC, allowing high-speed pulses from pulse generator to pass through to the output, while blocking DC from the SMU. The inductors function as low-impedance components for DC, and as high impedance components for high speed pulse, allowing the DC bias from the SMU to pass through to the output, while blocking the high speed pulses from the pulse generator.

3.3.3 Keithley Pulse-IV Hardware Setup

In this setup, the following equipments are used and the schematic setup of Keithley Pulse IV test system is pictured in Fig.3-4.

- Pulse Generator (4200-SCP2)
- Source Measurement Unit (4200-SMU)
- Remote Bias Tee (4200-RBT) / 3-port power divider
- Oscilloscope (4200-SCP2)

Both Pulse Generator (PG) and Oscilloscope (OSC) are used in UFS setup to achieve fast transient voltage source and simultaneous current capturing for easy software development, these equipments are integrated into the Keithley 4200 Semiconductor Parameter Analyzer measurement frame as module cards. The PG and OSC are used to test the coupling/ decoupling of the DC and AC signals on the device by 2 Remote Bias Tees (RBTs) and a 3-port power divider in which the RBT adapter is a coupler for DC bias and pulse output from the pulse generator. Fig. 3-4 demonstrates the hardware setup for the Pulse-IV measurement technique.

Figure 3-4: Schematic diagram of the Keithley Pulse-IV measurement technique hardware setup.

A pulse is applied by the Pulse IV setup to the gate of the device under test (DUT), while the drain is DC biased. The source and body connections are connected to the ground/ shield. The gate voltage and drain voltage are measured by the dual-channel scope card. The drain current is then calculated by the voltage drop across the 50 W termination of the scope. The corresponding waveforms, which are from some selected points to provide snapshots of the signals for the test system, are shown in Fig. 3-5. They also show the effects of various aspects of the setup. One thing to note is, though there are many waveforms being displayed in Fig. 3-5, there are only two waveforms that are actually measured by the scope card (waveforms B and E). The reason of showing all waveforms together is to compare the DC offset and the relative amplitudes in various parts of the schematic.

Figure 3-5: Waveform captured at selected points in the Pulse *IV* setup.

At the start of the test, the drain of the device under test (DUT) is biased with SMU2. A gate pulse is applied to turn the transistor on and to cause the drain current, I_d , to flow.

A. Gate Voltage Pulse

This waveform is the output from Channel 1 of the PG2 pulse generator card. Its amplitude is almost similar as that seen by the DUT gate (C), except for some small cable losses. There is no DC offset on this waveform, as any DC voltage would cause excessive power to be dissipated in the power divider.

B. Gate voltage pulse measured by the oscilloscope (oscilloscope channel 1)

This is the portion of the pulse that is transmitted through the power divider. Because of the divider and the 50 Ω input impedance of the scope, the amplitude of the pulse is reduced by 33%, including any additional cable losses.

SMU1: This is the voltage output by SMU1 during Pulse IV testing. In this illustration, the DC voltage is fixed at 0 V.

C. Voltage pulse at DUT gate

This waveform shows what the DUT gate “sees.” This is the pulse that turns on the transistor and causes the drain current to flow.

SMU2: DC Voltage bias applied to the drain, through the RBT.

D. Drain response

This waveform shows the DC bias and the resulting response to the gate pulse.

Note that the drain is DC biased and the pulse in this waveform is the result of

the gate pulse. There is no pulse applied to the drain, rather the pulse shown is the response of the drain current flowing.

E. Drain voltage response measured by oscilloscope (4200-SCP2 Channel 2)

The response of the drain is due to the gate pulse turning on the transistor, allowing the drain current to flow. This drain current (I_d) flows through the 50 Ω input impedance of the scope, which acts as a current sense resistor (R_{SENSE}), resulting in the voltage drop in the waveform (V_{SENSE}). This voltage response is negative due to the direction of current flow through the 50 Ω resistor and the fact that the scope is ground-referenced. Note that this waveform is AC shifted to 0 V, due to the coupling capacitor in the RBT.

3.4 Ultra-Fast Switching (UFS) Measurement Methodology

3.4.1 Experimental Setup of UFS

An Ultra-Fast Switching (UFS) method based on the commercial pulsed I - V set-up targeted at minimizing self-heating of the transistor during I - V measurement will be demonstrated first. Signal integrity at extremely short pulse width is guaranteed. The main advantages of UFS method are that it leverages on customary equipment and yet is able to achieve sub-100 ns measurement speed, the fastest reported to-date for a wafer-level set-up. Later in this chapter, an unified approach for consistent extraction of the threshold-voltage shift ($|\Delta V_{\text{th}}|$) by linear drain current ($I_{\text{d,lin}}$) measurement will be presented.

Fig. 3-6 demonstrates the physical setup of Ultra-Fast Switching (UFS) method based on the commercial pulsed I - V set-up. As mentioned earlier, the gate bias tee acts as a couple for both AC and DC voltage. The gate terminal of the Device Under Test (DUT) is connected via a gate bias tee and the DC input is sourced from a SMU; while the AC signal comes from a pulse generator, which has the capability of achieving pulse width down to 40 ns. Besides, the drain terminal of DUT is connected to a drain bias tee with DC connected to a SMU as can be seen in the diagram below (Fig. 3-6). Unlike the gate bias tee, the AC output of the drain bias tee is connected to an oscilloscope. This is done so as to capture any abrupt change in the drain current on the oscilloscope.

Figure 3-6: Schematic diagram of the UFS measurement set-up. [134]

3.4.2 How does UFS work: Principle of UFS Measurement

During UFS measurement, the gate terminal is pulsed to the measurement voltage within a short period of time and the abrupt change in the drain current is sampled within this duration by a high speed oscilloscope. This is generally the concept of Pulse I_d - V_g (similar to a pre-stress phase).

During the initial pre-stress phase, the fresh I_d - V_g curve is extracted to be the reference for the subsequent phases. In this example, the DC voltage, V_g^{DC} is kept constant at 0 V. The measurement is taken whereby a short pulse of 100 ns with the amplitude of the measurement voltage from the pulse generator is injected into the gate signal. For example, if the drain current were to be measured at $V_g^{\text{AC}} = -0.5$ V, a negative pulse with amplitude of 0.5 V would be injected. As a result, the overall voltage will be pulsed to the measurement voltage since $V_g^{\text{DC}} = 0$ V. During the gate pulse transition after a given stress interval $t = t_s$, the drain current denoted as I_d^{AC} , will be measured by a high-speed oscilloscope whereby the current-to-voltage conversion takes place automatically via the oscilloscope $50\ \Omega$ internal resistance, R_{in} . Based on the formula ($I_d^{\text{AC}} = V_g^{\text{AC}} / R_{\text{in}}$), I_d^{AC} can be back-calculated. As each gate pulse is pulsed to a defined measurement voltage, only one drain measurement can be measured. Therefore, multiple gate pulses are required to measure the whole I_d - V_g sweep.

When the DUT (p-MOSFET) is continuously stressed with a constant negative DC gate voltage denoted as V_{stress} during stress phase, this corresponds to a

constant DC drain current, I_d^{DC} which is sampled by the SMU at drain bias tee since DUT is in strong inversion. At selected time intervals, measurement is achieved by injecting a positive voltage pulse, V_g^{AC} into the gate bias-tee, which brings the overall gate voltage at the output of gate bias tee down to a measurement voltage magnitude ($V_{meas} = V_g^{DC} + V_g^{AC}$). The AC component of the drain current, I_d^{AC} (arising from V_g^{AC}) is measured using a high-speed oscilloscope whereby the current-to-voltage conversion takes place automatically via the oscilloscope 50 Ω internal resistance. This resistance-based current-to-voltage conversion eliminates the bandwidth constraint of amplifier-based methods [132]- [133], thus allowing very fast pulse transition time of a few nanoseconds. The drain current at the specific measurement voltage is calculated by taking $I_d = I_d^{DC} + I_d^{AC}$.

During relaxation, the DC gate voltage is set to relaxation voltage, V_g^{relax} . It can be set to 0 V or +1/ +2 V according to individual purposes. The gate pulse used for UFS measurement is set at pulse width of 100 ns and is periodically generated at an interval of 100 μs , which represent 0.01% of the overall stress cycle during measurement. Hence, an accurate $|\Delta V_{th}|$ measurement can be obtained as minimum stress interruption is ensured in UFS measurement methodology to achieve least measurement delay.

Fig. 3-7 shows the schematic of gate voltage in NBTI tests with UFS setup. During measurement, drain voltage is biased at -0.1 V and during NBTI stress,

it is grounded. The device degradation is monitored according to user defined time array after applying DC voltage stress. Subsequent pulses of $\pm\Delta$ ($\Delta = 50$ mV) difference in amplitude compared to the first are added. By pulsing the voltage from the stress level to the measurement level in a voltage step of $\pm\Delta$ 50 mV (as illustrated in Fig. 3-7), a complete I_d - V_g curve could be obtained. For example, at a stress level of -2.5 V, a pulse magnitude of + 2 V would be applied in order to capture the I_d measurement at $V_g = -0.5$ V. This pulsing is repeated with different amplitudes until the I_d measurement for the entire V_g (ranging from 0 till -1 V) is completed within ~ 7 s. With the I_d - V_g curves collected during NBTI experiments, the ΔV_{th} is obtained using the constant current method. It should be mentioned that the fresh measurement is taken at $V_g = -1$ V instead of $V_g = 0$ V to eliminate measurement errors caused by waveform overshoot and inconsistency between the SMU and the Oscilloscope. When DC input voltage has a fast transition, unexpected voltage spikes may be generated by the Remote Bias Tee (i.e. high frequency voltage) and thus degrade the testing device during measurement. Therefore, the fast transition with small voltage variation ($V_g = -1$ V $\rightarrow V_G^s = -2.6$ V, $\Delta V_G = -1.6$ V) has lower probability of causing the testing device to degrade as compared to the fast transition with large voltage variation ($V_g = 0$ V $\rightarrow V_G^s = -2.6$ V, $\Delta V_G = -2.6$ V). However, the V_g used for fresh measurement can be varied according to experimental needs (provided that the chosen V_g does not generate significant NBTI degradation).

Figure 3-7: Schematic shows the gate voltage during NBTI tests with UFS setup. Drain voltage is biased at -0.1 V during measurement and grounded during NBTI stress. A fresh measurement is taken at $V_g = -1$ V and device degradation is monitored according to user defined time array after applying DC voltage stress. Subsequent pulses of $\pm\Delta$ ($\Delta = 50$ mV) difference in amplitude compared to the first are carried out to bring the voltage level from the stress level to the measurement level to obtain the I_d - V_g [134], [135].

3.4.3 How accurate is UFS: Validation of UFS Measurement

In order to validate UFS measurement, it is necessary to ensure that the hardware used in UFS is able to perform up to expectations. Though UFS is able to achieve a pulse width of 40 ns, a pulse width of 100 ns is usually chosen to ensure better voltage and current stability. The waveforms of gate voltage V_g^{AC} and drain current I_d^{AC} , which are captured by oscilloscope during pulsing are shown in Fig. 3-8. It can be seen that the gate voltage blows up from V_g^{DC} to measurement voltage (2.6 V) in a very short time (rising/ falling time of 10 ns) with a pulse width of 100 ns. And, as the gate voltage blows up from V_g^{DC} to V_g^{meas} in a very short time (which is in order of ns), the drain current is observed to rise even slower due to the S/ D capacitance. Therefore, the oscillation of V_g

may result in a noisy $|\Delta V_{th}|$ versus time. However, by choosing a suitable pulse width and measurement window carefully, this problem could be resolved. Data in between 60% and 80% of the pulse width is averaged. It gives the values of V_g^{AC} and I_d^{AC} . Due to the damping effect and voltage overshoot, the best choice of pulse width is found to be in between 70 ns and 100 ns. The average of several pulses captured is taken to increase the accuracy. It should be noted that measurement is carried out at quasi steady-state, i.e. during the “flat” portion of the gate voltage and drain current waveforms in our approach. As a result, the inherent delay between the two waveforms is not critical. This helps to overcome the shortcoming of the ramped-voltage method [132] where synchronized gate voltage and drain current waveforms are crucial.

Apart, it is clearly discussed in Fig. 3-9 that nominal gate capacitance has no effect on the signal integrity. Gate to body/ Source/ Drain capacitance ($C_{gb}/ C_{gs}/ C_{gd}$) of DUT is not sufficient to distort waveform of the gate voltage pulse. The waveforms on the 1.5 pF capacitor, 0.018 pF capacitor, and open circuit are observed to merge together. One point to highlight here is that the DUTs used in most of the research have < 1.5 pF. The large area capacitors used are transistor-like capacitors, which have narrow Source/ Drain to supply excessive minority carriers to the channel. As can be seen in

Fig. 3-9, there is no apparent impact noticed on the waveform stabilization within the first 50 ns for gate capacitance < 1.5 pF (1.5 pF is equivalent to ~ 80 of our DUTs connected in parallel). This outlines the possibility of using this method for parallel

NBTI testing with a common pulse source (albeit a multi-channel OSC would be needed in this case).

Figure 3-8: Waveforms of gate voltage pulse, V_g^{AC} and drain current, I_d^{AC} . The gate voltage pulse has an amplitude of 2.6 V, pulse width of 100 ns, and with a rising/falling time of 10 ns. Data in between 60% and 80% of the pulse width window is averaged. It gives the values of V_g^{AC} and I_d^{AC} . [134]

Hence, to verify the measurement system further, I_d - V_g measurements were conducted on a similar unstressed device by both conventional DC measurements and UFS. The results obtained by both UFS and conventional DC in linear and sub-threshold regimes are shown in Fig. 3-10. It is clearly shown that the I_d - V_g measurement obtained by UFS is in well agreement with the DC in the linear regime. However, in the sub-threshold regime, the agreement lasts up to $\sim 5\mu\text{A}$. Unlike high resolution SMU which has a resolution down to $\sim\text{pA}$ range, the physical connection of the drain terminal is connected via drain bias tee which has caused the resolution limit to be degraded to $\sim 5\mu\text{A}$. However, this does not pose a problem as

the sub-threshold current in advanced technology like 65 nm is expected to increase due to the scaling of gate oxide and channel length. Therefore, this

Figure 3-9: Waveforms of gate voltage v_g with various capacitors connected. The v_g waveforms with probing on 1.5 pF capacitor, 0.018 pF capacitor (DUT), and open circuit merge together. No impact is apparent up to 1.5 pF, which is equivalent to ~ 80 devices in parallel. Larger capacitor could result in waveform distortion. [134]

Figure 3-10: Drain current, $|I_d|$ measured using both UFS and DC methods by pulsing/ sweeping the gate voltage from 0 to -1 V. Drain voltage is kept at -0.1 V. (a) Sub-threshold regime, (b) Linear regime. [136]

Figure 3-11: Comparison of $|\Delta V_{th}|$ measured by UFS and conventional DC. (a) Plotted on linear scale to highlight the recovery effect during stress measurement. This recovery effect seems negligible during relaxation measurement (b) Plotted on log-log scale to highlight the power law exponent which is critical for long term extrapolation. Constant current method is used to extract $|\Delta V_{th}|$ from I_d - V_g curve obtained at various time intervals. Devices used were stressed for a time period of 50,000 s and relaxed for 1000 s at $V_g = -2.4$ V / 0 V at 100° C. [136]

method can also be utilized in NBTI characterization for advanced technological nodes. The final step of validation is to compare NBTI characterization by UFS method in comparison with conventional DC method. Two identical devices were stressed at similar conditions to highlight the difference caused by measurement methodology. Though the devices had been stressed for a similar period of time, it can be clearly observed from Fig. 3-11 that the magnitude of $|\Delta V_{th}|$ captured by DC measurement is lower as compared to UFS measurement. This is expected as DC measurement suffers from the effect of recovery due to SMS measurement sequence as discussed earlier. Therefore, by using UFS measurement, the impact of recovery is shown to be greatly minimized, resulting in a smaller power law exponent of ~ 0.11 as compared to DC of ~ 0.19 .

3.5 Electrostatic Discharge (ESD): Very Fast Transmission Line Pulse (VFTLP)

Apart from Ultra-Fast Switching (UFS) measurement technique, the Very Fast Transmission Line Pulse (VFTLP) is another measurement methodology which was used in this project to study the interaction of dynamic NBTI with Electrostatic Discharge (ESD). As this method was not used as intensively as the UFS technique in this project, thus, only a brief description on the VFTLP will be done in this section.

In general, there are three different calibrations to be performed before starting the ESD experiments, Scope Calibration (SPC), Short Timing Calibration (STC) and Parallel Poll Configure (PPC) Calibration. These are done to ensure the accuracy and precision of the results obtained. Scope calibration (SPC) is done every time when the scope is powered up, and has sufficiently warmed up and stabilized. Usually, the oscilloscope will be turned on for three hours before starting the SPC. The second calibration, short timing calibration, is done to compute the timing data needed to extract incident and reflected pulses from the signals acquired by the oscilloscope. Lastly, PCC calibration is done every time when there are any changes in the setup (cables, probes or connection). It is needed by the program to perform some calculations on the system loss and distortions.

Figure 3-12: (Left) Barth 4012 VFTLP+ tester (Right) Simplified diagram for pulse testing system. [137]

The ESD measurements were done using Barth 4012 VFTLP+ (Very Fast Transmission Line Pulse) tester which is able to simulate a CDM event on wafer level devices. The system has the capability of simulating pulse width of 1, 2, 5 and 10 ns. The maximum pulse voltage ranges from -500 V to 500 V. There are two microwave probes located at the probe station. One is positively-charged while the other is negatively-charged. The spacing of the needles is fixed (i.e. 100, 125, 175, 200 and 250 μm) and they provide low resistance connections to the bond pads with minimal parasitic resistance. An approximately 10 m long 50 Ω coaxial cable serves as the pulse source. The length of the pulse depends on the length of the coaxial cable. The charged cable is connected to the device under test (DUT). Voltage and current probes on the output end are connected to a high speed oscilloscope to measure the current and voltage of the pulses. A

VLTLTLP measurement follows a specific sequence. To create the VFTLP pulse, the transmission line is charged to a voltage. The pulse passes through the coax cable and passes down to the DUT, reflects off the DUT and travels back toward the pulse source transmission line. The oscilloscope captures the incident and reflected signals. DUT experiences the sum of the incident and reflected pulses and its properties can be determined from the properties of the incident and reflected pulses. A measurement window is defined during the time period on the oscilloscope when the incident and reflected pulses overlap in order to obtain a current/ voltage pair from the pulse measurements (as shown in Fig. 3-13). To obtain the full IV curve, this process is repeated with varies charging voltages for the pulse source transmission line, usually starting at low charging voltages before proceeding on to higher voltages [210].

During the ESD experiments, the pulse width was set to 1 ns while the rise time used was 0.1 ns at room temperature. The initial voltage was specified to be 0.5 V, followed by a step voltage of 0.1 V. The leakage current measurement was performed at 0.5 V (DC) to gauge the leakage current across the gate oxide after each applied pulses. The voltage stress was increased (in a step voltage of 0.1 V) until it reached “failure”. In order to facilitate our discussion in the next chapter, “failure” is defined when there is an apparent increase of at least 4-5 orders of magnitude observed in the leakage current evolution.

Figure 3-13: (Left) VTFLP pulse followed by leakage current measurement (Right) Voltage and current waveform where the value is averaged up between 25% and 75% of the pulse duration. [137]

Fig. 3-13 above demonstrates how the I/V curve of a device was generated. After every pulsing, a leakage measurement was carried out to trace the leakage level of the DUT. By carefully selecting the pulse width and measurement window, noisy measurement data (caused by voltage overshoot or damping effect) could be avoided and a more stable measurement results could be obtained. Data between 25% and 75% (of the pulse duration) of the DUT voltage/ current versus time waveform (as illustrated in Fig. 3-13) would be averaged to generate a single current-voltage point. This was done for every waveform captured which corresponded to the pulses applied in a step voltage of 0.5 V until the device showed a significant increase in the leakage current evolution.

Thus, the I/V curve consists of a series of single current-voltage points. By doing so, the accuracy of the measurement results could be enhanced.

3.6 Chapter Summary

The shortcomings of conventional slow DC measurement and the impact of recovery effect on NBTI characterization have been specially highlighted in this chapter. The key characterization techniques for NBTI and ESD were summarized. The Ultra-Fast Switching (UFS) method was discussed in details, starting from its hardware setup till the system's verification.

CHAPTER 4: THE RECOVERY NATURE OF TRANSIENT “SWITCHING” HOLE-TRAPS (R COMPONENT) OBSERVED DURING DYNAMIC NEGATIVE-BIAS TEMPERATURE INSTABILITY (NBTI)

4.1 Introduction

As mentioned before in the previous few chapters, the most widely cited explanation for NBTI is none other than the Reaction-Diffusion (R-D) model [138], [139]. The essence of the R-D model may be summarized as follows. First of all, dangling Si bonds (or P_b centers) are formed and hydrogen is liberated at the Si/SiO₂ interface by an electrochemical reaction involving Si-H bonds and holes (from the inversion layer). Then, the released hydrogen will diffuse away from the interface. Ultimately, this diffusion process controls the net increase of interface trap density with time, since hydrogen that remains at the interface would repassivate the dangling Si bonds as to anneal out the interface traps. This framework of the R-D model encountered some modifications in recent years to incorporate dispersive transport behavior in the amorphous gate oxide [140], [141]. This move was aimed at enhancing the flexibility of the basic model to cater to wide variations in the state-of-the-art gate oxide technology. Nevertheless, the basic premise that NBTI is driven by a hydrogen-transport mechanism remains unchanged. On the other hand, there is another camp of thought which states that, on top of the R-D model, there exists another mechanism in NBTI. With the occurrence of the ultra-fast

measurements, the presence of hole-trapping is detected and reported as another NBTI mechanism, which is responsible for the fast “degradation transient” arising from the positive charging of oxide traps [18], [142]. The hole-trapping mechanism is found to be consistent with (i) the initial fast recovery, explained by spontaneous hole detrapping and interface traps passivation by interfacial hydrogen (the latter remains a theoretical proposition); (ii) the subsequent slow passivation of interface traps, rate-limited by back-diffusion hydrogen [139].

However, as the gate oxide gets thinner and thinner now, it is also universally accepted that there are two main components contributing to NBTI degradation, the (i) relatively permanent (P) component and (ii) recoverable (R) component. There has been considerable attention on the R component as its transient nature could pose significant challenges to both device and circuit reliability assessment and modeling. Recently, it is shown that the R component remains constant, regardless of the number of times the p-MOSFET is stressed and relaxed under typical NBTI oxide fields (~ 7 MV/cm) and temperature ($\sim 100^\circ\text{C}$) [19], [20], [143]. Some ascribe the “non-RD” characteristic of R to the activation of “switching” oxide traps, suggesting that it is an extrinsic effect. In this work, we reveal an interesting effect of a high oxide field stress (>11 MV/cm), applied prior to DNBTI, on the subsequent R component. A prior high oxide field stress is shown to reduce R . Most importantly, the reduction becomes more severe at a later stage when bulk (oxide) trap generation is relatively significant, as evident by a substantial increase in the Stress-Induced

Leakage Current (SILC). This observation does not support the notion that R is related to just a simple hole-trapping/ detrapping mechanism.

4.2 “Cyclic” Nature of Dynamic NBTI

It should be mentioned that almost all NBTI studies reported to-date have focused either only on the stress data or on a limited amount of stress and recovery data (typically, only one recovery cycle is measured and analyzed following electrical stressing). Before proceeding further, there is a need to clarify some terms which will be used frequently in this chapter in order to facilitate the discussion better. Fig. 4-1 depicts the typical evolution of $|\Delta V_t|$ across the stress and recovery (S&R) cycle, showing apparent fast and slow recovery phases. The $|\Delta V_t|$ at the end of the stress cycle is termed as $|\Delta V_t|^{\text{eos}}$ while the $|\Delta V_t|$ at the end of recovery cycle is termed as $|\Delta V_t|^{\text{eor}}$. The difference between the $|\Delta V_t|^{\text{eos}}$ of cycle 2 with $|\Delta V_t|^{\text{eor}}$ of cycle 1 is the $|\Delta V_t|$ during stress, $|\Delta V_t|^{\text{s}}$; similarly, the difference between the $|\Delta V_t|^{\text{eos}}$ of cycle 2 with $|\Delta V_t|^{\text{eor}}$ of cycle 2 itself will result in $|\Delta V_t|$ during recovery, $|\Delta V_t|^{\text{r}}$, which is also known as the R component. In general, dynamic NBTI consists of more than 1 stress and relax cycle. In general, these definitions also apply to the time period after cycle 1.

Figure 4-1: Evolution of threshold voltage shift, $|\Delta V_t|$ during typical stress and recovery cycles of a dynamic NBTI experiment.

Figure 4-2: Amount of change in $|\Delta V_t|$ during stress and recovery, $|\Delta V_t|^s$ and $|\Delta V_t|^r$, respectively, as a function of the number of stress and recovery (SR) cycles. [20], [160], [161]

As shown in Fig. 4-2 (a), it is interesting to note that although $|\Delta V_t|^s > |\Delta V_t|^r$ in the initial first few cycles, the former soon approaches the latter as dynamic stressing continues, i.e. in the later stage of dynamic stress, the amount of $|\Delta V_t|$ increased during stress cycle is almost entirely recovered in the ensuing relaxation cycle. And, the amount of $|\Delta V_t|$ recovery per cycle, R is observed to remain constant over many SR cycles. At this juncture, it is important to stress that analysis based on a limited number of stress/ recovery cycles (especially the first few ones) would mislead one into concluding that the result conforms to the R-D model, on the basis that $|\Delta V_t|^s > |\Delta V_t|^r$ which appears to suggest a self-limiting recovery behavior. But, the experimental data from the subsequent SR cycles which shows that $|\Delta V_t|^s$ almost equal to $|\Delta V_t|^r$, in conjunction with a constant $|\Delta V_t|^r$, right from the first SR cycle, clearly indicates that the conclusion is incorrect. The constant $|\Delta V_t|^r$ could not be explained by the hydrogen-transport model, which predicts that $|\Delta V_t|^r$ would decrease progressively with SR “cycling” (filled symbol; Fig. 4-2 (a)) [144]. This “non-RD” feature is also evident in Fig. 4-2 (b), in which precise reproduction of the $|\Delta V_t|^{\text{cor}}$ characteristic (solid line) can be achieved by subtracting $|\Delta V_t|^r$ or R of the first cycle from $|\Delta V_t|^{\text{eos}}$.

Figure 4-3: Evolution of $|\Delta V_t|$ shift during stress and recovery cycles showing highly repeatable characteristics over many cycles. Symbols denote averaged curves. [161]

In fact, apart from showing a constant nature, the R component is also found to exhibit a cyclic behavior as mentioned earlier. Fig. 4-3 shows highly repeatable shift of $|\Delta V_t|$ during stress and recovery over many SR cycles (thin lines). Although the time dependence of $|\Delta V_t|$ shift during stress and recovery are different, the values at the end of the stress and recovery period are strikingly similar for all SR cycles. This observation seems to imply that for a given time window, dynamic NBTI is always governed by the *same* group of “defects” charged/ discharged repeatedly [18], [20]. At this point of time, the cyclic behavior strongly suggests the role of “switching” hole- traps. Studies based upon electron spin resonance measurement confirmed that these “switching” hole-traps are related to oxygen vacancy defects in the gate dielectric [145], [146].

4.3 The Effect of High Oxide Field Stress on the R Component of Dynamic NBTI: Correlation between Bulk (Oxide) Trap Generation and Negative-Bias Temperature Instability (NBTI)

In addition to the generation of Si/ SiO₂ interface states (ΔN_{it}), the generation of oxide traps (ΔN_{ot}) has been observed under Negative-Bias Temperature (NBT) stress [147]-[149]. Views on the underlying mechanism of ΔN_{ot} are, however, divided. Some studies [147]- [148] ascribe ΔN_{ot} to the interaction between the SiO₂ network and the hydrogen species [150] which come from the dissociation of Si-H bonds [149]. Others [149] ascribe ΔN_{ot} to the breaking of Si-O bonds by the relatively high oxide field used by some NBT stresses. This second view point regards ΔN_{ot} as a separate high-field effect uncorrelated with NBT instability (NBTI). In this chapter, we present a new observation on the relationship between ΔN_{ot} and NBTI. Evidence which shows that substantial interface degradation under Negative-Bias temperature (NBT) stressing does not result in any apparent oxide trap generation is provided. The link between NBT instability and oxide trap generation is actually found in the recoverable hole-trapping component (R) of the former. When R is constant, independent of the number of stress/ relaxation cycles, no apparent oxide trap generation is observed in spite of nonnegligible interface degradation. However, when oxide trap generation occurs, a correlated *decrease* of R is observed. Analysis shows that the generated oxide traps are due to a portion of the trapped-holes being transformed into a more permanent form. A possible explanation based on the oxygen vacancy defect would be given in the later part of this chapter.

4.3.1 Experimental Details

Test devices used for experiments were p^+ polysilicon gate P-MOSFETs with 1.8 nm oxynitride gate prepared via decoupled plasma nitridation. The 1.8 nm thick SiO_2 was first prepared by rapid thermal oxidation. The SiO_2 films were then nitrided in plasma source, followed by a high temperature O_2 annealing where the nitrogen would flow downstream from the SiO_2 surface. Results reported in this section were obtained on devices with a drawn channel width and length of 10 μm and 0.1 μm respectively, unless stated otherwise. NBTI test was carried out at a gate stress voltage of -1.8 V (oxide field $\sim 7.7\text{ MV/cm}$) and at a temperature of 100° C . At specific intervals, I_d - V_g curve was measured using an ultrafast switching method [134]. The short delay of $\sim 60\text{ ns}$ not only minimizes recovery significantly, it suppresses cumulative recovery during I_d - V_g measurement [151]. Device degradation was measured in terms of $|\Delta V_t|$, extracted at a constant drain current of $\sim 250\text{ uA}$.

4.3.2 Results and Discussion

Fig. 4-4 illustrates the effect of the high oxide field stress on the P (mainly ascribed to N_{it}) and R (mainly ascribed to N_{ot}) component. The amount of increase in P is denoted by arrow A. In Fig. 4-5, it can be seen that the effect of high oxide field stress on P is relatively significant in the initial stage. However, it decreases at the later stage, as reflected on the subsequent dynamic NBTI cycles starting from the second application of the positive V_g stress.

Figure 4-4: In this experiment, alternate dynamic NBTI (DNBTI) and positive V_g stress (+2.9 V; 5 s) were applied to the device under test. Dynamic NBTI always consisted of three stress and recovery (SR) cycles (−1.8 V stress; 0 V recovery; stress and recovery intervals were 1000 s each) and was applied first. This was followed by the positive V_g stress and then dynamic NBTI and so on.

On the other hand, it is interesting to note that, on the contrary, the effect of high field stress on the R component is relatively small initially, but it grows to become more significant at the later stage as depicted by the decreasing red line. Most importantly, the reduction in R occurs at the later stage when oxide trap generation becomes very significant, as can be seen by the substantial increase in the SILC as positive V_g stress progresses, shown in Fig. 4-7.

Figure 4-5: $|\Delta V_t|$ at the end of each NBTI stress and recovery cycle, $|\Delta V_t|^{eos}$ and $|\Delta V_t|^{eor}$ respectively, and the amount of $|\Delta V_t|$ recovery per cycle, $|\Delta V_t|^f$ are shown as a function of the number of SR cycles. The thick solid line is obtained by subtracting the constant $|\Delta V_t|^f$ of the first three recovery cycles from $|\Delta V_t|^{eos}$. The purple line denotes the case when there is no decrease in the R component.

These distinct effects corroborate an earlier inference, based on temperature dependence study, of that the defect nature of R and P are likely to be different. As discussed earlier, the cyclic behaviour of R is likely to be due to the repetitive trapping and detrapping of the oxide vacancy defects. Hence, one would expect to observe an increase in the cyclic $|\Delta V_t|^f$ or R in the ensuing dynamic NBTI cycles as more oxygen vacancy defects have been generated by applying an alternate positive high field stress repetitively. However, a progressive decrease in R is observed in the experimental results instead. This suggests that the high oxide field applied has caused an impact on the recoverable nature of R , since a higher density of hole-traps did not correspond to a larger cyclic $|\Delta V_t|^f$. According to the experimental data, the decrease in R is

found to be $\sim 30.6\%$, after 60 cycles of $+2.9\text{ V}$ interruptions in between the dynamic NBTI cycles. It is, thus, suspected that a fraction of R has experienced a transformation from its recoverable nature into a more permanent kind of defect.

To further investigate the nature of the cyclic $|\Delta V_t|^r$ or R (ΔN_{ot}), as shown in Fig 4-6, all devices were first subjected to a cycle of dynamic NBT stress (DNBTS) comprising a stress phase at a gate voltage $V_g = -1.8\text{ V}$ ($\sim 8.5\text{ MV/cm}$ oxide field) and an ensuing relaxation phase at $V_g = 0\text{ V}$. The stress and relaxation phases each lasted $1 \times 10^3\text{ s}$. At specific intervals, the linear transfer curve was measured via an ultrafast switching method [134], and the threshold voltage shift (ΔV_t) was extracted by the constant subthreshold drain current method. To examine the correlation between ΔN_{ot} and NBTI, some devices were then subjected to a constant voltage stress (CVS) at a *larger* V_g magnitude for a given time. No measurement was made during this time. The DNBTS was resumed to examine the impact of the prior CVS on the $|\Delta V_t|$ evolution. This CVS–DNBTS sequence was repeated numerous times, and V_g transitions between the two were made on the fly. In a separate experiment, DNBTS was replaced by gate current I_g measurement to gauge the extent of ΔN_{ot} increase after CVS. On other devices, the CVS was skipped, and only DNBTS was repeated. For all experiments, the temperature was set at 100° C .

Figure 4-6: $|\Delta V_t|$ recovery per cycle or R as a function of the number of DNBTS or CVS-DNBTS cycles. The inset shows the evolution of $|\Delta V_t|$ in a typical DNBTS cycle. CVS: $V_g = 2.7$ V and $time = 50$ s.

The evolution of the R , the $|\Delta V_t|$ recovered in the relaxation phase (inset of Fig. 4-6), is shown as a function of the number of DNBTS or CVS-DNBTS cycles. For the case of DNBTS only, R is constant throughout in accordance with previous observations [20], [152]. As discussed in detail in [20] and [152], annealing of interface states by the back diffusion of hydrogen [190] could not explain the constant R or V_t recovery. And, as mentioned earlier, the constant R implies that NBTI recovery is always due to the relaxation of the same group of hole-traps charged positively during stress. This, also, is corroborated by the results from time-dependent defect spectroscopy [191]

Figure 4-7: Corresponding gate leakage current is measured after 20 DNBTS or 19 CVS–DNBTS cycles. Comparison is made between devices with and without CVS.

showing very consistent time constants of individual hole-trapping/ hole-detrapping events in small-area devices subjected repeatedly to NBT stress and relaxation. This suggests that it is always the same oxide traps that respond under a given stress condition. The fact that **no** new oxide traps are created is supported by the I_g measurement result in Fig. 4-7. Since the I_g was measured over a range of 3 V ($-1.5 < V_g < 1.5$), a considerable part of the oxide bandgap, both above and below the Si conduction and valence band edges, was scanned. The absence of any I_g increase after 20 DNBTS cycles or a cumulative stress time of 2×10^4 s strongly denies the existence of any new permanent oxide traps. We infer that the defects responsible for the relatively permanent V_t shift of ~ 50 mV [open circle; Fig. 4-10] must be situated not in the oxide bulk but very close to or at the SiON/ Si interface. Since this study does not give any

direct evidence on the nature of these defects, it is inconclusive whether they are associated with the Si–H bond dissociation mechanism that is widely discussed in the literature. Nevertheless, the result shows clearly that a substantial part of the interface degradation under NBT stress does not correlate with oxide trap generation.

While a constant R is consistently observed on our devices for the stress conditions studied, it is not always the case for other devices or stress conditions [153]- [155]. Gao *et al.* [153] reported a decrease in the R of the HfO_2 gate p-MOSFET, whereas those of the HfSiON and SiON counterparts were constant under similar stress conditions. Grasser *et al.* [154] also observed a decrease in the R of the nonnitrided SiO_2 gate p- MOSFET at higher temperatures ($\sim 200^\circ\text{C}$). A TDDS study on a SiON device at elevated temperatures revealed a halt in the hole emission event at a given defect for an extended period [155]. In the following, we show that a similar decrease of R also occurs for the SiON gate p-MOSFET stressed under 1) a *larger* oxide field or 2) an extended period (without interruptions) at lower field. For the case of CVS–DNBTS as shown in Fig. 4-7, a substantial increase in I_g is evident after 20 cycles. Since no I_g increase is observed for the case of DNBTS only, the observed I_g increase or oxide trap generation is due to the CVS. This observation tends to show that the oxide trap generation observed by some studies [147]- [148] is the effect of a high oxide field and is not related to NBTI [149]. However, the *reduction* in R evident in Fig. 4-6 warrants further examination.

Figure 4-8: (a) Fractional increase in the gate tunneling current $\Delta I_g / I_{go}$ (at $V_g = 1.5 \text{ V}$) or Stress-Induced Leakage Current (SILC) is observed to “track” the decrease in R closely. (b) Excellent linear correlation between $\Delta I_g / I_{go}$ (extracted at various voltages) and ΔR is observed.

Fig. 4-8 (a) shows that the decrease in R tracks the fractional increase in I_g closely; the two exhibit an excellent linear correlation (Fig. 4-8 (b)). This means that, with the occurrence of oxide trap generation by CVS, trapped-hole relaxation in the subsequent DNBTS cycle would be reduced. A more substantial decrease in R is noticed with a larger V_g of CVS as seen in Fig. 4-9. It is elaborated further in Fig. 4-10 that increasing magnitude of positive V_g from 2.3 V to 2.9 V results in a greater reduction in R . One point to take note of is, the stress interval for $V_g = 2.3$ V, 2.4 V and 2.5 V remains at 1000 s, but it is soon decreased to 50 s and 5 s respectively for $V_g = 2.7$ V and 2.9 V. This is done to avoid gate oxide breakdown because it is almost impossible to stress the gate dielectric at an extremely high stress for a long duration.

Figure 4-9: With a larger V_g of CVS (in comparison to Fig. 4-6), a more substantial decrease of R is noticed.

Figure 4-10: The reduction of $|\Delta V_t|^f$ (normalized to that of the first recovery cycle) is shown to be sensitive to the increasing oxide field stress. (Inset) $|\Delta V_t|^f$ decreases as $+V_g$ is increased; solid line is an eye guide only. For $V_g = 2.3$ to 2.5 V, the stress interval is 1000 s. Data are extracted at the 60th SR cycle (or after application of 20 positive V_g stress cycles).

Fig. 4-11 compares and studies the evolution of $|\Delta V_t|^{\text{eos}}$ and $|\Delta V_t|^{\text{eor}}$, the respective $|\Delta V_t|$ at the end of stress and relaxation phases, for CVS–DNBTS and DNBTS as a function of the number of cycles. Interestingly, when a more significant R decrease is observed in the late stage of the CVS–DNBTS (Fig. 4-9) the $|\Delta V_t|^{\text{eos}}$ is seen to increase at a rate comparable to that of the DNBTS. This suggests that, in both cases, the total positive trapped charge, $|\Delta V_t|^{\text{eos}}$ which probes both oxide and interface trapped charges, is increasing at a similar rate in the late stage.

Figure 4-11: Evolution of $|\Delta V_t|$ at the end of the stress cycle ($|\Delta V_t|^{eos}$) and at the end of the relaxation cycle ($|\Delta V_t|^{eor}$) as a function of the number of DNBTS or CVS-DNBTS cycles, for the same devices in Fig. 4-9.

However, the $|\Delta V_t|^{eor}$ of the CVS–DNBTS is observed to rise faster as compared to $|\Delta V_t|^{eos}$. This observation further supports the hypothesis that, in the DNBTS cycle following the CVS, the proportion of more permanent trapped holes is increased, i.e., the prior CVS had transformed a fraction of the recoverable trapped holes into a more permanent form. It also means that R can no longer recover spontaneously upon the removal of stress during recovery. The correlated increase of I_g as seen in Fig. 4-8 implies that the underlying oxide/bulk traps also stem from this transformation mechanism. On the other hand, $|\Delta V_t|^{eos}$ and $|\Delta V_t|^{eor}$ for the case of DNBTS both increase at a similar rate, yielding a constant R , in the absence of oxide trap generation as denoted in Fig. 4-7.

Figure 4-12: Longer CVS time is needed to produce an apparent reduction in R at a reduced V_g of CVS.

As can be seen in Fig. 4-12, apparent reduction of R could only be observed at a much longer CVS time when a smaller V_g of CVS is applied. This result indicates that transformation of the trapped holes into permanent oxide traps could occur under *dc* NBT stress after a sufficiently long time. However, under *ac* stress, this transformation is inhibited by a nearly complete relaxation of the trapped holes (constant R ; Fig. 4-6).

It should be mentioned that the first few applications of CVS always produce an evident “jump” in the $|\Delta V_t|^{\text{eor}}$, relative to that of the first DNBTS cycle (refer to Fig. 4-11). The increase is often more significant than the increase of I_g or the decrease in R . As also shown earlier in Fig. 4-8(a), both ΔI_g and ΔR are

approximately zero, whereas the $|\Delta V_t|^{\text{eor}}$ at the second DBNTS cycle (i.e., after the first CVS) is increased by ~ 20 mV (based on calculation, result's not shown here). The latter corresponds to a nonnegligible effective trap density of $2.5 \times 10^{11} \text{ cm}^{-2}$. A similar observation applies to the case of the 3.1 V CVS depicted in Fig. 4-11; $|\Delta V_t|^{\text{eor}}$ is increased by 50 mV, whereas the R is reduced by only 10 mV after the first CVS. The discrepancy again requires us to presume that the defects responsible for the $|\Delta V_t|^{\text{eor}}$ increase are situated at the SiON/ Si interface, indicating that part of the interface degradation is not correlated with oxide trap generation.

The oxygen vacancy defect or the E' center [156] is a major source of trapped-hole sites in the gate oxide. A recent work employing on-the-fly ESR measurement showed that NBTI recovery was correlated to the E' center [157]. On this basis, we provide a possible explanation for the transformation of trapped holes into more permanent bulk traps, notwithstanding that other defect types may also account for the observation. *Ab-initio* simulation studies have shown that the E'_δ center accounts for more than 90% of the total E' centers in SiO_2 [158]. As illustrated earlier in Chapter 2 (Fig. 2-11), when a hole is captured at the E'_δ center, the change in the distance between two Si atoms is marginal, i.e., there is marginal structural relaxation and, thus, there is a high tendency for the Si–Si bond to reform. Hence, the trapped-hole site is annihilated when the stress V_g is removed [158], [159]. On the other hand, a high oxide field could facilitate the transformation, via distortion of the oxide

network and/ or enhanced interaction between energetic holes and the lattice, of the E'_δ center into the E'_γ center. The latter is a relatively permanent form involving significant structural relaxation [158], [159]. As a result, the tendency for the trapped-hole site to revert to the Si–Si dimer precursor state is reduced. These more permanent trapped-hole sites, in turn, increase $|\Delta V_t|^{\text{eor}}$ and contribute an additional gate leakage current. It should be noted that the categorization of trapped holes as E'_δ or E'_γ is broad; one should expect the structural recovery time of a given trapped-hole site to be determined by the local atomic arrangement and random interaction with phonons. Thus, “intracategory” transformations and considerable spread of recovery time in each category are likely scenarios.

4.4 The Effect of High Temperature Stressing on the R Component of Dynamic NBTI: Evolution of Hole-Trapping in the Oxynitride Gate P-MOSFET Subjected to Negative-Bias Temperature Stressing

Although a consensus on the microscopic mechanisms of NBTI is not yet achieved, it has been broadly agreed that both hole-trapping and interface state generation are responsible for the threshold voltage shift (ΔV_t) observed during stressing. As discussed before, the latter is shown to be relatively permanent, resulting in a steady (ΔV_t) increase [147], [162]. The former, on the other hand, is highly transient in nature, accounting for almost the entire $|\Delta V_t|$ recovery typically observed under pulsed gate condition. At present, the exact impact of

the observed hole-trapping on NBTI remains an open question, though the cyclical behavior of V_t fluctuation under dynamic gate stressing [152] tends to imply that these hole-traps are pre-existing oxide defects related to a particular gate oxide process and are therefore irrelevant to the long term NBTI effect [163], which we have proven to be not the case in Section 4.3.2. In this section, we present experimental evidence of a *thermally activated* transformation of Negative-Bias Temperature Stress induced transient hole-trapping at pre-existing oxide traps into more permanent trapped holes in the ultra-thin oxynitride gate p-MOSFET. Similar to the effect of high oxide field stress on R , the transformation is also shown to correlate with the generation of Stress-Induced Leakage Current (SILC), indicating that it is one of the key mechanisms of the bulk trap generation process that limits gate oxide reliability. With metal oxides replacing the oxynitride as the gate dielectric, transient oxide charge trapping induced ΔV_t fluctuation in High- κ gate p-MOSFETs would become an even more serious problem due to the inherently higher density of pre-existing defects. In our group's recent study on the HfO_2 gate p-MOSFET [164], the ΔV_t recovery due to transient hole-trapping was found to decrease progressively when the device was subjected repeatedly to stressing and relaxation. Although similar observation [153] applies to the HfO_2 gate p-MOSFET, unlike the HfO_2 gate p-MOSFET, such transformation is not apparent at a temperature of $\sim 100^\circ\text{C}$ in SiON [152]. It only becomes obvious at higher temperatures. The results, again, imply that pre-existing oxide defects, usually deemed as irrelevant to NBTI, have a definite role on long term device

parametric drifts. In addition, an excellent linear correlation between hole-trap transformation and the generation of Stress-Induced Leakage Current or SILC (which signifies bulk trap generation) in the presence of high temperature will also be revealed. This suggests that a major part of bulk traps responsible for SILC had actually evolved from the hole-trap transformation process. The similarity of hole-trapping evolution in the oxynitride and HfO_2 gate p-MOSFETs indicates the possibility of the observed hole-trap transformation to be a common mechanism for bulk trap generation across different gate stack technologies. A possible reason for the observed difference in temperature dependence for both SiON and HfO_2 will be discussed later.

4.4.1 Experimental Details

Test devices used in this section were p-MOSFETs with p+ polysilicon gate and 1.7 nm oxynitride (decoupled plasma nitrided) dielectric. Results reported in this section were obtained on devices with a drawn channel width and length of 10 μm and 70 nm respectively, unless stated otherwise. The devices were subjected to 40 DNBTI stress and relaxation phases, each lasting 1×10^3 s. Relaxation was always performed under a 0 V gate voltage (V_g). As many as 20 devices were stressed under each of the following cases: Condition (A) $V_g = -1.8$ V; $T = 100^\circ$ C; Condition (B) $V_g = -2.1$ V; $T = 100^\circ$ C; Condition (C) $V_g = -1.8$ V; $T = 220^\circ$ C. Apart from the above two temperatures, hole-trapping evolution was also examined at other intermediate temperatures. Degradation

was monitored in terms of ΔV_t , extracted (via a constant subthreshold drain current method) from linear transfer curves measured by an ultra-fast switching method [134]. Gate current I_g measurements were also made before and after various DNBTI stress conditions (as mentioned above) to probe bulk trap generation.

4.4.2 Results and Discussion

Figure 4-13: Evolution of $|\Delta V_t|$ in a typical dynamic NBTI cycle, comprising a stress and relaxation phase each lasting 1×10^3 s.

Figure 4-14: $|\Delta V_t|$ recovery per cycle or R as a function of the number of dynamic NBTI cycles for different gate stress voltages and temperatures.

Fig. 4-13 shows a typical cycle of p-MOSFET V_t shift during stress and relaxation for case A, which is similar to which have been mentioned in Section 4.3. The evolution of R is examined in Fig. 4-14 as a function of the number of dynamic NBTI (DNBTI) cycles. Similarly, at 100 °C, a constant R is evident in accordance with our previous observations in Section 4.3.2 and a previous report [152], which implies that it is always the similar group of hole-traps that charge up positively under stress and completely discharge during relaxation. Moreover, this inference is also corroborated by time-dependent defect spectroscopy [165] showing very consistent capture/ emission time constants of individual hole-traps in small area devices.

Figure 4-15: Shows the P component, $|\Delta V_t|$ at the end of the 40th DNBTI cycle of stress for different conditions (A, B, and C) depicted in Fig. 4-14. Also shown is the decrease in R (as a result of its transformation into a more permanent form). For case C involving a substantial decrease in R , the P is inclusive of this transformed part of R . Data shown are the averages of 20 devices for each case.

Maintaining the temperature at 100° C and increasing the stress V_g to -2.1 V in case B resulted in a larger magnitude of the R component. This means that more hole-trapping is generated during stress due to the increased $|V_g|$. However, it also remained constant throughout as in case A. Although it has been reported in our previous section that a much higher oxide field (> 13 MV/cm) could also trigger a decrease of R , as shown in [166], for the oxide field (~ 8 -10 MV/cm) examined in this work, such effect is negligible within the period of study. For both cases A and B, the absence of any I_g increase after 40 DNBTI cycles, as shown in Fig. 4-17 (a) and (b) suggests very strongly that the hole- traps concerned are pre-existing defects in the gate oxide. However, keeping V_g at

-1.8 V or the oxide field fixed but increasing the temperature to 220° C (case C) resulted in a significant *decrease* of R .

Figure 4-16: The absolute and percentage decrease of R as a function of stress temperature for a gate stress voltage of -1.8 V.

Fig. 4-16 depicts the decrease in the transient hole-trapping/ R at intermediate temperatures between 100 and 220° C. A similar decrease at high temperature was also observed by Grasser *et al.* for the oxynitride p-MOSFET in [167] but no clear explanation for the decrease was offered. The decrease indicates that in each stress phase under $T > 100^\circ\text{C}$, a portion of the transient hole-trapping is rendered more permanent, which leads to an apparent reduction in $|\Delta V_t|$ recovery in the ensuing relaxation phase.

However, one should be cautioned against the tendency to infer the validity of the Reaction-Diffusion model based on the observation of a decreasing R *alone*. A combination of other observations clearly do not support this inference: 1) The thermal activation energy of hole- trapping is ~ 60 meV [152]. Thus, hole-trapping at 220°C is $\sim 1.5\times$ that at 100°C . The R for the first DNBTI cycle at 220°C is $\sim 1.4\times$ that at 100°C as evident in Fig. 4-14, which is in good agreement with the increased hole-trapping predicted above. This also suggests that the contribution of interface state relaxation to $|\Delta V_t|$ recovery or R remains negligible at 220°C . 2) At the 40th DNBTI cycle, the amount of R at 220°C is in fact smaller than that at 100°C . This implies and supports that a fraction of the transient hole-trapping at 220°C is being converted into more permanent trapped holes.

Figure 4-17: (a)-(c) show the impact of stress A, B and C on the generation of Stress-Induced Leakage Current (SILC) after the 40th dynamic NBTI cycle. In the case of case A and B where R is constant despite the $\sim 2\times$ greater $|\Delta V_t|^{\text{cor}}$ of the latter (Fig. 4-15), the gate tunneling current I_g is practically unchanged, i.e. there is negligible generation of SILC. As for case C, significant generation of SILC can be observed in conjunction with the $\sim 30\%$ reduction in R .

Interestingly, the observed transformation of transient hole-trapping into more permanent trapped holes for condition C happens concurrently with the generation of SILC or bulk traps, as depicted by the significant increase in I_g after the 40th DNBTI cycle in Fig. 4-17 (c) (Fig. 4-15; $\Delta R \sim 22$ mV, 30%). It should be emphasized that the occurrence of SILC is not coincidental but is tightly linked to the decrease in R , i.e. SILC is always *not* observed when R is constant and is always observed when R decreases. The evolution of $|\Delta V_t|^{\text{eos}}$ and $|\Delta V_t|^{\text{eor}}$ are examined as a function of the number of DNBTI cycles in Fig. 4-18 below.

Figure 4-18: $|\Delta V_t|^{\text{eos}}$ and $|\Delta V_t|^{\text{eor}}$, the respective $|\Delta V_t|$ at the end of stress (eos) and the end of relaxation (eor), as a function of the number of dynamic NBTI cycles for two different temperatures (100 and 220° C). The gate voltage was -1.8 V in both cases.

Similar to what has been observed for the high oxide field effect, at 100°C , both $|\Delta V_t|^{\text{eos}}$ and $|\Delta V_t|^{\text{eor}}$ increase in tandem, yielding a constant R . But, at 220°C , it is obviously noticed that $|\Delta V_t|^{\text{eor}}$ increases much faster than $|\Delta V_t|^{\text{eos}}$. Since the $|\Delta V_t|^{\text{eos}}$ which probes the effect of both transient hole-trapping and interface state generation of the 100 and 220°C stresses are increasing at a comparable rate, the possibility that the faster rate of $|\Delta V_t|^{\text{eor}}$ increase at the higher temperature is a result of a higher rate of interface state generation may be ruled out. The result thus confirms that a portion of the hole-trapping is rendered more permanent during stressing at a higher temperature.

Figure 4-19: (a) The decrease of R or ΔR during DNBTI tracks the increase in $\Delta I_g/I_{g0}$ or SILC generation very closely. (b) ΔR shows a good linear correlation with fractional increase of $\Delta I_g/I_{g0}$. The best-fit regression line is as shown. The p-MOSFET was stressed at -1.8 V at 200°C .

Fig. 4-19 (a) shows the decrease of R or ΔR closely tracks the increase of $\Delta I_g/I_{g0}$ or SILC generation (where I_{g0} denotes the pre-stress value). Furthermore, the

two exhibit a good linear correlation as depicted in Fig. 4-19 (b). Based on these results, we could infer that the relatively permanent bulk traps responsible for SILC and the more permanent trapped holes which evolved from the transient hole-trapping share a common defect origin. It is interesting to point out that a nonnegligible relatively permanent $|\Delta V_t|$ (~ 25 mV after 40 DNBTI cycles) can be observed at 100°C (as seen in Fig. 4-18) for which SILC generation is clearly absent. The latter implies that the defects responsible for the relatively permanent $|\Delta V_t|$ must be located at or very close to the Si interface. As reported in the literature, interface defects are generally believed to consist of dangling Si bonds or P_b centers resulting from Si-H bond dissociation, as supported by electron spin resonance measurement [168]. On the otherhand, bulk defects are generally believed to be oxygen vacancies where some of the promising candidates are none other than the E' and/or k_N centers [169]- [171]. But the co-existence of the E' and k_N centers as well as other non-paramagnetic defects at the interface could not be ruled out at this stage. Nevertheless, the results presented clearly shows that at moderately high temperatures ($\sim 150^\circ\text{C}$) that are still within the scope of interest of NBTI, bulk trap generation constitutes a substantial part of the relatively permanent $|\Delta V_t|$. Fig. 4-20 denotes the nonrecoverable nature of the more permanent trapped holes evolved from the transient hole-trapping during NBTI stressing at high temperature.

Figure 4-20: The I_g evolution (before and after) 20 DNBTI cycles of V_g stress = -1.8/ 0 V, SR = 1000 s at $T = 220^{\circ}\text{C}$. After DNBTI stress, the device was swept from -1.5 to 1.5 V and vice-versa repeatedly for 10 times. Almost no I_g recovery has been observed despite sweeping the device into a positive V_g region to detrapp the deeper trapped holes. It shows that the recovery of the more permanent trapped holes (evolved from ΔR) back to its original precursor state is negligible/ almost impossible within the period of study.

Figure 4-21: Ball and stick diagrams of the SiO_2 (left) and HfO_2 (right) supercells used in the VASP simulation study. The initial SiO_2 supercell comprised 8 α -cristobalite unit cells ($2 \times 2 \times 2$) of dimensions $9.96 \times 9.96 \times 13.90 \text{ \AA}^3$ and density is 2.32 g/cm^3 . The initial HfO_2 supercell comprised 8 cubic unit cells ($2 \times 2 \times 2$) of dimensions $10.23 \times 10.23 \times 10.23 \text{ \AA}^3$ and density 10.45 g/cm^3 . Molecular dynamic simulation was then used to achieve a pseudo-amorphous structure for both cases. There are a total of 96 atoms (64 O atoms and 32 Si or

Hf atoms) in each supercell. The electronic structure was described based on density functional theory using the PBE approximation. An oxygen vacancy defect is manually created at each of the 64 O lattice points by removing an O atom and allowing the system to fully relax at the Γ point. [Courtesy: C. J. Gu]

The exact mechanism for the observed hole-trap transformation is unclear since the atomic nature of the defect is not yet established. But the tendency for trapped-hole sites to become more permanent at high temperatures may be broadly explained by the expected increase of structural relaxation following bond breakage (or hole capture) due to enhanced phonon interaction. An interim explanation may also be based on the oxygen vacancy defect, which is a common source of hole-traps in the gate oxide [169] and whose presence after NBTI stress has been detected in the form of the paramagnetic E' or k_N center [170]- [171]. At a high temperature, the structural relaxation associated with the capture of hole at the oxygen vacancy defect [172] is expected to increase, rendering the trapped-hole site more permanent and could therefore be sensed by the slow I_g measurement when $E'_\delta \rightarrow E'_\gamma$ transformation occurs.

Figure 4-22: Mean square displacement (MSD) of 95 atoms in the supercell following the capture of a hole by an oxygen vacancy defect, for all (64) possible cases. Compared to the SiO₂ which exhibits minimal structural change, the HfO₂ exhibits significantly larger structural change upon a hole capture by an oxygen vacancy defect. This result implies that the tendency to form permanent defects is higher in the HfO₂. [Courtesy: C. J. Gu]

Although the evolution of hole-trapping during Negative-Bias Temperature stressing of the oxynitride gate p-MOSFET is broadly similar to that of the HfO₂ gate p-MOSFET [164], a subtle difference is worth mentioning. Transient hole-trapping in the latter is found to exhibit a greater susceptibility of being transformed into more permanent trapped holes under similar conditions. For instance, the R of the HfO₂ gate p-MOSFET, under an oxide stress field of ~ 8 MV/cm, is decreased by $\sim 38\%$ after 40 DNBTI cycles [164, Fig. 2] whereas that of the oxynitride gate p-MOSFET remains constant throughout as depicted earlier in Fig. 4-14. Apart, study which is carried out on the HfSiON gate p-

MOSFET having larger R (which implies a higher density of pre-existing oxide defects) than the oxynitride and HfO_2 gate devices also

Figure 4-23: (a) and (b): Charge transition levels (CTLs) (at 0 K) corresponding to all (64) possible oxygen vacancy defects in the (a) SiO_2 and (b) HfO_2 supercells. CTL is computed from the difference in the system energy of the positively charged and neutral oxygen vacancy defects, after band edge shift upon possible charging. Band gap correction is achieved using a hybrid functional scheme. For the SiO_2 case, the CTLs are clustered at ~ 2 eV above the oxide valence band edge, i.e. a majority of the defects constitute shallow hole traps which may be inactive under a nominal gate voltage of 1 V but are “activated” at voltages more than 2 V. In conjunction with a minimal structural change upon hole capture (cf. Fig. 4-22), they could account for the fast transient and highly cyclical V_t fluctuations observed under DNBTI (cf. Figs. 4-14, 4-17 (a), (b)). Only a very small percentage of the defects have relatively large structural relaxation and have slightly deeper CTLs. On the other hand, CTLs in the HfO_2 show a large scatter, with a much higher percentage of very deep CTLs (above the Si conduction band edge) corresponding to trapped hole sites exhibiting large structural relaxation (thus are permanent). [Courtesy: C. J. Gu]

shows that it remained constant after 40 DNBTI cycles at 100°C [164]. This suggests that fabrication process is not the main reason for the stronger dependence of hole-trap transformation on temperature in the HfO_2 gate p-MOSFET. A possible explanation lies in the different gate oxide materials (Fig. 4-21). *Ab-initio* simulation study [173] has shown a much stronger charge lattice interaction in more ionic materials such as the HfO_2 than in less ionic

materials such as the SiO_2 . Thus, as shown in Fig. 4-22 the inherently greater structural relaxation of the oxygen vacancy defect sites following hole capture may explain the presence of more stable trapped holes in the HfO_2 at a given temperature. Correspondingly, the lowering of system energy is more significant leading to a higher number of deeper hole traps (relative to the valence band edge) in the HfO_2 , which is demonstrated in Fig. 4-23.

4.5 Chapter Summary

In short, the impact of high oxide field and high temperature stressing on the R component (transient “switching” hole-trap) has been studied. From a dynamic NBTS study, we have found no evidence of I_g increase (or bulk trap generation) in spite of a nonnegligible relatively permanent V_t shift after numerous stress/relaxation cycles with a cumulative stress time in the order of 10^4 s. This finding implies that some of the more permanent defects responsible for the V_t shift are situated very close to or at the SiON/Si interface, i.e., a substantial part of the interface degradation under NBT stress is not correlated with oxide (bulk) trap generation. We also show that the link between oxide trap generation and NBTI is actually found in the hole-trapping component of the latter by introducing a CVS prior to the DNBTI cycles. When oxide trap generation occurs, a reduction of the recoverable hole-trapping component or an increase of the permanent hole-trapping component is observed. The results infer that the oxide trap generation observed under the stress condition studied is due to the conversion

of the recoverable trapped-hole sites into a more permanent form. A possible explanation based on the oxygen vacancy defect has been proposed.

Besides, based on the temperature experiments, transient hole-trapping at pre-existing oxide defects in the oxynitride gate dielectric, previously deemed as irrelevant to NBTI, is shown to play a definite role on the long term NBTI and gate oxide reliability. In particular, evidence similar to that obtained on the HfO_2 gate p-MOSFET, showing the transformation of transient hole-trapping into permanent trapped holes under NBTI stressing is presented. Similarly, the transformation corresponds to SILC or bulk trap generation, and the increase in the permanent trapped holes correlate linearly with the bulk trap generation. This suggests that the bulk traps and the more permanent trapped holes which arise from the transient hole-trapping originated from a common oxide defect precursor. As the transformation occurs at temperatures within the scope of the NBTI issue, the inclusion of this effect would be necessary to achieve a more complete NBTI and gate oxide aging model.

CHAPTER 5: A NEWLY DISCOVERED NON-ARRHENIUS TEMPERATURE DEPENDENCE AND FREQUENCY INDEPENDENCE OF THE “SWITCHING” HOLE-TRAP/ TRANSFORMATION IN 65 NM SION

5.1 Temperature Dependence

5.1.1 Introduction

The emergence of low-field excess leakage current through thin oxides of MOS structures is a common feature to many damaging process encountered during processing or normal use conditions. Its transport mechanism remains controversial. A decade ago, there were debates in the research community regarding the main mechanism which is closely associated to the Stress-Induced Leakage Current (SILC). Some were in favour of a modified direct tunneling process assisted by traps located at a tunneling distance of both interfaces, rather than through a triangular barrier (Fowler-Nordheim like) [193]; while some supported the claim that SILC has a Schottky-Poole Frenkel (PF) like property limited by the emptying process of the traps [192]. Nevertheless, none of them reported a full description about the origin of the traps located in the oxide which were involved in the tunneling process. In 1995, it has been demonstrated by H. Sadake that the activation energy of the appearance of SILC agreed well with that of electron trap generation (n-MOSFETs were used) so far reported. It was also, thus, concluded that a common mechanism dominates both SILC and

electron trap generation in the n-MOSFETs [194]. The author has mentioned that the temperature sensitive component showed an activation energy of ~ 0.1 eV and has therefore, considered the diffusion of atomic hydrogen released from O-Si-H bonds as the origin for generating tunneling sites for Stress-Induced Leakage Current. However, with the introduction of advance fast measurements since 2005, the activation energy of ~ 0.1 eV for the hydrogen released model was later proven to be not accurate [19], [22]. After decoupling the total $|\Delta V_t|$ into two distinct degradation mechanisms as observed in DNBTI, the activation energy of the interface state generation (ΔN_{it}) was noticed to remain at its classical value ~ 0.27 eV [19]; while the activation energy for the temperature insensitive hole-trapping (ΔN_{ot}) was found to be ~ 0.0614 eV [19]. These new observations did not conform to the hydrogen release model and the role of hydrogen was subsequently questioned. These indicate that there was still a lack of interest/ attention in investigating the missing link between the defects generated during BTI with SILC, though there were a few attempts made by M. Sato and Tsujikawa *et al.* [117], [195] in search of the common origin for both degradation mechanisms. In Chapter 4, we have shown the linear correlation between ΔN_{ot} with SILC, which is found in the “switching” hole-trap (SHT)/ R component during DNBTI. In this chapter, we will investigate more about this correlation from a different perspective with further evidences provided. The activation energy obtained for the “switching” hole-trap transformation using Ultra-Fast Switching method (UFS) will be discussed together with the temperature dependence of SILC, where both are observed to

be non-Arrhenius. A “roll-off” area, which happens at $110 < T < 125^\circ \text{C}$, separates the activation energy into two temperature regions for both ΔR and SILC. Surprisingly, the E_a observed for both mechanisms at these two temperature regions are comparable. This enhances the speculated, possible linear correlation between both degradation mechanisms. Besides, a comparison of the time exponents (n) for both ΔR and SILC are performed. Similar observations are also applied to HfSiON oxides (p-MOSFETs), implying a common, hidden mechanism which dominates ΔN_{ot} and SILC across different gate oxide technologies. Lastly, the study on the frequency dependence of this thermally activated hole-trapping transformation will be elaborated.

5.1.2 Experimental Details

Test devices (DUTs) were 1) p-MOSFETs with p^+ polysilicon gate and 1.7 nm oxynitride (decoupled plasma nitrided) dielectric; 2) High- κ metal gate p-MOSFETs with 1.7 nm HfSiON dielectric. The HfSiON p-MOSFETs used in the experiments were fabricated via a gate-first integration flow and were formed by ALD. An ultrathin SiON interfacial layer (IL) existed between the Hf-based dielectric and the substrate.

Devices under categories 1 and 2 were measured using UFS and SILC. As for UFS, the DUTs were subjected to 38 dynamic NBTI stress and relaxation cycles at various temperatures ranging from 100°C to 200°C (unless stated otherwise) at stress voltage, $V_g = -2 \text{ V}$ and relaxation voltage, $V_g = 0 \text{ V}$, each lasting $1 \times 10^3 \text{ s}$,

i.e. 50% duty cycle. Device degradation (in terms of ΔV_t extracted using a constant subthreshold drain current method from linear transfer curves measured by an ultra-fast switching method [134]) was monitored only during the DNBTI. The current used in the constant subthreshold drain current method was $\sim 300 \text{ uA}$. The ΔV_t calculated during each DNBTI cycle probed the effect of T on the recoverable behavior of the transient “hole-trapping” mechanism. On the other hand, another set of DUTs (for SiON and HfSiON p-MOSFETs) would first undergo a constant voltage stress (CVS) of $V_g = -2 \text{ V}$ for 1000 s, followed by a SILC measurement made by applying two directional voltage sweep from $-1 < V_g < 1$ and vice versa V (unless stated otherwise). Thereafter, this experimental sequence was repeated numerous times until a cumulative stress time of 38,000 s for every desired temperature. The $\Delta I_g / I_{g@fresh}$ calculated after each CVS cycle gauge the effect of T on the bulk trap generation.

Dimensions of devices used were $10 \times 0.06 \text{ }\mu\text{m}^2$ and $10 \times 0.07 \text{ }\mu\text{m}^2$ for SiON; $2 \times 0.04 \text{ }\mu\text{m}^2$ and $2 \times 0.044 \text{ }\mu\text{m}^2$ for HfSiON.

5.1.3 Results and Discussion

Fig. 5-1 demonstrates the evolution of activation energy across various temperatures of the SiON gate dielectric obtained using two independent measurement techniques for both ΔR and $\Delta I_g / I_{g@fresh}$. For Arrhenius dependence, a linear relationship with inverse temperature should result across the range of temperature studied. It can be clearly seen in Fig. 5-1 that the E_a has no

“continuous” linear relationship with the inverse temperature across the range of temperature studied, therefore, showing a “non-Arrhenius” temperature dependence of the E_a for both ΔR and $\Delta I_g/I_{g@fresh}$. First of all, let us gear our attention to the temperature dependence of ΔR for SiON devices. It should be mentioned that the measurement resolution limit of the UFS system is ~ 1 mV. Thus, results which are below this resolution limit (dashed line) would not be given any consideration as they are likely to be affected by noise during measurement. A “roll-off” has been observed near 125°C , which separates the activation energy into two regimes. One is termed as the low temperature region ($< 125^\circ\text{C}$) while the other is the high temperature region ($> 125^\circ\text{C}$). The activation energy (gradient) is obtained using the formula below:

$$\ln (\Delta R \text{ or } \Delta I_g / I_{g0}) = -E_a (1 / kT) + \ln \text{ constant} \quad (\text{Eqn. 5-1})$$

Figure 5-1: Evolution of ΔR and $\Delta I_g / I_{g@fresh}$ (where $I_{g@fresh}$ denotes the pre-stress measurement) as a function of temperature. Both show a non-Arrhenius temperature dependence. The activation energies obtained at low and high temperature regimes are comparable for ΔR and $\Delta I_g / I_{g@fresh}$, despite using totally different measurement methods to measure both parameters in SiON.

Two distinct activation energies are observed in Fig. 5-1. At the low temperature region, the $E_{a, \Delta R (low)} = \sim 0.90$ eV; whereas at the high temperature region, the $E_{a, \Delta R (high)} = \sim 0.347$ eV. These results imply that a larger amount of energy is needed to result in the transformation of “switching” hole-trap/ R into more permanent charge states when T is low. However, as the temperature increases, a very much smaller amount of energy is needed instead for this transformation to take place ($E_{a, \Delta R (high)} = \sim 0.347$ eV). This corroborates our inference where in order to activate the ΔR component, the structural relaxation must be significant enough to prevent the strained Si-Si bonds of the trapped-hole sites from returning back to its original positions (reform). Hence, at low

temperature region, it is understood that a larger amount of energy is required to activate the conversion. However, when the temperature is sufficiently/moderately high, the phonon vibration due to temperature itself has already reduced the tendency for the trapped-hole site to revert back to the Si-Si dimer precursor state. As a result, a relatively smaller amount of energy (E_a is smaller at high temperature region) is required to prevent the reformation of the structurally relaxed Si-Si bonds in the oxide defects. Hence, upon the release of gate bias during relaxation, these trapped-hole sites which are charged up during stress would be easily rendered permanent and thus, resulting in a relatively long emission time. Interestingly, similar observations to that of ΔR have been observed for $\Delta I_g/I_{g@fresh}$. Fig. 5-1 also depicts the non-Arrhenius temperature activation of the generated bulk traps obtained using SILC ($-1.5 \text{ V} < V_g < -1.5 \text{ V}$). The generated bulk traps are gauged by calculating the increment of gate leakage current in SILC as shown in Eqn. 5-2:

$$I_g \text{ increment} = (I_g' - I_{g@fresh}) / I_{g@fresh} (\%) \quad (@ V_g = -1.5 \text{ V})$$

(Eqn. 5-2)

The “roll-off” region occurs near $\sim 105^\circ \text{C}$ and separates the Arrhenius plot into the low and high temperature regimes. Though the $E_{a, \Delta I_g (\text{low})} = \sim 0.76 \text{ eV}$ and $E_{a, \Delta I_g (\text{high})} = \sim 0.26 \text{ eV}$ of $\Delta I_g/I_{g@fresh}$ obtained by SILC are slightly lower than ΔR (UFS), it would still be reasonable to consider them comparable with each other. And, although two independent measurement methods are used here, it should be noted that the evolution of E_a across the range of temperatures is very

similar for both ΔR and $\Delta I_g/I_{g@fresh}$. These results further affirm our earlier inference that ΔR is correlated linearly with the generated bulk traps observed in SILC. It should also be emphasized that, these observations are also evident in accordance with some previous reports [196]. Kaczer *et al.* has shown that the Arrhenius law did not correctly match the observed T dependence of time-to-breakdown (t_{bd}) [197] while Petit *et al.* has also observed the non-Arrhenius temperature dependence of oxide breakdown, which is in good agreement with [197]- [200]. Additionally, there were other studies reported by different authors about this non-Arrhenius temperature activation in ultra-thin SiON oxides [201], though there were arguments and different viewpoints about attributing this temperature dependence to the effect of oxide thickness or to the effect of voltage.

Similar observations for both ΔR and $\Delta I_g/I_{g@fresh}$ apply to High- κ gate p-MOSFETs (HfSiON), which is denoted in Fig. 5-2, further supports that the observed phenomenon is generic across different gate oxide materials. However, it should be mentioned that the activation energy at high temperature region for both ΔR ($E_{a, \Delta R (high)} = \sim 0.094$ eV) and ΔI_g ($E_{a, \Delta I_g (high)} = \sim 0.124$ eV) are very much smaller as compared to those observed in SiON dielectric. This might be due to the complexity of High- κ dielectric deposition which is generally understood to result in an inherent

Figure 5-2: (a) and (b): Evolution of ΔR and $\Delta I_g/I_{g@fresh}$ (where $I_{g@fresh}$ denotes the pre-stress measurement) as a function of temperature for HfSiON p-MOSFETs. Similar to SiON, both also show a non-Arrhenius temperature dependence. The activation energies obtained at low and high temperature regimes are comparable for ΔR and $\Delta I_g/I_{g@fresh}$, despite using totally different measurement methods to measure both parameters in HfSiON.

higher density of pre-existing defects. We suspect that, in addition to the phonon vibration/ lattice interactions due to the temperature effect, the presence of these pre-existing defects in the High- κ p-MOSFETs might be the reason

causing the energy barrier which is to be overcome during the emission process to lower drastically, i.e. it means that it would be rather easy for the “switching” hole-trap evolution process into permanent trapped-holes sites to occur in the High- κ dielectrics. Besides, it might also be due to the stronger lattice interactions in the more ionic Hf-based oxides reported by Ab-initio simulation study as compared to the less ionic amorphous SiON oxides [76]. Thus, HfSiON would have inherently greater structural relaxation of the trapped hole sites following hole capture. Another possibility of obtaining a smaller E_a for HfSiON at high temperature region would be the different fabrication process of SiON and HfSiON dielectrics.

Figure 5-3: The time exponent (n) extracted for ΔR and $\Delta I_g / I_{g0}$ in the SiON devices. Both increase in a similar, gradual trend.

Based on the classical power law, ΔI_g or $\Delta R = \text{constant} \times \text{time}^n$, n could be easily obtained from the gradient of the graphs where $\log_{10} [\Delta I_g \text{ (or } \Delta R)]$ is

plotted against $\log_{10}$ [stress time]. Fig. 5-3 examines the evolution of the time exponents (n) over a range of temperatures for both ΔR and $\Delta I_g/I_{g@fresh}$ for SiON devices are shown respectively. n at 100° C is not extracted as $\Delta R \sim 0$ mV, i.e. no “switching” hole-traps have been activated into more permanent defects at this temperature. In general, n is increasing with temperature. And, it could be clearly seen that the time exponent values for both the transformed/ evolved “switching” hole-traps and the generated bulk traps are comparable (in fact quite similar to each). Apart, the ΔR and $\Delta I_g/I_{g@fresh}$ follow a classical power law. It should be highlighted that the time exponent values obtained using both different techniques are noticeably similar to that of the classical exponent, α reported for SILC [193], [202]- [204]. In these reports [193], [202]- [204], the exponent α of SILC ranged from $\sim 0.22 - 0.47$. But, the difference in the values was not explained. It was then discussed by Petit *et al.* in [202] that the various α values obtained from one author to another was probably influenced by gate-processing technology.

However, based on our experimental results which are depicted in Fig. 5-3, we speculate that the variation as observed in α could also be likely due to the thermally activated “switching” hole-trap transformation process, i.e. n tends to be larger when ΔR or $\Delta I_g/I_{g@fresh}$ becomes more apparent at high temperature. Moreover, the n noticed for both the reduction in R and the corresponded generation of bulk traps which ranges from 0.21 to 0.45 across increasing temperatures, again, indicates the

Figure 5-4: The time exponent (n) extracted for ΔR and $\Delta I_g / I_{g0}$ in the HfSiON devices. Both are noticed to be comparable and they increase in a similar, gradual trend.

tight interaction between NBTI and SILC. And, this underlying correlation would only be evident when the transformation is activated, as explained and illustrated in Chapter 4. It is important to note that the observed evolution of the time exponent, n with increasing temperature for ΔR and $\Delta I_g / I_{g@fresh}$ in the SiON oxides are also applied to HfSiON dielectric p-MOSFETs as depicted in Fig. 5-4. Hence, these results highlight an important point that this discovered correlation between NBTI and SILC is a common phenomenon shared across different gate oxide technologies.

Besides, T. Grassler’s proposed model in [205], which is mainly derived from mathematical expressions and simulations, seems to support our experimental results on the “switching” hole-trap transformation process. This model was initially suggested and modified to explain the author’s frequency dependence

results. According to the proposed advanced capture/ emission time (CET) map model in [205], the initial precursor state is termed 1 and the positively charged state is named 2 while 2' is a metastable state (a third defect state introduced by T. Grassler) as shown in Fig. 5-5.

Figure 5-5: A simplified defect model which describe the transition of a neutral state (1) to a metastable state (2'), before reaching a relative permanent defect state (2) [205].

State 1 to 2' is similar to what has been observed in the dynamic NBTI (with the absence of CVS/ moderate high temperature) when the “switching” hole-trap/ cyclical R remains constant and recoverable. Hence, state 1 would transit to state 2' and vice versa repetitively during the charging and discharging process. The strained Si-Si bonds of the E' center could still be reverted back to its dimer precursor state as no significant structural relaxation is involved. At this point of time, there is least tendency for the charge state to transit from $2' \rightarrow 2$ as a kind of energy barrier has yet to be overcome. However, once the “switching” hole-trap transformation has been thermally activated, the charge state would by-pass stage 2' and proceed directly from state 1 to 2 (which is a more permanent, stable charge state). This is strongly supported by the results obtained in Figs. 5-1 and 5-2, whereby the energy barrier needed to be overcome is reduced

substantially as the activation energy for both ΔR and $\Delta I_g/I_{g@fresh}$ is found to be much lower at high temperature region. It is also mentioned by the T. Grassler that, once the charge is trapped at 2, it would not recover back to its initial position (state 1) immediately upon the release of gate bias. This explanation seems to support our notion that, once the conversion takes place, the structural relaxation associated with the capture of hole at the trapped sites is expected to increase, rendering the trapped-hole site more permanently. And thus, resulting in a relatively longer time needed for the strained Si-Si bonds to be reformed, i.e. less possible for the positive charge to be emitted from the trapped sites.

5.2 Frequency Dependence

Contradictory to earlier reports regarding the frequency independence of NBTI published in literature, with particularly older studies and those interpreted in the framework of the reaction diffusion model, newer studies have clearly shown a frequency-dependent component of BTI. It has been depicted by Tsai *et al.* in the literature that the fast states (shallow hole traps/ R) measured by fast measurements during NBTI experiments were observed to be frequency dependent and duty-cycle dependent [206]. On the other hand, slow traps and interface states which were easily measured by conventional slow measurements was frequency independent. Recently, the existence of a frequency dependent component has also been observed by T. Grassler, who has claimed that previous studies on the frequency dependence published in literature probably suffered from various issues such as unspecified delay or a

1 MHz, mainly at a temperature of 160° C and 200° C, unless stated otherwise.

Device dimension used was 10 x 0.06 μm^2 .

5.2.2 Results and Discussion

Figure 5-6: Illustrates the disadvantage of using ΔR as compared to ΔI_g to study the impact of frequency on the transient “switching” hole-trapping evolution.

We have observed that ΔI_g might have an advantage over ΔR (which is calculated in terms of V_1 or I_d) as a gauging parameter in order to study the frequency dependence of the “switching” hole-traps. The reason is explained based on Fig. 5-6.

As depicted in Fig. 5-6, two similar DUTs have initially undergone an AC stress, in which the devices have been charged/ discharged repeatedly by an alternating stress of -2 and 0 V, maintaining the frequency at 1 Hz at two different temperatures, 100 and 200° C. After reaching a cumulative stress time of 5000 s, a 10, 000 s of recovery at 0 V has then been performed. During measurement, the gate bias is brought down to a measurement voltage of -1 V (V_{DD}). It is observed that at 100° C, the device suffers from a lesser drain current degradation (smaller ΔI_d) as compared to that of the device at 200° C. Not to our surprise, the same observation applies when the frequency is increased to 10 kHz for both 100 and 200° C, as shown in Fig 5-6 (b). This result indicates a sign of conversion of the “switching” hole-traps taking place at high temperature regardless of any frequency applied. It also means that the amount of drain current recovered after the AC stress at 200° C is always lesser as compared to the amount of drain current recovered at 100° C. However, one should be cautioned against the tendency to infer the validity that the conversion of these transient “switching” hole-traps is frequency dependent because at 200° C, higher frequency (10 kHz) seems to result in a more severe drain current degradation as the I_d recovers slower as compared to 1 Hz at 200° C. It would be

misleading to compare these results without further analysis as the total amount of drain current degraded during AC stress ($|\Delta I_d|^{\text{eos}}$) is found to differ with various frequencies and temperatures. For instance, at a frequency of 1 Hz at 100° C, the $|\Delta I_d|^{\text{eos}}$ after 5000 s of AC stress is ~55 μA while the $|\Delta I_d|^{\text{eos}}$ at a frequency of 10 kHz at the same temperature is decreased till ~42 μA . This could be briefly explained as low frequency (1 Hz: half of the period is 0.5 s) is expected to charge up more trapped-hole sites as compared to a high frequency (10 kHz: half of the period is 50 μs). Therefore, for the case at 200° C of 10 kHz, a smaller magnitude of ΔR ($= |\Delta I_d|^{\text{eos}} - |\Delta I_d|^{\text{eor}} = 13 \mu\text{A}$) seems unlikely to be due to the effect of high frequency. It is more likely to arise from the smaller $|\Delta I_d|^{\text{eos}}$ instead. With this, the possibility that ΔR transformation is frequency dependent may be ruled out.

Hence, it has been proven that ΔR might not be a suitable indicator or parameter to gauge the influence of various frequencies on the “switching” hole-trap conversion due to the reduced trapping effect under high frequency. However, as reported in Chapter 4, it has been understood that when conversion of R into a more permanent defect form takes place, there would be a corresponding substantial increase in the gate tunneling current spectra. Based on these observations, the frequency dependence of R transformation could be easily studied by calculating the percentage of increase in the gate current, ΔI_g which is normalized to its fresh I_g as can be seen in Fig. 5-7.

First of all, Fig 5-7 and Fig 5-8 show the I_g evolution before and after applying an AC stress at 10, 000 Hz for two different cumulative stress time 1) 5000 s and 2) 10, 000 s at 100° C and 200° C respectively. It can be clearly seen that no bulk traps are generated at 100° C even after 10, 000 s of alternating stress $V_g = -2 \text{ V} / 0 \text{ V}$ at 10 kHz (conversion of “switching” hole-traps is not triggered). On the otherhand, there is an obvious increase in the SILC at 200° C for both cumulative stress of 5000 s and 10, 000 s. This indicates a substantial amount of oxide traps has been generated. The $\Delta I_g / I_{g@fresh}$ for each condition stated in Fig 5-7 and Fig 5-8 is summarized and compared in Fig 5-9.

Figure 5-7: (a) and (b) No significant increase in I_g is observed at a temperature of 100 °C for a particular frequency of 10,000 Hz, though the cumulative stress time has been increased from 5000 s to 10,000 s. V_g applied of stress/ recovery during AC is -2/ 0 V.

Figure 5-8: (a) An obvious increase in I_g is observed at a temperature of 200⁰ C for a particular frequency of 10, 000 Hz at 5000 s, (b) the gate leakage becomes more apparent as the cumulative stress time is increased from 5000 s to 10, 000 s, with all other conditions kept constant. V_g applied during stress/ recovery of AC is -2/ 0 V.

Figure 5-9: Shows $\Delta I_g / I_{g@fresh} (%)$ for both cumulative stress time of 5000 and 10, 000 s, at the temperatures of 100 and 200⁰ C respectively, keeping the frequency the same. It could be concluded that at a particular frequency, the hole-trapping transformation only takes place at high temperature and the conversion becomes severe with the increase in the cumulative stress time applied. It also shows that $\Delta I_g / I_{g@fresh} (%)$ seems to be a good indicator to gauge the impact of frequency on the *R* components.

Based on Fig. 5-9, when *R* transformation has been activated at 200⁰ C, the generated oxide traps become more apparent for the case where the cumulative stress is increased to 10, 000 s (~25% of increment is observed). These results clearly show that when a larger fraction of cyclic *R* is transformed into a more permanent form of defect, it would be reflected in the increase of $\Delta I_g / I_{g@fresh} (%)$. This also further supports that $\Delta I_g / I_{g@fresh}$ is a good indicator to gauge how frequency affects the transformation of “switching” *R*.

Figure 5-10: The gate spectra captured before and after the frequency stress at 200° C for various frequencies, ranging from 0.1 to 1 MHz. The impact of

frequency on the R transformation could be studied by extracting $\Delta I_g / I_{g@fresh}$ from the gate spectra.

To study the frequency dependence of this R conversion mechanism deeper, a temperature of 200° C is chosen and the frequency used ranges from 0.1 to 1 MHz. The gate bias, V_g alternates between -2/ 0 V during stress and a cumulative stress time of 10, 000 s is used for all experiments. The I_g evolution of the gate oxide (before and after stress) is monitored. Then, the $\Delta I_g / I_{g@fresh}$ are calculated to investigate the amount of oxide traps generated due to R conversion under the influence of various frequencies. Fig. 5-10 depicts the gate leakage current spectra for every chosen frequency, before and after the AC stress is exerted. Each experimental condition is repeated twice on two identical devices (fabricated together on the same sample) in order to improve the repeatability and accountability of the results obtained. The $\Delta I_g / I_{g@fresh}$ for all experiments are tabulated and summarized in Fig. 5-11 below.

Figure 5-11: Illustrates that $\Delta I_g / I_{g@fresh}$ (%) is unaffected by any frequency applied. It further implies that the transient hole-trapping transformation mechanism is independent of frequency.

It is clearly seen that $\Delta I_g / I_{g@fresh}$ (%) is independent of frequency as it does not show a steady increasing/ decreasing trend as a function of frequencies applied during experiments. Rather, it remains relatively constant and insensitive to the increasing frequencies. Though the slight "fluctuations" seen in the results might be questioned, the mean of $\Delta I_g / I_{g@fresh}$ (%) obtained for each individual frequency does not differ too much from one another. It is suspected that this slight "fluctuation" might be caused by the marginal variation in the devices' performance especially when they are not centered around the same location on the sample. Nevertheless, the results are still considered comparable and on the average, $\Delta I_g / I_{g@fresh}$ across all frequencies are estimated to be ~19 %. This

result infers that ΔR comprises of a group of defects which could be activated easily but would require a long time (exceeds our time window of study) to recover under DC quasi state stress.

Besides, we have repeated the experiment by maintaining all the conditions stated in Fig. 5-11, except for the temperature which is decreased to 160° C. We have also chosen similar SiON devices which are located next to each other. Similar to what has been observed in Fig. 5-11, the conversion of the cyclic R component into more permanent defect states is independent of frequency, so long as the temperature and cumulative stress time are kept constant as shown in Fig. 5-12. The smaller magnitude of $\Delta I_g / I_{g@fresh}$ (~10.5 %) as compared to that at 200° C (~19 %) is not coincidental. As the temperature is lowered to 160° C, a relatively smaller fraction of the “switching” hole-trap has been transformed and thus, causing a lesser amount of correlated oxide traps to be generated.

Figure 5-12: Similar experiment procedures performed in Fig. 5-11 has been repeated on another set of SiON devices which are located near to each other. All conditions are kept similar except for the temperature which is lowered to 160° C. It also depicts the frequency independence of the R transformation process.

5.3 Chapter Conclusion

In conclusion, the correlation between the “switching” hole-traps which are responsible for the V_t fluctuation during dynamic NBTI and the bulk (oxide) traps generated during Stress-Induced Leakage Current (SILC) has been further affirmed. Apart from the close interaction of ΔR with the corresponding increase in SILC which has been reported in Chapter 4, additional supporting evidences have been presented in this chapter. By using two distinct measurement methods, the Ultra-fast Switching Measurement (UFS) and SILC, we have provided results which show that both ΔR and $\Delta I_g / I_{g@fresh}$ have non-Arrhenius temperature dependence. The activation energies (E_a) extracted at

both temperature regimes seem comparable for ΔR and $\Delta I_g/I_{g@fresh}$. The E_a obtained at high temperature region is obviously smaller in magnitude. This is believed to be linked to the reduced energy barrier which is to be overcome when the charges transit from one to another charge state during a chemical reaction, especially in the presence of greater phonon vibration at high temperature. Additionally, the time exponent (n) for ΔR and $\Delta I_g/I_{g@fresh}$ as a function of temperature is also noticed to have similar increasing trend. Moreover, all these observations apply to the HfSiON p-MOSFETs, implying a common mechanism which dominates ΔN_{ot} and SILC across different gate oxide technologies/ processes/ materials. Another interesting observation is the value of n obtained for ΔR and $\Delta I_g/I_{g@fresh}$ (which is 0.22 – 0.47), is similar to the classical α observed in SILC. These results strongly conform to our inference of two different gate oxide degradations, NBTI and SILC sharing a common defect precursor, which would only surface under the conditions examined in Chapter 4. Lastly, we have also taken a step further to probe into the frequency dependence of this “switching” hole-trap transformation process. Our results show that the cyclic R transformation into permanent defect states mechanism is frequency independent. This study is vital because it helps us in understanding the behaviour of the transistor, especially when operating under moderately high temperature stressing conditions. Besides, it also proves that the pre-existing defect precursors which were neglected as they once deemed to be just a parasitic effect during NBT stress could result in a relatively permanent V_t shift in the transistors’ performance. All these new insights provoke us to

revisit some of the reliability models and to think deeper about the possible interdependence of different gate oxide reliability mechanisms, which will be presented in Chapter 6.

CHAPTER 6: THE INTERDEPENDENCE OF NEGATIVE-BIAS TEMPERATURE INSTABILITY (NBTI), ELECTROSTATIC DISCHARGE (ESD) AND TIME-DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

6.1 Introduction

Reliability mechanisms of CMOS transistors have been studied intensely throughout the years to understand their nature of failure in the gate oxide. However, these degradation mechanisms were studied separately and no/least attention has been placed on the interaction and interdependence of these reliabilities with one another. In Chapter 4, we discussed about the effect of high oxide field and high temperature stressing on the transient “switching” hole-trapping component, where part of the R was observed to constitute to the generated bulk traps. We have also discussed about the linear correlation of ΔR and the relatively permanent bulk traps generated during Stress-Induced Leakage Current (SILC) in terms of their non-Arrhenius temperature dependence and the similarity in the time exponent factor (n) in Chapter 5. Thus, it was reckoned that the increase phonon vibration due to high temperature would cause the oxygen vacancies to experience greater structural relaxation, besides causing an “upward-shift” of the trap-hole level. As a result, transformation of the oxygen vacancies from E'_{δ} -type to E'_{γ} -type would occur [158], [159], [174]. In this chapter, we will re-examine the interactions among Negative-Bias Temperature Instability (NBTI), Electrostatic Discharge (ESD)

and Time-Dependent Dielectric Breakdown (TDDB) based on our observations on the behavior of these “switching” hole-traps/ R components as discussed in the previous chapters.

Due to scaling, reliability mechanisms such as Time-Dependent Dielectric Breakdown (TDDB), Hot-Carrier Injection (HCI) and Bias-Temperature Instability (BTI) [175] are causing more severe impact on the device performances as a minima shift in the threshold voltage would have resulted in a significant reduction in the drain current and thus, causing the device to degrade over time. Another crucial degradation reported in the gate oxide along with the scaling effect is the Electrostatic Discharge (ESD) [81]. With scaling, devices are less susceptible to the very short but large magnitude pulses applied during ESD testing. Charged Device Model (CDM), which accounts for the common oxide damage in the industry, is known to emulate the fastest ESD event [82]. Hence, sub-nanosecond time-dependent characterization of gate oxide reliabilities and oxide breakdown mechanism are crucial for gate oxide modeling and lifetime prediction. It has been understood that ESD pre-stressing has worsen the subsequent NBTI degradation on thin oxide devices while NBTI pre-stressing has little dependence on the subsequent ESD performance [84] (refer Chapter 2, Section 2.7.1). However, it should be noted that the evidences/ explanations provided were less comprehensive as the effect of the applied NBTI pre-stressing conditions on the transient “switching” hole-trapping was not considered and studied carefully. Moreover, the ESD tests were performed using a TLP tester. Therefore, in order to capture the transient changes during

CDM, the gate oxides in our work are evaluated under the advance Very Fast Transmission Line Pulse (VFTLP) tester which is able to simulate CDM with a 1 ns pulse width.

In this chapter, the interactions of Negative-Bias Temperature Instability, Time-Dependent Dielectric Breakdown and Electrostatic Discharge analyzed under very fast transmission line pulsed (VFTLP) tester are outlined. The correlation among these degradation mechanisms is gaining much momentum recently with the aim to have a more accurate device lifetime prediction. We provide evidences which support the interdependence of these degradation mechanisms.

For the very first time, it is observed that NBTI pre-stressing will have an impact on ESD performance and TDDB lifetime **ONLY** when there is a substantial decrease in the R / “switching” hole-traps responsible for the threshold voltage fluctuation during dynamic NBTI. It is observed that devices which are stressed under high temperature, apart from having a decrease in R , would have a smaller magnitude in the breakdown voltage (V_{BD}) during ESD and shorter time-to-breakdown (t_{BD}) during TDDB in general. As a consequence, early breakdown is expected to occur, and this would in return, reduce the devices’ lifespan.

6.2 Experimental Details

Test devices (DUTs) were p-MOSFETs with p^+ polysilicon gate and 1.7 nm oxynitride (decoupled plasma nitrided) dielectric. Prior to ESD or TDDB tests,

the DUTs were subjected to various DNBTI test conditions. Case A, B and C were tests carried out to study the correlation between NBTI and ESD; while case 1, 2, 3 and 4 were tests performed to study the interaction between NBTI and TDDB. The details of each condition were as follow:

Case A, the ESD test was directly applied to pristine DUTs (i.e. the DNBTI phase was skipped).

Case B, the DUTs were first subjected to 40 DNBTI stress and relaxation cycles @ $100\text{ }^{\circ}\text{C}$ ($V_g = -2/0\text{ V}$, each lasting $1 \times 10^3\text{ s}$, i.e. 50% duty cycle) followed by ESD.

Case C, the DUTs were first subjected to 40 DNBTI stress and relaxation cycles @ $200\text{ }^{\circ}\text{C}$ ($V_g = -2/0\text{ V}$, each lasting $1 \times 10^3\text{ s}$, i.e. 50% duty cycle) followed by ESD.

Case 1, the TDDB test was directly applied to pristine DUTs (i.e. the DNBTI phase was skipped).

Case 2, the DUTs were first subjected to 40 DNBTI stress and relaxation cycles @ $100\text{ }^{\circ}\text{C}$ ($V_g = -1.8/0\text{ V}$, each lasting $1 \times 10^3\text{ s}$, i.e. 50% duty cycle) followed by TDDB ($V_g = -2.8\text{ V}$; $T = 100\text{ }^{\circ}\text{C}$).

Case 3, the DUTs were first subjected to 40 DNBTI stress and relaxation cycles @ $100\text{ }^{\circ}\text{C}$ ($V_g = -2.1/0\text{ V}$, each lasting $1 \times 10^3\text{ s}$, i.e. 50% duty cycle) followed by TDDB ($V_g = -2.8\text{ V}$; $T = 100\text{ }^{\circ}\text{C}$).

Case 4, the DUTs were first subjected to 40 DNBTI stress and relaxation cycles @ 220 °C ($V_g = -1.8/0$ V, each lasting 1×10^3 s, i.e. 50% duty cycle) followed by TDDB ($V_g = -2.8$ V; $T = 100$ °C).

Device degradation (in terms of ΔV_t extracted using a constant subthreshold drain current method from linear transfer curves measured by an ultra-fast switching method [134]) was monitored only during the DNBTI. The $|\Delta V_t|$ calculated during each DNBTI cycle probed the effect of T on the “switching” hole-trapping recoverable behavior. ESD tests were performed using Barth 4012 VFTLP tester (pulse width ~ 1 ns, voltage step of 0.5 V, DC voltage of 0.5V).

Dimensions of devices used were $10 \times 0.07 \mu\text{m}^2$ and $10 \times 0.24 \mu\text{m}^2$.

6.3 The Inter-relation of Negative-Bias Temperature Instability (NBTI) and Electrostatic Discharge (ESD)

Almost no comprehensive studies have been conducted to study the NBTI-ESD-TDDB correlation. One study has been reported on the NBTI-ESD interaction in 2007 [84]. This work showed that the ESD behavior has little dependence on NBTI pre-stressing. It was suspected that the carrier tunneling during IV measurement performance neutralized the oxide charge which was introduced during NBTI pre-stressing. Though this result seems to be born out in part of our observations (Fig. 6-4 and Fig. 6-5), this study is not conclusive enough. As mentioned earlier, the ESD performance was investigated using a TLP tester

which was not able to simulate extremely short pulses experienced by the device in real fabrication experiment [84]. Moreover, due to the statistical nature of trap generation, individual measurements may lead to inaccurate conclusion. Hence, a larger sample size is suggested for characterization in order to improve on the repeatability of the results observed. Apart, with the emergence of more evidences showing that the recoverable nature of V_t fluctuations during DNBTI could alter depending on the experimental conditions applied during NBTI tests, there is a need to reassess the impact of NBTI pre-stressing on the subsequent ESD degradation.

Fig. 6-1 shows the evolution of the transient hole-trapping as a function of DNBTI cycles at both 100° C and 200° C for case B and C. After NBTI pre-stressing, we went a step further to capture the leakage current of the devices for all categories A, B and C not by using SILC, but the ESD tester. 15 devices were measured for each category A, B and C. Fig. 6-2 summarizes the leakage current results for all devices. It is clearly shown that the leakage current level for categories A and B are almost similar. However, an average of ~15% reduction in R (Fig 6-1) for category C devices corresponds to an apparent increase in the leakage current (triangular symbol in Fig. 6-2).

Figure 6-1: Depicts the evolution of $|\Delta V_t|$ recovery per cycle or “switching” hole-trap as a function of the number of DNBTI cycles for varying DNBTI conditions B and C. R is decreased by $\sim 15\%$ (13 mV) at a higher temperature of 200°C (keeping V_g unchanged at -2.0 V). Result shown is obtained from a device’s measurement.

Figure 6-2: Leakage current measured before ESD using 0.5 V DC for fresh devices and after NBTI pre-stressing at 100 and 200°C .

Figure 6-3: Shows the IV characteristic curve. The bottom x axis is V_{DUT} and the vertical y axis is I_{DUT} . The top axis indicates the leakage evolution, done at a dc bias of 0.5 V. The leakage evolution plot represents the leakage changes at each incremental pulse current.

Firstly, before discussing about the effect of the “switching” hole-traps transformation process on the subsequent ESD performance, it will be necessary to have a careful look into the IV characteristic curve of the ESD results. Fig 6-3 illustrates how the breakdown voltages (V_{BD}) are obtained for all devices. In this work, “failure” is defined when there is an increase of at least 3-4 orders of magnitude observed in the leakage evolution. It could be seen that the leakage current changes from 10^{-11} to 10^{-6} A (~5 orders of magnitude) at I_{DUT} of ~0.60 A. Hence the corresponding “breakdown” voltage is extracted ≈ 3.40 V.

It is illustrated in Fig. 6-4 that the ESD breakdown voltages observed in category B devices (3.05 mV) are comparable with case A (3.10 mV), which has skipped NBTI pre-stressing. However, devices under case C have lower

breakdown voltages in general, with a mean $V_{BD} = 2.85$ V. It should be emphasized the smaller breakdown voltage of category C shown in Fig 6-4 is not coincidental but, is tightly linked to the decrease in R . Devices in case C have been stressed under high temperature, where the transient hole-trapping suffers from a 15% of reduction with a corresponding increase in the leakage current as depicted in Fig. 6-1 and Fig. 6-2. On the contrary, no indication of R decrease (remains constant) and no significant increase in the leakage current are observed for devices under category B (leakage level is comparable with the fresh devices). This further confirms that the reduced breakdown voltage (Fig. 6-4) and the substantially increased leakage current are unambiguously stemmed from the “switching” hole-trap transformation process, where part of the cyclic R has been rendered more permanent under high temperature.

Figure 6-4: Illustrates the impact of varying DNBTI conditions for 15 devices of case A, B and C on the V_{BD} . In general, the V_{BD} for condition C is lower than condition A and B, which gives an average of 2.85 V.

Therefore, there are two important observations evident in Fig. 6-1 till Fig. 6-4. One is the little dependence of ESD on NBTI pre-stressing when the “switching” hole-trapping mechanism remains constant during DNBTI; the other is the ESD performance *would have* dependence on NBTI pre-stressing only when the “switching” hole-trap transformation process is activated. This observation highlights and supports the notion that, there is likely a possible interaction between NBTI and ESD which could only be observed at high temperature.

Figure 6-5: (a) and (b) show the Weibull distribution of the impact of NBTI pre-stressing at 100⁰ C and 200⁰ C on the subsequent ESD performance. Despite after 40 DNBTI cycles of stress in case B, the expected V_{BD} is practically unchanged as compared to A (without NBTI pre-stressing). For case C, a 15 % reduction in R (Fig. 6-1) causes V_{BD} to decrease by 0.18 V (~6%). It should be mentioned that the voltage step size used was 0.1 V.

Next, the Weibull distribution for conditions A, B and C are compared in Fig. 6-5. In Fig. 6-5 (a), it is shown that NBTI pre-stressing does not lead to any significant change in the Weibull distribution of case B as compared to case A. On the otherhand, an obvious change in the Weibull behavior is observed for case C as documented in Fig. 6-5 (b). The expected breakdown voltage (V_{BD}) calculated for case A = ~ 3.18 V, case B = ~ 3.11 V and case C = ~ 3.0 V. It should be noted that the voltage step size used was 0.1 V. As a consequence, a vertical “step-like” distribution is obtained for case B, instead of a “smooth” distribution. Apart from this, the ΔV_{BD} of B as compared to A is found to be ~ 0.07 V (which is not more than the voltage step of 0.1 V). Therefore, with these taken into consideration, the expected V_{BD} of case B is considered comparable with A. As for devices under condition C, though the tiny difference (as compared to case A) might be questioned, its ΔV_{BD} which is calculated to be ~ 0.18 V ($\sim 6\%$), is already more than the voltage step/ range of 0.1 V. Moreover, case C is noticed to have a wider spread in the Weibull distribution with a gradient of ~ 14.81 as compared to case A and case B where their gradients are recorded to be ~ 22.25 and ~ 24.93 respectively. A smaller gradient of the Weibull distribution usually refers to the reduced number of traps required in forming a percolation path randomly. This result thus implies the presence of the permanent trapped holes in the gate oxide which arise from the transient hole-trapping transformation under high temperature stressing. As a result, this increases the probability of gate oxide breakdown to occur as the number of traps needed to form the breakdown path has now been reduced.

Therefore, the observed correlation of ΔR and the ESD featured in Fig. 6-2 till Fig. 6-5 has suggested that part of the bulk traps noticed during ESD are permanent trapped holes which stem from the conversion of R during DNBTI. The presence of these transformed permanent trapped holes is the main reason to obtaining a smaller V_{BD} and gradient for the Weibull distribution for devices in case C. This result also further indicates the hidden possibility of both ESD and NBTI sharing a same defect precursor, which means that they are interdependent and this could only be observed under certain operating conditions.

Figure 6-7: Illustrates the expected ΔR for case 3 and 4 which is extracted from the Weibull distribution. The extracted ΔR is found to be comparable with the statistical data shown in Fig. 6-6.

As illustrated in Fig. 6-6, the average of ΔR for case 2 and case 3 are 1.12 and 2.23 mV respectively. It means that least amount of R has become permanent defects. It is also important to note that even though the gate bias has been increased from -1.8 V to -2.1 V in case 3, the decrease in R is not substantial. A significant decrease in the transient hole-trapping is only noticed for devices in case 4 which is ~ 19.28 mV. The mean values for case 3 and 4 are comparable with the expected ΔR values extracted from the Weibull distribution depicted in Fig. 6-7, where the expected ΔR of case 3 and case 4 are ~ 2.52 and ~ 21.33 mV respectively.

Figure 6-8: (a) and (b) show the impact of conditions 2, 3 and 4 on the gate oxide lifetime t_{BD} . Despite after being subjected to 40 DNBTI cycles of -2.1 V stress in case 3, t_{BD} is practically unchanged as compared to those of case 1 (fresh device) and 2. For case 4, a more ~30 % reduction in R (refer to Chapter 4, Fig. 4-15) decreases t_{BD} (@63%) by nearly half. Interestingly, the generation of bulk traps that results in SILC and t_{BD} degradation is sensitive to the decrease of R (no effect when R remains constant).

Thereafter, the time-to-breakdown, t_{BD} for devices under categories 1-4 has been collected. The Weibull distribution plotted in Fig. 6-8 (a) shows the impact of the “switching” hole-trap transformation on TDDB. Interestingly, when R remains approximately constant, independent of SR cycling as observed in case 2 and 3 (the mean and expected ΔR values for devices under case 2 and case 3 are not more than 2.5 mV), no impact on the t_{BD} (@63%) is observed. Though there are only 4 devices in case 2, all 4 measurement points fall onto the distribution of the fresh devices perfectly. Hence, it is acceptable to assume that the t_{BD} for case 1, 2 and 3 are almost similar/ comparable. It should be noted that no corresponding increase in SILC is observed in case 2 and 3 (Chapter 4, Fig. 4-17). On the contrary, a severe degradation of $\sim 42\%$ in t_{BD} is however, evident upon a decrease in the transient hole-traps by a mere $\sim 30\%$ (Fig. 6-6) in case 4. One should be cautioned against the tendency to conclude that the decrease in the time-to-breakdown at 220°C might be caused by the increased interface state generation especially at high temperature where significant vibration could result in the increased generation rate of the dangling Si bonds at/ near the Si/ SiO_2 interface. As mentioned earlier, the gate stress during DNBTI has been increased to -2.1 V in case 3, no SILC generation and no impact on the TDDB lifetime are observed, despite the nonnegligible increase in P (interface state generation) after 40 DNBTI SR cycling (Chapter 4, Fig. 4-15). This infers that the interface states do not play a crucial part in the reduction of the TDDB lifetime. Therefore, the apparent impact on the TDDB lifetime is solely due to the presence of more permanent trapped holes which arise from

the decrease in the transient hole-trapping. Moreover, this result also corroborates our earlier observations in Chapter 4 that a substantial part of the interface degradation under NBT stress does not correlate with bulk (oxide) trap generation. Apart from that, Fig. 6-8 records the gradient for all cases. Similar to the ESD performance, case 4 shows the smallest gradient of ~ 1.66 and a wider spread in the Weibull distribution as compared to the other devices under conditions 1 (~ 2.0) and 3 (2.19). Thus, these observations again infer that a random percolation path could be formed more easily across the gate oxide as more trapped hole sites, originated from a fraction of the cyclic R during DNBTI at high temperature, have been generated in the bulk oxide. As a consequence, the device lifespan has been reduced!

Figure 6-9: The decrease in R in HfO₂ is also found to have an impact on the time-to-breakdown of the High- κ gate stack, just like the case of SiON device stressed under a high temperature in case 4.

A significant decrease in the TDDB lifetime, upon a decrease in the “switching” hole-traps, is also observed for devices with the High- κ TiN/HfO₂ gate stack as shown in Fig 6-9. Similar to that observed in SiON, the gradient seen for the case with high temperature DNBTI stressing is smaller. It suggests that the more permanent trapped holes, which could also be generated in the Hf-based oxides during DNBTI, could affect the TDDB lifetime of the High- κ devices. This further supports our postulation of a common bulk trap generation mechanism which occurs not only in the silicon-based oxides, but across various gate stack technologies.

Thus, based on these experimental results shown above, we re-emphasize, again, the importance of the permanent trapped holes which stem from R transformation at moderately high temperature that are still within the scope of interest of NBTI. With increased phonon/ lattice interaction at a higher temperature, greater structural change of the oxygen vacancy defects leads to more permanent bulk trap being generated. We infer that it is this transformation $E'_\delta \rightarrow E'_\gamma$ which reduces the number of traps needed to form a particular percolation path across the oxide. This transformation corresponds to a decrease in V_{BD} during ESD and t_{BD} during TDDB. This implies that NBTI, ESD and TDDB are interdependent and they arise from a common oxide defect precursor which is tightly linked to the transient “switching” hole-trapping component in NBTI.

Though our results obtained does not constitute direct proof of the Anode Hole Injection model, it does not conform to the Hydrogen Release model. M. Yatani has observed the correlation between released hydrogen from Si/ SiO₂ interface and gate oxide deterioration and has further inferred that the gate oxides degradation could be explained comprehensively by considering the hydrogen release from Si/ SiO₂ interface. This is, however, not seen in our results. First of all, the results presented in Chapter 4 shows that NBTI could not be explained by the R-D model (a hydrogen- transport model) due to the cyclical and constant nature of the transient V_t fluctuation during NBTI. Apart from this, our results strongly suggest that the release of hydrogen did not lead to any apparent bulk trap generation. Most importantly, the TDDB lifetime remains unaffected although the generation of interface states is further increased by $\sim 2\times$ in case 3 compared to case 2 (Chapter 4, Fig. 4-15). A substantial reduction in TDDB lifetime only occurs when there is a decrease in the transient hole-trapping, in which its precursors are suspected to be the oxygen vacancy defects. Hence, in light of these newly discovered insights, we believe that the hydrogen release might not play a role here and the gate oxide wear-out process may be more consistent with the AHI model, though further investigations are still needed for verification. From these results, it is also understood that the V_t fluctuation during DNBTI could not be modelled as a simple charging/ discharging, extrinsic effect at the pre-existing defect precursors anymore. An analytic capture/ emission time (CET) maps model has been proposed by T. Grassler to model a wide number of NBTI stress and recovery patterns which allowed a

more realistic lifetime extrapolation [207]. This model assumed the same capture/ emission time for a defect during the charging/ discharging process and less consideration was given to the tendency for these recoverable defect sites to become more permanent once they exhibited a significant structural relaxation upon capturing a hole. Unfortunately, our results have shown that the defect sites continue to evolve with time and structural change. Hence, it may not be possible to have a unique map which is invariant with time. Apart, many of the lifetime prediction data extracted in the industry still follows a linear extrapolation model by assuming all trapped sites are able to recover fully when the gate bias is terminated. This is, however, not so accurate as some of the precursors may become stable and permanent if the conditions performed were too stringent. Slight adjustments to these pessimistic conditions applied are therefore needed with the aim to have more accurate aging models and prediction of the transistors' performance. This is vital as it would help us to understand the behaviour of the transistors better by simulating the precursors' transformation process and to monitor the interdependence of various reliability mechanisms.

6.5 Chapter Summary

In conclusion, first experimental evidences are presented to show the participation of this transformation in the reduction of t_{BD} and V_{BD} . So far, *Ab-initio* simulations based on the oxygen vacancy defect ($E'_\delta \rightarrow E'_\gamma$) evolution seem to be able to explain the experimental observations. This work is crucial as it represents

an important milestone in the understanding of NBTI-ESD-TDDB interaction which is critical in developing more accurate circuit design strategies and fabrication guidelines across different gate oxide technologies.

CHAPTER 7: THE IMPACT OF LA-DOPING ON BIAS-TEMPERATURE INSTABILITY AND RECOVERY ON HIGH- κ / METAL GATE TRANSISTORS

7.1 Introduction

Due to its excellent thermal stability with Si, Hf-based oxides such as HfO_2 and HfSiO_x , have been regarded as promising candidates for High- κ dielectrics [114]. However, there are much more challenges to be addressed while implementing High- κ / metal gate stack into future CMOS technologies. Some eye catching obstacles reported are such as large V_t caused by the influence of High- κ / SiO_x interface dipoles [176], the high symmetric V_t 's for n- and p-transistors resulted from the Fermi-level “pinning” at the polysilicon/ High- κ interface [177] and the underestimation of the mobility of HfSiON devices which arises from transient charging during conventional characterization (which was later overcome by dielectric-stack optimization [178]). Threshold voltage of NMOS transistors with HfSiON gate dielectric is around 0.7 V [110] which is far away from the expected 0.25 V. Materials with various Fermi level energies were studied to achieve proper threshold voltage [92], [105]. Meanwhile, [110], [107], [108] tried to modulate threshold voltage (V_{TH}) by adding rare-earth metal into High- κ gate dielectric stack. A thin cap layer is inserted between the electrode metal and High- κ dielectric layer. Among various rare-earth metals, Lanthanum (La) has been reported as a strong candidate for n-MOSFETs because of its low V_{th} and therefore was introduced

to modulate the V_{th} by counteracting with the interface dipoles [176], [109]. In general, a La_2O_3 layer is capped on top of High- κ gate dielectric stack. During the high temperature Source/ Drain annealing, La_2O_3 capping layer which is electropositive would diffuse into the High- κ / SiO_2 interface to form a dipole during a high-temperature dopant-activation step. This results in the shifts of effective work function of the electrode [114].

Various models have been proposed to explain the V_t modulation resulted by the incorporation of La [107]- [112]. However, till date, the impact of La_2O_3 capping on the gate stack reliability (PBTI degradation) has yet to be studied and examined [117], [180]. Various measurement methods employed by different groups did not provide a fair ground of comparison on understanding the mechanisms of how and where the defects were generated in the presence of La [26], [89], [179]. There is still controversy on the impact of La on High- κ gate oxide reliability. It was suggested in [110] that the interface and bulk dielectric characteristics of the transistors could be improved by La doping. In [117], it was also demonstrated that La incorporation is effective in suppressing pre-existing defects. But, in contrary to that, [117] also showed the La incorporation caused the induced defect generation to be more sensitive to stress voltage and temperature. Hence, a more complete and comprehensive study on the impact of La incorporation on the High- κ / metal gate stack degradation should be carried out.

Du *et al.* has reported an abnormal slow recovery characteristic of La-doped HfSiON n-MOSFETs subjected to Bias-Temperature stress [120]. The drain current of the La-doped HfSiON n-MOSFETs were noticed to recover much more slowly than the undoped HfSiON and SiON n-MOSFETs. Two main observations of his study are as follows. 1) Consistency of La-related abnormal slow recovery is examined on various devices as a function of gate stress voltage and temperature. The abnormal recovery of La-doped transistors is proven to be independent of gate stress voltage, stress polarity, and also oxide thickness. 2) La introduces a new degradation mechanism which have a higher activation energy ($E_A = 0.26$ eV) and slower recovery than the conventional BTI mechanism ($E_A = 0.05$ eV). The activation energy (E_A) of BTI is shown to be different by adding La into the gate dielectric.

This observed new mechanism contributes significantly to n-MOSFET degradation in the high temperature regime ($> 100^\circ$ C) and is relatively permanent in comparison to the conventional BTI mechanism. Besides, Du *et al.* has also suggested that the La-related defects locates mainly inside the oxide instead of the oxide/ substrate interface as the interface states measured by charge pumping are much lesser than the total defects generated under BTI stress. This suggestion is further supported by the schematic of La atom distribution inside High- κ gate dielectric based on simulations which showed that the La-related defects are located around High- κ / IL interface [120]. A possible atomic model for the La-related defect is built to explain the abnormal slow recovery phenomenon.

Though Du *et al.* has done various investigations on the slow recovery by La incorporated in the n-MOSFETs, this distinctive effect of La on n-MOSFETs has been questioned due to some reports indicating that the degradation mechanism of Positive-Bias Temperature Instability (PBTI) is different from that of the Negative-Bias Temperature Instability (NBTI). The suggestion of NBTI driven mainly by the interface state generation while the former is related to electron-trapping in the High- κ layer has been widely accepted [86], [166]. At this point of time, it is therefore, crucial to (1) distinguish the defect nature of PBTI from the new degradation mechanism induced by La and (2) its irreversible nature.

In this chapter, Section 7.3 would discuss about the important observations made by Du *et al.*. Starting from Section 7.4 onwards, it consists mainly about our recent investigations and results on this La-induced degradation. We would particularly emphasize on how La incorporation into the HfSiON gate dielectric of n-MOSFETs affects the permanent shift in V_t , from a dynamic BTI experiment point of view, besides analyzing the role of BTI mechanisms on the abnormal slow recovery characteristic of the La-doped n-MOSFETs. Apart, the irreversible nature and polarity dependence of this additional bulk degradation mechanism introduced by La [120] is revisited by charging/ discharging the DUTs under both sweeping polarities. This investigation is then compared to the observations made by Cartier *et al.*, who has reported a dramatic recovery of

the SILC in HfO_2 n-MOSFETs during negative bias discharge by comparing the I_g - V_g measurements in both sweeping directions.

7.2 Experimental Details

Test devices (DUTs) were n-MOSFETs with TiN gate and La-doped HfSiON gate dielectric, fabricated via gate-first CMOS process. An ultrathin SiON interfacial layer (IL) existed between the Hf-based dielectric and the substrate. HfSiO_x , with an equivalent oxide thickness ~ 1.7 nm, was formed via atomic layer deposition (ALD) on an ultrathin SiON (< 1 nm) interfacial layer.

During high temperature rapid annealing step ($\sim 1000^\circ\text{C}$), a thin layer of LaOx (~ 0.3 nm) was deposited via atomic layer deposition (ALD) and was diffused into the HfSiO_x . For comparison, undoped p-MOSFETs fabricated on the same wafer were tested. The purpose is to validate that the observation on the La-doped n-MOSFET is not a consequence of any degradation caused by BTI mechanisms. Device degradation (in terms of ΔV_t extracted using a constant linear drain current method from linear transfer curves measured by an Ultra-Fast Switching method [134]) was monitored only during the Dynamic PBTI/NBTI. A 50% duty cycle of alternate gate stress and recovery between $-2/2$ V and 0 V were performed for 40 DNBTI/DPBTI cycles. The V_d was kept at $-0.1/0.1$ V. BTI experiments were carried out at a temperature range of 30 to 200°C . Dimensions of the undoped p- and La-doped n- transistors used were $1 \times 0.04 \mu\text{m}^2$, $2 \times 0.04 \mu\text{m}^2$ and $5 \times 0.04 \mu\text{m}^2$, unless stated otherwise.

7.3 Abnormal Slow Recovery of Transistors with La_2O_3

Studies have suggested that La-doped n-MOSFETs suffer from abnormal slow recovery. As reported by Du *et al.*, the universal recovery phenomenon has been observed on both conventional SiON devices and High- κ / metal gate devices [31], [72]. The author's investigation on the universal recovery of SiON and High- κ / metal has come to a consistent conclusion that the universal recovery characteristics was found to be independent of

- 1) Stress voltage V_G^S
- 2) Recovery gate voltage V_G^R
- 3) Whether the device is fresh or stressed (i.e. repeatability)
- 4) Gate oxide thickness

Fig. 7-1 (a) shows the recovery data which was captured after 100 s of NBTI stress over a range of gate voltages from -1.4 V to -2.6 V, at temperature 125° C. Gate recovery voltage and measurement voltage were set to V_{DD} (1 V). ΔI_d (the difference between I_d measured during recovery with the very first measurement point captured upon the removal of stress, $I_d @ 100\text{ s}$) is normalized to its first measurement point after stress was released for 1 ms. The drain current degradation and the absolute recovery upon the release of stress (for the same stress time) are noticed to increase with the applied stress voltage. Besides, Fig. 7-1 (b) shows the typical recovery behaviour as a function of recovery time. Interestingly, the drain current degradation $|\Delta I_d|$ of the conventional SiON p-MOSFET is recovering continuously as a function of recovery time at 125° C.

$$\text{Normalized } |\Delta I_d| = \frac{|\Delta I_d|}{|\Delta I_d| \text{ at } 100\text{s}} \quad (\text{Eqn. 7-1})$$

The ‘ $|\Delta I_d|$ at 100 s’ is the fastest point measured upon the removal of the gate bias, which reflects the real degradation (closest to) without any contamination of the recovery.

Figure 7-1: (a) Drain current degradation $|\Delta I_d|$ of conventional SiON p-MOSFET as a function of stress and recovery time at 125°C . Device was stressed for 100 s at various voltage [-1.4 V ~ -2.6 V] and recovered at V_{DD} for 100 s. (b) The typical recovery phenomena as a function of recovery time. Drain current degradation $|\Delta I_d|$ of conventional SiON p-MOSFET is continuously recovered as a function of recovery time at 125°C . [120]

As shown in Fig. 7-2, Du *et al.* has shown the universal recovery on conventional SiON devices. It is surprising to note that all the recovery data are similar to when the normalized $|\Delta I_d|$ is used. This is on contrary as it is generally known that the larger gate stress voltage induces larger degradation, followed by a faster recovery as depicted in the previous two figures, Fig. 7-1 (a), (b). The phenomena was also reported by S. Rangan [31] and T. Grassler [72], in which both conventional drain current sampling and On-The-Fly

measurement method were used. This result also indicates that the universal recovery follows a general trend in which the total degradation has log dependence on recovery time

The degradation can be modeled by the formula shown in Eqn. 7-2.

$$|\Delta I_d|(t) = 100\% - A * \log(t) \tag{Eqn. 7-2}$$

The model fits the data well as the straight lines are shown in Fig. 7-2.

Figure 7-2: Universal recovery data captured after 100 s of NBTI stress at various gate voltages [-1.4 V ~ -2.6 V] on conventional SiON devices. The recovery voltage is set at -1 V and the stress temperature is 125° C. $|\Delta I_d|$ is normalized to its first point. The data shows that recovery is independent of the amount of degradation. Recovery remains a constant at a given time. [120]

Figure 7-3: Recovery data at various gate recovery voltages $[-0.5 \text{ V} \sim -1.5 \text{ V}]$ as a function of recovery time in log scale. The data was captured after 100 s of stress at -2.6 V , 125°C on conventional SiON devices. $|\Delta I_d|$ is normalized to its first point. The data shows that recovery is independent of the recovery voltage. [120]

It is also proven that the recovery voltage does not affect the universal recovery as shown in Fig. 7-3. Du *et al.* has evident that transistor with La_2O_3 capping layer recovers slower in normalized recovery $|\Delta I_d|$ plots. To have solid and indisputable conclusion, experiments were done among a wide range of devices, including SiON & High- κ dielectrics transistors, thin and thick gate devices, n-type and p-type channel MOSFETs. Fig. 7-4 shows the long time recovery data captured after 100 s stress on three types of devices (1) High- κ transistors with La_2O_3 capping, (2) High- κ transistors without La_2O_3 capping, and (3) SiON transistors. The recovery behaviour is found to be similar for all devices, except transistors with La_2O_3 capping layer, 1-Hi κ -N-La.

Figure 7-4: Long time recovery data captured after 100 s of stress on three types of devices (1) High- κ transistors with La_2O_3 capping, (2) High- κ transistors without La_2O_3 capping, and (3) SiON transistors. The gate recovery voltage V_g^r is set to V_{DD} and the stress temperature is 125°C . The recovery speed is seen to be similar for all types of devices (slope: -0.13) except for transistors with La_2O_3 capping layer, 1-Hi κ -N-La (slope: -0.05). [120]

Figure 7-5: The remaining $|\Delta I_d|$ at various gate oxide thicknesses, ranging from 1.8 nm to 4.5 nm, as a function of recovery time. The recovery data is captured after 100 s of stress on devices with various dielectric thicknesses. Stress temperature is 125°C . [120]

Fig. 7-5 denotes the recovery data is independent of gate oxide thickness and possess almost similar recovery gradient, except transistors with La_2O_3 capping layer, 1-Hik-N-La. Hence, these results depicted in Fig. 7-4 and Fig. 7-5 draw a consistent conclusion that, the recovery speed is similar for all types of devices except transistors with La_2O_3 capping layer, 1-Hik-N-La. It also further implies that the abnormal slow recovery phenomenon is certainly related to the La_2O_3 capping layer of 1-Hik-N-La.

Figure 7-6: Consistent recovery data captured after stress at various gate voltages [± 1.4 V to ± 2 V] on transistors with/ without La_2O_3 capping, 1-Hik-N-La/ 1-Hik-P. The small V_g^s dependency of recovery does not affect the conclusion that BTI on 1-Hik-N-La recovers slower than BTI on 1-Hik-P. [120]

Fig. 7-6 shows the consistent recovery data captured after stress at various gate voltages [± 1.4 V to ± 2 V] on High- κ with La_2O_3 capping devices. The small V_g^s dependency of recovery does not affect to conclude that BTI on transistors with La_2O_3 capping layer, 1-Hik-N-La, recovers slower than BTI on transistors

without La_2O_3 capping layer 1-Hi κ -P. At measurement delay at 5 ms, the slope of the normalized $|\Delta I_d|$ vs. time in log scale is noticed to be around 5% per decade for 1-Hi κ -N-La and 15% per decade for 1-Hi κ -P.

Although Du. *et al.* has reported that La introduces a new degradation mechanism which is permanent in nature but yet different from the conventional BTI mechanisms [120], the effect of La on n-MOSFETs still remained questioned due to reports indicating that the degradation mechanism of Positive-Bias Temperature Instability (PBTI) is different from that of the Negative-Bias Temperature Instability (NBTI). The suggestion of NBTI driven by interface state generation while the former is related to electron-trapping in the High- κ layer has been widely accepted [86], [166]. At this point of time, it is therefore, crucial to distinguish/ separate (1) the involvement of BTI (especially PBTI) from the new degradation mechanism induced by La and (2) its irreversible nature/ gate polarity dependence.

7.4 The Role of Positive-Bias Temperature Instability (PBTI) and Negative-Bias Temperature Instability (NBTI) Mechanisms On the Abnormal Slow Recovery Induced by Lanthanum (La).

To address (1) as mentioned above, some results documented in Fig. 7-7 would be discussed further. It has been reported intensively that SILC is related to bulk trap (BT) generation [166]. In Chapters 4-5, we have shown that the transient “switching” hole-trapping responsible for the V_t fluctuation during dynamic NBTI share a common origin as the bulk traps generated during SILC in SiON p-MOSFETs [86], [166]. As outlined in these chapters, at high oxide field/temperature, a fraction of the cyclic R would be transformed into the permanent BT, resulting in a significant increase in the SILC. Similarly, Gao *et al.* reported a decrease in the R of the HfO₂ gate p-MOSFET, but at a lower temperature due to the suspected greater ionicity of the Hf-O bonds as compared to the amorphous SiON [153]. Analysis shows that a reduction in R happens in accordance with a substantial increase in the gate tunneling leakage current. However, a slightly different mechanism has been observed in the La-doped High- κ n-MOSFET, depicted in Fig. 7-8 (b).

To investigate (1), the ΔR and SILC characteristics of both La-doped n-MOSFETs and undoped p-MOSFETs are compared in Fig. 7-7 and Fig. 7-8. Both types of MOSFETs were first stressed for 40 dynamic BTI cycles ($E_{ox} = 8\text{MV/cm}$, $V_g \text{ relax} = 0\text{ V}$), followed by a I_g sweep from $\pm 1\text{ V}$ to 0 V to gauge the generation of bulk traps evolved from the transient charge trapping during BTI stress. This experiment was repeated over a range of temperatures.

Figure 7-7: Shows the decrease in R after subjecting the device to a 40 dynamic PBTI cycles of stress ($E_{ox} = 8\text{MV/cm}$, $V_g \text{ relax} = 0\text{ V}$) as a function of temperatures for both undoped and La-doped High- κ MOSFETs.

It can be clearly observed in Fig. 7-7 that HfSiON p-MOSFET experiences a decrease in the “switching” hole-traps at a temperature of 150°C ($\sim 5.4\text{ mV}$). For temperatures of 30 and 100°C , no apparent reduction is observed for the cyclic R component. Therefore, a corresponding increase in the I_g spectra (signifies bulk trap generation) has been noticed in Fig. 7-8 (a) at 150°C , whereas no significant increase in the gate leakage evolution has been observed at 100°C . These observations seem to support our earlier SiON experimental analysis provided in Chapters 4 and 5. Interestingly, likewise has been observed in the La-doped devices. On the contrary, a substantial generation of bulk traps has been observed for the La-doped n-MOSFETs in Fig. 7-8 (b) in the absence of R decrease (Fig. 7-7, $\Delta R \sim 0\text{ mV}$) at 100°C . The reduction of R only occurs at 150°C . At this temperature, the generation of bulk traps becomes more severe as reflected in the significant increase in the leakage current spectra.

Figure 7-8: (a) The evolution of I_g (shown is the I_g at the 40th cycle) of the undoped p-MOSFETs and (b) La-doped n-MOSFETs after 40 dynamic BTI cycles of stress ($E_{\text{ox}} = 8 \text{ MV/cm}$, $V_g \text{ relax} = 0 \text{ V}$) at different temperatures. A substantial increase in the I_g is observed at 100°C for the doped n-MOSFET even in the absence of ΔR .

Therefore, these results simply imply that the apparent increase in SILC of the doped transistors when the “switching” electron-trap transformation has not been activated (at 100° C) stems unambiguously from the presence of La itself. Apart, as the temperature increases to 150° C, the increase in the gate leakage is much more significant as compared to the SILC shown by the undoped p-MOSFETs at the same temperature. This may suggest that at 150° C, the severe degradation of the n-MOSFETs are contributed by 2 factors, 1) permanent defects evolved from the “switching” electron-trapping mechanism during PBTI and 2) La-induced defects; whereas the SILC observed for p-MOSFETs at 150° C is only a consequence of the “switching” hole-trapping evolution process.

At this point of time, though it is still early to infer that BTI mechanism plays a negligible role in the substantial generation of bulk traps for the La-doped n-MOSFETs, analysis may have ruled out the possible participation of the permanent charge states originated from the transient electron-trapping during PBTI in the degradation of doped n-MOSFETs, especially at lower temperature (< 100° C). This indicates the presence of an additional degradation induced by La-doping in the n-MOSFETs.

To probe deeper into (1), the comparison of the evolution of gate leakage current, I_g at various E_{ox} and T for both the La-doped n-MOS capacitors and undoped p-MOS capacitors is done in Fig. 7-9. After every 2000 s of constant

V_g stress (+/- 2 V), I_g was measured by sweeping V_g from +1.5 V to -1.5 V and vice-versa. Thereafter, the

Figure 7-9: Undoped High- κ / metal gate p-MOSFETs stressed at a constant voltage of (a) $V_g = -2$ V (NBT) (b) $V_g = +2$ V (PBT). After every 2000 s of constant V_g stress, I_g was measured by sweeping V_g from +1.5 V to -1.5 V or vice-versa. This test sequence was repeated up to a cumulative stress time of 40,000 s (E_{ox} applied were comparable for all transistors). Similar experimental

conditions were done on a La-doped high- κ / metal gate n-MOSFET (c) $V_g = -2$ V (NBT) (d) $V_g = +2$ V (PBT) to compare the effect of (with/ without) La on the gate leakage tunneling spectra.

Figure 7-9: La-doped High- κ / metal gate n-MOSFETs stressed at a constant voltage of (c) $V_g = -2$ V (NBT) (d) $V_g = +2$ V (PBT). After every 2000 s of constant V_g stress, I_g was measured by sweeping V_g from +1.5 V to -1.5 V or vice-versa. This test sequence was repeated up to a cumulative stress time of 40,

000 s (E_{ox} applied were comparable for all transistors). (a)- (d) are compared to study the effect of (with/ without) La on the gate leakage tunneling spectra.

Figure 7-10: $\Delta I_g (I_g @ 40,000 \text{ s} - I_g @ \text{fresh}) / I_g @ \text{fresh}$ was calculated for both undoped p-MOS and La-doped n-MOS capacitors. (a) La-doped n-capacitors track a higher I_g degradation independent of V_g applied regardless of NBT/ PBT stress. (b) Higher degradation is always observed for La-doped n-capacitors across different temperatures regardless of NBT/ PBT stress.

constant voltage stress was resumed. This test sequence was repeated up to a cumulative stress time of 40,000 s. (E_{ox} applied were comparable for all capacitors). It can be observed in Fig. 7-9 (c), (d) that for a particular electric field applied, the La-doped capacitors always mark a more severe degradation in the gate leakage current evolution as compared to the undoped capacitors as CVS progresses. $\Delta I_g (I_g @ 40,000 \text{ s} - I_g @ \text{fresh}) / I_{g,\text{fresh}}$ is calculated for both undoped p- and La-doped n-capacitors as depicted in Fig. 7-10. It can be clearly observed in Fig. 7-10 (a) that significant degradation experienced by the La-doped n-capacitors is constantly observed at all NBT and PBT stress voltages. This might imply that higher degradation rate recorded in the La-doped capacitors is independent of V_g applied. The same observations also apply for different temperatures. Fig. 7-10 (b) illustrates that by varying the experiment temperatures (with all other conditions kept constant), the La-doped capacitors always show more severe degradation as compared to the undoped capacitors. This strongly suggests that regardless of PBTI or NBTI stress being applied, the incorporation of La has increased the degradation rate of the capacitors, also implying that the possibly different PBTI and NBTI mechanisms do not play a major role here. Hence, Fig. 7-9 and Fig. 7-10 clarify the increased degradation rate in the n-capacitors is noticeably due to La-doping and is independent of BTI mechanisms. On this basis, we believe that La introduces a new degradation mechanism which is different in nature from the conventional BTI mechanism as mentioned in [120]. Furthermore, with R transformation activated at 150° C for both n- and p-capacitors (ΔR shown in Fig. 7-7), the larger amount

of degradation marked by the La-doped oxides under both PBT and NBT stress seems to support our earlier speculation that in addition to the permanent states which evolved structurally from the transient charge trapping, La-induced defects also constitute to the permanent degradation. As a result, the La-doped devices degrade faster as compared to the undoped p-capacitors.

7.5 The Irreversible Nature of the Abnormal Slow Recovery in La-Doped n-MOSFETs.

Next, Fig. 7-11 examines (2) the irreversible nature of the La-induced degradation observed in the doped n-MOSFETs. A temperature of 100° C is chosen because no ΔR transformation would be activated at this temperature (refer Fig. 7-7). Thus, any degradation in the SILC observed would be attributed mainly to the presence of La. It is important to note that the SILC does not encounter complete recovery after “discharging” it with a negative V_g in the range of $1.5 \text{ V} < V_g < -1.5 \text{ V}$ as pictured in Fig. 7-11. Fig. 7-11 (a) shows the I_g evolution when the doped n-MOSFET was swept from $1.5 \text{ V} < V_g < -1.5$ (“downward”) after 2000 s of constant voltage stress at 2 V. After the discharge at -1.5 V for 9 s, a second I_g - V_g was measured by sweeping the doped n-MOSFET in the opposite direction back to 1.5 V (“upward”) as evident in Fig. 7-11 (b). Thereafter, this test sequence was repeated up to a cumulative stress time of 20, 000 s. It should be mentioned that the SILC does not relax back to its pre-discharge level.

Figure 7-11: The evolution of I_g in both sweeping directions (a) $1.5 < V_g < -1.5$ V (down sweep) (b) $-1.5 < V_g < 1.5$ V (up sweep) for the La-doped n-MOSFET. Under the influence of La, the I_g degradation is shown to be irreversible and have less gate polarity dependence. Negligible I_g is observed to recover despite a 9 s discharge at -1.5 V.

Figure 7-12: The evolution of I_g in both sweeping directions (a) $-1.5 < V_g < 1.5$ V (up sweep) (b) $1.5 < V_g < -1.5$ V (down sweep) for the undoped p-MOSFET. The I_g spectra remains practically unchanged as no hole-trapping transformation has been activated at 100°C (refer Fig. 7-7).

The remarkable reversibility characteristic of the SILC in the n-MOSFETs as reported in [208] is not observed here. Cartier *et al.* has observed a dramatic recovery of the SILC in HfO₂ n-MOSFETs during negative bias discharge by comparing the I_g - V_g measurements in both sweeping directions. This strong gate-polarity dependence was thus, suggested to be due to the charge trapping in the newly generated shallow defects, presumably oxygen vacancy as proposed by Cartier *et al.* Hence, the non-negligible fraction of the permanent degradation left unrecovered in Fig. 7-11 (b) is undeniably induced by the incorporation of La into the gate oxide. It is important to note that the negligible portion of the I_g which is recovered after the discharge at -1.5 V as depicted in Fig. 7-11 (b) might be due to the recovery of some transient stress-induced charges. Nevertheless, this does not affect the conclusion that

Figure 7-13: (a) Local network of HfO₂, showing a substitutional La atom in an “unrelaxed” state, due to rapid cooling during spike annealing. (b) Applied electric field and thermal energy (during Bias-Temperature stress), coupled with the greater ionicity of the La-O bond, induce local structural relaxation via relative displacement of the La and O atoms. The resultant formation of $V_o - I_o$ Frenkel pairs induce relatively deep electronic trap levels (below the Si valence band edge) as illustrated in Fig. 7.15. [120]

La-induced degradation is irreversible. This experiment sequence was repeated on the undoped p-MOSFET as a comparison to the doped n-MOSFET. Fig. 7-12 denotes that no increase in SILC is observed for the undoped p-MOSFET as no ΔR conversion has been activated at 100° C. This again implies that for the undoped HfSiON p-MOSFET, the permanent trapped-hole sites manifested in SILC are mainly contributed by the ΔR evolution. This corroborates our results shown earlier in Fig. 7-7, Fig. 7-8 and Chapter 4.

All these analysis conform to the conclusion made by Du *et al.* that La introduces an additional permanent degradation. By making a step further to study the possible role played by BTI in this La-induced mechanism, we show that the nature of this additional degradation is of different origin as compared to the conventional BTI mechanisms. Solid experimental evidences have been presented to support the notion that this additional mechanism induced by La is irreversible and has less gate-polarity dependence.

An interim explanation based on the structural relaxation of the oxygen vacancy defects, a major source of electronic traps in the La-doped n-MOSFETs which was proposed earlier in [120] seems to be able to explain our experimental results well. Fig. 7-13 shows the simulation data of La impact on pure HfO₂ crystal without involving Si and N atoms. The PWSCF code of the QUANTUM ESPRESSO package, which based on the density-functional theory within the

generalized gradient approximation, is used in the simulation. Pseudo potentials are used to describe the electron configurations for Hf, O, and La.

In order to describe the HfO_2 structure, a bulk super cell following monoclinic crystal structure is constructed. Each cell contains 96 atoms, among which 32 are Hf atoms and 64 are O atoms. In order to inspect the impact of La, one Hf atom is replaced by La atom as documented in Fig. 7-13 (a). It should be mentioned that in real devices, the High- κ material used is HfSiON with La_2O_3 capping. However, since the abnormal slow recovery of n-MOSFETs is very much likely due to the La-related defects as evident in our experiments, illuminating Si, N atoms would not have any impact on the validity of the simulation. As shown in Fig. 7-13 (a), the local bonding network of a substitutional La atom is strained, since the La-O bond is intrinsically longer than the Hf-O. Under a combination of high electric field and temperature exerted onto the oxide (BTI conditions), greater structural relaxation which is enhanced by the greater ionicity of the La-O bond, would happen as illustrated in Fig. 7-13 (b). As a result, this relaxation leads to a substantial reduction in the energy of the local bonding network as shown in Fig. 7-14, causing it not possible for the reversed process (strained La-O bond to recover) to happen upon the removal of BTI stress. Hence, O vacancy-interstitial pairs with deep energy states in the HfSiOx bandgap [117], [181] which are relatively permanent in nature, are formed due to the incorporation of La.

Figure 7-14: First-principles simulation reveals a non-negligible lowering of the local network energy, rendering the structural relaxation process irreversible (i.e. defect formation is permanent). [120]

Based on these simulation results, we speculate that the greater ionicity of the La-O bonds and the apparent reduction in the energy of the local bonding network have resulted in the abnormal slow recovery and irreversible nature of the La-doped oxides. Moreover, the suspected trapping process of the electrons in a La-doped HfSiON n-MOSFET has also been illustrated in Fig. 7-15. The slower recovery speed in the presence of La is inferred to be due to the formation of some stress-induced defect pairs which have relatively deep energy trap level. Nevertheless, much more work has yet to be done to establish the atomic origin of the defect and to unlock the mechanism of La on the neighboring atoms.

Figure 7-15: (a) A simple schematic energy band diagram showing the trapping process of the electrons at the stress-induced $V_o - I_o$ Frenkel pairs during PBTI. (b) Since formation of the $V_o - I_o$ Frenkel pair is permanent and the I_o level is relatively deep, recovery speed of the La-doped n-MOSFETs is reduced significantly. [120]

7.6 Chapter Summary

In this chapter, we confirmed the abnormal slow recovery characteristic of La-doped HfSiON n-MOSFETs subjected to Bias-Temperature stress. The La-induced abnormal slow recovery to be a consistent phenomenon at various V_G^S , stress voltage polarity, V_G^R , dielectric materials and gate oxide thicknesses which was observed by Du *et al.* is discussed in Section 7.3. In Section 7.4, we present experimental evidences showing that this additional degradation mechanism in the presence of La has less gate-polarity dependence. Its irreversibility behaviour implies that the degradation is permanent. We also show that the nature of this additional degradation is of different origin as compared to the conventional BTI mechanisms. A possible atomic model for the La-related defect discussed by Du *et al.* is able to explain these experimental observations.

CHAPTER 8: CONCLUSION AND RECOMMENDATION

8.1 Conclusion

In this thesis, a detailed study mainly on the evolution of the transient “switching” hole-trapping observed during dynamic Negative-Bias Temperature Instability (NBTI) in the ultrathin SiON has been presented. With the emergence of fast measurement methods, recovery effect due to measurement delay during NBTI tests could be minimized drastically. The Ultra-Fast Switching method employed in this project is able to capture the transient charging/ discharging phenomenon during dynamic NBTI tests. With this, it has been observed that the hole-trapping possesses a “non-RD” behaviour. The threshold voltage recovered upon the release of gate bias (R) is shown to be cyclical and constant in nature as the SR cycling progresses. This characteristic does not conform to the hydrogen-transport model which predicts that R should decrease with the number of dynamic NBTI cycles. In this project, the nature/ physical origin of R has been probed further under high oxide field and temperature stressing. Analysis shows that there is a tendency for R to decrease under such conditions. It should be mentioned that the decrease of R is always evident in conjunction with a substantial increase in the gate tunneling leakage current (which signifies bulk (oxide) trap generation). We infer that under high oxide field or temperature stressing, a portion of the hole-trapping mechanism losses its recoverable nature. This further implies that a fraction of the transient

hole-trapping mechanism would structurally evolve into more permanent defect states. Apart, analysis also proves that interface state generation has a negligible role to play in the generation of these bulk traps observed during Stress-Induced Leakage Current (SILC). Similar observations apply to HfO_2 and HfSiON gate dielectrics. It is suspected that the greater ionicity of the Hf-O bonds in HfO_2 results in the R transformation to occur at lower temperatures ($< 100^\circ \text{C}$) as compared to that of SiON and HfSiON oxides. Nevertheless, this similarity of the tendency for the transient charge trapping to become permanent suggests a common mechanism for bulk trap generation generic across different gate stack technologies. The exact mechanism for the observed hole-trap transformation is unclear since the atomic nature of the defect is not yet established. But the tendency for trapped-hole sites to become more permanent at high temperatures may be broadly explained by the expected increase of structural relaxation following bond breakage (or hole capture) due to enhanced phonon interaction. An interim explanation may also be based on the oxygen vacancy defect, which is a common source of hole-traps in the gate oxide [169]. At a high temperature, the structural relaxation associated with the capture of hole at the oxygen vacancy defect [172] is expected to increase, rendering the trapped-hole site more permanent and could therefore be sensed by the slow I_g measurement when $E'_\delta \rightarrow E'_\gamma$ transformation occurs.

The linear correlation between ΔR and SILC has been established further. Strong evidences have been presented to show that both have non-Arrhenius temperature

dependence. Moreover, the time exponent (n) of both ΔR and SILC are noticed to be comparable. Interestingly, n (0.21-0.45) is found to be strikingly similar to the classical α value reported in various SILC studies. This result enhances our speculation that both dynamic NBTI and the generated bulk trap during SILC share a common defect origin. Most importantly, this newly discovered R transformation is observed to be frequency independent. This result is crucial as it marks a new understanding of the physical mechanism in the gate oxides. It also implies that hole-trapping mechanisms observed during NBTI, which were once thought to be just simple charging/ discharging of the pre-existing oxide defects and thus, deemed as irrelevant to NBTI, have a definite and significant role on long term device parametric drifts.

In the past, gate oxide reliabilities have been studied independently. However, in order to examine the possibility of different reliability mechanisms originating from a common defect precursor, the interdependence of various gate oxide reliabilities has been reviewed and reassessed again. It is shown that when R decreases, the breakdown voltages (V_{BD}) of Electrostatic Discharge (ESD) are generally smaller. The same applies to the time-to-breakdown (t_{BD}) during TDDB, where the lifetime of the devices is evident to decrease significantly by $\sim 42\%$ upon a mere $\sim 30\%$ reduction in R . The same applies to the t_{BD} of the HfO_2 oxides. Besides, a wider spread in the Weibull distribution (smaller gradient) of the V_{BD} and t_{BD} is always evident in the presence of R transformation. The smaller gradient of the Weibull distribution usually means that the number of traps needed to form a random

percolation path has been reduced. This implies the existence of some permanent trapped-holes evolved during high temperature DNBTI stressing. The impact of R decrease on ESD and TDDB further indicates the interactions among these reliability mechanisms. This supports the notion that they originated from a common oxide defect precursor, which arise from the transient hole-trapping. Apart from this, it should be mentioned that hydrogen release is noticed to play a negligible role in the gate oxide wear-out process. Our results seem to be more consistent with the Anode Hole Injection model, though the role of hydrogen release still warrants further investigations. With this, it is thus understood that it might not be possible to assume that all defect sites experience the same capture/emission time during the trapping/detrapping process. They are not invariant with time. These trapped-hole sites have been shown to evolve structurally with high oxide field/ moderately high temperature stressing. Considerable attention should be placed on the R component as its transient nature could pose significant challenges to both device and circuit reliability assessment and modeling.

The introduction of rare-earth material, Lanthanum (La) into the High- κ / metal gate stack was reported to induce a new degradation mechanism by Du *et al.* in [120]. An abnormal slow recovery characteristic was reported in La-doped HfSiON n-MOSFETs subjected to Bias-Temperature stress. The La-induced abnormal recovery was proven to be a consistent phenomenon at various V_G^S , stress voltage polarity, V_G^R , dielectric materials and gate oxide thicknesses. Though this additional new degradation mechanism was reported to have much higher activation

energy ($E_{AH} = 0.26\text{eV}$) and slower recovery than the conventional BTI mechanism ($E_{AL} = 0.05\text{eV}$), the role played by BTI mechanism in the La-induced degradation was still questioned. In this thesis, we focus mainly on investigating the involvement of PBTI/ NBTI on the La-doped oxides from a dynamic BTI point of view. A substantial increase in the SILC in the absence of R transformation at 100°C has suggested that the severe degradation observed in the La-doped devices is solely due to the effect of La itself. Analysis also shows that the possibly different PBTI and NBTI mechanisms do not play a major role in the La-induced degradation. Solid experimental evidences have been presented to support the notion that this additional mechanism induced by La is irreversible and has less gate-polarity dependence. All these results further enhance the conclusion made by Du *et al.* in [120]. Lastly, the atomic model for the La-related defect which was built earlier in [120] seems to be able to explain our experimental results.

8.2 Recommendation

This newly discovered transient “switching” hole-trapping evolution in SiON oxides has been studied intensively in this project. Its significance on the transistors’ performance and aging modeling has also been discussed and highlighted in this thesis. All the results obtained were done using electrical measurements. Simulations were done to assist us in understanding and explaining the experimental results to a certain extend. Although this work has brought us a step closer into understanding the gate oxide wear-out mechanism, there are much

more work to be covered in search of the physical structure of the common defect precursor. Below are some suggestions for possible future work:

- Research in small area devices is gaining more and more momentum in these recent years. In general, the small area transistor's behaviour is known to differ very much from big area transistor. Therefore, small area devices with only a few distinct traps in the oxide could be used to study the nature of R and its transformation process. It would be interesting to examine the behaviour of individual traps upon activating the R transformation.
- It is shown that NBTI mechanism does have a nonnegligible impact on the V_{BD} and t_{BD} upon activating the transient R evolution into a more permanent form of defect in SiON. Since our analysis has also shown that BTI mechanisms do not play a major role in the degradation of the La-doped devices, further investigations could be done to probe the effect of La-doping on V_{BD} , t_{BD} and other oxide degradations.
- With the existence of Ultra-Fast Switching measurement, it may worth the effort of studying the effect of mechanical stress on BTI mechanisms from a dynamic stressing point of view, besides taking the R conversion into consideration.

PUBLICATIONS

Journal Publications

- 1) A. A. Boo, D. S. Ang, Z. Q. Teo, and K. C. Leong, "Correlation Between Oxide Trap Generation and Negative-Bias Temperature Instability", *IEEE Electron Dev. Lett.*, **33**, p. 486 (2012).
- 2) A. A. Boo and D. S. Ang, "Evolution of Hole Trapping in the Oxynitride Gate p-MOSFET Subjected to Negative-Bias Temperature Stressing", *IEEE Trans. Electron Dev.*, **59**, p. 3133 (2012).
- 3) A. A. Boo, D. S. Ang, Z. Q. Teo, and K. C. Leong, "A Newly Discovered Non-Arrhenius Temperature Dependence and Frequency Independence of the "Switching" Oxide-Trap Transformation in 65 nm SiON", *IEEE Electron Dev. Lett.*, submitted (2012).
- 4) A. A. Boo, D. S. Ang, and G. A. Du, "An Additional Bulk Degradation Observed During Dynamic Bias Temperature Instability In The La-Doped n-MOSFETs", *IEEE Electron Dev. Lett.*, submitted (2013).
- 5) A. A. Boo, D. S. Ang, C. W. Kang, and W.H. Lai, "On the Interdependence of NBTI, ESD and TDDB under the Effect of Temperature", *IEEE Electron Dev. Lett.*, submitted (2013).
- 6) D. S. Ang, A. A. Boo, and Y. Gao, "Negative-Bias Temperature Instability – Insight from Recent Dynamic Stress Experiments", *ECS Transactions*, p. 73-85, 2012. (Invited paper)
- 7) T. J. J. Ho, D. S. Ang, A. A. Boo, Z. Q. Teo, and K. C. Leong, "Are Interface State Generation and Positive Oxide Charge Trapping Under Negative-Bias Temperature Stressing Correlated or Coupled?", *IEEE Trans. Electron Dev.*, **59**, p. 1013 (2012).
- 8) Y. Gao, D. S. Ang, A. A. Boo, and Z. Q. Teo, "On the Dynamic NBTI of the HfO₂ and HfSiON p-MOSFET", *Microelectron. Eng.*, **88**, p. 1392 (2011).

Conference Proceedings

- 1) A. A. Boo, D. S. Ang, Z. Q. Teo and C. M. Ng, "Effect of Positive Gate Stressing on The Recoverable Component of Negative-Bias Temperature Instability," in *Proc. SSDM 2010*, Tokyo, Japan, Sep. 22-24, 2010. (Oral presentation)
- 2) D. S. Ang, A. A. Boo, and Y. Gao, "Negative-Bias Temperature Instability – Insight from Recent Dynamic Stress Experiments", *ECS Transactions*, p. 73-85, 2012. (Invited paper)
- 3) Y. Gao, A. A. Boo, Z. Q. Teo, and D. S. Ang, "On the Evolution of the Recoverable Component of the SiON, HfSiON and HfO₂ P-MOSFETs under

Dynamic NBTI”, in *Proc. Intl. Reliab. Phys. Symp.*, p.943, 2011. (Poster presentation)

4) Z. Q. Teo, A. A. Boo, D. S. Ang, and K. C. Leong, “On the Cyclic Threshold Voltage Shift of Dynamic Negative-Bias Temperature Instability”, in *Proc. Intl. Reliab. Phys. Symp.*, p. 935, 2011. (Poster presentation)

5) Y. Gao, D. S. Ang, and A. A. Boo, “On the Dynamic NBTI of the HfO₂ and HfSiON p-MOSFET”, in *Proc. 17th International Conference on Insulating Films on Semiconductors*, vol. 88, p1392-1395, 2011. (Oral presentation)

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