Design of power management circuits for fully on-ship applications

Tan, Xiaoliang

2015

Tan, X. (2015). Design of power management circuits for fully on-ship applications. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/64897>

<https://doi.org/10.32657/10356/64897>

**DESIGN OF POWER MANAGEMENT CIRCUITS FOR
FULLY ON-CHIP APPLICATIONS**

TAN XIAO LIANG
**SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING**
2015

DESIGN OF POWER MANAGEMENT CIRCUITS FOR FULLY ON-CHIP APPLICATIONS

TAN XIAO LIANG

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2015

ACKNOWLEDGMENTS

I would like to take this opportunity to thank my supervisor, Associate Prof. Chan Pak Kwong, for his great help and guidance throughout the PhD research. He taught me a lot of important fundamental knowledge, provided many useful comments and suggestions during the course, and trained me many important skills to do research. He has been very generous to share his ideas, time and personal resources with me. Without his constant guidance and help, this work would not have been possible.

I am also grateful to Dr. Chong SauSiong, a PhD graduate of Prof. Chan. Without his support and discussions during my chip design and chip measurement, my research would not have been so smooth.

I would also like to express my gratitude to MediaTek, Singapore for providing the PhD scholarship and the chip fabrication. Without its support, it would be hard for me to start and continue my research in IC design.

My gratitude also extends to the technical staffs in VLSI, IC design I and II laboratory, Virtus for the uncountable support especially for the lending and usage of equipment.

Finally, I would like to thank my wife and my parents for their love, support, encouragement and sacrifice. I dedicate this thesis to them.

TABLE OF CONTENTS

Acknowledgments.....	i
Table of Contents.....	ii
Abstract	v
List of Figures	vii
List of Tables.....	xi
List of Glossary	xiii
Chapter 1 Introduction	1
1.1 Motivations	1
1.2 Objectives.....	13
1.3 Contributions.....	14
1.4 Organization of the Thesis.....	16
Chapter 2 Threshold Monitoring Circuit	17
2.1. Introduction	17
2.2. Review of V_{TH} Sensor Designs.....	19
2.2.1. Ferreira's V_{TH} Sensor [62]	19
2.2.2. Ueno's V_{TH} Sensor [63]	21
2.2.3. Lee's V_{TH} Sensor [65]	23
2.3. Proposed V_{TH} Sensor [85]	25
2.3.1. Nonlinear Temperature Effect of V_{GS}	25
2.3.2. Circuit Implementation	26
2.3.3. Working Principle	28
2.3.4. Results and Discussions	32
2.3.4.1. Measurement Setup and Calibration Procedure	32
2.3.4.2. Measurement Results	33
2.3.4.3. Scalability and Process Variations	35
2.3.4.4. Performance Comparison.....	37
2.4. Summary.....	40
Chapter 3 Review of LDO Regulators.....	41
3.1. Conventional Output Capacitor LDO (OC-LDO) Regulator Structure.....	41
3.2. Dynamic Biasing and Current Boosting in LDO Regulators	44
3.3. Output Capacitorless LDO (OCL-LDO) Regulator	45

3.3.1.	Single-Stage Error Amplifier Plus Power Transistor OCL-LDO Regulator Topology	45
3.3.2.	Multi-Stage Error Amplifier Plus Power Transistor Regulator Topology	47
3.3.3.	Flipped-Voltage-Follower (FVF) Based OCL-LDO Regulator Topology	49
3.4.	Layout Techniques	51
3.4.1.	Transistor Matching	51
3.4.2.	Power Transistor Layout	52
3.4.3.	Metallization	55
3.5.	Summary	58
Chapter 4 Wide Load Capacitance Range OCL-LDO Regulator:		
Type-I.....	59	
4.1.	Introduction	59
4.2.	Circuit Topology.....	61
4.3.	Stability and PSR Analysis and Discussions	63
4.3.1.	Small-Signal Model and Transfer Function	63
4.3.2.	Poles and Zero Locations	65
4.3.3.	Phase Margin under Different C_L	72
4.3.4.	Damping Factor and Gain Margin under Different C_L	73
4.3.5.	Sizing of Dual Miller Compensation Capacitors	78
4.3.6.	Power Supply Rejection Analysis.....	80
4.4.	Simulation Results and Performance Comparison	85
4.4.1.	Simulation Results and Discussions.....	85
4.4.2.	Performance Comparison.....	87
4.5.	Summary	90
Chapter 5 Wide Load Capacitance Range OCL-LDO Regulator:		
Type-II	91	
5.1.	Proposed Negative Current Feedback Technique.....	91
5.2.	Proposed Weighted Current Feedback Technique	94
5.3.	Dynamic Impedance Reduction and Small-Signal Model for WCF LDO Regulator.....	98
5.4.	Stability Analysis and WCF Design Strategy	101
5.4.1.	Design Strategy of β using Routh–Hurwitz Stability Criterion	102
5.4.2.	Pole and Zero Locations	108
5.4.3.	Phase Margin (PM) under C_L and I_L Variations.....	112
5.4.4.	Combined Frequency Compensation and Q-Factor	116
5.4.5.	Minimum C_L for a Stable Operation	117
5.5.	Circuit Implementation and Power Supply Rejection Analysis.....	118
5.5.1.	Schematic Implementation.....	118
5.5.2.	Power Supply Rejection Analysis.....	120

5.6.	Experimental Results and Discussions	124
5.7.	Summary	134
Chapter 6 Process, Voltage and Temperature (PVT) Compensation for Digital Circuit Systems		136
6.1.	Review of PVT compensation techniques	136
6.1.1.	Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations	137
6.1.2.	Mixed Body Bias Technique with Fixed V_{TH} and I_{ds} Generation Circuits.....	138
6.1.3.	On-chip PVT Compensation Technique Using Current Monitoring Circuit ...	139
6.1.4.	PVT Compensation Using Adaptive Supply Control	141
6.2.	Proposed PVT Compensated Supply (PVTCS).....	142
6.2.1.	Operation Principle	142
6.2.1.1.	Process Variation Compensation.....	143
6.2.1.2.	Temperature Variation Compensation	145
6.2.1.3.	Supply Independency	146
6.2.2.	Circuit Implementation	147
6.2.2.1.	Reference Block and P/N Diodes	147
6.2.2.2.	Differential Difference Amplifier (DDA)	149
6.2.2.3.	LDO Regulator	151
6.2.2.4.	Digital Tracked Oscillator	153
6.2.3.	Results and Discussions	154
6.3.3.1.	Results of Inverter Chain.....	154
6.3.3.2.	Results of Critical Path.....	160
6.3.3.3.	Performance Comparison	161
6.3.	Summary	163
Chapter 7 Conclusions and Future Works		164
7.1	Conclusions	164
7.2	Future Works	167
Author's Publications.....		169
References.....		170

ABSTRACT

With the fast growing electronic portable devices, power management becomes an important area in electronic industry to reduce the power consumption so as to extend the battery life of these devices. Low dropout (LDO) regulator is widely used in power management IC due to its simple structure, low noise and fast speed characteristics. As the technology continues scaling down to deep submicron, the digital circuits display less immunity to Process, Supply voltage, and Temperature (PVT) variations. Therefore, power management technique with PVT compensation becomes another important design approach. This work focuses on the design techniques which include process variation sensing circuit (V_{TH} sensor), wide load capacitance (C_L) range with fast speed LDO regulators and digital system supply with PVT compensation capability using LDO regulator.

First, the V_{TH} sensor circuit can generate the V_{TH} of a single MOSFET at 0 K (V_{TH0}). V_{TH0} is temperature and supply invariant but process dependent. The V_{TH} sensor can be utilized to sense the V_{TH} variation of the devices, hence providing the process information. Based on a Brokaw structure with the addition of the proposed current-mode second-order temperature compensation network, this improves the Temperature Coefficient (T.C.), the V_{TH} sensor.

Second, a DSMFC technique is proposed in a Flipped Voltage Follower (FVF) LDO regulator architecture. By adding an extra Miller compensation stage, the dominant pole of the feedback system can be pushed to lower frequency whilst the non-dominant pole(s) can be pushed to higher frequency. This extends the C_L driving range without sacrificing circuit complexity and quiescent power consumption.

Third, a novel Weighted Current Feedback (WCF) technique is proposed in a multi-gain stage LDO regulator architecture. Through feedback of a weighted current, the WCF permits smart management of the output impedance as well as the gain from the inter-gain stage. As a result, a good optimization of stability, speed and accuracy can be achieved in the context of wide C_L range.

Finally, a PVT Compensated Supply (PVTCS) for driving point-of-load digital system is designed. By adding a weighted combination of the V_{TH} drift of the PMOS (ΔV_{THP}) and NMOS (ΔV_{THN}) diodes onto the reference voltage of a high speed WCF LDO regulator, the supply voltage of the digital circuits is adjusted adaptively. This can reduce the speed deviations of the digital circuits under PVT variations.

With the low T.C. V_{TH} sensor circuit to sense the process information, the two wide C_L range LDO regulators to drive the digital circuits and the PVTCS to compensate the PVT variations of the digital systems, the works are useful for fully on-chip power management circuits with PVT compensation.

LIST OF FIGURES

Fig. 1.1: (a) PWM switching regulator structure. (b) Linear regulator structure. [1].....	2
Fig. 1.2 A typical SoC IC with power management unit [37].....	5
Fig. 1.3: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators.....	7
Fig. 1.4: A sample of power and ground plan of microprocessor [42].	7
Fig. 1.5: Digital circuit performance fluctuation with respect to supply voltage: (a) delay, (b) power consumption [48].....	9
Fig. 1.6: Generic block diagram of an exemplary PVT compensation system.	10
Fig. 2.1: Ferreira's V_{TH} sensor circuit [62].....	19
Fig. 2.2: Ueno's V_{TH} sensor circuit [63].....	21
Fig. 2.3: Lee's V_{TH} sensor circuit [65].	23
Fig. 2.4: Proposed V_{TH} monitoring based voltage reference circuit.....	27
Fig. 2.5: Temperature compensation in graphical illustration.....	28
Fig. 2.6: (a) Simulated V_{GS1} , V_{I2} and their slopes with respect to temperature variation. (b) Monte-Carlo simulation results for first-order Brokaw circuit and proposed temperature compensated V_{TH} sensor.	30
Fig. 2.7 Simulated V_{OUT} under different supply voltages and temperatures.	31
Fig. 2.8 Monte-Carlo simulation results for PSR @ 100 Hz.....	31
Fig. 2.9: Microphotograph of the proposed V_{TH} sensor.	32
Fig. 2.10: (a) Measured output voltage V_{OUT} as a function of temperature for 15 samples with 0.75V supply voltage. (b) Measured output voltage V_{OUT} as a function of temperature for different supply voltages.	33
Fig. 2.11: (a) Distribution of V_{OUT} for 15 samples at room temperature. (b) Distribution of the T.C. performance metric for 15 samples.....	34
Fig. 2.12: (a) Measured PSR. (b) Measured power supply ripple response at $V_{DD} = 0.75$ V, $V_{ripple} = 100$ mV for the proposed V_{TH} sensor.	34
Fig. 2.13: (a) Monte-Carlo simulation results of T.C. for die-to-die variations. (b) Monte-Carlo simulation results of T.C. for within-die variations.	36
Fig. 2.14: (a) Monte-Carlo simulation results of V_{OUT} for MOSFET-devices-only within-die variations. (b) Monte-Carlo simulation results of T.C. for resistors-only within-die variations.	37
Fig. 3.1: Conventional buffer based LDO regulator.	41
Fig. 3.2: Loop gain response for conventional buffer based LDO regulator.....	42
Fig. 3.3: Dynamic biased LDO regulator.	44

Fig. 3.4: Single-stage error amplifier plus power transistor OCL-LDO regulator topology.....	45
Fig. 3.5: Loop gain frequency response of the single-stage error amplifier plus power transistor OCL-LDO regulator at low I_L	46
Fig. 3.6: Multi-gain stage error amplifier plus power transistor OCL-LDO regulator topology.	47
Fig. 3.7: OCL-LDO regulator with Flipped Voltage Follower (FVF).	49
Fig. 3.8: Common centroid layout example.	52
Fig. 3.9: Typical multi-finger layout structure.	53
Fig. 3.10: A modified multi-finger layout structure.	54
Fig. 3.11: A Waffle layout structure.	55
Fig. 3.12: Top view of a vertical-metallization strategy for a welled power	56
Fig. 3.13: Top view lateral metallization strategy for a welled power MOSFET from second- to third-level metal planes and bond pads [1].	57
Fig. 4. 1 (a) Schematic of the proposed FVF based LDO regulator with DSMFC ($v_{fb\text{in}}$, $v_{fb\text{out}}$ indicate the loop breaking point). (b) Control voltage (V_{CTRL}) generator.	62
Fig. 4.2: Small-signal model of the proposed FVF LDO regulator.....	63
Fig. 4.3: Loop gain of the proposed FVF LDO regulator with poles and zero locations for (a) large C_L , (b) small C_L	67
Fig. 4.4: Simulated open-loop gain and phase responses at different I_L for (a) $C_L = 10$ nF and (b) $C_L = 10$ pF.	69
Fig. 4.5: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of C_L at different I_L using DSMFC.	71
Fig. 4.6: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of C_L at different I_L using SMC.	71
Fig. 4.7 Schematic of the LDO regulator with power supply noise injection paths.....	80
Fig. 4. 8 Simulated PSR of the LDO regulator under $I_L = 50$ mA for different C_L	84
Fig. 4.9 Transient simulation results for I_L switching between 0 to 50 mA at $C_L = 10$ pF, 100 pF, 1 nF and 10 nF (I_L time delay is introduced to differentiate the plot).	86
Fig. 5.1: A fast-transient multi-gain stage regulator topology.	91
Fig. 5.2: Proposed Negative Current Feedback (NCF) topology embedded in multi-gain stage in a LDO regulator.	92
Fig. 5.3: A LDO regulator architecture using the WCF technique.	95
Fig. 5.4: Simplified schematic of 2 nd , 3 rd gain stages and WCF for (a) low I_L , (b) moderate I_L , and (c) high I_L	96
Fig. 5.5: Small-signal model of the WCF LDO regulator.....	98
Fig. 5.6: Simulated β (β_{sim}) and R_{2f} at different I_L conditions.....	106

Fig. 5.7: Simulated open-loop gain and phase at different I_L for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF with $V_{DD} = 0.75$ V.....	111
Fig. 5.8: Simulated phase margin (PM) and gain margin (GM) for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L at $V_{DD} = 0.75$ V.....	112
Fig. 5.9: Schematic of the WCF LDO regulator.	119
Fig. 5.10: Exemplary transient response of the LDO regulator with proposed NCF and WCF technique.	120
Fig. 5. 11 Simulated PSR for $C_L = 470$ pF under different I_L	123
Fig. 5.12: Microphotograph of the WCF LDO regulator.	124
Fig. 5.13: Measured load transient responses with $V_{DD} = 0.75$ V, $V_{OUT} = 0.55$ V for (a) $C_L = 470$ pF, (b) $C_L = 1$ nF, (c) $C_L = 3.3$ nF and (d) $C_L = 10$ nF.	126
Fig. 5.14: Measured load transient responses at $V_{DD} = 0.75$ V with I_L switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.	127
Fig. 5.15: Measured load transient responses at $V_{DD} = 1.2$ V with I_L switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.	128
Fig. 5.16: Measured line transient response at $I_L = 1$ mA and $C_L = 470$ pF.....	129
Fig. 5.17: PSR measurement setup.....	130
Fig. 5.18: Measured PSR at $C_L = 470$ pF for different I_L	130
Fig. 5.19: Measured Output Noise at $C_L = 470$ pF with 0 mA I_L	131
Fig. 5.20: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators and the proposed two wide C_L range LDO regulators.....	135
Fig. 6.1: Block diagram of adaptive body bias for reducing impacts of Die-to-Die and Within-Die parameter variations [51].....	137
Fig. 6.2: Fixed V_{TH} and I_{ds} generator [46].....	138
Fig. 6.3: Fixed V_{TH} and I_{ds} body bias generator [46].....	139
Fig. 6.4: Schematic of the on-chip PVT compensation system [45].....	140
Fig. 6.5: Block diagram of the proposed PVT compensated supply (PVTCS) and load circuits.	143
Fig. 6.6: Voltage and current reference circuits.	148
Fig. 6. 7 Monte Carlo simulation results for $V_{REF}/2$ and I_{REF} under different temperatures....	148
Fig. 6.8: (a) Symbolic and (b) Schematic of the 3-port differential difference amplifier (DDA).	150
Fig. 6.9: Simulated V_R under different V_{GSN} and V_{SGP}	150
Fig. 6.10: LDO regulator circuit.....	151
Fig. 6.11. Simulated transient response for the LDO regulator.....	152
Fig. 6.12: Digital load circuits configured as oscillators: (a) Inverter Chain and Critical Path Circuit [27, 60].	153

Fig. 6.13: Microphotograph of the PVT compensated supply system.	154
Fig. 6.14: Comparison of oscillation frequency of inverter chain under MC simulations when (a) PVTCS and (b) UCS is applied.	155
Fig. 6.15: Comparison of oscillation frequencies of inverter chain under temperature variation between PVTCS and UCS.....	156
Fig. 6.16: Comparison of oscillation frequency of inverter chain for measured 12 chips at (a) PVTCS and (b) UCS.	156
Fig. 6.17: Comparison of oscillation frequency variation of inverter chain under temperature variation for measured 12 chips at (a) PVTCS and (b) UCS.	157
Fig. 6.18: Normalized oscillation frequency variation of inverter chain under supply variation for measured 12 chips at PVTCS and UCS.....	158
Fig. 6.19: Measured oscillation waveforms for a single chip under PVTCS and UCS at different input supply and temperature values.	159
Fig. 6.20: Comparison of oscillation frequency of critical path under MC simulations at (a) PVTCS and (b) UCS.	160
Fig. 6.21: Comparison of oscillation frequency of critical path under temperature variation at PVTCS and UCS.....	161

LIST OF TABLES

TABLE 1.1 PERFORMANCE COMPARISON OF LINEAR AND SWITCHING REGULATORS [1].	3
TABLE 1.2 SUMMARY OF CONTRIBUTIONS IN THIS RESEARCH WORK	15
TABLE 2.1 PERFORMANCE COMPARISON OF THE PROPOSED V_{TH} SENSOR WITH OTHER REPORTED NANOMETER CMOS VOLTAGE REFERENCE CIRCUITS.	38
TABLE 2.2 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER V_{TH} SENSOR WITH OTHER REPORTED V_{TH} SENSOR DESIGNS USING LONG CHANNEL-LENGTH TRANSISTORS.	39
TABLE 2.3 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER V_{TH} SENSOR WITH BANDGAP VOLTAGE REFERENCE CIRCUITS.	39
TABLE 4.1 POLES AND ZERO LOCATIONS FOR SIX CASES	66
TABLE 4.2 DAMPING FACTOR AND GM FOR CASES EXHIBITING COMPLEX POLE PAIR.	75
TABLE 4.3 MINIMUM DAMPING FACTOR AND MINIMUM GM WITH THEIR RESPECTIVE C_L LOCATIONS.	77
TABLE 4.4 RELATIVE PM AND GM FOR DIFFERENT C_{M1} & C_{M2} COMBINATIONS WITH REFERENCE TO NOMINAL CASE	79
TABLE 4.5 PM AND GM FOR DIFFERENT C_{M1} & C_{M2} COMBINATIONS	79
TABLE 4.6 PERFORMANCE SUMMARY UNDER PROCESS AND TEMPERATURE CORNERS	87
TABLE 4.7 PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS	89
TABLE 5.1 APPROXIMATED VARIABLES FROM a TO e FOR LARGE, MODERATE AND SMALL $C_L R_O$ CASES	102
TABLE 5.2 ROUTH TABLE FOR A 5 TH ORDER POLYNOMIAL	102
TABLE 5.3 ROUTH TABLE PARAMETER EXPANSION FOR THE WCF LDO REGULATOR CLOSED-LOOP TRANSFER FUNCTION IN (5.11).	104
TABLE 5.4 SUMMARY OF THE REQUIRED β_{RH} AT DIFFERENT I_L CONDITIONS TO MEET ROUTH–HURWITZ CRITERION	106
Table 5.5 DESIGN PARAMETERS, STABILITY VERIFICATION USING THEORETICAL β_{RH} AND SIMULATED β_{sim}	107
TABLE 5.6 FEEDBACK FACTOR β , POLES, ZERO, Q-FACTOR, ω_{UGF} FOR LARGE, MODERATE AND SMALL $C_L R_O$ CASES	109
TABLE 5.7 NUMERICAL EXAMPLE FOR PM VERIFICATION USING THEORETICAL β_{PM} AND SIMULATED β_{sim}	115
TABLE 5.8 COMBINED β DESIGN INEQUALITIES USING β_{RH} AND β_{PM}	116
TABLE 5.9 PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS	132
TABLE 6.1 NUMERICAL CALCULATION AND VALUE OF WEIGHT D	145

TABLE 6.2 PERFORMANCE IMPROVEMENT OF THE PVTCS WITH RESPECT TO THE UCS AT
WORST CASES 162

TABLE 6.3 PERFORMANCE COMPARISON WITH RESPECT TO THE REPORTED PVT
COMPENSATION CIRCUITS..... 162

LIST OF GLOSSARY

BBG	Body Bias Generator
BGR	Bandgap Reference
CG	Current Generator
CTAT	Complementary-to-absolute-temperature
Cox	Gate oxide capacitance
D2D	Die-to-Die
DDA	Differential Difference Amplifier
DSMFC	Dual Summed Miller Frequency Compensation
ESR	Equivalent Series Resistance
GM	Gain Margin
I_Q	Quiescent current
LDO	Low Dropout
MC	Monte-Carlo
NBG	Negative Bias voltage Generator
NCF	Negative Current Feedback
OC-LDO	Output Capacitor LDO
OCL-LDO	Output Capacitorless LDO
OTA	Operational Transconductance Amplifier
PCB	print-circuit-board
PM	Phase Margin
PSR	Power Supply Rejection
PTAT	Proportional To Absolute Temperature
PVTCS	PVT Compensated Supply
RHP	Right-Half-Plane
R_{on}	Transistor On-resistance
SoC	System on Chip
UCS	Un-Compensated Supply

V_{DS}	Transistor drain-to-source voltage
V_{GS}	Transistor gate-to-source voltage
V_T	Thermal voltage ($= k_B T/q$)
WCF	Weighted Current Feedback
WID	Within-Die
k_B	The Boltzmann constant
q	Elementary charge
μ	Carrier mobility
η	Subthreshold slope factor
T	Temperature
T_r	Room temperature ($T_r = 300$ K)
κ	T.C. of V_{TH}
m	Mobility temperature exponent whose typical value is 1.5 for CMOS

CHAPTER 1

INTRODUCTION

This Chapter gives the motivations, objectives, and contributions of this research work.

1.1 Motivations

With the fast growing electronic portable devices, power management becomes an important area in electronic industry to reduce the power consumption so as to extend the battery life of these devices. A power management circuit (IC) normally comprises switching regulator, linear regulator and power control logic [1]. The control logic inside the power management IC is normally used to control the power delivery to the loading circuit.

For the switching regulator, due to the switching nature, it can support AC-AC, AC-DC, DC-AC and DC-DC conversions. In the context of ICs, DC-DC converter predominates because the ICs normally derive power from the dc batteries and other dc supplies [1]. Figure 1.1(a) shows the most popular scheme among the DC-DC converters which employs the pulse width modulation (PWM) technique. A linear error amplifier compares the feedback output voltage with the reference voltage. Through a PWM converter, the error amplifier output voltage is converted into a digital switching signal having different duty ratios to drive the power transistors. Finally, a low power filter is applied on the digital switching waveform and a DC voltage can be generated. Due to the switching operation characteristics, the DC-DC converter can generate wide range of output voltages, including voltage below (buck converters [2-4]), above (boost converter [5-7]) and above-or-below (buck-boost

converter [8-10]). Since the voltage across the power transistor in DC-DC converter are small (10 mV – 100mV), above 80% power efficiency can be achieved. However, the output noise is high because of the on-off switching in the power transistors. Finally, due to the external large inductor and capacitor which are using to form the low pass filter, the DC-DC converter hardly supports full integration with the load circuits.

Fig. 1.1: (a) PWM switching regulator structure. (b) Linear regulator structure. [1]

Regarding the linear regulator, as shown Fig. 1.1(b), the error amplifier output voltage directly drive the power transistor and control its on-resistance instead of converting into digital signals. Since the current in the power transistor is continuous in time, the circuit is linear and analog in nature. The resulting output voltage has lower noise with respect to the DC-DC converter. However, the output voltage of linear regulator cannot exceed the input supply voltage. In addition, the voltage drop across the series switch in the linear regulator is normally larger than 0.2 V which limits its conversion power efficiency. Lastly but most importantly, the linear regulator can be designed with and without off-chip capacitors. They are named as the output-capacitor based linear regulator and the output capacitorless liner regulator, respectively. For output capacitorless linear regulator, it is possible to fully integrate it

with loading circuits which can reduce the cost by using less number of I/O pins, less print-circuit-board (PCB) area and less external components.

Table 1.1 compares the performance of switching regulator and linear regulator. As indicated in this table, the switching regulator can provide a wide range of output voltages and benefit from having high power efficiency while show large noise on the output voltage. On the other hand, the linear regulators exhibit limited power efficiency due to its quiescent current flow and the large input-to-output voltage difference across the power transistor. However, the linear regulator can give stable and low noise output voltage whilst offering the fully on-chip capability. It is therefore suitable for modern System-on-Chip (SoC) applications [11-15].

TABLE 1.1 PERFORMANCE COMPARISON OF LINEAR AND SWITCHING REGULATORS [1].

Linear Regulators	Switching Regulators
Output range is limited ($V_{OUT} < V_{IN}$)	✓ Output range is flexible ($V_{OUT} \leq$ or $\geq V_{IN}$)
✓ Simple circuit	Complex circuit
✓ Low noise content	High noise content
✓ Fast response	Slow response
Limited power efficiency ($\eta < V_{OUT}/V_{IN}$)	✓ High power efficiency ($\eta \approx 80\text{--}95\%$)
Good for low-power applications	Good for high-power applications
✓ Can be fully integrated with loading circuit	Normally stand-alone

LDO regulators belong to the linear voltage regulators with improved power efficiency by reducing the differences between the input voltage V_{IN} and the output voltage V_{OUT} . Due to the improved power efficiency and fast speed characteristics, LDO regulator can be utilized to drive the subsystem of the ICs including point-of-load digital circuits [16] and analog/mixed-signal blocks. Under low supply voltage environment, the digital circuits normally consume low to moderate power but the currents are fast switching. Besides, the parasitic capacitance at the supply line can be

large due to the large number of transistors connected to the supply line. As such, the LDO regulator to drive such circuit needs to have a wide load capacitance (C_L) driving ability with fast transient responses.

There are two categories for LDO regulator as well. They are output capacitor based LDO regulator (OC-LDO) and output capacitorless LDO (OCL-LDO) regulator. For OC-LDO regulator, it relies on a μF level off-chip capacitor to maintain stable operation. The off-chip capacitor can source and sink current during load switching which can reduce the transient overshoot and undershoot. However, it also limits the fully integration ability of LDO regulator. On the contrary, the OCL-LDO regulators [17-34] have received much attention recently since it eliminates the output capacitor through using internal compensation to achieve stability. The load capacitance C_L of the OCL-LDO regulator is then purely formed by the parasitic capacitance on the supply line of loading circuit which is normally from few ten pF to few nF range. The OCL-LDO regulators are widely used for on-chip applications for modern SoCs. For first example, the linear regulator, which is powered by switching regulators, delivers the current to sub-blocks of the system that requires low noise and stable supply voltage like LNA, frequency synthesizer, Mixers in cellular phones and PDA (personal digital assistant) [35, 36]. For second example, to implement fine-grain on-chip power domains or dynamic-voltage-scaling (DVS) [26], multiple on-chip LDO regulators are required to drive the sub-blocks (like memory banks, DSPs). Figure 1.2 depicts a typical structure of a switching regulator driving few LDO regulators in a power management system [37]. It can be seen that the OCL-LDO regulator is an essential building block in SoC IC.

Fig. 1.2 A typical SoC IC with power management unit [37].

Though the OCL-LDO regulator offers fully on-chip merit with respect to the OC-LDO regulator, the design challenges are increased in the OLC-LDO regulator. These are summarized as follows. First, without the large output capacitor to source or sink current, the undershoot and overshoot of OCL-LDO regulators are normally much larger than the OC-LDO regulator counterpart. To improve the transient performance, the adaptive biasing technique [25, 27] has been reported to dynamically increase the biasing current of the error amplifier, hence increasing the loop gain-bandwidth product. However, due to a positive feedback loop exists in the adaptive feedback loop, it is difficult to control the stability. Direct voltage spike detection technique [23] senses the output voltage spike and generates a spike current to charge or discharge the gate of power transistor and the output node with improved speed. Unfortunately, the structure is limited by the small feedback loop gain. More importantly, poor regulation accuracy is obtained due to its single-stage amplifier topology.

Second, to ensure regulation accuracy, a multi-gain stage amplifier topology is typically employed to drive the power transistor. Under low quiescent current constraint, the output impedances of the gain stages are high, leading to several low frequency poles. In order to achieve stability, some appropriate frequency

compensation techniques should be applied. For a standard Miller compensation, the required compensation capacitor C_m is proportional to the load capacitor C_L . For a large C_L , C_m will be large, thus contributing large silicon area. Moreover, a large C_m will also result in small gain bandwidth product (GBW), reducing the speed of LDO regulator. This in turn increases the design difficulty of the OCL-LDO regulator, especially for applications with wide range of C_L . Therefore, in most of the reported OCL-LDO regulator designs, they usually drive a maximum C_L up to tens of pF or 100 pF [21, 22, 24, 27, 28, 30]. Few designs can drive relatively large C_L [18, 23, 26, 29, 34]. Figure 1.3 depicts the maximum C_L versus quiescent current for reported state-of-the-art OCL-LDO regulators. It can be observed that under low quiescent current constraints, most of the reported works can only drive small C_L . This may not be useful for the SoC environment having large scale digital circuits. As a result, the effective supply line parasitic capacitance becomes very large. To drive such the circuits, the LDO regulator should have the ability to drive a wide C_L range (few hundred pF to few nF) [38].

With the above mentioned design challenges in the OCL-LDO regulators, in this research work, OCL-LDO regulator topologies and circuit techniques which can drive wide range of C_L with fast transient responses are explored.

To drive large scale digital circuits, the power management system needs to be well controlled in order to save power without affecting the circuit performance. A popular driving scheme is the dynamic voltage frequency scaling (DVFS) [39, 40]. Based on different workloads, computation conditions or objective functions, the supply voltage of the circuit is reduced when performance constraints are relaxed. For example, most DVFS-based mobile and embedded devices typically spend the majority of their lifetimes in operating in low-power mode [41]. Figure 1.4 depicts a

Fig. 1.3: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators.

Fig. 1.4: A sample of power and ground plan of microprocessor [42].

sample of power and ground plan using DVFS technique [42]. Though the DVFS can reduce the power consumption of digital circuits, the supply voltage is still fixed under normal operating condition. This may lead large speed deviation if nanometer technology with large process variation is used. This is given and discussed as follows:

As CMOS technology continues to scale down, transistors parameters including threshold voltage (V_{TH}), channel length, oxide thickness and mobility depicts large process variations [43, 44]. In addition, the environmental temperature variations change the mobility of the electrons and holes whilst modifying the V_{TH} of the devices, thereby causing the circuit speed variations [43, 45, 46]. Furthermore, the supply voltage V_{DD} is another critical parameter that directly affects the transient current of the digital circuits because the saturation current of the transistor is proportional to $\alpha/(V_{DD}-V_{TH})$, where α is the carrier mobility degradation factor [45, 47]. Through summing up these effects, the digital system will exhibit a wide deviation of performance under process, voltage and temperature (PVT) variations, particularly significant in nanometer CMOS technologies.

Of another concern, with the tremendous increase in portable electronic devices, the reduction of power consumption in digital Large-Scale Integration (LSI) becomes an important matter to extend the battery life. The most effective and direct way is to reduce the power supply voltage (V_{DD}) due to the square law relation between the power consumption and V_{DD} [45, 48]. However, when V_{DD} comes close to the threshold of transistor (V_{TH}), a small variation of PVT will result in the significant degradation of chip performance [49]. Figure 1.5 illustrates the CMOS digital circuit's delay and power parameters fluctuates with respect to V_{DD} [48]. As can be seen from the graphs, both the key parameters substantially increase when the V_{DD} scales down.

Fig. 1.5: Digital circuit performance fluctuation with respect to supply voltage: (a) delay, (b) power consumption [48].

To reduce the performance deviation of the digital circuits or improve the yield, for the fixed supply system using DVFS, the minimum supply voltage is chosen on the basis of the worst case corners (process and temperature). This may waste a lot of power since some of the function blocks may not need such high supply voltage. The speed of the digital circuit will also vary significantly under process variations. Another technique is to implement PVT compensation during design process. Under different process and temperature conditions, the supply voltage of the digital system is dynamically varied to reduce the variation of speed.

Figure 1.6 depicts the generic block diagram in an exemplary PVT compensation system. The PVT system comprises a reference block, a variation sensor block, a correction block and a driving stage. Of particularly noted, there are many possible circuit implementation alternatives for each block. The function for each block is described in the following.

Fig. 1.6: Generic block diagram of an exemplary PVT compensation system.

Reference Block: The reference block is to provide the reference signal(s) such as V_{REF} and I_{REF} . The voltage reference signal V_{REF} can be used to define a precise V_{GS} [44, 50] [46] or a precise body voltage [51] whereas the current reference signal I_{REF} can be used to define the saturation current of the PMOS and NMOS transistors [45] in the digital logic gates. To generate V_{REF} from the reference block, bandgap voltage references [52-58] are normally used because they can generate the precise output voltage with high temperature stability. CMOS voltage references [59-73] can also be used which can offer low voltage operation. But the CMOS voltage reference's output voltage is dependent on process and the temperature stability is normally poorer than the BJT based counterparts. As for the reference current I_{REF} , it can be generated in different ways. First, a threshold monitoring circuit (V_{TH} sensor) can be utilized. The V_{TH} sensor can generate the extrapolated V_{TH} of a single MOSFET absolute zero temperature (V_{TH0}) [61-63, 65]. In principle, V_{TH0} is insensitive to variations in temperature and supply, but having a process-dependent characteristic. As such, after scaling the V_{TH0} using resistors and applied the scaled V_{TH0} to a saturated MOSFET, a PVT-invariant I_{REF} can be generated [74]. Another way to generate I_{REF} is to using V-I converter in [75]. By applying a proportional-to-absolute-temperature (PTAT) voltage to a resistor with positive T.C., a temperature invariant current can be achieved.

However, due to the process variation of the resistor, the precision of I_{REF} may degrade under modern technologies.

Variation Sensor: The V_{TH} sensor can be used to sense the process variation [63] on the basis of the linkage between V_{TH0} and delay. However, it cannot provide the temperature variation information. Another simple circuit is to use diode transistors to sense the process and temperature variation together [44, 45, 50]. Finally, a phase-lock-loop (PLL) can also be used to detect the parameter and timing error of the digital circuits under PVT variation but a precision high-frequency reference clock signal is required [76]. Besides, to relax the on-chip PLL filter size, the clock frequency tends to be very high as the design tradeoff.

Correction Block: To compensate the PVT variation, the correction techniques on the basis of substrate bias control to change the V_{TH} of transistor are extensively reported [44-46, 48, 50, 51, 76-83]. At this juncture, it is common to observe that the effect of the substrate terminal on controlling the V_{TH} of the transistor is significantly reduced due to relatively lower body bias factor in advanced nanometer CMOS process technologies. As a result, the substrate bias control to minimize the PVT variation [50] becomes less effective. In addition, the substrate leakage current is considered high under the process, thereby contributing the potential large power overhead. More importantly, reliability becomes another major concern when the operating temperature potentially reduces the gap of safety margin in a forward-biased substrate, hence increasing the risk of latch up. This imposes the difficulty of employing substrate bias control in nanometer VLSI systems. Another one is the post-silicon compensation technique that of adaptively changing the supply of digital circuits [78, 79]. This method is effective since the delay of the digital circuit is

heavily dependent on its supply voltage. However, the cost is increased because of the post-silicon trimming process.

Driving Stage: For the adaptive body bias correction technique, a voltage buffer is employed to distribute the body voltage [45]. For the adaptive supply compensation, the driving stage can be implemented in a form of DC-DC converter [45] or LDO regulators. Despite of the efficiency, the DC-DC converter has the key disadvantage of large switching noise. Of major design concern, it needs the off-chip capacitors and inductors that do not support the fully integration design objective. Therefore it may not be suitable for on-chip PVT compensation. In the context of the LDO regulators, the OCL-LDO regulator architecture with wide C_L range driving capability becomes the optimum choice for use in driving the digital system.

From the above study of the PVT compensated system and the modern trend of low-power and variation-aware circuits in the advanced CMOS process technologies, they raise the motivation for the design of a total fully-integrated power management circuit/system with PVT supply compensation as the ultimate goal.

1.2 Objectives

Followed by the study and background work, the objectives of this thesis are:

- (i) To investigate, design and implementation of a small T.C. V_{TH} sensor.
- (ii) To research new circuit technique and topology for the design of OCL-LDO regulators to drive wide range of C_L with fast transient performance.
- (iii) To exploit the design and implementation of a PVT compensation supply system for point-of-load digital circuits.
- (iv) To conduct the detailed circuit analysis of the V_{TH} sensor, the LDO regulators and the PVT compensation system.
- (v) To conduct the test for the silicon prototypes which are realized in UMC 65-nm CMOS technology.

1.3 Contributions

The main contributions of this research work in this thesis are summarized as follows:

- (i) Propose a nonlinear temperature compensation technique for the design of V_{TH} sensor which can reduce the T.C. of the output voltage under low power constraint.
- (ii) Propose a frequency compensation technique for the OCL-LDO regulator to extend the C_L range. The regulator can achieve the widest C_L range driving capability with good stability and transient performance.
- (iii) Propose a current feedback technique for the OCL-LDO regulator which can drive a wide range of C_L whilst achieving fast transient performance metrics with good regulation accuracy.
- (iv) Propose a point-of-load digital system driving supply with PVT compensation. Such the PVT compensated supply (PVTCS) can reduce the performance deviation of digital circuits and demonstrate significant delay variation improvement with respect to that of the uncompensated digital supply counterpart.

Table 1.2 summarizes the proposed techniques together with their performances. It can be seen that all the proposed techniques have achieved good performance. As such, they are suitable for fully-integrated power management system with PVT compensation effects. First, the V_{TH} sensor can be used to generate the process information or to generate a constant current. Second, the two wide C_L range LDO regulators can be served as driver for digital load circuits. Lastly, using the circuit technique in Type-II LDO regulator, the PVTCS has demonstrated an exemplary fully on-chip power management system with PVT compensation.

TABLE 1.2 SUMMARY OF CONTRIBUTIONS IN THIS RESEARCH WORK

Proposed Techniques	Performances and Technical Merits
V_{TH} sensor	<ol style="list-style-type: none">1. Low T.C. (24.5 ppm/°C)2. Wide Temperature Range (-40 °C to 90°C)3. Low power (290 nW)4. Operate well under nanometer technology
LDO Regulator (Type-I)	<ol style="list-style-type: none">1. Wide C_L range (10 pF to 10 nF)2. Stable and work well from 0 to full loading current (50 mA).2. Simple structure3. Fast transient
LDO Regulator (Type-II)	<ol style="list-style-type: none">1. Wide C_L range (470 pF to 10 nF).2. Small compensation capacitor (3.8pF).3. Stable and work well from 0 to full loading current (50 mA).4. Fast transient response with <400 ns settling time
PVTCS	<ol style="list-style-type: none">1. Simple structure2. Can effectively compensate performance variations under PVT variations.3. Supply control with no latch up issue with respect to adaptive body bias.

1.4 Organization of the Thesis

This report is organized in seven Chapters as follows.

Chapter 1 gives the motivations, objectives and contributions of this research.

Chapter 2 reviews the V_{TH} sensor circuits pertaining to their temperature compensation principles. This is followed by the discussion and analysis of the proposed current-mode second-order temperature compensated V_{TH} sensor.

Chapter 3 reviews the representative LDO regulator structures. The gain stage structure, stability, transient performances will be discussed. Layout techniques for regulators will also be described.

Chapter 4 presents the Type-I OCL-LDO regulator that can drive wide C_L range. Detailed analysis is given. Simulation results are investigated and compared with the state-of-the-art OCL-LDO regulator topologies.

Chapter 5 presents the Type-II OCL-LDO regulator with wide C_L range driving capability. Design strategies, stability analysis, simulation and measurement results are explored in detail.

Chapter 6 reviews the PVT compensation techniques. A PVT compensated supply to drive point-of-load digital system is introduced. The simulation and measurement results are discussed. The performance is compared with the benchmark work.

Chapter 7 gives the concluding remarks as well as the recommendations for the future works of this research.

CHAPTER 2

THRESHOLD MONITORING CIRCUIT

In this Chapter, a review of threshold monitoring (V_{TH} sensor) circuit is first conducted. The temperature compensation principles for each design are discussed. This is followed by the proposed current-mode second-order temperature compensated V_{TH} sensor. The operating principle, simulation and measurement results are discussed in detail.

2.1. Introduction

A voltage reference is commonly employed to generate a constant DC voltage for digital, analog as well as mixed-signal circuits and systems. The popular application examples are operational amplifiers, data converters, and power management circuits [1, 84]. Consider the bandgap voltage reference design using bipolar transistor (BJT), it can provide quite a precise voltage [52-58]. Unfortunately, due to the fixed 0.6 – 0.7 V PN junction turn-on voltage at room temperature, it requires a high supply voltage for operation headroom. Meanwhile, it does not give any hint in MOS process information thus cannot be applied as a process monitoring sensor. Turning to the voltage reference without BJTs counterparts [59-73], they offer low-voltage operation capability and linkage with process information. However, due to intrinsic transistor's process parameters displaying relatively poor immunity against the process variations, there are few nanometer process based voltage reference designs [69-71] which achieve a small temperature coefficient (T.C.) under a wide temperature range.

Considering the V_{TH} sensor circuit, it can generate the extrapolated V_{TH} of a

MOSFET at absolute zero temperature (V_{TH0}) [61-63, 65]. V_{TH0} is insensitive to the changes in temperature and supply, but it is process-dependent. With these characteristics, a V_{TH} sensor can be used to sense the V_{TH} of the MOSFET so as to provide the process information. It also can generate a PVT-invariant constant current source [74] or process dependent supply voltage for compensating the process variations in digital LSIs [45, 63]. However, the reported V_{TH} sensor designs [61-63, 65] all use CMOS process technologies with large channel lengths. Therefore, if nanometer technology which is subject to large process variations is used, the difficulty to maintain their original low T.C. performance is increased.

2.2. Review of V_{TH} Sensor Designs

This section discusses the reported V_{TH} sensor designs. The temperature compensation principle, design challenges and considerations under nanometer technologies are all explored.

2.2.1. Ferreira's V_{TH} Sensor [62]

Fig. 2.1: Ferreira's V_{TH} sensor circuit [62].

Ferreira et al. proposes a V_{TH} sensor circuit using linear resistor and weak inversion transistors [62] as shown in Fig. 2.1. It generates the PTAT voltage through injecting a PTAT current into a linear resistor (R_2) to compensate the negative T.C. of V_{TH} . M_1 and M_3 are implemented as a composite transistor as shown in enclosed area. It cascades two transistors in series to increase the output impedance, thus the accuracy of the PTAT generator is improved.

The output voltage of this design can be derived as follows:

$$I_B(T) = \eta_p \frac{k_B T}{q} \frac{1}{R_1} \ln \left(\frac{(W/L)_2 (W/L)_{3Q1}}{(W/L)_4 (W/L)_{1Q1}} \right) \quad (2.1)$$

$$V_{GS4}(T) = V_{TH0} \left(1 - \frac{T}{T_r} \right) + V_{GS4}(T_r) \left(\frac{T}{T_r} \right) + (1 - \alpha) \eta_n \frac{k_B T}{q} \ln \left(\frac{T}{T_r} \right) \quad (2.2)$$

$$\begin{aligned} V_{OUT}(T) &= \eta_p \frac{k_B T}{q} \frac{R_2}{R_1} \ln \left(\frac{(W/L)_2 (W/L)_{3Q1}}{(W/L)_4 (W/L)_{1Q1}} \right) + V_{GS4}(T) \\ &= V_{TH0} \left(1 - \frac{T}{T_r} \right) + V_{GS4}(T_r) \left(\frac{T}{T_r} \right) + (1 - \alpha) \eta_n \frac{k_B T}{q} \ln \left(\frac{T}{T_r} \right) \\ &\quad + \eta_p \frac{k_B T}{q} \frac{R_2}{R_1} \ln \left(\frac{(W/L)_2 (W/L)_{3Q1}}{(W/L)_4 (W/L)_{1Q1}} \right) \end{aligned} \quad (2.3)$$

where η_p and η_n are the subthreshold slope factors for PMOS and NMOS respectively. α is a process dependent parameter. After the minimum temperature dependence is achieved, the output voltage is

$$V_{OUT}(T) = V_{TH0} - (1 - \alpha) \eta_n \frac{k_B T}{q} \left[1 - \ln \left(\frac{T}{T_r} \right) \right] \quad (2.4)$$

Referring to (2.4), the second term is small when compared with the first term. The output voltage is approximated as V_{TH0} . This circuit is simple but the first order temperature compensation limits its T.C. performance.

2.2.2. Ueno's V_{TH} Sensor [63]

Fig. 2.2: Ueno's V_{TH} sensor circuit [63].

Ueno et al. presents a V_{TH} sensor circuit under 0.35- μm process as shown in Fig. 2.2. It achieves 15 ppm/ $^{\circ}\text{C}$ while consuming a power of 300 nW [63]. It compensates the negative T.C. of V_{TH} through a stack of proportional-to-temperature (PTAT) voltage. Besides, the current generation is achieved by biasing a transistor (M_R) at linear region using the output voltage.

In Fig. 2.2, the transistors M_1 to M_7 all work in subthreshold region while the transistor M_R works in linear region. The output voltage of this circuit can be derived as follows:

$$I_p = \frac{V_{DSMR}}{R_{MR}} = S_R \mu C_{OX} (V_{OUT} - V_{TH}) \eta V_T \ln(S_2/S_1) \quad (2.5)$$

$$I_0 = \mu C_{OX} (\eta - 1) V_T^2 \quad (2.6)$$

$$\begin{aligned}
V_{OUT} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\
&= V_{GS4} + \eta V_T \ln \left(\frac{2S_3 S_5}{S_6 S_7} \right) \\
&= V_{TH} + \eta V_T \ln \left(\frac{3I_p}{S_4 I_0} \right) + \eta V_T \ln \left(\frac{2S_3 S_5}{S_6 S_7} \right) \\
&= V_{TH0} - \kappa T + \eta \frac{k_B T}{q} \ln \left(\frac{3I_p}{S_4 I_0} \right) + \eta \frac{k_B T}{q} \ln \left(\frac{2S_3 S_5}{S_6 S_7} \right)
\end{aligned} \tag{2.7}$$

Substituting I_p into V_{OUT} and taking the derivative of V_{OUT} respect to T , the final output voltage is V_{TH0} by setting the derivative to zero (the temperature dependent terms are cancelled). This means that the circuit yields the V_{TH0} after equalizing the negative and positive temperature dependent terms in ideal case.

The PTAT voltage inside this design is generated by stacking two transistors which are biased in saturated weak inversion region (M_3 & M_4 , M_5 & M_6). Under nanometer technology with a low threshold CMOS process, the V_{TH} of the NMOS transistor is small (< 400 mV at room temperature) when the channel length bigger than 500 nm. Moreover, to ensure that the transistor works in the saturated weak inversion region, V_{DS} must be bigger than 0.1 V [63]. This increases the design difficulty for the stacked transistors to work properly to generate a linear PTAT voltage. In addition, since the bias current I_p is generated through an active resistor, this T.C. may be sensitive to the process variation as far as the biasing voltage across the triode transistor M_R is minute.

2.2.3. Lee's V_{TH} Sensor [65]

Fig. 2.3: Lee's V_{TH} sensor circuit [65].

Lee et al. introduces a simple V_{TH} sensor circuit using a saturation region diode as the output voltage generator. The current is also produced on the basis of a linear region active resistor as that in [63]. The circuit is shown in Fig. 2.3. The output voltage could be expressed by

$$I_R = \frac{V_{DSR}}{R_{MR}} = S_R \mu C_{OX} (V_{OUT} - V_{TH}) \eta V_T \ln(S_2/S_1) \quad (2.8)$$

$$I_0 = \mu C_{OX} (\eta - 1) V_T^2 \quad (2.9)$$

$$\begin{aligned} V_{OUT} &= V_{GS3} \\ &= V_{TH0} - \kappa T + \sqrt{\frac{2NI_R}{S_3 \mu C_{OX}}} \\ &= V_{TH0} - \kappa T + \sqrt{\frac{2NS_R (V_{OUT} - V_{TH0} + \kappa T) \eta V_T \ln(S_2/S_1)}{S_3}} \end{aligned} \quad (2.10)$$

From (2.10), the output voltage could be derived as

$$V_{OUT} = V_{TH0} - \kappa T + \frac{2NS_R \eta \ln(S_2/S_1)}{S_3} \frac{k_B T}{q} \quad (2.11)$$

As a result, after the temperature dependent parts in (2.11) have been cancelled, the circuit gives an output voltage of V_{TH0} . Owing to the simple structure, this V_{TH} sensor circuit has the ability to achieve a small T.C. However, since the positive T.C. current is generated through an active resistor, the performance is still sensitive to process variations as well.

2.3. Proposed V_{TH} Sensor [85]

A current-mode second-order temperature compensation technique is proposed to reduce the nonlinear temperature effect in the V_{GS} of MOSFET. It is achieved by utilizing the different temperature properties of the high resistive poly resistor and the P+ diffusion resistor. The nonlinear temperature effect of V_{GS} , circuit implementation, working principle of the second-order temperature compensation, results and discussions are presented as follows.

2.3.1. Nonlinear Temperature Effect of V_{GS}

When a MOS transistor operates in the weak inversion region, its $V_{GS}(T)$ displays CTAT characteristic and a nonlinear temperature effect. This is due to the temperature dependency of carrier mobility ($\mu(T)$) and $V_{TH}(T)$. When a MOSFET work in weak inversion region with its drain-to-source voltage $V_{DS} > 0.1$ V, the drain current can be approximated as

$$I_D(T) \approx S\mu(T_r) \left(\frac{T}{T_r} \right)^{-m} C_{OX} (\eta - 1) V_T^2 \exp \left(\frac{V_{GS}(T) - V_{TH}(T)}{\eta V_T} \right) \quad (2.12)$$

By taking the ratio of I_D at T and T_r [$I_D(T)$ and $I_D(T_r)$] based on (2.12), we have

$$\frac{I_D(T)}{I_D(T_r)} = \left(\frac{T}{T_r} \right)^{2-m} \exp \left(\frac{q}{\eta k_B} \frac{A}{TT_r} \right) \quad (2.13)$$

where $A = V_{GS}(T)T_r - V_{GS}(T_r)T + V_{TH}(T_r)T - V_{TH}(T)T_r$

Since the transistor is biased by a PTAT current, $I_D(T)/I_D(T_r) = T/T_r$. In addition, $V_{TH}(T)$ can be approximated as

$$V_{TH}(T) = V_{TH}(T_r) - \theta(T - T_r) = V_{TH0} - \theta T \quad (2.14)$$

where θ is the T.C. of V_{TH} [63]. As such, $V_{GS}(T)$ can be obtained as

$$V_{GS}(T) = V_{TH0} + [V_{GS}(T_r) - V_{TH0}] \frac{T}{T_r} + (m-1) \frac{\eta k_B T}{q} \ln\left(\frac{T}{T_r}\right) \quad (2.15)$$

At the weak inversion region, since $V_{GS}(T_r) < V_{TH0}$, the second term shows a CTAT characteristic. The third term contributes a nonlinear temperature effect because of the $T \ln(T/T_r)$ term. Through a Taylor Series expansion, we can approximate $T \ln(T/T_r)$ as

$$T \ln(T / T_r) = T - T_r + (T - T_r)^2 / (2T_r) \quad (2.16)$$

Substituting (2.16) into (2.15), $V_{GS}(T)$ can be obtained as

$$V_{GS}(T) = V_{TH0} - (m-1) \frac{\eta k_B T_r}{2q} + [V_{GS}(T_r) - V_{TH0}] \frac{T}{T_r} + (m-1) \frac{\eta k_B}{2q T_r} T^2 \quad (2.17)$$

Since m is usually between 1.5 to 2 for CMOS transistors [86], the second-order (T^2) term is positive in (2.17). As a result, if a negative T^2 term is added to offset this nonlinear error, the objective of T.C. reduction can be achieved.

2.3.2. Circuit Implementation

To generate a negative T^2 term to offset the nonlinear temperature error in (2.17), the different temperature properties of Poly resistor and P+ diffusion resistor are used. The proposed V_{TH} sensor with current-mode second-order temperature compensation is shown in Fig. 2.4. It consists of a first-order Brokaw V_{TH} main circuit, a second-order temperature compensation current generator and an operational amplifier. The main circuit generates a current I_1 through a PTAT voltage source and a high resistive poly resistor (R_1). The second-order temperature compensation current (I_2) generator comprises a PTAT voltage source and a P+ diffusion resistor (R_5). When I_1 is dumped

Fig. 2.4: Proposed V_{TH} monitoring based voltage reference circuit.

into R_2 (high resistive poly), the temperature variability of R_1 and R_2 can cancel each other. A first-order PTAT voltage ($V_{I1} = V_{I1_1st} = 2I_1R_2$) is established. On the contrary, when I_2 is dumped into R_2 , both first-order and second-order temperature compensation voltages (V_{I2_1st} , V_{I2_2nd} , respectively, $V_{I2} = V_{I2_1st} + V_{I2_2nd} = I_2R_2$) are generated because of the different temperature properties of R_2 and R_5 . Finally, V_R ($=V_{I1}+V_{I2}=V_{I1_1st}+V_{I2_1st}+V_{I2_2nd}$) can compensate for both the first-order and second-order term in V_{GS1} in (2.17).

Figure 2.5 shows the temperature compensation principle of V_{TH} sensor in graphical illustration. As indicated, the T.C. difference between the poly resistor R_2 and the diffusion resistor R_5 yields a negative second-order compensation voltage term, which can compensate for the positive second-order term of V_{GS} in (2.17).

To ensure that an identical current flows through R_3 and R_4 ($R_3 = R_4$), as well as M_1 and M_2 , an operational amplifier is utilized to equalize the voltages V_A and V_B . The capacitor C_1 is used to increase power supply rejection (PSR) at high frequencies. The capacitor C_2 is added to maintain the stability of the loop. The working principle of the

V_{TH} sensor and the second-order temperature compensation effect are explained as follows.

Fig. 2.5: Temperature compensation in graphical illustration.

2.3.3. Working Principle

If M_1 and M_2 work in the weak inversion region, and assuming that $V_{TH1}(T) = V_{TH2}(T)$, $I_{DS1}(T) = I_{DS2}(T) = I_1$, we have $\Delta V_{GS} = V_{GS1} - V_{GS2} = \eta V_T \ln(S_2/S_1)$ according to (2.12). Hence, the currents I_1 and I_2 can be expressed in the form as $I_1 = [\eta V_T \ln(S_2/S_1)]/R_1(T)$ and $I_2 = [N\eta V_T \ln(S_4/S_3)]/R_5(T)$, respectively. $N(=S_9/S_8)$ is the current mirror ratio for M_9 to M_8 in Fig. 2.4. The output voltage is obtained as

$$\begin{aligned} V_{OUT} &= V_R + V_{GS1}(T) = 2I_1 R_2(T) + I_2 R_2(T) + V_{GS1}(T) \\ &= 2\eta \frac{k_B T}{q} \frac{R_2(T)}{R_1(T)} \ln\left(\frac{S_2}{S_1}\right) + N\eta \frac{k_B T}{q} \frac{R_2(T)}{R_5(T)} \ln\left(\frac{S_4}{S_3}\right) + V_{GS1}(T) \end{aligned} \quad (2.18)$$

where $V_{GS1}(T)$ is defined by (2.17). From (2.18), since R_1 and R_2 are both poly resistor and they have a similar T.C., $R_2(T)/R_1(T) \approx R_2(T_r)/R_1(T_r)$. In addition, based on a first-

order temperature modeling of $R_2(T)$ and $R_5(T)$, $TR_2(T)/R_5(T)$ in the second term of (2.18) can be approximated as

$$\begin{aligned} T \frac{R_2(T)}{R_5(T)} &= \frac{R_2(T_r) [1 + \alpha(T - T_r)]}{R_5(T_r) [1 + \beta(T - T_r)]} \\ &\approx \frac{R_2(T_r)}{R_5(T_r)} \{ [2(\alpha - \beta)T_r + 1]T + (\alpha - \beta)T^2 + (\alpha - \beta)T_r^2 \} \end{aligned} \quad (2.19)$$

using a Taylor Series expansion. In (2.19), α is the T.C. of $R_2(T)$ and β is the T.C. of $R_5(T)$. Since $\alpha < 0$, and $\beta > 0$, the T^2 term is negative. It can be used to offset the positive T^2 term in $V_{GS1}(T)$ in (2.17). Substituting (2.19) in (2.18), V_{OUT} can be obtained as

$$\begin{aligned} V_{OUT} &= V_{GS1}(T) + 2\eta \frac{k_B T}{q} \frac{R_2(T_r)}{R_1(T_r)} \ln\left(\frac{S_2}{S_1}\right) + N\eta \frac{k_B}{q} \frac{R_2(T_r)}{R_5(T_r)} \ln\left(\frac{S_4}{S_3}\right) \\ &\quad \times \{ [2(\alpha - \beta)T_r + 1]T + (\alpha - \beta)T^2 + (\alpha - \beta)T_r^2 \} \\ &\approx V_{TH0} \end{aligned} \quad (2.20)$$

From (2.20), by choosing the appropriate values for R_1 , R_2 and R_5 , V_{OUT} can be optimized to obtain a zero T.C., with its final value being approximately equal to V_{TH0} .

Figure 2.6(a) depicts the simulated V_{GS1} and V_{I2} ($V_{I2} = I_2 R_2$) and their slopes with respect to temperature. When the temperature increases, V_{GS1} decreases but the falling rate is continually reduced. This correlates with the analytical result in Section 2.3.1 that the T^2 term in $V_{GS1}(T)$ is positive. The second-order compensation voltage V_{I2} has a PTAT characteristic, with its positive slope decreasing as well. This confirms that the T^2 term in V_{I2} is negative. To compare the T.C. performance of V_{TH} sensors with and without the second-order compensation, a first-order Brokaw V_{TH} sensor is built and simulated. It is constructed by removing the second-order current generator in Fig. 2.4. In addition, resistor R_2 is increased to achieve optimal temperature compensation. To evaluate the performance of the circuit under process variations, Monte-Carlo (MC)

simulations are conducted. Transistor parameters including threshold voltage, mobility, and subthreshold slope factor are simulated across random process variations [71]. All the MC simulations in this Chapter are carried out with a sample size of 500 and 3 standard deviation (3σ) coverage. Figure 2.6(b) depicts the MC simulation results of T.C. for the first-order Brokaw circuit and the proposed V_{TH} sensor. The results suggest that the second-order temperature compensation reduces the mean T.C. of the V_{TH} sensor by 40%. It is noted that the standard deviation increases slightly with 1.8 ppm/ $^{\circ}C$. This fact stems from different variations for poly and diffusion resistors. However, the total first-order T.C. variation (Mean + Stdv.) of 81.7 ppm/ $^{\circ}C$ (first-order) is reduced to the T.C. of 53.5 ppm/ $^{\circ}C$ with first-order plus second-order compensation. This has confirmed that the second-order temperature compensation technique can reduce the nonlinear temperature effect of MOSFET V_{GS} and improve the temperature stability of a V_{TH} sensor.

Fig. 2.6: (a) Simulated V_{GS1} , V_{I2} and their slopes with respect to temperature variation. (b) Monte-Carlo simulation results for first-order Brokaw circuit and proposed temperature compensated V_{TH} sensor.

Figure 2.7 shows the simulated V_{OUT} under different temperature and supply voltages. It can be seen that the V_{TH} sensor can generate a stable output voltage when both temperature and supply varies. Figure 2.8 depicts the Monte-Carlos simulation

result for PSR @ 100 Hz. The mean PSR value is -38dB and the worst case PSR is still smaller than -30 dB.

Fig. 2.7 Simulated V_{OUT} under different supply voltages and temperatures.

Fig. 2.8 Monte-Carlo simulation results for PSR @ 100 Hz.

2.3.4. Results and Discussions

The proposed V_{TH} sensor is implemented in a UMC 65-nm CMOS process. The microphotograph is shown in Fig. 2.9. It occupies an active area of 0.0198 mm^2 .

Fig. 2.9: Microphotograph of the proposed V_{TH} sensor.

2.3.4.1. Measurement Setup and Calibration Procedure

To tackle the leakage effect of the I/O pads, a voltage buffer (non-inverting unity-gain Op-Amp) is added at the output of the V_{TH} sensor. The T.C. of the voltage buffer is also measured and subtracted from the measured output T.C. to get the actual T.C. performance of V_{TH} sensor.

Since R_1 , R_2 and R_5 may deviate from the design values due to process variations, a 4-bit binary weighted calibration is implemented for resistor R_2 . The calibration scheme is based on 2 temperature measurements. A successive approximation method is used in the process without exceeding maximum of 4 calibration steps. First, the voltage at the maximum temperature (90°C , V_{TMAX}) and the minimum temperature (-40°C , V_{TMIN}) are measured. Second, if V_{TMAX} is bigger than V_{TMIN} , this indicates that PTAT voltage is too strong. R_2 is then reduced. If V_{TMAX} is smaller than V_{TMIN} , this

indicates that PTAT voltage is too weak. R_2 is then increased. The calibration is conducted iteratively and stopped when $V_{TMAX} = V_{TMIN}$ [57].

2.3.4.2. Measurement Results

The V_{TH} sensor can operate from a supply of 0.75 V to 1.2 V with a temperature range of -40 °C to 90 °C. The power consumption measured at room temperature is 290 nW at a supply of 0.75 V. In this study, 15 samples were measured. Figure 2.10(a) depicts the measured V_{OUT} as a function of temperature at a 0.75 V supply, and shows that V_{OUT} is very stable across temperature variation for each sample. Figure 2.10(b) shows the DC output voltage against temperature at different supply voltages. Compared with the simulated results in Fig. 2.7, V_{OUT} becomes smaller due to the process variation. However, a stable V_{OUT} can still be achieved. This validates that the V_{TH} sensor can work well from 0.75 V to 1.2 V.

Fig. 2.10: (a) Measured output voltage V_{OUT} as a function of temperature for 15 samples with 0.75V supply voltage. (b) Measured output voltage V_{OUT} as a function of temperature for different supply voltages.

Figure 2.11(a) shows the distribution of V_{OUT} at room temperature. The measured mean output voltage (V_{OUT_MEAN}) is 474 mV with a standard deviation of 16 mV. Figure 2.11(b) depicts the measured T.C. distribution. Due to the proposed second-order compensation technique, the V_{TH} sensor achieves a minimum T.C. of 24 ppm/°C

and a maximum T.C. of 50.4 ppm/°C. The average T.C. is 40 ppm/°C with a standard deviation of 8.5 ppm/°C.

Fig. 2.11: (a) Distribution of V_{OUT} for 15 samples at room temperature. (b) Distribution of the T.C. performance metric for 15 samples.

Figure 2.12(a) illustrates the measured power supply rejection (PSR) for the V_{TH} sensor, which is -40 dB at 100 Hz and it's closed to the simulation results in Fig. 2.8. Figure 2.12(b) depicts the supply ripple response. When a sine wave ($f = 100$ Hz, amplitude = 100 mV_{pp}) is applied at the supply, the measured output ripple is about 1.04 mV_{pp}.

Fig. 2.12: (a) Measured PSR. (b) Measured power supply ripple response at $V_{DD} = 0.75$ V, $V_{ripple} = 100$ mV for the proposed V_{TH} sensor.

2.3.4.3. Scalability and Process Variations

Due to the precision analog design and the use of nonlinear terms and second-order effects, scaling cannot be directly applied. But the usual design steps for the V_{TH} sensor remain the same. Under different process technologies, based on (2.17) and (2.20), the ratio of R_1/R_2 and R_5/R_2 can be optimized to achieve first and second-order compensation, respectively. First, for the first-order compensation, R_1 and R_2 should be of the same type. Second, for a V_{GS} to have a positive nonlinear second-order term, the T.C. for R_5 must be positive whereas the T.C. for R_2 must be negative. On the contrary, for a V_{GS} to have a negative nonlinear second-order term, the T.C. for R_5 must be negative while the T.C. for R_2 must be positive. This fact will enable a low T.C. V_{TH} sensor to be designed with different technologies.

Process variations are discussed in two parts: (i) Die-to-Die (D2D) variations and (ii) Within-Die (WID) variations.

(i) Die-to-Die variations: All devices on the same die are assumed to be affected in the same way [50]. Since temperature compensation depends on resistor ratios, based on (2.20), the first-order compensation leads to approximately no change. In addition, the use of different resistor types for R_2 and R_5 mean that the variation in the R_2/R_5 ratio will lead to some deviation in the T.C. However, MC simulation results show that this T.C. drift is still low in the proposed V_{TH} sensor (Fig. 2.13(a)). Under D2D variations, the T.C. shows a 5.6 ppm/°C standard deviation.

(ii) Within-Die variations: In this scenario, devices on the same die are assumed to behave differently [50]. This local device mismatch also affects the behavior of the output. However, the MC simulation results (Fig. 2.13(b)) (T.C. standard deviation = 4.3 ppm/°C) illustrate that the V_{TH} sensor has a small sensitivity to WID variations.

Fig. 2.13: (a) Monte-Carlo simulation results of T.C. for die-to-die variations. (b) Monte-Carlo simulation results of T.C. for within-die variations.

To explain the effect using examples, the V_{TH} mismatch of M_1 and M_2 , R_3 and R_4 in Fig. 2.4 are then discussed next. If it is assumed that $V_{TH1} = V_{TH2} + \Delta V_{TH}$, where ΔV_{TH} is the mismatch error, based on (2.12), the generated non-ideal PTAT voltage (ΔV_{GS_n}) across R_1 can be obtained as

$$\Delta V_{GS_n} = V_{GS1} - V_{GS2} - (V_{TH1} - V_{TH2}) = \eta V_T \ln(S_2/S_1) + \Delta V_{TH} \quad (2.21)$$

If ΔV_{TH} is constant, an offset voltage ($V_{offset} = \Delta V_{TH} R_2/R_1$) will contribute to the V_{TH0} . Figure 2.14 (a) depicts V_{OUT} under MOSFET-devices-only WID variations. It shows that the standard deviation is only 4.6 mV. This is smaller than 1% of the mean value. In addition, even with an offset error, V_{OUT} can still link with process information so as to provide a threshold monitoring function.

In terms of the mismatch of R_3 and R_4 , if it is assumed that $R_3/R_4 = (1+\sigma)$, $V_A = V_B$ and $V_{TH1} = V_{TH2}$, where σ is the mismatch error (in ratio) between R_3 and R_4 , a non-ideal PTAT voltage is generated as follows:

$$\Delta V_{GS_n} = V_{GS1} - V_{GS2} = \eta V_T \ln(S_2/[(1+\sigma)S_1]) \quad (2.22)$$

From (2.22), the mismatch error of R_3 and R_4 modifies the slope of PTAT voltage, which subsequently changes the level of temperature compensation. Figure 2.14(b) depicts the T.C. under resistors-only WID variations, confirming that the T.C. is stable with typical variation.

Fig. 2.14: (a) Monte-Carlo simulation results of V_{OUT} for MOSFET-devices-only within-die variations. (b) Monte-Carlo simulation results of T.C. for resistors-only within-die variations.

2.3.4.4. Performance Comparison

The performance comparisons of the proposed V_{TH} sensor with the reported nanometer voltage reference circuits and V_{TH} sensors are depicted in Tables 2.1 and 2.2, respectively. Refer to Table 2.1, the voltage references [69, 70] display relatively larger T.C. values and significantly larger power. Despite another design [71] consumes smaller power and area, but it does not provide the process information based on the voltage generation method. Besides, the minimum T.C. is around 4 times and the maximum T.C. is more than 2 times with respect to this work. It turns out that this work offers good balanced performance metrics in nanometer voltage reference design. Refer to Table 2.2, the T.C. of the proposed V_{TH} sensor is close to that of the reported counterparts [61-63, 65] in large channel-length technologies. Table 2.3

presents the performance comparison of the proposed V_{TH} sensor with the BJT based bandgap voltage reference. It can be seen that the proposed V_{TH} sensor consumes the smallest power whilst achieve a comparable T.C. performance with respect to the BJT bandgap voltage reference. Most importantly, the proposed V_{TH} sensor can generate the V_{TH} of the transistor at 0 K and provide the process information. In summary, the proposed threshold monitoring circuit can provide good temperature stability, wide temperature range, low supply operation and relax the design difficulty to obtain lower T.C. in the context of design challenges in nanometer CMOS technology.

TABLE 2.1 PERFORMANCE COMPARISON OF THE PROPOSED V_{TH} SENSOR WITH OTHER REPORTED NANOMETER CMOS VOLTAGE REFERENCE CIRCUITS

	[69]	[69]	[70]	[71]	This Work
Year	2008	2008	2009	2012	2014
Technology (nm)	90	90	32	65	65
Temp. Range (°C)	10-100	5-100	0-125	-20-80	-40-90
V_{DD} (V)	0.55-1	0.55-1	0.9-1.4	0.5-2.5	0.75-1.2
V_{OUT} (mV)	251	243	540	330.1	474
Power (nW)	375000	547000	12600	0.24	290
Min. T.C. (ppm/°C)	263	160	962	89.1	24
Max. T.C. (ppm/°C)	N/A	N/A	N/A	118.2	50.4
Mean T.C. (ppm/°C)	N/A	N/A	N/A	N/A	40
Line Sens. (ppm/V)	119522	123457	N/A	3300	2423
PSR (dB) (@100 Hz)	N/A	N/A	N/A	-40	-40
Chip Area (mm²)	0.019	0.07	0.016	0.0009	0.0198
No. of Samples	18	16	N/A	17	15

TABLE 2.2 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER V_{TH} SENSOR WITH OTHER REPORTED V_{TH} SENSOR DESIGNS USING LONG CHANNEL-LENGTH TRANSISTORS

	[61]	[62]	[63]	[65]	This Work
Year	2007	2007	2009	2011	2014
Technology (μm)	0.35	0.35	0.35	0.13	0.065
Temp. Range ($^{\circ}\text{C}$)	0-80	-20-80	-20-80	-50-130	-40-90
V_{DD} (V)	0.9-4	0.95-3	1.4-3	0.7-1.8	0.75-1.2
V_{OUT} (mV)	670	741	745	501	474
Power (nW)	36	390 (@80 $^{\circ}\text{C}$)	300	210	290
Min. $T.C.$ (ppm/$^{\circ}\text{C}$)	10	38.8	7	23.8	24
Max. $T.C.$ (ppm/$^{\circ}\text{C}$)	N/A	40.1	45	41.1	50.4
Mean $T.C.$ (ppm/$^{\circ}\text{C}$)	N/A	39	15	29.3	40
Line Sens. (ppm/V)	2700	32524	20	337	2423
PSR (dB) (@100 Hz)	-47	-23.4 (@1kHz)	-45	N/A	-40
Chip Area (mm^2)	0.045	0.0759	0.055	0.023	0.0198
No. of Samples	20	3	17	12	15

TABLE 2.3 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER V_{TH} SENSOR WITH BANDGAP VOLTAGE REFERENCE CIRCUITS

	[54]	[53]	[56]	[57]	[58]	This Work
Year	1999	2002	2003	2007	2011	2014
Technology (μm)	0.4	0.6	0.6	0.35	0.16	0.065
Temp. Range ($^{\circ}\text{C}$)	27-125	0-100	0-100	-20-100	-40-125	-40-90
V_{DD} (V)	2.2-4	0.98	2-4	1.4	1.8	0.75-1.2
V_{OUT} (mV)	518	603	1142	858	1087.5	474
Power (μW)	4.62	17.64	46	162	99	0.29
Min. $T.C.$ (ppm/$^{\circ}\text{C}$)	N/A	N/A	N/A	N/A	5	24
Max. $T.C.$ (ppm/$^{\circ}\text{C}$)	N/A	N/A	N/A	N/A	12	50.4
Mean $T.C.$ (ppm/$^{\circ}\text{C}$)	± 59	15	5.3	12.4	N/A	40
Line Sens. (ppm/V)	N/A	N/A	626	N/A	N/A	2423
PSR (dB) (@100 Hz)	N/A	-44	-40	68	74	-40
Chip Area (mm^2)	0.1	0.24	0.057	1.152	0.12	0.0198
No. of Samples	23	1	1	1	61	15

2.4. Summary

In this Chapter, three V_{TH} sensor designs are reviewed. The temperature compensation principles and the design difficulties under nano-meter technology are discussed. In the proposed V_{TH} sensor topology, by using the different temperature properties of P+ diffusion and poly resistors, a current-mode based second-order temperature compensation effect is achieved. The simulation and measurement results have demonstrated that it has achieved better T.C. performance metrics than those of reported nanometer technology based voltage references. At the same time, its performance is also comparable with other reported V_{TH} sensor circuits using long channel-length CMOS technologies. Therefore, the proposed V_{TH} sensor is useful for on-chip sensing applications that require good temperature stability.

CHAPTER 3

REVIEW OF LDO REGULATORS

In this Chapter, the conventional output capacitor based LDO (OC-LDO) regulator topology is firstly discussed. This is followed by the review of output capacitorless (OCL-LDO) regulators based on different gain stage topologies. The stability and transient responses of the capacitor and capacitorless LDO regulators will be explored. Advantages and limitations of each topology are also presented. Finally, the layout techniques for LDO regulator are also described.

3.1. Conventional Output Capacitor LDO (OC-LDO) Regulator Structure

Fig. 3.1: Conventional buffer based LDO regulator.

The conventional buffer based OC-LDO regulator is shown in Fig. 3.1. It consists of an error amplifier, a buffer stage, a power transistor, a resistor feedback network and a voltage reference. The feedback signal is compared with the stable voltage reference (V_{REF}), thus generating a control signal at the gate of power transistor (M_p) to give a regulated output voltage of $(1+R_1/R_2)V_{REF}$. Due to the large size of M_p , there is a large parasitic capacitance (C_p) associated with the gate of power MOS which limits the response of the regulator.

This LDO regulator structure is intrinsically unstable because of the existence of three low-frequency poles (p_1 , p_2 and p_3) in the feedback loop. They are located at the output node, at the output of error amplifier and the gate of M_p . In usual practice, a zero is created using an off-chip capacitor (C_{out}) through its ESR (equivalent series resistance) which aims to cancel the pole at the output of error amplifier. Figure 3.2 shows the loop gain response of the conventional LDO regulator. With the addition of a low-impedance voltage buffer, the large parasitic capacitance C_p is tackled for the high output impedance of error amplifier. This pushes this parasitic pole to high frequency to stabilize the LDO regulator.

Fig. 3.2: Loop gain response for conventional buffer based LDO regulator.

The disadvantage of source follower implementation is that its voltage swing is restricted, especially under low supply voltage condition. Low output swing of buffer demands a large power transistor size, resulting in large parasitic capacitance as well as larger quiescent current to push p_3 to high frequency.

Refer to the transient responses of the conventional LDO regulator during load current (I_L) switching whilst prior to the feedback loop response, the output capacitor can function as a battery to source/sink current. Therefore, this permits a small undershoot/overshoot effect at the output voltage. The transient response time [1] can be expressed as

$$t_r = \frac{1}{BW_{CL}} + C_P \frac{\Delta V}{I_{sr}} \quad (3.1)$$

where BW_{CL} is the closed-loop bandwidth of the system, C_P is the parasitic capacitance at the gate of power transistor, ΔV is the voltage change associated with the C_P and I_{sr} is the slew rate limited current. For fast transient response, a large closed-loop bandwidth and slew rate are needed. If the loop bandwidth is extended, p_3 may locate inside the unity gain frequency (ω_{UGF}) which greatly limits the stability of LDO regulator. This is resolved at the expense of increasing quiescent power in the buffer stage so as to push p_3 beyond ω_{UGF} . Besides, fast transient implies high slew rate performance metric which is also translated to the large power consumption. These two factors contribute to the design tradeoff for power consumption.

3.2. Dynamic Biasing and Current Boosting in LDO Regulators

Fig. 3.3: Dynamic biased LDO regulator.

To overcome the potential large quiescent current problem in the topology depicted in Fig. 3.1, the dynamic biasing technique is implemented in the buffer stage design [11]. As illustrated in Fig. 3.3, it injects a I_L dependent biasing current into the buffer stage to enable the parasitic pole p_3 to be shifted to high frequency. When I_L increases, the buffer impedance is also simultaneously reduced so that it gives another aid for pushing the parasitic pole to higher frequency. This guarantees the stability of LDO regulator at all I_L conditions. Using the same concept in [87], an error amplifier with dynamic biasing with respect to I_L change is utilized. This improves the transient metrics whilst without sacrificing the quiescent power consumption.

During transient condition, a large current will flow to charge or discharge the parasitic capacitance C_p of power transistor. Such the large transient current only appears in the transient state instead of the steady state. A current boosting technique [6] is reported. It momentarily injects a current into the buffer stage enhance the transient performance of the LDO regulator. This provides a low-quiescent fast-transient solution.

3.3. Output Capacitorless LDO (OCL-LDO) Regulator

The conventional OC-LDO regulators usually rely on a large off-chip capacitor to form part of the frequency compensation in the design. From fully integration view point, it may not be favorable for on-chip applications. This increases the popularity on the research of OCL-LDO regulators. Based on the gain stage structures, a review of OCL-LDO regulators including the stability and transient performance is conducted in this section.

3.3.1. Single-Stage Error Amplifier Plus Power Transistor OCL-LDO Regulator Topology

Fig. 3.4: Single-stage error amplifier plus power transistor OCL-LDO regulator topology.

The topology in Fig. 3.4 shows the single-stage error amplifier plus the power transistor OCL-LDO regulator. The capacitor C_L represents the parasitic capacitance of the loading circuit. For the stability of the regulator, there are two poles inside unity gain frequency ω_{UGF} . If the transistor size of M_P is large, the parasitic capacitance C_{gd} of M_P becomes big such that it can serve as Miller compensation capacitor. The pole-splitting process generates a dominant low-frequency pole p_1 at the output of error

amplifier. At low I_L , the impedance at the output node is not low enough, causing a low-frequency pole p_2 associated with C_L . The loop gain frequency response of conventional OCL-LDO regulator at low I_L is presented in Fig. 3.5. To further stabilize the regulator, a Miller compensation capacitor can be added across the power transistor to ensure the location of p_1 at a sufficient lower frequency whilst p_2 at a sufficient higher frequency.

Fig. 3.5: Loop gain frequency response of the single-stage error amplifier plus power transistor OCL-LDO regulator at low I_L .

In order to drive the potential large size power transistor in the generic LDO architecture of Fig. 3.4, many well-known circuit techniques have been reported to increase the speed of the error amplifier [28, 31, 88, 89]. In [88], the topology is a push-pull output amplifier which relaxes the tradeoff between the small quiescent current and slew rate (SR) at the gate of power transistor. It is further improved in [28] in which a current subtractor is utilized to extend the attainable gain bandwidth (GBW). In [89], a class-AB amplifier together with an assistant push-pull output stage circuit is employed to improve the transient response. Since the transconductance (g_m)

of amplifier is intentionally made small to achieve stability, the GBW of regulator is small. This results in a large settling time. In [31], a class-AB transconductance amplifier (OTA) having large output current capability and output resistance is adopted. With the aid of a flipped voltage follower (FVF) based tail current booster and a direct voltage spike detection SR enhancement circuit, the regulator can settle fast with improved transient responses.

In modern CMOS technology, the output impedance of transistor becomes relatively smaller than that of long-channel counterpart. This often yields a small loop gain factor in the feedback loop of Fig. 3.4. The price paid for that will be translated to the poor regulation accuracy.

3.3.2. Multi-Stage Error Amplifier Plus Power Transistor Regulator Topology

Fig. 3.6: Multi-gain stage error amplifier plus power transistor OCL-LDO regulator topology.

To guarantee good regulation accuracy, the loop gain of the regulator should be high. Therefore, the error amplifier in Fig. 3.4 will be realized in a form of multi-gain stage (2 stages or more) topology. Figure 3.6 illustrates a generic OCL-LDO regulator architecture featuring a multi-gain stage based error amplifier with a power transistor output stage.

In Fig. 3.6, g_{mi} denotes the transconductance while R_i and C_i are the equivalent output resistance and lumped output parasitic capacitance of the i -th gain stage, respectively. R_O is the effective output resistance which includes the output resistance of power transistor as well as the loading resistance R_L . As indicated, the feedback system displays a four-pole (p_{-3dB} , p_2 , p_3 and p_O) characteristic. In general design, p_O locates at a lower frequency than that of p_2 and p_3 . Hence, p_2 and p_3 must be allocated to a high frequency to ensure the stability. The typical implementation of 2nd and 3rd gain stages is to keep node N_2 as a low impedance node ($R_2 \approx 1/g_m$) whereas node N_P as a high impedance node [20, 24, 25, 27, 30]. Since C_P is large on the basis of a large power transistor M_P , p_3 is low especially under low power constraint. As reported in [24], two parasitic poles are generated with frequency inversely proportional to $C_L R_O$. To stabilize the LDO regulator, C_L must be small. Moreover, since R_O is inversely proportional to I_L , a minimum I_L (e.g. 3 mA) is required to ensure a small R_O [24]. This restricts the application of this topology for wide C_L and I_L range application.

Turning to the transient speed of the LDO regulator architecture in Fig. 3.6, owing to the fixed bias and high output impedance characteristics in the 3rd gain stage, the speed at gate of power transistor becomes slow. This leads to large overshoot/undershoot as well as large settling time for the output voltage during I_L switching. Meanwhile, the fixed bias in 1st stage error amplifier limits the unity gain frequency of the feedback loop. This restricts the speed of the LDO regulator. To tackle this issue, the adaptively bias technique [13, 25, 27, 30] can be realized to increase the biasing current of 1st stage error amplifier when I_L increases. Unfortunately, it is hard to control for regulator's stability because of positive feedback involved in the adaptively bias circuit.

3.3.3. Flipped-Voltage-Follower (FVF) Based OCL-LDO Regulator Topology

Fig. 3.7: OCL-LDO regulator with Flipped Voltage Follower (FVF).

To reduce the impedance of the output node, a FVF based LDO regulator is proposed [22] as shown in Fig. 3.7. The output voltage is the reference voltage plus the V_{GS} of M_1 . The impedance of the output node at low I_L becomes $1/g_{m1}$ which is considered to be small. During transient transition, M_1 senses the output voltage changes and serves as a common gate amplifier. It amplifies the signal and couples it to the gate of power transistor. The FVF structure does not need any compensation capacitor to stabilize the LDO regulator as proved in [22]. Unfortunately, a large power transistor size is often required to reduce the swing of gate voltage to avoid jeopardizing the operation region of M_2 and current source transistor. This introduces large parasitic capacitance at the gate of M_p . As a result, the speed of the regulator is limited under low power constraint. To address the limited bias current in the FVF topology in Fig. 3.7, a voltage spike detection circuit is added [23] to increase the biasing current momentarily during load current switching. Hence, the biasing current

during transient event is significantly increased. This momentarily current can effectively increase the speed of regulator without consuming large quiescent current. Since both circuits [22, 23] suffer from limited loop gain, they display poor load regulation, line regulation and PSR performance. In [24], an extra gain stage is inserted to increase the loop gain of the conventional FVF LDO regulator. This yields the additional high impedance node. This turns out that the stability is sacrificed at low I_L . For a C_L of 50 pF, the minimum I_L is 1.5 mA at $V_{DD} = 0.75$ V and 3 mA at $V_{DD} = 1.2$ V. When C_L increases, the corresponding increase of minimum I_L is not favored in the low-quiescent LDO regulator design.

In summary, the OCL-LDO regulator eliminates the off-chip capacitor to achieve voltage regulation and hence can be fully integrated with the loading circuit and reduce the cost. However, without the output capacitor to form the dominant pole and source/sink current during load current switching, the loop stability and fast transient response are still the main design challenges for the OCL-LDO regulators, especially under low voltage, low quiescent current and wide C_L range conditions.

3.4. Layout Techniques

To accomplish high-performance analog circuit, a proper layout is essential. This is because the device properties including matching, parasitic capacitances, parasitic resistance, noise and so forth are all dependent on the critical circuit layout. Turning to the layout aspect of LDO regulator, the layout considerations are mainly focused on the matching of the transistors' pairs and the power transistor layout with minimum parasitic.

3.4.1. Transistor Matching

Transistor matching is a very important issue in analog circuit layout. The main purpose for layout matching is to reduce the mismatch offset arising from the fabrication process. Many circuit building blocks, such as current mirrors, input differential pairs and current mirror active loads involve matching with pair. There are two main techniques to match the transistors: inter-digitized technique and common-centroid technique. Figure 3.8 gives an exemplary symmetrical layout technique using common-centroid techniques. Device A and device B are laid out interleaved at the top, and are reversely order in the bottom. This gives the independence of process in both X and Y gradient directions. The dummy transistors are added at both sides to reduce lateral etching effect.

Fig. 3.8: Common centroid layout example.

3.4.2. Power Transistor Layout

The layout of power transistor is critical for a good performance regulator since it introduces large parasitic in the feedback loop and draws large current from the supply to the output. First, to reduce the on-resistance (R_{on}), the device size (W/L ratio) has to be large and the minimum channel length is used. Second, to minimize the distributed gate resistance, multi-fingers structures should be used. The multi-fingers are arranged to form a transistor array in which the fingers are connected to interleaved source and drain metallization. This is then connected to higher level of metal by contacts and vias up to the top metal level. Figure 3.9 depicts the typical multi-fingers connection of the transistor array which not only reduces the gate resistance but it also reduces the junction capacitances [90, 91].

Fig. 3.9: Typical multi-finger layout structure.

In general, R_{on} can be reduced by increasing the number of transistors in parallel configuration. However, at some point when the paralleled transistor number increases, R_{on} does not continue to reduce and it tends to be saturated. This is mainly because the interconnect resistance becomes the main portion of R_{on} . To further reduce the R_{on} , some layout design techniques have been reported. Figure 3.10 shows a modified version of the multi-finger layout technique [92]. In this layout, wider metal layers are used to minimize the R_{on} . Nevertheless, a tradeoff exists between the width of metal layer and the number of contacts for drain/source.

Fig. 3.10: A modified multi-finger layout structure.

Waffle transistor layout technique is another choice for the power transistor. Waffle transistor layout is depicted in Fig. 3.11. It achieves lower R_{on} by using a mesh of horizontal and vertical poly gate stripes to divide the source and drain implant into an array of squares. After connecting these drain and source contact alternately, one can arrange four drains around each source and four sources around each drain [93]. The drains/sources are connected together by a diagonal stripes formed by metal layers. In general, the waffle layout offers a better packing density than that of the multi-finger layout [92]. Despite of the CMOS design rule (e.g. minimum metal width and spacing) of the metal layer, the drain/source diffusion area should be made larger to accommodate the metal layer. Moreover, in more recent CMOS process, the R_{on} of the transistor is often dominated by the metallization. This causes the improvement of R_{on} less significant.

Fig. 3.11: A Waffle layout structure.

3.4.3. Metallization

In layout design for power transistor, the total width of the metal wire to supply and collect the large amount of load current also needs to be considered. The parasitic resistances of the metal layer (R_M) will cause additional voltage drop across the metal wire or bus of the regulator which may jeopardize the performance.

As discussed in [1], the general steps for passing output load current I_L from V_{DD} (or V_{IN}) to V_O through the power transistor M_P are listed as follows. (1) Steer I_L laterally from V_{DD} to a low-impedance plane (or planes) above power transistor M_P , (2) channel I_L down vertically to M_P 's input terminal, (3) direct I_L up vertically from M_P 's output terminal to another low-impedance plane (or planes), and (4) guide I_L laterally to output pad V_O . To reduce the vertical resistance, the first-level metal should cover the entire ohmic surface area of each source and drain areas. As depicted in Fig. 3.12, the first-to-second level vias carry the current vertically to low-impedance second-level metal buses.

Fig. 3.12: Top view of a vertical-metallization strategy for a wellled power MOSFET from the semiconductor interface to second-level metal planes [1].

In sourcing current from the bonding pad to M_P (or steering the current from M_P to the bond pads), a lateral metal track above M_P drives down (or “picks up”) parts of its current as it traverses across the IC. For instance, when sourcing current from the output terminal of M_P (source region in Fig. 3.12) to the output pad, the total current in the lateral metal plane increases as more current from underlying current-carrying semiconductor regions is passed to the metal plane. If a constant metal width lateral metal plane is used, the current density throughout the plane is inconsistent. This will lead to current crowding and inefficient use of the available metal area. As a result, the lateral metal width should be designed to be increase when the total current passing through it increases. The best metallization strategy of second- to third-level metal planes is illustrated in Fig. 3.13 [1]. The third-level metal is drawn in triangle thus equal current-flux regions are formed to carry increasing or decreasing currents. To further reduce the metal resistance, multi-level metals are normally used for power routing as the higher levels of metal have a lower sheet resistance.

Fig. 3.13: Top view lateral metallization strategy for a welled power MOSFET from second- to third-level metal planes and bond pads [1].

3.5. Summary

This Chapter first gives a review of conventional output capacitor LDO regulators. The stability and transient performances are discussed. Followed by the review of OCL-LDO regulators using different gain-stage topologies. For the topology with single-stage error amplifier and power transistor, the stability is easily achieved but at the price of limited regulator accuracy by the small loop gain. For the multi-stage error amplifier plus power transistor topology, the regulation accuracy is improved owing to an enhanced loop gain. However, the stability at low I_L and the transient speed are sacrificed due to the additional high impedance node. Finally, the FVF based LDO regulator can give a low output impedance, simple structure and fast response characteristics.

In addition, the layout techniques for LDO regulator are discussed. Transistor matching, design techniques pertaining to the power transistor to achieve low R_{on} are described.

CHAPTER 4

WIDE LOAD CAPACITANCE RANGE OCL-LDO REGULATOR: TYPE-I

In this Chapter, the Type-I wide CL range OCL-LDO regulator is introduced. The circuit structure, stability analysis, design methodology, and the other performances are discussed in detail.

4.1. Introduction

In System-on-Chip (SoC) environment pertaining to large scale digital circuits like DSP core(s) and memory banks, the effective supply line parasitic capacitance is large. To drive such circuits, the LDO regulator should have the ability to drive a wide load capacitance (C_L) range (few hundred pF to few nF) [38]. However, in most of the reported OCL-LDO regulator designs, they usually drive a maximum C_L up to tens of pF or 100 pF [21, 22, 24, 27, 28, 30]. Few designs can drive relatively large C_L [18, 23, 26, 29, 34].

In [18], a FVF topology is used as an output driver which gives a very fast speed with a recovering time of 0.54 ns. Since a quiescent current of 6 mA is used in this LDO regulator, it leads to unavoidable large quiescent power consumption. In addition, only a maximum C_L of 600 pF is reported. A direct voltage spike detection technique is reported in [23] that can support a C_L of 100 pF and 1 nF. Due to the LDO regulator utilizes a simple folded FVF topology, the loop gain is fairly limited. This in turn limits the regulation accuracy of the LDO regulator. In [26], an active

compensation scheme is realized in order to enable the LDO regulator to drive a C_L up to 1 nF. However, several poles and zeros exist within the unity gain frequency (ω_{UGF}), leading to complicated pole-zero tracking. Any mismatch between poles and zeros will contribute slower transient response. In [29], a current amplifier is adopted to multiply the Miller capacitor which can extend the C_L driving capability to 1 nF. However, the design needs a large compensation capacitor (tens of pF) to ensure stable operation. This may lead to relatively larger silicon area and slower transient speed. A Dual-Summed Miller Frequency Compensation (DSMFC) technique is implemented in a FVF based LDO regulator topology [34]. The LDO regulator has been demonstrated in a very wide C_L range. However, for the DSMFC network, the inverting driving transistor for the second Miller amplifier is biased by a high impedance current source with an open loop topology. To ensure a reliable dc operating region of the additional Miller stage, the power transistor has to be sized larger at the expense of larger silicon area so as to reduce the voltage swing at the Miller node. This will degrade the transient performances of the regulator.

In view of the need to support a wide C_L range and good transient performance metrics under low quiescent power design objectives, new circuit techniques are demanded in the design of OCL-LDO regulators. In this report, two circuit techniques are proposed to extend the C_L driving ability whilst maintain good transient performances. In this Chapter, the first type wide C_L range LDO regulator uses the DSMFC technique but with a simpler structure and a reliable DC biased dual-summed Miller amplifier [94] is discussed. It can be drive a C_L ranging from 10 pF to 10 nF with a total compensation capacitance (C_C) of 8 pF. The second type wide C_L range LDO regulator will be discussed in subsequent Chapter.

4.2. Circuit Topology

The schematic of LDO regulator using DSMFC technique is shown in Fig. 4.1(a). It contains a folded FVF first gain stage, a non-inverting second gain stage and a power MOS transistor. The LDO regulator is compensated using a DSMFC block (dash enclosed area). It contains a standard Miller compensation capacitor (C_{m1}) and an additional Miller compensation stage (C_{m2} , M_D and R_X). This realization permits a reliable DC operating point to be achieved in absence of high impedance node.

The control voltage for M_1 is generated through a symmetrical OTA amplifier which is shown in Fig. 4.1(b). Since the maximum load capacitor is in nF range, to reduce the settling time from overshoot, an overshoot reduction branch (C_B , R_B and M_7) is implemented to increase the sinking current momentarily.

4.3. Stability and PSR Analysis and Discussions

This section discusses the stability of the proposed LDO regulator using DSMFC technique. The small-signal mode, loop gain transfer function, poles and zeros locations, phase margin (PM), damping factor and gain margin (GM), and the sizing of the dual Miller compensation capacitors are investigated in detail.

4.3.1. Small-Signal Model and Transfer Function

The stability of proposed LDO regulator is examined using its small-signal model depicted in Fig. 4.2. It is obtained by breaking the feedback loop at the output branch as shown in Fig. 4.1(a). In the small-signal model, g_{mi} denotes the transconductance whereas R_i and C_i are the equivalent output resistance and lumped output parasitic capacitance of the i -th gain stage, respectively. C_{m1} and C_{m2} are the 1st and 2nd Miller compensation capacitors. R_O is the effective output resistance which includes the output resistance of power transistor and the loading resistance R_L . C_L is the load capacitance which has a value ranging from 10 pF to 10 nF.

Fig. 4.2: Small-signal model of the proposed FVF LDO regulator.

The loop gain transfer function is derived with the following assumptions: (i) C_1 , $C_D \ll C_2 \ll C_{m1}$, C_{m2} and C_L ; (ii) $g_{m1}R_1$, $g_{m2}R_2$ and $g_{md}R_D \gg 1$. It is obtained and expressed by (4.1), where A_{dc} is the dc loop gain and z_1 , z_2 , z_3 are the three zeros.

$$\begin{aligned}
T(s) &= \frac{v_{fbout}}{v_{fbin}} = - \frac{A_{dc} \left(1 + \frac{s}{z_1}\right) \left(1 + \frac{s}{z_2}\right) \left(1 + \frac{s}{z_3}\right)}{1 + as + bs^2 + cs^3 + ds^4} \\
A_{dc} &= g_{m1}g_{m2}g_{mp}R_1R_2R_O, \quad z_1 = -\frac{1}{C_{m2}R_D}, \\
z_2 &\approx \frac{-C_{m1} - 2R_2\sqrt{C_{m1}C_2g_{m2}g_{mp}}}{2C_{m1}C_2R_2}, \quad z_3 \approx \frac{-C_{m1} + 2R_2\sqrt{C_{m1}C_2g_{m2}g_{mp}}}{2C_{m1}C_2R_2}, \\
a &= C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O + C_LR_O, \\
b &= C_{m2}g_{md}R_DR_1(C_2R_2 + C_LR_O) + C_{m1}C_{m2}g_{m2}g_{mp}R_1R_DR_2R_O, \\
c &= C_{m2}C_2C_Lg_{md}R_DR_1R_2R_O + (g_{md}R_O + 1)C_{m1}C_{m2}C_2R_DR_1R_2 + C_{m1}C_{m2}C_LR_DR_1R_O, \\
d &= C_{m1}C_{m2}C_2C_LR_DR_1R_2R_O.
\end{aligned} \tag{4.1}$$

Based on the design parameters, $z_{2,3}$ locate at high frequencies. Thus it can be ignored in the stability analysis. In addition, the loop gain transfer function has two real poles (p_{-3dB} , p_2). As such, it can be simplified in the form as

$$T(s) = - \frac{A_{dc} \left(1 + \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right) \left(1 + \frac{s}{p_2}\right) \left(1 + \frac{c}{b}s + \frac{d}{b}s^2\right)} \tag{4.2}$$

4.3.2. Poles and Zero Locations

Since the C_L varies from 10 pF to 10 nF with the load current I_L switching between 0 and 50 mA, the stability of the LDO regulator is discussed at six different cases that deal with the C_L corners at different I_L . They are given as follows: (1) Large C_L with low I_L , (2) Large C_L with moderate I_L , (3) Large C_L with high I_L , (4) Small C_L with low I_L , (5) Small C_L with moderate I_L , (6) Small C_L with high I_L .

Based on (4.1) and (4.2), the poles and zeros locations for six cases are summarized in Table 4.1 and their relative locations are shown in Fig. 4.3(a) and Fig. 4.3(b) for large and small C_L , respectively. The loop gain transfer function shows that the first case denotes the system with four real poles whereas the other five cases denote the system having two real poles plus one pair of complex poles. Each case is explained as follows:

Case 1: Large C_L with low I_L

In this case, both power transistor's output resistance (R_{dsp}) and the equivalent load circuit resistance (R_L) are high. As a result, $R_O \approx 1/g_{m1}$. Due to a small bias current in M_1 , R_O is still fairly large (around 17 k Ω). It forms a low frequency dominant pole with the large C_L . p_2 is located at a lower frequency than that of z_1 , contributing a partial cancellation effect. In addition, due to the DSMFC, p_3 is pushed to a higher frequency by an extra frequency quantifying term, g_{md}/C_{m1} . As for p_4 , the gain of the last stage is small due to small g_{mp} . Thus the Miller effect arising from the C_{gd} of the power transistor is negligible, which results in a small C_2 . Therefore, p_4 is also located at a high frequency.

Case 2: Large C_L with moderate I_L

Due to large g_{mp} and moderate R_O , the loop gain is the highest in this range and the stability of the LDO regulator is at its worst condition. p_{-3dB} is formed by the Miller

TABLE 4.1 POLES AND ZERO LOCATIONS FOR SIX CASES

Parameter	z_1	p_{-3dB}	p_2	p_3^*	p_4^*
(Case 1) Large C_L /Low I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_L R_O}$	$-\frac{1}{C_{m2}g_{md}R_1R_D}$	$-\left(\frac{g_{md}}{C_{m1}} + \frac{g_{m2}g_{mp}R_2}{C_L}\right)$	$-\frac{1}{C_2R_2}$
(Case 2) Large C_L /Moderate I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_{m1}g_{m2}g_{mp}R_1R_2R_O}$	$-\frac{C_{m1}g_{m2}g_{mp}R_2}{C_{m1}C_{m2}g_{m2}g_{mp}R_2R_D + C_{m2}C_Lg_{md}R_D}$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L} + \frac{g_{md}}{C_{m1}C_2R_2}}$	
(Case 3) Large C_L /High I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O}$	$-\left(\frac{g_{md}}{C_{m1}g_{m2}g_{mp}R_2R_O} + \frac{1}{C_{m2}R_D}\right)$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}}$	
(Case 4) Small C_L /Low I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O}$	$-\left(\frac{g_{md}}{C_{m1}g_{m2}g_{mp}R_2R_O} + \frac{1}{C_{m2}R_D}\right)$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L} + \frac{g_{md}}{C_{m1}C_2R_2}}$	
(Case 5) Small C_L /Moderate I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_{m1}g_{m2}g_{mp}R_1R_2R_O}$	$-\frac{1}{C_{m2}R_D}$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}}$	
(Case 6) Small C_L /High I_L	$-\frac{1}{C_{m2}R_D}$	$-\frac{1}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O}$	$-\left(\frac{g_{md}}{C_{m1}g_{m2}g_{mp}R_2R_O} + \frac{1}{C_{m2}R_D}\right)$	$\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}}$	

* p_3 and p_4 form a pair of complex poles except for large C_L with low I_L condition.

* p_{i_l} , z_{i_l} , p_{i_m} , z_{i_m} , p_{i_h} , z_{i_h} represent the i^{th} pole and zero for low, moderate and high load current respectively.

Fig. 4.3: Loop gain of the proposed FVF LDO regulator with poles and zero locations for (a) large C_L , (b) small C_L .

compensation capacitor C_{m1} . More importantly, similar to Case 1, an additional term, $g_{md}/(C_{m1}C_2R_2)$, is generated for defining complex poles' frequency in the DSMFC scheme. As a result, the complex pole pair $|p_{3,4}|$ are shifted to a higher frequency which ensures the stability of the regulator is achieved.

Case 3: Large C_L with high I_L

In this case, R_O is approaching to its minimum value because of small R_{dsp} and small R_L . This leads to a small gain for the power transistor gain stage. The two Miller compensation effects are close to each other and form the dominant pole together. The second pole and zero (z_1 is around 2 times of p_2) exhibit a good cancellation. The complex poles are located at higher frequency due to large g_{mp} .

Case 4: Small C_L with low I_L

Due to small C_L , C_LR_O no longer forms a low frequency pole. The dominant pole is governed by two Miller compensation capacitors (C_{m1} and C_{m2}). A good pole and zero cancellation is also achieved in this case. Similar to Case 2, the complex poles are shifted to a higher frequency by the additional term generated by the DSMFC. The stability of the LDO regulator is ensured.

Case 5: Small C_L with moderate I_L

Similar to Case 2, the dominant pole is created by the standard Miller capacitor (C_{m1}). The complex poles are located at high frequency because of the small C_L . Thus they will not affect the stability of the LDO regulator.

Case 6: Small C_L with high I_L

Similar to Case 5, it is apparent that the stability of the LDO regulator at this condition can easily be achieved due to large g_{mp} and small C_L .

With the DSMFC technique, the dominant pole is formed through the summing Miller effect which offers better stability. Besides, when comparing with Single Miller Compensation (SMC) counterpart, the DSMFC also shifts the non-dominant pole(s) to a higher frequency, especially under the following three conditions: (i) large C_L with low I_L , (ii) large C_L with moderate I_L , and (iii) small C_L with low I_L . Since the DSMFC technique addresses the conservative stability issue for both small and large C_L , the proposed LDO regulator can achieve driving capability for a wide load capacitance range across the whole load current range.

Figure 4.4(a) and 4.4(b) depict the open-loop gain and phase responses at $I_L = 0$, 0.5 mA, 5 mA, and 50 mA for $C_L = 10$ nF and $C_L = 10$ pF, respectively. It can be observed that the simulated results match with the analysis. It also demonstrates that

the proposed FVF LDO regulator can achieve stability for both large and small C_L corners at different I_L .

Fig. 4.4: Simulated open-loop gain and phase responses at different I_L for (a) $C_L = 10$ nF and (b) $C_L = 10$ pF.

The PM, GM and unity gain frequency across the whole C_L range with different I_L are shown in Fig. 4.5. It can be observed that the LDO regulator with DSMFC technique achieves a minimum PM of 50° and a minimum GM of 8 dB. For benchmark comparison, the SMC for this LDO regulator topology without using the second Miller amplifier is applied. The total compensation capacitance in the proposed LDO regulator and the SMC LDO regulator are sized to be the same (8 pF). Figure 4.6 depicts the PM, GM and unity gain frequency simulation results. As can be seen from Fig. 4.6(a), based on a 50° PM, the SMC regulator is stable to support a load capacitor ranging from 10 pF to 250 pF. Moreover, when comparing the unity gain frequency simulation results in Fig. 4.5(c) and Fig. 4.6(c), the proposed LDO regulator using the DSMFC technique provides a larger unity gain frequency with respect to that of SMC LDO regulator. This suggests that the speed of the LDO regulator will be faster in the proposed LDO regulator.

Based on the above analysis and simulation results, the proposed FVF LDO regulator using DSMFC technique is able to maintain stable operation over the whole C_L range of 10 pF – 10 nF under the load current varying from 0 to 50 mA. With respect to the SMC counterpart, it achieves a wider C_L range at the same time a larger unity gain frequency.

Fig. 4.5: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of C_L at different I_L using DSMFC.

Fig. 4.6: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of C_L at different I_L using SMC.

4.3.3. Phase Margin under Different C_L

As can be seen in Fig. 4.5(a), at small I_L condition, the PM plot shows a “quadratic” behavior. When C_L increases, the PM drops from 83° to around 60° and then increases again. If C_L continues to increase, the PM will drop again. The phenomenon is due to shifting of the pole when C_L varies from small to large values. The analysis can be divided into two regions: (i) complex pole region for small C_L and (ii) real pole region for large C_L .

Region i: In this region, owing to small C_L , the dominant pole p_{-3dB} is formed by the two Miller compensation capacitors (C_{m1} and C_{m2}). It gives a C_L independent unity gain frequency ω_{UGF} as

$$\omega_{UGF} = \frac{g_{m1}g_{m2}g_{mp}R_1R_2R_O}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O} \quad (4.3)$$

In addition, the loop system gives a pair of complex poles which are given by

$$|p_{3,4}| = \sqrt{\frac{g_{m2}g_{mp}}{C_2C_L} + \frac{g_{md}}{C_{m1}C_2R_2}} \quad (4.4)$$

From (4.4), it can be seen that the location of the complex poles is inversely proportional to C_L . As C_L increases, the complex poles' frequency decreases and appears to be closer to ω_{UGF} . As a consequence, the PM is reduced and the stability of LDO regulator becomes worse. This explains why the PM plot in Fig. 4.5(a) shows a continuous drop first when C_L is less than 250 pF.

Region ii: For large C_L , the output capacitor also plays a role in the dominant pole formation. The dominant pole is given as

$$p_{-3dB} = \frac{1}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O + C_LR_O} \quad (4.5)$$

which leads to a C_L dependent ω_{UGF} as follows:

$$\omega_{UGF} = \frac{g_{m1}g_{m2}g_{mp}R_1R_2R_O}{C_{m2}g_{md}R_DR_1 + C_{m1}g_{m2}g_{mp}R_1R_2R_O + C_LR_O} \quad (4.6)$$

Since the zero z_1 generated from the DSMFC is fixed at $1/C_{m2}R_D$ (4.1) and the second pole (p_2) locates at a lower ($g_{md}R_1$ times) frequency, the loop phase response gives a small peak around the zero location. Based on this reason, when ω_{UGF} continues to reduce as C_L increases, the PM will increase and then drop again, depending on the relative location of ω_{UGF} and the fixed zero z_1 .

4.3.4. Damping Factor and Gain Margin under Different C_L

Damping factor is critical for the LDO regulator stability when a pair of complex poles exist in the loop gain transfer function (case 2 to case 6 in Table 4.1). Consider the second-order terms in (4.2) with a standard form as

$$1 + \frac{c}{b}s + \frac{d}{b}s^2 = 1 + \left(\frac{2\zeta}{\omega_o}\right)s + \left(\frac{s}{\omega_o}\right)^2 \quad (4.7)$$

where ζ is the damping factor and ω_o is the frequency of the complex poles.

Although the DSMFC increases the frequency of the complex poles (ω_o) which in turn improves the PM and GM, the ζ of the complex poles should be designed properly to avoid large frequency peaking and maintain a good GM. If it is assumed that the second pole p_2 and the zero z_1 generated by the DSMFC cancel each other, based on [25], the relationship between ζ and PM as well as ζ and GM in a second-order system is approximately as follows:

$$PM \approx 90^\circ - \tan^{-1} \left[\frac{2\zeta \left(\omega_{UGF} / \omega_O \right)}{1 - \left(\omega_{UGF} / \omega_O \right)^2} \right] \quad (4.8)$$

$$GM \approx 20 \times \log \left(\frac{2\zeta \omega_O}{\omega_{UGF}} \right) \quad (4.9)$$

From (4.8) and (4.9), a large ζ increases the GM but it gives a large negative phase shift which reduces the PM. On the other hand, a small ζ reduces the GM and makes a sharp phase drop which can lead to a 0° PM.

Based on transfer function in (4.1), the general expression for the ζ in the second-order system defined in (4.7) is obtained as

$$\zeta = \frac{1}{2} \frac{(C_2 g_{md} R_O R_2 + C_{m1} R_O) C_L + (g_{md} R_O + 1) C_{m1} C_2 R_2}{C_{m1} R_O R_2 \sqrt{C_2 C_L g_{m2} g_{mp}}} \quad (4.10)$$

It is noted that the GM without taking log function is $2\zeta \omega_O / \omega_{UGF}$. Therefore, the ζ and $2\zeta \omega_O / \omega_{UGF}$ for 5 cases exhibiting a complex pole pair (case 2 – case 6 in Table 4.1) are summarized in Table 4.2. For case 1 in Table 4.1 (large C_L , low I_L), the system displays four real poles, thus it is not included in Table 4.2 and the respective analysis.

From Table 4.2, when C_L increases, the observation is in the following. (i) For low I_L and small C_L (case 4), ζ increases. (ii) For moderate I_L (case 2 and case 5), ζ will reduce first and then increase again. (iii) For high I_L (case 3 and case 6), ζ decreases. Therefore, the minimum ζ ($\zeta_{(\min)}$) for low I_L occurs at $C_L = 10$ pF whereas for high I_L , $\zeta_{(\min)}$ occurs at $C_L = 10$ nF. For moderate I_L , $\zeta_{(\min)}$ occurs at middle C_L range. The value of $\zeta_{(\min)}$ can be approximated as

$$\zeta_{(\min)} \approx \frac{1}{C_{m1} R_O} \sqrt{\frac{C_{m1} (C_2 g_{md} R_2 R_O + C_{m1} R_O)}{g_{m2} g_{mp} R_2}} \quad (4.11)$$

TABLE 4.2 DAMPING FACTOR AND GM FOR CASES EXHIBITING COMPLEX POLE PAIR

Parameter	ζ ($C_L \uparrow$)	GM* ($C_L \uparrow$)
(Case 2)[#] Large C_L Moderate I_L	$\alpha \sqrt{\frac{C_L}{C_2 g_{m2} g_{mp}}}$ $\uparrow$	$\frac{\beta(C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1} R_2}$ $\uparrow$
(Case 3) Large C_L High I_L	$\frac{1}{2R_O} \sqrt{\frac{C_2}{C_L g_{m2} g_{mp}}}$ $\downarrow$	$\frac{C_{m2} g_{md} R_D + C_{m1} g_{m2} g_{mp} R_2 R_O}{C_L g_{m1} g_{m2} g_{mp} R_2 R_O^2}$ $\downarrow$
(Case 4)[#] Small C_L Low I_L	$\frac{1}{2R_2} \sqrt{\frac{C_L}{C_2 g_{m2} g_{mp}}}$ $\uparrow$	$\frac{\beta(C_{m2} g_{md} R_D + C_{m1} g_{m2} g_{mp} R_2 R_O)}{C_2 g_{m1} g_{m2} g_{mp} R_2^2 R_O}$ $\uparrow$
(Case 5) Small C_L Moderate I_L	$\frac{1}{2R_O} \sqrt{\frac{C_2}{C_L g_{m2} g_{mp}}}$ $\downarrow$	$\frac{C_{m1}}{C_L g_{m1} R_O}$ $\downarrow$
(Case 6) Small C_L High I_L	$\frac{1}{2R_O} \sqrt{\frac{C_2}{C_L g_{m2} g_{mp}}}$ $\downarrow$	$\frac{C_{m2} g_{md} R_D + C_{m1} g_{m2} g_{mp} R_2 R_O}{C_L g_{m1} g_{m2} g_{mp} R_2 R_O^2}$ $\downarrow$

$\uparrow$ and $\downarrow$ indicates the increase or decrease of ζ and GM when C_L increases, respectively.

* GM without taking log function.

$$\# \alpha = \frac{(C_2 g_{md} R_2 + C_{m1})}{2C_{m1} R_2}, \beta = \sqrt{1 + \frac{C_L g_{md}}{C_{m1} g_{m2} g_{mp} R_2}}$$

which occurs at

$$C_{L_{-\zeta}(\min)} \approx \frac{C_{m1} C_2 R_2}{C_2 g_{md} R_2 R_O + C_{m1} R_O} \quad (4.12)$$

Based on the above analytical expressions, the $\zeta_{(\min)}$ for different I_L conditions and their respective C_L location ($C_{L_{-\zeta}(\min)}$) are summarized in Table 4.3. They are governed by the design parameters in which the denoted symbols have their usual meanings.

Consider GM of the LDO regulator depicted in Table 4.2, when C_L increases, it follows the same trend as that of ζ under low, moderate and high I_L cases. Therefore, (i) At low I_L , the minimum GM ($GM_{(\min)}$) occurs at $C_L = 10$ pF. (ii) At high I_L , $GM_{(\min)}$ occurs at $C_L = 10$ nF. (iii) At moderate I_L , $GM_{(\min)}$ occurs at middle C_L range. The $GM_{(\min)}$ for three different I_L conditions and their respective C_L location ($C_{L_{-GM}(\min)}$)

are also summarized in Table 4.3. Turning to the GM plot of the proposed LDO regulator in Fig. 4.5(b), at $I_L = 0$, the minimum GM location is at $C_L = 10$ pF. On the other hand, at $I_L = 5$ and 50 mA, the minimum GM location is at $C_L = 10$ nF. This matches the $GM_{(\min)}$ location analysis for low and high I_L conditions, respectively.

At moderate I_L , through derivation and Binomial approximations, the minimum GM (without taking log function) is approximated as

$$GM_{(\min)}^* \approx \frac{(C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1} R_2} + \sqrt{\frac{2 g_{md} (C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1}^2 g_{m2} g_{mp} R_2^2 R_O}} \quad (4.13)$$

which occurs at

$$C_{L_GM(\min)} \approx C_{m1} R_2 \sqrt{\frac{2 C_2 g_{m2} g_{mp}}{g_{md} R_O (C_2 g_{md} R_2 + C_{m1})}} \quad (4.14)$$

To demonstrate the analysis with an example, at $I_L = 0.5$ mA, the design parameters are given as follows: $C_{m1} = 4$ pF, $C_2 = 1.04$ pF, $g_{m2} = 239$ μ S, $g_{mp} = 9$ mS, $g_{md} = 31$ μ S, $R_2 = 81$ k Ω , and $R_O = 540$ Ω . Using (4.14), it gives a $C_{L_GM(\min)}$ of 2.06 nF. The GM plot in Fig. 4.5(b) also shows that the minimum GM occurs around $C_L = 2$ nF. This validates that the analytical expression for the minimum GM location correlates well with the simulation result.

TABLE 4.3 MINIMUM DAMPING FACTOR AND MINIMUM GM WITH THEIR RESPECTIVE C_L LOCATIONS

Parameter	$\zeta_{(\min)}$	$C_{L_ \zeta(\min)}$	$GM_{(\min)}^*$	$C_{L_ GM(\min)}$
Low I_L	$\frac{1}{2R_2} \sqrt{\frac{C_{L(\min)}}{C_2 g_{m2} g_{mp}}}$	$C_{L(\min)}^{\#}$	$\frac{C_{m2} g_{md} R_D + C_{m1} g_{m2} g_{mp} R_2 R_O}{C_2 g_{m1} g_{m2} g_{mp} R_2^2 R_O} \sqrt{1 + \frac{C_{L(\min)} g_{md}}{C_{m1} g_{m2} g_{mp} R_2}}$	$C_{L(\min)}^{\#}$
Moderate I_L	$\frac{1}{C_{m1} R_O} \sqrt{\frac{C_{m1} (C_2 g_{md} R_2 R_O + C_{m1} R_O)}{g_{m2} g_{mp} R_2}}$	$\frac{C_{m1} C_2 R_2}{C_2 g_{md} R_2 R_O + C_{m1} R_O}$	$\frac{(C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1} R_2} + \sqrt{\frac{2 g_{md} (C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1}^2 g_{m2} g_{mp} R_2^2 R_O}}$	$C_{m1} R_2 \sqrt{\frac{2 C_2 g_{m2} g_{mp}}{g_{md} R_O (C_2 g_{md} R_2 + C_{m1})}}$
High I_L	$\frac{1}{2R_O} \sqrt{\frac{C_2}{C_{L(\max)} g_{m2} g_{mp}}}$	$C_{L(\max)}^{\#}$	$\frac{C_{m2} g_{md} R_D + C_{m1} g_{m2} g_{mp} R_2 R_O}{C_{L(\max)} g_{m1} g_{m2} g_{mp} R_2 R_O^2}$	$C_{L(\max)}^{\#}$

C_{L(min)} = 10 pF, C_{L(max)} = 10 nF. * GM_(min) without taking log function.

4.3.5. Sizing of Dual Miller Compensation Capacitors

The dimensions of the two Miller compensation capacitors (C_{m1} and C_{m2}) are depending on the gain of the main loop and the dual-summed amplifier. To analyze the influence, two cases of C_{m1} and C_{m2} are discussed and compared with the nominal case. It is assumed that the nominal case is at $C_{m1} = C_{m2}$ and the total sum is kept at a constant (8 pF in this design).

Case I: $C_{m1} > C_{m2}$. For large C_L under low I_L (case 1 in Table 4.1), a large C_{m1} degrades the stability of the LDO regulator. This is because large C_{m1} gives a lower frequency p_3 that leads to a poor PM. Under moderate I_L (case 2 in Table 4.1), the Miller effect is strong because of large C_{m1} . The stability of LDO regulator is improved. For small C_L under low and moderate I_L (case 4 and case 5 in Table 4.1), large C_{m1} improves the stability of the LDO regulator due to a stronger pole splitting effect. This occurs when the gain of the second stage plus the power transistor gain is larger than the gain of the dual-summed amplifier, which is especially true under low and moderate I_L . As for high I_L for both small and large C_L (case 3 and case 6 in Table 4.1), the stability improvement is small due to a small power transistor gain. This results in a similar Miller compensation effect for C_{m1} and C_{m2} .

Case II: $C_{m1} < C_{m2}$. Under this case, the LDO regulator stability is in opposite effect from those described in Case I ($C_{m1} > C_{m2}$). Therefore, it is not repeated here.

Based on the analysis in Case I and Case II, the relative PM and GM with reference to the nominal case of $C_{m1} = C_{m2}$ is summarized in Table 4.4 when C_{m1} and C_{m2} change their values in different combinations. The symbol “+” represents PM and GM increase whereas the symbol “—” represents PM and GM decrease with respect to the nominal case that $C_{m1} = C_{m2}$.

Table 4.5 gives the simulated PM and GM for the capacitor pair (C_{m1} , C_{m2}) which

corresponds to the design values of (5 pF, 3 pF), (4 pF, 4 pF) and (3 pF, 5 pF). For example one, at $I_L = 0$ mA (low I_L) and $C_L = 10$ pF (small C_L), when $C_{m1} = 5$ pF, $C_{m2} = 3$ pF, both PM and GM are larger than that of nominal case ($C_{m1} = 4$ pF, $C_{m2} = 4$ pF). For example two, at $I_L = 0$ mA (low I_L) and $C_L = 10$ nF (large C_L), when $C_{m1} = 5$ pF, $C_{m2} = 3$ pF, both PM and GM are smaller than the nominal case. This confirms that the simulation results on the size of C_{m1} and C_{m2} correlate well with the expected behavior as indicated in Table 4.4.

TABLE 4.4 RELATIVE PM AND GM FOR DIFFERENT C_{m1} & C_{m2} COMBINATIONS WITH REFERENCE TO NOMINAL CASE

Parameter	$C_{m1} > C_{m2}$			$C_{m1} < C_{m2}$		
I_L	<i>Low</i>	<i>Moderate</i>	<i>High</i>	<i>Low</i>	<i>Moderate</i>	<i>High</i>
Large C_L	—	+	+	+	—	—
Small C_L	+	+	+	—	—	—

TABLE 4.5 PM AND GM FOR DIFFERENT C_{m1} & C_{m2} COMBINATIONS

Parameter	$C_{m1} = 5$ pF $C_{m2} = 3$ pF			$C_{m1} = 4$ pF $C_{m2} = 4$ pF			$C_{m1} = 3$ pF $C_{m2} = 5$ pF		
I_L (mA)	0	0.5	50	0	0.5	50	0	0.5	50
10 pF (PM)	84	90	90	83	90	90	81	90	90
10 pF (GM)	9	21	—	8	20	—	7	18	—
10 nF (PM)	45	61	87	50	58	86	54	54	84
10 nF (GM)	40	12	14	40.5	11.5	12	41	11	10

— GM is too high and it is out of the simulation range.

4.3.6. Power Supply Rejection Analysis

The power supply rejection of LDO regulator indicates the ability to immune against the supply variation. Figure 4.7 depicts the schematic of the LDO regulator with power supply noise injection paths (in Red arrows).

Fig. 4.7 Schematic of the LDO regulator with power supply noise injection paths.

The PSR of the regulator is analyzed in low, moderate and high frequency ranges. To simplify the analysis, the loop gain of the regulator in (4.2) is assumed to be one-pole system within unity-gain frequency (UGF), which can be expressed as $T(s) = A_{dc} / (1 + s/p_{-3dB})$. Thus, the regulated output impedance can be expressed as

$$\begin{aligned}
 z_{reg} &= \frac{z_{out} \parallel R_{dsp}}{T(s)} \\
 &= \frac{z_{out} \parallel R_{dsp}}{A_{dc}} (1 + s/p_{-3dB}) z_{reg} = \frac{z_{out} \parallel R_{dsp}}{T(s)} \\
 &= \frac{z_{out} \parallel R_{dsp}}{A_{dc}} (1 + s/p_{-3dB})
 \end{aligned} \tag{4.15}$$

where $z_{out} = R_L \parallel (1/sC_L)$ and stands for the effective load impedance, R_{dsp} is the output impedance of the power transistor [95]. The PSR of the LDO regulator is analyzed in three regions: (i) low frequency, (ii) moderate frequency and (iii) high frequency. It is assumed the supply noise is ΔV_{DD} .

(i) At low frequency, for path 1, assume M_{11} - M_{14} and M_{16} - M_{17} are matched with each other, the noise for V_{CTRL} can be expressed as

$$\begin{aligned}
 \Delta V_{CTRL} &\approx \frac{(R_{ds17} \parallel R_{ds14}) / A_{CTRL}}{(R_{ds17} \parallel R_{ds14}) / A_{CTRL} + R_{ds14}} \Delta V_{DD} \\
 &\approx \frac{(R_{ds17} \parallel R_{ds14})}{A_{CTRL} R_{ds14}} \Delta V_{DD} \\
 &= \frac{\Delta V_{DD}}{g_{m9} R_{ds14}}
 \end{aligned} \tag{4.16}$$

After ΔV_{CTRL} is applied to M_1 , it goes through the first and second gain stage, the noise at node N_2 due to path 1 can be expressed as

$$\begin{aligned}
 \Delta V_{N2_1} &= -g_{m1} R_1 g_{m2} R_2 \Delta V_{CTRL} \\
 &= -\frac{g_{m1} R_1 g_{m2} R_2}{g_{m9} R_{ds14}} \Delta V_{DD}
 \end{aligned} \tag{4.17}$$

where g_{mi} and R_i stands for the transconductance of transistor M_i and equivalent output resistance of the i -th gain stage as that in Section 4.3.1.

For path 2, the supply noise will change the source voltage of M_2 and generate a noise current, this current will be mirrored to N_2 and generate a noise voltage at N_2 as

$$\Delta V_{N2_2} = g_{m2} R_2 \Delta V_{DD} \quad (4.18)$$

For path 3, since V_{B1} can be tracked with V_{IN} due to the diode transistor M_{B1} , thus the only way for the supply noise injecting into N_2 is due to limited R_{ds5} which can be expressed as

$$\Delta V_{N2_3} = \frac{R_{ds4}}{R_{ds4} + R_{ds5}} \Delta V_{DD} \quad (4.19)$$

For path 4, at low frequency, the capacitor C_{m1} has a very high impedance, supply noise cannot be coupled to N_1 leading to a zero noise contribution at V_{OUT} from path 4. As such, the total noise at N_2 can be expressed as

$$\begin{aligned} \Delta V_{N2} &= \Delta V_{N2_1} + \Delta V_{N2_2} + \Delta V_{N2_3} \\ &= -\frac{g_{m1} R_1 g_{m2} R_2}{g_{m9} R_{ds14}} \Delta V_{DD} + g_{m2} R_2 \Delta V_{DD} + \frac{R_{ds4}}{R_{ds4} + R_{ds5}} \Delta V_{DD} \\ &\approx g_{m2} R_2 \Delta V_{DD} - \frac{g_{m1} R_1 g_{m2} R_2}{g_{m9} R_{ds14}} \Delta V_{DD} \\ &= \left(1 - \frac{g_{m1} R_1}{g_{m9} R_{ds14}} \right) g_{m2} R_2 \Delta V_{DD} \end{aligned} \quad (4.20)$$

Finally, regarding path 5, there are two ways for the supply noise injecting into output. The first way is due to the non-zero V_{GS} of M_P . The second way is due to the limited R_{dsp} of M_P . Based on (4.20), the noise at the output can be derived as

$$\Delta V_{OUT} = g_{mp} z_{out_reg} \left[1 - \left(1 - \frac{g_{m1} R_1}{g_{m9} R_{ds14}} \right) g_{m2} R_2 \right] \Delta V_{DD} + \frac{z_{out_reg}}{z_{out_reg} + R_{dsp}} \Delta V_{DD} \quad (4.21)$$

As such, the PSR of the LDO regulator at low frequency can be expressed

$$\begin{aligned}
PSR &= g_{mp} z_{out_reg} \left[1 - \left(1 - \frac{g_{m1} R_1}{g_{m9} R_{ds14}} \right) g_{m2} R_2 \right] + \frac{z_{out_reg}}{z_{out_reg} + R_{dsp}} \\
&\approx g_{mp} \frac{(1 + s/p_{-3dB}) [R_L \parallel (1/g_{m1}) \parallel R_{dsp}]}{A_{dc}} \left[1 - \left(1 - \frac{g_{m1} R_1}{g_{m9} R_{ds14}} \right) g_{m2} R_2 \right] + \frac{(1 + s/p_{-3dB}) [R_L \parallel (1/g_{m1}) \parallel R_{dsp}]}{A_{dc} R_{dsp}} \\
&= \frac{(1 + s/p_{-3dB}) [R_L \parallel (1/g_{m1}) \parallel R_{dsp}]}{A_{dc}} \left\{ g_{mp} \left[1 - \left(1 - \frac{g_{m1} R_1}{g_{m9} R_{ds14}} \right) g_{m2} R_2 \right] + \frac{1}{R_{dsp}} \right\}
\end{aligned} \tag{4.22}$$

From (4.22), it can be seen that a good PSR can be achieved at low frequency by control the design parameters of g_{m1} , g_{m2} , g_{m9} , and A_{dc} . In addition, when frequency is larger than p_{-3dB} , the PSR will starts to drop as the loop gain starts to drop when frequency increases.

(ii) At moderate frequency, the loop gain of the LDO regulator equals or smaller than 1. The Miller compensation capacitor shorts the gate and drain nodes of M_D , forcing it to work as a diode transistor. As a result, the supply noise will directly inject to node N_1 through M_D and couple to V_{OUT} through C_{m1} . The PSR for this range is around 0 dB.

(iii) At high frequency, capacitor C_L shorts the output to ground, the PSR of the LDO regulator becomes smaller when frequency increases.

Figure 4.8 depicts the simulated PSR of LDO regulator under $I_L = 50$ mA for $C_L = 10$ pF, 100 pF, 1 nF and 10 nF, respectively. It can be seen that the PSR of LDO regulator follows the theoretical prediction and validates the analysis above: (i) At low frequency, the PSR of the regulator is determined by the feedback loop gain and shows a zero at p_{-3dB} . (ii) At moderate frequency, the PSR of the LDO regulator is around 0 dB. (iii) At high frequency, the PSR becomes smaller due to the output capacitor

filtering effect. For a large capacitor, the filtering effect will be stronger and the PSR will reduce at a lower frequency as indicated in Fig. 4.8.

Fig. 4. 8 Simulated PSR of the LDO regulator under $I_L = 50$ mA for different C_L .

4.4. Simulation Results and Performance Comparison

This Section presents the simulation results together with discussions. The performance comparison with the reported state-of-the-art OCL-LDO regulators is also investigated.

4.4.1. Simulation Results and Discussions

The proposed FVF LDO regulator using DSMFC technique is realized in a UMC 65-nm CMOS process. The compensation capacitors C_{m1} and C_{m2} are each in 4 pF. It consumes a quiescent current of 23.7 μ A at typical process and room temperature with 1.2 V voltage supply. The LDO regulator provides a 1 V output voltage with a maximum of 50 mA I_L . More importantly, it is able to drive a C_L range of 10 pF – 10 nF with good transient response. Figure 4.9 shows the transient responses for the LDO regulator with full current step (0 to 50 mA) at four different C_L values. When I_L switches between 0 and 50 mA with a 100 ns edge time, the undershoots are 41 mV, 40 mV, 46 mV and 58 mV whereas the overshoots are all close to 19 mV for $C_L = 10$ pF, 100 pF, 1 nF and 10 nF, respectively.

Fig. 4.9 Transient simulation results for I_L switching between 0 to 50 mA at $C_L = 10\text{pF}$, 100pF , 1nF and 10nF (I_L time delay is introduced to differentiate the plot).

To demonstrate the robustness of the proposed design, Table 4.6 lists the PM and GM, quiescent current (I_Q), load regulation, power supply rejection (PSR) and the load transient responses of the LDO regulator under extreme temperatures and process corners. Except the PM and GM, all the other parameters are obtained with $C_L = 100\text{pF}$. The PM and GM are simulated across the whole C_L range and I_L range. The minimum values or worst case values are obtained and presented in Table 4.6. For the load transient responses, two different load current switching steps (0 to 50 mA, and 1 mA to 50 mA) are used.

From Table 4.6, it can be concluded that the proposed LDO regulator is stable even under process and temperature variations with sufficient PM ($> 45^\circ$) and GM ($> 6\text{ dB}$).

Moreover, the LDO regulator's transient performance does not change significantly for different corners, especially when I_L switches between 1 mA to 50 mA.

TABLE 4.6 PERFORMANCE SUMMARY UNDER PROCESS AND TEMPERATURE CORNERS

Parameter	27 °C	- 40 °C				90 °C			
Corner	TT	SS	SF	FS	FF	SS	SF	FS	FF
PM_{min} (degree)	50.4	50.9	55.4	55.5	56.1	45.3	44.9	55.4	54.9
GM_{min} (dB)	7.8	6.1	6.9	6.5	7.4	8.2	9.1	8.7	9.9
I_Q (μA)	23.7	14.1	18.1	19.2	25.1	24.7	26.4	32.6	41.4
Load Reg. (μV/mA)	34	24	22	24	26	66	86	64	94
PSR (dB)	-52	-47.6	-53	-48.2	-55	-38.7	-39.3	-41.7	-38.9
ΔV_{OUT_U1} (mV)	40	34.1	35.7	33.4	31.7	63.7	74.5	56.6	73.9
ΔV_{OUT_O1} (mV)	18.1	20.4	17.5	17.4	15.5	29.1	26.3	26.5	17.3
T_{SETTLE1} (μs)	1.65	1.27	1.31	1.12	1.24	1.52	1.8	1.54	1.7
ΔV_{OUT_U2} (mV)	25.7	24.4	21.2	21.1	18.2	41.5	33.1	34.6	32.5
ΔV_{OUT_O2} (mV)	18.2	20.1	16.2	16.4	14.1	29.7	25.3	26.5	22.1
T_{SETTLE2} (μs)	0.94	0.79	0.66	0.56	0.62	0.98	0.97	0.99	0.87

* TT = Typical , SS = Slow Slow, SF = Slow N Fast P, FS = Fast N Slow P, FF = Fast Fast.

ΔV_{OUT_U1}, ΔV_{OUT_O1}, T_{SETTLE1} and ΔV_{OUT_U2}, ΔV_{OUT_O2}, T_{SETTLE2} represent the undershoot, overshoot and settling time for I_L switching from 0-50 mA and 1-50 mA, respectively.

4.4.2. Performance Comparison

Performance comparison between the proposed LDO regulator with other reported OCL-LDO regulators is presented in Table 4.7. To compare the C_L driving ability and the frequency compensation efficiency, the maximum C_L to the total compensation capacitance ratio ($C_{L(max)}/C_C$) is introduced. As indicated in Table 4.7, with the DSMFC technique, the proposed LDO regulator achieves the widest C_L range and the highest $C_{L(max)}/C_C$ ratio.

To compare the load transient performance, the OCL-LDO regulator figure-of-merit (FOM) [24] is adopted. It is given by

$$FOM = K \left(\frac{\Delta V_{OUT} \times I_O}{\Delta I_{OUT}} \right) \quad (4.23)$$

where K is the edge time ratio defined as

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}} \quad (4.24)$$

In Table 4.7, the smallest edge time (100 ps in [18]) is used as the reference while the others are normalized values. To get a fair comparison, all the parameters of the proposed LDO regulator is simulated at $C_L = 100$ pF. Furthermore, some of the LDO regulators [23, 24] were tested with some amount of minimum I_L . Therefore, two FOMs are obtained for the proposed FVF LDO regulator. The first one utilizes a I_L switching from 0 to 50 mA and vice versa, and the second one is based on the I_L switches between 1 mA to 50 mA. From Table 4.7, it can be observed that the proposed LDO regulator achieves a comparable or better FOM when compared with those of reported OCL-LDO regulators. It also gives reasonable and good results for other performances like load regulation, line regulation, settling time and PSR.

Comparing with the original LDO regulator [34] with wide load capacitance range driving capability, the proposed topology displays better transient performance due to a smaller power transistor, a simple non-inverting gain stage, smaller compensation capacitors and an increased quiescent power.

TABLE 4.7 PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS

Parameter	[18]	[21]	[22]	[23]	[24]	[26]	[27]	[30]	[34]	This Work	
Year	2005	2007	2008	2010	2010	2012	2012	2013	2013	2013	
Technology (μm)	0.09	0.35	0.35	0.35	0.09	0.09	0.35	0.065	0.065	0.065	
V_{IN} (V)	1.2	3	1.2-1.5	0.95-1.4	0.75-1.2	1.2	1.2	1.2	1.2	1.2	
V_{OUT} (V)	0.9	2.8	1	0.7-1.2	0.5-1	1	1	1	1	1	
Dropout Voltage (mV)	300	200	200	200	200	200	200	200	200	200	
I_{Q} (μA)	6000	65	95	43	8	408	28	0.9	13.2	23.7 [#]	
I_{OUT} (max) (mA)	100	50	50	100	100	100	100	100	50	50	
Total On-Chip Cap. (C_{T} , pF)	600	21	0	6	7	1.8	10	4.5	10	9	
Total Comp. Cap. (C_{C} , pF)	N/A	21	N/A	N/A	N/A	1.6	9	1.5	10	8	
Load Cap. Range (C_{L} , F)	N/A	0-100p	N/A	0, 100p, 1n	0-50p	0-1n	0-100p	0-100p	10p-10n [†]	10p-10n [†]	
Line Reg. (mV/V)	N/A	23	18	N/A	3.78	4.3	0.39	4.7	217	8.89	
Load Reg. ($\mu\text{V}/\text{mA}$)	1800	560	280	400	100	3	78.2	300	133	34	
PSR @1kHz, $I_{\text{L}} = 50\text{mA}$ (dB)	N/A	-57	N/A	N/A	-44	-56	-49.8	N/A	N/A	-52	
T_{SETTLE} (μs)	N/A	15	0.3	3	5	N/A	N/A	6	0.925	1.65	
ΔV_{OUT} (mV)	90	90	N/A	70	114	35	105	68.8	341.6	40	25.7 [*]
ΔI_{OUT} (mA)	100	50	50	99	97	100	100	100	50	50	49 [*]
Edge Time (μs)	0.0001	1	0.5	1	0.1	0.01	1	0.3	0.5	0.1	0.1 [*]
Edge Time Ratio K	1	10000	5000	10000	1000	100	10000	3000	5000	1000	1000 [*]
FOM	0.0054	1.17	N/A	0.304	0.0094	0.014	0.294	0.0019	0.45	0.019	0.012 [*]
$C_{\text{L(max)}}/C_{\text{C}}$	N/A	4.76	N/A	N/A	N/A	625	11.11	66.67	1000	1250	

The quiescent current includes the current consumptions of the biasing circuit and the OTA control voltage generator.

† Load capacitance range under worst process and temperature variations.

* Transient performance for I_{L} switches between 1 mA and 50 mA.

4.5. Summary

Due to the large parasitic capacitance at the supply line of the digital circuit, the LDO regulator need support wide load capacitance range with good transient performance metrics. In this Chapter, a FVF based LDO regulator with Dual-Summed Miller Frequency Compensation (DSMFC) is presented. Implemented with a simple resistive-loaded inverting amplifier, the DSMFC not only forms the low frequency dominant pole together with the conventional Miller compensation, it also shifts the non-dominant pole(s) to a higher frequency, especially under low and moderate load currents. The detailed stability analysis and simulation investigations have demonstrated that the proposed LDO regulator topology can support wide load capacitance range (10 pF to 10 nF) for different load current conditions whilst maintaining very good transient performance. It reaches a comparable or better FOM and achieves the highest $C_{L(max)}/C_C$ ratio with respect to other reported OCL-LDO regulator topologies. Therefore, it is useful for wide load capacitance range applications.

In this topology, R_2 is designed to be high whereas R_P is designed to be dominantly small ($\approx 1/g_m$). With this implementation, the 3rd gain stage can be dynamically biased which will increase the charging/discharging rate of V_P . As a result, the speed of the regulator is greatly improved with respect to the conventional topology (Fig. 3.3). It is important to note that C_P and R_2 may be large. They lead to large $C_P R_P$ and $C_2 R_2$, respectively. Based on Routh–Hurwitz stability criterion, the large time constant $C_2 R_2$ and $C_P R_P$ may introduce a right-half-plane (RHP) pole. To address this issue, a negative current feedback (NCF) technique is employed to avoid the RHP pole formation which is shown in Fig. 5.2.

Fig. 5.2: Proposed Negative Current Feedback (NCF) topology embedded in multi-gain stage in a LDO regulator.

In the NCF block depicted in Fig. 5.2, the current sensor senses the voltage V_P and generates a transconductance current $g_{mf}V_P$ (g_{mf} is the transconductance of the current sensor). The generated current is then fed back to the node N_2 . Not only does the feedback current increase the biasing current of 2nd stage as the first effect, it also forms a local negative current feedback loop (NCF loop in Fig. 5.2) as the second effect. Combining these two effects, the output impedance at node N_2 is reduced from R_2 to R_{2f} (R_{2f} is the negative current feedback loaded impedance at node N_2). As such,

both C_2R_{2f} and the regulator loop gain are reduced. This permits the feedback system to fulfill the Routh–Hurwitz stability criterion without introducing RHP pole. In addition, the NCF technique adds another advantage by shifting the non-dominant poles to a higher frequency. Hence the stability of the LDO regulator can be attained in the context of wide range of capacitive load (C_L) and load current (I_L).

However, there are two tradeoff issues in the design of NCF LDO regulator. They are given as follows: (i) The gain of 2nd stage is reduced because of a smaller R_{2f} . This in turn reduces the total loop gain of the LDO regulator, thus sacrificing some regulation accuracy. (ii) The negative feedback current reduces the charging/discharging rate of the node N_2 , which can reduce the transient speed. In view of the two drawbacks, a weighted current feedback (WCF) circuit technique [96] is further proposed to tackle the limitations arising from the foundation NCF technique.

5.2. Proposed Weighted Current Feedback Technique

Figure 5.3 shows a LDO regulator architecture using the WCF circuit technique. It comprises a fixed first gain stage, two variable gain stages (2nd and 3rd gain stages), a WCF block, a power transistor M_P , an overshoot reduction block and a frequency compensation network.

The shadowed area embodies the 2nd, 3rd gain stages as well as the WCF circuit (dash enclosed box). In the WCF circuit, two sense transistors (M_{a1} and M_{a2} , size of $M_{a2} > \text{size of } M_{a1}$) sense the same voltage V_P and each generates respective feedback current (I_{a1} , I_{a2}) at the output of 2nd gain stage. Moreover, the diode transistor M_{a3} is added in series with M_{a4} to control the operating region of M_{a2} during the change of I_L . The working principle of the WCF technique can be explained from Fig. 5.4. (i) At low I_L (Fig. 5.4(a)), both M_{a1} and M_{a2} are weakly biased for small negative current feedback. Each 2nd and 3rd gain stage works as a normal inverting amplifier. (ii) At moderated I_L (Fig. 5.4(b)), both M_{a1} and M_{a2} are designed to work in saturation region. Two feedback currents (I_{a1} , I_{a2} and $I_{a2} > I_{a1}$) are generated and fed back to the node N_2 . This results in a strong negative current feedback to the 2nd stage. (iii) At high I_L (Fig. 5.4(c)), only M_{a1} works in saturation region to give a small negative current feedback. M_{a2} is forced to work in linear region by the two diode transistors, M_{a3} and M_{a4} . Hence, the negative current feedback is reduced. Owing to this weighted control mechanism in the WCF technique, the impedance at the node N_2 as well as the gain of 2nd stage can be dynamically managed. Therefore, with reference to the proposed NCF technique, the advantages are as follows: (i) The gain of the WCF LDO regulator can be maintained reasonably well across the whole I_L range such that better regulation accuracy can be achieved. (ii) The charging/discharging rate of node N_2 is increased at high I_L , which results in faster transient speed.

Fig. 5.3: A LDO regulator architecture using the WCF technique.

Fig. 5.4: Simplified schematic of 2nd, 3rd gain stages and WCF for (a) low I_L , (b) moderate I_L , and (c) high I_L .

The 3rd gain stage is loaded by a resistor R_X and a diode transistor M_{d1} . The output impedance of this gain stage ($R_p \approx (1/g_{md1})//R_X$, g_{md1} representing the transconductance of M_{d1}) reduces when I_L increases. In this way, the resistor and diode transistor load provides an adaptive bias when I_L changes. This subsequently increases the speed of 3rd gain stage.

Turning to the frequency compensation design, a combined frequency compensation scheme using both cascode and Miller compensation techniques is adopted. The dominant pole is mainly formed by the cascode compensation capacitor whilst a small Miller compensation capacitor is utilized to reduce the Q factor of complex poles.

To complete the LDO architecture, an overshoot reduction block [30] is employed to reduce the overshoot magnitude and the settling time through a momentary discharging current.

5.3. Dynamic Impedance Reduction and Small-Signal Model for WCF LDO Regulator

To investigate the negative current feedback loaded impedance R_{2f} at the node N_2 , the small-signal model of the WCF LDO regulator is depicted in Fig. 5.5. It is obtained by breaking the loop at the output node as shown in Fig. 5.3. In the small-signal model, g_{mi} , R_i , and C_i have their usual meanings as defined in Section 5.1. Particularly, C_c is the cascode compensation capacitor whereas C_m is the Miller compensation capacitor. C_L is the load capacitance which has a value ranging from 470 pF to 10 nF.

Fig. 5.5: Small-signal model of the WCF LDO regulator.

Refer to Fig. 5.5, the total gain of the WCF feedback loop (A_{WCF}) in Fig. 5.3 is examined. It is given as

$$A_{WCF} = g_{m3}g_{mf}R_2R_P \quad (5.1)$$

while R_{2f} can be obtained as

$$R_{2f} = \frac{R_2}{A_{WCF} + 1} = \frac{R_2}{\beta} = \frac{1}{g_{m3}g_{mf}R_P + 1/R_2} \quad (5.2)$$

Comparing to the output impedance R_2 (without loaded feedback current source) in

(5.2), R_{2f} is reduced by $\beta (= A_{WCF} + 1)$ times. In addition, R_{2f} can be reduced via either increasing A_{WCF} or decreasing R_2 . Using this relationship in the WCF LDO regulator, at low I_L , R_{2f} is large since β is small and R_2 is large. At moderate I_L , R_{2f} is significantly reduced with respect to R_2 due to a large β . At high I_L , since R_2 is already small owing to a large current flowing in the 2nd gain stage, R_{2f} is small even with a small β .

As for the transfer function of the whole WCF LDO regulator, it is derived using the following assumptions: (i) $C_1, C_2 \ll C_m \ll C_c \ll C_L$; (ii) $g_{m1}R_1, g_{m2}R_2 \gg 1$, (iii) the input resistance at the cascode compensation node, is approximately equal to $1/g_{mc}$ and (iv) R_P is inversely proportional to I_L . Finally, the open-loop transfer function is obtained as follows:

$$A_{op}(s) = \frac{v_{fbout}}{v_{fbin}} = - \frac{A_{DC} (1 + s C_c / g_{mc})}{1 + as + bs^2 + cs^3 + ds^4 + es^5} \quad (5.3)$$

where

$$a = C_L R_O + C_c g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta \quad (5.4)$$

$$b = C_m C_L R_1 R_O + C_c C_m g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / (\beta g_{mc}) \quad (5.5)$$

$$c = C_m C_L R_1 R_O (C_c / g_{mc} + C_P R_P / \beta) \quad (5.6)$$

$$d = C_c C_m C_P C_L R_1 R_P R_O / (\beta g_{mc}) \quad (5.7)$$

$$e = C_c C_m C_2 C_P C_L R_1 R_2 R_P R_O / (\beta g_{mc}) \quad (5.8)$$

The DC loop gain of the LDO regulator is given by

$$A_{DC} = g_{m1} g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta \quad (5.9)$$

which indicates that the loop gain is reduced by a factor of β . This correlates well with the impedance reduction at the node N_2 , namely, $R_{2f} = R_2/\beta$. Besides, the cascode compensation generates a zero which is expressed as

$$z = -g_{mc}/C_c \quad (5.10)$$

Using (5.3) – (5.10), the stability of LDO regulator can be analyzed.

5.4. Stability Analysis and WCF Design Strategy

This section presents the stability and WCF design strategy of the WCF LDO regulator. The design strategy of the WCF technique is on the basis of the stability of the LDO regulator at different C_L and I_L conditions. Firstly, using the Routh–Hurwitz stability criterion, the required β (denoted as β_{RH}) can be obtained. Secondly, under a PM of 45° constraint, the required β (denoted as β_{PM}) is also investigated. The respective analysis is explained in the following.

As indicated in (5.4) to (5.8), all the parameters in the transfer function are a function of C_LR_O . Moreover, C_L varies from 470 pF to 10 nF and R_O is inversely proportional to I_L . For this reason, the design strategy for β and the stability of the regulator are analyzed in three cases: (I) C_LR_O is large (low I_L). The first term in (5.4) and (5.5) are dominant. (II) C_LR_O is moderate (low I_L). The first term is comparable with second term in (5.4) and the first term in (5.5) is dominant. (III) C_LR_O is small (moderate I_L and high I_L). The second term in (5.4) and (5.5) are dominant. Besides, the term C_pR_p/β in (5.6) is small due to a small R_p . Finally, the respective simplified expression for variables from a to e is summarized in Table 5.1.

TABLE 5.1 APPROXIMATED VARIABLES FROM a TO e FOR LARGE, MODERATE AND SMALL $C_L R_O$ CASES

Parameter		Large $C_L R_O$	Moderate $C_L R_O$	Small $C_L R_O$
Var.	Eqn.			
a	(5.4)	$C_L R_O$	$2C_L R_O$	$C_c g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta$
b	(5.5)	$C_m C_L R_1 R_O$		$C_c C_m g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / (\beta g_{mc})$
c	(5.6)	$C_m C_L R_1 R_O (C_c / g_{mc} + C_P R_P / \beta)$		$C_c C_m C_L R_1 R_O / g_{mc}$
d	(5.7)	$C_c C_m C_P C_L R_1 R_P R_O / (\beta g_{mc})$		
e	(5.8)	$C_c C_m C_2 C_P C_L R_1 R_2 R_P R_O / (\beta g_{mc})$		

5.4.1. Design Strategy of β using Routh–Hurwitz Stability Criterion

Routh–Hurwitz stability criterion has been widely used in the multi-stage amplifier designs [97-99]. It is simply evaluated by constructing the Routh Table 5.2 using the closed-loop transfer function. To achieve stability for the feedback system, the coefficients for a_0 – a_5 and b_1 , c_1 , d_1 in the second column of Table 5.2 must be positive. Since a_0 – a_5 is always larger than zero, the design condition for β_{RH} can be obtained by setting b_1 , c_1 and d_1 larger than zero respectively.

TABLE 5.2 ROUTH TABLE FOR A 5TH ORDER POLYNOMIAL

s^5	a_5	a_3	a_1
s^4	a_4	a_2	a_0
s^3	$b_1 = (a_3 a_4 - a_2 a_5) / a_4$	$b_2 = (a_1 a_4 - a_0 a_5) / a_4$	0
s^2	$c_1 = (a_2 b_1 - a_4 b_2) / b_1$	$c_2 = a_0$	0
s^1	$d_1 = (b_2 c_1 - a_0 b_1) / c_1$	0	0
s^0	$e_1 = a_0$	0	0

Refer to the WCF LDO regulator, the closed-loop transfer function can be expressed as

$$A_{cl}(s) = \frac{A_{op}(s)}{1 - A_{op}(s)} \approx \frac{-A_{DC}(1 + sC_c/g_{mc})}{A_{DC} + (A_{DC}C_c/g_{mc} + a)s + bs^2 + cs^3 + ds^4 + es^5} \quad (5.11)$$

where $A_{op}(s)$ is the open-loop transfer function defined in (5.3). By substituting the approximated expression for variables a to e from Table 5.1 as well as (5.9)–(5.10) into (5.11), the Routh table parameter expansion for Large, Moderate and Small $C_L R_O$ cases is listed in Table 5.3. Based on these parameters, β_{RH} for each case is analyzed as follows:

Case I): Large $C_L R_O$ (Low I_L) condition, the Routh Table parameters are shown in Case I of Table 5.3. To meet the stability criterion, the following conditions must be satisfied. They are obtained as

$$C_m C_L R_1 R_O (C_c/g_{mc} + C_P R_P/\beta_{RH}) > 0 \quad (5.12)$$

$$C_m C_L R_1 R_O > 0 \quad (5.13)$$

$$\beta_{RH} > C_c g_{m1} g_{m2} g_{m3} g_{mp} R_1 R_2 R_P / (C_L g_{mc}) \quad (5.14)$$

For (5.12) and (5.13), it is obviously valid for any β_{RH} . As for (5.14), the right hand side term is inversely proportional to C_L . Since C_L ranges from 470 pF to 10 nF, β_{RH} is small in this case.

Case II): Moderate $C_L R_O$ (Low I_L) condition, when $C_L R_O$ is equal to the cascode compensation term, namely,

$$C_c g_{m2} g_{m3} g_{mp} R_1 R_2 R_P R_O / \beta = C_L R_O \quad (5.15)$$

TABLE 5.3 ROUTH TABLE PARAMETER EXPANSION FOR THE WCF LDO REGULATOR CLOSED-LOOP TRANSFER FUNCTION IN (5.11)

Par.	Case I (Large $C_L R_O$)	Case II (Moderate $C_L R_O$)	Case III (Small $C_L R_O$)
a_0	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / \beta$		$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / \beta$
a_1	$C_L R_O$	$(2 + g_{m1}/g_{mc})C_L R_O$	$(1 + g_{m1}/g_{mc})C_c g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / \beta$
a_2	$C_m C_L R_1 R_O$		$C_c C_m g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / (\beta g_{mc})$
a_3	$C_m C_L R_1 R_O (C_c/g_{mc} + C_P R_P / \beta)$		$C_c C_m C_L R_1 R_O / g_{mc}$
a_4	$C_c C_m C_P C_L R_1 R_P R_O / (\beta g_{mc})$		$C_c C_m C_P C_L R_1 R_P R_O / (\beta g_{mc})$
a_5	$C_c C_m C_2 C_P C_L R_1 R_2 R_P R_O / (\beta g_{mc})$		$C_c C_m C_2 C_P C_L R_1 R_2 R_P R_O / (\beta g_{mc})$
b_1	$C_m C_L R_1 R_O (C_c/g_{mc} + C_P R_P / \beta)$		$(C_L - C_2 g_{m2}g_{m3}g_{mp}R_2^2 R_P / \beta) C_c C_m R_1 R_O / g_{mc}$
b_2	$C_L R_O$	$(2 + g_{m1}/g_{mc})C_L R_O$	$(1 + g_{m1}/g_{mc})C_c g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / \beta$
c_1	$C_m C_L R_1 R_O$		$[\chi C_m / g_{mc} - (1 + g_{m1}/g_{mc})C_P C_L R_P / \beta] C_c g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O / (\beta \chi)^*$
c_2	a_0		a_0
d_1	$C_L R_O - \frac{C_c g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O}{\beta g_{mc}}$	$C_L R_O \left[2 - \frac{C_P R_P g_{m1}}{\beta C_c} \right]$	$\frac{\left\{ \left(1 + \frac{g_{m1}}{g_{mc}} \right) \left[\chi \frac{C_m}{g_{mc}} - \left(1 + \frac{g_{m1}}{g_{mc}} \right) \frac{C_P C_L R_P}{\beta} \right] C_c g_{m2}g_{m3}g_{mp}R_1R_2R_P R_O \right\}}{\chi C_m / g_{mc} - (1 + g_{m1}/g_{mc})C_P C_L R_P / \beta} \bigg/ \beta - \frac{\chi^2 C_m g_{m1} R_1 R_O}{g_{mc}}^*$

* $\chi = C_L - C_2 g_{m2}g_{m3}g_{mp}R_2^2 R_P / \beta$

the Routh Table parameters are shown in Case II of Table 5.3. As indicated, b_1 and c_1 for Case I and Case II are the same. The design conditions for $b_1 > 0$ and $c_1 > 0$ can still be expressed by (5.12) and (5.13), respectively. Since (5.12) and (5.13) are always valid for any β_{RH} , the condition for β_{RH} to meet the criterion is obtained as

$$\beta_{RH} > C_P g_{m1} R_P / (2C_c) \quad (5.16)$$

From (5.16), the right hand side term is proportional to $g_{m1} R_P$. Since the maximum value for R_P is R_X as explained in Section 5.2, β_{RH} can be made small by proper sizing of R_P and g_{m1} .

Case III): Small $C_L R_O$ (Moderate and High I_L) condition, the Routh Table parameters are shown in Case III of Table 5.3. To meet the criterion, the following three design requirements for β_{RH} must be fulfilled. They are expressed as

$$\beta_{RH} > C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P / C_L \quad (5.17)$$

$$\beta_{RH} > (1 + g_{m1} / g_{mc}) C_P g_{mc} R_P / C_m \quad (5.18)$$

$$\beta_{RH} > \frac{C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P}{C_L} + \left(1 + \frac{g_{m1}}{g_{mc}} \right) \frac{C_P g_{mc} R_P}{C_m} \quad (5.19)$$

If the condition in (5.19) is met, (5.17) and (5.18) will be valid as well, but not vice versa. This suggests that (5.19) determines the only choice out of three β_{RH} inequalities. As such, at moderate I_L , R_2 and R_P are fairly large. β_{RH} is the largest. On the other hand, at high I_L , R_P is small owing to the large biasing current flowing in the diode transistor M_{d1} of 3rd gain stage. R_2 is also small due to the dynamic bias introduced by the WCF block. Thus β_{RH} at high I_L condition is reduced with respect to that of moderate I_L case. Based on the above analysis, Table 5.4 summarizes the β_{RH} at different I_L

conditions. From this table, it confirms that the WCF should be made strong at moderate I_L condition whilst weak at both low and high I_L conditions.

TABLE 5.4 SUMMARY OF THE REQUIRED β_{RH} AT DIFFERENT I_L CONDITIONS TO MEET ROUTH–HURWITZ CRITERION

Parameter	Low I_L	Moderate I_L	High I_L
R_P, R_2	Large	Moderate	Small
g_{m2}, g_{m3}, g_{mp}	Small	Moderate	Large
β_{RH} design eqn.	(5.14) and (5.16)	(5.19)	(5.19)
β_{RH} value	Small	Large	Small

Consider the WCF technique employed in the LDO regulator as discussed in Section 5.2, the feedback factor β (β_{sim}) and R_{2f} are simulated with respect to I_L . As can be observed in Fig. 5.6, the WCF technique can significantly reduce R_2 , especially for moderate and high I_L . Moreover, when I_L increases, β_{sim} increases to around 25 dB at $I_L = 200 \mu A$ first. Then it drops below 5 dB when I_L is larger than 10 mA.

Fig. 5.6: Simulated β (β_{sim}) and R_{2f} at different I_L conditions.

To verify that the WCF design can fulfill the stability criterion using numerical examples, the theoretical β_{RH} at different I_L conditions are calculated using the right hand side term of inequalities (5.14), (5.16) and (5.19). The design parameters and stability verification using theoretical β_{RH} and simulated β_{sim} at $I_L = 0$ mA, 1 mA and 50 mA are shown in Table 5.5. It can be seen that the WCF can meet the β_{RH} requirement for all three I_L conditions for both $C_L = 470$ pF and 10 nF.

Table 5.5 DESIGN PARAMETERS, STABILITY VERIFICATION USING THEORETICAL β_{RH} AND SIMULATED β_{sim}

Parameter	$I_L = 0 \text{ mA}$		$I_L = 1 \text{ mA}$		$I_L = 50 \text{ mA}$	
$g_{m1} \text{ (}\mu\text{S)}$	51		51		51	
$g_{m2} \text{ (}\mu\text{S)}$	24		357		755	
$g_{m3} \text{ (}\mu\text{S)}$	71		452		5290	
$g_{mp} \text{ (}\mu\text{S)}$	31		2.03e4		3.1e5	
$g_{mc} \text{ (}\mu\text{S)}$	131		131		131	
$R_1 \text{ (k}\Omega\text{)}$	617		617		617	
$R_2 \text{ (k}\Omega\text{)}$	342		22.2		6.46	
$R_P \text{ (k}\Omega\text{)}$	22.4		4.56		0.207	
$C_c \text{ (pF)}$	3.5		3.5		3.5	
$C_m \text{ (pF)}$	0.3		0.3		0.3	
$C_2 \text{ (fF)}$	26		31		30	
$C_p \text{ (pF)}$	2.58		3.22		3.09	
Theoretical β_{RH} and Simulated β_{sim}						
C_L	470 pF	10 nF	470 pF	10 nF	470 pF	10 nF
β_{RH} design eqn.	(5.16)	(5.14)	(5.19)	(5.19)	(5.19)	(5.19)
$\beta_{RH} \text{ (dB)}$	-7.5	-29.4	19.5	19.1	0.6	-7.5
$\beta_{sim} \text{ (dB)}$	6		22		3.3	
$\beta_{sim} > \beta_{RH}$ for stability	Yes		Yes		Yes	

From the above analysis together with the numerical examples, the WCF technique can provide an appropriate feedback to meet the Routh–Hurwitz stability criterion for low, moderate and high I_L conditions using the design equations (5.14), (5.16) and (5.19). As a result, these equations provide the design guidelines for the amount of feedback in the WCF at different I_L conditions.

5.4.2. Pole and Zero Locations

The feedback factor β , R_{2f} , poles, zero and related parameters for Large, Moderate and Small $C_L R_O$ cases are presented in Table 5.6. Owing to the cascode compensation, a LHP zero, expressed in (5.10), is generated. It locates outside the unity gain frequency ω_{UGF} . Hence, it will not jeopardize the settling time of LDO regulator. The pole location analysis for each case is discussed as follows:

Case I – Large $C_L R_O$ (Low I_L): At this condition, $C_L R_O$ forms the low frequency dominant pole ($p_{-3dB} = 1/(C_L R_O)$). Since p_{-3dB} locates at a very low frequency, the ω_{UGF} is small. At this juncture, all the parasitic poles locate at relative high frequencies. The LDO regulator can maintain a stable operation. This is the reason why a weak negative current feedback can be designed. It also correlates well with the Routh–Hurwitz stability criterion analysis in Section 5.4.1 that at large $C_L R_O$ condition, β_{RH} is small using (5.14). In view of the weak feedback, the regulator's gain and speed do not significantly change with respect to the regulator without WCF technique.

Case II – Moderate $C_L R_O$ (Low I_L): In this case, p_{-3dB} is constituted by both the $C_L R_O$ and the cascode compensation. The ω_{UGF} is increased with respect to that in Case I. However, ω_{UGF} remains small and only half of its maximum value. Besides, $|p_{2,3}|_f$ is also increased slightly when compared to that in Case I. The regulator can achieve a stable operation with a small feedback as suggested in (5.16).

Case III – Small $C_L R_O$ (Moderate and High I_L): In this case, p_{-3dB} is mainly constituted by the cascode compensation. Moreover, though the loop gain of regulator is reduced by a factor of β according to (5.9), the dominant pole p_{-3dB} frequency is increased by the same factor, which yields a constant ω_{UGF} .

TABLE 5. 6 FEEDBACK FACTOR β , POLES, ZERO, Q-FACTOR, ω_{UGF} FOR LARGE, MODERATE AND SMALL $C_L R_O$ CASES

Parameter	Case I: Large $C_L R_O$	Case II: Moderate $C_L R_O$	Case III: Small $C_L R_O$	
	Low I_L		Moderate I_L	High I_L
Feedback	Weak		Strong	Weak
β	$g_{m3}g_{mf}R_2R_p + 1$			
A_{DC}	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_pR_o / \beta$			
z_1	$-g_{mc}/C_c$			
p_{-3dB}	$-1/(C_L R_O)$	$-1/(2C_L R_O)$	$-\beta/(C_c g_{m2}g_{m3}g_{mp}R_1R_2R_pR_o)$	
$ p_{2,3} _f$	$\sqrt{\beta g_{mc}/[(\beta C_c + C_P g_{mc} R_P)C_m R_1]}$	$\sqrt{2\beta g_{mc}/[(\beta C_c + C_P g_{mc} R_P)C_m R_1]}$	$\sqrt{g_{m2}g_{m3}g_{mp}g_{mc}R_2R_p/(\beta C_m C_L)}$	
$ p_{4,5} _f$	$\sqrt{(\beta C_c + C_P g_{mc} R_P)/(C_c C_2 C_P R_2 R_P)}$		$\sqrt{\beta/(C_2 C_P R_2 R_P)}$	
$Q_{ p_{2,3} _f}$	$\sqrt{(\beta C_c + C_P g_{mc} R_P)/(\beta C_m g_{mc} R_1)}$	$\sqrt{2(\beta C_c + C_P g_{mc} R_P)/(\beta C_m g_{mc} R_1)}$	$\sqrt{\beta C_L g_{mc}/(C_m g_{m2}g_{m3}g_{mp}R_2R_p)}$	
$Q_{ p_{4,5} _f}$	$\sqrt{[(\beta C_c + C_P g_{mc} R_P)C_2 R_2]/(C_c C_P R_P)}$		$\sqrt{\beta C_2 R_2/(C_P R_P)}$	
ω_{UGF}	$g_{m1}g_{m2}g_{m3}g_{mp}R_1R_2R_p/(\beta C_L)$	$g_{m1}/(2C_c)$	g_{m1}/C_c	

For $|p_{2,3}|_f$, they are reduced by a factor of $\sqrt{\beta}$. However, $|p_{2,3}|_f$ can still be designed to be higher than that of ω_{UGF} through choosing a proper value of g_{mc} and C_c . This can be derived as

$$\sqrt{\frac{g_{m2}g_{m3}g_{mp}g_{mc}R_2R_P}{\beta C_m C_L}} \geq \frac{g_{m1}}{C_c} \quad (5.20)$$

which can be rewritten in a form of

$$C_c \sqrt{g_{mc}} \geq g_{m1} \sqrt{\frac{\beta C_m C_L}{g_{m2}g_{m3}g_{mp}R_2R_P}} \quad (5.21)$$

From (5.21), both C_c and g_{mc} can be increased to ensure that $|p_{2,3}|_f$ locates at a higher frequency than ω_{UGF} . By substituting the design parameters from Table 5.5 with $I_L = 1$ mA to (5.21) as a numerical example, the calculated minimum C_c is 1.5 pF. Since the designed C_c is 3.5 pF in the WCF LDO regulator, it is more than the required theoretical minimum value.

Of another important design consideration, besides the WCF LDO regulator can fulfill the Routh–Hurwitz stability criterion as discussed in Case III of Section 5.4.1, the open-loop transfer function (5.3) generates a high frequency LHP complex pole pair $|p_{4,5}|_f$. Its frequency is multiplied by a factor of $\sqrt{\beta}$ with respect to that without the feedback. In this way, at moderate I_L , due to a large β , the complex pole pair $|p_{4,5}|_f$ is located far away from the ω_{UGF} . At high I_L , though β is reduced with reference to that at moderate I_L , due to very small R_P and R_2 , the complex pole pair $|p_{4,5}|_f$ still locates at a much higher frequency than ω_{UGF} . This confirms the stability of LDO regulator at both moderate and high I_L conditions.

Figure 5.7 depicts the simulated open-loop gain and phase of the WCF LDO regulator for $C_L = 470$ pF and $C_L = 10$ nF under different I_L conditions. It can be seen

that the LDO regulator can provide a stable operation for both C_L corners. In addition, the loop gain of the LDO regulator maintains to be more than or equal to 50 dB for different I_L due to the weighted current feedback mechanism. Thus good regulation accuracy can be achieved.

Fig. 5.7: Simulated open-loop gain and phase at different I_L for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF with $V_{DD} = 0.75$ V.

Figure 5.8 shows the phase margin (PM) and gain margin (GM) for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L . The regulator achieves a minimum PM of 45° and a minimum GM of 11 dB. This has illustrated that the WCF LDO regulator is stable under different C_L and I_L combinations.

Fig. 5.8: Simulated phase margin (PM) and gain margin (GM) for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF when sweeping I_L at $V_{DD} = 0.75$ V.

5.4.3. Phase Margin (PM) under C_L and I_L Variations

Refer to the PM plot in Fig. 5.8, for $C_L = 3.3$ nF and 10 nF, when the I_L increases from 1 μ A to 50 mA, the PM of LDO regulator initially decreases to around 45° and then it increases until to 100° . This fact stems from different dominant factors between $C_L R_O$ and cascode compensation term in the formation of p_{-3dB} . The analysis can also be partitioned into three regions: (i) Under large $C_L R_O$ condition (low I_L), due to a small ω_{UGF} , $|p_{2,3}|_f$ is located at a much higher frequency than ω_{UGF} , resulting in a large PM. (ii) when I_L increases, R_O reduces. The continual reduction of $C_L R_O$ increases the ω_{UGF} . Since the load current I_L is still low, the $|p_{2,3}|_f$ is almost constant based on Table

5.6. As such, the PM of regulator will keep reducing as the ω_{UGF} becomes closer to the $|p_{2,3}|_f$. When $C_L R_O$ becomes moderate and comparable with cascode compensation term, the PM is approaching to the vicinity of the minimum point. (iii) When I_L further increases, $C_L R_O$ becomes small. On the contrary, the cascode compensation becomes the dominant term, leading to the fixed ω_{UGF} ($=g_{m1}/C_c$). Besides, $|p_{2,3}|_f$ will increase since g_{mp} becomes larger. This will cause the PM to rise when I_L increases.

Based on the analysis in Section 5.4.1, if the feedback factor β can meet the design conditions stated in (5.14), (5.16) and (5.19) according to the Routh–Hurwitz stability criterion, $|p_{4,5}|_f$ will be pushed to a much higher frequency than ω_{UGF} . This indicates that $|p_{4,5}|_f$ will not influence the PM of regulator. With this assumption, the PM of feedback system can be approximated as

$$PM \approx 90^\circ - \tan^{-1} \left\{ \frac{\omega_{UGF}}{Q_{|p_{2,3}|_f} |p_{2,3}|_f \left[1 - \left(\omega_{UGF} / |p_{2,3}|_f \right)^2 \right]} \right\} + \tan^{-1} \left(\frac{\omega_{UGF}}{z_1} \right) \quad (5.22)$$

based on [25]. Through substituting the respective expression of ω_{UGF} , $|p_{2,3}|_f$ and $Q_{|p_{2,3}|_f}$ for Large, Moderate and Small $C_L R_O$ case in Table 5.6 into (5.22), the design requirement of β_{PM} for a minimum PM of 45° is analyzed as follows:

Case (I) – Large $C_L R_O$ (Low I_L): To achieve a $PM \geq 45^\circ$, the necessary condition for β_{PM} to be satisfied is

$$\beta_{PM} \geq \frac{C_m g_{m1} g_{m2} g_{m3} g_{mp} R_1^2 R_2 R_P}{C_L} \quad (5.23)$$

From (5.23), the minimum β_{PM} (β_{PM_min}) is inversely proportional to C_L . A large C_L gives a smaller ω_{UGF} which subsequently reduces the feedback requirement for a $PM \geq 45^\circ$.

Case (II) – Moderate $C_L R_O$ (Low I_L): In the situation when the cascode compensation effect equals to that of $C_L R_O$ as defined in (5.15), for a larger C_L , a larger g_{mp} (implying a large I_L) in the left hand side is needed to balance the right hand side term. This implies that the minimum PM region will shift slightly to the right when C_L increases in context of whole current range (0–50mA). This is consistent with the observation of PM plot in Fig. 5.8. For a $PM \geq 45^\circ$, it suggests that β_{PM} should fulfill the condition of

$$\beta_{PM} \geq \frac{C_m C_P g_{m1}^2 R_1 R_P}{8C_c^2 - (2 + g_{m1}/g_{mc}) C_m C_c g_{m1} R_1} \quad (5.24)$$

It is noted that I_L is still small even the balance point for (5.15) shifts to a higher I_L when C_L increases. Moreover, since R_P is inversely proportional to $\sqrt{I_L S_{d1}/S_p}$, where S_p and S_{d1} is the respective aspect ratio of the power transistor M_P and the driving transistor M_{d1} in Fig. 5.3, R_P is approximated independent of C_L . As a result, β_{PM_min} is almost constant for the whole C_L range from (5.24).

Case (III) – Small $C_L R_O$ (Moderate and High I_L): As indicated in small $C_L R_O$ case of Table 5.6, $|p_{2,3}|_f$ is inversely proportional to $\sqrt{\beta}$. β should not be made too large to achieve a minimum 45° PM. The condition for the β_{PM} becomes

$$\beta_{PM} \leq \frac{C_c^2 g_{mc} g_{m2} g_{m3} g_{mp} R_2 R_P}{C_m C_L g_{m1}^2} \quad (5.25)$$

From (5.25), the maximum allowable β_{PM} (β_{PM_max}) is proportional to g_{mp} . At small $C_L R_O$ case, due to large I_L , g_{mp} becomes large, contributing a large β_{PM_max} . On the other hand, due to the WCF technique to reduce the feedback at large I_L , the design β is not easily exceeding the β_{PM_max} defined in (5.25).

To verify the WCF regulator can fulfill the design requirement for a minimum 45° PM using numerical examples, β_{PM_min} or β_{PM_max} at different $C_L R_O$ conditions are calculated using (5.23)–(5.25). Using the design parameters in Table 5.5, the theoretical β_{PM} and simulated β_{sim} for Large, Moderate and Small $C_L R_O$ are shown in Table 5.7. It is noted that (i) for Large $C_L R_O$ case, β_{PM} at $C_L = 3.3$ nF and $I_L = 0$ mA is chosen. This is because, for $C_L = 470$ pF and 1 nF, the $C_L R_O$ is already comparable with the cascode compensation term at 0 mA. For 10 nF, β_{PM_min} is smaller than that of 3.3 nF. (ii) For Moderate $C_L R_O$ case, the worst β_{PM} at $C_L = 470$ pF, $I_L = 0$ mA is chosen. (iii) For Small $C_L R_O$ cases, the β_{PM} at $C_L = 10$ nF, $I_L = 50$ mA is chosen. The results in Table 5.7 indicate that the WCF can meet the β requirement for all three $C_L R_O$ conditions. A minimum PM of 45° can be achieved as depicted in Fig. 5.8.

TABLE 5.7 NUMERICAL EXAMPLE FOR PM VERIFICATION USING THEORETICAL β_{PM} AND SIMULATED β_{sim}

Parameter	Large $C_L R_O$	Moderate $C_L R_O$	Small $C_L R_O$
C_L	3.3 nF	470 pF	10 nF
I_L	0 mA	0 mA	50 mA
β_{PM} Design Eqn.	(23)	(24)	(25)
β_{PM} (dB)	-2.9	3.3	50.6
β_{sim} (dB)	6	6	3.3
Criterion For 45° PM	$\beta_{sim} \geq \beta_{PM}$	$\beta_{sim} \geq \beta_{PM}$	$\beta_{sim} \leq \beta_{PM}$
Meet Criterion	Yes	Yes	Yes
Simulated PM	63°	52°	97°

In brief, for regulator's stability, both the Routh–Hurwitz stability criterion and 45° minimum PM should be fulfilled. By combining the design equations of β_{RH} in Section 5.4.1 [(5.14), (5.16) and (5.19)] and β_{PM} in Section 5.4.3 [(5.23)–(5.25)], the required β is summarized in Table 5.8. For large $C_L R_O$ case (Case I), since $C_m R_1 \gg C_c/g_{mc}$, if the condition in (5.23) is met, (5.14) is valid as well. This suggests that

(5.23) is the only choice for design inequalities. For Moderate $C_L R_O$ case (Case II), the design equations are decided by (5.16) and (5.24) together. For small $C_L R_O$ case (Case III), (5.19) and (5.25) gives the lower and upper bound for β_{req} respectively. Using this table, the design guidelines for β is investigated in details.

TABLE 5.8 COMBINED β DESIGN INEQUALITIES USING β_{RH} AND β_{PM}

Case	β
I	$\beta \geq C_m g_{m1} g_{m2} g_{m3} g_{mp} R_1^2 R_2 R_P / C_L$
II	$\left[\beta > C_P g_{m1} R_P / (2C_c) \right] \& \left[\beta \geq \frac{C_m C_P g_{m1}^2 R_1 R_P}{8C_c^2 - (2 + g_{m1}/g_{mc}) C_m C_c g_{m1} R_1} \right]$
III	$\frac{C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P}{C_L} + \left(1 + \frac{g_{m1}}{g_{mc}} \right) \frac{C_P g_{mc} R_P}{C_m} < \beta \leq \frac{C_c^2 g_{mc} g_{m2} g_{m3} g_{mp} R_2 R_P}{C_m C_L g_{m1}^2}$

Case I: Large $C_L R_O$ using (5.23). Case II: Moderate $C_L R_O$ using (5.16) and (5.24). Case III: Small $C_L R_O$ using (5.19) and (5.25).

5.4.4. Combined Frequency Compensation and Q-Factor

The WCF LDO regulator employs a combined cascode and Miller compensation. The dominant pole is determined by the cascode compensation since it can push the non-dominant pole to a higher frequency under a large capacitive load in comparison to the Miller compensation counterpart [100]. Unfortunately, the cascode compensation easily gives gain peaking due to a large parasitic Q factor [101]. To overcome the drawback, a small Miller compensation capacitor is added in this LDO regulator so as to reduce the Q factor. This is mainly because the Q factor value is inversely proportional to the capacitance at the Miller node [101]. This can also be validated from the Q factor expressions shown in Table 5.6. At moderate and high I_L conditions (cascode compensation dominating), $Q_{|p_{2,3}|_f}$ is inversely proportional to $\sqrt{C_m}$.

A large C_m contributes to a small Q factor which can reduce the peaking effect arising from the complex pole pair $|p_{2,3}|_f$. However, a large C_m will reduce the frequency of $|p_{2,3}|_f$ as well. This will jeopardize the cascode effect. For this reason, C_m is designed to be small (0.3 pF) in the WCF topology to achieve a reasonable Q factor whilst keeping the complex pole pair $|p_{2,3}|_f$ locating outside the ω_{UGF} .

5.4.5. Minimum C_L for a Stable Operation

As discussed in Section 5.4.3, when C_L is 470 pF, the dominant pole is in moderate C_LR_O region at $I_L = 0$ mA. If the minimum C_L (470 pF) is further reduced to a smaller value, the dominant pole will directly move into small C_LR_O region. To meet the Routh–Hurwitz stability criterion, β_{RH} must fulfill (5.19) across the whole I_L range. However, at small I_L , R_p becomes large and it causes a large β_{RH} . This suggests that a very strong feedback is needed at low I_L to ensure stable operation. The gain as well as the speed of regulator will be limited. Based on the tradeoff design considerations, the output C_L of regulator is preferably to start from the mid-range capacitive load (470 pF) onwards.

5.5. Circuit Implementation and Power Supply Rejection

Analysis

5.5.1. Schematic Implementation

The complete schematic implementation of the WCF LDO regulator is shown in Fig. 5.9. The red arrows indicate the power supply noise injection paths. It utilizes a folded cascode error amplifier constituted by ($M_0 - M_8$) as the first gain stage. The 2nd, 3rd inverting gain stages and the WCF block employ the same structure as that in Fig. 5.3. The overshoot reduction block (C_B , R_B , M_{13}) senses the voltage swing at the node N_P and generates a momentary sinking current to reduce the overshoot magnitude as well as settling time of the LDO regulator.

To compare the regulation accuracy and the speed of LDO regulator with the two proposed NCF and WCF technique, a NCF LDO regulator is also built and simulated. In the NCF LDO regulator, M_{a3} in the WCF block (Fig. 5.9) is removed. In such an arrangement, both M_{a1} and M_{a2} are working in saturation region. This turns out that the negative current feedback is kept strong for both moderate and high I_L conditions. Figure 5.10 shows the exemplary transient responses of the LDO regulator with NCF and WCF technique. Under the same load current switching condition, it can be observed that the WCF LDO regulator displays a 1.5 times smaller undershoot and overshoot, and an approximate 2 times better load regulation with respect to the NCF LDO regulator. This has demonstrated that the WCF technique addresses the limitations of the NCF and achieves a better optimization of stability, accuracy and speed.

Fig. 5.9: Schematic of the WCF LDO regulator.

Fig. 5.10: Exemplary transient response of the LDO regulator with proposed NCF and WCF technique.

5.5.2. Power Supply Rejection Analysis

As shown in Fig. 5.9, Assumed that the supply noise is ΔV_{DD} , the analysis for each path is discussed as follows:

For path 1 and path 2, as discussed in [95], the supply ripple is reflected at node N_1 . It can be expressed as

$$\begin{aligned}
 \Delta V_{N1} &= \frac{\Delta V_{DD}}{R_{ds7}} (R_{ds8} // g_{m6} R_{ds6} R_{ds4}) + \frac{\Delta V_{DD}}{R_{ds8} + (1 + g_{m6} R_{ds6} R_{ds4})} \\
 &\approx \frac{\Delta V_{DD}}{R_{ds7}} R_{ds8} \\
 &= \Delta V_{DD}
 \end{aligned} \tag{5.26}$$

For path 3, since the gate voltage variation of M_9 equals to its source voltage variation, the supply noise coming from paths 1-3 cancel each other. Thus, ΔV_{N2} due to path 1-3 equals to zero. Another noise path contributes to node N_2 is coming from the WCF circuit (path 6 and 7). As discussed in Section 5.2 and 5.3, at small I_L , g_{mf} is small. The noise contribution for WCF is small as well. At moderate I_L , g_{mf} increases,

the noise contribution at node N_2 can be expressed as $\Delta V_{N2_wcf} = -g_{mf} \Delta V_{DD} R_{2f}$. Since the feedback reduces the impedance R_{2f} , ΔV_{N2_wcf} is small as well. Finally, at high I_L , both g_{mf} and R_{2f} are small. ΔV_{N2_wcf} is also small. Therefore, the supply noise at node N_2 can be approximated as zero due to path 1-3 and path 6-7.

Refer to path 4 and path 5, since $R_X + 1/g_{m12} \ll R_{ds11}$, the noise at node N_P can be expressed as

$$\begin{aligned} \Delta V_{NP} &= \frac{R_{ds11}}{R_{ds11} + R_X + 1/g_{m12}} \Delta V_{DD} \\ &\approx \Delta V_{DD} \end{aligned} \quad (5.27)$$

Finally, for path 8, there are two ways for the supply noise coming into the output. The first way is to vary the V_{SG} of the power transistor M_P . As shown in (5.27), the gate voltage variation of M_P equals to the source voltage variation. The supply noise contribution due to ΔV_{SG} of M_P can be approximated as zero. The second way is due to the limited R_{dsp} for M_P . The limited R_{dsp} forms a resistor-divider with the regulated output impedance and injects parts of the supply noise into V_{OUT} . As a result, based on the analysis method in [95], the PSR of the WCF LDO regulator can be expressed as

$$\begin{aligned} PSR &= \frac{\Delta V_{OUT}}{\Delta V_{DD}} \\ &= \frac{(z_{out} \parallel z_{out_reg})}{(z_{out} \parallel z_{out_reg}) + R_{dsp}} \end{aligned} \quad (5.28)$$

where

$$\begin{aligned} z_{out} &= R_L \parallel (1/sC_L) \\ z_{reg} &= \frac{z_{out} \parallel R_{dsp}}{A(s)} \\ A(s) &= \frac{A_{DC}}{1 + s/p_{-3dB}} \end{aligned} \quad (5.29)$$

It is noted that the loop gain transfer function in (5.3) is simplified as a one-pole system within the unity gain frequency (UGF).

At low frequency, $A(s) \gg 1$, and $R_L \gg 1/sC_L$, from (5.28) and (5.29), the PSR of the regulator can be expressed as

$$\begin{aligned}
 PSR &\approx \frac{z_{out_reg}}{z_{out_reg} + R_{dsp}} \\
 &\approx \frac{R_L (1 + s/p_{-3dB}) / A_{DC}}{R_L (1 + s/p_{-3dB}) / A_{DC} + R_{dsp}} \\
 &\approx \frac{R_L (1 + s/p_{-3dB})}{A_{DC} R_{dsp}}
 \end{aligned} \tag{5.30}$$

As indicated in (5.30), the regulator shows a PSR inversely proportional to the DC gain of the feedback loop. It also depicts a zero at p_{-3dB} . This is because the loop gain starts to decrease after p_{-3dB} which reduces the output impedance reduction effect.

At moderate frequency when $A(s)$ is smaller or equal to 1, the feedback loop no longer reduces the impedance. In this frequency range, $R_L \gg 1/sC_L$, it yields a PSR of

$$\begin{aligned}
 PSR &\approx \frac{z_{out}}{z_{out} + R_{dsp}} \\
 &\approx \frac{R_L}{R_L + R_{dsp}}
 \end{aligned} \tag{5.31}$$

At high frequency when R_L is smaller than $1/sC_L$, z_{out} is dominated by C_L , the PSR of the LDO regulator can be derived as

$$\begin{aligned}
 PSR &\approx \frac{z_{out}}{z_{out} + R_{dsp}} \\
 &\approx \frac{1/(sC_L)}{1/(sC_L) + R_{dsp}} \\
 &= \frac{1}{1 + sC_L R_{dsp}}
 \end{aligned} \tag{5.32}$$

As indicated in (5.32), the PSR will become smaller when the frequency is further increased. This is because, when the frequency increases, the output capacitor

functions as a very small impedance reference to ground. Thus, the noise at the output becomes smaller when the frequency increases.

Figure 5.11 depicts the simulated PSR for $I_L = 0, 1 \text{ mA}, 10 \text{ mA}, 25 \text{ mA}$ and 50 mA for $C_L = 470 \text{ pF}$. It can be seen that PSR responses follows the theoretical predication trends and validates the PSR analysis. (i) At low frequency, the PSR of the LDO regulator is determined by the feedback loop gain and displays a zero around p-3dB. The low frequency PSR at 1 mA is worse than that at other I_L due to the strong loop gain reduction by the WCF. (ii) At moderate frequency, without the feedback loop to reduce the impedance, the PSR of the regulator approaches to the worst point. (iii) At high frequency, the PSR becomes smaller due to the output capacitor filtering effect. For a larger I_L , R_{dsp} becomes smaller, thus the PSR will becomes better at a higher frequency as indicated in (5.32) and Fig. 5.11.

Fig. 5.11 Simulated PSR for $C_L = 470 \text{ pF}$ under different I_L .

5.6. Experimental Results and Discussions

The WCF LDO regulator is implemented using UMC 65-nm CMOS process. The microphotograph of the WCF regulator is shown in Fig. 5.12. Excluding the supply and output PADs as connectors, the active area is 0.0133 mm^2 . To reduce the offset, common centroid layout matching technique is employed in the differential pair input transistors (M_1 and M_2) and all the current mirrors of Fig. 5.9. As for the power transistor, multi-finger layout in Section 3.5.2 (Fig. 3.10) and the metallization technique in Section 3.5.3 (Fig. 3.13) are utilized to minimize the parasitic effect.

At a 0.75 V supply voltage, the WCF LDO regulator can support a maximum I_L of 50 mA. The dropout voltage is less than 0.2 V at full I_L . The measured quiescent current at zero I_L is $15.9 \mu\text{A}$. With a total 3.8 pF (3.5 pF cascode + 0.3 pF Miller) compensation capacitance, the WCF LDO regulator offers stable operation for C_L ranging from 470 pF to 10 nF across the whole I_L range.

Fig. 5.12: Microphotograph of the WCF LDO regulator.

It is noted that external reference voltages are used and off-chip capacitors are added to model the C_L of the LDO regulator during the measurement. To test the

stability and the performance of the WCF LDO regulator for the whole C_L range, four standard load capacitors (470 pF, 1 nF, 3.3 nF and 10 nF) have been chosen. In addition, two I_L switching cases (0 to maximum I_L and 1 mA to maximum I_L) are used to measure the transient performance.

Figure 5.13 shows the measured load transient responses of the WCF LDO regulator when I_L is switching from 0 to 50 mA with an edge time of 100 ns for all four load capacitors. The supply voltage is 0.75 V and the output voltage is 0.55 V. As can be observed from the graphs, the undershoots are 113 mV, 109 mV, 98 mV, 72 mV whereas the overshoots are 29 mV, 29 mV, 27 mV, 32 mV for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF, respectively. The undershoot becomes smaller when the load capacitor increases. This is because a larger capacitor is able to absorb a larger transient current during I_L switching. In addition, due to the intelligent control of WCF and the high speed property of the 3rd gain stage, the settling time of the WCF LDO regulator is quite small. The measured settling time are 248 ns, 244 ns, 252 ns and 368 ns for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF, respectively.

(a)

(b)

(c)

(d)

Fig. 5.13: Measured load transient responses with $V_{DD} = 0.75\text{ V}$, $V_{OUT} = 0.55\text{ V}$ for (a) $C_L = 470\text{ pF}$, (b) $C_L = 1\text{ nF}$, (c) $C_L = 3.3\text{ nF}$ and (d) $C_L = 10\text{ nF}$.

Figure 5.14 shows the transient responses of the WCF LDO regulator at $V_{DD} = 0.75$ V when I_L switches from 1 mA to 50 mA (vice versa) for $C_L = 470$ pF and $C_L = 10$ nF. Using an identical edge time of 100 ns, the undershoots are substantially reduced when compared with that of I_L switching from 0 to 50 mA. The undershoots are 24 mV, 35 mV whereas the overshoots are 24 mV, 29 mV for $C_L = 470$ pF and 10 nF, respectively.

Fig. 5.14: Measured load transient responses at $V_{DD} = 0.75$ V with I_L switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.

Figure 5.15 depicts the transient responses of the WCF LDO regulator at $V_{DD} = 1.2$ V when I_L switches from 1 mA to 50 mA (vice versa) for $C_L = 470$ pF and $C_L = 10$ nF. The LDO regulator works well for a 1.2 V supply. Comparing the results with $V_{DD} =$

0.75 V in Fig. 5.14, the undershoot and overshoot increase by around 15 mV. This is because, at $V_{DD} = 1.2$ V, the large feedback transistor M_{a2} turns off at a higher I_L than that of $V_{DD} = 0.75$ V. Therefore, the regulator's speed at high I_L is slightly reduced. This leads to a small amount increment for transient undershoot and overshoot.

Fig. 5.15: Measured load transient responses at $V_{DD} = 1.2$ V with I_L switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.

The line transient response at $I_L = 1$ mA, $C_L = 470$ pF is depicted in Fig. 5.16. When V_{DD} switches from 0.75 V to 1.2 V with a 10 μ s edge time, the maximum output voltage spike is 4.3 mV and the introduced increment of error voltage is only 1.8 mV. To measure the power supply rejection of the LDO regulator, a measurement setup shown in Fig. 5.17 is used. A spectrum analyzer is utilized to generate an AC sine wave signal with different frequencies and to capture the output voltage variation. The

PSR of LDO regulator can be calculated by dividing the output and input voltages. The magnitude of the input sine wave is set to be 31 mV which will not force the LDO regulator moving into dropout region. Figure 5.18 shows the measured power supply rejection (PSR) of the WCF LDO regulator for $C_L = 470$ pF at different I_L conditions. At 1 kHz, it can be seen that the minimum PSR is around -44 dB when $I_L = 1$ mA. This is due to some loop gain reduction from the large feedback (β) as revealed in (5.9). At full I_L , the regulator achieves a PSR of -51 dB. Figure 5.19 depicts the measured output noise response of the LDO regulator at $C_L = 470$ pF and $I_L = 0$ mA. It can be seen that the noise is -98.7 dBm/Hz ($2.6 \mu\text{V}/\sqrt{\text{Hz}}$) at 100 Hz and -105 dBm/Hz ($1.25 \mu\text{V}/\sqrt{\text{Hz}}$) at 100 kHz, respectively.

Fig. 5.16: Measured line transient response at $I_L = 1$ mA and $C_L = 470$ pF.

Fig. 5.17: PSR measurement setup.

Fig. 5.18: Measured PSR at $C_L = 470 \text{ pF}$ for different I_L .

Fig. 5.19: Measured Output Noise at $C_L = 470$ pF with 0 mA I_L .

Performance comparison between the WCF LDO regulator and the other reported state-of-the-art OCL-LDO regulators is presented in Table 5.9. With the WCF circuit technique, the LDO regulator achieves good performance metrics with an additional merit to drive a wide C_L range. To compare the load transient performance, the OCL-LDO regulator figure-of-merit (FOM) expressed in (4.15) of Section 4.4.2 is adopted.

To provide a comparison, all the results in Table 5.9 for the WCF LDO regulator is based on $C_L = 470$ pF which is regarded as the closer load capacitance value with respect to the reported works. Since some of the designs [23, 24] were tested using some amount of minimum loading currents, two FOMs of the WCF LDO regulator are used for comparison. The first FOM (left column) represents the performance metric for I_L switching from 0 to 50 mA while the second FOM (right column) represents the performance metric for I_L switching from 1 mA to 50 mA.

TABLE 5.9 PERFORMANCE COMPARISON WITH THE REPORTED OCL-LDO REGULATORS

Parameter	[18]	[21]	[23]	[24]	[26]	[27]	[28]	[29]	[30]	[31]	This Work	
Year	2005	2007	2010	2010	2012	2012	2012	2012	2013	2013	2014	
Technology (μm)	0.09	0.35	0.35	0.09	0.09	0.35	0.35	0.35	0.065	0.11	0.065	
Chip Area (mm^2)	0.098	0.12	0.155	0.019	0.005 [#]	0.0987	0.064	0.4	0.017	0.21	0.0133	
V_{IN} (V)	1.2	3	0.95-1.4	0.75-1.2	1.2	1.2	2.5-4	1.2-1.5	1.2	1.8-3.8	0.75-1.2	
V_{OUT} (V)	0.9	2.8	0.7-1.2	0.5-1	1	1	2.35	1	1	1.6-3.6	0.55	
Dropout Voltage (mV)	300	200	200	200	200	200	150	200	200	200	200	
I_{Q} (μA)	6000	65	43	8	408	28-380.1	7	45	0.9-82.4	41.5	15.9*-487	
I_{OUT} (max) (mA)	100	50	100	100	100	100	100	50	100	200	50	
Total On-Chip Cap. (pF)	600	21	6	7	1.8	10	7.5	41	4.5	43.2	4.1	
Load Cap. Range (F)	600p	0-100p	0, 100p, 1n	0-50p	0-1n	0-100p	0-100p	0-1n	0-100p	40p	470p-10n	
Line Reg. (mV/V)	N/A	23	N/A	3.78	4.3	0.39	1	N/A	4.7	8.9	4	
Load Reg. (mV/mA)	1.8	0.56	0.4	0.1	0.003	0.0782	0.08	N/A	0.3	0.108	0.18	
PSR @1kHz (dB)	N/A	-57	N/A	-44	-56	-49.8	N/A	N/A	-58(@10kHz)	N/A	-51	
Settling Time (μs)	N/A	15	3	5	N/A	N/A	~ 0.15	~ 4	6	0.65	0.25	
$I_{\text{L(min)}}$ (mA) [†]	0	0	1	3	1	0	0.05	1	0	0.5	0	1
ΔI_{OUT} (mA)	100	50	99	97	100	100	99.95	49	100	199.5	50	49
ΔV_{OUT} (mV)	90	90	70	114	35	105	243	70	68.8	385	113	24
Edge Time (μs)	0.0001	1	1	0.1	0.01	1	0.5	1	300	0.5	0.1	0.1
Edge Time Ratio K	1	10000	10000	1000	100	10000	5000	10000	3000	5000	1000	1000
FOM	0.0054	1.17	0.304	0.0094	0.014	0.294	0.085	0.643	0.0019	0.4	0.036	0.0079

* Quiescent current includes the current consumption of bias circuit. † The minimum I_{L} used to test the transient performance. # Estimated area.

As can be seen from Table 5.9, the WCF LDO regulator design achieves a comparable or better FOM with respect to the reported OCL-LDO regulators. In addition, it can drive a wide C_L range with fast settling time and good performance metrics such as load regulation, line regulation and PSR.

5.7. Summary

A Type-II OCL-LDO regulator using weighted current feedback (WCF) technique is proposed in this Chapter. It establishes a weighted negative current feedback loop and provides an adaptive bias to the inter-gain stage. This permits smart management of the output impedance and gain of the inter-gain stage. As a result, using the WCF circuit technique and Routh–Hurwitz stability criterion to devise the design strategy and access the stability, the regulator can achieve stable operation, high accuracy and fast response simultaneously with small quiescent power consumption.

Validated by UMC 65-nm CMOS process, the simulation and measurement results have demonstrated that the WCF technique can stabilize the LDO regulator for load capacitance ranging from 470 pF to 10 nF whilst maintaining a very good transient performance metrics. The WCF regulator design reaches a comparable or better FOM with respect to the reported OCL-LDO regulators. Therefore, the WCF LDO regulator topology is useful for fully on-chip applications with wide load capacitance range.

Figure 5.20 gives an overall comparison of the performance metric using the maximum C_L versus quiescent current for the reported OCL-LDO regulators and the proposed Type-I and Type-II LDO regulators. For Type-I LDO regulator, under a quiescent current of 23.7 μA and a supply of 1.2 V, it achieves an undershoot of 40 mV and an overshoot of 19 mV when I_L is switching from 0 mA to 50 mA in 100 ns. The settling time is 1.65 μs . Based on Table 4.7, the Type-I LDO regulator offers one of the smallest undershoot/overshoot and settling time. Thus, the FOM of Type-I LDO regulator are significantly better or comparable with other reported designs whilst supporting the widest C_L range. Regarding the Type-II LDO regulator, under a quiescent current of 15.9 μA and a supply of 0.75 V, it displays an undershoot of 113

mV and an overshoot of 29 mV when I_L is switching from 0 to 50 mA in 100 ns. The settling time of this LDO regulator is only 250 ns. Based on Table 5.9, the Type-II LDO regulator achieves one of the smallest settling time. It also offers better or comparable FOM with respect to other LDO topologies. Therefore, it has demonstrated that both regulators have achieved wide C_L range driving ability whilst featuring small quiescent power and fast transient speed. As such, these two LDO regulators contribute the main part of this research work. They are useful for fully on-chip power management applications.

Fig. 5.20: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators and the proposed two wide C_L range LDO regulators.

CHAPTER 6

PROCESS, VOLTAGE AND TEMPERATURE (PVT) COMPENSATION FOR DIGITAL CIRCUIT SYSTEMS

In this Chapter, a review of reported PVT compensation techniques for digital circuit systems is firstly introduced. Then, a fully on-chip PVT compensated supply (PVTCS) which is targeted for point-of-load digital system is proposed. The working principle, circuit implementations, simulation and measurement results and performance comparison are presented and discussed in details.

6.1. Review of PVT compensation techniques

As discussed in Chapter 1, as technology scales down, the digital circuit performance exhibits high sensitivity to PVT variations. To tackle this issue, an adaptive body bias and adaptive supply control can be applied. For the adaptive bias technique, the threshold voltage (V_{TH}) of the devices can be adjusted accordingly through modifying the body voltage of the transistors. This turns out that the current and the speed or delay of the digital circuits can be changed. The prior-art adaptive body bias techniques are discussed as follows.

6.1.1. Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations

Fig. 6.1: Block diagram of adaptive body bias for reducing impacts of Die-to-Die and Within-Die parameter variations [51].

A bidirectional adaptive body bias technique is utilized in [51] to reduce the die-to-die (D2D) and within-die (WID) variations, with the circuit architecture shown in Fig. 6.1. As indicated, a target precision clock signal ϕ which represents the desired working frequency of the circuit is applied externally. The critical path output is then compared with ϕ through a phase detector. The comparison output “PD” is used to clock a 5-bit counter whose output is converted to a body bias voltage V_{BP} . Using this V_{BP} , the body voltage of the PMOS transistors in the digital load circuit as well as the critical path in Fig. 6.1 is adjusted simultaneously. Finally, the speed of digital load circuit can be set according to the designed clock frequency. This method is simple and effective, the measurement results have shown that it can reduce the die frequency variation by a factor of seven (85.7%).

6.1.2. Mixed Body Bias Technique with Fixed V_{TH} and I_{ds} Generation Circuits

Fig. 6.2: Fixed V_{TH} and I_{ds} generator [46].

In this method, a body bias control is applied on both the NMOS and PMOS transistors to ensure the V_{TH} and saturation current (I_{ds}) are fixed [46]. The fixed V_{TH} and I_{ds} generator is shown in Fig. 6.2. A bandgap voltage reference (BGR) generates two reference voltages to define V_{gsn} and V_{gsp} . Meanwhile, a current generator (CG) generates the adequate current to bias the body bias generator (BBG). Since the body voltage of the NMOS can be a negative value, a negative bias voltage generator (NBG) is realized by using a charge pump circuit. The simplified schematic of the BBG is depicted in Fig. 6.3, the body voltage V_{bn} is adjusted such that the V_{GS} of the NMOS transistor is equal to the constant V_{gsn} at a bias current of $CGN1$. The same goes for the PMOS transistors. The generated V_{bn} and V_{bp} will be applied to the digital circuits. As a consequence, the transistor's V_{TH} and I_{ds} are fixed and the digital circuit's speed is constant. This circuit technique is targeted for reducing the temperature variation of the digital circuits. The measurement results have proved that it can reduce the delay

variation by 85% under temperature variation when compared with the normal body bias technique.

Fig. 6.3: Fixed V_{TH} and I_{ds} body bias generator [46].

6.1.3. On-chip PVT Compensation Technique Using Current Monitoring Circuit

An on-chip PVT compensation technique using a current monitoring circuit is reported in [45] as illustrated in Fig. 6.4. The V_{TH0} generator in [63] is used to generate a constant current I_{REF} [74] which is then applied to the replica NMOS and PMOS diode transistors. Through a DC-DC converter which works as a buffer, the supply of the digital circuits is set to be equal to V_{GS} of NMOS diode transistor ($V_{GSN} = V_{REF}$). Turning to the PMOS transistor, under the same bias current of I_{REF} , the body voltage V_{BP} is adjusted such that the V_{GS} of PMOS diode (V_{GSP}) is equal to V_{GSN} and V_{REF} . The body voltage V_{BP} is then applied to drive the body of the PMOS transistors in digital circuits. With this implementation, the current of NMOS and PMOS transistors in digital circuits are kept constant ($= I_{REF}$) irrespective to the process and temperature variations. As such, the speed variations of the digital circuit can be reduced. The simulation results have revealed that it can

improve the performance by 71% and 90.4% under the process and temperature variations.

In this compensation system, a switching DC-DC converter is utilized to power up the digital circuits and a substrate bias to compensate the variation of PMOS transistors. The switching regulator may limit the speed of response and increase the complexity, hence leading to the increase of silicon area in this compensation architecture.

Fig. 6.4: Schematic of the on-chip PVT compensation system [45].

6.1.4. PVT Compensation Using Adaptive Supply Control

As technology scales down, the effectiveness of body bias to control the V_{TH} of the devices is reduced due to a smaller body factor. Together with the potential latch up problem and the high leakage effect under high operating temperature, the application of adaptive body bias technique to reduce PVT variations is limited. Another compensation method is to adaptively change the supply of the digital circuit through post-silicon trimming [78, 79]. This method is effective but the cost is increased due to the post-silicon trimming process.

In brief, both the adaptive body bias and the adaptive supply control can compensate the PVT variations of the digital circuits. However, the inherent limitations of body bias including reduced body bias factor, potential latch up problem and high leakage limit its applications for modern CMOS technology. The adaptive supply control is another effective method to perform PVT compensation but an on-chip circuit topology is needed. In view of that, a fully on-chip PVT compensation supply (PVTCS) is proposed and discussed in the subsequent sections.

6.2. Proposed PVT Compensated Supply (PVTCS)

In this section, the operation principle, circuit implementation, simulation and measurement results, performance comparison and discussions are presented for the proposed PVTCS system.

6.2.1. Operation Principle

The circuit architecture of PVTCS with the load circuits is depicted in Fig. 6.5. It contains a reference block that generates both voltage and current references, two separate biased PMOS and NMOS (P/N) diodes to sense the process and temperature variation of the digital circuits, a three-port differential difference amplifier (DDA) to generate an accurate weight and to perform subtraction and addition functions, a LDO regulator to drive the digital load circuit and a digitally-tracked oscillator which models as a digital load. The reference block provides a reference voltage ($V_{REF}/2$) for the DDA. It also generates two reference currents (both equal to I_{REF}) to bias the respective P and N diode. The DDA compares the reference voltage $V_{REF}/2$ with respect to half of gate-to-source voltage of $V_{GSN}/2$ and half of source-to-gate voltage $V_{SGP}/2$. It aims to generate a PVT compensated V_R for the LDO regulator. Finally, the high speed LDO regulator serves as a buffer and provides the supply to power the digital circuit. This load circuit is modeled by the digital tracked oscillator in form of a chain of inverters or combinations of logic gates so as to evaluate the performance under PVTCS. Similar to [45], the process and temperature compensation principles are analyzed using the delay model of a CMOS inverter chain. It is shown in the following.

Fig. 6.5: Block diagram of the proposed PVT compensated supply (PVTCS) and load circuits.

6.2.1.1. Process Variation Compensation

From the Alpha-Power law MOSFET Model [47], the delay of a CMOS inverter t_d (t_{pLH} , t_{pHL}) can be expressed as

$$t_d \approx \left[\frac{1}{2} - \frac{1 - (V_{TH}/V_{DD})}{1 + \alpha} \right] t_T + \frac{C_L V_{DD}}{2I_D} \quad (6.1)$$

where t_T is the transition time of input waveform, α is the velocity saturation index. I_D is the saturation current of MOSEFT which is given as

$$I_D = \beta (V_{GS} - V_{TH})^a \quad (6.2)$$

where β is defined as $0.5\mu(T)C_{OX}(W/L)$, $\mu(T)$ is the mobility of the electrons or holes in which T is the operating temperature, C_{OX} is the gate oxide capacitance. In comparison, the mobility of electrons and holes and their velocity saturation indexes are much less variation with respect to that of the threshold values. Therefore, β in (6.2) can be approximated as a constant under process variation. Besides, for a fast digital system, t_T is small. Since V_{GS} in (6.2) can be approximated as V_{DD} , t_d in (6.1) can be simplified as

$$t_d \approx \frac{C_L V_{DD}}{2\beta(V_{DD} - V_{TH})^a} \quad (6.3)$$

In order to maintain the delay of an inverter chain as a constant under the scenario of process variation, $t_{pLH} + t_{pHL}$ must be kept constant, which are translated into the following relationship:

$$\begin{aligned} t_{pHL} + t_{pLH} &= \frac{C_L V_{DD1}}{2\beta_N (V_{DD1} - V_{THN1})^{a_N}} + \frac{C_L V_{DD1}}{2\beta_P (V_{DD1} - V_{THP1})^{a_P}} \\ &= \frac{C_L V_{DD2}}{2\beta_N (V_{DD2} - V_{THN2})^{a_N}} + \frac{C_L V_{DD2}}{2\beta_P (V_{DD2} - V_{THP2})^{a_P}} \end{aligned} \quad (6.4)$$

where V_{DD1} , V_{THN1} and V_{THP1} are the supply voltage and the threshold voltages for NMOS and PMOS at typical process corner respectively. V_{DD2} is the compensated supply voltage. V_{THN2} and V_{THP2} are threshold voltages for NMOS and PMOS under process variation. From (6.4), the added compensation supply voltage ΔV_{DD} can be obtained as

$$\begin{aligned} \Delta V_{DD} &= V_{DD2} - V_{DD1} \\ &\approx \frac{\alpha_P \Delta V_{THP} + \gamma \alpha_N \Delta V_{THN}}{\gamma \alpha_N + \alpha_P} \\ &= D \Delta V_{THN} + (1 - D) \Delta V_{THP} \end{aligned} \quad (6.5)$$

where

$$\begin{aligned} \Delta V_{THP} &= V_{THP2} - V_{THP1}, \\ \Delta V_{THN} &= V_{THN2} - V_{THN1}, \\ \gamma &= \frac{\beta_P (V_{DD1} - V_{THP1})^{\alpha_P + 1}}{\beta_N (V_{DD1} - V_{THN1})^{\alpha_N + 1}}, \\ D &= \frac{\gamma \alpha_N}{\gamma \alpha_N + \alpha_P} \end{aligned} \quad (6.6)$$

As indicated in (6.5), ΔV_{DD} is the summation of weighted values for ΔV_{THN} and ΔV_{THP} . This is regarded as the process compensation which is accomplished by adding

a fraction of the threshold voltage variations for respective NMOS and PMOS with a proper weight on the supply voltage. Moreover, based on (6.6), D is a function of β_N and β_P . This turns out that the equivalent aspect ratios (W/L) of PMOS and NMOS transistor in the logic gates affect the weight factor D . In this work, the transistors in the logic gates of digital circuits are sized such that D is around 0.5. This is also commonly used in digital circuit design because when D is 0.5, $t_{pLH} \approx t_{pHL}$ which leads to a symmetrical pull down/up performance. Table 6.1 lists the numerical values for the P and N diodes and the calculated weight D using (6.6). It has shown that the calculated D is very close to the simulated value of 0.5, which validates the analysis.

TABLE 6.1 NUMERICAL CALCULATION AND VALUE OF WEIGHT D

Parameters	μC_{ox} ($\mu A/V^2$)	W/L (nm/nm)	β ($\mu A/V^2$)	α	V_{TH} (mV)	D
NMOS	48.9	720/65	271	1.641	389.1	0.4857
PMOS	29.04	2160/65	482	2.09	367.2	

6.2.1.2. Temperature Variation Compensation

Under temperature variation, the mobility of electrons and holes $\mu(T)$ displays a complementary-to-absolute-temperature (CTAT) characteristic. When the temperature increases, β [$=0.5\mu(T)C_{OX}(W/L)$] decreases. Since the threshold voltage also shows a CTAT characteristic [63], the temperature deviation of t_d in (6.3) is determined by the rate of change in β and V_{TH} against temperature for an un-compensated supply (UCS). Of particularly noted, ΔV_{THN} and ΔV_{THP} in (6.5) also involve the V_{TH} variation when temperature changes. If the process compensated ΔV_{DD} is applied to the nominal supply to partially track with the V_{TH} changes as depicted in (6.5), the variation of t_d can be partially compensated when temperature varies. On the other hand, when temperature increases, β_N and β_P decrease. Meanwhile, the temperature coefficient of

V_{THN} is not equal to that of V_{THP} . This leads to different values for ΔV_{THP} and ΔV_{THN} across the temperature range. Taken these two effects into account, a temperature compensation error exists in ΔV_{DD} according to (6.5). Based on the observed temperature behavior in the simulation, ΔV_{DD} needs to be slightly reduced in order to tackle the temperature compensation error when temperature increases. This is accomplished by injecting a CTAT current into the P and N diodes. As such, when the temperature increases, a temperature-dependent biasing current in the P and N diodes will cause V_{DD2} to be further reduced. This in turn eliminates the temperature compensation error and keeps t_d almost independent of temperature variation.

6.2.1.3. Supply Independency

Refer to Fig. 6.5, the nominal value of supply is decided by the bandgap output voltage V_{REF} . After adding the process and temperature compensation voltages, the final supply voltage of digital system is well defined. Due to the power supply rejection (PSR) of the reference block, the DDA and the LDO regulator, the output voltage V_{DD_C} is insensitive to the supply fluctuation. This permits the performance of the digital circuits insensitive to the supply variation.

6.2.2. Circuit Implementation

The PVTCS in Fig. 6.5 is implemented in a UMC 65-nm CMOS process. The detailed circuit topology for each block is discussed as follows.

6.2.2.1. Reference Block and P/N Diodes

Figure 6.6 shows the reference block circuit together with the P and N diodes formed by the transistors M_N and M_P , respectively. R_{iA} is equal to R_{iB} for $i = (2, 3, 5, 6)$ to achieve a good matching characteristic. To get a reasonable precise V_{REF} , a current-mode bandgap voltage reference topology [54] is utilized. It can provide a low T.C. metric with low supply and low power consumption. The current I_{REF} comprises two parts: I_1 and I_2 . Due to the small T.C. property of V_{REF} and the negative T.C. property of R_1 – R_3 , the current $I_1(T)$ ($\propto V_{REF}/(2R_{3B})$) shows a PTAT characteristic. At this juncture, through a voltage-to-current converter formed by the amplifier and R_4 , $I_2(T)$ is generated and its value is equal to V_A/R_4 , where V_A is the voltage at node A. Since V_A is a CTAT voltage, $I_2(T)$ exhibits CTAT characteristic as well. $I_2(T)$ is designed to be 3 times of $I_1(T)$, the summed current ($I_{REF}(T) = I_1(T) + I_2(T)$) flowing into the respective P and N diode retains a CTAT property.

M_P and M_N are the process and temperature sensing transistors which operate in saturation region on the basis of diode topology. Due to process variation of resistors, I_1 and I_2 may deviate from their designed values. To alleviate the V_{GS} drift rising from this variation, the aspect ratios of M_N and M_P are designed to be relatively large. In addition, M_N and M_P are placed in close vicinity to the target digital circuit in order to accurately sense the process and temperature information.

Figure 6.7 depicts the Monte-Carlo simulation results for $V_{REF}/2$ and I_{REF} under different temperatures. The results have shown that the reference block can generate a

temperature stable V_{REF} and a linear CTAT current under process and temperature variations.

Fig. 6.6: Voltage and current reference circuits.

Fig. 6.7 Monte Carlo simulation results for $V_{REF}/2$ and I_{REF} under different temperatures.

6.2.2.2. Differential Difference Amplifier (DDA)

DDA is an extension of the op-amp concept dedicated to the multiple floating voltages being forced to equal in a closed-loop feedback circuit [102]. It can be utilized to perform both the addition and subtraction operations. The symbolic as well as the schematic for a 3-port DDA circuit is shown in Fig. 6.8(a) and Fig. 6.8(b), respectively. In this design, the aspect ratio $S(M_{3A}/M_{3B})$ is twice of $S(M_{1A}/M_{1B})$ and $S(M_{2A}/M_{2B})$. Since the bias current is doubled in M_{3A}/M_{3B} , the transconductance (g_m) of M_{3A}/M_{3B} are two times as that of M_{2A}/M_{2B} and M_{1A}/M_{1B} . With this implementation, the final output voltage V_R can be obtained as

$$\begin{aligned} V_R &= \frac{V_{GSN} - V_{REF}}{2} + \frac{V_{GSP} - V_{REF}}{2} + V_{REF} \\ &\approx \frac{\Delta V_{THN}}{2} + \frac{\Delta V_{THP}}{2} + V_{REF} \end{aligned} \quad (6.7)$$

As revealed in (6.7), the V_{TH} variations (ΔV_{THN} and ΔV_{THP}) arising from the process and temperature variations are embedded into the normal V_{REF} with the appropriate weights. Since the designed weight for respective ΔV_{THN} and ΔV_{THP} is 0.5, we have $S(M_{iA}) = S(M_{iB})$, $S(M_{iC}) = S(M_{iD})$ for $i = (4, 5, 6)$. If a different weight of ΔV_{THN} and ΔV_{THP} is required, the current mirror ratio of $S(M_{iA})/S(M_{iB})$ and $S(M_{iC})/S(M_{iD})$ for $i = (4, 5, 6)$ can be changed accordingly.

Figure 6.9 shows the simulated V_R for different V_{GSN} and V_{SGP} . V_{REF} is set to be 0.6V. As indicated, the DDA can perform both subtraction and addition functions and generate an accurate V_R based on (6.7).

Fig. 6.8: (a) Symbolic and (b) Schematic of the 3-port differential difference amplifier (DDA).

Fig. 6.9: Simulated V_R under different V_{GSN} and V_{SGP} .

6.2.2.3. LDO Regulator

To drive the digital circuits, a low-dropout (LDO) regulator is employed and depicted in Fig. 6.10. It is based on a simple current-mode feedback buffer structure as the first gain stage whilst using a weighted current feedback (WCF) technique [96]. Through feeding back a weight current to the second gain stage, the WCF can reduce the output impedance to achieve stable operation. Moreover, owing to the low output impedance and the adaptive biasing characteristic for the power transistor driving stage, the regulator has a fast transient response. Due to the point-of-load digital circuit, the minimum C_L in this regulator is designed to be 200 pF and a simple Miller compensation is utilized.

Fig. 6.10: LDO regulator circuit.

Figure 6.11 shows the simulated transient response of the LDO regulator when I_L switches from 1mA to 50 mA in 50ns. As indicated, the LDO regulator displays a

small undershoot and overshoot with fast settling time. Therefore, it is suitable to drive the fast switching digital circuits.

Fig. 6.11. Simulated transient response for the LDO regulator.

6.2.2.4. Digital Tracked Oscillator

To demonstrate the effectiveness of PVT compensated supply, two digital tracked oscillator blocks are investigated. The first circuit block is a 41-stage inverter chain (Fig. 6.12(a)) to generally model the digital logic gates. The second circuit is a sample critical path (Fig. 6.12(b)) with 45 CMOS logic gates including inverter gates, NAND gates, NOR gates and Transmission gates which are similar to that of the test circuit in [44, 51]. Both circuits are configured as an oscillator. The oscillation frequency is examined under PVT variations. The inverter chain is implemented into silicon to demonstrate the effectiveness of the PVTCS. To ease the measurement, a frequency divider with 64x division is employed to reduce the measured frequency. Extensive simulations of both the inverter chain and the critical path circuit are also conducted.

Fig. 6.12: Digital load circuits configured as oscillators: (a) Inverter Chain and Critical Path Circuit [27, 60].

6.2.3. Results and Discussions

The microphotograph of proposed circuit is depicted in Fig. 6.13. The active area of the supply system (including the reference block, DDA, and LDO regulator) is 0.1053 mm^2 . The supply for the reference block and DDA is 1.2 V whilst the supply for LDO regulator is 0.9 V. The total power consumption is $734 \text{ } \mu\text{W}$. To evaluate the improvement factor, the oscillation frequencies from the inverter chain and the critical path using the PVTCS and UCS (nominal value is 0.6 V) are both obtained. The results and discussions are in the subsequent sub-sections as follows.

Fig. 6.13: Microphotograph of the PVT compensated supply system.

6.2.3.1. Results of Inverter Chain

To verify the process variation compensation performance, Monte Carlo (MC) simulations are conducted. The sample size is 500 with 3 sigma (3σ) variation

coverage. Figure 6.14 shows the simulated oscillation frequency distribution of the inverter chain under MC simulations at $T = 27^\circ$. With the PVTCS, the standard deviation (σ) of the oscillation frequency is reduced by 45.2%.

Fig. 6.14: Comparison of oscillation frequency of inverter chain under MC simulations when (a) PVTCS and (b) UCS is applied.

Fig. 6.15 compares the simulated oscillation frequency when the temperature changes from -40 to 90°C . If the total frequency variation across the temperature range (-40 to 90°C) is defined as $\Delta f = f_{\text{max}} - f_{\text{min}}$, the ratio of Δf over the room temperature frequency f_{mean} ($\Delta f/f_{\text{mean}}$) is obtained. The result has suggested that $\Delta f/f_{\text{mean}}$ is reduced by 91% from the comparison between the PVTCS and UCS.

Fig. 6.15: Comparison of oscillation frequencies of inverter chain under temperature variation between PVTCS and UCS.

Fig. 6.16: Comparison of oscillation frequency of inverter chain for measured 12 chips at (a) PVTCS and (b) UCS.

The measured frequency distribution of 12 chips at room temperature is illustrated in Fig. 6.16(a) for the PVTCS and 6.16(b) for the UCS. Due to the limited samples, the

compensation improvement is smaller than that of the simulated value in Fig. 6.14. However, with PVTCS, the σ of the oscillation frequency still shows a 33% reduction.

Figure 6.17(a) and 6.17(b) present the measured $\Delta f/f_{\text{mean}}$ (same definition as that in Fig. 6.15) distribution when the temperature changes from -40 to 90 °C for PVTCS and UCS, respectively. The average value (μ) of $\Delta f/f_{\text{mean}}$ is reduced by 82.9% when the PVTCS is applied.

Fig. 6.17: Comparison of oscillation frequency variation of inverter chain under temperature variation for measured 12 chips at (a) PVTCS and (b) UCS.

The test result of supply variation is illustrated in Fig. 6.18. For the PVTCS system, the supply voltages of the reference block, the DDA and the LDO regulator are

varied by $\pm 5\%$. Regarding for the UCS performance, the supply voltage of inverter chain is also varied by the same amount. As indicated, the frequency of inverter chain is independent of the supply change for the PVTCS system since the supply voltage of the inverter chain is generated internally by the reference block and DDA. On the contrary, when the UCS increases or decreases by 5%, the frequency is increased or decreased by around 25%. UCS digital circuit is considered quite sensitive to the supply voltage variation.

Fig. 6.18: Normalized oscillation frequency variation of inverter chain under supply variation for measured 12 chips at PVTCS and UCS.

Figure 6.19 depicts the measured waveforms for a single chip under simultaneous temperature and supply variations for both PVTCS and UCS. When the PVTCS is applied, the frequency variation is significantly reduced by 93.8% under temperature and supply variations. Through the built-in frequency divider, the measured frequency values shown in Fig. 6.19 are 1/64 of the actual oscillation frequency of the inverter chain. From the simulation and measured results, it has confirmed that the PVTCS can reduce the frequency deviation of the inverter chain based oscillator under a total of PVT variations.

Fig. 6.19: Measured oscillation waveforms for a single chip under PVTCS and UCS at different input supply and temperature values.

6.2.3.2. Results of Critical Path

The simulated oscillation frequency distribution of critical path under MC simulations at PVTCS and UCS are presented in Fig. 6.20(a) and 6.20(b), respectively. Regarding the input supply variation in case of the PVTCS, σ of the frequency is reduced by 42.1%. Regarding the temperature variation, the result is shown in Fig. 6.21. Similar to the inverter chain, the PVTCS can significantly reduce the frequency deviation of the critical path circuit by 87.3% in the temperature range. Finally, when the supply voltage of critical path is decreased or increased by 5% on the basis of nominal value (0.6 V), the frequency of critical path is reduced by 23% or increased by 26%, respectively. It has confirmed that the PVTCS can minimize the speed deviation of the critical path under a total of PVT variations as well.

Fig. 6.20: Comparison of oscillation frequency of critical path under MC simulations at (a) PVTCS and (b) UCS.

Fig. 6.21: Comparison of oscillation frequency of critical path under temperature variation at PVTCS and UCS.

6.2.3.3. Performance Comparison

Table 6.2 summarizes the simulated $\Delta f/f_{\text{mean}}$ for both inverter chain and critical path under worst case in corresponding corner of UCS and PVTCS. As indicated, the PVTCS can significantly reduce the variations of the $\Delta f/f_{\text{mean}}$ in worst case corners. Table 6.3 compares the performance of the proposed PVT compensation supply system with the other reported works. Due to the mismatch of sensing P diode, N diode and the digital circuit transistors, the PVTCS shows reasonable compensation improvement during process variations. However, both the simulation and the measurement results have validated that the PVTCS can reduce the σ of oscillation frequency from 30% to 40%. For the temperature compensation, the PVTCS shows better than 80% improvement. Finally, the PVTCS is insensitive to the supply variation which in turn shields the digital circuits from the noisy supplies. Most significantly, due to the simple adaptive supply voltage control mechanism without affecting the body voltage of the digital circuits, the PVTCS system is reliable without encountering the latch-up issue.

TABLE 6.2 PERFORMANCE IMPROVEMENT OF THE PVTCS WITH RESPECT TO THE UCS AT WORST CASES

Parameters	Inverter Chain			Critical Path		
	PVTCS	UCS	Improv. Factor	PVTCS	UCS	Improv. Factor
SS, -40°C, $V_{DD} - 5\%$	27.2%	79.9%	65.9%	28.7%	80.7%	64.4%
FF, 90°C, $V_{DD} + 5\%$	38.6%	123%	68.6%	38.2%	123%	68.9%

SS: Slow NMOS Slow PMOS. FF: Fast NMOS Fast PMOS.

TABLE 6.3 PERFORMANCE COMPARISON WITH RESPECT TO THE REPORTED PVT COMPENSATION CIRCUITS

Parameters	JSSC[51]	JSSC[46]	IEICE[45]	TVLSI[44]	TVLSI[50]	This Work		
Year	2002	2005	2010	2011	2012	2014		
Process (nm)	150	130	350	65	65	65		
Power (μW)	NA	N/A	141	N/A	N/A	734		
Body Bias	Yes	Yes	Yes	Yes	Yes	No		
Sim./Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim. Inv. Chain	Meas. Inv. Chain	Sim. Crit. Path
Process Var.	85.7%	N/A	71%	82.1%	84.8%	45.2%	33%	42.1%
Temperature Var.	N/A	85%	90.4%	N/A	N/A	91%	82.9%	87.3%
Supply Var.	N/A	N/A	N/A	N/A	N/A	22.5%	21.2%	23%

6.3. Summary

In this Chapter, the PVT compensation techniques using adaptive body bias and adaptive supply control are firstly reviewed. The limitations and advantages of each method are discussed.

Followed by the review, a point-of-load digital system supply with PVT compensation (PVTCS) is proposed. By adding a weighted combination of the variation of V_{TH} from the P/N transistor diodes on the supply, the delay and the speed of the digital circuits can be kept constant. The operation principle and circuit implementation of each block of the PVTCS are all presented. Validated in a UMC 65-nm process with both inverter chain and critical path digital circuit examples, the simulation and measurement results have demonstrated the PVTCS can minimize the speed deviation of digital circuits under a total of PVT variations. With an on-chip high speed LDO regulator as a supply driver, the PVTCS, which is latch-up free design, is suitable for driving fully on-chip point-of-load digital circuit with PVT compensation.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

This Chapter gives the conclusions and future work of this research work.

7.1 Conclusions

This thesis presents a study of threshold monitoring circuits (V_{TH} sensor), wide load capacitance (C_L) range output capacitorless LDO (OCL-LDO) regulators and process-voltage-temperature (PVT) compensation techniques for digital circuit systems. All the proposed works are realized in CMOS 65-nm process and analyzed in detail. The results are compared with the representative state-of-the-art works. It turns out the performance metrics of each proposed work meet the design objectives.

The V_{TH} sensor circuits are firstly reviewed. It can generate the V_{TH} of the transistor device at absolute temperature (V_{TH0}). Therefore, it can provide the process information. The temperature compensation principle, design constraints under nanometer technologies are discussed. A current-mode second-order temperature compensated V_{TH} sensor is proposed by using the different temperature properties of resistors. It aims to reduce the nonlinear temperature effect of transistor gate-to-source voltage (V_{GS}) so as to achieve a low temperature coefficient (T.C.). The results have shown the proposed V_{TH} sensor design achieves a better T.C. with respect to other nanometer voltage reference based designs. It also achieves a comparable T.C. when compared to the V_{TH} sensor circuits which using long channel-length process technologies.

Regarding the LDO regulators, the relevant topologies are discussed. The fundamental understanding of output capacitor (OC) and output capacitorless (OCL) LDO regulators are both presented. The stability and transient performance of each topology are explored in detail. Due to the limitation of driving ability for the conventional frequency compensation techniques, the reported OCL-LDO regulators can only support small C_L range. This raises the motivation to research and investigate new circuit techniques to extend the C_L range driving ability.

Two circuit techniques for OCL-LDO regulator dedicated to drive wide C_L range are proposed. First, a Dual-Summed Miller Frequency Compensation (DSMFC) is employed on a flipped voltage follower (FVF) based regulator circuit architecture. By utilizing an additional simple Miller compensation stage on the basis of Single Miller Compensation (SMC), the non-dominant pole(s) can be pushed to a higher frequency. As such, the stability of regulator under wide C_L range conditions can be achieved. Second, based on a fast-transient multi-gain stage LDO regulator topology, a new weighted current feedback (WCF) technique is proposed. It can dynamically manage the output impedance as well as the gain of the inter-gain stage. With this circuit architecture, the WCF can avoid the right-half-plane (RHP) pole and push the left-half-plane (LHP) non-dominant complex pole pair to a higher frequency. This permits the regulator achieve good stability, high accuracy, fast speed under a wide C_L range. Of particular importance, both proposed wide C_L range LDO regulators achieve good transient figure-of-merit (FOM) with small compensation capacitance.

Finally, compensation techniques to address the performance variations of digital circuits under PVT variations are reviewed and investigated. The adaptive body bias and adaptive supply control are the two typical methods to reduce the PVT variations. Due to the fundamental limitations of body bias for large scale of digital circuits, a

fully on-chip PVT compensated supply (PVTCS) system is thereby proposed. Through adding a weighted combination of V_{TH} variation of PMOS and NMOS transistors onto the normal supply, the speed or delay variations of digital system can be minimized in the context of PVT variations. The WCF technique is also utilized in the regulator design of the PVTCS system.

Overall, the small T.C. V_{TH} sensor, wide C_L range LDO regulators and the PVT compensation supply will be useful for on-chip circuits and systems, particularly for power management system.

7.2 Future Works

The V_{TH} sensor circuit, wide C_L range LDO regulator and PVT compensated supply system have been successfully researched and realized. Although the design objectives of this research work have been met, there are further future research directions that can be investigated.

For the V_{TH} sensor design, low T.C. is achieved by using different type of resistors to construct a second-order temperature compensation. Under process variations, the resistor value may be hard to control, hence trimming is required. This will increase the cost due to the additional T.C. calibration procedure. Based on the limitation, further low T.C. V_{TH} sensor design without temperature trimming can be investigated.

The proposed Type-I and Type-II LDO regulators can drive 10 pF – 10 nF and 470 pF – 10 nF C_L range. Typ-I offers a wider C_L range but a slower response whereas Type-II offers a slightly small C_L range but a faster transient speed. Therefore, a new circuit techniques that can achieve fast transient response and a very wide C_L range, starting from 0 pF, are still in demand.

Besides, digital implementation LDO regulator can be useful due to the continual push from advanced CMOS nanometer technologies. This is mainly because digital implementation is less sensitive to environment disturbances and more robust to the process and temperature variations. It can also works at a lower supply voltage with low quiescent current consumption. This permits the increase of current efficiency of LDO regulator.

Regarding the PVT compensation systems, the proposed PVTCS can reduce the performance variations of digital circuits. However, the improvement factor for process variation is limited due to the mismatch of the P/N diodes and the target digital

circuits. As a result, more precision based process and temperature variation sensor for digital circuit needs to be explored to improve the sensing accuracy.

In addition, the current reference generator in PVTCS is implemented using the bandgap reference circuit and resistors. Due to the variation of resistor values, the generated currents may not be accurately generated, thus degrading the compensation effectiveness. Since the V_{TH} sensor can generate a PVT insensitive constant current source, the current reference design using the low T.C. V_{TH} sensor is another research direction.

Finally, to drive the fast transient digital circuit, the LDO regulator has to be fast with high power supply noise rejection. Therefore, high frequency PSR enhancement circuit techniques are desired. The same goes for the V_{TH} sensor circuit.

AUTHOR'S PUBLICATIONS

- 1) X. L. Tan, K. C. Koay, S. S. Chong, and P. K. Chan, "A FVF LDO Regulator With Dual-Summed Miller Frequency Compensation for Wide Load Capacitance Range Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1304-1312, May 2014.
- 2) X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A LDO Regulator with Weighted Current Feedback Technique for 0.47nF-10nF Capacitive Load" *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2658 – 2672, Nov. 2014.
- 3) X. L. Tan, P. K. Chan, and U. Dasgupta, "A Sub-1V 65-nm MOS Threshold Monitoring Based Voltage Reference" *IEEE Trans. Very Large Scale Integr. (VLSI) Syst. Appeared In IEEE Explore*.
- 4) X. L. Tan and P. K. Chan, "A Fully-Integrated Point-of-Load Digital System Supply with PVT Compensation" *IEEE Trans. Very Large Scale Integr. (VLSI) Syst. In Minor Revision*

REFERENCES

- [1] G. A. Rincon-Mora, *Analog IC design with low-dropout regulators*: McGraw-Hill, 2009.
- [2] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3-14, Jan. 2004.
- [3] P. Y. Wu, S. Y. S. Tsui, and P. K. T. Mok, "Area- and Power-Efficient Monolithic Buck Converters With Pseudo-Type III Compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1446-1455, Aug. 2010.
- [4] X. Zhang, P.-H. Chen, Y. Okuma, K. Ishida, Y. Ryu, K. Watanabe, *et al.*, "A 0.6 V Input CCM/DCM Operating Digital Buck Converter in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2377-2386, Nov. 2014.
- [5] G. Moschopoulos, P. K. Jain, L. Yan-Fei, and G. Joos, "A zero-voltage-switched PWM boost converter with an energy feedforward auxiliary circuit," *IEEE Tran. Power Electron.*, vol. 14, no. 4, pp. 653-662, Jul. 1999.
- [6] X. C. Jing, P. K. T. Mok, and M. C. Lee, "A Wide-Load-Range Constant-Charge-Auto-Hopping Control Single-Inductor-Dual-Output Boost Regulator With Minimized Cross-Regulation," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2350-2362, Oct. 2011.
- [7] X. C. Jing and P. K. T. Mok, "A Fast Fixed-Frequency Adaptive-On-Time Boost Converter With Light Load Efficiency Enhancement and Predictable Noise Spectrum," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2442-2456, Oct. 2013.
- [8] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 443-452, Mar. 2004.
- [9] P. Malcovati, M. Belloni, F. Gozzini, C. Bazzani, and A. Baschiroto, "A 0.18 μm CMOS, 91% Efficiency, 2-A Scalable Buck-Boost DC-DC Converter for LED Drivers," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5392-5398, Oct. 2014.
- [10] E. Lefeuvre, D. Audigier, C. Richard, and D. Guyomar, "Buck-Boost Converter for Sensorless Power Optimization of Piezoelectric Energy Harvester," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2018-2025, Sep. 2007.
- [11] G. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36-44, Jan. 1998.
- [12] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732-1742, Aug. 2007.

- [13] Y. H. Lam and W. H. Ki, "A 0.9V 0.35 μm Adaptively Biased CMOS LDO Regulator with Fast Transient Response," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 442-626.
- [14] K. N. Leung and Y. S. Ng, "A CMOS Low-Dropout Regulator With a Momentarily Current-Boosting Voltage Buffer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2312-2319, Sep. 2010.
- [15] M. Ho, K. N. Leung, and K. L. Mak, "A Low-Power Fast-Transient 90-nm Low-Dropout Regulator With Multiple Small-Gain Stages," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2466-2475, Nov. 2010.
- [16] S. Kose, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter-Based Hybrid On-Chip DC-DC Converter for Point-of-Load Voltage Regulation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 4, pp. 680-691, Apr. 2013.
- [17] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691-1702, Oct. 2003.
- [18] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933-940, Apr. 2005.
- [19] H. Lee, P. K. T. Mok, and K. N. Leung, "Design of low-power analog drivers based on slew-rate enhancement circuits for CMOS low-dropout regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 9, pp. 563-567, Sep. 2005.
- [20] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A Low-Dropout Regulator for SoC With Q-Reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658-664, Mar. 2007.
- [21] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp. 1879-1890, Sep. 2007.
- [22] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 5, pp. 1392-1401, Jun. 2008.
- [23] P. Y. Or and K. N. Leung, "An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458-466, Feb. 2010.
- [24] J. Guo and K. N. Leung, "A 6- μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896-1905, Sep. 2010.
- [25] C. Zhan and W. H. Ki, "Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator for System-on-Chips," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 5, pp. 1017-1028, May 2010.
- [26] S. Lai and P. Li, "A fully on-chip area-efficient CMOS low-dropout regulator with fast load regulation," *Analog Integrated Circuits and Signal Processing* vol. 72, no. 2, pp. 433-450, Aug. 2012.

- [27] C. Zhan and W. H. Ki, "An Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator With Subthreshold Undershoot-Reduction for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 1119-1131, May 2012.
- [28] X. Ming, Q. Li, Z.-K. Zhou, and B. Zhang, "An Ultrafast Adaptively Biased Capacitorless LDO With Dynamic Charging Control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 1, pp. 40-44, Jan. 2012.
- [29] G. Giustolisi, G. Palumbo, and E. Spitale, "Robust Miller Compensation With Current Amplifiers Applied to LDO Voltage Regulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 1880-1893, Sep. 2012.
- [30] S. S. Chong and P. K. Chan, "A 0.9- μ A Quiescent Current Output-Capacitorless LDO Regulator With Adaptive Power Transistors in 65-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1072-1081, Apr. 2013.
- [31] Y. Kim and S. Lee, "A Capacitorless LDO Regulator With Fast Feedback Technique and Low-Quiescent Current Error Amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 6, pp. 326-330, Jun. 2013.
- [32] C.-J. Park, M. Onabajo, and J. Silva-Martinez, "External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4-4 MHz Range," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 486-501, Feb. 2014.
- [33] C. Zhan and W.-H. Ki, "Analysis and Design of Output-Capacitor-Free Low-Dropout Regulators With Low Quiescent Current and High Power Supply Rejection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 625-636, Feb. 2014.
- [34] K. C. Koay, S. S. Chong, and P. K. Chan, "A FVF based output capacitorless LDO regulator with wide load capacitance range," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 1488-1491.
- [35] W. Oh, B. Bakkaloglu, B. Aravind, and S. K. Hoon, "A Low 1/f Noise CMOS Low-Dropout Regulator with Current-Mode Feedback Buffer Amplifier," in *IEEE Custom Integrated Circuits Conf.*, Sep. 2006, pp. 213-216.
- [36] S. K. Hoon, S. Chen, F. Maloberti, J. Chen, and B. Aravind, "A low noise, high power supply rejection low dropout regulator for wireless system-on-chip applications," in *IEEE Custom Integrated Circuits Conf.*, Sep. 2005, pp. 759-762.
- [37] K. N. Leung, M. Ho, J. P. Guo, and P. Y. Or, "Development of energy-efficient fast-transient CMOS low-dropout regulators for SoC applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 305-308.
- [38] V. Ivanov, "Design Methodology and Circuit Techniques for Any-Load Stable LDOs with Instant Load Regulation and Low Noise," *Analog Circuit Design*, pp. 339-358, 2009.
- [39] L. Benini, A. Bogliolo, and G. De Micheli, "A survey of design techniques for system-level dynamic power management," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 3, pp. 299-316, Jun. 2000.
- [40] A. B. Kahng, S. Kang, R. Kumar, and J. Sartori, "Enhancing the Efficiency of Energy-Constrained DVFS Designs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 10, pp. 1769-1782, Oct. 2013.

- [41] A. Shye, B. Ozisikyilmaz, A. Mallik, G. Memik, P. Dinda, R. Dick, *et al.*, "Learning and leveraging the relationship between architecture-level measurements and individual user satisfaction," in *Proc. Int. Symp. Comput. Arch.*, 2008, pp. 427-438.
- [42] D. N. Truong, W. H. Cheng, T. Mohsenin, Y. Zhiyi, A. T. Jacobson, G. Landge, *et al.*, "A 167-Processor Computational Platform in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1130-1144, Apr. 2009.
- [43] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Body Bias Voltage Computations for Process and Temperature Compensation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 3, pp. 249-262, Mar. 2008.
- [44] H. Mostafa, M. Anis, and M. Elmasry, "A Novel Low Area Overhead Direct Adaptive Body Bias (D-ABB) Circuit for Die-to-Die and Within-Die Variations Compensation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 10, pp. 1848-1860, Oct. 2011.
- [45] Y. Tsugita, K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "An On-Chip PVT Compensation Technique with Current Monitoring Circuit for Low-Voltage CMOS Digital LSIs," *IEICE TRANSACTIONS on Electronics* vol. E93-C, no. 6, pp. 835-841, Jun. 2010.
- [46] M. Sumita, S. Sakiyama, M. Kinoshita, Y. Araki, Y. Ikeda, and K. Fukuoka, "Mixed body bias techniques with fixed V_t and I_{ds} generation circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 60-66, Jan. 2005.
- [47] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584-594, Apr. 1990.
- [48] M. Miyazaki, G. Ono, and K. Ishibashi, "A 1.2-GIPS/W microprocessor using speed-adaptive threshold-voltage CMOS with forward bias," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 210-217, Feb. 2002.
- [49] S. Hanson, Z. Bo, S. Mingoo, B. Cline, K. Zhou, M. Singhal, *et al.*, "Exploring Variability and Performance in a Sub-200-mV Processor," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 881-891, Apr. 2008.
- [50] H. Mostafa, M. Anis, and M. Elmasry, "On-Chip Process Variations Compensation Using an Analog Adaptive Body Bias (A-ABB)," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 4, pp. 770-774, Apr. 2012.
- [51] J. W. Tschanz, J. T. Kao, S. G. Narendra, R. Nair, D. A. Antoniadis, A. P. Chandrakasan, *et al.*, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396-1402, Nov. 2002.
- [52] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. 9, no. 6, pp. 388-393, Dec. 1974.
- [53] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/ $^{\circ}$ C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526-530, Apr. 2002.
- [54] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, *et al.*, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670-674, May 1999.

- [55] B.-S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 634-643, Dec. 1983.
- [56] K. N. Leung, P. K. T. Mok, and C. Y. Leung, "A 2-V 23- μ A 5.3-ppm/ $^{\circ}$ C curvature-compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 561-564, Mar. 2003.
- [57] R. T. Perry, S. H. Lewis, A. P. Brokaw, and T. R. Viswanathan, "A 1.4 V Supply CMOS Fractional Bandgap Reference," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2180-2186, Oct. 2007.
- [58] G. Ge, C. Zhang, G. Hoogzaad, and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of $\pm 0.15\%$ From 40 $^{\circ}$ C to 125 $^{\circ}$ C," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2693-2701, Nov. 2011.
- [59] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 146-150, Jan. 2003.
- [60] P.-H. Huang, H. Lin, and Y.-T. Lin, "A Simple Subthreshold CMOS Voltage Reference Circuit With Channel- Length Modulation Compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 9, pp. 882-885, Sep. 2006.
- [61] G. D. Vita and G. Iannaccone, "A Sub-1-V, 10 ppm/ $^{\circ}$ C, Nanopower Voltage Reference Generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536-1542, Jul. 2007.
- [62] L. H. C. Ferreira, T. C. Pimenta, and R. L. Moreno, "An Ultra Low-Voltage Ultra Low-Power CMOS Threshold Voltage Reference," *IEICE Transactions on Electronics*, vol. E90-C, no. 10, pp. 2044-2050, Oct. 2007.
- [63] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15 ppm/ $^{\circ}$ C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2047-2054, Jul. 2009.
- [64] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465-474, Feb. 2011.
- [65] J. Lee and S. Cho, "A 210 nW 29.3 ppm/ $^{\circ}$ C 0.7 V voltage reference with a temperature range of -50 to 130 $^{\circ}$ C in 0.13 μ m CMOS," in *IEEE Symp. VLSI Circuits*, Jun. 2011, pp. 278-279.
- [66] C.-Y. Hsieh, H.-W. Huang, and K.-H. Chen, "A 1-V, 16.9 ppm/ $^{\circ}$ C, 250 nA Switched-Capacitor CMOS Voltage Reference," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 4, pp. 659-667, Apr. 2011.
- [67] Z.-K. Zhou, P.-S. Zhu, Y. Shi, H.-Y. Wang, Y.-Q. Ma, X.-Z. Xu, *et al.*, "A CMOS Voltage Reference Based on Mutual Compensation of V_{tn} and V_{tp} ," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 341-345, Jun. 2012.
- [68] Z.-K. Zhou, P.-S. Zhu, Y. Shi, X. Qu, H.-Y. Wang, X.-M. Zhang, *et al.*, "A Resistorless CMOS Voltage Reference Based on Mutual Compensation of V_T and V_{TH} ," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 9, pp. 582-586, Sep. 2013.

- [69] P. Kinget, C. Vezyrtzis, E. Chiang, B. Hung, and T. L. Li, "Voltage references for ultra-low supply voltages," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2008, pp. 715-720.
- [70] A. J. Annema, P. Veldhorst, G. Doornbos, and B. Nauta, "A sub-1V bandgap voltage reference in 32nm FinFET technology," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 332-333.
- [71] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534-2545, Oct. 2012.
- [72] M. Seok, G. Kim, D. Sylvester, and D. Blaauw, "A 0.5V 2.2pW 2-transistor voltage reference," in *Proc. IEEE Custom Integrated Circuit Conf. (CICC)*, Sep. 2009, pp. 577-580.
- [73] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "Variability analysis of a digitally trimmable ultra-low power voltage reference," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2010, pp. 110-113.
- [74] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 46-ppm/°C temperature and process compensated current reference with on-chip threshold voltage monitoring circuit," in *Proc. Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2008, pp. 161-164.
- [75] J. Lee and S. Cho, "A 1.4- μ W 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2527-2533, Oct. 2012.
- [76] K. Kang, S. P. Park, K. Kim, and K. Roy, "On-Chip Variability Sensor Using Phase-Locked Loop for Detecting and Correcting Parametric Timing Failures," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 2, pp. 270-280, Feb. 2010.
- [77] M. Miyazaki, G. Ono, T. Hattori, K. Shiozawa, K. Uchiyama, and K. Ishibashi, "A 1000-MIPS/W microprocessor using speed adaptive threshold-voltage CMOS with forward bias," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 420-421.
- [78] J. W. Tschanz, S. Narendra, R. Nair, and V. De, "Effectiveness of adaptive supply voltage and body bias for reducing impact of parameter variations in low power and high performance microprocessors," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 826-829, May 2003.
- [79] T. Chen and S. Naffziger, "Comparison of adaptive body bias (ABB) and adaptive supply voltage (ASV) for improving delay and leakage under the presence of process variation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 5, pp. 888-899, Oct. 2003.
- [80] N. Olivieri, G. Scotti, and A. Trifiletti, "A novel yield optimization technique for digital CMOS circuits design by means of process parameters run-time estimation and body bias active control," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 5, pp. 630-638, May 2005.
- [81] N. Kamae, A. Tsuchiya, and H. Onodera, "An area effective forward/reverse body bias generator for within-die variability compensation," in *Proc. Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2011, pp. 217-220.

- [82] H. Mostafa, M. Anis, and M. Elmasry, "NBTI and Process Variations Compensation Circuits Using Adaptive Body Bias," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 3, pp. 460-467, Aug. 2012.
- [83] G. Ono, M. Miyazaki, K. Watanabe, and T. Kawahara, "An LSI system with locked in temperature insensitive state achieved by using body bias technique," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2005, pp. 632-635.
- [84] P. E. Allen and D. R. Holberg, *CMOS Analog Circuits Design*: Oxford University Press, 2000.
- [85] X. L. Tan, P. K. Chan, and U. Dasgupta, "A Sub-1V 65-nm MOS Threshold Monitoring Based Voltage Reference," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Appeared in IEEE Explore.
- [86] K. Kanda, K. Nose, H. Kawaguchi, and T. Sakurai, "Design impact of positive temperature dependence on drain current in sub-1-V CMOS VLSIs," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1559-1564, Oct. 2001.
- [87] Y.-S. SHYU and J.-C. WU, "A 60 μ A Quiescent Current, 250 mA CMOS Low Dropout Regulator," *IEICE Transactions on Electronics*, vol. E84-C, no. 5, pp. 693-703, 2001.
- [88] T. Y. Man, P. K. T. Mok, and M. Chan, "A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 9, pp. 755-759, Sep. 2007.
- [89] X. Qu, Z.-K. Zhou, B. Zhang, and Z.-J. Li, "An Ultralow-Power Fast-Transient Capacitor-Free Low-Dropout Regulator With Assistant Push-Pull Output Stage," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 2, pp. 96-100, Feb. 2013.
- [90] A. Yoo, "Design, Implementation, Modeling and Optimization of Next Generation Low-Voltage Power MOSFETs," PhD dissertation, Materials Science and Engineering, University of Toronto, 2010.
- [91] A. Yoo, M. Chang, O. Trescases, and W. T. Ng, "High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in a 0.25 μ m Standard CMOS Process," in *Int. Symp. Power Semiconductor Devices and IC's*, May 2008, pp. 95-98.
- [92] A. Hastings, *The Art of Analog Layout*: Pearson/Prentice Hall, 2006.
- [93] L. Baker, R. Currennes, S. Law, C. L. M. Le, and S. T. Lin, "A waffle layout technique strengthens the ESD hardness of the NMOS output transistor," in *EOS.ESD Symp. Proc. EOS-11*, 1989, pp. 175-181.
- [94] X. L. Tan, K. C. Koay, S. S. Chong, and P. K. Chan, "A FVF LDO Regulator With Dual-Summed Miller Frequency Compensation for Wide Load Capacitance Range Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1304-1312, May 2014.
- [95] V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE Int. SOC Conf*, Sep. 2004, pp. 311-315.

- [96] X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A LDO Regulator with Weighted Current Feedback Technique for 0.47nF-10nF Capacitive Load " *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2658 - 2672, Nov. 2014.
- [97] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511-520, Mar. 2003.
- [98] X. Peng and S. Willy, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2074-2079, Nov. 2004.
- [99] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in Reversed Nested Miller Compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1459-1470, Jul. 2007.
- [100] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 629-633, Dec. 1983.
- [101] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 919-925, Dec. 1984.
- [102] E. Sackinger and W. Guggenbuhl, "A versatile building block: the CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. 22, no. 2, pp. 287-294, Apr. 1987.