Model-based fault diagnosis for voltage source inverters

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Model-based Fault Diagnosis for Voltage Source Inverters

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Summary

This thesis introduces a fault detection and isolation (FDI) method for diagnosis faulty semiconductor switches of a pulsewidth modulated (PWM) voltage source inverter (VSI). This method analyses the pole voltage signals in a time-free domain called voltage space. For a healthy inverter, the projection of the state transitions in the voltage space results in a cubic pattern. It shows that each switch fault changes the voltage space pattern (VSP) uniquely that allows isolating the faulty switch. The mathematical model of the inverter can predict these patterns. Monitoring the transition vectors in the voltage space and comparing to the fault signatures can diagnose the faults. An experimental set-up has been designed and implemented to simulate the switch faults in a three-phase inverter. Simulations and experimental results validate the efficiency and consistency of the VSP-based FDI. The fault detection time is within only one PWM carrier period which is significantly faster than current-based conventional FDI methods. It shows that the VSP-based FDI method can overcome the FDI problem of multilevel multiphase inverters with only one voltage detector per phase leg. It is sufficiently fast to be integrated with a fault tolerant control to maintain maximum efficiency of the inverter in the presence of a faulty switch.

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List of Acronyms

ac	Alternative Current
AM	Amplitude Modulation
ASD	Adjustable Speed Drives
BG	Bond Graph
BJT	Power Bipolar-Junction Transistor
CBR	Case Based Reasoning
CMC	Cascade multilevel converter
dc	Direct Current
DCMC	Diode-Clamped Multilevel Converter
DVR	Dynamic Voltage Restorer
FACTS	Flexible ac Transmission Systems
FCMC	Flying Capacitors Multilevel Converter
FDI	Fault Detection and Isolation
FFT	Fast Fourier Transform
FTC	Fault Tolerant Control
GARRs	Global Analytical Redundancy Relations
GTO	Gate Turn-off Thyristor
HB	Half-Bridge
HBG	Hybrid Bond Graph
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LSE	Least Square Error
MBD	Model-Based Diagnosis
MCT	MOS Controlled Thyristor
MLI	Multi Level Inverter
MMC	Modular Multilevel Converters
MOSFET	Metal Oxide Field Effect Transistor
MPPT	Maximum Power Point Tracking
NN	Neural Networks
NPC	Neutral Point Clamped
P2MC	P2 Multilevel Converter

LIST OF ACRONYMS

PDE	Partial Differential Equation
PMSM	Permanent Magnet Synchronous Machine
PV	Photo Voltaic
PWM	Pulsewidth Modulated
rms	Root Mean Square
SIT	Static Induction Transistor
SITH	Static Induction Thyristor
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Compensators
TCG	Temporal Causal Graph
THD	Total Harmonic Distortion
UPFC	Unified Power Flow Controller
VSI	Voltage Source Inverter
VSP	Voltage Space Pattern
WTS	Wind turbine systems

List of Notation

$(\cdot)^T$	Matrix or vector transpose
$\bullet$	Elementary multiplication
$\text{diag}(\mathbf{x})$	Makes a diagonal matrix whose diagonal elements are the elements of vector $\mathbf{x}$
c	Control junction in HBG
d	derivative operator
$\oplus$	binary XOR operator
$\wedge$	Logical AND
$!$	Factorial
$\neg$	Logical NOT
$\vee$	Logical OR
$^\circ$	Degree
mod	Modulo operation
$\leftarrow$	Implied

Chapter 1

Introduction

Inverters are one of the most critical components found in every power plant generation and distribution systems. They are responsible to control the flow of energy between battery, grid, and load. Malfunctioning of them can decrease the efficiency of the power plant and may lead to catastrophic failure and shut down in the power system. Fig. 1.1 depicts a central inverter which is used in a solar power system. Each inverter consists of several switches that can fail to short-circuit or open-circuit faults. In this thesis, a FDI method is proposed to allocate switch faults in a three-phase VSI. The method is extended for the MLIs. After the faulty switch is detected, the switching patterns are reconfigured to tolerate the faulty condition and to prevent the propagation of the fault to the other components of the MLI.

Section 1.1 gives a brief introduction about power electronic inverters. Common faults in the inverters are described in Section 1.2. Section 1.3 discusses the motivation of doing FDI for power electronic inverters. Section 1.4 describes the problem formulation. The contributions of this thesis are stated in Section 1.5. Section 1.6 describes the organization of the thesis.

1.1 Power Electronic Inverters

In general, power electronic converters are classified into four groups as demonstrated in Fig. 1.2;

Figure 1.1: A standard household grid-connected solar energy system.

1. Dc–dc converters such as level shifters are used to maintain the amplitude of a dc source like a battery.
2. Dc/AC converters generate ac waveform from a dc source. Because their circuit topology looks like an inverted ac–dc converter, they are called inverters. An example of inverters is the ac motor drive in mobile applications which are used to control the frequency and torque in the ac motors.
3. Ac–dc converters, called rectifiers, are used to generate dc from an ac source such as line voltage. Battery chargers and adaptors used for laptops and mobile phones are common examples of ac–dc converters.
4. Ac–ac converters change the frequency of an ac source. Adaptors which generate 50Hz from 60Hz line voltage are an example of ac–ac converters. They are a combination of two cascade ac–dc and dc–ac converters.

In this thesis, a model-based FDI method for diagnosis switch faults in the inverters has been developed.

Figure 1.2: Power electronic converters.

1.1.1 Basic structure of an Inverter

Figure 1.3 depicts a single-phase HB inverter. This circuit is the basic module of more complicated inverters such as multi-phase MLI. The circuit combines two semiconductor switches, Q_1 and Q_2 , which are fully controlled through their gates. Based on the operating voltage, current, power, switching speed, temperature, and the other circuit requirements, the switch can be selected from the following semiconductor components used in their saturated region:

- Insulated Gate bipolar transistor (IGBT)
- Gate Turnoff Thyristor (GTO)
- Bipolar Junction Transistor (BJT)
- Metal Oxide Field Effect Transistor (MOSFET)
- Integrated Gate Commutated Thyristor (IGCT)
- Static Induction Transistor (SIT)
- Static Induction Thyristor (SITH)
- MOS Controlled Thyristor (MCT)

Figure 1.3: Single-phase VSI [1]

The switches are controlled in complementary states, i.e., when Q_1 is closed and Q_2 is open, $v_\phi = \frac{E}{2}$, and when Q_1 is open and Q_2 is closed, $v_\phi = -\frac{E}{2}$. Therefore, phase voltage, V_ϕ , have a rectangular waveform whose width is controlled by gate signals of the switches. In many applications, it is desired to obtain a sinusoidal waveform in the load side using SPWM technique.

1.1.2 Sinusoidal Pulse Width Modulation

There exist several modulation methods that are used to control switches of an inverter to generate desired output waveforms. They are classified into two main groups [2];

1. High switching frequency PWM (e.g., space vector PWM and sinusoidal PWM)
2. Fundamental switching frequency (e.g., space vector control and selective harmonic elimination)

Their objectives are to reduce THD and maintain desired amplitude and frequency in the generated ac waveform. In this thesis, inverters with SPWM control are considered.

SPWM is one of the most common modulation methods introduced by Schoänung in 1964 [17]. Figure 1.4 illustrates SPWM pulses generated by comparing a triangular carrier waveform, $c(t)$, to a reference modulating signal, $r(t)$, where

$$r(t) = A_r \sin(\omega_r t + \phi), \quad (1.1)$$

Figure 1.4: Reference, carrier, and PWM Signals.

$$c(t) = A_c tri(\omega_c t), \quad (1.2)$$

and,

$$p(t) = \begin{cases} 1 & \text{if } A_r > \frac{A_c}{M}, \\ 0 & \text{if } A_r \leq \frac{A_c}{M}. \end{cases} \quad (1.3)$$

$$(1.4)$$

In (1.2), tri is a triangular waveform which will be defined in the next chapter. From [18],

$$\begin{aligned} v_\phi(t) = & M \frac{E}{2} \cos(\omega_r t + \phi) + \frac{2E}{\pi} \sum_{\xi=1}^{\infty} \mathbf{J}_0\left(\frac{\xi\pi M}{2}\right) \sin\left(\frac{\xi\pi}{2}\right) \cos(\xi\omega_c t) \\ & + \frac{2E}{\pi} \sum_{\xi=1}^{\infty} \sum_{v=\pm 1}^{\pm\infty} \frac{\mathbf{J}_v\left(\frac{\xi\pi M}{2}\right)}{\xi} \sin\left(\frac{(v+\xi)\pi}{2}\right) \cos(\xi\omega_r t + v\omega_c t + (\xi+v)\phi) \end{aligned} \quad (1.5)$$

In (1.5), v_ϕ is the phase pole voltage, M is the modulation index which is defined as the ratio of the reference signal amplitude, A_r , and carrier signal amplitude, A_c , as shown in (1.6)

$$M = \frac{A_r}{A_c}. \quad (1.6)$$

The angular frequencies of the reference signal and carrier signal are ω_r and ω_c respectively, ϕ is the displacement angle between modulating and carrier signal, and $\mathbf{J}$ shows the Bessel functions of the first kind. Thus, the voltage signal contains infinite frequency contents.

The current signal is dependent to the load type and value. In the motor drive application, the load usually acts as a low pass filter. Hence the current waveform contains only the first component of the voltage spectrum. Thus, the current waveform is a sinusoidal signal with frequency ω_r . However, if the load cannot filter the harmonic frequencies well, the current waveform will contain some harmonics. Figure.1.5 shows a pulse shaped voltage of a full bridge inverter and the sinusoidal current after filtering. By increasing the switching frequency, the waveform looks more like a sinusoidal wave, i.e., the THD reduces. With the use of other topologies such as MLIs, low THD can be achieved with a lower switching frequency.

Figure 1.5: Output pulses before and after filter.

1.1.3 Multi-Level Inverters (MLIs)

In 1981 the principle of MLI was proposed [19] to reduce the THD in power inverters by proper phase shifting in multiple cascade unit inverters. Figure 1.6 depicts the schematic of basic MLIs.

The simplest MLI is a 2-level inverter or a HB inverter (Fig. 1.3) which generates two voltage levels in the output. By cascading N single-phase HB inverters, an n -level inverter can be achieved where

$$n = N + 1. \quad (1.7)$$

Nowadays, MLIs are becoming more popular in the solar plants. Because each solar panel can be controlled separately and the efficiency of the whole generation system can be increased. In a MLI lower rate switches can be used to achieve the same

Figure 1.6: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels [2].

level of voltage in comparison to a single two-level inverter with high rating switches. The multilevel VSIs can reach high levels of voltage and power without the use of transformers which extremely reduce their weight. Hence, they are becoming more popular in mobile applications such as electrical cars and space power systems.

Moreover, by synthesizing a great number of output levels, more sinusoidal output voltage waveforms will be achieved [20] and the THD can be decreased (Fig. 1.7). However, as it can be seen in Table 1.1, as the number of levels increases, the number

Figure 1.7: THD of the line voltage and current versus number of switches in MLIs [3].

of required components grows rapidly. Utilizing a large number of components brings

Converter configuration	DCMC	FCMC	P2MC	CMC
Main switching devices	$2(n-1)$	$2(n-1)$	$n(n-1)$	$2(n-1)$
Main diodes	$2(n-1)$	$2(n-1)$	$n(n-1)$	$2(n-1)$
Clamping diodes	$(n-1)(n-2)$	0	0	0
Dc bus capacitors	$n-1$	$n-1$	$n-1$	$\frac{n-1}{2}$
Balancing capacitors	0	$\frac{1}{2}(n-1)(n-2)$	$\frac{1}{2}(n-1)(n-2)$	0
Total	$n^2 + 2n - 3$	$\frac{1}{2}n^2 + 8n - 8$	$\frac{5}{2}n(n-1)$	$\frac{9}{2}(n-1)$

Table 1.1: Power component per phase leg required by n -level inverters [15].

reliability issues to the MLIs and limits their applications. Fault diagnosis of MLIs is a key to solve this limitation and to make the MLIs more reliable for safety critical applications.

1.2 Faults in Inverters

Electrolyte capacitors and semiconductor switches are reported to have the most failure rates in the electronic converters [21], [22], [23], [24], [25]. As reported in [26], the VSDs are responsible for 63% of the drive faults in the first year of usage. Approximately 70% of such faults are related to power electronic switches, e.g., short-circuit, open-circuit, and gate-misfiring faults [23], [26].

Power electronic switches are subject to failure due to thermal stress, aging, overloading, over voltage, and over current [27]. The failure may be caused by the electromagnetic spike, electrostatic discharge, unpredicted operational conditions, or transient condition of the system or ambient such as lightning [27]. The high instantaneous power dissipated in the switch increases the semiconductor temperature which is one of the most important roots of switch failure [28]. A switch fault, if not detected, may lead to catastrophic failure and damage the other components of the system.

Short-circuit faults, also known as transistor latch-ups, are one of the most common failures in semiconductor switches [29], [30]. When a short-circuit fault occurs, the switch become closed and remains in the on state regardless to the gate control voltage. The first problem occurring after a short-circuit fault is a very high current flowing in the two switches of one phase leg and the dc source, as soon as the other switch of

the leg is turned on [28]. These faults can cause severe damages to the battery or the load connected to the inverter. Open-circuit faults generally do not cause shutdown in the VSIs [31], however, they cause unbalance operation in the three-phase system and reduces the efficiency of the three-phase motor and causes failure to the motor drive and the mechanical load connected to it. On the other hand, short-circuit faults can cause an explosion [28] and an expensive down time [32] and must be stopped within a few microseconds [28] by means of a fast FDI method.

1.3 Motivation of FDI for Power Electronic Inverters

Inverters have a vital role in renewable electrical energy systems [33] and electrically driven loads in wind farms, solar plants, automotive, aerospace, marine vessel, and space power systems. Wind mills need frequency converters to generate 50 Hz line voltage. Solar panel plants need dc–ac inverters and dc–dc converters to regulate the output voltage. Inverters have also been used in adjustable speed drives (ASDs) to control the speed of ac motors, by changing the frequency of the ac voltage waveform as shown in Fig. 1.8. About 38% of the faults in ASDs in industry are because of failures in power converters [23] , [34].

Figure 1.8: An inverter connected to an ac motor [4].

To guarantee continuous safe operation of inverters, proper FDI methods are needed to detect the faulty component and propose fault tolerant strategies to extend the circuit

operation in presence of the faults and prevent unwanted shut down in vital systems. FDI is also an important part of PHM and can decrease the maintenance cost of large plants such as offshore wind farms (Fig. 1.9) and distributed solar plants (Fig. 1.10), where the inverters are placed in the areas difficult to access.

Figure 1.9: An offshore wind plant

Figure 1.10: A distributed solar plant

Recently, micro-inverters and MLIs have been introduced to be used in renewable electrical energy systems. With the use of micro-inverters, more efficient maximum power point tracking (MPPT) control for the photo-voltaic (PV) or wind power systems is possible [35]. They take advantage of lower rate, lower cost switches in comparison to conventional inverters. However, the reliability and maintenance of such systems are more difficult comparing to the central inverters, because of high number of

switches they have. Advanced control and integrated diagnosis of the grid converters are the requirements in the renewable electrical generation systems [36]. For example, for one phase leg of a 51-level diode clamped multi-level converter (DCMC), 100 power transistors would be required [37] (Refer to Table 1.1). Hence, for a three-phase 51-level inverter the number of switches increases to 300. As the number of switches increases, the probability of inverter failure grows rapidly, and FDI of them become extremely complicated. FDI of these switches is a bottle neck in growing new generation of solar systems based on MLIs.

Many fault diagnosis approaches have been used in the literature to detect abnormalities in the mechanical and electromechanical systems. However, these approaches cannot be applied directly to FDI for electronic circuits. Some of the challenges in FDI for electronic circuits from measurement limitations and fault nature aspects are listed bellows.

- **Sensor type:** There exist several kinds of measurements for electro-mechanical systems to monitor the system's behavior. For example, for FDI in a motor, vibration, sound, voltage, current, torque, speed, temperature, and a combination of them can be measured. While for electronic circuits, the information of fault should be extracted from either voltage and/or current.
- **Sensor placement:** Sometimes it is not practical to add extra sensors to the circuit. Also in the modern integrated circuits, there is limited accessibility to circuit nodes [38], [39].
- **Measurement errors:** The tolerance of the circuit elements can be mixed with the fault signatures [38], [39]. The ambient noise and disturbances can also affect the accuracy of the FDI. Some fault signatures may be omitted by the noise cancelers.
- **Degradation:** Analog circuits have a continuum of possible faults [38]. So, it is not possible to define a complete rule-based fault dictionary to map faults to the cause. There always can exist undefined situations and unknown faults.

- **Number of components:** In an electrical circuit, the number of components are much more than the number of components in a mechanical system. So, the the number of the candidate fault locations increases and isolation task would be extremely difficult.
- **Propagation time:** The constant time of the fault propagation is very short and fault to failure progress is very fast. Therefor, the fault detection time should be very short to provide enough time for fault management to prevent the failure.
- **Fault root:** The roots of faults in mechanical systems are well known, e.g., friction, temperature, vibration, while in an electrical system it is more complicated and not only the same mechanical roots can cause faults, but also electricity field, magnetic field, electrostatic shock, operation circumstances, and many other phenomenas can change the characteristics of electrical components. The roots of faults differ from circuit to circuit and the topology and design affects the cause-effect relationship.
- **Hybrid behavior:** Voltage and current variables of an analog circuit are continuous while switches have binary states. Therefor, inverters have a combination of discrete and continuous behaviors called hybrid systems. Switches introduce mode changes to the system. The circuit behavior for each mode can be completely different. If the current mode of the system is unknown, the FDI engine can fail. It is not easy to detect the current mode of the system because it is a time-variant nonlinear phenomena affected by the controller, load, and operation conditions.

1.4 Problem Formulation

This thesis aim to solve the FDI problem of VSIs using the minimum number of detectors and maximum FDI speed. To achieve these objective, an FDI method is developed based on the measurement of the pole voltage signals of the VSI. Unlike the existing FDI methods which require the voltage and/or current measurement of each switch in

the inverter, we aim to solve the FDI problem of a VSI with many switches with only one voltage detector per phase leg. In this case, the number of required sensors is reduced and the problem of sensor mounting will be solved.

Reduction of the FDI time is a main objective of this work which is the prerequisite of fault tolerant control. The existing FDI methods are either based on the measurements of the current output that results in a fault detection time in the order of one reference period, or are based on the measurements of voltage/current signals of each switch that need several additional sensors. In this thesis, the number of the required sensors is decreased to only a few pole voltage measurements of the output of the inverter, and in the meantime the fault detection time is decreased to only one switching period which is significantly shorter than a reference period.

The problem of using switching voltage signals for FDI purpose lays behind the time-variant behavior of the SPWM signals. The width of the PWM signals of the pole voltage varies with the frequency and amplitude of the reference signal caused by feedback loop or the operating condition. Also, SPWM signals contain a wide range of frequency contents. It is not possible to model the pole voltage behavior without knowing the details of the feedback loop, operating condition, and other parameters of the system. In this thesis, this problem is solved by developing VSP-based FDI method. The non-equal adjacent switching states are defined and the SPWM signals of the three phases are compared together in a time-free space.

Existence of several identical switches in the multi-phase multi-level inverters makes the FDI of these systems very complicated. The probability based methods fail to address the isolation problem of the faulty switches in the MLIs. In this thesis, an active isolation method is developed that can identify the faulty switches of a multi-phase multi-level inverter with only one voltage detector per phase leg.

Most of the model-based FDI method depends on the detail description of the circuit components. This makes the FDI methods device specific. Such approaches need tuning and adjustment for each type of switches. In this thesis, the FDI method is developed for a general on-off switch and can be applied for a wide range of switches which are used in their saturation on-off modes.

1.5 Contributions

This thesis has developed a frame work of a model-based FDI for faulty switches in VSIs. The concept of VSP-based FDI is proposed and the fault-banned zones are introduced as the fault signatures of the switches. Experimental set-up were built to simulate the switch faults and validate the VSP-based FDI method. Voltage-based fault detection, isolation, and fault tolerant control algorithms were developed for multi-level multi-phase inverters with large number of switches. It is shown that the switch faults are diagnosed successfully with only one voltage detector per phase leg. The fault diagnosis time is less than one switching period which is only limited by the implementation hardware. The main contributions of the thesis are as follow:

1. Modeling VSI based on its switching states: An input–output model of the three-phase inverter is built based on the on–off state of its switches. This model is based on the structure of the inverter and is independent to the type of the switch. It describe the input–output behavior of the inverter in the healthy situation and in presence of short-circuit or open-circuit switch faults.
2. Introduction of non-equal adjacent switching states: The switching states are defined and uniquely assigned to each switching mode of the inverter. It is proven that these states can be uniquely identified based on the digitized values of the phase voltage signals. The voltage signals are sampled with a constant sampling rate, hence, the calculated states have the same constant sampling rate. To extract the non-equal adjacent switching states, only the transitions of the states are considered that result in a sequence of switching states with non-equal adjacent members. Thus, a sequence of data with variable sampling time is achieved. Extraction of non-equal adjacent switching states, cancels out the time-variant behavior of the SPWM voltage signals. To our own advantage, it keeps the information about switches which are reflected in the state transitions and will use in the FDI stage.
3. Introduction of VSP: Dynamic patterns in the voltage space are introduced based on the non-equal adjacent switching states. It is shown that for a three-phase

two-level inverter the VSP constructs a cube in the voltage space. In the faulty situation, the VSP will be disturbed. Hence, by monitoring the VSP for a period of time the faulty switch can be isolated using fault signature sets. In this thesis the VSP is obtained from the digitized quantities of the pole voltages. However, the concept of VSP can be used for the continuous quantities. Since there exists a kind of symmetry in the three-phase quantities, the parameters that affect the three phases identically, do not change the VSP overall shape. For example, if a rise in the ambient temperature occurs, all of the switches reflect identically, hence, a symmetric cubic pattern will be obtained in the voltage space. However, if a temperature rise occurs in only one of the switches the cubic pattern will be distorted. Thus, by monitoring the centroid of the VSP, the incipient switch faults can also be detected. Thus, the VSP can be used for prognosis of the switch faults.

4. Introduction of FBZ: Fault banned zones are defined as the fault feature sets. It is proven that the VSP cannot enter a certain zone of the voltage space in the faulty conditions. These zones are calculated based on the structural model of the inverter. For a three-phase inverter, the fault-banned zones refer to a face of the cubic pattern. Six faces of the cubic pattern allow isolating six different faulty switches. The FBZ is independent to the modulation technique and is a time and frequency independent feature. Thus, the FDI based on the FBZ is very robust to the time variant behavior of the inverter. Also, the FBZs are the same for every type of switches used in the inverter. Therefore, the features are device independent which allow implementation of the VSP-based FDI method for a wide range of inverters without knowing the details of the switch's type and internal parameters.
5. Determination of FDI window for PWM VSI: For the isolation purpose, the switching states must be monitored for a window of time which is proven to be equal to one period of the PWM carrier signal. In this case, the FDI module needs to know the carrier frequency. However, the carrier frequency can be changed by

the feedback loop and might not be known for the FDI module. In order to make the FDI system independent of the switching frequency and feedback loop, the FDI window is defined based on the number of state transitions. The minimum numbers of required states in the FDI window is determined based on the modulation technique of the control module. It is proven that the minimum length of the FDI window is equal to six for a three-phase two level SPWM inverter.

6. Validation through simulation and experiment: Several simulation and experiments were run and the efficiency of the VSP-based FDI method was investigated. The performance of this method was validated for a three-phase VSI which was used as the drive of a PMSM motor. It is shown that the disturbances in the mechanical load of the motor does not affect the FDI result and all of the six switch faults are isolated quickly. Isolation of open-circuit and short-circuit faults in a six-switch inverter are investigated and the VSP were derived. The FDI time is calculated for every experiment.
7. Development of VSP-based FDI algorithm: The VSP-based FDI algorithm was developed and implemented in MATLAB Simulink. The FBZs are calculated automatically given the topology of the inverter. The switch faults are isolated based on the measurements of the phase voltage outputs. The algorithm includes a digitization state which is a prerequisite to calculate the switching states. Then the switch transitions are extracted the FDI window is formed. The FDI algorithm compares a finite number of non-equal adjacent switching states with the FBZ, and isolates the faulty switch.
8. Design and implementation of a fault simulator set-ups: In order to validate the VSP-based FDI method, a proper set-up was needed to simulate the switch faults. Therefore, a three-phase inverter was designed with six main switches and 12 relays in serial and parallel to the main switches. With this configuration, all of the open-circuit and short-circuit faults were simulated by opening and closing the fault insertion relays. So, the abrupt faults were simulated without damaging the switches. For the safety reasons, the experiments were carried

on with scaled down power quantities. In this set-up the data was gathered with an oscilloscope and was analysed later in the MATLAB Simulink. Thus, the FDI was implemented off-line and the switch faults were diagnosed successfully.

To improve the test-bed, another inverter was designed and implemented as a hardware-in-loop using MATLAB Real-Time Window Target. The SPWM control and VSP-based FDI algorithm were implemented in MATLAB and used as a block in the Simulink. Thus, an on-line control and diagnosis for the designed inverter was possible in this set-up. Nonetheless, the switching frequencies were scaled down because of low performance of Windows for the small sampling times. This set-up is appropriate for examining FDI, prognosis and fault tolerant control algorithms for several types of inverters in a laboratory scale.

9. Modeling multi-level cascade VSIs based on its switching states: The structural model of the three-phase VSI is modified and extended to model n -level m -phase cascade inverters. This modeling allows definition of the operating modes based on the switching states for normal and faulty situations.
10. Design for isolability: It is shown how to calculate the proper switching modes of a n -level m -phase cascade inverters with $(n - 1) \times m$ switches. The proper modes of the inverter are defined as the modes which allow obtaining all the healthy levels of the inverter in the output, and in the meantime guarantee the isolability of the switch faults. Using the proper modes of the system, the location of the faulty switch out of $m \times (n - 1)$ switches can be isolated with only one voltage detector per phase.
11. Development of voltage-based FDI for MLIs: An algorithm is developed to define the fault signatures of each switch and to detect and isolate a faulty switch of a n -level m -phase cascade inverters. In this method, the faults are diagnosed independently for each phase leg, and the diagnosis time is only $n \times T_s$ where T_s is the sampling time of the measurement. This method is validated in MATLAB Simulink for 4-level inverter with 18 switches.

12. Development of FTC algorithm for multi-phase MLIs: After the switch faults were successfully isolated, a fault tolerant control strategy is applied to control the inverter in the faulty condition. The FTC method achieved three results; protecting the other devices of the inverter, reducing the THD of the sinusoidal signal of the fault leg, and balancing the line voltage.

1.6 Organization of the thesis

This chapter gave an introduction to the FDI for power electronic inverters. The basic structure of the VSIs was also described. The rest of the thesis is organized as follows: Chapter 2 describes the model-based FDI techniques which have been applied for power electronic inverters in the literature. Chapter 3 proposes the VSP-based FDI method for diagnosis short-circuit switch faults in a three-phase 2-level inverter with six switches. The method is verified through simulations and experiments. The VSP-based FDI is modified to diagnose open-circuit faults in Chapter 4. FDI results from simulations and experiments for diagnosis open-circuit faults are shown in this chapter. The VSP-based FDI with some modifications for n -level m -phase inverters is described in Chapter 5. In Chapter 6 the FDI method has been applied to a 4-level 3-phase inverter and the SPWM switching patterns are changed to maintain minimum THD and maximum balance of the inverter in the presence of the faulty switch. Chapter 7 concludes the thesis and proposes future research directions.

Chapter 2

Literature Review

2.1 Introduction

This chapter reviews the FDI techniques which have been applied to the power electronic inverters.

Table 2.1 gives the terminology in the area of FDI. In [40] the fault and failure are defined with more details. The sequence of the FDI tasks are illustrated in Fig. 2.1.

Fault	Physical defect or material damage of an element or system causing a failure [4].
Failure	The state or condition of not meeting a desirable or intended objective [16].
Fault detection	Determination of faults present in a system [41].
Fault isolation	Determination of type, location and time of faults [41].
Fault identification	Determination of size and time-variant behavior of a fault [41].
Fault diagnosing	Combines fault isolation and fault identification [41].
Fault detection time	The time interval between fault occurrence and the fault detection.
Fault tolerance	The ability of a system to continuously operate in present of some faulty components.
Prognosis	To predict the remaining useful lifetime of the system.

Table 2.1: Terminology in the area of FDI.

When a fault occurs in a system, its performance degrades. Fault detection methods detect the abnormality in the system. Then the fault isolation process try to locate

the faulty component. The fault diagnosis usually contains fault detection, isolation and identification. Failure prognosis determines the remaining useful lifetime (RUL) of the system based on the severity of the fault. Fault tolerant control strategies aim to extend the operation of the system in presence of the faults. The fault isolation is the key toward failure prognosis and FTC. The model based diagnosis and the FDI techniques are described in the following sections.

Figure 2.1: FDI tasks.

2.2 Model-Based Diagnosis

Over the last four decades, a framework for system diagnosis, called model-based diagnosis (MBD), has been developed [42]. In general, MBD is based on comparing system's behavior with some redundancies. As depicted in Fig. 2.2, a domain-independent reasoning engine calculates the diagnoses from the model of faults, model of the system, and the redundancies.

Based on the nature of the system and the available information about it, the system's behavior may be given in the form of partial differential equations (PDEs), state

space equations, fuzzy descriptions, Neural Networks (NNs), look-up tables, if-then rules, input-output transfer functions, or other models. Some of the modeling techniques for power electronic inverters are described in Section 2.3.

Figure 2.2: Perspective of MBD.

The redundancies give more information about the system's behavior. They may be physical redundancies obtained by observations from sensors which are placed in the input, output, or interior points of the system; On the other hand are analytical redundancies which are usually in the form of extra equations that define the system's behavior.

If the predefined behavior of the system, which is described by the system's model, is not consistent with the redundancies, a fault is detected. Knowing the behavior of the faults, the model based engine maps the error to the faults. The reasoning engine can be a rule-based system, a NN, a look-up table, or a fault tree. The feature extraction and fault isolation techniques which have been used for fault diagnosis for power inverters are discussed in Section 2.4 and Section 2.5 respectively.

2.3 Modeling Techniques

"A model is a description of the possible ways a certain system can behave" [43]. Some of the common modeling formalisms are listed bellows [43]:

- Algebraic equations
- Differential equations

- Qualitative differential equations
- Constraints difference equations
- Causal graphs
- Rules
- Logics
- Finite state machines
- Petri nets
- Discrete event models
- Bond graphs

All we expect from the model for the diagnosis purpose, is to decided whether the system's behavior obeys the defined model or not [43]. The model should preferably contains only information about possible faulty components. Extra information about the system details are not only difficult to obtain, but also can sometimes degrade the FDI result. Therefore, we should select the best diagnostic model of the system. It may be different from the system's model used for the control purpose. For example, the inverter's model which is used for control purpose includes snubber capacitance and balance resistors, which both difficult to obtain and inaccurate [44]. Thus we intent to find the simplest model which can describe the system's behavior in healthy and faulty situations.

2.3.1 Logic

Sometimes it is possible to define the system's behavior with a set of logic rules. Although logical models are very precise and consistent, they might not be proper for applications in the engineering domains [43]. It may be difficult or impossible to model a circuit behavior with first-order logic.

2.3.2 Quantitative Modeling

Quantitative modeling is the common modeling method used for FDI in power electronics. It requires precise numerical models of the system which may be given in the form of mathematical equations such as:

- Input/output transfer functions
- Partial differential equations (PDEs)
- State space equations
- Differential-algebraic equations (DAEs)

Circuit simulation models in PSPICE and MATLAB relies on PDEs extracted from circuit Kirchhoff equations. They are originally linear continuous equations. Therefore, are not appropriate for physical systems that contain switching operations, which are non-linear dynamic systems. During switching, the mode of operation may be changed. For example, for a system with n switches, there exist 2^n possible operating modes. Thus, 2^n sets of equations are needed to represent the system. Continuous behavior of the system in that specific mode is describe by each set [45]. For a PWM inverter, the mode of the operation is changed dynamically. Due to unknown mode of operation, it is not possible to use such kind of modeling for diagnosis purpose.

2.3.3 Statistical Modeling

A statistical model is a set of possible observations and their possible probability distributions. The probability of each diagnoses can be predicted using statistical modeling of the system. The conditional probability can be used to determine the failure probability of each component given certain observations and probability of failure of each component. The probability of failure of each component can be achieved from its manufacturer, by observation, or from previous experiences [42]. For example, Fig. 2.3 shows a system with $\mathbf{I} = 5$ inputs and $\mathbf{O} = 2$ outputs, consisting of $\mathbf{C} = 7$ components. The system contains two types of components; adders ($\mathbf{A}_1$, $\mathbf{A}_2$, and $\mathbf{A}_3$), and multipliers ($\mathbf{M}_1$, $\mathbf{M}_2$, $\mathbf{M}_3$, and $\mathbf{M}_4$). The system is modeled by the following matrices:

Figure 2.3: A system with seven components under MBD test.

1. System's model which is described by the connections between components

$$D = \begin{pmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \end{pmatrix}_{I \times (I+C)},$$

that defines the network of the components. If the input of the K^{th} component of the system is connected to the output of another component or a system input, then corresponding value is set to 1.

2. Input values of the system

$$I = [1 \ 2 \ 1 \ 2 \ 1]_I.$$

3. Input–output functionality of each component

$$B = [1 \ 1 \ 1 \ 2 \ 2 \ 2 \ 1]_C,$$

where $B(K) = 1$ indicates that the K^{th} component is a multiplier (**M**), and $B(K) = 2$ represents an adder (**A**). Their functionality is defined in the program.

4. Failure probability of each component

$$\mathbb{P} = [0.01 \quad 0.01 \quad 0.01 \quad 0.01 \quad 0.01 \quad 0.005 \quad 0.005]_{\mathbf{C}},$$

where the probability of failure for each component can be achieved from the historical data or their data-sheets.

5. Observations which are obtained from sensors in the system

$$\mathbb{O} = [\text{NaN} \quad \text{NaN} \quad \text{NaN} \quad \text{NaN} \quad \text{NaN} \quad 10 \quad 6]_{\mathbf{C}},$$

where $\mathbb{O}(K) = \text{'NaN'}$ indicates no sensor is connected to the output of the $\mathbf{K}^{th}$ component.

Given the $\mathbb{P}$, $\mathbb{O}$, and $\mathbf{C}$ matrices the diagnoses can be calculated based on the Bayesian technique as described in Section 2.5.5.

2.3.4 Hybrid Bond Graph

Bond graph was first introduced by Henry Paynter in 1960 for modeling dynamic systems [46]. Bond graph is a graphical modeling tool based on the flow of the energy. The basic elements of bond graph are the junctions and arrows. Junction elements are power-conserving elements. Two junction elements are defined in BG; Bonds that are connected to a **1**-junction has the same flow and the summation of the efforts of all bond connecting to the same **1**-junction is zero. It is dual to a loop in the electrical circuit in the electrical domain and the Kirchhoff's Voltage Law. On the other hand, the bonds that are connected to a **0**-junction have the same effort and the summation their flows is zero. It is dual to a node in the electrical circuit in the electrical domain and the Kirchhoff's current Law [47]. Table 2.2 shows the effort and flow in the common energy domains.

Energy Domain	Effort (e)	Flow (f)
Electrical	Electromotive force	Current
Mechanical	Translation force	Linear velocity
Mechanical	Rotation torque	Angular velocity
Magnetic	Magneto-motive force	Flux rate
Hydraulic	Pressure	Volumetric flow rate
Thermal	Temperature	Entropy flow rate

Table 2.2: The effort and flow in the common energy domains [16].

In 1998 hybrid bond graph (HBG) was introduced to model physical dynamic systems with discontinuities. Unlike the BG which was only for the continuous systems, HBG has a switching junction which allows using the energy based model of BG for hybrid systems which has discontinuities [48]. A control junction, indicating by "c" determines if the junction is controlled by an external signal. Hence, a switch can be modeled as a control junction. With the use of switched power junctions all feasible modes of the system are shown at the same time on one graph [45]. The arrows of the bonds show the direction of the flow. Causal strokes indicate whether a specific power variable is the cause or the effect [45] in the causal bond graph.

A unified graphical method of modelling dc-dc converters using bond graphs has been presented in [47] and a few examples were given. This method is applicable to switching mode power converters, in both continuous and discontinuous conduction modes. We have modeled a single-phase HB inverter with HBG as illustrates in Fig. 2.4. Each parallel branch in an electrical circuit is mapped to a **0**-junction, and each serial branch is mapped to a **1**-junction.

HBG is a useful modeling tool for multi-domain problems. It can model complicated systems which are a combination of mechanical, electrical, magnetic, hydraulic, and thermal systems. However, as it can be seen in Fig. 2.4, R_{on} and R_{off} which are internal resistances of switches in close and open states are required to build the HBG model. Thus, if the switch type changes, the model would be affected. also, the accuracy of the model is affected by the tolerance of the components. The other problem of using HBG models of diagnosis purpose is that the exact model of the

The HBG model becomes very complicated for inverters with large number of switches. Because each control junction (switch) introduces a binary parameter in the model, and the combination of all switch states compose several modes of operation. For diagnosis purpose, the mode of the operation need to be estimated by a mode tracker witch brings more complexity for the systems with unknown mode changes.

2.4 Feature Extraction Techniques

Feature extraction techniques are used to determine the fault signatures from the observations. Selecting a proper feature can facilitate the diagnosis step and increase the accuracy and speed of it. Different features of a given signal can be selected for the diagnostic purpose. However, for a robust FDI result, the selected feature should be a function of the fault and independent to the rest of parameters in the system.

When the fault parameter is known, the value of that specific parameter can be assumed as the feature of the fault. Parameter estimation methods, described in Section 2.4.1, can directly extract the fault value by estimating the parameter of the fault. In some cases, one or more features of the monitored signal contain the information about a fault. Thus, signal processing methods are applied to extract those specific features either in time domain (Section 2.4.2), frequency domain (Section 2.4.3), or time-frequency domains (Section 2.4.4 and Section 2.4.5). In case of three-phase power electronic systems, all of the three phases can contain the information about the faulty components. In order to reduce the feature domain size coordinate transformations such as Park's vector and Concordia have been widely used to convert the 3D current space into 2D space (Section 2.4.7). After the coordinate transformation is done, a proper pattern recognition method can be applied to extract the fault's features of from the transformed pattern in a 2D space [49]. Section 2.4.6 discussed the space vector analysis method which has been used to achieve time-independent features form sinusoidal waveforms.

2.4.1 Parameter Estimation

Some of the parameters of the system's model can be affected by a specific fault. Parameter estimation methods are used to determine those parameters in the form of solving optimization problems. Least square error (LSE) is one of the optimization methods which has been applied in [5] and [50] for diagnosis faults using HBG. This estimation technique is based in global analytical redundancy relations (GARRs), as a set of equations that describe the hybrid system. Equation (2.1) shows the GARRs of the inverter system of Fig. 2.4,

$$\text{GARRs} = \begin{cases} \text{GARR}_1 = D_e - V_1 + D_{f1}(g_1 R_{on1} + (1 - g_1) R_{off1}) \\ \text{GARR}_2 = D_e + V_2 + D_{f2}(g_2 R_{on2} + (1 - g_2) R_{off2}) \end{cases} \quad (2.1)$$

In (2.1), D_e is the effort detector that measures the load voltage. The gate control signals are shown by g_1 and g_2 . The dc voltage sources are determined by V_1 and V_2 .

The load voltage can also be calculated based on the observations from the other two detectors D_{f1} and D_{f2} as shown in (2.2).

$$D_e = L \frac{d(D_{f1} + D_{f2})}{dt} + R_L(D_{f1} + D_{f2}), \quad (2.2)$$

where L is the load inductance and R_L is the load resistance. In this example, it is assumed that both switches have similar internal resistances, i.e.,

$$R_{on1} = R_{on2} = R_{on}$$

and

$$R_{off1} = R_{off2} = R_{off}.$$

In the healthy situation,

$$GARR_1 = GARR_2 = 0, \quad (2.3)$$

however, if a fault exists in the system, (2.3) is not valid anymore and the fault can be identified by minimizing the error function of (2.4),

$$Error^2 = GARR_1^2 + GARR_2^2. \quad (2.4)$$

The isolability and detectability of this method are discussed in [5]. If the number of detectors is less than the number of unknown parameters, a pseudo inverse matrix must be used to solve the problem. In this case, the LSE solution will be obtained. However, the LSE is not always the best solution for an FDI problem. For example, when several types of components parameters in a circuit are being estimated, the acceptable diagnostic error for a special expensive component, must be very small comparing to the regular components. LSE can also lead to multiple solutions. Choosing the initial value for solving the LSE problem as an iterative method is also an important problem which may cause long convergence time [5].

The method proposed in [50], gives all the GARRs equal weights in the error function, which can cause inaccuracy in parameter estimation for power electronic circuits. The parameters of an electronic circuit may differ in values for more than three orders of magnitude. For example, a resistor may be in the range $K\Omega$ while an inductor

value is of the order of μH . Therefore, when applying the LSE for minimizing the error function, the effect of the inductor might be neglected [5]. Thus, some kinds of normalizations are necessary to improve this method. However, for the hybrid systems such as inverters, it is not possible to do normalization without knowing the operating mode of the system.

2.4.2 Time Domain Analysis

In this analyzing method, the values of measured parameters are compared to some references in the time domain. Comparison of the ac voltage and its PWM reference in the time domain is reported in [51] to detect open-circuit damage in voltage-fed PWM motor drive system. The resulting fault detection is quite fast (one-fourth of a period). However, it requires access to the PWM control unit, since the reference signal cannot be defined as a fixed function. For the inverter as a time-variant dynamic system, the PWM reference signal is not constant and can be changed by the load variations or the feedback loop. It is more common to use the features from current waveform rather than voltage in for FDI for power electronic systems, because unlike the voltage switching waveform, the current (in healthy condition) is sinusoidal and it is possible to use its time-invariant features.

In [52], the polarity and value of the dc offset of the phase current were used as the FDI feature and a fault detection time equal to five cycles was reported. The average value of the current was also reported as a fault detection feature but without the isolation capability [34]. In [53] the switch open-circuit faults were detected based on near-zero value of output current and the ratio of the average phase current, and the average magnitude thereof was used for fault isolation. For extracting fault's features based on the current waveform, at least one cycle of the current waveform is required and it leads to a quite long fault detection time [34] .

In [54], the entropy of the current signals and the magnitude of phase voltages after filter were used as switches fault's features. Entropy can capture the faulty behavior of the inverter in the form of an unstructured signal [54]. However, because different faults may have equal entropy value in the current waveform, the faults may not be

isolable and more measurement points are needed to achieve isolability. Moreover, the current waveforms will change if the fault occurrence time or if load parameter changes, so the FDI result is not robust.

2.4.3 Frequency Analysis

Frequency analysis is a common technique for analyzing periodic signals. Fast Fourier transform (FFT) is used to extract frequency contents of the monitored signal. It is assumed that each fault will lead to a specific sideband frequency [55] or will change the magnitude of some specific harmonics [3], [56]. Therefore, by mapping the frequency changes to the faults, the diagnosis step is conducted. Frequency analysis has been widely used to diagnose motor faults by monitoring current signals. For example, Fig. 2.5 shows the normalized line-current spectra for healthy and short-circuited turn faults in a motor [6].

Feature extraction based on frequency analysis has some limitations. Not all the faults change the frequency spectrum of the measured signal uniquely. For example, two switches may have the same sideband frequencies. Moreover, this method can only extract features from a periodic signals. At least one period of the measured signal is required to extract the frequency contents. Thus, the fault detection time is at least one cycles. For example, for a 50 Hz inverter, the fault detection time is more than 20 ms.

Although the feature is independent to the time, it is dependent to the frequency. If the carrier frequency of the PWM waveform, or the output frequency of the current change by feedback loop or operating conditions, the features also change. FFT is also computationally expensive. This method is also based on the superposition assumption; each signal can be decomposed as summation of sinusoidal signals with different amplitudes and phases. For non-sinusoidal signals, the frequency spectrum is continuous and for limited signals, the frequency spectrum is unlimited. Thus, FFT is not proper for analyzing the signals with sharp edges like PWM signal. Because the pulse-shaped signals have a continuous and unlimited frequency spectrum. Therefore, it is difficult to extract accurate features from the frequency spectrum.

(a) Normalised line-current spectra of a motor for healthy condition [6].

(b) Normalised line-current spectra for a motor with short-circuit turn fault [6].

Figure 2.5: Normalized line-current spectra of a motor for healthy and faulty situations [6].

2.4.4 Short Fourier Transformation

FFT is based on the assumption of signal periodicity. For non-stationary signals where the frequency contents vary in time, the FFT cannot detect the frequency changes in time. Short Fourier transform analyses a window of the signal and assume the rest of signal is periodic. By moving this window over time, the frequency contents of the signal for different time slots are achieved. According to the Heisenberg-Gabor uncertainty principle, because the time-frequency resolution is constant, determining

the windows length is a problem in this method. An accurate time resolution needs a short window; On the other hand, an accurate frequency resolution needs a long window. However, in the context of diagnosis, this long analysis window introduces extra detection delays [57].

2.4.5 Wavelet Analysis

Real life signals are not periodic. They start at one point in time and end in another time. Sinusoidal signal is not always the best choice for decomposing a given signal. To overcome the limitations of the FFT, the wavelet theory was introduced. The origin of the wavelet is based on the Haar sequence proposed in 1909 by Alfrd Haar. In wavelet theory, any signal can be decomposed as summation of wavelets with different amplitude and scales. The wavelet is an arbitrary non-stationary signal which is selected based on the nature of the original signal. Thus, it is proper for analysing non-periodic non-stationary signals.

The square shape of the Haar wavelet is make it appropriate for analysis of signals that have sudden changes, such as signals obtained from tool failures [58]. In addition to that, the assumption of the stationarity of the signal is not required in the Wavelet transformation. Thus, it is suitable to analyze signals that change over the time [57]. Normalized wavelet coefficients of the phase currents were used in [59] as fault's features. In [60], the wavelet transform was applied to extract switch open-circuit fault's features from one cycle of the dc-link current. Discrete wavelet components of normalized current waveforms are used in [61] and [62] as features for switch open-circuit faults in a three-phase VSI.

2.4.6 Space Vector Analysis

The space-vector theory has been developed for analyzing transients occurring in electrical machines. In the space vector theory a three-phase quantity is represented by a single space vector rotating in the complex plane as shown in Fig. 2.6. In this figure, $\theta_{\varphi t}$ represents phase φ vector at moment of observation t . The amplitude of

vectors $\theta_{A1}, \theta_{B1}, \theta_{C1}$ are equal to the instantaneous values of i_A, i_B, i_C at observation moment $t = 1$, and the phases of $\theta_{A1}, \theta_{B1}, \theta_{C1}$ are equal to $0^\circ, 120^\circ, 240^\circ$ respectively.

Figure 2.6: The space vector representation of three phase currents [7].

For a healthy balanced three-phase quantity, the frequency and amplitude of the space vector is constant. Using the angle and the instantaneous frequency of the space vector, short-circuit fault in the converter diodes can be detected [11]. The complex state vector is a powerful tool in the analysis of ac machines [63]. In [8] and [9], the open-circuit faults in a three-phase VSI are detected using the trajectory of the current space vector. For a fault-free VSI, the current trajectory has a circular pattern as illustrated in Fig. 2.7. The open transistor fault will change the circle pattern into a semicircle (Fig. 2.8). In [8], the circle of the mass of the current space vector

Figure 2.7: Trajectory of current space vector in the no-fault situation [8].

Figure 2.8: Current space patterns for an open-circuit fault in Q_1 to Q_6 of a three-phase VSI [8].

patter is extracted as the fault's feature. As shown in Fig. 2.9 at least one period of the current signal is required to extract the patterns and the features. This causes at least one cycle delay in the FDI procedure.

Figure 2.9: Experimental output currents and space vector pattern for an open-circuit fault in Q_3 [9].

2.4.7 Coordinate Transformation

Coordinate transformation methods, such as Park, Clark, and Concordia transform, are usually used in three-phase induction motors for describing the three-phase currents in a two-dimensional plane. Equation 2.5 shows how to transform the three phase currents , i_A , i_B , and i_C , to i_D , and i_Q [10], [15],

$$\begin{bmatrix} i_D \\ i_Q \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_C \\ i_B \\ i_A \end{bmatrix}. \quad (2.5)$$

Looking to the data points in a non-time dependent frame can make the interpretation of faults easier [15]. A healthy three-phase inverter is determined by a circle in the DQ frame. A fault in the inverter can be shown by a distortion in the circle. Pattern recognition techniques reduce the computational complexity [10]. Fig. 2.10 shows the Concordia patterns for an open-circuit fault in a three-phase VSI relating to a particular switch (Q_1 to Q_6).

Figure 2.10: The Concordia patterns for an open-circuit fault in a three-phase VSI in Q_1 to Q_6 [10].

Current Park's vector pattern were used in [64] to detect open phase and stator voltage unbalance faults. The properties of the trajectories of the mean DQ current vector such as magnitude and phase have been also used by [65], [64], and [44] to address switch faults in three-phase VSIs.

In [11], the angle transitions of the current space vector have been used as open diode fault's features in a three-phase rectifier. Figure 2.11 illustrates the $\mathbb{DQ}$ pattern of the current which has the characteristic form of a normal hexagon. The angle starts from 30° and decreases up to 330° with steps of 60° during commutation [11]. In every vertex only two diodes are conducting. During the open diode faults, the vertices of the faulty switch will be omitted and the hexagon will be changed to a trapezoidal shape [11]. Thus, by tracking the hexagon position, the faulty diode will be isolated.

Figure 2.11: Current space vector locus in the no-fault operation [11].

Figure 2.12 compares the Park's vector patterns for various frequencies from simulations and experiment [12]. When the frequency decreases from 50 Hz to 10 Hz, the trajectory is stretched and shifted. The major drawback of these methods is being load dependent and frequency dependent. Hence, its performance in the closed loop, where the frequency is changing by the feedback, will not be effective.

In 1998 a geometric modeling for m -leg inverters were proposed [66] to overcome the limitations of $\mathbb{DQ}$ transformation for m -leg inverters. The trajectory matrices were derived to illustrate a 4-phase inverter in a 2-dimensional plane. However, it has not yet been used for FDI purpose.

Figure 2.12: Ac currents of the inverter in Park's Vector frame for various frequencies; 10 Hz (top), 20 Hz, 25 Hz, 30 Hz, 40 Hz, 50 Hz (bottom) [12].

2.5 FDI Techniques

FDI techniques aim to map the features to the faults. Regardless to the feature extraction technique, different methods can be used for FDI. In this section, the FDI techniques which have been applied for VSIs in the literature are described.

2.5.1 Limit Checking

Limit checking is one of the preliminary methods used for fault detection. In this method, the amplitude of the output signal is compared with some thresholds. If the minimum or maximum of the signal exceed the predefined threshold, a fault is detected. Sometimes the trend of the signal (derivative) is also compared with some thresholds. For example, the fault detection method proposed in [13] for a cascade MLIs is based on limit checking method. As illustrated in Fig. 2.13, the rms value of sinusoidal voltage, $\hat{E}_{out}$ is compared to a threshold voltage E' . If the output voltage fall bellow the predefined threshold value, E' , a short-circuit fault is detected. In this method, the fault detection time is around one cycle of the reference signal (50 Hz output) which is around 20 ms. Moreover, the exact faulty switch was not isolated and only the faulty module was located.

Figure 2.13: STATCOM filtered output voltage and threshold value [13].

Setting a proper threshold value is a challenge in the limit checking methods. Especially when dealing with dynamic systems, the threshold is not constant and in some cases it is not possible to define it accurately. Moreover, some of the faults do not change the minimum or maximum of the signal, or different faults affect the signal amplitude identically. Therefore, it is not possible to differentiate between the faults.

2.5.2 Rule Based Expert Systems

Given faults and symptoms in all possible fault scenarios, a case based reasoning (CBR) engine maps the observed symptoms to the faults. Usually, a database memorizes the fault conditions. For example, Table 2.3 illustrates the features to faults relationships in the HB VSI of Fig. 2.4. This table is extracted based on the fact that the state of the two switches in an inverter leg are complementary. Figure 2.14 depicts the overall procedure of the FDI applied to the HB inverter, and the simulation results are shown in Fig. 2.15. A short-circuit fault is inserted in the Q_1 by closing fault insertion switch at $t=0.06s$. The load current is depicted in Fig. 2.15d. Figures 2.15a and 2.15b illustrate parameter values of Q_1 and Q_2 , $\hat{g}_1$, and $\hat{g}_2$ respectively which are estimated from the system equations (see 2.4.1). After the short-circuit fault has occurred, $\hat{g}_1$ is stick to 1, which means that a short-circuit fault has occurred in Q_1 .

Table 2.3: Diagnostic table [5]

$\hat{g}_1$	$\hat{g}_2$	Diagnosis
0	0	open-circuit fault
0	1	No fault
1	1	short-circuit fault
1	0	No fault

Figure 2.14: The procedure of model-based FDI applied to the inverter [5].

2.5.3 Fuzzy Logic

When the number of the system components or the features of the faults increase, the database becomes very large. Rule-based expert systems can reduce the database size by defining a rule to map a category of faults to the symptoms. Logic rules as well as fuzzy rules can be defined for fault conditions. The human knowledge and skill can be defined as qualitative rules in fuzzy systems.

The rule-based method needs complete knowledge about the system to build a reliable database. They have no learning capabilities, thus, it often has difficulties in dealing with novel faults [67]. In real applications, the fault conditions may deviate from the defined rule-based database leading to false diagnosis. Fuzzy systems can solve this problem to some extent [60], however, membership functions if not defined properly, can increase the false diagnoses.

2.5.4 Neural Network (NN)

When the feature-to-fault relations are complicated and cannot be achieved by a few linear equations, a NN can be designed to capture these non-linear relationships. The NN is trained based on the available feature-to-fault information. NNs have been

Figure 2.15: Diagnosis of a short-circuit fault in Q_1 of the single-phase HB inverter [5].

applied for three-phase VSI to detect and isolate multiple open-circuit and short-circuit faults [67], [54].

To train a NN, several runs of the system under faulty and healthy conditions are needed. Naturally, the faults can occur at anytime instance, and it is not feasible to train the NN for all fault scenarios for all possible fault occurrence times. Also, for any new fault scenario that did not happened before, the system needs to be retrained. For example, if the inverter's load or the dc input voltage change, the data driven based FDI system needs to be trained again. The accuracy of NNs depends to the accuracy of the data which was used in the training step [44].

2.5.5 Bayesian Networks

The Bayesian FDI aims to find the probability of each diagnosis given the system's model and the failure probability of each component. We investigated Bayesian FDI approach to construct an algorithm for finding the probability of diagnoses of the system illustrated in Fig. 2.3 [14]. This algorithm resulted in the probability value of each possible diagnosis. Multiple dependent and independent faults were considered. The most probable diagnoses are shown in Fig. 2.16.

M1	M2	M3	A1	A2	A3	M4	Probability
ok	ok	ok	ok	ok	ok	broken	0.8768
ok	broken	ok	broken	ok	ok	ok	0.0178
ok	broken	ok	ok	broken	ok	ok	0.0178
ok	ok	ok	broken	broken	ok	ok	0.0178
broken	ok	ok	ok	ok	ok	broken	0.0089
ok	broken	ok	ok	ok	ok	broken	0.0089
ok	ok	broken	ok	ok	ok	broken	0.0089
ok	ok	ok	broken	ok	ok	broken	0.0089
ok	ok	ok	ok	broken	ok	broken	0.0089
ok	broken	ok	ok	ok	broken	ok	0.0089
ok	ok	ok	ok	broken	broken	ok	0.0089
ok	ok	ok	ok	ok	broken	broken	0.0044

Figure 2.16: Diagnoses calculated by the Bayesian algorithm [14].

Bayesian Networks with learning capability are reported in [68]. They learn knowledge dynamically from previous sample, which made the diagnosis system be self-adaptive [69]. Bayesian Network is proper to diagnose systematically repeating failing mechanisms [70]. However, the diagnoses are not deterministic and it is always based on the probabilities. In most cases a no-fault scenario can have the most probable diagnosis, or several diagnosis with the same probability [4]. The Bayesian approach has some limitations which make it inappropriate for FDI for power electronic inverters:

1. The prior probabilities of failures of each component is needed as an input of the MBD reasoning engine.

2. When the number of components increases, more observation points are needed to achieve an accurate diagnosis. This method can propose more measurement points to increase the diagnosis accuracy. However, it needs more sensors and detectors.
3. Switching converters are dynamic systems in which the structure of the system changes with time. Thus, the probabilities of the diagnoses change with time and it is not possible to judge the system health based on the probabilities of the diagnoses without knowing the operating mode of the system.
4. Power electronic inverters consist of several identical switches with the same probability of failure. Thus, the statistical methods result in similar diagnoses probability for all switches. To isolate the faulty switch, more observation points need to be added to the system. This requires high number of detectors and higher implementation cost.

2.5.6 Qualitative Bond Graph

In Section 2.3.4 the HBG was described as a modeling method. The causal assignments in the bond graph model can be used for fault diagnosis purpose. Thus, a temporal causal graph (TCG) can be obtained from the bond graph model. The procedure contains assigning causal path and tracing them. The TCG and Qualitative based FDI is described in details in [71] and [72]. Hypotheses of the faults are generated with the TCG and the existing error between measurements and the model. In this model, deviations from normal behavior are in a qualitative form, i.e., -, +, 0 for below, above, and within normal range respectively. By mapping the measurements onto the TCG and propagating backward, the fault hypotheses are formed [73].

Qualitative FDI methods do not require precise numerical models [73] and therefore, they are more robust to the noise and modeling errors. However, they cannot determine the fault magnitude accurately.

FDI method	Complexity	Accuracy	Robustness	Speed
Limit checking	Simple	Good	Poor	Good
Rule Based	Moderate	Good	Poor	Moderate
NNs	Complex	Moderate	Good	Low
Bayesian Networks	Complex	Moderate	Good	Low
QHBG	Moderate	Poor	Good	Moderate

Table 2.5: Comparison of FDI methods.

2.6 Comparison of the FDI Approaches

Different combinations of feature extraction methods and FDI methods have been applied to the power electronic inverters. Table 2.4 compares the complexity, speed, and implementation effort of the feature extraction methods. A technique with low computational complexity, high speed, and low implementation effort is desired. It is ideal to extract the features by time domain analysis, because it is fast and has low computational and implementation costs. However, if the feature does not show up in the time domain, a transformation or analysis in the other domains is inevitable.

Feature extraction method	Complexity	Speed	Implementation effort
Parameter estimation	High	Fast	Moderate
Time domain analysis	Low	Fast	Low
Frequency analysis	High	Slow	High
Short Fourier transform	High	slow	High
Wavelet analysis	High	slow	High
Space vector analysis	Low	Moderate	Low
Coordinate Transformation	Moderate	Moderate	Low

Table 2.4: Comparison of feature extraction methods.

Table 2.5 compares the complexity, accuracy, robustness, and speed of FDI methods. The speed of a FDI system is particularly important for FTC purpose. The faults in electronic devices can propagate very fast and can lead to catastrophic failures within a few microseconds. Table 2.6 compares fault diagnosis approaches which have been used in the literature for isolating faulty switches in VSIs. These FDI methods necessitate monitoring either phase currents, e.g., [28], [74], [67], [75], [76], [77],

[78], [79], [80], [81], [75], phase voltages, e.g., [28], [67], [32], [13], [5], switch gate voltage, e.g., [74], [82], motor torque, e.g., [67], or a combination of these signals [83]. Open-circuit FDI methods for other types of converters such as dc-dc converters are reported in [49], [84], [51], [85]. Although placing more detectors can make the FDI algorithm simpler, it adds extra cost and weight to the system. Moreover, it can involve new reliability problems related to the sensors and detector health issues.

In [77], rms value of the wavelet packet decomposition coefficients and the 2nd harmonic of dc side current were used to diagnose the switch faults with a look up table. Delpha [76] utilised phase and amplitude of the Concordia current vector. Fault detection time is about one reference frequency in the current-based FDI methods. In [86] open-circuit faults were diagnosed using offset polarity of dc current in more than 3s. In [67] Max, Min, Median, Mean, Standard deviation, and dc component of the power spectrum of phase current, phase voltage, and motor torque were measured and a NN were trained to diagnose the faults in a approximately 20ms. Gilreath [10] utilised Centroid of the current pattern in $\alpha - \beta$ plane and case-based reasoning to isolate the open-circuit faults. In [9], 2.2ms diagnosis time was reported using average absolute values of the three normalised phase currents.

Most of the existing FDI methods analyze sinusoidal output of the inverter. Usually, a few cycles of the inverter sinusoidal output are required for the fault detection purpose. It makes the fault detection time in the order of one period of the main sinusoidal waveform (20 ms), e.g., in [75] and [13]. Modern IGBTs (or MOSFETs) can tolerate current values between 2 – 10 times the nominal current [28]. However, the switch may be destroyed due to the temperature rise induced by the extremely high instantaneous power dissipated in the switch [28]. Therefore, it is ideal to detect a short-circuit fault within one switching period to prevent short-circuit failures caused by two closed serial switches in one phase leg.

CHAPTER 2. LITERATURE REVIEW

FDI time	Fault Type	Fault Feature	Requirements	Feature Extraction Method	Fault Diagnosis Method	Comments
> 3s [86]	Open circuit fault	Offset polarity of dc current	-Phase current	dc filtering and limit checking	Expert system (Look-up-table)	-Needs threshold setting. -Detection time depends on the parameters of the low pass filter. -Assumption of balance phase voltages -Assumption of magnetic linearity Assumption of infinite inertia of rotor.
< 20ms [67]	Open circuit and short circuit faults	Max, Min, Median, Mean, Standard deviation, and dc component of the power spectrum of V, I, and T	-Phase current, -Phase voltage, -Motor torque	Neural networks	Limit checking and rule-based reasoning	-Training -Threshold setting
< 20ms [10]	Open circuit faults	Centroid of the current pattern in $\alpha \beta$ plane	Phase current	Concordia Transform	Limit checking and case-based reasoning	-Cannot isolate short-circuit faults -Load dependent -Frequency dependent
$\approx$ 20ms [13]	short circuit faults	RMS value of all phase filtered Voltages	Three phase Voltage	Filtering and RMS calculating	Limit checking and minimization	-Only can isolate the faulty cell not the faulty switch -Threshold setting
< 20ms [75]	short circuit faults	2^{nd} and e^{rd} harmonic oscillations of phase currents	Three phase current	Filtering ringing frequency	Look-up table	-Fault isolation is dependent to the circuit parameters and need further works -When the number of switches increase, the fault diagnosis become complicated. -The switch faults may not be isolable.
$\approx$ 20ms [54]	Open circuit and short circuit faults	Polarity of phase voltage and entropy of phase Voltage and current	Three phase current, and voltage	Entropy calculation	Neural networks	-Training -Dependent to fault occurrence time -Computational Complexity -Load dependent
$\approx$ 2.2ms [9]	Open circuit faults	Average absolute values of the three normalised phase currents	Three phase current	Coordinate transform	Look-up table	-Threshold setting -Load dependant
$\approx$ 85 μ s [87]	Open circuit faults	Average absolute values of the three normalized phase currents	Three phase voltages -Switch control Signals	Coordinate transform	Parameter estimation	-Requires access to the -Gate control signals -Not scalable to circuit with high number of switches

Table 2.6: Comparison of FDI time of different approaches for three-phase VSIs.

The methods which are based on analysis of the current signal, e.g. [28], [76], [77], [80], [78], are load dependent. Thus, changing the load can increase the false alarm rate of the diagnostic system. In many situations, the load is not constant and can be changed by user or by environment conditions during the operation. In the real applications such as wind turbines [81], the mechanic load changes randomly which affects the current waveforms. Thus, the current based FDI methods are sensitive to the operating condition and can lead to false alarms while the load changes. Moreover, the fault detection time depends on the time constant of the load [56].

Although the sinusoidal signal is easier than the PWM switching signal to be analyzed, it has some disadvantages for FDI purpose. Filtering the switching signal can eliminate some useful information about switch faults. It can also make some delays. Moreover, the faults can be mistaken by fluctuations of the load or filter parameters. Use of switching signals for detecting IGBT faults in a three-phase VSI is reported in [26], [87], [88], [83]. Karimi [87] has reported a $85\mu s$ detection time and [88] achieved a 0.91ms detection time. In [87], the diagnosis is conducted by comparing the gate control signals to the phase voltage signals. Thus, they require two sensors for each switches. This method is not proper for circuits with high number of switches such as MLI.

2.7 Summary

In this chapter, several FDI methods were reviewed. The most common modeling, feature extraction, and fault isolation methods were studied. The FDI techniques which have been applied to the VSIs to diagnose short-circuit and open-circuit faults were compared. In the next chapter, a FDI method based on the VSPs is presented. With the proposed method, a very fast FDI result can be achieved by analyzing PWM switching waveforms in the voltage space.

Chapter 3

VSP-based FDI for short-circuit faults

3.1 Introduction

In this chapter, the VSP-based FDI (Voltage Space Pattern based Fault Detection and Isolation) method is described. This method is developed to diagnose short-circuit switch faults in the VSIs (Voltage Source Inverters). The pole voltages of each phase of the inverter are monitored and illustrated in the voltage space. The voltage space patterns (VSPs) are then used to isolate the faulty switch. The model of the inverter in the healthy and faulty situations is used to determine the fault signatures. The VSP-based FDI is validated through simulations and experiments for diagnosis of short-circuit faults in a three-phase VSI with six switches.

The theory of VSP-based FDI is described in Section 3.2. The properties of VSP for the SPWM inverters are discussed in Section 3.3. Section 3.4 describes the FDI procedure based on the state transition patterns in the voltage space. The simulation results are illustrated in Section 3.5. The application of VSP-based FDI for diagnosis of short-circuit switch faults for an inverter in a motor drive system is presented in this chapter. Section 3.6 describes the experimental set-up which was designed to validate the VSP-based FDI. The experimental results for diagnosis of short-circuit switch faults in a six-switch inverter are shown in Section 3.7. Section 3.8 proposes some modifications to reduce the diagnosis time. The experimental results from the modified approach are depicted in Section 3.8.1. This chapter is concluded in Section 3.9.

3.2 Theory of VSP-based FDI

In this section, the theory of the VSP-based FDI and its basic concepts are described. This method is based on input–output model of the inverter. Section 3.2.1 describes the modeling of the VSI. Section 3.2.2 defines switching states based on the inverter's model. In Section 3.2.3 and Section 3.2.4, the state transitions in the voltage space are introduced. Section 3.2.5 introduces the fault-banned zones for short-circuit faults that are used as fault signatures in the voltage space.

3.2.1 Modeling the VSI

This section describes a structural model for the three-phase VSI. Fig. 3.1 illustrates a VSI circuit with six identical switches, Q_i for $i = 1$ to 6. Gate control signals g_i control on–off state of Q_i ; for $g_i = 1$, Q_i is in the on state and the switch conducts. On the other hand, when $g_i = 0$, Q_i is in the off state, and it does not conduct.

Figure 3.1: A Three-phase inverter.

Gate signals of two switches of one phase leg are complementary; for example, if $g_1 = 1$ then $g_2 = 0$ and Q_1 is closed, resulting in $v_A = +E_N$; conversely, if $g_1 = 0$ then $g_2 = 1$ and Q_2 is closed, resulting in $v_A = -E_N$, where E_N is a constant value proportional to the voltage of the dc source. Hence, the output voltage of each phase alternates regularly between two levels of voltage that forms a square wave. A control block determines the pulsewidth of the waveform.

Assume R_u is the internal resistance of an upper switch of a phase leg, e.g., Q_1 for $\varphi = A$, and R_l is the internal resistance of the lower switch of that phase leg, i.e. Q_2 in

this example. From the circuit equations,

$$v_\varphi = \frac{E}{2} \cdot \frac{R_l - R_u}{R_l + R_u} = \frac{E}{2} \cdot \frac{1 - \frac{R_u}{R_l}}{1 + \frac{R_u}{R_l}} \quad (3.1)$$

Let R_{on} , and R_{off} be the internal resistances of a healthy switch in the on and off states, and

$$\rho_0 := \frac{R_{\text{on}}}{R_{\text{off}}}. \quad (3.2)$$

The internal resistance of a switch R_i is equal to R_{on} , when $g_i = 1$; conversely, $R_i = R_{\text{off}}$ when $g_i = 0$, therefore,

$$\frac{R_u}{R_l} = \begin{cases} \rho_0, & \text{if } g_u = 1 \text{ and } g_l = 0, \\ \frac{1}{\rho_0}, & \text{if } g_u = 0 \text{ and } g_l = 1. \end{cases} \quad (3.3)$$

Replacing $\frac{R_u}{R_l}$ from (3.3) in (3.1)

$$v_\varphi = \begin{cases} \frac{E}{2} \varepsilon_0, & g_u = 1 \text{ and } g_l = 0 \\ -\frac{E}{2} \varepsilon_0, & g_u = 0 \text{ and } g_l = 1 \end{cases} \quad (3.4)$$

where

$$\varepsilon_0 := \frac{1 - \rho_0}{1 + \rho_0}. \quad (3.5)$$

For a healthy switch,

$$R_{\text{on}} \ll R_{\text{off}}; \quad (3.6)$$

thus,

$$\rho_0 \approx 0, \quad (3.7)$$

and

$$\varepsilon_0 \approx 1. \quad (3.8)$$

Let

$$E_N = \frac{E}{2} \varepsilon_0 \quad (3.9)$$

be the absolute value of the phase voltage for the inverter in the no-fault condition.

Thus,

$$\mathbf{v}(t) := \mathbf{e} \cdot \mathbf{D}(t) \quad (3.10)$$

where

$$\mathbf{v}(t) = [v_C(t) \quad v_B(t) \quad v_A(t)], \quad (3.11)$$

$$\mathbf{e} = [E_N \quad -E_N], \quad (3.12)$$

and

$$\mathbf{D}(t) := \begin{bmatrix} d_1(t) & d_3(t) & d_5(t) \\ d_2(t) & d_4(t) & d_6(t) \end{bmatrix} \quad (3.13)$$

is a binary matrix representing the dynamic model of the inverter

$$d_i(t) := \begin{cases} 1 & \text{if } Q_i \text{ is on at time } t, \\ 0 & \text{if } Q_i \text{ is off at time } t. \end{cases} \quad (3.14)$$

3.2.2 Switching States

Each switch has two states, on or off. Therefore, for six independent switches, 2^6 states can be defined. The gate control signals are generated from the PWM signals, p_ϕ , based on (3.15)–(3.20). Thus, only 2^3 states belongs to the no-fault conditions where only one switch per phase leg is on, i.e.,

$$g_1(t) := p_A(t), \quad (3.15)$$

$$g_2(t) := 1 - p_A(t), \quad (3.16)$$

$$g_3(t) := p_B(t), \quad (3.17)$$

$$g_4(t) := 1 - p_B(t), \quad (3.18)$$

$$g_5(t) := p_C(t), \quad (3.19)$$

$$g_6(t) := 1 - p_C(t). \quad (3.20)$$

Table 3.1 shows $\mathbf{D}_s$ for all no-fault switching states, s . Each switching mode results in a set of pole voltages that can be calculated by (3.10).

Table 3.1: Switching states and output phase voltages.

s	$\mathbf{D}_s$	$\mathbf{v}_s$
0	$\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	$[-E_N \quad -E_N \quad -E_N]$
1	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$	$[-E_N \quad -E_N \quad E_N]$
2	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$[-E_N \quad E_N \quad -E_N]$
3	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$[-E_N \quad E_N \quad E_N]$
4	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$[E_N \quad -E_N \quad -E_N]$
5	$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$[E_N \quad -E_N \quad E_N]$
6	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$[E_N \quad E_N \quad -E_N]$
7	$\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}$	$[E_N \quad E_N \quad E_N]$

The switching state of the inverter at a given time t is

$$s(t) := \mathbf{u} \cdot \mathbf{b}, \quad (3.21)$$

where

$$\mathbf{b} := [4 \quad 2 \quad 1]^T, \quad (3.22)$$

and

$$\mathbf{u} := [1 \quad 0] \cdot \mathbf{D}(t). \quad (3.23)$$

In the other word, s is the decimal value of the first row of $\mathbf{D}$. By this definition, (3.21) assigns a unique number for each switching state of the inverter. Proposition 3.2.1 proofs this fact.

Proposition 3.2.1. *Let $\mathbb{D} = \{\mathbf{D}_s : \forall s \in \mathbb{S}\}$, be the set of all no-fault switching combinations and $\mathbb{S}$ be the set of no-fault states*

$$\mathbb{S} = \{0, 1, \dots, 7\}. \quad (3.24)$$

For every $\iota, \kappa \in \mathbb{S}$ and $\iota \neq \kappa$, $\mathbf{D}_\iota \neq \mathbf{D}_\kappa$.

Proof. From (3.13), (3.14), and 3.15)–(3.20),

$$\mathbf{D}(t) = \begin{bmatrix} p_C(t) & p_B(t) & p_A(t) \\ 1 - p_C(t) & 1 - p_B(t) & 1 - p_A(t) \end{bmatrix}, \quad (3.25)$$

and

$$\mathbf{u}(t) = \begin{bmatrix} 1 & 0 \end{bmatrix} \cdot \mathbf{D} = \begin{bmatrix} p_C(t) & p_B(t) & p_A(t) \end{bmatrix}. \quad (3.26)$$

Equation 3.21 gives the binary to decimal conversion of $\mathbf{u}$. Thus, there exists a one-to-one correspondence between s and $\mathbf{u}$. On the other hand, from (3.25) $\mathbf{u}$ uniquely defines $\mathbf{D}$ for a healthy inverter. Therefore, the switching combination of the inverter $\mathbf{D}$ can be represented uniquely by s for each switching state. Given the switching state s the switching combination $\mathbf{D}$ can be determined from (3.25) with $p_A(t)$, $p_B(t)$, and $p_C(t)$ being the first, second, and third digits of a binary number equal to $s(t)$, i.e.,

$$p_A(t) = s(t) \mod 2, \quad (3.27)$$

$$p_B(t) = \lfloor \frac{s(t) \mod 4}{2} \rfloor, \quad (3.28)$$

and

$$p_C(t) = \lfloor \frac{s(t)}{4} \rfloor. \quad (3.29)$$

□

3.2.3 Voltage Space

Assume a voltage space consisting of $v_A(t)$, $v_B(t)$, and $v_C(t)$ as its axes and a cube centered at the origin with the side length of $2E_N$ (Fig. 3.2).

Figure 3.2: Voltage space and the eight normal switching states.

The switching states from Table 3.1 can be mapped to the vertexes of this cube in the voltage space. A state transition is shown by a line in the voltage space.

3.2.4 State Transitions

In this section, the state transition patterns in the voltage space are introduced. Assume the phase voltages are monitored for $t \leq t_0$ and the switching states are extracted. Whenever two adjacent switching states are non-equal, a transition occurs. Equation (3.30) defines a sequence of nonequivalent adjacent switching states X observed for $t \leq t_0$

$$X(t_0) = \langle s(t_0), s(t_1), s(t_2), \dots, s(t_n), \dots \rangle, \quad \text{for } n \in \mathbb{N} \quad (3.30)$$

where

$$t_0 > t_1 > t_2 > \dots > t_n > \dots \quad (3.31)$$

and t_n is every time instance at which the value of the switching state changes, i.e.,

$$s(t_n) \neq s(t_n^-). \quad (3.32)$$

where t^- is a time instance very near to t but less than it.

3.2.5 Fault Banned Zones

Consider a short-circuit fault in a switch of phase leg $\tilde{\varphi}$. Let $\tilde{R}_{\text{off}}$ and $\tilde{R}_{\text{on}}$ denote the internal resistances of the faulty switch in the off and on states respectively. In the

faulty situation,

$$\tilde{R}_{\text{off}} \approx \tilde{R}_{\text{on}} \approx 0. \quad (3.33)$$

If the upper switch of the phase leg is faulty,

$$v_{\tilde{\varphi}} = v^u, \quad (3.34)$$

where

$$v^u = \begin{cases} \frac{E}{2} \cdot \varepsilon_1 & \text{for } g_u = 1, g_l = 0 \\ \frac{E}{2} \cdot \varepsilon_2 & \text{for } g_u = 0, g_l = 1 \end{cases}, \quad (3.35)$$

$\varepsilon_1 \approx 1$, and $\varepsilon_2 \approx 0$; thus,

$$v^u \neq -E_N. \quad (3.36)$$

In this situation, the VSP does not appear in the $v_{\tilde{\varphi}} = -E_N$ plane of the voltage space. This plane is associated with four switching states that indicate a face of the cubic pattern in the voltage space. The VSP cannot enter this zone in the presence of the fault; thus, this area is named a fault-banned zone. Six faces of the cubic pattern allow isolating six different faulty switches. On the other hand,

$$v = v^l, \quad (3.37)$$

if the lower switch of phase $\tilde{\varphi}$ is faulty, where

$$v^l = \begin{cases} -\frac{E}{2} \cdot \varepsilon_2 & \text{for } g_u = 1, g_l = 0 \\ -\frac{E}{2} \cdot \varepsilon_1 & \text{for } g_u = 0, g_l = 1 \end{cases}. \quad (3.38)$$

Thus,

$$v^l \neq +E_N, \quad (3.39)$$

and the fault banned zones is in the $v_{\tilde{\varphi}} = +E_N$ plane in the voltage space; thus, the fault-banned zones of upper and lower switches of a phase leg are in the opposite faces of the cubic pattern. For example, Fig. 3.3 illustrates the fault-banned zones for Q_1 and Q_2 where $\tilde{\varphi} = A$.

Figure 3.3: Fault-banned zones for a faulty switch in phase A.

The fault-banned zone of Q_j can be represented by $\mathbf{F}_j$, a set of four switching states that are not achievable in the presence of a fault in Q_j . In (3.21), the switching states were determined based on the state of the upper switches of the inverter, $\mathbf{u}$. Conversely, equation (3.43) calculates $\tilde{s}$, the switching state based on the on–off states of the lower switches $\mathbf{l}$, where

$$\mathbf{l} := [0 \ 1] \cdot \mathbf{D}(t). \quad (3.40)$$

From (3.25),

$$\mathbf{l} = [1 - p_C(\alpha_n) \ 1 - p_B(\alpha_n) \ 1 - p_A(\alpha_n)]$$

and

$$\mathbf{u} + \mathbf{l} = [1 \ 1 \ 1]; \quad (3.41)$$

thus,

$$\mathbf{u} = [1 \ 1 \ 1] - \mathbf{l}, \quad (3.42)$$

by applying $\mathbf{u}$ in (3.21)

$$\tilde{s}(t) := ([1 \ 1 \ 1] - \mathbf{l}) \cdot \mathbf{b}. \quad (3.43)$$

In the no-fault situation, $\tilde{s}(t) = s(t)$. However, in the presence of a faulty switch $\tilde{s}(t)$ can be different from $s(t)$. This difference is used to define fault-banned zones,

$$\mathbf{F}_j := \mathbf{Y}_j^u \cup \mathbf{Y}_j^l - \mathbf{Y}_j^u \cap \mathbf{Y}_j^l. \quad (3.44)$$

In (3.44), $\mathbf{Y}_j^u$ and $\mathbf{Y}_j^l$ are two sets of all possible $s(t)$ and $\tilde{s}(t)$ that can be obtained in the presence of a short-circuit fault in Q_j

$$\mathbf{Y}_j^u = \{s(t) | d_j(t) = 1, \forall g_i(t) \in \{0, 1\}\}$$

and

$$\mathbf{Y}_j^l = \{\tilde{s}(t) | d_j(t) = 1, \forall g_i(t) \in \{0, 1\}\}.$$

3.3 Properties of VSP for SPWM Inverter

In this section, it is proven that the following properties exist for the VSP obtain from the pole voltages of a three-phase two level inverter

- The switching state s changes whenever one of the PWM signals of a phase leg varies.
- The state transitions occur at the edges of the cube rather than its diagonals;
- The state transitions occur at different time instances within one carrier period.
- For a healthy inverter, six transitions occur within one carrier period.

These properties are concluded based on the working principle of a three-phase SPWM VSI, and will be used in the VSP-based FDI procedure.

3.3.1 Working Principle of a SPWM Three-Phase Inverter

Consider the three-phase two-level inverter of Fig. 3.1. Three PWM signals are required to control its switches. A control block generates SPWM pulses $p_\phi(t)$, by comparing a triangular carrier waveform $c(t)$, to the reference modulating signals, $r_\phi(t)$ for $\phi = A, B, C$,

$$p_\phi(t) := \begin{cases} 1, & r_\phi(t) \geq c(t) \\ 0, & r_\phi(t) < c(t) \end{cases}, \quad (3.45)$$

where

$$r_\varphi(t) := A_r \sin(2\pi F_r t + \phi_\varphi), \quad (3.46)$$

For a three-phase SPWM inverter, the displacement angle $\phi = 0, -\frac{2\pi}{3}, \frac{2\pi}{3}$ for $\varphi = A, B, C$ respectively. The carrier signal, with amplitude A_c and frequency F_c , is

$$c(t) := \begin{cases} 4A_c(F_c t - k - \frac{1}{4}), & \text{if } kT_c \leq t < (k + \frac{1}{2})T_c \\ -4A_c(F_c t - k - \frac{3}{4}), & \text{if } (k + \frac{1}{2})T_c \leq t < (k + 1)T_c \end{cases}$$

where $k = \lfloor \frac{t}{T_c} \rfloor$. (3.47)

In (5.18), T_c and T_r are the periods of $c(t)$ and $r_\varphi(t)$ respectively. The frequency–modulation ratio, N , is chosen as a multiple integer of three to ensure elimination of the dominant harmonics and perfect symmetry in the three-phase outputs [1], [89], thus,

$$N := \frac{F_c}{F_r} = \frac{T_r}{T_c} = 3m_1, \quad m_1 \in \mathbb{N}^+.$$

The amplitude–modulation ratio or the modulation index M is less than one for the power electronic applications when the over–modulation is avoided, hence,

$$M := \frac{A_r}{A_c} \quad 0 < M < 1. \quad (3.48)$$

Figure 3.4 illustrates the concept of SPWM modulation. In this figure, $M = 0.8$ and $F_r = 60\text{Hz}$ are chosen as the typical power inverter application. Typically F_c in the 1 to 20 kHz range are applied [13]; however, in this figure, F_c is reduced to 540 Hz for better illustration purpose. The gate control signals and the resulting phase voltages v_A , v_B , and v_C are shown in Fig. 3.5 and Fig. 3.6 for a no-fault situation.

3.3.2 Mathematical Proofs

Considering the working principle of the SPWM VSI, in the following propositions it is proven that the state transitions occur at the edges of the cube (rather than its diagonals); Proposition 3.3.1 shows that the switching state s changes whenever one of the PWM signals of a phase leg varies, and Proposition 3.3.2 proves that the phase changes occur at different time instances within one carrier period (T_c).

Figure 3.4: Reference, carrier, and PWM Signals, $M = 0.8$, $F_r = 60\text{Hz}$, and $F_c = 540\text{Hz}$.

Proposition 3.3.1. Assume the value of p_A , p_B , and p_C changes at $t = \alpha$, $t = \beta$, and $t = \gamma$ respectively,

$$p_\varphi(t_n) \neq p_\varphi(t_n^-) \Leftrightarrow s(t_n) \neq s(t_n^-).$$

Proof. Denote

$$t_n = \begin{cases} \alpha_n & \text{if } p_A(t_n) \neq p_A(t_n^-), \\ \beta_n & \text{if } p_B(t_n) \neq p_B(t_n^-), \\ \gamma_n & \text{if } p_C(t_n) \neq p_C(t_n^-). \end{cases}$$

If

$$p_A(\alpha_n) \neq p_A(\alpha_n^-), \quad (3.49)$$

then

$$p_A(\alpha_n) = 1 - p_A(\alpha_n^-) \quad \text{for } p_\varphi(t) \in \{0, 1\}. \quad (3.50)$$

From (3.25),

$$\begin{aligned} \mathbf{D}(\alpha_n) &= \begin{bmatrix} p_C(\alpha_n) & p_B(\alpha_n) & p_A(\alpha_n) \\ 1 - p_C(\alpha_n) & 1 - p_B(\alpha_n) & 1 - p_A(\alpha_n) \end{bmatrix} \\ &= \begin{bmatrix} p_C(\alpha_n^-) & p_B(\alpha_n^-) & 1 - p_A(\alpha_n^-) \\ 1 - p_C(\alpha_n^-) & 1 - p_B(\alpha_n^-) & p_A(\alpha_n^-) \end{bmatrix}. \end{aligned} \quad (3.51)$$

Applying $\mathbf{D}(\alpha_n)$ in (3.21),

$$s(\alpha_n) = 4p_C(\alpha_n^-) + 2p_B(\alpha_n^-) + 1 - p_A(\alpha_n^-).$$

Figure 3.5: Gate control signals.

On the other hand,

$$s(\alpha_n^-) = 4p_C(\alpha_n^-) + 2p_B(\alpha_n^-) + p_A(\alpha_n^-). \quad (3.52)$$

Thus,

$$s(\alpha_n) - s(\alpha_n^-) = 1 - 2p_A(\alpha_n^-), \quad (3.53)$$

and since

$$p_A(\alpha_n^-) \in \{0, 1\}, \quad (3.54)$$

$$s(\alpha_n) - s(\alpha_n^-) \neq 0 \Rightarrow s(\alpha_n) \neq s(\alpha_n^-). \quad (3.55)$$

Figure 3.6: Current and voltage waveforms in the no-fault situation.

Similarly, it can be proven that

$$\text{if } p_A(\beta_n) \neq p_A(\beta_n^-) \Leftrightarrow s(\beta_n) \neq s(\beta_n^-), \quad (3.56)$$

and

$$\text{if } p_A(\gamma_n) \neq p_A(\gamma_n^-) \Leftrightarrow s(\gamma_n) \neq s(\gamma_n^-). \quad (3.57)$$

The result shows a change in the switching state $s(t)$ happens whenever one of the $p_A(t)$, $p_B(t)$, or $p_C(t)$ changes. $\square$

Proposition 3.3.2. Assume that $W(t_0)$ is a subsequence of $X(t_0)$ as described in (3.30) with the length of w such that $t_0 - t_w < T_c$.

For $w = 6$, $t_0 - t_w < T_c$ and the changes of the PWM signals (p_A , p_B , p_C) occur at different time instances α_{n_1} , β_{n_2} , and γ_{n_3} , where $n_1 \neq n_2 \neq n_3$, and $\min\{n_1, n_2, n_3\} \geq 0$, and $\max\{n_1, n_2, n_3\} \leq w$, i.e.,

$$p_A(\alpha_{n_1}) \neq p_A(\alpha_{n_1}^-), p_B(\alpha_{n_1}) = p_B(\alpha_{n_1}^-), p_C(\alpha_{n_1}) = p_C(\alpha_{n_1}^-), \quad (3.58)$$

$$p_A(\beta_{n_2}) = p_A(\beta_{n_2}^-), p_B(\beta_{n_2}) \neq p_B(\beta_{n_2}^-), p_C(\beta_{n_2}) = p_C(\beta_{n_2}^-), \quad (3.59)$$

and

$$p_A(\gamma_{n_3}) = p_A(\gamma_{n_3}^-), p_B(\gamma_{n_3}) = p_B(\gamma_{n_3}^-), p_C(\gamma_{n_3}) \neq p_C(\gamma_{n_3}^-). \quad (3.60)$$

Proof. Let define $\tau(q) := \{t | \frac{q}{2}T_c \leq t < \frac{q+1}{2}T_c\}$ for $q \in \mathbb{Z}$. If the theorem is true, there exist α_{n_1} , β_{n_2} , and γ_{n_3} in $\tau(q)$, such that $\alpha_{n_1} \neq \beta_{n_2}$, $\alpha_{n_1} \neq \gamma_{n_3}$, and $\beta_{n_2} \neq \gamma_{n_3}$. From Proposition 3.3.1 if $s(t_n) \neq s(t_n^-)$, then $p_\varphi(t_n) \neq p_\varphi(t_n^-)$ and from (3.45)

$$r_\varphi(t_n) = c(t_n). \quad (3.61)$$

Let $q = \lfloor \frac{2t}{T_c} \rfloor$; thus, from (5.18),

$$c(t) = \begin{cases} 4A_c(F_c t - k - \frac{1}{4}), & \text{for } q = 2k \\ -4A_c(F_c t - k - \frac{3}{4}), & \text{for } q = 2k + 1 \end{cases} \quad (3.62)$$

Let assume $q = 2k$. Applying (3.3), and (3.62) in (3.61)

$$A_r \sin(2\pi F_r t_n + \phi) - 4A_c(F_c t_n - k - \frac{1}{4}) = 0, \quad (3.63)$$

$$M \sin(2\pi F_r t_n + \phi) = 4(F_c t_n - k - \frac{1}{4}). \quad (3.64)$$

Let

$$\chi_\varphi := \sin(2\pi F_r t_n + \phi). \quad (3.65)$$

Applying χ_φ in (3.64),

$$M\chi_\varphi = 4(F_c t_n - k - \frac{1}{4}) \quad (3.66)$$

hence,

$$t_n = T_c(\frac{1}{4} + k + \frac{M\chi_\varphi}{4}). \quad (3.67)$$

From (3.65),

$$-1 \leq \chi_\varphi \leq 1, \quad (3.68)$$

and consequently,

$$kT_c < t_n < (\frac{1}{2} + k)T_c; \quad (3.69)$$

thus,

$$2k < \frac{2t_n}{T_c} < 2k + 1, \quad (3.70)$$

and $q = \lfloor \frac{2t_n}{T_c} \rfloor = 2k$. The result proves the existence of $\alpha_{n_1}, \beta_{n_1}, \gamma_{n_1}$ for even $q = \lfloor \frac{2t_n}{T_c} \rfloor$. Similar proof can be used for the odd $q = 2k + 1$. So, for every $t_0 \geq \tau(q')$ there exists an integer $q = q' - 1$ where $q' = \lfloor \frac{2t_0}{T_c} \rfloor - 1$ such that $\{\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3}\} \in \tau(q)$.

Now, it is shown $\alpha_{n_1} \neq \beta_{n_2} \neq \gamma_{n_3}$. From (3.67),

$$\alpha_{n_1} = T_c \left(\frac{1}{4} + k + \frac{M\chi_A}{4} \right), \quad (3.71)$$

$$\beta_{n_2} = T_c \left(\frac{1}{4} + k + \frac{M\chi_b}{4} \right), \quad (3.72)$$

and

$$\gamma_{n_3} = T_c \left(\frac{1}{4} + k + \frac{M\chi_c}{4} \right). \quad (3.73)$$

If α_{n_1} were equal to β_{n_2} , from (3.71) and (3.72)

$$\chi_A = \chi_b. \quad (3.74)$$

Replacing χ_ϕ from (3.65) yields

$$\sin(2\pi F_r \alpha_{n_1}) = \sin(2\pi F_r \alpha_{n_1} - \frac{2\pi}{3}). \quad (3.75)$$

Solving the above equation gives

$$\alpha_{n_1} = \frac{6m_2 + 5}{12F_r}, \quad m_2 \in \mathbb{Z}. \quad (3.76)$$

Now it is shown that α_{n_1} is not an acceptable solution. From (3.71),

$$M = \frac{4F_c \alpha_{n_1} - 4k - 1}{\sin(2\pi F_r \alpha_{n_1})}, \quad (3.77)$$

by replacing α_{n_1} from (3.76),

$$M = \frac{\frac{F_c}{3F_r} (6m_2 + 5) - 4k - 1}{\sin(\frac{5\pi}{6} + m_2\pi)}. \quad (3.78)$$

From (3.48), $\frac{F_c}{3F_r} = m_1$; thus,

$$M = \frac{6m_2m_1 + 5m_1 - 4k - 1}{(-1)^{m_2} \sin(\frac{5\pi}{6})} = (-1)^{m_2} (12m_2m_1 + 10m_1 - 8k - 2). \quad (3.79)$$

Equation (3.79) forces M to be an integer value which contradicts the assumption, so it is forced to conclude that $\alpha_{n_1} \neq \beta_{n_2}$.

Similarly, $\alpha_{n_1} = \gamma_{n_3}$ results in

$$\alpha_{n_1} = \frac{6m_3 + 1}{12F_r}, m_3 \in \mathbb{Z}. \quad (3.80)$$

Applying α_{n_1} in (3.77)

$$M = \frac{\frac{N}{3}(6m_3 + 1) - 4k - 1}{\sin(\frac{\pi}{6}m_3\pi)} = \frac{6m_1m_3 + m_1 - 4k - 1}{(-1)^{m_3}\sin(\frac{\pi}{6})} = (-1)^{m_3}(12m_1m_3 + 2m_1 - 8k - 2). \quad (3.81)$$

$$\Rightarrow M \in \mathbb{Z}$$

Also, $\beta_{n_2} = \gamma_{n_3}$ results in

$$\beta_{n_2} = \frac{2m_4 + 1}{4F_r}, \quad m_4 \in \mathbb{Z}. \quad (3.82)$$

From (3.72),

$$M = \frac{4F_c\beta_{n_2} - 4k - 1}{\sin(2\pi F_r\alpha_{n_1} - \frac{2\pi}{3})}. \quad (3.83)$$

Applying β_{n_2} from (3.82) in (3.83),

$$M = \frac{\frac{F_c}{F_r}(2m_2 + 1) - 4k - 1}{\sin(-\frac{\pi}{6} + m_4\pi)} = \frac{6m_4m_1 + 3m_1 - 4k - 1}{(-1)^{m_4}\sin(-\frac{\pi}{6})} = (-1)^{1+m_4}(12m_4m_1 + 6m_1 - 8k - 2). \quad (3.84)$$

$$\Rightarrow M \in \mathbb{Z} \quad (3.85)$$

The results show M is an integer which is inconsistent with the assumption

$$0 < M < 1. \quad (3.86)$$

Therefore, it is concluded that $\alpha_{n_1} \neq \beta_{n_2}$, $\alpha_{n_1} \neq \gamma_{n_3}$, and $\beta_{n_2} \neq \gamma_{n_3}$ exist in $\tau(q)$.

Therefore, $W(t_0)$ for $t_0 \in \tau(q+1)$ and $t_w \in \tau(q-1)$ includes $\tau(q)$. It means within $t_0 - t_w < T_c$ all $\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3} \in \tau(q)$ can be observed. Since only three states change within $\tau(q)$

$$\lfloor \frac{n_1}{3} \rfloor = \lfloor \frac{n_2}{3} \rfloor = \lfloor \frac{n_3}{3} \rfloor = q \quad (3.87)$$

and the minimum w that certainly includes $\tau(q)$ is

$$w_{min} = 6. \quad (3.88)$$

□

Proposition 3.3.3. *If v_A is monitored for a time span such as $W(t_0)$ where α^- and α belong to $W(t_0)$, then both levels of voltage, $\pm E_N$, will be observed. The same condition exists for the other two phases;*

$$\{v_A(\alpha^-), v_A(\alpha)\} = \{-E_N, E_N\},$$

$$\{v_B(\beta), v_B(\beta^-)\} = \{E_N, -E_N\},$$

and

$$\{v_C(\gamma), v_C(\gamma^-)\} = \{E_N, -E_N\}.$$

Proof. Let $\varphi = A$, applying $\mathbf{D}(\alpha_n)$ from (3.51) in (3.10) yields

$$\begin{aligned} \mathbf{v}(\alpha_n) = \mathbf{e} \cdot \mathbf{D}(\alpha_n) &= [E_N, -E_N] \begin{bmatrix} p_C(\alpha_n^-) & p_B(\alpha_n^-) & 1 - p_A(\alpha_n^-) \\ 1 - p_C(\alpha_n^-) & 1 - p_B(\alpha_n^-) & p_A(\alpha_n^-) \end{bmatrix} \\ &= [v_C(\alpha_n^-), v_B(\alpha_n^-), -v_A(\alpha_n^-)]. \end{aligned} \quad (3.89)$$

From (3.10)

$$\mathbf{v}(\alpha_n^-) = [v_C(\alpha_n^-), v_B(\alpha_n^-), v_A(\alpha_n^-)]. \quad (3.90)$$

Squaring both sides yields

$$v_A(\alpha_n) = -v_A(\alpha_n^-). \quad (3.91)$$

Thus,

$$v_A(\alpha_n) = \begin{cases} E_N, & \text{if } v_A(\alpha_n^-) = -E_N \\ -E_N, & \text{if } v_A(\alpha_n^-) = E_N \end{cases}$$

Similar proofs can be done for $\varphi = B$, and $\varphi = C$. Thus,

$$\{v_A(\alpha), v_A(\alpha^-)\} = \{E_N, -E_N\}, \quad (3.92)$$

$$\{v_B(\beta), v_B(\beta^-)\} = \{E_N, -E_N\}, \quad (3.93)$$

and

$$\{v_C(\gamma), v_C(\gamma^-)\} = \{E_N, -E_N\}. \quad (3.94)$$

□

As a result of Proposition 3.3.3, if just one of the voltage levels is observed in a window of time containing α , β , or γ , then a fault is detected in phase A, B, or C. In this situation, some switching states cannot be observed that can be indicated by a fault-banned zone in the VSP. From (3.88), the minimum length of the observation window is equal to six. Therefore, by monitoring six consequent non-adjacent switching states and comparing them to the predefined fault-banned zones, the fault can be detected and the faulty switch can be isolated.

3.4 Procedure of VSP-based FDI

In this section, a fault diagnosis algorithm is proposed for unknown switching frequencies; where access to the control signals is not possible or the switching frequency changes by the feedback loop. Suppose that the system is healthy at time t_0 and a fault occurs at $t_f > t_0$. The objective is to detect and isolate the faulty switch at time $t_e > t_f$ given the switching states. The process contains four stages; extracting switching states, initialization, fault detection, and fault isolation.

3.4.1 Extracting Switching States

Fault diagnosis process starts by monitoring three-phase voltages and extracting the corresponding switching states. Let

$$\mathbf{v}(t) = [v_C(t), v_B(t), v_A(t)] \quad (3.95)$$

be the vector of observed voltages from the detectors. A threshold span ϵ_m in the neighborhood of each normal voltage level E_N is defined, and the monitored voltage vector in this neighborhood is mapped to a known $\mathbf{v}_s$. The neighborhood of $\mathbf{v}_s$ is defined as

$$\mathbf{h}_s = \mathbf{v}_s \cdot \text{diag}(\epsilon_C, \epsilon_B, \epsilon_A), \quad (3.96)$$

where ϵ_φ for $\varphi = A, B, C$ is the distance between $\mathbf{v}_s$ and $\mathbf{h}_s$ in each direction of the voltage space. Equation (3.97) defines a set of all voltages in the neighborhood of $\mathbf{v}_s$ within a distance of ϵ_m in each direction of the voltage space.

$$\mathbf{H}_s =: \{\mathbf{h}_s | \forall 1 - \epsilon_m \leq \epsilon_\varphi < 1 + \epsilon_m\} \quad (3.97)$$

Threshold value ε_m is selected such that both levels of voltage in the faulty situation, v^u and v^l , are isolable, e.g., $\varepsilon_m = 0.25$. This threshold should be big enough to cancel out the effect of the noise, disturbance, and component tolerances as well as the on-state voltage drop in the IGBTs. The threshold value can automatically be adjusted by monitoring the healthy system for a few periods if required.

From Proposition 3.2.1 and (3.10), there exists a one-to-one correspondence between $\mathbf{v}_s$ and s . Thus, any observed voltage vector $\mathbf{v}(t)$ can be mapped to a known state $\kappa \in \mathbb{S}$, where $\mathbb{S}$ is as defined in (3.24), as shown in (3.98)

$$s(t) := \begin{cases} \kappa, & \text{if } \mathbf{v}(t) \in \mathbf{H}_\kappa \\ s(t^-) & \text{otherwise} \end{cases}. \quad (3.98)$$

3.4.2 Initialization

Let

$$W(t_0) = \langle s(t_0), s(t_1), s(t_2), \dots, s(t_5) \rangle = \langle w_1, w_2, \dots, w_6 \rangle \quad (3.99)$$

be a subsequence of non-equal adjacent switching states. The sequence $W(t_0)$ contains α_{n_1} , β_{n_2} and γ_{n_2} in a random order, therefore, $W(t_0)$ is shown as a sequence of sets

$$W(t_0) = \langle S'_{q_0+1}, S_{q_0}, S'_{q_0-1} \rangle, \quad (3.100)$$

where

$$S_q = \{s(\alpha_{n_1}), s(\beta_{n_2}), s(\gamma_{n_3})\}, \quad (3.101)$$

$$q = \lfloor \frac{n_1}{3} \rfloor = \lfloor \frac{n_2}{3} \rfloor = \lfloor \frac{n_3}{3} \rfloor, \quad (3.102)$$

$$S'_q \subset S_q, \quad (3.103)$$

$$|S'_{q_0+1}| = \psi, \quad (3.104)$$

and

$$t_\psi = \max\{\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3}\}. \quad (3.105)$$

To find ψ , three consequent states that contain changes of all three phases, i.e., S_q should be found. Let $\oplus$ be the XOR operator which is applied to the binary value of $s(t)$. From the state definition,

$$p_A(\alpha_{n_1}) \neq p_A(\alpha_{n_1}^-) \Rightarrow s(\alpha_{n_1}) \oplus s(\alpha_{n_1}^-) = 1, \quad (3.106)$$

$$p_B(\beta_{n_2}) \neq p_B(\beta_{n_2}^-) \Rightarrow s(\beta_{n_2}) \oplus s(\beta_{n_2}^-) = 2, \quad (3.107)$$

$$p_C(\gamma_{n_3}) \neq p_C(\gamma_{n_3}^-) \Rightarrow s(\gamma_{n_3}) \oplus s(\gamma_{n_3}^-) = 4. \quad (3.108)$$

Therefore, there exists a subsequence of $W(t_0)$ such that

$$\{w_\psi \oplus w_{\psi+1}, w_{\psi+1} \oplus w_{\psi+2}, w_{\psi+2} \oplus w_{\psi+3}\} = \{1, 2, 4\},$$

where $1 \leq \psi \leq 3$. The initialization stage will be accomplished by finding ψ .

3.4.3 Fault Detection

After the initialization stage, the system is being monitored for more new states. Let

$$\lambda = \psi + 3\theta \quad (3.109)$$

and

$$U(t_{\lambda-\eta}) = \langle x_{\lambda-\eta}, \dots, x_{\lambda-1}, x_\lambda \rangle, \quad 1 \leq \eta \leq 3. \quad (3.110)$$

Whenever a new state is detected, the fault detection test is carried on. Let

$$\hat{U}(\eta) = x_{\lambda-\eta} \oplus x_{\lambda-\eta+1}. \quad (3.111)$$

A fault is detected if

$$\hat{U}(\eta) \notin \{1, 2, 4\}. \quad (3.112)$$

or

$$\hat{U}(\eta) = \hat{U}(\eta - 1). \quad (3.113)$$

If a fault is detected, the fault occurrence time is

$$t_{\lambda-\theta} < t_f < t_{\lambda-\eta} \quad (3.114)$$

which is less than one carrier period. However, if

$$\{x_{\lambda-3} \oplus x_{\lambda-2}, x_{\lambda-2} \oplus x_{\lambda-1}, x_{\lambda-1} \oplus x_\lambda\} = \{1, 2, 4\} \quad (3.115)$$

no fault is detected. Thus, θ is increased by one, and the fault detection test will be continued by restarting η . If a fault is detected, the fault isolation stage will be run.

3.4.4 Fault Isolation

Based on what was described in Section 3.4.3, if the phase voltages are monitored for a period of T_c , the value of all phase voltages will definitely change from one level to another one. Therefore, the VSP will not remain inside one face of the cubic pattern for $t_w = t_0 - T_c$. Thus, if none of the monitored states was a subset of F_j , as defined in Section 3.2.5, Q_j is diagnosed as the faulty switch. All fault-banned zones are calculated in Table 3.2 for a short-circuit fault in Q_j where $j = 1$ to 6. For the isolation

Table 3.2: Fault-banned zones of short-circuit faults.

Short-circuit fault location (Q_j)	Fault-banned zone (F_j)
Q_1	$\{0, 2, 4, 6\}$
Q_2	$\{1, 3, 5, 7\}$
Q_3	$\{0, 1, 4, 5\}$
Q_4	$\{2, 3, 6, 7\}$
Q_5	$\{0, 1, 2, 3\}$
Q_6	$\{4, 5, 6, 7\}$

purpose, the intersection of

$$W(t_e) = \langle x_{\lambda-2}, x_{\lambda-1}, \dots, x_{\lambda+3} \rangle \quad (3.116)$$

and each fault-banned zone is calculated. If

$$W(t_e) \cap F_j = \emptyset \quad (3.117)$$

then Q_j is isolated as the faulty switch. Fig. 3.7 illustrates the fault isolation in the voltage space for all six switches. After the fault occurs, the pattern cannot enter the fault-banned zone of the faulty switch.

Figure 3.7: Fault isolation in the voltage space.

3.5 Simulations

To evaluate the performance of the VSP-based FDI method, a three-phase two-level VSI with six power switches is modeled using MATLAB SimPowerSystems as shown in Fig. 3.8. In this figure, $Q_1, Q_2, \dots, Q_6$ implements an ideal IGBT, Gto, or MOSFET and anti-parallel diode. In this model, all six switches are similar, and the internal resistance of each switch is $R_{on} = 1\text{m}\Omega$, and $R_{off} = 100\text{ K}\Omega$ in on and off states respectively.

In order to simulate the short-circuit faults, a circuit breaker with internal resistance $R_f = 1\text{m}\Omega$ was added in parallel to each switch. In the normal situation, F1 to F6 of Fig. 3.8 are low; thus, SW1 to SW6 are open. The fault simulator block inserts a short-circuit fault in Q_j by closing the parallel switch at $t = t_f$. For example, if F1=1 then SW1 is closed which simulates a short-circuit fault in Q_1 . This model covers

Figure 3.8: Simulink model of the VSI.

short-circuit faults caused either by gate-misfiring, or damaging of internal diode, or drain-source junction. Only single faults are considered in the simulations. Fig. 3.9 depicts the FDI system in MATLAB Simulink.

Figure 3.9: Simulink model of the FDI procedure.

3.5.1 Sampling Time

In this model, three voltage detectors monitor the phase voltages as shown in Fig. 3.8. The sampling period should be chosen so that all changes in the voltage signals are detectable,

$$T_s < \frac{P_m}{2}. \quad (3.118)$$

where P_m is the minimum pulse width of the voltage signal. The minimum pulse width occurs at the peak of the reference signal; thus,

$$\frac{P_m}{T_c} = \frac{1 - M}{2}, \quad (3.119)$$

hence,

$$P_m = \frac{1-M}{2} T_c. \quad (3.120)$$

Thus, considering the NyquistShannon sampling theorem, the following condition should be considered for selecting a proper sampling time,

$$T_s < \frac{1-M}{4} T_c. \quad (3.121)$$

3.5.2 Results

Fig. 3.10 illustrates the simulation results for diagnosis of a short-circuit fault which occurs at $t_f = 9ms$ in Q_1 . In this experiment $F_r = 60Hz$, $F_c = 900Hz$, and $M = 0.8$ and

Figure 3.10: Fault diagnosis result of a short-circuit fault in Q_1 .

the output of the inverter is connected to a three-phase grounded Y-connected series RL load. The load is selected such that its time constant is selected as

$$\tau_L = \frac{L}{R} = \frac{1}{3F_r} \quad (3.122)$$

to satisfy (3.48). In this model, $R = 1\Omega$ and $L = 5.6mH$ for all three phases, and $E = 400$. In this figure, i_A , i_B , and i_C represents the current signals of phases A, B, and C respectively. The current signal is illustrated in order to show the effect of the switch fault in the load. However, the current is not used for the FDI purpose.

Fig. 3.11 shows the switching state pattern in the voltage space. After the fault occurs the pattern does not appear on a face of the cube determined by $\mathbf{v}_0, \mathbf{v}_2, \mathbf{v}_4$, and $\mathbf{v}_6$. Comparing to the fault-banned zones of Table 3.2, Q_1 is isolated as the faulty switch. The last diagram of Fig. 3.10 shows the diagnosis result, $j = 0$ represents the no-fault situation and $j = 1$ indicates the existence of a fault in Q_1 . In this example, the fault is detected in $t_d = 392.5\mu s$ which is equal to 35% of T_c . The simulation results verify the proposed method in all cases.

Figure 3.11: Switching state pattern in the voltage space in presence of a short-circuit fault in Q_1 .

The maximum fault detection time is proportional to the carrier period. Therefore, for higher carrier frequencies, the fault detection time is lower. In the theory, an infinite sampling frequency was assumed. However, in the simulations, the sampling period is limited. Therefore, in some instances where $\alpha - \beta < T_s$ (or $\beta - \gamma < T_s$, or $\alpha - \gamma < T_s$), the difference between α and β (or β and γ , or α and γ) is not detectable, and two phase voltages can change at the same time which results in a diagonal transition in the voltage space. This transitions can cause false alarms. In order to prevent this false alarms, the fault detection procedure is skipped and fault isolation task is continually running. If $j \neq 0$ a fault is detected. Although this modification can increase the maximum fault detection time, no false alarm will be detected.

3.5.3 FDI For Motor Drive

In the following experiments, the three-phase inverter is connected to a PMSM as shown in Fig. 3.12. The stator windings are connected in Wye to an internal neutral point. The three-phase machine has trapezoidal back EMF waveform with a round rotor. The motor parameters are shown in Table 3.3. Rotor flux position when $\theta = 0$ is 90 degree behind phase A axis. The mechanical torque is implemented at $t = 10$ ms in the form of a step with final value of $T_m = 3 \text{ N.m}$.

Figure 3.12: Simulink model of a three-phase motor drive feeding a permanent magnet synchronous motor with IGBT fault simulator and fault diagnosis modules.

Table 3.3: Parameters of the motor used in the simulations.

Motor Parameter	Value
Stator phase resistance R_s	$2.8750 \, \Omega$
Stator phase inductance L_s	$8.5e - 3 \, \text{H}$
Flux linkage established by magnets	$0.175 \, \text{V.s}$
Back EMF flat area	120°
Inertia	$0.8e - 3 \, \text{Kg.m}^2$
viscous damping	$1e - 3 \, \text{N.m.s}$
static friction	$4 \, \text{N.m}$
Initial conditions ω_m	$0 \, \text{rad/s}$
θ_m	0°

A short-circuit fault (SCF) is inserted in Q_1 , the upper switch of phase A of the motor drive, at $t_f = 47$ ms. As it can be seen in Fig. 3.13, the stator current exceeds its nominal value. In the meantime, the rotor speed fluctuates and even the rotation direction changes (Fig. 3.14). In this condition, motor experiences a high electromagnetic

force (Fig. 3.15). Therefore, a single short-circuit fault in the motor drive, can cause catastrophic damages to the motor and the mechanical load connected to it within a few milliseconds.

Figure 3.13: Stator currents with a short-circuit fault in Q_1 .

Figure 3.14: Rotor speed with a short-circuit fault in Q_1 .

Figure 3.15: Electromagnetic torque with a short-circuit fault in Q_1 .

In Figures 3.16 and 3.17 the fault diagnosis algorithm is applied and the short-circuit faults in Q_1 and Q_2 are diagnosed within a few microseconds. In these figures, j indicates the location of the faulty switch (Q_j) and $j = 0$ indicates no-fault situation. Table 3.4 summarizes the fault diagnosis time gained in the simulations. For all six tests, the fault is inserted at t_f , the sampling time is set to $T_s = 2.5\mu s$, and the switching period is $T_c \approx 50\mu s$. All switch faults were diagnosed successfully in $65\mu s$ on average.

Figure 3.16: Phase voltages and voltage state with a short-circuit fault occurs in Q_1 .

 Figure 3.17: Phase voltages and voltage state with a short-circuit fault occurs in Q_2 .

Table 3.4: Summary of the fault diagnosis time gained in the simulations. The fault is inserted in two different time instances.

Fault insertion time	$t_f = 52.0\text{ms}$	$t_f = 47.0\text{ms}$
Fault location	FDI time (μs)	FDI time (μs)
Q_1	42.5	67.5
Q_2	92.5	67.5
Q_3	72.5	50.0
Q_4	22.5	75.0
Q_5	55.0	40.0
Q_6	77.5	90.0
Average FDI time	60.4	65.0

The switches were controlled by a SPWM digitized controller. The controller was implemented as a Simulink block in Matlab as shown in Fig. 3.19. Six gate control signals were then delivered to the inverter switches through NI PCI6025e I–O card. The sampling time was selected $T_s = 4.6296e - 4s$, Matlab could not perform well for the smaller sampling times. Thus, the carrier frequency was reduced accordingly and the experiments were done with $F_r = 7.5Hz$, $F_c = 45.0003 Hz$, $T_c = 0.0222s$, and $T_r = 0.1333s$.

Figure 3.19: SPWM control block for generating six gate signals.

Fig. 3.20 illustrates the SPWM control signals in the no-fault situation. In the upper diagram, the sinusoidal reference signals and the carrier signals are shown. The other three diagrams show the PWM signals of each phase leg. The gate control signals are then generated based on the PWM signals as shown in Fig. 3.21.

Figure 3.20: SPWM control signals in no-fault situation.

Figure 3.21: Gate control signals in no-fault situation.

For the FDI purpose, the phase voltages are needed. Thus, the pole voltage signals of the three phases were measured using the same NI PCI6025e I–O card. The inputs are set in the differential mode. In this mode, the input can accept bidirectional voltage values in $\pm 10V$ range. Thus, the dc sources are set to 5V to ensure safety and protection for the I–O card. An amplifier needs to be added in the input of the NI PCI6025e if voltages out of this range are to be measured. Fig. 3.22 shows the Simulink model of the SPWM control, fault insertion, and diagnosis.

Figure 3.22: Implementation of the FDI block and the inverter as Hardware-In-Loop in Simulink.

The outputs of the SPWM controller were connected to a fault insertion block. The fault location, j , fault type, and the fault insertion time, t_i was defined by the user. The fault was inserted as a gate-misfiring fault at the desired time instance defined by the user. Thus,

$$G_j(t > t_j) = 1. \quad (3.123)$$

The Fault Diagnosis block implements the VSP-based FDI algorithm to derive the non-equal adjacent switching states and diagnose the short-circuit faults. Hence, on-line control and diagnosis for a real inverter circuit was possible with this set-up.

3.7 Experimental Results

Fig. 3.23 illustrates the FDI results for diagnosis of a short-circuit fault in Q_1 . As shown in Fig. 3.23a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_1 is short circuited at $t_f = 0.5s$. However, the effect of fault shows itself when Q_2 turns on at $t = 0.51$. In this situation, v_A cannot reach $-5V$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{1, 5, 7, 3, 1, 3\}$. As it can be seen in Fig. 3.23b, the left face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_1 . Hence, $J = 1$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{1, 5, 7, 3, 1, 3\} \cap \{0, 2, 4, 6\} = \{\} = \emptyset, \quad (3.124)$$

$$W \cap F_2 = \{1, 5, 7, 3, 1, 3\} \cap \{1, 3, 5, 7\} = \{1, 3, 5, 7\} \neq \emptyset, \quad (3.125)$$

$$W \cap F_3 = \{1, 5, 7, 3, 1, 3\} \cap \{0, 1, 4, 5\} = \{1, 5\} \neq \emptyset, \quad (3.126)$$

$$W \cap F_4 = \{1, 5, 7, 3, 1, 3\} \cap \{2, 3, 6, 7\} = \{3, 7\} \neq \emptyset, \quad (3.127)$$

$$W \cap F_5 = \{1, 5, 7, 3, 1, 3\} \cap \{0, 1, 2, 3\} = \{1, 3\} \neq \emptyset, \quad (3.128)$$

$$W \cap F_6 = \{1, 5, 7, 3, 1, 3\} \cap \{4, 5, 6, 7\} = \{5\} \neq \emptyset, \quad (3.129)$$

$$W \cap F_j = \emptyset \implies j = 1. \quad (3.130)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.23a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 70.83% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.23: Experimental results of on-line diagnosis of a SCF in Q_1 with 8 states.

Fig. 3.24 illustrates the FDI results for diagnosis of a short-circuit fault in Q_2 . As shown in Fig. 3.24a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_2 is short circuited at $t_f = 0.5$, and the effect of fault shows itself instantly because at this moment Q_1 was on. In this situation, v_A cannot stay at $+5V$ and $v_A \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{0, 2, 6, 2, 0, 2\}$. As it can be seen in Fig. 3.24b, the right face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_2 . Hence, $J = 2$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 2, 4, 6\} = \{0, 2, 6\} \neq \emptyset, \quad (3.131)$$

$$W \cap F_2 = \{0, 2, 6, 2, 0, 2\} \cap \{1, 3, 5, 7\} = \{\} = \emptyset, \quad (3.132)$$

$$W \cap F_3 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 4, 5\} = \{0\} \neq \emptyset, \quad (3.133)$$

$$W \cap F_4 = \{0, 2, 6, 2, 0, 2\} \cap \{2, 3, 6, 7\} = \{2, 6\} \neq \emptyset, \quad (3.134)$$

$$W \cap F_5 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 2, 3\} = \{0, 2\} \neq \emptyset, \quad (3.135)$$

$$W \cap F_6 = \{0, 2, 6, 2, 0, 2\} \cap \{4, 5, 6, 7\} = \{6\} \neq \emptyset, \quad (3.136)$$

$$W \cap F_j = \emptyset \implies j = 2. \quad (3.137)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.24a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 158.33% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.24: Experimental results of on-line diagnosis of a SCF in Q_2 with 8 states.

Fig. 3.25 illustrates the FDI results for diagnosis of a short-circuit fault in Q_3 . As shown in Fig. 3.25a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_3 is short circuited at $t_f = 0.5$, and the effect of fault shows itself as $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{7, 3, 2, 3, 7, 3\}$. As it can be seen in Fig. 3.25b, the front face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_3 . Hence, $J = 3$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 2, 4, 6\} = \{2\} \neq \emptyset, \quad (3.138)$$

$$W \cap F_2 = \{7, 3, 2, 3, 7, 3\} \cap \{1, 3, 5, 7\} = \{3, 7\} \neq \emptyset, \quad (3.139)$$

$$W \cap F_3 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 1, 4, 5\} = \{\} = \emptyset, \quad (3.140)$$

$$W \cap F_4 = \{7, 3, 2, 3, 7, 3\} \cap \{2, 3, 6, 7\} = \{2, 3, 7\} \neq \emptyset, \quad (3.141)$$

$$W \cap F_5 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 1, 2, 3\} = \{2, 3\} \neq \emptyset, \quad (3.142)$$

$$W \cap F_6 = \{7, 3, 2, 3, 7, 3\} \cap \{4, 5, 6, 7\} = \{7\} \neq \emptyset, \quad (3.143)$$

$$W \cap F_j = \emptyset \implies j = 3. \quad (3.144)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.25a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 106.25% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.25: Experimental results of on-line diagnosis of a SCF in Q_3 with 8 states.

Fig. 3.26 illustrates the FDI results for diagnosis of a short-circuit fault in Q_4 . As shown in Fig. 3.26a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_4 is short circuited at $t_f = 0.5$, and the effect of fault shows itself as $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{1, 0, 1, 5, 1, 0\}$. As it can be seen in Fig. 3.26b, the back face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_4 . Hence, $J = 4$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 2, 4, 6\} = \{0\} \neq \emptyset, \quad (3.145)$$

$$W \cap F_2 = \{1, 0, 1, 5, 1, 0\} \cap \{1, 3, 5, 7\} = \{1, 5\} \neq \emptyset, \quad (3.146)$$

$$W \cap F_3 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 1, 4, 5\} = \{0, 1, 5\} \neq \emptyset, \quad (3.147)$$

$$W \cap F_4 = \{1, 0, 1, 5, 1, 0\} \cap \{2, 3, 6, 7\} = \{\} = \emptyset, \quad (3.148)$$

$$W \cap F_5 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 1, 2, 3\} = \{1\} \neq \emptyset, \quad (3.149)$$

$$W \cap F_6 = \{1, 0, 1, 5, 1, 0\} \cap \{4, 5, 6, 7\} = \{5\} \neq \emptyset, \quad (3.150)$$

$$W \cap F_j = \emptyset \implies j = 4. \quad (3.151)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.26a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 131.25% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.26: Experimental results of on-line diagnosis of a SCF in Q_4 with 8 states.

Fig. 3.27 illustrates the FDI results for diagnosis of a short-circuit fault in Q_5 . As shown in Fig. 3.27a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_5 is short circuited at $t_f = 0.5$, and the effect of fault shows itself as $v_C \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{5, 7, 5, 4, 5, 7\}$. As it can be seen in Fig. 3.27b, the bottom face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_5 . Hence, $J = 5$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 2, 4, 6\} = \{4\} \neq \emptyset, \quad (3.152)$$

$$W \cap F_2 = \{5, 7, 5, 4, 5, 7\} \cap \{1, 3, 5, 7\} = \{7\} \neq \emptyset, \quad (3.153)$$

$$W \cap F_3 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 1, 4, 5\} = \{4, 5\} \neq \emptyset, \quad (3.154)$$

$$W \cap F_4 = \{5, 7, 5, 4, 5, 7\} \cap \{2, 3, 6, 7\} = \{7\} \neq \emptyset, \quad (3.155)$$

$$W \cap F_5 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 1, 2, 3\} = \{\} = \emptyset, \quad (3.156)$$

$$W \cap F_6 = \{5, 7, 5, 4, 5, 7\} \cap \{4, 5, 6, 7\} = \{7\} \neq \emptyset, \quad (3.157)$$

$$W \cap F_j = \emptyset \implies j = 5. \quad (3.158)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.27a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 70.83% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.27: Experimental results of on-line diagnosis of a SCF in Q_5 with 8 states.

Fig. 3.28 illustrates the FDI results for diagnosis of a short-circuit fault in Q_6 . As shown in Fig. 3.28a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_6 is short circuited at $t_f = 0.5$, and the effect of fault shows itself as $v_C \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{3, 1, 0, 1, 3, 2\}$. As it can be seen in Fig. 3.28b, the top face of the cube is not touched by the members of W . From Table. 3.2, it can be seen that this face of cube determines the FBZ of Q_6 . Hence, $J = 6$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 2, 4, 6\} = \{0, 2\} \neq \emptyset, \quad (3.159)$$

$$W \cap F_2 = \{3, 1, 0, 1, 3, 2\} \cap \{1, 3, 5, 7\} = \{1, 3\} \neq \emptyset, \quad (3.160)$$

$$W \cap F_3 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 1, 4, 5\} = \{0, 1\} \neq \emptyset, \quad (3.161)$$

$$W \cap F_4 = \{3, 1, 0, 1, 3, 2\} \cap \{2, 3, 6, 7\} = \{2, 3\} \neq \emptyset, \quad (3.162)$$

$$W \cap F_5 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 1, 2, 3\} = \{0, 1, 2, 3\} \neq \emptyset, \quad (3.163)$$

$$W \cap F_6 = \{3, 1, 0, 1, 3, 2\} \cap \{4, 5, 6, 7\} = \{\} = \emptyset, \quad (3.164)$$

$$W \cap F_j = \emptyset \implies j = 6. \quad (3.165)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.28a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 131.25% of T_c .

(a) Time domain results.

(b) VSP.

Figure 3.28: Experimental results of on-line diagnosis of a SCF in Q_6 with 8 states.

3.8 Modifications

Table 3.5 summaries the experimental results. At it can be seen from this table, the average fault isolation time of the experiments was $111.42\%T_c$, and in some cases the FDI time was more than one switching period. In order to decrease the fault diagnosis

Table 3.5: Summary of fault diagnosis results obtained from experiments for short-circuit and open-circuit faults in Q_1 – Q_6 using unmodified approach with 8 states.

Fault location (Q_j)	Diagnosis time for SCF (% T_c)
Q_1	70.83
Q_2	158.33
Q_3	106.25
Q_4	131.25
Q_5	70.83
Q_6	131.25
Average FDI time	111.42

time and limit it to only one switching period, a new level of voltage is considered in the digitalization stage. Hence, three levels of voltage has been considered which results in $3^3 = 27$ states in the voltage space as shown in Fig. 3.29. Only eight states which indicates the vertexes of the cube are the healthy states and the rest belongs to the faulty situations.

Figure 3.29: 27 states in the voltage space.

In these experiments, $\mathbf{b} = [1 \ 3 \ 9]$, and 27 healthy and faulty states were considered. When a short-circuit fault occurs, a new state can appear because of the fault

occurrence. Therefore, we have to consider this new state in the length of the fault detection window. The new length of the FDI window is $n = 6 + 1 = 7$.

The Fault banned zones are calculated based on the 27 states as shown in Table 3.6;

Open-circuit fault location (Q_j)	Fault-banned zone (F_j)
Q_1	$\{0, 3, 6, 9, 12, 15, 18, 21, 24\}$
Q_2	$\{2, 5, 8, 11, 14, 17, 20, 23, 26\}$
Q_3	$\{0, 1, 2, 9, 10, 11, 18, 19, 20\}$
Q_4	$\{6, 7, 8, 15, 16, 17, 24, 25, 26\}$
Q_5	$\{0, 1, 2, 3, 4, 5, 6, 7, 8\}$
Q_6	$\{18, 19, 20, 21, 22, 23, 24, 25, 26\}$

Table 3.6: Fault-banned zones of 27 states for short-circuit faults.

3.8.1 Experimental Results of the modified approach

In the following experiments the modified VSP-based FDI has been applied. Fig. 3.30 illustrates the FDI results for diagnosis of a short-circuit fault in Q_1 . As shown in Fig. 3.30a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_1 is short circuited at $t_f = 0.5s$. In this situation, $v_A \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{2, 20, 26, 8, 2, 1, 2\}$. As it can be seen in Fig. 3.30b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 3.30: Experimental results of on-line diagnosis of a SCF in Q_1 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_1 . Hence, $J = 1$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{\} = \emptyset, \quad (3.166)$$

$$W \cap F_2 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 8, 20, 26\} \neq \emptyset, \quad (3.167)$$

$$W \cap F_3 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{1, 2, 20\} \neq \emptyset, \quad (3.168)$$

$$W \cap F_4 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 26\} \neq \emptyset, \quad (3.169)$$

$$W \cap F_5 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{1, 2, 8\} \neq \emptyset, \quad (3.170)$$

$$W \cap F_6 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{20, 26\} \neq \emptyset, \quad (3.171)$$

$$W \cap F_j = \emptyset \implies j = 1. \quad (3.172)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.30a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 60.42% of T_c .

Fig. 3.31 illustrates the FDI results for diagnosis of a short-circuit fault in Q_2 . As shown in Fig. 3.31a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_2 is short circuited at $t_f = 0.5s$. In this situation, $v_A \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{25, 7, 1, 0, 1, 7, 25\}$. As it can be seen in Fig. 3.31b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

Figure 3.31: Experimental results of on-line diagnosis of a SCF in Q_2 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_2 . Hence, $J = 2$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (3.173)$$

$$W \cap F_2 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{\} = \emptyset, \quad (3.174)$$

$$W \cap F_3 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 1\} \neq \emptyset, \quad (3.175)$$

$$W \cap F_4 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{7, 25\} \neq \emptyset, \quad (3.176)$$

$$W \cap F_5 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 1, 7\} \neq \emptyset, \quad (3.177)$$

$$W \cap F_6 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{25\} \neq \emptyset, \quad (3.178)$$

$$W \cap F_j = \emptyset \implies j = 2. \quad (3.179)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.31a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 3.32 illustrates the FDI results for diagnosis of a short-circuit fault in Q_3 . As shown in Fig. 3.32a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_3 is short circuited at $t_f = 0.5s$. In this situation, $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{26, 8, 5, 3, 5, 8, 26\}$. As it can be seen in Fig. 3.32b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 3.32: Experimental results of on-line diagnosis of a SCF in Q_3 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_3 . Hence, $J = 3$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{3\} \neq \emptyset, \quad (3.180)$$

$$W \cap F_2 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{5, 8, 26\} \neq \emptyset, \quad (3.181)$$

$$W \cap F_3 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{\} = \emptyset, \quad (3.182)$$

$$W \cap F_4 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 26\} \neq \emptyset, \quad (3.183)$$

$$W \cap F_5 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{3, 5, 8\} \neq \emptyset, \quad (3.184)$$

$$W \cap F_6 = \{26, 8, 5, 3, 5, 8, 26\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{8, 26\} \neq \emptyset, \quad (3.185)$$

$$W \cap F_j = \emptyset \implies j = 3. \quad (3.186)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.32a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 3.33 illustrates the FDI results for diagnosis of a short-circuit fault in Q_4 . As shown in Fig. 3.33a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_4 is short circuited at $t_f = 0.5s$. In this situation, $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{23, 5, 2, 0, 2, 5, 23\}$. As it can be seen in Fig. 3.33b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 3.33: Experimental results of on-line diagnosis of a SCF in Q_4 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_4 . Hence, $J = 4$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (3.187)$$

$$W \cap F_2 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 5, 23\} \neq \emptyset, \quad (3.188)$$

$$W \cap F_3 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 2\} \neq \emptyset, \quad (3.189)$$

$$W \cap F_4 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{\} = \emptyset, \quad (3.190)$$

$$W \cap F_5 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 2, 5\} \neq \emptyset, \quad (3.191)$$

$$W \cap F_6 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{23\} \neq \emptyset, \quad (3.192)$$

$$W \cap F_j = \emptyset \implies j = 4. \quad (3.193)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.33a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 3.34 illustrates the FDI results for diagnosis of a short-circuit fault in Q_5 . As shown in Fig. 3.34a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_5 is short circuited at $t_f = 0.5s$. In this situation, $v_C \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{20, 26, 17, 11, 9, 11, 17\}$. As it can be seen in Fig. 3.34b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 3.34: Experimental results of on-line diagnosis of a SCF in Q_5 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_5 . Hence, $J = 5$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{9\} \neq \emptyset, \quad (3.194)$$

$$W \cap F_2 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} \quad (3.195)$$

$$= \{11, 17, 20, 26\} \neq \emptyset, \quad (3.196)$$

$$W \cap F_3 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{9, 11, 20\} \neq \emptyset, \quad (3.197)$$

$$W \cap F_4 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{17, 26\} \neq \emptyset, \quad (3.198)$$

$$W \cap F_5 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{\} = \emptyset, \quad (3.199)$$

$$W \cap F_6 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} \quad (3.200)$$

$$= \{20, 26\} \neq \emptyset, \quad (3.201)$$

$$W \cap F_j = \emptyset \implies j = 5. \quad (3.202)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.34a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 70.83% of T_c .

Fig. 3.35 illustrates the FDI results for diagnosis of a short-circuit fault in Q_6 . As shown in Fig. 3.35a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_6 is short circuited at $t_f = 0.5s$. In this situation, $v_C \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{17, 8, 2, 0, 2, 8, 17\}$. As it can be seen in Fig. 3.35b, the left face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

Figure 3.35: Experimental results of on-line diagnosis of a SCF in Q_6 with 27 states.

From Table. 3.6, it can be seen that this face of cube determines the FBZ of Q_6 . Hence, $J = 6$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (3.203)$$

$$W \cap F_2 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 8, 17\} \neq \emptyset, \quad (3.204)$$

$$W \cap F_3 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 2\} \neq \emptyset, \quad (3.205)$$

$$W \cap F_4 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 17\} \neq \emptyset, \quad (3.206)$$

$$W \cap F_5 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 2, 8\} \neq \emptyset, \quad (3.207)$$

$$W \cap F_6 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{\} = \emptyset, \quad (3.208)$$

$$W \cap F_j = \emptyset \implies j = 6. \quad (3.209)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 3.35a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

3.9 Summary

In this chapter the theory of VSP-based FDI for isolating short-circuit switch faults in the three-phase VSIs was described. The voltage states were defined based on the structural input–output model of the inverter. A set of states were introduces as the fault signature set for every faulty switch. The diagnosis was conducted by comparing a finite sequence of monitored non-equal adjacent switching states with the predefined fault signatures. The ability to locate a faulty switch in a six-switch inverter feeding a permanent magnet synchronous motor has been demonstrated. It has been shown that the fault diagnosis result is robust to the load changes and the variation of the PWM frequency. All six switch faults were isolated in about one switching period. The experimental set-up was described and the proposed method was validated through

experiments. Some modifications were done to reduce the fault detection time. As shown in Table 3.7, all the switch faults were isolated in less than one switching period using the modified approach.

Fault location (Q_j)	Diagnosis time (% T_c) obtain from	
	Unmodified Approach (8 states)	Modified approach (27 states)
Q_1	70.83	60.42
Q_2	158.33	95.83
Q_3	106.25	95.83
Q_4	131.25	95.83
Q_5	70.83	70.83
Q_6	131.25	95.83
Average FDI time	111.42	85.76

Table 3.7: Summary of fault diagnosis results obtained from experiments for short-circuit faults in Q_1 – Q_6 .

In the next chapter, the application of VSP-based FDI for open-circuit switch faults is discussed.

Chapter 4

VSP-based FDI for Open-Circuit Faults

4.1 Introduction

In this chapter, the VSP-based FDI is applied to diagnose the open-circuit faults in a six-switch the VSIs. The VSI is describes in Section 4.2. Section 4.3 explains the fault detection and isolation procedure. Section 4.4 depicts the simulation results. The experimental results are discussed in Section 4.5. The results validate that the proposed algorithm successfully isolates all switch faults in less than one switching period that is significantly faster than current-based conventional FDI methods.

4.2 System's Description

This section describes a three-phase pulsewidth modulated (PWM) voltage source inverter (VSI) with six switches. In the no-fault situation, the switches are fully controllable through their gates. When an open-circuit fault occurs in a switch, it become open and remain in this situation regardless of the gate control signal. Open-circuit switch faults do not cause short-circuit current, thus, they may remain undetected for a long time until a failure occurs in the load side. Therefore, the FDI of open-circuit faults is extremely vital to ensure maximum efficiency in the load and to prevent the catastrophic failures. Fig. 4.1 illustrates a VSI circuit with six identical switches, Q_i for $i = 1$ to 6. Gate control signals g_i control on–off state of Q_i ; for $g_i = 1$, Q_i is in the on

state and the switch conducts. On the other hand, when $g_i = 0$, Q_i is in the off state, and it does not conduct.

Figure 4.1: A Three-phase inverter.

Gate signals of two switches of one phase leg are complementary; for example, if $g_1 = 1$ then $g_2 = 0$ and Q_1 is closed, resulting in $v_A = +E_N$; conversely, if $g_1 = 0$ then $g_2 = 1$ and Q_2 is closed, resulting in $v_A = -E_N$, where E_N is a constant value proportional to the voltage of the dc source. Hence, the output voltage of each phase alternates regularly between two levels of voltage that forms a square wave. A control block determines the pulsewidth of the waveform. The input–output of the inverter can be described based on its switching states as shown in (4.1):

$$\mathbf{v}(t) := \mathbf{e} \cdot \mathbf{D}(t) \quad (4.1)$$

where $\mathbf{v}(t) = [v_C(t), v_B(t), v_A(t)]$, $\mathbf{e} = [E, E]$, and $\mathbf{D}$ is defined as

$$\mathbf{D}(t) := \begin{bmatrix} d_1(t) & d_3(t) & d_5(t) \\ d_2(t) & d_4(t) & d_6(t) \end{bmatrix}, \quad (4.2)$$

and

$$d_i(t) := \begin{cases} g_i(t) & \text{if } Q_i \text{ is healthy} \\ 0 & \text{if an open-circuit fault exists in } Q_i \end{cases}. \quad (4.3)$$

The switching states of the inverter are defined based on $\mathbf{D}$ as described the next section. The fault-banned zone of Q_j are a set of switching states that are not achievable in the presence of a fault in Q_j . In this section the fault-banned zones, $\mathbf{F}_j$, for open-circuit faults are calculated for two and three levels of voltage. FDI based on the two levels (8 states) is slightly slower than the one with 3 levels (27 states). However, it is useful for the cases where the faulty state of the inverter is unknown, i.e., the FDI is achieved only based on the healthy states.

4.3 Fault Detection and Isolation

In this section, the VSP-based FDI is applied for the open-circuit faults. This method as described in Section 3.2 is based on the structural model of the inverter. Knowing the model of the inverter in the faulty and healthy situations, the fault-banned zones are defined and the FDI procedure described in Section 3.4 is applied to detect and isolate the switch faults. The VSP-based fault diagnosis algorithm is described for unknown switching frequency; where access to the control signals is not possible or the switching frequency changes by the feedback loop. Suppose that the system is healthy at time t_0 and a fault will occur at $t_f > t_0$. The process contains two main stages; extracting switching states, and comparison of the observed states to the fault-banned zones.

4.3.1 Extracting Switching States

Fault diagnosis process commences by monitoring three phase voltages and extracting the corresponding switching states. Let

$$\mathbf{v}(t) = [v_C(t), v_B(t), v_A(t)] \quad (4.4)$$

be the vector of observed voltages from the detectors. A threshold span ε_m in the neighborhood of each normal voltage level E_N is defined, and the monitored voltage vector in this neighborhood is mapped to a known $\mathbf{v}_s$. The neighborhood of $\mathbf{v}_s$ is defined as

$$\mathbf{h}_s = \mathbf{v}_s \cdot \text{diag}(\varepsilon_C, \varepsilon_B, \varepsilon_A) \quad (4.5)$$

where ε_φ for $\varphi = A, B, C$ is the distance between $\mathbf{v}_s$ and $\mathbf{h}_s$ in each direction of the voltage space. Equation (4.6) defines a set of all voltages in the neighborhood of $\mathbf{v}_s$ within a distance of ε_m in each direction of the voltage space.

$$\mathbf{H}_s =: \{\mathbf{h}_s | \forall 1 - \varepsilon_m \leq \varepsilon_\varphi < 1 + \varepsilon_m\} \quad (4.6)$$

ε_m is selected such that both levels of voltage in the faulty situation, v^u and v^l , are isolable, e.g., $\varepsilon_m = 0.15$.

From definition (4.1), there exists a one-to-one correspondence between $\mathbf{v}_s$ and s . Thus, any observed voltage vector $\mathbf{v}(t)$ can be mapped to a known state, κ .

$$s(t) := \begin{cases} \kappa, & \text{if } \mathbf{v}(t) \in \mathbf{H}_\kappa \\ s(t^-) & \text{otherwise.} \end{cases} \quad (4.7)$$

4.3.2 Fault detection and Isolation

Based on the model of the SPWM inverter, if the phase voltages are monitored for a period of T_c , the value of all phase voltages will definitely change from one level to another one. Therefore, the voltage space pattern will not remain inside one face of the cubic pattern for $t_w = t_0 - T_c$. Thus, if non of the monitored states were a subset of F_j , an open-circuit fault in Q_j is diagnosed. The fault-banned zones are defined in Section 4.3.3 and 4.3.3 for an open-circuit fault in Q_j where $j = 1$ to 6.

4.3.3 Fault-banned Zones based on 8 states

In (4.8), the switching states are defined based on the state of the upper switches of the inverter, $\mathbf{u}$.

$$s(t) := \mathbf{u} \cdot \mathbf{b}, \quad (4.8)$$

where

$$\mathbf{b} := [1 \ 2 \ 4]^T, \quad (4.9)$$

and

$$\mathbf{u} := [1 \ 0] \cdot \mathbf{D}(t). \quad (4.10)$$

In the other word, s is the decimal value of the first row of $\mathbf{D}$. By this definition, (4.8) assigns a unique number for each switching state of the inverter. In the no-fault situation, the states of the upper switches and lower switches of each phase leg are complementary. Thus, we can also calculate the switching state based on the second row of $\mathbf{D}$. The difference between the states which are calculated based on the upper row which the one calculated with the lower ro determines the fault banned zones. Let

$$\mathbf{l} := [0 \ 1] \cdot \mathbf{D}(t), \quad (4.11)$$

and

$$\mathbf{u} = [1 \ 1 \ 1] - \mathbf{1}. \quad (4.12)$$

by applying $\mathbf{u}$ in (4.8)

$$\tilde{s}(t) := ([1 \ 1 \ 1] - \mathbf{1}) \cdot \mathbf{b}. \quad (4.13)$$

In the no-fault situation, $\tilde{s}(t) = s(t)$. However, in the presence of a faulty switch $\tilde{s}(t)$ can be different from $s(t)$. This difference is used to define fault-banned zones,

$$\mathbf{F}_j := \mathbf{Y}_j^u \cup \mathbf{Y}_j^l - \mathbf{Y}_j^u \cap \mathbf{Y}_j^l. \quad (4.14)$$

In (4.14), $\mathbf{Y}_j^u$ and $\mathbf{Y}_j^l$ are two sets of all possible $s(t)$ and $\tilde{s}(t)$ that can be obtained in the presence of a open-circuit fault in Q_j

$$\mathbf{Y}_j^u = \{s(t) | d_j(t) = 0, \forall g_i(t) \in \{0, 1\}\}$$

and

$$\mathbf{Y}_j^l = \{\tilde{s}(t) | d_j(t) = 0, \forall g_i(t) \in \{0, 1\}\}.$$

Table 4.1 shows the FBZs for open-circuit faults in six different locations. The FBZ indicates a face of the cubic pattern in the voltage space.

Table 4.1: Fault-banned zones of open-circuit faults using 8 states.

Open-circuit fault location (Q_j)	Fault-banned zone (F_j)
Q_1	$\{1, 3, 5, 7\}$
Q_2	$\{0, 2, 4, 6\}$
Q_3	$\{2, 3, 6, 7\}$
Q_4	$\{0, 1, 4, 5\}$
Q_5	$\{4, 5, 6, 7\}$
Q_6	$\{0, 1, 2, 3\}$

4.3.4 Fault-banned Zones based on 27 states

If the voltage level in the faulty situation is known, e.g., for a two switch inverter, if both switches are open at the same time, the output voltage is equal to zero. Thus, the switching state of the inverter at a given time t is defined as

$$s(t) := \mathbf{u} \cdot \mathbf{b} \quad (4.15)$$

where

$$\mathbf{b} := [1 \ 3 \ 9]^T, \quad (4.16)$$

and

$$\mathbf{u} := [1 \ -1] \cdot \mathbf{D}(t) + [1 \ 1 \ 1]. \quad (4.17)$$

For $d_i \in \{0, 1\}$, $s(t) \in \mathbf{S}_N$, where

$$\mathbf{S}_N = \{0, 1, 2, \dots, 25, 26\} \quad (4.18)$$

is the set of all normal and faulty states. With this definition, three levels of voltage have been used for a two level inverter, i.e, two healthy levels and one faulty level of voltage have been considered. Consider an open-circuit fault in Q_1 . From (4.3),

$$\mathbf{D}(t) := \begin{bmatrix} 0 & d_3(t) & d_5(t) \\ d_2(t) & d_4(t) & d_6(t) \end{bmatrix} \quad (4.19)$$

Thus, for $d_i \in \{0, 1\}$, $s(t) \in \mathbf{S}_1$, where

$$\mathbf{S}_1 = \{0, 1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 16, 18, 19, 21, 22, 24, 25\} \quad (4.20)$$

is the set of all states that may be observed in presence of an open-circuit fault in Q_1 . F_1 , fault-banned zone of Q_1 , is defined as a set of states that definitely will not be observed in presence of an open-circuit fault in Q_1 ,

$$F_1 := \mathbf{S}_N - \mathbf{S}_1 = \{2, 5, 8, 11, 14, 17, 20, 23, 26\}. \quad (4.21)$$

Similarly, the fault-banned zone for an open-circuit fault in Q_j is determined by a set of states, F_j , where,

$$\mathbf{F}_j := \mathbf{S}_N - \mathbf{S}_j, \quad (4.22)$$

and

$$\mathbf{S}_N = \{s | d_i \in \{0, 1\}, 1 \leq i \leq 6\}, \quad (4.23)$$

$$\mathbf{S}_j = \{s | d_j \in \{0\}, d_i \in \{0, 1\} \forall 1 \leq i \leq 6, i \neq j\}. \quad (4.24)$$

In (4.22), $\mathbf{Y}_j^u$ and $\mathbf{Y}_j^l$ are two sets of all possible $s(t)$ and $\tilde{s}(t)$ that can be obtained in the presence of a open-circuit fault in Q_j

$$\mathbf{Y}_j^u = \{s(t) | d_j(t) = 0, \forall g_i(t) \in \{0, 1\}\}$$

and

$$\mathbf{Y}_j^l = \{\tilde{s}(t) | d_j(t) = 0, \forall g_i(t) \in \{0, 1\}\}.$$

Table 4.2 shows the FBZs for open-circuit faults in six different locations. The FBZ indicates a face of the cubic pattern in the voltage space.

Table 4.2: Fault-banned zones for open-circuit faults with 27 states.

Open-circuit fault location (Q_j)	Fault-banned zone (F_j)
Q_1	$\{2, 5, 8, 11, 14, 17, 20, 23, 26\}$
Q_2	$\{0, 3, 6, 9, 12, 15, 18, 21, 24\}$
Q_3	$\{6, 7, 8, 15, 16, 17, 24, 25, 26\}$
Q_4	$\{0, 1, 2, 9, 10, 11, 18, 19, 20\}$
Q_5	$\{18, 19, 20, 21, 22, 23, 24, 25, 26\}$
Q_6	$\{0, 1, 2, 3, 4, 5, 6, 7, 8\}$

4.4 Simulations

Fig. 4.2 depicts the simulation model for FDI of the open circuit faults of a three-phase inverter. The model includes the SPWM control, fault insertion, and fault diagnosis blocks. The three-phase inverter is illustrated in Fig. 4.3. In the simulations, $F_c = 16.7\text{K Hz}$, $F_r = 55.6\text{ Hz}$, and $T_s = 2.5\mu\text{s}$. Fig. 4.4a illustrates the simulation results of diagnosis an open-circuit fault in Q_1 . The first three diagrams show the pole voltage signals. The switching states are extracted from the pole voltages and illustrated in the forth diagram. The transition patterns in the voltage state is illustrated in Fig. 4.4b. The seven last non-equal adjacent switching states does not touch the right face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_1 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $100.00\%T_c$.

Figure 4.2: Simulink model for FDI of open-circuit faults in a three-phase inverter.

Figure 4.3: Simulink model of the three-phase inverter.

(a) Time domain results.

(b) VSP.

 Figure 4.4: Simulation results of diagnosis of an OCF in Q_1 .

Fig. 4.5a illustrates the simulation results of diagnosis an open-circuit fault in Q_2 . The first three diagrams show the pole voltage signals. The switching states are extracted from the pole voltages and illustrated in the forth diagram. The transition patterns in the voltage state is illustrated in Fig. 4.5b. The seven last non-equal adjacent switching states does not touch the left face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_2 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $66.77\%T_c$.

(a) Time domain results.

(b) VSP.

 Figure 4.5: Simulation results of diagnosis of an OCF in Q_2 .

Fig. 4.6a illustrates the simulation results of diagnosis an open-circuit fault in Q_3 . The first three diagrams show the pole voltage signals. The switching states were extracted from the pole voltages and illustrated in the forth diagram. The transition patterns in the voltage state is illustrated in Fig. 4.6b.

(a) Time domain results.

(b) VSP.

 Figure 4.6: Simulation results of diagnosis of an OCF in Q_3 .

The seven last non-equal adjacent switching states does not touch the back face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_3 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $100\%T_c$.

Fig. 4.7a illustrates the simulation results of diagnosis an open-circuit fault in Q_4 . The first three diagrams show the pole voltage signals. The switching states are extracted from the pole voltages and illustrated in the forth diagram. The transition pat-

terns in the voltage state is illustrated in Fig. 4.7b. The seven last non-equal adjacent switching states does not touch the front face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_4 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $100\%T_C$.

(a) Time domain results.

(b) VSP.

Figure 4.7: Simulation results of diagnosis of an OCF in Q_4 .

Fig. 4.8a illustrates the simulation results of diagnosis an open-circuit fault in Q_5 . The first three diagrams show the pole voltage signals. The switching states are extracted from the pole voltages and illustrated in the forth diagram. The transition pat-

terns in the voltage state is illustrated in Fig. 4.8b. The seven last non-equal adjacent switching states does not touch the top face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_5 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $100\%T_c$.

(a) Time domain results.

(b) VSP.

Figure 4.8: Simulation results of diagnosis of an OCF in Q_5 .

Fig. 4.9a illustrates the simulation results of diagnosis an open-circuit fault in Q_6 . The first three diagrams show the pole voltage signals. The switching states are extracted from the pole voltages and illustrated in the forth diagram. The transition pat-

terns in the voltage state is illustrated in Fig. 4.9b. The seven last non-equal adjacent switching states does not touch the bottom face of the cube in the voltage space. Comparing to the fault-banned zone of Table 4.2, Q_6 is diagnosed as the faulty switch. As soon as the fault is diagnosed, the gate-misfiring fault is cleared and normal gate signals are applied to the inverter. In this experiment, the fault is isolated in $50\%T_c$.

(a) Time domain results.

(b) VSP.

Figure 4.9: Simulation results of diagnosis of an OCF in Q_6 .

As shown by simulations, all of the open-circuit faults were successfully diagnosed within only one switching period ($T_c \approx 60\mu$ s). In the next section, the experimental results of diagnosis pen circuit faults are shown.

4.5 Experiments

The experiments were done using the experimental set-up which was described in Section 3.6. In each experiment, one of the six switches was open circuited by the programmed software. The desired fault location and the fault insertion time was given by the user. The open-circuit fault was inserted as a gate misfiring fault, i.e.,

$$G_j(t > t_j) = 0. \quad (4.25)$$

The Fault Diagnosis block implements the VSP-based FDI algorithm to derive the non-equal adjacent switching states and diagnose the open-circuit faults. The results are shown as follow.

4.5.1 Experimental Results using 8 states

Fig. 4.10 illustrates the FDI results for diagnosis of an open-circuit fault in Q_1 . As shown in Fig. 4.10a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_1 is open-circuited at $t_f = 0.5s$. Thus, $v_A \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{0, 2, 6, 2, 0, 2\}$. As it can be seen in Fig. 4.10b, the right face of the cube is not touched by the members of W . From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_1 . Hence, $J = 1$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{0, 2, 6, 2, 0, 2\} \cap \{1, 3, 5, 7\} = \{\} = \emptyset, \quad (4.26)$$

$$W \cap F_2 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 2, 4, 6\} = \{0, 2, 6\} \neq \emptyset, \quad (4.27)$$

$$W \cap F_3 = \{0, 2, 6, 2, 0, 2\} \cap \{2, 3, 6, 7\} = \{2, 6\} \neq \emptyset, \quad (4.28)$$

$$W \cap F_4 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 4, 5\} = \{0\} \neq \emptyset, \quad (4.29)$$

$$W \cap F_5 = \{0, 2, 6, 2, 0, 2\} \cap \{4, 5, 6, 7\} = \{6\} \neq \emptyset, \quad (4.30)$$

$$W \cap F_6 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 2, 3\} = \{0, 2\} \neq \emptyset, \quad (4.31)$$

$$W \cap F_j = \emptyset \implies j = 1. \quad (4.32)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram of Fig. 4.10a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 158.33% of T_c .

(a) Time domain results.

(b) VSP.

Figure 4.10: Experimental results of on-line diagnosis of a OCF in Q_1 with 8 states.

Fig. 4.11 illustrates the FDI results for diagnosis of an open-circuit fault in Q_2 . As shown in Fig. 4.11a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_2 is open-circuited at $t_f = 0.5s$. Thus, $v_A \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure.

(a) Time domain results.

(b) VSP.

Figure 4.11: Experimental results of on-line diagnosis of a OCF in Q_2 with 8 states.

The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{0, 2, 6, 2, 0, 2\}$. As it can be seen in Fig. 4.11b, the left face of the cube is not touched by the members of W . From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_2 . Hence, $J = 2$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{0, 2, 6, 2, 0, 2\} \cap \{1, 3, 5, 7\} = \{\} = \emptyset, \quad (4.33)$$

$$W \cap F_2 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 2, 4, 6\} = \{0, 2, 6\} \neq \emptyset, \quad (4.34)$$

$$W \cap F_3 = \{0, 2, 6, 2, 0, 2\} \cap \{2, 3, 6, 7\} = \{2, 6\} \neq \emptyset, \quad (4.35)$$

$$W \cap F_4 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 4, 5\} = \{0\} \neq \emptyset, \quad (4.36)$$

$$W \cap F_5 = \{0, 2, 6, 2, 0, 2\} \cap \{4, 5, 6, 7\} = \{6\} \neq \emptyset, \quad (4.37)$$

$$W \cap F_6 = \{0, 2, 6, 2, 0, 2\} \cap \{0, 1, 2, 3\} = \{0, 2\} \neq \emptyset, \quad (4.38)$$

$$W \cap F_j = \emptyset \implies j = 2. \quad (4.39)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram of Fig. 4.11a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 158.33% of T_c .

Fig. 4.12 illustrates the FDI results for diagnosis of an open-circuit fault in Q_3 . As shown in Fig. 4.12a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_3 is open-circuited at $t_f = 0.5s$. Thus, $v_B \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{1, 0, 1, 5, 1, 0\}$. As it can be seen in Fig. 4.12b, the back face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 4.12: Experimental results of on-line diagnosis of a OCF in Q_3 with 8 states.

From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_3 . Hence, $J = 3$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{1, 0, 1, 5, 1, 0\} \cap \{1, 3, 5, 7\} = \{1, 5\} \neq \emptyset, \quad (4.40)$$

$$W \cap F_2 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 2, 4, 6\} = \{0\} \neq \emptyset, \quad (4.41)$$

$$W \cap F_3 = \{1, 0, 1, 5, 1, 0\} \cap \{2, 3, 6, 7\} = \{\} = \emptyset, \quad (4.42)$$

$$W \cap F_4 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 1, 4, 5\} = \{0, 1, 5\} \neq \emptyset, \quad (4.43)$$

$$W \cap F_5 = \{1, 0, 1, 5, 1, 0\} \cap \{4, 5, 6, 7\} = \{5\} \neq \emptyset, \quad (4.44)$$

$$W \cap F_6 = \{1, 0, 1, 5, 1, 0\} \cap \{0, 1, 2, 3\} = \{0, 1\} \neq \emptyset, \quad (4.45)$$

$$W \cap F_j = \emptyset \implies j = 3. \quad (4.46)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram of Fig. 4.12a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 131.25% of T_c .

Fig. 4.13 illustrates the FDI results for diagnosis of an open-circuit fault in Q_4 . As shown in Fig. 4.13a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_4 is open-circuited at $t_f = 0.5s$. Thus, $v_B \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{7, 3, 2, 3, 7, 3\}$. As it can be seen in Fig. 4.13b, the front face of the cube is not touched by the members of W . From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_4 . Hence, $J = 4$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{7, 3, 2, 3, 7, 3\} \cap \{1, 3, 5, 7\} = \{3, 7\} \neq \emptyset, \quad (4.47)$$

$$W \cap F_2 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 2, 4, 6\} = \{2\} \neq \emptyset, \quad (4.48)$$

$$W \cap F_3 = \{7, 3, 2, 3, 7, 3\} \cap \{2, 3, 6, 7\} = \{2, 3, 7\} \neq \emptyset, \quad (4.49)$$

$$W \cap F_4 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 1, 4, 5\} = \emptyset, \quad (4.50)$$

$$W \cap F_5 = \{7, 3, 2, 3, 7, 3\} \cap \{4, 5, 6, 7\} = \{7\} \neq \emptyset, \quad (4.51)$$

$$W \cap F_6 = \{7, 3, 2, 3, 7, 3\} \cap \{0, 1, 2, 3\} = \{2, 3\} \neq \emptyset, \quad (4.52)$$

$$W \cap F_j = \emptyset \implies j = 4. \quad (4.53)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram

of Fig. 4.13a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 106.25% of T_C .

(a) Time domain results.

(b) VSP.

Figure 4.13: Experimental results of on-line diagnosis of a OCF in Q_4 with 8 states.

Fig. 4.14 illustrates the FDI results for diagnosis of an open-circuit fault in Q_5 . As shown in Fig. 4.14a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In

this experiment, Q_5 is open-circuited at $t_f = 0.5s$. Thus, $v_C \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e., $W = \{3, 1, 0, 1, 3, 2\}$. As it can be seen in Fig. 4.14b, the top face of the cube is not touched by the members of W . From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_5 . Hence, $J = 5$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{3, 1, 0, 1, 3, 2\} \cap \{1, 3, 5, 7\} = \{1, 3\} \neq \emptyset, \quad (4.54)$$

$$W \cap F_2 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 2, 4, 6\} = \{0, 2\} \neq \emptyset, \quad (4.55)$$

$$W \cap F_3 = \{3, 1, 0, 1, 3, 2\} \cap \{2, 3, 6, 7\} = \{2, 3\} \neq \emptyset, \quad (4.56)$$

$$W \cap F_4 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 1, 4, 5\} = \{0, 1\} \neq \emptyset, \quad (4.57)$$

$$W \cap F_5 = \{3, 1, 0, 1, 3, 2\} \cap \{4, 5, 6, 7\} = \{\} = \emptyset, \quad (4.58)$$

$$W \cap F_6 = \{3, 1, 0, 1, 3, 2\} \cap \{0, 1, 2, 3\} = \{0, 1, 2, 3\} \neq \emptyset, \quad (4.59)$$

$$W \cap F_j = \emptyset \implies j = 5. \quad (4.60)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram of Fig. 4.14a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 131.25% of T_c .

(a) Time domain results.

(b) VSP.

 Figure 4.14: Experimental results of on-line diagnosis of a OCF in Q_5 with 8 states.

Fig. 4.15 illustrates the FDI results for diagnosis of an open-circuit fault in Q_6 . As shown in Fig. 4.15a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_6 is open-circuited at $t_f = 0.5s$. Thus, $v_C \approx 0V$ for the instances when both switches of the faulty phase are open. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last six non-equal adjacent switching states, i.e.,

$W = \{0, 2, 6, 2, 0, 2\}$. As it can be seen in Fig. 4.15b, the bottom face of the cube is not touched by the members of W . From Table. 4.1, it can be seen that this face of cube determines the FBZ of Q_6 . Hence, $J = 6$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{5, 7, 5, 4, 5, 7\} \cap \{1, 3, 5, 7\} = \{5, 7\} \neq \emptyset, \quad (4.61)$$

$$W \cap F_2 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 2, 4, 6\} = \{4\} \neq \emptyset, \quad (4.62)$$

$$W \cap F_3 = \{5, 7, 5, 4, 5, 7\} \cap \{2, 3, 6, 7\} = \{7\} \neq \emptyset, \quad (4.63)$$

$$W \cap F_4 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 1, 4, 5\} = \{4, 5\} \neq \emptyset, \quad (4.64)$$

$$W \cap F_5 = \{5, 7, 5, 4, 5, 7\} \cap \{4, 5, 6, 7\} = \{4, 5, 7\} \neq \emptyset, \quad (4.65)$$

$$W \cap F_6 = \{5, 7, 5, 4, 5, 7\} \cap \{0, 1, 2, 3\} = \{\} = \emptyset, \quad (4.66)$$

$$W \cap F_j = \emptyset \implies j = 6. \quad (4.67)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter. Thus, the width of the pulse in the forth diagram of Fig. 4.15a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 70.83% of T_c . The maximum sampling time was selected based on (3.118),

$$T_{s(Max)} = (1 - M) \frac{T_c}{4} = 11e - 4s.$$

In these experiments, the sampling time was selected $T_s = 4.6296e - 4s$, MATLAB could not perform well for the smaller sampling times.

(a) Time domain results.

(b) VSP.

 Figure 4.15: Experimental results of on-line diagnosis of a OCF in Q_6 with 8 states.

Table 4.3 summarizes the fault diagnosis time for all of the six experiments using eight states. The diagnosis time varies based on the fault insertion time. However, it is limited to a time equal to six non-equal adjacent switching states which is approximately equal to one switching period. In these experiments, the average diagnosis time is 111% of the switching period. In these experiments $F_r = 7.5\text{Hz}$, $F_c = 45.0003\text{Hz}$, $T_c = 0.0222\text{s}$, and $T_r = 0.1333\text{s}$. The sampling time $T_s = 4.6296e - 04$, and

$M = 0.8$.

Table 4.3: Summary of fault diagnosis results obtained from experiments for open-circuit faults in Q_1 – Q_6 using unmodified approach with 8 states.

Fault location (Q_j)	Diagnosis time for OCF (% T_c)
Q_1	158.33
Q_2	70.83
Q_3	131.25
Q_4	106.25
Q_5	131.25
Q_6	70.83
Average FDI time	111.42

4.5.2 Experimental Results using 27 states

In order to decrease the fault diagnosis time to even a shorter time, a new level of voltage is considered in the digitalization stage. Hence, three levels of voltage has been considered which results in $3^3 = 27$ states in the voltage space. Only eight states are the healthy ones and the rest belong to the faulty situations. Fig. 4.16 illustrates the FDI results for diagnosis of an open-circuit fault in Q_1 . As shown in Fig. 4.16a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_1 is open-circuited at $t_f = 0.5s$. The faulty situation is indicate by $v_A \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{25, 7, 1, 0, 1, 7, 25\}$. As it can be seen in Fig. 4.16b, the right face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

 Figure 4.16: Experimental results of on-line diagnosis of a OCF in Q_1 with 27 states.

From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_1 . Hence, $J = 1$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{\} = \emptyset, \quad (4.68)$$

$$W \cap F_2 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (4.69)$$

$$W \cap F_3 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{7, 5\} \neq \emptyset, \quad (4.70)$$

$$W \cap F_4 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 1\} \neq \emptyset, \quad (4.71)$$

$$W \cap F_5 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{25\} \neq \emptyset, \quad (4.72)$$

$$W \cap F_6 = \{25, 7, 1, 0, 1, 7, 25\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 1, 7\} \neq \emptyset, \quad (4.73)$$

$$W \cap F_j = \emptyset \implies j = 1. \quad (4.74)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.16a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 4.17 illustrates the FDI results for diagnosis of an open-circuit fault in Q_2 . As shown in Fig. 4.17a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_2 is open-circuited at $t_f = 0.5s$. The faulty situation is indicate by $v_A \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{2, 20, 26, 8, 2, 1, 2\}$. As it can be seen in Fig. 4.17b, the left face of the cube is not touched by the members of W .

From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_2 . Hence, $J = 2$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_2 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 8, 20, 26\} \neq \emptyset, \quad (4.75)$$

$$W \cap F_2 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{\} = \emptyset, \quad (4.76)$$

$$W \cap F_3 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 26\} \neq \emptyset, \quad (4.77)$$

$$W \cap F_4 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{1, 2, 20\} \neq \emptyset, \quad (4.78)$$

$$W \cap F_5 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{20, 26\} \neq \emptyset, \quad (4.79)$$

$$W \cap F_6 = \{2, 20, 26, 8, 2, 1, 2\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{1, 2, 8\} \neq \emptyset, \quad (4.80)$$

$$W \cap F_j = \emptyset \implies j = 2. \quad (4.81)$$

(a) Time domain results.

(b) VSP.

 Figure 4.17: Experimental results of on-line diagnosis of a OCF in Q_2 with 27 states.

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.17a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 60.42% of T_c .

Fig. 4.18 illustrates the FDI results for diagnosis of an open-circuit fault in Q_3 . As

shown in Fig. 4.18a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_3 is open-circuited at $t_f = 0.5s$. The faulty situation is indicate by $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{23, 5, 2, 0, 2, 5, 23\}$.

As it can be seen in Fig. 4.18b, the back face of the cube is not touched by the members of W . From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_3 . Hence, $J = 3$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 5, 23\} \neq \emptyset, \quad (4.82)$$

$$W \cap F_2 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (4.83)$$

$$W \cap F_3 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{\} = \emptyset, \quad (4.84)$$

$$W \cap F_4 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 2\} \neq \emptyset, \quad (4.85)$$

$$W \cap F_5 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{23\} \neq \emptyset, \quad (4.86)$$

$$W \cap F_6 = \{23, 5, 2, 0, 2, 5, 23\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 2, 5\} \neq \emptyset, \quad (4.87)$$

$$W \cap F_j = \emptyset \implies j = 3. \quad (4.88)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.18a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

(a) Time domain results.

(b) VSP.

 Figure 4.18: Experimental results of on-line diagnosis of a OCF in Q_3 with 27 states.

Fig. 4.19 illustrates the FDI results for diagnosis of an open-circuit fault in Q_4 . As shown in Fig. 4.19a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_4 is open-circuited at $t_f = 0.5s$. The faulty situation is indicate by $v_B \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{28, 8, 5, 3, 5, 8, 26\}$.

(a) Time domain results.

(b) VSP.

 Figure 4.19: Experimental results of on-line diagnosis of a OCF in Q_4 with 27 states.

As it can be seen in Fig. 4.19b, the front face of the cube is not touched by the members of W . From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_4 . Hence, $J = 4$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{5, 8, 26\} \neq \emptyset, \quad (4.89)$$

$$W \cap F_2 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{3\} \neq \emptyset, \quad (4.90)$$

$$W \cap F_3 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 26\} \neq \emptyset, \quad (4.91)$$

$$W \cap F_4 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{\} = \emptyset, \quad (4.92)$$

$$W \cap F_5 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{26\} \neq \emptyset, \quad (4.93)$$

$$W \cap F_6 = \{28, 8, 5, 3, 5, 8, 26\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{3, 5, 8\} \neq \emptyset, \quad (4.94)$$

$$W \cap F_j = \emptyset \implies j = 4. \quad (4.95)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.19a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 4.20 illustrates the FDI results for diagnosis of an open-circuit fault in Q_5 . As shown in Fig. 4.20a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_5 is open-circuited at $t_f = 0.5s$. The faulty situation is indicate by $v_C \approx 0$. The switching states are calculated and shown in the forth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{17, 8, 2, 0, 2, 8, 17\}$. As it can be seen in Fig. 4.20b, the top face of the cube is not touched by the members of W . From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_5 . Hence, $J = 5$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} = \{2, 8, 17\} \neq \emptyset, \quad (4.96)$$

$$W \cap F_2 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{0\} \neq \emptyset, \quad (4.97)$$

$$W \cap F_3 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{8, 17\} \neq \emptyset, \quad (4.98)$$

$$W \cap F_4 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{0, 2\} \neq \emptyset, \quad (4.99)$$

$$W \cap F_5 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} = \{\} = \emptyset, \quad (4.100)$$

$$W \cap F_6 = \{17, 8, 2, 0, 2, 8, 17\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{0, 2, 8\} \neq \emptyset, \quad (4.101)$$

$$W \cap F_j = \emptyset \implies j = 5. \quad (4.102)$$

(a) Time domain results.

(b) VSP.

 Figure 4.20: Experimental results of on-line diagnosis of a OCF in Q_5 with 27 states.

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.20a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 95.83% of T_c .

Fig. 4.21 illustrates the FDI results for diagnosis of an open-circuit fault in Q_6 . As

shown in Fig. 4.21a, v_A , v_B , and v_C , fluctuates between $v \approx \pm 5V$ for $t < 0.5s$. In this experiment, Q_6 is open-circuited at $t_f = 0.5s$. The faulty situation is indicated by $v_C \approx 0$. The switching states are calculated and shown in the fourth diagram of this figure. The fault detection window at the detection time consists of the last seven non-equal adjacent switching states, i.e., $W = \{20, 26, 17, 11, 9, 11, 17\}$. As it can be seen in Fig. 4.21b, the bottom face of the cube is not touched by the members of W .

(a) Time domain results.

(b) VSP.

Figure 4.21: Experimental results of on-line diagnosis of a OCF in Q_6 with 27 states.

From Table. 4.2, it can be seen that this face of cube determines the FBZ of Q_6 . Hence, $J = 6$ is diagnosed by comparing W to the FBZs, i.e.,

$$W \cap F_1 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{2, 5, 8, 11, 14, 17, 20, 23, 26\} \quad (4.103)$$

$$= \{11, 17, 20, 26\} \neq \emptyset, \quad (4.104)$$

$$W \cap F_2 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 3, 6, 9, 12, 15, 18, 21, 24\} = \{9\} \neq \emptyset, \quad (4.105)$$

$$W \cap F_3 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{6, 7, 8, 15, 16, 17, 24, 25, 26\} = \{17, 26\} \neq \emptyset, \quad (4.106)$$

$$W \cap F_4 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 1, 2, 9, 10, 11, 18, 19, 20\} = \{9, 11, 20\} \neq \emptyset, \quad (4.107)$$

$$W \cap F_5 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{18, 19, 20, 21, 22, 23, 24, 25, 26\} \quad (4.108)$$

$$= \{20, 26\} \neq \emptyset, \quad (4.109)$$

$$W \cap F_6 = \{20, 26, 17, 11, 9, 11, 17\} \cap \{0, 1, 2, 3, 4, 5, 6, 7, 8\} = \{\} = \emptyset, \quad (4.110)$$

$$W \cap F_j = \emptyset \implies j = 6. \quad (4.111)$$

As soon as the faulty switch was diagnosed, the fault is cleared by applying the normal gate signals to the inverter to protect the devices. Thus, the width of the pulse in the forth diagram of Fig. 4.21a indicated the fault diagnosis time, and the amplitude of it determines the location of the faulty switch. In this experiment, the diagnosis time is equal to 70.83% of T_c .

Table 4.4 summarizes the fault diagnosis time for all of the 6 experiments using 27 states. As it can be seen from the experimental results, all of the open-circuit switch faults were successfully diagnosed within only one switching period.

Table 4.4: Summary of fault diagnosis results obtained from experiments for open-circuit faults in Q_1 – Q_6 using modified approach with 27 states.

Fault location (Q_j)	Diagnosis time for OCF (% T_c)
Q_1	95.83
Q_2	60.42
Q_3	95.83
Q_4	95.83
Q_5	95.83
Q_6	70.83
Average FDI time	70.83

4.6 Summary

In this chapter, the VSP-based FDI method for open-circuit faults was described. Fault-banned zones for the open-circuit switch faults were defined. Simulations and experiments were carried out for a six-switch inverter and all of the switch faults were successfully isolated with the VSP-based FDI method. It has been shown that the VSP-based FDI method successfully isolates the open-circuit switch faults in less than one carrier period of the SPWM signal which is significantly faster than the conventional methods.

Chapter 5

Fault Diagnosis for Multi-Level Inverters

5.1 Introduction

This chapter presents a FDI method for diagnosis of short-circuit switch faults in m -phase n -level cascade inverters based on the measurement of pole voltages of each phase leg of the inverter. A brief introduction of FDI for multi-level inverters is discussed in Section 5.2. Section 5.3 proposes an input–output model of an n -level m -phase inverter. The SPWM control of the multi-level inverter is described in Section 5.4. The procedure of FDI is described in Section 5.5.

5.2 Background

The concept of multi-level inverters (MLIs) was first introduced in the early 70's [90]. Instead of connecting a high power dc source to a central inverter with high rating switches (Fig. 5.1a), several full bridge (FB) inverters with lower voltage sources can be cascaded to generate the same level of output voltage. In this case, lower rate, lower cost switches can be used and a more efficient MPPT control for the PV or wind power systems is possible [91]. The quality of the ac output can also be improved through amplitude modulation (AM) techniques [37]. Low switching frequency can be used and in the meantime the THD can be reduced. In general, the switch losses are reduced and the efficiency and quality of the power conversion is improved by using

MLIs. MLIs well suit today's requirements of solar power systems. Each solar panels can be connected to an individual dc-ac module as shown in Fig. 5.1b.

(a) Solar modules with central Inverter

(b) Solar modules with micro-inverters

Figure 5.1: Central inverters versus micro-inverters for solar energy conversion.

These modules can be cascaded in a multi-level topology to generate high level ac voltage in the output. The MLIs are more probable to fail because of existence of numerous switches in the circuit. Therefore, the reliability of MLI is a big concern. Fortunately, there exist duplicate switching states in the MLI which bring sufficient degree of freedom to tolerate the internal fault conditions [92]. Naturally, the switch faults occur and propagate very fast that bring several challenges in having a practical and reliable FTC [92]. The prerequisite of the fault tolerant control is fast and accurate FDI [92].

Different MLI topologies and their industrial applications in PV, wind power, marine propulsion, train traction, automotive applications, regenerative conveyors, class D amplifiers, hydropump storage, flexible ac transmission systems (FACTS), distributed generations, active filters, static compensators (STATCOM), dynamic voltage restorers (DVRs), unified power flow controllers (UPFCs), and unified power quality conditioners were studied in [92]. Liu *et al.* review fault diagnosis and tolerant control methods for modular multilevel converters (MMCs) in high voltage direct current (HVDC)

systems [93]. Multiple open-circuit fault detection and fault tolerant methods for the 3-level 3-phase neutral point clamped (NPC) active rectifier have been addressed in [94]. Boettcher *et al.* evaluate fault-tolerant 3L-NPC based back-to-back converter topologies for wind turbine systems (WTS) [95]. Ribeiro *et al.* presented a fault diagnosis and tolerant reconfiguration for a three-level boost converter in a PV power system [96].

In the spite of energy conversion systems, motor drives also benefit from MLIs in VSDs. Fault diagnosis and FTC of electrical machines and drives are reported to be the future research focus in this field [33]. FDI and FTC for electrical hybrid systems is reported in [97] and [98]. Several FDI methods have been used in the literature to diagnose faulty semiconductor switches in the MLIs. These methods include Park's vector, normalized dc current, slope method, wavelet, fuzzy, and NNs. The majority of these methods only detect the faulty arm [93]. However, the exact location of the faulty switch is needed for an accurate and successful FTC.

5.3 Modeling the n -level m -phase Inverter

A multi-level inverter is a type of dc–ac converters which generates an ac waveform by converting dc voltage to a staircase waveform. Figure 5.2 illustrates a cascade n -level m -phase inverter. As it is shown in this figure, the basic module of a MLI is a HB inverter. Each HB inverter consists of two switches and adds a level of voltage to the output with amplitude v_{bk} where v_{bk} is the dc source connected to the k^{th} HB inverter. In each phase leg,

$$N = n - 1 \quad (5.1)$$

HB inverter exist. Thus,

$$q = 2N \quad (5.2)$$

switches are in each phase leg. These switches are controlled such that n levels of voltage are achieved in the output of each phase. For an n -level inverter $2n - 1$ levels are defined that contain all healthy and faulty levels, i.e., for $Z_\phi \in \mathbb{N}_0, Z_\phi \leq 2N$,

$$L_\phi(t) = Z_\phi \leftarrow 0 \leq |v_\phi(t) - (Z_\phi - N)E| \leq \varepsilon. \quad (5.3)$$

 Figure 5.2: An n -level m -phase cascade HB inverter.

Based on the structural model of the inverter, different switching states may exist that result in the desired voltage level. The value of the pole voltage of the i^{th} HB module,

$$v_{i,i-1} = v_i - v_{i-1}, \quad (5.4)$$

can be calculated based on the value of the gate signals of its switches G_{2i}^φ and G_{2i-1}^φ and the amplitude of its dc source v_{bi} as shown by (5.5),

$$v_{i,i-1} = \left[G_{2i}^\varphi \quad 1 - G_{2i-1}^\varphi \right] \cdot \left[\frac{v_{bi}}{2} \right]. \quad (5.5)$$

In this equation, G_i^φ determines the gate signal of the i^{th} switch of phase φ . The phase voltage $v_{N,0}$ can be calculated as the summation of the pole voltages of all modules of

that phase leg,

$$v_{N,0} = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_N \cdot \begin{bmatrix} v_{1,0} \\ v_{2,1} \\ \vdots \\ v_{N,N-1} \end{bmatrix}_N. \quad (5.6)$$

Here, it is assumed all batteries are identical and $v_{bn} = 2E$, thus,

$$\begin{aligned} v_\phi &= \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_N \cdot \begin{bmatrix} G_2^\phi & 1 - G_1^\phi \\ G_{4\phi}^\phi & 1 - G_3^\phi \\ \vdots & \vdots \\ G_{2N}^\phi & 1 - G_{2N-1}^\phi \end{bmatrix} \cdot \begin{bmatrix} E \\ E \end{bmatrix} \\ &= E \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_n \cdot \begin{bmatrix} G_2^\phi & 1 - G_1^\phi \\ G_4^\phi & 1 - G_3^\phi \\ \vdots & \vdots \\ G_{2N}^\phi & 1 - G_{2N-1}^\phi \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \end{aligned} \quad (5.7)$$

Hence, the voltage level of phase ϕ at time t is

$$L_\phi(t) = \frac{v_\phi}{E} = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_N \cdot \begin{bmatrix} G_2^\phi(t) & 1 - G_1^\phi(t) \\ G_4^\phi(t) & 1 - G_3^\phi(t) \\ \vdots & \vdots \\ G_{2N}^\phi(t) & 1 - G_{2N-1}^\phi(t) \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \quad (5.8)$$

For the no-fault situation, the switches of each arm are complementary. Therefore,

$$G_{2k}^\phi(t) = 1 - G_{2k-1}^\phi(t), \quad (5.9)$$

and (5.8) can be simplified as follows;

$$L_\phi(t) = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_N \cdot \begin{bmatrix} G_2^\phi(t) & G_2^\phi(t) \\ G_4^\phi(t) & G_4^\phi(t) \\ \vdots & \vdots \\ G_{2N}^\phi(t) & G_{2N}^\phi(t) \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} = 2 \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}_N \cdot \mathbf{G}^\phi, \quad (5.10)$$

where

$$\mathbf{G}^\phi = [G_2^\phi(t) \ G_4^\phi(t) \ \cdots \ G_{2N}^\phi(t)]^T. \quad (5.11)$$

The operating mode of the system at time t , is defined as

$$M^\phi(t) := \mathbf{B} \cdot \mathbf{G}^\phi, \quad (5.12)$$

where

$$\mathbf{B} = [2^0 \ 2^1 \ 2^2 \ \cdots \ 2^{N-1}]_N. \quad (5.13)$$

5.4 Control of the n -level m -phase Inverter

To generate sinusoidal waveform, SPWM control strategy is the common method to convert dc voltage into a sinusoidal waveform. To control the on–off state of each semiconductor switch in a SPWM n -level inverter, a control block generates N PWM pulses $p_{\varphi 1}(t)$, $p_{\varphi 2}(t)$, $\dots$, $p_{\varphi N}(t)$, by comparing the reference modulating signal, $r_{\varphi}(t)$, to N triangular carrier waveforms $c_1(t)$, $c_2(t)$, $\dots$, $c_N(t)$. For $i = 1, 2, \dots, N$, and $\varphi = 1, 2, 3, \dots, m$,

$$p_{\varphi i}(t) := \begin{cases} 1, & r_{\varphi}(t) \geq c_i(t) \\ 0, & r_{\varphi}(t) < c_i(t) \end{cases}, \quad (5.14)$$

where,

$$r_{\varphi}(t) := A_r \sin(2\pi F_r t + \phi_{\varphi}) \quad (5.15)$$

is the reference signal and A_r and F_r are the amplitude and frequency of the reference signal. The displacement angle between reference and carrier signals, ϕ_{φ} , is determined by (5.16),

$$\phi_{\varphi} = (\varphi - 1) \frac{2\pi}{m}. \quad (5.16)$$

The carrier signals, $c_i(t)$ for $i = 1, 2, \dots, N$, is defined as

$$c_i(t) = \frac{c(t) + (n - 2i)}{N}. \quad (5.17)$$

In this equation, $c(t)$ is the main carrier signal with amplitude A_c , frequency F_c , and period T_c ,

$$c(t) := \begin{cases} 4A_c(F_c t - k - \frac{1}{4}), & \text{if } kT_c \leq t < (k + \frac{1}{2})T_c \\ -4A_c(F_c t - k - \frac{3}{4}), & \text{if } (k + \frac{1}{2})T_c \leq t < (k + 1)T_c \end{cases}$$

where $k = \lfloor \frac{t}{T_c} \rfloor$. (5.18)

Based on the PWM signals, the level of the pole voltage is determined,

$$H(t) = \mathbf{H}(1, h), \quad (5.19)$$

where

$$h = 1 + \log_2(1 + \sum_{i=1}^N 2^{N-i} p_{\varphi i}), \quad (5.20)$$

and

$$\mathbf{H} = [0 \ 2 \ 4 \ \cdots \ 2N]_n \quad (5.21)$$

is the set of all healthy voltage levels.

5.4.1 Switching Modes

In this section, the switching modes are selected with two criteria:

1. All of the even voltage levels (normal levels) must be obtained with the selected modes.
2. The selected modes should result in different voltage levels under each fault scenario so that all of the switch faults be isolable.

Let $\hat{G}_i^\varphi$ be the state of i^{th} switch of phase φ in the faulty situation. If Q_j^φ for $1 < j < q$ is short-circuited at $t = t_f$, then

$$\hat{G}_j^\varphi(t) = 1, \quad (5.22)$$

and

$$\hat{G}_{j-1}^\varphi(t) = 1 - G_j^\varphi(t), \quad (5.23)$$

for $t > t_f$, and from (5.8) the voltage levels which can be achieved in the faulty situation can be calculated. For $j = 2k - 1$,

$$\begin{aligned} L_j(t) = \frac{v_{\varphi N}}{E} &= [1 \ 1 \ \cdots \ 1]_N \cdot \begin{bmatrix} G_2^\varphi(t) & G_2^\varphi(t) \\ G_4^\varphi(t) & G_4^\varphi(t) \\ \vdots & \vdots \\ G_j^\varphi(t) & 0 \\ \vdots & \vdots \\ G_{2N}^\varphi(t) & G_{2N}^\varphi(t) \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} \\ &= [1 \ 1 \ \cdots \ 1]_N \cdot \begin{bmatrix} 2G_2^\varphi(t) \\ 2G_4^\varphi(t) \\ \vdots \\ G_j^\varphi(t) \\ \vdots \\ 2G_{2N}^\varphi(t) \end{bmatrix}. \quad (5.24) \end{aligned}$$

On the other hand, for $j = 2k$

$$\begin{aligned}
 L_j(t) &= \frac{v_{\varphi N}}{E} = [1 \quad 1 \quad \cdots \quad 1]_N \cdot \begin{bmatrix} G_2^\varphi(t) & G_2^\varphi(t) \\ G_4^\varphi(t) & G_4^\varphi(t) \\ \vdots & \vdots \\ 1 & G_j^\varphi(t) \\ \vdots & \vdots \\ G_{2N}^\varphi(t) & G_{2N}^\varphi(t) \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 1 \end{bmatrix} \\
 &= [1 \quad 1 \quad \cdots \quad 1]_N \cdot \begin{bmatrix} 2G_2^\varphi(t) \\ 2G_4^\varphi(t) \\ \vdots \\ 1 + G_j^\varphi(t) \\ \vdots \\ 2G_{2N}^\varphi(t) \end{bmatrix}. \tag{5.25}
 \end{aligned}$$

From (5.25) and (5.24),

$$\mathbf{L}_j^\varphi(t) = \mathbf{T}_j \cdot (\mathbf{G}^\varphi + \mathbf{A}_j), \tag{5.26}$$

where

$$\begin{aligned}
 \mathbf{T}_j &= [t_1 \quad t_2 \quad \cdots \quad t_N], \\
 t_i &= \begin{cases} 1 & \text{for } i = k, \\ 2 & \text{otherwise,} \end{cases} \tag{5.27}
 \end{aligned}$$

$$k = 1 + \lfloor \frac{j-1}{2} \rfloor, \tag{5.28}$$

and $j \in \{1, 2, 3, \dots, q\}$ is the location of the faulty switch, and

$$q = 2(n-1) \tag{5.29}$$

is the number of switches per phase leg of an n -level inverter. and

$$\begin{aligned}
 \mathbf{A}_j &= [a_{xy}]_{N \times 2N}, \\
 a_{xy} &= \begin{cases} 1 & \text{if } j = 2x \\ 0 & \text{otherwise.} \end{cases} \tag{5.30}
 \end{aligned}$$

From (5.31), all of the voltage levels that can be achieved for different modes of the system can be calculated;

$$\mathbf{L}_j (1 \times 2^N) = \mathbf{T}_j (1 \times N) \cdot (\mathbb{G} + \mathbb{A}_j) (N \times 2^N), \quad (5.31)$$

where the columns of $\mathbb{G}$ are the mode numbers in base 2, i.e, and $\mathbb{G}(x, y)$ is the x^{th} digit of y in base 2, and

$$\mathbb{A}_j(x, y) = \begin{cases} 1 & \text{if } x = k \wedge j = 2k, \\ 0 & \text{Otherwise.} \end{cases} \quad (5.32)$$

For the no-fault situation $j = 0$, and from (5.65)

$$\mathbf{A}_0 = [\mathbf{0}]_{N \times 2^N} \quad (5.33)$$

and

$$\mathbf{T}_0 = [2 \quad 2 \quad \cdots \quad 2]_N. \quad (5.34)$$

The voltage levels that can be observed in mode M of the system under fault condition Q_j are determined as

$$O(M, j) := \mathbf{W}(1 + j, 1 + M), \quad (5.35)$$

where

$$\mathbf{W} = \begin{bmatrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \vdots \\ \mathbf{L}_j \\ \vdots \\ \mathbf{L}_q \end{bmatrix}_{(q+1) \times 2^N}, \quad (5.36)$$

From $\mathbf{W}_{(q+1) \times 2^N}$, proper modes of operation can be chosen such that all of the normal states are achieved in the no-fault situation. There exist V selections where

$$V_{max} = \binom{2^N}{n} = \frac{2^N!}{(2^N - n)!(n!)}. \quad (5.37)$$

Proper modes of operation are shown in $\mathbf{W}_v (q+1 \times n)$ for $v = 1, 2, \dots, V$, where

$$\forall y, z \in \mathbb{N}, 1 \leq y \leq n, 1 \leq z \leq 2^N | y = 1 + \frac{\mathbf{W}(1, z)}{2} \implies \mathbf{W}_v(x, y) = \mathbf{W}(x, z), \quad (5.38)$$

for $x = 1, 2, \dots, q+1$. Several $\mathbf{W}_v$ matrices may be achieved from the above condition. One of them should be chosen by selecting v such that isolability of all of the switch faults is obtained. To achieve this objective, an identification vector, $\mathbf{D}_v$, is assigned to $\mathbf{W}_v$, i.e.,

$$\mathbf{D}_v(x) = \sum_{h=1}^n 2^{\mathbf{W}_v(x,h)}. \quad (5.39)$$

If the members of $\mathbf{D}_v$ are unique, all of the switch faults are isolable using selected v . In this case, the operating modes are calculated by (5.40),

$$\mathbf{M}_v = [1 \ 0 \ 0 \ \dots \ 0]_{q+1} \cdot \mathbf{W}_v. \quad (5.40)$$

5.4.2 Control of a Three-Level Inverter

Figure 5.3 shows a 3-level 3-phase cascade VSI. For $n = 3$ levels, from (5.1) and (5.2), there exist $N = 2$ HB modules and $q = 4$ switches in each phase leg. From (5.21), the matrix of the healthy voltage levels is

$$\mathbf{H} = [0 \ 2 \ 4], \quad (5.41)$$

from (5.11),

$$\mathbf{G}^\Phi = [G_2^\Phi(t) \ G_4^\Phi(t)]^T, \quad (5.42)$$

and from (5.13),

$$\mathbf{B} = [1 \ 2]. \quad (5.43)$$

Thus, from (5.12),

$$\mathbf{M}^\Phi(t) := [1 \ 2] \cdot [G_2^\Phi(t) \ G_4^\Phi(t)]^T. \quad (5.44)$$

For no-fault situation, $j = 0$, and from (5.33) and (5.34),

$$\mathbf{T}_0 = [2 \ 2], \quad (5.45)$$

and

$$\mathbf{A}_0 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}. \quad (5.46)$$

For $j = 1, 2, 3, 4$, from (5.27),

$$\mathbf{T}_1 = \mathbf{T}_2 = [1 \ 2], \quad (5.47)$$

Figure 5.3: Three-phase three-level inverter with 12 switches.

and

$$\mathbf{T}_3 = \mathbf{T}_4 = \begin{bmatrix} 2 & 1 \end{bmatrix}, \quad (5.48)$$

and from(5.30),

$$\mathbf{A}_1 = \mathbf{A}_3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad (5.49)$$

$$\mathbf{A}_2 = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \quad (5.50)$$

$$\mathbf{A}_4 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix}, \quad (5.51)$$

and

$$\mathbf{G} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix}. \quad (5.52)$$

Replacing (5.45)–(5.42) in 5.31,

$$\mathbf{L}_0 = \mathbf{T}_0 \cdot (\mathbb{G} + \mathbb{A}_0) = [2 \ 2] \cdot \left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \right) = [0 \ 2 \ 2 \ 4], \quad (5.53)$$

$$\mathbf{L}_1 = \mathbf{T}_1 \cdot (\mathbb{G} + \mathbb{A}_1) = [1 \ 2] \cdot \left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \right) = [0 \ 1 \ 2 \ 3], \quad (5.54)$$

$$\mathbf{L}_2 = \mathbf{T}_2 \cdot (\mathbb{G} + \mathbb{A}_2) = [1 \ 2] \cdot \left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} + \begin{bmatrix} 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \right) = [1 \ 2 \ 3 \ 4], \quad (5.55)$$

$$\mathbf{L}_3 = \mathbf{T}_3 \cdot (\mathbb{G} + \mathbb{A}_3) = [2 \ 1] \cdot \left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \right) = [0 \ 2 \ 1 \ 3], \quad (5.56)$$

and

$$\mathbf{L}_4 = \mathbf{T}_4 \cdot (\mathbb{G} + \mathbb{A}_4) = [2 \ 1] \cdot \left(\begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix} \right) = [1 \ 3 \ 2 \ 4]. \quad (5.57)$$

Thus, from(5.36),

$$\mathbf{W} = \begin{matrix} & M_0 & M_1 & M_2 & M_3 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \end{matrix} & \begin{pmatrix} 0 & 2 & 2 & 4 \\ 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 4 \\ 0 & 2 & 1 & 3 \\ 1 & 3 & 2 & 4 \end{pmatrix} \end{matrix} \quad (5.58)$$

The voltage levels in each mode of operation, under different fault scenarios are determined by (5.58). For example, $\mathbf{W}(1,3) = 2$ shows in the no-fault situation, operating mode 2 results in $L = 2$, and $\mathbf{W}(4,3) = 1$ shows if Q_3 is faulty, operating mode 2

results in $L = 1$. Using (5.38), W_v is obtained for $v = 1, 2$;

$$\mathbf{W}_1 = \begin{matrix} & M_0 & M_1 & M_3 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \end{matrix} & \begin{pmatrix} 0 & 2 & 4 \\ 0 & 1 & 3 \\ 1 & 2 & 4 \\ 0 & 2 & 3 \\ 1 & 3 & 4 \end{pmatrix} \end{matrix}, \quad (5.59)$$

and

$$\mathbf{W}_2 = \begin{matrix} & M_0 & M_2 & M_3 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \end{matrix} & \begin{pmatrix} 0 & 2 & 4 \\ 0 & 2 & 3 \\ 1 & 3 & 4 \\ 0 & 1 & 3 \\ 1 & 2 & 4 \end{pmatrix} \end{matrix}. \quad (5.60)$$

From (5.39),

$$\mathbf{D}_1 = \begin{bmatrix} 21 \\ 11 \\ 22 \\ 13 \\ 26 \end{bmatrix}, \quad (5.61)$$

and

$$\mathbf{D}_2 = \begin{bmatrix} 21 \\ 13 \\ 26 \\ 11 \\ 22 \end{bmatrix}. \quad (5.62)$$

Since the members of $\mathbf{D}_1$ and $\mathbf{D}_2$ are unique, in both cases all of the switch faults are isolable. The operation modes of systems are calculated from (5.40);

$$\mathbf{M}_1 = [0 \quad 1 \quad 3], \quad (5.63)$$

and

$$\mathbf{M}_2 = [0 \quad 2 \quad 3]. \quad (5.64)$$

5.5 Fault Detection and Isolation for the n -level m -phase Inverter

In this section, the procedure of the FDI of diagnosis single short-circuit faults for an n -level inverter is described. The fault diagnosis procedure starts by monitoring pole voltages and extracting the corresponding voltage levels. For $Z_\varphi = 0, 1, 2, \dots, 2N$,

$$L_\varphi(t) = \begin{cases} Z_\varphi & \text{if } \leq |v_\varphi(t) - (Z_\varphi - N)E| \leq \varepsilon \\ L_\varphi(t - T_s) & \text{Otherwise} \end{cases}. \quad (5.65)$$

As it is shown in (5.10), in the no-fault situation $L_\varphi(t)$ is an even number. Thus, if

$$L_\varphi(t_d) = 2k - 1, \quad (5.66)$$

a fault in phase φ is detected at $t = t_d$. Fig. 5.4 shows the fault detection flowchart.

Figure 5.4: Flowchart of fault detection procedure for one phase leg.

After the faulty phase is detected at t_d , the location of the faulty switch should be determined. To achieve this objective, the normal switching is interrupted and isolating modes of the system are applied;

$$M(t_d + w.T_s) = \mathbf{M}_v(1, w), \quad (5.67)$$

and the system's responses are collected in vector $\mathbf{O}$ for $w = 1, 2, \dots, n$ observations, where

$$\mathbf{O}(w) = L_{\varphi}(t_d + w.T_s). \quad (5.68)$$

Then the collected voltage levels are compared to the rows of $\mathbf{W}_v$. If for $y = 1, 2, \dots, n$ $\mathbf{O} = \mathbf{W}_v(j+1, y)$, then Q_j of phase φ is diagnosed as the faulty switch, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < n, \mathbf{O} = \mathbf{W}_v(i+1, y) \implies j = i. \quad (5.69)$$

This procedure needs maximum n observations of the system, thus, diagnosis time is

$$t_g = nT_s,$$

that is equal to a few microseconds. The diagnosis is fast enough to be used as the first step towards the FTC. Fig. 5.5 shows the isolation procedure.

Figure 5.5: Flowchart of fault isolation procedure for one phase leg.

The FDI procedure is described for one phase leg of the inverter, and the FDI procedure is the same for all of the phases. The phase legs are considered independent to each other. Thus, multiple faults of different phases can be diagnoses simultaneously. In this procedure, it is assumed that the inverter responses to the mode changes

immediately within one sampling time T_s . Simulations verify this approach. However, in the experiments, the transitions between two level of voltage can be mistaken with a faulty level. In order to prevent false alarms caused by the transitions of the switching signals, the voltage signals of all phases can be considered together and the VSP-based FDI can be applied to diagnose the faults. In this case, the diagnosis time will be equal to T_c as described in the previous section.

5.6 Simulations

Fig. 5.6 shows a 4-level 3-phase inverter. The 4-level 3-phase inverter consists of $q = 6$ IGBT switches per phase leg and 18 switches in total. To control the VSI in the no-fault situation, the proper modes of operation must be chose. These modes are calculated as described in Section 5.4.1 to ensure isolability in the faulty situation.

For a 4-level inverter, $n = 4$, $N = 3$, and $q = 6$. The healthy levels are

$$\mathbf{H} = [0 \quad 2 \quad 4 \quad 6], \quad (5.70)$$

and from (5.3), all of the normal and faulty voltage levels are calculated for $n = 4$;

$$L_\phi(t) = \begin{cases} 0 & 0 \leq |v_\phi(t) + 3E| \leq \epsilon \\ 1 & 0 \leq |v_\phi(t) + 2E| \leq \epsilon \\ 2 & 0 \leq |v_\phi(t) + E| \leq \epsilon \\ 3 & 0 \leq |v_\phi(t)| \leq \epsilon \\ 4 & 0 \leq |v_\phi(t) - E| \leq \epsilon \\ 5 & 0 \leq |v_\phi(t) - 2E| \leq \epsilon \\ 6 & 0 \leq |v_\phi(t) - 3E| \leq \epsilon \\ L_\phi(t - T_s) & \text{Otherwise.} \end{cases} \quad (5.71)$$

From (5.11),

$$\mathbf{G}^\phi = [G_2^\phi(t) \quad G_4^\phi(t) \quad G_6^\phi(t)]^T \quad (5.72)$$

Figure 5.6: Schematic of a 3-phase 4-level HB inverter.

From (5.31), $\mathbf{W}$ is calculated, as shown in (5.73), and the proper operating modes are found, as shown in (5.74–5.79), through a search algorithm by a program written

in MATLAB;

$$\mathbf{W} = \begin{matrix} & M_0 & M_1 & M_2 & M_3 & M_4 & M_5 & M_6 & M_7 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \\ \mathbf{L}_5 \\ \mathbf{L}_6 \end{matrix} & \begin{pmatrix} 0 & 2 & 2 & 4 & 2 & 4 & 4 & 6 \\ 0 & 1 & 2 & 3 & 2 & 3 & 4 & 5 \\ 1 & 2 & 3 & 4 & 3 & 4 & 5 & 6 \\ 0 & 2 & 1 & 3 & 2 & 4 & 3 & 5 \\ 1 & 3 & 2 & 4 & 3 & 5 & 4 & 6 \\ 0 & 2 & 2 & 4 & 1 & 3 & 3 & 5 \\ 1 & 3 & 3 & 5 & 2 & 4 & 4 & 6 \end{pmatrix} \end{matrix}, \quad (5.73)$$

$$\mathbf{M}_1 = [0 \ 1 \ 3 \ 7], \quad (5.74)$$

$$\mathbf{M}_2 = [0 \ 1 \ 5 \ 7], \quad (5.75)$$

$$\mathbf{M}_3 = [0 \ 2 \ 3 \ 7], \quad (5.76)$$

$$\mathbf{M}_4 = [0 \ 2 \ 6 \ 7], \quad (5.77)$$

$$\mathbf{M}_5 = [0 \ 4 \ 5 \ 7], \quad (5.78)$$

$$\mathbf{M}_6 = [0 \ 4 \ 6 \ 7]. \quad (5.79)$$

Any of the calculated proper modes M_1 – M_6 can be selected for the control purpose. All of them result in the healthy voltage levels in the no-fault situation and in the meantime, guarantee isolability of faults in the faulty conditions. In the following experiments, M_1 was selected to control the switches, i.e., $v = 1$, and

$$\mathbf{W}_1 = \begin{matrix} & M_0 & M_1 & M_3 & M_7 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \\ \mathbf{L}_5 \\ \mathbf{L}_6 \end{matrix} & \begin{pmatrix} 0 & 2 & 4 & 6 \\ 0 & 1 & 3 & 5 \\ 1 & 2 & 4 & 6 \\ 0 & 2 & 3 & 5 \\ 1 & 3 & 4 & 6 \\ 0 & 2 & 4 & 5 \\ 1 & 3 & 5 & 6 \end{pmatrix} \end{matrix}. \quad (5.80)$$

Fig. 5.7 illustrates one cycle of the reference and carrier signals for the no-fault situation. The selected control modes of the inverter are $\mathbf{M} = [0, 1, 3, 7]$. All of the phase voltages are monitored and digitized. As soon as an odd-level is observed in φ , it is detected as the faulty phase.

Figure 5.7: PWM reference and carrier signals for a 4-level inverter under no-fault condition.

For the isolation purpose, the isolating modes of the system are applied to the faulty phase and the digitized values of the pole voltage of the faulty phase are collected, i.e.,

$$\text{For } w = 1, \quad M(t_d + T_s) = M(1, 1) = 0, \implies \mathbf{O}(1) = L_1(t_d + T_s) = 0 \quad (5.81)$$

$$\text{For } w = 2, \quad M(t_d + 2T_s) = M(1, 2) = 1, \implies \mathbf{O}(2) = L_1(t_d + 2T_s) = 1 \quad (5.82)$$

$$\text{For } w = 3, \quad M(t_d + 3T_s) = M(1, 3) = 3, \implies \mathbf{O}(3) = L_1(t_d + 3T_s) = 3 \quad (5.83)$$

$$\text{For } w = 4, \quad M(t_d + 4T_s) = M(1, 4) = 7, \implies \mathbf{O}(4) = L_1(t_d + 4T_s) = 5 \quad (5.84)$$

$$\mathbf{O} = [0 \quad 1 \quad 3 \quad 5], \quad (5.85)$$

Comparing to (5.80), $\mathbf{O}$ is equal to the second row of $\mathbf{W}_1$, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < 4, \mathbf{O} = \mathbf{W}_1(2, y) \implies j = 1, \quad (5.86)$$

therefore, Q_1 of phase $\varphi = 1$ is diagnosed as the faulty switch. Fig. 5.8 illustrates the pole voltage of the faulty phase v_φ and its digitized value u_φ . For the healthy situation,

$u_A = 0, 2, 4, 6$ and as soon as $u_A(t_d) = 3$ is monitored, the faulty phase is detected at $t = t_d$. Fig. 5.9 illustrates the simulation results of diagnosis a short-circuit fault in Q_1 .

Figure 5.8: The continuous and digitized values of the faulty phase.

Figure 5.9: The simulation results of diagnosis a short-circuit fault in Q_1 of a 4-level inverter.

In this experiment, $F_r = 60.0$ Hz, $F_c = 1$ KHz, and the sampling time T_s is equal to 38.58μ s. Fig. 5.10 illustrates the simulation results of diagnosis a short-circuit fault in Q_2 . In this experiment, the switch fault is detected in $\varphi = 1$ by observing $U_a = 1$. Then the isolating modes are applied and the following voltage levels are observed:

$$\text{For } w = 1, \quad M(t_d + T_s) = M(1, 1) = 0, \implies \mathbf{O}(1) = L_1(t_d + T_s) = 1 \quad (5.87)$$

$$\text{For } w = 2, \quad M(t_d + 2T_s) = M(1, 2) = 1, \implies \mathbf{O}(2) = L_1(t_d + 2T_s) = 2 \quad (5.88)$$

$$\text{For } w = 3, \quad M(t_d + 3T_s) = M(1, 3) = 3, \implies \mathbf{O}(3) = L_1(t_d + 3T_s) = 4 \quad (5.89)$$

$$\text{For } w = 4, \quad M(t_d + 4T_s) = M(1, 4) = 7, \implies \mathbf{O}(4) = L_1(t_d + 4T_s) = 6 \quad (5.90)$$

$$\mathbf{O} = [1 \quad 2 \quad 4 \quad 6], \quad (5.91)$$

Comparing to (5.80), $\mathbf{O}$ is equal to the third row of $\mathbf{W}_1$, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < 4, \mathbf{O} = \mathbf{W}_1(3, y) \implies j = 2, \quad (5.92)$$

hence, Q_2 of phase $\varphi = 1$ is diagnosed as the faulty switch.

Figure 5.10: The simulation results of diagnosis a short-circuit fault in Q_2 of a 4-level inverter.

Fig. 5.11 illustrates the simulation results of diagnosis a short-circuit fault in Q_3 . In this experiment, the switch fault is detected in $\varphi = 1$ by observing $U_a = 3$. Then the isolating modes are applied and the following voltage levels are observed:

$$\text{For } w = 1, \quad M(t_d + T_s) = M(1, 1) = 0, \implies \mathbf{O}(1) = L_1(t_d + T_s) = 0 \quad (5.93)$$

$$\text{For } w = 2, \quad M(t_d + 2T_s) = M(1, 2) = 1, \implies \mathbf{O}(2) = L_1(t_d + 2T_s) = 2 \quad (5.94)$$

$$\text{For } w = 3, \quad M(t_d + 3T_s) = M(1, 3) = 3, \implies \mathbf{O}(3) = L_1(t_d + 3T_s) = 3 \quad (5.95)$$

$$\text{For } w = 4, \quad M(t_d + 4T_s) = M(1, 4) = 7, \implies \mathbf{O}(4) = L_1(t_d + 4T_s) = 5 \quad (5.96)$$

$$\mathbf{O} = [0 \quad 2 \quad 3 \quad 5], \quad (5.97)$$

Comparing to (5.80), $\mathbf{O}$ is equal to the forth row of $\mathbf{W}_1$, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < 4, \mathbf{O} = \mathbf{W}_1(4, y) \implies j = 3, \quad (5.98)$$

hence, Q_3 of phase $\varphi = 1$ is diagnosed as the faulty switch.

Figure 5.11: The simulation results of diagnosis a short-circuit fault in Q_3 of a 4-level inverter.

Fig. 5.13 illustrates the simulation results of diagnosis a short-circuit fault in Q_5 . In this experiment, the switch fault is detected in $\varphi = 1$ by observing $U_a = 5$. Then the isolating modes are applied and the following voltage levels are observed:

$$\text{For } w = 1, \quad M(t_d + T_s) = M(1, 1) = 0, \implies \mathbf{O}(1) = L_1(t_d + T_s) = 0 \quad (5.105)$$

$$\text{For } w = 2, \quad M(t_d + 2T_s) = M(1, 2) = 1, \implies \mathbf{O}(2) = L_1(t_d + 2T_s) = 1 \quad (5.106)$$

$$\text{For } w = 3, \quad M(t_d + 3T_s) = M(1, 3) = 3, \implies \mathbf{O}(3) = L_1(t_d + 3T_s) = 3 \quad (5.107)$$

$$\text{For } w = 4, \quad M(t_d + 4T_s) = M(1, 4) = 7, \implies \mathbf{O}(4) = L_1(t_d + 4T_s) = 7 \quad (5.108)$$

$$\mathbf{O} = [0 \quad 2 \quad 4 \quad 5], \quad (5.109)$$

Comparing to (5.80), $\mathbf{O}$ is equal to the sixth row of $\mathbf{W}_1$, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < 4, \mathbf{O} = \mathbf{W}_1(6, y) \implies j = 5, \quad (5.110)$$

hence, Q_5 of phase $\varphi = 1$ is diagnosed as the faulty switch.

Figure 5.13: The simulation results of diagnosis a short-circuit fault in Q_5 of a 4-level inverter.

Fig. 5.14 illustrates the simulation results of diagnosis a short-circuit fault in Q_6 . In this experiment, the switch fault is detected in $\varphi = 1$ by observing $U_a = 5$. Then the isolating modes are applied and the following voltage levels are observed:

$$\text{For } w = 1, \quad M(t_d + T_s) = M(1, 1) = 0, \implies \mathbf{O}(1) = L_1(t_d + T_s) = 1 \quad (5.111)$$

$$\text{For } w = 2, \quad M(t_d + 2T_s) = M(1, 2) = 1, \implies \mathbf{O}(2) = L_1(t_d + 2T_s) = 5 \quad (5.112)$$

$$\text{For } w = 3, \quad M(t_d + 3T_s) = M(1, 3) = 3, \implies \mathbf{O}(3) = L_1(t_d + 3T_s) = 5 \quad (5.113)$$

$$\text{For } w = 4, \quad M(t_d + 4T_s) = M(1, 4) = 7, \implies \mathbf{O}(4) = L_1(t_d + 4T_s) = 5 \quad (5.114)$$

$$\mathbf{O} = [1 \quad 3 \quad 5 \quad 6], \quad (5.115)$$

Comparing to (5.80), $\mathbf{O}$ is equal to the seventh row of $\mathbf{W}_1$, i.e.,

$$\forall y \in \mathbb{N}, 1 < y < 4, \mathbf{O} = \mathbf{W}_1(7, y) \implies j = 6, \quad (5.116)$$

hence, Q_6 of phase $\varphi = 1$ is diagnosed as the faulty switch.

Figure 5.14: The simulation results of diagnosis a short-circuit fault in Q_6 of a 4-level inverter.

5.7 Experiments

In this section, experimental results of diagnosis switch faults of a three-phase three-level inverter are shown. Figure 5.15 shows a three-phase full-bridge VSI consisting of 12 MOSFET switches.

Figure 5.15: Three-phase full-bridge inverter with 12 switches.

Figure 5.16 depicts the schematic of the experimental set-up which was designed to diagnose switch faults in a MLI based on full-bridge topology. The RFP70N06 MOSFETS were selected for this set-up. The MOSFETS were driven with the full-bridge drive IC HIP4082. The power side was isolated from the control side using HPCL2232 opto-couplers. The control signals were generated in a PC and applied to the circuit through NI PCI6025e I–O card as described in Section 3.6. The HIP4082 has an intrinsic safety operation that prevents some of the gate-misfiring faults. Thus, it was not possible to simulate gate misfiring faults in the upper switches of the full bridge inverter, Q_3 and Q_2 .

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Figure 5.16: The schematic of the experimental set-up

Table 5.1 shows the truth table of the HIP4082. In Fig. 5.17 the experimental result

TRUTH TABLE						
INPUT					OUTPUT	
ALI, BLI	AHI, BHI	VDDUV	VHBUV	DIS	ALO, BLO	AHO, BHO
X	X	X	X	1	0	0
X	X	1	X	X	0	0
0	X	0	1	0	0	0
1	X	0	X	0	1	0
0	1	0	0	0	0	1
0	0	0	0	0	0	0

NOTE: X signifies that input can be either a "1" or "0".

Table 5.1: Truth table of HIP 4082 H-Bridge FET Driver IC (Appendix D).

of diagnosis of an a short-circuit fault Q_{a1} is illustrated. The first four diagrams of this figure show the gate control signal, and the voltage signals of the three phases are shown in the next three diagrams. In the FDI stage, 5 levels of voltage have been defined (three healthy plus two faulty levels) that results in $5^3 = 125$ levels. Thus, the state value varies between 0 to 124 as shown in the eight diagram. The last diagram in this figure shows the FDI result; $J=0$ indicates no-fault and $J=1$ indicates diagnosis a short-circuit fault in Q_1 . In this experiment, $G_1(t > t_f) = 1$ where $t_f = 1.95$ ms is the time when the fault was inserted. As it can be seen in this figure, for the no-fault situation, v_A , v_B , and v_C fluctuate between three levels of voltage (-10, 0, +10). However, after the fault occurred in phase A, $v_A \neq +10V$. Considering the structural model of the inverter and the truth table of the driver IC, the FBZs of the FBI were updated and the VSP-based FDI was applied to diagnose the faulty switch.

 Figure 5.17: Experimental results of FDI for short-circuit fault in Q_{a1} .

In the other experiment, a short-circuit fault was inserted in Q_{a4} . In Fig. 5.18, the first four diagrams show the gate control signal, and the voltage signals of the three phases are shown in the next three diagrams. The last diagram in this figure shows the FDI result; $J=0$ indicates no-fault and $J=4$ indicates diagnosis a short-circuit fault in

Q_4 . In this experiment, $G_4(t > t_f) = 1$ where t_f is the time when the fault was inserted.

Figure 5.18: Experimental results of FDI for short-circuit fault in Q_{a4} .

As it can be seen in this figure, for the no-fault situation, v_A , v_B , and v_C fluctuate between three levels of voltage (-10, 0, +10). However, after the fault occurred in phase A, $v_A \neq -10$ V. Considering the structural model of the inverter and the truth table of the driver IC, the FBZs of the FBI were updated and the VSP-based FDI was applied to diagnose the faulty switch.

5.8 Summary

In this chapter, a FDI method was proposed for locating semiconductor switch faults in the multi-level multi-phase VSIs. A general model describing the cascade HBI was introduced and the operating modes of the system were defined. It was shown how to control the switches and to select proper switching modes to obtain isolability in the FDI stage

This chapter presented a FDI method for diagnosis of short-circuit switch faults in m -phase n -level cascade inverters based on the measurement of pole voltages of each phase leg of the inverter. The proposed FDI method requires only one voltage detector per phase leg to accurately isolate a faulty switch among $2m(n - 1)$ switches in a n -level m -phase VSI. The pole voltage of each phase was monitored and digitized into $2n - 1$ levels. A fault was detected when an odd level of voltage was observed. After the fault was detected, certain switching modes were applied to the inverter and the resulting voltage levels were gathered. By comparing finite numbers of the observed voltage levels to the fault signature sets, the location of the faulty switch was determined. The diagnosis time was equal to only a few sampling time which is significantly faster than the existing FDI methods. It takes only $t_g = n.T_s$ between the time when the switch fault affects the circuit and the time when it is isolated. This quick FDI time allows isolating the switch and implementation of a proper FTC after the fault isolation.

In the next chapter, a FTC strategy is described and the ability of diagnosis switch faults in a 18-switch cascade HB VSI with only three voltage detectors using the FDI method which was described in this Chapter is demonstrated.

Chapter 6

Fault tolerant Control

6.1 Introduction

In this chapter, the fault tolerant control (FTC) of a multi-level inverter containing a short-circuit fault is described. A short-circuit switch fault causes high short-circuit current in the faulty module of the inverter which can damage the other switches of the inverter and the voltage sources connecting to them. It also distorts the switching pattern and the resulting sinusoidal waveform which increases the THD. In this case, the balance of the multi-phase inverter is also missed. The control of the inverter in the faulty situation should be changed so that it can continue its operation with minimum side effects. The objective of FTC can be divided into two main items:

1. Self-healing for the phase with the faulty switch which includes protecting the healthy components by preventing the short-circuit current, and reducing total harmonic distortion (THD) of the faulty phase.
2. Re-phasing the gate control signals for the balance of the multi-phase inverter.

Consider the 4-level 3-phase inverter of Fig. 6.1 with $q = 6$ IGBT switches per phase leg and 18 switches in total.

Figure 6.1: Schematic of a 3-phase 4-level HB inverter.

In the no-fault situation, the phase voltages are as follow:

$$v_1(t) \propto X_1(t) = A_1 \sin(2\pi F_r t + \phi_1), \quad (6.1)$$

$$v_2(t) \propto X_2(t) = A_2 \sin(2\pi F_r t + \phi_2), \quad (6.2)$$

$$v_3(t) \propto X_3(t) = A_3 \sin(2\pi F_r t + \phi_3). \quad (6.3)$$

and

$$A_1 = A_2 = A_3 = NA_s, \quad (6.4)$$

where A_s is the amplitude of the sinusoidal signals and $A_s \propto E$ which is the amplitude of each dc source. Thus, the line voltages are in balance, i.e,

$$|X_1(t) - X_2(t)| = |X_1(t) - X_3(t)|, \quad (6.5)$$

$$|X_1(t) - X_2(t)| = |X_2(t) - X_3(t)|, \quad (6.6)$$

$$|X_1(t) - X_3(t)| = |X_2(t) - X_3(t)|. \quad (6.7)$$

In the faulty situation, (6.4) is not valid anymore, disturbing the line voltage balance of (6.5–6.7). Let define the three phases quantities in the faulty situation with $\hat{\cdot}$. The FTC problem of a three-phase inverter can be solved by finding appropriate switching states which result in

$$|\hat{X}_1(t) - \hat{X}_2(t)| = |\hat{X}_1(t) - \hat{X}_3(t)|, \quad (6.8)$$

$$|\hat{X}_1(t) - \hat{X}_2(t)| = |\hat{X}_2(t) - \hat{X}_3(t)|, \quad (6.9)$$

$$|\hat{X}_1(t) - \hat{X}_3(t)| = |\hat{X}_2(t) - \hat{X}_3(t)|. \quad (6.10)$$

The first task of the FTC is the protection of the other devices of the faulty module, reducing THD of the faulty leg, and achieving the balance in the line voltages which are described in the next sections.

6.2 Protection

Existence of the faulty switch causes a very high short-circuit current in the inverter and the voltage source of the faulty HB module. For example, consider a short-circuit fault in Q_1a of the inverter of Fig. 6.1. Fig. 6.2 illustrates how the current signal of the faulty phase is distorted after fault occurred for $t > t_f$. The current signals of Q_1 and the dc source connected to it are shown in Fig. 6.3.

Figure 6.2: Current signals of the three phases and the digitized voltage of the faulty phase. A short-circuit fault has occurred at $t=0.05$ s.

As it can be seen in Fig. 6.3, existence of the faulty switch causes a very high short-circuit current in the inverter and the voltage source of the faulty HB module. Thus, the FTC needs to be applied to protect the switches and the voltage source. To achieve this objective, the first task is to break the short-circuit loop by opening the complementary switch of the faulty leg. Let assume Q_j is faulty and j is known from the FDI stage.

Figure 6.3: Current signals of the faulty switch and the connected voltage source. A short-circuit fault has occurred at $t=0.05$ s.

The location of the faulty module is determined by k as shown in (5.28). In the faulty situation,

$$\hat{G}_j^\varphi(t) = 1, \quad (6.11)$$

and the state of the faulty switch is not controllable anymore. Thus, the first task is to open the complementary switch of module k ;

$$\hat{G}_{2k}^\varphi(t) = 0, \quad \text{for } j = 2k - 1, \quad (6.12)$$

$$\hat{G}_{2k-1}^\varphi(t) = 0, \quad \text{for } j = 2k. \quad (6.13)$$

By this reconfiguration, the faulty module is bypassed and one level of voltage is missed in the faulty phase φ , i.e.,

$$\hat{A}_\varphi = (N - 1)A_s. \quad (6.14)$$

6.3 Reducing THD

The THD is the ratio of the root mean square (rms) value of the total harmonics of a periodic signal to the rms value of its fundamental harmonic. Fig. 6.4 illustrates the pole voltage signals of one phase leg of a 4-level inverter. The current signal is shown for a series RL load with $R = 1\Omega$ and $L = 5.6mH$. The THD in the no-fault operating condition is $THD=0.02741$. In these simulations, the fundamental THD is calculated, i.e.,

$$THD = \frac{\sqrt{\sum_{\alpha=2} I_{\alpha}^2}}{I_{rms}}. \quad (6.15)$$

As it can be seen in Fig. 6.5, in the presence of a short-circuit fault in Q_1 , some voltage levels are not achieved and the sinusoidal current waveform is distorted. The THD for the current signal with a short-circuit fault in Q_1 is $TDH=0.06055$.

Figure 6.4: Current and voltage signals of phase 1 in no-fault situation.

Figure 6.5: Current and voltage signals of phase 1. A short-circuit fault exists in Q_1 .

Fig. 6.6 shows that in the presence of a short-circuit fault in Q_2 , the sinusoidal current waveform is distorted, thus, THD for the current signal increases in comparison to the no-fault situation. $TDH=0.06057$ in this case. Similarly, Fig. 6.7–6.10 show the voltage and current signals in the presence of a short-circuit fault in Q_3 – Q_6 . As the sinusoidal current waveform is distorted the THD level increases in comparison to the no-fault situation. The THD for the current signal with a short-circuit fault in Q_3 – Q_6 is $TDH=0.04736$, $TDH=0.04736$, $TDH=0.5392$, and $TDH=0.0541$ respectively.

Figure 6.6: Current and voltage signals of phase 1. A short-circuit fault exists in Q_2 .

Figure 6.7: Current and voltage signals of phase 1. A short-circuit fault exists in Q_3 .

Figure 6.8: Current and voltage signals of phase 1. A short-circuit fault exists in Q_4 .

Figure 6.9: Current and voltage signals of phase 1. A short-circuit fault exists in Q_5 .

Figure 6.10: Current and voltage signals of phase 1. A short-circuit fault exists in Q_6 .

As it was shown in these figures, existence of a faulty switch in the inverter distorts the voltage switching waveform, hence the resulting filtered signal (e.g. load current) will not be a perfect sinusoidal waveform anymore and the level of the THD increases in the faulty signal.

To reduce the THD of the faulty phase, the switching modes need to be modified to gain a perfect sinusoidal output with the maximum possible amplitude. As a result of protection stage (6.14), after bypassing the faulty module one voltage level is missed. Thus, the PWM control signals of the n -level inverter results in an imperfect sinusoidal waveform. To reduce the THD the reference sinusoidal signal of the SPWM control module is changed to a lower amplitude signal and the SPWM control of $n - 1$ -level inverter are applied to the remaining modules. This reconfiguration ensures a perfect sinusoidal output which has the same THD as the healthy $n - 1$ -level inverter. Thus, the operating modes of the system are changed as follow;

$$1 \leq y \leq 2^{N-1}, 0 \leq i \leq N : \mathbf{W}(j+1, y) = 2i \implies {}_j\hat{\mathbf{M}}(x) = y - 1, \quad (6.16)$$

for $1 \leq x \leq n$, where $\mathbf{W}$ is the proper modes of operation as defined in (5.36). For example, for the 4-level inverter of Fig. 5.6, as described in Section 5.6, $\mathbf{W}$ is calculated, as shown in (6.17), and the proper operating modes are found, as shown in (6.18–6.23) in the no-fault situation.

$$\mathbf{W} = \begin{matrix} & M_0 & M_1 & M_2 & M_3 & M_4 & M_5 & M_6 & M_7 \\ \begin{matrix} \mathbf{L}_0 \\ \mathbf{L}_1 \\ \mathbf{L}_2 \\ \mathbf{L}_3 \\ \mathbf{L}_4 \\ \mathbf{L}_5 \\ \mathbf{L}_6 \end{matrix} & \begin{pmatrix} 0 & 2 & 2 & 4 & 2 & 4 & 4 & 6 \\ 0 & 1 & 2 & 3 & 2 & 3 & 4 & 5 \\ 1 & 2 & 3 & 4 & 3 & 4 & 5 & 6 \\ 0 & 2 & 1 & 3 & 2 & 4 & 3 & 5 \\ 1 & 3 & 2 & 4 & 3 & 5 & 4 & 6 \\ 0 & 2 & 2 & 4 & 1 & 3 & 3 & 5 \\ 1 & 3 & 3 & 5 & 2 & 4 & 4 & 6 \end{pmatrix} \end{matrix}, \quad (6.17)$$

$$\mathbf{M}_1 = [0 \ 1 \ 3 \ 7], \quad (6.18)$$

$$\mathbf{M}_2 = [0 \ 1 \ 5 \ 7], \quad (6.19)$$

$$\mathbf{M}_3 = [0 \ 2 \ 3 \ 7], \quad (6.20)$$

$$\mathbf{M}_4 = [0 \ 2 \ 6 \ 7], \quad (6.21)$$

$$\mathbf{M}_5 = [0 \ 4 \ 5 \ 7], \quad (6.22)$$

$$\mathbf{M}_6 = [0 \ 4 \ 6 \ 7]. \quad (6.23)$$

From (6.16) and (6.17), the operating modes of the system in the faulty condition ${}_j\hat{\mathbf{M}}$ are calculated where j is the location of the faulty switch which was obtained from the FDI stage. For example, ${}_j\hat{\mathbf{M}}$ is calculated for $j = 0$ to 6;

$${}_1\hat{\mathbf{M}} = [0 \ 2 \ 4 \ 6], \quad (6.24)$$

$${}_2\hat{\mathbf{M}} = [1 \ 3 \ 5 \ 7], \quad (6.25)$$

$${}_3\hat{\mathbf{M}} = [0 \ 1 \ 4 \ 5], \quad (6.26)$$

$${}_4\hat{\mathbf{M}} = [2 \ 3 \ 6 \ 7], \quad (6.27)$$

$${}_5\hat{\mathbf{M}} = [0 \ 1 \ 2 \ 3], \quad (6.28)$$

$${}_6\hat{\mathbf{M}} = [4 \ 5 \ 6 \ 7]. \quad (6.29)$$

Figures 6.11–6.16 illustrates the voltage and current signals of a 4-level inverter with the fault tolerant control. In the spite of existence of a faulty switch in the inverter, the resulting THD is reduced to $\text{THD}=0.03963$ in all of the fault scenarios.

Figure 6.11: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_1 .

Figure 6.12: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_2 .

Figure 6.13: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_3 .

Figure 6.14: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_4 .

Figure 6.15: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_5 .

Figure 6.16: Current and voltage signals of phase 1 with FTC when a short-circuit fault exists in Q_6 .

[H]

6.4 Balancing the faulty Inverter

The third objective of FTC is to maintain the balance of the multi-phase system in presence of fault. For a single phase inverter this objective is eliminated. The FTC used in this section results in the same phase differences as in the healthy situation. However, the amplitude of the faulty phase is reduced by one level and the line voltages are not equal anymore. In some applications it is necessary to ensure the balance of the line voltage. Thus, a method is adopted to ensure the balance of the line voltages with the maximum possible amplitude in the faulty situation. This concept is similar to what was used by ADLINK [99]. From (5.15)

$$v_1(t) \propto X_1(t) = A_1 \sin(2\pi F_r t + \phi_1), \quad (6.30)$$

$$v_2(t) \propto X_2(t) = A_2 \sin(2\pi F_r t + \phi_2), \quad (6.31)$$

$$v_3(t) \propto X_3(t) = A_3 \sin(2\pi F_r t + \phi_3). \quad (6.32)$$

In the healthy situation,

$$A_1 = A_2 = A_3 = NA_s, \quad (6.33)$$

where A_s is the amplitude of the sinusoidal signals and $A_s \propto E$. However, after the FTC is applied to the faulty phase, a sinusoidal signal with a reduced amplitude is achieved, i.e., for $\varphi = 1$,

$$\hat{X}_1(t) = (N - 1)A_s \sin(2\pi F_r t + \phi_1), \quad (6.34)$$

In the no-fault situation,

$$X_1(t) + X_2(t) + X_3(t) = 0, \quad (6.35)$$

while in the FTC condition,

$$\hat{X}_1(t) + X_2(t) + X_3(t) = A_s \sin(2\pi F_r t + \phi_0), \quad (6.36)$$

where $\phi_0 = \pi$. Therefore, a sinusoidal component appears in the null, and the line-line voltages are not equal. A balance in the line-line voltages can be obtained by solving

the following equations and obtaining proper $\hat{\phi}$ for each phase,

$$|\hat{X}_1(t) - \hat{X}_2(t)| = |\hat{X}_1(t) - \hat{X}_3(t)|, \quad (6.37)$$

$$|\hat{X}_1(t) - \hat{X}_2(t)| = |\hat{X}_2(t) - \hat{X}_3(t)|, \quad (6.38)$$

$$|\hat{X}_1(t) - \hat{X}_3(t)| = |\hat{X}_2(t) - \hat{X}_3(t)|. \quad (6.39)$$

Replacing (6.30), (6.31), and (6.32) in (6.38), (6.39), and (6.37) yields

$$|\hat{A}_1 \angle \hat{\phi}_1 - \hat{A}_2 \angle \hat{\phi}_2| = |\hat{A}_1 \angle \hat{\phi}_1 - \hat{A}_3 \angle \hat{\phi}_3| \quad (6.40)$$

$$|\hat{A}_1 \angle \hat{\phi}_1 - \hat{A}_2 \angle \hat{\phi}_2| = |\hat{A}_2 \angle \hat{\phi}_2 - \hat{A}_3 \angle \hat{\phi}_3| \quad (6.41)$$

$$|\hat{A}_1 \angle \hat{\phi}_1 - \hat{A}_3 \angle \hat{\phi}_3| = |\hat{A}_2 \angle \hat{\phi}_2 - \hat{A}_3 \angle \hat{\phi}_3|. \quad (6.42)$$

Where

$$\hat{A}_2 = \hat{A}_3 = NA_s, \quad (6.43)$$

to keep the maximum amplitude of the healthy phases, and

$$\hat{A}_1 = (N - 1)A_s, \quad (6.44)$$

to obtain minimum THD for the faulty phase. Also, we know

$$\hat{\phi}_1 + \hat{\phi}_2 + \hat{\phi}_3 = 2\pi. \quad (6.45)$$

By solving (6.37)–(6.39), the phase angles in the FTC mode, $\hat{\phi}$, will be obtained. From (6.40)–(6.42),

$$\hat{A}_1^2 + \hat{A}_2^2 - 2\hat{A}_1\hat{A}_2 \cos(\hat{\phi}_1 - \hat{\phi}_2) = \hat{A}_1^2 + \hat{A}_3^2 - 2\hat{A}_1\hat{A}_3 \cos(\hat{\phi}_1 - \hat{\phi}_3), \quad (6.46)$$

$$\hat{A}_1^2 + \hat{A}_2^2 - 2\hat{A}_1\hat{A}_2 \cos(\hat{\phi}_1 - \hat{\phi}_2) = \hat{A}_2^2 + \hat{A}_3^2 - 2\hat{A}_2\hat{A}_3 \cos(\hat{\phi}_2 - \hat{\phi}_3), \quad (6.47)$$

$$\hat{A}_1^2 + \hat{A}_3^2 - 2\hat{A}_1\hat{A}_3 \cos(\hat{\phi}_1 - \hat{\phi}_3) = \hat{A}_2^2 + \hat{A}_3^2 - 2\hat{A}_2\hat{A}_3 \cos(\hat{\phi}_2 - \hat{\phi}_3). \quad (6.48)$$

From (6.46)–(6.48),

$$\cos(\hat{\phi}_1 - \hat{\phi}_2) = \cos(\hat{\phi}_1 - \hat{\phi}_3) \quad (6.49)$$

$$\hat{\phi}_1 - \hat{\phi}_2 = -2\pi - \hat{\phi}_1 + \hat{\phi}_3 \quad (6.50)$$

$$\hat{\phi}_1 = -\pi + \frac{\hat{\phi}_2 + \hat{\phi}_3}{2} \quad (6.51)$$

From (6.47), (6.43), and (6.44)

$$(N-1)^2 - 2N(N-1)\cos(\hat{\phi}_1 - \hat{\phi}_2) = N^2 - 2N^2\cos(\hat{\phi}_2 - \hat{\phi}_3) \quad (6.52)$$

$$-2N(N-1)\cos(\hat{\phi}_1 - \hat{\phi}_2) + 1 - 2N + 2N^2\cos(\hat{\phi}_2 - \hat{\phi}_3) = 0 \quad (6.53)$$

Implementing (6.51) in (6.53),

$$2N(N-1)\cos\left(\frac{\hat{\phi}_3 - \hat{\phi}_2}{2}\right) + 1 - 2N + 2N^2\cos(\hat{\phi}_2 - \hat{\phi}_3) = 0. \quad (6.54)$$

Let

$$x = \frac{\hat{\phi}_3 - \hat{\phi}_2}{2}, \quad (6.55)$$

replacing x in (6.54),

$$2N(N-1)\cos(x) + 1 - 2N + 2N^2\cos(2x) = 0 \quad (6.56)$$

$$2N(N-1)\cos(x) + 1 - 2N + 2N^2(2\cos^2(x) - 1) = 0 \quad (6.57)$$

$$4N^2\cos^2(x) + 2N(N-1)\cos(x) - 2N^2 - 2N + 1 = 0 \quad (6.58)$$

$$\cos(x) = \frac{-2N(N-1) \pm \sqrt{(2N(N-1))^2 - 16N^2(-2N^2 - 2N + 1)}}{8N^2} \quad (6.59)$$

$$\cos(x) = \frac{-N+1 \pm \sqrt{9N^2+6N-3}}{4N} \quad (6.60)$$

$$x = \arccos\left(\frac{-N+1 \pm \sqrt{9N^2+6N-3}}{4N}\right) \quad (6.61)$$

For the 4-level inverter, $N = 3$ and from (6.61),

$$\cos(x) = -0.9832, 0.6498 \quad (6.62)$$

$$x = 49.47^\circ, 169.47^\circ, \quad (6.63)$$

From 6.55,

$$\hat{\phi}_3 - \hat{\phi}_2 = 2x = 98.94^\circ \quad (6.64)$$

is the acceptable solution. Taking

$$\hat{\phi}_1 = 0 \quad (6.65)$$

as the reference phase, from (6.51)

$$\hat{\phi}_3 = 2\pi - \hat{\phi}_2, \quad (6.66)$$

and

$$2\pi - 2\hat{\phi}_2 = 2x, \quad (6.67)$$

$$\hat{\phi}_2 = \pi - x = 130.53^\circ. \quad (6.68)$$

Hence,

$$\hat{\phi}_3 = \hat{\phi}_2 + 2x = \pi + x = 229.47^\circ \quad (6.69)$$

With this modification, the amplitudes of all of the three line voltages will be equal and a balance in the line voltages will be achieved with maximum amplitude in the faulty situation. i.e.,

$$\begin{aligned} |X_{32}| = |X_3 - X_2| &= \sqrt{\hat{A}_2^2 + \hat{A}_3^2 - 2\hat{A}_2\hat{A}_3 \cos(\hat{\phi}_2 - \hat{\phi}_3)} = \sqrt{2N^2A_s^2(1 - \cos(2x))} \\ &= NA_s \sqrt{2(1 - \cos(2x))} = 2NA_s \sin(x) = 1.52. \end{aligned} \quad (6.70)$$

The phasor diagram of the three phases are shown in Fig. 6.17 for the no-fault, faulty, and fault tolerated conditions.

Figure 6.17: Phasor diagrams of the three-phase 4-level inverter for different situations.

6.5 Results

In this section, the simulation results of fault diagnosis and fault tolerant control of a 4-level 3-phase inverter is described. Fig. 6.18 depicts the simulation model for the FDI and FTC for the 4-level 3-phase inverter.

Figure 6.18: Simulation model for FDI and FTC for a ML VSI.

Three gate control modules exist in this model, one for the normal operations, one for isolation purpose which implies the isolating modes, and the other one for controlling the inverter in the fault tolerant mode. The voltage signals of the three phases are monitored by the FDI module and after diagnosis of a fault, the control modes were changed so that only the healthy levels of voltage were obtained in the output.

Fig. 6.19 illustrates the gate signals of the faulty phase before and after diagnosis a fault in Q_6 . Since $G_6(t > t_f) = 1$, the fault tolerant control forces $G_5 = 0$ to open the

short-circuit loop in the third HB module of the inverter (Faulty module). Since after bypassing the faulty module one voltage level is missed, the SPWM control signals of a 3-level inverter were applied to the remaining modules. This reconfiguration ensures a perfect sinusoidal output.

Figure 6.19: Gates signals of a 3-phase 4-level cascade HB inverter with a fault in Q_6 .

Figure 6.20 shows the SPWM control signals of a 4-level inverter in the FTC mode. The resulting phase current and the digitized voltage signal of the faulty phase are illustrated in Fig. 6.21. As it can be seen in these figure, the FTC results in a sinusoidal current waveform with the same phase and reduced amplitude. In Figs. 6.22–6.26, The FDI algorithm has been applied to diagnose short-circuit switch faults in Q_1 – Q_5 .

Figure 6.20: PWM reference and carrier signals for a 4-level inverter under fault tolerant condition.

Figure 6.21: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_6 .

Figure 6.22: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_1 .

Figure 6.23: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_2 .

Figure 6.24: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_3 .

Figure 6.25: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_4 .

Figure 6.26: Phase current signals and voltage levels of a 3-phase 4-level cascade HB inverter with a fault in Q_5 .

The FTC has been successfully applied to all of the fault scenarios and a perfect sinusoidal waveform was obtained which has the same level of THD as the no-fault condition.

6.6 Summary

In this chapter, a fault tolerant control method was proposed to achieve maximum efficiency of the MLI in presence of a short-circuit fault in an n -level inverter. The simulations were carried on for a three-phase four-level HB cascade MLI. The results validated the efficiency of the proposed method.

Chapter 7

Conclusions and Recommendations for Further Research

7.1 Conclusion

Fault diagnosis for power electronic circuits is extremely important in the safety-critical systems. Semiconductor switches are critical components of the power electronic circuits. Existence of the switches in the circuit introduces mode changes in the system, thus, these circuits are hybrid in nature. There exist several modes of operation based on the switching states of a hybrid circuit. The mode of operation usually changes based on the operating condition and the load demand. Thus, in general, the operating mode of the system is unknown for the FDI module unless extra mode detectors and sensor are added to the system. Hence, FDI of the switching circuits is complicated and adding several sensors to a safety critical system is practically expensive, if not impossible.

In this thesis, VSP-based FDI method was proposed to diagnose switch faults in the VSIs with only one voltage detector per phase leg. The method was validated through simulations and experiments. The major achievements are as follow:

An input-output model of the three-phase inverter has been built based on the on–off state of its switches which describes the input-output behavior of the inverter in the healthy situation and in presence of short-circuit or open-circuit switch faults.

The time-variant effect of the PWM switching signals has been eliminated using non-equal adjacent switching states, resulting in a robust and accurate diagnosis. In

principle, the diagnosis module does not require the frequency of the carrier or reference signal or even the modulation index. Thus, this method is appropriate to be used in the inverters with closed-loop control such as VSDs where the frequency is changed by the operating conditions.

Dynamic patterns in the voltage space were introduced based on the non-equal adjacent switching states. It was shown that for a three-phase two-level inverter the VSP constructs a cube in the voltage space, and the VSP is disturbed in the faulty situations. Hence, by monitoring the VSP for a period of time the faulty switch was isolated using the fault signature sets. In this thesis, the VSP was obtained from the digitized quantities of the pole voltages. However, the concept of VSP can be used for the continuous quantities. Since there exists a kind of symmetry in the three-phase quantities, the parameters that affect the three phases identically, do not change the VSP overall shape. For example, if a rise in the ambient temperature occurs, all of the switches reflect identically; hence, again a symmetric cubic pattern will be obtained in the voltage space. However, if a temperature rise occurs in only one of the switches the cubic pattern will be distorted. Thus, by monitoring the centroid of the VSP, the incipient switch faults can also be detected. Thus, the VSP can be used for prognosis of the switch faults.

The VSP-based FDI algorithm was developed and implemented in MATLAB Simulink. The FBZs were calculated automatically given the topology of the inverter. The switch faults were isolated based on the measurements of the phase voltage outputs. The algorithm includes a digitization state which is a prerequisite to calculate the switching states. Then the switch transitions were extracted, and the FDI window was formed. The FDI algorithm compared finite number of non-equal adjacent switching states with the FBZs and isolated the faulty switch.

Two experimental set-ups were designed and built to simulate abrupt switch faults in 6-switch and 12-switch three-phase inverters. The switches control and FDI blocks were implemented in MATLAB Simulink and the inverter was implemented in a hardware-in-loop configuration using MATLAB real time windows target. The diagnostic tests were run on-line, and the switch faults were diagnosed successfully within only one switching period.

Several simulation and experiments were run and the efficiency of the VSP-based FDI method was investigated. The performance of this method was validated for a three-phase VSI which was used as the drive of a PMSM motor. It is shown that the disturbances in the mechanical load of the motor does not affect the FDI result and all of the six switch faults are isolated quickly. Isolation of open-circuit and short-circuit faults in a six-switch inverter are investigated and the VSP were derived. The FDI time is calculated for every experiment.

A fast diagnosis Time was achieved which was validated through simulations and experiments; VSP based FDI was implemented with the on-line set-up and the fault were inserted automatically at a given time instance. The FDI module could successfully detect the faulty switch and its location in less than one switching period which is significantly faster than the conventional current-based FDI methods.

The number of required sensors for FDI purpose is extremely low. Only one voltage detector per phase leg was used for a MLI with large number of switches. In some circuits, the pole voltages are available for control reason which can also be used for the FDI purpose without adding extra detectors. FDI with no or less additional sensors is a requisition by the mobile applications such as e-vehicles, robotics, and space applications.

The structural model of the three-phase VSI was modified and extended to model n -level m -phase cascade inverters. This modeling allows definition of the operating modes based on the switching states for normal and faulty situations.

It was shown how to calculate the proper switching modes of a n -level m -phase cascade inverter. The proper modes of the inverter were defined as the modes which allow obtaining all the healthy levels of the inverter in the output, and in the meantime guarantee the isolability of the switch faults. Using the proper modes of the system, the location of the faulty switch out of $m \times (n - 1)$ switches were isolated with only one voltage detector per phase.

An algorithm was developed to define the fault signatures of each switch and to detect and isolate a faulty switch of a n -level m -phase cascade inverters. In this method, the faults were diagnosed independently for each phase leg, and the diagnosis time

is only $n \times T_s$, where T_s is the sampling time of the measurement. This method was validated in Matlab Simulink for 4-level inverter with 18 switches.

After the switch faults were successfully isolated, a fault tolerant control strategy was applied to control the inverter in the faulty condition. The FTC method achieved three results; protecting the other devices of the inverter, reducing the THD of the sinusoidal signal of the fault leg, and balancing the line voltage.

7.2 Recommendations for Further Research

In this thesis, the VSP-based method has been described for the SPWM method which is a high frequency modulation technique. However, this method can be extended to address inverters with other modulation techniques. For a general modulation technique, a fixed length fault detection windows can be applied. The knowledge about the inverter circuit and the modulation technique can help to achieve the length of the fault detection window. The fault-banned zones and the VSPs will remain unchanged and a similar fault isolation algorithm can be applied for other modulation techniques.

In this thesis, only the single faults were considered. The VSP can easily be applied to detect multiple faults as well. While FBZ of a single fault refers to a face of the cubic pattern in the voltage space, the FBZ of multiple faults refers to the edges and vertexes of the cubic pattern which can be studied in details in future. Also, the application of VSP for detecting other types of faults such as incipient faults, aging, and degradation of semiconductor switches and diodes can be studied in future. In this case, the patterns might be needed to be analyzed in a continuous space rather than digitized one.

Interestingly, the VSP can be used for the prognosis purpose. If the degradation can be modeled and the effect of the degradation of a component appears in the VSP, then it is possible to define prognostic patterns. Especially for prognosis of systems with identical components, the pattern based prognosis can be helpful. For example, in a six-switch inverter, there exist six identical switches. The operating condition, noise, variation of internal switch parameter due to temperature, and so on will be almost the

same for all of the switches. Hence, only an abnormal behavior of a faulty component can distort the symmetry of the VSP. By modeling the degradation and relating them to some of the properties of VSP such as centroid of the VSP, the degrading component can be located. The dynamic behavior of the VSP can be used to predict the remaining useful lifetime (RUL) of the degrading system.

This thesis focused on the FDI for the power electronic systems using VSP. For diagnosis of load side faults, such as motor windings, the current waveforms will be affected. Thus, the current space patterns can be investigated and used for diagnosis and prognosis of mechanical faults in motor drive applications. Building a proper model for each faulty component and relating them to the current space patterns can be investigated in future.

To locate the faulty switch, only one voltage detectors is needed per phase leg. It might be possible to use the built-in voltage detectors of the switch driver IC and implement the FDI software inside the driver IC without adding extra voltage detectors. Thus, motor drive ICs with fault detection, isolation, and fault tolerant capabilities can be available and the FDI and FTC of motor drives and MLIs can be standardized without additional detectors.

Publications

1. **M. Alavi**, D. Wang, and M. Luo, "Short-Circuit Fault Diagnosis for Three-Phase Inverters based on Voltage Space Patterns", *IEEE Trans. Ind. Electron.*, vol. 61, pp. 5558–5569, Oct. 2014.
2. **M. Alavi**, D. Wang, and M. Luo, "Open-Circuit Fault Diagnosis for Three-Phase Inverters based on Voltage Space Patterns", *IEEE Trans. Power. Electron.*, TPEL-Reg-2015-01-0053 submitted, Jan 2015.
3. **M. Alavi**, D. Wang, and M. Luo, "Switch Fault Diagnosis for Multi-Level Multi-Phase Voltage Source Inverters", *IEEE ISIE 2014*, ED-012319, accepted, Jan 2014.
4. **M. Alavi**, D. Wang, and M. Luo, "Fault Diagnosis in Voltage-Fed PWM Motor Drives based on Discrete Voltage States", in *Proc. IEEE IECON 2013*, Vienna, AUSTRIA, Nov. 2013.
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Appendices

IRF620, SiHF620

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.80
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.9	
Configuration	Single

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF620PbF
	SiHF620-E3
SnPb	IRF620
	SiHF620

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	200	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	5.2	A
		T _C = 100 °C		3.3	
Pulsed Drain Current ^a			I _{DM}	18	
Linear Derating Factor				0.40	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	110	mJ
Repetitive Avalanche Current ^a			I _{AR}	5.2	A
Repetitive Avalanche Energy ^a			E _{AR}	5.0	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	50	W
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)		for 10 s		300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 6.1\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 5.2\text{ A}$ (see fig. 12).
 c. $I_{SD} \leq 5.2\text{ A}$, $dI/dt \leq 95\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
 d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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IRF620, SiHF620

Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{GS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.29	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.1 A ^b	-	-	0.80	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.1 A		1.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	260	-	pF
Output Capacitance	C _{oss}			-	100	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.8 A, V _{DS} = 160 V, see fig. 6 and 13 ^b	-	-	14	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	7.9	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 4.8 A, R _g = 18 Ω, R _D = 20 Ω, see fig. 10 ^b		-	7.2	-	ns
Rise Time	t _r			-	22	-	
Turn-Off Delay Time	t _{d(off)}			-	19	-	
Fall Time	t _f			-	13	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	18	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 5.2 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.8 A, dI/dt = 100 A/μs		-	150	300	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.91	1.8	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

IRF620, SiHF620

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

IRF620, SiHF620

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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area

IRF620, SiHF620

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Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

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Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

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Fig. 14 - For N-Channel

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IR2130/IR2132(J)(S) & (PbF)

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
 Fully operational to +600V
 Tolerant to negative transient voltage
 dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Cross-conduction prevention logic
- Also available LEAD-FREE

Description

The IR2130/IR2132(J)(S) is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain **FAULT** signal indicates if an over-current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Product Summary

V_{OFFSET}	600V max.
I_{o+/-}	200 mA / 420 mA
V_{OUT}	10 - 20V
t_{on/off} (typ.)	675 & 425 ns
Deadtime (typ.)	2.5 μs (IR2130) 0.8 μs (IR2132)

Packages

Typical Connection

IR2130/IR2132(J)(S) & (PbF)

International
IR Rectifier

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{S0} . The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 50 through 53.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	625	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	$V_{CC} - 25$	$V_{CC} + 0.3$	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic Input Voltage ($HIN1,2,3$, $LIN1,2,3$ & ITRIP)	$V_{SS} - 0.3$	$(V_{SS} + 15)$ or $(V_{CC} + 0.3)$ whichever is lower	
V_{FLT}	FAULT Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CAO}	Operational Amplifier Output Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$	—	1.5	W
	(28 Lead DIP)	—	1.6	
	(28 Lead SOIC)	—	2.0	
	(44 Lead PLCC)	—	83	$^\circ\text{C/W}$
R_{thJA}	Thermal Resistance, Junction to Ambient	—	78	
	(28 Lead DIP)	—	63	
	(28 Lead SOIC)	—	150	
T_J	Junction Temperature	—	150	$^\circ\text{C}$
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0} . The V_S offset rating is tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figure 54.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3} + 10$	$V_{S1,2,3} + 20$	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($HIN1,2,3$, $LIN1,2,3$ & ITRIP)	V_{SS}	$V_{SS} + 5$	
V_{FLT}	FAULT Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	$V_{SS} + 5$	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	$V_{SS} + 5$	
T_A	Ambient Temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of ($V_{S0} - 5V$) to ($V_{S0} + 600V$). Logic state held for V_S of ($V_{S0} - 5V$) to ($V_{S0} - V_{BS}$).

(Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, $CA-$ and CAO pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} , C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 3 through 5.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	11	500	675	850	ns	$V_{IN} = 0$ & 5V $V_{S1,2,3} = 0$ to 600V
t_{off}	Turn-Off Propagation Delay	12	300	425	550		
t_r	Turn-On Rise Time	13	—	80	125		
t_f	Turn-Off Fall Time	14	—	35	55		
t_{trip}	ITRIP to Output Shutdown Prop. Delay	15	400	660	920		V_{IN} , $V_{ITRIP} = 0$ & 5V
t_{bl}	ITRIP Blanking Time	—	—	400	—		$V_{ITRIP} = 1V$
t_{fit}	ITRIP to FAULT Indication Delay	16	335	590	845		V_{IN} , $V_{ITRIP} = 0$ & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	—	310	—		$V_{IN} = 0$ & 5V
t_{ftr}	LIN1,2,3 to FAULT Clear Time	17	6.0	9.0	12.0	μs	V_{IN} , $V_{ITRIP} = 0$ & 5V
DT	Deadtime (IR2130) (IR2132)	18	1.3 0.4	2.5 0.8	3.7 1.2		$V_{IN} = 0$ & 5V
SR+	Operational Amplifier Slew Rate (+)	19	4.4	6.2	—	V/μs	
SR-	Operational Amplifier Slew Rate (-)	20	2.4	3.2	—		

NOTE: For high side PWM, HIN pulse width must be $\geq 1.5\mu\text{sec}$

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	21	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	22	—	—	0.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	23	400	490	580	mV	
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	24	—	—	100		$V_{IN} = 0V$, $I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	25	—	—	100	μA	$V_{IN} = 5V$, $I_O = 0A$
I_{LK}	Offset Supply Leakage Current	26	—	—	50		$V_B = V_S = 600V$
I_{OBS}	Quiescent V_{BS} Supply Current	27	—	15	30	mA	$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	28	—	3.0	4.0		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	29	—	450	650	μA	$V_{IN} = 0V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	30	—	225	400		$V_{IN} = 5V$
I_{ITRIP+}	"High" ITRIP Bias Current	31	—	75	150	nA	ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	32	—	—	100		ITRIP = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	33	7.5	8.35	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	34	7.1	7.95	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	35	8.3	9.0	9.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	36	8.0	8.7	9.4		
$R_{on,FLT}$	FAULT Low On-Resistance	37	—	55	75	Ω	

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Static Electrical Characteristics -- Continued

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $HIN1,2,3$ & $LIN1,2,3$. The V_O and I_O parameters are referenced to $V_{S0,1,2,3}$ and are applicable to the respective output leads: $HO1,2,3$ or $LO1,2,3$.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
I_{O+}	Output High Short Circuit Pulsed Current	38	200	250	—	mA	$V_O = 0V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	39	420	500	—		$V_O = 15V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
V_{OS}	Operational Amplifier Input Offset Voltage	40	—	—	30	mV	$V_{S0} = V_{CA-} = 0.2V$
I_{CA-}	CA- Input Bias Current	41	—	—	4.0	nA	$V_{CA-} = 2.5V$
CMRR	Op. Amp. Common Mode Rejection Ratio	42	60	80	—	dB	$V_{S0} = V_{CA-} = 0.1V$ & $5V$
PSRR	Op. Amp. Power Supply Rejection Ratio	43	55	75	—		$V_{S0} = V_{CA-} = 0.2V$ $V_{CC} = 10V$ & $20V$
$V_{OH,AMP}$	Op. Amp. High Level Output Voltage	44	5.0	5.2	5.4	V	$V_{CA-} = 0V$, $V_{S0} = 1V$
$V_{OL,AMP}$	Op. Amp. Low Level Output Voltage	45	—	—	20	mV	$V_{CA-} = 1V$, $V_{S0} = 0V$
$I_{SRC,AMP}$	Op. Amp. Output Source Current	46	2.3	4.0	—	mA	$V_{CA-} = 0V$, $V_{S0} = 1V$ $V_{CAO} = 4V$
$I_{SRC,AMP}$	Op. Amp. Output Sink Current	47	1.0	2.1	—		$V_{CA-} = 1V$, $V_{S0} = 0V$ $V_{CAO} = 2V$
$I_{O+,AMP}$	Operational Amplifier Output High Short Circuit Current	48	—	4.5	6.5		$V_{CA-} = 0V$, $V_{S0} = 5V$ $V_{CAO} = 0V$
$I_{O-,AMP}$	Operational Amplifier Output Low Short Circuit Current	49	—	3.2	5.2		$V_{CA-} = 5V$, $V_{S0} = 0V$ $V_{CAO} = 5V$

Lead Assignments

<p>28 Lead PDIP</p>	<p>44 Lead PLCC w/o 12 Leads</p>	<p>28 Lead SOIC (Wide Body)</p>
IR2130 / IR2132	IR2130J / IR2132J	IR2130S / IR2132S
Part Number		

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Functional Block Diagram

Lead Definitions

Symbol	Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
LIN1,2,3	Logic inputs for low side gate driver output (LO1,2,3), out of phase
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
VCC	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
VSS	Logic ground
Vb1,2,3	High side floating supplies
HO1,2,3	High side gate drive outputs
Vs1,2,3	High side floating supply returns
LO1,2,3	Low side gate drive outputs
Vs0	Low side return and positive input of current amplifier

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Figure 1. Input/Output Timing Diagram

Figure 2. Floating Supply Voltage Transient Test Circuit

Figure 3. Deadtime Waveform Definitions

Figure 4. Input/Output Switching Time Waveform Definitions

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Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

Figure 5.5 Input Filter Function

Figure 6. Diagnostic Feedback Operational Amplifier Circuit

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Figure 7. Operational Amplifier Slew Rate Measurement

Figure 8. Operational Amplifier Input Offset Voltage Measurement

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

Figure 11A. Turn-On Time vs. Temperature

Figure 11B. Turn-On Time vs. Supply Voltage

Figure 11C. Turn-On Time vs. Voltage

Figure 12A. Turn-Off Time vs. Temperature

Figure 12B. Turn-Off Time vs. Supply Voltage

Figure 12C. Turn-Off Time vs. Input Voltage

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Figure 13A. Turn-On Rise Time vs. Temperature

Figure 13B. Turn-On Rise Time vs. Voltage

Figure 14A. Turn-Off Fall Time vs. Temperature

Figure 14B. Turn-Off Fall Time vs. Voltage

Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

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Figure 16A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

Figure 16B. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Voltage

Figure 17A. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Temperature

Figure 17B. $\overline{\text{LIN1,2,3}}$ to $\overline{\text{FAULT}}$ Clear Time vs. Voltage

Figure 18A. Deadtime vs. Temperature (IR2130)

Figure 18B. Deadtime vs. Voltage (IR2130)

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Figure 18C. Deadtime vs. Temperature (IR2132)

Figure 18D. Deadtime vs. Voltage (IR2132)

Figure 19A. Amplifier Slew Rate (+) vs. Temperature

Figure 19B. Amplifier Slew Rate (+) vs. Voltage

Figure 20A. Amplifier Slew Rate (-) vs. Temperature

Figure 20B. Amplifier Slew Rate (-) vs. Voltage

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Figure 21A. Logic “0” Input Threshold vs. Temperature

Figure 20B. Logic “0” Input Threshold vs. Voltage

Figure 22A. Logic “1” Input Threshold vs. Temperature

Figure 22B. Logic “1” Input Threshold vs. Voltage

Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

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Figure 24A. High Level Output vs. Temperature

Figure 24B. High Level Output vs. Voltage

Figure 25A. Low Level Output vs. Temperature

Figure 25B. Low Level Output vs. Voltage

Figure 26A. Offset Supply Leakage Current vs. Temperature

Figure 26B. Offset Supply Leakage Current vs. Voltage

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Figure 27A. V_{BS} Supply Current vs. Temperature

Figure 27B. V_{BS} Supply Current vs. Voltage

Figure 28A. V_{CC} Supply Current vs. Temperature

Figure 28B. V_{CC} Supply Current vs. Voltage

Figure 29A. Logic "1" Input Current vs. Temperature

Figure 29A. Logic "1" Input Current vs. Voltage

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Figure 30A. Logic "0" Input Current vs. Temperature

Figure 30B. Logic "0" Input Current vs. Voltage

Figure 31A. "High" ITRIP Current vs. Temperature

Figure 31B. "High" ITRIP Current vs. Voltage

Figure 32A. "Low" ITRIP Current vs. Temperature

Figure 32B. "Low" ITRIP Current vs. Voltage

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Figure 33. V_{BS} Undervoltage (+) vs. Temperature

Figure 34. V_{BS} Undervoltage (-) vs. Temperature

Figure 35. V_{CC} Undervoltage (+) vs. Temperature

Figure 36. V_{CC} Undervoltage (-) vs. Temperature

Figure 37A. $\overline{FAULT}$ Low On Resistance vs. Temperature

Figure 37B. $\overline{FAULT}$ Low On Resistance vs. Voltage

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Figure 38A. Output Source Current vs. Temperature

Figure 38B. Output Source Current vs. Voltage

Figure 39A. Output Sink Current vs. Temperature

Figure 39B. Output Sink Current vs. Voltage

Figure 40A. Amplifier Input Offset vs. Temperature

Figure 40B. Amplifier Input Offset vs. Voltage

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Figure 41A. CA- Input Current vs. Temperature

Figure 41B. CA- Input Current vs. Voltage

Figure 42A. Amplifier CMRR vs. Temperature

Figure 42B. Amplifier CMRR vs. Voltage

Figure 43A. Amplifier PSRR vs. Temperature

Figure 43B. Amplifier PSRR vs. Voltage

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Figure 44A. Amplifier High Level Output vs. Temperature

Figure 44B. Amplifier High Level Output vs. Voltage

Figure 45A. Amplifier Low Level Output vs. Temperature

Figure 45B. Amplifier Low Level Output vs. Voltage

Figure 46A. Amplifier Output Source Current vs. Temperature

Figure 46B. Amplifier Output Source Current vs. Voltage

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Figure 47A. Amplifier Output Sink Current vs. Temperature

Figure 47B. Amplifier Output Sink Current vs. Voltage

Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

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Figure 50. Maximum VS Negative Offset vs. V_{BS} Supply Voltage

Figure 51. IR2130/IR2132 T_J vs. Frequency (IRF820)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

Figure 52. IR2130/IR2132 T_J vs. Frequency (IRF830)
 $R_{GATE} = 20\Omega$, $V_{CC} = 15V$

Figure 53. IR2130/IR2132 T_J vs. Frequency (IRF840)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

Figure 54. IR2130/IR2132 T_J vs. Frequency (IRF450)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

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Figure 55. IR2130J/IR2132J
T_J vs. Frequency (IRGPC20KD2)
R_{GATE} = 33Ω, V_{CC} = 15V

Figure 56. IR2130J/IR2132J
T_J vs. Frequency (IRGPC30KD2)
R_{GATE} = 20Ω, V_{CC} = 15V

Figure 57. IR2130J/IR2132J
T_J vs. Frequency (IRGPC40KD2)
R_{GATE} = 15Ω, V_{CC} = 15V

Figure 58. IR2130J/IR2132J
T_J vs. Frequency (IRGPC50KD2)
R_{GATE} = 10Ω, V_{CC} = 15V

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Case outline

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LEADFREE PART MARKING INFORMATION

ORDER INFORMATION

Basic Part (Non-Lead Free)

28-Lead PDIP IR2130 order IR2130
 28-Lead SOIC IR2130S order IR2130S
 28-Lead PDIP IR2132 order IR2132
 28-Lead SOIC IR2132S order IR2132S
 44-Lead PLCC IR2130J order IR2130J
 44-Lead PLCC IR2132J order IR2132J

Leadfree Part

28-Lead PDIP IR2130 order IR2130PbF
 28-Lead SOIC IR2130S order IR2130SPbF
 28-Lead PDIP IR2132 order IR2132PbF
 28-Lead SOIC IR2132S order IR2132SPbF
 44-Lead PLCC IR2130J order IR2130JPbF
 44-Lead PLCC IR2132J order IR2132JPbF

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This product has been qualified per industrial level
 Data and specifications subject to change without notice. 4/2/2004

Application Note AN-985

Six-Output 600V MGDs Simplify 3-Phase Motor Drives

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Traditionally the functions described above have required discrete circuits of some complexity but International Rectifier's IR213X series six-channel gate drivers perform all the requirements for interfacing logic level control circuits to high power MOS-gated devices in high-side/ low-side switch configurations using up to six devices.

APPLICATION NOTE

AN-985

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Six-Output 600V MGDs Simplify 3-Phase Motor Drives

1. Gate Drive Requirements

MOS-gated transistors commonly used in motor drives, UPS and converters operating at dc bus voltages up to 600VDC require voltage drive in order to achieve a saturated "ON" state condition. The drive signal must have the following characteristics:

- 1) An amplitude of 10V to 15V.
- 2) A low source resistance for rapid charge and discharge of the gate capacitance.
- 3) A floating output so that high side switches can be driven.

In addition to the above requirements the actual driver should be capable of driving combinations of devices in both low-side and high-side switch configurations. With this in mind the driver should also provide the following:

- 1) Low internal power loss at high switching frequency and maximum offset voltage.
- 2) Accept ground referenced logic level input signals.
- 3) Protect the power switch from damage by clamping the gate signal to the low state in the event of gate undervoltage or overvoltage or if the load current exceeds a predetermined peak value.
- 4) Protect the power switch by clamping the signal to the low state if the signal inputs are disconnected.

Traditionally the functions described above have required discrete circuits of some complexity but International Rectifier's IR213X series six-channel gate drivers perform all the requirements for interfacing logic level control circuits to high power MOS-gated devices in high-side/ low-side switch configurations using up to six devices.

2. IR213x Block Diagram

As shown in Figure 1 the I.C. consists of six output drivers which receive their inputs from the three input signal generator blocks each providing two outputs. The three low-side output drivers are driven directly from the signal generators L1, L2 and L3 but the high-side drive signals H1, H2 and H3 must be level shifted before being applied to the high-side output drivers.

An undervoltage detector circuit monitoring the VCC level provides an input to inhibit the six outputs of the signal generator circuits. In addition, there are individual undervoltage lockout circuits for the high-side outputs should any of the floating bias supplies fall below a predetermined level.

The ITRIP signal which can be derived from a current sensor in the main power circuit of the equipment (current transformer, viewing resistor, etc.) is compared with a 0.5volt reference and is then "OR-ed" with the UV signal to inhibit the six signal generator outputs.

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The diagram illustrates the internal logic of the 74VHC163 3-bit binary counter, including fault detection and under-voltage protection features. The circuit is organized into three main sections: input logic, counting logic, and output logic.

Input Logic: The inputs HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3 are connected to three 3-input AND gates. The outputs of these AND gates are connected to the H1, H2, and H3 inputs of three Input Signal Generators (ISGs). The ISGs are also connected to the L1, L2, and L3 inputs of three Pulse Generator Level Shifters (PGLSs). The PGLSs are connected to the SET and RESET inputs of three Latches. The Latches are connected to the UV DETECTOR inputs of three Drivers. The Drivers are connected to the V_B, V_S, and V_{LS} outputs.

Counting Logic: The LIN1, LIN2, and LIN3 inputs are connected to the counting inputs of the three ISGs. The HIN1, HIN2, and HIN3 inputs are connected to the H1, H2, and H3 inputs of the three ISGs. The ISGs are connected to the L1, L2, and L3 inputs of the three PGLSs. The PGLSs are connected to the SET and RESET inputs of the three Latches. The Latches are connected to the UV DETECTOR inputs of the three Drivers. The Drivers are connected to the V_B, V_S, and V_{LS} outputs.

Fault Detection: The FAULT input is connected to the CLEAR LOGIC block. The CLEAR LOGIC block is connected to the CLEAR input of the three ISGs. The FAULT input is also connected to the FAULT LOGIC block. The FAULT LOGIC block is connected to the FAULT output. The FAULT output is connected to the FAULT input of the three ISGs.

Under-Voltage Protection: The ITRIP input is connected to the 0.5V input of the CURRENT COMPARATOR. The CAO input is connected to the non-inverting input of the CURRENT AMP. The CA- input is connected to the inverting input of the CURRENT AMP. The CURRENT AMP is connected to the UNDER-VOLTAGE DETECTOR. The UNDER-VOLTAGE DETECTOR is connected to the UNDER-VOLTAGE input of the three ISGs.

Outputs: The outputs of the three Drivers are connected to the V_B, V_S, and V_{LS} outputs. The outputs of the three Drivers are also connected to the LO, LO, and LO outputs.

Figure 1. Functional block diagram of the IR2130/2132 drivers.

2.1. Input Control Logic

Internal 50k pull-up resistors to V_{CC} ensure that all outputs are low if the inputs are open-circuited. Inputs are TTL and CMOS compatible with V_{IH} set at 2.2V and V_{IL} at 0.8V. A 500 nsec input filter prevents spurious triggering from fast noise pulses. The input logic circuitry also provides deadtime to avoid overlap when nearly coincident transitions take place at the LIN and HIN input pins in the same channel. This is illustrated in Figure 2.

Timing diagram showing the input filter time (T_{fil}) and deadtime (T_{dt}) for the MOSFET driver. The signals shown are LIN1, HIN1, LO1, and HO1z. The input filter time is approximately $0.3\mu s$ and the deadtime is approximately $1.2\mu s$.

INPUT FILTER TIME : $T_{fil} \sim 0.3\mu s$
 DEADTIME : $T_{dt} \sim 1.2\mu s$

Figure 2. Input to output timing diagram for IR2130/2132 only

For some applications such as variable reluctance drives it is necessary to enable the high side and low side outputs simultaneously. The logic circuitry of the IR2131 allows this (see table 2) and permits any output condition determined only by the 6 input logic levels.

HIN	LIN	HO	LO
1	1	0	0
1	0	0	1
0	1	1	0
0	0	0	0

Table 1. IR2130, IR2132 Truth table for each input/output pair

HIN	LIN	HO	LO
1	1	0	0
1	0	0	1
0	1	1	0
0	0	1	1

Table 2. IR2131 Truth table for each input/output pair

2.2 Protection Circuits and Fault Reporting

2.2.1 UV Protection

An undervoltage condition on the V_{CC} level, defined as less than 8.9V (as V_{CC} is reduced) and less than 9.3V nominal (as V_{CC} is increased) causes all outputs to shutdown (see Section 2.2.3).

With V_{CC} at around 9 volts the drivers provide marginally adequate drive voltages to ensure full enhancement of the power switches for most applications. Separate UV lockout circuits are provided on the three high-side outputs. They also have a 0.4V hysteresis band with levels of 8.3 volts for a falling bias voltage and 8.7 volts for a rising voltage. Unlike the V_{CC} UV circuit they inhibit only their particular high-side output and do not affect the operation of any other output.

2.2.2 Current Trip

In the event of a shoot-through current or an output overload it is desirable to terminate all the output signals from the driver. This is accomplished through a current comparator circuit which monitors the voltage drop across a low side viewing resistor and compares it with a 0.5 volt reference level. The current comparator output is "OR-ed" with the V_{CC} UV circuit output (2.2.1) so that a fault condition of either type causes the fault logic circuit to actuate.

2.2.3 Fault Logic

This circuit consists of a latch which is set by the conditions described in 2.2.2 and is reset by holding all three low-side inputs high for more than 10 microseconds or by recycling the V_{CC} bias supply. When the fault latch is set it produces two output signals. One is used to inhibit all three input signal generator circuits thus inhibiting all six outputs. The other output signal appears as a fault indicator which goes low in the presence of a fault condition as defined in 2.2.2. The active low condition can drive an LED fault indicator or external logic circuit.

Figure 3. Current Amplifier Operation with Triangular Waveform Input

2.2.4 Current Sensing in IR2130, IR2132

Using the same current viewing resistor described in 2.2.2 the current sense voltage of 0-0.5V is amplified in the current amplifier to generate a 0-5V analog function for processing in an external control circuit.

In actual operation the voltage difference between the V_{S0} and V_{SS} pins forms the input voltage for the noninverting amplifier although only the positive current (V_{S0} positive WRT V_{SS}) is measured. Two resistors R_f and R_{IN} set the gain of the amplifier as shown in Figure 3.

Actual voltage gain is given by the relationship

$$A = \frac{R_f + R_{IN}}{R_{IN}}$$

for a gain of 10 with $R_{IN} = 1k$:

$$10 = \frac{R_f + 1K}{1K}$$

$$R_f + 1K = 10K$$

$$R_f = 9K$$

Power for the current amplifier is supplied from V_{CC} .

The shape of the current seen in the DC link will depend on the switching topology used for the three phase bridge. Two such topologies are the "Six Step Inverter" and the "Pulse Width Modulated Inverter". Suffice to say that for reasonable load levels at moderate to high power factors the DC link current will always be a positive value. Any negative current passed back through the free wheeling diodes in the bridge due to the lagging current will be absorbed in the bridge and not appear in the DC link.

At light or low power factor loads the negative current levels will begin to exceed the positive demands in the bridge and a net negative current will flow in the DC link. The same will occur if the load is caused to regenerate back into the system.

Figure 4. Current Amplifier Operation with Triangular Waveform Input

The output of the amplifier will not provide a negative voltage. This means that any negative current excursions in the DC link through the current sensing resistor will not appear at the output of the amplifier. This loss of information is further compounded by a characteristic of the amplifier that is not obvious from the data sheet. A recovery delay exists in the current sense amplifier operation as the input signal changes from a negative to a positive value.

The loss of negative input signals and the recovery delay of the amplifier is illustrated in Figure 4 where a triangular input was used as an example. The length of the delay is related to the dv/dt at the zero crossover of the input signal. As described earlier, negative inputs to the current sense amplifier are possible at light and low power factor loads. These negative excursions of current will be lost by the current amplifier.

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The recovery delay of the amplifier is due to the V_{s0} input pin to the amplifier saturating when a negative voltage is applied. The charge accumulated requires time to be removed or dissipated before the amplifier will begin to function correctly. The only method to stop this recovery delay time is to inhibit the V_{s0} input voltage from going negative.

The input voltage will generally be of a small magnitude (less than 1 volt) since it is desirable to minimize the losses across the current sensing resistor and not introduce excessive voltages that will upset the drive circuitry. Such a small voltage signal is unsuitable for diode clipping.

Figure 5 shows one way of preventing the non-inverting input to the amplifier from going negative. If a differential amplifier is used with a voltage reference to shift the effective zero current reference input signal, the output will appear as an amplified version of the input signal, offset by some positive voltage.

The relevant calculations for the selection of components for the given circuit are given in Appendix 1. It can be seen that the choice of components is limited by the total amount of resistance allowed in the gate loop, and the maximum current that can be sourced by the internal amplifier.

For those motor drives that do not use co-pak IGBTs, it is a relatively simple operation to prevent the negative component of dc link current from flowing into the current sensing resistor. The circuit in Figure 6 shows an implementation of this technique in a bridge that utilizes IGBTs. When MOSFETs are used as the switching devices an additional diode is required in series with each MOSFET to negate the internal body-drain diode.

Another possibility, suitable for lower power applications is shown in Figure 7.

Negative current components are blocked by the shunt resistor diode and forced through a second rated parallel diode. Schottky diodes are suitable for this application.

Note: The IR2131 does not have an analog current amplifier.

2.3 Output Drivers

The International Rectifier 213X family has six output drivers, three referenced to V_{s0} and three floating drivers capable of operating with offset voltages up to 600V positive to V_{s0} . All outputs have inverted logic, i.e., they go positive when the corresponding LIN or HIN goes low unless there is an over-riding fault condition (see 2.2.3). The output current is typically 0.25A on the positive edge and 0.5A on the negative edge of the output pulse, and when driving a typical MOS gate of 1000pF results in a maximum risetime of 100 nsec and falltime of 50 nsec.

Figure 2 shows the time relationship between input and output waveforms for the IR2130, IR2132. The input filter delay is typically 300 nsec and the deadtimes are 1.5 msec minimum and 2.0 msec maximum for the IR2130 and 700 ns for the IR2131.

Figure 5. Different Amplifier with Voltage Offset

Figure 6. Measurement of Positive Current Components in the DC Link

Because of the current amplifier requirements and to increase noise immunity between the power ground and the ground reference of the logic circuits, the V_{S0} to V_{SS} offset voltage capability is bi-directional at $\pm 5V$.

When driving inductive loads the V_{S1} , V_{S2} and V_{S3} terminals are driven negative with respect to V_{S0} as inductive energy is commutated by the diodes across each low side power switch. For this reason the total offset capability is specified as -5V to +600V. The -5V spec is needed to accommodate instantaneous diode drops due to forward recovery as well as inductive effects of high current wiring, etc.

During long pulses, with the bootstrap capacitors supplying all the energy for the floating drivers, the capacitors gradually discharge until at 8.3 volts nominal the UV detector shuts down the output and prevents the power switch from overdissipating.

- 1) Using larger bootstrap capacitors.
- 2) Refreshing bootstrap charge by momentarily turning off and reapplying input command pulse.
- 3) Providing continuous bias from floating dc power supplies.

3.0 APPLICATION GUIDELINES

3.1 Bootstrap and Decoupling Capacitors

Three bootstrap capacitors are required to supply power for the floating outputs of the driver, the values of which are a function of the gate charge requirements of the power switch and the maximum power switch "ON" times.

The internal floating driver current also must be supplied from the bootstrap capacitors. After all these energy requirements have been met there must still be enough charge remaining on C_{BOOT} to avoid UV shutdown (8.3V nominal).

Example:

What is the maximum t_{ON} under the following conditions?

If V_{CC} = 15V and the charging of the bootstrap capacitor occurs when V_{S0} = -1.0V and V_F of the bootstrap diode is 1.0V we have a net voltage on C_{BOOT} of 15Vdc. Let us also assume that we are using a #5 size power switch such as an IRF450 or IRGPC50U either of which require a total gate charge of around 0.12 mC and that we want to maintain a C_{BOOT} of 0.1pF at a minimum voltage of 10Vdc:

during discharge $\Delta v = 5V$

$$Q_{AVAIL} = CV = 0.1 \times 10^{-6} \times 5 \text{ Volts} = 0.5 \text{ mC}$$

$$Q_{REQD} = 0.12 \text{ mC} \quad (\text{See data sheet IRF450 or IRGPC50U})$$

Hence, having supplied the gate charge, the gate voltage is 13.8 V (0.38 mC). From the point on, a constant leakage current I_{QBS} = 15 μ A discharges the bootstrap capacitor. The time it takes for the bootstrap capacitor to discharge to 10 V can be calculated as follow:

$$\Delta t = C \times \Delta v / I = 0.1 \mu F \times 3.8 V / 15 \mu A = 25 \text{ ms.}$$

The above calculation neglects the leakage current in the bootstrap diode, which must be a fast recovery type to avoid discharging C_{BOOT} as the diode starts to block voltage.

In practice, as indicated in INT-978 Section 5, it is not advisable to use a bootstrap capacitor smaller than 0.47 μ F

In terms of decoupling requirements, a capacitor at least 10X the value of C_{BOOT} is required from V_{CC} to V_{SS} to provide adequate charging current for C_{BOOT} and also to minimize voltage transients on the V_{CC} supply resulting from these currents.

3.2 Power Dissipation

The drivers have a "fault" output on pin 8 which is really an open drain MOSFET with its source connected to V_{SS} (pin 12) . The intrinsic diode of this MOSFET has a negative temperature coefficient of V_f almost exactly equal to -0.002V/°C. Thus we have a "built-in" thermometer to monitor die temperature using a -1mA constant current supply to pin 8.

Actual die temperatures are dependent on frequency of operation, the offset voltage (HVDC bus voltage) and the capacitance of the MOS-gated power switches being driven. The value of the series gate resistors also determines overall switch loss but has little effect on the driver temperature. A detailed analysis of losses in MGDs can be found in INT-978 Section 4.

Curves of junction temperature using various 500-volt MOSFETs and gate resistors versus switching frequency are to be found in the individual date sheets for the IR213X series of MOS gate drivers.

4.0 LAYOUT GUIDELINES

The driver forms the interface between the low level logic circuitry and the high power switching devices. It follows then that signal grounds and high power returns should not be mixed together indiscriminately but should follow carefully formulated rules so that crosstalk problems can be avoided. Some detailed rules are contained in Sections 5 and 6 of INT-978.as follows:

- 1) The gate drive returns from the three low side devices should be run to the V_{S0} pin with separate and independent tracks to avoid crosstalk between the different legs of the inverter
- 2) Common mode currents arising from wiring layouts that allow load currents to flow in signal return circuits must be avoided.
- 3) Load current loop size must be small to minimize circuit inductance.
- 4) High current buses must be adequately decoupled at the switching point to minimize inductive spiking.
- 5) Adequate shielding between high voltage, high dv/dt points and low level signal circuits must be provided.
- 6) Transformer designs must minimize voltage gradients between adjacent windings and to the core to prevent capacitively coupled currents from flowing in sensitive signal circuits.
- 7) Power switch dv/dt values should be kept as low as possible consistent with overall system efficiency so that induced bus voltage spikes are minimized.

Contrary to generally accepted theory that faster switching is better, there are several conflicting requirements in the interface between the driver and the driven power device:

- 1) If the distance between driver and power stage is more than a couple of inches, the drive signal should be run in a twisted pair routed directly to the gate and source (or emitter) of the power device.
- 2) Drivers such as the IR2130 have low impedance outputs and consequently cause very fast switching of power MOSFETs. Severe ringing occurs at the switching transistors resulting in unwanted RFI generation and possible dv/dt failure of the power MOSFETs. A quarter-watt non-inductive series gate resistor of about 10 to 33 Ohms usually provides sufficient roll-off with C_{ISS} to damp out the ringing. With small HEXFETs (die sizes 1 to 3) the resistor value should be increased from about 30 to 50 Ohms.
- 3) In motor drive circuits where the load inductance is high, the motor current is commutated by diodes across the power switches when the switches are "OFF." As the opposite switch in a particular bridge leg is turned "ON" it must pull the conducting commutation diode out of conduction through its reverse recovery condition. A spike of current occurs at this time which causes ringing and RFI generation. The magnitude of the current spike can be reduced by the use of the series gate resistor described in (2) above.

5. SPECIFIC APPLICATIONS

5.1 Six-Step 3-Phase Motor Drive

Figure 4 shows a typical 3-phase non-regulated motor drive in which the IR2130 supplies all the gate drive signals for the high-side and low-side IGBTs. The IR2130 is operated from a 15-volt dc supply from a 3-terminal regulator and the inputs are derived from a six-step ring counter with its input signal supplied by a 555 astable multi-vibrator operating at 360 Hertz. The dc bus for the six-step inverter is supplied off-line by rectifying the 115-volt ac input and filtering it with a 50 microfarad 250-volt capacitor.

Motor current is sensed by a series viewing resistor in the negative bus with a 20-Ohm pot across the resistor so that a voltage proportional to load current is delivered to the ITRIP pin 9 of the IR2130. Also, a dc voltage proportional to motor current is available at pin 10. This uses a 9K Ω feedback resistor and a 1K Ω input resistor on pin 11, the inverting input to the current amplifier.

5.2 A 3-Phase Variable Reluctance Drive Using IR2131

Figure 6 shows a variable reluctance motor drive using IGBT's and the IR2131 MOS Gate Driver. High side and low side outputs are simultaneously provided to drive each set of motor phase coils.

The inputs can be simple logic levels spaced 120 electrical degrees apart or can be pulse width modulated to control motor torque.

The values of the bootstrap capacitors are selected to prevent undervoltage lockout at the minimum frequency of operation.

Typically when the minimum frequency is around 30Hz, 10mF electrolytic capacitors are used. They must be selected for low ESR/ESL particularly when large power switches are used as the peak demand currents can be fairly high.

Figure 8. Six-step motor drive waveforms

When starting with the bootstrap capacitors discharged, the first input commands are used to charge them and subsequent commands provide rotational power for the motor. To avoid this problem, the bootstrap capacitors can be pre-charged by connecting high value resistors across the 3 low side power switches. With the bootstrap pre-charged, all input logic signals provide rotational inputs to the motor.

Figure 9. Three-phase variable reluctance motor drive

5.3 General Considerations Using MOS Gate Drivers

Although the IR213X family of drivers can considerably simplify 3-phase motor drives there are some pitfalls to be avoided.

- 1) The V_{S1} , V_{S2} and V_{S3} pins have a maximum specified rating of only -5Vdc. In high current drives it is quite common for inductive spike voltages to exceed -5V because of stray inductances, diode forward recovery problems etc. We recommend techniques as described in AN-978 Sec. 6 to address this problem.
- 2) High current motor drives can also generate ground bus currents which are sometimes severe enough to disrupt logic circuits and cause mis-commutation of the power switches. This usually results in catastrophic failure of the entire drive. To combat this we recommend the use of high speed optical couplers as shown in Figure 7. Using this technique, the power return and logic grounds are completely isolated from one another (see Figure 7).

Appendix 1 Component Selection

When selecting components to use with the internal current amplifier the following design guidelines should be followed.

- 1) The maximum value of resistor that can be inserted in the gate return path is 47 Ohms. Larger values than this may affect the switching performance of the device.
- 2) The maximum output current of the amplifier is 2mA under worst case conditions.

Consider the circuit configuration shown in Figure 2. The gain of the non-inverting amplifier stage is:

$$V_{cao} / V_{s0} = 1 + R1/R2 \quad (1)$$

The signal at the V_{s0} pin may be defined by the equation:

$$V_{s0} = V_{sense} + (V_{ref} - V_{sense}) * R4 / (R3 + R4) \quad (2)$$

Combining equations (1) and (2) gives:

$$V_{cao} = V_{sense} (1 + R1/R2) + [(V_{ref} - V_{sense}) * R4 / (R3 + R4)] * (1 + R1/R2)$$

If the conditions $R1 = R3$ and $R2 = R4$ are true, then the last equation collapses to:

$$V_{out} = V_{ref} + V_{sense} * R1/R2$$

Using the design guidelines sets the range of resistor values that may be chosen. The 2mA current limit sets a minimum for the resistance sum $R1 + R2$. -This limit is defined by:

$$I_{limit} = V_{cao(max)} / (R1 + R2); I_{limit} = 2mA, V_{cao(max)} = 5V.$$

This means that $R1 + R2 > 2.5 \text{ kOhm}$. $R2$ is limited to 47 Ohms and $R1 > 2.45 \text{ kOhm}$. This gives a gain in the circuit of $R1/R2 = 52$. If the output of the amplifier is in the range $[0; +5V]$, then the offset could be 2.5V, giving an allowable output voltage variation of $\pm 2.5V$. The maximum variation of the input voltage is thus $\pm 50mV$.

Figure 10. Recommended opto-isolated input circuit to the IR2130

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This small signal level is possible with commercially available shunts that are low inductance to reduce noise from power device switching. It does mean however that the internal current trip function of the IR2130 cannot be used, as it has an internal 0.5V trip point. Care should be taken when using small input signal levels as the data sheet specification for the amplifier offset voltage is 10mV. An offset adjustment may need to be included in the circuit.

FIGURE CAPTIONS FOR INT-985

Figure No.	Title
1	Functional block diagram of the IR2130/2132 drivers
2	Input to output timing diagram for IR2130/2132 only
3	Current feedback amplifier connection
4	Current Amplifier Operation with Triangular Waveform Input
5	Differential Amplifier with Voltage Offset
6	Measurement of Positive Current Components in the DC Link
7	Three-phase six-step motor drive and 6 x HFA04TB60 HEXFRED diodes
8	Six-step motor drive waveforms
9	Three-phase variable reluctance motor drive
10	Recommended opto-isolated input circuit to the IR2130

HIP4082**Data Sheet****January 3, 2006****FN3676.4**

80V, 1.25A Peak Current H-Bridge FET Driver

The HIP4082 is a medium frequency, medium voltage H-Bridge N-Channel MOSFET driver IC, available in 16 lead plastic SOIC (N) and DIP packages.

Specifically targeted for PWM motor control and UPS applications, bridge based designs are made simple and flexible with the HIP4082 H-bridge driver. With operation up to 80V, the device is best suited to applications of moderate power levels.

Similar to the HIP4081, it has a flexible input protocol for driving every possible switch combination except those which would cause a shoot-through condition. The HIP4082's reduced drive current allows smaller packaging and it has a much wider range of programmable dead times (0.1 to 4.5 μ s) making it ideal for switching frequencies up to 200kHz. The HIP4082 does not contain an internal charge pump, but does incorporate non-latching level-shift translation control of the upper drive circuits.

This set of features and specifications is optimized for applications where size and cost are important. For applications needing higher drive capability the HIP4080A and HIP4081A are recommended.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP4082IB*	HIP4082IB	-55 to +125	16 Ld SOIC (N)	M16.15
HIP4082IBZ* (Note)	4082IBZ	-55 to +125	16 Ld SOIC (N) (Pb-free)	M16.15
HIP4082IP	HIP4082IP	-55 to +125	16 Ld PDIP	E16.3
HIP4082IPZ (Note)	HIP4082IPZ	-55 to +125	16 Ld PDIP** (Pb-free)	E16.3

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Features

- Independently Drives 4 N-Channel FET in Half Bridge or Full Bridge Configurations
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load in Free Air at 50°C with Rise and Fall Times of Typically 15ns
- User-Programmable Dead Time (0.1 to 4.5 μ s)
- DIS (Disable) Overrides Input Control and Refreshes Bootstrap Capacitor when Pulled Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Shoot-Through Protection
- Undervoltage Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- UPS Systems
- DC Motor Controls
- Full Bridge Power Supplies
- Switching Power Amplifiers
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- Medium/Large Voice Coil Motors
- Related Literature
 - TB363, Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)

Pinout

HIP4082

Application Block Diagram

Functional Block Diagram

APPENDIX D: DATASHEET OF HIP4082

HIP4082

Absolute Maximum Ratings

Supply Voltage, V_{DD} -0.3V to 16V
 Logic I/O Voltages -0.3V to V_{DD} +0.3V
 Voltage on AHS, BHS -6V (Transient) to 80V (25°C to 150°C)
 Voltage on AHS, BHS -6V (Transient) to 70V (-55°C to 150°C)
 Voltage on AHB, BHB $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ + V_{DD}
 Voltage on ALO, BLO V_{SS} -0.3V to V_{DD} +0.3V
 Voltage on AHO, BHO $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V Input
 Current, DEL -5mA to 0mA
 Phase Slew Rate 20V/ns
 NOTE: All voltages are relative V_{SS} unless otherwise specified.

Operating Conditions

Supply Voltage, V_{DD} +8.5V to +15V
 Voltage on V_{SS} -1.0V to +1.0V
 Voltage on AHB, BHB $V_{AHS, BHS}$ +7.5V to $V_{AHS, BHS}$ + V_{DD}
 Input Current, DEL -4mA to -100 μ A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Thermal Resistance θ_{JA} (°C/W)
 SOIC Package 115
 DIP Package 90
 Maximum Power Dissipation See Curve
 Storage Temperature Range -65°C to +150°C
 Operating Max. Junction Temperature +150°C
 Lead Temperature (Soldering 10s) +300°C
 (For SOIC - Lead Tips Only))

Electrical Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$

PARAMETER	SYMBOL	TEST CONDITIONS	T _J = +25°C			T _J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS & UNDER VOLTAGE PROTECTION								
V _{DD} Quiescent Current	I _{DD}	All inputs = 0V, R _{DEL} = 100K	1.2	2.3	3.5	0.85	4	mA
		All inputs = 0V, R _{DEL} = 10K	2.2	4.0	5.5	1.9	6.0	mA
V _{DD} Operating Current	I _{DDO}	f = 50kHz, no load	1.5	2.6	4.0	1.1	4.2	mA
		50kHz, no load, R _{DEL} = 10kΩ	2.5	4.0	6.4	2.1	6.6	mA
AHB, BHB Off Quiescent Current	I _{AHBL} , I _{BHBL}	AHI = BHI = 0V	0.5	1.0	1.5	0.4	1.6	mA
AHB, BHB On Quiescent Current	I _{AHBH} , I _{BHBH}	AHI = BHI = V _{DD}	65	145	240	40	250	μA
AHB, BHB Operating Current	I _{AHBO} , I _{BHBO}	f = 50kHz, CL = 1000pF	.65	1.1	1.8	.45	2.0	mA
AHS, BHS Leakage Current	I _{HLK}	V _{AHS} = V _{BHS} = 80V V _{AHB} = V _{BHB} = 96 V _{DD} = Not Connected	-	-	1.0	-	-	μA
V _{DD} Rising Undervoltage Threshold	V _{DDUV+}		6.8	7.6	8.25	6.5	8.5	V
V _{DD} Falling Undervoltage Threshold	V _{DDUV-}		6.5	7.1	7.8	6.25	8.1	V
Undervoltage Hysteresis	UVHYS		0.17	0.4	0.75	0.15	0.90	V
AHB, BHB Undervoltage Threshold	VHBUV	Referenced to AHS & BHS	5	6.0	7	4.5	7.5	V
INPUT PINS: ALI, BLI, AHI, BHI, & DIS								
Low Level Input Voltage	V _{IL}	Full Operating Conditions	-	-	1.0	-	0.8	V
High Level Input Voltage	V _{IH}	Full Operating Conditions	2.5	-	-	2.7		V
Input Voltage Hysteresis			-	35	-	-	-	mV
Low Level Input Current	I _{IL}	V _{IN} = 0V, Full Operating Conditions	-145	-100	-60	-150	-50	μA
High Level Input Current	I _{IH}	V _{IN} = 5V, Full Operating Conditions	-1	-	+1	-10	+10	μA
TURN-ON DELAY PIN DEL								
Dead Time	T _{DEAD}	R _{DEL} = 100K	2.5	4.5	8.0	2.0	8.5	μs
		R _{DEL} = 10K	0.27	0.5	0.75	0.2	0.85	μs

HIP4082**Electrical Specifications** $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	T _J = +25°C			T _J = -55°C TO +150°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, & BHO								
Low Level Output Voltage	V _{OL}	I _{OUT} = 50mA	0.65		1.1	0.5	1.2	V
High Level Output Voltage	V _{DD} -V _{OH}	I _{OUT} = -50mA	0.7		1.2	0.5	1.3	V
Peak Pullup Current	I _O ⁺	V _{OUT} = 0V	1.1	1.4	2.5	0.85	2.75	A
Peak Pulldown Current	I _O ⁻	V _{OUT} = 12V	1.0	1.3	2.3	0.75	2.5	A

Switching Specifications $V_{DD} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{AHS} = V_{BHS} = 0V$, $R_{DEL} = 100K$, $C_L = 1000pF$.

PARAMETER	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ C$			$T_J = -55^\circ C$ TO $+150^\circ C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-off Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPHL}		-	25	50	-	70	ns
Upper Turn-off Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPHL}		-	55	80	-	100	ns
Lower Turn-on Propagation Delay (ALI-ALO, BLI-BLO)	T_{LPLH}		-	40	85	-	100	ns
Upper Turn-on Propagation Delay (AHI-AHO, BHI-BHO)	T_{HPLH}		-	75	110	-	150	ns
Rise Time	T_R		-	9	20	-	25	ns
Fall Time	T_F		-	9	20	-	25	ns
Minimum Input Pulse Width	$T_{PWIN-ON/OFF}$		50	-	-	50	-	ns
Output Pulse Response to 50 ns Input Pulse	T_{PWOUT}			63			80	ns
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}		-	50	80	-	90	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$		-	75	100	-	125	ns
Disable Turn-on Propagation Delay (DIS - ALO & BLO)	T_{DLPLH}		-	40	70	-	100	ns
Disable Turn-on Propagation Delay (DIS- AHO & BHO)	T_{DHPLH}	$R_{DEL} = 10K$	-	1.2	2	-	3	μs
Refresh Pulse Width (ALO & BLO)	T_{REF-PW}		375	580	900	350	950	ns

TRUTH TABLE

INPUT					OUTPUT	
ALI, BLI	AHI, BHI	VDDUV	VHBUV	DIS	ALO, BLO	AHO, BHO
X	X	X	X	1	0	0
X	X	1	X	X	0	0
0	X	0	1	0	0	0
1	X	0	X	0	1	0
0	1	0	0	0	0	1
0	0	0	0	0	0	0

NOTE: X signifies that input can be either a "1" or "0".

HIP4082**Pin Descriptions**

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
2	BHI	B High-side Input. Logic level input that controls BHO driver (Pin 16). BLI (Pin 3) high level input overrides BHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides BHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	BLI	B Low-side Input. Logic level input that controls BLO driver (Pin 14). If BHI (Pin 2) is driven high or not connected externally then BLI controls both BLO and BHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides BLI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	ALI	A Low-side Input. Logic level input that controls ALO driver (Pin 13). If AHI (Pin 7) is driven high or not connected externally then ALI controls both ALO and AHO drivers, with dead time set by delay currents at DEL (Pin 5). DIS (Pin 8) high level input overrides ALI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
5	DEL	Turn-on DELay. Connect resistor from this pin to V_{SS} to set timing current that defines the dead time between drivers. All drivers turn-off with no adjustable delay, so the DEL resistor guarantees no shoot-through by delaying the turn-on of all drivers. The voltage across the DEL resistor is approximately $V_{DD} - 2V$.
6	V_{SS}	Chip negative supply, generally will be ground.
7	AHI	A High-side Input. Logic level input that controls AHO driver (Pin 10). ALI (Pin 4) high level input overrides AHI high level input to prevent half-bridge shoot-through, see Truth Table. DIS (Pin 8) high level input overrides AHI high level input. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
8	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
9	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin.
10	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
11	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
12	V_{DD}	Positive supply to control logic and lower gate drivers. De-couple this pin to V_{SS} (Pin 6).
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
15	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
16	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

HIP4082**Timing Diagrams**

X = A OR B, A AND B HALVES OF BRIDGE CONTROLLER ARE INDEPENDENT

FIGURE 1. INDEPENDENT MODE

FIGURE 2. BISTATE MODE

FIGURE 3. DISABLE FUNCTION

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Performance Curves

FIGURE 4. I_{DD} SUPPLY CURRENT vs TEMPERATURE AND V_{DD} SUPPLY VOLTAGE

FIGURE 5. V_{DD} SUPPLY CURRENT vs TEMPERATURE AND SWITCHING FREQUENCY (1000pF LOAD)

FIGURE 6. FLOATING (IXHB) BIAS CURRENT vs FREQUENCY AND LOAD

FIGURE 7. GATE SOURCE/SINK PEAK CURRENT vs BIAS SUPPLY VOLTAGE AT 25°C

FIGURE 8. GATE CURRENT vs TEMPERATURE, NORMALIZED TO 25°C

FIGURE 9. $V_{DD}-V_{OH}$ vs BIAS VOLTAGE TEMPERATURE

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Performance Curves (Continued)

FIGURE 10. V_{OL} vs BIAS VOLTAGE AND TEMPERATURE

FIGURE 11. UNDERVOLTAGE TRIP VOLTAGES vs TEMPERATURE

FIGURE 12. UPPER LOWER TURN-ON/TURN-OFF PROPAGATION DELAY vs TEMPERATURE

FIGURE 13. UPPER/LOWER DIS(ABLE) TO TURN-ON/OFF vs TEMPERATURE (°C)

FIGURE 14. FULL BRIDGE LEVEL-SHIFT CURRENT vs FREQUENCY (kHz)

FIGURE 15. MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE

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Performance Curves (Continued)

FIGURE 16. DEAD-TIME vs DEL RESISTANCE AND BIAS SUPPLY (V_{DD}) VOLTAGE

FIGURE 17. MAXIMUM OPERATING PEAK AHS/BHS VOLTAGE vs TEMPERATURE

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Dual-In-Line Plastic Packages (PDIP)

- NOTES:
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
 4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
 6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
 7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
 8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
 9. N is the maximum number of terminal positions.
 10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		6
eB	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Small Outline Plastic Packages (SOIC)

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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