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**High Temperature Low Noise SOI-CMOS
Preamplifier for Wireless Telemetry System**

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“The progressive development of man is vitally dependent on invention.”

---- *Nikola Tesla*

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ABSTRACT

High temperature electronics find many applications such as down-hole drilling, aerospace, automotive and nuclear. Elevated temperatures are required for these applications to operate reliably. Electronics for drilling application explore oil wells by sensing, logging and processing data like temperature, inclination, heading and pressure of the strata. Data acquisition system's biggest challenge for down-hole-drilling application is the very high operating temperature, which may be up to 200 °C under more than 2 km of the earth's surface.

At high temperature, bulk-CMOS transistors exhibit many drawbacks: increase in junction leakage, shift of threshold voltages, and reduction of mobility. Among these drawbacks, the most serious problem is the excess junction leakage current at high temperature. Circuit performance is reduced due to the loss of charges at dynamic node or the loss of bias current or more seriously, the latch-up. A proper technology choice is a first consideration for successful operation of integrated circuits in such high temperature regime. By getting rid of the reverse-biased diodes between substrate/well and the source/drain region, Silicon-on-insulator (SOI) technology significantly reduces the leakage current while keeping most of the desirable properties of bulk CMOS technology.

Wireless telemetry system for Measurement While Drilling operations, which is also known as Logging While Drilling, is an effective way to improve drilling operations' efficiency. The front end amplifier is the most critical component of the receiver in a wireless telemetry system. The noise performance of the front-end amplifier determines the detection accuracy of the overall system. Front-end amplifiers used in down-hole-drilling wireless telemetry system at low

frequencies is a main challenge due to the flicker noise of the MOS transistors. Power efficient high temperature capable preamplifiers with low input noise are required. In this thesis, two high temperature low-noise 1- μm partially depleted (PD) SOI CMOS preamplifiers for wireless telemetry system are presented. These designs are targeted for operation at up to 200 $^{\circ}\text{C}$. To achieve low flicker noise, PMOS devices, operating in moderate inversion, are used for the differential input of the preamplifier. MOS devices in the deep triode region are used for resistive source degeneration to reduce flicker noise and the effective transconductance of NMOS devices. Simulation shows that the input-referred noise of the preamplifier is 83 nV/sqrt(Hz) at 800 Hz. The chopper technique is chosen mainly for its very low noise performance at low frequency. For the three opamp chopper amplifier, simulation shows that the output-referred noise is 25.6 nV/sqrt(Hz) at 800 Hz.

The purpose of these designs is to investigate low noise performance of the front end amplifiers under high-temperature condition. Both the circuits are fabricated using XFAB SOI 1- μm process. Experiments prove that the preamplifier can work properly at the temperature 180 $^{\circ}\text{C}$ with a gain of 17.65 dB at 20 kHz and the chopper amplifier can work properly at 225 $^{\circ}\text{C}$ with a gain of 19.65 dB at 20 kHz.

CHAPTER 1 INTRODUCTION

In this chapter, background of measurement while drilling (MWD) for down-hole drilling applications is introduced. Different technologies of MWD are compared. Working environment and communication frequency band for wireless telemetry system are discussed. The motivation and challenge, followed by the objective of this project are specified. The organization of this thesis are presented in the end of this section.

1.1 Background

MWD is an effective way to improve the drilling operation efficiency of down-hole drilling applications. It collects and transforms data in real-time on the drilling process such as oil exploring, which occurs thousands of feet under the surface of the earth. Unfortunately, telemetry of such data is extremely difficult due to the hostile down-hole environments. Circuit designs that can increase the data rate without increasing the complexity of the drilling process will have significant impact on the drilling operation efficiency, for example, if sufficient feedback data are transmitted from underground, better decision can be made for the drilling process.

Due to the low carrier frequencies, traditional wireless MWD telemetry system such as mud pulse telemetry (MPT) system and Electromagnetic telemetry (EMT) system are rate limited systems. MPT system is a popular system presently employed in the industry, providing <10 bits-per-second (bps) data rate. The

carrier frequency of MPT system is typically below 100 Hz, while EMT operates at lower than 30 Hz [1].

Higher data rates are required to enable the drilling operation to be more efficient. However, wireless communication at high frequencies is difficult to implement due to the high attenuation from the earth formation. Low frequency EM waves have been used, but are limited in data rate. A better wireless method to communicate down-hole data up to the surface has been searching in the industry for the over 50 years. One promising way is based on the acoustical carrier waves generated within the drill itself. It is identified as a potential method for high speed communication to transmit information by acoustic stress waves propagating through the pipe-string. This method could accommodate data rates up to 100 bps. Acoustic wireless telemetry using drill pipe as the transmission medium has achieved more than 40 bps in controlled field experiments. As shown in Figure 1-1, the telemetry system can be installed inside the drill collar.

Figure 1-1 (a) typical acoustic wireless telemetry system using for oil exploration application (b) drill collar.

Laboratory experiments and field tests have examined the basic principles of acoustic wave propagating in the drill. Previous results indicate that the frequency bands which are shown in Figure 1-2 are virtually free of attenuation and suitable for high bit rates data transmission. The acoustic channel is the drill, which is a periodic structure of pipes and threaded tool joints. Extensive studies on the acoustic characteristics of the drill had been carried out and published since 1948. Barnes and Kirkwood in 1972 [2] followed by Drumheller [3] in 1989 laid the foundation for analysing acoustic wave propagation in drill. Lee [4] and Ramarao [5] provided a further understanding of acoustic attenuation processes in drill-pipes by their analysis of wave propagation in fluid loaded drill. The frequency response of acoustic wave propagating through the drill string is shown in Figure 1-2. It exhibits a banded and dispersive structure. The acoustic noise level from the drill bit and at the surface is very high at low frequencies (band #1). It is not practical to generate such high acoustic signal levels (at the transmitter) to communicate over these bands over the drill-string (pipes). Hence band #1 is not used for acoustic communication.

Figure 1-2 the acoustic wave pass-band in typical drill pipe [1].

Typical oil wells can reach more than 2 km under the earth's surface. To achieve communication over this distance, a high power acoustic wave has to be launched from the tool down-hole. Piezoelectric material is used as transducers for launching high powered acoustic signal. The receiver has to be able to separate the desired acoustic signal from noise signal coming from the drilling and surface operations. The conditions of the down-hole are harsh. The electronic systems are required to withstand vibration, high pressures, shock in confined space, and at high temperature (HiT) which can be higher than 170 °C. Instruments that can operate at such high temperature will hence be required. The long-term stability of these instruments forms one of their key parameters of the wireless telemetry system because maintenance and recalibration are impossible or extremely expensive.

1.2 Motivation and Challenges

As stated in the background section, higher uplink telemetry rates during MWD operations, which is also known as Logging while drilling (LWD), is of great significant. Real-time measurement of the well-bore pressure, temperature and geo-steering enable better control of the bore-hole trajectories to achieve optimization of the drilling fluid program, hence enhancing the well-bore stability. By getting rid of wire or cable in the borehole annulus, transmission of information wirelessly would be safer and environment related risks will be reduced. These advantages of acoustic transmission for MWD motivate researchers world-wide to develop the acoustic telemetry system. Application Specific ICs (ASICs) for the

acoustic telemetry system are a major and important topic for the research of the acoustic telemetry system.

The key challenges in developing the wireless acoustic telemetry system for the drilling process are to ensure communication robustness in the presence of drilling noise and electronics that can operate at high temperature ($>170\text{ }^{\circ}\text{C}$) encountered at great depth typically over 2 km under the surface of the earth. The key challenges to overcome in achieving high data rate are: (a) comb-like frequency response of the acoustic channels that extends only up to a couple of kHz in actual drill strings; (b) acoustic noise from drilling and surface operations. These combined with the fact that the system electronics have to operate on battery power and at $> 170\text{ }^{\circ}\text{C}$ pose a lot of problems both at the communication system level design and at circuit level design. Also, as temperature increases, materials such as polymers and solders can melt or break down; causing the circuits may work on unstable condition.

Electrical noise is the main source of noise affecting the performance of integrated circuits (ICs) used in the extreme environment of deep space operating at low frequencies. These noises mainly include flicker noise, thermal noise and shot noises. Flicker and thermal noises are the dominant noise while the shot noise can usually be ignored since it is significantly smaller. The flicker noise is inversely related to the operation frequency, hence, it highly dominant at low frequencies. The thermal noise, on the other hand, is directly proportional to the temperature and has no relation with the frequency of operation. Thus, it is extremely difficult to design low noise amplifiers that can operate in high temperature for low frequency application.

Also, low-power operation of the wireless telemetry system is required because of the stringent power requirements in deep space missions. This requires designs which can minimize both the white noise and flicker noise at given level power budget while maintaining radiation and temperature hardness.

Although high temperature electronics development is a system problem, development of ICs may be the most challenging aspect of the problem. At high temperature, bulk-CMOS transistors exhibit several drawbacks such as junction leakage incensement, threshold voltages shift, and mobility reduction. Among these drawbacks, excess junction leakage current at high temperature poses the most serious problem. It reduces performance of the circuit due to loss of bias current or charges store at the dynamic nodes, or more seriously, may even destroy the IC due to latch-up.

1.3 Objectives

The system level architecture of the wireless telemetry system, which is proposed by Institute of Microelectronics (IME), is shown in Figure 1-3. The preamplifier is designed for the receiver of the wireless telemetry system. This project is funded by the Agency for Science, Technology and Research (A*STAR), Singapore, through SERC grant number: 102 165 0087.

Figure 1-3 wireless telemetry transceiver.

For the transmitter, it includes the digital signal processor which will receive data from several kinds of sensors such as temperature, pressure, heading and inclination. The processor also generates multiple carriers. Multi-carrier modulation is selected to make effective use of the frequency spectrum in the acoustic telemetry system. This is completed by creating multiple carriers within the narrow pass bands of the channel. Compared with using analogue approach, the creation of carriers through the Direct Digital Synthesis (DDS) provides more robustness as well as more control over the carrier generation [21]. The high voltage driver IC is used to drive a set of piezoelectric disks, which are modelled as a capacitive load of about 0.3 μF and across a broadband from 400 Hz to 2 kHz [7].

For the receiver, the acoustic signal received by the piezoelectric transducer is the input of the low noise preamplifier, followed by the filter and the amplifying

component. An ADC is employed to convert the analog signal to digital signal. After the ADC, the signal will be processed by a Field Programmable Gate Array (FPGA). All the devices in the receiver need to work under high temperature environment. The performance of the preamplifier is of great importance among all the components since the signal being amplified is in the order of few millivolts, the noise added by the amplifier must be minimized to avoid overwhelming the signal to be amplified.

The objective of this project is to develop high temperature low noise preamplifiers for the receiver of the acoustic telemetry system, to transfer data collected from various sensors at the bottom of the drill-string to the surface. The primary goals of this project include the followings:

- a) To develop a high temperature low noise cascode preamplifier for the analogue front-end circuits of the wireless telemetry system. The preamplifier is required to work under high temperature environment, up to 200 °C and exhibit low noise specification within the expected 400 Hz to 2 kHz bandwidth.
- b) To design a chopper stabilized low noise amplifier for the receiver of the wireless telemetry system. The chopper amplifier must be able to work under high temperature environment up to 200 °C. The chopping technique is selected for its very low flicker noise performance.
- c) Two versions of the front end amplifier designs are implemented to explore circuit design techniques that are able to compensate for the high-temperature effects on the MOSFETs, to allow Silicon-On-Insulator (SOI) CMOS IC to operate at temperature up to 225 °C with low flicker noise performance.

1.4 Organization of the Thesis

The rest of this thesis is organized as follows.

Chapter 2 provides a literature review of the prior works on high temperature amplifier design. The general design considerations for high temperature preamplifiers are included and the related designs are studied. The existing low noise amplifiers (LNA) are evaluated and the related design techniques are compared.

In Chapter 3, analog front end preamplifier design for the receiver of the wireless telemetry system is discussed. The detailed circuit description of the preamplifier is presented. Spectre simulations are completed. The test configuration of the chip, as well as the measurement results of the preamplifier are provided also in the chapter.

A chopper stabilized amplifier for the receiver of the wireless telemetry system is then discussed in Chapter 4. Circuit description of the chopper amplifier is presented. Simulations of transient analysis, frequency response, high temperature performance and noise are given. The test configuration of the chip, measurement results of the chopper amplifier are shown in the end of the chapter.

Lastly, Chapter 5 summarizes the research achievement and draws the conclusions. Future works for the design of the high temperature low noise preamplifier are given and discussed in the chapter.

CHAPTER 2 LITERATURE REVIEW ON LOW NOISE

HiT PREAMPLIFIER

A review of the prior works on high temperature low noise amplifier design is presented. The general design considerations for high temperature preamplifiers are included and the related designs are studied. The existing low noise amplifier (LNA) is evaluated and the related design techniques are compared.

2.1 Potential Input Signal from Piezoelectric Transducer

A piezoelectric transducer can be modelled as a voltage generator, in the express of $E_h = S_h * P$, with its equivalent capacitor C_h in series, the operating frequency ranges from 400 Hz to about 2 kHz. S_h presents for the transducer sensitivity with the unit of volt/Pascal and P presents for the acoustic pressure in pascals [5]. Typically, the value of C_h is from 100 pF to 10 nF. The input-impedance of the amplifier must be nearly infinite due to the very large output impedance of the sensor, hence bipolar transistors are prohibited in the input stage.

Figure 2-1 (a) configuration of voltage amplifier, (b) Configuration of charge amplifier.

Two amplifier configurations may be used for a piezoelectric transducer: (1) the voltage amplifier as shown in Figure 2-1(a); (2) the charge amplifier as shown in Figure 2-1(b). Except for its input-referred noise voltage E_n and the input-equivalent capacitance C_{in} , Amplifier A is assumed to be ideal. The expressions followed present the characteristics of the two settings in terms of the voltage gain V_o/E_h and the total input-referred noise power En_i^2 [7]:

Voltage amplifier:

$$\frac{V_o}{E_h} \approx (1 + \frac{R_2}{R_1}) (\frac{C_h}{C_h + C_{in} + C_c}) , \omega > \frac{1}{R_g(C_c + C_h + C_{in})} \quad (2.1)$$

$$E_{n_i}^2 = (E_n^2 + 4kT \frac{R_1 R_2}{R_1 + R_2}) (\frac{C_h + C_{in} + C_c}{C_h})^2 + \frac{4kT}{R_g s^2 C_h^2} \quad (2.2)$$

Charge amplifier:

$$\frac{V_o}{E_h} \approx \frac{-sR_f C_h}{1 + sR_f C_f} \approx \frac{-C_h}{C_f} , \omega > \frac{1}{R_f C_f} \quad (2.3)$$

$$E_{n_i}^2 = E_n^2 (\frac{C_h + C_{in} + C_c + C_f}{C_h})^2 + \frac{4kT}{R_f s^2 C_h^2} \quad (2.4)$$

Since the coaxial line in the application of wireless telemetry system is very short, the C_c will be little. As presented in the Equations (2.1) and (2.3), it is clear that the charge amplifier configuration offers better performance in terms of gain, because there is no dependence upon the coaxial line capacitance C_c . Expressions (2.2) and (2.4) indicate that for the input-referred noise voltage En_i , both configurations are quite equivalent, at least for gains greater than 10, i.e., $C_f \ll C_h$, where C_f is the off-chip capacitor of the amplifier as shown in Figure 2-1(b). In both cases of charge amplifier configuration and voltage amplifier configuration, the value of R_f , which is the external off-chip resistor as shown in Figure 2-1(b),

or R_g , which is the resistor as shown in Figure 2-1(a), has to be made extremely large (may be several tens of mega Ohms) to minimize its influence. Besides, if the values of the resistors R_1 and R_2 are small, the output driving capability of the amplifier will be large. For the charge amplifier configuration, if a large capacitor C_h is used for low gain, the upper limit of the bandwidth will be large.

Figure 2-2 differential inputs with two buffers.

The noise performances of these two configurations are quite the same; however, the charge amplifier configuration is better since it is able to process differential sensor signal. The differential input differential output (DIDO) amplifier is showed in Figure 2-2.

For the receiver of the telemetry system, the performance of the preamplifier is of great importance among all the components since the signal to be amplified usually is on the order of few mv, the noise generated by the amplifier must be minimized to avoid mix with the signal being amplified.

The potential signals for the receiver of the telemetry system are produced by the piezoelectric transducers which will convert acoustic waves to electrical signals.

The magnitude of the signal is few millivolts and the frequency ranges from 400 Hz to 2 kHz as shown in Figure 2-3.

Figure 2-3 signal output from piezoelectric transducers [6].

2.2 High Temperature Behaviour of MOSFET Integrated Circuits

For high temperature MOSFET ICs, the intrinsic carrier density, carrier concentration, carrier mobility[13], threshold voltage and leakage current will be different from those operate in normal temperature, usually less than 120 °C.

2.2.1 Threshold Voltage

According to [11], the threshold voltage V_T of a long-channel MOSFET without substrate bias can be expressed as

$$V_T = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \pm 2\phi_F \pm \gamma_{n,p} \sqrt{2\phi_F}, \quad (2.5)$$

Where positive is for NMOSFET and negative is for PMOSFET. Here, Q_{ss} is the surface-state charge density, C_{ox} is the gate capacitance, $\gamma_{n,p}$ is body-effect constant, ϕ_F is the Fermi potential of the bulk which is $\phi_F = \frac{kT}{q} \ln(\frac{N_B}{n_i})$ where N_B

is the bulk doping level, and ϕ_{ms} is the contact potential difference between gate and substrate. The gate doping is usually n-type. For a conventional n-well process, $\phi_{ms} = -\frac{kT}{q} \ln(\frac{N_B N_g}{n_i^2})$ for NMOS and $\phi_{ms} = -\frac{kT}{q} \ln(\frac{N_g}{N_B})$ for PMOS, where N_g is the gate doping level.

The threshold-voltage's temperature-dependence of NMOS is given by [15]

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} + \frac{2\phi_F}{T} + \frac{\gamma_n}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} \quad (2.6)$$

For a PMOS device, the temperature dependence of its threshold voltage becomes

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} - \frac{2\phi_F}{T} - \frac{\gamma_p}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T} + \frac{1}{T} \left(\frac{E_g}{q} + \frac{3kT}{q} \right) \quad (2.7)$$

To be compared with (2.6), it decrease -0.5 mV/°C in magnitude of the first term of equation (2.7) [16], the second term' sign becomes negative, so as the third term. Besides, one more term with value of 4.3 mV/°C is added. Hence, when temperature continues to go up, the threshold voltage of NMOS will be negative and PMOS becomes more positive; furthermore, the threshold voltage of PMOS is changing faster compared with that in NMOS. Measurement result shows the threshold voltage will change for a half from 25 °C to 250 °C for both PMOS and NMOS [17].

2.2.2 Leakage Current

There are two basic types of leakage current in a MOSFET: subthreshold channel current and junction leakage current. In the subthreshold region, the gate-to-source voltage V_{GS} is below the threshold, but the channel of the transistor is “weakly” inverted. The drain current is mainly due to carrier diffusion through the channel, and it has a strong temperature dependence because of changes in mobility, threshold voltage, and the parameter n_0 , which acts as idealistic factor. Subthreshold current may be written as [18]

$$I_D(T) \approx \mu(T) \left(\frac{W}{L} \right) \frac{C_{ox}^2}{C_{ox} + C_d} \left[\frac{n_0(T) kT}{q} \right]^2 e^{\left[\frac{q[V_{GS} - V_{th}(T)]}{n_0(T) kT} \right]} \quad (2.8)$$

The easiest way to reduce leakage current is to lower the power supply voltage [14], but this also reduces circuit speed, noise margins and dynamic range.

A approach to reduce the effect of leakage current has been suggested in [17] that for a given node, the leakages into the node from VDD must be matched by leakages out of the node to VSS. Figure 2-4 shows a diagram of an NMOS transistor whose source and drain have been connected to complementary diodes in order to cancel leakage current into these nodes, as proposed by Harvey [36]. The requirement of cancellation is that the complementary diodes have matched leakage current over temperature.

Figure 2-4 parasitic diodes at drain and source junctions of a NMOS transistor.

2.3 High Temperature Capable Amplifier Design

In addition to technology consideration for high temperature electronics application, analog circuit design technique is to be considered. There are many other techniques available to mitigate the above temperature induced drawbacks. Generally such methods depend on the specific structure circuit of interest. Examples are zero temperature coefficients (ZTC) gate biasing, substrate biasing feedback, leakage current feedback cancellation, and constant- g_m biasing. Among them constant- g_m biasing is the most relevant technique to op-amp design. Constant- g_m biasing makes “temperature-stable” transconductance g_m of op-amp and thus stable closed-loop gain of op-amp is obtained.

This section reports a high temperature amplifier design using constant- g_m bias circuit for electronic data acquisition system application [19]. The amplifier is designed to be two-stage where the first stage is a folded cascode. A constant- g_m

bias circuit is adopted to ensure no degradation of the closed loop gain and high cut-off frequency of the op-amp in high temperature application.

Figure 2-5 shows the core design of the amplifier. The amplifier consists of a two-stage miller amplifier of which the first stage is a folded-cascode differential input to obtain a high dc-gain. PMOS transistors are used for the differential input stage since PMOS transistor has better threshold voltage mismatch property, lower flicker noise, and a quite comparable current driving capability compared to its counterpart NMOSFET, the second stage is designed to be a PMOS input inverting amplifier with NMOS cascode current source and thus the op-amp has less output resistance. For high temperature measurement environment, long cable from DUT (device under test) in hot chamber may induce large capacitance thus the second stage is designed to drive high capacitance.

Figure 2-5 folded cascode two stage op-amp.

Figure 2-6 shows the constant- g_m bias circuit in the design. A simple analysis of the bias circuit is presented as below.

Figure 2-6 schematic of constant- g_m bias circuit.

Transconductance g_m of NMOS in saturation region, assuming neglecting channel length modulation and the body effect, is given by

$$g_m = \sqrt{2\mu_n c_{ox} \left(\frac{W}{L}\right) I_D} \quad (2.9)$$

When bias current I_D is inversely proportional to the mobility, transconductance g_m is ideally independent of the mobility degradation and thus temperature-independent.

The bias circuit is based on

$$V_{GS,M1} = V_{GS,M2} + I_B \cdot R_B \quad (2.10)$$

In (2.10) V_{GS} is gate-source and I_B is the current through R_B . With keeping $I_B = I_{REF}$, neglecting body effect and assuming $V_{th,M1} = V_{th,M2}$, we have

$$I_B = \left(\frac{2}{\mu_n C_{ox} (W/L)_{M1} R_B^2} \right) \left(I - \frac{I}{\sqrt{K}} \right)^2 \quad (2.11)$$

In the design, K is set to 4; hence I_B can be expressed as follow:

$$I_B = \left(\frac{I}{2\mu_n C_{ox} (W/L)_{M1} R_B^2} \right) \quad (2.12)$$

Leading to

$$g_m = \left(\frac{I}{R_B} \right) \quad (2.13)$$

From (2.13) it is known transconductance g_m will be stable over temperature when R_B has a zero-temperature coefficient.

2.4 Noise of an Amplifier

Noise specifications of an amplifier will be presented in this part, including noise types in an amplifier, noise amplitude and noise spectra.

2.4.1 Noise Types

In amplifier circuits, 5 noise sources are commonly observed, they are thermal noise, shot noise, flicker noise, burst noise, avalanche noise.

For amplifiers, avalanche and burst noises are normally be eliminated if they exist. Hence, when doing the noise analysis of the circuit, burst and avalanche noise are not included.

- **Shot Noise**

Whenever charges go through a potential barrier, such as a PN junction, shot noise will be present. It is totally a random event to cross a potential barrier. Hence, the instantaneous current includes many independent, random current pulses with a mean value, I_D . Shot noise is basically described by the mean-square variance of its average value. It is depicted as $\overline{i_n^2}$:

$$\overline{i_n^2} = \overline{(i - i_D)^2} = \int 2i_D q df \quad (2.14)$$

In (2.14) df is differential frequency and q is on behalf of the electron charge, which is 1.62×10^{-19} C. Shot noise shows an uniform-power-density, which means that its spectra is flat. Shot noise has no direct connection with temperature. The term $i_D q$, the units A^2/Hz , is the power density of the current.

- **Thermal Noise**

The thermal excitement of charge carriers in a conductor causes the thermal noise. It exists in almost all passive resistive devices. Just as shot noise, thermal noise has a uniform-power -density, however thermal noise has nothing to do with current flow.

Voltage or current sources are two different ways to represent for thermal noise. A noiseless resistor in series with the voltage is used for voltage model to present the thermal noise. If the thermal noise is modelled as a current source, then a noiseless resistor will be placed in parallel with the current. The average voltage mean square value or the average current mean square of noise source is predicted in (2.15):

$$\overline{e^2} = \int 4kRTdf \text{ or } \overline{i^2} = \int (4kT / R)df \quad (2.15)$$

Where k represents for Boltzmann's constant which is 1.38×10^{-23} J/K, R is the conductor's resistance in ohms (Ω), T is the absolute temperature in the unit of Kelvin (K), and df is differential frequency. The terms $4kTR$ and $4kT/R$ are current and voltage power densities in units of A^2/Hz , V^2/Hz , respectively.

- **Flicker Noise**

Flicker noise, which is also known as $1/f$ noise, exists in almost all active components and has different sources. Flicker noise is always presented with a dc current, and its average mean-square-value is as in the equation (2.16):

$$\overline{e^2} = \int (K_e^2 / f)df \text{ or } \overline{i^2} = \int (K_i^2 / f)df \quad (2.16)$$

Where df stands for differential frequency, K_i and K_e are the appropriate device constants in amps and volts, respectively, f is the operating frequency.

Carbon composition resistor also presents flicker noise, which is also called excess noise. Other kinds of resistors also present flicker noise in different degrees. If the current of the resistor is low enough, thermal noise will dominate as it is proportional to the current in the resistor, thus the type of resistor used will not influence the noise in the circuit.

The terms K_e^2 / f and K_i^2 / f are voltage and current power densities which having units of V^2/Hz and A^2/Hz , respectively. Although both the bipolar and MOSFET transistors experience flicker noise, it is a significant noise source only in MOS transistors and can be ignored in bipolar transistors since it is very small usually.

- **Burst Noise**

Burst noise, which is also called popcorn noise, consists of sudden step-like transitions between two or more discrete voltage or current levels, as high as several hundred microvolts, at random and unpredictable times. It is related to imperfections in semiconductor material and heavy ion implants. Burst noise will make a popping sound at rates below 100 Hz if connected to a speaker. To achieve low burst noise, clean device processing is required.

- **Avalanche Noise**

Avalanche noise presents in the case that a PN junction works in the reverse breakdown mode. Within the depletion region of a PN junction, a strong reverse electric field is presented; electrons in the PN junction have enough kinetic energy to form additional electron-hole pairs when they bump with the crystal lattice's atoms. These random collisions generate random current pulses, which is similar but much intense compared with the shot noise.

2.4.2 Noise Amplitude

Noise sources can only be represented by a probability density function since their amplitudes vary randomly with time. Shot noise and thermal noise have Gaussian probability density functions. However, the amplitudes of other noises do not consist of Gaussian probability density functions. By definition, δ represents the Gaussian distribution's standard deviation, δ^2 represents the average mean-square variation about the average value. The instantaneous value lies between

$\pm\delta$ 68% of the time and the average value of the signal. This means that in noise signals with the amplitude of Gaussian distributions, the average-mean-square variation, $\overline{i^2}$ or $\overline{e^2}$, is the variance δ^2 , and the standard deviation is δ the root-mean-square (RMS) value of the noise signals. Figure 2-8 presents the relationship between the probability of the amplitude and its RMS value. Values between 4 (95.4%) and 6.8 (99.94%) are used to ensure that a signal is within peak-to-peak limits 99.7% of the time.

Figure 2-7 gaussian distribution of noise amplitude.

2.4.3 Noise Spectra

There is only one frequency for the power of a pure sine wave. However, for noise power, it is spread over the frequency spectrum. In noise calculations, voltage noise power density, $\overline{e^2} / \text{Hz}$, and current noise power density, $\overline{i^2} / \text{Hz}$ are often used.

The power density is integrated over the operation frequency to calculate the mean-square value.

Flicker noise and thermal noise are the main noise source affecting the performance of preamplifiers of the acoustic telemetry system. Flicker noise dominant at low frequencies while thermal noise is directly proportional to the absolute temperature and not related to the frequency of operation as shown in Equations (2.17) and (2.18), respectively [9].

$$v_f^2(f) = \frac{k_f}{2\mu_n(c_{ox})^2 W L f} \quad (2.17)$$

$$v_t^2(f) = \frac{4\gamma k T}{\sqrt{2\mu_n c_{ox} (W / L) I_D}} \quad (2.18)$$

Where W and L are the channel width and length of the MOSFET respectively, T represents for temperature in Kelvins, v_f represents for flicker noise, c_{ox} is the gate capacitance per unit area, v_t represents for thermal noise, k is the Boltzmann's constant, μ_n is of carrier mobility, k_f is the flicker noise coefficient, γ is the MOSFET thermal noise coefficient, I_D is the bias current of the MOSFET, f is the frequency at which the circuit is operating.

Figure 2-9 below shows the spectra of flicker noise and white noise per root hertz.

Figure 2-8 $1/f$ and white noise spectra.

When plotted with frequency on the log-log scales, white noise (thermal noise) is a horizontal line of constant value; flicker noise is a line with constant slope. If the power density V^2 / Hz is plotted, the slope is -1 decade per decade. If the square roots of the power density, $V_{\text{RMS}} / \sqrt{\text{Hz}}$, is plotted, the slope is -0.5 decade per decade.

2.5 Low Noise Preamplifier Design

The low noise front-end amplifier is one of the most important modules in the receiver of the acoustic telemetry system, as it comes at the most front-end of the system and most of the system parameters depend on the performance of the front-end amplifier. First of all, the noise performance of the front-end amplifier determines the detection accuracy of the overall system. Minimizing the input

referred noise of the front-end amplifier is very critical, which usually requires high quiescent current. On the other hand, the tight power budget may limit the current allocated to the front-end amplifier. As a result, achieving optimum noise to power trade-off for the front-end amplifier becomes more and more important. In this section, common noise reduction techniques are reviewed in order to highlight their noise reduction efficiencies.

2.5.1 PMOS Input Noise Reduction Technique

An extremely low noise CMOS front end amplifier for capacitive sensor is proposed by Bruno [7]. The structure is shown in figure 2-10. It is a differential input balanced-output preamplifier. The low input-referred noise aims at about 3.5 nV/sqrt (Hz) at 700 Hz. A PMOS differential pair (M1, M2) for high input impedance constitutes the input stage since P-channel transistors show lowest 1/f noise for a certain gate area. To improve matching and reduce the input-referred thermal noise, M1 and M2 are intentionally worked near the sub-threshold region, thus ensuring a high common-mode rejection, as well as making the total offset voltage of the whole stage lower. To lower the corner frequency of the flicker noise, large area is required, which also result in an input capacitance of about 100 pF. It is of good practice to introduce some voltage gain in the first stage of an amplifier to lower the offset voltage and input-referred noise. However, this limits the use of active loads as their output impedance is very high. Small resistors RD_1 and RD_2 were used to introduce a low gain (typically 10 dB), but without sacrificing noise performance. Thus, this method can make a very low noise front end amplifier for a given power level.

Figure 2-9 feedback noise reduction circuit [7].

The gain stage, which is composed of Q1, Q2 and M3-M10, is a fully differential folded cascode stage. It is designed to reach both wide bandwidth and high open-loop gain. Bipolar transistors are used in the differential pair (Q1, Q2) since they almost present no $1/f$ noise and show the largest achievable transconductance at a given bias current. But for SOI process, there are no bipolar transistors available. In this design, the intensive use of bipolar transistors leads to good dc and ac characteristics and very low-noise performance for a given moderate power consumption.

2.5.2 Chopper Stabilized Amplifier

Another approach employs chopper stabilized amplifier to reduce the input-referred noise. The offset and noise of the input amplifiers limit the overall

performance of the system in many applications, such as sensor interfaces. The shift from bipolar to CMOS processes, which have significantly higher $1/f$ noise and offset, has enhanced the problem previously. The dynamic offset cancellation techniques give solutions for low offset and flicker noise. Among these techniques, autozero and chopper techniques are good examples. The basic principle of the autozero technique is to first measure the offset and then subtracts it in a next phase. The basic principle of the chopping technique is to modulate the offset and the flicker noise to higher frequencies, with the input signal modulate and demodulated during the amplifying process. Further analysis will be explained in this thesis.

This section describes the principle of chopper amplifier. Chopping technique has been considered for low frequency signals such as acoustic wave signal, of which the frequency is less than 2 kHz, to reduce $1/f$ noise.

Figure 2-10 chopping principle [22].

The principle of chopping technique is depicted in Figure 2-11. Here, the input signal $V_{in}(t)$ is multiplied with a periodic rectangular signal $m(t)$ with unity amplitude and 50% duty-cycle. Offset V_{OS} and $1/f$ noise V_N are modulated at odd harmonics leaving the baseband free of $1/f$ noise. After amplification, V_A is demodulated by $m(t)$, and then we derive $V_o(t)$. As shown in Figure 2-11 $m(t)$ is modulation signal as well as demodulation signal. $T = 1/f_{chop}, f_{chop}$ is the chopping frequency.

The Fourier transform of a rectangular signal $m(t)$ with unity amplitude and 50% duty cycle is given by

$$m(t) = 2 \sum_{k=1}^{\infty} \frac{\sin\left[\frac{k\pi}{2}\right]}{\left[\frac{k\pi}{2}\right]} \cos(2\pi f_{chop} kt) = \sum_{k=1}^{\infty} M_k \cos(2\pi f_{chop} kt)$$

$$(M_k = \frac{4}{k\pi} \sin(\frac{k\pi}{2})) \quad (2.20)$$

$V_{in} * m(t)$ is the input signal after modulated. From the spectrum of $V_{in} * m(t)$, we can see that the input signal V_{in} is modulated at odd harmonics of the modulation signal $m(t)$. This signal is demodulated by $m(t)$ after amplified, then we get the low noise signal $V_o(t)$.

$$V_o(t) = AV_{in}(t) \sum_{k=1}^{\infty} M_k \cos(2\pi f_{chop} kt) \cdot \sum_{l=1}^{\infty} M_l \cos(2\pi f_{chop} lt) \quad (2.21)$$

In the above formula, k and l are both odd number. The Fourier transform of the low noise output signal after demodulated $V_o(t)$ is shown in Figure 2-12.

Figure 2-11 fourier transform of $V_o(t)$.

In order to get the amplified $V_{in}(t)$, the low noise output $V_o(t)$ must be filtered by a low pass filter (LPF), of which the cut-off frequency is higher than that for the modulated input signal ($> f_{chop}/2$). The signal after the LPF is the amplified low noise output signal $V_{out}(t)$.

The principle of chopping technique can also be analysed in the time-domain as shown in Figure 2-11. In the time domain, the input signal V_{in} is periodically inverted with the function of the first multiplier or chopper. After amplified by the amplifier, the inverted signal is re-inverted, resulting again in a dc signal. However, the flicker noise and the offset is periodically inverted only once and therefore appears as a square wave at the output.

In literature, many basic analysis of these types of flicker noise and offset cancellation techniques can be found, such as the correlated-double-sampling [23],[24], ping-pong opamp [25], [26], self-calibrating opamp [27], synchronous detection, the two or three signal approach[28] and dynamic element matching(DEM).

The lower noise specification of the chopper technique is the main reason to use this technique for the front end amplifier of the receiver for the wireless telemetry system.

2.5.3 Technology Selection

For proper operation of the ICs in the high temperature regime of interest in this work, from 0 °C to 200 °C, a proper technology choice is first considered. Recent development on ICs using wide band-gap semiconductors such as GaAs, Gap, GaN, SiC, and Diamond , have been noted that they are better suited for high temperatures than silicon [10]. The major drawback of all these approaches is that the materials and processes are still in their infancy and are much more expensive than Si.

For high temperature application, the silicon-on-insulator (SOI) process is a promising candidate. The leakage current of the SOI devices is much lower than CMOS transistors. This is because the thin bulk region of the SOI devices is isolated with insulator. Besides, the threshold voltage changes less with temperature in SOI transistors than their bulk-CMOS counterparts. In addition, the latch-up immunity of SOI devices is better, which helps to improve the reliability of circuit operation at higher temperature. Most of the commercial SOI processes are specified over 200 °C. For XFab 1.0- μm SOI process, it is specified up to 225 °C which fully meet the requirement of our project.

The following models listed in Table 2-1 are supported by XFab for the specified revision of the circuit simulator:

Table 2-1 Simulation Models

Simulator	MOS Transistor Model	
	BSIM3SOI	Monte Carlo & Matching
Spectre	b3soidp	-
HSPICE	Level 57 (BSIM3PD2.0.1)	-

The simulation parameters are intended for use with the analog circuit simulators SPECTRE and HSPICE or any other simulation program which contains SPICE compatible models.

Figure 2-12 characteristic curves for NMOS transistors.

Figure 2-13 shows the characteristic curves for NMOS transistors which have been measured on typical wafers. The characteristic curves are intended for checking the correct implementation of the SPICE model and SPICE parameters in a particular simulator. Output characteristics of several NMOS transistor geometries

for zero bulk voltage and several gate voltages are shown. The figures contain the measured and the simulated drain current for the BSIM3PD2.0 model.

Figure 2-14 shows the characteristic curves for NMOS transistors which have been measured on typical wafers.

Figure 2-13 characteristic curve for PMOS transistors.

In this thesis, all circuit simulations are performed on SPECTRE simulator with the SIM3SOI MOS transistor models.

CHAPTER 3 DESIGN OF HiT LOW NOISE PREAMPLIFIER

Preamplifier is the most critical component of the receiver in a wireless telemetry system. The original signal before amplified can have magnitude in the order of a few millivolt. After the front end amplification, the signals will be at least ten times higher in magnitude. The original signal will be interfered after amplification if there is any noise injected in the front end amplification,. However, any noise injected in the remaining signal processing circuitry will have much less significance. Hence, low noise front end amplifier is very critical for system performance. This chapter will focus on the preamplifier design for the receiver of the wireless telemetry system, including the discussion of the preamplifier design specifications, the simulation of the preamplifier as well as the measurement after the designed circuit was fabricated.

3.1 Design Requirements

The preamplifier must have a very low intrinsic noise level as it adds thermal noise and flicker noise to the signal being amplified. The chip should be able to work at high temperature, possibly up to 200 °C due to the high temperature occurred at 2 km to 3 km meters underground. The detail specifications of the preamplifier for wireless telemetry system are summarized in Table 3-1.

Table 3-1 Design Specification of the Preamplifier.

Preamplifier						
Parameters	Conditions	Value			Unit	Remarks
		Min	Typ.	Max		
Supply Voltage	-	4.5	5	5	V	-
Working Temperature	-	0	25	225	°C	Process limitation
Gain(dB)	@25 °C	18	20	22	dB	-
Bandwidth	@25 °C	200	2k	200k	Hz	-
Noise	@800Hz		100		nV/sqrt(Hz)	Input-referred
Total Current consumption	@25 °C	40	40	40	μA	-

The specifications are designed according to the target signal, the power consumption, input referred noise requirement, silicon area consumption, etc. If a large gain of more than 100 is required, two-stage amplification is necessary, as it is not practical to implement using single amplifier due to the large silicon area consumption.

3.2 Front End Amplifier with Noise Reduction Techniques

In this section, a PMOS input capacitive feedback preamplifier is presented, as well as the simulations of the preamplifier in Spectre.

3.2.1 PMOS Transistors as Input Devices

The leakage current of a MOS transistor is relatively small at room temperature, normally on the order of pA. The increase of the junction leakage current is caused due to two effects as temperature rises [11]. Firstly, due to thermally generated electron-hole pairs in the depletion region, a drift current will be formed, and generated carriers will be swept across the junction by the electric field. This effect is proportional to the intrinsic carrier concentration. It normally dominates to temperatures up to 100-150 °C. Secondly, at higher temperature, the junction leakage is dominated by diffusion of thermally generated minority carriers away from the junction area, which is proportional to the square of the intrinsic carrier concentration. These carriers are swept across the junction by the electric field when they reach the edge of the depletion region. The concentration of minority carriers is inversely proportional to the doping concentration but a strong function of the temperature. Consequently, PMOS transistors have much less leakage current than NMOS in an N-well process [37].

The junction leakage current of SOI-CMOS is remarkably smaller than bulk-CMOS due to the absence of diffusion leakage towards the substrate and reduced junction area. Since the dominant leakage current is the generation term in the depleted region in SOI transistors, this volume decreases with the reduction of device length [8]. Therefore it is worthwhile examining the leakage current of the SOI-CMOS transistors for design of op-amp and the bias circuit required in the preamplifier.

Figure 3-1 junction leakage current in NMOS transistor.

Figure 3-1 and 3-2 show the simulation results of gate-length dependent junction leakage current in NMOS and PMOS transistors from 0 °C to 200 °C.

Figure 3-2 junction leakage current in PMOS transistor.

All the simulations in this thesis are based on the Cadence Spectre simulation tool. The junction leakage current increases in both transistors with temperature increasing. No further increasing of junction leakage current in PMOS transistor beyond 150 °C is observed. It is also found that junction leakage current in NMOS transistor decreases with the reduction for all temperature. Otherwise the junction leakage current of PMOS transistor show little gate-length dependence.

Excess leakage current increases self-heating of the circuit, shifts operating points in an analogue circuit, lower output resistance of high-impedance nodes, erases charge stored in the memory node and can be the source of latchup-triggering current. It can also greatly increase offset among matching devices. Therefore, minimization excess leaking current is among the most serious challenges in silicon high temperature electronics.

Channel length modulation parameter is also different between NMOS and PMOS transistors. The output conductance is one of the parameters determine the amplifier's open-loop gain. The output conductance of a MOS transistor is expressed using channel length modulation parameter λ and drain-source current I_{DS} as

$$g_{ds} = \lambda I_{DS} \quad (3.1)$$

It is well known that the channel length modulation parameter is inversely proportional to gate length of MOS transistors [9].

Figure 3-3 channel length modulation parameter of PMOS transistor.

Figure 3-3 exhibits the temperature dependence of channel length modulation parameter (λ) for PMOS transistor with various gate lengths. Channel length modulation parameter decreases in both NMOS and PMOS transistors as temperature increases. PMOS transistor shows higher channel length modulation parameter for all temperatures when compared to NMOS transistor. Interestingly it is found that PMOS transistor with 4 to 6 μm gate length shows around 1.5 times more channel length modulation parameter for all temperatures. More than 2 time channel length modulation parameter is obtained in PMOS transistor with shorter gate lengths.

As described in the above, PMOS transistor has better threshold voltage mismatch property, lower flicker noise and a quite comparable current driving capability

compared to its counterpart NMOS in 1.0 μm SOI Technology. So PMOS input stage is selected in the preamplifier design.

3.2.2 Circuit Implementations of Preamplifier

In this part, a low-noise 1.0- μm partially depleted (PD) SOI CMOS preamplifier for extremely high temperature environment in the down-hole-drilling application is proposed. The first stage is a PMOS differential input stage while the second stage is a folded cascode gain stage, the third stage is a source follower output. The schematic of the PMOS differential input capacitive feedback preamplifier is shown in Figure 3-4. V_{in+} and V_{in-} are the differential input, I_{bias1} and I_{bias2} is the input biasing current, 1 μA and 10 μA respectively. V_{B3} is input voltage for biasing, which can be tuned when doing testing for the preamplifier.

Figure 3-4 open loop schematic of the differential voltage input preamplifier.

Large area PMOS transistors, M1 and M2, are used as the differential input pair due to its very low flicker noise in low frequency, and they are operated in moderate inversion region for low input-referred white noise voltage. M3 and M4 are resistively degenerated current sources utilizing M7 and M8 operating in the triode region as degeneration resistors. Current source degeneration is applied to remarkably lower NMOS $1/f$ noise contributed by M3 and M4. The differential input pair devices M1 and M2 are connected to folded cascode devices M10 and M11 and PMOS devices M14 and M15 provide an active current mirror load for M10 and M11. The high NMOS flicker noise of folded cascode devices M10 and M11 is heavily degenerated through the high output resistance of current source M3 and M4. Power efficiency for the differential input preamplifier can be improved by lowering the current in the folded cascade stage (M10 and M11) below that of the input differential pair (M1 and M2). The dominant gain and dominant pole are contributed by node 3, where the current signal is converted to high voltage gain. Capacitor C_c provides dominant pole negative feedback compensation. An output stage based on source follower M16 provides a proper DC output level and improves the driving capability of the amplifier.

The Spectre transient response simulation result of the preamplifier is as shown in Figure 3-5. From the simulation result, it can be observed that the peak-to-peak value of the input signal, green wave in the figure, is 0.1 mV, the peak-to-peak value of the output signal, red wave in the figure, is 1 V. The output signal will become stable after 5 ms.

Figure 3-5 simulated transient response of the preamplifier.

As described in 2.1, charge amplifier configuration is used for piezoelectric transducers. Figure 3-6 shows the capacitive feedback op-amp, which is a prototype for the analogue frontend in an acoustic telemetry receiver part for the down-hole drilling application.

Figure 3-6 capacitive feedback close loop of the op-amp.

The close loop gain is given by

$$A_c = \frac{C_1}{C_2} \quad (3.2)$$

3.3 Simulation of the Preamplifier

The circuit shown in Figure 3-4 is simulated by Cadence Spectre, including the AC simulation for frequency response, the DC simulation for checking the transistors' operating points, the noise simulation and the post-layout simulation.

3.3.1 Simulation of Frequency Response

The AC simulation in the Spectre is to check the frequency response of the circuit, including the gain, and bandwidth of the circuit. When conducting AC simulation, we need to set the circuit in its right DC operating point. In this work, the input is a 1-V AC signal for ease of measurement of the circuit gain. The AC simulation setup is shown in Figure 3-7. Preamp2 is the close loop of preamp1. The resistor is off-chip since $500\text{ M}\Omega$ will require a large circuit area. The supply voltage V_{DD} is of 5 V. VB3, I1, and I5 are the biasing inputs of the circuit, VB3 is 5 V, I1 is $1\text{ }\mu\text{A}$, and I5 is $10\text{ }\mu\text{A}$. The positive input is the 1-V AC signal with a 2.5-V DC offset and 700 Hz frequency. The negative input has a 2.5-V DC offset.

Figure 3-7 AC simulation setup.

The PMOS differential input capacitive feedback preamplifier is designed to have a gain of 20 dB in the frequency range from 200Hz to 186 kHz operating in temperature from 0 °C to 200 °C. The close loop AC response of the preamplifier is shown as in Figure 3-8. The simulation results match the design target.

Figure 3-8 AC response of the preamplifier.

3.3.2 Simulation for High Temperature Requirement

The circuit need to meet the requirement to work under high temperature which may up to 225 °C. For the temperature simulation, firstly, we can check the output signal DC variance using the Spectre DC simulation. If the circuits are not able to work under such high temperature regime, the DC of output signal won't be as what we expected. The simulation library of XFab SOI process supports the temperature up to 225 °C, which meet the design requirement. The DC simulation result is shown in Figure 3-9.

Figure 3-9 output signal DC simulation as temperature range from 0 °C to 225 °C.

The purpose of the DC simulation for the output signal of the preamplifier is to check the temperature effects on the circuit. The temperature will change from 0 °C to 225 °C in the simulation. From the simulation result, we can see that the output voltage has a little change of about 0.25 mV when temperature increases from 0 °C to 100 °C. After 100 °C, the output signal suffers a relatively rapid drop, at approximately 1 mV drop from 0 °C to 225 °C. Nevertheless, this small change is acceptable in the wireless telemetry system.

The DC simulation is a general check for the high temperature capability. To further verify the stability of high temperature performance, we also need to check the gain of the amplifier under different temperature. This is done in Spectre with AC simulation setting different temperature. A simulation result of different gains

under different temperature is shown in Figure 3-10, a 50 °C step is chosen in the plot.

Figure 3-10 gain under different temperature.

In the simulation result, we can see that, the gain is changing little from 0 °C to 225 °C in the frequency less than 2 kHz, which is the main bandwidth we use in this application. A more detail statistics is shown in the Table 3-2.

Table 3-2 Gain under Different Temperature at 800 Hz

Gain & Temperature (800 Hz)			
Temperature (°C)	Gain	Temperature (°C)	Gain
0	9.57	150	9.74
50	9.63	200	9.78
100	9.68	225	9.79

We can see that, from 0 °C to 225 °C, which is the extreme condition, the gain only change 2 %, which is acceptable for this application.

3.3.3 Noise Simulation

In this simulation, the focus is on the flicker noise since it contributes most noise in low frequency. Two simulation models are widely used for flicker noise modelling. One of the flicker noise model is the SPICE model; the other flicker noise model is BSIM3 model. Parameters of the flicker noise in both models are listed in the Table 3-3.

Table 3-3 Flicker Noise Model Parameters.

Symbols used in equation	Symbols used in SPICE	Description	Default	Unit
Noia	noia	Noise parameter A	(NMOS) 1e20 (PMOS) 9.9e18	none
Noib	noib	Noise parameter B	(NMOS) 5e4 (PMOS) 2.4e3	none
Noic	noic	Noise parameter C	(NMOS) -1.4e-12 (PMOS) 1.4e-12	none
Em	em	Saturation field	4.1e7	V/m
Af	af	Flick noise exponent	1	none
Ef	ef	Flicker noise frequency exponent	1	none
Kf	kf	Flicker noise coefficient	0	none

In the XFab SOI Process Library, the BSIM3 model is deployed, and the flicker noise parameters are showed in Figure 3-11.

$Af = 1.000e+20$, $kf = 0.000e+00$, $ef = 1.000e+00$, $noia = 1.000e+20$, $noib = 5.000e+04$, $noic = -1.40e-12$.

```

pbth4.scs x
+ mo1n=1.500e+01
+ rdsw=1.200e+03      wr=1.000e+00
+ cdsc=2.400e-04      cdsch=0.000e+00      cdsd=0.000e+00
+ prwb=-2.995e-01     prwg=8.067e-02      cit=0.000e+00
+ tsi=2.500e-07       tbox=1.000e-06      tox=2.500e-08
+ nlx=7.000e-09       xj=2.500e-07
+ nch=6.000e+16       nsub=-7.000e+14      ngate=9.570e+19
+ alpha0=4.000e-09    fbjtii=0.000e+00
+ beta0=0.000e+00     beta1=4.210e-02      beta2=1.442e-01
+ vdsatii0=2.000e+00  tii=0.000e+00      lii=0.000e+00
+ esatii=1.000e+07    sii0=9.605e-01      sii1=1.000e-01
+ sii2=0.000e+00      siid=0.000e+00
+ agidl=0.000e+00     bgidl=0.000e+00      ngidl=1.200e+00
+ ntun=1.000e+01      ndiode=1.230e+00     nrecf0=2.000e+00
+ nrecr0=1.000e+01    isbjt=1.120e-03      isdif=1.380e-04
+ isrec=7.852e-04     istun=0.000e+00      ln=1.000e-05
+ vrec0=0.000e+00     vtun0=0.000e+00      nbjt=1.074e+00
+ lbjt0=1.000e-06     vabjt=2.361e+00      aely=0.000e+00
+ ahli=8.930e-10      rbody=5.000e+01      rbsh=0.000e+00
+ af=1.000e+00        kf=0.000e+00        ef=1.000e+00
+ noia=1.000e+20      noib=5.000e+04      noic=-1.40e-12
+ rsh=6.400e+01
+ lint=-2.782e-08     wint=-8.796e-07
ends pbth4
*

```

Figure 3-11 flicker noise parameters used in XFab SOI Process.

The formulations of the BSIM3 model [29] are detailed as follows:

If $V_{gs} > V_{th} + 0.1$,

$$\begin{aligned}
 \text{Noise density} = & \frac{q^2 k T \mu_{eff} I_{ds}}{C_{ox} L_{eff}^2 f^{ef} \cdot 10^8} \left(Noia \cdot \log \left(\frac{N_0 + 2 \times 10^{14}}{N_l + 2 \times 10^{14}} \right) + Noib \cdot (N_0 - N_l) + \frac{Noic}{2} (N_0^2 - N_l^2) \right) \\
 & + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} \cdot L_{eff}^2 f^{ef} \cdot 10^8} \cdot \frac{Noia + Noib \cdot N_l + Noic \cdot N_l^2}{(N_l + 2 \times 10^{14})^2}
 \end{aligned}$$

Where μ_{eff} represents the effective mobility under the given bias condition, f^{ef} is flicker noise frequency exponent, default value of ef is 1, V_{tm} represents the

thermal voltage and W_{eff} and L_{eff} are the effective channel width and length, respectively. N_0 is the parameter of the charge density at the source side given by

$$N_0 = \frac{C_{ox}(V_{gs} - V_{th})}{q} \quad (3.4)$$

N_1 is the parameter of the charge density at the drain end given by

$$N_1 = \frac{C_{ox}(V_{gs} - V_{th} - \min(V_{ds}, V_{dsat}))}{q} \quad (3.5)$$

ΔL_{clm} is the channel length reduction due to channel length modulation and given by

$$\Delta L_{clm} = \begin{cases} Litl \cdot \log \left(\frac{V_{ds} - V_{dsat} + E_m}{E_{sat}} \right) & (\text{for } V_{ds} > V_{dsat}) \\ 0 & (\text{otherwise}) \end{cases} \quad (3.6)$$

$$E_{sat} = \frac{2 \times v_{sat}}{\mu_{eff}}$$

where

$$Litl = \sqrt{3X_j T_{ox}} \quad (3.7)$$

Otherwise

$$Noise\ density = \frac{S_{limit} \times S_{wi}}{S_{limit} + S_{wi}} \quad (3.8)$$

where, S_{limit} is the flicker noise calculated at $V_{gs} = V_{th} + 0.1$ and S_{wi} is given by

$$S_{wi} = \frac{Noia \cdot V_{tm} \cdot I_{ds}^2}{W_{eff} L_{eff} \cdot f^{ef} \cdot 4 \times 10^{36}} \quad (3.9)$$

To obtain a noise spectrum of the amplifier, the circuit was simulated using Spectre. If an input signal is provided, the Spectre will calculate the noise contribution of all the devices as well as the input-referred noise or output-referred noise, correspondingly. The noise simulation setup is depicted in Figure 3-12. The supply voltage V_{DD} is set to 5 V. VB3, I1, and I5 are the biasing inputs of the circuit, VB3 is 5 V, I1 is set to 1 μ A, and I5 is of 10 μ A. The negative input is the 1-V AC input with a 2.5-V DC offset. The positive input is a 2.5-V DC offset voltage.

Figure 3-12 noise simulation unity gain configuration.

In an amplifier structure as shown in Figure 3-4, the most significant noise contributions are M2, M1, M8, M7, M15, M14, successively. A noise contribution summary of all transistors is listed in Figure 3-13.

Device	Param	Noise Contribution	% Of Total
Preamp2.I16.M2.m1	id	1.15028e-15	16.54
Preamp2.I16.M1.m1	id	9.22235e-16	13.26
Preamp2.I16.M2.m1	fn	5.26006e-16	7.56
Preamp2.I16.M1.m1	fn	4.21274e-16	6.06
Preamp2.I16.M8.m1	id	2.36866e-16	3.41
Preamp2.I16.M7.m1	id	2.31616e-16	3.33
Preamp2.I16.M15.m1	id	2.04338e-16	2.94
Preamp2.I16.M14.m1	id	1.91296e-16	2.75
Preamp2.I16.M15.m1	fn	4.95642e-17	0.71
Preamp2.I16.M14.m1	fn	4.85916e-17	0.70
Preamp2.I16.M4.m1	id	4.23569e-17	0.61
Preamp2.I16.M3.m1	id	4.14349e-17	0.60
Preamp2.I16.MA7.m1	fn	3.85324e-17	0.55
Preamp2.I16.M0.m1	fn	1.03061e-17	0.15
Preamp2.I16.MA7.m1	id	7.0411e-18	0.10
Preamp2.I16.M4.m1	fn	6.19625e-18	0.09
Preamp2.I16.M3.m1	fn	6.06072e-18	0.09
Preamp2.I16.M8.m1	fn	3.61371e-18	0.05
Preamp2.I16.M7.m1	fn	3.53355e-18	0.05
Preamp2.I16.M0.m1	id	1.92192e-18	0.03

Spot Noise Summary (in V ² /Hz) at 800 Hz Sorted By Noise Contributors			
Total Summarized Noise = 6.95607e-15			
Total Input Referred Noise = 6.54855e-15			
The above noise summary info is for noise data			

Figure 3-13 noise contribution summary.

The simulated output-referred noise, as shown in Figure 3-14, is 83.4 nV/sqrt(Hz) at 800 Hz, which is very low noise.

Figure 3-14 output referred noise simulation.

3.3.4 Post-layout Simulation

The layout of the preamplifier is carefully designed using Cadence Virtuoso Layout Editor. To diminish the negative effects generated by the fabrication process, temperature variances and the mechanical constraints as well, the large area PMOS differential input pairs of the preamplifiers are drawn at the center of the layout. Capacitive dummies are used to fill in the empty space which can also enhance low-noise performance. The layout is as shown in Figure 3-15. The chip size is $3325\text{ }\mu\text{m} \times 3150\text{ }\mu\text{m}$.

Figure 3-15 layout of the preamplifier.

After the layout, it is necessary to do a post-layout simulation to ensure the correctness of the layout design. The post layout simulation results of the

preamplifier are summarised in Table 3-4. Simulations for checking process, voltage and temperature (PVT) variation effects on on-chip interconnect, as well as via structures are performed. Typical mean (*TM*) parameters is extracted from typical wafers. *WP* stands for worst case power, which is the fast NMOS and fast PMOS parameters. *WS* stands for worst case speed, namely the slow NMOS and slow PMOS are used.

Table 3-4 Post Layout Simulation Results for Close Loop Preamplifier

Parameters	Description	Spec.	Temp (°C)	Worst(WP)	Typcial	Best(WS)	Unit
				VDD - 10%	VDD	VDD +5%	
Gain	Gain	20	-50	19.67	19.72	19.62	dB
			0	19.67	19.73	19.70	
			25	19.67	19.74	19.73	
			100	19.68	19.74	19.78	
			175	19.68	19.75	19.80	
			225	19.68	19.75	19.82	
PM	Phase Margin with 10 pF Load	>30	-50	84.22	84.06	84.0	Degree
			0	84.22	84.07	84.06	
			25	84.22	84.07	84.08	
			100	84.22	84.07	84.11	
			175	84.22	84.07	84.13	
			225	84.22	84.07	84.14	
UGB	Unity Gain Bandwidth	16	-50	18.78	16.3	13.94	MHz
			0	18.76	16.29	13.92	
			25	18.75	16.28	13.91	
			100	18.72	16.25	13.88	
			175	18.69	16.23	13.85	
			225	18.67	16.21	13.83	

3.4 Preamplifier Measurements

The chip has been fabricated using XFab 1.0 μm SOI process. A measurement PCB is designed according to the Spectre simulation setup as shown in Figure 3-16. This PCB is used for normal temperature measurement, on which the components are as labelled. The preamplifier is the only chip on the PCB. The red connector is for VDD, the black is for GND, The three BNC connector as labelled on the PCB are input signal for the preamplifier. The blue components are resistors, including 500 M Ω external resistor and the potentiometers for the biasing current using. In the measurement, the following 4 steps will be conducted.

Figure 3-16 measurement PCB.

- Step 1, Steady state signal waveform;
- Step 2, Frequency response;
- Step 3, Noise Measurement;
- Step 4, High temperature performance.

Step 1 is to verify the amplifying function of the preamplifier; Step 2 is to measure the frequency response of the preamplifier; Step 3 is conducted to test the output-referred noise; Step 4 aims to test the high temperature performance of the preamplifier.

3.4.1 Steady State Signal Waveform

To verify the amplifying function of the preamplifier, an ultra-low distortion function generator is used to generate a small signal with 50 mV magnitude and 800 Hz frequency to the negative input of the preamplifier, a 2.5 V common mode DC voltage is set to the positive input, a power supply of 5 V is provided. The measurement setup is shown in Figure 3-17.

Figure 3-17 measurement setup.

The amplified signal waveform of the preamplifier is presented by an Agilent DSO5054A Oscilloscope as in Figure 3-18. The preamplifier and the measurement PCB is working properly. But the gain is only 12 dB at 800 Hz. This may be caused by the parasitic capacitor of the PCB since the preamplifier gain is decided by the capacitors.

Figure 3-18 steady state signal waveform of the preamplifier.

When the input signal frequency varied from 300 Hz to 200 kHz, a general frequency response of the preamplifier was obtained statistically. Table 3-5 shows different input signal frequency and the corresponding output magnitude. The magnitude of the input signal is 50 mV.

Table 3-5 Input Frequency and Corresponding Output Magnitude

Input Frequency (Hz)	Output Magnitude (mV)	Input Frequency (Hz)	Output Magnitude (mV)	Input Frequency (Hz)	Output Magnitude (mV)	Input Frequency (Hz)	Output Magnitude (mV)
300	172	10k	225	35k	330	95k	406
600	172	12k	238	45k	350	100k	406
700	172	15k	256	55k	369	105k	400
800	172	18k	275	65k	388	107k	397
900	172	19k	281	75k	400	117k	378
1k	172	20k	284	78k	400	127k	350
2k	172	21k	289	82k	406	137k	320
3k	175	22k	294	88k	406	147k	288
5k	188	25k	300	91k	406	160k	247
7k	200	28k	331	93k	409	200k	163

Using Matlab, we can get the statistical frequency response as shown in Figure 3-19.

Figure 3-19 statistical frequency response.

By this method, we can get a general frequency response. We can also using the equipment to get the frequency response, which will be more accurate.

3.4.2 Frequency Response

To measure the frequency response of the preamplifier, Agilent 35670A Dynamic Signal Analyzer is used. The Dynamic Signal Analyzer is able to process signal from ~ 0 Hz to 51.2 kHz. The installing sketch for frequency response measurement of the preamplifier and the measurement setup are shown in Figure 3-20.

Figure 3-20 (a) installing sketch for frequency response measurement, (b) the measurement setup.

The Dynamic Signal Analyzer will generate a source signal to the input of the preamplifier, to calculate the gain, the source signal is also input to Channel 1. The output signal of the preamplifier is input to Channel 2. The analyzer will do FFT transform and show the gain of the preamplifier as Figure 3-21.

Figure 3-21 frequency response of the preamplifier.

In the low frequency, the gain of the preamplifier is less than simulation result. This may because the effect of PCB's parasitic capacitor.

3.4.3 Noise Measurement

The noise is measured also by the Dynamic Signal Analyzer. The input signals are both set to the common mode voltage 2.5 V. Under this condition, the output signal is supposed to be the noise of the amplifier. The output signal has a DC voltage of 2.5 V. In order to make the noise be displayed without the DC signal, we need to add a DC block component before the output signal is input to the analyzer. The power spectra will be displayed by the Dynamic Signal Analyzer.

Figure 3-22 noise power spectra of the preamplifier.

The measured noise power spectrum is shown in Figure 3-22. The output-referred noise at 720 Hz is about 1.62 μVrms . The noise is larger than the simulated result of the preamplifier. This is because of the noise from PCB itself and from the 500 M Ω resistor.

3.4.4 High Temperature Performance

In order to measure the high temperature performance of the PMOS differential input capacitive feedback preamplifier up to 225 $^{\circ}\text{C}$, a high temperature capable PCB is designed. The HiT PCB, as shown in Figure 3-23(a), contains only the preamplifier. High temperature capable wires will connect the pins of the chip to the normal temperature PCB, which is the the right one in Figure 3-23(a). The high temperature capable PCB will be put in a temperature chamber as shown in Figure 3-23(b). The temperature chamber is ESPEC SU-240, it can provide temperature in the chamber up to 330 $^{\circ}\text{C}$.

(a)

(b)

Figure 3-23 (a) high temperature PCB, (b) measurement setup of high temperature performance.

The gain of the preamplifier is measured under different temperature as shown in Table 3-6. 20 kHz is chose since it is near the cent frequency of the preamplifier.

Table 3-6 Gain of the Preamplifier at 20 kHz under Different Temperature.

Temperature ($^{\circ}\text{C}$)	20	40	60	80	100	120	140	160	180	200	225
Gain (dB)	17.97	17.95	17.96	17.94	17.92	17.90	17.86	17.78	17.65	16.67	16.01

The preamplifier is working properly under 180 $^{\circ}\text{C}$. Beyond 180 $^{\circ}\text{C}$, its gain is changing a lot.

CHAPTER 4 DESIGN OF LOW NOISE CHOPPER AMPLIFIER

Chopper stabilization technique is implemented to further reduce flicker noise. Chopping as a technique for reducing $1/f$ noise has been considered for low frequency signals like acoustic wave signal whose frequency is less than 1 kHz. The ultra-lower noise characteristic of the chopper technique is the main reason for its use this technique at the front end amplifier of the receiver for the wireless telemetry system.

4.1 Chopper Stabilized Technique for Low Noise Amplifier

This section describes how to design a chopper amplifier. Basically, when we design a chopper amplifier, an amplifier without chopper is first designed, and then we add the chopper in the input and the output, the modulator for the input and demodulator for the output, respectively. In basic chopper amplifiers, the input signal is modulated before the differential input pair, amplified by the amplifier and then transposed back at the output nodes as illustrated in Figure 4-1.

Figure 4-1 conventional choppers.

The output signal is differential in this structure. It is not possible to operate in very high frequency for differential signal; thus, this approach is constrained in few kHz. In addition, the noise generated by the transistors of the demodulator is directly coupled to the output signal. Since switches exist in the middle of the supply, for low voltage amplifiers a charge pump is needed to make sure all switches are firmly open and/or closed.

not necessary. The output node, used for Miller compensation, also help to filter out the undesired high frequency spectral components resulting from switching, making the output signal free of offset and flicker noise. Therefore, unlike the common chopper amplifiers, this approach does not need an extra low-pass filter. The only limitation of this structure would be the charge injection residual offset.

Low thermal and flicker noise specification is desired in the front end amplifier for the receiver of the wireless telemetry system. Chopping technique can remarkably minimize the low frequency noise of the amplifier, including the flicker noise and the thermal noise at low frequency part. As mentioned in 2.5.2, the process of the chopping technique removing the low frequency noise of the amplifier could be analysed either in time domain and frequency domain.

A. Time domain analysis

Figure 4-3 noise chopping process.

A simplified low frequency noise chopping process is illustrated in Figure 4-3. V_N is the input-referred noise, including the flicker and thermal noise of the amplifier. The modulated input-referred noise voltage V_{NO} can be expressed in equation (4.1), of which ω_l represents for the chopping frequency of $m(f)$, $m(f)$ is the modulate signal, namely the chopping signal.

$$V_{NO}(t) = \sum_{\substack{k=1 \\ k=odd}}^{\infty} \frac{4}{k\pi} \cdot V_N(t) \cdot \sin(k\omega_l t) \quad (4.1)$$

1) Narrowband noise:

For a narrowband noise, as the case of flicker noise, $V_n(t)$, with standard Gaussian distribution, namely zero mean value, $N_0/2$ power spectral density (PSD) in $(\omega_n - B/2 \sim \omega_n + B/2)$, could be decomposed into two dependent low frequency components $n_c(t)$ and $n_s(t)$ [33], as shown in (4.2) below.

$$V_n(t) = n_c(t) \cos \omega_n t - n_s(t) \sin \omega_n t \quad (4.2)$$

The modulated noise voltage V_{NO} is

$$V_{NO}(t) = \sum_{\substack{k=1 \\ k=odd}}^{\infty} \left[\frac{4}{k\pi} (n_c(t) \cos \omega_n t - n_s(t) \sin \omega_n t) \sin(k\omega_1 t) \right] \quad (4.3)$$

The modulated noise voltage V_{NO} will pass through a LPF. The final output signal after the LPF is

$$V_{Nout}(t) = -\frac{2}{\pi} [n_c(t) \cdot \sin(\omega_1 - \omega_n) t + n_s(t) \cdot \cos(\omega_1 - \omega_n) t] \quad (4.4)$$

When $\omega_n \approx \omega_1$, which is usually the case when the modulated noise output signal passes filtered by a LPF, the first part in (4.4) could be ignored. Therefore, the input-referred noise is reduced after chopping.

$$V_{Nout}(t) \approx -\frac{2}{\pi} n_s(t) \quad (4.5)$$

2) Wideband noise:

When the input-referred noise, $V_n(t)$, is wideband just like the thermal noise, the output noise signal after modulated is

$$V_{NO}(t) = \sum_{\substack{k=1 \\ k=odd}}^{\infty} \frac{4}{k\pi} \times V_n \sin(\omega_n t + \varphi) \times \sin(k\omega_1 t)$$

$$= \frac{2}{\pi} V_n \sum_{\substack{k=1 \\ k=odd}}^{\infty} \frac{1}{k} \{ \cos[(k \omega_1 - \omega_n) t - \varphi] - \cos[(k \omega_1 + \omega_n) t + \varphi] \} \quad (4.6)$$

After passing through a LPF, the second part in (4.6) is removed and the final output noise voltage is

$$V_{Nout} = \frac{2}{\pi} V_n \sum_{\substack{k=1 \\ k=odd}}^{\infty} \frac{1}{k} \cos[(\omega_n - k \omega_1) t + \varphi] \quad (4.7)$$

Therefore, the modulated noise voltage, V_{NO} , is not only presented around $\omega_n = \omega_1$ but also around $\omega_n = (2n-1)\omega_1$, of which n is integer. It exhibits a comb like filter of which the magnitude with frequency response is illustrated in Figure 4-4. If the noise component, of which the frequency is $(2n-1)\omega_1$, modulated by the chopper signals' correspond harmonic components, a DC output signal will show up after passing through the LPF. This DC output will add the output noise voltage and the output signal's harmonic components.

Figure 4-4 output noise harmonics response.

B. Frequency domain analysis

It has been widely discussed in details in [33-34] of the noises characteristics of a chopper amplifier. The input-referred noise PSD of the amplifier are shown in

equation (4.8), in which f_k stands for the corner frequency of the flicker noise and S_{N0} represents for the thermal noise PSD

$$S_{N,in} = S_{N0} \cdot \left(1 + \frac{f_k}{f}\right) \quad (4.8)$$

If the chopper frequency is much smaller than the bandwidth of the amplifier, then the PSD of the final output low frequency noise after passing through LPF is

$$S_{Nout} = \left(\frac{2}{\pi}\right)^2 \cdot S_{N0} \cdot A_0^2 \cdot \left(\sum_{\substack{n=-\infty \\ \text{odd}}}^{\infty} \frac{1}{n^2} + \frac{1}{|n|^3} \frac{f_k}{f_{chop}}\right) \quad (4.9)$$

So the input equivalent noise PSD is

$$S_{Nin} \approx S_{N0} \cdot \left(1 + \frac{17f_k}{2\pi^2 f_{chop}}\right) \quad (4.10)$$

Equation (4.10) indicates that when the amplifier's bandwidth is infinite, the thermal noise keeps constant before and after chopper modulation. Compared to autozero amplifiers, which is also widely used when designing a low noise front end amplifier, the thermal noise of a chopper amplifier isn't aliased. Furthermore, a chopper amplifier could reach a very low noise at low frequency. The flicker noise is minimized when $f_{chop} \gg f_k$. But the frequency of the chopping amplifier, f_{chop} , cannot be too high since high f_{chop} will add substantial residual offset, which will decrease the chopper amplifier's accuracy.

4.2 Circuit Implementation of Chopper Amplifier

In this section, a low-noise 1 μm partially depleted (PD) SOI-CMOS chopper amplifier for the extreme temperature environment of down-hole-drilling

In the schematic of the chopper amplifier, VP, VPN, VBP, VN is from the biasing circuit as shown in Figure 4-6. I20u is an input of the amplifier which provide 20 μ A current.

Figure 4-6 schematic of the bias circuit for the chopper amplifier.

In this design, the low frequency input signal is modulated before the differential pair M1 and M2, amplified by the folded cascode stage and then the output signal is demodulated at the output nodes. CH1 is the modulation block, namely the chopper for the input. The chopper amplifier is a three-stage operational amplifier except for the additional choppers. The first stage, which is formed by M1, M2, R1 and R2, is a low-gain low-noise PMOS input stage since PMOS exhibit lower flicker noise compared with their NMOS counterpart. The gain of the first stage is about ten times in magnitude. The low noise specification is first achieved by utilizing resistors R1 and R2 instead of an active load and secondly by applying high W over L ratio of input PMOS transistors M1 and M2 to make them operating in moderate inversion. The low noise performance of the input stage is critical as it determines the overall noise performance. The second stage is a folded cascode gain stage, comprising of transistors from M3 to M12 and the current sources. It

is designed to have high gain and low transconductance. The high gain is required to meet the high offsets of the subsequent stage. The reason for low transconductance is to make the unity-gain in low frequency, which helps to filter the modulated noise and offset intrinsically. The low transconductance is accomplished through utilising a current source of only $8\text{ }\mu\text{A}$ and a low W/L ratio. To minimize effects of the chopper switches' charge injection, the first two stages of the amplifier are kept fully differential. A common-mode control circuit is applied to define the common-mode voltage on the drains of M3 and M4. This is achieved by measuring the common mode current through M5 to M8, and using this value to control the drain current of M3 and M4. The third stage is formed by M13 and M14 and performs as Miller stage. This stage contributes the dominant poles, the gain is only one. To ensure the amplifier operating stably the Miller stage is necessary. Besides, this stage also performs as a LPF for the modulated noise and offset signals.

Figure 4-7 realization of the Chopper.

The realization of the chopper is shown in Figure 4-7. The chopper engages 8 transistors to achieve the switching functions both as modulator and a demodulator. C is the clock signal with 50% duty cycle and the frequency is 32 kHz (the chopper frequency is usually equal to $0.2 \cdot f_c$, f_c is the cut-off frequency of the amplifier). CB is the same clock signal but with complementary phase.

Figure 4-5 shows the single stage of the chopper amplifier. A three opamp instrumentation structure to further reduce the noise of a chopper amplifier is shown in Figure 4-8.

Figure 4-8 three-opamp instrument amplifier structure.

This structure consists of two stages, a differential input-differential output (DIDO) stage followed by a differential input-single ended output stage (DISO) [35]. The basic idea of this three-opamp instrumentation structure is applying the precise instrumentation methodology with its low noise specification while considering

the proposed chopper amplifier as a regular amplifier with low $1/f$ noise and reduced offset.

4.3 Simulation of the Chopper Amplifier

This section will present the simulation of the chopper amplifier, including the transient analysis, the frequency response, high temperature performance, and the noise simulation.

4.3.1 Transient Analysis of the Chopper Amplifier

The Spectre transient analysis is first completed. The simulation result is shown in Figure 4-9. The input signal, the red curve, is sine wave with a magnitude of 10 mV and 1 kHz frequency. The chopping signal is a rectangle signal with a frequency of 32 kHz and 50% duty cycle.

Figure 4-9 steady response of the chopper amplifier.

The input signal are modulated with the chopper, the signal after modulated is shown in yellow curve in time domain. The modulated signal is amplified by the

amplifier; the signal after amplified is shown by green curve. The amplified signal is demodulated by the output chopper, and the final output signal is shown by the blue curve.

4.3.2 Frequency Response of the Chopper Amplifier

The Spectre AC simulation result with frequency and phase response is shown in Figure 4-9. The chopper amplifier is designed to have a gain of 20 dB. The low cut-off frequency is 80 Hz. The high cut-off frequency is 145 kHz. From the chopping principle, we know that the cut-off frequency of the amplifier should be much larger than the chopping frequency.

Figure 4-10 AC response of the fully configured chopper amplifier.

The unit gain frequency is 1.096 MHz. The low cut-off frequency is 80 Hz. The high cut-off frequency is 145 kHz. Thus, it is a narrow bandwidth amplifier. The

phase of the chopper amplifier is also shown in the Figure 4.10. The phase also meets the design requirement as it only changes 80 degrees at high cut off frequency. Usually amplifiers are designed to achieve a typical phase margin of 60 degrees.

4.3.3 High Temperature Simulation for the Chopper Amplifier

The circuits need to meet the requirement to work under high temperature which may up to 200 °C. DC simulation aims to check the stability of the output DC point under the temperature variance from 0 °C to 225 °C. The DC simulation result is shown in Figure 4-11.

Figure 4-11 DC simulation of chopper amplifier.

The temperature will change from 0 °C to 225 °C in the simulation. From the simulation result, the output voltage has a little change of about 0.01 mV when

temperature increases from 0 °C to 225 °C. This small change is totally acceptable in this application.

The DC simulation is a general check for the high temperature capability. To further verify the stability of high temperature performance, we also check the gain of the amplifier under different temperature. This is done in Spectre with AC simulation setting different temperature. A simulation result of different gains under different temperature is shown in Figure 4-12, a 50 °C step is chosen in the plot.

Figure 4-12 gain under different temperature.

In the simulation result, the gain shows little change from 0 °C to 225 °C in the frequency less than 2 kHz, which is the main bandwidth for this application. More detailed results are shown in the Table 4-1.

Table 4-1 Gain under Different Temperature at 800 Hz

Gain & Temperature (800 Hz)			
Temperature (°C)	Gain	Temperature (°C)	Gain
0	10.08	150	10.04
50	10.07	200	10.02
100	10.06	225	10.03

We can see that, from the extreme condition 0 °C to 225 °C, the gain only changes by 0.5 %, which is acceptable for this application.

4.3.4 Noise Simulation of the Chopper Amplifier

By modulating the low frequency input signal to high chopping frequency and then demodulated back, while the noise and the offset is modulated only once to high frequency, chopper amplifiers use chopping technique to remove the low frequency noise. The chopper is realized with eight MOS switches as illustrated in Figure 4-6. Common SPICE-like noise simulators calculate noise based on a linearized small-signal model with the circuit operating at DC point. Frequency translation noise, due to the chopping switch, cannot be directly calculated in these simulators because of the linearization model basis. For instance, such SPICE-like simulators could only simulate the noise of those circuits based on the DC operating point with Φ and Φb fixed, but they could not calculate those with Φ and Φb are periodically changing. Therefore, the conventional SPICE-like noise simulators could not estimate noise in chopper amplifiers.

The SpectreRF simulator [32] enhance the conventional time-domain methodology to deal with RFIC calculations. The Newton shooting approach is applied to simulate the periodic-steady-state (PSS) response of RFIC circuits such as oscillators. The chopper amplifier's period is the time with a modulation switch opening once and closing once, namely the reciprocal of the chopping frequency. In addition, SpectreRF can efficiently process strong linearized circuits.

PSS response of the circuit need to be run first in order to simulate a chopper amplifier with SpectreRF, the PSS response determines the periodical operating point of the circuit. During the PSS simulation, only the chopper clock will be applied and the periodic input of the circuit is biased to a common input voltage. With the help of the chopper clock, PSS response will determine the period of the circuit. Based on the simulated periodical operating point, SpectreRF can then analysis the noise of the chopper amplifier by running the Periodic Noise (Pnoise) analysis. PNoise analysis is similar to the conventional noise analysis, except that it includes frequency conversion effects. Hence, it is useful for predicting the noise behaviour of chopper amplifier. The output referred noise of the chopper amplifier is shown in Figure 4-13 as a result of the simulation of SpectreRF Pnoise analysis.

Figure 4-13 output referred noise plot at 700 Hz.

The output referred noise at 700 Hz is about 25.61 nV/sqrt(Hz). As expected, a spike at about 32 kHz chopping frequency is present in the output noise with chopping, and this inconsequential spike constitutes the energy of the modulated offset and noise.

A comparison simulation result of the chopper amplifier with and without chopping is shown in Figure 4-14.

Figure 4-14 output noise with and without chopping comparison.

With chopping techniques, the output referred noise is reduced much in low frequency. For high frequency, the thermal noise dominates the noise contribution, so they become closer.

4.3.5 Post-layout Simulation

The layout of the chopper amplifier were carefully drawn to realise good low noise specification and high temperature performance. To diminish the negative effects generated by the fabrication process, temperature variances and the mechanical constraints as well, the large area PMOS differential input pairs of the preamplifiers are drawn at the centre of the layout. Capacitive dummies are used

to fill in the empty space which can also enhance low-noise performance. The Micrograph of the chopper amplifier is as shown in Figure 4-15. The chip size is $3325\text{ }\mu\text{m} \times 3150\text{ }\mu\text{m}$.

Figure 4-15 micrograph of XMX2319A.

The post layout simulation of the preamplifier is shown in Table 4-2. Simulations for checking process, voltage and temperature (PVT) variation effects on on-chip interconnect, as well as via structures are performed. Typical mean (*TM*) parameters is extracted from typical wafers. *WP* stands for worst case power, which is the fast NMOS and fast PMOS parameters. *WS* stands for worst case speed, namely the slow NMOS and slow PMOS are used.

Table 4-2 Post-layout Simulation Results for Chopper Amplifier

Parameters	Description	Spec.	Temp (°C)	Worst(wp)	Typcial	Best(ws)	Unit
				VDD -10%	VDD	VDD +5%	
Gain	Gain	20	-50	20.07	20.06	20.06	dB
			0	20.07	20.07	20.06	
			50	20.06	20.05	20.03	
			100	20.09	20.05	20.04	
			175	20.10	20.04	20.03	
			225	20.08	20.02	20.04	
PM	Phase Margin with 10 pF Load	>30	-50	97.81	99.16	115.1	Degree
			0	104.4	77.58	86.52	
			50	106.7	77.9	77.08	
			100	75.51	87.96	70.08	
			175	79.69	83.67	74.16	
			225	86	64.59	74.64	
UGB	Unity Gain Bandwidth	1	-50	2.081	1.406	0.859	MHz
			0	1.667	1.319	0.825	
			50	1.443	1.269	0.807	
			100	1.339	1.059	0.748	
			175	1.197	0.845	0.670	
			225	1.057	0.804	0.605	

4.4 Chopper Amplifier Measurements

The chip has been fabricated using XFab 1.0 μm SOI process. A measurement PCB is designed according to the Spectre simulation setups. This PCB is used for normal temperature measurement. In the measurement, the following 4 steps will be conducted.

- Step 1, Steady state signal waveform;
- Step 2, Frequency response;
- Step 3, Noise Measurement;
- Step 4, High temperature performance.

Step 1 is to verify the amplifying function of the preamplifier; Step 2 is to measure the frequency response of the preamplifier; Step 3 is conducted to test the output-referred noise; Step 4 aims to test the high temperature performance of the preamplifier.

4.4.1 Steady State Signal Waveform

The chopper amplifier measurement setup is shown in Figure 4-16. The accuracy of the input capacitance is important for the gain of the chopper amplifier. The current source is provided by the resistor divider circuit. The temperature test will be carried out after the PCB back.

(a)

(b)

Figure 4-16 (a) steady state response measurement setup, (b) measurement PCB for the chopper amplifier.

The steady response of the chopper amplifier is shown in Figure 4-17. We can see from the input (green one in the oscilloscope) wave and output signal wave (white one), the signal performance of low-noise characteristic is good.

Figure 4-17 steady state response of the chopper amplifier.

4.4.2 Frequency Response

Agilent 35670A Dynamic Signal Analyzer is used to measurement the frequency response of the chopper amplifier. The Dynamic Signal Analyzer is able to process signal from ~0 Hz to 51.2 kHz. The measurement setup and results are shown in Figure 4-18.

Figure 4-18 (a) measurement setup, (b) frequency response of the chopper amplifier.

At 20 kHz, the gain is 19.65 dB. Since the Analyzer is limited band within 50 kHz. The full band frequency response is not available. But for chopper amplifier, the low frequency is used only. So it is enough to observe the frequency response within 50 kHz.

4.4.3 Noise Measurement

Agilent Dynamic Signal Analyzer 35670A is used to measure the noise power spectra. The input signals are both set to the common mode voltage 2.5 V. Under this condition, the output signal is supposed to be the noise of the amplifier. The output signal has a DC voltage of 2.5 V. In order to make the noise be displayed without the DC signal, we need to add a DC block component before the output signal is input to the analyzer. The power spectra will be displayed by the Dynamic Signal Analyzer.

(a)

(b)

Figure 4-19 (a) noise measurement setup, (b) noise power spectra of chopper amplifier.

The measured noise power spectra are shown in Figure 4-19. The output-referred noise at 1 kHz is about 599 nVrms. The noise is larger than the simulated result.

This is because PCB itself also contributes quite much noise. As expected, near the chopping frequency 32 kHz, there is a peak.

4.4.4 High Temperature Performance

In order to measure high temperature performance up to 225 °C, a high temperature capable PCB is designed. The measurement setup and results are shown in Figure 4-10. The temperature chamber is ESPEC SU-240, it can provide temperature in the chamber up to 330 °C.

(a)

(b)

Figure 4-20 (a)high temperature measurement setup, (b) high temperature frequency response.

The gain of the preamplifier is measured under different temperature as shown in Table 4-3. 20 kHz is chose since it is near the center frequency of the preamplifier. The preamplifier is working properly under 300 °C.

Table 4-3 Gain under Different Temperature at 20 kHz

Temperature(° C)	Gain(d B)	Temperature(° C)	Gain(d B)	Temperature(° C)	Gain(d B)
20	19.65	180	19.20	250	18.78
40	19.56	200	19.17	255	18.74
60	19.50	220	19.01	260	18.70
80	19.41	225	18.97	265	18.68
100	19.35	230	18.92	270	18.62
120	19.23	235	18.88	280	18.46
140	19.39	240	18.87	290	18.29
160	19.32	245	18.82	300	18.16

From 20 °C to 160 °C, the gain attenuate 0.33 dB; when the temperature increasing to 225 °C, which is the XFab SOI 1- μ m process supporting temperate, the gain is 18.97, losing 0.68 dB compared with that on 20 °C. It is interesting that when the temperature goes all the way up to 300 °C, the gain and the bandwidth of the amplifier are still in good condition. In 300 °C, the gain of the chopper amplifier is 18.16 dB; it has only 1.49 dB attenuation compared with 20 °C. So the high temperature performance of the chopper amplifier is excellent.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The design and implementation of two high temperature low noise front end amplifiers for the receiver of acoustic telemetry system are presented in this thesis. The potential input signals for the receiver of the telemetry system, which are produced by the piezoelectric transducers, are introduced. High temperature behaviours of MOSFET ICs are discussed; a constant- g_m bias circuit for cascode amplifier are studied. Literature review on noise specification of an amplifier is conducted. Various design methods on low noise preamplifier are reviewed with a discussion of the requirements and important issues involved in the design.

For successful operation of integrated circuits in high temperature regime ($> 170\text{ }^{\circ}\text{C}$), a proper technology choice is a first consideration. For high temperature application, the silicon-on-insulator (SOI) process is a promising candidate. The leakage current of the SOI devices is much lower than CMOS transistors. This is because the thin bulk region of the SOI devices is isolated with insulator. Besides, the threshold voltage changes less with temperature in SOI transistors than their bulk-CMOS counterparts. In addition, the latch-up immunity of SOI devices is better, which helps to improve the reliability of circuit operation at higher temperature. Most of the commercial SOI processes are specified over $200\text{ }^{\circ}\text{C}$. XFab $1.0\text{ }\mu\text{m}$ SOI process is chose for the amplifier design; it is specified up to $225\text{ }^{\circ}\text{C}$ which fully meet the requirement of the project.

The front end amplifier is the most critical component of the receiver in a wireless telemetry system as it comes at the most front-end of the system and most of the

system parameters depend on the performance of the front-end amplifier. The noise performance of the front-end amplifier determines the detection accuracy of the overall system. A PMOS input capacitive feedback preamplifier is designed. In an N-well process, PMOS transistors have much less leakage current than NMOS. PMOS transistor has better threshold voltage mismatch property, lower flicker noise and a quite comparable current driving capability compared to its counterpart NMOS transistor. Using PMOS as the input devices can reduce the noise at the first stage. Capacitive feedback noise reduction circuit is used in this design. Simulations show that the preamplifier can work up to 225 °C with a input-referred noise about 83.4 nV/sqrt(Hz) at the total current consumption of 40 μ A.

Due to the very low flicker noise available, chopping technique is applied in the low noise high temperature SOI-CMOS preamplifier for the receiver of the wireless telemetry system. Chopping as a technique for reducing $1/f$ noise has been considered for low frequency signals like acoustic wave signal which frequency is less than 2 kHz. Three opamp structure chopper amplifier is designed in chapter 4 to gain better low noise performance. Simulations showed that the chopper amplifier is able to work up to 225 °C with a input-referred noise about 25.6 nV/sqrt(Hz) at a total current consumption of 5.496 mA.

The PMOS input capacitive feedback preamplifier and the chopper amplifier are designed and fabricated using 1.0- μ m XFab SOI process. The PMOS input capacitive feedback has much lower power consumption while providing quite good low noise performance. The chopper amplifier can achieve better low noise performance but it is at the sacrifice of more power consumption. Measurements

show that the PMOS input preamplifier is able to work under 180 °C and the chopper amplifier is able to work under 300 °C.

5.2 Future Work

The research conducted during my master study focuses mainly on the design of the analog front-end amplifier for the receiver of the acoustic telemetry system. The proposed circuits realize the basic function of piezoelectric signal amplifying. However, there is still some work to be done.

First, measurements of the amplifier circuits need to be explored. The measured noises of the circuits are much larger than the simulated results. This may because the measuring PCB contributes much noise. Low noise PCB design for noise measurement purpose will be explored.

Second, the integration of the preamplifiers into the receiver of the telemetry system may be another topic. For the receiver, as shown in Figure 5-1, the acoustic signal received by the piezoelectric transducer will be first received by the low noise preamplifier, followed by the filter and the amplifying component. An ADC will be employed to convert the analogue signal to digital signal. After ADC, the signal will be processed by a signal process unit. All the devices in the receiver need to work under the high temperature environment. The integration of the receiver may be a good topic.

Receiver

Figure 5-1 receiver of the telemetry system.

Another further research topic may be the low power low noise preamplifier design for high temperature applications such as the wireless telemetry system. Power efficiency of the preamplifier for the receiver of the wireless telemetry system application is very important due to the limit power available from a battery under 2 km to 3 km from the surface of the ground. This requires the preamplifier designs optimize between white and flicker noise level and power consumption level while maintaining radiation and temperature hardness. This may be another interesting topic.

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