Reconfigurable amplifier design techniques for microwave and millimeter-wave applications

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Reconfigurable Amplifier Design Techniques for Microwave and Millimeter-wave applications

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other university or institution.

09/09/2015 — Date

Bharatha Kumar Thangarasu — Bharatha Kumar Thangarasu

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List of Abbreviations

3D	Three dimensional
ADC	Analog to digital converter
AGC	Automatic gain control
ASIC	Application specific integrated circuit
BB	Baseband
BDA	Bi-directional amplifier
BER	Bit error rate
BGR	Bandgap reference
BiCMOS	BJT and CMOS transistors
BJT	Bipolar junction transistor
BW	Bandwidth
CB	Common-base
CC	Common-collector
CD	Common-drain
CE	Common-emitter
CG	Common-gate
CMFB	Common mode feedback
CMOS	Complementary metal oxide semiconductor
CS	Common-source
DAC	Digital to analog converter
dB	Decibel
dB-Linear	Linear-in-decibel
DCOC	DC offset canceller
DCR	Direct conversion receiver

DVGA	Digitally variable gain amplifier
EM	Electro-magnetic
FBW	Fractional bandwidth
FCC	Federal communications commission
FoM	Figure-of-merit
GaAs	Gallium-arsenide
GBW	Gain-bandwidth product
GND	Ground
HBT	hetero-junction bipolar transistor
HFSS	High frequency structural simulator
HICUM	High current model
HPF	High pass filter
IF	Intermediate frequency
IP_{1dB}	Input 1-dB compression point
ISM	Industry-scientific-medical
ITRS	International technology roadmap for semiconductors
LC	Inductor-capacitor
LMDS	Local multipoint distribution service
LNA	Low noise amplifier
LPF	Low pass filter
LSB	Least significant bit
MOS	Metal oxide semiconductor
MSB	Most significant bit
NF	Noise figure
NMOS	N-channel metal oxide semiconductor

OP_{1dB}	Output 1-dB compression point
PAE	Power added efficiency
PD	Power down
PDK	Process design kit
PGA	Programmable gain amplifier
pHEMT	Pseudomorphic high electron mobility transistor
PMOS	P-channel metal oxide semiconductor
PNA	Performance network analyzer
Psat	Saturated power
PTAT	Proportional to absolute temperature
PVT	Process-voltage-temperature
PwrDwn	Power down
Q-factor	Quality factor
RC	Resistor-capacitor
RF	Radio frequency
RFIC	Radio frequency integrated circuit
SiGe	Silicon-germanium
SNR	Signal-to-noise ratio
SoC	System-on-chip
S-parameter	Scattering parameters
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier

Abstract

In recent years, the motivation for both the academic and industrial research on radio frequency integrated circuit (RFIC) design is driven by the commercial need to support large data rate wireless communication accompanied by multiple functionalities within a single consumer mobile device. There are many baseband standards for wireless communication such as IEEE 802.11 that defines the parameters and characteristics of the design to support such applications in the 2.4, 3.6, 5 and 60 GHz frequency bands. However, the cost of semiconductor fabrication in the state-of-the-art process technology as well as the demand for smaller form factor of the final product to support such high data rate RFIC transceiver design and to meet specifications of various standards simultaneously becomes a challenging aspect for the RFIC designers. Hence the re-configurability is evolving as a major keyword for such "Smart" designs that can support various standards and functionalities by changing the operating conditions of the same fabricated design using external digital/analog control settings.

The amplifiers provide an excellent option for re-configurability in the RF transceiver design such as control of the amplifier's gain (amplification/attenuation), center frequency, bandwidth, directionality (uni- or bi-directional), etc. The re-configurability for amplifiers can be achieved by discretely or continuously changing one of the design parameters by using the transistor switches such as the load resistance, biasing voltage, biasing current, degeneration resistance, etc., that influence the amplifier performance parameters. One such popular example for reconfigurable design is the variable gain amplifier (VGA) circuit block that performs the key function of varying the gain in accordance with either digital or analog gain control.

The VGA is a key building block to control the gain of a RF transceiver chain to maintain the link budget according to the baseband requirements and to support mobile applications with dynamic transmitting and receiving signal strengths. The system requirement of a generic VGA in the RF transceiver is to provide a seamless (unchanged) integration with a minimum tolerance for the deviation of the impedance matching, interface common mode dc, bandwidth, gain flatness, dc power consumption, and stability over the entire VGA's gain control range.

As the level of integration for the modern day “Smart” mobile devices like the cell phones, tablets, laptops, PDA, etc. against the same or compact form-factor results in the limited silicon die area required for including and implementing the various transceiver blocks to meet most of the standards. Hence a better alternative to alleviate this constraint can be achieved by designing reconfigurable amplifier blocks which have research potential with many possibilities like the multiple path selection, bi-directional amplifiers, multi-band, etc. Such designs provide efficient silicon area utilization and also low power consumption that reduces the demand on the battery life of the final product.

Chapter 1. Introduction

1.1. Introduction to reconfigurability and emphasis to amplifier design

This is the world of "Smart" devices including the smart phones, smart television, smart automobiles, smart home, etc. The economy and research in the electronics industry is being driven by this interest of the modern generation. This interest transforms into integrating several functionalities and features into a single device as well as to support mobile communications. To achieve such varying range of functionalities requires that the design building blocks can support multi-band, multimode and multi-standard RF transceivers. To increase the battery-life and also the product form factor the building blocks must consume low DC power and have compact design footprint. To simultaneously achieve both the support for various functionalities (diversity) as well as improved performance (efficiency), one of the most promising research option is the "reconfigurability".

Reconfigurability is defined as a property of a system/design to configure/ program either by itself or by providing external controls and changing its behavior or its operating conditions by reusing the same resources. By incorporating reconfigurability, the building blocks of the smart devices can support large data-rate wireless communication protocols and multiple functionalities within a single consumer device by avoiding redesign and re-fabrication. This reconfigurability option can also be used as a post-fabrication corrective option to achieve the best performance.

One of the main building blocks in the smart devices/wireless transceivers is the "amplifiers" that can selectively improve the strength of the desired signals and filter out the other unwanted signals. A general transceiver for wireless communication needs to handle a variable signal strength at the receiver and the transmitter chain. This

is achieved by using the automatic gain control (AGC) block that provides a stable output power level to the digital baseband processing section [1.1] as shown in the Figure 1.1.

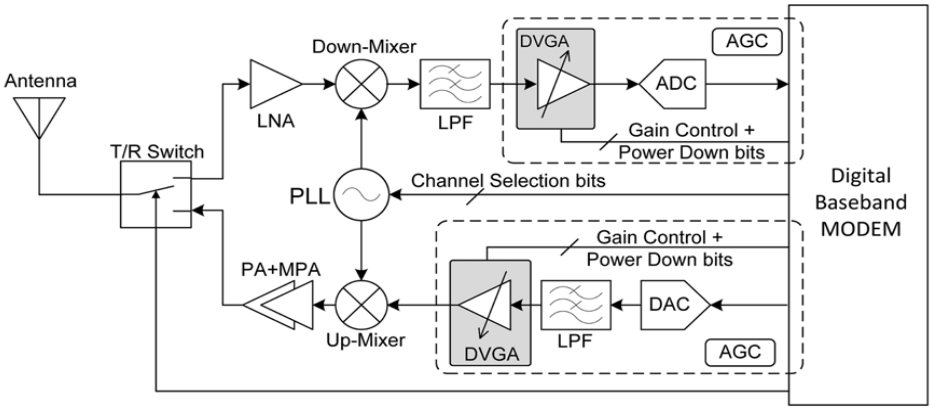

Figure 1.1 RF transceiver with amplifiers and AGC block interfacing with baseband.

1.2. Motivation

As this research direction is been perceived in the electronics industry, to provide a quick time-to-market as well as a uniform interface definition depending on the final application of the product, several international standards [1.2] have been put forth such as Wi-Fi (IEEE 802.11a/b/g/n), WiGig (IEEE 802.11ad), etc. as shown in the Figure 1.2. In the past, to minimize the design efforts several application specific integrated circuits (ASIC) were designed but their scope was limited to only that application. With the design reconfigurability, there exists a scope to support multiple standards, multiple modes and multi-functionalities by a single design. This greatly reduces the form factor of the end product as well as cut down on the fabrication costs involved in designing multiple building blocks.

Figure 1.2 Smart devices and multiple standards.

Along with the state-of-the-art advancement in the performances of the radio frequency integrated circuits (RFIC) building blocks, the fabrication houses have also shown a constant trend in shrinking the transistor device node that can support higher frequency, low power and also operate at low voltages. In the past, only the III-V (GaAs pHEMT) semiconductor technology was used in designing such high frequency RFICs. However, such process technology which was engineered to provide high performance at the RF, involved complex fabrication steps and eventually resulted in higher cost. Recently, the complementary metal oxide semiconductor (CMOS) process is evolving to support such high frequencies although with limitations due to the device physics [1.3]. In parallel, the process supporting hetero-junction bipolar transistors (HBT) along with the CMOS devices such as the silicon germanium (SiGe) BiCMOS process have paved way for supporting the high density digital CMOS integration with the RF high performance that can meet the requirements of the micro-wave and millimeter-wave applications [1.4]. This SiGe process is based on the silicon substrate with an epitaxial layer of germanium grown to form the hetero-junction base

region of the bipolar junction transistors (BJT). This improves the device performance including the gain and noise characteristics and also provides an additional improvement for high frequency designs by controlling the doping density of the base even with an older process node dimension. Most of the implementation in this research work is fabricated using the Tower Jazz Semiconductors 0.18 µm SiGe BiCMOS process as well as Global Foundries 65nm CMOS process.

1.3. Objectives

By designing and verifying the reconfiguration capability of the RFIC amplifiers, a design approach to simultaneously achieve both the support for various functionalities (diversity) as well as improved performance (efficiency) is proposed in this research work. Several amplifier design techniques are recommended and the proposed amplifier reconfigurability is verified by on-wafer measurement of the fabricated dice.

A typical amplifier has a frequency response as shown in Figure 1.3 that is characterized by its gain (A), bandwidth (BW), center frequency (fc), directionality (uni- or bi-directional), etc. This research work involved in the analysis of the amplifier parameters that affect these performance characteristics and then provide options in the form of switching (digital control) or fine tuning (analog control) by external control signals. A more detailed illustration on the analysis and design techniques is provided in the following chapters.

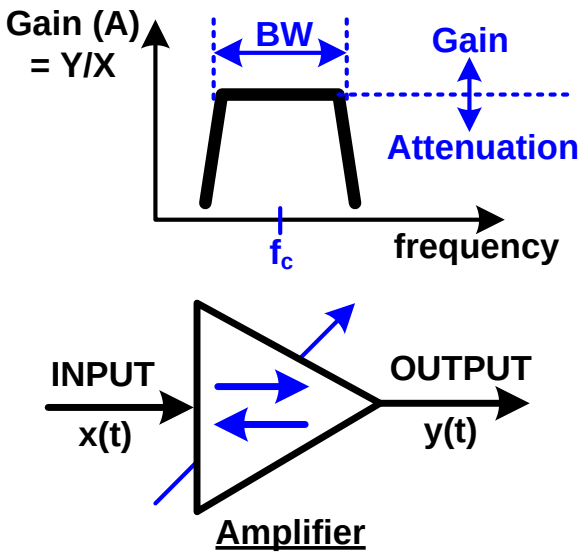

Figure 1.3 Amplifier characteristics with reconfigurability options.

1.4. Thesis Overview

This thesis presents design techniques along with verification by on-wafer probing measurements for the various reconfigurable amplifier designs that are fabricated using the Tower Jazz Semiconductor 0.18 µm SiGe BiCMOS process and the Global Foundries 65nm CMOS process.

Chapter 2 reviews the various types of amplifier reconfigurability options including the control of the gain (amplification/attenuation), bandwidth, center frequency (operating frequency range), directionality, phase shifters using vector modulators, etc. This study is followed by the classifications of reconfigurable amplifiers based on the modes of reconfigurability (digital, analog or mixed-mode control), circuit parameters affecting reconfigurability (transconductance, load resistance, etc.), active devices used in the design (III-V pHEMT, SiGe HBT, CMOS, etc.), frequency range (microwave, millimeter-wave, THz, etc.), transceiver mode (receiver/transmitter), and the parameter control mode (current-mode or voltage-mode). This chapter concludes with the desirable performance considerations of the reconfigurable amplifiers.

Chapter 3 proposes some of the design evolutions of the variable gain amplifiers (VGA) that incorporates several features to support its integration into a robust RF transceiver without degrading the performance in this process. This chapter is derived from the authors published works namely [A.1], [A.2], [A.4], [A.7], and [A.8]. This chapter illustrates the design techniques and the circuit analysis involved with gain control linearity (linear and dB-linear), DC offset cancellation (DCOC), temperature compensation, on chip linearizer, common mode feedback (CMFB), gain-bandwidth (GBW) extension, etc. This chapter also provides the details of circuit implementation and the on-wafer measurement results.

Chapter 4 proposes a variable bandwidth VGA with a compact design highlighting the current mode linear gain control along with a switch control to activate or deactivate DCOC as well as a fine tuning control of the amplifier bandwidth's lower cutoff frequency. This design is fabricated in a 65nm CMOS process and the work is published in [A.3].

Chapter 5 proposes a variable center frequency VGA by using a transformer coupled load. This implementation gives a new dimension for designing multi-band amplifiers. By using the Q-factor enhancement techniques an improved amplifier power efficiency is achieved in this work. This work is based on a current reuse differential amplifier design and this work is submitted for publication in [A.9].

Chapter 6 presents a variable directionality VGA that is designed based on the bidirectional control by the amplifier power down control and low loss transmission line matching. This design has two back-to-back connected 60 GHz low noise amplifiers (LNA) providing an improved BW, low loss and NF performance and is implemented by using the 65nm CMOS process. The work based on the on-wafer measurement result of the standalone LNA is submitted for publication in [A.10].

Chapter 7 provides the thesis conclusion and also recommends the various reconfigurability options for future work in this research direction.

References

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Chapter 2. Literature Review of the various types of amplifier reconfigurability options

Amplifiers are needed in the wireless transceivers to boost the signal strength overcoming the losses introduced by the signal path [2.1]-[2.13]. The amplifiers provide gain to the input signal transforming the energy from a dc source. Such amplifiers are characterized predominantly based on their frequency domain response as follows.

2.1. Types of Amplifier reconfigurability

2.1.1. Gain (Amplification/Attenuation)

VGA is a key radio frequency frontend building block that supports mobile communication of wireless transceivers [2.14]-[2.26]. The range of VGA gain control also determines the receiver input dynamic range that provides a stable regulated power to the baseband chipset. The research drive for recent RFIC design is to focus on high data rate communication in giga-bit per second (Gbps) range. Hence the VGA that interfaces with the baseband may need to support large bandwidth. As the state-of-the-art improves, the supported applications as well as the design density for system integration of the RF transceivers also gradually increasing towards System-on-chip (SoC) solutions.

For the proposed VGA to be integrated in a compact transceiver system, it is desirable to have certain enhanced features such as low dc power consumption, small die area, impedance matching achieved at input and output ports, less sensitive to Process-Voltage-Temperature (PVT) variations, high linearity performance for both

RF signal input as well as gain control input, good wideband gain-flatness, and easy interface to digital baseband which are independent of a stable gain control.

Based on the modes for gain control, the VGA can be classified as analog gain control (VGA) [2.14]-[2.22] and discrete or digital gain control VGA (DVGA) or programmable gain amplifier (PGA) [2.23]-[2.26]. In analog VGA the digital baseband requires an additional digital to analog converter (DAC) to control the gain variation that eventually increases circuit complexity. DVGA can be directly interfaced with the digital baseband without the need for DAC.

A DVGA can be implemented at circuit level by switching between fixed gain amplifier stages [2.24] or by using a binary weighted array of passive or active circuit components selected discretely using transistor switches [2.23], [2.25], [2.26]. The switching gain stage DVGA consumes large die area due to circuit duplication, while the DVGA with switching circuit components are compact and consuming less gain control linearity errors.

Linearizer:

One of the desirable quality of an amplifier is high linearity performance, which determines the maximum signal level that can be amplified without output signal distortion. The linearity performance in the RF receiver chain ensures a large dynamic range and in the RF transmitter chain ensures long communication distance. This output signal distortion is caused due to large input signal resulting in the circuit components entering their non-linear operating region. To improve linearity of the amplifier, a diode-connected linearizer is used in power amplifier designs [2.27]-[2.29]. Although they require reference voltages to bias the linearizer diode that are higher

than supply voltage. It is desirable that the DVGA supports large signal amplitudes without saturation and in this process consumes low dc power.

GBW enhancement:

To support low power applications the process node as well as the supply voltage are gradually down-scaled. This limits the gain of a single amplifier stage. Hence to increase the gain without increase in the supply voltage we need to implement the multi-stage cascaded amplifier topology. Theoretically the cascaded identical amplifier stages [2.30] provides the desirable increased gain shown in (2.1) but at the expense of shrinking the bandwidth determined by the number of cascaded stages given by (2.2).

$$|A_T| = \frac{|A_0|^n}{\left[\sqrt{1+\left(\omega/\omega_0\right)^2}\right]^n} \tag{2.1}$$

$$\omega_T = \omega_0 \cdot \sqrt{2^{1/n}-1} \tag{2.2}$$

where, the gain and bandwidth of the overall cascaded amplifier are A_T and ω_T which consists of *n* identical stages with A_0 and ω_0 as the individual stage gain and bandwidth, respectively.

By incorporating interconnect stage with gain peaking such as the resistor-inductor-capacitor (RLC) bandpass network [2.31], peaking inductors [2.32], on-chip transformers [2.34]-[2.35] and also by using wideband distributed amplifiers [2.33], an enhanced bandwidth can be achieved. However this enhancement techniques results in large die area and also affects the pass-band gain flatness and in some cases result in system instability. One of the possibilities with small die area is to replace inductors with resistor-capacitor (RC) bandpass networks which is proposed in chapter 3.

In chapter 3, the proposed design is a high performance DVGA based on digital gain control by using SiGe BiCMOS HBT as the amplifying device and the amplifier transconductance is varied by using NMOS switches as current mirrors. In this chapter a detailed design consideration based on the low cost, compact size, good linearity, and less temperature sensitive digitally controlled variable gain amplifier (DVGA) with integrated dB-linearizer, passive dc offset cancellation and transimpedance load based linearizer is studied and developed. By employing bipolar transistors in current mirror configuration and by canceling the effect of the thermal voltage (V_T) across the transistor's base-emitter junction, a temperature compensated DVGA core along with a good dB-linear characteristics is achieved in this design. To enhance the gain control range as well as increased gain bandwidth product, the proposed PGA consisting of two identical cascaded DVGA core and a fixed gain post amplifier with differential RC interconnect networks are theoretically analyzed and experimentally verified by on-wafer probing measurements. Additionally, by implementing the current mode gain control technique that improves the accuracy of proposed PGA's dB-linear gain steps and the as well as limits the rail-to-rail dc current reducing the overall dc power consumption as compared to the existing state-of-the-art.

2.1.2. Bandwidth

Bandwidth is defined as the range of frequencies that has the amplifier gain above half the peak gain. In this frequency range the amplifier gain flatness is to be maintained to avoid any instabilities or spurious frequency components. The variable bandwidth amplifiers are proposed to provide a tradeoff between the wideband signal amplification to support large data-rate applications as well narrowband designs with improved frequency selectivity to reject any nearby interference signals [2.30].

The dc component in baseband spectrum along with manufacturing mismatches in differential pair results in offset amplification that may saturate the following stages in baseband circuitry and also introduce non-linearity effects [2.36]. There are various circuit methods to overcome the dc offset, specifically by implementing dc offset canceller (DCOC) such as, feedback offset cancellation [2.18], [2.43] using low pass filters (LPF), and feed-forward offset cancellation [A.4] using ac coupling between the stages by large decoupling capacitors [2.44]. The DCOC can also be achieved by complex digital signal processing (DSP) offset cancellation technique [A.8] which is based on feedback obtained from the digital baseband by tracking the average signal value. It is a complicated approach consuming more dc power and die area [A.8]. Therefore, a low loss, low power, and compact DCOC becomes essential for VGA designs.

As a comparison among the passive (resistors and capacitors) DCOC, RC-LPF with a same cutoff frequency has larger passband insertion loss than high pass filter (RC-HPF) equivalent DCOC. This is mainly due to the large filter resistor of RC-LPF that appears in series along the signal path. For increased dc offset suppression using RC-LPF in the feedback DCOC, the amplitude of dc component filtered out by the LPF must be equal to the dc component of the input signal. To achieve the required loop gain at dc (0 Hz frequency), high gain amplifiers are incorporated in the DCOC loop [2.18], [2.43], [A.4]. The amplifiers compensates for the loss due to feedback LPF and effectively cancels the dc offsets. However, such high gain amplifiers consume additional dc power. Hence a RC-HPF based DCOC is proposed and described in Chapter 3 but comes with the trade-off of additional die area.

To prevent this increased area utilization of RC-HPF DCOC, a CMOS high gain VGA is proposed in Chapter 4 that can provide a dc rejection by using the dc offset

cancellation (DCOC) by feedback low pass filtering (LPF). By providing a higher DCOC cutoff frequency as a band pass filter (BPF) response, a good dc offset suppression can be achieved to meet the BER requirement of the specified baseband standard [2.37].

For a majority of baseband communication standards [2.36], at the receiver chain, a high signal to noise ratio (SNR) at the baseband is a critical specification. Due to a higher DCOC corner frequency [2.41], the signal in baseband spectrum close to dc [2.37] are lost and hence the SNR gets degraded. Conversely, a lower cutoff frequency close to dc results in an ineffective dc offset cancellation. To provide a better compromise between these two complementary circuit requirements such as BER and SNR from the baseband standards, many reconfigurable RF frontend to BB interface techniques are proposed in the literature such as digitally switching VGAs with and without DCOC [2.38], by using active amplifier based RC filters with switched capacitors [2.39], by using channel-select dual-mode filters that switch between complex high order LPF and BPF transfer functions implemented by operational amplifier based auto-tuned RC filters [2.40], by using lumped RC arrays that are switched digitally for tuning filter cut-off values [2.41] and also by using current-mode programmable complex OPAMP based integrator [2.42]. However, there are some limitations for such works namely redundancy due to duplicated circuitry leading to large die area, increased circuit complexity involving high order filters, high dc power consumption by the active filters and additional signal insertion losses with delays in the RF signal path introduced by the parasitic components.

In Chapter 4, a CMOS based VGA is the proposed that provides a flexibility of digitally turning ON/OFF the DCOC functionality by using a digital switchable feedback amplifier along with an analog voltage continuously controlled filter lower

cutoff frequency that can provide an enhanced compromise between the contrasting baseband SNR and BER requirements. Hence this reconfigurable capability along with variable gain control can support multi-standard baseband [2.36] interface that can easily switch between direct conversion receiver (DCR) i.e. zero-IF (direct conversion scheme) and tunable low-IF (superheterodyne) receiver topology schemes [2.40].

2.1.3. Center frequency (operating frequency range)

The rising demand for the short-range high-speed wireless communication systems in the recent decades have motivated the research work of radio frequency (RF) integrated transceiver design for the diversified *K*-band (18–27 GHz) and *Ka*-band (26.5– 40 GHz) applications including the wireless sensor network (WSN) [2.46], the 24 GHz Industrial Scientific and Medical (ISM) band for gigabit-per-second wireless network solution [2.45], the local multipoint distribution service (LMDS) for wireless point-to-multipoint communication (27.5–29.5GHz) [2.48] and also the short-range automotive radar applications (22–29 GHz) for anti-collision detection [2.46], [2.49], [2.50]. This requires multiple designs operating at different center frequencies to be included within the same system. Hence resulting in increased die area and design duplication. An efficient way of switching circuit components that can switch center frequency of the operating frequency range of the transceiver becomes desirable.

The most power consuming section in a RF transceiver is the transmitter and in particular, the power amplifier (PA). A critical design requirement for mobile applications is how the PA can efficiently convert the input and dc power to the RF output power which directly translates into a low product cost and a long battery life, besides delivering high output power and power added efficiency (PAE), the PA linearity is another important requirement that preserves the signal integrity with less

distortion. The design of PAs often involves the tradeoff between the efficiency and linearity.

The alternative choice is the CMOS process. However, the CMOS transistors have limited power handling capability and as the operating frequency increases towards GHz range and above, the amplifying device size becomes smaller for reduced parasitic, higher f_T and lower V_{beo}. As discussed in [2.51], the output power level increases with increase in the supply voltage of the output stage. To simultaneously mitigate the device limitation of low V_{beo} and support a large supply voltage that increases the output power, a stacked amplifier design using the dc current reuse technique was proposed in [2.52]. However, a large form factor of the battery is required to support such large supply voltage. This limitation of the CMOS PA can be simplified by using several design techniques. One such design technique is the switched mode PA in which the circuit operation adapts dynamically, based on the instantaneous characteristics (amplitude, phase, frequency) of the input signal such as the Class E in [2.53] and Class F^{-1}/F in [2.51] that minimizes power in the amplifying transistors by avoiding overlap between the current and voltage waveforms by using digital ON/OFF switches. However, such designs require special linearization techniques to overcome the non-linearity introduced by the harmonics of the switching distorted output waveforms. In contrast, the CMOS PA based on continuous power control such as the adaptive biasing technique implemented in [2.54] and by using load impedance modulation technique of the Doherty PA in [2.55], where gain compression of the main amplifier operating in the Class AB mode is compensated by the gain expansion of an auxiliary amplifier operating in Class C mode to improve the overall linearity. However, these PA design techniques involve additional large dynamic range complex circuitry that consumes dc power.

To support the recent CMOS technology that can tolerate small signal swings, some of the power combining solutions are proposed, as the PA efficiency enhancement techniques, such as using transformers [2.56], [2.57], Wilkinson couplers [2.58], thin-film micro-strip lines [2.59], and the transmission lines [2.60] as the power splitter/combiner (with input signal distributed to multiple parallel PA stages and their outputs combined). This technique involves large die area. Another implementation technique to enhance PA efficiency is to reduce the losses involved in the passive components by implementing them as distributed equivalents in the physical layout such as the substrate-shielded coplanar waveguide (CPW) structures [2.61], transmission line transformers (TLT) [2.47] and the substrate-shielded microstrip-lines (MSL) [2.50], [2.62]. However, these distributed structures also increase the die area.

By using reverse body bias in [2.63], to reduce the leakage current of the reverse biased parasitic diodes that are formed between the substrate and the source terminal of the sub-micrometer CMOS devices, the dc power dissipation loss can be reduced and eventually improve the PA efficiency. However, this technique requires a negative voltage which has to be externally supplied or internally (on-chip) generated.

In chapter 5, a SiGe BiCMOS based dual-band (*K*-band/*Ka*-band) high power efficient differential amplifier with a hybrid solution of both a variable gain and a tunable center frequency is proposed, implemented and verified experimentally. The proposed design improves the power efficiency by simultaneously reducing the overall dc power consumption (using the stacked architecture with dc current reuse technique) and improving the amplifier linearity (using a high quality factor transformer coupled load) that increases the output signal swing and the power level. Additionally, the proposed 2-stage stacked amplifier achieves frequency band re-configurability together with the load inductance *Q* enhancement by using a tank circuit (consisting of a 2-coil

monolithic transformer coupled with a MOS varactor bank) as the tunable amplifier load. By using digital re-configurability and frequency band switching, the proposed design provides a wideband gain flatness that can support multiple K-band standards. A qualitative design analysis of the proposed frequency tunable digitally controlled variable gain amplifier (DVGA) addressing the various system considerations are discussed in this chapter.

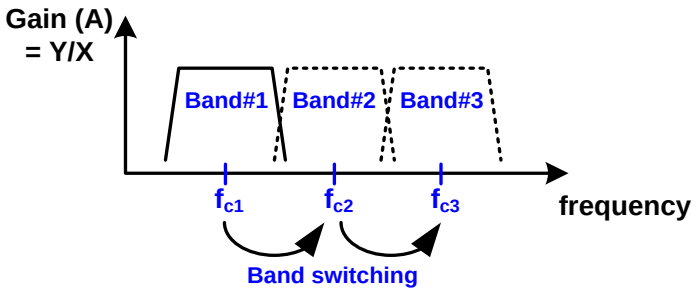
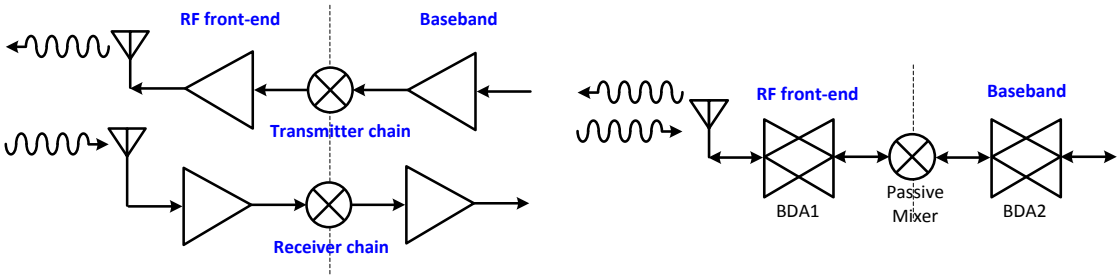


Figure 2.1 Amplifier with band switching.

2.1.4. Directionality (Uni- or bi-directional)

Most of the RF transceivers incorporated in the phase arrays to achieve beam forming and beam scanning in the radar and defense communication systems are constrained by the silicon form-factor mainly due to the transceiver's footprint duplication as shown in Figure 2.2 (a). One of the options to reduce the transceiver footprint is to combine both the transmitter and receiver chain with bi-direction signal flow capability [2.7] as shown in Figure 2.2 (b). Although the mixer design that converts frequency between RF and baseband (BB) frequency can be implemented by using passive components which will have conversion loss but can achieve bi-direction frequency conversion capability [2.8]. Somehow if the amplifiers at the RF frontend as well as the baseband amplifiers have bi-directional capability then the overall transceiver can be reduced to a single chain (saves one antenna) and just by using a digital configuration pin can operate as either transmitter or receiver [2.9]. But unlike

the passive mixer design, the bi-directional amplifiers (BDA) require active components for achieving amplification which are uni-directional devices. A detailed analysis on the design constrained and the limitation of such BDA are discussed in Chapter 6 based on a design fabricated in 65nm CMOS process.



(a) (b)

Figure 2.2 (a) Transceiver with separate transmitter and receiver chain (b) Bi-directional transceiver with single chain.

2.1.5. Phase shifters using vector modulator based on VGA

The phase arrays discussed in [2.7] mainly consists of a matrix comprising of several cascaded chains of RF transceivers and phase shifters. Phase shifters can be implemented in several ways and one of the options incorporating VGA is the vector modulators as shown in the Figure 2.3. The phase of the input x(t) is modified by the $\tan^{-1}(Q/I)$ term which are determined by the gain of VGAs (I and Q). The limitation of this design is the amplitude balance between the two VGAs.

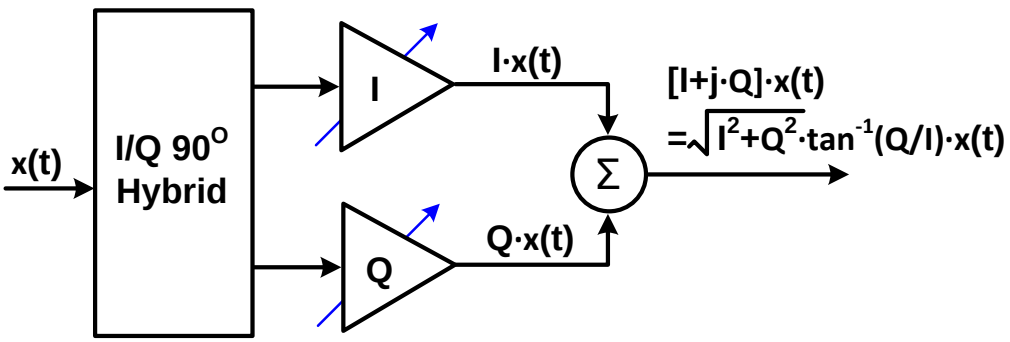


Figure 2.3 Vector Modulator.

2.2. Classifications of reconfigurable amplifiers

The reconfigurable amplifiers can be classified based on the following considerations.

2.2.1. Modes of reconfigurability - Digital and Analog control

Depending on the application requirement and the desired resolution of the reconfigurable parameters as discussed in section 2.1, the variation can be provided as discrete (digital) or continuous (analog) function of the control signal. It can be achieved by discretely or continuously varying one or more of the amplifier design parameters using controllable switches that can select or tune active or passive circuit component values that mainly influence the reconfigurable amplifier performance parameters. For the digital control the parameter control transistor is used as a switch and operated in the saturation or cut-off regions while for the analog control the parameter control transistor is operated in the linear region as shown in the Figure 2.4.

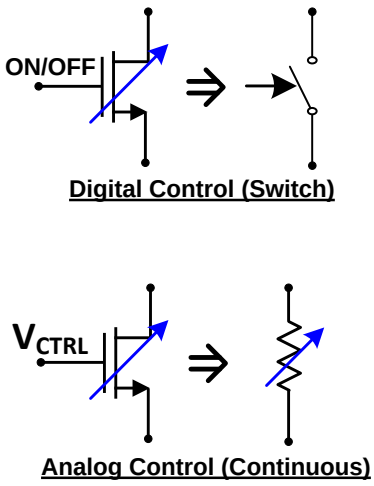


Figure 2.4 Control mode of reconfigurability.

2.2.2. Circuit parameters affecting reconfigurability

Reconfigurability in amplifiers can be achieved by discretely or continuously varying one or more of the amplifier design parameters using controllable switches that can select or tune either the load resistance, biasing voltage, biasing current, degeneration resistance or the transistor size, that mainly influence the amplifier performance parameters. A more detailed analysis is discussed in the following chapters.

2.2.3. Active devices used in the design

With the invention of semiconductor transistors the integrated electronics evolved and by device down-scaling the level of integration increased over the past several decades. Transistors are the most critical design components used in amplifiers and their characteristics mainly determine the amplifier performance. For utilizing the transistors in high frequency wireless transceiver amplifiers, they must be engineered to meet certain desirable characteristics namely provide device gain for a wide frequency range, consume low DC power, handle wide signal levels, temperatures, low noise, etc. In the past, only the III-V (GaAs pHEMT) technology was used in designing such high frequency amplifiers as it was engineered to provide high performance by involving complex fabrication steps and eventually resulted in higher cost [2.10]. Recently, the complementary metal oxide semiconductor (CMOS) process has evolved as a contender for the high frequency amplifier designs although with limitations due to the device physics [2.11]. In parallel, the silicon germanium (SiGe) BiCMOS process combining the devices to support high power namely the hetero-junction bipolar transistors (HBT) along with the CMOS devices for high density digital integration with the RF high performance can meet the requirements of the

micro-wave and millimeter-wave applications [1.4]. This SiGe process is based on the silicon substrate with an epitaxial layer of germanium grown to form the hetero-junction base region improves the device performance including the gain and noise characteristics and also provides an additional improvement for high frequency designs. Most of the implementation in this proposed research work are either fabricated using the Tower Jazz Semiconductors 0.18 µm SiGe BiCMOS process or in Global Foundries 65nm CMOS process.

2.2.4. Transceiver mode – Rx/Tx

The amplifier requirements for transmitter and receiver chain varies and are usually complementary with each other. The amplifiers used in transmitter chain must have high linearity and be able to handle large signals and increased temperature [2.12]. In contrast, the amplifiers in the receiver chain must be sensitive to small received signals and must suppress the noise signals. Hence the noise performance becomes a crucial aspect for such receiver amplifiers [2.13]. Hence designers must ensure these aspects while incorporating the reconfigurability to such amplifiers.

2.3. Performance considerations of reconfigurable amplifiers

The most critical consideration of the reconfigurable amplifiers is that the amplifier performance parameters must not be significantly altered after introducing the reconfiguration. The most desirable performance parameters that have to be additionally considered for amplifiers used in the RF transceivers are low DC power consumption, input/output impedance matching for improved power transfer, unconditional stability, compact die size, easy reconfigurability, insensitive to PVT

(process-voltage-temperature) variations, high linearity to both RF input as well as the gain control input, wide bandwidth and passband gain-flatness.

The following chapters discusses in detail about the various proposed reconfigurable design techniques that are analyzed mathematically and the findings are verified using on-wafer measurement results.

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Chapter 3. Variable gain amplifier (VGA) design

A well-known reconfigurability option of amplifier is the variable gain amplifiers (VGA) and was designed several decades before for incorporating them into AGC blocks [3.1], [3.2]. We can illustrate the VGA gain control by considering a typical amplifier topology as shown in Figure 3.1.

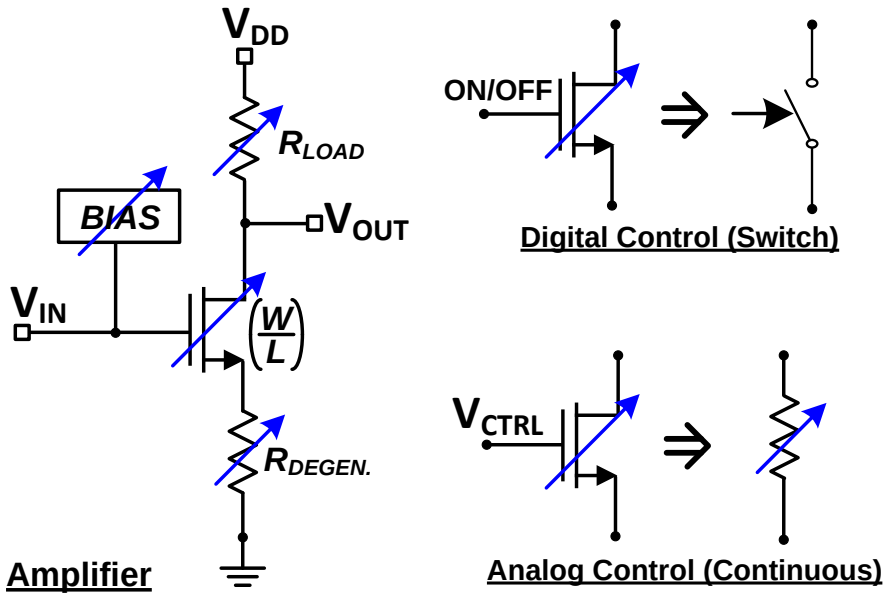


Figure 3.1 Typical a4mplifier topology to support variable gain.

The gain of such a typical amplifier is defined as,

$$A_V = \frac{g_m \cdot R_{LOAD}}{(1 + g_m \cdot R_{DEGEN})} \tag{3.1}$$

where, g_m is the transconductance, R_{LOAD} is the load resistance and R_{DEGEN} is the degeneration resistance. The transconductance is a function of the amplifying transistor size and the bias operating condition given as,

$$g_m = f\left(BIAS, (W/L)\right) \tag{3.2}$$

The gain control can be achieved by discretely (digitally variable gain amplifier (DVGA) or programmable gain amplifier (PGA)) or continuously varying (VGA) one or more of the amplifier design parameters using controllable switches that can select

or tune either the load resistance, biasing voltage, biasing current, degeneration resistance or the transistor size, that mainly influence the amplifier performance parameters. Similarly, along with the amplification control even variable attenuation control can be achieved in the same design.

The research work on VGA had started many decades ago [3.1] and is even today a topic of research interest. Based on the gain variation techniques we can classify them mainly as analog VGA and digital VGA (DVGA) or PGA. The analog VGA requires additional digital to analog converter (DAC) to acquire the gain control information from the digital baseband. Meanwhile the DVGA can be implemented either by switching between fixed gain stages or by switching discretely using binary weighted arrays of active (transistors or varactors) or passive (resistors or capacitors) circuit components. The former type of DVGA requires redundant die area due to circuit layout replication.

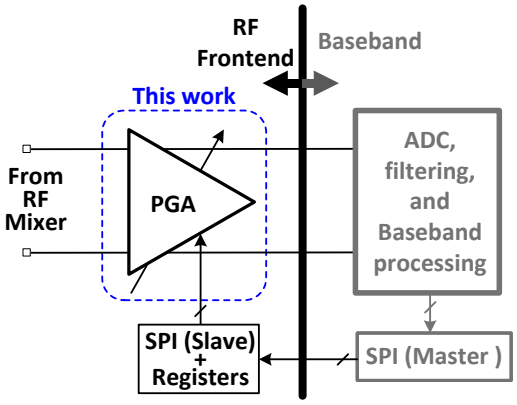


Figure 3.2 Practical application of PGA in a digital AGC.

Based on the desirable performance characteristics of a PGA, this chapter provides circuit analysis as well as the on-wafer measurement results taking into consideration the proposed PGA (consisting of DVGA core and post amplifier) design which has evolved from their previous version [A.4]. The PGA is mainly designed to interface the RF front-end with the baseband section. By using the digital AGC the

output power to the baseband section ADC is almost fixed to a predetermined power level to minimize the dynamic range requirement of the circuits at the baseband. This is illustrated in Figure 3.2.

dB-Linearity: Practically gain is expressed in decibel (dB) scale which has a logarithmic equation defined as,

$$A_V\big|_{dB} = 20 \cdot \log_{10}(A_V) = 20 \cdot \log_{10}\left[\frac{g_m \cdot R_{LOAD}}{(1 + g_m \cdot R_{DEGEN})}\right] \tag{3.3}$$

where, g_m is transconductance, R_{LOAD} is load resistance and R_{DEGEN} is degeneration resistance of a typical amplifier topology. By design, we can achieve $g_m \cdot R_{DEGEN} << 1$, R_{LOAD} as constant and g_m as an exponential function of a parameter such as "x", then the gain in dB ($A_V\big|_{dB}$) will become directly proportional to the exponential parameter (x). This property of gain control is called linear-in-decibel or dB-linearity.

Although the state-of-art VGA designed in CMOS process [3.2]-[3.4], [3.6]-[3.11], [3.13], [3.14] have a few advantages, such as the large dynamic range with low power consumption, they also possess the transconductance [3.8] with square law characteristics as,

$$g_{m,CMOS} = \frac{\delta I_D}{\delta V_{GS}} = \sqrt{2\,\beta\, I_D} \tag{3.4}$$

where, I_D is the bias drain current and V_{GS} is gate to source voltage, with β as MOS transistor parameter.

A CMOS based VGA design demonstrating a linear gain control variation without dB-linearity, yet achieving a large gain control range and wide bandwidth performance is proposed and analyzed in Chapter 4.

To achieve dB-linear gain variation, the CMOS DVGA requires additional pseudo-exponential conversion circuits. The DVGA is based on the bipolar devices

which have exponential transconductance characteristic based on the bias voltage (V_{be}) and linear transconductance characteristic based on the bias current (I_{CT}) as,

$$g_{m,BJT} = \frac{\delta I_{CT}}{\delta V_{be}} = \frac{I_0 \cdot e^{\left(\frac{V_{be}}{\eta \cdot V_T}\right)}}{\eta \cdot V_T} = \frac{I_{CT}}{\eta \cdot V_T} \tag{3.5}$$

The BJT bias voltage cannot be precisely controlled while the bias current using current mirrors can be controlled precisely. Hence we need an exponential current conversion to achieve a precise dB-linear gain control design by varying the bias current using digital switches.

The temperature compensation by using the biasing voltage prediction [3.7] and the stabilization of circuit parameters affected by temperature [3.8-3.10] results in increased circuit complexity. For low power applications, an uncomplicated design consuming low power becomes essential for a temperature insensitive VGA as described in the proposed DVGA of this Chapter.

3.1. Topology and analysis

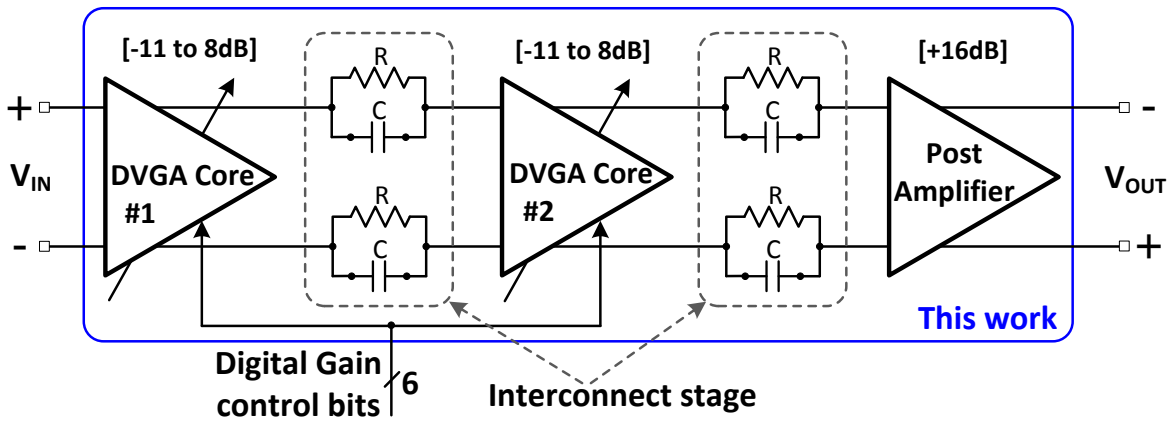


Figure 3.3 Block diagram of the proposed PGA.

The proposed PGA as shown in Figure 3.3 has a fully differential three stage cascaded topology with two identical DVGA cores, a post fixed gain amplifier stage and RC interconnect networks with a symmetric RF signal path. Each of the DVGA core is a 6-bit dB-linear low power digitally controlled -11 to +8 dB DVGA with on-chip dc offset cancellation (DCOC). The corresponding gain control bits B_5~B_0 of both the DVGA cores are shorted in pairs to provide an overall 6-bit programmable gain control for the PGA. The post amplifier design is based on the similar topology as DVGA core and provides a +16 dB fixed gain with DCOC capability.

The sequence of the PGA sub-blocks are arranged carefully taking into consideration the RF receiver frontend to the baseband interface requirement of providing a undistorted regulated power level over a large receiver input dynamic range. This application requirement based on the PGA linearity specification translates into a gain independent output 1-dB gain compression point (OP_{1dB}) over the entire bandwidth and gain control range with the gain difference reflected in the input 1-dB compression point (IP_{1dB}). For simplifying the circuit analysis we assume that the non-linearity contribution from the RC interconnect stages are negligible and are later verified by the measurement results discussed in the sub-section 3.4. The determination of the overall OP_{1dB} is not straightforward, since the characteristic curve depends on the amplifying devices that transits earlier from the linear operation into saturation region which is also reflected by the overall OP_{1dB} of the proposed PGA. Hence we can estimate the overall OP_{1dB} by converting back and forth between the input power and OP_{1dB} values with one stage at a time over the entire cascaded chain.

We analyze the circuit building blocks of the proposed PGA mainly the DVGA core, since the post amplifier performance is just a special case of fixed maximum gain

of the DVGA core. The mainly gain control of the overall PGA can be derived by the operating principle of the DVGA cores embedded in the cascaded PGA chain.

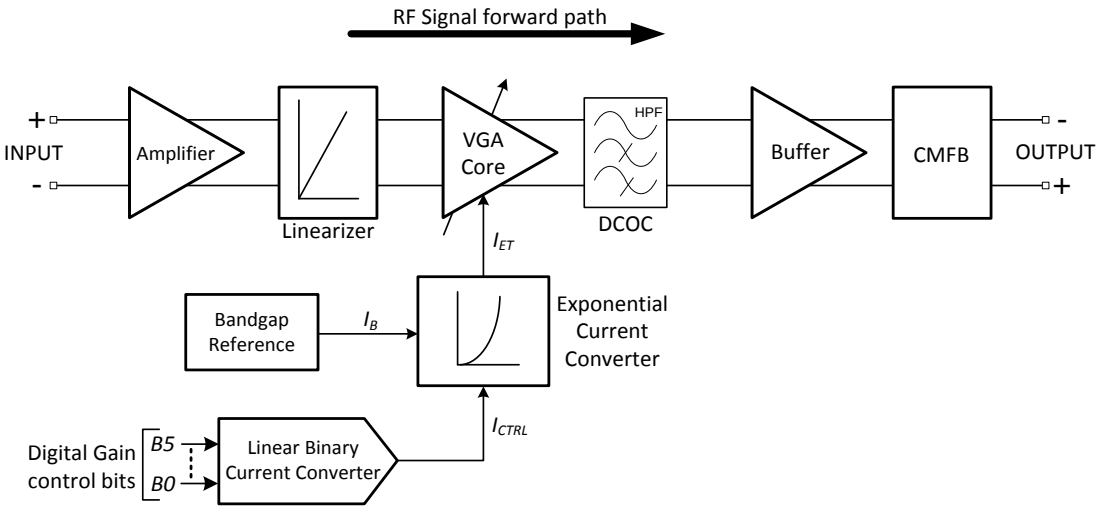


Figure 3.4 Block diagram of the proposed DVGA core.

The proposed DVGA core topology is a fully differential 3-stage cascaded amplifier as shown in Figure 3.4. The input fixed gain amplifier stage is a common-base (CB) amplifier that provides a stable low impedance input matching which is independent of gain control. Similarly, output buffer is a common-collector (CC) configuration and provides a low output impedance that is independent of gain control. The VGA core is a common-emitter (CE) stage responsible for providing the variable gain control which is reflected across the 3-stage design. The gain is controlled by a gain control current (I_{ET}) that in turn varies the amplifier transconductance as discussed in (3.5). Additionally, there are several blocks namely DC offset cancellation (DCOC), common mode feedback (CMFB), exponential current converter, linear binary current converter and the linearizer whose functionality are discussed in the following sub-sections.

3.2. Circuit analysis of the overall PGA

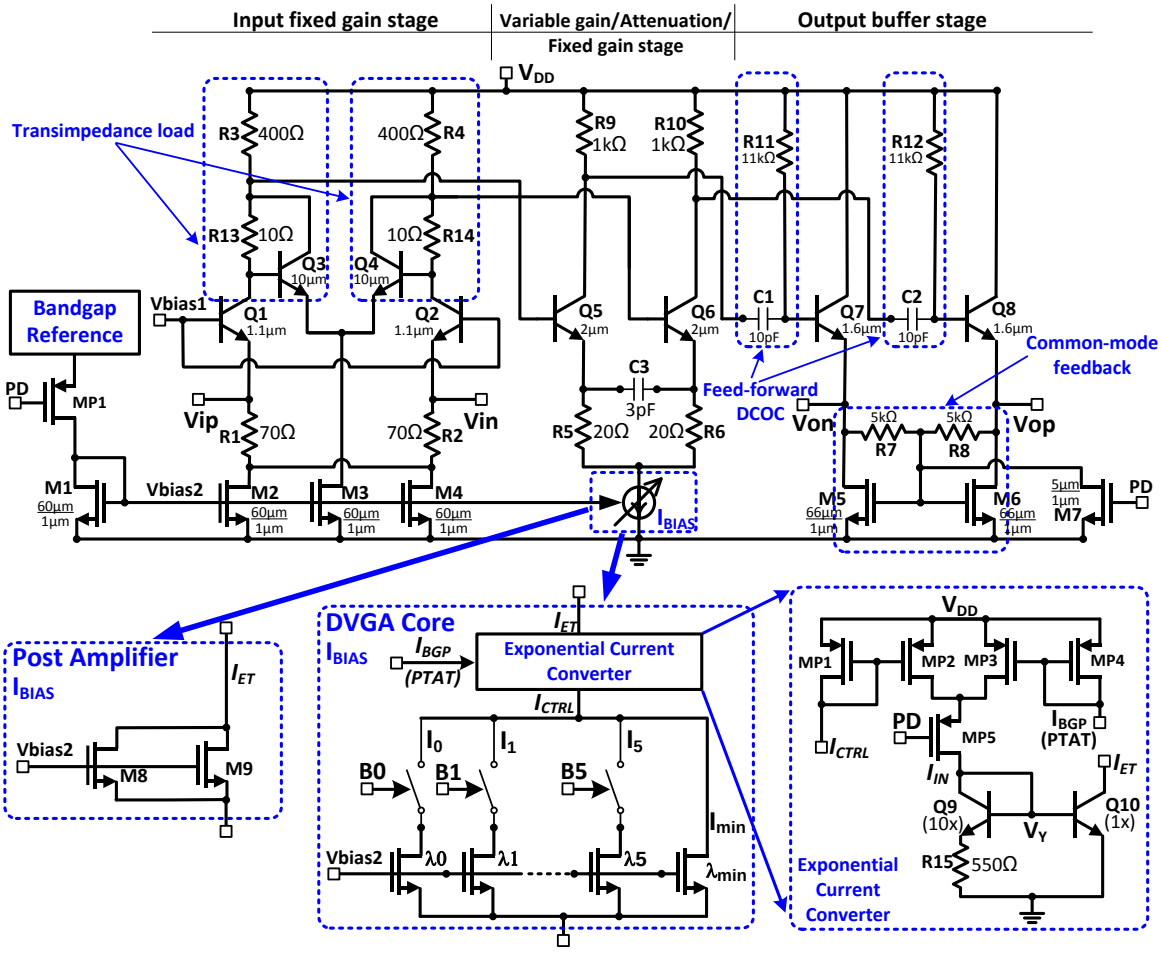


Figure 3.5 Circuit schematic of proposed PGA (DVGA core and post amplifier).

The circuit schematic of the proposed PGA design is given in Figure 3.5 along with the circuit for the DVGA core and post amplifier used in the final PGA design. The PGA stages are biased by using current mirrors from a bandgap reference. This design supports power down functionality by using a digital pin PD. The input stage has the transimpedance load used as the linearizer and the buffer stage has a feed-forward DCOC implemented as high pass filter (HPF) located at the input and CMFB at the output portion. The linear binary current converter acts as a current mode DAC which is implemented by using MOS switches and current mirrors obtained from the bandgap reference. The exponential current converter is the block that generates

exponential gain control current variation from the current derived from the linear binary current converter. The post amplifier has the same topology as the DVGA core except for the I_{BIAS} of the VGA core which has fixed current sink. This post amplifier is used only in the third DVGA design for gain bandwidth enhancement.

3.2.1. Small signal and frequency response

The small signal gain frequency response of the proposed DVGA core, is considered based on the half circuit AC equivalent of the CE variable gain stage (VGA core) as shown in Figure 3.6 (a) and the hybrid-π model in Figure 3.6 (b).

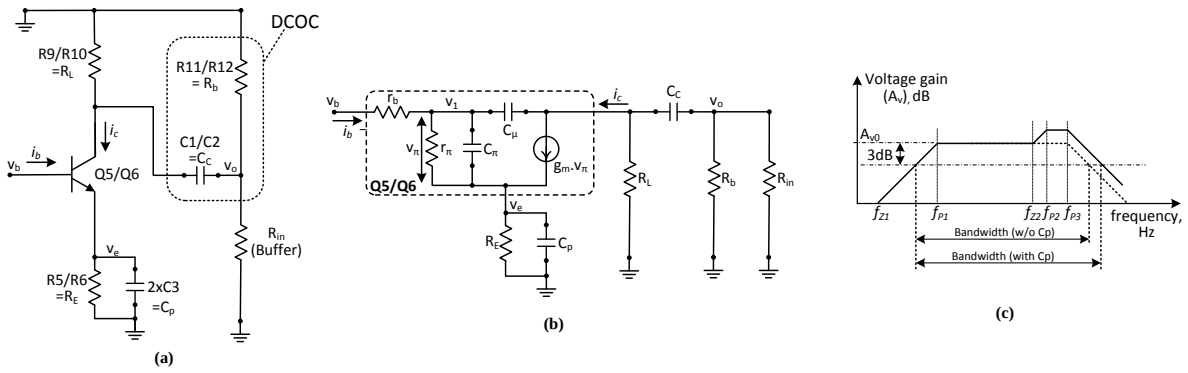


Figure 3.6 Half circuit of CE amplifier stage with DCOC (a) AC equivalent circuit (b) hybrid-π model (c) frequency response.

The gain variation contribution of the input CB (fixed gain amplifier) and the output CC (buffer) stages on the frequency response can be ignored. Since the peaking capacitor is for half circuit implementation is taken the value of $2xC3$ and R_{in} is the input resistance of the emitter follower buffer.

The frequency response shown in Figure 3.6 (c) is due to dominant pole and zero obtained from the DCOC and the gain-peaking capacitor, C_P. At low frequencies, the contribution of the transistor parasitic capacitors (C_π and C_μ) can be ignored to obtain the low frequency small signal gain,

$$A_v(s) = \frac{v_O}{v_b} = \frac{(-g_m)\cdot(R_b \parallel R_L \parallel R_{in})\cdot s\cdot\left(s + \dfrac{1}{R_E \cdot C_P}\right)}{s^2 + s\cdot\left[\dfrac{1}{C_P\cdot\{R_E \parallel (r_\pi + r_b)/(\beta+1)\}} + \dfrac{1}{C_C\cdot(R_b \parallel R_{in} + R_L)}\right] + \dfrac{1}{C_P\cdot R_E\cdot C_C\cdot(R_b \parallel R_{in} + R_L)}} \tag{3.6}$$

The poles and zeroes from (26) are,

$$f_{Z1} = \frac{\omega_{Z1}}{2\pi} = 0 \tag{3.7}$$

$$f_{P1} = \frac{1}{2\pi\cdot C_C\cdot\left[(R_b \parallel R_{in}) + R_L\right]} \approx 1.4\times10^6\ Hz \tag{3.8}$$

$$f_{Z2} = \frac{1}{2\pi\cdot R_E\cdot C_P} \approx 1.3\times10^9\ Hz \tag{3.9}$$

$$f_{P2} = \frac{1}{2\pi\cdot C_P\cdot\left[R_E \parallel (r_\pi + r_b)/(\beta+1)\right]} \approx 1.6\times10^9\ Hz \tag{3.10}$$

The zero f_{Z1} provides an initial launch with a gain slope = 6-dB/octave of the frequency response plot with a high pass filter response until the pole frequency f_{P1} is reached. Then on, the mid-band flat gain response with gain A_{v0} proceeds towards the high frequency pole (along the dashed line) at f_{P3}. The parasitic capacitors (C_π and C_μ) of the transistor pair Q5/Q6 and the interconnects then decreases the gain at high frequencies from f_{P3} onwards given in (3.11).

$$f_{P3} = \frac{1}{2\pi \cdot \left[C_\pi + C_\mu \cdot \left\{1 + g_m \cdot \left(R_b \parallel R_L \parallel R_{in}\right)\right\}\right] \cdot \left(r_\pi \parallel r_b\right)} \approx 1.8 \times 10^9\ Hz \qquad (3.11)$$

Due to peaking capacitor C_P included in the design, an additional zero at f_{Z2} is introduced which initiates the peaking and the parasitic capacitors of the transistor pair Q5/Q6 along with the interconnect losses then drops the gain from f_{P3} (3.11) onwards. The contribution of the second pole at f_{P2} depends on the value of the parasitics of the transistors and eventually rolls the gain downwards into the stop band. As a result of incorporating the peaking capacitor C_P in the design an increase in the 3-dB bandwidth of the proposed DVGA is observed as shown in Figure 3.6 (c) at the upper cutoff frequency. However the lower cutoff frequency of the DVGA is predominantly determined by the pole at f_{P1}, which mainly depends on the DCOC components and the input resistance of the output buffer, R_{in} which is described in the following section 3.2.6. The first pole at f_{P1} can be moved to a lower frequency by either increasing capacitance C_C at the cost of increased die area or by increasing R_b (limited by R_{in}) resistance that may affect the biasing of the output buffer or by increasing load resistance R_L which by (3.11) may reduce the upper cutoff frequency, f_{P3} of the DVGA.

3.2.2. Gain control linearity (dB-Linearity) of DVGA core

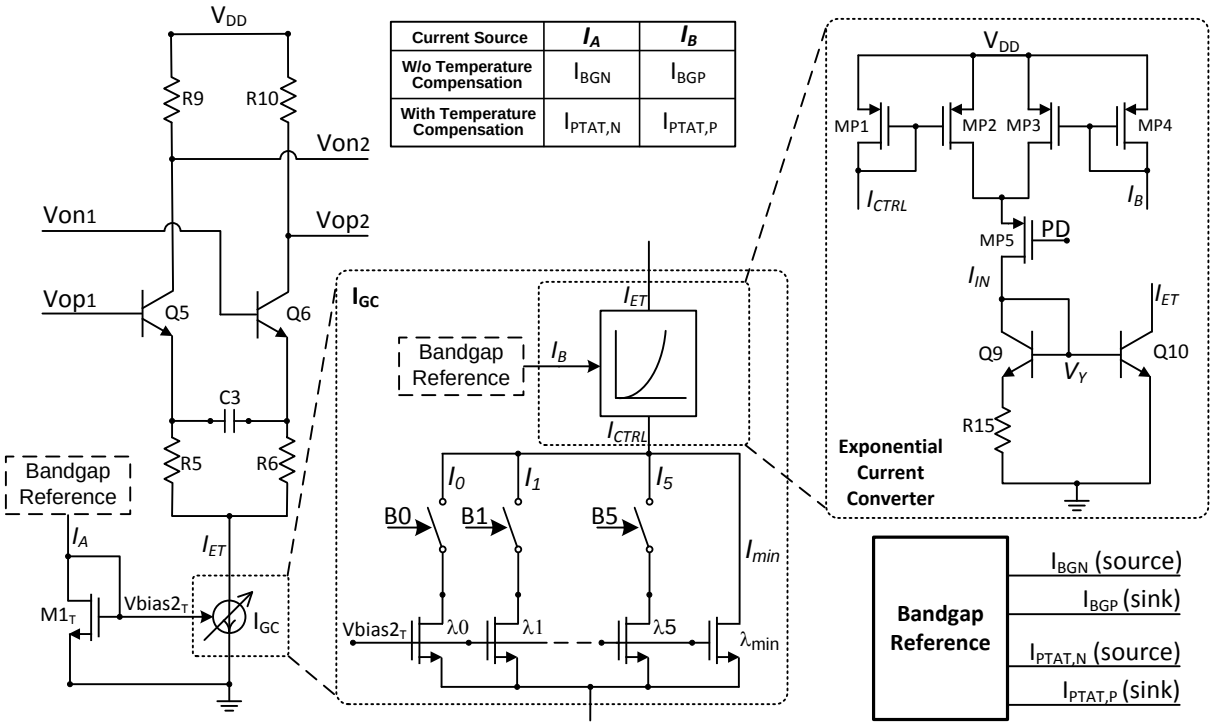


Figure 3.7 VGA core dB-linear gain control without and with temperature compensation.

The operating principle of the VGA core is determined by the small signal gain characteristics discussed in the previous sub-section 3.2.1 and is obtained from the variable transconductance (g_m) of amplifier by controlling the biasing current (I_{ET}).

For enhancing the input dynamic range of the DVGA core by compensating for the signal strength variations caused by the wireless/wired communication channel, a linear-in-decibel (dB-linearity) gain control is desirable. Additionally, such dB-linear gain control improves the settling time of the AGC as explained in [2.2]. The proposed DVGA core claims to achieve dB-linearity by using simple circuit design improvement over the initial linear gain control. The relation between the VGA core's gain and the gain control biasing current is depicted in (3.12) and (3.13) as,

$$A_v = g_{m5,6} \cdot R_{9,10} \tag{3.12}$$

where, $R_{9,10}$ is the VGA core's load resistance and $g_{m5,6}$ is the transconductance of the amplifying transistor pair Q5/Q6 given as,

$$g_{m5,6} = \frac{\delta I_{CT}}{\delta V_{be}} = \frac{\alpha}{\eta \cdot V_T} \cdot \left[\sum_{n=0}^{5} B_n \cdot I_n \cdot 2^n + I_{\min} \right] \tag{3.13}$$

where the common base current amplification factor defined as α, the ideality factor as η and the thermal voltage V_T are model parameters indicated for the transistor pair Q5/Q6, I_n (n = 0 to 5) are the constant current coefficients of the estimated linear gain function, B_n (n = 0 to 5) are the digital bit coded value (either '1' or '0') received from the digital baseband SPI control as shown in Fig 3.2 and $I_{\min}$ is the DC current corresponding to minimum gain when all the digital control bits B_n are reset (= '0').

The transconductance $g_{m5,6}$ from (3.13) implies that a linear variation of gain associated with the 6-bit digital gain control word (B_5~B_0) can be verified in DVGA core design 1. Since the variable emitter biasing current I_{ET} (shown in Figure 3.7) controls the transconductance $g_{m5,6}$ which can be derived from the bandgap reference as V_{bias2}, the gain (A_v) also becomes insensitive to the temperature variations.

The VGA core's gain from (3.12) in decibel (dB) is given as,

$$A_v, dB = 20 \cdot \log_{10}(g_{m5,6} \cdot R_{9,10}) \tag{3.14}$$

From (3.14), the VGA core gain A_v, dB is a logarithmic function of the gain control current I_{ET} though the $g_{m5,6}$. Although the gain control block in [A.4] has a good temperature insensitive gain variation as shown in Figure 3.8, it does not possess the dB-linearity characteristics. In order to increase the DVGA core's dynamic range and to provide a minimum dB-linear error, the above mentioned gain control block is enhanced by including an exponential current converter block based on HBT as shown

in Figure 3.7, and the circuit performing the exponential current conversion is considered as the proposed dB-linearizer, to convert the linear current I_{IN} into exponential gain control current I_{ET}.

The proposed dB-linearizer block comprises of bipolar transistor pair (Q9/Q10) connected as current mirror. The voltage drop across R_{15} (by neglecting I_{BT}) is given as,

$$\Delta V_{BE} = I_{IN} \cdot R_{15} = V_{BE,10} - V_{BE,9} \tag{3.15}$$

The exponential gain control current obtained as I_{ET} is deduced as,

$$I_{ET} = \left(\frac{I_{IN}}{10}\right) \cdot e^{\left(\frac{I_{IN} \cdot R_{15}}{V_T}\right)} \tag{3.16}$$

By using equations (3.13) in (3.14) with $\eta \approx 1$ and $\alpha \approx 1$, VGA gain is given as,

$$A_v, dB = 20 \cdot \log_{10}\left(\frac{I_{ET}}{V_T} \cdot R_{9,10}\right) \tag{3.17}$$

By using (3.16) in (3.17), we get,

$$A_v, dB = K_1 \cdot I_{IN} + 20 \cdot \log_{10}(K_2 \cdot I_{IN}) \tag{3.18}$$

where, $K_1 = \left(\frac{20 \cdot R_{15} \cdot \log_{10} e}{V_T}\right)$ and $K_2 = \left(\frac{R_{9,10}}{10 \cdot V_T}\right)$.

Both the above mentioned terms in (3.18) are functions of I_{IN} and hence differentiating (3.18) by I_{IN} we get,

$$\frac{\delta A_v, dB}{\delta I_{IN}} = K_1 + \frac{20}{I_{IN} \cdot \log_e 10} \tag{3.19}$$

From (3.19), the first term *K1* indicating that dB-linearity is the dominating term for the DVGA core's gain control and the contribution of the second term becomes trivial. This dB-linear gain control characteristics is further emphasized by the measurement results discussed in the sub-section 3.2.6.

This additional circuit shown in Figure 3.7, as the exponential current converter, has very few circuit components that significantly improves the DVGA core's dB-linearity along with consuming a low DC power and a small die area. Since the exponential current conversion is accomplished by just using a bipolar junction transistor pair with a resistance, the inherent temperature sensitivity of the PN junction potential appears and this needs for a temperature compensation as illustrated in the following sub-section 3.2.3.

3.2.3. Temperature compensation

The DVGA core (without dB-linearity) has the gain control biasing current I_{ET} derived directly from the bandgap reference (BGR) and hence the DVGA core's gain is less temperature sensitive as shown by the simulation plot in Figure 3.8.

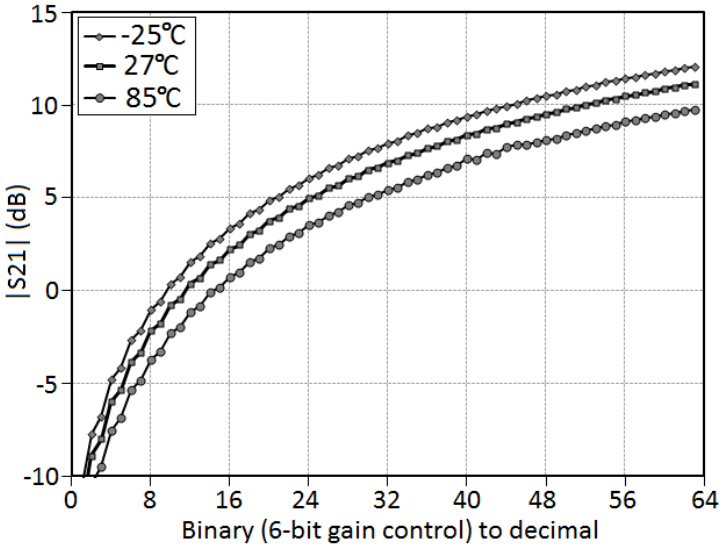


Figure 3.8 Simulated gain characteristics against temperature for DVGA without dB-Linearizer.

Unlike the proposed dB-linear DVGA core as shown in Figure 3.7, the temperature independent currents I_{CTRL} and I_{BGP} are derived directly from the bandgap

reference, due to the temperature dependency of the bipolar junction devices discussed previously in the exponential current converter, the gain control biasing current I_{ET} eventually becomes temperature sensitive. The low resistivity unsalicided polysilicon resistor from the process design kit (PDK) that is used in this proposed design has very small temperature coefficient [1.4], and hence resistance sensitivity against temperature (T) can be neglected in this temperature analysis as,

$$\frac{\delta R_{15}}{\delta T} \approx \frac{\delta R_{9,10}}{\delta T} \approx 0 \tag{3.20}$$

From (3.16), temperature (T) variation resulting in variation of the biasing current is given as,

$$\frac{\delta I_{ET}}{\delta T} = \left(\frac{1}{10}\right) \cdot e^{\left(\frac{I_{IN} \cdot R_{15}}{V_T}\right)} \cdot \frac{\delta I_{IN}}{\delta T} + \left(\frac{I_{IN} \cdot R_{15}}{10 \cdot V_T^2}\right) \cdot e^{\left(\frac{I_{IN} \cdot R_{15}}{V_T}\right)} \cdot \left(V_T \frac{\delta I_{IN}}{\delta T} - I_{IN} \frac{k}{q}\right) \tag{3.21}$$

Hence we can deduce that the most temperature sensitive block of the proposed DVGA core is the exponential current conversion and care must be ensured to nullify the temperature sensitivity of this block without any further complication in the design. The condition for the temperature insensitivity is given as,

$$\frac{\delta I_{ET}}{\delta T} \approx 0 \tag{3.22}$$

As an assumption, if the first term of (3.21) is insignificant, then (3.22) becomes,

$$\left(\frac{I_{IN} \cdot R_{15}}{10 \cdot V_T^2}\right) \cdot e^{\left(\frac{I_{IN} \cdot R_{15}}{V_T}\right)} \cdot \left(V_T \frac{\delta I_{IN}}{\delta T} - I_{IN} \frac{k}{q}\right) \approx 0 \tag{3.23}$$

Hence reduces to,

$$\frac{\delta I_{IN}}{\delta T} = \frac{I_{IN}}{T} \tag{3.24}$$

From (3.24), for achieving temperature compensation of the gain control current I_{ET} it is obvious that the current I_{IN} has to be derived/mirrored from a proportional to

absolute temperature (PTAT) current source. By design of the bandgap reference there are temperature independent constant currents obtained as $I_{BG,N}$ and $I_{BG,P}$ of 50 µA as shown in Figure 3.7. For the PTAT, currents $I_{PTAT,N}$ and $I_{PTAT,P}$ that are also obtained from the same bandgap reference have a constant temperature gradient for the current which is equal to $\left(\frac{50\mu A}{274.15^{O}K}\right) = 0.182\ \mu A/K$.

By assigning the designed values into the first term of (3.21) along with V_T = 26 mV (at room temperature of 27^{O}C) and a $\frac{\delta I_{IN}}{\delta T}$ = 0.182 µA/K we get,

$$\left(\frac{1}{10}\right)\cdot e^{\left(\frac{I_{IN}\cdot R_{15}}{V_T}\right)}\cdot\frac{\delta I_{IN}}{\delta T}\approx 10^{-8} \tag{3.25}$$

From (3.25), we can easily verify that the assumption made previously in (3.21) to obtain (3.23) is valid. Hence temperature sensitivity of the proposed dB-linearizer can be mitigated by extracting the gain control current from the PTAT current source and feeding to the exponential current converter at specific nodes as shown in the Figure 3.7.

By extending the analysis further to determine temperature effect on overall gain of the proposed DVGA, using (3.16) and (3.17),

$$\frac{\delta A_v, dB}{\delta T} = \frac{20\cdot V_T}{I_{IN}}\cdot\left(1+\frac{I_{IN}\cdot R_{15}}{V_T\cdot\log_e 10}\right)\cdot\frac{\delta}{\delta T}\left(\frac{I_{IN}}{V_T}\right) \tag{3.26}$$

The DVGA core gain that is temperature compensated is obtained from (3.26) as,

$$\frac{\delta A_v, dB}{\delta T} = 0 \tag{3.27}$$

Using (3.27), we get,

$$\frac{\delta}{\delta T}\left(\frac{I_{IN}}{V_T}\right) = \frac{1}{V_T^2}\cdot\left(V_T\cdot\frac{\delta I_{IN}}{\delta T} - I_{IN}\cdot\frac{\delta V_T}{\delta T}\right) = 0 \tag{3.28}$$

As discussed, by using I_{IN} current from the PTAT source of the bandgap reference ($I_{PTAT,N}$ and $I_{PTAT,P}$), with (3.24) substituted in (3.28), a temperature independent dB-linear gain control is accomplished and the condition in (3.27) is also satisfied. If we consider the scenario that the current I_{IN} is derived from the bandgap reference constant currents (I_{BGN} and I_{BGP}) with $\frac{\delta I_{IN}}{\delta T} = 0$, then (3.26) reduces to,

$$\frac{\delta A_v, dB}{\delta T} = 20 \cdot \left(1 + \frac{I_{IN} \cdot R_{15}}{V_T \cdot \log_e 10}\right) \cdot \left(-\frac{1}{T}\right) \tag{3.29}$$

From (3.29), the temperature gradient of the gain is a negative term which indicates that the DVGA gain decreases as the temperature increases. This is also depicted by the simulation plot of gain with different operating temperatures for the dB-linear DVGA core (see Figure 3.7) without temperature compensation as shown in Figure 3.9.

The improved version design 2 of the gain control block with a linear to exponential current converter block using PTAT currents from the bandgap eventually improves the overall dB-linearity and is also insensitive to temperature variations. As shown in Figure 3.9, the temperature compensation of the proposed exponential current converter can be accomplished by using the PTAT currents ($I_{PTAT,N}$ and $I_{PTAT,P}$) of the bandgap reference. The rest of the amplifier is already temperature insensitive and is biased from the constant temperature insensitive currents (I_{BGN} and I_{BGP}) obtained from the bandgap reference. From Figure 3.9, due to the small current (I_{CTRL}) at the minimum DVGA gain, the huge portion of the gain control current (I_{ET}) is predominantly from PTAT source ($I_{PTAT,P}$) and hence nullifies the temperature sensitivity of the DVGA core gain much better than at maximum gain setting.

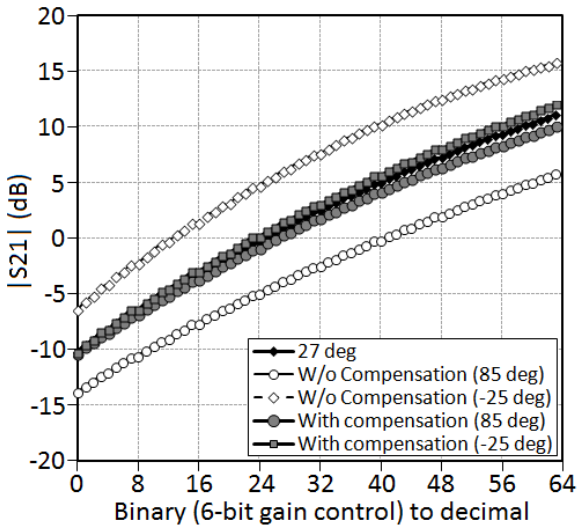


Figure 3.9 Simulated gain characteristics against temperature for DVGA using dB-Linearizer with/without temperature compensation.

From this investigation we can deduce that the exponential current converter along with the PTAT currents, achieves a temperature compensated dB-linear gain control in the proposed DVGA core that occupies small die area with low DC power. By this analysis we can safely conclude that both the DVGA core and the post amplifier used in the proposed PGA makes the overall design temperature compensated from -25 ^{O}C to +85^{O}C.

3.2.4. DC Offset cancellation

The DCOC of the proposed PGA design (both DVGA core and the post amplifier) can be considered as the AC coupled low-loss high pass filter (HPF). Unlike for the capacitor-only AC coupling that requires large capacitors between each stage to achieve cutoff frequency closer to DC, the DCOC in the proposed PGA alleviates the need for a large capacitor value by choosing a large HPF resistor value to achieve the lower cutoff frequency even with smaller capacitor. The resistor of the HPF is in parallel to the input impedance of the CC buffer stage which can be large value and

hence the desired cutoff frequency is determined by a parallel resistance combination. The large HPF resistor value, other than minimizing the capacitance, also provides biasing for the CC buffer stage. The design of the HPF in the DCOC is explained in section 3.2.5 along with the CMFB circuit design.

Inherently, the DCOC design is simplified for the bipolar differential pairs (unlike for the CMOS devices) and hence the proposed 3-stage design is based on only one DCOC stage between the final two DVGA stages. This cancels the DC offsets generated from the differential pairs from propagating further, unlike for the CMOS multi-stage VGAs wherein the DCOC is applied at each stage to avoid saturation of any output stages. The DCOC in the proposed DVGA can suppress most of the DC offsets generated or propagated along the signal path with a low cutoff frequency and a large gain roll off is achieved. Although the DCOC occupies nearly 50% die area of the proposed DVGA core, the overall DVGA core area is only 160 μm x 300 μm.

3.2.5. Buffer with Common Mode Feedback (CMFB)

The output differential buffer stage of the proposed DCOC PGA design incorporates the CMFB that enforces a fixed value for the output common mode voltage. The proposed PGA (both the DVGA core and the post amplifier) ascertains both the input and output common mode voltages to predetermined values by using the input fixed gain amplifier and the output CMFB respectively, ensuring that the PGA biasing is stable and gain-independent.

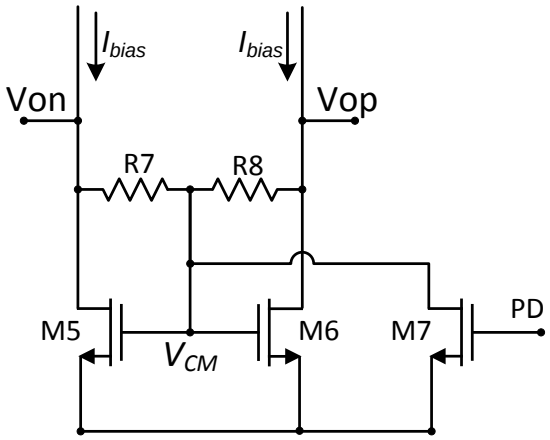


Figure 3.10 Common mode feedback (CMFB).

The CMFB is self-regulating based on the voltage V_{CM} that is set by the emitter follower bias current I_{bias}as shown in Figure 3.10.

The gate currents of the transistors M5 and M6 and eventually the voltage drop across resistors R7 and R8 are negligible. This results in a back-to-back diode-connected transistor configuration that normally operates in the saturation region and sets the DC voltage to V_{CM} by averaging the output voltages V_{on} and V_{op} as,

$$V_{CM} = \sqrt{\frac{2 \cdot I_{bias}}{\beta_N}} + V_{THN} \tag{3.30}$$

where, $\beta_N = \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_N$ with μ_n, C_{ox}, $\left(\frac{W}{L}\right)_N$ and V_{THN} are electron mobility, gate oxide capacitance per unit area, aspect ratio, and the threshold voltage of the transistors M5/M6, respectively.

This CMFB additionally provides a wideband 50 Ω output resistive matching that is independent of resistance value R7/R8 and is equivalent to a parallel resistance combination of the reciprocal of the M5 and M6 NMOS transconductance as,

$$Z_{OUT} = \frac{1}{g_{mN5}} \| \frac{1}{g_{mN6}} \tag{3.31}$$

where, g_{mN5} and g_{mN6} are transconductance of the M5 and M6 transistors, respectively.

The transistor M7 is introduced to switch OFF M5 and M6 active loads of the CC buffer during the *power down* mode.

3.2.6. Design procedure of the DCOC and CMFB of the proposed PGA design

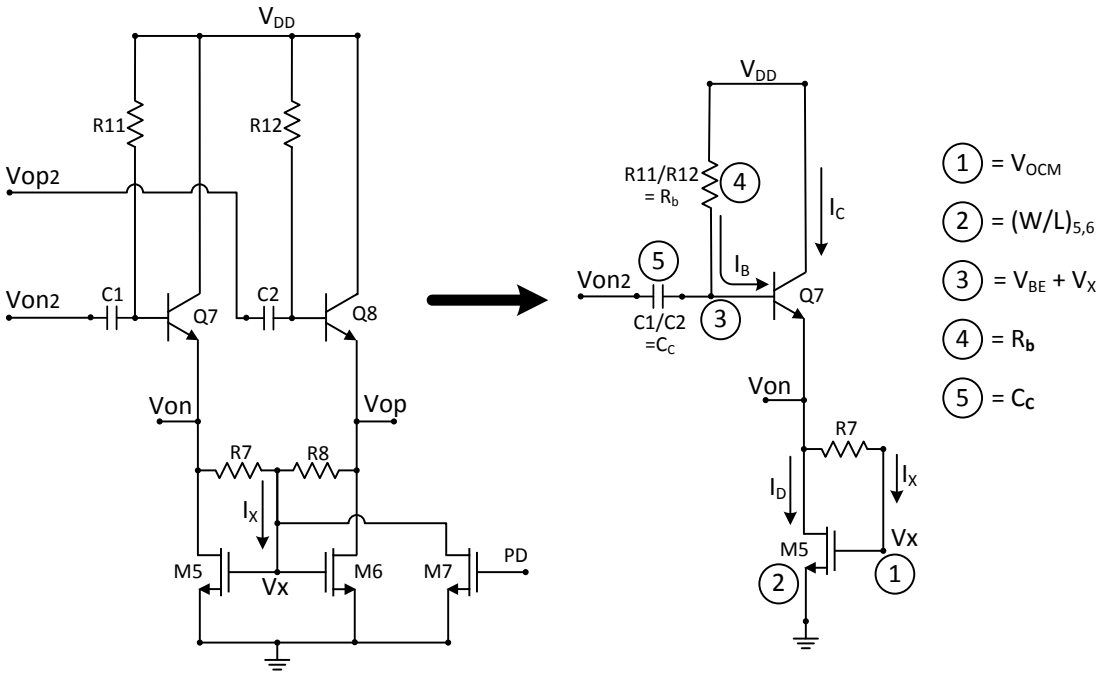


Figure 3.11 Output Buffer stage with DC offset canceller (DCOC) and CMFB.

Figure 3.11 shows the circuit schematic and the half circuit equivalent of the output buffer with the DCOC and CMFB.

Step 1: Determining transistor size for M5/M6

A large common mode voltage (V_{OCM}) is usually avoided that may result in the shut off the buffer transistor pair Q7/Q8. Since the gate current I_X shown in Figure 3.11 is trivial, the voltage drop across the resistors R7/R8 is negligible and the V_{OCM} voltage becomes the gate-source voltage V_X of the transistors M5/M6. This results in a back-to-back diode-connected transistor M5/M6 structure which operate in the

saturation region. By knowing the CC buffer's optimum operating currents I_B and I_C for the transistor pair Q7/Q8, the aspect ratio for M5/M6 can be obtained as,

$$\left(\frac{W}{L}\right)_{5,6} = \frac{2 \cdot I_D}{K_{Pn} \cdot (V_X - V_{THN})^2} \approx \frac{66\mu m}{1\mu m} \tag{3.32}$$

Step 2: Determine the resistance for output buffer biasing used in the DCOC

The base voltage for biasing the transistor pair Q7/Q8, by neglecting the voltage drop across resistors R7/R8, is $V_{BE} + V_X$. Resistors R11/R12 are used for biasing the output differential buffer and it forms a part of the DCOC HPF design.

$$R_b = \frac{V_{DD} - (V_{BE} + V_X)}{I_B} \approx 11\,k\Omega \tag{3.33}$$

Step 3: Determining the capacitance of the DCOC HPF design

The effective parallel resistance between R_b and the input resistance (R_{in}) of the output CC buffer along with the AC coupling C_C capacitor forms the DCOC HPF design. The HPF cutoff frequency is given by f_{P1} as discussed in the sub-section 3.2.1. For practical design consideration based on the criteria of $(R_L << R_b << R_{in})$, we can neglect the resistances R_{in} and R_L, and the DCOC capacitor value is obtained as,

$$C_C \cong \frac{1}{2\pi \cdot f_{P1} \cdot (R_b)} \approx 10\,pF \tag{3.34}$$

3.2.7. Large signal (Linearizer) and P1dB analysis

The input stage of the proposed DVGA core as well the post amplifier is shown in Figure 3.12 is similar to the previous DVGA design from the same authors [A.4] except for the inclusion of the resistors R13/R14. With this, the input stage transforms into a common base (CB) amplifier with a transimpedance load circuit [3.45] and the resistors R13/R14 as the shunt feedback resistors for the transistor pair Q3/Q4. As the input CB stage does not possess the Miller effect that contributes to a pole frequency due to this stage along with the transimpedance load to be moved farther away and the PGA bandwidth is unaffected. This newly introduced transimpedance load apparently consumes low DC power and acts as a pre-distortion linearizer in improving the overall PGA linearity significantly.

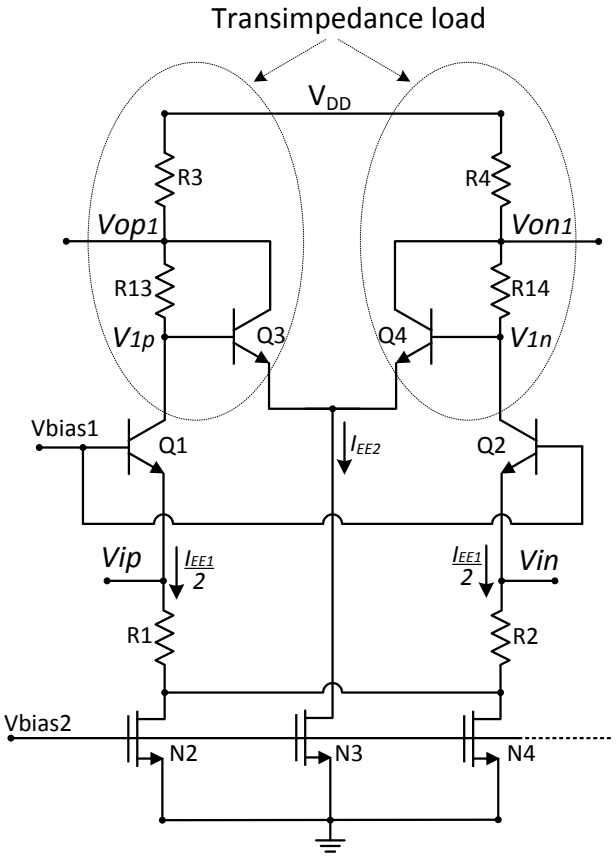


Figure 3.12 Input stage fixed gain amplifier.

The improvement in the PGA linearity from each of the DVGA core and the post amplifier are due to this transimpedance load circuit which can be justified by understanding the large signal analysis as described in [A.4] along with the addition of shunt resistors R13/R14. The output signal distortion based on the non-linearity mainly arises due to the altering of the DC bias conditions of the PGA stages by large a voltage signal swing at the input. For simplifying the expressions used in the large signal analysis, we assume that the resistors are named as $R13 = R14 = R_f$ and $R3 = R4 = R_L$. The maximum voltage signal swing at the differential input of the transimpedance load circuit is the DC voltage difference [3.38] given by,

$$V_{1p} - V_{1n} \cong \left(R_f + R_L\right) \cdot I_{EE1} \cdot \tanh\left(\frac{V_{ip} - V_{in}}{2 \cdot V_T}\right) - \left(\frac{R_f + R_L}{\beta} + R_L\right) \cdot I_{EE2} \cdot \tanh\left(\frac{V_{1p} - V_{1n}}{2 \cdot V_T}\right) \qquad (3.35)$$

$$V_{op1} - V_{on1} = R_L \cdot I_{EE1} \cdot \tanh\left(\frac{V_{ip} - V_{in}}{2 \cdot V_T}\right) - \left(\frac{R_L}{\beta}\right) \cdot I_{EE2} \cdot \tanh\left(\frac{V_{1p} - V_{1n}}{2 \cdot V_T}\right) \qquad (3.36)$$

From (3.35), we find that the voltage difference $V_{1p} - V_{1n}$ is obtained based on the input voltage difference $V_{ip} - V_{in}$ and by an iterative subtraction. This difference voltage $V_{1p} - V_{1n}$ gradually converges and the final difference output voltage is computed as shown in (3.36). The subtraction (voltage difference) terms based on $V_{1p} - V_{1n}$ in (3.35) and also in (3.36) are originated due to the negative feedback offered by the transimpedance load stage and hence provides a DC voltage regulation. Therefore the transimpedance load stage performs the pre-distortion linearization by stabilizing the bias votlages of the PVGA transistor pairs. The contribution of the transimpedance load circuit on the linearity and also the stability is determined by the current I_{EE2} controlled by the M3 current sink. By introducing the shunt feedback resistors R_f, without affecting overall DC power consumption, an additional improvement of the DVGA linearity is achieved over [A.4] for the whole gain range and it is evident from

experimental results shown in Table 3.1 for the DVGA core. In addition to the linearity improvement discussed in [A.4], the resistors R13/R14 introduced as a part of the transimpedance load circuit contributes further to the improvement of the linearity in the proposed PGA stages. This can be explained using a simulation plot shown in Figure 3.13 by parameter sweeping of the resistance R13/R14 values from 0 Ω to 10 Ω for maximum gain state. We observe that, as the resistor value increases, there is a decrease in gain and a corresponding increase in the IP_{1dB} with the OP_{1dB} unchanged. This characteristics is similar to the linearity improvement illustrated in [A.4] and the linearity is further improved without any additional power consumption and significant die area.

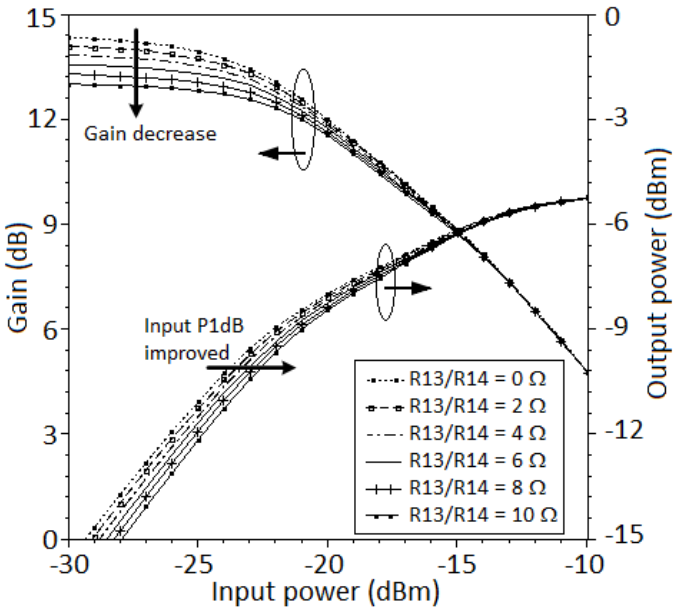


Figure 3.13 Simulated DVGA linearity with varying R13/R14 resistors of the Transimpedance load linearizer at 1 GHz frequency.

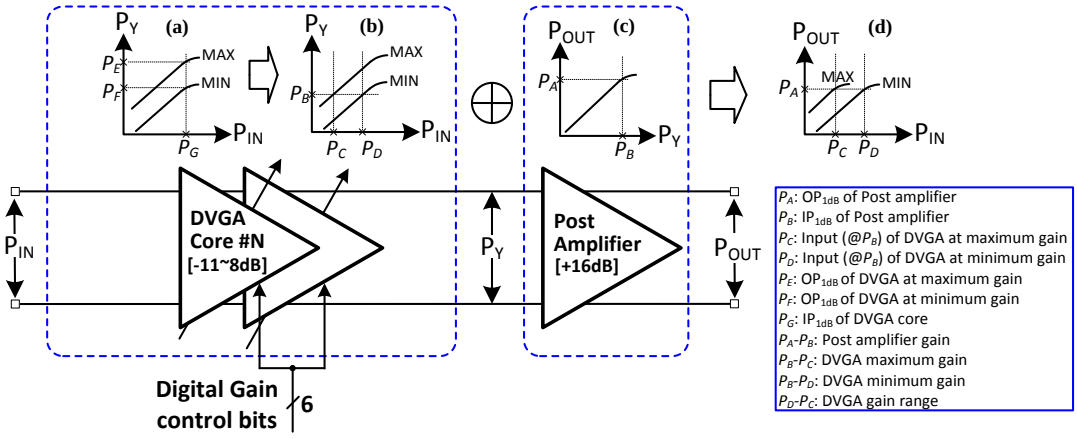


Figure 3.14 Linearity analysis of proposed PGA for receiver frontend to baseband interface.

The large signal analysis of the overall proposed PGA topology can be illustrated from Figure 3.14 by neglecting the interstage network. The DVGA core has a nearly gain-independent measured IP_{1dB} (~ -12.5 to -11 dBm) for the entire DVGA gain range denoted as P_G in Figure 3.14 (a) which is determined by the CC buffer stage and the DVGA core gain difference is mainly reflected in its OP_{1dB} as P_E and P_F (shown in Figure 3.14 (a)). We consider the IP_{1dB} and OP_{1dB} points of the post amplifier as P_B and P_A respectively for illustration purpose. For the proposed PGA to be used in the RF receiver frontend application, the post amplifier design has to ensure that $P_B \leq P_F$. So that the overall PGA's OP_{1dB} becomes gain independent and it will be approximated to OP_{1dB} of the post amplifier (P_A) as shown in Figure 3.14 (d). This will eventually transform and then limit the cascaded DVGA characteristics from the Figure 3.14 (a) to Figure 3.14 (b).

We perform the large signal analysis of the proposed PGA under both the maximum and minimum gain conditions as follows,

At PGA maximum gain (B5~B0: 111111'b) condition:

From the post amplifier transfer characteristics as shown in Figure 3.14 (c), the OP_{1dB} of the overall PGA design is determined by the OP_{1dB} of the fixed gain post

amplifier, P_A with its IP_{1dB} value, the P_B value determining the maximum output power level that the cascaded DVGA core can reach before the post amplifier goes into saturation region. By traversing back in the PGA cascaded chain, the characteristics of the cascaded DVGA core together shown in Figure 3.14 (b) is limited by P_B with the overall PGA's IP_{1dB} set to P_C shown in Figure 3.14 (d).

Hence by ensuring $P_B \leq P_F$ the overall PGA's non-linearity within PGA gain control range is reached mainly due to the early saturation of the post amplifier while the DVGA core stages are still operating linearly.

At PGA minimum gain (B5~B0: 000000'b) condition:

From the cascaded DVGA core's power performance transfer characteristics shown in Figure 3.14 (a) and Figure 3.14 (b), by ensuring that $P_B \leq P_F$, eventually the overall PGA's OP_{1dB} is determined by the OP_{1dB} of the fixed gain post amplifier (P_A) as discussed in the previous condition and the overall PGA's IP_{1dB} set to P_D as shown in Figure 3.14 (d).

The conventional cascaded amplifier stages [3.45] provide desired high gain as shown in (3.37), however the bandwidth likewise shrinks as the number of cascaded stages increases given by (3.38).

$$|A_T| = \frac{|A_0|^n}{\left[\sqrt{1+\left(\omega/\omega_0\right)^2}\right]^n} \tag{3.37}$$

$$\omega_T = \omega_0 \cdot \sqrt{2^{1/n} - 1} \tag{3.38}$$

where, A_T and ω_T are gain and bandwidth of the overall cascaded amplifier consisting of n identical stages with A_0 and ω_0 as the gain and bandwidth, respectively.

3.2.8. GBW extension of the proposed PGA using the interconnect stage

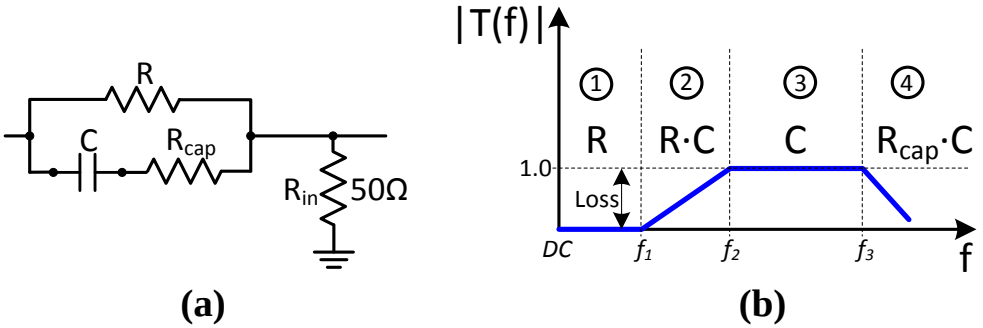


Figure 3.15 Interconnect stage (a) circuit (b) frequency response.

The matching network is a crucial circuit in the amplifier design that provides a good low loss signal path for cascading any two adjacent stages. In this proposed PGA design the interstage parallel RC network shown in Figure 3.15 (a) is used to interface between the DVGA core stages as well as with the post amplifier stage as shown in the PGA block diagram, Figure 3.3. The circuit operation of the interconnect network can be understood by following the sequence numbered in Figure 3.15 (b):

1) At very low frequencies close to dc, the shunt capacitor C acts as open circuit and hence the interstage network operates as a voltage divider leading to RF signal loss as shown in Figure 3.15 (b).
2) As the operating frequency increases the effective impedance offered by the capacitor decreases and a shunt RC network introduces a zero at f_1 frequency.
3) With further increase in operating frequency, the impedance of the capacitor C drops below the resistance R and depending on the capacitance C the network acts as a short circuit with low signal loss beyond f_2 frequency.
4) From f_3 frequency onwards the high frequency parasitic resistance R_{cap} mainly due to the metal traces' skin effect appears and results in a high frequency pole.

This resulting frequency response as shown in Figure 3.15 (b) is similar to a gain peaking characteristics and the interstage network transfer function is given as,

$$T(\omega) = \frac{R_{in} \cdot \left[1 + j\omega C \cdot \left(R + R_{cap}\right)\right]}{R_{in} \cdot \left[1 + j\omega C \cdot \left(R + R_{cap}\right)\right] + R \cdot \left[1 + j\omega C \cdot R_{cap}\right]} \tag{3.39}$$

A GBW improvement is crucial for the proposed PGA design operating with a large gain control range in order to support the receiver's large dynamic range as well as a wide bandwidth that supports high data rate. To provide the GBW improvement, the cascaded amplifier stages of the proposed PGA provides the gain enhancement while the introduced interconnect RC parallel network provides the bandwidth enhancement. The bandwidth enhancement obtained by the introduced zero at f_1 frequency mainly due to the interconnect stage (gain peaking) at high frequency cancels the dominant pole of the amplifier stage that limits the upper cutoff frequency of overall PGA bandwidth [3.52]. The frequency response affected by the cascaded stages is clearly indicated in the Figure 3.16 (a) and Fig 3.16 (b).

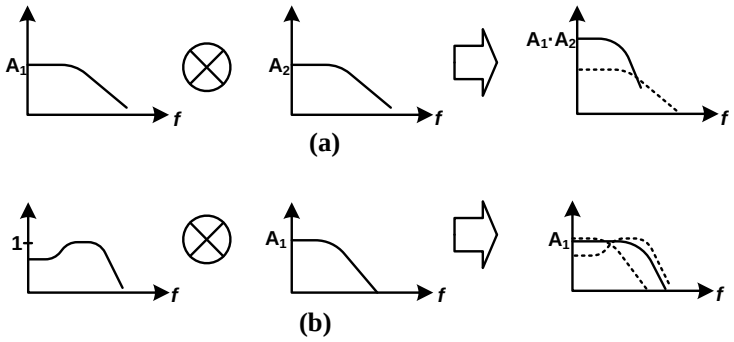


Figure 3.16 Frequency response of cascaded stages (a) without and (b) with bandwidth enhancement interstage.

This technique, is similar to an amplifier gain predistortion technique, in which the bandwidth is first enhanced by using the gain peaking onbtained from the parallel RC interstage network before cascading with the following amplifier stage. Thus the overall PGA bandwidth is closer to the bandwidth of the individual DVGA core (which is the bandwidth limiting stage than the post amplifer) is achieved. This technique ensures that the gain is not significantly affected and also the overall

cascaded bandwidth does not shrink unlike the scenario shown in Figure 3.16 (a) based on (3.38). This improves the overall PGA's GBW which is very desirable in the receiver frontend.

This proposed bandwidth enhancement technique provides an easy interface option for cascading several DVGA cores and post amplifier stages with very low effect on the gain, matching, amplifier linearity and interface dc performance without any addition DC power consumption. This technique is also validated by the measurement results shown in Table 3.1.

Additionally, the parallel RC interconnect stage provides an inherent dc coupling with an additional voltage drop that depends on the biasing conditions of the previous stage output and input of the next stage unlike the interconnect peaking inductors with smaller voltage drop (as determined by the inductor Q-factor) across it. Thus it overcomes the loading effect that may also degrade the bandwidth [3.47] and each stage can be optimized separately to have different dc voltages.

To validate this theoretical analysis, a plot of the simulated PGA's output power against the parametric sweep of the input power at 1 GHz frequency is shown in Figure 3.17. From the plot we find that the overall PGA's OP_{1dB} is almost gain variation independent (≈ -7.1 dBm) for the proposed PGA design. For the curves that is closer to the minimum gain condition, the degradation of PGA's OP_{1dB} is due to saturation of the DVGA core in addition to the already saturated post amplifier stage. This can be accounted for the condition described as $P_F \leq P_B < P_E$ (see Figure 3.14) and is verified by observing the P_{1dB} linearity performance in Table 3.1 that summarize the overall performance of the proposed PGA against the sub-blocks namely the DVGA core and the post amplifier.

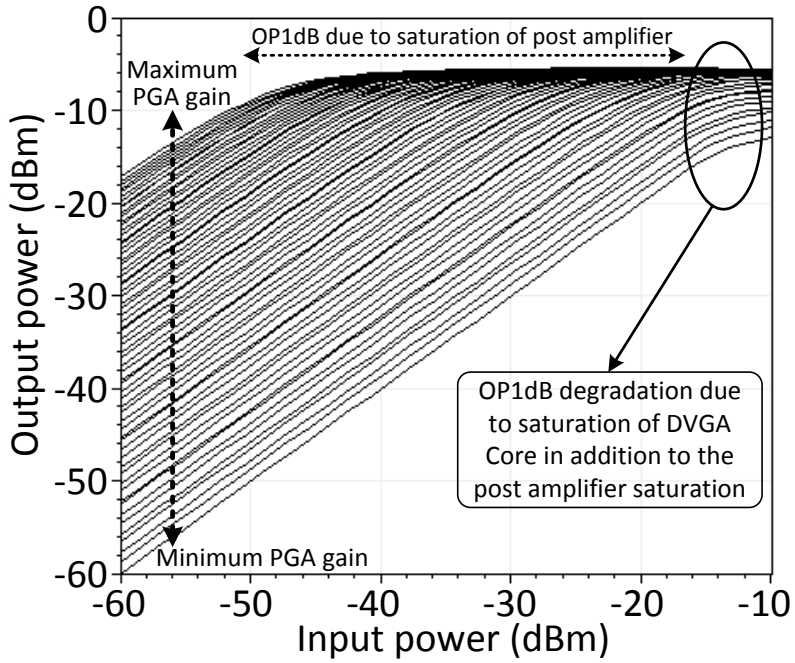


Figure 3.17 Simulated P_{1dB} linearity plot of the proposed PGA design for 64 gain steps at 1 GHz.

The component values of the interstage network (R and C) are to be carefully chosen and a design guideline is provided in the following based on design tradeoffs considered for the performance parameters of the overall proposed PGA design.

Factors affected by the resistor R in the interstage network:

1) The gain peaking and the resulting GBW product enhancement can be achieved by choosing smaller f_1 (zero frequency) and by positioning it within PGA's passband.

$$f_1 = \frac{1}{(2\pi \cdot R \cdot C)} \tag{3.40}$$

2) In the meantime, the group delay variation increases as the gain peaking is increased. In the proposed design, group delay variation is compromised by the GBW enhancement.
3) The resistor R is along the RF signal path as series connection and consequently a large value of R increases the signal loss.

$$Loss = 20 \cdot \log_{10}\left[\frac{(R + R_{in})}{R_{in}}\right] \tag{3.41}$$

4) The interconnect network has very little influence on overall PGA's input/output reflection coefficients. This is mainly caused due to the input fixed gain stage of the first stage DVGA core and the output buffer stage of post amplifier.

Hence a small value of R is normally preferred and the designed value is chosen as 45 Ω which along with the shunt capacitor C provides the GBW enhancement as well as it is mitigated based on the discussed overall PGA's performance degradations.

Factors affected by the capacitor C in the interstage network:

1) As a product with a smaller resistor R value, the capacitance C mainly determines the GBW enhancement based on (3.40). The R_{cap} which is a frequency-dependent resistive loss due to the skin effect is determined mainly by the quality factor of capacitor C and can be reduced by proper layout techniques such as by using short low loss thick metal interconnect traces. The overall PGA's upper cutoff frequency f_3 increases as capacitance C is decreased and is shown as,

$$f_3 = \frac{1}{(2\pi \cdot R_{cap} \cdot C)} \tag{3.42}$$

2) A smaller C results in a reduced layout size based on the predetermined capacitance of the parallel plate metal-insulator-metal (MIM) capacitor supported in the PDK which is given as,

$$C = \varepsilon_{ox} \cdot W \cdot L \tag{3.43}$$

Hence a small value of C is also normally preferred. However, to meet the desired gain peaking requirement based on (3.40) with a reduced degrading effect on the overall PGA's performance by a small resistor R, the designed capacitance C value is chosen as 5 pF.

3.2.9. Stability analysis

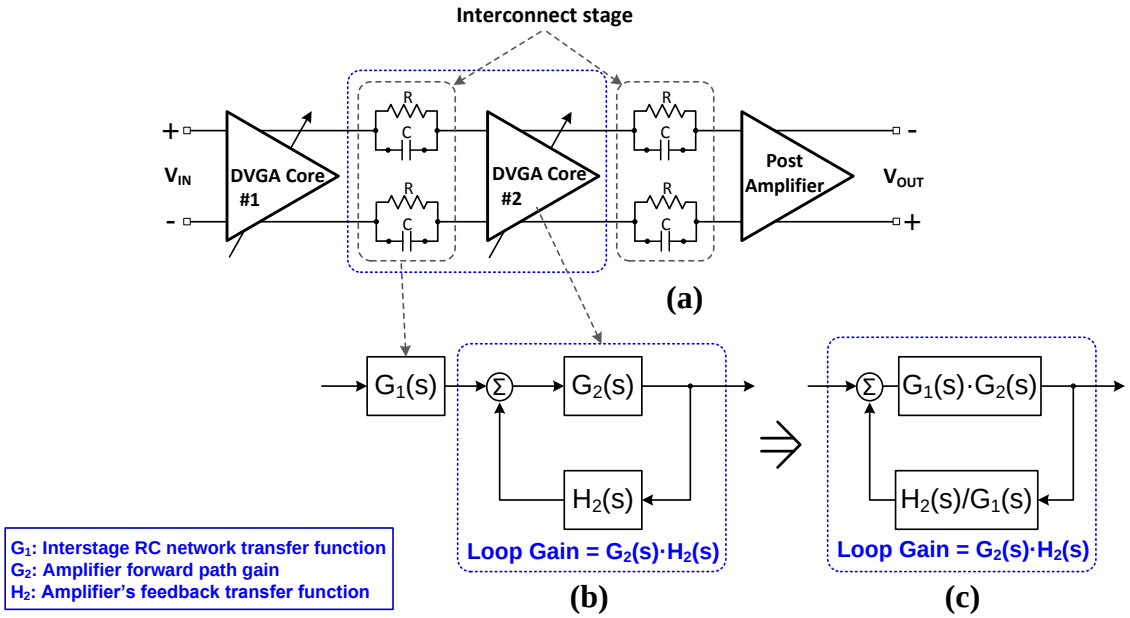


Figure 3.18 Block diagram deduction of the overall PGA stability criterion.

The proposed interstage RC network, consisting of a parallel resistor and a capacitor, is a cascaded network which is external (not in a feedback loop) to the PGA's sub-block amplifiers (DVGA core and post amplifier). Hence the RC interstage network does not form a part of the sub-block amplifiers' feedback loop and do not significantly affect the stability criteria of the overall cascaded PGA amplifier chain as shown in Figure 3.18.

3.2.10. PGA Power Shutdown

The proposed PGA is designed for low power transceiver application, by consuming a minimized DC power along with a provision of the power down (sleep) mode, during which the non-functional PGA in the transceiver system can be turned OFF, using a digital control pin (PD/PwrDwn). The DC current dissipated is insignificant when the power down/sleep mode of the PGA is active without turning OFF the supply voltage VDD of the whole transceiver system.

3.3. Circuit Implementation

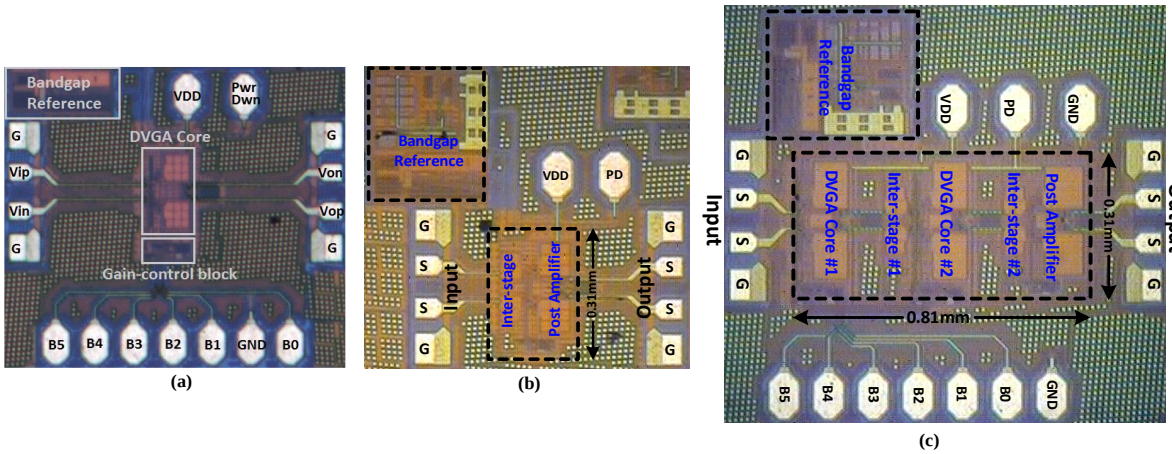


Figure 3.19 Die microphotograph of (a) DVGA core (b) post amplifier (c) PGA.

The proposed post amplifier design with input interstage network and the overall proposed dB-linear PGA with DCOC design are realized by using a 0.18-µm SiGe BiCMOS process from Tower Jazz Semiconductors Inc., Newport Beach, CA, USA. The microphotograph of the DVGA core, the post amplifier with input interstage network and the proposed PGA along with bandgap reference is shown in Figure 3.19 (a), (b) and (c) respectively. The overall proposed PGA occupies a core die area of 810 µm × 310 µm excluding the measurement probing pads. The proposed PGA, DVGA core and the post amplifier performance are experimentally verified by on-wafer probing by using the Agilent E8364B PNA network analyzer, RoHS SMBV 100A signal generator, LeCroy Waverunner 6000A series high speed oscilloscope, and Agilent E4407B ESA-E series spectrum analyzer.

3.4. Experimental results

The experimental plots of the overall PGA is shown in the following from Figure 3.20 to Figure 3.25 while the performance parameters for each of the DVGA core and the post amplifier stages against the estimated and the actual PGA is tabulated in the Table 3.1. The performance comparison of the PGA as well as the DVGA core against the state-of-the-art VGA performance is provided in Table 3.2.

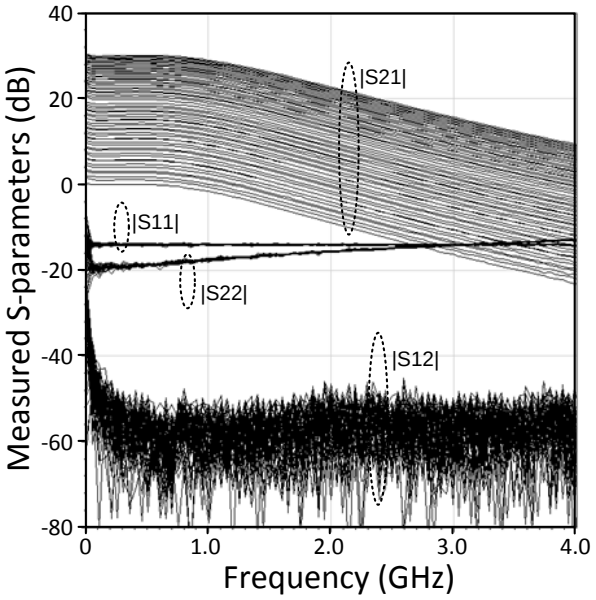


Figure 3.20 Measured PGA S-parameters over the 64 gain steps.

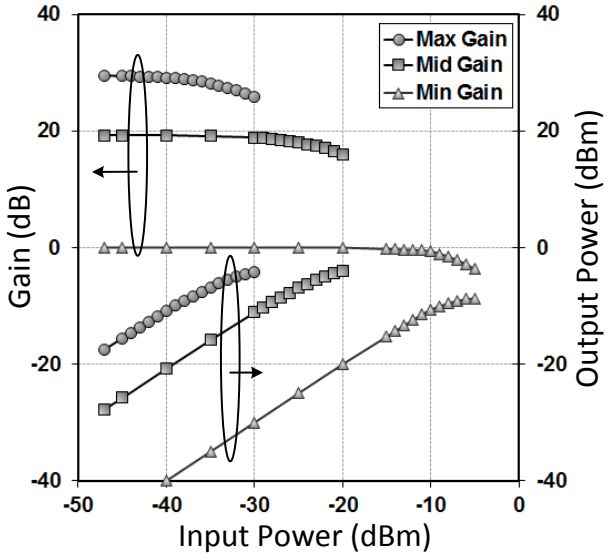


Figure 3.21 Measured P_{1dB} linearity plots for max, mid and min PGA gain at 1 GHz.

Table 3.1 Summary of measured performance of PGA, DVGA core and post amplifier

Parameter	Units	DVGA Core	Post amplifier	PGA (Actual)	PGA (Estimated)
Gain	dB	-10 to +7.8	+16	-1.4 to 30.2	-4 to 31.6
3-dB Bandwidth	Hz	2M to 1.9G	2M to 2.4G	3M to **1.7G**	2M to **0.97G***
Power consumption	mW	12.2	9.86	35.3	34.26
Input P_{1dB}	dBm	-12.5 to -11	-22	-9 to -36	-8.5 to -38.5
Output P_{1dB}	dBm	-22.4 to -5.8	-7.1	-10 to -7.5	-7.5
Gain control	-	6-bit	Fixed	6-bit	12-bit
Power down current	µA	310	308	915	926
Core die area	mm^2	0.048	0.03	**0.25****	**0.126**

*Equation (3.38), with n = 3 and ω_o = 1.9 GHz (worst case: limited by stage with narrower bandwidth).
** Area increase due to the parallel RC interstage network.

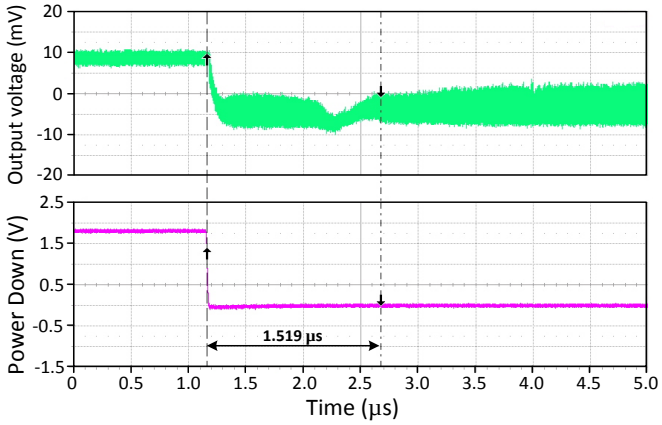
The estimated values in the Table 3.1 are obtained as,
1. Gain = DVGA Core gain×2 + Post amplifier gain
   For minimum gain condition, PGA gain = -10×2+16 = -4 dB
   For maximum gain condition, PGA gain = +7.8×2+16 = 31.6 dB
2. 3-dB Bandwidth $= \omega_T = \omega_0 \cdot \sqrt{2^{1/n} - 1} = 1.9 \times 10^9 \cdot \sqrt{2^{1/3} - 1} = 0.97\ GHz$
3. Power consumption = 12.2×2+9.86 = 34.26 mW
4. Input P_{1dB} = Output P_{1dB} – PGA Gain
   For minimum gain condition, Input P_{1dB} = -12.5 – (-4) = -8.5 dB (Due to DVGA core + post amplifier saturation)
   For maximum gain condition, Input P_{1dB} = -7.1 – (31.6) = -38.7 dB (Due to only post amplifier saturation)
5. Output P_{1dB} = Output P_{1dB} (Post amplifier)
6. Gain control = DVGA Core ×2 = 6 ×2 = 12 bits
7. Power down current = DVGA Core ×2 + Post amplifier = 310 ×2 +308 = 928 µA
8. Core die area = DVGA Core ×2 + Post amplifier = 0.048 ×2 +0.03 = 0.126 mm^2

Table 3.2 Measured performance of state-of-the-art VGA with wide gain range

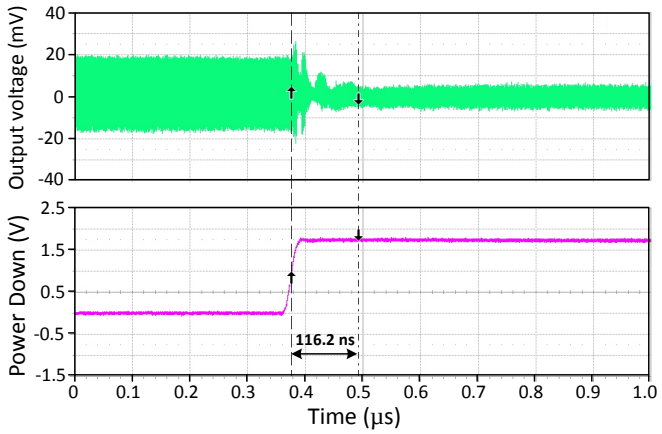
Parameter	Unit	This Work [A.2]	This work [A.1]	RFIC'13 [3.53]	RWS'13 [3.54]	JSSC Jun'12 [3.24]
Technology	-	**0.18 µm SiGe**	**0.18 µm SiGe**	65 nm CMOS	90 nm CMOS	0.13 µm SiGe
Gain control range	dB	**-1.4 to +30.2**	**-10.6 to +7.8**	+3 to +31	-25.3 to +59	-10 to +30
Linearity error	dB	**±0.1**	**±0.1**	-	-	±0.3
3-dB Bandwidth	Hz	**3 M to 1.7 G**	**2 M to 1.9 G**	20 M to 0.98 G	1 G	0.2 M to 7.5 G
Power consumption	mW	**35**	**12.2**	48	21.9	72
Supply voltage	V	**1.8**	**1.8**	1.1	1.4	1.2
Active core area	mm^2	**0.25**	**0.048**	0.2	0.07	1
Output swing	mVpp	**200 to 266**[§]	**47.9 to 323**[§]	632[§]	100 to 178[§]	35
Gain control mode	-	**Digital**	**Digital**	Digital	Digital	Analog

[§]Based on output 1-dB gain compression (P_{1dB}) point

The difference between the actual and estimated results from Table 3.1 are significant for upper cutoff frequency of 3-dB bandwidth and the core die area which are the trade-off considered by introducing the proposed interstage network. The marginal differences in other parameters namely the gain range, power consumption, input and output P_{1dB} can be attributed to the minimum change in the bias condition due to the interstage network.



(a)



(b)

Figure 3.22 Measured PGA switching time based on the single-ended output against the power down (PwrDwn/PD) digital input (a) Turn ON (≈ 1.52 µs) and (b) Turn OFF (≈ 116 ns).

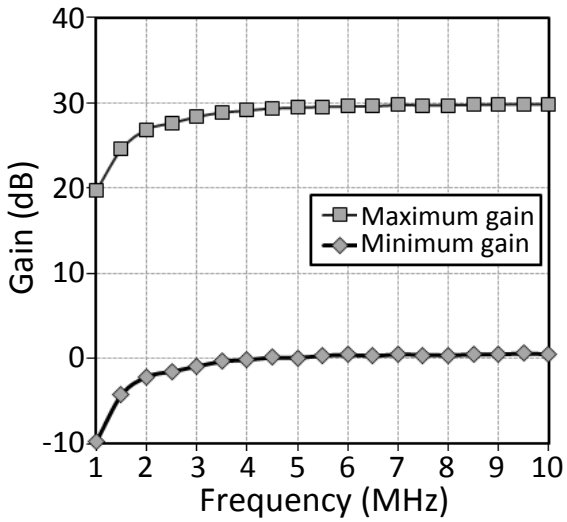


Figure 3.23 Measured low frequency gain plot for max and min PGA gain condition.

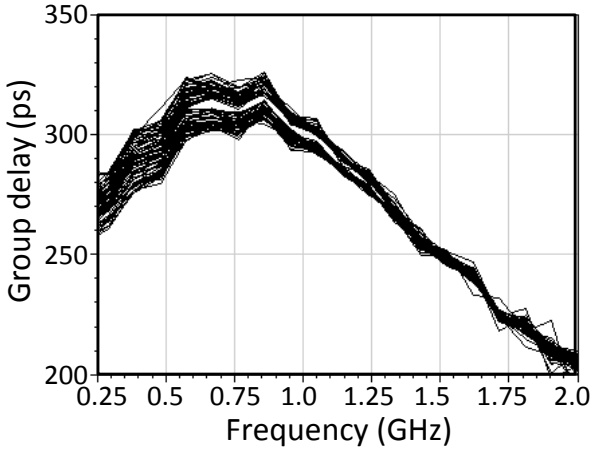


Figure 3.24 Measured group delay of proposed PGA over the 64 gain steps.

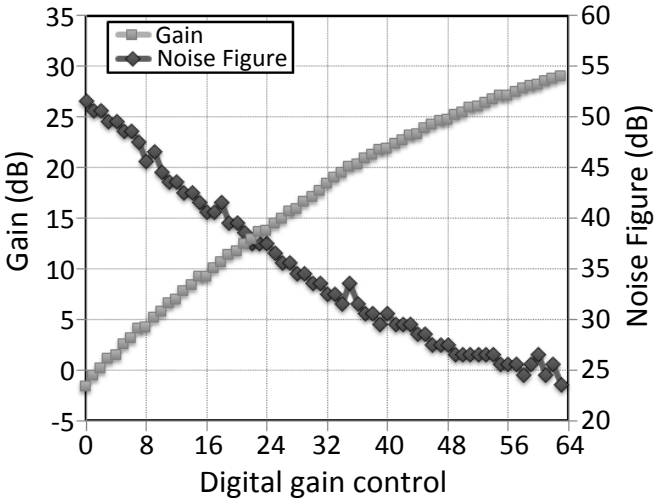


Figure 3.25 Measured dB-linear gain and noise figure characteristics at 1 GHz frequency of the proposed PGA.

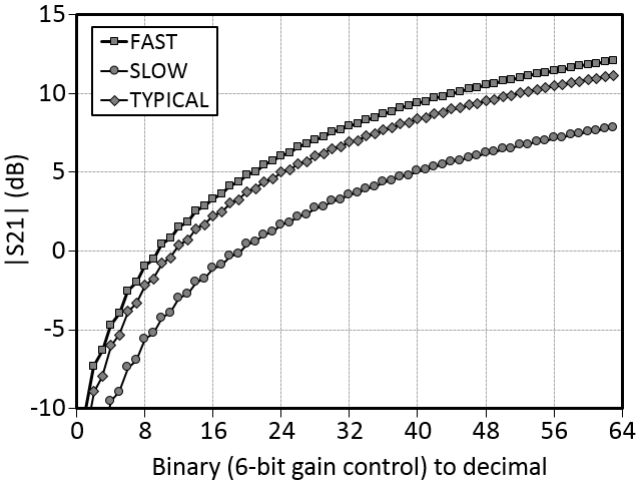


Figure 3.26 Simulated gain characteristics against process corner variation for the DVGA without dB-Linearizer at 1 GHz frequency.

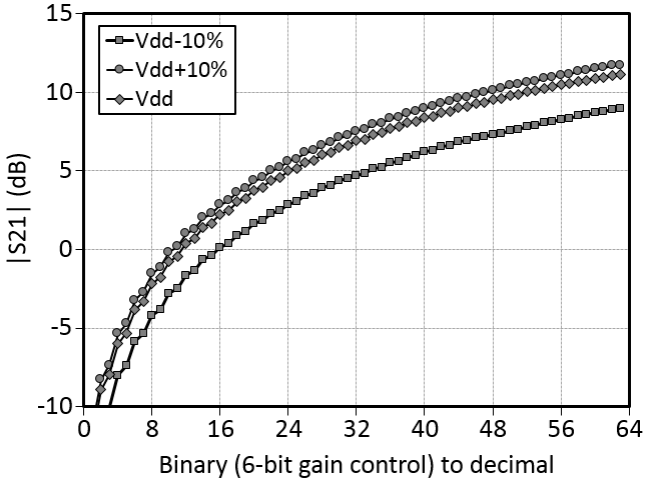


Figure 3.27 Simulated gain characteristics against supply voltage variation for the DVGA without dB-Linearizer at 1 GHz frequency.

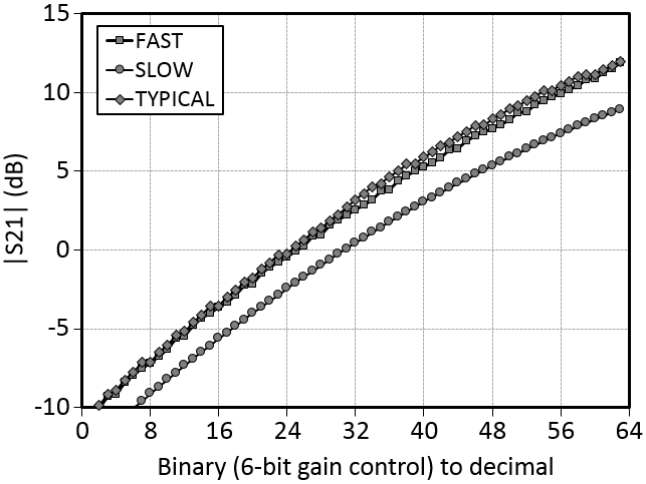


Figure 3.28 Simulated gain characteristics against process corner variation for the DVGA with dB-Linearizer at 1 GHz frequency.

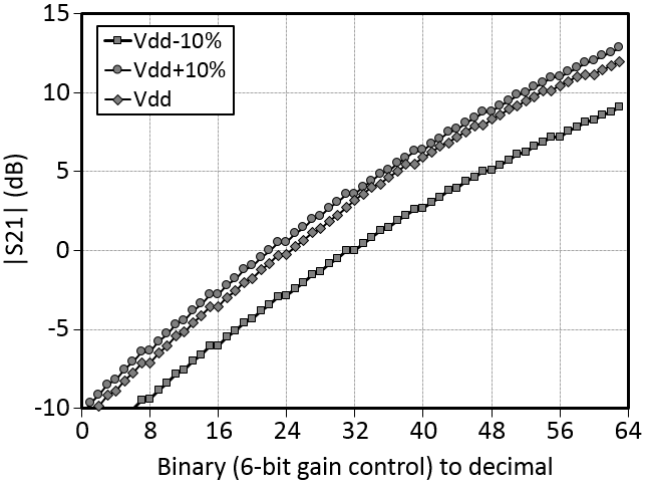


Figure 3.29 Simulated gain characteristics against supply voltage variation for the DVGA with dB-Linearizer at 1 GHz frequency.

The simulated process and supply voltage sensitivity on the DVGA core gain based on without the proposed dB-linearizer is shown in Figure 3.26 and Figure 3.27, respectively and based on with dB-linearizer is shown in Figure 3.28 and Figure 3.29, respectively.

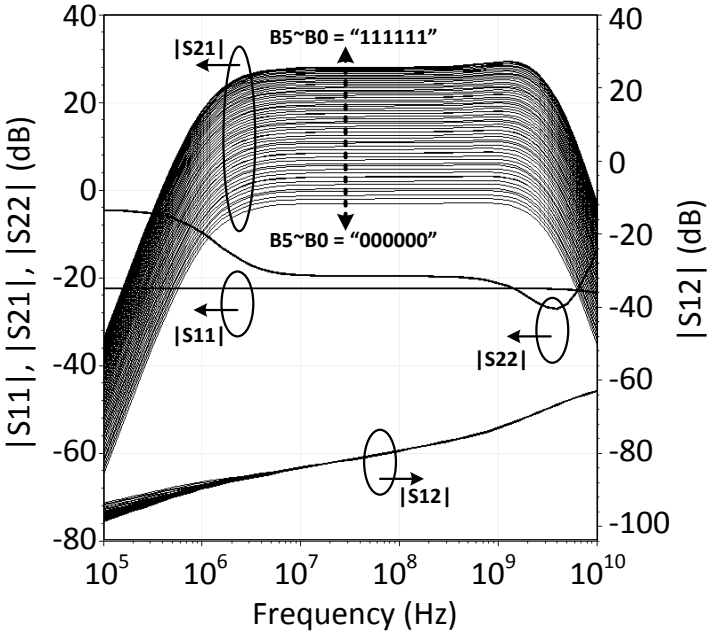


Figure 3.30 Simulated PGA S-parameters over the 64 gain steps.

The simulation S-parameter plot of the proposed PGA over all the 64 gain steps is included as Figure 3.30.

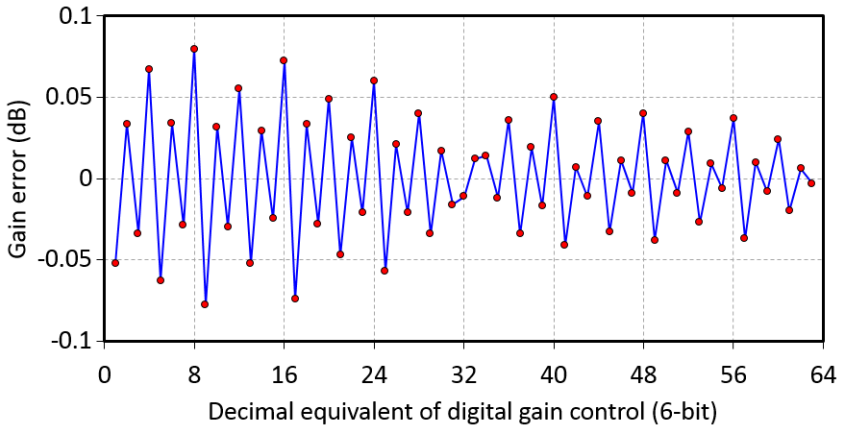


Figure 3.µ Measured dB-linear gain error of the proposed PGA.

The measured linearity error of the proposed PGA is shown in Figure 3.31 and is within a tolerance of ±0.1 dB over the entire 64 gain steps.

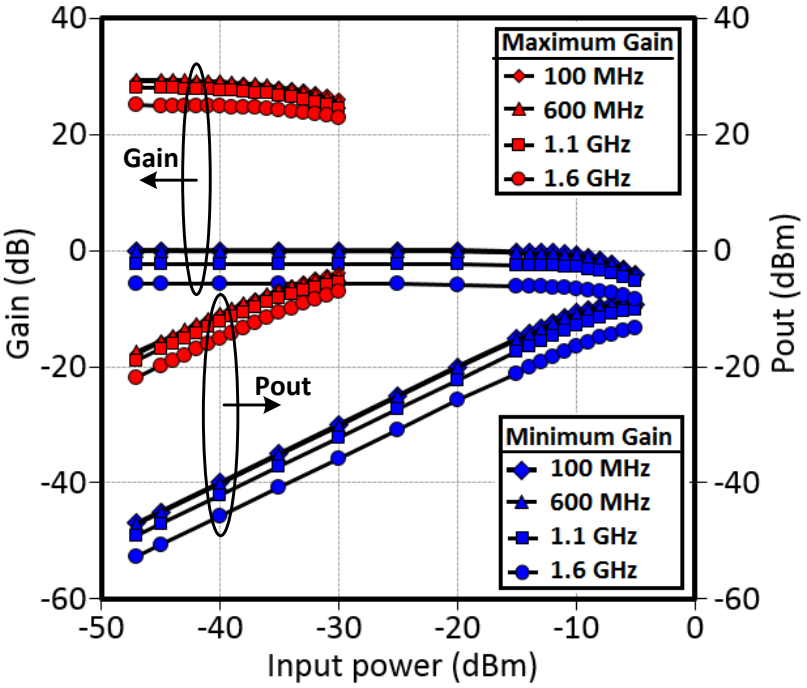


Figure 3.31 Measured PGA gain and output power against frequency sweep from 100 MHz to 1.6 GHz (step = 500 MHz).

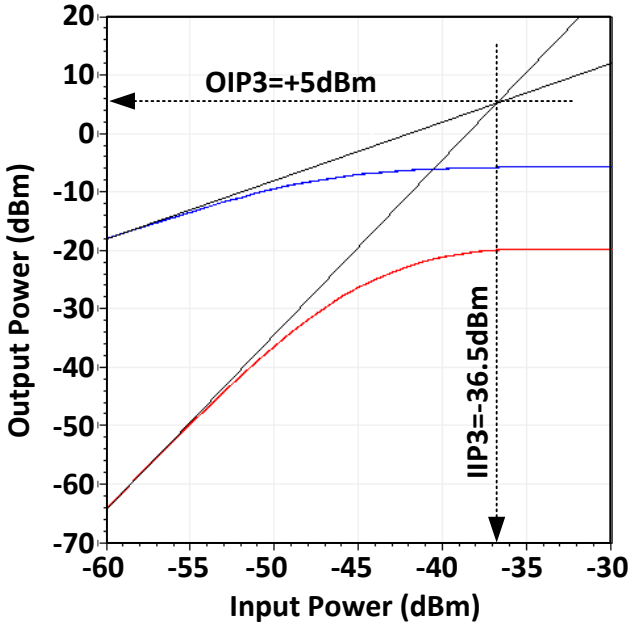


Figure 3.32 Simulated IIP3 of proposed PGA at 1 GHz frequency with maximum gain condition.

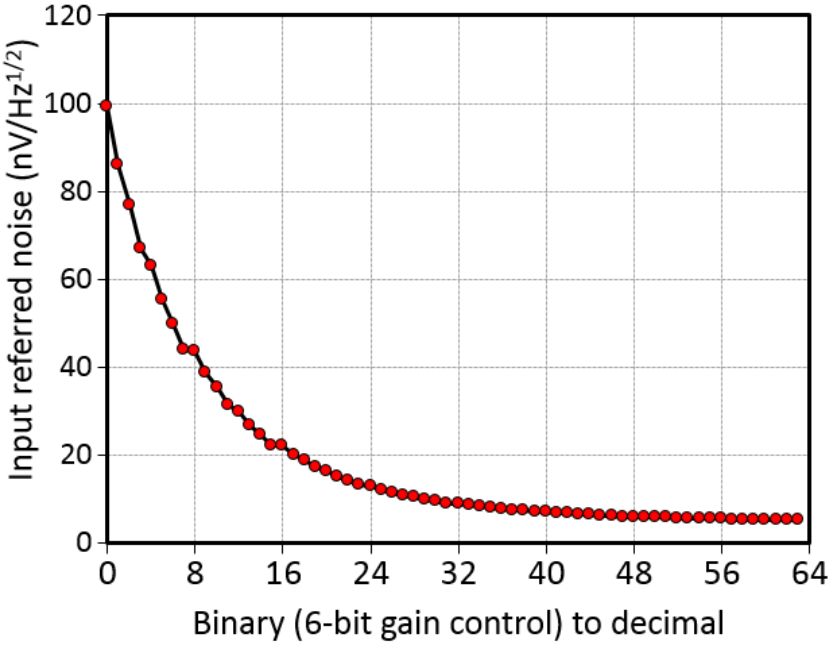


Figure 3.33 Simulated IRN plot of the proposed PGA over the 64 gain steps at 1 GHz.

The simulated input referred noise (IRN) of the proposed PGA is shown in Figure 3.34 for 64 gain steps at 1 GHz frequency and for maximum gain condition is 5.1 nV/sqrt(Hz).

3.5. Summary

This chapter presents the design of a 6-bit programmable gain amplifier (PGA) with large gain control range along with the DVGA core and the post fixed gain amplifier design considerations which is used as sub-blocks in the proposed PGA. All the three designs are fabricated in a 0.18-µm SiGe BiCMOS process and measured by using on-wafer probing. The proposed PGA design simultaneously achieves an enhanced GBW product and a better OP_{1dB} linearity performance with a large dynamic range without significantly increasing the circuit complexity which are the most desirable characteristics for the integration into the receiver RF frontend of the low-cost low-power consumer applications requiring good gain control precision.

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Chapter 4. Variable bandwidth VGA with tunable on-chip DCOC

In this chapter, the proposed CMOS based VGA circuit provides a flexibility of switching ON/OFF the DCOC functionality by using a digital PMOS switch along with voltage controlled lower cutoff frequency. Hence by providing this reconfigurable capability in the CMOS analog VGA design, a post-fabrication tradeoff between the baseband SNR and BER requirements can be realized. Additionally, the RF transceivers can support a multi-standard baseband [4.1] interface by switching between the direct conversion receiver (DCR) with zero-IF (direct conversion scheme) and the tunable low-IF (superheterodyne) receiver schemes [4.5].

4.1. Circuit topology and design

The proposed design is a CMOS based compact variable gain amplifier (VGA) as shown in Figure 4.1 with four sub-blocks namely the input buffer, the four-stage VGA core, the output buffer and the programmable DCOC. To ensure a low DC power consumption, the design is biased using NMOS current sinks mirrored from the stable current sources (I_{const} and I_{gc}) that limits the rail-to-rail DC current of the overall design. The input stage is a common-gate (CG) amplifier to provide fixed gain that is biased by using I_{const} current (≈50μA) and a wideband input impedance matching which are independent of the VGA gain. The VGA core comprises of four-stage common-source (CS) amplifier with resistive load to provide wideband gain flatness. The output buffer is a common-drain (CD) source follower with common mode feedback circuit providing a stable output common mode voltage and a good output impedance matching.

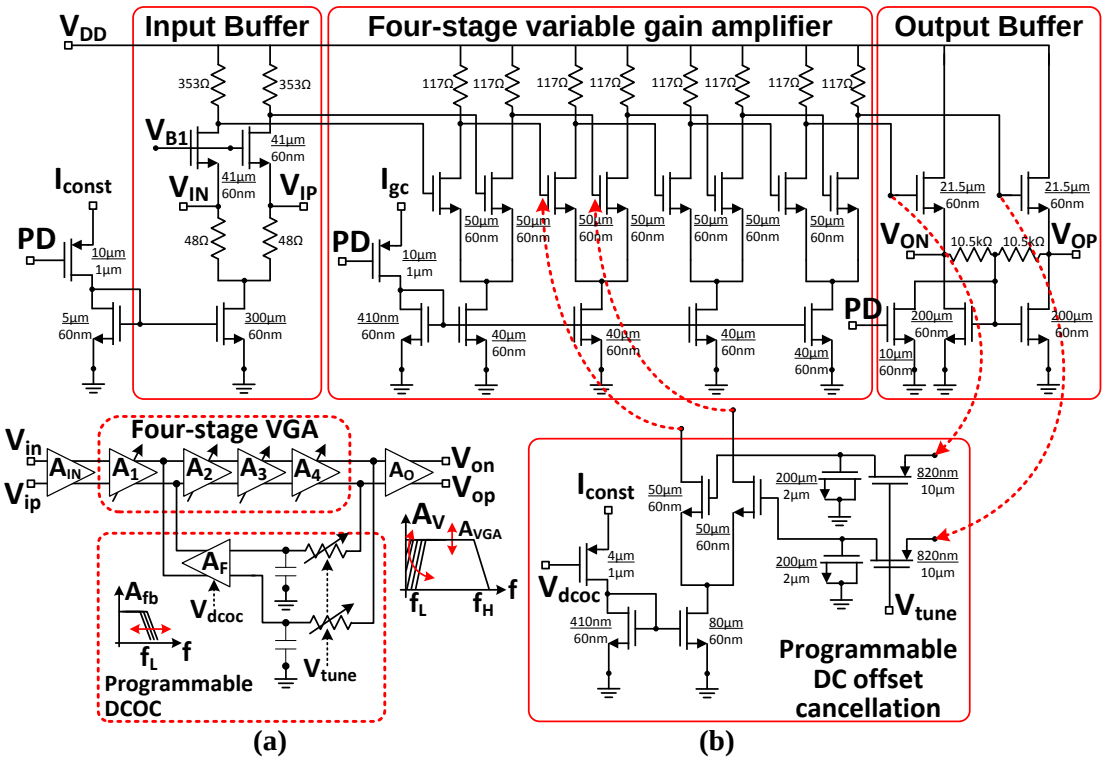

Figure 4.1 Circuit schematic of the proposed CMOS variable gain amplifier.

4.1.1. Linear Gain control with a gain control range

By using current mirrors the gain control current I_{gc} is used to bias the differential 4-stage CE amplifiers. As the I_{gc} current varies it linearly varies the amplifying transistor-pair transconductance (g_m) and hence a linear gain control is achieved by this proposed design. This result is verified by the measurement results obtained from the on-wafer probing. By using the PD input pin the gain control current that biases the amplifier stages can be shutoff and hence results in the overall VGA's power down or sleep mode. During the power down mode the VGA consumes very small current and hence contributes to the DC power saving.

4.1.2. DCOC switch control and fine tuning lower bandwidth cutoff frequency

The programmable DCOC comprises of a MOS transistor based RC LPF that extracts the DC from output and cancels it with the input of the second stage by using a differential amplifier as shown in Figure 4.1 (b).

When the V_{dcoc} = 1.2V, the DCOC functionality is turned OFF by using a PMOS switch, thus the VGA forward path has a low pass filter (LPF) response apparently allowing the DC component to pass to the baseband section. Conversely when the V_{dcoc} = 0V, the DCOC functionality is activated, thus extracting the DC component from the output and cancelling the DC signal from the RF input signal via the feedback path. The VGA lower cutoff frequency (determining by the DCOC) is tunable by using V_{tune} analog control voltage which varies the channel resistance of the PMOS pass transistor used in the DCOC LPF. This DCOC functionality with variable lower cutoff frequency provides a reconfigurability option in the receiver RF frontend interface based on the baseband standard specifications with a better tradeoff between the baseband processing efficiency with an improved SNR against the circuit DC offset effects such as the BER specification.

The size of lumped RC components from the process design kit (PDK) used in a DCOC LPF depends on VGA's operating frequency and it is usually very large for frequencies close to the baseband. To avoid large die area (mainly due to the passive lumped RC filter components) and a high fabrication cost, the RC components of LPF are implemented by using the MOS transistors in the proposed VGA. The large resistor value is implemented by using the PMOS transistors biased to operate in the triode region with the gate voltage controlling the channel resistance and is given by (4.1).

$$R_{ch} \cong \left[\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L} \right)_p \cdot \left(V_{DD} - V_{tune} - |V_{THP}| \right) \right]^{-1} \tag{4.1}$$

where μ_p, C_{ox}, $\left(\frac{W}{L}\right)_P$ and V_{THP} are the electron mobility, the gate oxide capacitance per unit area, the transistor aspect ratio, and the threshold voltage of the LPF PMOS.

The fixed large shunt capacitor used in the feedback LPF is designed by using NMOS transistor with the source and drain connected to GND as the bottom plate and the gate terminal as the top capacitor plate. This results in a very compact design which is easily integrated for mobile applications.

4.1.3. Common mode feedback control (CMFB)

The proposed design has the CMFB similar to the DVGA core design discussed in the previous chapter. The CMFB is implemented as the diode connected active load of the CD buffer stage to provide a stable fixed common-mode output DC that can be used to bias the following stages. Also this common-mode voltage is independent of the gain control.

4.2. Circuit implementations and experimental results

The proposed design is fabricated by using the Global Foundries 65nm CMOS process. The die microphotograph of the proposed VGA along with the layout is shown in Figure 4.2. The VGA occupies a compact die area of 75 μm × 80 μm (excluding measurement pads) and 510 μm × 620 μm (with measurement pads for the testability). Since the dummy fill covers the actual active core area to meet the metal density requirement of the fabrication house. Hence the layout of the core design is included as the Figure 4.2 (b).

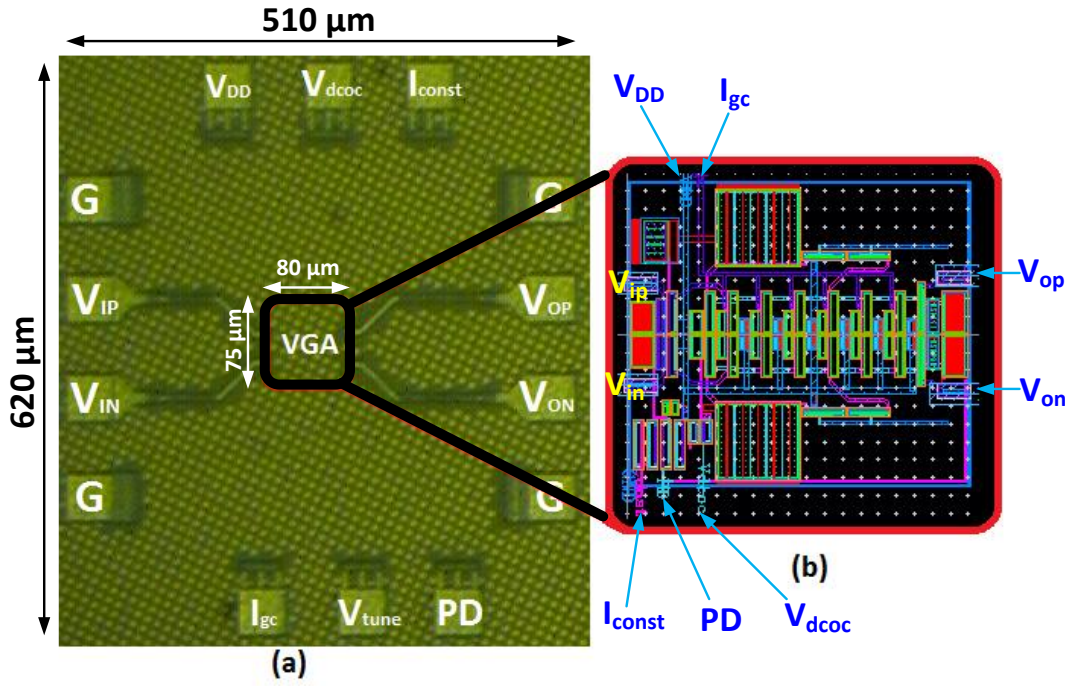

Figure 4.2 (a) Die microphotograph (b) Layout of core CMOS variable gain amplifier.

The measured data is obtained by on-wafer probing with the Agilent E8364B network analyzer (PNA) and HP 8970B noise figure (NF) meter by using differential calibration until the RF probe tips. The measured variable gain along with the input/output return loss are shown in Figure 4.3 and Figure 4.4, respectively by varying I_{gc} from 3µA to 150µA. The gain control shown in Fig 4.3 is not dB-linear as discussed in the previous sub-section 4.1.1. The analog tunable DCOC is achieved by activating the DCOC digital switch (V_{dcoc} = 0V) and by controlling the VGA's lower cutoff frequency by varying the V_{tune} voltage from 0 to 1.2V as shown in Figure 4.5. From Figure 4.5 (a) with the minimum gain setting (I_{gc} = 3µA) a passband gain drop is seen when the DCOC lower cutoff frequency is increased by decreasing the V_{tune} from 1.2V to 0V which is not observed in Figure 4.5 (b) for the maximum VGA gain (I_{gc} = 150µA). This behavior is caused by the subtraction of the lower forward path signal (VGA minimum gain) with the increasing feedback signal strength due to the reduced DCOC LPF loss (series R_{ch} of the PMOS pass transistor is decreasing) that increases

the VGA's passband attenuation. Although this does not significantly affect the baseband interface performance, since for VGA minimum gain condition, the DC component along with the input RF signal is also attenuated that prevents saturation of the baseband circuitry due to DC offsets and additionally enhances the VGA gain control range. The monotonous not dB-linear trend of the measured gain and the noise figure against I_{gc} is shown in Figure 4.6. The linearity performance based on the 1-dB compression point (P_{1dB}) plots for a maximum (I_{gc} = 150μA), mid (I_{gc} = 30μA) and minimum (I_{gc} = 5μA) VGA gain conditions are consolidated in Figure 4.7. The maximum measured in-band group delay variation over the entire VGA gain range is 20 ps as shown in Figure 4.8.

The on-wafer probing measured results of the proposed VGA are summarized and compared with the existing state-of-the-art VGAs [4.8]–[4.13] in Table 4.1. From the comparison we find that the proposed CMOS VGA has better bandwidth, compact die area and tunable DCOC while simultaneously achieving comparable gain range and dc power consumption as compared to the CMOS based VGAs [4.8]–[4.11]. The dc power consumption of the VGA in [4.11] is lower than the proposed VGA design. However, for the purpose of measurement, additional output buffers are necessary in [4.11] to achieve the required 50-Ω output impedance matching. As compared to the state-of-the-art SiGe HBT based DVGA designs in [A.2], [A.4] as proposed in the previous chapter, the proposed CMOS VGA has improved gain control range, a tunable DCOC and a compact die area. The power consumption and the bandwidth of [A.4] is better than the proposed VGA design. However, the design in [A.4] lacks the on-chip DCOC capability. The VGA design in [A.2] has passive RC based DCOC that occupies large die area and is overcome in the proposed design by using MOS based active-RC components.

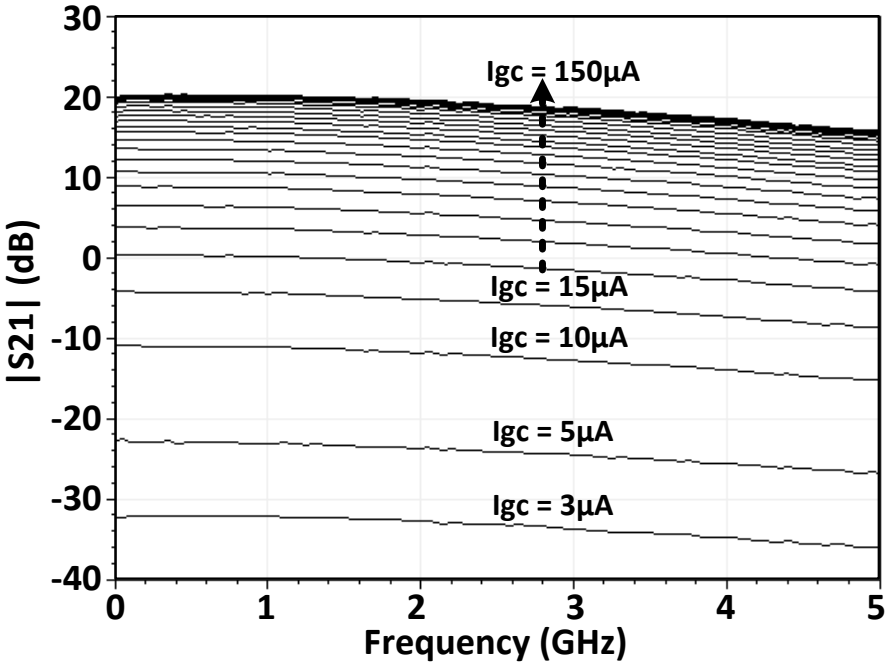

Figure 4.3 Measured V GA gain (I_{gc} = 3 µA to 150 µA, step = 5µA).

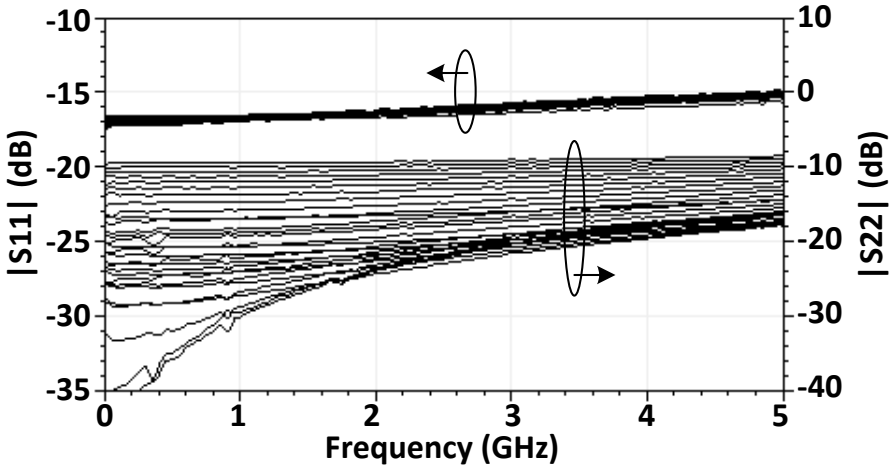

Figure 4.4 Measured VGA return loss (I_{gc} = 3 µA to 150 µA, step = 5 µA).

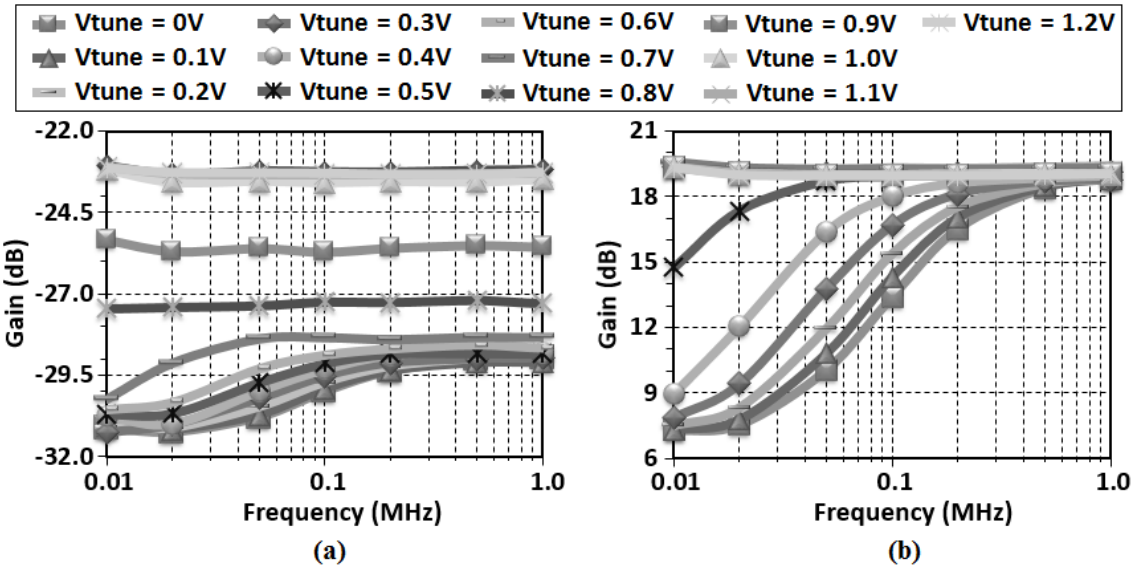

Figure 4.5 Measured VGA low frequency response with and without the DCOC (V_{dcoc} = 0V and V_{tune} = 0 to 1.2V, step = 0.1V) (a) I_{gc} = 3 µA (b) I_{gc} = 150 µA.

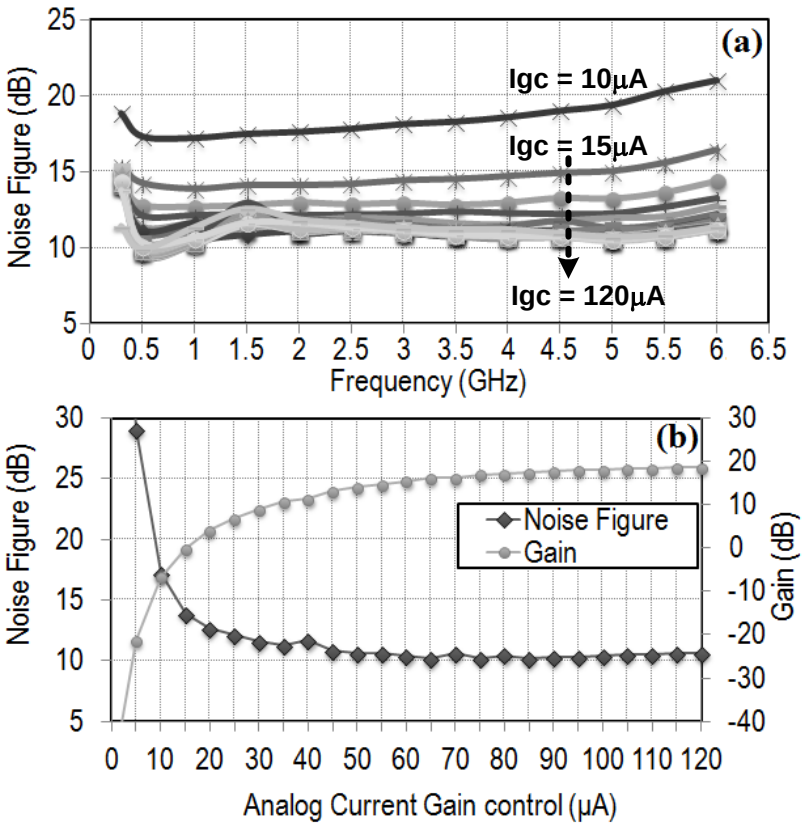

Figure 4.6 (a) Measured noise figure against frequency (b) Measured gain and noise figure characteristics at 1 GHz for I_{gc} = 5 µA to 120 µA, step = 5 µA.

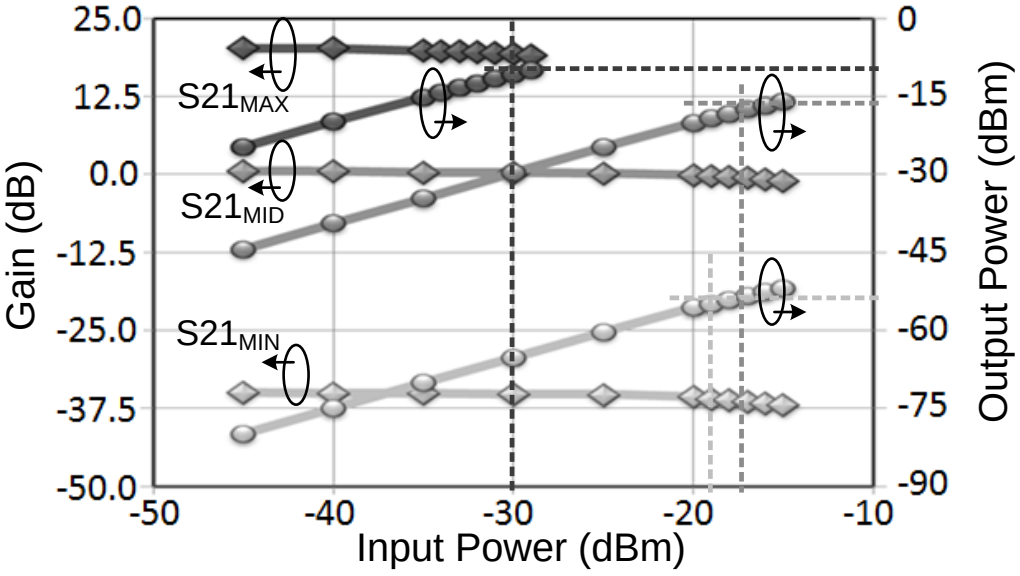

Figure 4.7 Measured P_{1dB} for maximum (I_{gc} = 150 µA), mid (I_{gc} = 30 µA) and minimum (I_{gc} = 5 µA) VGA gain at 1GHz.

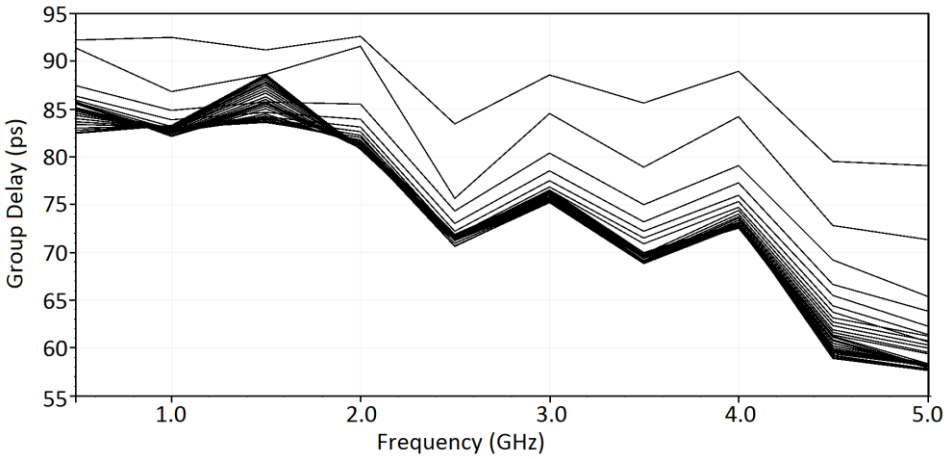

Figure 4.8 Measured group delay of proposed VGA (I_{gc} = 3 to 150 µA, step = 5 µA).

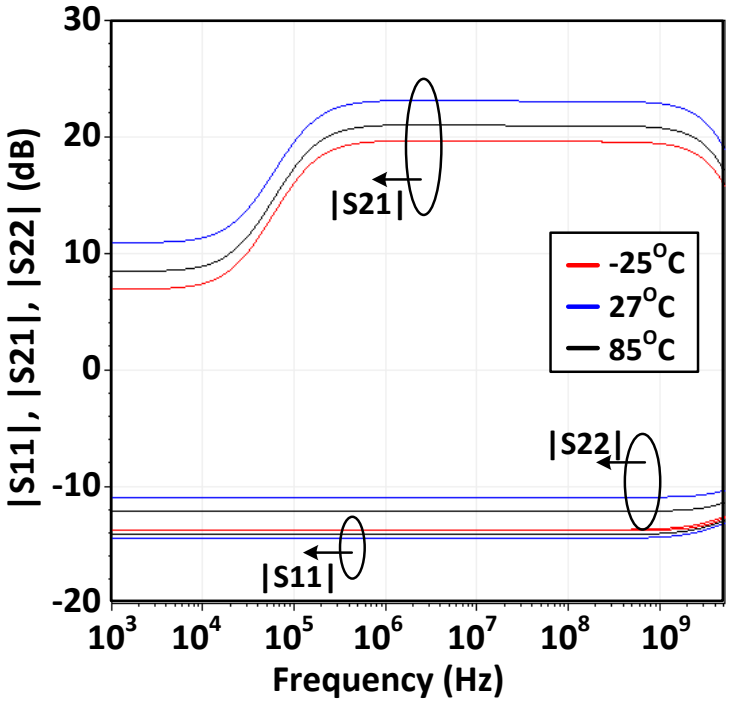

Figure 4.9 Simulated gain and IO return loss of proposed VGA against temperature variation.

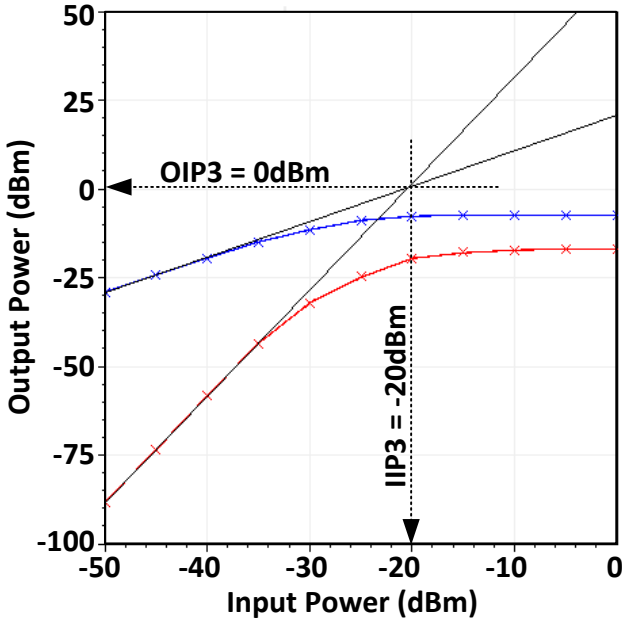

Figure 4.10 Simulated IIP3 plot of the proposed VGA for maximum gain at 1GHz.

Table 4.1 Measured performance summary of the state-of-the-art VGA

Parameters	**Unit**	**This Work [A.3]**	**[4.8]**	**[4.9]**	**[4.10]**	**[4.11]**	**[A.4]**	**[A.2]**
Technology	-	**65nm CMOS**	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	0.18μm SiGe HBT	0.18μm SiGe HBT
Gain range	dB	**-39.4 to 20.2**	-29 to +23	+3 to +31	-25.3 to +59	-10 to 50	-16.5 to 6.5	-1.4 to +30.2
3-dB bandwidth	Hz	**(0~0.2M) to 4G**	0.8G	20M to 0.98G	1G	0.1M to 2.2G	5.6 G	3M to 1.7G
Noise Figure	dB	**10 to 27**	-	6 to 21	15.2 to 50	17 to 30	16.5 to 27.1	23.5 to 52
Input P_{1dB}	dBm	**-17 to -30**	-15 to -26	-4 to -31	~+9 to -70.1	-13 to -55	-17 to -27	-9 to -36
Core Area	μm^2	**75 × 80**	71 × 490	330 × 470	660 × 106	270 × 50	170 × 60	810 × 310
DC power	mW	**26**	31.2	48	21.9	2.5	7.9	35.3
On-chip DCOC	-	**Yes**	No	Yes	Yes	Yes	No	Yes
Tunable DCOC	Hz	**Yes (0 to 0.2M)**	No	No	No	No	No	No
Gain control mode	-	**Analog current**	Digital voltage	Digital voltage	Digital voltage	Analog voltage	Digital current	Digital current

4.3. Summary

A compact variable gain amplifier (VGA) with analog tunable and digitally switched DCOC capability is proposed and developed by using a commercial CMOS technology in this research work. A gain control range of 60 dB, a die size of 75 μm × 80 μm and a wide operating bandwidth of over 4 GHz are achieved, simultaneously which are verified by using on-wafer probing measurement. The tunable DCOC capability provides a better reconfigurable baseband interface to tradeoff between the SNR and BER conflicting requirements of the baseband standards even in the post-fabricated design. This design hence proposes a VGA with reconfigurable bandwidth by controlling the gain frequency response lower cutoff frequency.

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Chapter 5. Variable center frequency VGA

In this chapter, a SiGe BiCMOS based *K*-band high power efficient differential amplifier with a hybrid solution of both a variable gain and a tunable center frequency is proposed, implemented and verified experimentally. The proposed design improves the power efficiency by simultaneously reducing the overall dc power consumption (using the stacked architecture with dc current reuse technique) and improving the amplifier linearity (using a high quality factor (*Q*) inductive load) that increases the output signal swing and the power level. Additionally, the proposed 2-stage stacked amplifier achieves frequency band re-configurability together with the load inductance *Q* enhancement by using a tank circuit (consisting of a 2-coil monolithic transformer coupled with a MOS varactor bank) as the tunable amplifier load. By using digital re-configurability and frequency band switching, the proposed design provides a wideband gain flatness that can support multiple *K*-band standards. A qualitative design analysis of the proposed frequency tunable digitally controlled variable gain amplifier (DVGA) addressing the various system considerations are discussed.

This chapter is organized as follows: Section 5.1 describes the topology of the proposed design, Section 5.2 emphasizes about detailed analysis of the proposed circuit design. The design and implementation details of the proposed frequency tunable amplifier load are covered in Section 5.3. Section 5.4 discusses about the design validation with experimental results that are proven using on-wafer measurement and the performance is compared with the state-of-the-art *K*- and *Ka*-band amplifiers. Finally, the chapter conclusion is provided in Section 5.5.

5.1. Circuit topology

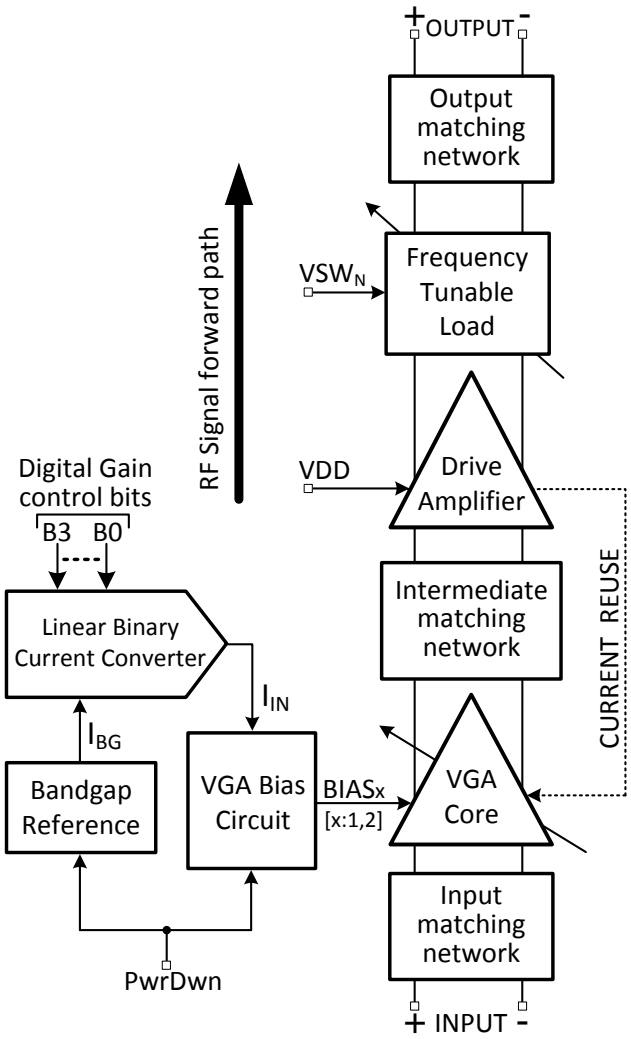

Figure 5.1 Block diagram of proposed frequency tunable *K*-band amplifier.

The proposed *K*-band frequency tunable amplifier is a non-inverting fully-differential two stage cascaded amplifier with the stacked architecture and reusing dc current between the two stages. The structure of the proposed amplifier design is summarized as a block diagram shown in Figure 5.1. The first stage amplifier is a variable gain amplifier (VGA) with a four bit (B3~B0) digital gain control and the second stage is a frequency tunable amplifier. In order to provide an improved power transfer efficiency, the stacked amplifier stages include impedance matching networks at input, output and at the intermediate stage.

The gain control is achieved by using a linear binary current converter that digitally controls the bias current of the first stage amplifier.

The frequency tunable load determines the center frequency of the overall amplifier gain and the output matching as illustrated in Section 6.2. The frequency tuning with voltage VSW_N (N = 1, 2) can be either analog control with fine resolution or N-bit digital control with frequency band selection capability.

In addition, the proposed tunable amplifier has a power down mode using a digital pin PwrDwn that can de-activate the differential output and dissipate very low leakage dc power. This feature is useful for integrating this tunable amplifier in a low power system-on-chip (SoC) with sleep/stand-by mode. Normally, the stacked amplifier design suffers from head-room limitation that deteriorates the P1dB linearity performance [5.8], [5.21]. However, the limitation of the stacked architecture is minimized by using the high *Q*-factor frequency tunable load and intermediate matching network components resulting in an increased voltage swing with low loss. By using the varactor band selection, the design can cover a wide frequency range with superior gain-flatness while retaining the frequency band switching operation.

5.2. Circuit analysis

The circuit schematic of the proposed frequency tunable amplifier as shown in Figure 5.2 (a) is a stacked fully differential 2-stage common emitter amplifier. The first stage is a variable gain amplifier with inductive load and the second stage is a frequency tunable amplifier.

The circuit in Figure 5.2 (a) is symmetric and can be folded along the vertical axis of symmetry as shown in Figure 5.2 (b). The block depicted as the frequency tunable load is the proposed tunable tank circuit that consists of an integrated 2-coil spiral transformer and the varactor bank. The inductors and the transformer used in the

proposed differential circuit are chosen with center tap configuration to significantly improve the die area utilization. The capacitors C7 and C8 provide the ac ground for second stage differential amplifier. The resistors Rb1 and R3 shown in Figure 5.3 are the base biasing resistors in shunt for the first stage and the second stage amplifiers, respectively. Re-arranging the circuit components, by shorting the dc sources in the half circuit equivalent of the proposed frequency tunable amplifier, shown in Figure 5.2 (b), results in the ac equivalent half circuit shown in Figure 5.3. Based on this ac equivalent half circuit the proposed tunable amplifier is investigated in the following.

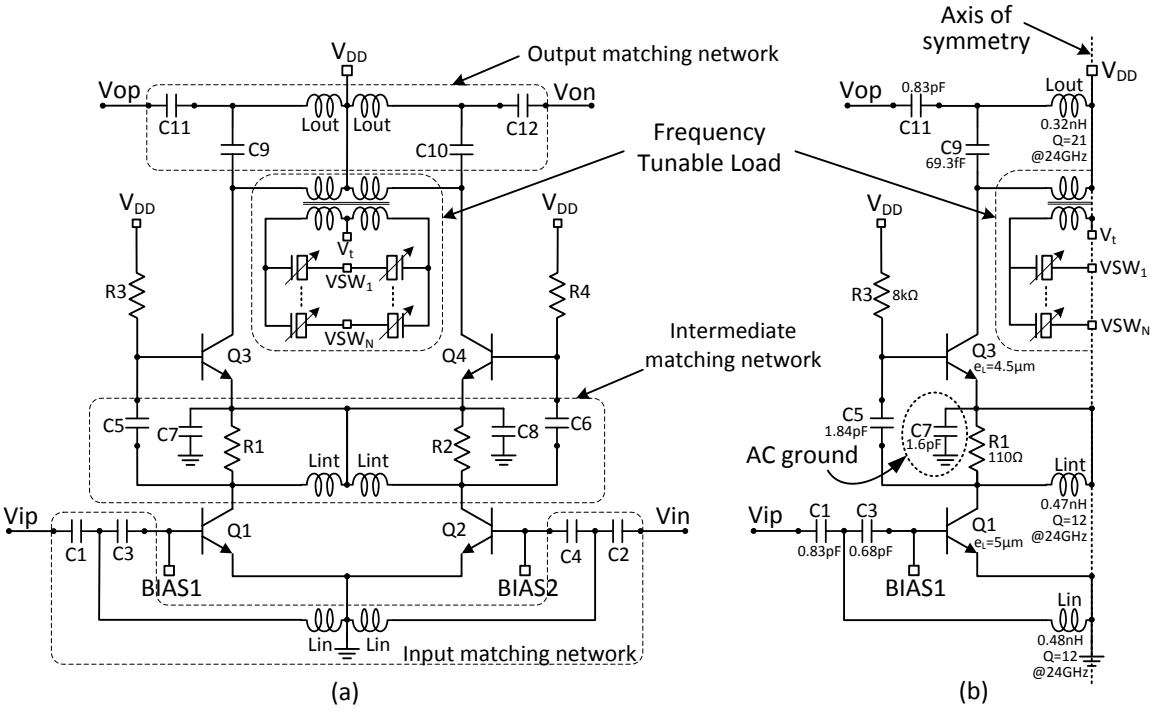

Figure 5.2 Circuit schematic of (a) the proposed *K*-band frequency tunable amplifier (b) half circuit equivalent.

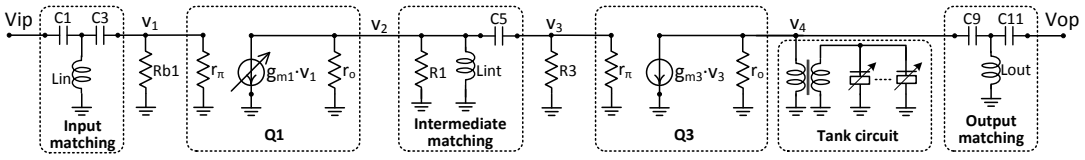

Figure 5.3 Hybrid-π small signal half circuit equivalent of proposed *K*-band tunable amplifier.

By replacing the transistors with the hybrid-π model of the Q1 and Q3 bipolar transistors in Figure 5.2 (b), the small signal equivalent half-circuit of the proposed tunable amplifier is obtained as shown in Figure 5.3.

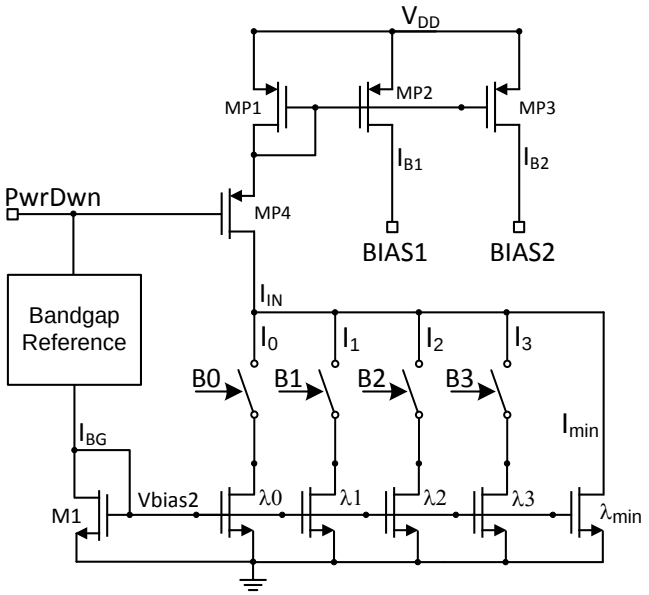

Figure 5.4 Variable gain control base biasing circuit.

5.2.1. Variable gain amplifier stage analysis (A_{v1}):

The output power of the proposed tunable amplifier can be dynamically adjusted by varying the gain of the first stage amplifier using a four bit digital code (B3~B0). Based on Figure 5.3 and Figure 5.4, the gain of the first stage amplifier is given as,

$$A_{v1}(s) = \frac{\beta}{\eta \cdot V_T} \cdot \left[\sum_{n=0}^{3} B_n \cdot I_n \cdot 2^n + I_{\min} \right] \cdot \left[r_{01} \parallel Z_{\text{int}}(s) \right] \tag{5.1}$$

where the transistor forward current gain β, ideality factor η and thermal voltage V_T are indicated for transistor pair Q1 and Q2, I_n (n = 0 to 3) are the constant coefficients of the estimated linear gain function, B_n (n = 0 to 3) are the digital gain control value (received from digital controller or digital baseband) and $I_{\min}$ is the dc current corresponding to minimum gain when all the digital control bits B_n are reset (=

0 V), r_{on} (n = 0 to 3) is output resistance of the bipolar transistors Q1 to Q4 used in this design and $Z_{\text{int}}(s)$ is the intermediate matching network impedance.

From the variable gain control bias circuit shown in Figure 5.4, the mirrored variable biasing currents I_{BT} (T = 1 and 2) has to be matched to avoid offset errors in first stage differential amplifier. Unlike the voltage biasing of amplifiers, the current biasing circuit provides a linear gain control along with the power down (PwrDwn) capability.

5.2.2. Frequency tunable amplifier stage analysis (A_{v2}):

The gain of the second stage amplifier from Figure 5.3 is based on the fixed biasing transconductance (g_{m3}) of the Q3/Q4 transistor pair and the frequency tunable load impedance given in [5.22], [5.23] as,

$$A_{v2}(s) = g_{m3} \cdot \left[r_{03} \parallel Z_L(s) \right] \tag{5.2}$$

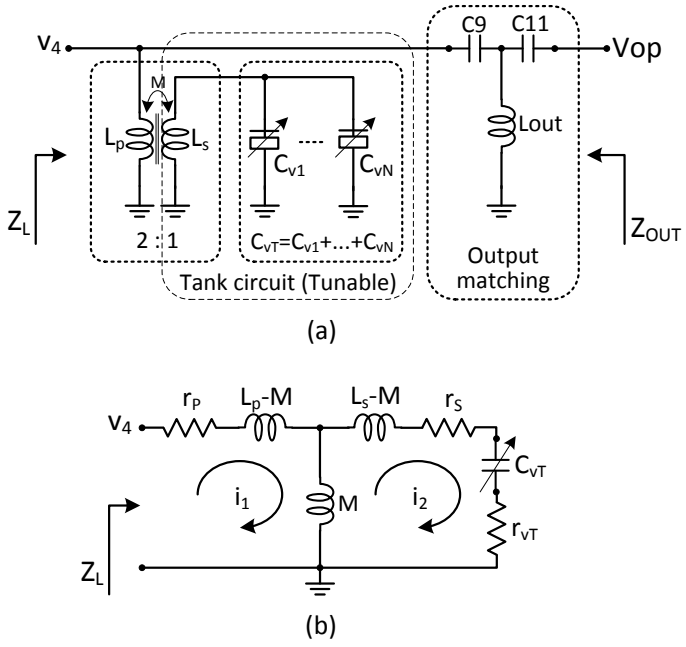

Figure 5.5 (a) Tunable load (transformer and MOS-varactor bank) with output matching network (b) T-section model of transformer with MOS-varactor.

From Figure 5.5 (a), the load impedance of the second stage amplifier is determined by a high *Q*-factor transformer with the primary coil (L_p) magnetically coupled (M) to a LC tank circuit which is built by using the transformer secondary coil (L_s) and the varactor bank (C_{vT}). This load impedance is connected in parallel to the output matching network and the influence of the tank circuit on the output matching is described in the following section. The transformer used in the load circuit can be represented as a T-network based on [5.24] and also the varactor bank can be modeled as a series combination [5.25] of the capacitor C_{vT} and the varactor loss r_{vT} as shown in Figure 5.5 (b). By using loop analysis of the network in Figure 5.5 (b), we obtain the load impedance as,

$$Z_L(s) = \frac{s^3 \cdot \left[\left(L_P L_S - M^2\right) \cdot C_{vT}\right] + s^2 \cdot \left[\left(r_P L_S + r_S L_P + r_{vT} L_P\right) \cdot C_{vT}\right] + s \cdot \left(L_P + r_P \cdot \left(r_S + r_{vT}\right) \cdot C_{vT}\right) + r_P}{\left(s^2 \cdot L_S \cdot C_{vT} + s \cdot \left(r_S + r_{vT}\right) \cdot C_{vT} + 1\right)} \quad (5.3)$$

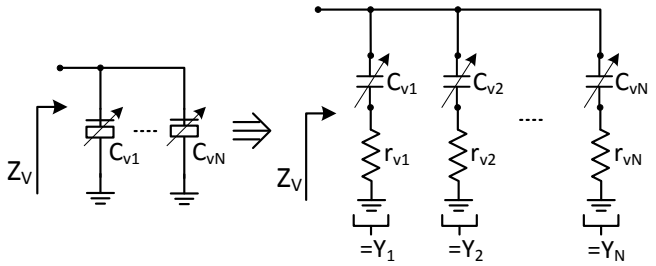

Figure 5.6 Varactor bank with equivalent lumped circuit model.

Varactor bank Q-factor:

The varactor bank, as viewed from the transformer secondary coil (shown in Figure 5.5 (a)), consists of parallel connected variable capacitors with equivalent impedance Z_v. The equivalent lumped circuit model of the varactor bank impedance Z_v, including the varactor parasitic resistance r_{vT} as determined by [5.25] is shown in

Figure 5.6. The varactor bank impedance consisting of N identical varactors is given by,

$$Z_v = \frac{1}{N \cdot Y_1} = \frac{r_v}{N} - \frac{j}{N \cdot \omega \cdot C_v} \tag{5.4}$$

From (5.4), the varactor bank Q-factor is,

$$Q_{CvT} = -\frac{\mathrm{Im}(Z_v)}{\mathrm{Re}(Z_v)} = \frac{1}{\omega \cdot C_v \cdot r_v} = Q_{Cv} \tag{5.5}$$

Based on (5.5) we can deduce that by connecting any number of varactors (N) in parallel for the tunable tank circuit, the Q-factor contribution resulting from the varactor bank is almost fixed.

Q-factor of transformer's secondary coil:

The transformer secondary coil's Q-factor is given as,

$$Q_{Ls} = \frac{\omega_n \cdot L_s}{r_S} \tag{5.6}$$

Q-factor of the overall tank circuit:

For the tunable load's impedance transfer function [5.26], as given in Equation (5.3), we can deduce that,

$$\omega_n^2 = \frac{1}{L_S \cdot C_{vT}} \tag{5.7}$$

$$\omega_n \cdot Q_{tank} = \frac{1}{(r_S + r_{vT}) \cdot C_{vT}} \tag{5.8}$$

where ω_n is the angular resonant frequency and Q_{tank} is the overall Q-factor of the tank circuit.

Equation (5.7) suggests that, by changing C_{vT} using the corresponding varactor tuning voltage VSW_N (N = 1, 2, etc.), the center frequency of the overall amplifier gain frequency response can be shifted.

By re-arranging equation (5.8), the overall tank Q-factor is given as,

$$Q_{tank} = \frac{1}{(r_S + r_{vT})} \cdot \sqrt{\frac{L_S}{C_{vT}}} \tag{5.9}$$

The overall tank *Q*-factor [5.27] based on the individual *Q*-factors of the inductance and the varactor bank is given by,

$$Q_{tank} = \frac{Q_{Ls} \cdot Q_{CvT}}{Q_{Ls} + Q_{CvT}} \tag{5.10}$$

By using (5.5) and (5.6) in (10) we get,

$$Q_{tank} = \frac{\omega_n \cdot L_s}{r_S + r_{vT}} = \frac{1}{(r_S + r_{vT})} \cdot \sqrt{\frac{L_s}{C_{vT}}} \tag{5.11}$$

Equation (5.11) is the same as the overall tank *Q*-factor as determined by (9). The *Q*-factor of the second-stage amplifier response in (5.2) in turn is determined mainly by the transformer secondary coil and the single identical varactor of the varactor-bank. This enables the design to be scalable in frequency along with a voltage controlled tuning range. The noticeable tradeoff is that, as the number of varactors in parallel (N) are increased, they increase the tank minimum capacitance that is limited by $(N \cdot C_{MIN})$ and eventually decreases the operating frequency as well as the frequency tuning range which is illustrated in the following Section 5.3.

Hence, the overall *Q*-factor of the second stage amplifier load is obtained by considering the mutual magnetic coupling due to the in-phase currents of the transformer primary coil and the induced current from the secondary coil shunted with the varactor bank.

By assuming a negligible effect of the large shunt resistors Rb1 and R3 on small signal analysis, the overall tunable stacked amplifier gain (A_v) is determined by the product of the gains of the individual stages that are cascaded as,

$$A_v(s) = g_{m1} \cdot g_{m3} \cdot [r_{01} \parallel Z_{\text{int}}(s)] \cdot [r_{03} \parallel Z_L(s)] \tag{5.12}$$

From Equation (5.12), we can infer that the frequency response of the overall proposed stacked amplifier gain is a function of the tunable varactor control voltage ($VSW_1 = VSW_2 = VSW_N$). This correlation is also established by the simulation gain plot against the tunable voltage (VSW_N) for both the maximum and minimum gain configuration shown in the Figure 5.7. It is evident that the bandwidth increases with increase in center frequency to obtain an overall *Q*-factor that is almost constant and hence results in improved gain flatness over this narrow tuning range of the center frequency.

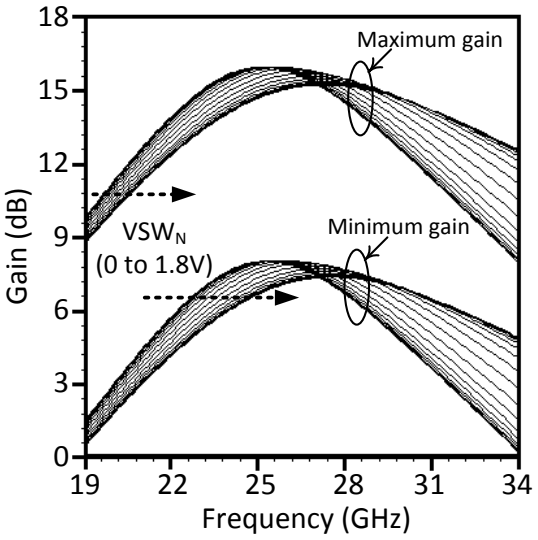

Figure 5.7 Simulated gain of the proposed amplifier based on the frequency tunable voltage VSW_N ($VSW_1 = VSW_2$) varied together from 0 V to 1.8 V (step = 0.1V).

5.2.3. Impedance matching analysis:

The amplifier input and output terminals are impedance matched to 50 Ω by using T-networks as shown in Figure 5.2. The component values of the T-networks are obtained by using a Smith chart. The intermediate matching network is L-network and its passive component values, including the de-*Q* resistors (R1 and R2), are optimized for better overall amplifier performance, such as wide frequency coverage, high gain,

high output power, and linearity. In order to conserve the die area of the proposed differential circuit, the inductors and the load transformer are chosen with center tap configuration. Based on the circuit topology, the input and intermediate matching stage return losses are almost unaffected by tank circuit tuning. However, the output return loss is mainly determined by the output matching T-network as well as the load tank circuit. By using the 2-bit frequency band selection input VSW_N of the tank circuit, an adaptive output matching|S22| is achieved as shown in Figure 5.8. This allows the output matching (|S22|) to be frequency band reconfigurable. The bandwidth for each frequency band is governed by the *Q*-factor (loaded *Q*-factor) of the output matching network over the tank *Q*-factor by considering the design tradeoff between the wide frequency tuning range and the reduced number of tuning bits (N = 2 for our design).

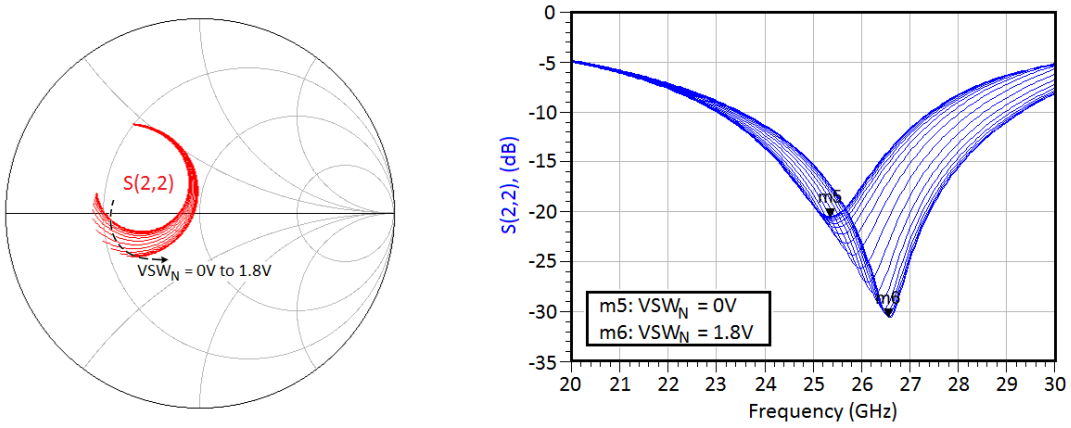

Figure 5.8 Simulation plots of output matching by tuning the tank circuit load with VSW_N (VSW_1 = VSW_2) varied together from 0 V to 1.8 V (step = 0.1V).

The proposed frequency tunable load can be easily implemented and integrated with the existing state-of-the-art amplifiers by taking into consideration of the design aspects discussed in the subsequent Section 5.3.

Frequency tunable load design

The frequency tunable load in the second stage amplifier consists of a 2-coil center tap transformer with a varactor bank connected to the secondary coil as shown in Figure 5.9.

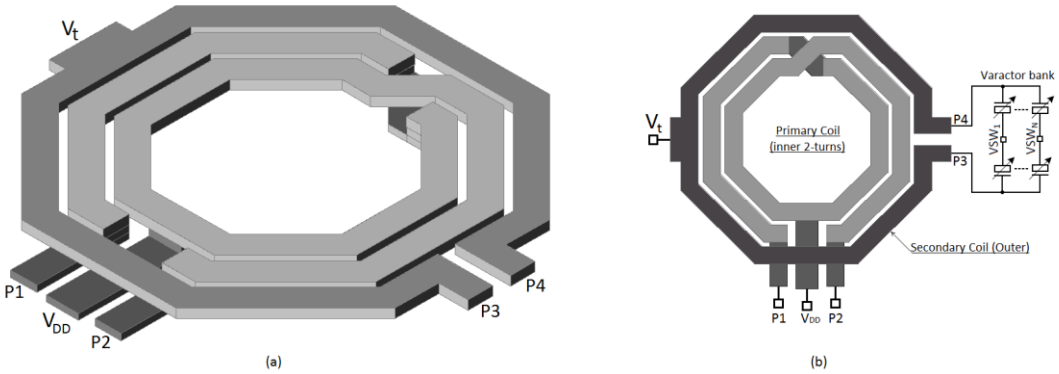

Figure 5.9 Transformer layout (a) 3D view (b) Top view with interface to varactor.

The transformer has the primary and the secondary coils built on the same plane to avoid the formation of large parasitic leakage and mutual capacitance between the vertically stacked coils. The transformer coils are oriented in a non-inverting mode [5.24] and is designed using the top metal supported by the fabrication process for a high *Q*-factor, with a metal thickness of 2.81 μm and a sheet resistance of 10.5 mΩ/□. The varactor bank is connected across the transformer secondary coil between P3 and P4 nodes as shown in Figure 5.9 (b). The transformer primary is the inner planar concentric coil comprising of 2 turns and it is connected to the second stage differential amplifier's collector terminals at P1 and P2. The center tap of the primary coil is connected to the VDD supply that provides the dc power to the entire amplifier. The transformer secondary is one turn, and outer coil with the center tap connected to node V_t. The transformer is designed using Agilent ADS Momentum EM simulator and transformer coil size (114 μm), width (8 μm) and spacing (2 μm) are optimized to meet the desired operating frequency range and *Q*-factor as shown in simulation plots

of Figure 5.10 (a) and (b), respectively. The amplifier *Q*-factor due to the transformer's mutual coupling effect across the primary coil (secondary coil loaded with the varactor bank) is higher than the *Q*-factor of the primary coil with the open-circuited secondary coil based on the EM simulation and is shown in Figure 5.10 (b).

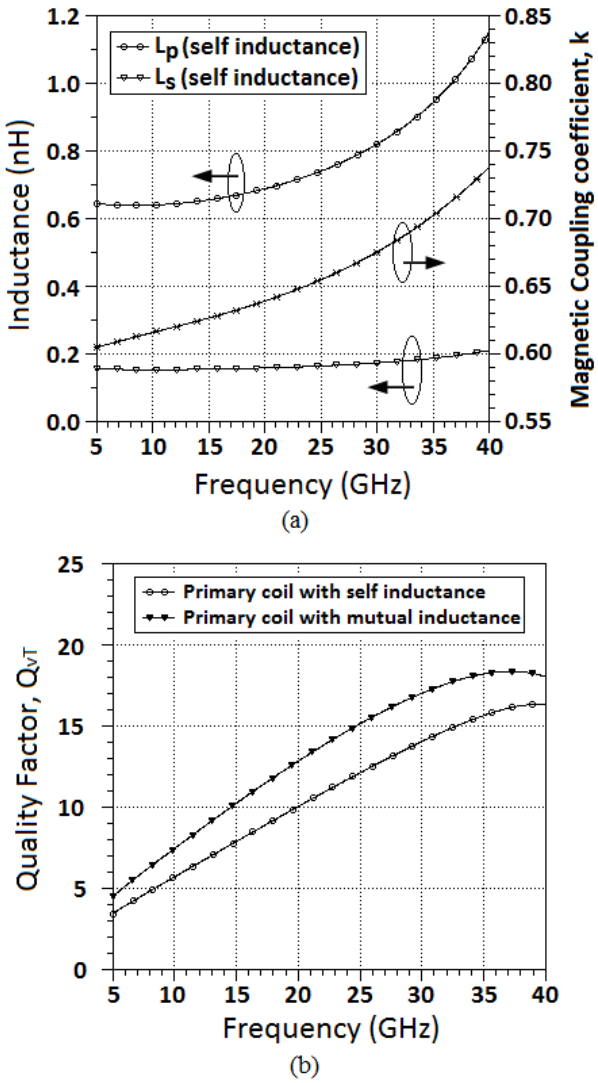

Figure 5.10 EM simulation plots of the designed transformer's (a) primary and secondary inductance with coupling coefficient (b) quality factor looking into primary coil with self-inductance (with secondary coil open) and mutual inductance (with secondary coil connected to the varactors).

The transformer used in the second stage amplifier provides a tuning circuit with additional design flexibility which is achieved by using a strong magnetic coupling.

When compared to a simpler inductor and variable capacitor scheme, the transformer provides an enhanced *Q*-factor at the primary by increasing the effective primary coil inductance given by,

$$L_{p,eff} = L_p \cdot (1+k) \tag{5.13}$$

where ($0.6 < k < 0.75$) is the mutual coupling coefficient as shown in Figure 5.10 (a). The *Q*-factor enhancement due this effective inductance is shown in Figure 5.10 (b). Due to the increased primary inductance by the magnetic coupling, the length of the primary coil can be reduced to provide the same inductance value as a standalone inductance for the circuit in the required frequency range. This reduces electrical resistive loss associated with the primary coil and eventually enhances the *Q*-factor at the primary due to the transformer coupled tank circuit when compared to standalone LC tank as load.

The varactor bank employs parallel connected MOS varactors that are operating in the accumulation mode with the gate-source tuning voltage (V_{gs}) ranging from -0.9 V to +0.9 V to traverse across varactor's C_{MIN} to C_{MAX}, respectively. To avoid negative external tuning voltage, VSW_N (N = 1 and 2) applied at the varactor source/drain terminals, the varactor gate voltage is level-shifted to +0.9 V through the secondary transformer's center tap (V_t) as shown in Figure 5.9. This ensures that the external varactor tuning voltage (VSW_N) to be a positive voltage [5.28] ranging from 0 V to +1.8 V with the capacitance tuning characteristics as shown in Figure 5.11 (a).

The simulation plots in Figure 5.11 (a) and Figure 5.11 (b) are obtained for identical varactors (N as depicted in Figure 5.11 is the number of varactors in the bank) connected in parallel against the same external varactor tuning voltage VSW_N (N = 1 to 4). From Figure 5.11 (a), the equivalent capacitance adds up as the number of identical varactors in parallel increases. An interesting observation noticed in the

varactor bank *Q*-factor plot (Figure 5.11 (a)) is the equivalent *Q*-factor of the varactor bank is unaffected by the number of varactors connected in parallel (*N*). This behavior agrees with Equation (5.5) described in Section 5.2.

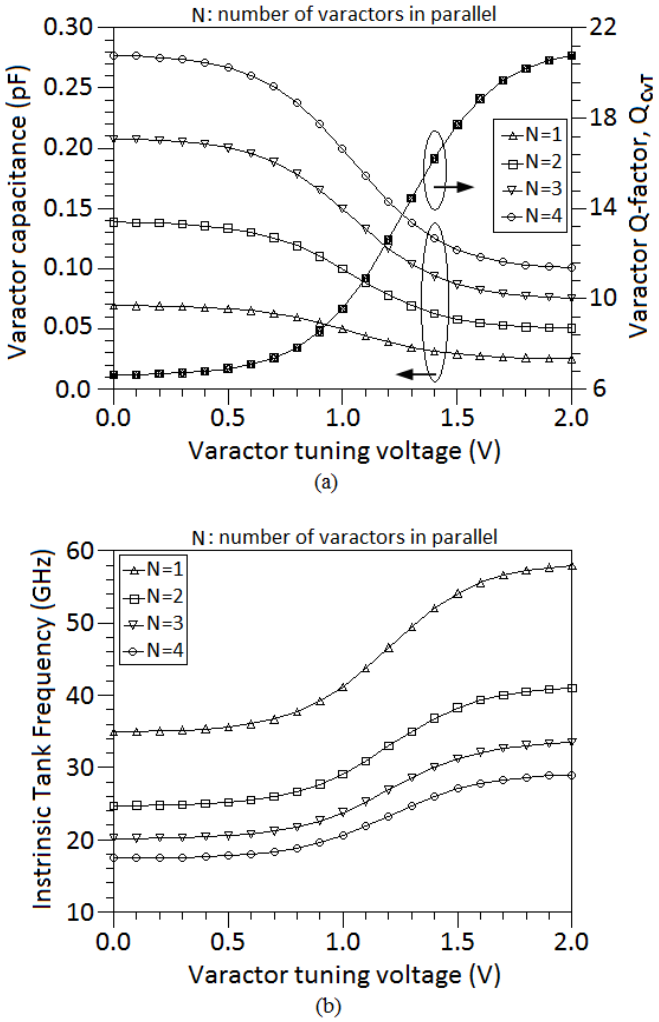

Figure 5.11 Simulation plots of the designed varactor's (a) capacitance and quality factor (b) intrinsic tuned tank frequency.

This is one of the merits of this proposed design and the amplifier operating frequency range can be easily reconfigured based on the number of varactors in parallel (N) as shown by the intrinsic tank frequency plot in Figure 5.11 (b). As the number of varactors (N) in the varactor-bank increases, the trade-off taken into consideration in the design is the shrinking of the tunable frequency range.

5.3. Experimental results

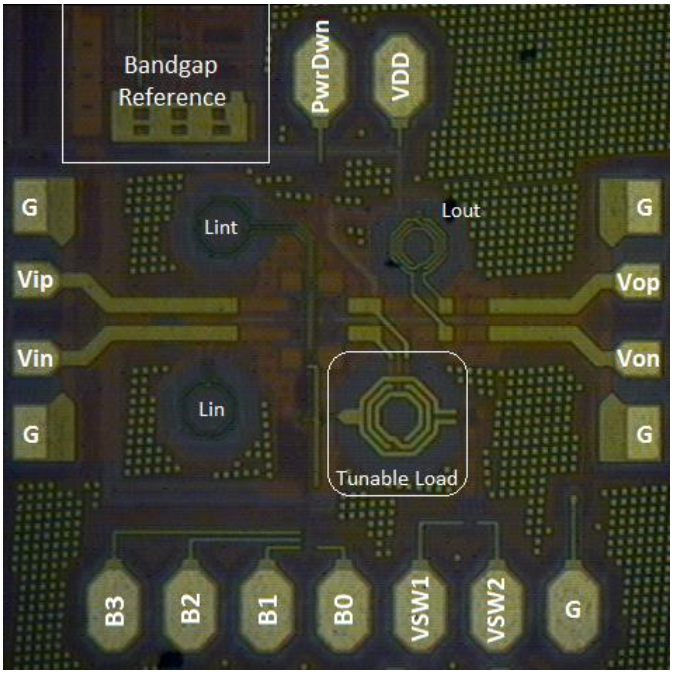

Figure 5.12 Microphotograph of the proposed *K*-band amplifier with tunable load and bandgap reference (Core area: 455 μm × 430 μm).

The proposed *K*-band frequency tunable stacked amplifier is implemented in a 0.18-μm SiGe BiCMOS process from Tower Jazz Semiconductors. The microphotograph of the proposed amplifier and a standard bandgap reference in the fabricated wafer is shown in Figure 5.12 which occupies an overall die area of 0.89 mm × 0.81 mm including the on-wafer probing pads. The proposed design performance is experimentally verified by using on-wafer probing with the Agilent E8364B PNA network analyzer, Agilent E4407B ESA-E series spectrum analyzer and Agilent E8267D vector signal generator. The proposed stacked amplifier consumes a dc current ranging from 7.9 mA to 9.8 mA for maximum to minimum gain variation, respectively during its normal operation mode (PwrDwn = 0 V) and during the *power down* mode (PwrDwn = 1.8 V) dissipates a dc current of 107 μA from a single 1.8 V supply voltage. The gain reduction with increase in bias current is due to the transition

of first stage amplifying transistors (Q1/Q2) from active region (maximum gain) towards saturation region (minimum gain).

The measurement setup consists of wafer probe station with two RF GSSG probes for probing the amplifiers' differential input and output, along with a 7-pin dc probe that provides a 4-bit digital gain control (B_3~B_0) signal along with a 2-bit frequency band selection (VSW_1~VSW_2) input, and a pair of individual dc probes for VDD supply voltage and the *power down* mode control (PwrDwn) as marked in Figure 5.12. The digital pins namely B_3~B_0, VSW_1, VSW_2 and PwrDwn are applied with dc voltages of either 0 V (for bit "0") or 1.8 V (for bit "1").

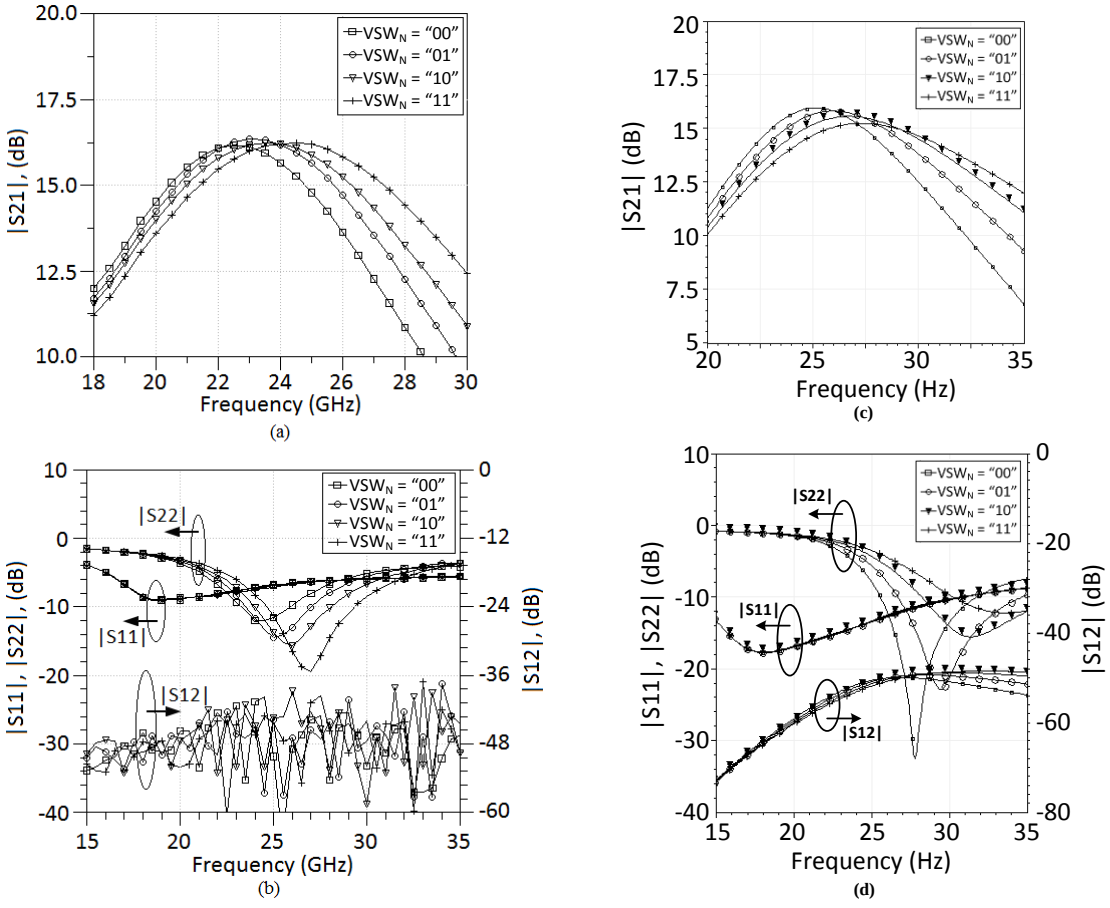

Figure 5.13 S-parameter plots of the proposed tunable amplifier for maximum gain with band switching VSW_N (a) measured gain, (b) measured return loss and isolation, (c) simulated gain, (d) simulated return loss and isolation.

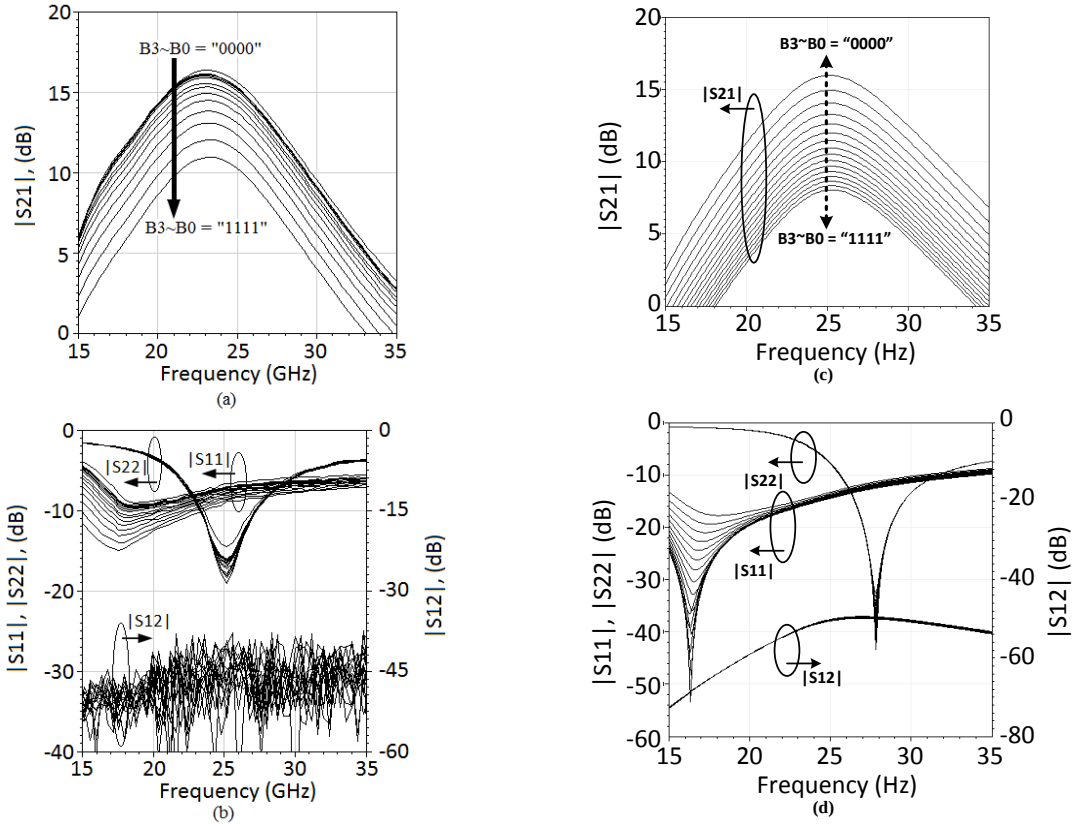

Figure 5.14 S-parameter plots of the proposed frequency tunable amplifier band#1 with gain variation B_3~B_0 (a) measured gain, (b) measured return loss and isolation, (c) simulated gain, (d) simulated return loss and isolation.

The frequency band switching functionality of the proposed amplifier is verified in Figure 5.13 (a) and Figure 5.13 (b) for the maximum gain (B_3~B_0 = "0000") condition and by providing separate digital inputs, to VSW_1 as most significant bit (MSB) and VSW_2 as least significant bit (LSB), together depicted as "VSW_N". The proposed circuit being a frequency tunable amplifier has the total 3-dB bandwidth of the multiple bands as the useful operating frequency range. By providing the option of frequency tuning, the center frequency of the gain response can be changed. For a particular gain setting based on B_3~B_0, the measured frequencies for the 4-bands are listed in Table 5.1. The 3-dB bandwidth for each selected band is wide enough to support the *K*-band standard by selecting band #1 with VSW_N = "00" and the 24 GHz

short range ISM band by selecting band #4 with VSW_N = "11". Similarly, a ±0.5 dB gain flatness is achieved for the frequency ranging from 20.65 GHz to 27 GHz across the four frequency bands.

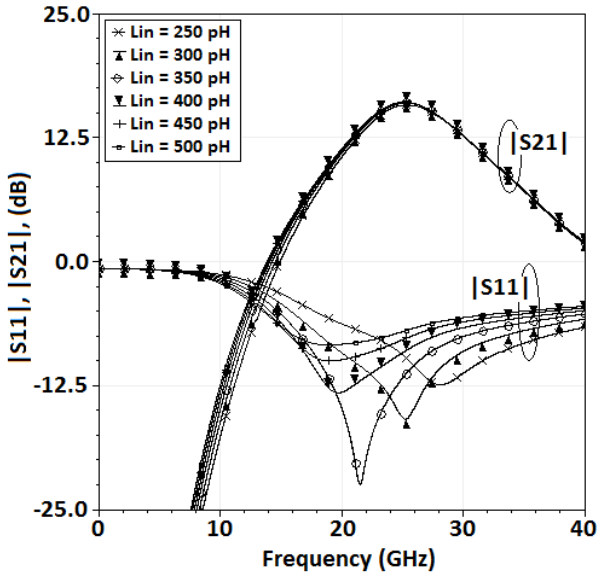

Figure 5.15 Simulated gain and input return loss with variation of input matching T-network's inductance (Lin) from 250 to 500 pH.

The measured input return loss, shown in Figure 5.13 (b) and Figure 5.14 (b), can be improved by circuit optimization of the input matching T-network's inductance L_{in} (shown in Figure 5.2). This is evident from the S-parameter simulation plot shown in Figure 5.15. From Figure 5.15, with a value of L_{in} = 0.3 nH, the minimum |S11| (valley point) shifts to a higher frequency and falls within the proposed amplifier's operating frequency range 18.9 GHz to 29.2 GHz. Hence improving the amplifier's input return loss (|S11| < –10 dB) without significantly compromising on other performance parameters like the amplifier overall gain (with an attenuation less than 0.2 dB) and dc power consumption.

The difference between the simulation and measured results can be attributed to the transistor and varactor model inaccuracy at such high frequencies.

Table 5.1 Measurement results of proposed digital band switching

Band#	VSW1 [V]	VSW2 [V]	Center Frequency [GHz]	3dB Bandwidth [GHz]
1	0	0	22.97	18.9 to 26.3
2	0	1.8	23.72	19.3 to 27.1
3	1.8	0	24.29	19.4 to 28.0
4	1.8	1.8	24.85	19.7 to 29.2

Table 5.2 Performance summary of wideband *K-/Ka*-band drive power amplifiers

Ref.	Technology	Technique / Topology	Frequency [GHz]	Gain [dB]	OP_{1dB} [dBm]	PAE [%]	Power [mW]	Voltage dc [V]	Die area [mm^2]
[5.20]	0.18-µm CMOS	Reverse body bias	24	19	15.7	24.7	-	± 3.6	0.56 × 0.67
[5.17]	0.18-µm CMOS	Driver + 2 parallel PA	20 to 24	16.3	14.3	10.7	-	3.6	0.7 × 0.5
[5.18]	0.18-µm CMOS	Substrate-shielded CPW€	22.9 to 26	7	11	6.5	280	2.8	0.7 × 1.8
[5.3]	0.18-µm CMOS	Darlington + TLT£	18 to 33	15.2	16	10.2	711	3.6	1.41 × 0.61
[5.6]	0.18-µm CMOS	Substrate-shielded MSL¥	27 ± 1.5**	14.5	-	13.2	169.2	1.8	0.7 × 1.2
[5.19]	0.18-µm CMOS	Tuned amplifier	27	17	-	-	300	3	1.2 × 1.7
[5.11]	0.18-µm CMOS	Adaptive bias	20 to 25	11.9	15.4	12	108	3.6	0.83 × 0.48
[5.16]	0.18-µm CMOS	4-way combining PA	24	8	20	20	504	3.6	0.6 × 0.7
[5.10]	0.13-µm CMOS	Class E + mode locking	20	26	-	20.5	52.5	1.5	0.9 × 0.4
[5.13]	0.13-µm CMOS	1-stage push-pull PA	20.5 to 31	8.4	-	13.2	-	1.5	1 × 1
[5.9]	45-nm SOI CMOS	Dynamic bias + stacked	6 to 26.5	6	18.5/22.5	20.5/11	-	4.5/7.2	0.75 × 0.7
[5.7]	0.15-µm pHEMT	Binary combining PA	17 to 35	12	21~22	30~40	498	4	1.5 × 1
[5.4]	0.15-µm pHEMT	High efficiency device	27.5 to 29.5	16	-	37	-	5 to 6	-
[5.14]	0.2-µm SiGe HBT	Transformer + I/O balun	21 to 26	19	18.8	19.75	828	1.8	2.45 × 2.41
[5.15]	0.18-µm SiGe HBT	Driver + 2 parallel PA	16.5 to 28	37.6	15**	22.3	228	2.4	2 × 1
[5.8]	0.13-µm SiGe HBT	1-stage Class F^{-1}/F	24 to 31	10.3	15	40.7	-	2.2	0.6 × 0.45
This work	**0.18 µm SiGe HBT**	**Stacked + tunable load**	**18.9 to 29.2***	**16.3**	**6.7**	**37.7**	**14.2**	**1.8**	**0.89 × 0.81**

Coplanar waveguide€, Transmission Line Transformer£, Micro-strip line¥ * Tunable bandwidth
** Estimated value from the measurement plot

Along with the frequency band switching, the gain control of the proposed amplifier is measured for frequency band #1 (VSW_N = "00") by configuring the amplifier's four gain control bits (B_3 to B_0) as shown in Figure 5.14 (a) and Figure 5.14 (b) with a maximum gain of 16.3 dB (B_3~B_0 = "0000") and a minimum gain of 10.9 dB (B_3~B_0 = "1111"). This digital gain control (B_3~B_0) capability works for all the four frequency bands (using the VSW_N digital setting).

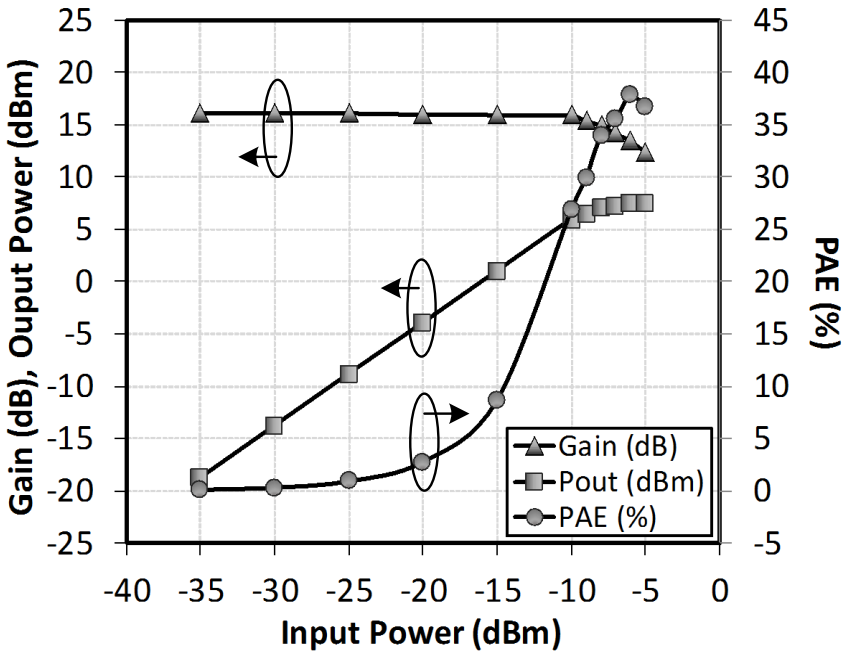

Figure 5.16 Large signal measurement plot of the proposed tunable amplifier at 28 GHz frequency, maximum gain setting, and band #4 (VSW_N = "11").

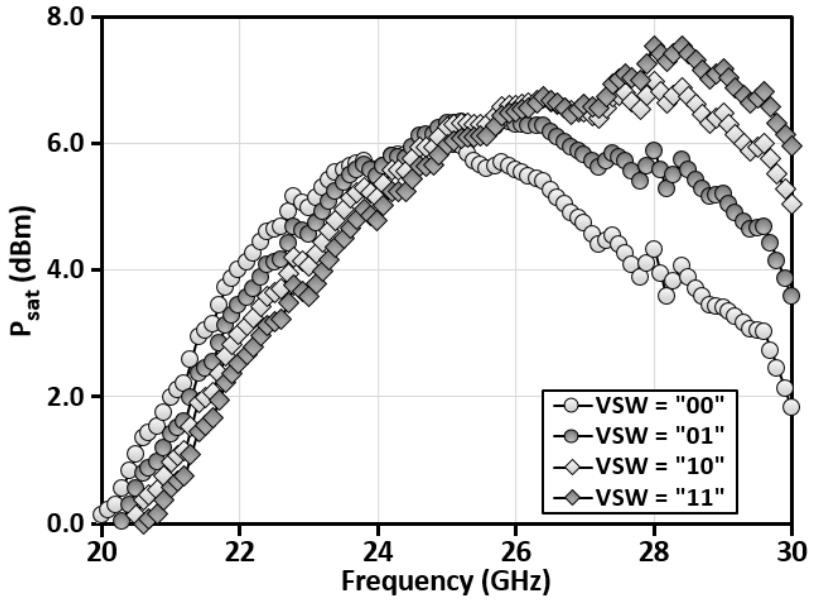

Figure 5.17 Measured saturated power over the four switchable frequency bands based on VSW_N of the proposed tunable amplifier for maximum gain.

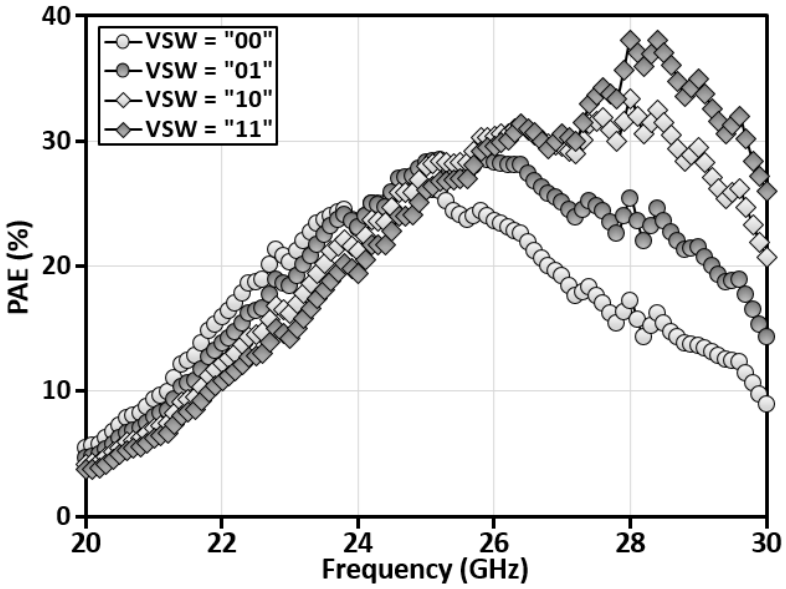

Figure 5.18 Measured PAE over the four switchable frequency bands based on VSW_N of the proposed tunable amplifier for maximum gain.

The high *Q* transformer coupled load of the proposed design provides a high gain and an improved linearity performance together with low dc power consumption, resulting in an improved 37.7% peak PAE at a saturated power of +7.5 dBm. The output 1-dB gain compression point (OP_{1dB}), as shown in Figure 5.16, for the frequency band #4 (VSW_N = "11"), the maximum gain condition (B_3~B_0 = "0000"), and measured frequency of 28 GHz is +6.7 dBm.

The measured P_{sat} and PAE of the proposed tunable amplifier over the four switchable frequency bands based on VSW_N and maximum gain setting (B_3~B_0 = "0000") is shown in Figure 5.17 and Figure 5.18, respectively. Both these plots indicate that the linearity performance is improved for the band #4 (VSW_N = "11") considering the fact that the *Q* of the transformer load increases with increase in frequency.

The performance of the proposed tunable stacked amplifier is consolidated in Table 5.2 and compared with the state-of-the-art *K*- and *Ka*-band monolithic amplifier

designs. By using the stacked architecture along with a high *Q* frequency tunable transformer coupled load and a variable gain control option, the PAE and the overall amplifier performance is improved. From Table 5.2, it is evident that the amplifier's linearity performance (P_{sat} and OP_{1dB}) is directly dependent upon a large supply voltage (increased headroom) and also high dc power consumption that supports large signal swing (as discussed in [5.8]). The PAE performance of the proposed stacked *K*-band amplifier with a 1.8 V supply voltage is comparable to the amplifier designs in [5.4], [5.7] based on the expensive III-V devices that are engineered to provide a high power and high PAE performance.

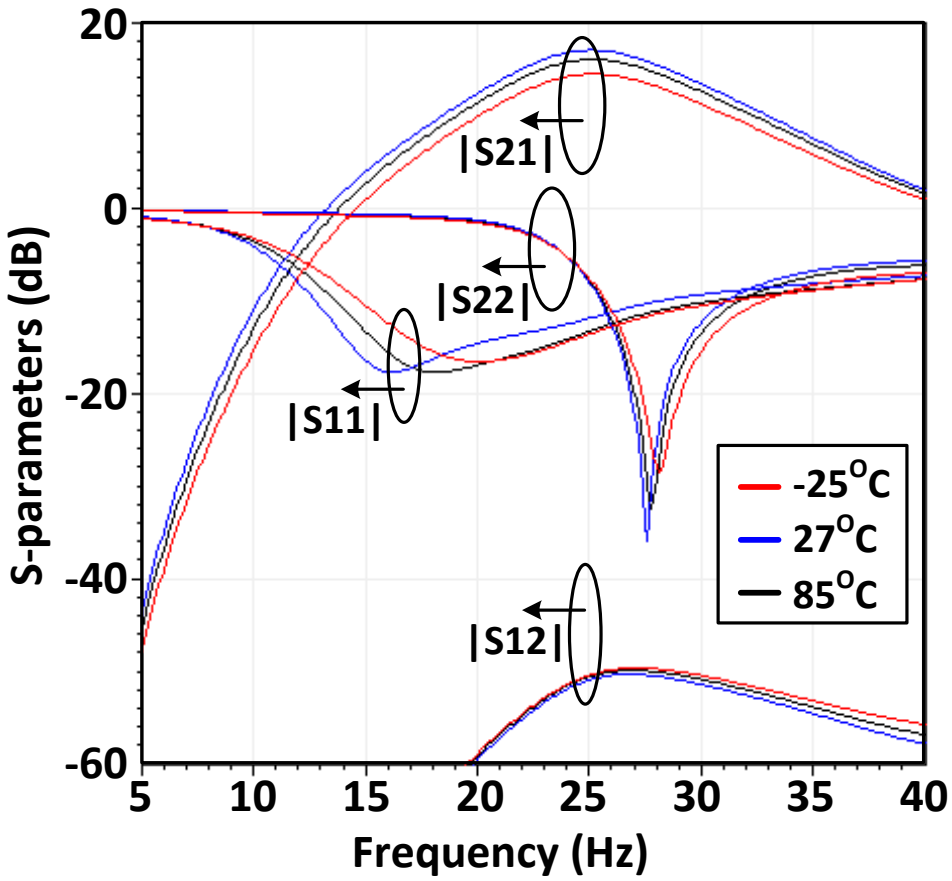

Figure 5.19 Simulated S-parameters of proposed VGA against temperature variation.

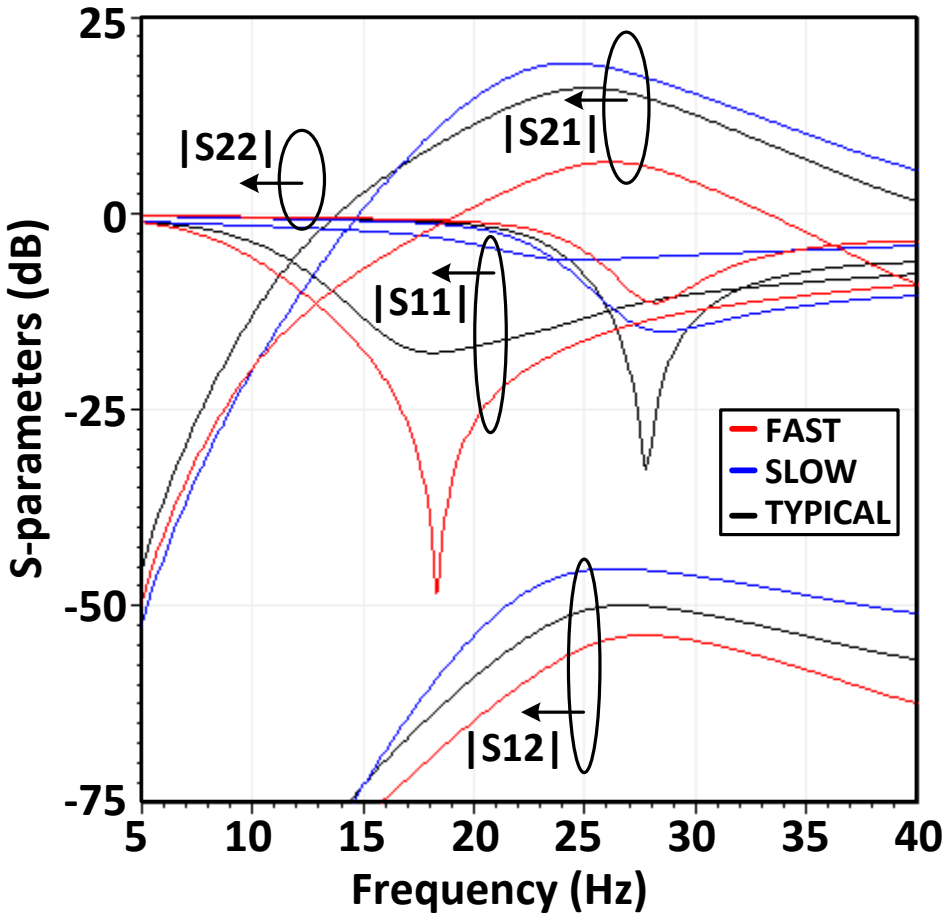

Figure 5.20 Simulated S-parameters of proposed VGA against process variation.

The proposed amplifier achieves a digitally reconfigurable wide bandwidth coverage (from Table 5.1) that can incorporate multiple standards such as the *K*-band (18–26.5 GHz), the LMDS band (27–29.5 GHz), and the 24 GHz short range ISM band (22–29 GHz) with low supply voltage, high PAE, variable gain control, good linearity together with a low power consumption. Hence the proposed tunable amplifier can be integrated in a low power reconfigurable transceiver SoC.

5.4. Summary

This chapter presents a high power efficient broadband amplifier with a variable gain and reconfigurable frequency band capability to support the *K*-band (18–27 GHz) satellite communication and the 24 GHz short range ISM (22–29 GHz) automotive radar applications. The proposed design is aimed at wide range of commercial wireless transceiver applications, taking into consideration the re-configurability of the gain and frequency band with low cost, low dc power and an improved linearity. A detailed design analysis investigating the proposed stacked amplifier for frequency tuning control, input/output matching, the construction and design of the transformer coupled frequency tunable load, and variable gain control current biasing design, is addressed in this chapter. The circuit analysis is verified by on-wafer measurements. The proposed stacked amplifier using a 0.18-μm SiGe BiCMOS technology achieves a 37.7% PAE at the P_{sat} of +7.5 dBm, a 10.9 dB to 16.3 dB variable gain control, and a tunable 3-dB bandwidth from 18.9 GHz to 29.2 GHz.

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Chapter 6. Variable directionality low noise amplifier (LNA)

This chapter, presents a low noise amplifier (LNA) design and is further extended to provide a variable directionality. Such bi-directional amplifiers are mainly used in the compact RF transceivers and a prominent application is the phase array systems used to achieve beam forming and beam scanning in the radar and defense communication systems. One of the options to reduce the transceiver footprint is to combine some of the building blocks operating at similar frequency range of the transmitter and receiver chains and introduce a bi-direction signal flow capability [2.8]. Unlike the passive mixer design that converts frequency between RF and baseband (BB) frequency can be easily implemented which will have conversion loss but can achieve bi-direction frequency conversion capability [2.9]-[2.10]. By some means if the amplifiers at the RF frontend as well as the baseband amplifiers can have bi-directional capability then the overall transceiver can be reduced to a single chain and just by using a digital configuration pin the whole system can operate as either transmitter or receiver [2.11] switched in the time-division-multiplexing scheme. But unlike the passive mixer design, the bi-directional amplifiers (BDA) require active components for achieving amplification which are uni-directional devices. A detailed analysis on the design constrained and the limitation of such BDA are discussed in this chapter based on a design fabricated in 65nm CMOS process.

6.1. Topology and analysis

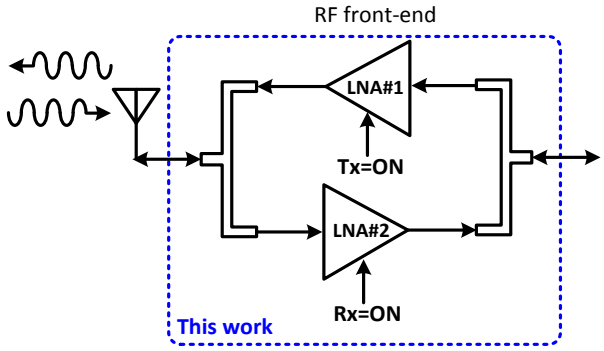

Figure 6.1 Block diagram of the proposed bi-direction low noise amplifier.

The proposed bi-directional amplifier (BDA) comprises of two back-to-back connected low noise amplifiers (LNA) as shown in the Figure 6.1. The complementary switch input signals are provided to the LNA to select the direction of the signal flow. When the BDA is operating in the transmitter mode then Tx = ON activates the LNA#1 to enable signal flow to the antenna, meanwhile the Rx = OFF is set and the LNA#2 is turned OFF. Similarly for the receiver mode the role of LNA#1 and LNA#2 are interchanged. The design consideration for this implementation is to make sure that the interconnects provide low loss as well as mitigates the impedance matching that may result from the ON/OFF states of the back-to-back connected LNAs. Firstly in this chapter we analyze the LNA design and how the switch control can be achieved in the design. Secondly we look into the aspect of designing the interconnect trace that provides low loss and also mitigates the input/output return loss degradations. Finally we provide the measurement results obtained by on-wafer probing that verifies this bi-directional reconfigurability option of the amplifiers.

6.1.1. Literature review of LNA design

The high data rate applications can be achieved by using RF transceivers operating at high frequency and wide bandwidth such as the V-band (40-75 GHz). Many standards are defined at the V-band for applications that use the frequency band from 57 to 64 GHz for unlicensed wireless systems allocated by the Federal Communications Commission (FCC) such as IEEE 802.11ad, ECMA-387, etc.

At such high frequencies (40–75 GHz), the passive components and interconnects in the front-end amplifiers gets transformed by the transistors into negative resistances resulting in severe instability conditions [6.1]. Hence a careful study of such sensitive passive components and techniques of mitigating the formation of such negative resistances becomes critical [6.2], [6.3]. Moreover, such front-end amplifiers must accomplish wideband, enhanced noise performance and power drive capabilities by trade-off with die area, dc power consumption and the supply voltage.

The passive components used in LNA operating at millimeter-wave frequencies can be based on either transmission lines or spiral inductors as discussed in [6.4]. In this design to improve the gain flatness over a wide bandwidth, a common-gate inductive peaking technique is adopted. The performance enhancement is achieved at a trade-off of marginal stability. A low power 60-GHz LNA is demonstrated in [6.5] which employs a 4-stage cascaded CS amplifier with the gate-source transformer feedback technique for the input stage to achieve a simultaneous noise and input matching. Meanwhile, a drain-source transformer feedback is used to achieve enhanced interstage and output impedance matching. Since the design is operated at low power, the gain and linearity performance are affected.

A comparative linearity performance of the power amplifier in [6.6] consumes a larger dc power consumption to achieve a comparable gain compression point. This work uses multiple amplifiers connected by using Wilkinson divider and combiner that increases the die area utilization. To achieve an improved linearity performance in the LNA, built-in linearizer can be included as presented in [6.7]. This design is based on source sensed derivative superposition technique that utilizes large dc power consumption. A bipolar LNA adopting T-type matching network and differential architecture in [6.8] achieves a wide bandwidth and higher gain with an expense of larger dc power consumption. A 3-stage single ended LNA almost covering the wide V-band from 52 to 75GHz is presented in [6.9] which use pi-matching network and source degeneration. This design consumes high dc power with a high supply voltage. In [6.10] a V-band LNA with enhanced bandwidth based on a positively coupled cascade transformer using cascade inductors at the cascade transistor's emitter achieves good noise figure performance at the cost of poor gain and linearity performance.

In this chapter, firstly the stability analysis of the millimeter-wave 3-stage cascode low-noise amplifier (LNA) in CMOS technology is studied. Two implementation prototypes of the same design are fabricated for demonstrating both the extreme conditions of the stability criteria. Additionally, an enhanced figure-of-merit (FoM) determining a better noise and linearity performance is achieved by the proposed design as compared to the state-of-the-art works [6.4]-[6.10].

6.1.2. LNA design details and power down control by V_{bias}

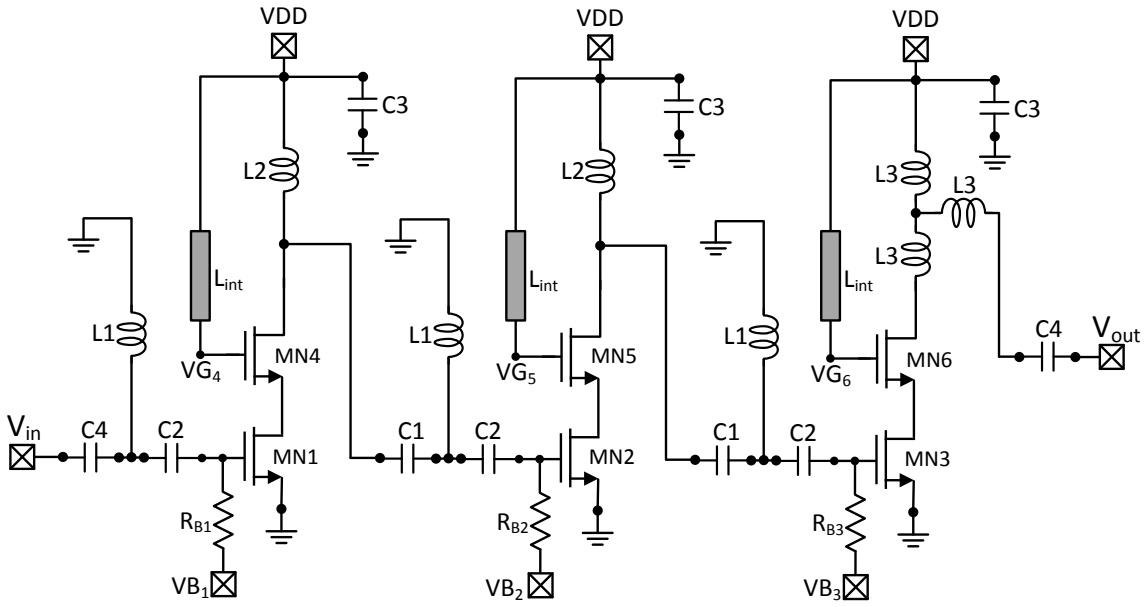

Figure 6.2 Proposed broadband LNA circuit schematic.

The proposed LNA is a 3-stage single-ended cascode amplifier using the NMOS transistors (*MN1~MN6*) and the circuit schematic is shown in Figure 6.2. The design has impedance matching T-networks and the capacitors *C3* are included in the design to bypass the supply-related high frequency noise fluctuations. The bottom transistors *MNx* [*x*: 1~3] are externally biased from VB_X through a high resistance *RBx* while the top transistors *MNy* [*y*: 4~6] are biased by *VDD*. The input and output nodes are matched to 50-Ω impedance. The octagonal inductors *Lx* [*x*: 1~3] are custom-built and modelled by EM simulation using Ansoft HFSS v15.0 as shown in Figure 6.3. The inductors *L1* and *L3* are identical with outer dimension of 63 µm and a width of 6 µm while the smaller *L2* inductor has outer dimension of 52 µm and a width of 6 µm. The inductance and *Q*-factor have less variation around the interested frequency range from 40 GHz to 70 GHz as shown in Figure 6.3 (a).

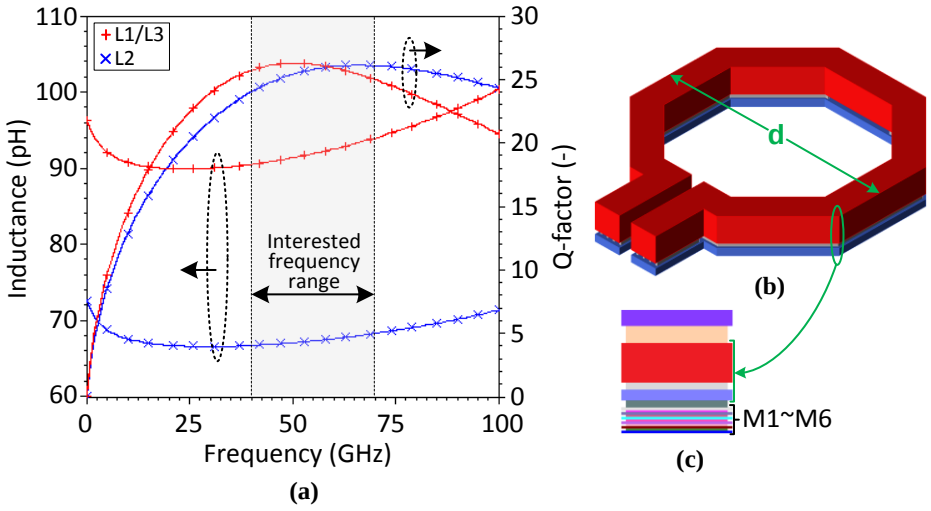

Figure 6.3 (a) Inductance and *Q*-factor of the customized inductors – *L1*/*L3* (d = 63µm, w = 6µm) and *L2* (d = 52µm, w = 6µm), (b) the 3D view, and (c) the metal-stack supported by process technology.

6.1.3. Improved BW, low loss and NF performance of the transmission line

By using Ansoft HFSS v15.0 EM simulator the interconnect transmission line is designed to provide low loss performance. The impedance of this transmission line can be controlled by the dimensions similar to the micro-strip lines. By stacking several metal layers using vertical vias for the signal trace and also similarly stacking some lower metal layers to form the ground plane of the transmission line we can achieve the desired impedance matching as shown in the 3D view of line as Figure 6.4.

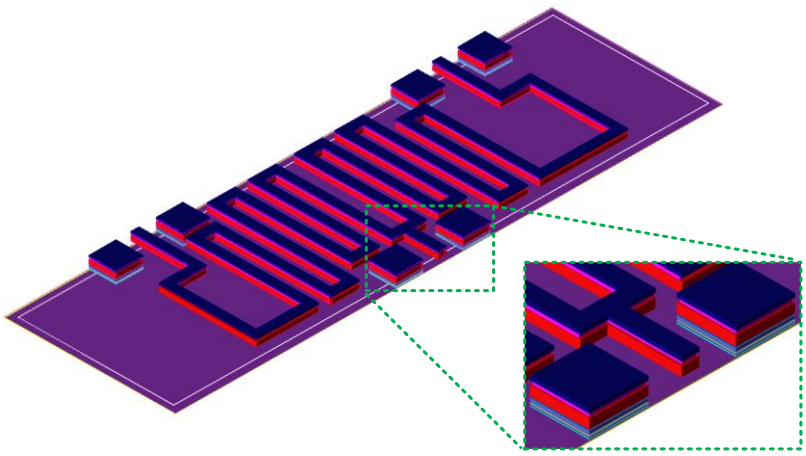

Figure 6.4 Interconnect transmission line (3D-view).

6.1.4. Bidirectional control by Power down control and transmission line design

The impedance of the LNA at the input and output at turn ON and turn OFF conditions differ according to the transistor model parameters. This can be ascertained only by using EM simulation of the passive traces and running S-parameter simulation on the transistor model provided in the PDK from the fabrication house. Based on this the impedance of the combiner transmission line is optimized by adjusting the dimensions mainly the length and width of the signal trace. Since both the LNAs used in the BDA are identical and the combiner transmission line is symmetrical, the final response in either direction will be same as shown in the experimental results.

6.2. Circuit Implementation and experimental results of LNA and the BDA

6.2.1. LNA design

The LNA is fabrication in Global Foundries 65 nm CMOS process with same die area (0.6×0.4 μm^2) as shown in Figure 6.5 (a). By extending the metal stack with vias along the entire interconnect trace from *VDD* pad to the metal-2 *VDD* mesh as shown in the Figure 6.5 (b) results in a parallel low resistance equivalent network. This significantly reduces the voltage drop as well as the trace inductance (L_{int}) from *VDD* to the $VG_{4/5/6}$ nodes. This minimized L_{int} mitigates the formation of negative resistance and hence results in unconditional stability.

The measured *S*-parameter plot agrees well with the simulation as shown in Figure 6.5 (c) and hence verifies the stability condition. The simulated noise figure (NF) specifies a minimum value of 6.2 dB. The stability factors obtained from the measured *S*-parameters highlights that the unconditional stability is achieved by the LNA implementation.

From Figure 6.6, we observe that output 1-dB compression point (OP_{1dB}), output saturation power (P_{sat}), and the peak PAE are +1 dBm, +5.8 dBm and 10.3%, respectively, with a 1.2 V supply voltage at 58 GHz. Furthermore, for a 2.1 V supply voltage the OP_{1dB}, the P_{sat}, and the peak PAE measured at 58 GHz are +6.3 dBm, +9.6 dBm and 16%, respectively.

The measured performance of the proposed broadband LNA is summarized and compared with the state-of-the-art works in the Table 6.1. A FoM taking into consideration the NF, linearity performance and the dc power consumption of the proposed design exhibits a superior performance with the exception of the design in [6.8] and is defined as,

$$FoM[-] = \frac{OP_{1dB}[mW] \cdot FBW[\%]}{(NF_{mag} - 1) \cdot P_D[mW]} \tag{6.1}$$

where, OP_{1dB} is the output 1-dB compression point in mW, FBW is the fractional bandwidth, NF_{mag} is the noise factor and P_D is dc power consumption of the broadband amplifier.

The higher FoM of the design in [6.8] can be attributed to the performance trade-off with differential implementation and higher supply voltage that increases the dc power consumption as well as the die area as compared to the proposed work.

Table 6.1 Performance summary of state-of-the-art 60 GHz wideband LNAs

Reference	Frequency [GHz]	FBW[Γ] [%]	Peak Gain [dB]	NF [dB]	OP_{1dB} [dBm]	Power [mW]	Vdd [V]	Die area [mm²]	FoM [×10⁻³]	Topology [SE[£]/DE[¥]]	Technology
[6.4] RFIC'11	53.4 to 67.5	23.3	21.7	4.9	–8.4	33.6	1.2	1.7	0.48	SE LNA	65nm CMOS
	56.5 to 68.7	19.5	18.1	4	–5	28.8	1.2	0.54	1.42	SE LNA	65nm CMOS
[6.5] MWCL'12	55.2 to 61.2	10.3	12.5	5.4	–4.5*	4.4	1	0.36	3.37	SE LNA	90nm CMOS
[6.6] El. Ltr'12	57 to 64	11.6	13	–	6	44.4	–	0.39	–	SE PA	90nm CMOS
[6.7] IMS'13	55 to 67	19.7	24	4.5	1*	38	1/2	0.26	3.58	SE LNA	65nm CMOS
[6.8] JSSC'13	47 to 77	48.4	22.5	<7.2	4.5[$]	52	2.5	0.5	8.8	DE LNA	0.25µm SiGe
[6.9] El. Ltr'12	52 to 75	36.2	14	4.8	–	32	2	0.22	–	SE LNA	90nm CMOS
[6.10] IMS'14	59 to 67	12.7	13.5	4.4	–6.5	4.8	1.3	0.14	3.38	SE LNA	0.13µm SiGe
This work [A.10]	**47.6 to 67.1**	**34**	**13.7**	**6.2[$]**	**1**	**27.6**	**1.2**	**0.24**	**4.89**	**SE LNA**	**65nm CMOS**

[Γ]fractional bandwidth, *estimated value from the measurement plot, [$]simulated, [£]single-ended, [¥]differential-ended

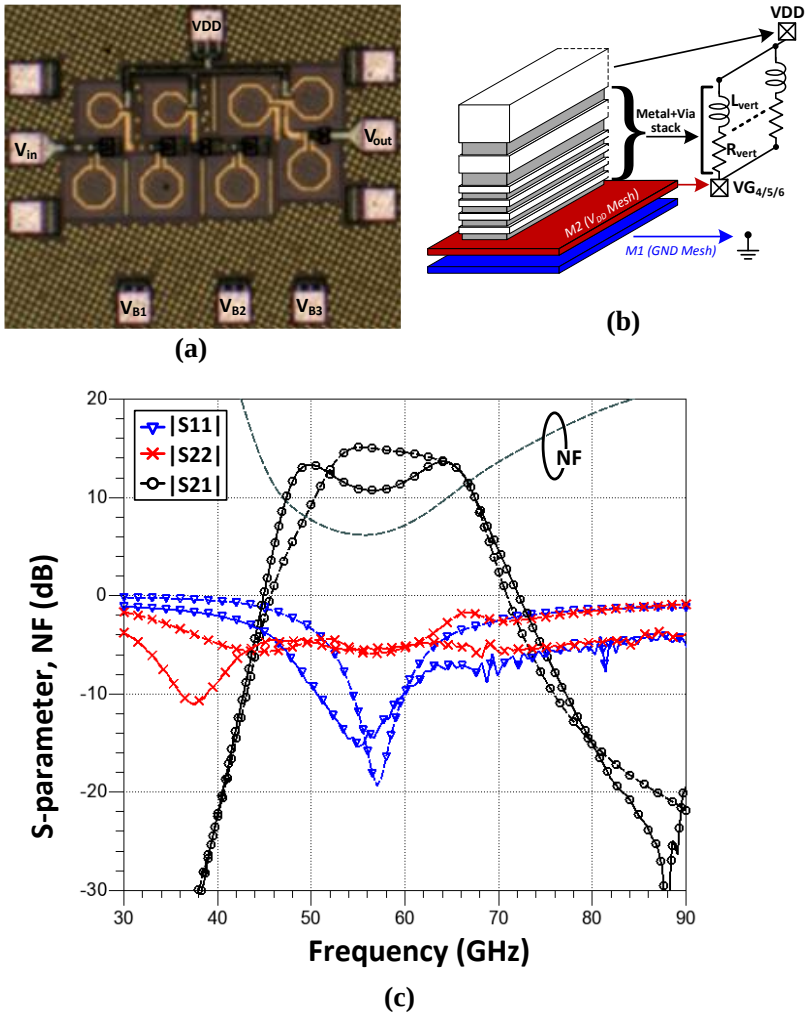

Figure 6.5 LNA (a) die microphotograph (b) interconnect circuit equivalent (c) measured (solid line), simulated (dotted line) *S*-parameters and simulated NF with unconditional stability.

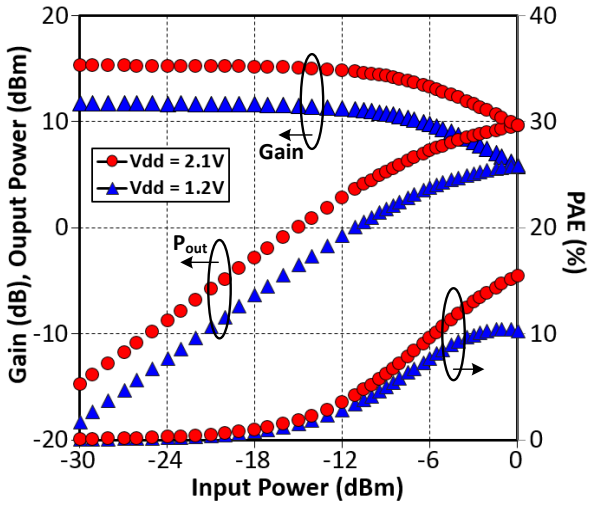

Figure 6.6 Measured linearity performance of proposed LNA implementation.

6.2.2. BDA design

The BDA is also fabrication in Global Foundries 65 nm CMOS process with die area (0.8 × 0.6 μm^2) as shown in Figure 6.7. By using the back-to-back connected proposed LNA design along with the interconnect transmission lines the bi-directional functionality is experimentally verified by switching ON/OFF one LNA while biasing the other LNA in a complementary fashion by using on-wafer probing.

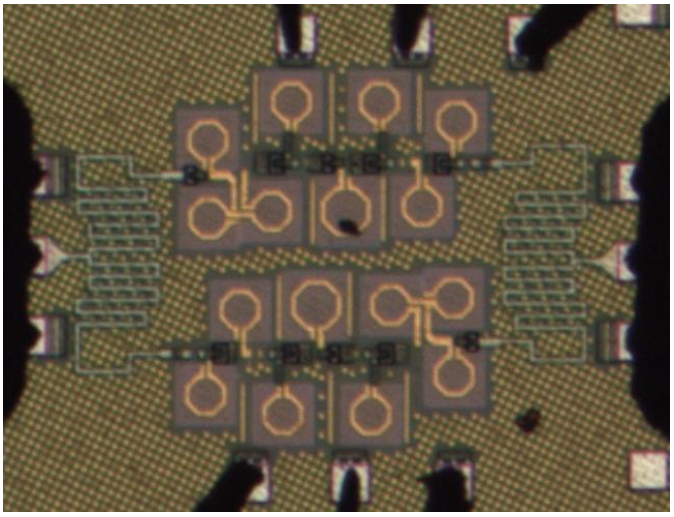

Figure 6.7 Die microphotograph of the BDA.

Based on the simulation and measurement S-parameters as shown in Figures 6.8 and 6.9, respectively the proposed BDA has identical forward and reverse S-parameter characteristics. There is a measured drop in gain of about 2-3 dB as compared to the simulation result which can be accounted for the inaccuracy of the extracted *Q*-factor at such high frequency by the 2.5D EM simulation using ADS Momentum EDA tool.

The measured S-parameters results are shown for both the transmitter (red) and receiver (blue) mode as follows in Figure 6.9. This symmetric result with isolation of about 40dB is achieved between the two modes and the return loss is also not significantly affected and provides the proof of bi-directional reconfigurability of amplifiers. However, the performance of the BDA is degraded from the standalone

LNA design and can be ascertained to the interconnect losses of the transmission lines that needs further optimization.

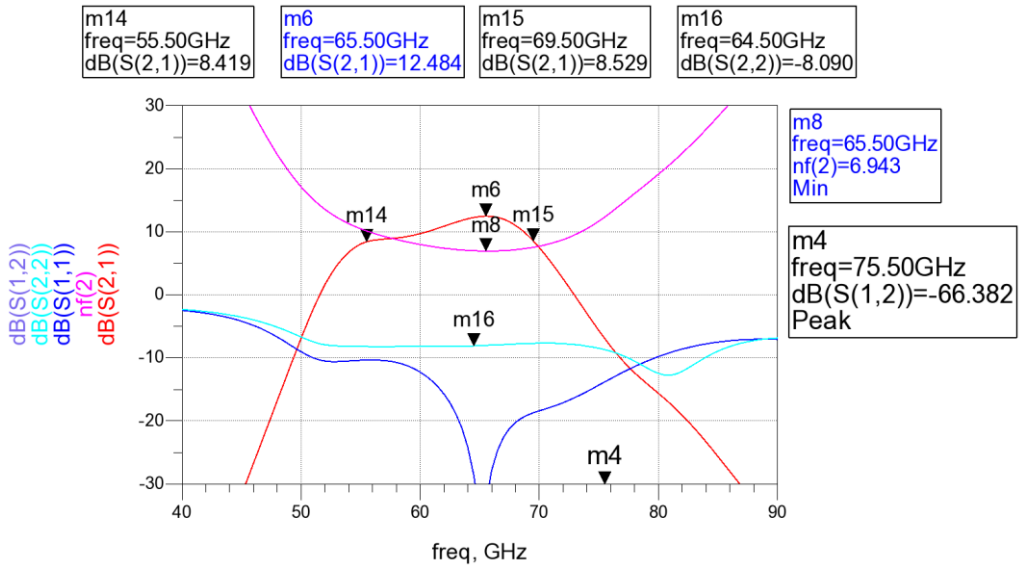

Figure 6.8 Simulated S-parameters and noise figure of the proposed BDA design.

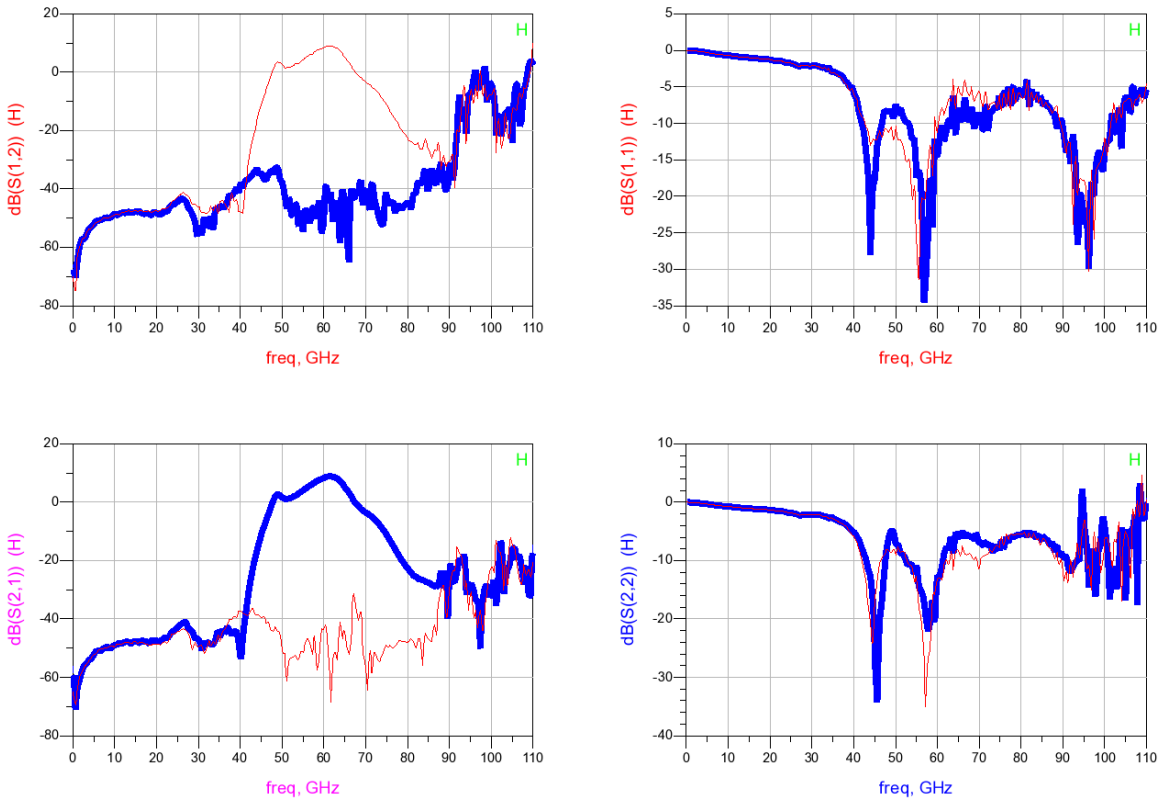

Figure 6.9 Measured S-parameters of the proposed BDA design.

Table 6.2 Performance summary of state-of-the-art 60 GHz wideband BDAs

Parameter	**[6.11]**		**[6.12]**		**This work**
Technology	90 nm CMOS		65 nm CMOS		**65 nm CMOS**
Frequency [GHz]	56.5 to 63*	55 to 66*	54 to 66	56 to 66	**55 to 66**
Peak gain [dB]	20	19	17.8	21.5	**8.6**
NF [dB]	8 to 10*	-	5.6 to 9*	-	**6.8 (Sim)**
S11/S22	-	-	< -10 dB	< -10 dB	**< -8 dB**
Power [mW]	15.6	22.1	13.2	96.2	**18.0**
OP1dB [dBm]	-9	+4	-11.2	-	**-2.0**
Psat [dBm]	+3.5	+7.5	-	+5.6	**-**
Topology [SE£/DE¥]	SE LNA	SE PA	SE LNA	SE PA	**SE LNA**

*estimated value from the measurement plot, $simulated, £single-ended, ¥differential-ended

Based on Table 6.2 we find that the proposed BDA has comparable wide bandwidth, low noise figure, and input/output matching to the state-of-the-art designs. The proposed design does not incorporate SPDT switches has low power consumption and smaller die area of 0.6×0.8 mm^2.

6.3. Summary

The proposed LNA achieves unconditional stability by using layout optimization technique and achieves a peak gain of 13.7 dB, a wide bandwidth of 47.6 – 67.1 GHz, and a dc current consumption of 23 mA from a 1.2 V supply voltage. Moreover, the proposed design simultaneously achieves low noise performance and an enhanced linearity which is quantified by a FoM that is better than the state-of-the-art works. By incorporating this high performance LNA into the BDA design along with an interconnect transmission line results in the bi-directional reconfigurability of amplifiers.

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Chapter 7. Conclusion & Future Work

7.1. Conclusion

In this dissertation, the motivation behind the need for reconfigurable designs along with the various amplifier reconfiguration options are extensively investigated theoretically and the analysis is verified experimentally. Several reconfiguration approaches are proposed by incorporating them in amplifier designs, successfully fabricated the proposed designs and measured by using on-wafer probing.

Besides the conventional amplifier design circuits, several reconfiguration options such variable gain, variable bandwidth, variable center frequency and variable directionality are extensively discussed. In addition to incorporating the reconfigurable options, several design techniques are aggregated to provide a high performance design that are comparable with the state-of-the-art. This thesis will be useful for the RFIC designer working predominantly in the high frequency amplifier design area.

The major contributions reported in this dissertation includes the following,

1) A SiGe BiCMOS based variable gain amplifier topology, circuit schematic design methodology, layout implementation, and measurement procedure are explained in detail. The topology has the advantage of providing a gain control independent input/output matching to 100-Ohm differential impedance. The topology also explains on the enhanced gain-bandwidth product of the cascading amplifier stages by using the proposed interstage network. At the circuit design level a new technique to provide a precise digital gain control with dB-linearity and temperature compensation, with feed-forward high pass filter dc offset cancellation, diode connected transistor load of the output buffer for common mode feedback, transimpedance load of the input fixed gain amplifier for linearity improvement,

current mode biasing to limit the rail-to-rail dc power consumption and to provide the power down mode.

2) A CMOS based VGA with additional reconfigurable bandwidth using tunable on-chip dc offset cancellation is proposed. The problem statement mentioning about the need for such a reconfigurable dc offset cancellation design providing an optimum compromise between the contrasting digital baseband trade-off of BER (bit error rate) and SNR (signal to noise ratio). The design proposes a feedback low pass filter cancellation technique to provide a DCOC that can be bypassed by using a DCOC switchable feedback amplifier. Additionally, using a MOS based RC low pass filter provides a fine tunable option of the DCOC cut-off frequency.

3) A SiGe BiCMOS based frequency band-switchable high efficiency drive amplifier is proposed to signify the amplifier center frequency reconfiguration. By using current reuse technique the design provides biasing that improves linearity of the output drive stage as well as consumes low dc power that provides a better conflict resolution between the contrasting tradeoff of the drive amplifier namely the efficiency and the linearity performance. Additionally, the design incorporates a transformer based tank circuit as the load for the output stage. The tank circuit provides an enhanced Q-factor due to magnetic coupling by using a 2-coil transformer with a varactor bank in the secondary coil. The varactor supports frequency band switching.

4) A bi-directional amplifier using identical low noise amplifier is proposed and implemented in a CMOS technology. Such amplifiers are mainly required for smaller form-factor phase array matrix. By using a low-loss micro-strip transmission line as interconnect between the two amplifiers we can achieve a two port bi-directional amplifier. This design has identical S-parameter characteristics with signal flow in

forward as well as reverse direction as determined by the amplifier biasing. Additionally the amplifier stability improvement by layout technique is illustrated.

The amplifier reconfiguration options as well as the need for several design techniques introduced in this dissertation are mainly driven by the application requirement as well as the constraint of low power design and compact die area specification. Thus making them a suitable options for integration into the "Smart" mobile applications.

7.2. Future Work

As the level of integration for the modern day "Smart" mobile devices like cell phones, tablets, laptops, PDA, etc. against the same or compact form-factor results in the limited silicon die area required for including and implementing the various transceiver blocks to meet most of the standards. Hence a better alternative to alleviate this constraint can be achieved by designing reconfigurable amplifier blocks which have great research potential with many possibilities like the phase shifters using vector modulators, multiple path selection, bi-directional amplifiers, etc.

The motivation for design of the proposed reconfigurable amplifier is to incorporate them into larger system such as,

1) Automatic Gain Control (AGC) closed loop system provides a regulated power level to the following circuit blocks even at the expense of a large input signal variation (dynamic range). The AGC is extended for application such as RF transceivers to provide constant signal strength to the circuitry in digital baseband, even with signal strength fluctuation across the channel between the transmitter and receiver. VGA is the crucial circuit integrated in the AGC that performs the key

function of the gain variation in accordance with the acquired input signal strength. By using this gain control mechanism based on the input signal strength, the AGC sets the output signal strength to a predetermined fixed level.

2) Reconfigurable high performance RF transceiver system are the key for accommodating multiple standards within a same mobile device as well as providing a flexibility to control the performance at various stages of RF transceiver. Such a flexibility can be obtained by incorporating the amplifiers with the proposed reconfiguration options.

3) Reconfigurable smart sensor networks system requires three sections acquiring the required data from sensors, processing them to extract more useful information and finally communication of the information across the network. This requires better control of each node which can be provided by the reconfigurable amplifiers and to operate with low power and small area constraints.

4) The variable bandwidth VGA design provides a reconfigurable solution to the RF transceivers that can support multi-standard baseband interface by switching (reconfiguration) the system topology between the direct conversion receiver (DCR) i.e. zero-IF scheme and the tunable low-IF (superheterodyne) receiver schemes. Furthermore, by using tunable low-IF (superheterodyne) scheme we can achieve a better compromise between the BER and SNR contrasting baseband system requirements.

5) Conventionally the multi-band applications such as the software defined radio (SDR) system has several set of transceivers, each of them operating at different frequency bands. By using software configuration one can switch between these transceivers to shift between the frequency bands. Only one transceiver is operational at a time resulting in design redundancy. This can be overcome by integrating the

proposed variable center frequency VGA in SDR and just by band switching of both the VGA (used as LNA and PA) as well as the VCO we can shift between the various operating bands.

6) Beam-forming by using phase array matrix requires multiple sets of transceivers and the main directional component in the transceiver is the amplifiers. Due to this reason, we need to have duplication of the transceiver chain to work as transmitter and receiver. By incorporating a passive mixer which works as bi-directional component and the proposed bi-directional amplifier we can achieve a whole transceiver as a single chain which is bi-directional. This also reduces the number of antennas in the array by half.

7) One major concern at the product manufacturing stage is the low cost maintenance support. One of the possibility to achieve this is by using on-chip built-in calibration circuits. To support such a feature, the proposed reconfigurable amplifiers can be incorporated in the system and externally controlled to automatically correct post-fabrication errors.

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Research related to this thesis has resulted in following publications:

Journal:

[A.1] **T. B. Kumar**, K. Ma, and K. S. Yeo, "Temperature compensated dB-linear digitally controlled variable gain amplifier with dc offset cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2648–2661, Jul. 2013.

[A.2] **T. B. Kumar**, K. Ma, K. S. Yeo, and W. Yang, "A 35-mW 30-dB gain control range current mode linear-in-decibel programmable gain amplifier with bandwidth enhancement," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3465–3475, Dec. 2014.

[A.3] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A 4 GHz 60 dB variable gain amplifier with tunable dc offset cancellation in 65nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 1, pp. 37–39, Jan. 2015.

[A.4] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A 7.9-mW 5.6-GHz digitally controlled variable gain amplifier with linearization," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3482–3490, Nov. 2012.

[A.5] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A reconfigurable K-/Ka-band amplifier with high PAE in 0.18-μm SiGe BiCMOS for multi-band applications," *IEEE Trans. Microw. Theory Techn.* (Accepted).

[A.6] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A *Ku*-band digitally variable gain LNA with temperature compensation in 0.18 μm SiGe BiCMOS technology," *IEEE Microw. Wireless Compon. Lett.* (Reviewed for resubmission).

[A.7] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A 28.8-/57.6-GHz triple-mode dual-band ring oscillator with controllable second harmonic," *IEEE Trans. Circuits Syst. I, Reg. Papers* (To be submitted).

Conference papers:

[A.8] **T. B. Kumar**, K. Ma, K. S. Yeo, and W. Yang, "A 35mW 30dB gain control range current mode programmable gain amplifier with dc offset cancellation", in *IEEE MTT-S Int. Microwav. Symp. Dig. (IMS 2014),* FL, Jun. 1–6, 2014.

[A.9] K. S. Yeo, **T. B. Kumar**, and K. Ma, "Low power digitally variable gain amplifier techniques based on SiGe BiCMOS technology (Invited Paper)", in *2014 IEEE 12th Int. Conf. Solid-State and Integrated Circuit Technology (ICSICT 2014),* Grand Link Hotel, Gulin, China, Oct. 28–31, 2014.

[A.10] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A low power programmable gain high PAE *K*-/*Ka*-band stacked amplifier in 0.18 μm SiGe BiCMOS technology", in *IEEE MTT-S Int. Microwav. Symp. Dig. (IMS 2015),* AZ, May 16–23, 2015.

[A.11] K. Ma, S. Mou, N. Mahalingam, Y. Wang, **T. B. Kumar**, J. Yan, Y. Wanxin, et. al., "An integrated 60 GHz low power two-chip wireless system based on IEEE 802.11ad standard", in *IEEE MTT-S Int. Microwav. Symp. Dig. (IMS 2014),* FL, Jun. 1–6, 2014.

[A.12] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A compact 60 GHz LNA design with enhanced stability by layout optimization technique in a 65nm CMOS technology", in *IEEE Int. SoC Design Conf. (ISOCC 2015)* (Accepted).

[A.13] **T. B. Kumar**, K. Ma, and K. S. Yeo, "A switch-less low-loss CPW based two port bi-directional variable gain amplifier in 0.18 μm SiGe BiCMOS", in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.* (*ISSCC*) (Submitted).