Design of voltage-controlled oscillators and frequency dividers for 60 GHZ wireless communication applications

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**DESIGN OF VOLTAGE-CONTROLLED
OSCILLATORS AND FREQUENCY DIVIDERS
FOR 60 GHZ WIRELESS COMMUNICATION
APPLICATIONS**

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Abstract

A frequency synthesizer which is used to provide the local oscillation (LO) frequency of a transceiver is a fundamental block in a wireless communication system. For 60 GHz applications, the voltage-controlled oscillator (VCO) and the first-stage frequency divider (FD) are the most challenging blocks of a synthesizer due to their high operation frequency and their significant influence on the overall performance of the synthesizer.

As frequency increases, the trade-offs between phase noise, power consumption, and tuning range of VCO becomes more difficult. In this thesis, firstly, the Q enhancement of multiple-coupled LC -tank has been investigated, mainly for the purpose of designing VCOs with low phase noise under low power consumption for 60 GHz transceivers with a multi-conversion super-heterodyne architecture. Secondly, a Ku-band VCO using dual LC -tanks and transformer-based feedback technique is designed. Thirdly, to cater for the requirement of wide tuning range for 60 GHz applications, a new dual-mode VCO topology with switchable coupled VCO-cores has been proposed to design low phase noise and wide frequency tuning range 60 GHz VCOs.

For the first-stage FD, the injection-locked frequency divider (ILFD) with high division ratio is an attractive solution for mm-wave frequency synthesizers, but normally ILFDs suffer from narrow locking ranges, making them difficult to design for 60 GHz applications. In the thesis, a V-band divide-by-4 ILFD has been proposed. With the special topology involving dual oscillation loops, a wide locking range has been achieved at 60 GHz.

Chapter 1

Introduction

1.1 Motivation

With a typically available bandwidth of 7 GHz (from 5 to 9 GHz) in the world, the unlicensed 60 GHz band provides an exciting opportunity to support the next generation wireless terminals with data rates of Gbps [1-6]. The agreement of regulators throughout the world on the common spectrum, as shown in Figure 1.1 [2], facilitates global productions based on this frequency band and promises a worldwide market. International standards using the 60GHz band such as IEEE802.15.3c, IEEE802.11ad and ECMA-387 have been developed to support various types of applications.

Compared to the 2.4 GHz and 5 GHz band, the 60 GHz band offers a greater bandwidth and allows data rates up to several Gbps [4]. Despite of high path loss at 60 GHz due to oxygen absorption, the 60 GHz band provides extra spatial isolation and higher implicit security, allowing the reuse of bandwidth in two close offices [5]. Moreover, as frequency goes into millimeter wave (mm-wave) region, the signal wavelength is greatly reduced, enabling antennas with compact size and low cost to provide the required gain at the 60 GHz band [6].

Figure 1.1: Worldwide spectrum of the 60 GHz band.

Figure 1.2: 60 GHz applications.

Figure 1.2 depicts the main applications of the 60 GHz band. With data rates of multi-Gbps, file synchronization with gigabytes of data can be accomplished in a few seconds. Peripherals such as hard disks and monitors can be connected to computers through wireless docking. Wireless display, which is a good replacement of video

cables such as HDMI, allows the transfer of display content from portable devices to large screens for better experiences. When used for wireless networking, wireless routers supporting 60 GHz can provide a connection speed that is around 10 times of that of 802.11n at the 2.4 GHz or 5 GHz band.

The silicon based technologies, such as CMOS and SiGe BiCMOS, have offered devices with sufficient speeds to support highly integrated low cost mm-wave circuits. In particular, as the gate length of transistors shrinks into deep sub-micrometer levels below 50 nm, the transit frequency of CMOS transistors reaches hundreds of gigahertz, which is much higher than 60 GHz [7]. Advanced silicon technologies currently have $f_{\max}$ (the maximum frequency of operation) near 325 GHz for high-resistivity silicon-on-insulator (HR SOI) processes and near 300 GHz for CMOS and BiCMOS processes [8].

A frequency synthesizer which is used to provide the local oscillation (LO) frequency of a transceiver plays an important role in 60 GHz wireless communication systems [9, 10]. As the most crucial blocks of a frequency synthesizer, a voltage-controlled oscillator (VCO) and a frequency divider significantly influence the overall performance of a frequency synthesizer. Firstly, the phase noise of VCO and frequency divider dominates the phase noise of the synthesizer output, and thus greatly influences the transceiver's selectivity and signal to noise ratio. Secondly, the operation ranges of VCO and frequency divider determine the output frequency range of the frequency synthesizer. Thirdly, at mm-wave frequency, VCOs and frequency dividers are particularly power-hungry and could occupy the most power consumption of frequency synthesizers. For example, in [11], the power consumption of the divider chain is as high as 74% of the total power consumption of the synthesizer. Therefore, the design of high performance VCOs and frequency dividers is extremely important

to frequency synthesizers. However, the design of VCOs and frequency dividers at such a high frequency involves a variety of challenges.

For VCO design, it is well known that there are trade-offs between the key specifications such as phase noise, tuning range, and power consumption. These trades-offs become very difficult when frequency goes up to the mm-wave region mainly because of the low quality factor (Q) of LC -tank, the decreased gain of transistor, as well as the increased effects of parasitics in the circuit at mm-wave frequency [12]. Thus, new techniques or new topology are needed to overcome those problems and obtain better trade-off between the VCO key specifications. [13] has demonstrated a Colpitts VCO at 76 GHz, however, the tuning range of the VCO is only 4.9% and power consumption is as large as 65 mW. In [14], a 40 GHz VCO based on transmission line has achieved a tuning range of 20%, but it suffers from the major drawbacks of large power consumption and chip area.

For frequency dividers in a synthesizer, the first-stage divider is the most challenging [15], because it needs to operate at the highest frequency of the divider chain and provide wide operation range to support the entire tuning range of VCO. Moreover, as the highest frequency stage of the divider chain, the first stage divider is also the most power-hungry. Therefore, considering the power consumption as well as the chip area, it is attractive to use a high division ratio frequency divider as the first-stage divider [16-18]. An injection-locked frequency divider (ILFD) is a promising solution for the first-stage divider because of its potential for high operation frequency and low power consumption [7], [15]. However, the ILFD inherently suffers from narrow locking range. Many efforts have been made to improve the locking range of divide-by-2 ILFDs, such as using the shunt peaking technique [19] and the frequency tracking technique [20]. Recently, ILFDs with division ratio larger than 2 have been

reported, for instance, the divide-by-3 ILFD in [21], the divide-by-4 ILFD in [22], and the divide-by-5 ILFD in [23]. However, comparing to divide-by-2 ILFD, the locking range of high division ratio ILFD is much narrower due to the low power level of high order harmonic components.

1.2 Objectives

The objective of this thesis is to design high performance VCOs and frequency dividers for 60 GHz wireless communication applications. The targets for VCO design in this thesis are as follows:

- To design low phase noise VCOs with low power consumption.
- To design low phase noise VCOs with wide tuning range

In the frequency divider chain, the first-stage frequency divider which operates at the highest frequency is the most challenging. This thesis will focus on the design of the first-stage frequency divider for 60GHz application, and the design target is:

- To design high division ratio ILFD with low power consumption and wide locking range

1.3 Major Contributions

The major contributions of this thesis are as follows:

The multiple-coupled LC -tank with an arbitrary tank order of N has been investigated. Through theoretical deduction, the Q enhancement of multiple-coupled LC -tank compared with normal single LC -tank has been demonstrated. Besides, the effects of key parameters on the Q enhancement have also been studied. As an application case, a mm-wave VCO with five-coupled LC -tank is designed and

implemented with a 65 nm CMOS technology. The VCO achieves a low phase noise of -107 dBc/Hz at 1MHz offset from carrier frequency of 37 GHz, while consumes only 7.2 mW DC power. The figure of merit (FOM) of the VCO is -189.7 dBc/Hz when taking into account its power consumption and phase noise.

A Ku-band VCO using dual LC -tanks together with feedback is proposed and designed with a 0.18 μm BiCMOS process. A triple-coil transformer is employed to provide strong coupling between the two LC -tanks and simultaneously introduce the transformer-based feedback. The parameters of the transformer have been optimized to provide the required inductance ratios and reduce the unwanted parasitics. The proposed VCO has achieved a low phase noise of -117.4 dBc/Hz at 1MHz offset from a carrier frequency of 12.64 GHz while dissipating a DC power consumption of 4.3 mW on VCO core.

A mm-wave dual-mode VCO topology with switchable coupled VCO-cores has been presented for wide frequency tuning range and low phase noise application. By taking advantage of the different parasitic capacitance of cross-coupled pair when the VCO-core operates at ON and OFF states, the dual-mode operation of VCO can be realized, and the oscillations for both modes can be excited at the lower resonant frequency of the tank, such that tank Q and phase noise performance could be improved for both modes. A strongly coupled transformer with large coupling coefficient (k) is utilized to increase the oscillation stability at the desired resonant frequency for both modes. The large k transformer also facilitates the enhancement of tank Q at the lower resonant frequency. The frequency tuning range of the VCO is increased by properly designing the VCO-cores and combining the frequency bands of the two modes. In addition, the cross-coupled pair of the VCO-core at OFF state is able to act as a high Q active capacitor, which can further increase the tank Q and thus

reduce the phase noise. Implemented in a 0.18 μm BiCMOS process, the VCO exhibits a wide tuning range of 17.2% from 55.7 GHz to 66 GHz, and a low phase noise of -87.5 dBc/Hz to -93.5 dBc/Hz at 1 MHz offset over the entire tuning range.

A V-band wide locking range divide-by-4 ILFD with two coupled positive feedback loops (i.e., an injection-loop and an output-loop) has been proposed. By properly designing the LC -tank, the injection-loop could enhance the third harmonic component to facilitate the fundamental mixing and improve the locking range, while the output-loop could assist the ILFD to achieve stable oscillation at the fundamental frequency and also suppress the third harmonic component at the output, so that allowing a further enhancement of the third harmonic component in the injection-loop. The locking range and design consideration for the proposed ILFD has been analyzed. The ILFD is fabricated in a 65 nm CMOS process and exhibits a wide locking range of 14.9% from 60.2 GHz to 69.9 GHz.

1.4 Organization of the Thesis

This thesis is organized into seven chapters. Chapter 1 gives the motivation, the objective, and the contributions of the thesis. Chapter 2 first gives a brief overview of the basic topology of a PLL-based synthesizer and the synthesizer architectures of 60 GHz transceivers with different frequency conversion schemes, and then studies the fundamentals of VCOs and frequency dividers which are the two most important building blocks of a synthesizer. Chapter 3 begins by examining the multiple-coupled LC -tank and demonstrates its Q enhancement compared with a normal single LC -tank. To verify the theory, a mm-wave VCO using five-coupled LC -tank is designed, implemented and measured. Chapter 4 introduces a Ku-band VCO using dual LC -tanks

and drain-to-source feedback techniques. In Chapter 5, a wide tuning range and low phase noise mm-wave VCO using switchable coupled VCO-cores is presented. In Chapter 6, a V-band wide locking range divide-by-4 ILFD with two coupled positive feedback loops is proposed. Finally, Chapter 7 draws the conclusion and list key research areas for the further investigations.

Chapter 2

Fundamentals of High Frequency Building Blocks in mm-Wave Frequency Synthesizers

The VCO and the first-stage frequency divider which are termed as high frequency building blocks of synthesizers in this thesis are the most challenging blocks when designing mm-wave synthesizers due to their high operation frequency. For 60 GHz transceivers with various frequency conversion schemes, the architecture of synthesizers can also be different. In this chapter, Section 2.1 reviews the basic topology of frequency synthesizers, and also synthesizer architectures for 60 GHz transceivers with various frequency conversion schemes. Section 2.2 presents the theory, the key specifications, and some existing topologies of VCOs. Section 2.3 gives an overview of several typical types of frequency dividers.

2.1 Architectures of mm-Wave Frequency Synthesizers

2.1.1 The topology of a PLL based Frequency Synthesizer

A frequency synthesizer is an essential building block in a wireless transceiver. It is used to generate the local oscillation (LO) signal for up-conversion in a transmitter and down-conversion in a receiver. With negative feedback, a phase-locked loop (PLL) based frequency synthesizer is a control system used to synchronize the phase of the output signal to that of the input reference signal. In the locked status, the phase difference between the output signal and the reference signal is a constant, so that the frequency of them can be synchronized. The block diagram of a simple PLL based frequency synthesizer is shown in Figure 2.1. It consists of a phase/frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a VCO, and a divide-by- N frequency divider chain consisting of a high speed first-stage divider and some low speed subsequent dividers. We separate the first-stage divider from the subsequent dividers in this diagram because the first-stage divider is required to operate as fast as the VCO, and thus its design considerations would be quite different from the subsequent frequency dividers for a mm-wave frequency synthesizer.

As shown in Figure 2.1, the output frequency of the VCO is divided by a series of frequency dividers and then applied to the input of PFD and compared with a reference signal. A PFD is a circuit operates as a frequency detector (FD) if its input frequencies are not equal and as a phase detector (PD) if they are. The using of PFD rather than standalone PD or FD can solve the issue of the limited acquisition range [24]. During the locking procedure, the PFD first acts as a FD to force the frequency of the VCO to

approach to that of the reference signal, and then acts as PD which generates an output proportional to the phase difference of the two inputs.

Figure 2.1: The topology of a typical PLL based frequency synthesizer.

The CP is a circuit that can sink or source current for a limited period of time. It usually contains two switches controlled by the output of the PFD. By charging or discharging the load capacitor, the CP circuit converts the pulse of which the width represents the input phase difference detected by the PFD into a ramp-like signal. This signal is then filtered by the loop filter and applied as the control voltage of the VCO. With the negative feedback, the control voltage of the VCO will change the VCO frequency towards reducing the input phase difference of the PFD, and finally achieves a phase-locked status.

If the overall division ratio of the divider chain is N , the output frequency of the synthesizer is given by

$$f_{out} = N \times f_{ref} \quad (2.1)$$

By changing the division ratio N , different frequencies can be synthesized. Based on the type of frequency division, there are integer- N frequency synthesizers and fractional- N frequency synthesizers. Generally, fractional- N frequency synthesizers are used for high resolution and small channel spacing transceivers, while integer- N frequency synthesizers are used for wideband and lower resolution applications. For

mm-wave, the requirement of frequency resolution is relaxed, thus integer- N frequency synthesizers are usually preferred.

2.1.2 Frequency Synthesizers in 60 GHz Transceivers

The requirement and architecture of a synthesizer is determined by the system specifications. For 60 GHz transceivers, either a direct-conversion architecture or a multi-conversion super-heterodyne architecture can be used. A direct conversion architecture requires a LO frequency of 60GHz, while a super-heterodyne architecture uses LO frequencies lower than 60GHz.

Figure 2.2 (a) shows the general block diagram of a direct conversion transceiver architecture. The conversion between the baseband signals and the RF signal is performed in a single step. This architecture is simple and well suited for integration. However, since the RF frequency is the same as the LO frequency, there is the problem of LO leakage. Moreover, the design of frequency synthesizers at such a high frequency is very difficult. Therefore, some alternative super-heterodyne architectures aiming at reducing the output frequency of synthesizer have been adopted for 60 GHz transceivers [25-29]. As shown in Figure 2.2 (b) and (c), these transceiver architectures can be categorized into two types: direct conversion architecture and dual conversion architecture. Different from the conventional direct conversion architecture, in the direct conversion architecture shown in Figure 2.2 (b), a frequency multiplier is connected to the output of the frequency synthesizer. The use of the frequency multiplier reduces the synthesizer frequency, however, the power consumption of multipliers at these frequencies can be very large.

Figure 2.2: General block diagrams of 60 GHz transceiver architecture: (a) the conventional direct conversion architecture with frequency of synthesizer at 60 GHz, and (b) a direct conversion architecture with reduced frequency of synthesizer (c) a dual conversion architecture with reduced frequency of synthesizer.

The dual conversion architecture with a lower output frequency of synthesizer involves two steps of frequency conversion. The output of the frequency synthesizer is multiplied by M to provide the LO frequency for the first step of frequency conversion, and divided by P to provide the LO frequency for the second step of frequency conversion. By using the two steps of frequency conversion, the frequency of the synthesizer can be reduced without the use of the multiplier (i.e., $M=1$). If the multiplier is used, then the synthesizer output frequency can be further reduced. Since the divide-by- P stage can reuse the high frequency dividers in frequency synthesizer, no additional power consumption is need to produce the LO for the second step of frequency conversion. Due to the good trade-off between system level complexity and robustness, this approach has been proven to be an effective solution for 60GHz transmitters or receivers. Figure 2.3 (a) shows the 60 GHz receiver architecture with $M=1$, $P=2$, which is demonstrated by [27, 28]. This architecture has two stages of conversion but relatively simple structure. The LO frequency is far from the IF frequency and hence less interference. Since the RF frequency is integer multiples of the LO frequency and IF frequency, the harmonics and sub-harmonics may lead to interference issues. The second harmonic of the LO which mixes with the 60GHz RF gives rise to the near IF frequency of 20GHz. This harmonic interference adds on with the down-converted original IF and degrades the performance of the transceiver. Figure 2.3 (b) shows the 60 GHz receiver architecture in [29] with $M=2$, $P=2$. Since the LO for the first step frequency conversion is high, this architecture provides better rejection of nearby interferers and DC offset suppression, thus relaxing the design of channel selection filter. However, the frequency doubler requires additional power consumption, and the design of frequency doubler at such a high frequency may require unconventional circuitry, leading to more design complexity.

Figure 2.3: Examples of 60 GHz dual conversion transceiver architecture: (a) with $M=1, P=2$ and (b) $M=2, P=2$.

2.2 Voltage-Controlled Oscillators

As a key building block, the voltage-controlled oscillator (VCO) has great influence on the overall performance of a synthesizer. The most widely used topology of VCO is *LC*-tank based VCO which is termed as *LC*-VCO due to its simple structure and good performance. Therefore, in this section, after a brief introduction of general oscillator theory in the first part, we present the key specifications of an *LC*-VCO and the design considerations for these specifications. Lastly, the state-of-art topologies of *LC*-VCO are shown.

2.2.1 General Oscillator Theories

The oscillator behavior can be explained by either a feedback model or a negative resistance model [24] as shown in Figure 2.4. The feedback model treats the oscillator as a linear feedback system, while the negative resistance model separates the oscillator into two one port networks (resonator and active circuit) connected to each other.

Figure 2.4: Oscillator models: (a) the feedback model, (b) the negative resistance model.

Considering the simple linear feedback system in Figure 2.4(a), the overall transfer function can be written as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)G(s)}{1 - A(s)G(s)} \quad (2.2)$$

For steady oscillation, the loop gain and phase shift must satisfy the Barkhausen criteria[24]:

- (1) The loop gain, $|A(s)G(s)| \geq 1$.
- (2) The total phase shift around the loop, $\angle A(s) + \angle G(s) = 0^\circ$ or 360° .

By solving the above conditions for oscillation, we can obtain the oscillation frequency and the required gain. In most RF oscillators, $G(s)$ in the feedback loop can be a frequency selective network, which is also called a "resonator". It should be noted that Barkhausen's criteria is necessary but not sufficient [30] for oscillation. For instance, the circuit may latch up rather than oscillate, when the phase shift of the loop equals to 360° and the loop gain is sufficient.

The negative resistance model can be depicted as in Figure 2.4 (b), where the oscillator is divided into two parts: the active circuit and the resonator. The resonator is symbolized as parallel resonant LC -tank consisting of an inductor L and a capacitor C . Generally, the LC -tank determines the frequency of oscillation, while the active circuit provides a negative resistance $-R_n$ to compensate the loss of the resonator (R_p in Figure 2.3(b)) and sustain the oscillation. Once the energy provided by the active circuit is equal to the loss of the resonator, a stable oscillation could be sustained.

The startup condition of the oscillation and the oscillation frequency can be given by

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (2.3)$$

$$|R_n| < R_p \quad (2.4)$$

In practical, R_p is usually designed as three times of R_n to ensure a robust oscillation against process, voltage and temperature (PVT) variations.

(a)

(b)

Figure 2.5: Topology of typical oscillator (a) RC-ring oscillator (b) cross-coupled pair LC oscillator.

For mm-wave frequency, there are two types of oscillators: the resonator-based oscillator and the resonator-less oscillator. RC ring oscillators are a well-known type of resonator-less oscillators. As shown in Figure 2.5 (a), the ring oscillator is always made up of three or more stages of inverters or delay cells with the output feedbacked to the input. The oscillation frequency of a ring oscillator is determined by the delay of each stage. Hence, the oscillation frequency of a ring oscillator can be tuned by varying the delay of each stage [31]. An RC ring oscillator is popular for low frequency low cost application due to its wide tuning range, multi-phase outputs, and

low power consumption. However, the phase noise of ring oscillators suffers from the low open loop Q and the noisy active devices in the signal path [32]. In addition, the frequency of ring oscillator relies on the delay of each stage, thus it is difficult to be applied to mm-wave frequency.

The LC oscillator is probably the most popular resonator-based oscillator. The topology of an LC -VCO with a cross-coupled pair is shown in Figure 2.5 (b). The operation of the LC -VCO can be easily understood by using the negative resistance model [Figure 2.4(b)]. The cross-coupled NMOS transistors provide a negative resistance and add energy into the circuit to sustain the oscillation. The oscillation frequency is determined by the LC -tank. When the added energy is larger than the energy dissipated in the LC -tank, the oscillation can be excited. The start-up condition of an oscillator can be written as

$$g_m \geq \frac{2}{R_p} \quad (2.5)$$

where g_m is the transconductance of the cross-coupled transistors, and R_p represents the parallel resistive loss of the LC -tank. To ensure robust oscillation against PVT variation, g_m is usually designed as three times of $2/R_p$. Similarly, the cross-coupled pair also can be realized using PMOS transistors. With lower flicker noise, PMOS only LC -VCOs may have lower phase noise. However, compared to NMOS transistors, PMOS transistors have approximately half the speed and require a nearly doubled size to achieve the same transconductance. An overview of other popular LC -VCO topologies will be given in Section 2.2.3. With a simple and symmetrical structure, LC -VCOs provide many advantages for high speed and differential designs with low power consumption and reasonable tuning range, making it an attractive solution for mm-wave VCO design.

2.2.2 Key Specifications of *LC*-VCOs

2.2.2.1 Quality factor

Since *LC*-VCOs are based on *LC*-tank, the performance of *LC*-tank is important for the VCO performance. To improve the start-up of oscillation, the loss of *LC*-tank need to be minimized. Quality factor (Q) is usually used to describe the loss of an *LC*-tank. The fundamental definition of Q is from the energy view, which is given by the energy stored divided by the energy dissipated per cycle.

$$Q = 2\pi \frac{\text{Energy stored}}{\text{Energy loss in one oscillation cycle}} \quad (2.6)$$

For the *LC*-VCO shown in Figure 2.5(b), the impedance of the *LC*-tank is expressed as:

$$Z(j\omega) = \frac{1}{\frac{1}{j\omega L} + j\omega C + \frac{1}{R_p}} \quad (2.7)$$

Figure 2.6: Magnitude and phase response of the *LC*-tank.

The magnitude and phase response of the LC -tank is shown in Figure 2.6. It can be seen that the oscillation occurs at the frequency where the phase shift of the LC -tank is zero. The magnitude response of the LC -tank is like the bandpass characteristic of a filter, therefore the Q of the LC -tank can also be defined as the ratio between the center frequency and the 3 dB-bandwidth:

$$Q = \frac{\omega_o}{\omega_{3dB}} \quad (2.8)$$

Since the magnitude response of an LC -tank is easy to obtain from the S-parameter, this definition of Q provides a convenient way to observe the Q of the LC -tank based on the magnitude response of the LC -tank.

Another useful definition of Q is the phase steepness of the oscillator open loop transfer function at the resonance [33]. Considering the oscillator as a feedback system and the phase shift of the open loop transfer function ϕ , the Q is then defined as

$$Q = -\frac{\omega_o}{2} \frac{\partial \phi}{\partial \omega} \bigg|_{\omega=\omega_o} \quad (2.9)$$

In addition to the three different definitions of Q described above, the overall Q of an LC -tank can be expressed by the Q of individual devices in an LC -tank, i.e., the inductor and the capacitor:

$$Q_{Tank} = \frac{Q_L Q_C}{Q_L + Q_C} \quad (2.10)$$

where Q_L and Q_C are the Q of the inductor and the capacitor respectively. This expression has provided the insight into the relationship between the LC -tank Q and the individual devices Q . It can be seen that the device with lower Q will dominate the overall Q of the LC -tank. Generally, when the frequency is low, the Q of a capacitor is much higher than the Q of an inductor. Thus, the loss of capacitors can be ignored, and

the overall Q of an LC -tank is determined by the Q of the inductor. When the frequency is high, such as at mm-wave frequency, the Q of capacitors is comparable or even lower than the Q of inductors, then the loss of capacitors can not be ignored, and the Q of an LC -tank is determined by the Q of both the inductor and the capacitor.

Figure 2.7: The typical structure of an MOM capacitor.

The capacitance in an LC -tank can be divided into two parts: one is the fixed capacitance provided by the linear capacitor, and the other is the variable capacitance which is usually provided by varactors. Most CMOS processes offer linear capacitors in the form of a metal-insulator-metal (MIM) capacitor. Due to the use of top metal, MIM capacitor provides good Q and less parasitic. However, it requires extra masks, and the minimum capacitance of MIM capacitor is usually much larger than the typical capacitances needed for 60 GHz VCOs. Alternatively, another linear capacitor which can be realized with the standard metal layers is MOM (metal-oxide-metal) capacitor. The typical structure of an MOM capacitor is depicted in Figure 2.7. It is composed of a large number of parallel fingers connected to either port of the device. With a combination of fringing capacitance and area capacitance between metal layers, this kind of capacitor features large capacitance but only occupies small area. Though the

Figure 2.8: Admittance transforming technique.

The variable capacitance in LC -tank is usually provided by varactors. Although linear capacitors combined with switches can provide capacitance varied in certain steps to switch frequency band, the continuous frequency tuning of VCO still relies on varactors. The most widely used varactors are MOS varactors. The Q of a MOS varactor and the maximum capacitance variation versus its control voltage are trade-off between each other, which is a major limitation to the design of wide tuning range VCOs at mm-wave. An admittance transforming technique can be used to reduce the load effect of varactor on the overall tank [34], as shown in Figure 2.8. By inserting

inductive elements in series connection with the varactor, the equivalent shunt conductance of the tank can be effectively reduced at higher frequencies, leading to a larger Q of the tank. However, this technique will also reduce the variation of capacitance in LC -tank, resulting in a small tuning range.

Figure 2.9: Typical layout of spiral inductor: (a) octagon and (b) square. (c) Two shunt connected metal layers of inductor. (d) Patterned ground shield

The typical layouts of octagon and square spiral inductor in standard CMOS process are shown in Figure 2.9 (a) and (b). The loss of an inductor is mainly contributed by the lossy substrates and series resistance of winding [31, 35]. Modern CMOS processes offer 4 to 9 metal layers, the top thick metal is usually used for an inductor for less loss on metal and smaller coupling from substrate. In some cases, two

metal layers are in shunt connection to reduce the series resistance of the winding, as shown in Figure 2.9 (c). The substrate loss of inductor can be reduced by using patterned ground shield [36]. Figure 2.9 (d) shows an example of patterned ground shield. The slots are cut into the plane perpendicular to the direction of magnetic current flow, thus the current flow into substrate can be prevented. However, the patterned ground shield would introduce parasitic capacitance to the inductor. Therefore, the ground shield should be placed far away from the inductor. Though the Q of an inductor can be improved by using proper layout technique, the maximum achievable Q is still limited by the process, such as metal thickness and the distance between the top metal and the substrate. Therefore, a method which can improve the inductor Q over the limitation of process is demanded.

2.2.2.2 Phase Noise

Phase noise is probably the most important specification of a VCO. The output of an ideal oscillator is an ideal sinusoidal signal

$$V_{out}(t) = V_0 \cos[2\pi f_0 t + \phi], \quad (2.11)$$

with constant amplitude V_0 , center frequency f_0 , and a fixed phase ϕ . In the frequency domain, it should be a single impulse, as shown in Figure 2.10 (a). However, in practical, there are inevitably fluctuations on signal amplitude and phase. Thus, a real oscillator signal is given by

$$V_{out}(t) = V_0(t) \cos[2\pi f_0 t + \phi(t)] \quad (2.12)$$

In frequency domain, the fluctuations $V_0(t)$ and $\phi(t)$ are transferred into a symmetrical “skirts” shape sideband around the oscillating frequency f_0 [37]. The phase noise is the signal sideband noise spectral density in a unit bandwidth at an

offset of Δf from the center frequency f_0 divided by the carrier signal power. It is defined as

$$L(\Delta f) = 10 \log \left(\frac{P_{\text{noise}}(f_0 + \Delta f, 1\text{Hz})}{P_{\text{carrier}}} \right) \text{ (dBc/Hz)} \quad (2.13)$$

Figure 2.10: (a) Spectrum of ideal and real oscillator. (b) Effect of oscillator phase noise in a receiver.

In a practical oscillator, the amplitude is limited by non-linear active devices and $L(\Delta f)$ is dominated by the phase part of the phase noise [37]. Figure 2.10 (b) depicts the frequency conversion situation in a receiver to describe the importance of phase noise. Supposing there is a large power unwanted signal in an adjacent channel from the wanted signal, and the LO signal used for down-conversion has a noisy spectrum,

then after mixing with the LO, the down-converted spectrum consists of two overlapped spectra because the LO sideband down-converts both the desired signal and the interfering signal. As a result, the desired signal suffers from significant noise. Therefore, stringent phase noise specifications have to be met in wireless communication systems in order to detect the signal accompanied with interferers.

Figure 2.11: Typical phase noise plot.

The phase noise of *LC*-VCO is described by the insightful model first presented by Leeson [38]:

$$L(\Delta f) = 10 \log \left\{ \frac{2FKT}{P_s} \left[1 + \left(\frac{f_o}{2Q\Delta f} \right)^2 \right] \left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|} \right) \right\} \quad (2.14)$$

where K is the Boltzmann constant, F is the excess noise factor, T is the temperature, f_o is the oscillation frequency, Δf is frequency offset, $\Delta f_{1/f^3}$ is the corner frequency between $1/f^3$ and $1/f^2$ phase noise regions, P_s is the power of carrier signal, and Q is the Q of the *LC*-tank. Figure 2.11 plots a general phase noise based on Lesson's phase noise model. There are three regions: $1/f^3$ region, $1/f^2$ region, and flat noise floor region. The phase noise in $1/f^3$ region is declined in a slope of -30 dBc/decade, and is

mainly contributed by AM-PM noise and flicker noise. The $1/f^2$ region is between the $1/f^3$ region and noise floor, and rolls off with -20 dBc/decade. The flat noise floor at large frequency offset is mainly contributed by thermal noise. Since a PLL exhibits a high pass for the noise from VCO, $1/f^2$ region noise usually dominates the phase noise. From Leeson formula, the phase noise of $1/f^2$ region could be reduced by enhancing the LC -tank Q or the voltage amplitude of carrier signal. However, increasing the signal power is usually at the expense of larger power consumption. Thus, the effective way to reduce phase noise should be improving the Q of LC -tank.

2.2.2.3 Tuning Range

The frequency tuning range is the next important specification of LC -VCO. The oscillation frequency of VCO is determined by the tank inductor and capacitor, thus changing either of them could change the oscillation frequency. However, in practical, inductor is difficult to be varied continuously. The normal method for frequency tuning is using varactor. The tuning range of a VCO is defined as

$$TR(\%) = \frac{\Delta f}{f_{center}} \times 100 \quad (2.15)$$

where $\Delta f = f_{\max} - f_{\min}$, $f_{center} = (f_{\max} + f_{\min})/2$. If the inductor is fixed, $f_{\max}$ and $f_{\min}$ are determined by the minimum and maximum capacitances of varactor. Considering the fixed capacitance of LC -tank as C_{fix} , and the maximum and minimum capacitance of varactor as $C_{v\max}$ and $C_{v\min}$, then the equation (2.15) can be rewritten as

$$TR(\%) = \frac{\sqrt{\frac{C_{v\max}}{C_{v\min}} + \frac{C_{\text{fix}}}{C_{v\min}}} - \sqrt{1 + \frac{C_{\text{fix}}}{C_{v\min}}}}{\sqrt{\frac{C_{v\max}}{C_{v\min}} + \frac{C_{\text{fix}}}{C_{v\min}}} + \sqrt{1 + \frac{C_{\text{fix}}}{C_{v\min}}}} \times 200 \quad (2.16)$$

It should be noted that the parasitic capacitance of transistors will contribute to the capacitance of LC -tank and degrade the tuning range. This situation will become even

worse at mm-wave frequency, because the increasing transistors size to sustain oscillation at such a high frequency will inevitably increase the transistors parasitic capacitance, which will further limit the frequency tuning range.

Figure 2.12: 3-bits switched capacitor array.

It is well known that the phase noise of LC -VCO is trade-off with tuning range, mainly due to trade-off between the C_{vmax}/C_{vmin} and Q of varactor. The technique of employing a parallel combination of switched capacitor array for coarse frequency tuning and MOS varactors for fine frequency tuning has been applied to some wide tuning range VCOs [39-41]. An example of frequency tuning scheme with 3 bits switched capacitors array is shown in Figure 2.12. The total frequency tuning range is divided into 8 smaller sub-bands, and each sub-band is covered by the continuously tuning using varactor. Since the required C_{vmax}/C_{vmin} of varactor is much smaller, the Q of varactor can be increased. However, the switches required in this technique would be a large loss at mm-wave frequency. The turn-on resistance of switches will loaded on the LC -tank, decreasing the Q of LC -tank and resulting in a worse phase noise. Although increasing switch size can reduce its turn-on resistance, the large parasitic capacitance of switches would prevent the switch from being turn-off at mm-wave

frequency. Coarse frequency tuning using switched inductors is an alternative way to achieve wide frequency tuning range in mm-wave frequency where the Q of capacitor is low. In [42], switchable inductor is realized by a switchable artificial grounded metal guard ring. However, the special guard ring requires large chip area, and the switches on guard ring actually still are loaded on the LC -tank through magnetic coupling, thus the phase noise of VCO still suffers from the loss of switches.

Figure 2.13: (a) Transformer-based LC -tank, and (b) impedance magnitude of conventional dual-mode VCO with transformer-based LC -tank.

Transformer-based LC -tank with two resonant frequencies can be used for coarse frequency tuning of VCO [43-46], and has been applied to dual-mode wideband mm-wave VCO [47-49]. Figure 2.13 (a) shows a transformer-based LC -tank. In those wideband dual mode VCOs, the oscillation of one mode is excited at the lower resonant frequency of tank, and the other mode is excited at the higher resonant frequency, as shown in Figure 2.13 (b). The dual-mode operation of VCO can be used as coarse frequency tuning, and if oscillation frequency of the two modes and the tuning range for single mode is properly designed, the frequency bands of two modes are possible to form a continuing wideband. This method can extend tuning range, and comparing to single LC -tank with the same component Q , the tank Q at the lower frequency band can be increased. However at the same time, the tank Q at the higher

frequency band will be decreased [45]. Furthermore, to ensure stable oscillation at both the lower and the higher resonant frequency of LC -tank, small coupling coefficient of transformer is required [50], which will in return limit the Q enhancement at the lower frequency band.

2.2.3 LC -VCO Topologies

2.2.3.1 Cross-coupled LC -VCO

The cross-coupled LC -VCO is an attractive VCO topology due to its easy start-up oscillation and simple structure. Beside the NMOS cross-coupled LC -VCO in Figure 2.5(b), there are the other basic topologies as shown in Figure 2.14.

The first topology [Figure 2.14 (a)] utilizes PMOS transistors instead of NMOS transistors as cross-coupled pair to provide negative resistance. It is known that the PMOS transistors are about half as fast as NMOS transistors, and for the same required negative resistance, double width of transistor is needed. PMOS transistors have lower flicker noise, thus use PMOS instead of NMOS will reduce phase noise. The second topology [Figure 2.14 (b)] use both NMOS and PMOS cross-coupled pair to generate negative resistance, therefore, if the requirement of the negative resistance is same, then the power consumption can be reduced by half. However, the voltage swing is limited to the supply voltage. Though the PMOS only cross-coupled LC -VCO and complementary LC -VCO has good phase noise and lower power performance, however, double width of PMOS transistor would bring double parasitic capacitance, resulting in even difficulty design of mm-wave VCO. As mentioned previously, the noise from bias current source can bring disturbs to the voltage at common source node of cross-coupled pair and modulate with the oscillation frequency of the

Figure 2.14: (a) A PMOS cross-coupled LC -VCO, (b) a complementary LC -VCO with current source to ground, (c) a modification of complementary LC -VCO by omit bias current source, (d) a modification of NMOS LC -VCO with tail noise filter.

nonlinear VCO, degraded the close-in phase noise [51]. One direct modification of Figure 2.14 (b) is removing the bias current source, as shown in Figure 2.14(c). This topology omits the use of current source, allowing larger signal swing and eliminating the noise from current source. However, the lack of current source will increase the sensitivity of oscillator to power supply. Another approach to reduce the noise of

current source is illustrated in Figure 2.14 (d), where a noise filter is used in the tail [52]. Despite the use of inductor that would require larger chip area, it can lead to a very low noise bias, leading to low phase noise designs.

Figure 2.15: LC -VCOs with transformer-based feedback (a) drain-to-source feedback, and (b) drain-to-gate feedback.

Transformer-based feedback technique can be applied to cross-coupled LC -VCO to enhance the voltage swing of oscillator and improve the phase noise. Figure 2.15 (a) shows an LC -VCO with transformer-based drain-to-source feedback [53]. This topology allows the drain voltage higher than VDD and the source voltage could be lower than GND. Since the drain voltage is in phase with source voltage, the oscillation amplitude can be enhanced. Consequently, the phase noise would be reduced. Figure 2.15 (b) shows another topology of an LC -VCO with transformer-based feedback, where the NMOS transistors are cross-coupled connected through the transformer-based drain-to-gate feedback. It will bring an advantage that the gate and drain of transistors can be separately biased in DC. By properly design the turn ratio of transformer, the voltage swing at the gate of transistor can be much smaller than that at

the drain. Hence, the voltage swing of VCO output could be increased for same bias current, resulting in an improvement of phase noise.

2.2.3.2 Colpitts VCO

Another category of LC -VCO is Colpitts VCO [54],[55],[56]. Different from the cross-coupled LC -VCO, Colpitts VCO provides negative resistance based on capacitive feedback. The Colpitts oscillator was first proposed in 1920's using only one transistor [57], as shown in Figure 2.16 (a). The operation of Colpitts oscillator can be easily understood by examining the resonance circuit shown in Figure 2.16 (b). By investigating the small signal equivalent circuit, the admittance looking into the gate-drain port of the circuit can be expressed as

Figure 2.16: (a) A traditional Colpitts oscillator, (b) one-port view of Colpitts oscillator, (c) differential common gate Colpitts oscillator, (d) differential common drain Colpitts oscillator.

$$Y_{eq,b} = \frac{-C_1 C_2 \omega^2 g_m}{g_m^2 + \omega^2 (C_1 + C_2)^2} + \frac{j C_1 C_2 \omega^3 (C_1 + C_2)}{g_m^2 + \omega^2 (C_1 + C_2)^2} \quad (2.17)$$

which is equivalent to a negative conductance in parallel with a capacitor. If the negative admittance is large enough to compensate the loss on the tank, the circuit may oscillate. Due to their non-differential structure, the single-ended Colpitts VCOs were rarely adopted as an integrated circuit. The differential common gate and common drain Colpitts oscillator topology are shown in Figure 2.16(c) and (d). The differential Colpitts oscillator shows a good close-in phase noise [58], however, the poor start-up characteristic require high-power dissipation.

Figure 2.17 (a) An improved differential Colpitts VCO with Gate-to-source feedback. (b) A W-band Colpitts VCO.

To ease the start-up condition of traditional differential Colpitts oscillator, [56] combined the cross-coupled LC -VCO and Colpitts VCO, as shown in Figure 2.17 (a). The positive feedback is generated by connecting the gates of $M_{3,4}$ to the gates of opposite switching transistors $M_{1,2}$. The positive feedback enhances the overall small-signal loop gain of VCO, increasing the negative conductance and reducing the start-up current.

The Colpitts LC -VCO is a promising topology for high frequency because of the better performance in terms of phase noise and tuning range at a given bias current[59]. A W-band Colpitts VCO is realized in 0.13 μm BiCMOS technology using the topology depicted in Figure 2.17 (b) [13]. A transformer is used as inductive component in LC -tank at the base of transistor, and providing output for VCO. The inductors connected to emitter provide high impedance path.

2.3 Frequency Divider

A frequency divider is another challenging block in a frequency synthesizer. For the first-stage divider in the synthesizer, its operation frequency should be as high as VCO, and the operation range needs to be larger than the whole tuning range of VCO while its power consumption should be as small as possible. There are several typical types of frequency divider: D-flip-flop (DFF) frequency divider, regenerative frequency divider, and injection-locked frequency divider (ILFD). The DFF frequency divider is subdivided into static and dynamic DFF frequency divider, whereas ILFD consists of RC ring oscillator based ILFD and LC oscillator based ILFD. This section provides an overview of the operation principles and performance merits of above frequency dividers.

Figure 2.18: Topology of a DFF frequency divider with division ratio of 2.

2.3.1 DFF Frequency Divider

A simple divide-by-2 DFF frequency divider is composed of 2 D-latches (master and slave D-latches) in a negative feedback loop, as shown in Figure 2.18. Driven by the anti-phase input clocks, the outputs of slave D-latch are simply cross connected to the inputs of master D-latch to achieve the divide-by-2 function. Depending on the

type of D-latches in the flip-flop, the DFF frequency dividers can be further categorized into static frequency dividers and dynamic frequency dividers.

2.3.1.1 Static Frequency Divider

Static frequency dividers have been widely applied to synthesizer design for its simple realization and robustness. Usually, MOS current mode logic (CML) is adopted for D-latch implementation in a static frequency divider. The CML logic could support high operation frequency because the small voltage swing of CML logic can decrease the rise and fall times. Moreover, the inherent differential configuration of CML logic would reduce the switching and supply noise [60].

Figure 2.19 shows a D-latch based on CML logic. M3 and M4 form the cross-coupled pair to store the signal. The bias current source at the bottom which is used to control the power consumption can be removed for low voltage application. The highest operation frequency is determined by the intrinsic propagation delay of the latch, which can be estimated by

$$f_{\max} \leq \frac{1}{2\tau_{pd}} \quad (2.18)$$

where τ_{pd} is the propagation delay. In CML logic, τ_{pd} is proportional to the charging time constant,

$$\tau_{pd} \propto R_L C_L, \quad (2.19)$$

where C_L is the load capacitance including parasitic capacitance at the output node, and R_L is the load resistance. Obviously, in order to increase the operation frequency, R_L and C_L should be as small as possible. However, if we reduce R_L , then larger transistors are needed to ensure sufficient gain, resulting in an increasing of C_L . On the other hand, if we use smaller transistors to reduce C_L , then R_L has to be increased to provide enough output voltage swing.

Inductor peaking technique which is connecting an inductor in series with resistor to tune out parasitic capacitance at output nodes may be used to increase the operation frequency of CML dividers. However, it is at the expense of reduced operation range, not mention the large area consumed by the additional four inductors.

Figure 2.19: A standard CML D-latch.

2.3.1.2 Dynamic Frequency Divider

Distinguished from the static frequency divider, the D-latches in a dynamic frequency divider is implemented based on dynamic logic of which the current only exists for a part of a clock cycle. True single phase clocking (TSPC) is a common dynamic logic style employed in a frequency divider. Figure 2.20 (a) shows the schematic of a TSPC flip-flop. When CLK is high, the second stage is disabled, and the first stage operates as an inverter, transfers $\overline{D}$ to the input of second stage. When CLK is low, the second stage becomes transparent, and the first latch is disabled, $\overline{D}$ is written to output through two times of inversion, thus making output Q equal to $\overline{D}$. The divide-by-2 operation can be realized by connecting Q to the input D of TSPC flip flop. Figure 2.21 shows an alternative schematic of divide-by-2 TSPC frequency

divider. The advantage of dynamic frequency divider is the lower power consumption. However, it requires rail-to-rail clock swings for proper operation [24]. Moreover, for mm-wave frequency dividers, the main drawback of this class of dividers is the operation frequency limitation due to intrinsic RC delay.

(a)

(b)

Figure 2.20: (a) TSPC flip-flop, (b) TSPC divide-by-2 frequency divider.

2.3.2 Regenerative Frequency Divider

The regenerative frequency divider (RFD) which is also called Miller divider is proposed by Miller 1939 [61]. Figure 2.21(a) shows the operation principle of regenerative frequency divider (RFD) with division ratio of 2, where the RFD is modeled as a feedback loop with a mixer and a low-pass filter (LPF). The output of RFD is mixed with its input, generating two components $f_{in}/2$ and $3f_{in}/2$, if $f_{out}=f_{in}/2$. Through the low-pass filter, the component of $3f_{in}/2$ is filter out, and the component of $f_{in}/2$ persists in the loop. The low-pass filter can be replaced by band-pass filter which is commonly an LC -tank. The parasitic capacitance of mixer could be absorbed by the LC -tank, allowing high operation frequency of RFD.

Figure 2.21: (a) A simple model of RFD, (b) Schematic of a divide-by-2 RFD with gilbert cell.

Figure 2.21(b) shows the schematic of a divide-by-2 RFD with gilbert cell, where the outputs are feedback to the LO ports of the mixer, while the input signals are applied to the RF ports of the mixer. Many research efforts have been made to the regenerative frequency dividers in recent years including the modeling and circuit design [19, 62-64]. The state-of-the-art Miller divider can operate at very high frequency. In [65], the RFDs employing the inductive feedback configuration achieve the locking ranges of 88-104 GHz, 96-111 GHz, and 117–125 GHz in 90 nm CMOS technology.

2.3.3 Injection Locked Frequency Divider

The injection-locked frequency divider (ILFD) is a promising divider type for high frequency applications. The ILFD is based on phenomenon of injection locking where an oscillator does not operate at its self-oscillation frequency, but follows the frequency of injected signal [66, 67].

Figure 2.22: Concept of injection locking in an oscillator.

Figure 2.22 shows the principle of injection locking, where an external sinusoid current is injected into an oscillator. The injection current will introduce a phase shift

ϕ_0 in the loop, which will force the oscillation frequency varied from the resonant frequency ω_0 to ω_1 for providing the phase shift to compensate ϕ_0 [68]. Intuitively, the injection locking could only happen in the frequency closed to ω_0 . The locking range of ILFD can be derived using different approaches [20, 68, 69]. The expression is given by

$$\Delta\omega = \frac{\omega_0}{Q} \frac{I_{inj}}{I_{osc}} \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (2.20)$$

where Q is tank quality factor. If $I_{inj} \ll I_{osc}$, the locking range expression can be simplified as

$$\Delta\omega \approx \frac{\omega_0}{Q} \frac{I_{inj}}{I_{osc}} \quad (2.21)$$

A frequency divider can be realized based on injection locking technique. Figure 2.23(a) shows a divide-by-2 ILFD based on LC oscillator, where an external signal is injected at common mode node of the oscillator. Since the second harmonic is presented at the common mode node, if the frequency of injected signal is close to twice of the self-oscillation frequency, the frequency of oscillator will be locked at half of the injected frequency. Besides LC oscillator, injection locking technique can also be applied to RC ring oscillator to achieve dividing operation. Figure 2.23 (b) shows a divide-by-3 ILFD based on RC ring oscillator. Higher division ratios are possible to be achieved using the similar approach. The locking range of RC-ring oscillator based ILFD is wide, however, since the operation frequency of ring oscillator is limited by the delay of inverter, it can only operate at low frequency.

The LC based ILFD in Figure 2.23 (a) provides a simple structure to realize divide-by-2 operation, however, it has two issues: one issue is that the parasitic capacitance at

the common mode node creates a path to ground, decreasing the effective injected current to the LC -tank, the other problem is that the single-ended injection wastes 50% of the injected power. From the Equation (2.21), either of the problems will result in a degradation of the locking range. If we reduce the bias transistors size to reduce the parasitic capacitance at the common mode point, then the bias current will be reduced.

Figure 2.23: Schematic of ILFDs. (a) Divide-by-2 LC oscillator based ILFD, (b) Divide-by-3 RC oscillator based ILFD.

To improve the locking range of ILFD, new topologies and circuit design techniques have been reported [69-71]. Figure 2.24 (a) shows the topology of a direct injection divide-by-2 ILFD, where the input injection transistor M3 is in the parallel connection with cross-coupled pair. Different from the conventional ILFD in Figure 2.23(a), the injection transistor does not have any bias function, thus the transistor size can be small to reduce parasitic capacitance and the improve injection efficiency. Inductive peaking technique can be utilized to resonate with the parasitic capacitance of injection transistor [70], the direct injection ILFD with peaking inductors is shown in Figure 2.24 (b). The direct injection topology in Figure 2.24(a) can be conveniently

changed to differential injection by adding a PMOS injection transistor, and injecting the differential output of VCO to the gate of the transistor, as shown in Figure 2.24(c).

Figure 2.24: Schematic of an ILFD with (a) direct injection, and (b) direct injection with inductive peaking technique, (c) differentially direct injection.

The injection locking technique can be also used to realize dividers with higher division ratio [16-18, 21-23, 72, 73]. A 70 GHz divide-by-4 ILFD has been reported in [73] with the divide-by-4 ILFD topology in Figure 2.24(a). Different from the divide-

by-2 operation, the input transistor M3 is act as harmonic mixer, and the third-order harmonic of M3 is comparable with the fundamental component. The injection frequency ($4f_0$) mixes with the third-order harmonic of the output ($3f_0$), then the resulted frequency is filtered by band pass filter at f_0 . However, due to the low conversion gain at third-order harmonic of mixer, the divide-by-4 ILFD usually exhibits much narrower locking range compared to the divide-by-2 ILFD.

Chapter 3

Analysis of Multiple-Coupled *LC*-tank and its Application to Low Phase Noise VCO Design

Despite of many advantages of 60 GHz unlicensed bands, designing a VCO directly operating at 60 GHz is challenging. Due to the low Q of varactors and the reduced gain of transistors at 60 GHz, the trade-offs between those VCO key parameters, such as phase noise, tuning range and power consumption become more difficult than that at the lower frequency. Fortunately, heterodyne architecture with multi-conversion can be used for 60 GHz transceiver, thus the VCO frequency can be lower than 60 GHz. The lower LO frequency can greatly reduce the design difficulty of the frequency synthesizer and allows better trade-offs between VCO key performances. In [74], a dual-conversion heterodyne architecture with LO frequency at 36 GHz has been proposed for a 60 GHz transceiver.

A transformer can be used as a substitute of inductor in an *LC*-tank [43-45, 75-80]. However, in the previous works with the transformer-based *LC*-tank, the orders of transformers are limited to three. It is well known that the standard RF CMOS process usually can provide 6-9 metal layers, which is possible to support the transformer with

higher order [78]. Therefore, it is needed to give the design formulas for the high order transformer-based LC -tanks. To this end, in this chapter, the multiple-coupled LC -tank with N -coil transformer has been analyzed theoretically. Then, as an application example, a low phase noise 36 GHz VCO which can be used for the dual-conversion heterodyne architecture in [74] is designed with five-coil transformer. Section 3.1 has investigated the multiple-coupled LC -tank with tank order of N . With the theoretical deduction, the enhancement of the effective Q of the multiple-coupled LC -tank is demonstrated. In Section 3.2, the multiple-coupled LC -tank has been applied to a mm-wave frequency VCO with five-coupled LC -tank. The summary is given in Section 3.3.

Figure 3.1: Topology of (a) single LC -tank, and (b) multiple-coupled LC -tank.

3.1 Analysis of Multiple-coupled LC -tank

Figure 3.1 shows the topology of single LC -tank and multiple-coupled LC -tank. The multiple-coupled LC -tank consists of multiple single LC -tanks with coupling from each other. The couplings between those LC -tanks are provided by multi-coils transformer composed of the inductors of single LC -tanks. For the purpose of deduction, we use N to represent tank order which is the number of single LC -tank in the multiple-coupled LC -tank topology. The effective Q of the multiple-coupled LC -tank can be calculated from the impedance looking into the primary LC -tank (i.e., the LC -tank directly connecting to cross-coupled pair).

Figure 3.2 shows the equivalent model for multiple-coupled LC -tank. To simplify the calculation and facilitate the comparison with single LC -tank, we assume each coil of transformer in the multiple-coupled LC -tank has identical self-inductance equal to L/N , i.e., $L_1=L_2=\dots=L_N=L/N$, and the capacitors in the multiple-coupled LC -tank are also identical and equal to C , i.e., $C_1=C_2=\dots=C_N=C$. The parasitic resistance of each coil of the transformer is modeled by a resistor, and the resistance is assumed be proportional to the self-inductance, which is close to its physical situation [35].

Figure 3.2: Simplified equivalent model for multiple-coupled LC -tank.

If the coupling coefficients between any two individual tanks are the same, the mutual inductance of transformer can be written as

$$M_{ij} = k\sqrt{L_i L_j} = \frac{kL}{N} \quad (3.1)$$

where k is the coupling coefficient. As denoted in Figure 3.2, $i_{1,2,\dots,N}$ is the currents on each coil of the transformer, and $V_{1,2,\dots,N}$ is the voltage drop on each tank. Based on V-I equations of transformer, the relationship of $i_{1,2,\dots,N}$ and $V_{1,2,\dots,N}$ can be given as

$$\begin{bmatrix} \frac{R}{N} + \frac{Ls}{N} & \frac{kLs}{N} & \dots & \frac{kLs}{N} \\ \frac{kLs}{N} & \frac{R}{N} + \frac{Ls}{N} & \dots & \frac{kLs}{N} \\ \dots & \dots & \dots & \frac{kLs}{N} \\ \frac{kLs}{N} & \frac{kLs}{N} & \dots & \frac{R}{N} + \frac{Ls}{N} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \dots \\ i_N \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ \dots \\ V_N \end{bmatrix}. \quad (3.2)$$

Also $V_1, V_2, \dots, V_N$ can be expressed as the voltage drop on corresponding capacitor, which is given by

$$V_n = -i_n \frac{1}{sC}, \quad n=1,2,3\dots N. \quad (3.3)$$

Substituting (3.3) to (3.2), the equation systems concern with $i_2, i_3, \dots, i_N$ can be obtained as

$$\begin{bmatrix} \frac{R}{N} + \frac{Ls}{N} + \frac{1}{sC} & \frac{kLs}{N} & \dots & \frac{kLs}{N} \\ \frac{kLs}{N} & \frac{R}{N} + \frac{Ls}{N} + \frac{1}{sC} & \dots & \frac{kLs}{N} \\ \dots & \dots & \dots & \dots \\ \frac{kLs}{N} & \frac{kLs}{N} & \dots & \frac{R}{N} + \frac{Ls}{N} + \frac{1}{sC} \end{bmatrix} \begin{bmatrix} i_2 \\ i_3 \\ \dots \\ i_N \end{bmatrix} = \begin{bmatrix} -\frac{i_1 kLs}{N} \\ -\frac{i_1 kLs}{N} \\ \dots \\ -\frac{i_1 kLs}{N} \end{bmatrix} \quad (3.4)$$

By solving the linear Equation (3.4) using Cramer's rule, the expressions of $i_2, i_3, \dots, i_n$ can be obtained as

$$i_2 = i_3 = i_4 \dots i_N = \frac{-i_1 k L C s^2}{N + R C s + [1 + (N-2)k] L C s^2} \quad (3.5)$$

Then, V_1 can be expressed as

$$V_1 = i_1 \left(\frac{Ls}{N} + \frac{R}{N} \right) + (i_2 + i_3 + \dots + i_N) \frac{k L s}{N} = i_1 \left(\frac{R + Ls}{N} + \sum_{n=2}^N \frac{i_n}{i_1} \frac{k L s}{N} \right) \quad (3.6)$$

where $\sum_{n=2}^N \frac{i_n}{i_1} = \frac{-(N-1)k L C s^2}{N + R C s + [1 + (N-2)k] L C s^2}.$

Therefore, the input impedance of the multiple-coupled LC -tank Z_{in} can be expressed as

$$Z_{in} = \frac{V_1}{i_1 + s C V_1} = \frac{R + Ls + \left(\sum_{n=2}^N \frac{i_n}{i_1} \right) k L s}{N + R C s + L C s^2 + \left(\sum_{n=2}^N \frac{i_n}{i_1} \right) k L C s^2} \quad (3.7)$$

To calculate resonant frequencies of tank, we can make R as zero. Then the resonant frequencies can be obtained as

$$\omega_1 = \sqrt{\frac{N}{L C [1 + (N-1)k]}} \quad (3.8)$$

$$\omega_2 = \sqrt{\frac{N}{L C (1-k)}} \quad (3.9)$$

Though the multiple-coupled LC -tank is a complexity high order network, there are only two resonant frequencies because our assumptions (i.e., identical individual tank and same coupling coefficient k) have significantly simplified the calculation.

Figure 3.3 plots the resonant frequency ω_1 , ω_2 with the changing of coupling coefficient, when choosing a set of typical tank component values $L=600$ pH, $C=0.8$ pF. It can be seen that when k is increased, the lower resonant frequency ω_1 is

decreased, and the higher resonant frequency ω_2 is increased, resulting in the two resonant frequencies getting far away from each other.

Figure 3.3: Resonant frequencies ω_1 and ω_2 versus coupling coefficient with different values of N .

The effective Q of the multiple-coupled LC -tank at ω_1 or ω_2 can be calculated using the well-known definition as in [33]

$$Q_{eff} = -\frac{\omega_{1,2}}{2} \frac{\partial \psi}{\partial \omega} \bigg|_{\omega=\omega_{1,2}} \quad (3.10)$$

where ψ is the phase response of Z_{in} [33]. For a special case when $k=1$, $\omega_1 = 1/\sqrt{LC}$, and ω_2 approaches to infinite, the expression of Q_{eff} at ω_1 can be given by

$$Q_{eff} = \left(\frac{N^3 + 1.5N \frac{CR^2}{L} + 0.5 \left(\frac{CR^2}{L} \right)^2}{N^3 + N(1+N) \frac{CR^2}{L} + \left(\frac{CR^2}{L} \right)^2} \right) \frac{N\omega L}{R} \quad (3.11)$$

If $R^2C/L \ll 1$, which is the case in most RFIC oscillators [31], the expression of effective Q can be simplified as

$$Q_{eff} = \frac{N\omega L}{R} \quad (3.12)$$

Since the tank Q of single LC -tank with inductance L and capacitance C is $\omega L/R$ multiple-coupled LC -tank can improve the tank Q by a factor of N compared with the single LC -tank. According to Leeson's formula [38], with Q improve by N , the phase noise of VCO with multiple-coupled LC -tank can be improved by $20\log(N)$ dB.

Figure 3.4: Effective Q of multiple-coupled LC -tank at the two resonant frequencies (a) ω_1 , (b) ω_2 .

When k is less than 1, the effective Q of multiple-coupled LC -tank Q_{eff} at ω_1 and ω_2 can be calculated and plotted with the changing of k , as shown in Figure 3.4 (a) and (b). A set of typical tank component values $L=600$ pH, $C=0.8$ pF, $R=3.6$ Ω is used

during the calculation. It can be seen that Q_1 is increased with k increased, while Q_2 is decreased with k increased. Though there are two resonant frequencies, we can choose one of them as the oscillation frequency of VCO by properly design the loop gain at our interest resonant frequency. It is noted that the multiple-coupled LC -tank shows better Q at ω_1 than ω_2 , thus we would prefer to choose ω_1 as the oscillation frequency of VCO for better phase noise performance.

In addition to the coupling coefficient, the tank order N is another important design parameter of multiple-coupled LC -tank. For example in Figure 3.4(a), when $k=0.6$, for $N=2$, $N=3$, $N=4$, and $N=5$, Q_1 is 13, 19, 25, and 31 respectively. Comparing to single LC -tank where $Q=7$ ($L=600$ pH, $C=0.8$ pF, $R=3.6$ Ω), Q_1 has been greatly improved, and the improvement is increased with tank order N . Therefore, both large tank order and high coupling coefficient are required to benefit from the Q enhancement of multiple-coupled LC -tank.

Figure 3.5: Effective Q of multiple-coupled LC -tank at ω_1 considering the loss of capacitor in the tanks.

It is noted that the loss of capacitors has been ignored in the model [Figure 3.2] to simplify the deduction. If considering the loss of capacitor, we can use another resistor R_c in series connection with the capacitor to represent its loss, and derive the tank Q .

Similarly, the tank Q at lower resonant frequency Q_1 can be plotted with a set of tank parameters, as shown in Figure 3.5. $L=200$ pH, $C=100$ fF, $R=1.46\ \Omega$ and $R_C=1.51\ \Omega$ are chosen, and the Q of single LC -tank with L and C can be calculated as 15. It can be seen that the multiple-coupled LC -tank can still improve tank Q considering the loss of capacitor. The difference is the improvement of Q is reduced compared with the case without capacitor loss, because the enhancement of Q by coupled LC -tank needs to compensate the loss brought by capacitors. Fortunately, the enhancement of tank Q is increased with tank order N and coupling coefficient. Therefore, if the coupling of transformer is strong enough and with a large tank order, the tank Q can still benefit from the multiple-coupled LC -tank.

To summary, the multiple-coupled LC -tank can enhance the tank Q compared to single LC tank. The improvement of tank Q is related to the transformer coupling coefficients and tank order. To achieve more enhancement of tank Q , higher coupling coefficients of transformer and larger number of tank order are both needed. It should be noted that as the tank order increases, the coupling between the windings which are far away from each other becomes weak, resulting in a degradation of coupling coefficient and thus tank Q . Therefore, in order to get large tank order and maintain high coupling coefficients among transformer windings, the transformer structure should be properly designed according to the available metal layers in the target process. As an application example, the Section 3.2 will present a mm-wave VCO with five-coupled LC -tank in a 1P9M 65 nm CMOS technology.

3.2 A mm-Wave VCO with Five-coupled LC -tank

Figure 3.6 presents the schematic of the proposed VCO with five-coupled LC -tank. To better show the merits of multiple-coupled LC -tank, the proposed VCO adopts the classical LC -VCO topology and replaces the conventional LC -tank with a five-coupled LC -tank. The five-coupled LC -tank contains a five-coil transformer of which the self-inductances are represented by $L_1 \sim L_5$ respectively, and two pairs of fixed capacitor as well as two pairs of varactor for frequency tuning. The fixed capacitor adopts MOM (metal-oxide-metal) capacitor which has the advantages of small area. The P-type MOS varactor is used for its relative higher Q compared with N-type MOS varactor.

Figure 3.6: Schematic of the proposed VCO.

3.2.1 Circuit Design and Implementation

As a key component of the five-coupled LC -tank, the five-coil transformer needs to be carefully designed. Except for minimizing the loss of those coils, the coupling coefficients between those coils need to be large to enhance the effective Q of the multiple-coupled LC -tank from the previous analysis. Usually, on chip inductors or

transformers are often designed using the top metal layers in order to keep the inductors far away from the substrate, so that the capacitive couplings from substrate can be reduced. Moreover, in a commercial RFIC process, the top metals layers are usually much thicker than the bottom metal layers, thus the resistive loss can be much smaller. Therefore, the top metal layers are preferred to design the required five-coil transformer.

As the example of transformers shown in Figure 3.7, generally, there are two ways to realize a transformer: stacked and concentric [81, 82]. To obtain large coupling coefficients, the stacked transformer structure which involves conductors on different planes is preferred. However, our target process has only three thick metal layers, which is not enough for stacked five-coil transformer. Also, in the stacked transformer, as the number of coils goes large, the coupling between the coils on the top and bottom plane would become weak. Therefore, to obtain large couplings and take advantage of the thick top metal layers to reduce the loss, the stacked transformer structure and concentric transformer structure are combined in the proposed five-coil transformer.

Figure 3.7: Examples of transformer realization with concentric and stacked coupling method.

As shown in Figure 3.8, the proposed transformer is designed using the top three metal layers naming LB, OI, and EA with the thickness of 1.325 μm , 3.3 μm , and 0.9 μm . L_2 and L_3 are concentrically coupled and stacked under L_1 . Simultaneously, L_4 and L_5 are stacked on L_1 and also concentrically coupled. The outer dimension of transformer is 120 μm , and the winding width is 11 μm . The interval space between L_2

and L_3 , L_4 and L_5 are both 3 μm . L_1 utilizes the two parallel connected windings with width of 11 μm to reduce the parasitic capacitances and increase the coupling between L_2 , L_3 and L_4 , L_5 . The transformer is simulated using an EM simulator High Frequency Structural Simulator (HFSS). The simulated self-inductances $L_1 \sim L_5$ are 94 pH, 111 pH, 98 pH, 121 pH, and 103 pH respectively at 36 GHz. Table 3-1 lists the simulated self-inductances and coupling coefficients among those coils. Benefiting from the specially designed structure, all the coupling coefficients are larger than 0.6. k_{12} , k_{13} are larger than k_{14} and k_{15} , because the VIA layer between OI and EA is thinner than that between OI and LB.

Figure 3.8: Transformer structure.

TABLE 3-1 SUMMARY OF TRANSFORMER PARAMETERS

Coil Name	Layer Name	Ind. (pH)	Coupling coefficient				
L_1	OI	94	--	$k_{12}=-0.71$	$k_{13}=-0.76$	$k_{14}=-0.64$	$k_{15}=-0.69$
L_2	EA	111	$k_{21}=0.71$	--	$k_{23}=0.69$	$k_{24}=0.65$	$k_{25}=0.61$
L_3	EA	98	$k_{31}=0.76$	$k_{32}=-0.69$	--	$k_{34}=0.61$	$k_{35}=0.66$
L_4	LB	121	$k_{41}=0.64$	$k_{42}=-0.65$	$k_{43}=-0.61$	--	$k_{45}=0.60$
L_5	LB	103	$k_{51}=0.69$	$k_{52}=-0.61$	$k_{53}=-0.66$	$k_{54}=-0.60$	--

To demonstrate the enhancement of tank Q of multiple-coupled LC -tank, a normal single LC -tank is used for comparison of which the inductor has the same outer

dimension and total inductance with the designed five-coil transformer. In the single LC -tank, the inductor Q is 17, and the capacitor Q is 15 at the resonate frequency of tank, thus the Q of single LC -tank can be calculated as $Q_{\text{tank}} = (Q_L^{-1} + Q_C^{-1})^{-1} = 8$. The Q of five-coupled LC -tank can be evaluated by simulating the magnitude of the impedance looking into the primary coil (i.e., L_1). During the simulation, each coil of the transformer is connected to the capacitor with the same Q value as that in the single LC -tank for a fair comparison. Figure 3.9 plots the simulated impedance of the five-coupled LC -tank. It can be calculated that the tank Q of the five-coupled LC -tank is about 21, which is 2.6 times of the single LC -tank Q .

Figure 3.9: Impedance magnitude of five-coupled LC -tank.

According to the oscillation start-up condition [Equation (2.5)], the negative conductance provided by the cross-coupled pair should be able to compensate the loss on the LC -tank, thus the minimum transconductance (g_m) of the transistor to start oscillation is $2/R_P$, where R_P represents the equivalent parallel resistance of the LC -tank. In this work, we set g_m as 2 times of the minimum value, i.e., $4/R_P$ to start oscillation against PVT variation. For the proposed LC -tank, R_P is about 360Ω , and then the transistor g_m is set as 11 mS.

Figure 3.10: (a) The f_T versus V_{gs} for different transistor size, where $V_{gs}=V_{ds}$. (b) The f_{max} and NF_{min} of transistor versus the finger number (fn) of transistor when $W/L=11\mu\text{m}/60\text{nm}$, and $V_{gs}=V_{ds}=0.9\text{V}$.

The bias voltage of cross-coupled transistors is chosen to achieve the optimum f_T . Figure 3.10 (a) plots the f_T versus V_{gs} for different transistor size, where $V_{gs}=V_{ds}$. It can be seen that for different transistor sizes, the maximum f_T are all achieved when V_{gs} (V_{ds}) is around 0.9 V. With the bias voltage $V_{gs}=V_{ds}=0.9\text{V}$, the size of transistor is selected as $W/L=11\mu\text{m}/60\text{nm}$ to make the g_m of transistor as 11 mS to start up the oscillation. The finger number of transistor is selected according to the trade-offs among the f_T , the f_{max} and the minimum noise figure (NF_{min}) of transistor. Figure 3.10

(b) plots the $f_{\max}$ and the $NF_{\min}$ of transistor versus finger number (fn) of transistor when $W/L=11\ \mu\text{m}/60\ \text{nm}$, and $V_{gs}=V_{ds}=0.9\ \text{V}$. When the finger number increases from 10 to 22, the $f_{\max}$ increases and $NF_{\min}$ decreases due to the reduced gate resistance. On the other hand, as the increasing of the finger number, f_T is decreased which can be seen from Figure 3.10 (a). For a mm-wave VCO, high f_T and $f_{\max}$ are required to achieve high gain of transistor at its operation frequency, while the low $NF_{\min}$ of transistor is needed for low phase noise of the VCO. In this work, we choose $fn=18$, where high $f_{\max}$ and low $NF_{\min}$ are both achieved, at the same time f_T is higher than 4 times of the operation frequency.

Figure 3.11: Chip micrograph.

3.3.2 Experimental Results

The proposed VCO with five-coupled LC -tank is implemented in a 1P9M 65nm CMOS technology. The micrograph of the circuit is shown in Figure 3.11, where the size of the core circuit is $0.15 \times 0.364\ \text{mm}^2$. The characterization of the circuit performance is carried out via on-wafer probing. The measurement system setup is illustrated in Figure 3.12, where the output spectrum is obtained using a PNA-X

network analyzer N5247A, and the phase noise is measured using Agilent signal source analyzer E5052B.

Figure 3.12: Measurement setup for the test of (a) output power, and (b) phase noise.

With a supply voltage of 0.9 V, the VCO core consumes a DC current of 8 mA. The measured output spectrum of the VCO is shown in Figure 3.13, where we can see the output power is -8.7 dBm as the oscillation frequency is 37.1 GHz. Figure 3.14 shows the measured and the simulated oscillation frequency and phase noise at 1 MHz offset with the changing of tuning voltage. When the tuning voltage increases from 0 to 1.2 V, the measured oscillation frequency decreases from 37.1 GHz to 35.2 GHz. Compared to the simulated result, the center frequency is shifted down by only 130 MHz (less than 0.3%), which is close to the simulation. Over the tuning range, the measured phase noise at 1MHz offset changes from -107.2 dBc/Hz to -94 dBc/Hz. Compared to the simulated result which is from -108.4 dBc/Hz to -100.6 dBc/Hz, the measured phase noise is degraded by 1 dB to 6 dB as the changing of tuning voltage. The difference between measured and simulated phase noise is large at the lower frequency end of the tuning range due to the contribution of AM-PM noise. In the measurement, the noise on the DC power supply and ground modulates the voltage on the varactors, and hence affects the oscillation frequency and degrades the phase noise.

Therefore, the phase noise is degraded more at the lower frequency end of the tuning range where the capacitance of varactor changes faster with the tuning voltage. Figure 3.15 shows the measured phase noise versus the offset frequency when the tuning voltage is 0. The phase noise is -107 dBc/Hz at 1 MHz offset frequency.

Figure 3.13: Measured output spectrum.

Figure 3.14: Measured (solid line) and simulated (dash line) oscillation frequency and phase noise at 1MHz offset with the changing of control voltage.

Figure 3.15: Measured phase noise.

TABLE 3-2 PERFORMANCE COMPARISON WITH RECENT WORKS

Ref.	Process	Freq. (GHz)	V _{DD} (V)	P _{DC} (mW)	PN@1MHz (dBc/Hz)	TR (%)	FOM (dBc/Hz)
[83]	65 nm CMOS	39.9	1.2	14.4	-98.1	15.1	-178.5
[84]	90 nm CMOS	39	0.75	1.65	-96.7	8.9	-186.3
[85]	0.18 μ m CMOS	29.4	1.8	16.2	-110.3	8.3	-187.6
This work	65 nm CMOS	37	0.9	7.2	-107.2	5.2	-189.7

The overall performance of the proposed VCO is summarized in Table 3-2 and compared with other reported VCOs [83-85]. The figure-of-merit (FOM) taking into account of phase noise and power consumption is used for comparison [7],[53],[86].

The FOM is defined as

$$\text{FOM} = L(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log(P_{\text{DC}}) \quad (3.13)$$

where $L(f_m)$ is the phase noise from the oscillator frequency (f_0) at a frequency offset of f_m , and P_{DC} is the DC power consumption of VCO in milliwatt. The FOM of this work is -189.7 dBc/Hz, which is better than other works in the table.

3.3 Summary

The multiple-coupled LC -tank with tank order of N has been investigated in this chapter. Through theoretical deduction, the Q enhancement of the multiple-coupled LC -tank compared to the normal single LC -tank has been demonstrated. Besides, the effects of key parameters on the Q enhancement have also been studied. A 36 GHz VCO with a five-coupled LC -tank is designed to verify the theory. From the simulation, the five-coupled LC -tank has demonstrated an enhancement of tank Q at 2.6 times compared to the single- LC -tank with the same total inductance and size. Implemented in a 65 nm CMOS technology, the VCO demonstrates a low phase noise of -107 dBc/Hz at 1MHz offset, while consumes only 7.2 mW DC power. Taking into account of power consumption and phase noise, the VCO shows a better FOM of -189.7 dBc/Hz compared to other mm-wave works.

Chapter 4

Design of a Ku-band VCO with Dual *LC*-tanks

4.1 Introduction

The transceiver architecture with dual-conversion of frequency is widely used by 60 GHz transceivers because of its relatively simple structure and low LO frequency. In [28] and [29], VCOs with frequencies of 40 GHz and 24 GHz have been used respectively for two 60 GHz receivers with two-step frequency conversion. In [87], the VCO frequency of the transmitter is further reduced to 15 GHz by using a $\times 4$ frequency multiplier. With a lower VCO frequency, the design complexity of the VCO and also the frequency synthesizer can be significantly reduced. In this chapter, a 12 GHz VCO is designed for the 60 GHz receiver as shown in Figure 4.1. The receiver adopts a dual-conversion super-heterodyne architecture with the VCO frequency at 12 GHz and a $\times 4$ frequency multiplier. The 12 GHz LO frequency is multiplied by 4 and is used to down-convert 60 GHz to 12 GHz. Then, the resulted 12 GHz middle IF frequency is down-converted to baseband frequency with the 12 GHz LO. Benefiting from the low LO frequency at 12 GHz, the performance of the VCO in the receiver can

get better trade-offs. Although the frequency multiplier dissipates additional power consumption, designing the VCO at 12 GHz eliminates the need of mm-wave frequency dividers in PLL, which reduces the power consumption and the design complexity of PLL.

Figure 4.1: Dual-conversion receiver architecture for 60 GHz.

Phase noise is one of the most important specifications of a VCO since it heavily influences the selectivity and signal to noise ratio of receivers and transmitters. Even though numerous VCO topologies aiming at reducing phase noise have been reported in the past decade [53, 76, 88-91], it is difficult to achieve low phase noise and maintain low DC power consumption in VCO design. In this chapter, the dual LC -tanks and the transformer-based feedback technique have been used in the proposed 12 GHz VCO to achieve low phase noise and low power consumption. A triple-coil transformer is adopted to provide the strong magnetic coupling of the two LC -tanks and the feedback. The parameters of the transformer, which are crucial to determine the oscillation frequency, phase noise and output signal swing, have been optimized. This chapter is organized as follows. Section 4.2 presents the circuit and the

Figure 4.2: Schematic of the proposed VCO with dual LC -tanks and transformer-based feedback.

4.2 Circuit Design and Implementation

The schematic of the proposed VCO with the dual LC -tanks configuration is shown in Figure 4.2. The transistors M_1 and M_2 form a cross-coupled pair to generate the negative conductance for oscillation. C_{v1} and C_{v2} are MOS varactors for frequency tuning. L_1 , L_2 and L_3 are the self-inductance of each coil of the transformer. L_1 and L_2 incorporating with C_{v1} and C_{v2} act as primary LC -tank, while L_3 and MIM capacitor C_3 form the secondary LC -tank. The secondary LC -tank is passive and isolated from the primary one in DC, thus it does not consume any DC power. The triple-coil transformer can provide magnetic coupling between the two LC -tanks and transformer-

based feedback between drain and source, so that both the voltage swing and the Q of the tank can be increased.

Figure 4.3: Small signal equivalent circuit of the half VCO.

The equivalent circuit of the half VCO is illustrated in Figure 4.3 using the small signal model. R_{t1} and R_{t2} are the parallel resistors which stand for the resistive loss of the primary and secondary LC -tank. The currents through L_1 , L_2 and L_3 are expressed as i_1 , i_2 and i_3 . The v_1 , v_2 and v_3 are the node voltage of L_1 , L_2 and L_3 , respectively. For simplicity, the coupling coefficients are assumed to be unity, and the inductance ratios between corresponded coils of transformer are defined as $\alpha = (L_2/L_1)^{1/2}$ and $\beta = (L_3/L_1)^{1/2}$ in the following discussion. The triple-coil transformer can be represented by the means of impedance matrix as below

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = L_1 s \begin{bmatrix} 1 & \alpha & \beta \\ \alpha & \alpha^2 & \alpha\beta \\ \beta & \alpha\beta & \beta^2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \quad (4.1)$$

Based on the equivalent circuit, the current through L_1 , L_2 and L_3 are given by

$$i_1 = -(v_{in} - v_2) g_m - v_1 s C_{v1} - \frac{v_1}{R_{t1}} \quad (4.2)$$

$$i_2 = (v_{in} - v_2) g_m - v_2 s C_{v2} \quad (4.3)$$

$$i_3 = -v_3 s C_3 - \frac{v_3}{R_{t2}} \quad (4.4)$$

From (4.4) to (4.7), the transfer function $H(s) = v_1/v_{in}$ can be solved as shown in (4.5).

$$H(s) = \frac{-g_m L_1 (1-\alpha) s}{1 + s L_1 \left[g_m \alpha (1-\alpha) + \frac{1}{R_{t1}} + \frac{\beta^2}{R_{t2}} \right] + s^2 L_1 (C_{v1} + \alpha^2 C_{v2} + \beta^2 C_3)} \quad (4.5)$$

Substituting $s=j\omega$ to (3.18), the phase shift of $H(s)$ can be written as

$$\psi = 270^\circ - \tan^{-1} \left(\frac{R_{t1} R_{t2} g_m \alpha (1-\alpha) + R_{t2} + \beta^2 R_{t1}}{1 - \omega^2 L_1 (C_{v1} + \alpha^2 C_{v2} + \beta^2 C_3)} \right) \quad (4.6)$$

When the phase delay of $H(s)$ is 180° , the oscillation frequency can be calculated as

$$\omega_{osc} = \frac{1}{\sqrt{L_1 (C_{v1} + \alpha^2 C_{v2} + \beta^2 C_3)}} = \frac{1}{\sqrt{L_1 C_{v1} + L_2 C_{v2} + L_3 C_3}} \quad (4.7)$$

It can be seen that the oscillation frequency depends on the inductances and capacitances of the dual LC -tanks. For the same aimed oscillation frequency, the required inductance of the dual LC -tanks VCO has been separated into three smaller strong coupled inductors, resulting in smaller size and less metal loss of the transformer compared to a single LC -tank.

The Q can be deduced using the general definition in [33] and expressed as

$$\begin{aligned} Q &= \frac{\omega_{osc}}{2} \left| \frac{d\psi}{d\omega} \right|_{\omega=\omega_{osc}} \\ &= \left| g_m (\alpha - 1) \alpha + \frac{1}{R_{t1}} + \frac{\beta^2}{R_{t2}} \right|^{-1} \sqrt{\frac{C_{v1} + \alpha^2 C_{v2} + \beta^2 C_3}{L_1}} \end{aligned} \quad (4.8)$$

We can observe that if $\alpha < 1$, the value of α and β can be designed to make $g_m(\alpha-1)\alpha + 1/R_{l1} + \beta^2/R_{l2}$ much smaller than 1, then the Q value of the VCO can be dramatically improved. Since the phase noise is reduced as Q increases, the phase noise performance of the VCO can be enhanced. It can be seen that the improvement of phase noise benefits from the strong coupling between the two LC -tanks together with the transformer-based feedback from drain to source of the transistors. On the other hand, the secondary LC -tank is isolated in DC from the primary tank and does not dissipate extra DC power, thus the power consumption could be saved. Therefore, the overall performance of the VCO can be improved. As the Q of capacitor is much higher than that of inductor, the R_{l1} and R_{l2} are mainly determined by the resistive loss of the inductors. Since the value of α and β depends on the turn ratios of the transformer, the design of the transformer is crucial for the oscillator performance.

Figure 4.4: The 3D structure of the triple-coils transformer (center tap not shown).

The transformer is implemented in a commercial 0.18 μm 1P6M BiCMOS technology from Tower Jazz Semiconductor. In this design, the inductance ratios $\alpha = \beta = 0.5$ are chosen for a better trade off among phase noise, power consumption and implementation. Simultaneously, the advantages of stacked and concentric topology can provide strong magnetic coupling and thus keep a compact size. Figure 4.4 shows the 3D structure of the triple-coil transformer applied in proposed circuit. The top two metal layers M5 and M6 are used for the inner and outer spirals of L_1 respectively. The

spiral of L_2 using M6 is stacked on the inner spiral of L_1 and placed concentrically with the outer spiral of L_1 . L_3 is built with M6, surrounding L_1 and L_2 . The outer dimension of the transformer is $208\text{ }\mu\text{m}$, and the metal width of each spiral is $14\text{ }\mu\text{m}$.

Figure 4.5: The simulated coupling coefficients of the triple-coils transformer.

Figure 4.6: The simulated quality factor of the each coil of the transformer.

The transformer is simulated and optimized by using Agilent Momentum in order to optimize the parasitic capacitance and minimize the metal loss. The simulated self-inductance of each coil of the transformer L_1 , L_2 and L_3 are 439 pH, 159 pH, and 119 pH at 12 GHz. The simulated coupling coefficients of the transformer are given in Figure 4.5, where k_{12} , k_{13} and k_{23} are 0.82, 0.58 and 0.42 at 12 GHz, respectively. k_{12} is

high because of the stacked coupling method. k_{13} and k_{23} are low due to their concentric topology. Since the value of k represents the strength of magnetic coupling in the transformer, when k approaches unity, the coupling between the two LC -tanks will be maximized. Then, the tank Q will be optimized as the previous deduction. Physically, it is mainly because the mutual inductance provided by the magnetic coupling would contribute to the oscillation with minimized resistance loss, thus the Q is improved. From our investigation, when k is less than 1, the Q is still improved, but the improvement will be reduced compared with $k=1$. The Q values of L_1 , L_2 and L_3 versus frequency are plotted in Figure 4.6. At the required oscillation frequency, the Q of L_1 , L_2 and L_3 are 15.15, 15.11 and 12.91 respectively. A ground shield in silicided active is inserted below the transformer to improve the noise isolation and boosted factor performance. The shield is 25 μm larger than the transformer and a M1 frame connects the shield fingers which are active, keeping the resistive loss over the shield small.

The size of the cross-coupled transistors is designed to satisfy the start-up condition of oscillation. From the transfer function [Equation (4.5)], the required minimum transconductance of transistor can be derived by making $H(j\omega_{\text{osc}}) \geq 1$, which is given by

$$g_m \geq \frac{1}{(1-\alpha)^2} \left(\frac{1}{R_{t1}} + \frac{\beta^2}{R_{t2}} \right) \quad (4.9)$$

To start an oscillation against PVT variation, g_m can be chosen as twice of the minimum value. Similar to the procedure in section 3.2.1, the transistor size then can be designed according to the g_m value.

The gate width and length of the varactors will determine the maximum and minimum capacitance of the varactor as well as the component Q . Increased gate area

will give a wider tuning range but a lower Q due to the increased Nwell and ploy gate resistance. Since we focus on reducing the phase noise in this design, the varactors with multi-fingers and minimum gate width and length are utilized to keep a high Q of the tank.

4.3 Experimental Results

The chip photograph of the proposed VCO is shown in Figure 4.7. The total chip size is $0.633 \times 0.713 \text{ mm}^2$ including output buffers and I/O pads. The characterization of the circuit performance was carried out by on-wafer probing. The phase noise was measured using Agilent signal source analyser E5052B, and the output power is measured with a PNA-X network analyzer N5247A. The proposed dual LC -tanks VCO core consumes a DC power of only 4.3 mW with a supply voltage of 0.7 V.

Figure 4.8 shows the measured output spectrum. The power level at the fundamental frequency is -16.72 dBm with a suppression of 28 dB to the second harmonic. Figure 4.9 plots the simulated and measured results of oscillation frequency and output power versus the tuning voltage. With the tuning voltage changing from 0 to 1.8 V, the measured output power of the VCO after cable loss calibration is from -11.3 dBm to -12.48 dBm, which is close to the simulated results. The measured frequency tuning range is from 13.07 GHz to 12.64 GHz. Compared to the simulated result, the center frequency is shifted down by 90 MHz which is mainly due to the inaccurate simulation of parasitic capacitance in the circuit. The simulated phase noise of the VCO is -119 dBc/Hz at 1 MHz offset. The measured VCO phase noise is shown in Figure 4.10. It can be seen that the VCO achieves a phase noise of -117.4 dBc/Hz at 1 MHz offset, which is only degraded by 1.6 dB compared to the simulated result.

Figure 4.7: Chip micrograph.

Figure 4.8: Measured output spectrum.

The overall performance of the proposed VCO is listed in TABLE 4-1 and compared with other reported works [76, 88-91]. In order to compare the overall performance of the VCOs, the FOM which considers phase noise and power consumption is adopted in the comparison [7],[53],[86]. The FOM is given by

$$\text{FOM} = L(f_m) - 20 \log \left(\frac{f_0}{f_m} \right) + 10 \log (P_{\text{DC}}) \quad (4.10)$$

Figure 4.9: Measured and simulated results of oscillation frequency and output power versus tuning voltage.

Figure 4.10: Measured phase noise.

where $L(f_m)$ is the phase noise from the oscillator frequency (f_0) at a frequency offset of f_m , and P_{DC} is the DC power consumption of the VCO in milliwatts. Compared to other designs, the proposed work has achieved a better FOM value of -193.1 dBc/Hz

due to the low phase noise and low power consumption. Since this work focuses on the design trade-off between phase noise and power consumption, the VCO tuning range is not optimized. To improve the tuning range of the VCO, the C_3 in the secondary LC -tank can be replaced by a varactor or a switched capacitor array [92],[93],[94]. Meanwhile, the size of the transformer should be properly scaled to locate the tuning range at the desired frequency band.

TABLE 4-1 PERFORMANCE COMPARISON OF VCOS

Ref.	Process	VDD (V)	Freq. (GHz)	PN* (dBc/Hz)	FTR (%)	Pdc,core (mW)	FOM (dBc/Hz)
[88]	0.18 μm CMOS	1.8	11.5	-110.8	5.4%	8.1	-183
[76]	0.18 μm CMOS	1.8	11.2	-109.4	2.6%	6.8	-181.8
[89]	0.18 μm CMOS	0.6	11.0	-110.4	9.9%	4.1	-185.2
[90]	0.18 μm CMOS	1.8	9.83	-89**	11.2%	5.8	-181.2
[91]	0.18 μm CMOS	1	13.5	-112	7.7%	6.2	-184
This work	0.18 μm BiCMOS	0.7	12.6	-117.4	3.3%	4.3	-193.1

* Phase noise (PN) is @1MHz offset.

**Phase noise is @100kHz offset.

4.4 Summary

A Ku-band VCO with dual LC -tanks and transformer-based feedback is proposed and designed in this chapter using a commercial 0.18 μm BiCMOS process. By theoretical analysis, the improvement of Q resulting from the strong coupling between the two LC -tanks and the transformer-based feedback has been demonstrated. A low phase noise of -117.4 dBc/Hz at 1 MHz offset has been obtained from the carrier frequency of 12.64 GHz. Benefiting from the special configuration of dual LC -tanks, the VCO exhibits low power consumption, and achieves a better FOM of -193.1 dBc/Hz compared to the currently reported designs.

Chapter 5

A Wide Tuning Range and Low Phase Noise mm-Wave VCO Using Switchable Coupled VCO-Cores

5.1 Introduction

Conventionally, wide tuning range and low phase noise of VCO can be obtained by employing a parallel combination of switched capacitor array for coarse frequency tuning and MOS varactors for fine frequency tuning [39-41]. However, when operation frequency increases to the mm-wave region, the Q of LC -tank will be significantly reduced due to the low Q of capacitor/varactor and the high loss incurred in switches. As a result, the phase noise of VCO will be degraded. On the other hand, to sustain oscillations at mm-wave, the size of transistors has to increase which will inevitably increase the parasitic capacitance and further limits the tuning range.

Transformer-based coupled LC -tanks with two resonant frequencies can be used to realize dual-mode VCOs [43-46] and increase frequency tuning range [47-49]. In those dual-mode VCOs, the oscillation of one mode is excited at the lower resonant

frequency of tank, and the other mode is excited at the higher resonant frequency of tank. This method can extend frequency tuning range, and when the loss of tank capacitor is much smaller than that of inductor, the tank Q at lower resonant frequency can be enhanced compared to the single LC -tank with the same component Q . However, the tank Q at higher resonant frequency will be decreased [45], resulting the phase noise being improved for one mode but degraded for the other mode. What is worse, when the loss of tank capacitor is comparable with the loss of inductor at mm-wave frequency, as will be shown in this work, the tank Q at the lower resonant frequency can only be enhanced when the coupling coefficient (k) is larger than a certain value. But, at the same time, to ensure stable oscillation at higher resonant frequency of tank, small k of transformer is required [50] (e.g., 0.2 in [48]), which will in return limits the enhancement or even degrades the tank Q at the lower resonant frequency.

To achieve low phase noise and stable oscillation for both modes, a new dual-mode mm-wave VCO topology involving switchable coupled VCO-cores is proposed in this chapter. Taking advantage of different parasitic capacitance of the cross-coupled pair as the corresponding VCO-core in ON and OFF states, the dual-mode operation at mm-wave frequency can be realized, and the oscillations for both modes are allowed to be excited at the lower resonant frequency of tank, thus the tank Q and phase noise performance of VCO can be improved for both modes. Simultaneously, the stability of oscillation at desired resonant frequency can be improved for both modes by using large k transformer, which in return facilitates the enhancement of tank Q for both modes. Besides, the frequency tuning range of VCO can be increased by properly designing the VCO-cores and combining the frequency bands of the two modes. Moreover, the cross-coupled pair of VCO-core operating in OFF state is able to act as

high Q active capacitor to further improve the tank Q and phase noise performance of VCO. Using the proposed topology, a dual-mode mm-wave VCO with the wide tuning range of 17.2% and low phase noise from -97.5 dBc/Hz to -92 dBc/Hz at 1 MHz offset over the entire tuning range has been successfully demonstrated in 0.18 μm SiGe BiCMOS process. This chapter is organized as follows. Section 5.2 presents the theoretical analysis of the proposed VCO including the operation mechanism, tank Q , oscillation stability, and high Q active capacitor. Section 5.3 gives the details of circuit design and implementation. The experimental results are shown in Section 5.4, and the conclusion is given in Section 5.5.

5.2 Analysis of the Proposed VCO

Figure 5.1 (a) shows the schematic of the proposed dual-mode VCO which is composed of two switchable coupled VCO-cores (i.e., Core1, Core2) and a frequency doubler. Bipolar transistors $Q_1 \sim Q_4$ form the two cross-coupled pairs of the two VCO-cores. C_{v1} and C_{v2} are varactors for frequency tuning. I_{B1} and I_{B2} are the bias currents of Core1 and Core2. A triple-coil strongly coupled transformer is adopted to couple the two VCO-cores and also couple the oscillated signal to the input of frequency doubler, such that the output of the two operation modes can be obtained at the same port. L_1 , L_2 , and L_3 are self-inductance of the primary, secondary and tertiary coils of transformer.

The two operation modes of VCO are denoted as Mode A and Mode B. By controlling I_{B1} and I_{B2} , Core1 is switched on and Core2 is switched off for Mode A, while Core1 is switched off and Core2 is switched on for Mode B. As shown in Figure 5.1(b), supposing the frequency tuning range of VCO is from f_0 to f_1 for Mode A, and f_2 to f_3 for Mode B, when the frequency tuning ranges of Mode A and Mode B have

been carefully designed to make $f_0 < f_2 \leq f_1 < f_3$, a continuous wide frequency tuning range of VCO from f_0 to f_3 can be achieved.

Figure 5.1: (a) Schematic of the proposed VCO with switchable coupled VCO-cores. (b) Frequency allocation for Mode A and Mode B.

Figure 5.2: Input parasitic capacitance of cross-coupled pair with bias current.

5.2.1 Dual-mode Operation with Switchable Coupled VCO-cores

As shown in Figure 5.2, when the bias current of cross-coupled pair is set to I_{on} or I_{off} , the value of input parasitic capacitance of cross-coupled pair, C_{on} or C_{off} are different. Denoting C_{on1} and C_{off1} , C_{on2} and C_{off2} as the input parasitic capacitance of cross-coupled pair in Core1 and Core2 in their ON and OFF state, respectively, the equivalent circuits of VCO (without doubler) for Mode A and Mode B can be shown as in Figure 5.3(a) and (b). Using C_1 and C_2 to represent the capacitance loaded on the primary and secondary coil of transformer, then there are $C_1 = C_{v1} + C_{on1}$, $C_2 = C_{off2} + C_{v2}$ for Mode A, and $C_1 = C_{v1} + C_{off1}$, $C_2 = C_{on2} + C_{v2}$ for Mode B. R_{c1A} and R_{c2A} , R_{c1B} and R_{c2B} represent the overall resistive loss of C_1 and C_2 for Mode A and Mode B. C_3 represents the input parasitic capacitance of doubler and R_{c3} is its parasitic resistance. For simplicity of calculation, the coupling coefficients between any two windings of transformer are assumed to be identical and labeled as k . R_1 , R_2 and R_3 are the parasitic resistance of transformer.

Figure 5.3: Equivalent circuit of VCO (without doubler) and equivalent tank network for tank impedance calculation: (a) Mode A and (b) Mode B.

The equivalent network of tank impedance ($Z_{in,A}$ and $Z_{in,B}$) for Mode A and Mode B are also shown in Figure 5.3 (a) and (b). Ignoring $R_1 \sim 3$, $R_{c1A} \sim c1B$, $R_{c2A} \sim c2B$, and R_{c3} , the resonant frequencies can be calculated. In this work, C_3 is much smaller than C_1 and C_2 , and we can assume $C_3 L_3 \omega^2 \ll 1$ which is reasonable in our target frequency range. Then, L_{eq1} and L_{eq2} can be derived and simplified as

$$L_{eq1} \approx L_1 - \frac{k^2 \omega^2 L_1 L_2 C_2}{\omega^2 L_2 C_2 - 1}, \quad (5.1)$$

$$L_{eq2} \approx L_2 - \frac{k^2 \omega^2 L_1 L_2 C_1}{\omega^2 L_1 C_1 - 1}. \quad (5.2)$$

Therefore, the resonant frequencies of tank for Mode A can be solved by $\omega = 1 / \sqrt{L_{eq1} C_1}$, and the resonant frequencies of tank for Mode B can be solved by $\omega = 1 / \sqrt{L_{eq2} C_2}$. It can be found that the tank resonant frequency expressions for Mode A are the same as the expressions for Mode B. For each mode, the resonant frequencies are given by

$$\omega_{H/L} = \sqrt{\frac{L_1 C_1 + L_2 C_2 \pm \sqrt{(L_1 C_1 - L_2 C_2)^2 + 4k^2 L_1 C_1 L_2 C_2}}{2L_1 C_1 L_2 C_2 (1 - k^2)}} \quad (5.3)$$

To take advantage of the Q enhancement of coupled LC -tanks, as will be discussed in Section 5.2.2, the oscillations of VCO are excited at the lower resonant frequency ω_L for both modes. Though the expression of ω_L are the same for Mode A and Mode B, the parameters C_1 and C_2 vary as mode changes, resulting in different value of ω_L in Mode A and Mode B. Without loss of generality, the capacitance ratio is defined as $\alpha = C_1 / C_T = 1 - C_2 / C_T$ ($0 < \alpha < 1$), where $C_T = C_1 + C_2$ is the total capacitance of C_1 and C_2 . When the operation mode of VCO changes from Mode A to Mode B, the capacitance ratio α and total capacitance C_T would vary from α_A and $C_{T,A}$ to α_B and $C_{T,B}$, respectively. Substituting α and C_T to (5.3), the expression of ω_L can be rewritten as a function of α and C_T , which is given by

$$\omega(\alpha, C_T) = \sqrt{\frac{\alpha + n(1 - \alpha) - \sqrt{(\alpha - n + n\alpha)^2 + 4n\alpha(1 - \alpha)k^2}}{2(1 - k^2)n\alpha(1 - \alpha)L_1 C_T}} \quad (5.4)$$

where the N is inductance ratio $n=L_2/L_1$. Thereby, the operation frequencies for Mode A and Mode B can be expressed as $\omega(\alpha_A, C_{T,A})$ and $\omega(\alpha_B, C_{T,B})$. Assuming $\omega(\alpha_A, C_{T,A}) < \omega(\alpha_B, C_{T,B})$, if $\Delta f = (\omega(\alpha_B, C_{T,B}) - \omega(\alpha_A, C_{T,A})) / 2\pi$ is properly designed, the frequency tuning ranges of the two modes are able to form a continuous wide frequency tuning range [Figure 5.1(b)]. In order to obtain a suitable Δf , the design parameters α_A , α_B , $C_{T,A}$ and $C_{T,B}$ need to be carefully chosen. In addition to the requirement of Δf , the range of α_A , α_B , $C_{T,A}$ and $C_{T,B}$ can be restrained by optimized power consumption and requirement of C_{v1} and C_{v2} . Besides, the selection of α_A and α_B need consider the tank Q and stability of oscillation. The detail of parameter selections will be discussed in Section 5.3.1.

The proposed VCO takes advantage of parasitic capacitance variation of cross-coupled pair at ON and OFF states to change the frequency band. At mm-wave frequency, the required tank capacitance is relatively small and the variation of parasitic capacitance of cross-coupled pair is comparable with other capacitors in LC -tank, therefore its effect on frequency would be more obvious. By controlling the bias current of cross-coupled pair, the mode switching between Mode A and Mode B is achieved without using any switches directly connected to LC -tank, avoiding the degradation of tank Q from lossy switches. In addition, for both modes, the oscillation of VCO is at the lower resonant frequency of tank, as will be shown in the following, the strongly coupled transformer in proposed VCO will not only better enhance the tank Q of modes, but also mandate more stable oscillation on the desired resonant frequency of tank.

5.2.2 Tank Q

The tank Q at the resonant frequency ω_L and ω_H can be calculated using the open loop Q definition from Razavi in [95],

Figure 5.4: Calculated and simulated tank quality factors (a) $Q_A(\omega_L)$, (b) $Q_A(\omega_H)$, for Mode A, and (c) $Q_B(\omega_L)$, (d) $Q_B(\omega_H)$ for Mode B, and quality factor of conventional LC -tank with same component Q (dashed line).

$$Q(\omega_{H/L}) = \frac{\omega_{H/L}}{2} \left| \frac{d\varphi_{A/B}}{d\omega} \right|_{\omega=\omega_{H/L}} \quad (5.5)$$

where $\varphi_{A/B}$ denotes the phase shift of tank impedance $Z_{in,A}$ or $Z_{in,B}$. Based on the equivalent network of $Z_{in,A}$ or $Z_{in,B}$ in Figure 5.3 (a) and (b), the tank Q for Mode A and Mode B can be calculated, respectively. Since C_3 is much smaller than C_1 and C_2 , the effects of R_3 and R_{c3} on tank Q are negligible. Then, the expression of equivalent inductance L_{eq1} and L_{eq2} considering parasitic resistance are derived as

$$L_{eq1} = L_1 + \frac{C_2 k^2 L_1 L_2 \omega^2 (1 - C_2 L_2 \omega^2)}{(1 - C_2 L_2 \omega^2)^2 + C_2^2 \omega^2 (R_2 + R_{c2A})^2} \quad (5.6)$$

$$L_{eq2} = L_2 + \frac{C_1 k^2 L_1 L_2 \omega^2 (1 - C_1 L_1 \omega^2)}{(1 - C_1 L_1 \omega^2)^2 + C_1^2 \omega^2 (R_1 + R_{c1B})^2} \quad (5.7)$$

and the equivalent resistance R_{eq1} and R_{eq2} are given by

$$R_{eq1} = R_1 + \frac{C_2^2 k^2 L_1 L_2 \omega^4 (R_2 + R_{c2A})}{(1 - C_2 L_2 \omega^2)^2 + \omega^2 C_2^2 (R_2 + R_{c2A})^2} \quad (5.8)$$

$$R_{eq2} = R_2 + \frac{C_1^2 k^2 L_1 L_2 \omega^4 (R_1 + R_{c1B})}{(1 - C_1 L_1 \omega^2)^2 + \omega^2 C_1^2 (R_1 + R_{c1B})^2} \quad (5.9)$$

Then, the phase shift of $Z_{in,A}$ or $Z_{in,B}$ can be calculated and expressed as

$$\begin{aligned} \varphi_A &= \tan^{-1} \frac{\omega(L_{eq1} - C_1 R_{eq1}^2 - C_1 L_{eq1}^2 \omega^2 + C_1^2 L_{eq1} R_{c1A}^2 \omega^2)}{R_{eq1} + C_1^2 R_{c1A} R_{eq1} \omega^2 (R_{c1A} + R_{eq1}) + C_1^2 L_{eq1}^2 R_{c1A} \omega^4} \\ \varphi_B &= \tan^{-1} \frac{\omega(L_{eq2} - C_2 R_{eq2}^2 - C_2 L_{eq2}^2 \omega^2 + C_2^2 L_{eq2} R_{c2B}^2 \omega^2)}{R_{eq2} + C_2^2 R_{c2B} R_{eq2} \omega^2 (R_{c2B} + R_{eq2}) + C_2^2 L_{eq2}^2 R_{c2B} \omega^4} \end{aligned} \quad (5.10)$$

Figure 5.4 (a)-(d) plot the calculated and simulated tank Q at resonant frequencies ω_L and ω_H for Mode A and Mode B with a set of normal tank parameters at target frequency range: $L_1=140$ pH, $C_T=230$ fF, $L_3=126$ pH, $C_3=20$ fF, $Q_{L1}=Q_{L2}=Q_{L3}=20$, $Q_{c1}=Q_{c2}=Q_{c3}=15$ at 31 GHz, and $n=0.9$. For comparison, Q of conventional single LC -tank with same component Q_s (i. e., $Q_L=20$, $Q_c=15$ at 31 GHz) is plotted in dashed lines. The trend of calculated tank Q matches well with the simulated tank Q at the target resonant frequency ω_L which validates the derivation. The discrepancy between the calculated and simulated tank Q at ω_H is mainly due to the approximation procedure during the deduction of resonant frequencies. Comparing to the conventional single LC -tank, the tank Q at lower resonant frequency $Q_A(\omega_L)$ and $Q_B(\omega_L)$ can be both enhanced when k and α are properly selected, while the tank Q at the higher resonant frequency $Q_A(\omega_H)$ and $Q_B(\omega_H)$ are always degraded. Since the

target resonant frequency for both Mode A and Mode B of proposed VCO is the lower resonant frequency ω_L of tank, the tank Q and phase noise of VCO can be improved for both of modes. Furthermore, for diverse values of α , $Q_A(\omega_L)$ and $Q_B(\omega_L)$ are all increased with the increasing of k , therefore the strongly coupled transformer with large k in proposed VCO is able to better enhance the tank Q at the lower resonant frequency compared to the previous dual-mode VCOs with low k transformer.

Figure 5.5: Feedback system of the proposed VCO.

5.2.3 Oscillation Stability

For VCO with transformer-based LC -tanks which has more than one resonant frequency, it needs to avoid the potential stability problem that the oscillation could jump from one equilibrium oscillation frequency to the other with some disturbance [45]. Stable oscillation at only the target frequency is highly desired.

As shown in Figure 5.5, the open loop transfer functions of proposed VCO are $H(s)=g_{m1}Z_{in,A}$ and $H(s)=g_{m2}Z_{in,B}$ for Mode A and Mode B. To start oscillation, the barkhausen criteria should be satisfied which is the open loop gain $|H(s)|=g_{m1/2}|Z_{in,A/in,B}|\geq 1$, and $\angle H(s)$ is 0 or 180° [30]. In this work, $\angle H(s)$ is 0 at both ω_L and ω_H . Therefore, the magnitude of tank impedance ($|Z_{in,A}|$ or $|Z_{in,B}|$) will dominate the start-up of oscillation. According to [50], one necessary condition for the oscillation only occurring at ω_L is that the impedance magnitude peak at ω_L is larger than that at ω_H . Specifically, it is $|Z_{in,A}(\omega_L)| > |Z_{in,A}(\omega_H)|$ for Mode A and $|Z_{in,B}(\omega_L)| > |Z_{in,B}(\omega_H)|$ for Mode B. If the oscillation is free to choose equilibrium point,

when $|Z_{in,A}(\omega_L)| \gg |Z_{in,A}(\omega_H)|$ and $|Z_{in,B}(\omega_L)| \gg |Z_{in,B}(\omega_H)|$, the oscillations for Mode A and Mode B are more probable at ω_L rather than at ω_H . In another word, large ratio of the impedance magnitude peaks at ω_L and ω_H can help to increase oscillation stability at ω_L .

Figure 5.6: Plot of (a) $|Z_{in,A}(\omega_L)|/|Z_{in,A}(\omega_H)|$ in 10log scale for Mode A, and (b) $|Z_{in,B}(\omega_L)|/|Z_{in,B}(\omega_H)|$ in 10log scale for Mode B.

Figure 5.6 (a) and (b) plot the ratios of tank impedance magnitude peaks $|Z_{in,A}(\omega_L)|/|Z_{in,A}(\omega_H)|$ and $|Z_{in,B}(\omega_L)|/|Z_{in,B}(\omega_H)|$ in 10log scale, using the same component values as in Figure 5.4. Apparently, both $|Z_{in,A}(\omega_L)|/|Z_{in,A}(\omega_H)|$ and

$|Z_{in,B}(\omega_L)| / |Z_{in,B}(\omega_H)|$ are increased with the increasing of k , which implies that transformer with large k is able to facilitate the stability of oscillation for both modes at the lower resonant frequency ω_L . For Mode A, $|Z_{in,A}(\omega_L)| / |Z_{in,A}(\omega_H)|$ is increased with the increasing of α for a fixed k , and $|Z_{in,A}(\omega_L)| / |Z_{in,A}(\omega_H)|$ for all k values are always larger than 1 after $\alpha > 0.5$. On the contrary, for Mode B, $|Z_{in,B}(\omega_L)| / |Z_{in,B}(\omega_H)|$ is reduced with the increasing of α , and when $\alpha < 0.5$, $|Z_{in,B}(\omega_L)| / |Z_{in,B}(\omega_H)|$ for all k values are always larger than 1. Although both k and α could affect the ratios of tank impedance magnitude so as to influence the stability of oscillations, since the different values of α in Mode A and Mode B are related to the design of cross-coupled pair, it is better to reserve more freedoms for the choice of α by adopting large k . For instance, supposing the requirements of tank impedance ratios for stable oscillation at ω_L are $|Z_{in,A}(\omega_L)| > 4|Z_{in,A}(\omega_H)|$ and $|Z_{in,B}(\omega_L)| > 4|Z_{in,B}(\omega_H)|$, if $k=0.2$, it requires $0.6 < \alpha < 1$ for Mode A and $0 < \alpha < 0.4$ for Mode B, however, if $k=0.8$, the range of α for Mode A and Mode B are enlarged to $0.3 < \alpha < 1$ and $0 < \alpha < 0.6$ respectively.

In previous transformer-based dual-mode VCOs [43, 45-49], to cope with the potential stability problem calls for low k transformer, however, low k would limit the enhancement or even degrade the tank Q at lower resonant frequency of tank. Differently, in proposed VCO, the strongly coupled transformer with large k is able to simultaneously increase the oscillation stability and tank Q at the target resonant frequency for both modes [Figure 5.4, Figure 5.6].

5.2.4 High Q Active Capacitor

Active capacitor which provides negative input series resistance was introduced into active filter designs to compensate the loss of other components [96, 97]. High Q active capacitor based on cross-coupled pair was reported in [98]. In proposed VCO, the special configuration of switchable coupled VCO-cores and alternative operation

of two cores not only provide dual-mode operation but also enable the utilization of active capacitor. When one VCO-core is switched on to sustain oscillation, the cross-coupled pair of the switched off VCO-core is able to act as a high Q active capacitor. Different from the active capacitor used in filter, the current consumption of active capacitor in this work is reduced by biasing the cross-coupled pair in the region where the input conductance is still positive and in the vicinity of zero. In that case, the Q of active capacitor can be greatly enhanced while consuming very small current.

Figure 5.7: Cross-coupled pair and transistor model of BJT.

Based on the transistor model of BJT shown in Figure 5.7, the input admittance of cross-coupled pair $Y_{in,ccp}$ can be given by

$$Y_{in,ccp} = \frac{1}{2r_o} + \frac{4Z_\pi + Z_\mu + r_b + g_m r_b Z_\pi - g_m r Z_\mu Z_\pi}{2(r_b Z_\mu + r_b Z_\pi + Z_\mu Z_\pi)} \quad (5.11)$$

where $Z_\pi = r_\pi / (1 + j\omega C_\mu r_\pi)$, and $Z_\mu = 1 / j\omega C_\mu$. C_μ is the junction capacitance between base and collector terminals, and C_π is the junction capacitance between base and emitter terminal. With $Y_{in,ccp} = G_{in,ccp} + j\omega C_{in,ccp}$, the input conductance $G_{in,ccp}$ and input parasitic capacitance $C_{in,ccp}$ are given by

$$G_{in,ccp} = \text{Re}[Y_{in,ccp}] \quad (5.12)$$

$$C_{in,ccp} = \frac{\text{Im}[Y_{in,ccp}]}{\omega} \quad (5.13)$$

The Q of $C_{in,ccp}$ is the absolute value of image part of $Y_{in,ccp}$ divided by the real part of $Y_{in,ccp}$, which is given by

$$Q_{in,ccp} = \left| \frac{\omega C_{in,ccp}}{G_{in,ccp}} \right|. \quad (5.14)$$

It is known that g_m and bias current (I_c) of BJT transistor have the relationship of $g_m = qI_c/KT$, where $KT/q = 26$ mV at 300K. The I_c for $G_{in,ccp} = 0$ can be solved as

$$I_{co} = \frac{KT}{q} \frac{(r_b + r_\pi)(r_0 + r_b + r_\pi)}{r_0 r_\pi (r_b + r_\pi) - C_\mu (C_\pi + C_\mu) r_0^2 r_b^2 \omega^2} + \frac{KT}{q} \frac{r_b \omega^2 [C_\mu^2 r_0 r_b + (C_\pi + 2C_\mu)^2 r_0 r_\pi + (C_\pi + C_\mu)^2 r_b r_\pi]}{r_0 (r_b + r_\pi) - C_\mu (C_\pi + C_\mu) r_0^2 r_b^2 \omega^2} \quad (5.15)$$

When $I_c \rightarrow I_{co}$ and $I_c < I_{co}$, $G_{in,ccp}$ can be reduced and approaches to zero. In that case, $Q_{in,ccp}$ can be greatly enhanced, and the cross-coupled pair acts as a high Q active capacitor. Figure 5.8 shows the simulated $Q_{in,ccp}$ and $C_{in,ccp}$ when I_c is increased from 0 to 0.5 mA at 30 GHz, where the emitter length of BJT transistor is 6 μm . The high Q value of more than 250 can be obtained when I_c is 270 μA , and, the input capacitance $C_{in,ccp}$ for $I_c = 270$ μA is only changed by 2 fF (from 32.6 to 34.6 fF) compared to that for $I_c = 0$.

Therefore, to get high Q of active capacitor, the bias current of the VCO-core in OFF state (I_{off}) can be increased from 0 to $2I_{co}$. Since the variation of capacitance as I_{off} increases from 0 to $2I_{co}$ is negligible, the VCO operation frequency is nearly the same with that when the transistor is completely off. Thus, we still denote this state as OFF state. The active capacitor is in parallel connection with the LC -tank, thus the high Q of active capacitor can help to enhance the tank Q and also improve the phase noise performance of VCO.

Figure 5.8: Quality factor and capacitance of active capacitor versus the bias current of transistor.

5.3 Circuit Design and Implementation

From the above analysis, it can be seen that selecting proper values for α_A , α_B , $C_{T,A}$, $C_{T,B}$ and k is essential to design a VCO with the proposed topology. The next step involves the design of the triple-coil transformer with proper coupling coefficient. Then, the cross-coupled pairs, such as the size, bias current can be designed and optimized with certain requirement of current density.

5.3.1 Considerations of Parameter Selection

Based on Figure 5.3, the equations about tank capacitors and design parameters can be given by

$$C_{v1} + C_{on1} + C_{v2} + C_{off2} = C_{T,A} \quad (5.16)$$

$$C_{v1} + C_{on1} = \alpha_A C_{T,A} \quad (5.17)$$

$$C_{v1} + C_{off1} + C_{v2} + C_{on2} = C_{T,B} \quad (5.18)$$

$$C_{v1} + C_{off1} = \alpha_B C_{T,B} \quad (5.19)$$

We also can define the difference of C_{on} and C_{off} as $\Delta C_{p1}=C_{on1}-C_{off1}$, and $\Delta C_{p2}=C_{on2}-C_{off2}$. From (5.20) and (5.21), we can get

$$\Delta C_{p1}-\Delta C_{p2}=C_{T,A}-C_{T,B} \quad (5.20)$$

$$\Delta C_{p1}=\alpha_A C_{T,A}-\alpha_B C_{T,B} \quad (5.21)$$

Therefore, if α_A , α_B , $C_{T,A}$ and $C_{T,B}$ are known, ΔC_{p1} and ΔC_{p2} can be calculated through (5.20) and (5.21). Then, the transistors of cross-coupled pairs and bias current can be designed according to ΔC_{p1} and ΔC_{p2} . First of all, the values of design parameters α_A , α_B , $C_{T,A}$, $C_{T,B}$ need to satisfy the requirement of Δf , where $\Delta f=f(\alpha_B, C_{T,B})-f(\alpha_A, C_{T,A})$. Then, since ΔC_{p1} and ΔC_{p2} are determined by bias current of cross-coupled pair, the ranges of α_A , α_B , $C_{T,A}$ and $C_{T,B}$ can be restrained for optimized power consumption. Finally, these ranges can be further restrained to satisfy the requirement of C_{v1} and C_{v2} .

To cover the 60 GHz unlicensed band which is from 57 GHz to 66 GHz, the oscillation frequency range of the VCO before the frequency doubler should be from 28.5 to 33 GHz. Supposing the frequency tuning ranges of the two modes are equal, then it will require $\Delta f \geq 2.25$ GHz, and $f(\alpha_A, C_{T,A})$ needs to be smaller than 29.625 GHz, $f(\alpha_B, C_{T,B})$ needs to be larger than 31.875 GHz. In our design, we make our targets as $f(\alpha_A, C_{T,A}) = 29.5$ GHz, $f(\alpha_B, C_{T,B}) = 32$ GHz to provide more tolerance to the circuit against the PVT variation.

Based on (5.21), Figure 5.9 plots the available α and C_T satisfying $f(\alpha, C_T)=32$ GHz and $f(\alpha, C_T)=29.5$ GHz, where the required α_A , $C_{T,A}$ can be chosen from the lines of $f=29.5$ GHz, and α_B , $C_{T,B}$ can be chosen from the lines of $f=32$ GHz. With different k of transformer, those lines are different, thus the range of k should be specified firstly. Although large k of transformer facilitates the enhancement of tank Q and stable oscillation at target resonant frequency, the selection of k also needs to consider $C_{T,A}$

and $C_{T,B}$. Since $\Delta C_{p1} - \Delta C_{p2} = C_{T,A} - C_{T,B}$, the increased value of $C_{T,A} - C_{T,B}$ implies that larger parasitic capacitance of cross-coupled pair will be needed, and thus more DC current and larger size transistor will be required. Therefore, $C_{T,A} - C_{T,B}$ should be minimized. As shown in Figure 5.9, as k increases from 0.5 to 0.8, the lines of $f=32$ GHz and $f=29.5$ GHz both gradually become flat, resulting in a decreasing of maximum value of $C_{T,B}$. Since the minimum value of $C_{T,A}$ is not changed, the minimum value of $C_{T,A} - C_{T,B}$ will be increased. It can be seen in Figure 5.9, $\min(C_{T,A} - C_{T,B}) < 0$ when $k=0.7$, but $\min(C_{T,A} - C_{T,B}) > 0$ when $k=0.8$. Therefore, in this case, k needs to be smaller than 0.8.

Figure 5.9: C_T versus α for $f=32$ GHz and $f=29.5$ GHz with different k values, when $L_1=140$ pH, $n=0.9$.

For the selection of α_A and α_B , the stability issue should be considered. Referring to Section 5.2.3, the choosing of α will affect the ratios of tank impedance magnitude, and thus influence oscillation stability. If $k=0.7$, it needs $0.4 < \alpha_A < 1$ and $0 < \alpha_B < 0.5$ to make the ratios of tank impedance magnitude at ω_L to ω_H larger than 4. Besides, the range of α_A and α_B can be further restrained by C_{v1} and C_{v2} . Supposing C_{v1} and C_{v2} need to be at least larger than 30 fF, which is a small capacitor value for this frequency, then from (5.20) to (5.21), we can get

$$\alpha_A C_{T,A} > 30 \text{ fF} + C_{on1} > 30 \text{ fF} \quad (5.22)$$

$$(1 - \alpha_A) C_{T,A} > 30 \text{ fF} + C_{off2} > 30 \text{ fF} \quad (5.23)$$

$$\alpha_B C_{T,B} > 30 \text{ fF} + C_{off1} > 30 \text{ fF} \quad (5.24)$$

$$(1 - \alpha_B) C_{T,B} > 30 \text{ fF} + C_{on2} > 30 \text{ fF} \quad (5.25)$$

For $k=0.7$, $0.4 < \alpha_A < 1$, $0 < \alpha_B < 0.5$, minimum value of $C_{T,A}$ is 210 fF, and $C_{T,B}$ is 200 fF. Based on (5.22)-(5.25), the ranges of α_A and α_B for smallest C_{v1} and C_{v2} are $0.14 < \alpha_A < 0.86$, and $0.15 < \alpha_B < 0.85$ with $C_{T,A}=210$ fF and $C_{T,B}=200$ fF. Therefore, by considering the requirement of C_{v1} and C_{v2} (e. g, 30 fF), the ranges of α_A and α_B shrink to $0.4 < \alpha_A < 0.86$ and $0.15 < \alpha_B < 0.5$. In addition, another rule for choosing α_A and α_B is that $\alpha_A - \alpha_B$ needs to be as small as possible in order to minimize ΔC_{p1} , and thus saving power consumption [Equation (5.21)].

5.3.2 Triple-coil Transformer

In this work, the concentric coupling method is used for transformer primary and secondary coil for its moderate coupling coefficient compared to other coupling methods, such as the stacked coupling and the inter-wound coupling [99]. Moreover, the coupling coefficient of concentric coupled transformer can be easily designed by varying the distance between metal traces.

Figure 5.10: Structure of the transformer.

The front view and side view of the triple-coil transformer is shown in Figure 5.10. L_1 and L_2 are concentrically coupled using the top metal layer to keep far away from the lossy silicon substrate. Since the oscillation signals of the VCO-cores are coupled to the doubler by L_3 , it is better to make the coupling strength between L_1 and L_3 same with that between L_2 and L_3 . Thus, L_3 is stacked under the gap between L_1 and L_2 . This structure also can reduce the coupling capacitance brought by stacked coupling, such that increase the self-resonant frequency of transformer.

The outer dimension of transformer is 142 μm , and the metal trace width of L_1 and L_2 are 12.5 μm and 11.5 μm , respectively. The distance between metal trace of L_1 and L_2 is 2.3 μm . The simulated self-inductance for L_1 , L_2 , L_3 are 140 pH, 131 pH, and 137 pH at 30 GHz, respectively. The coupling coefficient k_{12} , k_{13} , and k_{23} are 0.59, 0.69, and 0.66 respectively. Although k_{12} , k_{13} , and k_{23} are not identical, which is different from the assumption in the deduction, the major coupling coefficient influencing the oscillation frequency is k_{12} . Assuming those coupling coefficients as identical has simplifies the deduction and confers insight to circuit mechanism.

5.3.3 Design of Cross-coupled Pairs

The size of transistors, bias current can be optimized for a designed triple-coil transformer. When $k=0.59$, $n=0.93$, the relationship between C_T and α for $f=32$ GHz and $f=29.5$ GHz is plotted in Figure 5.11. Based on the guidelines for parameters selection in Section 5.3.1, the ranges for α_A and α_B , where $0.5 < \alpha_A < 0.86$ and $0.16 < \alpha_B < 0.5$, are marked. We can choose $\alpha_A=0.6$ and $\alpha_B=0.45$ as a good trade-off between small $\alpha_A - \alpha_B$ and $C_{T,A} - C_{T,B}$, because $C_{T,A}$ is decreased with the increasing of α_A at the target range, $\alpha_A=0.6$ would be a moderate value. Meanwhile, $\alpha_B=0.45$ corresponds to the peak value of $C_{T,B}$, such that both $\alpha_A - \alpha_B$ and $C_{T,A} - C_{T,B}$ can be very small. Then, from $\alpha_A=0.6$ and $\alpha_B=0.45$, $C_{T,A}=264$ fF and $C_{T,B}=231$ fF are obtained.

Substituting α_A , α_B , $C_{T,A}$, and $C_{T,B}$ to (5.20) and (5.21), there are $\Delta C_{p1}=54$ fF, $\Delta C_{p2}=21$ fF.

Figure 5.11: C_T versus α for $f=32$ GHz and $f=29.5$ GHz with different k values, when $k=0.59$, $n=0.93$, $L_1=140$ pH.

Figure 5.12: f_T and minimum noise figure (NF_{min}) versus current density.

ΔC_{p1} and ΔC_{p2} are determined by the transistors size and bias current. Generally, for a mm-wave VCO design, a proper current density I_C/L_E of transistors needs be chosen for a good f_T and minimum noise figure (NF_{min}). Figure 5.12 shows f_T and NF_{min} versus current density for the target process. The current density for best f_T is $I_C/L_E=1.4$ mA/ μ m, and for best NF_{min} is $I_C/L_E=0.4$ mA/ μ m. Thus, to get a good trade-

off between f_T and NF_{min} , $I_{C1}/L_{E1}=1$ mA/ μ m and $I_{C2}/L_{E2}=0.8$ mA/ μ m for the cross-coupled pairs in Core1 and Core2 are selected, where the $NF_{min}<2.4$ dB, and $f_T>165$ GHz.

Figure 5.13: (a) Contour lines of ΔC_p versus emitter length and bias current, where $I_B/L_E=1$ mA/ μ m, $I_B/L_E=0.8$ mA/ μ m are marked. (b) C_{off} with the changing of emitter length.

Figure 5.13 (a) plots the contours of ΔC_p with the changing of bias current (I_c) and emitter length (L_E) of BJT, where the line of current density $I_C/L_E=1$ mA/ μ m and $I_C/L_E=0.8$ mA/ μ m are marked. Figure 5.13 (b) shows C_{off} with the changing of L_E . Thereby, from junction between $\Delta C_{p1}=54$ fF and $I_C/L_E=1$ mA/ μ m, along with $\Delta C_{p2}=21$

fF and $I_C/L_E=0.8$ mA/ μm , the required $I_{C1}=6.4$ mA, $L_{E1}=6.4$ μm , $I_{C2}=3.1$ mA, and $L_{E2}=3.9$ μm can be obtained. Then, with L_{E1} and L_{E2} , the corresponding $C_{\text{off}1}=34$ fF and $C_{\text{off}2}=22$ fF can be found from Figure 5.13(b). Therefore, C_{v1} and C_{v2} can be solved as $C_{v1}=70$ fF and $C_{v2}=84$ fF by (5.20) and (5.21). It should be noted that parasitic capacitance of transformer is loaded on tank, and it can be absorbed into C_{v1} and C_{v2} . The varactors with multi-fingers and minimum gate width, length are utilized in this design, and C_{v2} is formed by an MIM-cap in parallel connection with a MOS varactor to enhance Q . With implemented tank, the simulated impedance magnitude ratios at ω_H and ω_L are $Z_{\text{in},A}(\omega_L)/Z_{\text{in},A}(\omega_H)=8$, $Z_{\text{in},B}(\omega_L)/Z_{\text{in},B}(\omega_H)=5$.

Figure 5.14: Chip photomicrograph of the fabricated VCO.

5.4 Measurement Results

The proposed VCO is implemented in a 0.18 μm SiGe BiCMOS process with 6 metal layers. The chip photomicrograph of VCO is shown in Figure 5.14. Shielding is used under the transformer to enhance the isolation to substrate. The total chip size including the I/O pads is 0.503×0.69 mm². The bias current source of the cross-coupled pair is realized by MOS transistors to save the voltage headroom. With a 1.2 V supply voltage, the two VCO-cores consume 12.8 mA to 12.95 mA current for

Mode A, and 6.24 mA to 6.39 mA for Mode B. The power consumption of the frequency doubler is 3.6 mW.

Figure 5.15: Measured oscillation frequency.

Figure 5.16: Phase noise measurement setup.

The measured and simulated oscillation frequency with the variation of tuning voltage (V_T) for Mode A and Mode B is shown in Figure 5.15. The measured frequency tuning range of VCO is 10.3 GHz (17%), from 55.7 GHz to 60.5 GHz for Mode A, and from 59.9 GHz to 66 GHz for Mode B. The measured oscillation frequency is quite close to the simulated results. Compared to the simulated results, the oscillation frequency is shifted down by about 200 MHz (less than 0.4% over 60 GHz). The setup for phase noise measurement is shown in Figure 5.16, where two cascaded amplifiers V-LNA-50-75-4 are adopted to amplify the output signal and compensate the cable loss and harmonic mixer loss, and Signal Source Analyzer (SSA) E5052B is used to measure the phase noise. Figure 5.17 shows the phase noise at 1MHz offset

versus the bias current of off-status cross-coupled transistors ($I_{c,off}$). With $I_{c,off}$ increased from 0 to 0.15 mA, the phase noise is reduced, and the improvement on phase noise is roughly increased with the increasing of V_T . The reason should be that the Q of varactor at small V_T is much lower than that of active capacitance, so the low Q of varactor is the major factor to limit the phase noise at small V_T . When V_T is increased, the Q of varactor is increased, thus the improvement of phase noise is also increased. Figure 5.18 shows the measured and simulated phase noise over the entire frequency tuning range when setting $I_{c,off}=0.15$ mA. The measured phase noise is degraded less than 2 dB compared to simulated phase noise, which is acceptable for 60 GHz VCO. The measured phase noise at 1 MHz is from -91.4 dBc/Hz to -93.45 dBc/Hz for Mode A, and from -87.6 dBc/Hz to -89.4 dBc/Hz for Mode B. The phase noise variation on the frequency tuning range for each mode is less than 2 dB. The worst and best phase noise over the frequency tuning range are shown in Figure 5.19 (a) and (b) with the changing of offset frequency. The $1/f^3$ and $1/f^2$ regions are shown by -30 dB/decade and -20/dB/decade lines. Since the MOS transistors are used for tail current source, the flick noise of tail transistor can up-convert to phase noise (AM-to-PM noise) and contribute to the phase noise at low frequency offset.

The measurement of output power is performed with a PNA-X network analyzer N5247A. The measured output power is from -32.8 dBm to -28.8 dBm over the frequency tuning range after calibration, while the simulated output power is above -5 dBm. The measured output power is degraded a lot mainly due to the frequency doubler. The frequency doubler utilizes the 2rd harmonic frequency which is at 60 GHz. However, the bipolar transistor in this process is only modeled to 50 GHz. Another reason might be that the practical output swing of VCO core is lower than that in the simulation. Due to the Class-C operation, the doubler gain can drop quickly as

the input swing decreases. Nevertheless, using the frequency doubler can reduce VCO design frequency by half and allows better trade-off between low phase noise and wide tuning range. Besides, the topology of proposed VCO with frequency doubler omits 60 GHz frequency divider in PLL, which can significantly reduce the PLL design complexity. In order to drive mixer/modulator in RF front-end, driven amplifier can be added.

Figure 5.17: Phase noise at 1 MHz offset frequency with I_{off} .

Figure 5.18: Measured phase noise at 1 MHz offset versus V_T .

(a)

(b)

Figure 5.19: Measured phase noise as a function of offset frequency, (a) Mode B, $f_0=61.4$ GHz, and (b) Mode A, $f_0=60.1$ GHz.

TABLE 5-1 PERFORMANCE SUMMARY AND COMPARISONS

Ref.	Pub.	Tech.	Freq. (GHz)	TR (%)	P _{out} (dBm)	P _{dc} _core (mW)	P _{dc} _buff (mW)	PN@ 1MHz (dBc/Hz)	FOM _T ⁽²⁾ (dBc/Hz)
[100]	TCAS1 2012	90nm CMOS	52.2 ~61.3	16.7	-10	8.7	5.6	-94 ~ -118.7 ⁽¹⁾	-189
[12]	JSSC 2013	90nm CMOS	56.2 ~62.2	10	-3.4	12	21.6	-90.5~ -93	-178
[101]	RFIC 2013	40nm CMOS	50.7 ~57.5	12.6	--	24	--	-86.5 ~ -101.8	-184
[103]	MWCL 2011	65nm CMOS	57.6 ~60.8	5.4	-0.9	16.5	16.5	-83 ~ -90.3	-168
[102]	RFIC 2012	0.13 μm BiCMOS	60.9 ~63.7	4.5	10	39	93.6	-102 ~ -106	-179
[41]	RFIC 2013	0.13 μm BiCMOS	73.9 ~83.5	12.1	--	41	--	-111 ~ -114.5 ⁽¹⁾	-178
[13]	TMTT 2013	0.13 μm BiCMOS	72.5 ~76.1	4.86	2	65	20	-94 ~ -99.3	-172
[104]	ISSCC 2013	0.13 μm BiCMOS	28 ~37.8	30	--	10	--	-103.6 ⁽³⁾	-193.5
[14]	JSSC 2007	0.18 μm CMOS	34.4 ~41.9	20	-9.1	27	15	-100.2 ⁽³⁾	-183.9
This work		0.18 μm BiCMOS	55.7 ~66	17.2	-30	19.1/ 11.2	0	-87.5~ -93.5	-181

(1)Phase noise (PN) is at 10 MHz offset.

(2) FOM_T is calculated using the best phase noise case.

(3) Average phase noise across the TR.

The overall performance of the proposed VCO is listed in TABLE 5-1 and compared to the recent mm-wave VCOs [12-14, 41, 100-104]. To compare with these VCOs around 30 GHz [14],[104], the frequency doubler should be excluded. Then, the power consumption of our proposed work is 15.5 mW/7.6 mW for Mode A/B, and the phase noise would be 6dB lower (i.e., -93.5~-99.5 dBc/Hz). A commonly used figure of merit FOM_T which takes into account phase noise and tuning range as well as power consumption is adopted in the comparison. The FOM_T is defined as

$$\text{FOM}_T = L(f_m) - 20 \log \left(\frac{f_0}{f_m} \right) + 10 \log (P_{DC}) - 20 \log \left(\frac{\text{FTR}}{10\%} \right) \quad (5.26)$$

where $L(f_m)$ is the phase noise from the oscillator frequency (f_0) at a frequency offset of f_m , and P_{DC} is the DC power consumption of VCO in milliwatt, and FTR stands for the frequency tuning range [100, 105, 106]. The proposed VCO achieves a wide tuning range, and also competitive phase noise compared to other works in more advanced technologies, demonstrating the merits of the proposed topology.

Although [100] and [101] have better FOM_T , the variation of phase noise when tuning the frequency is much larger. Benefiting from the tank Q enhancement for both modes, good phase noise over the whole tuning range are achieved in our proposed work. Though the VCO output is single-ended at 60 GHz, we may use a balun to convert the single-ended output to a differential signal for transceivers requiring differential LOs. Passive balun based on transformer, or active balun [107] which can also serve as a drive amplifier can be used.

5.5 Summary

In this chapter, a new dual-mode VCO topology with the switchable coupled VCO-cores are presented and successfully demonstrated. The proposed topology utilizing the parasitic capacitances of cross-coupled pair to realize dual-mode operation is particularly suitable for VCO design at mm-wave frequency. Comparing to conventional transformer-based dual-mode VCOs, the proposed topology allows using large k transformer to simultaneously enhance tank Q and increase the oscillation stability for both modes. With the proposed VCO topology, better design compromise between wide frequency tuning range and low phase noise can be achieved.

Chapter 6

A V-Band Wide Locking Range Divide-by-4 Injection-locked Frequency Divider

6.1 Introduction

With the emerging of mm-wave frequency applications such as WPAN and image sensing, high performance frequency synthesizers are highly demanded by mm-wave transceivers [16]. For PLL-based frequency synthesizers, a frequency divider is a main building block. Usually, a divider chain consisting of a numbers of cascaded frequency dividers is used to obtain the required division ratio.

In the divider chain, the first-stage divider is the most challenging [15], because it should be able to operate as fast as VCO and provide a wide enough operation range to support the entire tuning range of VCO. In addition, due to the highest operation frequency of the divider chain, the first stage divider is the most power-hungry. Therefore, considering the power consumption as well as the chip area, it is attractive to design the first stage divider with high division ratio [16-18]. The injection-locked frequency divider (ILFD) is an attractive solution for first-stage divider because of its

high operation frequency and low power consumption [7, 15]. However, the ILFD inherently suffers from narrow locking range. Many efforts have been made to improve the locking range of divide-by-2 ILFD, such as using the shunt peaking technique [19], and frequency tracking technique [20]. Recently, the ILFDs with division ratio larger than 2 have been reported, for instance, the divide-by-3 ILFD in [21], the divide-by-4 ILFD in [22], and the divide-by-5 ILFD in [23]. However, comparing to divide-by-2 ILFD, the locking range of high division ratio ILFD is much narrower due to the low power level of high order harmonic components[73].

Figure 6.1: Block diagram of the divide-by-4 ILFD in [16].

In [16], the third harmonic component of a divide-by-4 ILFD is boosted by using an *LC*-tank of which the lower resonant frequency locates at the fundamental frequency of the ILFD and the higher resonant frequency locates at the third harmonic frequency of the ILFD. The block diagram of the ILFD is shown in Figure 6.1. This method can improve the locking range of ILFD. However, the large component of third harmonic at the output of ILFD could cause wrong operation of the following stages. Moreover, to avoid stability problem, the impedance peak at the third harmonic frequency need be smaller than that at the fundamental frequency, which would limit the improvement of locking range.

In this chapter, a novel topology of mm-wave divide-by-4 ILFD employing two positive feedback loops (i.e., injection-loop and output-loop), has been proposed. By properly design the LC -tank, the injection-loop can enhance the third harmonic component to facilitate the fundamental mixing and improve the locking range, meanwhile the output-loop can assist the ILFD to achieve a stable oscillation at the fundamental frequency and also suppress the third harmonic component at output, allowing further enhancement of the third harmonic component in the injection-loop. The proposed divide-by-4 ILFD has demonstrated a 14.9% locking range from 60.2 GHz to 69.9 GHz, while consuming only 4.8 mW DC power in a 65nm CMOS process.

This chapter is organized as follows. The schematic and operation concept of the ILFD is given in Section 6.2, together with the analysis of locking range and details of the circuit implementation. The experimental results are shown in Section 6.3, and the conclusions are given in Section 6.4.

Figure 6.2: Schematic of the proposed divide-by-4 ILFD.

Figure 6.3: Operation concept of the proposed divide-by-4 ILFD.

6.2 Proposed Divide-by-4 ILFD

6.2.1 Concept and Schematic of the Proposed ILFD

Figure 6.2 shows the schematic of the proposed divide-by-4 ILFD, where a two-port *LC*-tank is used. Transistors M1~M4 form two cross-coupled pairs (i.e., CCP1, CCP2) connecting to the two ports of the *LC*-tank respectively. The injection transistor M5 is connected in shunt with CCP2 to perform the direct injection which can increase injection efficiency. The output of the ILFD is extracted at the drain node of CCP1. The operation concept of the proposed ILFD is illustrated in Figure 6.3. The ILFD can be viewed as two oscillation feedback loops coupled by a two-port *LC*-tank. The CCP1 is connected to Port1 of the *LC*-tank forming the output-loop, while the CCP2 and the injector which is modeled as a mixer are connected to the port2 of the *LC*-tank forming

the injection-loop. The two-port LC -tank in the ILFD is designed to make the resonant frequencies of LC -tank locate at the fundamental and third harmonic frequency of the ILFD. If the peaks of impedance looking into the Port2 of the tank (Z_{22}) are comparable at the fundamental and the third harmonic frequency, then the third harmonic component in the injection loop can be boosted. Since the third harmonic component can assist the fundamental mixing which has much higher efficiency than harmonic mixing, the locking range can be improved. Meanwhile, in the output-loop, for the impedance looking into Port1 of tank (Z_{11}), if the impedance peak at the third harmonic frequency is very small and can be ignored comparing to that at fundamental frequency, then the third harmonic component at output would be significantly suppressed, eliminating the effects on the following stages. In addition, different from [16], since the output-loop of the proposed ILFD can actually assist to achieve stable oscillation at fundamental frequency, the proposed ILFD allows the impedance peak of Z_{22} at the third harmonic frequency as high as that at the fundamental frequency, which can further enhance the third harmonic component. Benefiting from the special topology, the third harmonic component can be boosted in the injection-loop and suppressed in the output-loop, so that the locking range of the proposed ILFD can be improved without suffering from large component of the third harmonic at the output.

The 2-ports LC -tank is crucial for the proposed ILFD. As shown in Figure 6.2, high order LC network composed of L_P , L_{S1} , L_{S2} , C_S is used as the LC -tank to provide the desired impedance characteristic. It should be noted that the design of impedance of LC -tank also needs to consider the parasitic capacitance of transistor and inductors. The implementation of the LC -tank and the detail of circuit design will be given in Section 6.2.3.

6.2.2 Locking Range Analysis

Figure 6.4: (a) Currents and voltages at the two ports of *LC*-tank, (b) Phasor diagram of Equation (6.6) (c) Phasor diagram of Equation (6.7).

Figure 6.4 (a) shows the currents and voltages at the two ports of *LC*-tank. To deduce the locking range, we denote the drain node voltage of CCP1 as V_{o1+} , V_{o1-} , and $V_{o1} = V_{o1+} - V_{o1-}$, and the drain node voltage of CCP2 as V_{o2+} , V_{o2-} , and $V_{o2} = V_{o2+} - V_{o2-}$. When the oscillation frequency of ILFD is locked to ω , V_{o1+} , V_{o1-} , V_{o2+} , and V_{o2-} can be expressed as

$$V_{o1+}(t) = V_{dc} + A_{1,\omega} \cos(\omega t + \beta) \quad (6.1)$$

$$V_{o1-}(t) = V_{dc} - A_{1,\omega} \cos(\omega t + \beta) \quad (6.2)$$

$$V_{o2+}(t) = V_{dc} + A_{2,\omega} \cos(\omega t) + A_{2,3\omega} \cos(3\omega t + \varphi) \quad (6.3)$$

$$V_{o2-}(t) = V_{dc} - A_{2,1\omega} \cos(\omega t) - A_{2,3\omega} \cos(3\omega t + \varphi) \quad (6.4)$$

where V_{dc} is the common mode voltage at the drain of CCP1 and CCP2, β is the phase difference of fundamental component of V_{o1} and V_{o2} , φ is the phase difference between the fundamental and third harmonic component of V_{o2} .

The current flowing into the two ports LC -tank are denoted as I_1 and I_2 , then the voltage and current equation can be given using Z parameters as

$$\begin{aligned} I_1 &= \frac{Z_{22}}{Z_{11}Z_{22} - Z_{12}Z_{21}} V_{o1} - \frac{Z_{12}}{Z_{11}Z_{22} - Z_{12}Z_{21}} V_{o2} \\ I_2 &= \frac{-Z_{21}}{Z_{11}Z_{22} - Z_{12}Z_{21}} V_{o1} + \frac{Z_{11}}{Z_{11}Z_{22} - Z_{12}Z_{21}} V_{o2} \end{aligned} \quad (6.5)$$

When there is no injection signal, the circuit will self-oscillate at the free running frequency ω_0 , I_2 is in phase with V_{o2} , I_1 is in phase with V_{o1} , and the phase shift of LC -tank is zero. When there is an injection frequency 4ω deviated from $4\omega_0$, I_1 will remain in phase with V_{o1} , while I_2 will bear a phase difference of ϕ from V_{o2} , and the oscillation frequency of ILFD will shift from ω_0 , so that the LC -tank can exhibit a phase shift φ_Z at ω to compensate ϕ . Assume Z_{11} , Z_{12} , Z_{21} , and Z_{22} has the same phase shift of φ_Z at ω , then Equation (6.5) in time domain can be expressed as

$$I_1(t) = 2 \left| \frac{Z_{22}}{Z_d} \right| A_{1,\omega} \cos(\omega t + \beta - \varphi_Z) - 2 \left| \frac{Z_{12}}{Z_d} \right| A_{2,\omega} \cos(\omega t - \varphi_Z) \quad (6.6)$$

$$I_2(t) = -2 \left| \frac{Z_{21}}{Z_d} \right| A_{1,\omega} \cos(\omega t + \beta - \varphi_Z) + 2 \left| \frac{Z_{11}}{Z_d} \right| A_{2,\omega} \cos(\omega t - \varphi_Z) \quad (6.7)$$

where $|Z_d| = |Z_{11}Z_{22}| - |Z_{12}Z_{21}|$. As indicated in Figure 6.4 (a), I_1 is in phase with V_{o1} , then I_1 can be expressed as

$$I_1(t) = |I_1| \cos(\omega t + \beta) \quad (6.8)$$

Separating the in-phase and quadrature-phase component of Equation (6.6) and (6.8), we can draw the current phasor diagram as shown in Figure 6.4 (b) and obtain following equation,

$$\begin{aligned} |I_1| \cos(\beta) &= 2 \left| \frac{Z_{22}}{Z_d} \right| A_{1,\omega} \cos(\beta - \varphi_Z) - 2 \left| \frac{Z_{12}}{Z_d} \right| A_{2,\omega} \cos(\varphi_Z) \\ |I_1| \sin(\beta) &= 2 \left| \frac{Z_{22}}{Z_d} \right| A_{1,\omega} \sin(\beta - \varphi_Z) + 2 \left| \frac{Z_{12}}{Z_d} \right| A_{2,\omega} \sin(\varphi_Z) \end{aligned} \quad (6.9)$$

Solving Equation (6.9), then $\cos(\beta)$ and $\sin(\beta)$ can be solved as

$$\cos(\beta) = \frac{2A_{2,\omega} |Z_{12}| (2A_{1,\omega} |Z_{22}| - |I_1| |Z_d| \cos(\varphi_Z))}{4A_{1,\omega}^2 |Z_{22}|^2 - 4A_{1,\omega} \cos(\varphi_Z) |I_1| |Z_{22}| + |I_1|^2 |Z_d|^2} \quad (6.10)$$

$$\sin(\beta) = \frac{2A_{2,\omega} |I_1| |Z_{12}| |Z_d| \sin(\varphi_Z)}{4A_{1,\omega}^2 |Z_{22}|^2 - 4A_{1,\omega} \cos(\varphi_Z) |I_1| |Z_{22}| + |I_1|^2 |Z_d|^2} \quad (6.11)$$

If the phase difference of I_2 and V_{o2} is $\phi = \eta + \varphi_Z$, then Equation (6.7) can be rewritten as

$$|I_2| \cos(\omega t - \eta - \varphi_Z) = -2 \left| \frac{Z_{21}}{Z_d} \right| A_{1,\omega} \cos(\omega t + \beta - \varphi_Z) + 2 \left| \frac{Z_{11}}{Z_d} \right| A_{2,\omega} \cos(\omega t - \varphi_Z) \quad (6.12)$$

As the phase diagram shown in Figure 6.4(c), by separating the component of Equation (6.12) as in-phase with $-\varphi_Z$ and quadrature-phase with $-\varphi_Z$, then $\tan(\eta)$ and $\sin(\eta)$ can be obtained as

$$\begin{aligned} |I_2| \sin(\eta) &= 2 \left| \frac{Z_{21}}{Z_d} \right| A_{1,\omega} \sin(\beta) \\ |I_2| \cos(\eta) &= -2 \left| \frac{Z_{21}}{Z_d} \right| A_{1,\omega} \cos(\beta) + 2 \left| \frac{Z_{11}}{Z_d} \right| A_{2,\omega} \end{aligned} \quad (6.13)$$

With the Equations (6.10), (6.11), (6.13), and $\tan(\phi) = \tan(\eta + \varphi_Z)$ can be rewritten and simplified as

$$\tan(\phi) = \frac{-\sin(\phi_Z)}{\frac{2A_{1,\omega}|I_1||Z_{12}||Z_{21}|}{4A_{1,\omega}^2|Z_{22}| - 4A_{1,\omega}\cos(\phi_Z)|I_1||Z_d| + |I_1|^2|Z_{11}||Z_d|} - \cos(\phi_Z)} \quad (6.14)$$

The phase difference ϕ between I_2 and V_{o2} is produced by the injection signal. Assuming the injection signal is

$$V_{inj}(t) = V_g + A_{inj} \cos(4\omega t + \theta) \quad (6.15)$$

where θ is the phase difference between the input signal and V_{o2} , V_g is the gate DC voltage of M5. The transistor square-law model [69] can be used to expressed the injected current $I_{inj}(t)$, which is given by

$$I_{inj}(t) = \mu C_{ox} \frac{W}{L} \left\{ [V_{inj}(t) - V_{o2-}(t) - V_{th}][V_{o2+}(t) - V_{o2-}(t)] - \frac{1}{2}[V_{o2+}(t) - V_{o2-}(t)]^2 \right\} \quad (6.16)$$

Substituting Equations (6.3)-(6.4) and (6.15) into (6.16), $I_{inj}(t)$ can be rewritten as

$$I_{inj}(t) = 2K \left[V_{ov}A_{2,\omega} \cos(\omega t) + V_{ov}A_{2,3\omega} \cos(3\omega t + \phi) + A_{inj}A_{2,\omega} \cos(4\omega t + \theta) \cos(\omega t) + A_{inj}A_{2,3\omega} \cos(4\omega t + \theta) \cos(3\omega t + \phi) \right] \quad (6.17)$$

where $K = \mu C_{ox} W / L$, $V_{ov} = V_g - V_{dc} - V_{th}$. Considering the frequency component of ω , the in-phase and quadrature-phase component of I_{inj} can be written as

$$\overline{I_{inj,\omega,i}} = \left[2KV_{ov}A_{2,\omega} + KA_{inj}A_{2,3\omega} \cos(\theta - \phi) \right] e^{j0} \quad (6.18)$$

$$\overline{I_{inj,\omega,q}} = KA_{inj}A_{2,3\omega} \sin(\theta - \phi) e^{j90} \quad (6.19)$$

It can be found that the locus of $\overline{I_{inj,\omega}}$ is a circle centered at $(2KV_{ov}A_{2,\omega}, 0)$ with a radius of $KA_{inj}A_{2,3\omega}$ in the complex plane when $\theta - \phi$ changes from 0 to 2π , as shown in Figure 6.5. Since the sum of current at the drain node of CCP2 should be zero as the ILFD is locked at ω , there is

$$\overline{I_2} + \overline{I_{CCP2}} + \overline{I_{inj}} = 0 \quad (6.20)$$

The corresponding phasor diagram is also depicted in Figure 6.5, from which the maximum value of ϕ can be obtained as

$$\phi_{\max} = \arcsin \left(\frac{KA_{inj}A_{2,3\omega}}{|I_{ccp2}| - 2KV_{ov}A_{2,\omega}} \right) \quad (6.21)$$

Figure 6.5: Current phasor diagram at the drain node of CCP2.

Noted that frequency locking occurs at vicinity of free running frequency, ϕ and φ_Y are very small, there are $\sin(\phi) \approx \tan(\phi)$, $\sin(\varphi_Z) \approx \tan(\varphi_Z)$, and $\cos(\varphi_Z) \approx 1$.

$$\tan(\varphi_Z) = \frac{2Q(\omega - \omega_0)}{\omega_0} \quad (6.22)$$

where $\omega - \omega_0$ is the frequency offset of the locking frequency from the free running frequency, Q is the quality factor of LC -tank. Therefore, with (6.21), (6.22), and (6.14), then $LR = 8(\omega - \omega_0)$ can be given by

$$LR = \frac{4\omega_0 KA_{inj}A_{2,3\omega}}{Q(|I_{ccp2}| - 2KV_{ov}A_{2,\omega})} \left(1 - \frac{2A_{1,\omega}|I_1||Z_{12}||Z_{21}|}{4A_{1,\omega}^2|Z_{22}| - 4A_{1,\omega}|I_1||Z_d| + |I_1|^2|Z_{11}||Z_d|} \right) \quad (6.23)$$

Since $|I_1| = |I_{ccp1}| \approx g_{m1}A_{1,\omega}$ and $|I_{ccp2}| \approx g_{m2}A_{2,\omega}$ [69], then the expression of locking range can be further simplified as

$$LR = \frac{4\omega_0 KA_{inj}A_{2,3\omega}}{QA_{2,\omega}(g_{m2} - 2KV_{ov})} \left(1 - \frac{2g_{m1}|Z_{12}||Z_{21}|}{4|Z_{22}| - 4g_{m1}|Z_d| + g_{m1}^2|Z_{11}||Z_d|} \right) \quad (6.24)$$

It can be seen that locking range is strongly depended on the amplitude of third harmonic component $A_{2,3\omega}$. In the conventional divide-by-4 ILFD based on harmonic mixing [73], the LC -tank has only one resonant frequency, so the third harmonic component in the circuit is very small, resulting in a narrow locking range. In this work, the Z_{22} provides high impedance peak at the fundamental and third harmonic frequency of ILFD, the third harmonic component in the injection-loop can be significantly boosted, such that the fundamental mixing which has much higher efficiency than harmonic mixing would assist to achieve divide-by-4 operation. Consequently, the locking range can be greatly improved. On the other hand, the output loop will suppress the third harmonic component, so that eliminate the effect of third harmonic component on the following stages.

6.2.3 Circuit Design and Implementation

The two-port LC -tank is the key block in the proposed ILFD. It needs to exhibit the high impedance peak at both the fundamental and third harmonic frequency of ILFD in injection-loop, and simultaneously provide large rejection of third harmonic component in output-loop. Figure 6.6 (a) shows the structure of the two-port LC -tank in the proposed ILFD. To save chip area, L_p is implemented by a symmetrical inductor, and the coupled inductors L_{S1} and L_{S2} are realized by a 2 turns tapped inductor (L_S). One terminal of L_S is connected to capacitor C_{S1} , while the other terminal is connected to the CCP2 as well as the injection transistor for signal input. The two terminals of L_P are connected to the tap of L_S . Capacitors C_P are shunt with L_P and connected to CCP1 for output the signal after division. The equivalent model of half LC -tank is shown in Figure 6.6(b). C_C represents the coupling capacitance between L_{S1} and L_{S2} . C_{S2} is the parasitic capacitance at Port2 which includes the parasitic capacitance of CCP2 and injection transistor. The parasitic capacitance of CCP1 has been absorbed by C_P during

the design of LC -tank. Based on this model, the resonant frequencies of the LC -tank can be calculated and designed at required frequency (i.e., the fundamental and third harmonic frequency of ILFD). The injection transistor M5 is biased in sub-threshold region ($V_{OV} < 0$) to increase the nonlinear effects. From the locking range expression [Equation 6.24], K should be large to get a wide locking range, thus the size of injection transistor should be large. Also, the size of transistor M3 and M4 has to be small to achieve a small g_{m2} . M1 and M2 are designed with the same size with M3 and M4. The capacitors in the LC -tank are implemented using Vncap for a convenient connection and high Q .

Figure 6.6: (a) Structure of two ports LC -tank, and (b) equivalent model.

The inductors are all implemented using the top two metal layers in shunt connection to reduce the resistive loss and improve Q . Simulated by the High Frequency Structural Simulator (HFSS), L_P , L_{S1} , and L_{S2} have the inductance of 920 pH, 183.5 pH, and 110 pH at 15.7 GHz, respectively. The coupling coefficient between L_{S1} and L_{S2} is 0.16. The simulated Z parameters of the LC -tank are shown in Figure 6.7. The Z_{22} has two high impedance peaks at ω_0 and $3\omega_0$, which means the third harmonic component in the injection-loop can be significantly boosted. At the same time, Z_{11} shows only one high impedance peak at ω_0 , and $Z_{11}(3\omega_0)$ is much smaller than $Z_{11}(\omega_0)$, indicating a good rejection of third harmonic component in the output-loop. Different from [16] where the impedance at $3\omega_0$ have to be smaller than $3/4$ of that at ω_0 to avoid stability problem, in the proposed ILFD topology, $Z_{22}(3\omega_0)$ can be as high as $Z_{22}(\omega_0)$, because the output-loop can help to achieve stable oscillation at fundamental frequency of ILFD.

Figure 6.7: Simulated Z parameters of the two ports LC -tank.

Figure 6.8 plots the simulated spectrum of the signal at Port1 and Port2 of the LC -tank (i.e., V_1 and V_2) when the ILFD is locked. It can be seen that there is a large component of third harmonic of V_2 in the injection loop [Figure 6.8 (a)], which can

facilitate the fundamental mixing and improve the locking range. At the same time, the ILFD output signal V_1 shows 203 mV rejection of third harmonic component compared with the fundamental component in the output-loop [Figure 6.8(b)].

Figure 6.8: Simulated spectrum of signals at (a) drain node of CCP2, and (b) drain node of CCP1.

6.3 Experimental Results

The proposed divide-by-4 ILFD is implemented in a 65nm CMOS process. For the purpose of measurement, inductor loaded common source amplifiers are connected to the output of the proposed ILFD as output buffers. Figure 6.9 shows the chip

micrograph, the total chip size including the output buffer and I/O pads is $652 \times 497 \mu\text{m}^2$. The proposed ILFD core dissipates power consumption of 4.8 mW from a 0.75 V supply voltage.

Figure 6.9: Chip micrograph of the ILFD.

Figure 6.10: Measurement setup.

Figure 6.10 shows the measurement setup of the ILFD, where the output frequency of the ILFD is measured by a PNA-X network analyzer N5247A, and the phase noise of ILFD output is measured by a Signal Source Analyzer (SSA) E5052B. Figure 6.11 shows the measured input sensitivity curves of the ILFD, where the simulated result is also plotted for comparison. Compared to the simulated results, the measured locking range of ILFD is reduced and shifted to a higher frequency. The reason for the

shrinking of locking range might be that the resistive loss of inductors or capacitors is larger than that in the simulation, resulting in a degradation of voltage amplitude of the injection loop, and hence reducing the locking range. However, the proposed ILFD still achieves a wide locking range of 14.9% from 60.2 GHz to 69.9 GHz with the input signal power at -3 dBm.

Figure 6.11: Input sensitivity curves of ILFD.

The output spectrums of ILFD when it is locked at the lowest and highest frequencies are shown in Figure 6.12. The measured input and output phase noise of ILFD are shown in Figure 6.13. The phase noise of input and output signals are -91 dBc/Hz and -102.7 dBc/Hz at 1MHz offset. The phase noise difference is close to 12 dB which agrees well with the theoretical value for a noise free divide-by-4 ILFD.

Table 6-1 summaries the performance of proposed ILFD and compares it with the other state-of-arts mm-wave frequency ILFDs with high division ratio [16-18, 21-23]. The FOM considering locking range, power consumption and injection power to evaluate a ILFD design can be cited from [22], [63],[108]. However, the locking range of ILFD is also strongly depended on division ratio, therefore a modified FOM defined in [109, 110] which has considered division ratio is more proper for a fair comparison. The FOM is given by

$$\text{FOM} = \frac{\text{LR}(\%) \times \text{Division Ratio}}{P_{\text{inj}}(\text{mW}) \times P_{\text{dc}}(\text{mW})} \quad (6.25)$$

where LR is the locking range, and P_{inj} is the input power in mW, and P_{dc} is the power

(a)

(b)

Figure 6.12: Measured output spectrum of ILFD.

Figure 6.13: Measured phase noise for (a) input signal and (b) output signal of the ILFD.

consumption. The proposed ILFD achieves a competitive locking range and FOM compared with other works. Although the locking range of proposed work is smaller than [16], the output of proposed ILFD does not suffer from large third harmonic component. The novel divide-by-4 ILFD topology proposed in this work not only enhance the third harmonic of ILFD which can facilitate fundamental mixing and improve the locking range, but also provide rejection of third harmonic at the output, so that avoid wrong operation of the following divider stages.

TABLE 6-1 PERFORMANCE COMPARISON OF MM-WAVE ILFDS

Ref.	Pub.	Tech.	Ratio	VDD	Pdc (mW)	Pin (dBm)	Input Freq. (GHz)	Locking range		FOM
								GHz	%	
[17]	2014 MWCL	90nm CMOS	3	1.1	10.8	3	73.1~84.3	11.2	14.2%	1.97
[21]	2012 MWCL	28nm CMOS	3	1.0	8.8	0	52.6~55.1	2.51	4.6%	1.57
[16]	2013 TCAS1	65nm CMOS	4	0.6	2.2	0	58.5~72.9	14.4	21.9%	39.8
[18]	2011 TMTT	0.18um CMOS	4	1.8	12.6	0	57.4~59.8	2.44	4.1%	1.30
[22]	2012 MWCL	90nm CMOS	4	1.2	15.5	-1	67~72.4	5.4	7.7%	2.50
[23]	2012 TMTT	90nm CMOS	5	0.6	3.75	0	59.4~63.5	4.1	6.6%	8.8
Our work		65nm CMOS	4	0.75	4.8	-3	60.2~69.9	9.7	14.9%	24.8

6.4 Summary

A novel V-band wide locking range divide-by-4 ILFD has been proposed. By employing both the injection loop and the output loop, the third harmonic component in the injection loop is boosted to facilitate the fundamental mixing and improve the locking range, while the third harmonic component in the output loop is suppressed, avoiding the wrong operation of the following stages. Moreover, the output-loop could assist the ILFD to achieve stable oscillation at fundamental frequency, so that allowing

further enhancement of third harmonic component in the injection-loop. Implemented in a 65 nm CMOS technology, the proposed ILFD has achieved a wide locking range of 14.9% from 60.2 GHz to 69.9 GHz, while consuming only 4.8 mW DC power.

Chapter 7

Conclusions and Future Works

7.1 Conclusions

This thesis presents the theory and the design of high performance VCOs and frequency dividers for 60 GHz applications.

In Chapter 2, the fundamentals of high frequency building blocks for mm-wave frequency synthesizer have been reviewed. Firstly, the topology of PLL based frequency synthesizers, and synthesizer architectures for 60 GHz transceivers with various frequency conversion schemes are studied. Secondly, the operation theory of oscillator has been presented, followed by the discussions of the key parameters of LC -VCOs, including the Q of LC -tank, phase noise, and tuning range. The typical LC -VCO topologies are also presented. Finally, the overview of the principles and the advantages and disadvantages of several different types of frequency dividers are investigated.

In Chapter 3, to improve the Q of LC -tank, the multiple-coupled LC -tank with tank order of N has been analyzed. The enhancement of Q has been demonstrated through theoretical deductions. A low phase noise VCO with five-coupled LC -tank has been

designed and implemented in a 65 nm CMOS technology. Benefiting from the Q enhancement of multiple-coupled LC -tank, the VCO achieves a low phase noise of -107 dBc/Hz at 1MHz offset, while consumes only 7.2 mW DC power.

In Chapter 4, a Ku-band VCO with dual LC -tanks and transformer-based feedback is proposed and designed in a 0.18 μm BiCMOS process. The dual LC -tanks configuration enhances the Q of the LC -tank, and the drain-to-source feedback increases the voltage swing of the VCO. The measured phase noise of the proposed VCO is -117.4 dBc/Hz at 1 MHz offset from the carrier frequency of 12.64 GHz. With a power consumption of 4.3 mW, the VCO has achieved an FOM of -193.1 dBc/Hz.

In Chapter 5, a wide tuning range dual-mode VCO involving switchable coupled VCO-cores has been presented. The VCO takes advantage of the parasitic capacitance of the cross-coupled pair to achieve a dual-mode operation at mm-wave frequency without using any switches loaded on the LC -tank. Comparing to conventional transformer-based dual-mode VCOs, the proposed topology allows the using of a large k transformer to simultaneously enhance the tank Q and increase the oscillation stability for both modes. Implemented in a 0.18 μm SiGe BiCMOS process, the proposed VCO has achieved a wide tuning range of 17.2% and the low phase noise from -97.5 dBc/Hz to -92 dBc/Hz at 1 MHz offset over the entire tuning range.

In Chapter 6, a novel V-band wide locking range divide-by-4 ILFD involving two coupled positive feedback loops (i.e., an injection-loop and an output-loop) has been proposed. By properly designing the LC -tank circuit, the third harmonic component of the ILFD in the injection-loop has been boosted to facilitate fundamental mixing and improve the locking range of the ILFD. Simultaneously, the third harmonic at the output has been suppressed to avoid the wrong operation of the following divider stages. The proposed ILFD is implemented in a 65 nm CMOS process. With a power

consumption of 3.84 mW, the proposed divide-by-4 ILFD has demonstrated a locking range of 14.9% from 60.2 GHz to 69.9 GHz.

7.2 Future Works

The phase noise of VCOs comes from both active and passive components. In the previous research, we have mainly focused on improving the Q of LC -tank to reduce the phase noise contribution of passive components. Therefore, one possible target for the future VCO design could be reducing the phase noise contribution from the active devices. The flicker noise of transistors plays an important role for mm-wave frequency VCOs. Although the flicker noise is usually considered as a low frequency noise source, it can be converted to high frequencies due to the non-linear effects of circuit and influence the close-in phase noise of mm-wave VCOs [51]. One solution to reduce the noise from active devices is the Class-C VCO of which the transistors are biased to not enter the deep triode region [111]. However, it is not suitable for mm-wave VCOs due to the large parasitic capacitance in the bias circuit. New circuit techniques are required to improve the linearity of cross-coupled pair and prevent the noise of tail current source from entering into the LC -tank.

For a dual-conversion transceiver, LO signals with quadrature phase are needed for I/Q mixing. Passive components such as poly-phase filters, can convert the differential outputs of a frequency divider into quadrature and differential signals, but it needs large power consumption and chip area. Therefore, if the quadrature signals can be generated by the first-stage frequency divider itself, then the total power consumption and area of the system can be reduced. Thus, another possible future work could be designing mm-wave frequency dividers with quadrature outputs. Quadrature outputs can be obtained based on ILFD by coupling two identical ILFDs [22]. Other

techniques such as transformer coupling can also be used to realize quadrature outputs [63]. However, those methods require extra circuits and power consumption. A static frequency divider which can be viewed as a two-stage ring oscillator is inherently able to provide highly matched quadrature outputs [112]. However, static frequency dividers usually suffer from large power consumptions.

The last future work is designing other lower frequency building blocks in the synthesizer and integrating the whole system. The design of lower frequency building blocks includes challenges such as the large power consumption in frequency divider chain, the precision of PFD and the matching of charge-pump. The integration of VCO and the first-stage frequency divider needs a careful co-design and skillful layout to ensure that the divider can be locked in the whole frequency tuning range of the VCO.

List of Publications

Journal Papers:

Q. Zou, K. Ma, and K. S. Yeo, "A Low Phase Noise and Wide Tuning Range Millimeter-Wave VCO Using Switchable Coupled VCO-Cores," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 2, pp. 554-563, Feb. 2015.

Q. Zou, K. Ma, K. S. Yeo, and W. M. Lim, "Design of a Ku-band Low-Phase-Noise VCO Using the Dual LC Tanks," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 59, no. 5, pp. 262-266, May 2012.

Conference Papers:

Q. Zou, K. Ma, and K. S. Yeo, "A wideband 60 GHz VCO with linear tuning range," in *URSI General Assembly and Scientific Symposium*, Aug. 2014, pp. 1-4.

Q. Zou, K. Ma, W. Ye, and K. S. Yeo, "A low power millimetre-wave VCO in 0.18 μm SiGe BiCMOS technology," in *IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS)*, Dec. 2012, pp. 244-247.

Q. Zou, K. S. Yeo, J. Yan, B. Kumar, and K. Ma, "A fully symmetrical 60GHz transceiver architecture for IEEE 802.15.3c application," in *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Nov. 2010, pp. 713-715.

K. Ma, **Q. Zou**, S. Mou, N. Mahalingam, and K. S. Yeo, "Transformer based multiple coupled LC tanks for on-chip VCO design and applications," in *Proc. IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Nov. 2012, pp. 192-194.

B. K. Thangarasu, J. Yan, K. Ma, **Q. Zou**, J. Ma, and K. S. Yeo, "A New 24/36-GHz Transceiver architecture for 60-GHz applications," in *IEEE International SoC Design Conference (ISOCC)*, Nov. 2009, pp. 9-12.

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