Printed electronics : analog and digital signal processing

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Printed Electronics:
Analog and Digital Signal Processing

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Summary

Printed electronics (PE) on flexible substrates (e.g. plastic-film) is an emerging technology that is likely to complement the ubiquitous silicon-based electronics. It is frequently touted as ‘Electronics Everywhere, Big Opportunities’, often envisioned as a ‘printing press’ capable of realizing ‘green’ electronic products whose attributes include On-Demand (print quickly, anywhere and anytime), Scalability (large format, e.g. wallpaper), and Flexibility (printed on flexible substrates such as plastic, etc.) such that they can be molded or bent to fit in odd and uneven spaces, yet so inexpensive that they can be everywhere print media is used (cost in terms of cents, and hence disposable).

The broad objectives of this multidisciplinary Ph.D. program are to investigate, design and realize PE analog and digital circuits and systems on flexible substrates, thereby augmenting ‘intelligence’ thereto. Specifically, this research focuses on the second and the third chains of the supply chain of the emerging PE technology: printing (processing/equipment platforms) and circuits, respectively. A number of contributions are made herein.

First, a novel simple Fully-Additive printing process – a screen printing process – involving only depositions, for realizing PE circuits and systems on flexible plastic films is proposed. This process is Green, On-Demand, Scalable and Low-Cost, congruous to aforesaid envisioned PE ‘printing press’ (vis-à-vis Subtractive printing, a complex process involving deposition and etching that otherwise requires expensive/sophisticated specialized IC (integrated circuit) fabrication facilities and is hence Un-Green, Not-On-Demand, Un-scalable and High-Cost). The proposed Fully-Additive process features printed transistors with high ($\sim 1.5 \text{ cm}^2/\text{Vs}$) semiconductor carrier-mobility, $\sim$ three times higher than competing state-of-the-art Fully-Additive processes and comparable to Subtractive processes. Furthermore, the proposed Fully-Additive process is capable of realizing a full array of passive elements, including capacitors, resistors, and inductors, and at least two layers of metal-interconnect. To

the best of the author's knowledge, the proposed process hitherto is the only Fully-Additive process capable of realizing complete and complex circuits and systems on flexible plastic films.

Second, a comprehensive open-platform for the proposed Fully-Additive screen printing process to facilitate the design and realization of PE analog and digital circuits is proposed. The proposed open-platform embodies a novel printed transistor model that is simple, accurate and compatible with industry-standard IC electronic design automation tools. To the best of the author's knowledge, the proposed model is the only model that accommodates and accurately models the effect of the channel length on carrier mobility, leakage current and parasitic capacitances, and is valid for all transistor operating regions, from cut-off to supra-threshold. The proposed open-platform further embodies, to the best of the author's knowledge, for the first time, process variations (statistical data) and matching based on various layout techniques of the printed transistors. These comprehensive models are imperative for the practical design and simulation of PE circuits, including manufacturability and implications with respect to the challenges of PE circuits.

Third, on the basis of the proposed open-platform, several analog and digital circuits are designed, Fully-Additive printed and measured. These circuits include conventional and proposed differential amplifiers, inverters and oscillators. The measured parameters of the printed circuits agree well with that obtained from simulations (using the open-platform derived herein), depicting the efficacy of the open-platform. The Fully-Additive printed proposed amplifier embodies a novel feedback with both positive and negative paths to simultaneously significantly improve the gain and reduce susceptibility to process variations, yet without compromising the printed area (compared to the conventional three-stage amplifier). It is also benchmarked against reported realizations (all Subtractive-based processes), and are shown to be highly competitive despite its realization based on our simple low-cost Fully-Additive process.

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List of Abbreviations

A-Si:H TFT	<u>H</u> ydrogenated <u>A</u> morphous <u>S</u> ilicon <u>T</u> hin <u>F</u> ilm <u>T</u> ransistors
BC	<u>B</u> ottom <u>C</u> ontact
BG	<u>B</u> ottom <u>G</u> ate
DAC	<u>D</u> igital to <u>A</u> nalog <u>C</u> onverter
DG	<u>D</u> ual <u>G</u> ate
IC	<u>I</u> ntegrated <u>C</u> ircuit
HOMO	<u>H</u> ighest <u>O</u> ccupied <u>M</u> olecular <u>O</u> rbital
IPA	<u>I</u> sopropyl <u>A</u> lcohol
ITO	<u>I</u> ndium <u>T</u> in <u>O</u> xide
LUMO	<u>L</u> owest <u>U</u> noccupied <u>M</u> olecular <u>O</u> rbital
MIM	<u>M</u> etal- <u>I</u> nsulator- <u>M</u> etal
OE-A	<u>O</u> rganic <u>E</u> lectronics <u>A</u> ssociation
OTFT	<u>O</u> rganic <u>T</u> hin <u>F</u> ilm <u>T</u> ransistors
PC	<u>P</u> olycarbonate
PE	<u>P</u> rinted <u>E</u> lectronics
PEDOT: PSS	<u>P</u> oly-3, 4- <u>e</u> thylened <u>i</u> oxy <u>t</u> hiophene: <u>s</u> tyrene <u>s</u> ulfonic acid
PEN	<u>P</u> oly <u>e</u> thylene <u>N</u> aphthalate
PET	<u>P</u> oly <u>e</u> thylene <u>T</u> erephthalate
PFBT	<u>P</u> entafluorobenzene <u>t</u> hiol
R2R	<u>R</u> oll-to- <u>R</u> oll
SAM	<u>S</u> elf- <u>A</u> ssembled <u>M</u> onolayer
SS	<u>S</u> ub-threshold <u>S</u> lope

TC	<u>T</u> op <u>C</u> ontact
TG	<u>T</u> op <u>G</u> ate
TFT	<u>T</u> hin <u>F</u> ilm <u>T</u> ransistors

Chapter 1   Introduction

1.1   Motivations

Printed Electronics (PE) is frequently touted as ‘Electronics Everywhere, Big Opportunities’, often envisioned as a ‘printing press’ for realizing ‘green’ electronic products whose attributes include On-Demand (print quickly, anywhere and anytime), Scalability (large format, e.g. wallpaper), and Flexibility (printable on flexible substrates such as plastic, etc.) such that they can be molded or bent to fit in odd and uneven spaces, yet so inexpensive that they can be everywhere print media is used (cost in terms of cents, and hence disposable). PE is also known as ‘Organic Electronics’, perhaps a slight misnomer because, although the early materials were organic, many recent materials are inorganic. PE is also sometimes known as ‘Large Area Thin Film Transistor’, and this is also perhaps a slight misnomer because other circuit elements such as capacitors, resistors, etc., are also printable. The PE technology is an emerging technology and holds much promise as a complementary electronics technology to the ubiquitous electronics based on silicon.

The size of the PE market is potentially gargantuan – the Organic Electronics Association (OE-A) [1] envisions the market to grow from US\$2.2 billion in 2011 to

US\$6.5 billion in 2017, and to US\$44.2 billion in 2021. Although at this juncture, the market for conventional silicon-based electronics is substantially larger, it is possible that the PE market may, at a future juncture, be a significant portion of the overall electronics market. Nevertheless, as the active semiconductor carrier mobility for PE thin film transistors (TFTs) remains very low ($>$ one thousand times slower) compared to conventional silicon-based semiconductors, the application of PE is rendered to very low-speed applications [2-6]. In this sense, PE complements silicon-based electronics. The sanguine market projection, to a large extent, assumes that ‘intelligence’ (analog and digital signal processing) can be augmented in PE circuits and systems – conversely, PE today is largely relegated to ‘dummy’ applications such as conductors on flexible plastic foils, photovoltaic and display applications [7-17].

The PE printing technologies can in general be classified as either ‘Subtractive’ or ‘Additive’ processes. Subtractive-based processes, including Laser Ablation [18] and Photolithography [19], are presently dominant, and largely resembles and leverages on present-day conventional silicon-based integrated circuit (IC) fabrication processing, involving a series of additive (deposition) and subtractive (etching, lift-off, etc.) steps. The primary shortcoming of this process is the complexity of the steps thereof and associated high costs – they involve highly specialized processing (and associated expensive/sophisticated equipment and infrastructure), including the use of corrosive chemicals for the subtractive steps. Consequently, it can be argued that the Subtractive-based PE is Un-Green (use of corrosive chemicals), Not-On-Demand (slow throughput and long (duration) processing), Un-Scalable (printing sizes are limited to wafer size due to the specialized equipment, e.g. 200 mm and 300 mm) and

Not-Cheap (expensive/complex equipment and infrastructure, high wastage of chemicals, in part due to etching/lift-off, etc.). In this sense, Subtractive-based PE somewhat contravenes the aforesaid frequently-touted attributes of PE.

At this juncture, several Fully-Additive processes have been reported [20-28], where the steps strictly involve depositions only (without etching or lift-off) – each printed layer is deposited on layer-upon-layer to realize transistors, passive components (resistors, capacitors and inductors) and interconnections thereto. It is instructive to note that the denotation ‘Fully-Additive’ used herein explicitly stipulates that all processing steps in the process are strictly depositions. There is somewhat a misnomer to the denotation ‘Additive’ because several reported processes, e.g. [18], were inadvertently deemed ‘Additive’ when some of the printing steps therein are Subtractive. Not unexpectedly, in these processes, some of the same aforesaid shortcomings of Subtractive-based processes apply. In short, Fully-Additive processes are advantageous over Subtractive-based processes because they are congruous with the aforesaid often-touted description of PE due to their simple deposition-only processing and associated low-cost unsophisticated equipment and infrastructure.

Nevertheless, reported hitherto Fully-Additive processes are uncompetitive when compared to their Subtractive-based counterparts due their low printed organic semiconductor carrier mobility, thereby further and severely limiting the ensuing applications to even lower speed. Furthermore, unlike Subtractive-based PE, Fully-Additive printing processes have yet to demonstrate the capability to print complex

circuits/systems that include at least two layers of metal-interconnect between transistors and passive components.

It has been established that the challenges for PE are highly formidable [16, 17, 29, 30], particularly if PE is to include complex functionality applications such as ‘intelligent’ circuits including analog, mixed-signal and digital signal processing. These formidable challenges, also termed ‘red bricks’ by players in the PE industry, include:

- (i) Cost effective Fully-Additive printing processes,
- (ii) Resolution, registration and process stability,
- (iii) Charge carrier mobility and electrical conductivity of the materials,
- (iv) Device characterization and modeling, and
- (v) Circuit design and realization including CMOS transistors.

These formidable challenges are directly related to the supply chain for PE, as depicted below in Figure 1-1. It is well recognized that to address these fundamental formidable challenges, highly inter- and multi-disciplinary expertise encompassing chemistry, physics, material, electronics and engineering sciences is required.

Figure 1-1 Supply Chain for Printed Electronics

In the first supply chain for PE, ‘Materials’ is largely in the realm of chemistry, materials and chemical engineering. Not unexpectedly, there is substantial research in this first chain both in academia and in industry [31-34]. With respect to the formidable challenges, the charge carrier mobility of the printed semiconductor materials is typically three to four orders of magnitude slower than that of silicon, hence the speed of the devices would at least be commensurably slower – and given the large minimum resolution compare to IC fabrication, the printed devices are even slower. Furthermore, the overall process variation (both inter- and intra- foil) is larger than that in IC fabrication.

A further formidable challenge is the environmental stability of the process. For example, many of the printed *n*-type organic semiconductors are not air stable, i.e. they degrade when exposed to air; and some printed organic semiconductors are sensitive to the light, humidity, temperature, etc., the process parameters of the printed transistors (such as charge carrier mobility and threshold voltage) varies a lot when these conditions change.

The second chain pertains to the printing/patterning methods and the associated equipment. Figure 1-2 depicts the various state-of-the-art printing/patterning methods for PE. These printing/patterning methods can in

general be classified as Subtractive and Additive processes, as delineated earlier. The former includes the processes within the smaller circle in Figure 1-2, the laser ablation [18] and R2R (roll-to-roll) photolithography [19]. These processes are akin to the standard prevalent silicon-based IC fabrication process which involves a sequence of deposition and removal steps, and typically involves expensive equipment and toxic ‘non-green’ chemicals. Not unexpectedly, the resolutions from these processes are small, less than $10\text{ }\mu\text{m}$, and compared to the other processes, the devices printed are faster (but still considerably slower than silicon-based IC due to the low carrier mobilities of the printed semiconductors). The other disadvantages of these Subtractive-based processes include the lack of scalability, i.e. the inability to print large areas, the inability to use viscous inks (inks used need to be viscous), and very slow throughput, hence overall limiting and expensive.

Figure 1-2 PE printing methods

The latter printing processes (Additive processes), have generally received higher acceptance (than the Subtractive processes) due to their similarity to graphics arts, including their processing from relatively low-cost equipment, use of viscous inks, high throughput and the high scalability [35-37]. The shortcoming, however, is the larger minimum resolution (from 10 μm to larger than 100 μm), hence the lower circuit density and reduced speed. This lower circuit density shortcoming is typically not serious at this juncture, largely because the low cost is a mitigating factor.

Of the various Additive printing processes, there are several that are competitive, and details will be described in Chapter 2. Arguably, the screen printing process offers the most advantages, in part due to its strong correlation with the mature silk screen printing technology for printing tee-shirts (the masks are largely the same). Further, the possibility of developing patterning technologies to realize two layers of interconnects to facilitate the fabrication of complex electronic circuits that have thus far been largely been elusive.

In terms of formidable challenges, the second chain is related to printing/patterning methods (Subtractive vis-à-vis Additive), to resolution and to registration. Registration refers to the alignment of the different layers of printing. Arguably, registration is less of an issue with Subtractive process than with Additive process because part of the former's process is self-aligning.

The third chain in Figure 1-1 is highly correlated to the designs and applications – the circuits/power source/memory/sensors. One formidable challenge is the open-platform for the design and simulation of PE circuits and systems remains

unreported. Akin to standard silicon-based Integrated Circuit (IC) practices, accurate modeling of the printed transistors and passive components are needed to facilitate their design and simulation of PE circuits and systems. Furthermore, another formidable challenge is the design of robust circuits that can tolerate the high process variations. At this juncture, due to the limitations delineated above, the reported circuits are largely with very limited ‘intelligence’ (signal processing), including photovoltaic and display applications. It is worthwhile noting that the recently reported ‘intelligent’ applications and realizations [18, 19, 38-40] are based on Subtractive processes – they are not unlike the ubiquitous silicon-based IC processes. However, as delineated earlier, they contravene the frequently-touted attributes of PE.

The fourth and fifth chains, the system integration and test/verification pertain more closely to the industry and lesser to academia. These aspects are important to ensure that devices printed do have a reasonable lifetime and are manufacture-able, with sufficient rigor in testing and verification. For a reasonable lifetime, the printed devices would need to be adequately packaged.

In view of the aforesaid formidable challenges of PE, it is not unexpected that at this juncture, the complexity of reported PE applications are largely of very limited ‘intelligence’ or signal processing (save that reported for Subtractive processes that are contravene the frequently-touted attributes of PE). In short, in view of the nascence of PE, there are many unresolved issues, and of particular interest, pertaining to PE by means of Fully-Additive processing. Some of the most fundamental issues include the development of a Fully-Additive process capable of

realizing circuits and systems of note, and the design of ‘intelligent’ circuits and systems that can accommodate the limitations and shortcomings of said Fully-Additive process. To facilitate, said design, there is also the need for an adequate model of the transistors and other elements, i.e. an open-platform for PE circuit and system design (and simulations). These three fundamental issues are the primary motivations of this Ph.D. program.

1.2 Objectives

In view of the above mentioned motivations, the objectives of the Ph.D. research program pertain to the development of a Fully-Additive process, its associated device model and to the realization of PE analog and digital circuits on flexible plastic substrates – second (printing process) and third (circuit design) chains of the PE supply chain.

The specific objectives pertaining to the printing process (second chain) are to:

- (i) Investigate and develop a Fully-Additive printing method/procedure that features all frequently-touted attributes of PE – ‘green’, on-demand, flexible and inexpensive;
- (ii) Following (i), critically select/screen out commercially-available chemical materials for said Fully-Additive printing process for the printing of organic

thin film transistors (OTFTs) and passive components (capacitors, resistors and inductors);

- (iii) Optimize the characteristics of the printed devices to improve their performance, particularly, semiconductors to feature relatively high carrier mobility, relatively good environmental stability, electrical stability and low process variations; and
- (iv) Develop the process for at least two layers of interconnects.

The specific objectives pertaining to the circuit design (third chain) are to:

- (i) Develop a comprehensive printed transistor model, particularly to include for the first time, the effect of the channel length on carrier mobility, leakage current and parasitic capacitances and to be valid for all transistor operating regions, from cut-off to supra-threshold;
- (ii) Following (i), develop an open-platform based on the developed Fully-Additive printing process to facilitate the design and realization of PE analog and digital circuits;
- (iii) Investigate and characterize the process variations of the developed Fully-Additive printed devices and integration into the developed open-platform; and

- (iv) Further to (iii), investigate the variations of OTFTs matching based on different layout of printed transistors, and to ascertain the layout with the lowest variations.

The specific objectives pertaining to the realization of analog and digital circuits (third chain) are to:

- (i) Investigate, design, print and verify several core basic building analog circuits (operational amplifiers) whose architectures innately accommodate the shortcomings of PE printing (including low mobility, registration, etc.); and
- (ii) Similar to (i), for basic digital circuits.

1.3 Contributions

Congruous to the objectives delineated above, a number of contributions are made in this Ph.D. research program. These contributions are largely reported in two published journal article* [6, 41], and four technical disclosures [42-45] . To the best of the author's knowledge, all contributions herein are novel and unreported in literature.

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* This publication was the second-most downloaded article in the ScienceDirect database (a database of > 2,500 journals) in the field of printed electronics for the last 90 days in June 2014. The number of downloads is ~ 1,800 downloads.

The contributions pertaining to the printing process (second chain) include:

- (i) Development of a novel simple Fully-Additive printing process – a screen printing process – involving only depositions for realizing PE circuits and systems on flexible plastic films. This process is demonstrated for ‘large’ format, up to A3 (297 mm × 420 mm) sized films and requiring only low temperature ($< 150\text{ }^{\circ}\text{C}$), thereby printable on a pleathore of flexible substrates, including low-cost high-temperature-intolerant plastic films. On the basis of the demonstrations herein, the developed printing process can easily be scaled to much larger formats, including roll-to-roll processing;
- (ii) The printed devices include both active devices (*p*-type OTFTs) and a full array of passive elements including resistors, capacitors and inductors. Hence, the complete family of printed components necessary for realizing analog, digital and mixed-signal circuits;
- (iii) Further to (ii), this process is capable of printing at least two layers of metal-interconnects, thereby facilitating the realization of full circuits whose complexity are of note (i.e. complex circuits and systems may be realized);
- (iv) Proposal of a novel semiconductor deposition method – slot die coating, where the printed OTFT features high carrier mobility ($\sim 1.5\text{ cm}^2/\text{Vs}$) with TIPS-Pentacene as the active *p*-type semiconductor. This mobility is the highest of all reported Fully-Additive processes to date – three times higher than competing state-of-the-art Fully-Additive processes (such as spin coating,

drop casting and inkjet printing) and comparable to the substantially more complex and expensive Subtractive processes; and

- (v) Development of a device modification procedure, specifically the electrode-semiconductor interface modification. The ensuing silver source/drain electrodes with PFBT (pentafluorobenzenethiol) modified surface featured ~ one hundred times improvement on the resulting semiconductor carrier mobility. The carrier mobility, $\sim 1.5 \text{ cm}^2/\text{Vs}$, is in part due to the embodiment of this procedure in the overall processing.

The contributions pertaining to circuit design (third chain) based on the contributions pertaining to the printing process (second chain) in (i) – (v) above include:

- (i) Development of a novel printed OTFT model that is simple, accurate and compatible with industry-standard IC electronic design automation tools. To the best of the author's knowledge, the proposed model is the only model that accommodates and accurately models the effect of the channel length on carrier mobility, leakage current and parasitic capacitances, and is valid for all transistor operating regions, from cut-off to supra-threshold regions;
- (ii) Proposal of a comprehensive open-platform for the proposed Fully-Additive screen printing process to facilitate the design and realization of PE analog and digital circuits. The proposed open-platform further embodies the process variations (statistical data) and matching based on various layout techniques

of printed transistors. These comprehensive models are imperative for the practical design and simulation of PE circuits, including manufacturability and implications with respect to the challenges of PE circuits;

- (iii) The process variations of the developed Fully-Additive printed OTFTs are investigated in terms of charge carrier mobility and threshold voltage. The measurements depict that the standard deviation of charge carrier mobility is 30.7% from its mean value and the standard deviation of threshold voltage is 45.41% from its mean value; and
- (iv) Further to (iii), an investigation into the effect of layout on matching accuracy of printed OTFTs is investigated. By means of appropriate layout, it is shown that the printed transistors can be accurately (in the context of PE) matched – a relatively low standard deviation of charge carrier mobility of ~8% can be achieved by the 2D common centroid layouts. To the author's knowledge, this is the best matching reported in literature for Fully-Additive processes.

The contributions pertaining to the realization of analog and digital circuits (third chain) based on the contributions above include:

- (i) On the basis of the proposed open-platform, several analog circuits are designed, Fully-Additive printed and measured. These circuits include both conventional single-stage and proposed single-stage differential amplifiers. By means of simulations (including Monte Carlo simulations of these circuits

(based on the open-platform herein)) and measurements on printed circuits, the performance of these circuits are benchmarked and their design implications are delineated. The benchmarking shows good agreement between simulations and measurements, depicting the efficacy of the aforesaid proposed open-platform.

The proposed novel amplifier embodies a novel feedback with both positive and negative paths to simultaneously improve the open loop gain (~ 27 dB, ten times higher than that in the conventional single-stage amplifier) and reduce susceptibility to process variations, yet without compromising the printed area (compared to the conventional three-stage amplifier); and

- (ii) Similar to (i), several digital circuits are designed, Fully-Additive printed and measured. These circuits include inverters and ring oscillators based on the conventional design and a simple improved design embodying a level shifter. By means of simulations (including Monte Carlo simulations of these circuits (based on the open-platform herein)) and measurements on printed circuits, the performance of these circuits are benchmarked and their design implications are delineated.

From an overall perspective, the contributions made in this research program are significant – they provide useful insight to PE researchers on both second and third supply chains of PE (printing processes and circuit designs to realize ‘intelligent’

PE circuits and systems on flexible substrates based on inexpensive, ‘green’, on-demand and scalable Fully-Additive methods).

1.4 Organization of the Thesis

The subsequent chapters of this thesis are organized in the following manner.

In Chapter 2, a comprehensive literature review on PE technology is provided. The PE OTFT principles are first reviewed, including device structure, device operating principles and materials. Thereafter, the PE printing/patterning technologies, including both Subtractive (photolithography, laser ablation, etc.) and Additive (inkjet, screen printing, gravure printing, etc.) methods are reviewed and compared. The major challenges of PE are also presented and discussed.

In Chapter 3, a Fully-Additive printing process is proposed that circumvents the aforesaid shortcomings of state-of-the-art Fully-Additive processes, rendering the proposed Fully-Additive printed circuits/systems competitive to the (substantially more complex) Subtractive processes in terms of carrier-mobility and the ability to print complex circuits/systems including transistors, passive components (capacitors, resistors and inductors) and two metal-interconnect layers on flexible substrates. On the basis of the proposed Fully-Additive screen printing process, three fundamental analog (a proposed and two conventional differential amplifiers) circuits are demonstrated.

In Chapter 4, an open-platform for PE is proposed for the proposed Fully-Additive screen printing process, including a novel model for printed transistors, and their process variations (based on the measurement data). The proposed model is verified to be accurate (and useful) by benchmarking it against measurements on individual transistors and on the basis of a number of analog and digital circuits. The effect of layout on matching accuracy of printed transistors is investigated to facilitate practical design of PE circuits and systems. On the basis of the proposed comprehensive platform, several fundamental analog and digital circuits are designed, printed and measured. By means of simulations (including Monte Carlo simulations of these circuits (based on the open-platform herein)) and measurements on printed circuits, the performance of these circuits are benchmarked and their design implications are delineated.

In Chapter 5, conclusions of the research program are drawn and recommendations for further work are presented.

Chapter 2   A Review of PE Technology

This chapter provides a comprehensive literature review of PE technology and serves as preamble to the contributions delineated in Chapters 3 and 4.

In Section 2.1, OTFTs principles are first reviewed, including the various device geometries, operating principle, and OTFT characteristic parameters.

In Section 2.2, the various materials employed for each layer of the OTFT are reviewed, including the substrates, electrodes, dielectrics and semiconductors. Of specific interest, the semiconductors can be classified into three categories: *p*-type, *n*-type and ambipolar. At this juncture, the *p*-type organic semiconductors feature the highest performance in terms of charge carrier mobility, process-ability and air stability. More specifically, small molecule *p*-type organic semiconductors feature higher charge carrier mobility than polymer *p*-type organic semiconductors. On the basis of these advantages, small molecule *p*-type organic semiconductor (TIPS-Pentacene) is of interest (and selected) in this research program.

In Section 2.3, various printing/patterning technologies, including both Additive and Subtractive processes are reviewed. As delineated in Chapter 1, Additive processing is preferred over the latter for its ‘green-ness’, ease of printing, associated low cost and scalability. Of the various Additive processes that are reviewed herein, the screen printing arguably has the most advantages, largely for its

leveraging on the well-established silk screen printing for garments and graphics art, thereby its cost advantage, scalability, applicability, etc. This is the printing process adopted and of specific interest in this research program.

In Section 2.4, on the basis of this review, the formidable challenges of PE are delineated and discussed. A conclusion is drawn in Section 2.5.

2.1 A Review of Organic Thin Film Transistors (OTFTs)

This review introduces the OTFTs and in part serves as a preamble to the improved OTFT model (proposed in this Ph.D. program delineated in Chapter 4).

2.1.1 Device Geometry

OTFTs are developed based on the technology of TFTs (deposition of different functional thin film layers) [34] and are fabricated/printed similarly with various types of device structures. These structures can be classified by the orientation of the source-drain channel (either planner or vertical), by the number of gate layers (such as single gate structure and dual gate structure), and by the deposition sequence of different layers (gate layer, source/drain layer and semiconductor layer). Each type of OTFT structure has its unique advantages and disadvantages, and these will now be delineated.

Single Gate Structures (Planner Channel Structures)

The Single Gate OTFT [34] is a conventional TFT structure where only one gate layer is presented to control the electrostatic characteristics over the channel of the transistor. This structure can be further classified on the basis of the relative position of the gate layer with respect to the semiconductor layer – the top gate (TG) structure (on the top of the semiconductor layer), and the bottom gate (BG) structure (on the bottom of the semiconductor layer). These are depicted in Figures 2-1 and 2-2 respectively.

Figure 2-1 Top gate OTFTs: (a) Top gate Bottom contact; and
(b) Top gate Top contact

Figure 2-2 Bottom gate OTFTs: (a) Bottom gate Bottom contact; and
(b) Bottom gate Top contact

Although the TG OTFT structure is similar to the conventional MOSFET structure, most OTFTs are fabricated using the BG structure due to the process-ability of the active organic semiconductors. In some fabrication processes, relatively high temperature and wet treatments are required for the deposition of the electrode and dielectric layers. These may cause defects and impairments in the organic semiconductor layer and the resulting degraded semiconductor layer will lead to low performance OTFTs. In this respect, for ease of processing, BG structures are preferred over the TG structures.

Besides the TG and BG structures which are based on the relative position of the gate layer with respect to the semiconductor layer, the structures may also be classified based on the relative position of the source/drain layer with respect to the semiconductor layer. On this basis, the structures may be classified as either the top contact (TC) structure (on the top of the semiconductor layer), or the bottom contact (BC) structure (on the bottom of the semiconductor layer). Figures 2-1 (a) and (b) depicts the OTFT structures in the top gate configuration, top gate bottom contact (TGBC) and top gate top contact (TGTC) structures. Figures 2-2 (a) and (b), on the other hand, respectively depict the bottom gate configuration, bottom gate bottom contact (BGBC) and bottom gate top contact (BGTC) structures.

Interestingly, despite all the four single gate structures delineated above reportedly having been fabricated and measured with relatively the same materials, fabrication techniques, dimensions and biasing condition, their electrical characteristics (such as charge carrier mobility, threshold voltage, etc.) are different.

There are several reasons [46] for the difference and the most significant is probably due to the mobile charge carriers traveling in different path between source and drain electrodes for the different structures.

In reported literature, the OTFTs with the BC structure in general feature the best performance in terms of subthreshold slope, and the OTFTs with TC structure feature the best performance in terms of charge carrier mobility and on/off current ratio.

The most imperative factors [46-48] that affect the OTFT behavior are probably due to the morphology of the organic semiconductor layer and the existence of the electrode-organic semiconductor contact resistance. The morphological orientation [47] of the organic semiconductor layer depends on the surface roughness before deposition. It was reported [48] that the Schottky energy barrier influences the contact resistance in the BC structure but has negligible influence in the TC structure. More specifically, a 0.4 eV increase in the Schottky energy barrier height will lead to 1 k Ω increase in the electrode-organic semiconductor contact resistance.

In the BC structure, as the source/drain electrodes are deposited before the deposition of the semiconductor, the resulting surface will have two types of materials. This leads to a poorly formed organic semiconductor layer and a high electrode-organic semiconductor contact resistance, results in an elevated contact barrier for the charge carrier to transport from source to drain, leading to a lower current. A reported [49] benchmarking of the TC and BC OTFTs with same fabrication techniques and biasing conditions showed that the TC OTFT structure has

~133 times higher in saturation current and corresponding at least two orders of magnitude higher in charge carrier mobility. Nevertheless, despite of lower performance of the BC structure, it is preferred (virtually universally adopted) for PE applications, because of the simplicity of its fabrication for both Additive and Subtractive process. For this reason, the BC structure, more specifically the Bottom Gate Bottom Contact structure (Figure 2-2 (a)), is adopted in this Ph.D. program.

Dual Gate Structures (Planner Channel Structure)

To achieve better control of the charge carrier transportation, an additional gate layer was reported introduced [50], resulting a dual gate (DG) OTFT structure, as depicted in Figure 2-3. It was shown that with an additional gate layer, better OTFT performance in terms of saturation current, sub-threshold slope and threshold voltage can be achieved. One of the primary advantages of DG OTFT structure is that the threshold voltage can be adjusted by means of biasing the additional gate. The DG OTFT also features significant enhancement in terms of the on/off current ratio, especially the reduced off state current, rendering them more reliable in terms of digital circuit operation. At this juncture, some PE circuits such as oscillators and amplifiers have been demonstrated [51] using DG structure.

Figure 2-3 Dual gate OTFTs: (a) Dual gate Bottom contact; and
(b) Dual gate Top contact

As shown in Figure 2-3, the typical DG OTFT structure embodies six layers, including a bottom gate layer with its bottom dielectric layer, a top gate layer with its top dielectric layer, source and drain electrodes and an organic semiconductor layer. The structures of DG transistors for both BC and TC are shown in Figures 2-3(a) and (b), respectively.

In the DG OTFT, the bottom gate serves as the main gate and it applies the electrical field to accumulate the charge carriers in the channel. The top gate serves as the biasing gate, further applying an additional electrical field, thereby changing the conductivity of the channel. In this fashion, the threshold voltage (V_{TH}) of OTFT can be controlled by biasing the top gate, and the device operation can be controlled by the external control of the bottom gate.

The DG OTFTs can be set into three different operating modes based on different biasing conditions. If the voltage applied to the bottom gate and the top gate kept at ground, the OTFT will operate as a BG structure. If the voltage applied to the top gate and the bottom gate kept at ground, the OTFT will operate as a TG structure.

If the voltage applied to both bottom and top gates, the OTFT will operate as a DG structure. In the single gate operating mode, the second gate has no effect, whereas in dual gate mode, both the gates play a vital role in accumulating the charge at the organic semiconductor-dielectric interface.

In the DG operating mode, the total charge, Q_{Total} (C) accumulated by the two gates is:

$$Q_{Total} = C_B \times V_B + C_T \times V_T \quad (2.1)$$

where C_B (F) is the capacitance at the bottom gate,

C_T (F) is the capacitance at the top gate,

V_B (V) is the voltage at the bottom gate, and

V_T (V) is the voltage at the top gate.

By biasing the external top gate, and the threshold voltage, V_{TH} (V), can be adjust accordingly:

$$\Delta V_{TH} = \frac{C_T}{C_B} \times \Delta V_T \quad (2.2)$$

By this means the adjustment of V_{TH} can be large. For example, it was reported [52] that by sweeping the external top gate bias from -10 V to 10 V, the V_{TH} of OTFT is changed from 1.95 V to -9.8 V. The mobility and on/off current ratio are also increased in DG as compared to the BG. For example, $\sim$ five times increase in the charge carrier mobility in the DG OTFT compared to the single gate structure was reported [50].

In the context of this Ph.D. research program, the DG structure is not adopted due to the added difficult fabrication steps involved; this is recommended future work (see Chapter 5).

Vertical Channel Structure

The performance of a conventional planar structure OTFT is limited by the morphology of the organic semiconductor, and the relatively long channel length. In the TC OTFT, reducing the channel length to the submicron range using low cost Additive methods is very challenging; short channel length is desired to minimize the operating voltage of the OTFT without compromising the output driving capability. One reported [53] means to reduce the channel length is the vertical structure for the OTFT. The vertical channel OTFT consists of four different layers and its structure is shown in Figure 2-4.

Figure 2-4 Vertical channel OTFT

It was reported [54] that the charge carrier mobility of the vertical channel OTFT is ~ 3.3 times higher and the on/off current ratio is ~ 11 times higher compared to the planar channel OTFT. These improvements in the OTFT performance are due to the reduction of the channel length.

Despite the advantage of the vertical structure for the OTFT, it is not adopted in this Ph.D. program due to the complexity of the fabrication process involved.

2.1.2 Operating Principle

For simplicity, consider the BGBC structure OTFT as depicted in Figure 2-5 to illustrate a typical OTFT device characteristic. For a given source-drain voltage, V_{DS} , the amount of current that flows through the organic semiconductor layer from source to drain electrode is a function of the gate-source voltage, V_{GS} .

Figure 2-5 Bottom Gate Bottom Contact OTFT

The principle of the gate voltage induced charge carrier and the operation of OTFT are well-established [55], and can be explained by the simplified electronic energy level diagrams depicted in Figure 2-6. The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) of the organic semiconductor and the work functions of the source-drain electrodes, are depicted in Figure 2-6 (a).

Figure 2-6 Illustration of the working principle of OTFT: (a) Energy level diagram at $V_G = 0$ and $V_{DS} = 0$; (b) Operation for hole accumulation; (c) Operation for electron accumulation; (d) Operation for hole transport; and (e) Operation for electron transport

With gate bias $V_{GS} = 0$, as depicted in Figure 2-6 (a), there will be no charge carriers induced in the semiconductor. The current flow in the organic semiconductor arises from a flow of mobile charge carriers from the source to drain electrode. As there is largely no charge carrier, the current will be relatively small owing to the low conductivity of the organic semiconductors. This is the ‘off’ state.

With an applied negative gate voltage with $V_{DS} = 0$ and $V_{DS} < 0$, as depicted in Figures 2-6 (b) and (d), respectively, a large electric field (a *p*-type conducting channel) is induced. This induced electrical field leads to a shift up of the HOMO and LUMO levels of the organic semiconductor. When the gate voltage is sufficiently large, the included field will cause the HOMO level of the organic semiconductor to be compatible with the work functions of the electrodes. Electrons will then be injected into the electrodes from the organic semiconductor, and holes will remain in the semiconductor. The positive charge holes become the mobile charge carriers that flow from source to drain, as depicted in Figure 2-6 (d). These types of organic semiconductors that able to induce positive charge carriers are termed as *p*-type semiconductors.

Conversely, with an applied positive gate voltage with $V_{DS} = 0$ and $V_{DS} > 0$, as depicted in Figures 2-6 (c) and (e), respectively, a large electric field (an *n*-type conducting channel) is induced. This induced electrical field leads to a shift down of the HOMO and LUMO levels of the organic semiconductor. When the gate voltage is sufficiently large, the included field will cause the LUMO level of the organic semiconductor to be compatible with the work functions of the electrodes. In this case,

electrons become mobile charge carriers. These types of organic semiconductors that able to induce negative charge carriers are termed as *n*-type semiconductors.

The description above is simple and ideal, and certain quantitative effects are lacking and needed to be account for, such as traps and dopants. Details are well reported in literature [56].

In summary, organic semiconductors can be classified according to *p*-channel (hole) semiconductors or *n*-channel (electron) semiconductors. Moreover, some organic semiconductors have the ability to induce both negative and positive charge carriers are termed as ambipolar semiconductors.

2.1.3 OTFT Characterization

There are two common methods to characterize the performance of OTFTs. The first, commonly referred as transfer curve, involves keeping V_{DS} constant and sweeping V_{GS} . The second, commonly referred as output curve, involves keeping V_{GS} constant and sweeping V_{DS} .

The characteristics of the *p*-type OTFT printed in this Ph.D. program by both methods are shown in Figure 2-7; see details in Section 3.1 later.

Figure 2-7 Transfer and output characteristics of the OTFT

Consider now a review of the basic model of an OTFT; the improved model derived in this Ph.D. program is delineated in Chapter 4 as part of the development of an open-platform for the process developed. For simplicity, the *n*-type OTFT is reviewed and its extension to a *p*-type is straight-forward; the review in this section somewhat resembles the well-known *n*-MOSFET.

For the *n*-type semiconductor operation with $V_{DS} = 0$, assuming that the electrode-organic semiconductor contact resistance is negligible and $V_{TH} = 0$, the applied positive V_{GS} will induce holes at the gate-dielectric interface, and electrons at the organic semiconductor-dielectric interface. If $V_{DS} = 0$, the density of charge carriers will be equally distributed in the channel. On the other hand, if $V_{DS} \neq 0$, as depicted in Figure 2-8 (b), the charge density, q_{ind} (C/m^2), is a function of the relative position in the channel and it can be expressed [57] as:

$$\begin{aligned}q_{ind}(x) &= n(x) \cdot e \cdot t \\ &= C_{ox}(V_{GS} - V(x))\end{aligned}\tag{2.3}$$

where C_{ox} (F) is the of the dielectric capacitance,

$n(x)$ (m^{-3}) is the charge carrier concentration,

e (C) is the unit charge, and

t (m) is the thickness of the semiconductor.

Figure 2-8 (a) Charge density of an OTFT in the linear regime; (b) Pinch-off ; and (c) Charge density of an OTFT in the saturation regime

For an n -type organic semiconductor, the energy gap between the work functions of the electrodes and the LUMO level of the organic semiconductor results an injection barrier between the electrodes and the organic semiconductor, leading to a shift of the flat band condition of the organic semiconductor. Due to this effect, an

additional V_{GS} offset is needed to biasing the organic semiconductor at flat band condition.

For an n -type organic semiconductor, doping the channel reduces V_{TH} , while traps (a semiconductor defect) increase the V_{TH} , and the energy gap between the LUMO level of the organic semiconductor and work function of the electrode may shift V_{TH} in either direction.

Taking V_{TH} into account, eqn. (2.3) becomes [57] :

$$\begin{aligned} q_{ind}(x) &= n(x) \cdot e \cdot t \\ &= C_{ox}(V_{GS} - V_{TH} - V(x)) \end{aligned} \quad (2.4)$$

As depicted in Figure 2-8 (a), when V_{DS} is sufficiently small, the charge density in the channel is equally distributed for a given V_{GS} (as V_{TH} is an intrinsic constant, if $V_{DS} = 0$, $V(x) = 0$). However, when a small V_{DS} is applied and $V_{DS} < V_{GS} - V_{TH}$, the charge density will be a first order function of V_{DS} . For a given V_G voltage, the average value of q_{ind} is $C_{ox}(V_{GS} - V_{TH} - V_{DS}/2)$. When the applied drain-source voltage reaches to the point that $V_{DS} = V_{GS} - V_{TH}$, as depicted in Figure 2-8 (b), the charge density will be zero at the edge of source contact.

By applying Ohm's law and by definition of conductivity, the output drain current for an OTFT, I_{DS} (A), can be expressed [57] as:

$$\frac{I_{DS}}{tW} = \sigma \frac{V_{DS}}{L} \quad (2.5)$$

$$I_{DS} = \frac{W}{L} (n_{ind,av} \cdot e \cdot t) \mu V_{DS} \quad (2.6)$$

where σ (S/m) is the conductivity of the organic semiconductor,

μ (cm²/Vs) is the carrier mobility, and

$n_{ind,av}$ (m⁻³) is the average charge carrier concentration.

By substituting the eqn. (2.4) into eqn. (2.6), the output drain current for an OTFT, I_{DS} (A), can be expressed as a function of V_{GS} and V_{DS} [57]:

$$I_{DS} = \frac{W}{L} \mu C_{OX} [(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}] V_{DS} \quad (2.7)$$

and eqn. (2.7) can be expressed [57] as:

$$I_{DS} = \frac{W}{L} \mu C_{OX} [(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2}] \quad (2.8)$$

Eqn. (2.8) is the standard OTFT output drain current equation in the linear regime. When V_{DS} is sufficiently small such that $(V_{GS} - V_{TH}) \gg V_{DS}$, $V_{DS}^2/2$ is negligible and the OTFT behaves like a resistor.

The channel has largely a uniform distributed charge density across the channel when V_{DS} is small ($(V_{GS} - V_{TH}) \gg V_{DS}$), as depicted in Figure 2-8 (a)). As V_{DS}

is increased, the charge density becomes increasingly non-uniform, and scales linearly with V_{DS} .

When $V_{DS} = V_G - V_{TH}$ (as depicted in Figure 2-8 (b)), the channel becomes “pinch-off”, and there is no mobile charge carriers at the edge of the source electrode. Thereafter, the increasing of V_{DS} beyond this point will only shift the pinch-off point to the drain electrode side (as depicted in Figure 2-8 (c)). In this case, there will be no additional drain current when $V_{DS} > V_G - V_{TH}$.

Substituting $V_{DS} = V_{GS} - V_{TH}$ into eqn. (2.8) will be the I - V characteristics of the OTFT in saturation, and is expressed [57] as:

$$I_{DS,sat} = \frac{1}{2} \frac{W}{L} \mu_{sat} C_{OX} (V_{GS} - V_{TH})^2 \quad (2.9)$$

Hence, the charge carrier mobility of the OTFT in the saturation region can be calculated from the gradient of the $(I_{DS,sat})^{1/2}$ vs V_{GS} line plot and the threshold voltage of the OTFT can be obtained from the intercept.

2.1.4 Characteristic Parameters of OTFT

There are several important parameters that determine the performance of an OTFT, including charge carrier mobility (μ), threshold voltage (V_{TH}), on/off current

ratio (I_{ON} / I_{OFF}), and sub-threshold slope (SS). These parameters are determined and influenced by several factors, including device geometry, materials of different layers, morphology of the organic semiconductor, dimensions, etc. In general, a high performance OTFT should feature high charge carrier mobility, low threshold voltage, large on/off current ratio and a sharp sub-threshold slope.

Charge Carrier Mobility

The charge carrier mobility of an OTFT is the average drift velocity of the charge carrier per unit electric field. This parameter is particularly important as it ascertains the operating speed of the OTFT. In general, high charge carrier mobility is required to obtain a large saturation current. At this juncture, the mobility of n -type organic semiconductors is reported [31] to be substantially lower than the p -type due to their process-ability and environmental stability.

At this juncture, the mobility of p -type organic semiconductors such as pentacene, is relatively high but low compared to that of silicon, $\sim 3.2 \text{ cm}^2/\text{Vs}$ [58]. Not unexpectedly, there is concerted effort within the PE community to realize high mobility and stability of n -type organic semiconductor materials. From electronic design perspective, the n -type is highly desirable to allow the realization of complementary (p - and n - type) circuits.

The charge carrier mobility is strongly dependent on the morphology of the organic semiconductor, such as grain size and orientation [59]. In some OTFTs, it

was reported [60] that the mobility increases with the gate voltage and this phenomenon is called field dependent mobility. This field dependent mobility, μ (cm^2/Vs), is expressed as:

$$\mu = \mu_0 (V_{GS} - V_{TH})^\alpha \quad (2.10)$$

where α is the power law parameter, and

μ_0 (cm^2/Vs) is the band mobility of the organic semiconductor.

This power law parameter, α , is dependent on the structure of the device, organic semiconductor, and the dielectric. It was reported [61] that the charge carrier mobility of an OTFT increased from $0.02 \text{ cm}^2/\text{Vs}$ to $1.26 \text{ cm}^2/\text{Vs}$ with the increase of V_{GS} from -14 V to -146 V , using pentacene as semiconductor.

Threshold Voltage

The threshold voltage, V_{TH} , determines the switching behavior of an OTFT, and is used to control and biasing the OTFT to operate in proper regime to facilitate the function of circuits [62-64]. V_{TH} is strongly dependent on the channel length, organic semiconductor, dielectric and the thicknesses of both the organic semiconductor (t_{OSC}) and the dielectric (t_{OX}) layers. It was reported [64] that the threshold voltage can be reduced by a smaller channel length, a thicker organic

semiconductor layer thickness and a thinner dielectric layer thickness. From practical circuit design perspective, low threshold voltage is desired as it allows low operating voltage and power consumption.

There are traps (due to the crystalline structures and defects [62]) in the organic semiconductor materials, and these affect V_{TH} . Specifically, as the mobile charge carriers can only be induced and accumulated in the organic semiconductor-dielectric interface after the traps are filled, V_{TH} is inevitably increased. It was reported [63] that the charge states or dipoles at the SiO₂ dielectric surface lead to an increase in the traps. To reduce the traps, PE processes usually include interface modulation between the dielectric and organic semiconductor layers and deposition of a well orientated semiconductor layer.

On/Off Current Ratio

The on/off current ratio of the OTFT is the ratio of current in the saturation region to the current in cut-off region. This parameter is important to determine the switching behavior of an OTFT, particularly in digital and switching applications. It was reported [65] that the on/off current ratio is strongly dependent on the dielectric and the organic semiconductor. The on/off current ratio can be increased with dielectric material with higher dielectric constant (k), a thinner dielectric layer thickness and a thinner organic semiconductor layer thickness. This parameter can be expressed [65] as:

$$\frac{I_{ON}}{I_{OFF}} = \frac{C_{OX}\mu(V_{GS} - V_{TH})^2}{\sigma t_{OSC} V_{DS}} \quad (2.11)$$

$$I_{OFF} = \frac{W}{L} \sigma t_{OSC} V_{DS} \quad (2.12)$$

where σ (S/m) is the conductivity of the semiconductor at cut-off state,

L (m) is the channel length,

W (m) is the channel width,

t_{OSC} (m) is the thickness of the semiconductor layer, and

C_{OX} (F/m²) is the gate dielectric capacitance per unit area.

It can be seen that a reduced dielectric layer thickness and organic semiconductor layer thickness lead to desirable increased saturation current, I_{ON} , and decreased cut-off current, I_{OFF} , respectively. The on/off current ratio is more dependent on the thickness of the organic semiconductor layer due to the dominant influence of the off-current over the on-current. Of specific interest, the off-current can be reduced substantially by reducing the thickness of the organic semiconductor. It was reported [66] that the off-current is reduced by six orders of magnitude with a decreased thickness of semiconductor layer from 45 nm to 10 nm. For an OTFT [67] with P3HT as the organic semiconductor, the on/off current ratio is substantially increased from 10 to 5×10^{10} with a decreased thickness of the organic semiconductor

layer from 160 nm to 20 nm. OTFTs with shorter channel length are also desired to achieve a high on/off current ratio.

Sub-Threshold Slope

The sub-threshold slope, SS (mV/decade), of an OTFT is determined by the ratio of change in the gate-source voltage to the change in the output drain current in logarithmic scale. The sub-threshold slope can be expressed [57] as:

$$SS = \frac{dV_{GS}}{d \log_{10}(I_{DS})} \quad (2.13)$$

This parameter is important as it determines the switching behavior of an OTFT. The sub-threshold slope is strongly dependent on the traps of the organic semiconductor, on the electrode-organic semiconductor interface and on the dielectric-organic semiconductor interface. Higher carrier mobility will also result in a desirable sharper (higher gradient) sub-threshold slope; a sharper sub-threshold slope is desirable and a lower sub-threshold slope is desirable.

It was reported [68] that the disorientated organic semiconductor layer will lead to an increase in the traps and results in an undesirable increase in the sub-threshold slope. By surface modifying the dielectric-organic semiconductor interface and the electrode-organic semiconductor interface [69], a self-assembled monolayer (SAM) can be added into the dielectric and electrode surfaces. These treatments will facilitate the reduction of the traps and desirably reduce the sub-threshold slope. It

was reported [70] that the sub-threshold slope of the OTFT reduced desirably from 800 mV/decade to 100 mV/decade after the modification of the Al_2O_3 dielectric surface. In [50], the DG OTFT structure was reported with a lower sub-threshold slope compared to the single gate OTFT structure.

Some of the aforesaid methods are employed in an innovation fashion in the Fully-Additive process developed in this Ph.D. program; see Chapter 3 later.

2.2 Materials

There is substantial research and concerted effort by the PE community to develop and synthesize functional materials for PE applications, particularly, the organic semiconductors [34]. In general, other than high performance (e.g. carrier mobility), it is desired that materials used are low cost, feature high environmental stability, high process-ability, etc. While the performance of an OTFT strongly depends on the materials of the organic semiconductor layer, the materials of other layers, including substrates, dielectrics, electrodes, etc., are also important. The different materials of the OTFTs, including substrates, electrodes, dielectrics and semiconductors, will now be reviewed.

2.2.1 Substrates

A number of substrates [71] have reportedly been used for OTFTs. The plethora of materials include inorganic and organic materials, rigid and flexible materials, etc. Inorganic substrates such as glass and silicon wafer offer high temperature resistance, high flatness and low solubility. On the other hand, organic substrates such as polycarbonate (PC), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), and polyimide offer high toughness, flexibility and light weight.

The selection of a substrate material to a large part depends on the intended applications. The silicon wafer is often used as a substrate because of its intrinsic properties and for the ease of producing a dielectric layer. Glass substrate is necessary for making organic light emitting diodes and solar cells. Organic substrates are essentially required for flexible (in terms of bending) electronics. At this juncture, the OTFTs fabricated on the organic substrates, e.g. polyimide [72], have shown comparable performance to that fabricated on the glass substrates [73]. Many PE applications, such as solar cells and circuits, have been demonstrated on glass and organic substrates.

The substrate used in this Ph.D. program is the PET plastic film. This is largely for its low cost and flexibility (to bending, etc.)

2.2.2 Electrodes

The electrode materials require high conductivities, good adhesion and amend-ability to patterning. There are both inorganic and organic materials for electrodes. In general, the inorganic materials for electrodes are easy to pattern, while organic materials for electrodes feature high solution print-ability and high flexibility.

Metals are the most frequently used materials for the electrodes of OTFTs. Metals such as gold (Au), silver (Ag), aluminum (Al), etc. can be prepared and deposited by thermal evaporation or modified with organic materials to become nanoparticles-based polymer and deposited by printing methods.

As delineated earlier, one of the important parameters of the materials for electrodes to obtain high performance OTFTs is the work function. With the compatible work function (Fermi level) of the electrode and the HOMO/LUMO of the organic semiconductor, the electrode-organic semiconductor interface will be matched and lead to a low contact resistance and energy gap. Moreover, the work function of the gate electrode should also be compatible with the HOMO/LUMO of the organic semiconductor to attain low threshold voltage. The work functions of some typical inorganic electrode materials are summarized in Table 2-1.

Table 2-1 Work functions of inorganic electrode materials

Electrode Materials	Work Function (eV)
Heavily doped <i>n</i> -type silicon	4.15
Heavily doped <i>p</i> -type silicon	5.27
ITO	5.3
Gold (Au)	5.1 – 5.47
Platinum (Pt)	5.12 – 5.93
Silver (Ag)	4.26 – 4.74
Aluminum (Al)	4.06 – 4.26
Magnesium (Mg)	3.66
Palladium (Pd)	5.12
Chromium (Cr)	4.5
Nickel (Ni)	5.04 – 5.35

Since the HOMO level of most *p*-type organic semiconductors is between 4.5 eV – 6.5 eV, Au is frequently used as the source and drain electrodes in *p*-type OTFTs due to its high work function (~ 5.3 eV). Due to the poor adhesively of Au with the dielectric layer, a thin layer of metal such nickel (Ni), titanium (Ti), and chromium (Cr) is often added and deposited prior to Au. Indium tin oxide (ITO) is often used in solar cells for both its high work function (~ 5 eV) and its transparency. Meanwhile, low work function metals such as magnesium (Mg), lithium (Li), and calcium (Ca) are selected as cathode terminal in solar cells.

At this juncture, besides the organic materials that make use of metal nanoparticles as the electrode materials, a series of conducting polymers have been reported [74] with better transparency and flexibility. These include Poly-3,4-ethylenedioxythiophene:styrene sulfonic acid (PEDOT:PSS), PSS (poly-(styrene

sulfonate)), and PANI-CSA (polyaniline doped with camphor-sulphonic acid), and their chemical structures are depicted in Figure 2-9.

Figure 2-9 Chemical structures of commonly used organic conducting polymer electrode materials: (a) PEDOT: PSS; (b) PSS; and (c) PANI-CSA

In Chapter 3, we will provide details of the material used for the electrodes and the associated modification processes to obtain an appropriate work function.

2.2.3 Dielectrics

The dielectric materials require high resistivity to isolate the gate and organic semiconductor layer, and high dielectric constant. These materials can also serve as the encapsulation layer for isolation and packaging. The charge density at the dielectric-organic semiconductor interface strongly depends on the dielectric constant

(k) and the thickness of the dielectric layer (t_{ox}). Moreover, it should feature good interface with the semiconductor to avoid the generation of traps. High- k dielectric materials, due to their smaller band gaps, are generally preferred because sharper sub-threshold slope and lower threshold voltage can be achieved compared to the low- k dielectric materials. Moreover, thin dielectric layer is desired to lower the operating voltage. The dielectric materials should also feature sufficient breakdown voltage and environmental stability.

Inorganic dielectrics generally have high dielectric constant and can be easily realized by the oxidation of the gate layer by thermal treatment. The performance, in terms of dielectric constant, for the different inorganic dielectric materials is summarized in Table 2-2.

Table 2-2 Dielectric constant of inorganic dielectric materials

Inorganic Dielectric Materials	Dielectric Constant
Silicon dioxide (SiO_2)	3.5–4.5
Aluminum oxide (Al_2O_3)	9
Zirconium dioxide (ZrO_2)	25
Lanthanum oxide (La_2O_3)	30
Hafnium oxide (HfO_2)	22
Titanium dioxide (TiO_2)	80
Silicon nitride (Si_3N_4)	6.5

Organic dielectric materials, such as PMMA, PVP, and PVA, have reportedly [75] demonstrated processing by means of low cost printing techniques, high

adherence, and with reasonable dielectric properties. The performance, in terms of dielectric constant, for the different organic dielectric materials is summarized in Table 2-3. In general, high operating voltage is observed in the OTFTs with organic dielectric due to their low dielectric constant and relatively thick layer with printing methods. Although a thin dielectric layer of organic materials is generally desired, this is somewhat difficult because it often leads to a high leakage current due to the pin holes in the thin organic dielectric layer.

Table 2-3 Dielectric constant of organic dielectric materials

Organic Dielectric Materials	Dielectric Constant
Polyimide (PI)	2.6
Poly vinyl phenol (PVP)	5.3
Poly (4-vinyl phenol) (P4VP)	5.3
Polystyrene (PS)	2.6
Polyvinyl alcohol (PVA)	7.8
Polymethyl methacrylate (PMMA)	3.6
Barium zirconate titanate (BZT)	3.8

2.2.4 Organic Semiconductors

There has been concerted effort with the PE community to improve the carrier mobilities and other characteristics of the organic semiconductors for practical commercial applications. Organic semiconductors are classified as the conducting polymers and small molecules. The mobility of conducting polymers was reported [76] to be lower than small molecules due to their higher molecular weight. For

example, the mobility of small molecules ($\sim 3.2 \text{ cm}^2/\text{Vs}$) [58] is higher than that of polymers ($\sim 0.9 \text{ cm}^2/\text{Vs}$) [76]. To achieve high carrier mobility, the grains of the semiconductor should be large in size. Furthermore, highly oriented organic semiconductor films result in a significant performance improvement of the OTFTs. The organic semiconductor materials are categorized to *p*-type organic semiconductors, *n*-type organic semiconductors and ambipolar semiconductors.

P-type Organic Semiconductors

Most of the organic semiconductors reported thus far feature the hole as the charge carrier. At this juncture, the emphasis of *p*-type organic semiconductors appears to be polymers and π -conjugated oligomers (small molecules). Typical *p*-type conducting polymers include Poly(3-hexylthiophene) (P3HT), Poly(triarylamine) (PTAA), Poly-9,9'-dioctyl-fluorene-co-bithiophene (F8T2), and Poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophenes (PBTTT). On the other hand, the commonly used small molecule organic materials include pentacene, Copper phthalocyanine (CuPc), and tetracene. The performance, in terms of charge carrier mobility, for the various reported *p*-type semiconductors is summarized in Table 2-4.

Table 2-4 Charge carrier mobility of various reported *p*-type organic semiconductors

<i>P</i>-type Organic Semiconductor Materials	Mobility (cm²/Vs)	Supply Voltage (V)	Reference
Pentacene	1.8	6	[77]
CuPc	0.02	100	[78]
TIPS-Pentacene	0.02	60	[79]
DiF-TESADT	0.17	40	[80]
Tetracene	0.25	60	[81]
P3HT	0.11	100	[60]
PDBT-co-TT	0.94	75	[76]
F8T2	0.0001	10	[82]
PTAA	0.041	40	[83]
PBTTT	0.34	70	[84]

Pentacene is probably the most widely used *p*-type organic semiconductor due to its relatively high carrier mobility. In addition to high mobility, it features advantages in terms of high stability in the ambient environment, highly orientated thin film morphology and compatible interface with commonly used electrode metals such as gold and aluminum [85]. Nevertheless, its disadvantage is that it cannot be used for low cost printing methods due to its extreme low solubility. In comparison to pentacene, P3HT [86] exhibits much lower mobility but features high solubility in a wide range of organic solvents, thereby rendering it suitable for low cost printing methods [87].

In order to enable the high performance pentacene material to be compatible with the solution-based printing methods, soluble pentacene precursors [88, 89] were synthesized to obtain the pentacene thin film. Some of the commonly used pentacene

precursors include 6,13-bis(triisopropyl-silyl)ethynyl pentacene (TIPS-Pentacene) and difluoro-tri(tetracenethylsilyl)ethynyl anthradithiophene (diF-TESADT).

In this Ph.D. program, the *p*-type organic semiconductor is adopted, specifically, TIPS-Pentacene. This is largely because of its intrinsic high carrier mobility and high solubility; see Chapter 3 later.

N-type Organic Semiconductors

At this juncture, the majority of the research effort is largely focused on achieving high performance *p*-type organic semiconductors, with considerably lesser effort on *n*-type organic semiconductors. From a circuit design perspective, both types are desirable as they facilitate designs with lower static power. Put simply, the development of *n*-type organic semiconductors is probably equally important if practical printed electronic circuits of note are to be realized.

To realize an *n*-type OTFT, the semiconductor used would allow the injection of electrons into its LUMO level. At this juncture, virtually all *n*-type organic semiconductors suffer from instability in the ambient conditions because of the reaction with either water or oxygen. Furthermore, most of the commonly used electrode materials are incompatible because they exhibit work functions better suited for the injection of holes into the HOMO level (*p*-type) than the electrons into the LUMO level (*n*-type). It is perhaps not surprising that high performance *n*-type

transistors are yet to be reported, and this is evident in the summary of the performance for various reported *n*-type semiconductors in Table 2-5.

Table 2-5 Charge carrier mobility of various reported *n*-type organic semiconductors

<i>N</i>-type Organic Semiconductor Materials	Mobility (cm²/Vs)	Supply Voltage (V)	Reference
F ₁₆ CuPc	0.03	20	[90]
PCBM	0.13	80	[91]
Perfluoropentacene	0.22	100	[92]
Polyera Activink N1400	0.037	60	[83]
PDI-8CN2	0.33	50	[93]
PTCDI-C13H27	0.6	100	[94]
PDPP-TBT	0.1	40	[95]
P(NDI2OD-T2)	0.5	60	[96]
NDI	0.41	100	[97]

The performance of *n*-type organic semiconductors may be improved by adding –Cl, –CN, and –F functional groups into the materials, since these functional groups are capable of withdrawing the electrons. It was reported [90] that by adding –F functional group into the CuPc, the resulting Copper hexadecafluorophthalocyanine (F₁₆CuPc) features the *n*-type mobility of ~ 0.03 cm²/Vs. It nevertheless suffers from being affected by the ambient conditions. It was reported [97] that in inert atmosphere, the mobility of NDI can reach a respectable ~ 6.2 cm²/Vs, but under ambient conditions, it was found to be a somewhat low ~ 0.41 cm²/Vs.

In this Ph.D. program, there has been little effort in attempts to synthesize or to realize *n*-type OTFTs. This is a further research proposal delineated in Chapter 5.

Ambipolar Organic Semiconductors

As delineated earlier, a semiconductor that allows the injection of both holes and electrons under certain conditions is known as an ambipolar semiconductor. It is possible to operate an ambipolar transistor as a *p*-channel device or an *n*-channel device, simply by controlling the drain and the gate bias. For an ambipolar transistor, it is necessary that the work functions of the source and drain electrodes should be close to both the HOMO and the LUMO levels of the organic semiconductor to enable a balanced charge injection of holes and electrons. This implies that the energy gap of the ambipolar semiconductor should be sufficiently small (up to few hundred meV) [98]; however, in most of the organic semiconductors, due to the large energy gap (> 1.5 eV), only one type of charge carriers (either holes or electrons) can be injected. The performance of various reported ambipolar semiconductors is summarized in Table 2-6.

Table 2-6 Charge carrier mobility of various reported ambipolar organic semiconductors

Material	Mobility (cm ² /Vs)		Supply Voltage (V)	Reference
	hole	electron		
NiDT	2.5×10^{-4}	2.5×10^{-4}	30	[99]
Indigo	0.005	0.01	10	[100]
PDPP-TBT	0.5	0.17	40	[101]
C60/Pentacene	0.14	0.23	100	[102]
PDPP3T	0.2	0.2	80	[103]

2.3 Printing/Patterning Technologies

Electrode and semiconductor printing and patterning are necessary for the fabrication of OTFTs. Specifically, the patterning of organic semiconductors would need to be established such that low parasitic leakage (leakage current from the semiconductor to the gate due to the overlap between the gate layer and semiconductor layer outside the channel region) and low crosstalk (leakage current directly from semiconductor layer to the gate layer due to the contact of these two layers) are obtained. This is to obtain a high I_{ON} / I_{OFF} ratio. Typically, the channel length of OTFTs would need to be $\leq 100 \mu\text{m}$ to be useful for most applications.

The major considerations for patterning include cost, throughput, achievable feature size, and compatibility with organic semiconductors. Various patterning techniques have been reported and they can be generally categorized into three types: optical photolithography [104, 105], shadow masking [106, 107], and printing [36, 108, 109]; another classification is Additive and Subtractive processes delineated in

Chapter 1. Of the three techniques types, optical photolithography is a Subtractive process while the other two methods, shadow masking and printing, are Additive processes. These patterning methods will now be critically reviewed, including their advantages and disadvantages.

2.3.1 Optical Photolithography

Optical photolithography is an established Subtractive technique, used over three decades for micro-fabrication of semiconductor devices [110]. This technique allows the realization of highly complex circuits and systems with multiple layers of interconnections and with resolutions as small as 22 nm.

Photolithography, as described in [111], essentially involves a way to transfer geometric shapes from a mask to a substrate such as a silicon wafer. During this process, photoresist is applied to the wafer and subsequently exposed to UV (ultra violet) light through a mask. The mask can be aligned against the substrate in a contact mode, proximity mode, or projection mode. Chemical changes occur in the exposed regions making the photoresist either more soluble (positive resist) or less soluble (negative resist) in a given solvent. The soluble part of the resist is subsequently removed leaving behind a photoresist pattern. An organic semiconductor or other materials is then deposited on the photoresist pattern. Dissolving the photoresist pattern removes the active material above it giving the patterned semiconductor or metal. A photoresist layer can also be patterned on an un-

patterned metal or semiconductor layer and used as a protecting layer when the exposed active material region is etched or dissolved away.

Both metal and conducting polymer electrodes can be fabricated using standard photolithography followed by a “lift-off” process. In this case, a dissolving photoresist removes the metal or polymer deposited above it, leaving behind the desired metal or polymer patterns [110].

Optical photolithography generally has relatively high cost per unit area. The substrate size is limited by the size of the exposure tools – the area is small. It is largely suitable for the production of high-end electronics such as microprocessors, etc. However, for low-end applications of PE, the high expense is prohibitive. These shortcomings and the small areas render this patterning method un-scalable.

For these reasons, the optical photolithography is not adopted in this Ph.D. program.

2.3.2 Shadow Masking

Organic semiconductors and metals can be patterned through a shadow mask to form OTFTs [112, 113]. Shadow masking process, is “dry”, i.e. there is no damage to the semiconductors/active materials. The feature size achievable with typical commercially available stencil shadow masks is somewhat large – typically 100 μm . Although evaporation at an angle with a culminated vapor can yield feature sizes less than the feature size of the mask, this requires precise control of the

substrate and evaporation source positions and is generally undesirable in manufacturing. In addition, the size of the substrate is limited by the size of the mask. Furthermore, multilayer alignment of the shadow mask over a large area is formidable. Overall, shadow masking is expensive (a vacuum evaporation process) and small size area rendering this un-scalable patterning method.

For these reasons, shadow masking is not adopted in this Ph.D. program.

2.3.3 Additive Printing Methods

Driven by the need for low cost and scalability, it is not surprising that at this juncture, Additive printing methods have gained increasing acceptance over the photolithography and shadow mask methods. As delineated in Chapter 1, Additive printing methods including screen-printing, ink-jet printing, gravure printing and flexography printing are already widely used for PE albeit for ‘simplistic’ devices and circuits such as solar cells, inverters, etc.; ‘simplistic’ in the sense of limited intelligence/signal processing. In this section, these Additive methods will be critically reviewed and the reasons for adopting the screen printing method will be explained, including the challenges thereof.

Screen Printing

Screen printing is a well-established and relatively simple printing method that has been used for extensively printing tee-shirts (graphic art) and printed circuit boards. It is parsimonious in the sense that little of the coating solution is wasted during printing. Its main distinction from all other printing and coating techniques is a relatively thick wet film thickness, and a requirement for a relatively high viscosity and a low volatility coating solution.

Screen printing, as described in [42], is typically a stencil process where the ink is transferred to the substrate through a stencil covering a fine fabric mesh screen. The latter is stretched on a frame, allowing pressure to be applied to the stencil by a squeegee. The ink is poured on the stencil and the squeegee is drawn across the frame, forcing the ink through the stencil, as depicted in Figure 2-10.

Figure 2-10 Screen printing process

Screen printing may also be a rotary process, where the mesh screen has a cylinder shape, and the ink is poured inside the cylinder and the squeegee, also within

the cylinder, forces the ink out of it, through the stencil. Screen printing inks are viscous (0.1 Pa·s to 10 Pa·s) and allow thick ink films (varying from 1 μm to 100 μm). Inks may dry through solvent evaporation or be UV cured. The possibility of large area printing and relatively thick films (allowing bending of the substrate) render screen printing particularly interesting. Nevertheless, the primary limitations with screen printing are the relatively large resolution/feature, approximately 100 μm and the high viscosity of available inks (difficulty of processing).

Interestingly, screen printing to date has largely been used for photovoltaic applications and not for complex ('intelligent' or with signal processing) circuits [18, 114, 115]. The reasons for this will be delineated in Section 2.4 below.

Ink Jet Printing

Ink jet printing is, at this juncture, a mature technique for printing texts and pictures with high resolution. OTFTs can be printed by replacing conventional inks in the cartridges with specially formulated polymer solutions [27, 104, 116-118]. From a technological evolution viewpoint, this method is arguably the most developed printing process over the last decade. This can probably be attributed to its versatility – this digital, non-contact printing process, can print directly from computer data onto virtually any substrate, of any size. Not unexpectedly, this requires very complex ink formulations which may be water-based, solvent-based or hot melt, with viscosities ~ 0.01 Pa·s.

In the ink jet process, as described in [42], a single ink droplet can be jetted from the ink cartridge through the nozzle, as depicted in Figure 2-11. This happens when the pressure within the ink cartridge increases, and the droplets will form the pre-defined pattern without using a mask. Not requiring masks is a major cost and versatility advantage.

Figure 2-11 Ink jet printing process

Ink jet printing is a promising technique for printing large area electronics due to its flexibility – printing of contacts, semiconductors, and dielectrics on large substrates. Using this method, the printing resolution for the channel length can be desirably small – as small as 10 μm . Nevertheless, the major drawbacks of ink-jet printing are its relatively low throughput (lowest amongst Additive processes, as depicted in Figure 1-2), the unavailability of inks for conductors and dielectrics (no problems with ink jetting semiconductors), and de-wetting issues.

Gravure Printing

Gravure printing is well established and adopted in the publication industry for long runs, largely due to its excellent consistency and seamless printing process. Despite its ubiquity in conventional printing, there is relatively little research to exploit this processing method to print and pattern organic devices [56, 119-121].

Gravure printing, as described in [42], is an intaglio process where an engraved cylinder transfers liquid ink held by its cells to the substrate under very high pressure, as depicted in Figure 2-12 – effectively, roll-to-roll processing. A steel-based cylinder is covered with a thin nickel layer, and then electrochemically covered with a thick copper layer. It is then engraved. The resulting cells may vary both in width and depth (the latter can reach 40 μm). After engraving, the cylinder is covered with a thin chrome layer, allowing hardness and resistance to wear. To print, the cylinder steeps and rotates in an ink reservoir. The excess ink is wiped away by a doctor blade and the ink remaining in the cylinder cells is transferred to the substrate under pressure against the cylinder.

Figure 2-12 Gravure printing process

Gravure inks may be water-based or solvent-based, their viscosities and ink film thicknesses vary from 0.01 Pa·s – 0.05 Pa·s and from 8 μm – 12 μm , respectively. However, this process has three limitations. First, the pressure required to print is so high that it limits its applications only to flexible substrates; not an issue in the context of this Ph.D. program. A more complex, however, offset gravure does exist and could overcome this difficulty where an intermediate, compressible cylinder is inked under pressure and transfers the ink to the rigid substrate. The second limitation of gravure comes from its principle of printing – since the image is built from separate cells, a straight line is actually a jagged line. Although laser engraving can drastically reduce this phenomenon, this is to be taken into account when printing electronic components, in order to avoid any possible edge effects. Third, this method does not render itself to realize complex circuits because there is a lack of appropriate conductor inks (such as silver or gold), and the alignment (registration) is challenging.

Flexography Printing

Flexography printing process was initially developed for packaging applications (e.g. corrugated cardboard) [122-124]. Flexography, as described in [42], uses a relief flexible plate that applies fluid ink to the substrate. The ink usually comes from an ink chamber, in contact with a metering roller called "anilox" and closed by two doctor blades, as depicted in Figure 2-13. The metering roller surface contains cells of regular size and shape, where the number of cells per centimeter varies from 40 to 230, according to the ink film thickness and to the resolution required. The doctor blade wipes the excess ink from the surface of the anilox, leaving only the needed amount within the cells. The plate thickness goes from fractions of a millimeter to several millimeters, depending on the substrate to be printed. The viscosities of flexographic inks vary from 0.01 Pa·s to 0.1 Pa·s. Inks may be water-based or solvent-based. The flexographic process is able to print on a very wide variety of substrates, including paper, board, corrugated cardboard, flexible and rigid polymers, metals, glass, etc. The printed ink film thicknesses vary from 6 μm to 8 μm , which is suitable for printing electronics, and the resolution is typically 250 μm .

Figure 2-13 Flexography printing process

Although the flexography is an improvement of the gravure method, they both share similar limitations. The advantage here nevertheless is largely its applicability to various types of substrates, unlike the gravure which is largely only applicable to soft substrates.

2.4 Major Challenges of Printed Electronics

Given the critical review of various printing technologies in the proceeding sections of this chapter, it can be appreciated that the formidable challenges of PE, as delineated in Chapter 1, include:

- (i) Charge carrier mobility and electrical conductivity of materials;
- (ii) Resolution, registration (alignment between printed layers) and process stability; and

- (iii) Circuit design accommodating the aforesaid challenges (see Chapter 3 later).

Challenge (i) pertains to the materials, the first supply chain in Figure 1-1. Despite the considerable research into materials, the materials available today remain largely nascent (in terms of performance, particularly when compared to silicon) and remain limited for the printing of conductors, dielectrics and organic semiconductors. Undoubtedly, each printing process requires its unique ink formulation. In this respect, one of the first steps of any PE effort is the selection of a specific printing process and thereafter, to ascertain appropriate materials for the printing to yield the highest potential for compatibility with the substrate and other pertinent printed layers. At this juncture, the available organic semiconductors suffer from low carrier mobility ($< 1 \text{ cm}^2/\text{Vs}$) and relatively poor air stability. The performance is highly influenced by the printing process and the compatibility of the interface between layers.

Challenge (ii) pertains to the printing process, the second supply chain in Figure 1-1. The review in this chapter showed that there is no well-developed Additive printing/patterning procedures for Fully-Additive printed devices, including OTFTs, interconnects and passive components. Conversely, Subtractive processes do offer all said steps but as delineated earlier, these processes have major shortcomings including ‘non-greenness’ (toxic chemicals), not-on-demand, not-scalable and expensive. It is apparent that to meet the objectives of this Ph.D. program, many unknown/undeveloped procedures would need to be investigated and developed for a Fully-Additive process, including multiple layers of interconnection for complex

circuits and scalability. Amongst the Additive printing/patterning techniques reviewed, the resolution ranges from 10 μm to 250 μm , these resolutions are more than ten technology nodes behind silicon process. This large resolution renders the application of PE to substantially lower speed.

An important consideration between the materials and printing is that the mobility of the organic semiconductor degrades significantly upon printing. For example, as reported in literature (and observed during this Ph.D. program), the mobility of TIPS-Pentacene typically reduces by one to two orders of magnitude when printed. In other words, the research effort in printing, as delineated in Chapter 1, would also include a printing procedure that minimally degrades the mobility of the semiconductor.

In view of this Ph.D. program, with the primary objective of printing complex electronic circuits (with ‘intelligence’ and/or signal processing) on flexible substrates, yet low cost, on-demand, scalable and “green”, an Additive printing method – the screen printing process – is adopted. This printing process offers a mid-low resolution of $\sim 100 \mu\text{m}$. As delineated earlier, despite the potential of this process, to the best of the author’s knowledge, the state-of-the-art screen printing [125-128] remain rudimentary. For example, [125] reported only one layer (electrode) is screen printed and the semiconductor is thereafter deposited by means of vacuum evaporation. In [18], the electrode layer is deposited/patterned by laser ablation (Subtractive method) and the following layers are screen printed. In the case of

reported Fully-Additive screen printing, state-of-the-art screen printing [115] has only realized solar cells for photovoltaic applications.

In short, in view of the critical review of printed electronics, a Fully-Additive screen printing process with substantially improved carrier mobility will be developed with the possibility of realizing complete (and complex) circuits.

2.5 Conclusions

In this chapter, OTFT principles, materials and printing methods (for both ‘Subtractive’ and ‘Additive’) have been reviewed. Different structures of OTFT were reviewed in terms of performance (charge carrier mobility, threshold voltage, etc.) and process-ability. Of the structures reviewed, the BGBC structure was deemed to be the most appropriate due to its compatibility to Additive (low cost) printing methods and process stability.

A comprehensive review of materials, including organic semiconductors, has been provided. On the basis of the review, it was ascertained that the small molecule *p*-type organic semiconductors (such as TIPS-Pentacene) offer the most advantages in terms of charge carrier mobility, print-ability and ambient stability. Also on the basis of the review, the Additive printing process, specifically, screen printing process, was selected for its compatibility for printing on flexible substrates – it is ‘green’, on-

demand, scalable, flexible, and inexpensive. Nevertheless, there are major challenges in this process, including low carrier mobility and the absence of any reported realized circuits and systems of note.

Chapter 3   A Novel Fully-Additive Printing Electronics Process on Flexible Substrates and Analog Amplifiers

3.1 Introduction

A large portion of this chapter has been published* in the Organic Electronics journal [6].

In this Chapter, a Fully-Additive printing process [45, 129, 130] that circumvents the aforesaid shortcomings of state-of-the-art Fully-Additive processes (refer to Chapter 1 and Chapter 2) is proposed. This proposed process renders the ensuing Fully-Additive printed circuits/systems competitive to (substantially more complex) Subtractive-based processes in terms of carrier mobility and the ability to print complex circuits/systems including transistors, passive components (capacitors, resistors and inductors) and two metal-interconnect layers on flexible substrates (such as plastic films, e.g. polycarbonate film [42]). Of specific interest, the ensuing PE circuits/systems from the proposed Fully-Additive printing process feature the aforesaid often-touted merits of PE – ‘green’, on-demand, scalable, flexible and

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* This publication was the second-most downloaded article in the science direct database (a database of > 2,500 journals) in the field of printed electronics for the last 90 days in June 2014. The number of downloads exceeded 1,700 downloads.

inexpensive. To the best of the author's knowledge, the proposed process is the first Fully-Additive process that features the ability of realizing complex circuits/systems on flexible plastic films. The printing herein is a screen printing process similar to that ubiquitously used for printing multiple-colored prints on tee-shirts, and the equipment and facilities used are largely the same (save the chemicals and curing steps) – put simply, low-cost and unsophisticated. The proposed Fully-Additive printing process features the highest semiconductor carrier-mobility of all reported Fully-Additive processes ($\sim 1.5 \text{ cm}^2/\text{Vs}$, which is three times higher than state-of-the-art; see Table 3-2 later) and capable of Fully-Additive printing to realize passive components (capacitors, resistors and inductors), and two metal-interconnect layers. The range of the values of the printed capacitors, resistors and inductors are large: respectively 224 pF/cm^2 to 1.1 nF/cm^2 , $3.3 \text{ k}\Omega/\square$ to $800 \text{ k}\Omega/\square$ and $1 \text{ }\mu\text{H}$ to $8 \text{ }\mu\text{H}$ with quality factor Q of 2; Q of 2 is sufficient for many applications, including RFIDs. These large ranges are desirable for sake of generality for the efficacious design and realization of analog and mixed-signal circuits/systems.

In this chapter, on the basis of the proposed Fully-Additive screen printing process, three fundamental analog (a proposed and two conventional differential amplifiers) circuits are demonstrated. Of specific interest in terms of circuit design, a novel feedback with both positive and negative paths is proposed and employed for the proposed amplifier to simultaneously improve the gain ($> 14 \text{ dB}$ higher than the conventional Fully-Additive three-stage amplifier of equivalent hardware and printed area) and higher than reported Subtractive-based amplifiers, and mitigate the effects of process variations (reduced to 5% of the Fully-Additive conventional amplifiers).

Despite the analog circuits realized by means of a Fully-Additive process, it is shown that they are highly competitive when compared to reported circuit counterparts based on the substantially more complex and expensive Subtractive-based processes.

This chapter is organized in the following manner. In Section 3.2, the proposed Fully-Additive screen printing process is presented. In Section 3.3, several Fully-Additive analog circuits are demonstrated, including proposed and conventional differential amplifiers. Finally, conclusions are drawn in Section 3.4.

3.2 Proposed Fully-Additive Printing Process

The overall spirit of the proposed screen printing process is low-cost and simplicity (including processing steps, chemicals used, and the associated equipment (and infrastructure)), yet high performance (in terms of high carrier-mobility, capability to print complete circuits/systems on plastic films, and in terms of ensuing circuits/systems parameters) when compared to the substantially more expensive and complex state-of-the-art Subtractive-based processes. As delineated earlier, the need for low-cost and simplicity, thereby realizing the aforesaid often-touted attributes of PE, mandates a Fully-Additive process.

For sake of printing simplicity, the adopted structure of the printed transistor is the conventional Bottom Gate Bottom Contact structure, which is reviewed in Section 2.1, as depicted in Figure 3-1 (a). The simplicity further includes the use of readily available and ‘easy-to-handle’ (non-corrosive) materials/chemicals, and low

temperature $< 120\text{ }^{\circ}\text{C}$ that is easily tolerated by low-cost flexible plastic film. The associated equipment and infrastructure are also simple and unsophisticated (hence low-cost), as delineated earlier, is largely the same ubiquitous equipment for printing multi-colored tee-shirts. Specifically, these include a screen printer (essentially a mask holder to mount a screen mask and a squeegee to spread the ink on the mask); the added equipment required are also low-cost and unsophisticated, including an ultra violet (UV) light source and a slot die coater.

(a)

(b)

Figure 3-1   (a) Cross section of printed transistors, capacitors, resistors and inductors; and (b) their microphotographs

The proposed printing method encompassing the printing of Layers 0-5 is summarized in Table 3-2 below, where the simplicity of the printing process and the equipment (and infrastructure) is evident.

Table 3-1   Proposed Fully-Additive printing process

	Layers	Materials	Printing Procedure
Layer 0:	Substrate (flexible plastic film)	Polycarbonate	Clean the substrate to remove contaminants
Layer 1:	Gate, bottom electrode of capacitors, inductor	Silver	With the First stainless screen mask, print the pattern of Layer 1, and then cure in an oven
Layer 2:	Dielectric of transistors and capacitors, isolation between top and bottom interconnections	Dupont 5018 [123]	With the Second stainless screen mask, print the pattern of Layer 2, and then cure in UV light
Layer 3:	Resistor	Dupont 5036 [123], Dupont 7082 [123]	With the Third stainless screen mask, print the pattern of Layer 3, and then cure in an oven
Layer 4:	Drain, source, top electrode of capacitors, vias, interconnections	Silver	With the Fourth stainless screen mask, print the pattern of Layer 4, and then cure in an oven. Thereafter, immerse into the PFBT (Pentafluorobenzenethiol) solution for 1 hour
Layer 5:	Semiconductor	TIPS-Pentacene	Coat Layer 5 using a slot die coater and then cure on a hotplate

The designed resolution of the current screen printing is 100 μm – comparable with that reported in literature. Nevertheless, due to the de-wetting of the silver paste, the actual resolution (including the channel length of OTFTs) between different printed foils (inter-foil) varies between 90 μm to 100 μm ; nevertheless within the same film (intra-foil), the channel length is largely the same and the variations are yet to be ascertained.

The measured finger length (the width of the printed electrodes line) and height (depth of the printed electrode line) is 300 μm and 20 μm respectively, consistent with the design; the variations are also small and yet to be ascertained. The relative small variations observed in the finger length and height are due to a thick film and thus, more controllable during the screen printing process. The thickness of the gate layer, dielectric layer and vias are 5 μm , 20 μm and 20 μm respectively. After numerous printing and fine-tuning of the process, for the resolution of 100 μm , the yield is quite consistent – almost 100% for a substrate as large as A3 size for the screen printed circuits with one layer of interconnect. Despite the laboratory conditions (vis-à-vis a more controlled manufacturing environment), this outcome gives the confidence that the proposed printing process would allow the realization of low cost, large area and complex circuits for the PE applications, yet green since the process is Additive.

The printing of Layers 1-4 is similar to reported screen printing methods, e.g. [18], for PE. However, to circumvent the severe low carrier mobility problem of these reported methods, two innovations are proposed.

The first innovation involves an augmentation process step to Layer 4 for the drain and source of the transistor for modifying the electrode-semiconductor interface. In the proposed process, silver is used as the electrode material largely because screen-printable silver paste is readily available and its electrical and thermal conductivities are high. However, a major drawback of silver is its low work function, $\Phi_{Ag} = 4.7$ eV. Specifically, as the HOMO (highest occupied molecule orbital) of TIPS-Pentacene ($\Phi_{TIPS-PEN} = 5.28$ eV) is relatively high while Φ_{Ag} relatively low, the overall work function is poorly matched, resulting in high injection barrier, hence low carrier mobility. To mitigate this mismatch, the increment of the work function of silver is proposed [42] by immersing the printed drain and source electrodes into PFBT (Pentafluorobenzenethiol) solution.

On the basis of experiments and reiterations thereof, the developed modification process of the silver electrodes is summarized as follows:

1. Clean the screen printed devices with isopropyl alcohol (IPA) and Di-H₂O to remove residual particles and ions on the devices sheet.
2. Prepare PFBT (Pentafluorobenzenethiol) solution with a concentration of 10 mM in ethanol.
3. Immerse the device sheet into the prepared PFBT solution for 60 min.
4. Remove the device sheet from the solution and thereafter, rinse and clean with ethanol and Di-H₂O to form the mono Ag-PFBT layer.

The measured PFBT modified silver features an improvement of the work function from 4.7 eV to 5.35 eV. Specifically, the change in the work function decreases the injection barrier to the TIPS-Pentacene from silver electrode. The work function of PFBT modified Ag now matches the HOMO level of TIPS-Pentacene (5.28 eV). Ultimately, this energy level alignment leads to efficient hole injection into the TIPS-Pentacene and thus enhances the carrier mobility.

The second innovation involves a proposed printing step for the semiconductor. Specifically, the use of the slot die coater [42] is proposed instead of the reported inkjet [20, 24, 25], spin coating [22], drop casting [28], etc. to print the TIPS-Pentacene semiconductor layer. It is interesting to note that although slot die coating is commonly used for printing the active materials for solar cells, to the author's knowledge, this is the first application for printed transistors [42]. The advantage of using a slot die coater is that the crystal formation of the TIPS-Pentacene is well controlled so that the crystal grain boundaries are decreased, thereby facilitating the flow of electrons between the source and drain of the transistor.

Figure 3-2 depicts the slot die coating process where the ink is feed to the coating head via a pump/pressure system, and thereafter deposited to the substrate at the certain speed and direction.

Figure 3-2   Slot die coating process

The developed slot die coating procedure for deposition of TIPS-Pentacene as *p*-type semiconductor is summarized as follows:

1. Pre-clean and PFBT modify the silver electrodes for appropriate compatibility with TIPS-Pentacene.
2. Heat the holder of the slot die coater to 70 °C.
3. Prepare the TIPS-Pentacene solution with a concentration of 3 wt% in 80% toluene 20% anisole solvent blend.
4. Place the PET foil onto the holder of the slot die coater.
5. Set the gap of substrate-coater to 150 μm and speed of 0.3 mm/s.
6. Initiate coating and place the PET foil onto a hot plate at 90 °C for 30 min.

With the aforesaid setting, the formation and orientation of TIPS-Pentacene crystal can be controlled and thus, high carrier mobility can be achieved.

Figure 3-3 depicts the semiconductor crystal orientation effect of the coating direction. In Figure 3-3 (a), the slot-die moves along the ordinate while in Figure 3-3 (b), the slot-die moves along the abscissa, and it is apparent that the TIPS-Pentacene crystal forms along the direction of coating. In both cases, the coating is relatively uniform; the specific uniformity is yet uncertain. The coating direction along the abscissa – across the channel in Figure 3-3 (b) – will yield a substantially higher mobility as the holes will cross less grain boundaries whilst transporting from source to drain. Specifically, on the basis of measurements, the mobility is $\sim 1.5 \text{ cm}^2/\text{Vs}$ for Figure 3-3 (b) while that for Figure 3-3 (a) only yields mobility $\sim 0.1 \text{ cm}^2/\text{Vs}$. The chosen coating direction is the ‘across channel’ – that of Figure 3-3 (b).

Figure 3-3   Crystal formation with coating direction of (a) Follow; and (b) Across channel

The aforesaid said first and second innovations collectively increase the carrier-mobility substantially. Specifically, the carrier-mobility is very significantly

increased from $\sim 0.03 \text{ cm}^2/\text{Vs}$ (reported screen printing methods [18]) to $\sim 1.5 \text{ cm}^2/\text{Vs}$ herein – to the best of the author’s knowledge, the highest carrier mobility of all Fully-Additive processes to-date, and comparable to the substantially more complex and expensive Subtractive-based processes. The other pertinent parameters of the p -type transistors based on the proposed Fully-Additive printing process includes: threshold voltage (V_{TH}) = 0 V, and I_{ON} / I_{OFF} ratio = 10^5 . This I_{ON} / I_{OFF} ratio is also amongst the highest of all printing processes reported to-date and is desirable for realizing robust digital circuits/systems [127, 131-133]. The typical input-output and output characteristics of the printed p -type transistor are depicted in Figure 3-4.

Figure 3-4 Transfer characteristics of proposed Fully-Additive printed transistors

In addition to transistors and to enable the realization of complete circuits/systems, it is imperative that passive elements (resistors, capacitors and inductors) can likewise be Fully-Additive printed, and all circuit elements interconnected by at least two layers of metal-interconnect. In the case of resistors, a blend of high (Dupont 5036 [123]) and low (Dupont 7082 [123]) resistivity materials is used here to obtain a reasonably large range of printed resistor resistivities. By means of this composition blending, the ensuing resistivities of the printed resistors range from $3.3 \text{ k}\Omega/\square$ to $800 \text{ k}\Omega/\square$. Although the layout of the resistors can be of any shape, typical IC layouts are adopted here, i.e. either serpentine or straight as depicted in Figure 3-1 (b) earlier.

In the case of capacitors, a large range of capacitances (whilst requiring small area) is likewise desirable. To obtain this, a multiple dielectric-layer structure is employed, similar to the double MIM-cap in silicon processes [57]. Figure 3-5 depicts the cross-section of a Fully-Additive triple dielectric-layer (four metal layers) printed capacitor. Depending on the number of dielectric layers, the capacitance ranges from 224 pF/cm^2 (for single dielectric-layer) to 1.1 nF/cm^2 (for quintuple dielectric-layer). The cost of realizing multiple-layer capacitors is the added printing steps, and as the process is Fully-Additive, this is easily printed. Figure 3-1 (b) earlier depicted the microphotograph of several single dielectric-layer capacitors.

Figure 3-5   Cross section view of a Fully-Additive triple dielectric-layer capacitor

In the case of Fully-Additive inductors, the inductance ranges from 1 μH to 8 μH with $Q = 2$ at 10 MHz. Although the Q factor is relatively low, the printed inductor is nevertheless sufficient for many applications, including the 13.56 MHz RFID.

Table 3-2 tabulates the benchmarking of the proposed Fully-Additive process against reported Fully-Additive processes. Of particular interest, the proposed process features not only the highest carrier-mobility (three times higher), but also to the author's knowledge, at this juncture, the only Fully-Additive process capable of realizing complete circuits/systems (embodying transistors, resistors, capacitors and inductors, and with two metal-interconnect layers) on flexible plastic films. In short, the proposed Fully-Additive process is arguably the most competitive Fully-Additive

process to-date, and comparable to substantially more complex and expensive Subtractive-based processes (see later).

Table 3-2   Comparison of Fully-Additive printing processes on flexible substrates

	Channel Length (μm)	Printing Technology	Mobility (cm^2/Vs)	V_{th} (V)	Circuits	V_{DD} (V)
This work	100	Screen printing and slot die coating	1.5	0	Diff amps and DAC	60
[20]	50	Inkjet printing	0.02	-1.2	Inverter	60
[21]	70	Flexography and gravure printing	p : 0.0039 n : 0.0029	p : -1.5 n : -1	Ring oscillator	100
[22]	140	Inkjet, drop casting and evaporation	p : 0.0078 n : 0.0037	N.A.	-	80
[23]	50	Aerosol jet printing	N.A	0.25	-	2
[24]	N.A.	Inkjet printing	0.0035	-3.85	-	30
[25]	20	Inkjet printing	0.053	-7.8	-	60
[26]	12.6	Gravure and flexography with PDMS stamp	0.1	-3.54	-	20
[27]	N.A.	Inkjet printing	0.45	10.5	-	60
[28]	5	Inkjet printing and spin coating	0.25	1.3	-	40

3.3 Fully-Additive Printed Analog Amplifiers

In this section, several printed analog circuits based on the proposed Fully-Additive process are demonstrated, including a proposed and two conventional differential amplifiers. These circuits are the first-ever demonstration of complete Fully-Additive circuits with relatively complex electronic functionality realized on flexible substrates.

At this juncture, the second chain in the supply chain of PE (Figure 1-1) is largely established. Given the substantial competency developed, the third chain of PE – circuits – printed on a flexible plastic film will now be investigated and processed.

In this section, the design challenges associated in PE will be first described – which is delineated earlier in Chapters 1 and 2. The description here is however different – specifically, from an electronics designer’s perspective. The design of a proposed differential amplifier is subsequently described and finally the realization and verification using the proposed Fully-Additive printing process is demonstrated; its performance will also be benchmarked.

Design challenges

At this juncture, to the best of the author's knowledge, the Fully-Additive printed analog circuit is virtually non-existent – the very few reported designs are based on Subtractive processes [111, 114]; see Chapter 2 for the major shortcomings of the Subtractive processes. The reasons that stymied such work are not unexpected – poor performance of OTFTs, such as low carrier mobility, poor registration, poor environmental stability, etc.

From the electronics designer's point of view, in this case for an amplifier design, these reasons translate to three major design challenges in PE:

Challenge 1: Poor performance of organic semiconductors

Practical electronic circuits, including PE, are expected to have a certain minimum lifespan or reliable operation over a minimum time. In this context, organic semiconductors (and other printed components) require high air-stability unless there are specialized packaging – such specialized packaging is largely incompatible with the general objectives of low cost and scalability.

In the search/review of available organic semiconductors, the only commercially available organic semiconductors that feature relative good air stability (significant mobility degradation is not observed after a few months) are *p*-type. At this juncture, the author is not cognizant of any *n*-type organic semiconductors that feature air stability – experiments on several depict significant mobility degradation

after a few hours. Further, their carrier mobilities are lower than that of *p*-type semiconductors (often 1-2 orders of magnitude). Consequently, only *p*-type semiconductors – hence *p*-type OTFTs – are considered and applied for circuit design.

In short, it is a challenge to design amplifiers with only *p*-type OTFTs.

Challenge 2: Variations of carrier mobility (μ)

Mobility variations affect many attributes of the OTFT, particularly the current therein. In the experiments and measurements, the variations of the carrier mobility are observed from batch-to-batch (inter-foil) is large ($\sim$ two times), while the variations within the same batch (intra-foil) are relatively small ($< 20\%$).

The challenge in amplifier design is hence the design such that its important parameters, e.g. gain and bandwidth, are tolerant to variations of carrier mobility.

Challenge 3: Variation of the threshold voltage (V_{TH})

There are several mechanisms that cause the variations of the threshold voltage of OTFTs, and these include the variations in the printing and the shift of the threshold under bias stress [134].

The challenge in amplifier design is hence the design such that its important parameters, e.g. gain and common-mode output voltage, are tolerant to variations of threshold voltage.

The general desirable attributes of an amplifier include high gain and high gain-bandwidth. In the context of PE, amplifier designs are challenging, due to the absence of n -type transistors, established gain-boosting methods such as cascade topologies used in silicon-based designs are inapplicable here. Several reported gain boosting methods [51, 135, 136] in PE employ zero- V_{GS} connected transistors (transistors in the cut-off region) as the active load. From a practical PE perspective, this practice is avoided here because of the ensuing high sensitivity of the amplifier parameters (including gain and output common-mode voltage, etc.) to process variations – a serious drawback. This is because the impedance of zero- V_{GS} connected transistor is very sensitive to process variations, largely due to poor matching.

Proposed Amplifier Design

The proposed amplifier design embodying design techniques that meets the three aforesaid challenges is delineated here as follows:

To Challenge 1, p -type OTFTs are applied as load transistors in a differential amplifier design. There are two types of load transistor configurations in amplifier design – diode-connected and zero- V_{GS} connected. Specifically, the gate of the load

p -OTFT can be respectively connected to the drain, resulting in a diode load with the load transistor biased in saturation region, or to the source, hence biased in cut-off region.

The diode-connected load provides for higher bandwidth and is less sensitive to threshold voltage shift over time whereas the zero- V_{GS} connected load yields higher input-output gain but is sensitive to leakage current variations. Furthermore, the diode-connected load structure suffers from low gain; design methodology should be implied to improve the open loop gain. In view of Challenges 2 and 3, the diode-connected load configuration is hence adopted in the proposed design.

To Challenge 2, in terms of p -type only amplifier designs, the variations of carrier mobility results only in bandwidth variation. The DC bias of the OTFTs in the amplifier is largely unaffected for the transistors operating at saturation region because the various DC bias points are a ratio; biasing in the linear region is inappropriate because the ensuing ratio(s) are less precise. Therefore, all transistors in the amplifier will be designed to operate in saturation region – this is also the usual practice in silicon-based amplifiers.

To Challenge 3, in the p -type OTFT amplifier design, the open loop gain can be designed by a ratio the geometry of the OTFT (W/L) – this is also the usual practice in silicon-based amplifiers for current mirrors. This design methodology offers the advantages of threshold voltage variation insensitivity. Furthermore, the common-mode output voltage level needs to be designed to be insensitive with threshold voltage shift under biasing stress. Negative feedback will be applied in the

proposed amplifier design to suppress the variations of the common-mode output voltage level.

The proposed differential amplifier embodies a novel feedback with both positive and negative paths to circumvent these challenges and drawbacks. The positive feedback path serves to significantly increase the gain whilst the negative feedback path reduces the output common-mode sensitivity of the amplifier. It is interesting to note that positive feedback is usually avoided in silicon-based amplifier designs due to the increased possibility of instability. However, positive feedback herein is appropriate due to the low (relative to silicon) carrier-mobility (hence low gain) where the possibility of instability is virtually negligible.

Figures 3-6 (a)-(c) respectively depict the schematic of the proposed single-stage, conventional single-stage and the conventional three-stage differential amplifiers. The microphotograph of the proposed and conventional single-stage differential amplifiers printed based on the proposed Fully-Additive process is depicted in Figures 3-6 (d) and (e) respectively, and the layout of the conventional three-stage amplifier is depicted in Figure 3-6 (f). From Figures 3-6 (a)-(f), it can be seen that the conventional single-stage amplifier is the hardware simplest and as expected, its ensuing printed area (2.75 cm x 3.5 cm) is the smallest. On the other hand, the hardware complexity (in terms of transistor count) and printed area of the proposed single-stage and the conventional three-stage amplifiers are approximately the same: 12 transistors on 3.25 cm x 4.25 cm and 13 transistors on 3.25 cm x 5 cm

for the proposed single-stage and conventional three-stage amplifiers respectively; their performance is however markedly different, see below.

Figure 3-6 (a) - (c) Schematic of the proposed and conventional differential amplifiers; (d) and (e) Microphotographs of the proposed and conventional amplifiers; (f) Layout of conventional three-stage amplifier; (g) and (h) Measured and Simulated input and output waveforms, and frequency responses; and (i) Simulated output common-mode voltage variations due to threshold voltage variations

On the basis of measurements and simulations on the printed proposed and conventional single-stage amplifiers and of simulations on the conventional three-stage amplifier, Figures 3-6 (g), (h) and (i) respectively depict their time-domain responses, frequency responses, and output common-mode variations due to threshold voltage (process) variations. As the simulations and measured plots in Figures 3-6 (g) and (h) agree well, the derived models (which will be delineated in Chapter 4) for Fully-Additive printed transistors are precise. The power dissipation of these amplifiers is 55mW, 20mW and 60mW for the proposed single-stage, conventional single-stage and the conventional three-stage differential amplifiers, respectively.

The proposed amplifier features two advantages over the conventional designs, particularly the exploitation of simultaneous feedback with both positive and negative paths therein. First, from Figures 3-6 (g) and (h), the gain of the proposed amplifier is ~ 27 dB, and is significantly higher than that of the conventional three-stage and single-stage amplifiers, whose gain is ~ 13 dB and ~ 7 dB respectively. With respect to the conventional three-stage amplifier, this significantly higher gain is obtained largely without compromising the gain-bandwidth and without incurring hardware or printed area penalty. The functionality of the transistors in the proposed design in Figure 3-6 (a) is as follows. Two differential pairs with diode-connected load configuration are employed, comprising M_7, M_1, M_4, M_6 forming one pair, and M_8, M_2, M_3 , and M_5 forming the second pair. M_7, M_8 are current biasing transistors, M_1, M_4, M_2, M_3 are input transistors, and M_5, M_6 are diode-connected load transistors of M_3 and M_4 , respectively. The output of each differential pair (source of M_5 and M_6) is fed back to the current biasing transistor (M_7 and M_8) of another pair through a voltage

level shifter (M_9 , M_{11} and M_{10} , M_{12} , respectively). The gain of the proposed amplifier A_V can be easily derived as:

$$A_V = \frac{g_{m1}}{g_{m5} - \frac{1}{2} g_{m8} \frac{g_{m1}}{g_{m5}}} \quad (3.1)$$

where g_{m1} , g_{m5} , and g_{m8} (S) are respectively the transconductance of M_1 , M_5 and M_8 .

Second, the application of negative feedback reduces the output common-mode voltage sensitivity of the amplifier to the process variations. For instance, when the output common-mode voltage (V_{out1} and V_{out2}) increases due to process variations (e.g. threshold voltage variations), the source voltage of M_9 and M_{10} (the gate voltage of M_7 and M_8) also increases, thereby reducing the current in M_7 and M_8 and consequently, reducing V_{out1} and V_{out2} . Conversely, when V_{out1} and V_{out2} reduce due to process variations, the negative feedback will pull up V_{out1} and V_{out2} . On the basis of simulations, Figure 3-6 (i) compares the output common-mode variations as a function of threshold voltage variations of the proposed and conventional signal-stage, and conventional three-stage amplifiers. It is apparent here that as a consequence of the embodiment of negative feedback, the output common-mode sensitivity to process variations of the proposed amplifier is significantly improved compared to the conventional amplifiers. As a case in point, for 5 V threshold voltage variation, the output common-mode variation for the proposed amplifier is a mere 0.3 V vis-à-

vis 5.6 V and 6.5 V respectively for the conventional single-stage and three-stage amplifiers, equivalent to a significantly reduced 5% thereof.

To put the attributes of the proposed amplifier design in perspective, Table 3-3 benchmarks the proposed amplifier (Fully-Additive process) against reported state-of-the-art differential amplifiers (all based on Subtractive processes) on flexible substrates; note that amplifiers based on Fully-Additive process are not included as to the best of the author's knowledge, they are hitherto unreported. It is apparent from this table that the proposed amplifier features the highest gain despite its realization based on the proposed simple low-cost Fully-Additive process. Further, the reported relatively high gain amplifiers [51, 135, 136] are based on zero- V_{GS} connected load, which as delineated earlier, are disadvantageous as they are very sensitive to process variations. Nevertheless, although the bandwidth of the proposed amplifier is somewhat modest due to the low-cost 'tee-shirt' printing equipment, the proposed amplifier remains highly competitive for PE.

Table 3-3   Benchmarking printed differential amplifiers on flexible substrates

		Printing Technology	Channel Length (μm)	Load Configuration	Gain (dB)	Band width (Hz)
This work	Fully-Additive Process	Screen printing and slot die coating	100	Diode connected	27	70
[135]	Subtractive Process	Photolithography and vacuum evaporation	10	Zero- V_{GS} connected	18.6	N.A.
[136]		Photolithography and vacuum evaporation	5	Diode connected	10	1400
[51]		Photolithography and vacuum evaporation	5	Bootstrapped zero V_{GS} -connected	18	600
[137]		Photolithography and vacuum evaporation	5	Zero- V_{GS} connected	23.5	7.5
[18]		Laser ablation and screen printing	20	Complementary configuration	22.4	1025

3.4 Conclusions

A printing process, embodying simple depositions-only processing steps, for realizing PE circuits/systems on flexible substrates has been proposed in this Chapter. Specifically, the process is Fully-Additive (vis-à-vis Subtractive-based processes embodying complex deposition-cum-etching steps) – green, on-demand and low-cost. This process is not only uniquely capable of printing the semiconductor of transistors

with high carrier-mobility ($\sim 1.5 \text{ cm}^2/\text{Vs}$, equivalent to three times higher than reported Fully-Additive processes, and comparable to Subtractive-based process), but unique amongst Fully-Additive process because of its capability to print passive elements (capacitors, resistors and inductors) and two metal-interconnect layers, hence complete circuits/systems on flexible substrates. By means of the proposed Fully-Additive process, several analog and mixed-signal circuits have been demonstrated, including proposed and conventional single-stage differential amplifiers and conventional three-stage differential amplifier. By means of a novel feedback with both positive and negative paths, the proposed amplifier has been shown to feature significantly higher gain and significantly lower susceptibility to process variations compared to conventional amplifiers realized using the same Fully-Additive process, and highly competitive to amplifiers realized using Subtractive processes.

Chapter 4   A Fully-Additive Printed Electronics Open-Platform, Transistor Model and Fundamental Circuit Designs

4.1 Introduction

A large portion of this chapter is extracted from journal paper in Organic Electronics [41].

In view of the present nascency of PE, irrespective of the printing process, it is interesting to note that an open-platform for the design of PE circuits and systems remains unreported. On view of the practice of the IC design community within the IC industry eco-system, this open-platform is imperative for the PE community, more particularly PE electronics designers, to facilitate their designs and simulations of PE circuits and systems.

Furthermore, at this juncture, despite several reported printed transistor models [138-144], an accurate model for printed transistors remains lacking where reported models have three major shortcomings. First, the effect of transistor channel length on the carrier mobility is not modeled – in reported models, the carrier mobility (μ) is assumed to be independent of channel length (L); in some designs, because the width of the transistor is extremely wide [145], a shorter L may be

required. However, this assumption is usually not the case when the transistors are printed using a Fully-Additive printing process, especially for small molecule-based semiconductors such as Pentacene, TIPS-Pentacene, etc.; see later. Second, reported models are usually inaccurate in the subthreshold region and/or cut-off region. Note that from the circuit design perspective, transistor characteristics in deep-subthreshold region and/or cut-off region are important especially in digital circuit designs [146] as they affect several key parameters including noise margin, leakage current, etc. Third, statistical data (such as process variations), matching accuracy and the effect of layout are unreported. Collectively, these are important as they largely determine the reliability, robustness, manufacturability and yield of PE circuits and systems.

In this chapter, the open-platform for PE targeted for the proposed Fully-Additive screen printing process, including a novel model for printed transistors, and their process variations (statistical data), is proposed. The proposed transistor model is based on the established AIM-SPICE level 15 model [147] but with three imperative augmentations to account for the effect of channel length on carrier mobility, for all operating regions – from the supra-threshold region to the cut-off region, and for the leakage current and parasitic capacitances. The proposed model is verified to be accurate (and useful) by benchmarking it against measurements on individual transistors and on the basis of a number of analog and digital circuits.

To augment the comprehensiveness of the proposed open-platform to facilitate practical design of PE circuits and systems, the effect of layout on matching accuracy of printed transistors is further investigated; the layout includes layout techniques

commonly adopted by the IC design community. By means of appropriate layout, it is shown that printed transistors can be accurately (in the context of PE) matched – a relatively low mismatch of $\sim 8\%$ can be achieved despite variations of $\sim 30\%$ between individual transistors.

On the basis of the proposed comprehensive platform, several fundamental analog and digital circuits are designed, printed and measured. These circuits encompass simple conventional circuits (including an amplifier, inverter and ring oscillator) and improved circuits (including the proposed high gain amplifier, inverter with level shifter and ring oscillator with level shifter). By means of simulations (including Monte Carlo simulations of these circuits (based on the open-platform herein)) and measurements on printed circuits, the performance of these circuits are benchmarked and their design implications are delineated. The benchmarking shows good agreement between simulations and measurements, thereby depicting the accuracy of the proposed printed transistor model and invaluable insights to PE circuits and systems designers.

This Chapter is organized in the following manner. In Section 4.2, the effect of channel length on carrier mobility is investigated and the novel transistor model for the Fully-Additive printing process is proposed. In Section 4.3, statistical measurement data are presented and an investigation into the effect of layout on transistor matching is discussed. In Section 4.4, several fundamental analog and digital circuits are designed and printed. The proposed transistor model is verified by comparing simulations based on the proposed model and measurements on printed

circuits. The performance of these circuits is discussed and compared, and the implications of printed circuits are delineated. Finally, conclusions are drawn in Section 4.5.

4.2 Printed Transistors Model

4.2.1 OTFT Modeling

In this section, the development of the model for the OTFTs printed from the developed process delineated in Chapter 3 is described and this model is based on an existing a-Si: H TFT (hydrogenated amorphous silicon based TFT) model.

At this juncture, the development of the OTFTs is nascent, and the behavior and physics for the devices are likewise nascent [142]. Lacking an accepted model, Shockley equations used in silicon and germanium are adopted for purposes of approximation in PE. Specifically, the Shockley model, as reviewed in Chapter 2, describes the drain current, I_{DS} (A), of the OTFT as a function of its drain/source voltage, V_{DS} (V), and the gate/source voltage, V_{GS} (V), for three regions of operation:

$$\text{OFF Region: } |V_{GS}| - |V_T| < 0 \quad I_{DS} = 0 \quad (4.1)$$

$$\text{Triode Region: } 0 < |V_{DS}| < |V_{GS}| - |V_T| \quad I_{DS} = \frac{W}{L} \mu C_i \left[(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \quad (4.2)$$

$$\text{Saturation Region: } 0 < |V_{GS}| - |V_T| < |V_{DS}| \quad I_{DS} = \frac{W}{2L} \mu C_i (V_{GS} - V_T)^2 \quad (4.3)$$

where μ (cm²/vs) is the carrier mobility,

C_i (F/m²) is the dielectric capacitance per area,

V_T (V) is the threshold voltage, and

W and L (m) are the channel width and length.

The approximation of the Shockley equations for the region above the threshold (triode and saturation) is relatively good (in terms of being accepted by the printed electronics community) as long as an ohmic characteristic exists in the source-semiconductor and drain-semiconductor contacts. The approximation in the sub-threshold region, on the other hand, is not good and no model has been accepted thus far – in part of this region, the circuit designs will only be for above threshold (and cut-off) regions.

In general, the Shockley equations are inadequate because certain defects in OTFTs (e.g. surface traps and gate-voltage-dependent mobility) that would need to be considered are not – these are usually ignored in silicon as these defects are largely

small or negligible. Interestingly, such defects in OTFTs are mostly similar to those of a-Si: H TFTs [148] and for the latter, they have been reported in the literature. Not unexpected, using existing models for a-Si: H TFTs to model these defects in OTFTs have been likewise reported [139].

The proposed transistor model is based on the established AIM-SPICE Level 15 model for hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) with augmentations to account for the effect of channel length on carrier mobility, for both supra-threshold and cut-off regions and for leakage current and parasitic capacitances. The AIM-SPICE Level 15 model is adopted because it is compatible with IC industry standard electronic design automation tools and because the defects of printed transistors (being similar to a-Si: H TFTs) can be sufficiently modelled.

Nevertheless, for the Fully-Additive printed transistors, the AIM-SPICE Level 15 model is inadequate for the following shortcomings. First, the effect of channel length (L) on carrier mobility (μ) of printed transistors is not modeled; note that unlike conventional silicon transistors and a-Si: H TFTs, the carrier mobility of printed transistors with small molecule semiconductor materials (such as pentacene and TIPS-pentacene) is channel length dependent. Although this is somewhat unexpected, this phenomenon can be easily explained from the channel formation of the printed transistors (see later). Second, the AIM-SPICE Level 15 model can only adequately model the operation of Fully-Additive printed transistors in the supra-threshold region but not in the linear (and sub-threshold) and cut-off regions. Third, the AIM-SPICE Level 15 model does not adequately model the leakage current and

the parasitic capacitances of the Fully-Additive printed transistors. This is largely because both the leakage current and the parasitic capacitances in a-Si: H TFTs are much lower.

In view of these three shortcomings, three augmentations are made to the conventional AIM-SPICE level 15 model and these will now be discussed in turn.

(a) The effect of channel length on carrier mobility

In printing processes where the semiconductors are based on small molecule materials (such as TIPS-Pentacene), the channel is formed by numerous small crystals instead of a single crystal or a film. In this case, the carrier mobility is largely limited by the number of crystals because the speed of the carrier traveling across the crystal boundaries is much slower than its speed in a single crystal. This explains the phenomenon of substantially reduced carrier mobility (1-3 orders of magnitude) of the printed transistor compare to the intrinsic single crystal carrier mobility. From a printing perspective, to improve the carrier mobility of printed transistors, it is imperative that semiconductor crystal in the channel is well oriented and the number of grain boundaries is less. In the proposed Fully-Additive printing process, this is achieved by means of slot die coating for the deposition of semiconductor (TIPS-Pentacene) and the formation of highly orientated semiconductor crystals between

electrodes of transistors is obtained. In this fashion, the number of grain boundaries is small when the channel length is short (in PE perspective).

On the basis of measurements on numerous printed transistors, μ is empirically derived and can be expressed as:

$$\mu = \frac{\theta + 5 \frac{L_{norm}}{L}}{\theta + 5 \frac{L}{L_{norm}}} \mu_{norm} \quad (4.4)$$

where L (μm) is the channel length,

μ_{norm} (cm^2/Vs) is the carrier mobility when channel length is L_{norm} (μm), and

L_{norm} (μm) is the nominal channel length which is 100 μm .

(b) Cut-off region coefficient

To model the transistor for all operating regions from cut-off to supra-threshold regions, a cut-off region coefficient is augmented to the reported AIM-SPICE Level 15 model. For the proposed Fully-Additive printing process, the cut-off region coefficient is empirically derived and can be expressed as:

$$C_{cutoff} = \frac{1 + \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{TH}} \right)^\omega}{1 + [1 + V_m - \varphi(V_{GS} + V_m + V_{TH})] \left(\frac{V_{GS} + V_{DS}}{V_{DS} + V_m + V_{TH}} \right)^\omega} \quad (4.5)$$

where V_{TH} (V) is the threshold voltage,

V_{DS} (V) is the voltage across the drain and source,

V_{GS} (V) is the voltage across the gate and source,

V_m (V) is the modulation voltage,

ϕ is the voltage modulation parameter, and

ω is the power law modulation parameter.

(c) Leakage current and parasitic capacitances

In Fully-Additive printed transistors depicted in Figure 3-1 (a), the gate capacitance is largely determined by the overlap between the gate electrode and drain/source electrodes and is largely independent of the operating region of the transistor. It is interesting to note the converse is true for the conventional silicon transistors. Specifically the gate capacitance thereof is largely due to the overlap between the gate electrode and the silicon substrate and is significantly affected by its operating region. In view of this, the parasitic capacitances of the Fully-Additive printed transistor can be easily modeled as ideal capacitors, C_{GS} and C_{GD} , as depicted in Figure 4-1 below.

The leakage current of the printed transistor is largely due to the leakage in the dielectric material, because of the finite impedance of the overlapping capacitor between gate electrode and drain/source electrodes. On the basis of measurements, the leakage current is found to be largely proportional to the voltage across the

electrodes. Hence the leakage current can be simply modeled as resistors across the gate and drain/source electrodes, R_{GS} and R_{GD} , also depicted in Figure 4-1 below.

Figure 4-1   Equivalent circuit of Fully-Additive printed transistors

On the basis of measurements, the parasitic elements (capacitors (F) and resistors (R)) can be empirically derived and modeled as follows:

$$C_{GS} = C_{GD} = C_{ox} \times W \times F \quad (4.6)$$

$$R_{GS} = R_{GD} = \frac{R_{ox}}{W \times (L + F)} \quad (4.7)$$

where F (m) is the electrode finger width, and

R_{ox} (Ω) is the gate-electrodes resistance.

Based on the AIM-SPICE Level 15 a-Si: H TFT model, two phenomena contribute to the drain current, I_{DS} , of printed OTFT. The first is the field effect current due to the accumulation of carriers, I_{ab} , and the second is the leakage current due to the intrinsic conductivity of the organic semiconductor, $I_{leakage}$, collectively expressed in eqn. (4.8). For completeness, note that the inversion behavior of carriers in a-Si: H TFT is not included in the proposed model because this effect is generally not observed in organic semiconductors.

$$I_{DS} = I_{ab} + I_{leakage} \quad (4.8)$$

The leakage current, $I_{leakage}$ (A), can be easily described as a linear resistor between the two electrodes (source and drain):

$$I_{leakage} = SIGMA0 \times V_{DS} \quad (4.9)$$

where $SIGMA0$ (S) is the minimum leakage current parameter.

On the other hand, the current due to carrier accumulation, I_{ab} , is a function of the charge carrier concentration, n_s . The carrier concentration, n_s , comprises two parts, the free carrier concentration, n_{sa} , and the carriers from deep traps, n_{sb} , and expressed in eqn. (4.10):

$$n_s = \frac{n_{sa} \times n_{sb}}{n_{sa} + n_{sb}} \quad (4.10)$$

The free carrier concentration, n_{sa} (m^{-3}), can be calculated by carrier equilibrium approach,

$$n_{sa} = \frac{\epsilon_0 \epsilon_r \times V_{gte}}{q \times t_{ox}} \times \left(\frac{V_{gte}}{VAA} \right)^{GAMMA} \quad (4.11)$$

where q (C) is the elementary charge,

VAA (V) is the characteristic voltage for field effect mobility,

$GAMMA$ is the power law mobility parameter,

t_{ox} (m) is the thickness of the dielectric layer,

ϵ_r is the relative dielectric constant of dielectric,

ϵ_0 (F/m) is the permittivity of free space, and

V_{gte} (V) is the effective gate voltage overdrive.

V_{gte} equals to V_{gt} for regions above threshold and is of an order higher than thermal voltage in the sub-threshold regime. The following expression is used to model this behavior:

$$V_{gte} = \frac{VMIN}{2} \times \left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1 \right)^2} \right] \quad (4.12)$$

where V_{MIN} (V) is the convergence parameter,

$DELTA$ is the transition width parameter, and

V_{gt} (V) is given by $V_{gt} = V_{GS} - V_{TH}$, V_{TH} is the threshold voltage.

The trap carrier concentration, n_{sb} (m^{-3}), is calculated by the same approach for a-Si: H TFTs, and expressed as:

$$n_{sb} = n_{s0} \times \left(\frac{t_m}{t_{ox}} \times \frac{V_{gfbe}}{V_0} \times \frac{\epsilon_r}{\epsilon_{rs}} \right)^{\frac{2V_0}{V_e}} \quad (4.13)$$

where ϵ_{rs} is the relative dielectric constant of substrate,

V_0 (V) is the characteristic voltage for deep states,

V_e (V) is effective thermal voltage in deep states,

t_m (m) is effective thickness of the substrate,

n_{s0} (m^{-3}) is the interface carrier concentration, and

V_{gfbe} (V) is the effective gate flat band voltage override.

V_{gfbe} equals to V_{gfb} above flat band and is of order of the thermal voltage in the sub-threshold regime. The following expression is used to model this type of behavior:

$$V_{gte} = \frac{VMIN}{2} \times \left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1 \right)^2} \right] \quad (4.14)$$

where V_{gfb} (V) is given by $V_{gfb} = V_{GS} - VFB$, and VFB is the flat band voltage.

The effective thermal voltage in deep states, V_e (V), is expressed as:

$$V_e = \frac{2V0 \times V_{th0}}{2V0 - V_{th0}} \quad (4.15)$$

where V_{th0} (V) is the thermal voltage in semiconductor, and

$V0$ (V) is the characteristic voltage for deep states.

The effective thickness of the substrate, t_m (m), is expressed as:

$$t_m = \sqrt{\frac{\epsilon_0 \epsilon_{rs}}{2q \times GMIN}} \quad (4.16)$$

The interface carrier concentration, n_{s0} (m^{-3}), is expressed as:

$$n_{s0} = N_c t_m \frac{V_e}{V0} \exp\left(-\frac{DEF0}{V_{th0}}\right) \quad (4.17)$$

where N_c is the carrier conducting band concentration given by $3.0 \times 10^{25} m^{-3}$, and

$DEF0$ (V) is the dark Fermi level position.

Thus, the conductivity of the channel, g_{chi} (S) can be get from the carrier concentration, n_s , and expressed as:

$$g_{chi} = qn_s\mu W / L \quad (4.18)$$

where μ (cm²/Vs) is the carrier mobility of the semiconductor,

W (m) is the channel width, and

L (m) is the channel length of the transistor.

By taking the resistance of the drain (RD) and source (RS) into account, the effective conductivity, g_{ch} (S), is expressed as:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)} \quad (4.19)$$

Hence, the current due to carrier accumulation, I_{ab} (A), can be expressed as:

$$I_{ab} = g_{ch} V_{dse} (1 + LAMDA \times V_{DS}) \quad (4.20)$$

where $LAMDA$ (V⁻¹) is the output conductance parameter, and

V_{dse} (V) is the effective drain-source voltage.

The effective drain-source voltage, V_{dse} (V), can be expressed as:

$$V_{dse} = \frac{V_{DS}}{\left[1 + (V_{DS} / V_{sate})^M\right]^{1/M}} \quad (4.21)$$

where V_{DS} (V) is the drain-source voltage,

M is the knee shape parameter, and

V_{sate} (V) is the asymptotic upper limit.

The asymptotic upper limit, V_{sate} (V), is selected for V_{dse} to eliminating the negative output conductance problem and:

$$V_{sate} = ALPHASAT \times V_{gte} \quad (4.22)$$

where $ALPHASAT$ is the saturation modulation parameter.

In the Fully-Additive printed OTFTs, the effective gate voltage (V_{gte}) is equals to V_{gt} , and the free carrier concentration n_{sa} is much smaller than the carriers from deep traps n_{sb} . On that basis, assuming $V_{gte} = V_{gt}$ and $n_s = \frac{n_{sa} \times n_{sb}}{n_{sa} + n_{sb}} = n_{sa}$, together with the three augmentations delineated earlier, the drain current, I_{DS} (A), in can be simplified and summarized in eqn. (4.23):

$$I_{DS} = \frac{\frac{W}{L} \times C_{ox} \times \mu \times (V_{GS} - V_{TH})^{1+GAMMA}}{(VAA)^{GAMMA} + K \times R \times (V_{GS} - V_{TH})^{1+GAMMA}} \times \frac{V_{DS} (1 + LAMDA \times V_{DS})}{\left[1 + (V_{DS} / V_{sate})^M\right]^{1/M}} C_{cutoff} \quad (4.23)$$

where W (m) is the channel width,

C_{ox} (F) is the gate dielectric capacitance,

V_{TH} (V) is the threshold voltage,

R (Ω) is the drain and source resistance,

VAA is characteristic voltage for field effect mobility,

$GAMMA$ is the power law mobility parameter,

$LAMDA$ (S) is the output conductance parameter,

$ALPHASAT$ is the saturation modulation parameter,

M is the knee shape parameter, and

$V_{sate} = ALPHASAT (V_{GS} - V_{TH})$ (V) is the saturation voltage.

4.2.2 Parameter extraction

Following the model (eqn. (4.23)) in the last section, the developed procedure to ascertain the parameters to eqn. (4.23) will be described.

The proposed OTFT model parameter extraction procedure is summarized below. Steps 1 – 3 are for operation in the linear region while Steps 4 – 6 are for the saturation region.

Step 1 Linear Region: Extraction of the threshold voltage, V_{TH} and the power law mobility parameter, $GAMMA$

When the OTFTs are operating in linear region with a small V_{DS} , eqn. (4.23) is approximated to:

$$I_{DS,lin} = \frac{K \times (V_{GS} - V_{TH})^{1+GAMMA} V_{DS}}{(VAA)^{GAMMA} + K \times R \times (V_{GS} - V_{TH})^{1+GAMMA}} \quad (4.24)$$

By neglecting the small drain and source resistance R , eqn. (4.24) can be simplified to:

$$I_{DS,lin} = \frac{K \times (V_{GS} - V_{TH})^{1+GAMMA} V_{DS}}{(VAA)^{GAMMA}} \quad (4.25)$$

The function $H(V_{GS})$ [141] is applied by the integration of eqn. (4.25), applicable in the linear region:

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x) dx}{I_{DS}(V_{DS})} \quad (4.26)$$

The function $H(V_{GS})$ after the integration and dividing by I_{DS} , yields:

$$H(V_{GS}) = \frac{1}{2 + GAMMA}(V_{GS} - V_{TH}) \quad (4.27)$$

Thus, V_{TH} can be obtained from the intercept, and $GAMMA$ can be obtained from the gradient of eqn. (4.27).

Step 2 Linear Region: Extraction of the characteristic voltage for field effect mobility, VAA

Eqn. (4.24) can be re-written as:

$$I_{DS,lin}^{\frac{1}{1+GAMMA}} = \frac{K \times V_{DS}^{\frac{1}{1+GAMMA}}}{(VAA)^{GAMMA}} (V_{GS} - V_{TH}) \quad (4.28)$$

For the gradient S_1 of $I_{DS,lin}^{\frac{1}{1+GAMMA}}$ vs. V_{GS} in eqn. (4.28), the value of VAA can be ascertained:

$$VAA = \left[\frac{KV_{DS}}{S_1^{1+GAMMA}} \right]^{\frac{1}{GAMMA}} \quad (4.29)$$

Step 3 Linear Region: Extraction of the drain and source resistance, R

R is obtained by substituting the values of VAA , $GAMMA$ and V_{TH} into eqn. (4.24).

Step 4 Saturation Region: Extraction of saturation modulation parameter,

ALPHASAT

For simplification, assuming $V_{GS} = V_{DS}$ (ensuring the OTFT operates in saturation region), and the drain current in eqn. (4.23) becomes:

$$I_{DS,sat} = \frac{K \times ALPHASAT}{(VAA)^{GAMMA}} \times (V_{GS} - V_{TH})^{2+GAMMA} (1 + LAMDA \times V_{DS}) \quad (4.30)$$

For the gradient S_2 of $I_{DS,sat}^{\frac{1}{2+GAMMA}}$ vs. V_{GS} in eqn. (4.30), the value of $ALPHASAT$ can be ascertained:

$$ALPHASAT = \frac{(VAA)^{GAMMA} S_2^{2+GAMMA}}{K} \quad (4.31)$$

Step 5 Saturation Region: Extraction of the output conductance parameter, LAMDA

$LAMDA$ is calculated from the gradient of $I_{DS,sat}$ vs. V_{DS} at fixed V_{GS} in eqn. (4.30).

Step 6 Saturation Region: Extraction of the knee shape parameter, M

By making the assumption that effect of R , $LAMDA$ and leakage current is negligible, M is approximated at saturation voltage V_{sate} (eqn. (4.22) to:

$$M = \log 2 / \log \left[\frac{K}{(VAA)^{GAMMA}} \frac{ALPHASAT (V_{GS} - VTH)^{2+GAMMA}}{I_{DSsat}(V_{sate})} \right] \quad (4.32)$$

With the six derived steps procedures delineated above, the major parameters in the proposed OTFT model, VTH , $GAMMA$, VAA , R , $ALPHASAT$, M , can be extracted. Default values are assigned for the rest of the model parameters (minor parameters) in the AIM-SPICE a-Si: H TFT level 15 model. Table 4-1 summarizes the nominal process parameters of the Fully-Additive printed transistors embodying the three augmentations to the established AIM-SPICE level 15 model.

Table 4-1 Process parameters of the Fully-Additive printed transistors

Parameter	Value	Parameter	Value
μ_{norm}	0.81 cm ² /Vs	KVT	-0.036 V/ °C
L_{norm}	100 μm	LAMDA	0.0008 V
ϕ	0.08	M	1.5474
θ	45	RD	9 × 10 ⁴ Ω
ω	60	RS	9 × 10 ⁴ Ω
ALPHASAT	0.6875	SIGMA0	1.97 × 10 ⁻¹⁶ S
CGDO	0	TNOM	27 °C
CGSO	0	TOX	2 × 10 ⁻⁵ m
DEF0	0.6 eV	V0	0.12 V
DELTA	2	VAA	10 ⁹ V
EL	0.35 eV	VDSL	12 V
EMU	0.06 eV	VFB	-92.6 V
EPS	4	VGSL	12 V
EPSI	34	VMIN	0.3 V
GAMMA	10 ⁻¹⁰	V _{TH}	-0.7 V
GMIN	10 ²³ m ⁻³ eV ⁻¹	C _o	223 pF/cm ²
IOL	3 × 10 ⁻¹⁴ A	R _{ox}	6 × 10 ⁶ Ωm ²
KASAT	0.006 °C ⁻¹	V _m	3 V

Using the aforesaid transistor model and the parameters in Table 4-1, Figure 4-2 compares the input-output and output characteristics of the Fully-Additive printed transistors obtained from the transistor model and that obtained experimentally. It can be seen that there is good agreement, thereby depicting the accuracy of the transistor model. The accuracy (and usefulness) of this developed model will be further verified in Section 4.4 by comparing the simulation results and the measurements on several fundamental PE circuits.

Figure 4-2 Model verification of transfer and output characteristics of proposed Fully-Additive printed transistors

4.3 Process Variations and Mismatch of Printed Transistors

In this section, process variations and the effect of layout on transistor mismatch will be discussed. As delineated earlier, these considerations are imperative for practical PE circuits, including manufacturability.

4.3.1 Process Variations

The electrical characteristics of 35 Fully-Additive printed transistors are measured and summarized in Figure 4-3. The mean carrier mobility is $0.837 \text{ cm}^2/\text{Vs}$ with a standard deviation of 30.7% from the mean value. The mean threshold voltage is 1.97 V with a standard deviation of 45.41% from the mean value.

Figure 4-3   Characteristics distribution of Fully-Additive printed OTFTs

It is interesting to note that the process variations of the Fully-Additive printed transistors is relatively low in the context of PE and the benchmarking of the variations of mobilities for different reported processes, as summarized in Table 4-2. This ‘low variation’ is important in view of the low cost, simplicity, etc. of the Fully-Additive processes compared to the expensive, considerably more complex, etc. of the subtractive processes; refer to Chapter 1 earlier.

Table 4-2   Benchmarking of the carrier mobility, range and standard deviation of reported printed *p*-type OTFTs

	Printing technology	Carrier mobility (cm ² /Vs)	Range (cm ² /Vs)	Standard deviation
This work	Screen printing and slot die coating	0.837	0.4-1.5	30.7%
[19]	Photolithography and vacuum evaporation	0.05	-	39%
[149]	Photolithography and solution coating	0.03	-	120%
[149]	Photolithography and air flow solution coating	0.1	-	20%
[150]	Photolithography and solution coating	0.13	-	40%
[151]	Gravure printing and ink-jet printing	0.06	0.015-0.06	-
[152]	Ink-jet-printing	0.06	0.01-0.06	-

For completeness, the measurements show that the transistors located at the edges of the coating direction tend to have higher carrier mobility. Specifically, the mean carrier mobility of printed transistors located at the edge of coating direction is 0.96 cm²/Vs, equivalent to ~ 15% higher than that located in the center. However, the process variations of printed transistors located at the edges are significantly higher. From a practical circuit design perspective, it is hence prudent to layout transistors requiring higher mobility to be placed at the edges. However, if a circuit design

requires transistors with reduced variations, the placement of dummy transistors at the edges is recommended – a practice practiced in some silicon-based designs.

Another practical means to reduce variations is to employ larger transistors, a similar practice in silicon-based circuit designs. Specifically, the standard deviation of the carrier mobility of the Fully-Additive printed transistors is 45.41% for transistors with small width (e.g. $W = 4,000 \mu\text{m}$) and 30.7% for transistors with large width (e.g. $W = 40,000 \mu\text{m}$).

4.3.2 Layout and Mismatch

In this section, transistor matching based on four well-established layout techniques are compared. These techniques include simple layout, interdigitation, common centroid and the 2D common centroid layouts. Figure 4-4 depicts the microphotographs and measured input-output characteristics (with variations $\Delta I/I$) of Fully-Additive printed transistors based on these layout techniques. The aspect ratio of these transistors is $W/L = 40000 \mu\text{m}/100 \mu\text{m}$. For sake of matching and to eliminate aforesaid effects of edge coating, dummy transistors are strategically placed accordingly. In the microphotograph, M_{1a} and M_{1b} respectively denote the first and second half of the first transistor M_1 ; M_{2a} and M_{2b} respectively denote the first and second half of the second transistor M_2 ; and M_0 denotes dummy transistors.

Figure 4-4 Microphotograph and measured input-output characteristics of (a) Simple layout; (b) Interdigitation; (c) Common centroid; and (d) The 2D common centroid layout

From Figure 4-4, the following observations are made:

- (i) Overall, the matching accuracy is relatively good in the context of PE transistors. Specifically, the mismatch between a transistor pair is a mere ~ 48 % for the simple layout (Figure 4-4 (a)), and in the best case, is marked improved by 5.5 times to ~ 8.71% for the 2D common centroid layout (Figure 4-4 (d)).
- (ii) Compared to simple layout, the interdigitation layout and common centroid layout improve the matching accuracy by ~ 2.2 times (21.6%) and ~ 2.8 times (17.05%), respectively – but the cost of increased area by 55% and 36% respectively. The area overhead is largely due to the interconnections.
- (iii) Further to (ii), for small transistors which are split into 3 or less sub-transistors, common centroid is recommended as common centroid results in better

matching accuracy with little increment in the area. In contrast, for large transistors which are split into three or more sub-transistors, interdigitation layout is recommended as the area increment and connection complexities are exacerbated with increased number of sub-transistors.

- (iv) Of these layout techniques, the 2D common centroid layout results in the best matching accuracy. Compared to simple layout, interdigitation and common centroid layout, the 2D common centroid layout improves the matching accuracy by 5.5 times, 2.5 times and 1.9 times respectively. Obviously, the drawback here is the increased area of 65%, 7% and 21% compared to simple layout, interdigitation and common centroid layout respectively.

4.4 Implications of Printed Transistor Characteristics on Analog and Digital Circuits

The implications of the process variations and employment of various transistor matching techniques will now be delineated by comparing the performance of several fundamental analog and digital circuits designed based on conventional design methods and that based on improved methods for PE. The performance of these circuits are benchmarked on the basis of hardware measurements on Fully-Additive printed circuits and on the basis of simulations (including Monte Carlo simulations) using the derived transistor model (including process variations) in Section 4.2 earlier. The comparisons between the measurement results and simulation results also serve as verification of the proposed open-platform for the Fully-Additive

printed transistors. These circuits include analog amplifiers (conventional and proposed), and digital inverters, and ring oscillators. These circuits will now be delineated in turn.

4.4.1 Fundamental Analog Circuits – Amplifiers

The conventional amplifiers and the proposed amplifier are depicted in Figure 3-6, and the details of these amplifiers have been delineated in detail in Chapter 3 [6].

To verify the proposed open-platform and to delineate the advantages of the proposed amplifier over the conventional amplifier, Figures 3-6 (g)-(h) respectively depict their time domain input-output waveforms and frequency responses obtained from simulations and from measurements. It is apparent herein that the simulation results agree well with the measurements, thereby verifying the accuracy of the proposed open-platform. It is also apparent that the gain of the proposed single-stage amplifier is significantly higher than the conventional single-stage amplifier whilst their gain-bandwidth product is comparable. For completeness, the simulation results for the conventional three-stage amplifier are also depicted. It is apparent that although the printed area and transistor count of the proposed single-stage and conventional three-stage amplifiers are similar, the proposed single-stage amplifier features significantly improved gain (~ 30 dB vis-à-vis ~ 13 dB) and gain-bandwidth product (~ 80 Hz vis-à-vis ~ 5 Hz).

To compare the sensitivity of the conventional single-stage and proposed single-stage amplifiers on process variations and to further verify the proposed open-platform, 500 Monte Carlo simulations on several key parameters of said two amplifiers are performed. These parameters include the gain, gain-bandwidth product, common-mode voltage variation and offset voltage, and are depicted in Figure 4-5. For completeness, the measurements of the printed amplifiers are indicated in the histograms.

Figure 4-5 Monte Carlo Simulations: (a) Gain; (b) Gain-bandwidth product; (c) Common-mode voltage variation; and (d) DC offset. Measurements are denoted by 'x' and 'o' for the conventional single-stage and proposed single-stage amplifiers

On the basis of the histograms in Figure 4-5, the following observations are made:

- (i) From Figures 4-5 (a), (b) and (d), the respective measured gain, gain-bandwidth product and DC offset of the printed designs are relatively close to the average of the 500 Monte Carlo simulations.
- (ii) From Figure 4-5 (a), and as expected, the gain of the proposed single-stage amplifier is significantly higher than the conventional single-stage design –

this is due to the positive feedback path embodied in the proposed amplifier. Specifically, the mean value of the gain and standard deviation for conventional and proposed single-stage amplifiers are 7.26 dB and 11.2%, and 34.1 dB and 25.5%, respectively.

- (iii) From Figure 4-5 (b), and as expected, the gain-bandwidth product of the two amplifiers is comparable. Specifically, the mean value of the conventional and proposed single-stage amplifiers is 85 Hz and 84 Hz. Interestingly, the spread of the gain-bandwidth product of the conventional single-stage amplifier is wider – its standard deviation is 9.5% vis-à-vis 2.7% for the proposed single-stage amplifier.
- (iv) The output common-mode voltage variation of the proposed single-stage amplifier is significantly smaller than that of the conventional single-stage amplifier. From a practical circuit perspective, this is an important advantage.
- (v) The DC offset and the spread of the DC offset of the two amplifiers are largely comparable, despite the gain of the proposed single-stage amplifier being significantly higher (see item (ii)).

4.4.2 Fundamental Digital Circuits – Inverters and Ring oscillators

Consider now the implications of the printed transistor characteristics on fundamental digital circuits, represented by inverters and ring oscillators based on the conventional design and a simple improved design embodying a level shifter. As the matching between the transistors in typical digital designs are less of a consideration

than in typical analog designs, the investigation herein is now largely limited to the two critical parameters, input-output characteristics and to the noise margins. These two critical parameters are investigated, measured and compared against simulations.

Figures 4-6 (a)-(d) depict the schematic and microphotograph of the conventional inverter and the inverter with level shifter. ZeroVgs connected load configuration inverter is chosen because of the high gain and associated high voltage swing. Their input-output characteristics obtained from simulations and from measurements are depicted in Figures 4-6 (e)-(f). The supply voltage and the bias voltage are respectively $V_{DD} = 60$ V and $V_{bias} = 90$ V. It is apparent that for both designs, the simulation results agree well with measurements, thereby verifying the proposed open-platform. Furthermore, a comparison of the noise margin of the two inverters shows, as expected, that the inverter with level shifter features significantly improved noise margin. Specifically, the noise margin of the conventional inverter and inverter with level shifter is respectively 0.8 V and 19.9 V. From a circuit perspective, the improved noise margin yields improved robustness of digital circuits, and it is an imperative consideration in digital designs [146], see later. Nevertheless, the penalty is the $\sim 100\%$ increased printed circuit area and $\sim 40\%$ reduced speed.

Figure 4-6 (a) and (b) Schematics of the conventional inverter and the inverter with level shifter; (c) and (d) Their microphotographs; (e) and (f) Input-output characteristics and corresponding noise margin (▨)

500 Monte Carlo simulations to ascertain the noise margin of the two different inverters are performed and benchmarked as depicted in Figure 4-7. It is apparent that the measured noise margin of both inverters is very close to the respective mean values obtained from Monte Carlo simulations, hence verifying the open-platform. It is also apparent, as expected, that the noise margin of the inverter with level shifter is improved significantly over the conventional inverter. Specifically, the noise margin of the conventional inverter is noise margin high (NMH) =1.4 V with a standard deviation of 104.3% and noise margin low (NML) =50.5 V with a standard deviation of 11.4%. In comparison, the noise margin of the inverter with level shifter is improved to NMH = 27.6 V with a standard deviation of 11.2% and NML = 24.2 V with a standard deviation of 19.2%. From a circuit perspective, the positive noise margins ensure proper operation of the inverter and negative values result in a failure of the operation and signal propagation – improved noise margins consequently result in improved circuit reliability.

Figure 4-7 Monte Carlo simulations: (a) Noise margin high; and (b) Noise margin low. Measurements are denoted by ‘x’ and ‘o’ for inverter and inverter with level shifter

To illustrate its effect on reliability and speed, the simple conventional ring oscillator and ring oscillator with level shifter are designed, printed and measured. Their schematics, microphotographs and Monte Carlo simulations on oscillating frequency are depicted in Figure 4-8. Similar to the case of inverters, the supply voltage and the bias voltage are respectively $V_{DD} = 60$ V and $V_{bias} = 90$ V. Note that on the basis of Monte Carlo simulations, the failure rate of the simple conventional ring oscillator and the ring oscillator with level shifter is $\sim 53\%$ and 0% , respectively. Put simply, because of the significantly improved noise margin of the inverter with level shifter, it is significantly more robust than the simple ring oscillator. However, as mentioned earlier, the penalty is $\sim 40\%$ lower oscillating frequency and the printed area doubled.

Figure 4-8 (a)-(d) Schematic and microphotograph of the simple ring oscillator and ring oscillator with level shifter; and (e) Oscillating frequency of simple ring oscillator and ring oscillator with level shifter. Measurements are denoted by 'x' and 'o' for the simple ring oscillator and ring oscillator with level shifter

4.5 Conclusions

An open-platform embodying an accurate yet simple model for Fully-Additive screen printed transistors has been proposed. The open-platform is comprehensive, embodying the effect of channel length on carrier mobility, leakage current and parasitic capacitances and is valid for all operating regions of the transistor. The open-platform further embodied statistical data and the matching accuracy of printed transistors based on various layout techniques. On the basis of the open-platform, several fundamental analog and digital circuits have been designed, realized and verified.

Chapter 5   Conclusions and Recommendations

5.1   Conclusions

In this Ph.D. research program, various aspects of the PE second (printing (processing/equipment platforms)) and third (circuits) supply chains have been investigated. Broadly, these aspects included the development of a novel Fully-Additive printing method that is fully congruous to the frequently-touted attributes of PE, the first-ever development of comprehensive open-platform for PE (more specifically for the proposed Fully-Additive screen printing process) to facilitate the design and realization of PE analog and digital circuits, and the design and realization of PE analog and digital circuits and systems on flexible substrates. These work in this research program is arguably of high impact to PE literature – this is the first ever demonstration of circuits of note based on a Fully-Additive process (rivaling Subtractive processes without shortcomings thereof) and the first ever development of a comprehensive open-platform to facilitate the design of circuits and systems. Put differently, the work herein is an important step for the realization of ‘intelligent’ PE circuits and systems on flexible substrates, whose attributes include the frequently-touted attributes of PE – ‘green’, on-demand, scalable, flexible and inexpensive.

In Chapter 2, OTFT principles, materials and printing methods (for both ‘Subtractive’ and ‘Additive’) have been reviewed. Different structures of OTFT were reviewed in terms of performance (charge carrier mobility, threshold voltage, etc.) and process-ability. Of the structures reviewed, the BGBC structure was deemed to be the most appropriate due to its compatibility to Additive (low cost) printing methods and process stability.

A comprehensive review of materials, including organic semiconductors, has been provided. On the basis of the review, it was ascertained that the small molecule *p*-type organic semiconductors (such as TIPS-Pentacene) offer the most advantages in terms of charge carrier mobility, print-ability and ambient stability. Also on the basis of the review, the Additive printing process, specifically, screen printing process, was selected for its compatibility for printing on flexible substrates – it is ‘green’, on-demand, scalable, flexible, and inexpensive. Nevertheless, there are major challenges in this process, including low carrier mobility and the absence of any reported realized circuits and systems of note.

In Chapter 3, a printing process, embodying simple depositions-only processing steps, for realizing PE circuits/systems on flexible substrates has been proposed. Specifically, the process is Fully-Additive (vis-à-vis Subtractive-based processes embodying complex deposition-cum-etching steps) – green, on-demand and low-cost. This process is not only uniquely capable of printing the semiconductor of transistors with high carrier-mobility ($\sim 1.5 \text{ cm}^2/\text{Vs}$, equivalent to three times higher than reported Fully-Additive processes, and comparable to

Subtractive-based process), but unique amongst Fully-Additive process because of its capability to print passive elements (capacitors, resistors and inductors) and two metal-interconnect layers, hence complete circuits/systems on flexible substrates. By means of the proposed Fully-Additive process, several analog and mixed-signal circuits have been demonstrated, including proposed and conventional single-stage differential amplifiers and conventional three-stage differential amplifier. By means of a novel feedback with both positive and negative paths, the proposed amplifier has been shown to feature significantly higher gain and significantly lower susceptibility to process variations compared to conventional amplifiers realized using the same Fully-Additive process, and highly competitive to amplifiers realized using Subtractive processes.

In Chapter 4, an open-platform embodying an accurate yet simple model for Fully-Additive screen printed transistors has been proposed. The open-platform is comprehensive, embodying the effect of channel length on carrier mobility, leakage current and parasitic capacitances and is valid for all operating regions of the transistor. The open-platform further embodied statistical data and the matching accuracy of printed transistors based on various layout techniques. On the basis of the open-platform, several fundamental analog and digital circuits have been designed and realized. The simulated results and measurements on realized PE circuits agreed well, depicting the efficacy of the open-platform.

5.2 Recommendations for Future Work

On the basis of the literature review and work completed in this research program, the following further work is recommended:

- (i) Pertaining to the second PE supply chain: Investigations into the printing structures to achieve low variation, area effective OTFT circuits.

Despite the simplicity of the proposed Fully-Additive screen printing process, and the large minimum feature of $\sim 100\ \mu\text{m}$, the charge carrier mobility is relatively high. However, because of the large minimum feature, the area of the printed devices and the ensuing form-factor of the PE are relative large. To reduce said form-factor, it would be interesting to print the OTFTs on both sides of the plastic foil and/or on top of the printed devices (stacked 3D structure). Undoubtedly, although the challenges of the printing process are increased, the advantages are probably worthwhile.

- (ii) Pertaining to the second PE supply chain: Investigations to reduce the operation voltage of printed OTFTs.

The present operating voltage of the Fully-Additive printed OTFT is $\sim 60\ \text{V}$ – although this ‘high voltage’ is consistent with reported Fully-Additive printed OTFTs elsewhere, this ‘high voltage’ is incompatible with commercially

available low-voltage (3-6 V) power suppliers. In Chapter 2, the literature review showed that the threshold voltage of OTFT is strongly affected by the intrinsic characteristics and thickness of the dielectric and semiconductor. It would be interesting to investigate the employment of other dielectric materials and their associated printing to reduce the thickness of the dielectric, thereby possibly reducing the operating voltage of printed OTFTs.

- (iii) Pertaining to the second PE supply chain: Investigations to improve the operating frequency of printed OTFTs.

The present operating frequency of the Fully-Additive printed OTFTs is lower than that of subtractive printed OTFTs. To improve the operating frequency of the printed OTFTs, it would be interesting to investigate the patterning of the gate electrodes to reduce the parasitic capacitance, and to investigate other printing techniques, thereby possibly improving the operating frequency of printed OTFTs.

- (iv) Pertaining to the second PE supply chain: Investigations into the characterizations of the printed OTFTs.

In this research program, the fundamental issues in the proposed Fully-Additive process such as carrier mobility and process variations have been investigated. However, several other issues of the printed OTFTs are yet to be

characterized. It would be interesting to fully characterize the behavior of the printed OTFTs. Specifically, it would be interesting to investigate the impact of the ambient conditions (i.e. temperature, humidity, etc.) on printed OTFTs, the influence of time and the reliability of the printed OTFTs, the behavior of the printed OTFTs when the substrate is bent, and the distortions of various printed elements and ensuing circuits.

- (v) Pertaining to the third PE supply chain: Investigations into the completeness of the open-platform (Process Development Kit).

Despite the comprehensiveness and efficacy of the proposed PDK delineated in Chapter 4, the PDK remains rudimentary compared to mature PDKs for silicon. For completeness, it would be interesting to investigate the upper frequency and dimension limitations of printed OTFTs, and the effects of printed interconnects.

- (vi) Pertaining to the third PE supply chain: Investigations into the applications of PE.

As reviewed in Chapter 2 and observed in measurements of PE circuits in Chapter 3 and 4, the characteristic (carrier mobility and threshold voltage) of the printed OTFTs vary with the ambient condition, such as light, humidity, temperature, pressure, etc. It would be interesting to analyze the impact of the

ambient conditions on OTFTs, and to design and realize low cost sensors that can detect the change in the environment.

- (vii) Pertaining to the third PE supply chain: Design of ‘Intelligent’ PE circuit.

The proposed Fully-Additive screen printing process features the ability of realizing complex circuits/systems on flexible plastic films. It would be interesting to design and realize more complex ‘intelligent’ circuits, including full-fledged microcontroller. However, due to the large number of transistors, it is probably interesting to investigate the design of microcontrollers with a reduced transistor count – leading to a realistic form-factor realization.

Author's Publications

Journal Publications

- [1] J. Chang, X. Zhang, T. Ge and J. Zhou ^{*}
"Fully printed electronics on flexible substrates: High gain amplifiers and DAC"
Organic Electronics, vol. 15, pp. 701-710, 2014.

- [2] X. Zhang, T. Ge and J. Chang
"Fully-Additive Printed Electronics: Transistor model, process variation and fundamental circuit designs"
Organic Electronics, vol. 26, pp. 371-379, 2015.

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^{*} This publication was the second-most downloaded article in the ScienceDirect database (a database of > 2,500 journals) in the field of printed electronics for the last 90 days in June 2014. The number of downloads is ~ 1,800 downloads.

Patent and Technology Disclosures

- [1] J. Chang, T. Ge and X. Zhang
"Printed electronics"
Singapore Provisional Patent 201205357-5, 2012.

- [2] J. Chang, T. Ge and X. Zhang
"A Novel Fully-Printed operational amplifier on Flexible Substrates"
Technology Disclosure TD/090/12, 2012.

- [3] J. Chang, T. Ge, X. Zhang, J. Zhang, K. L. Chang, and X. Hou
"A Novel Fully-Printed Process for 2D and 3D Printed Electronics on Flexible Substrates"
Technology Disclosure TD/091/12, 2012.

- [4] J. Chang, X. Zhang, T. Ge, J. Zhou, and P. J. Ng
"Printed Electronics on Flexible Substrates: Fully-Additive Printing Process and the Process Development Kits"
Technology Disclosure TD /233/14, 2014.

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